

Compal Confidential

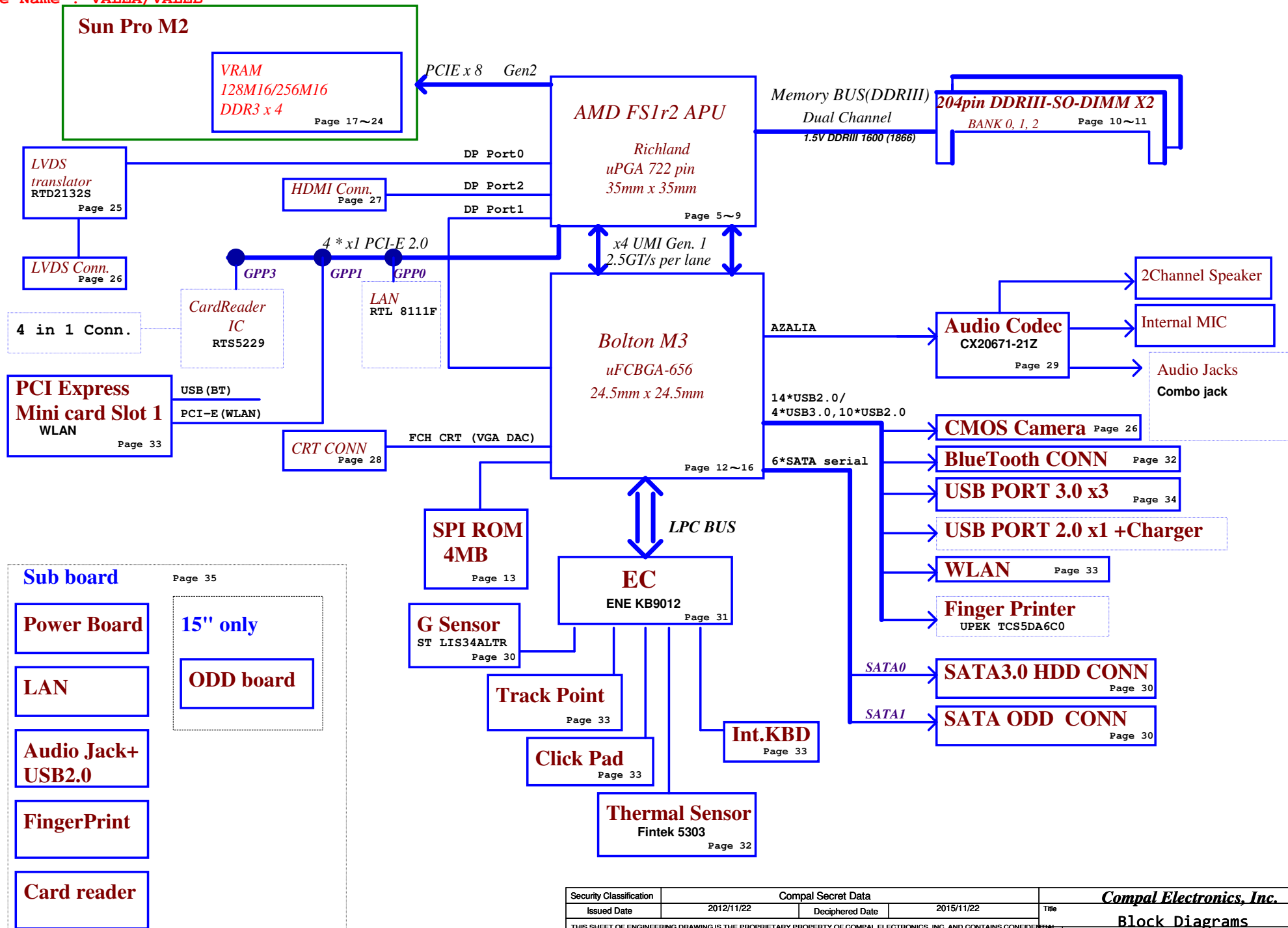
VALEA/VALEB Schematics Document

AMD APU Richland FS1r2 + FCH Bolton-M3 + GPU Sun Pro M2

2012-11-22

REV: 1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	Cover Page
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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS_WLAN	3.3V power rail for WLAN	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	F75303 (DDR,VRAM,CPUCORE)	1001-101xb	9AH
			SB-TSI	1001-100xb	98H
			Sun Pro M2	1000-0010b	82H
			LVDS translator		

FCH SMB0 (FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		
Security ROM		

Stencil Memo

FCH Hudson-M2/3 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List		
APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	Card Reader
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M2/3 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	USB2.0 Port
Port1	NC
Port2	NC
Port3	NC
Port4	NC
Port5	WLAN
Port6	CMOS
Port7	FP
Port8	BT
Port9	NC
Port10	USB 3.0
Port11	USB 3.0
Port12	USB 3.0
Port13	NC

BOM Structure

UMA@ : UMA only
DIS@ : DIS muxless

CMOS@ : USB camera

CONN@ : ME components
X76@, H1G@, S1G@ : VRAM

BOM option and stencil

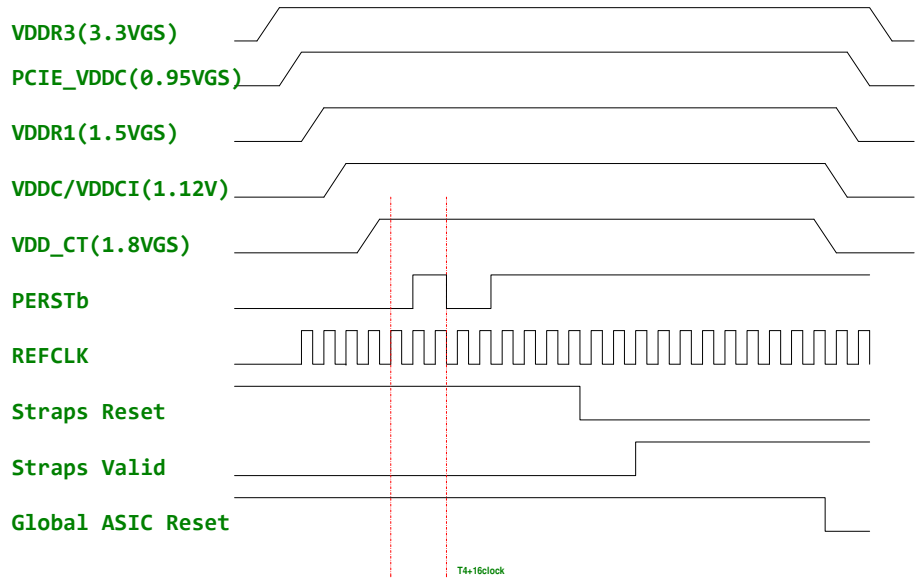
SDV:
CMOS@/DIS@ + X76@

PJ201,PJ401,PJ502,PJ503,PJ504,PJ601,PJ603,PJ604,
PJ701,PJ702,PJ703,PJ704,J1,J2301,J2401,J2402,J2403
PJ402,PJ403,PJ501,PJ602,PJ801,PJ802,PJ803,PJ805

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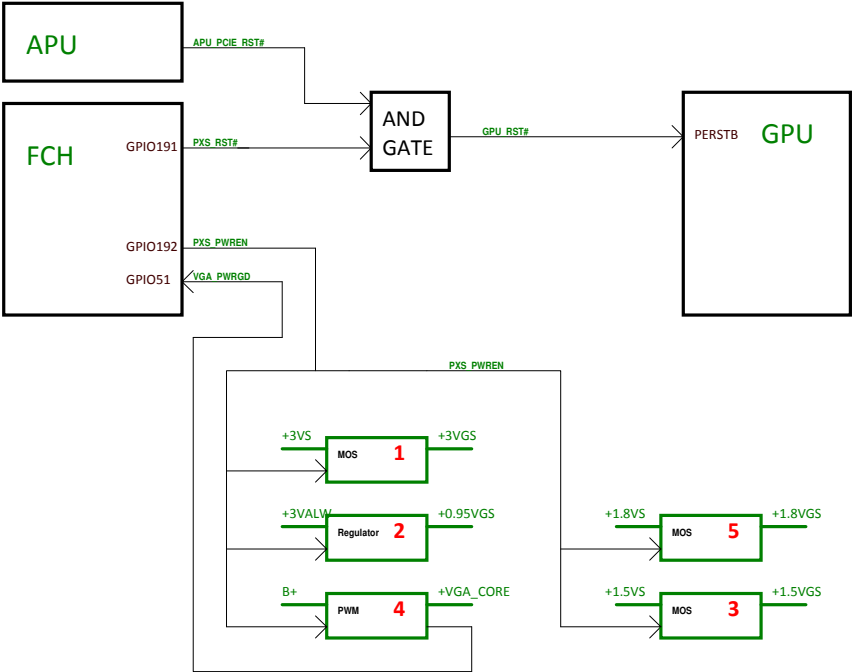
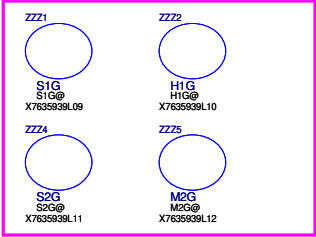
Power-Up/Down Sequence

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



SUN PRO VRAM STRAP

Vendor	PS_3[2]	PS_3[1]	PS_3[0]	R_pu	R_pd
H5TQ2G63DFR-11C SA00003Y070	0	0	0	R1430 NC	R1436 4.75K
K4W2G1646E-BC11 SA00005SH00	0	0	1	R1430 8.45K	R1436 2K
MT41J128M16JT-093G SA000067510 FBGA Code:D9PTD	0	1	0	R1430 4.53K	R1436 2K
K4W4G1646B-HC11 SA000068R00	0	1	1	R1430 6.98K	R1436 4.99K
MT41K256M16HA-107G SA000065D00 FBGA Code:D9PZD	1	0	0	R1430 4.53k	R1436 4.99K
MT41J128M16JT-107G SA00005SM30 FBGA Code:D9PRS	1	0	1	R1430 3.24k	R1436 5.62k
K4W2G1646E-BC1A SA000068U10	1	1	0	R1430 3.4k	R1436 10k
	1	1	1	R1430 4.75K	R1436 NC



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[17] PCIE_CRX_GTX_P[0..7]

[17] PCIE_CRX_GTX_N[0..7]

PCIE_CTX_GRX_P[0..7] [17]

PCIE_CTX_GRX_N[0..7] [17]

JCPU1A

PCI EXPRESS

PCIE_CRX_GTX_P0 AB8
PCIE_CRX_GTX_N0 AB7
PCIE_CRX_GTX_P1 AA9
PCIE_CRX_GTX_N1 AA8
PCIE_CRX_GTX_P2 AA5
PCIE_CRX_GTX_N2 AA6
PCIE_CRX_GTX_P3 Y8
PCIE_CRX_GTX_N3 Y7
PCIE_CRX_GTX_P4 W9
PCIE_CRX_GTX_N4 W8
PCIE_CRX_GTX_P5 W5
PCIE_CRX_GTX_N5 W6
PCIE_CRX_GTX_P6 V8
PCIE_CRX_GTX_N6 V7
PCIE_CRX_GTX_P7 U9
PCIE_CRX_GTX_N7 U8

P_GFX_RXP0
P_GFX_RXN0
P_GFX_RXP1
P_GFX_RXN1
P_GFX_RXP2
P_GFX_RXN2
P_GFX_RXP3
P_GFX_RXN3
P_GFX_RXP4
P_GFX_RXN4
P_GFX_RXP5
P_GFX_RXN5
P_GFX_RXP6
P_GFX_RXN6
P_GFX_RXP7
P_GFX_RXN7
P_GFX_RXP8
P_GFX_RXN8
P_GFX_RXP9
P_GFX_RXN9
P_GFX_RXP10
P_GFX_RXN10
P_GFX_RXP11
P_GFX_RXN11
P_GFX_RXP12
P_GFX_RXN12
P_GFX_RXP13
P_GFX_RXN13
P_GFX_RXP14
P_GFX_RXN14
P_GFX_RXP15
P_GFX_RXN15

P_GFX_TXP0
P_GFX_TXN0
P_GFX_TXP1
P_GFX_TXN1
P_GFX_TXP2
P_GFX_TXN2
P_GFX_TXP3
P_GFX_TXN3
P_GFX_TXP4
P_GFX_TXN4
P_GFX_TXP5
P_GFX_TXN5
P_GFX_TXP6
P_GFX_TXN6
P_GFX_TXP7
P_GFX_TXN7
P_GFX_TXP8
P_GFX_TXN8
P_GFX_TXP9
P_GFX_TXN9
P_GFX_TXP10
P_GFX_TXN10
P_GFX_TXP11
P_GFX_TXN11
P_GFX_TXP12
P_GFX_TXN12
P_GFX_TXP13
P_GFX_TXN13
P_GFX_TXP14
P_GFX_TXN14
P_GFX_TXP15
P_GFX_TXN15

AB2 PCIE_CTX_C_GRX_P0 C1 DIS@ 1
AB1 PCIE_CTX_C_GRX_N0 C2 DIS@ 1
AA3 PCIE_CTX_C_GRX_P1 C3 DIS@ 1
AA2 PCIE_CTX_C_GRX_N1 C4 DIS@ 1
Y5 PCIE_CTX_C_GRX_P2 C5 DIS@ 1
Y4 PCIE_CTX_C_GRX_N2 C6 DIS@ 1
Y2 PCIE_CTX_C_GRX_P3 C7 DIS@ 1
Y1 PCIE_CTX_C_GRX_N3 C8 DIS@ 1
W3 PCIE_CTX_C_GRX_P4 C9 DIS@ 1
W2 PCIE_CTX_C_GRX_N4 C10 DIS@ 1
V5 PCIE_CTX_C_GRX_P5 C11 DIS@ 1
V4 PCIE_CTX_C_GRX_N5 C12 DIS@ 1
V2 PCIE_CTX_C_GRX_P6 C13 DIS@ 1
V1 PCIE_CTX_C_GRX_N6 C14 DIS@ 1
U3 PCIE_CTX_C_GRX_P7 C15 DIS@ 1
U2 PCIE_CTX_C_GRX_N7 C16 DIS@ 1

2 .1U 0402 16V7K PCIE_CTX_GRX_P0
2 .1U 0402 16V7K PCIE_CTX_GRX_N0
2 .1U 0402 16V7K PCIE_CTX_GRX_P1
2 .1U 0402 16V7K PCIE_CTX_GRX_N1
2 .1U 0402 16V7K PCIE_CTX_GRX_P2
2 .1U 0402 16V7K PCIE_CTX_GRX_N2
2 .1U 0402 16V7K PCIE_CTX_GRX_P3
2 .1U 0402 16V7K PCIE_CTX_GRX_N3
2 .1U 0402 16V7K PCIE_CTX_GRX_P4
2 .1U 0402 16V7K PCIE_CTX_GRX_N4
2 .1U 0402 16V7K PCIE_CTX_GRX_P5
2 .1U 0402 16V7K PCIE_CTX_GRX_N5
2 .1U 0402 16V7K PCIE_CTX_GRX_P6
2 .1U 0402 16V7K PCIE_CTX_GRX_N6
2 .1U 0402 16V7K PCIE_CTX_GRX_P7
2 .1U 0402 16V7K PCIE_CTX_GRX_N7

SDV/FVT, NO.1

SDV/FVT, NO.1

LAN

WLAN

[35] PCIE_CRX_DTX_P0 AE5
[35] PCIE_CRX_DTX_N0 AE6
[33] PCIE_CRX_DTX_P1 AD7
[33] PCIE_CRX_DTX_N1 AC9
[35] PCIE_CRX_DTX_P3 AC5
[35] PCIE_CRX_DTX_N3 AC6

P_GPP_RXP0
P_GPP_RXN0
P_GPP_RXP1
P_GPP_RXN1
P_GPP_RXP2
P_GPP_RXN2
P_GPP_RXP3
P_GPP_RXN3

P_GPP_TXP0
P_GPP_TXN0
P_GPP_TXP1
P_GPP_TXN1
P_GPP_TXP2
P_GPP_TXN2
P_GPP_TXP3
P_GPP_TXN3

AD5 PCIE_CTX_C_DRX_P0 C33 1
AD4 PCIE_CTX_C_DRX_N0 C34 1
AD2 PCIE_CTX_C_DRX_P1 C123 1
AD1 PCIE_CTX_C_DRX_N1 C124 1
AC3
AC2
AB5 PCIE_CTX_C_DRX_P3 C35 1
AB4 PCIE_CTX_C_DRX_N3 C36 1

2 .1U 0402 16V7K PCIE_CTX_DRX_P0
2 .1U 0402 16V7K PCIE_CTX_DRX_N0
2 .1U 0402 16V7K PCIE_CTX_DRX_P1
2 .1U 0402 16V7K PCIE_CTX_DRX_N1
2 .1U 0402 16V7K PCIE_CTX_DRX_P3
2 .1U 0402 16V7K PCIE_CTX_DRX_N3

PCIE_CTX_DRX_P0 [35]
PCIE_CTX_DRX_N0 [35]
PCIE_CTX_DRX_P1 [33]
PCIE_CTX_DRX_N1 [33]
PCIE_CTX_DRX_P3 [35]
PCIE_CTX_DRX_N3 [35]

Card Reader

[12] UMI_RXP0 AG8
[12] UMI_RXN0 AG9
[12] UMI_RXP1 AG6
[12] UMI_RXN1 AG5
[12] UMI_RXP2 AF7
[12] UMI_RXN2 AF6
[12] UMI_RXP3 AE8
[12] UMI_RXN3 AE9

P_UMI_RXP0
P_UMI_RXN0
P_UMI_RXP1
P_UMI_RXN1
P_UMI_RXP2
P_UMI_RXN2
P_UMI_RXP3
P_UMI_RXN3

P_UMI_TXP0
P_UMI_TXN0
P_UMI_TXP1
P_UMI_TXN1
P_UMI_TXP2
P_UMI_TXN2
P_UMI_TXP3
P_UMI_TXN3

AG2 UMI_TXP0_C C37 1
AG3 UMI_TXN0_C C38 1
AF4 UMI_TXP1_C C39 1
AF5 UMI_TXN1_C C40 1
AF1 UMI_TXP2_C C41 1
AF2 UMI_TXN2_C C42 1
AE2 UMI_TXP3_C C43 1
AE3 UMI_TXN3_C C44 1

2 .1U 0402 16V7K UMI_TXP0 [12]
2 .1U 0402 16V7K UMI_TXN0 [12]
2 .1U 0402 16V7K UMI_TXP1 [12]
2 .1U 0402 16V7K UMI_TXN1 [12]
2 .1U 0402 16V7K UMI_TXP2 [12]
2 .1U 0402 16V7K UMI_TXN2 [12]
2 .1U 0402 16V7K UMI_TXP3 [12]
2 .1U 0402 16V7K UMI_TXN3 [12]

UMI_TXP0 [12]
UMI_TXN0 [12]
UMI_TXP1 [12]
UMI_TXN1 [12]
UMI_TXP2 [12]
UMI_TXN2 [12]
UMI_TXP3 [12]
UMI_TXN3 [12]

+1.2VS 1 R1 2 P_ZVDDP 196_0402_1% AG11

P_ZVDDP

CONN@

LOTES_ACA-ZIF-109-P12-A_FS1R2

Power Sequence of APU

+1.5V

+2.5VS

+1.5VS

+APU_CORE

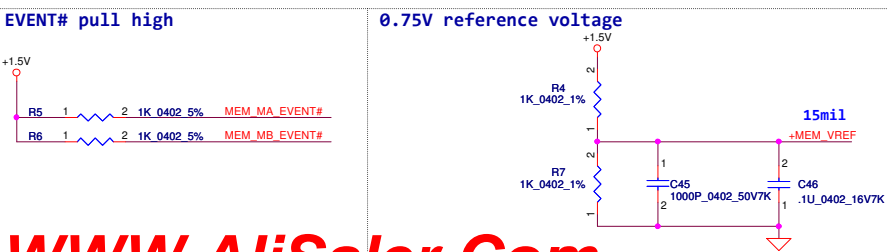
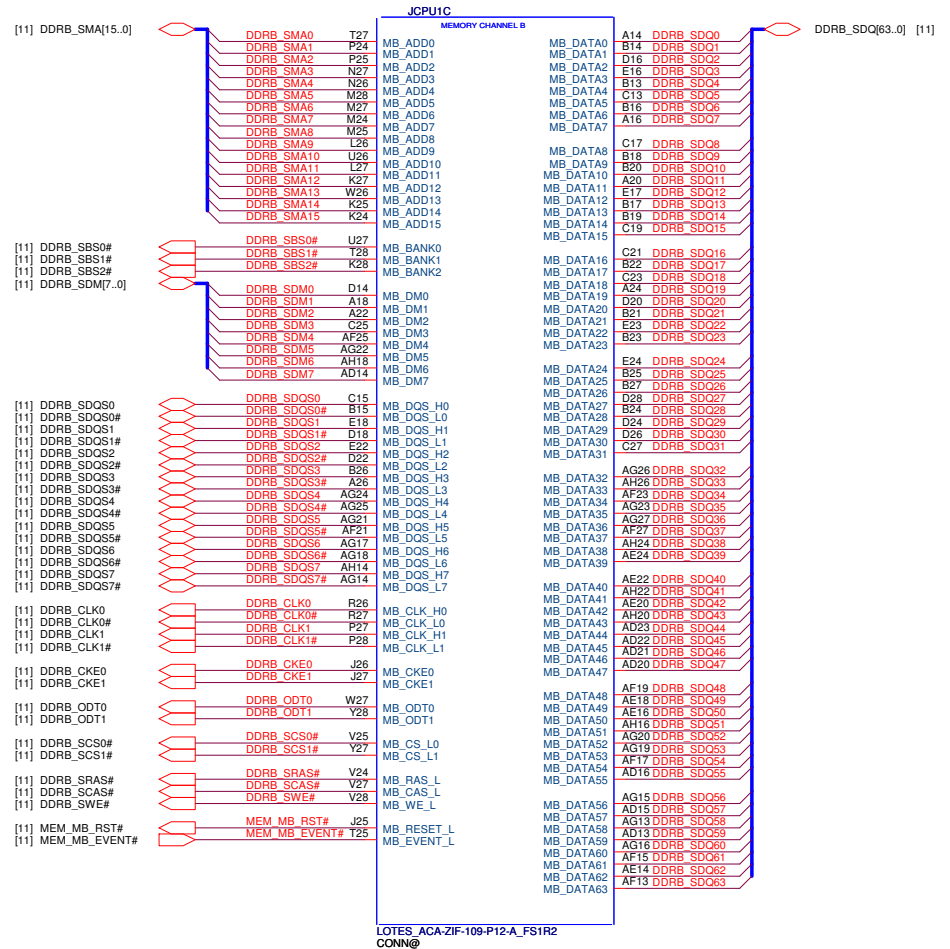
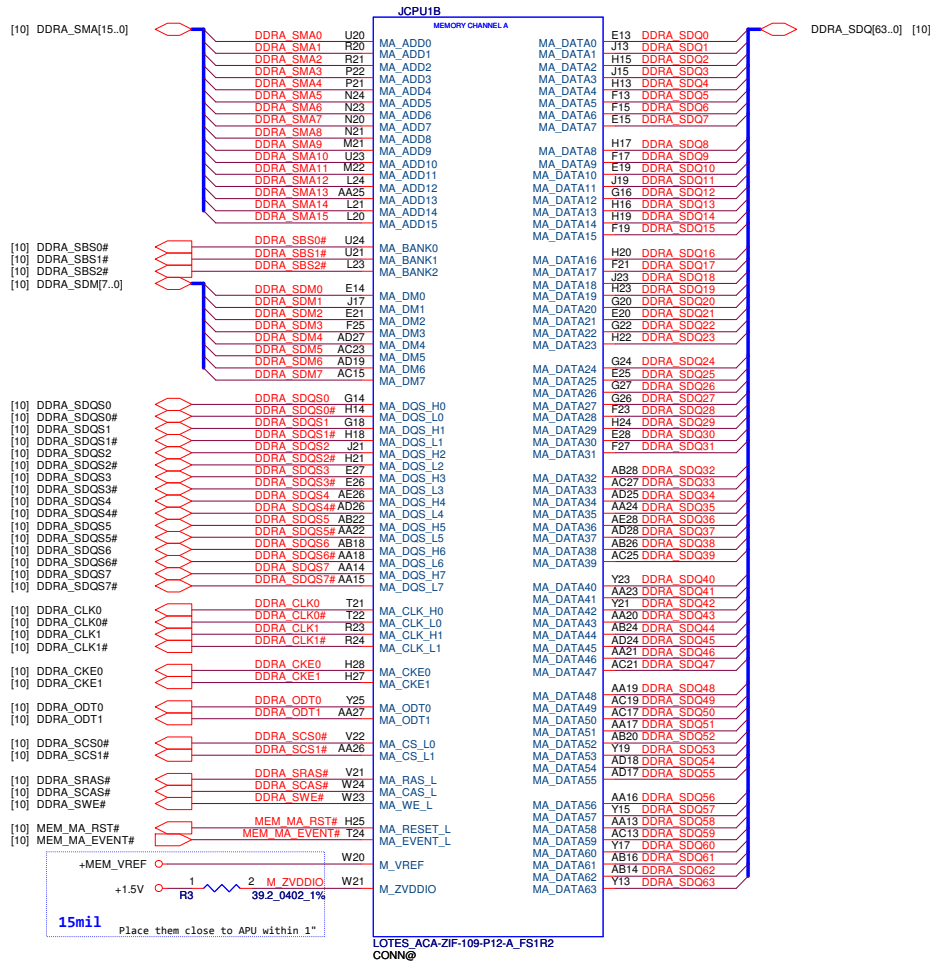
+APU_CORE_NB

+1.2VS

Group A

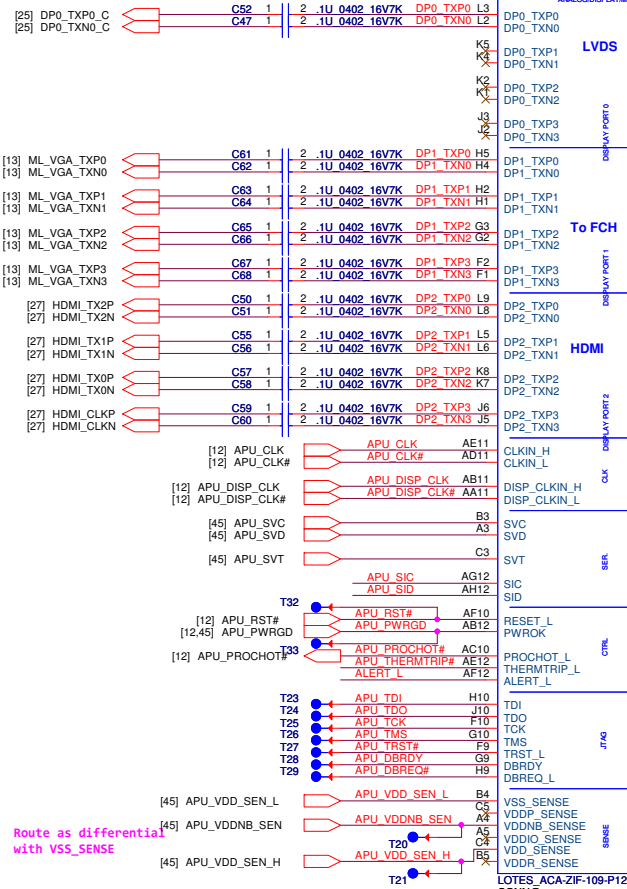
Group B

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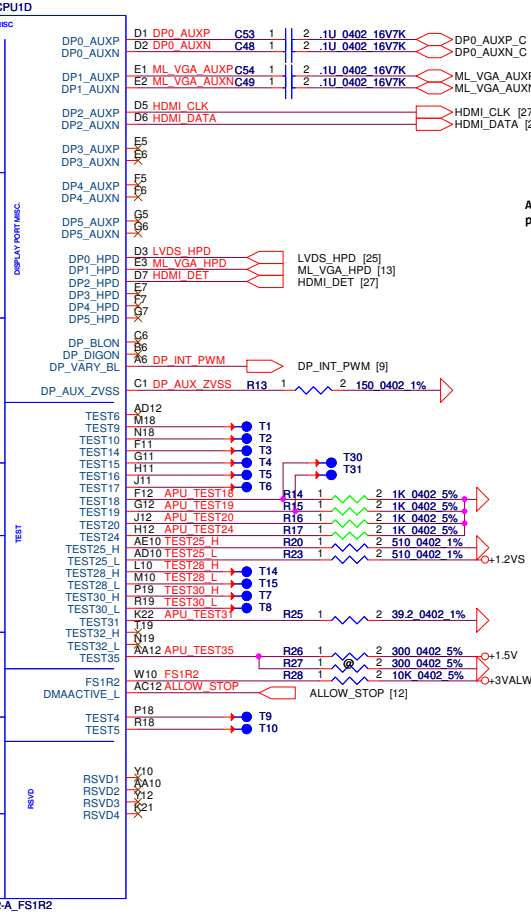
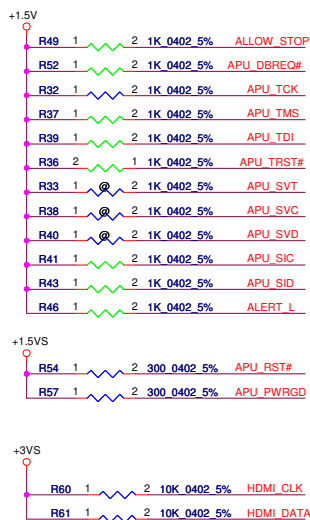


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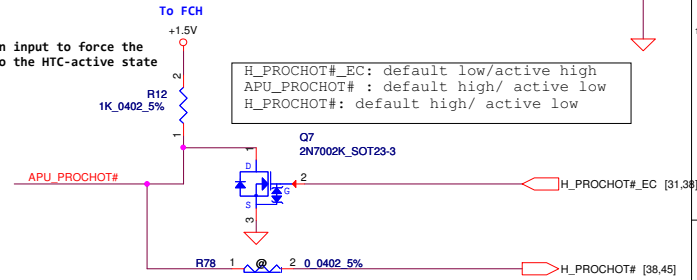
Place near APU



Route as differential with VSS_SENSE



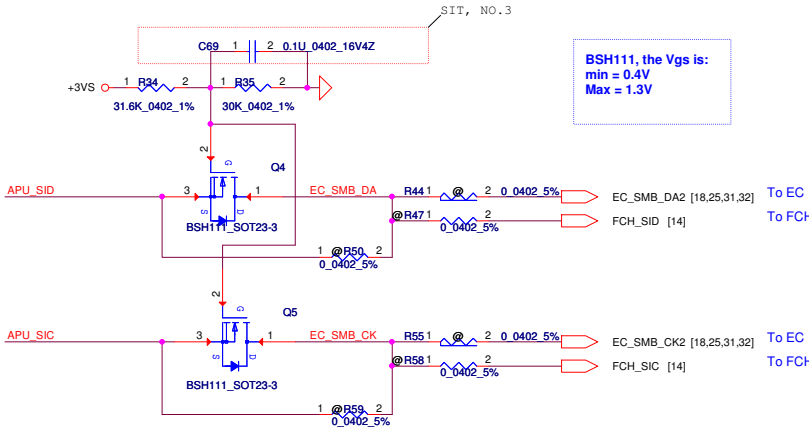
Asserted as an input to force the processor into the HTC-active state



THERMTRIP shutdown
Temperature: 125 degree

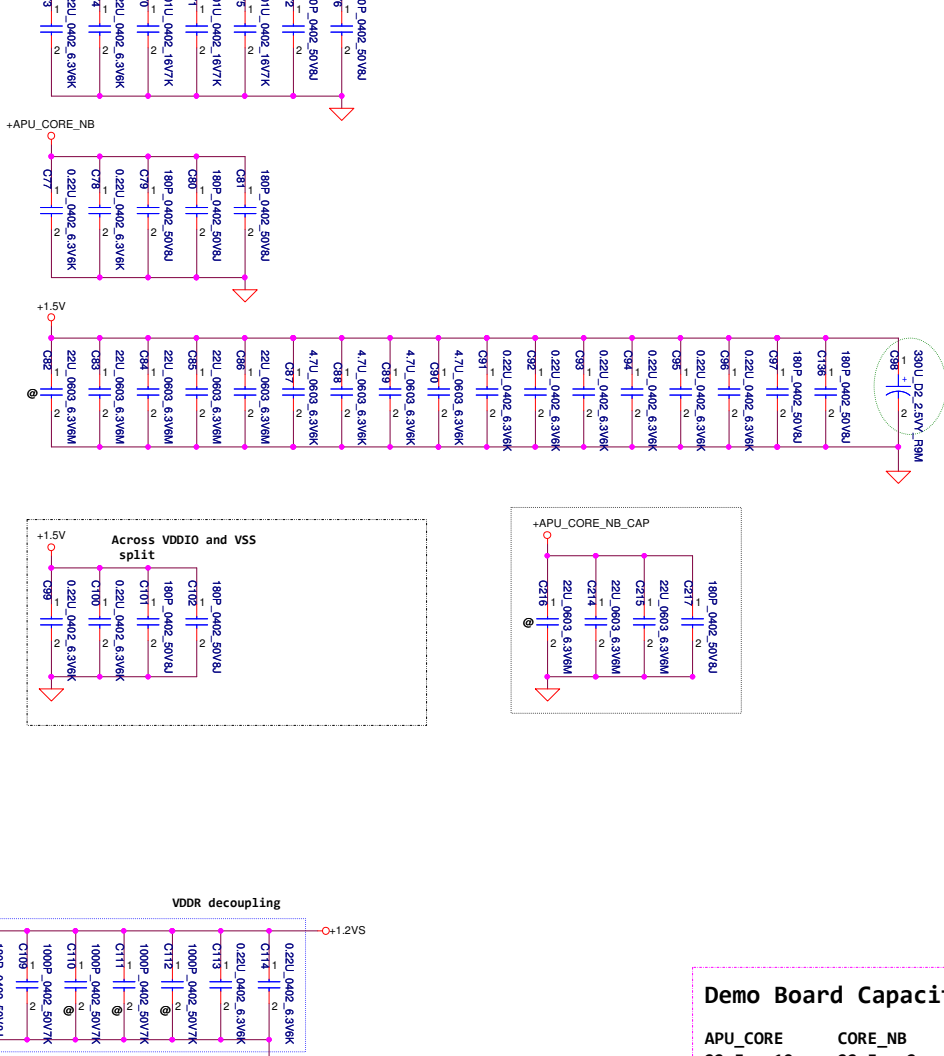
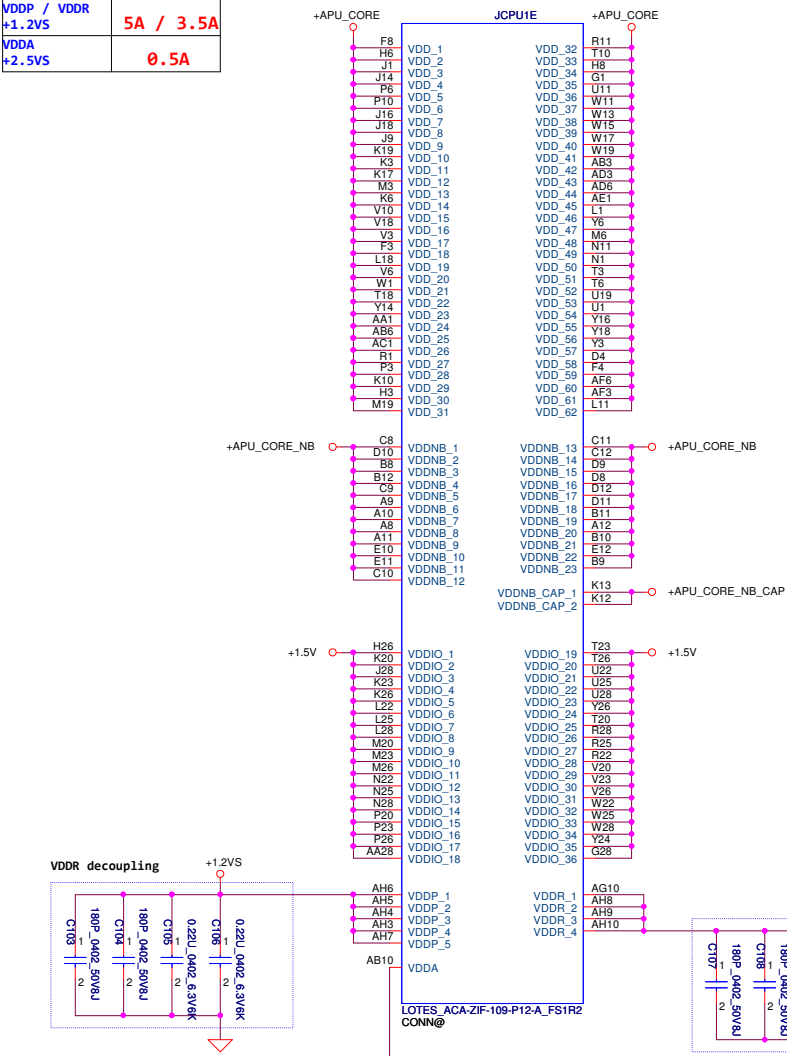
Indicates to the FCH that a thermal trip has occurred. Its assertion will cause the FCH to transition the system to S5 immediately

CPU TSI interface level shift



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Power Name	Consumption
VDD +APU_CORE	60A
VDDNB +APU_CORE_NB	44A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



JCPU1E			
J20	L4	VSS_1	VSS_73
R7	VSS_2	VSS_74	A21
W18	VSS_3	VSS_75	A23
A15	VSS_4	VSS_76	A25
AB17	VSS_5	VSS_77	A7
AC22	VSS_6	VSS_78	AA4
AF24	VSS_7	VSS_79	AB13
AH23	VSS_8	VSS_80	AB15
AH25	VSS_9	VSS_81	AB19
B7	VSS_10	VSS_82	AB21
C14	VSS_11	VSS_83	AB23
C16	VSS_12	VSS_84	AB25
C20	VSS_13	VSS_85	AB27
C22	VSS_14	VSS_86	AB9
C24	VSS_15	VSS_87	AC14
C26	VSS_16	VSS_88	AC15
C28	VSS_17	VSS_89	AC18
D13	VSS_18	VSS_90	AC20
D15	VSS_19	VSS_91	AC24
D17	VSS_20	VSS_92	AC28
D19	VSS_21	VSS_93	AC28
D23	VSS_22	VSS_94	AC4
D25	VSS_23	VSS_95	AC7
D27	VSS_24	VSS_96	AD9
E4	VSS_25	VSS_97	AE13
E9	VSS_26	VSS_98	AE15
F14	VSS_27	VSS_99	AE17
F16	VSS_28	VSS_100	AE7
F18	VSS_29	VSS_101	N10
F20	VSS_30	VSS_102	N4
F22	VSS_31	VSS_103	N7
F24	VSS_32	VSS_104	N10
F26	VSS_33	VSS_105	R4
F28	VSS_34	VSS_106	T11
G13	VSS_35	VSS_107	T9
G15	VSS_36	VSS_108	U10
G17	VSS_37	VSS_109	U18
G19	VSS_38	VSS_110	U7
G21	VSS_39	VSS_111	U7
G23	VSS_40	VSS_112	V11
G25	VSS_41	VSS_113	AE19
G4	VSS_42	VSS_114	AE23
G12	VSS_43	VSS_115	AE25
J24	VSS_44	VSS_116	AE27
J4	VSS_45	VSS_117	AE4
J7	VSS_46	VSS_118	AE7
K11	VSS_47	VSS_119	AF14
K14	VSS_48	VSS_120	AF16
K9	VSS_49	VSS_121	AF18
K11	VSS_50	VSS_122	AF20
L19	VSS_51	VSS_123	AF22
L7	VSS_52	VSS_124	AF26
M11	VSS_53	VSS_125	AF28
AF11	VSS_54	VSS_126	AF9
V19	VSS_55	VSS_127	AG4
V9	VSS_56	VSS_128	AG7
W16	VSS_57	VSS_129	AH15
W4	VSS_58	VSS_130	AH17
W7	VSS_59	VSS_131	AH19
Y11	VSS_60	VSS_132	AH21
Y20	VSS_61	VSS_133	AH23
Y22	VSS_62	VSS_134	P9
Y9	VSS_63	VSS_135	C18
A17	VSS_64	VSS_136	D21
A13	VSS_65	VSS_137	W14
K16	VSS_66	VSS_138	C7
F24	VSS_67	VSS_139	E8
G8	VSS_68	VSS_140	K18
H7	VSS_69	VSS_141	W12
J8	VSS_70	VSS_142	
	VSS_71	VSS_143	
	VSS_72	VSS_144	

VDD decoupling

VDDNB decoupling

VDDIO decoupling

VDDP/VDDR decoupling

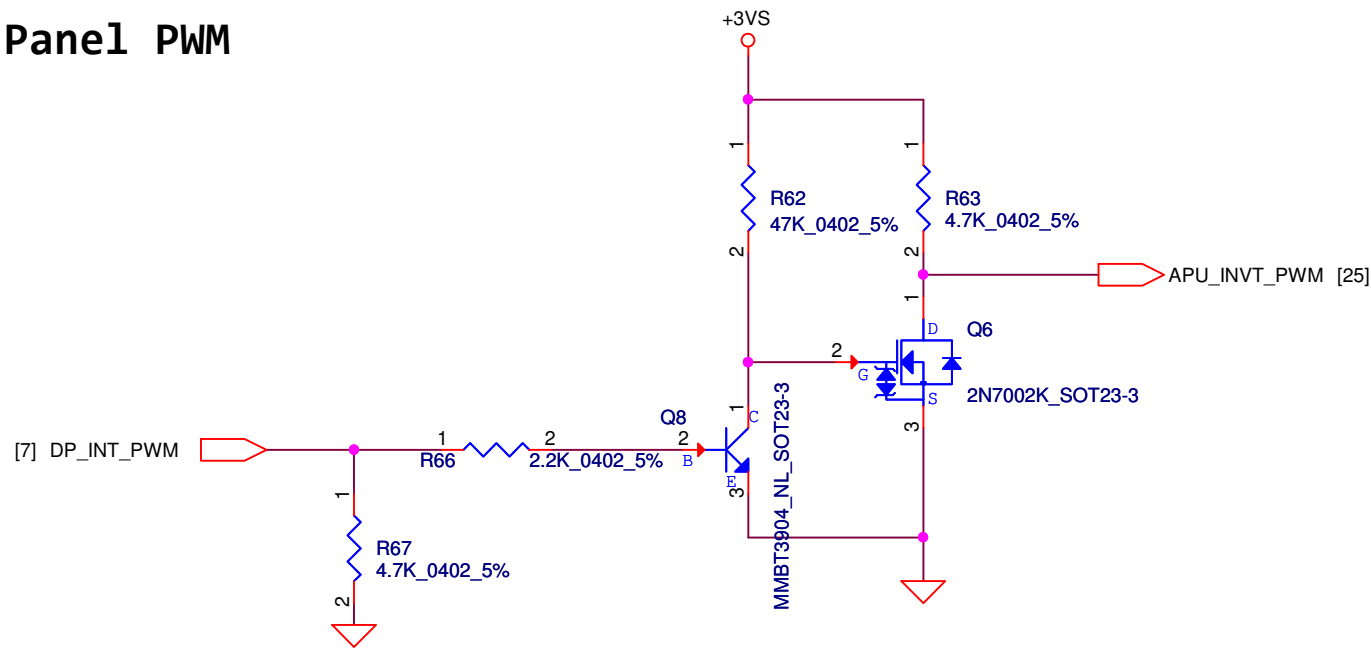
VDDA decoupling

Demo Board Capacitor

APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)

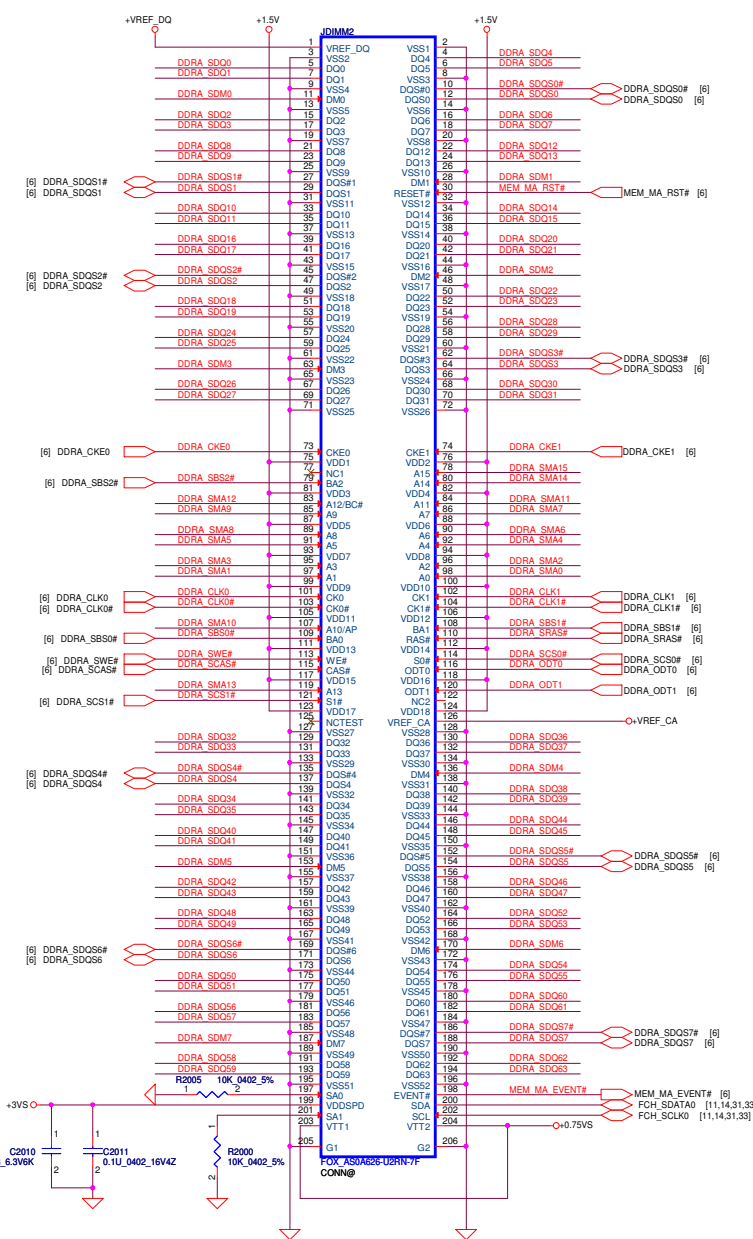
VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

Panel PWM

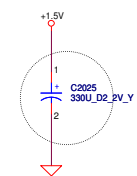
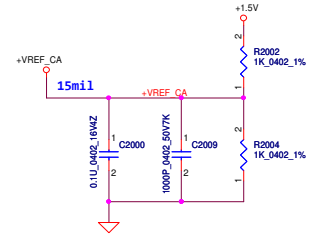
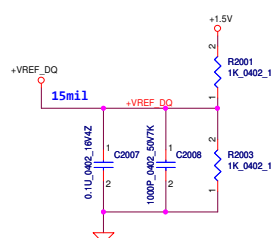
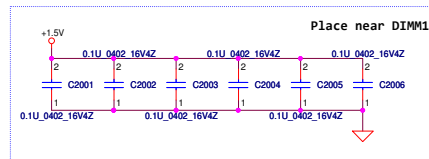
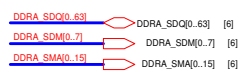


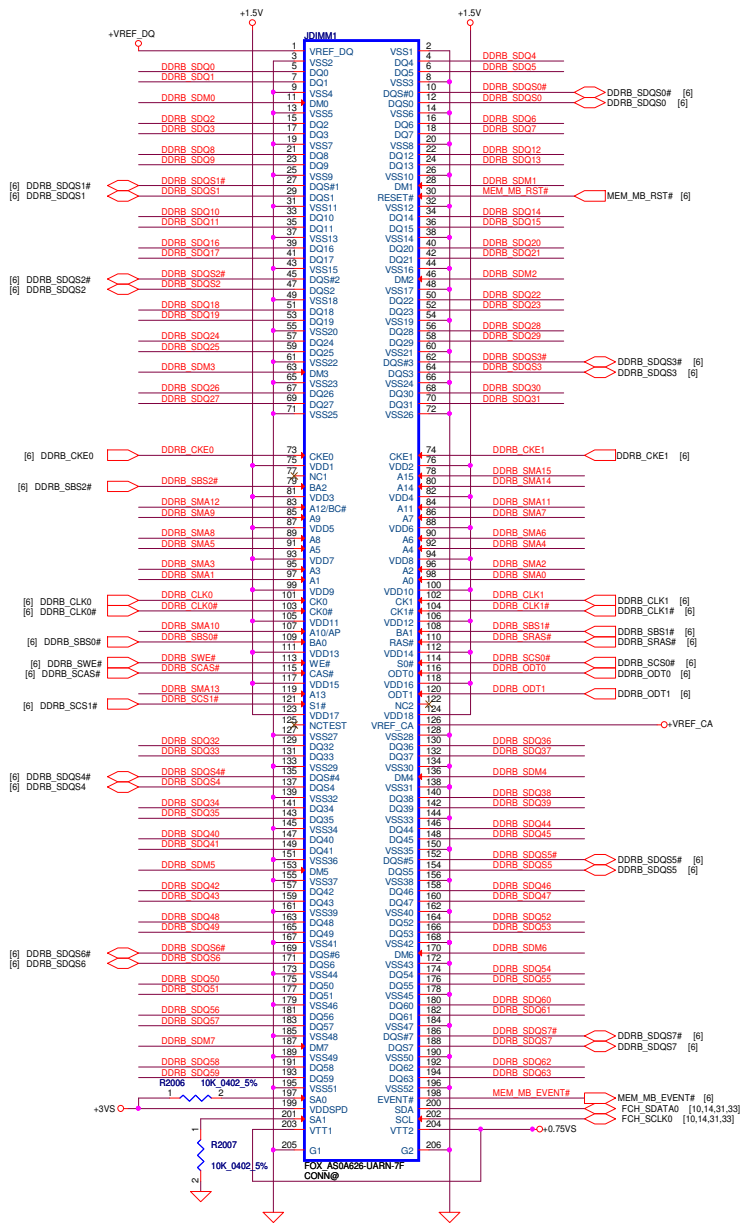
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	FS1r2 Signal Level Shifter
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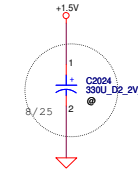
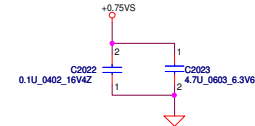
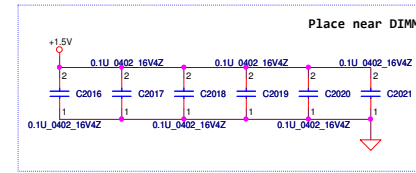
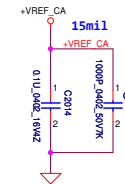
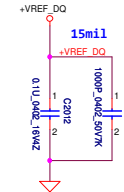


Reverse H:5.2mm



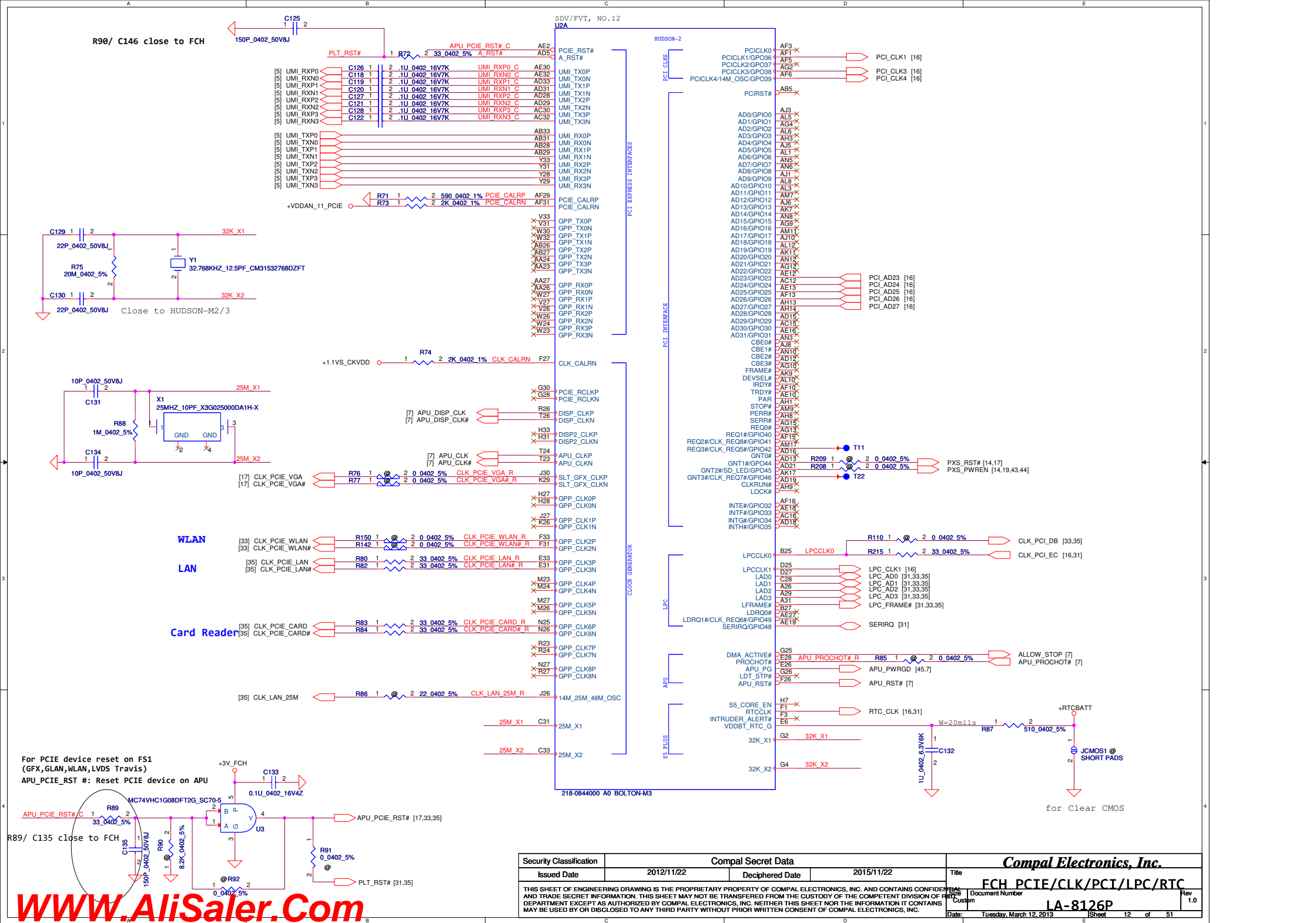


DDR8_SDQ[0..63] DDR8_SDQ[0..63] [6]
 DDR8_SDM[0..7] DDR8_SDM[0..7] [6]
 DDR8_SMA[0..15] DDR8_SMA[0..15] [6]

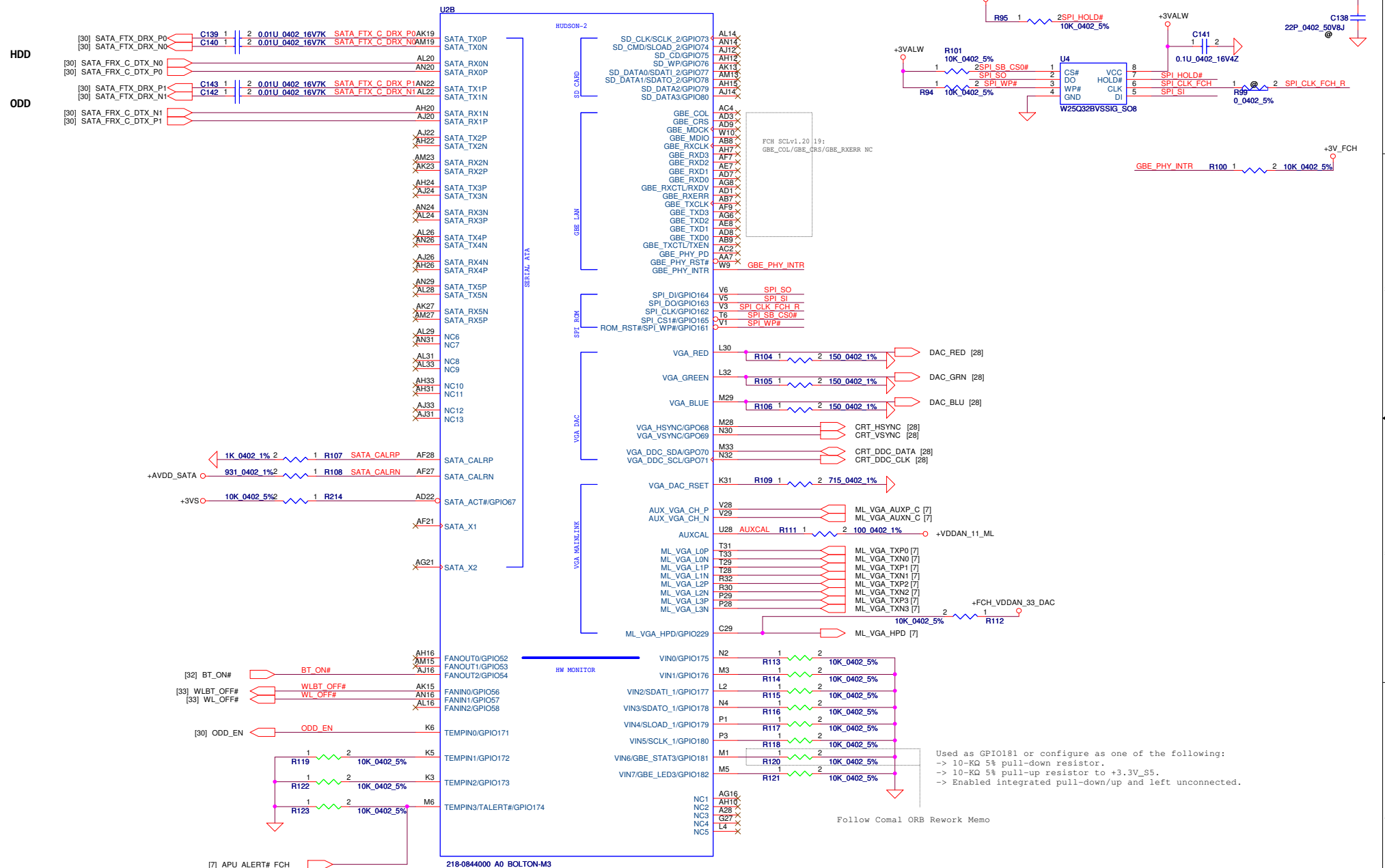


Reverse H:9.2mm

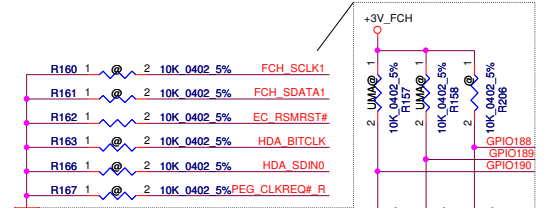
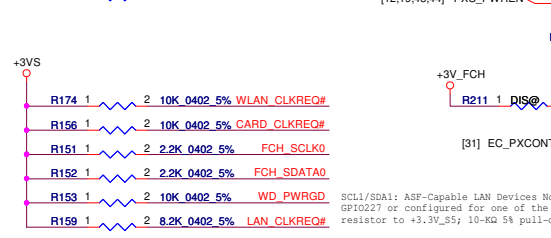
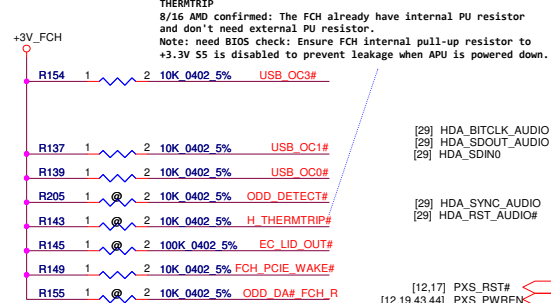
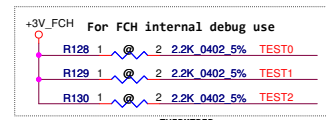
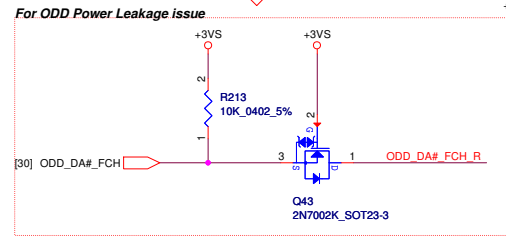
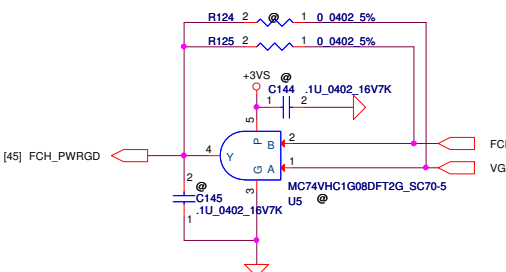
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title
				DDRIII SO-DIMM 2
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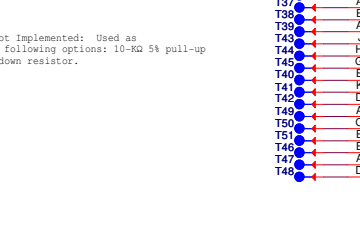
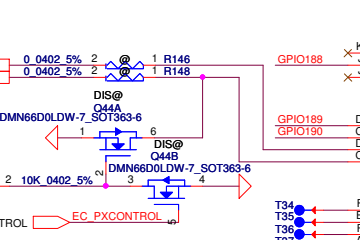
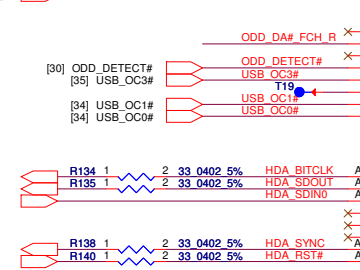
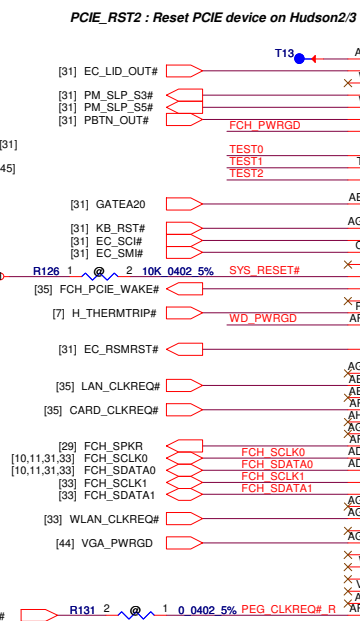
**4MB SPI ROM
& Non-share ROM.**



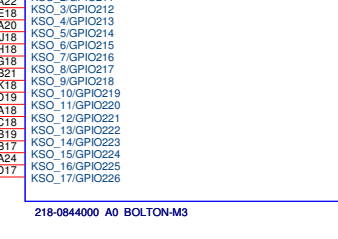
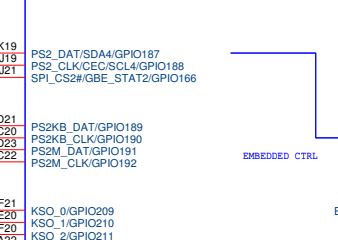
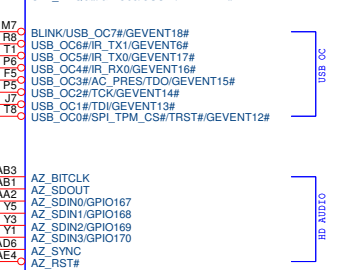
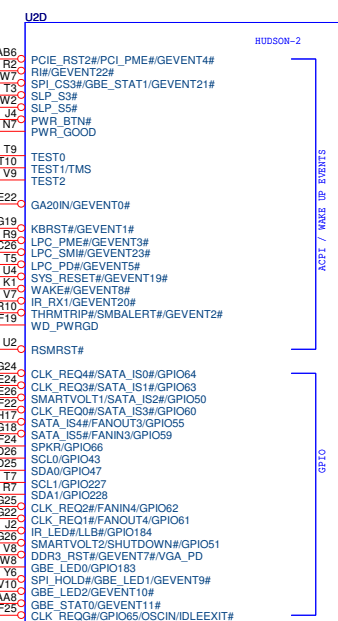
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	FCH SATA/SPT/VGA/HWM/SD	
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				Custom	1.0	
Date: Tuesday, March 12, 2013				Sheet	13	of 51



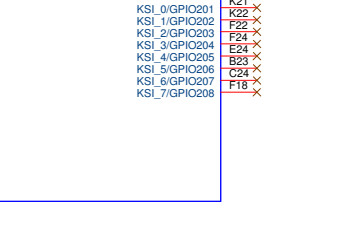
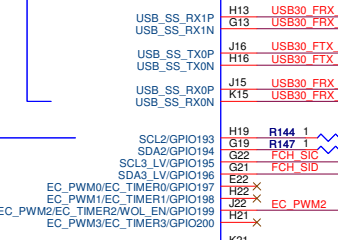
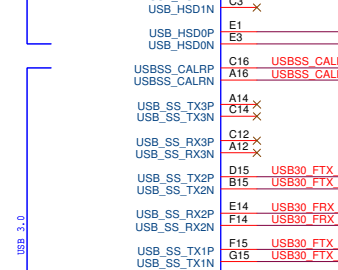
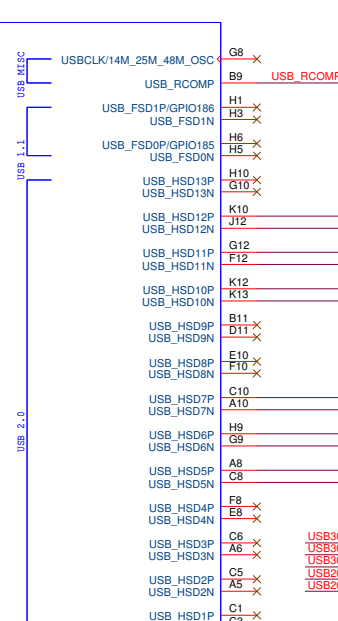
CLKREQG Not Implemented:
Used as GPIO65, IDLEEXIT#, or left unconnected.



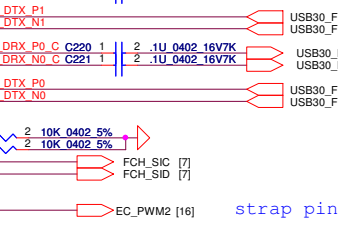
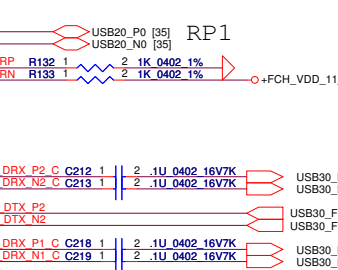
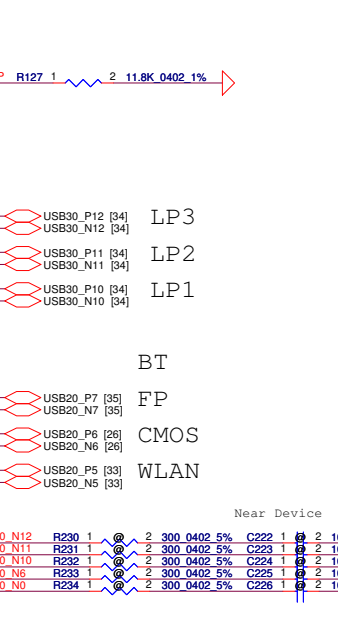
GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
1	1	1	UMA



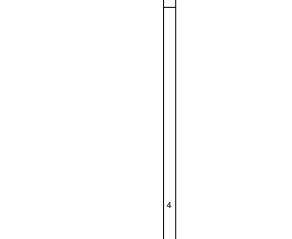
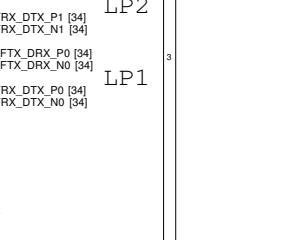
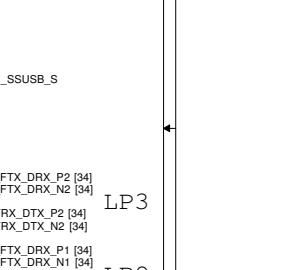
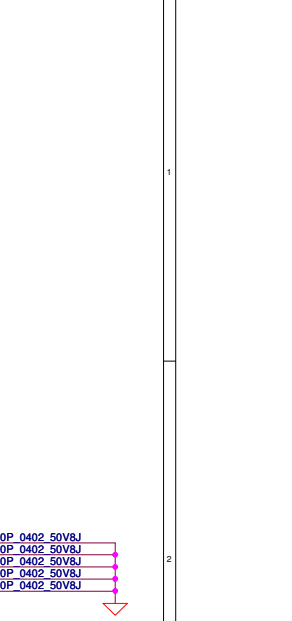
GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
1	1	1	UMA



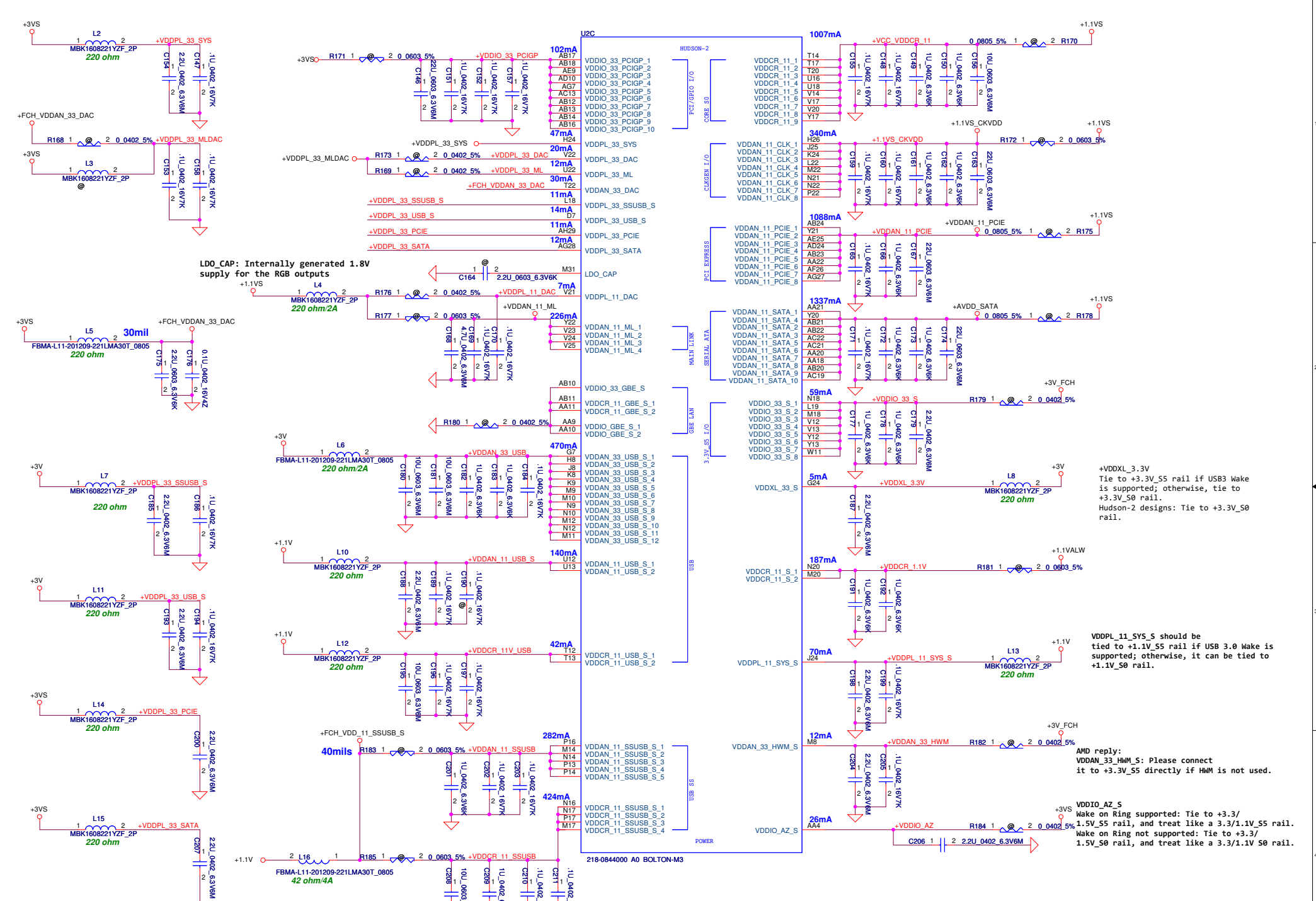
GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
1	1	1	UMA



GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
1	1	1	UMA



GPIO188	GPIO189	GPIO190	Function
0	0	0	PX
0	0	1	Reserved
0	1	0	DISCRET
1	1	1	UMA



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				Rev	Custom	1.0
				Date	Tuesday, March 12, 2013	Sheet 15 of 51

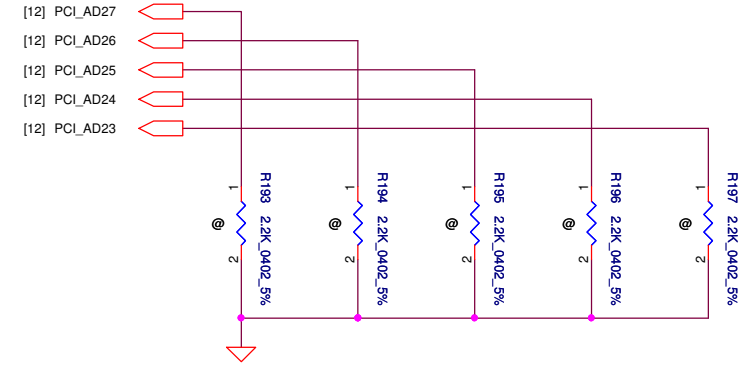
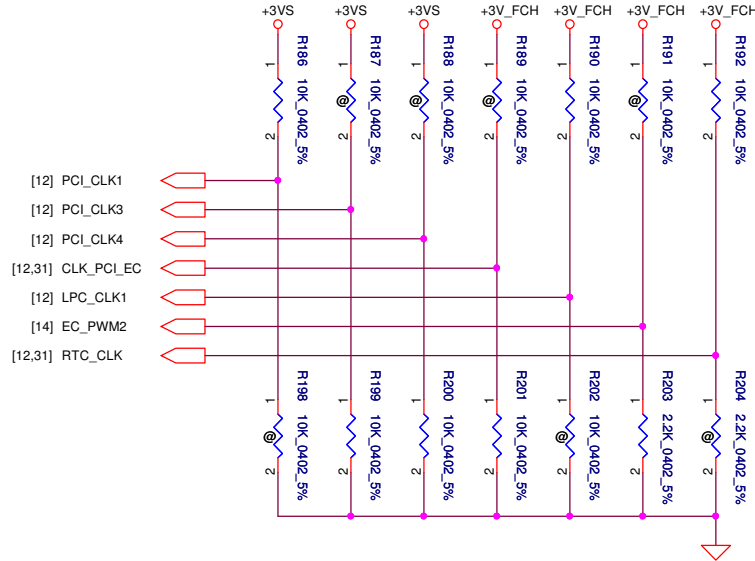
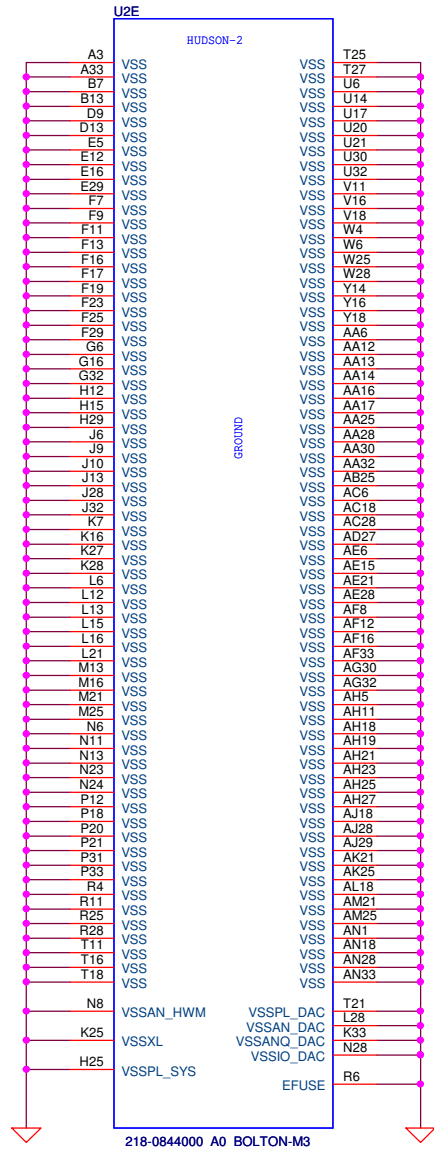
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS DEFAULT	NON FUSION CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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SDV/FVT, NO.11

SDV/FVT, NO.6

+1.8VGS

+1.8VGS

GPIO 28 FDO	MLPS
H	Disable
L	Enable

+1.8VGS

TSVDD MarsCRB Design

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U1401B

PART 2 OF 9

DPA

DPB

DPC

DPD

DAC1

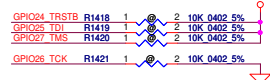
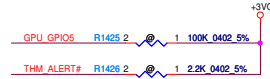
MLPS

DOCAUX

THERMAL

TSVDD

STRAPS

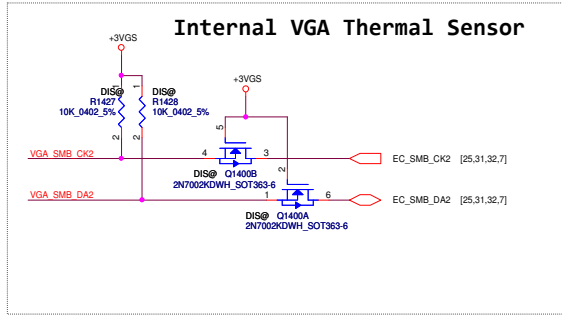


Resistor Divider Lookup Table		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	NC	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are required

Capacitor Divider Lookup Table		
Cap (nF)	Bitd [5:4]	Compal PN
680nF	00	SE00000YJ80
82nF	01	SE076823K80
10nF	10	SE074103KN0
NC	11	

AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

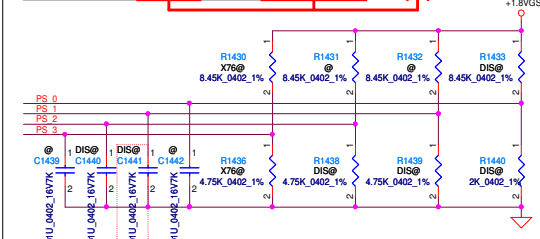
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 10K RESISTOR
X= DESIGN DEPENDANT
NA= NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRNS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFQ[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100-512Kbit M2SP05A (ST) 101-1Mbit M2SP10A (ST) 101-2Mbit M2SP20 (ST) 101-4Mbit M2SP40 (ST) 101-8Mbit M2SP80 (ST) 100-512Kbit Pm2SLV010 (Chingss) 101-1Mbit Pm2SLV010 (Chingss)	XXX
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	X
AUD[1]	NA	00- No audio function 01- Audio for DP only 10- Audio for DP and HDMI if dongle is detected 11- Audio for both DP and HDMI	XX
AUD[0]	NA	HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	
CEC_DIS	PS_0[4]	Reserved for future ASIC	0
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111= 0 usable endpoints 110= 1 usable endpoints 101= 2 usable endpoints 100= 3 usable endpoints 011= 4 usable endpoints 010= 5 usable endpoints 000= 6 usable endpoints 000= all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1	0 0 1	NC	8.45K	2K
PS_1[5:1]	1 1	0 0 0	NC	NC	4.75K
PS_2[5:1]	0 0	0 0 0	680 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	NC	X	X

Mapping to VRAM type please refer to page 04



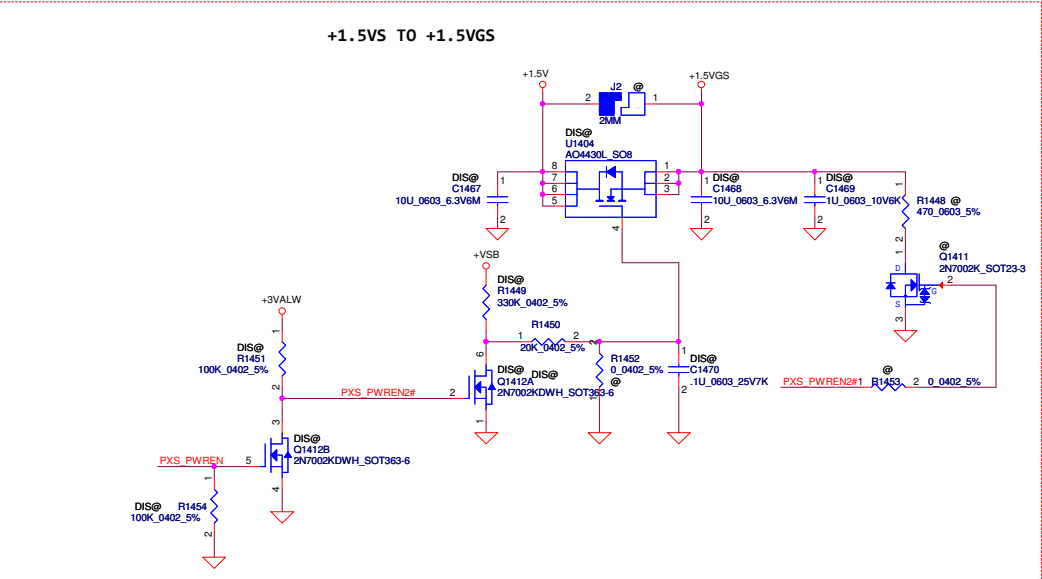
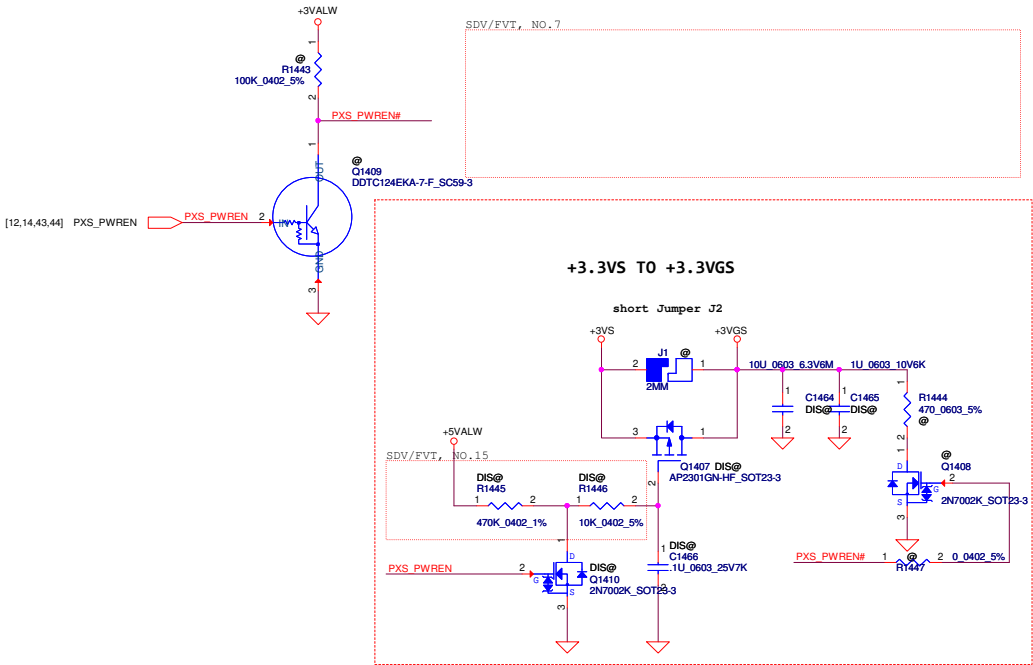
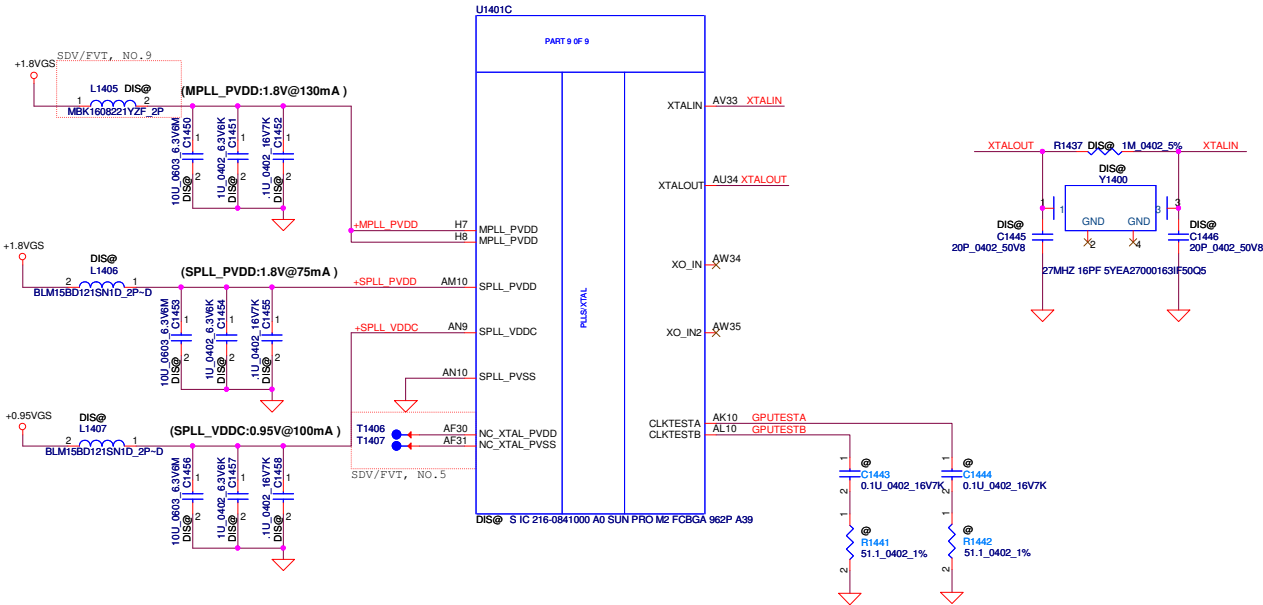
Place CLOSE VGA CHIP

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Size C	Document Number	LA-8126P		Rev 1.0
Date:	Tuesday, March 12, 2013	Sheet	18	of 51

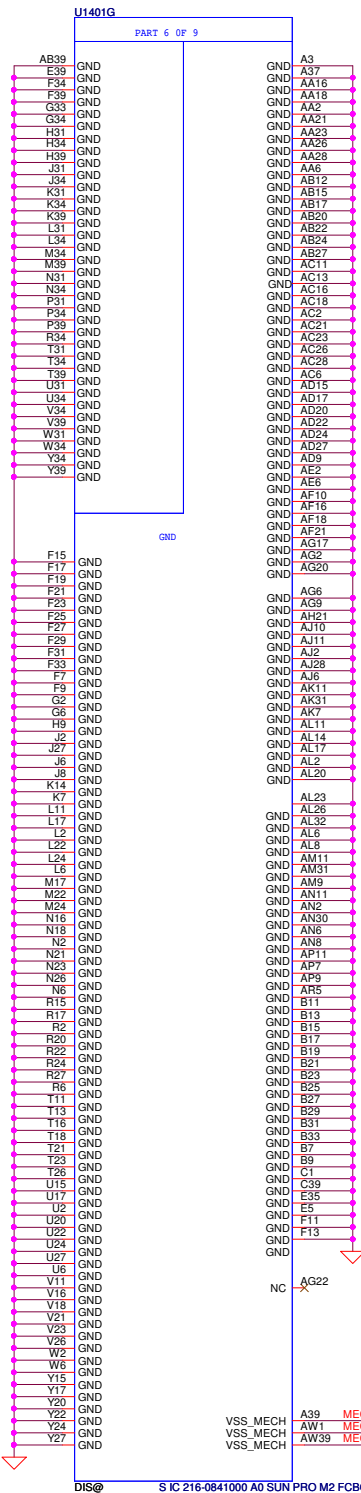
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



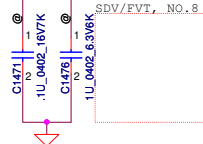
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title
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Date: Tuesday, March 12, 2013				Document Number LA-8126P
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DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

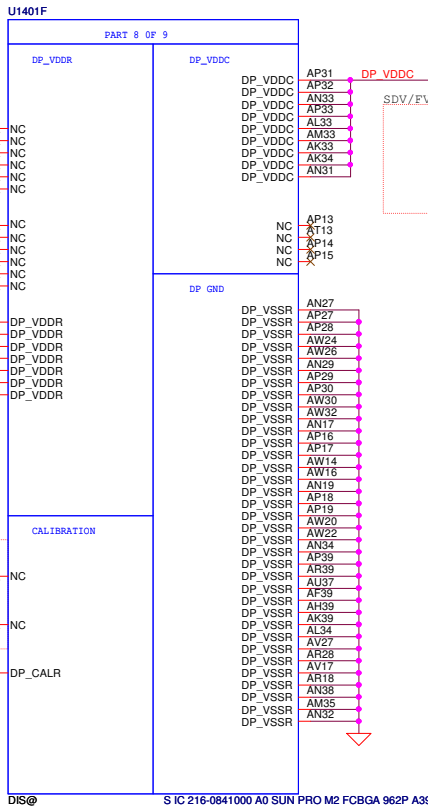
AMD:
no display from GPU,
can uninstall the capacitors

+1.8VGS
R1456 1 2 0.0402 5% (DP_VDDR:1.8V@237mA/link)

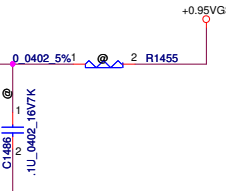


SDV/EVT, NO.10

R1459 2 DIS@ 1 150 0402 1% AM39 DP_CALR



(DP_VDDC:0.95V@280mA/link)



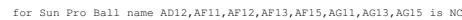
DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

S IC 216-0841000 A0 SUN PRO M2 FCBGA 962P A39

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								AT1 Sun Pro M2 PWR GND	
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						LA-8126P		1.0	
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(VDDR1:1.5V@3A,GDDR5:1125MHz)



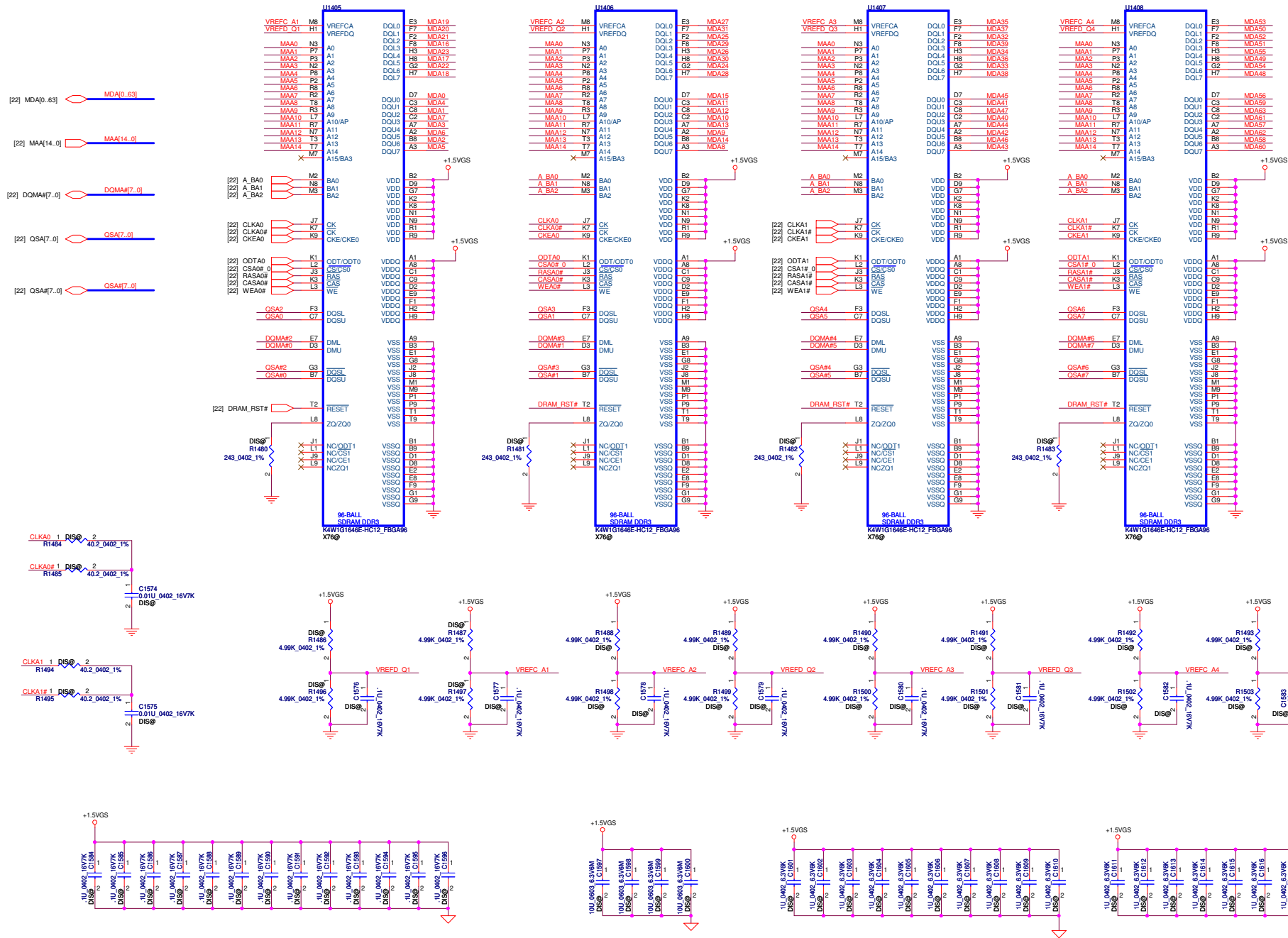
[44] VCCSENSE_VGA

[44] VSSSENSE_VGA

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

The Seymour M2 only support channel B (64 bit),
this page unmount all parts

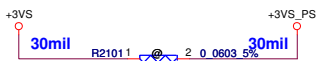


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Size	Document Number	LA-8126P	Rev	1.0
Date:	Tuesday, March 12, 2013	Sheet	23	of 51

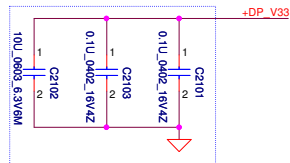
The Mars Pro M2 only support channel B (64 bit)

SDV/EVT., No.4

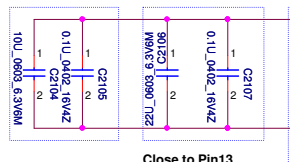
Security Classification	Compal Secret Data			Title	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	ATT Sun Pro M2 VRAM B	
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				Sheet 24 of 51	



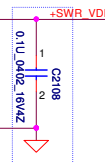
Close to Pin3



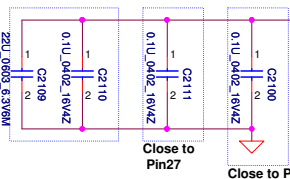
Close to L27



Close to Pin18



Close to L29

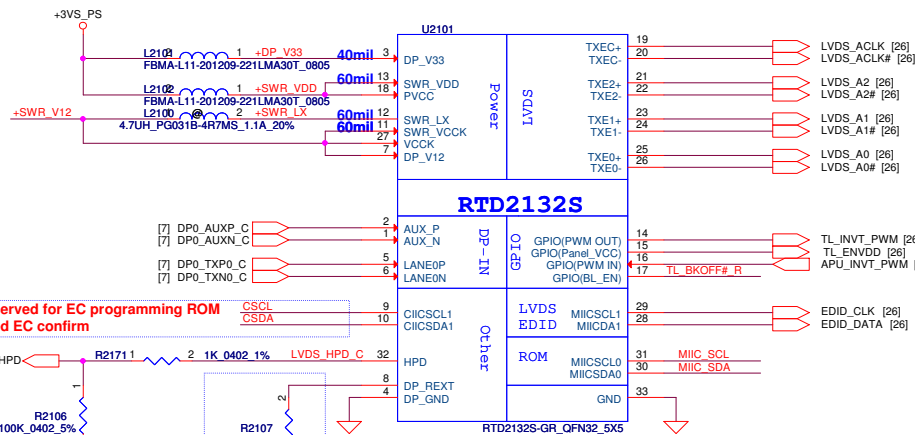


Close to Pin13

Close to Pin27

Close to Pin7

Part number: SA00004EU10



[7] DP0_AUXP_C
[7] DP0_AUXN_C
[7] DP0_TXP0_C
[7] DP0_TXN0_C

Reserved for EC programming ROM
Need EC confirm

CSCS
CSDA

[7] LVDS_HPD

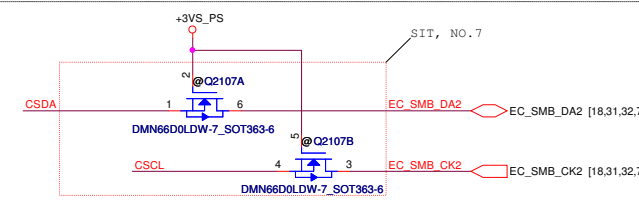
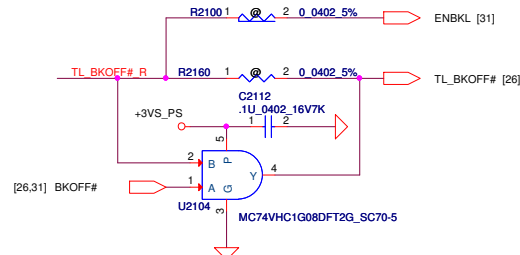
LVDS_HPD_C

R2106 100K_0402_5%

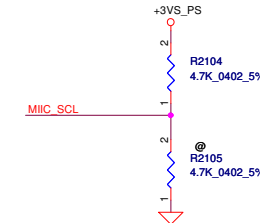
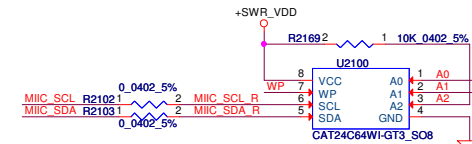
R2107 12K_0402_1%

Change to 12Kohm 1% (DG ref.)
20101114

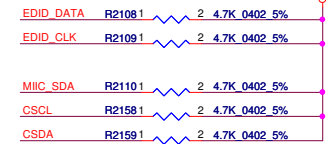
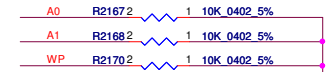
Vendor advise reserve it



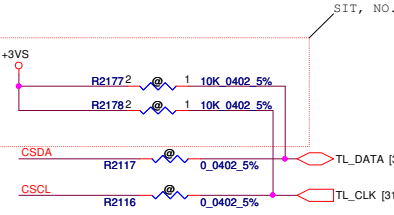
EEROM



2132S-Ver E: External ROM, pin31 PU +3VS
Internal RAM support, pin31 PD to GND
EEROM EEROM EEROM EEROM



Vendor Suggest 2011.08.15



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LCD POWER CIRCUIT

LCD/LED PANEL Conn.

CMOS Camera Conn

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Date:	Tuesday, March 12, 2013	Sheet	26	of	51

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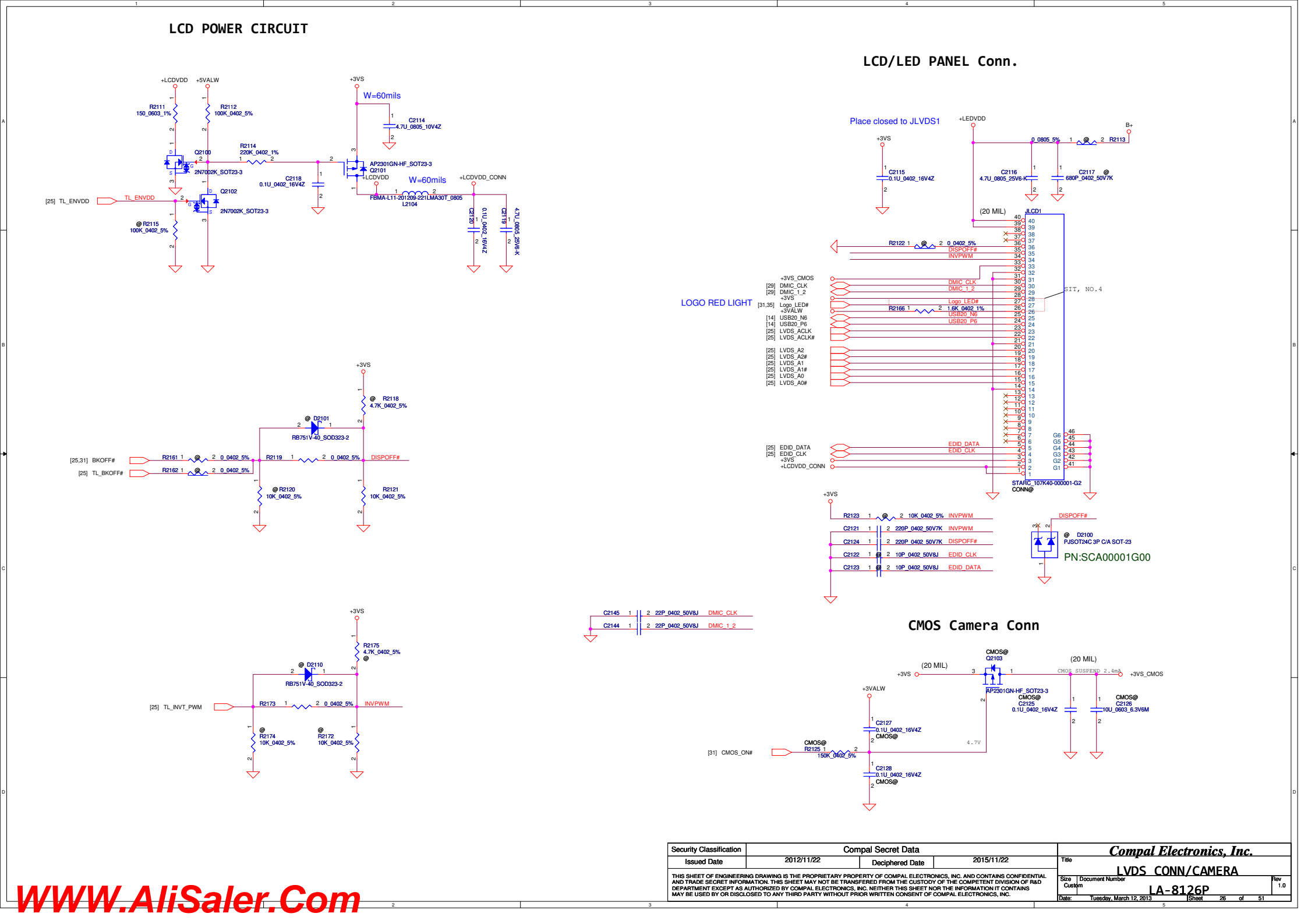
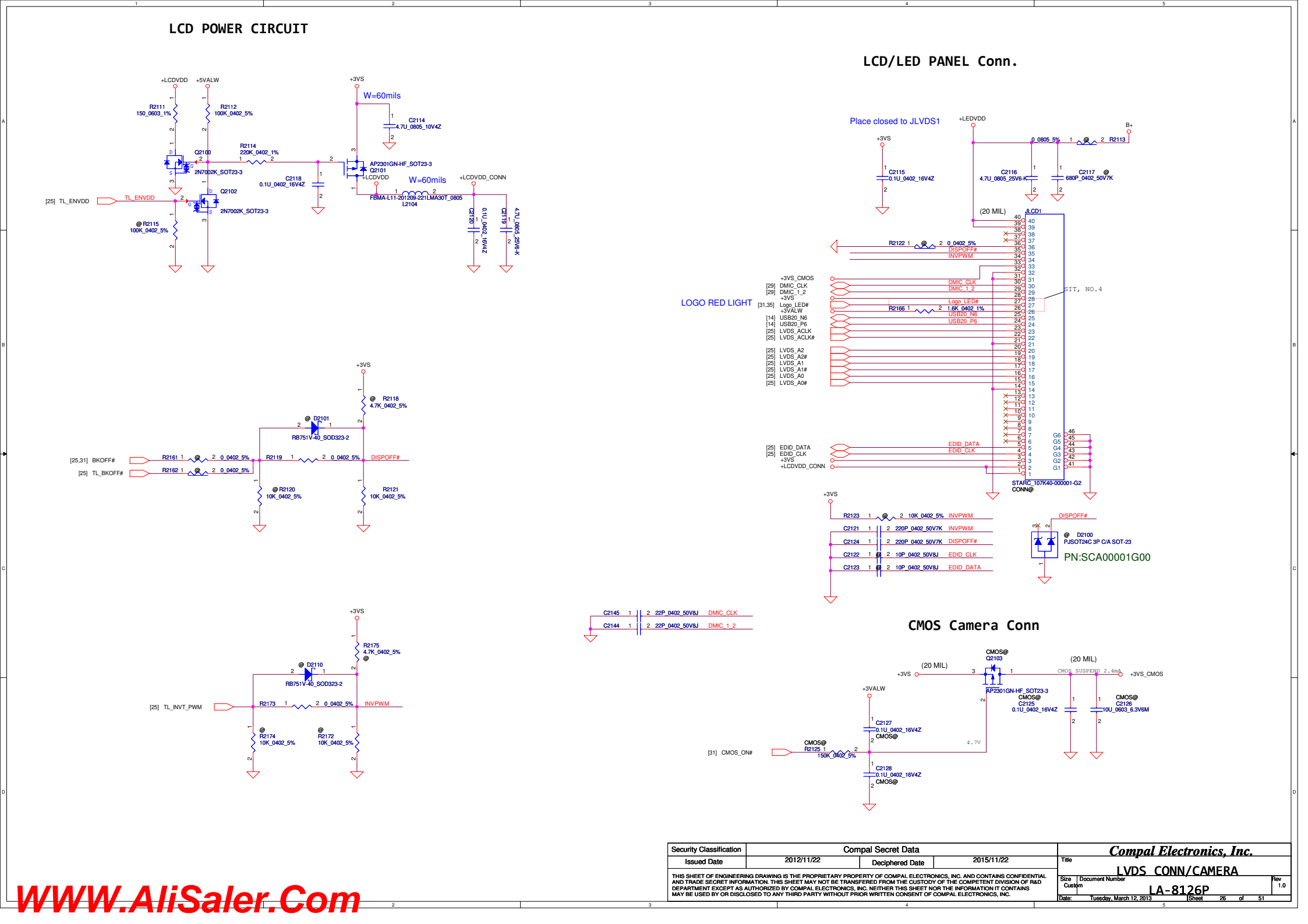
LCD POWER CIRCUIT

LCD/LED PANEL Conn.

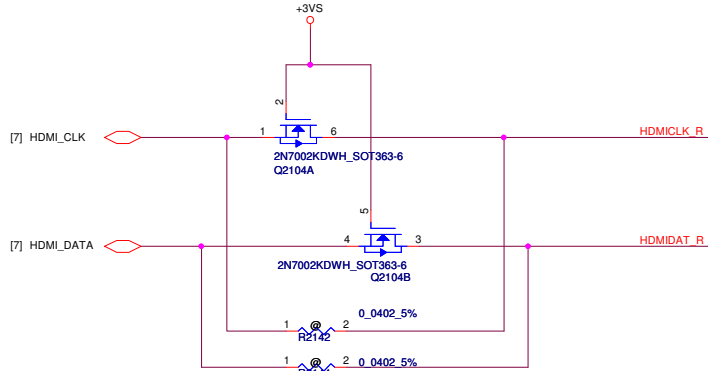
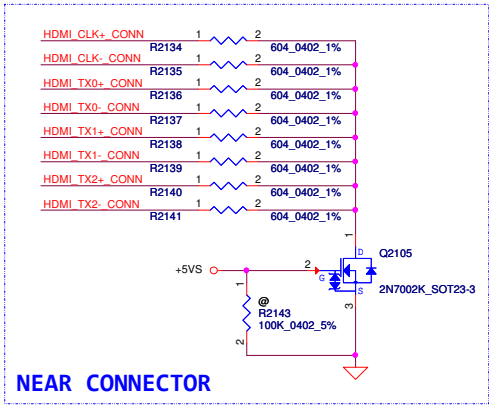
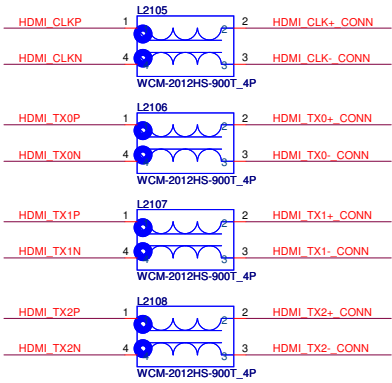
CMOS Camera Conn

Security Classification		Compal Secret Data		Title	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	LVDS CONN/CAMERA	
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Date:	Tuesday, March 12, 2013	Sheet	26 of 51	LA-8126P	

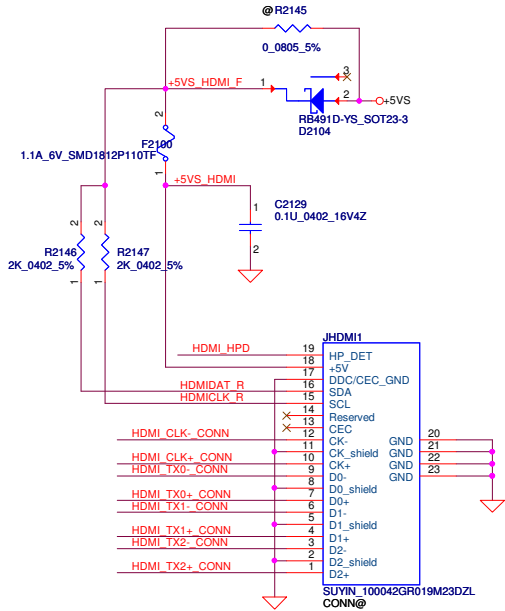
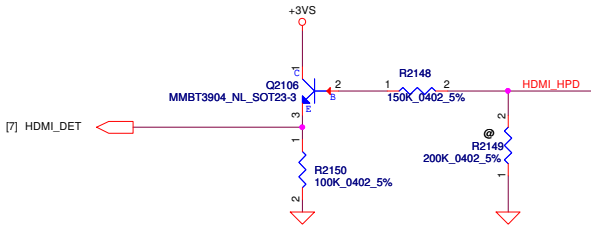
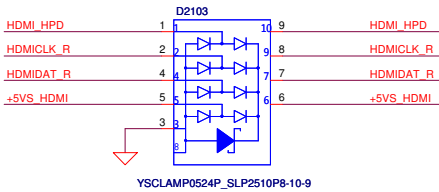
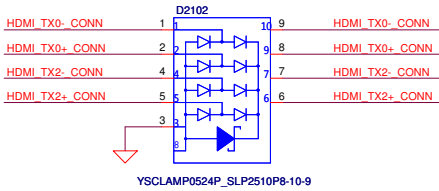
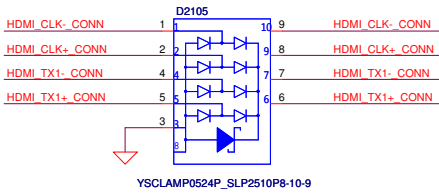
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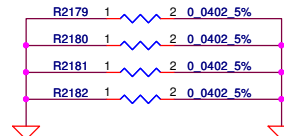
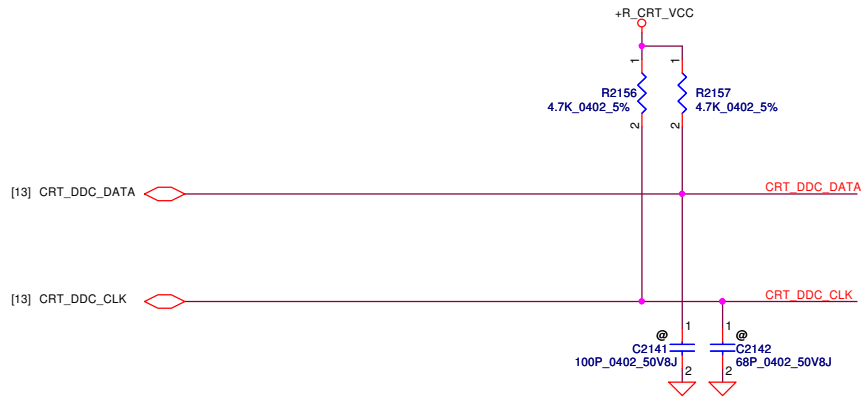
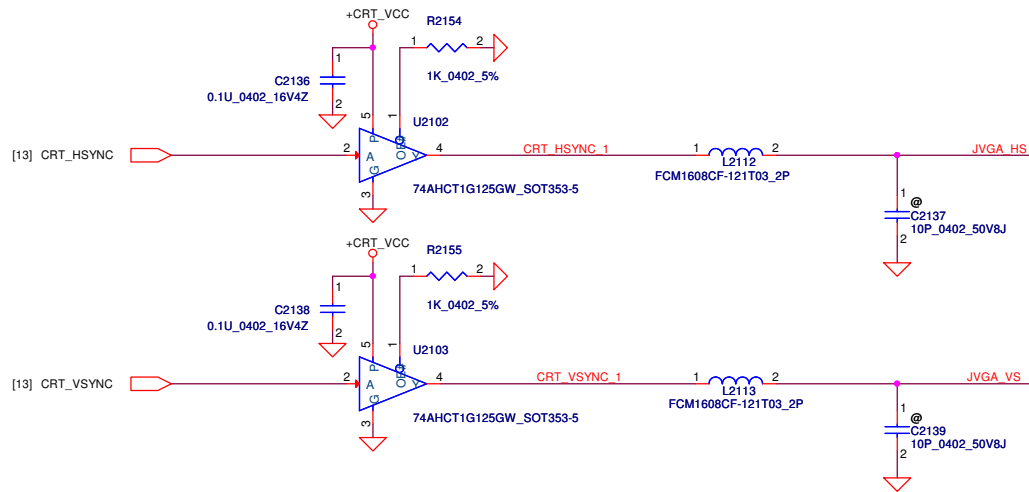
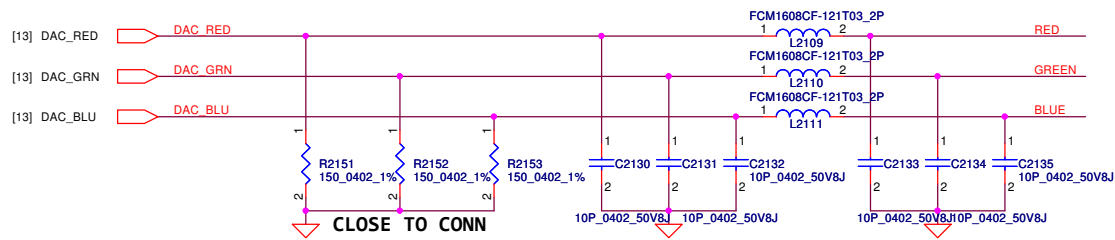
[7] HDMI_CLKP	R2126	1	2	0	0402_5%	HDMI_CLK+_CONN
[7] HDMI_CLKN	R2127	1	2	0	0402_5%	HDMI_CLK-_CONN
[7] HDMI_TX0P	R2128	1	2	0	0402_5%	HDMI_TX0+_CONN
[7] HDMI_TX0N	R2129	1	2	0	0402_5%	HDMI_TX0-_CONN
[7] HDMI_TX1P	R2130	1	2	0	0402_5%	HDMI_TX1+_CONN
[7] HDMI_TX1N	R2131	1	2	0	0402_5%	HDMI_TX1-_CONN
[7] HDMI_TX2P	R2132	1	2	0	0402_5%	HDMI_TX2+_CONN
[7] HDMI_TX2N	R2133	1	2	0	0402_5%	HDMI_TX2-_CONN



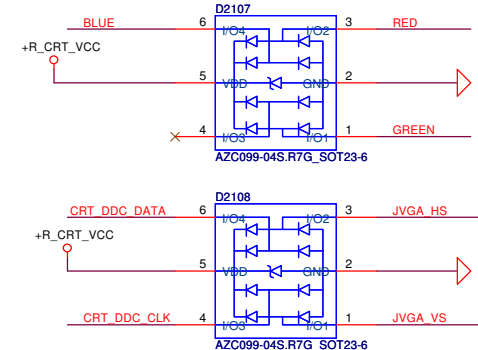
ESD Request



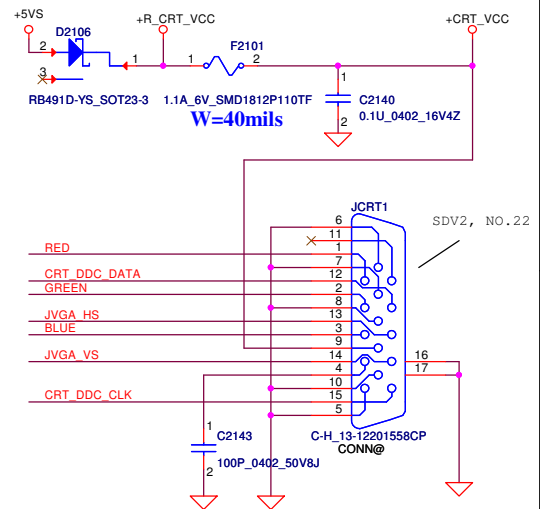
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ESD Request



CRT Connector



AMD check list update
20101110

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				Size		Document Number			Rev	
				Custom		LA-8126P			1.0	
				Date:		Tuesday, March 12, 2013		Sheet		28 of 51

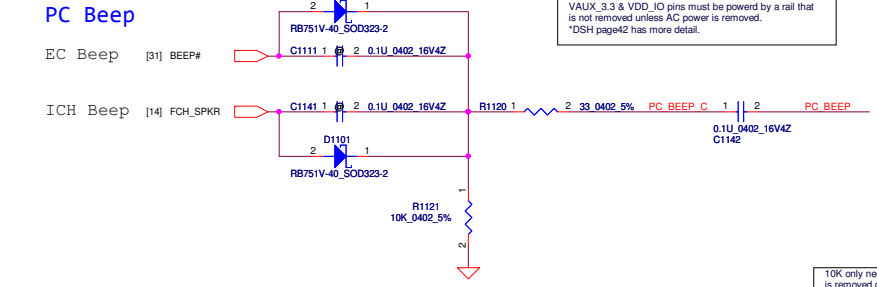
Compal Electronics, Inc.

CRT Connector

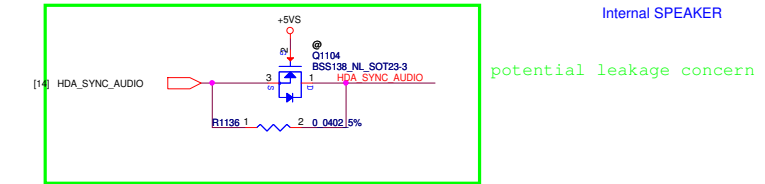
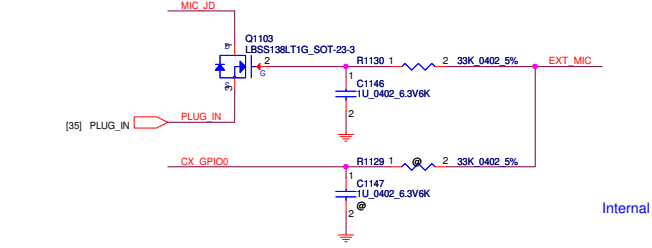
LA-8126P

Rev 1.0

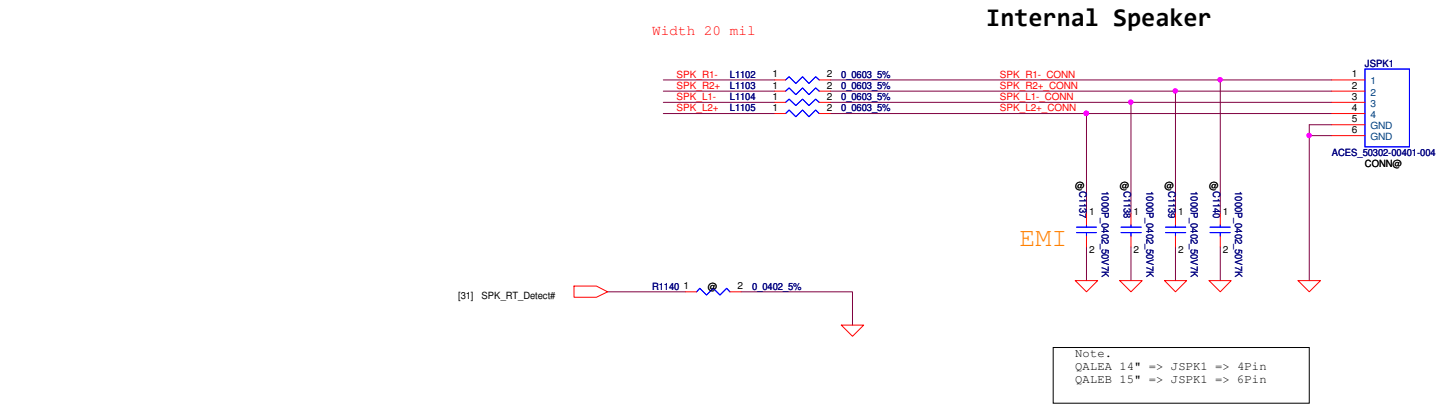
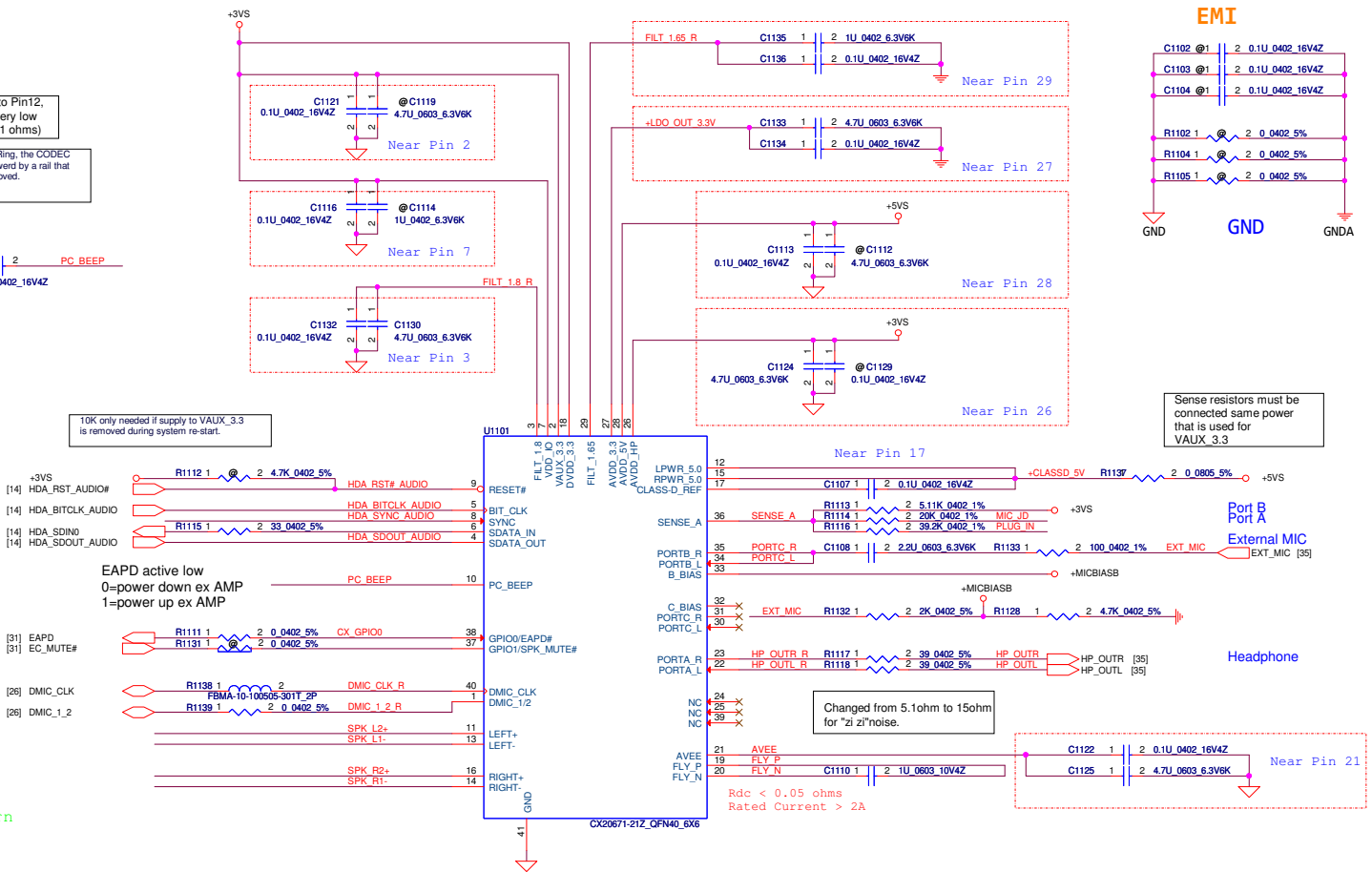
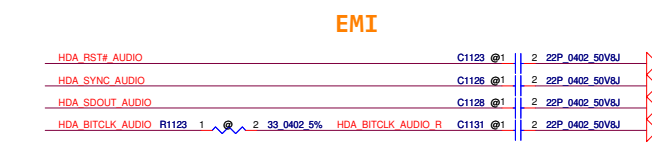
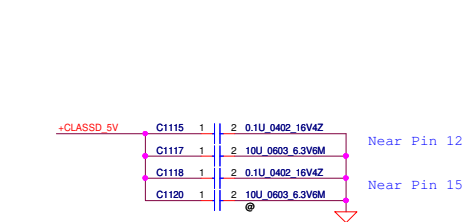
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Combo Jack detect (normal close)

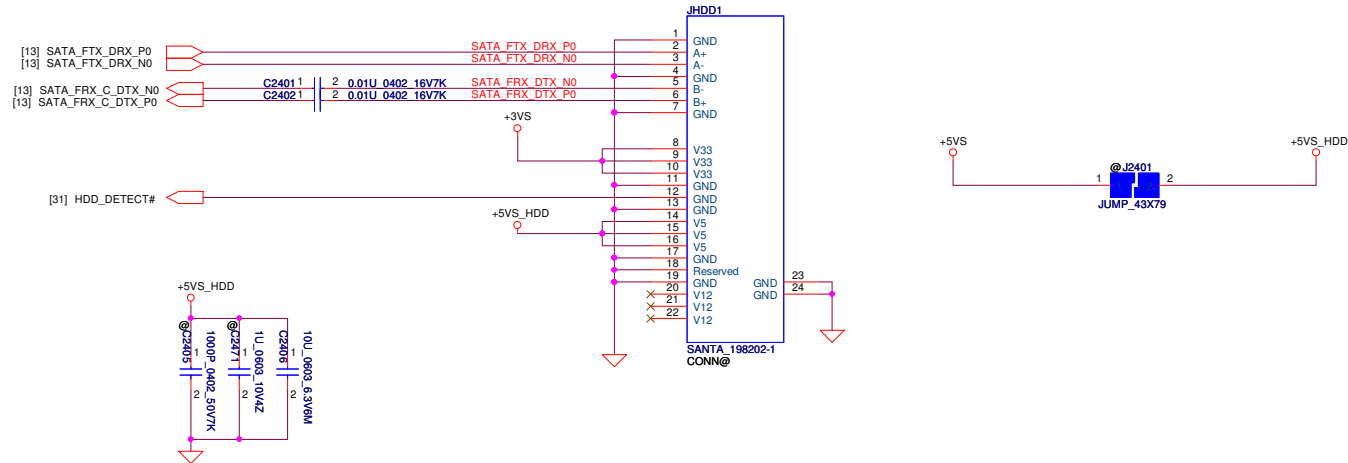


Decoupling CAP

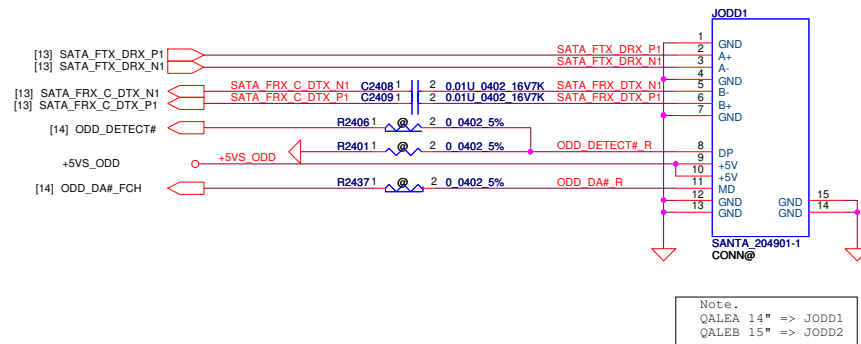


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Title		Compal Electronics, Inc.	
Size		HD Audio Codec CX20671	
Customer		LA-8126P	
Date		Tuesday, March 12, 2013	
Sheet		29 of 51	

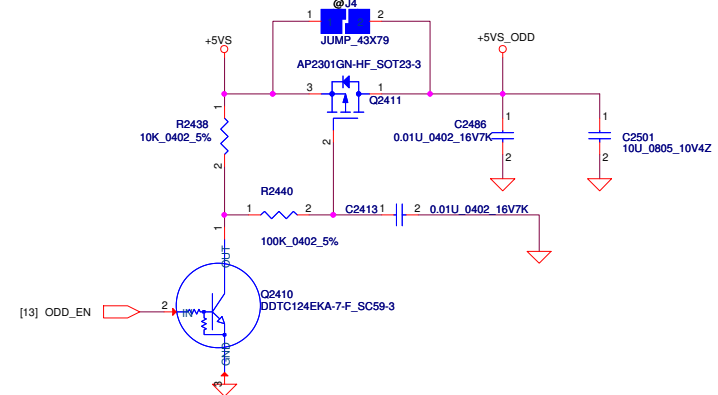
SATA HDD Conn.



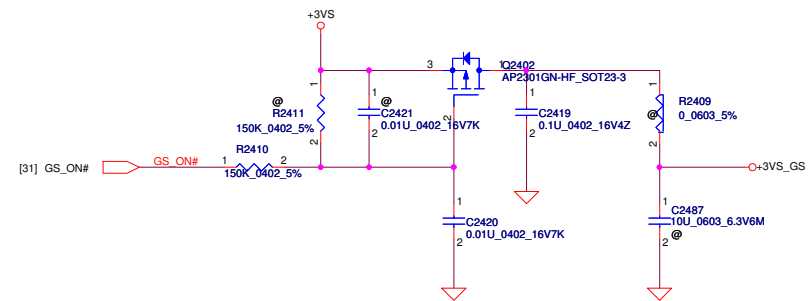
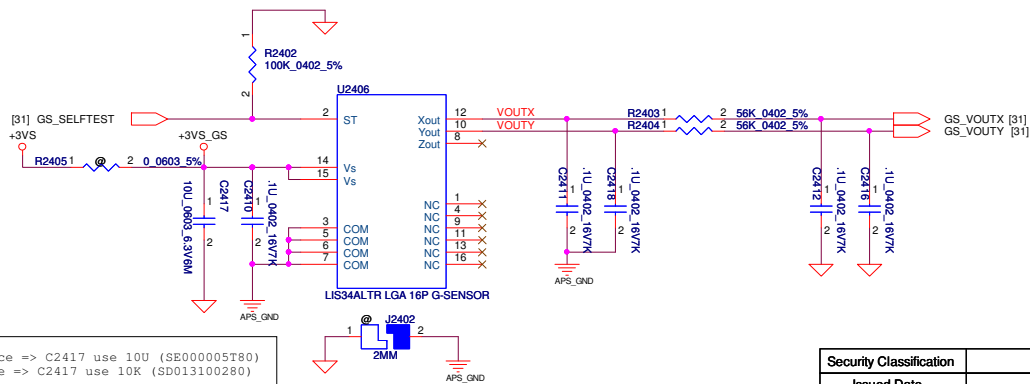
SATA ODD Conn.



ODD Power Control1

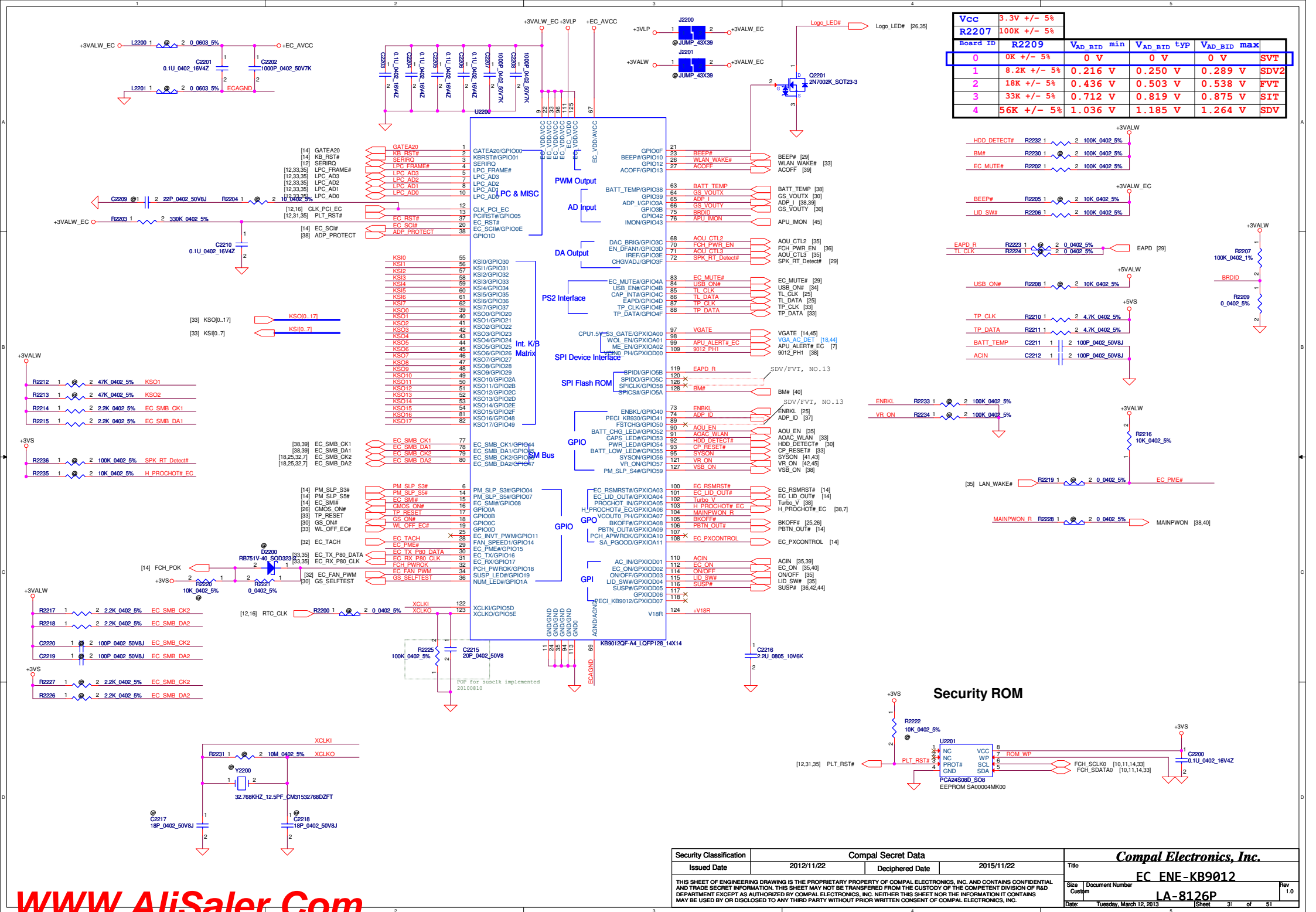


APS G-Sensor



Note.
Main Source => C2417 use 10U (SE000005T80)
2nd Source => C2417 use 10K (SD013100280)

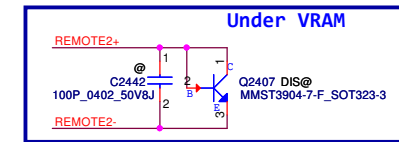
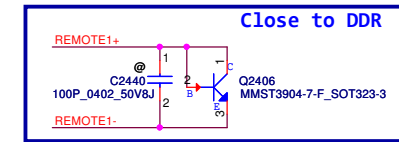
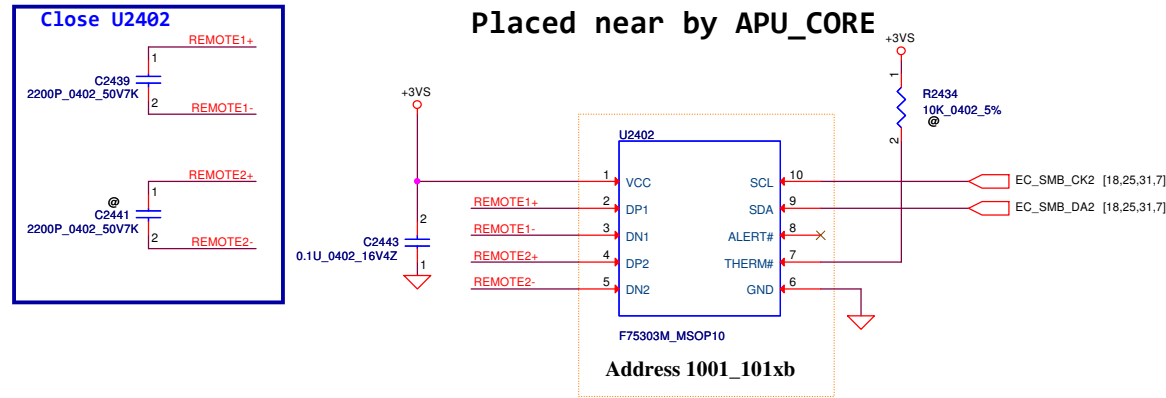
Security Classification		Compal Secret Data		Title	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	HDD/ODD/G-Sensor	
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Vcc		3.3V +/- 5%			
R2207		100K +/- 5%			
Board ID	R2209	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	
0	0K +/- 5%	0 V	0 V	0 V	SVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	SDV

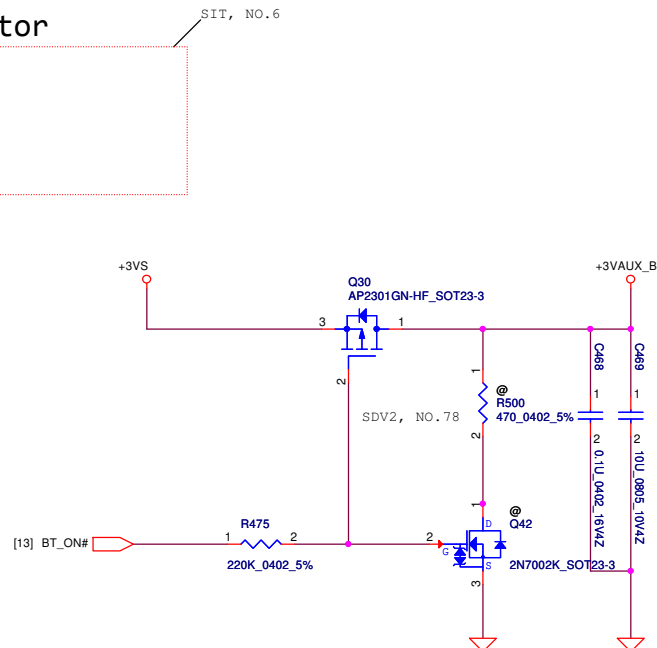
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Issued Date	2012/11/22	Deciphered Date	2015/11/22
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EC ENE-KB9012		Rev 1.0	
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Fintek Thermal sensor Placed near by APU_CORE

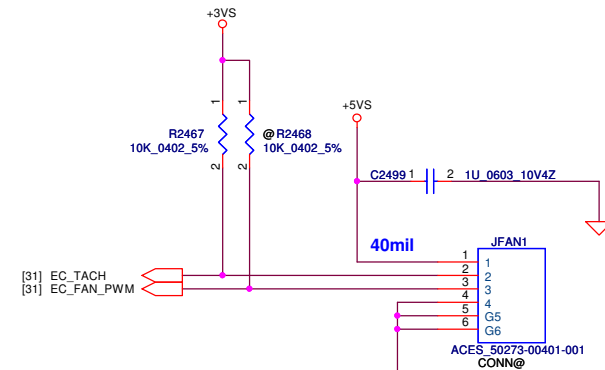


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

BT Connector

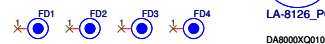
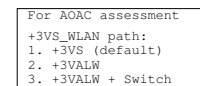
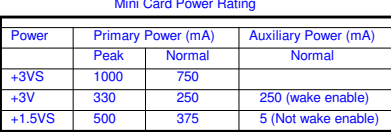


FAN1 Conn



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The schematic diagram illustrates the electrical connections for the ACES 51522-01001-001 connector. It shows a +5VS supply connected to the TP_CLK2, TP_DATA2, TP_RESET, and TP_DETECT lines. A +3VS supply is connected to the FCH_SCLK1_R and FCH_SDATA1_R lines. The connector is labeled ACES 51522-01001-001 CONN@.

Signal Connections:

- FCH_SCLK1:** Connected to TP_CLK2 (R2473, 2 4.7K 0402 5%).
- FCH_SDATA1:** Connected to TP_DATA2 (R2464, 2 4.7K 0402 5%).
- CP_RESET#:** Connected to TP_RESET (R2470, 2 4.7K 0402 5%).
- TP_CLK:** Connected to TP_DETECT (R2472, 2 0.0402 5%).
- TP_DATA:** Connected to CP_RESET# (R2471, 2 100K 0402 1%).

Power Connections:

- +5VS:** Connected to TP_CLK2, TP_DATA2, TP_RESET, and TP_DETECT.
- +3VS:** Connected to FCH_SCLK1_R and FCH_SDATA1_R.

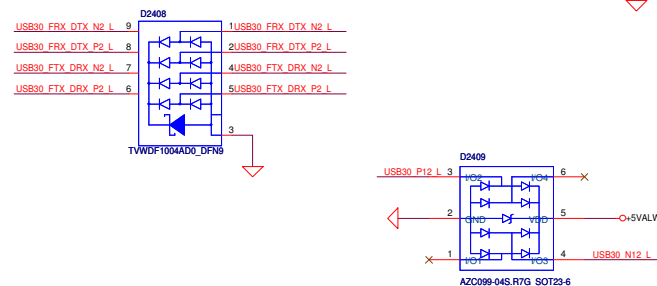
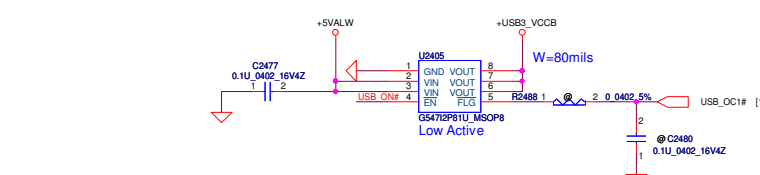
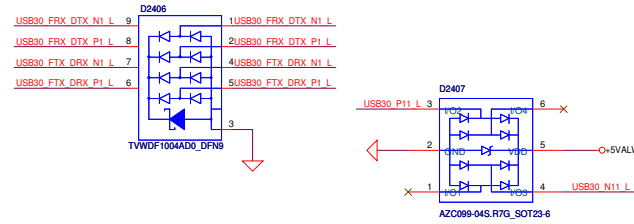
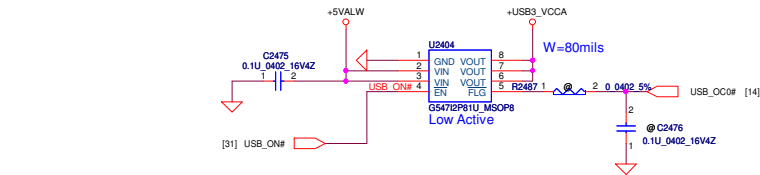
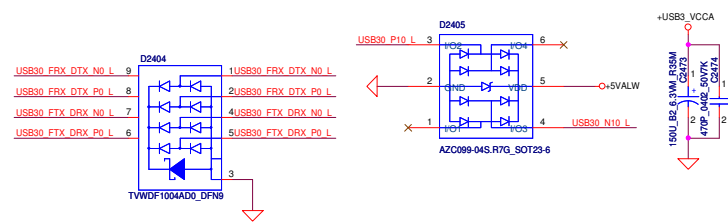
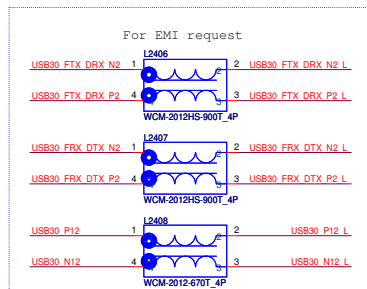
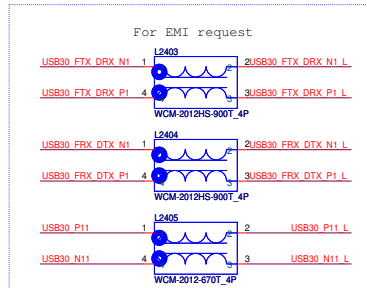
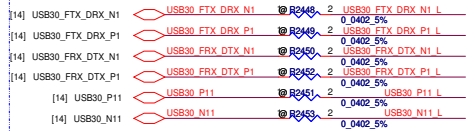
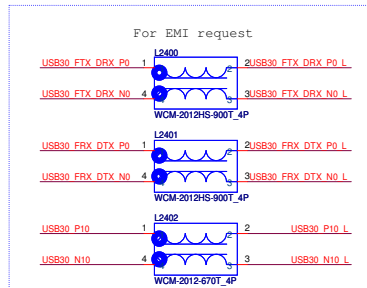
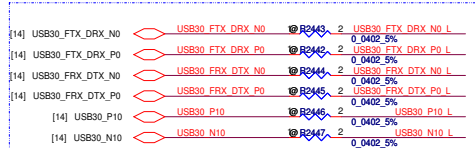
Resistor Values:

- R2473: 2 4.7K 0402 5%
- R2464: 2 4.7K 0402 5%
- R2470: 2 4.7K 0402 5%
- R2472: 2 0.0402 5%
- R2471: 2 100K 0402 1%
- R2497: 2 2.2K 0402 5%
- R2498: 2 2.2K 0402 5%

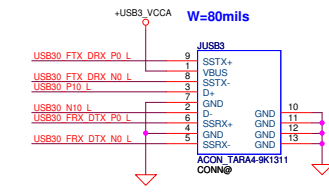
Connector Pinout:

- 1: FCH_SCLK1_R
- 2: FCH_SDATA1_R
- 3: TP_DETECT
- 4: TP_DATA2
- 5: TP_CLK2
- 6: CP_RESET#
- 7: TP_DATA
- 8: TP_CLK
- 9: TP_DATA
- 10: TP_DATA
- 11: GND
- 12: GND

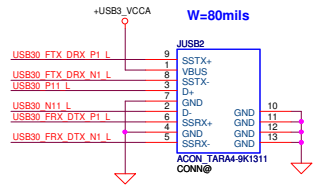
USB3.0 Conn *3



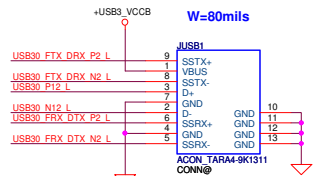
LP1



LP2

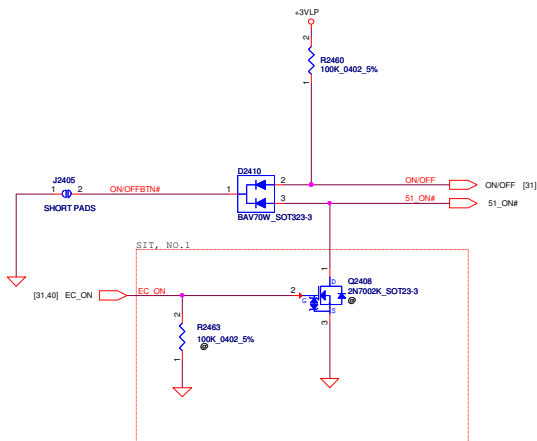


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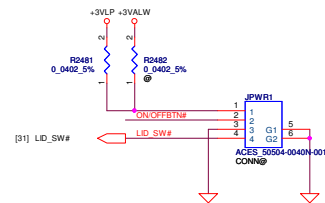


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				USB 3.0 Conn	
				Size	Document Number
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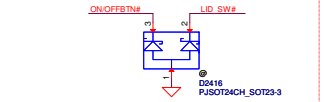
ON/OFF switch



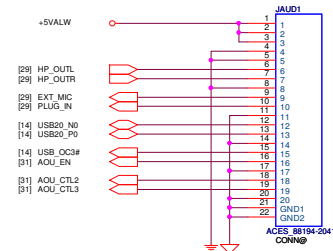
Power Button Board Conn



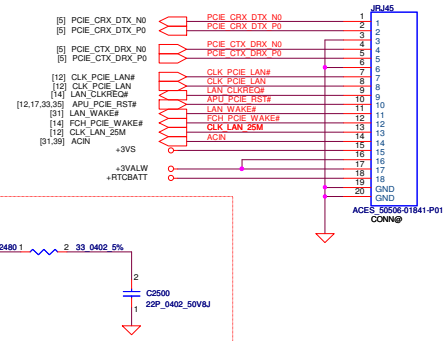
ESD Request



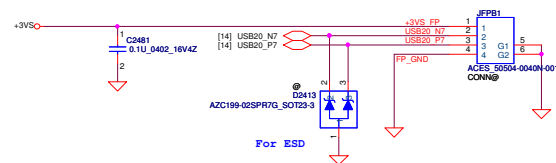
USB2.0/Audio Jack SB CONN



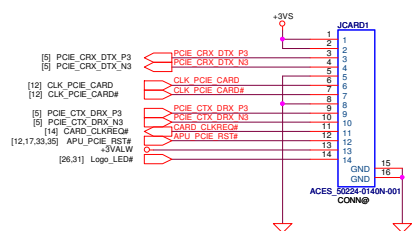
Lan Conn



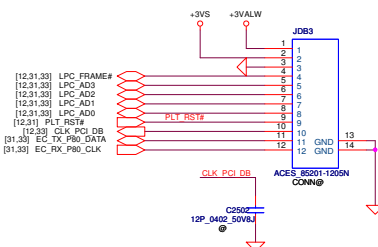
Finger Printer



Card Reader

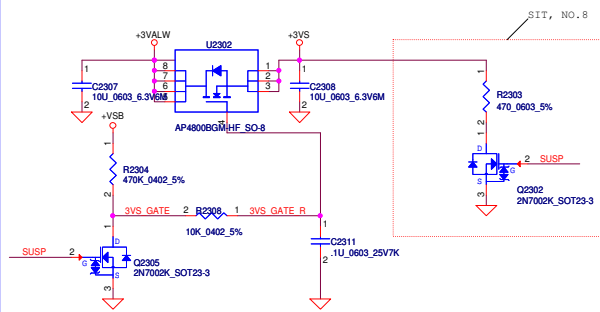


Debug Conn.

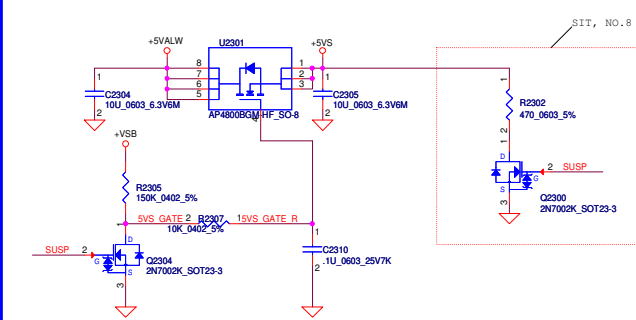


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				Outline	LA-8126P	1.0
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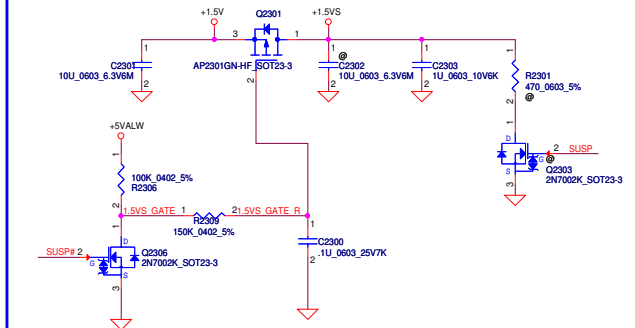
+3VALW TO +3VS



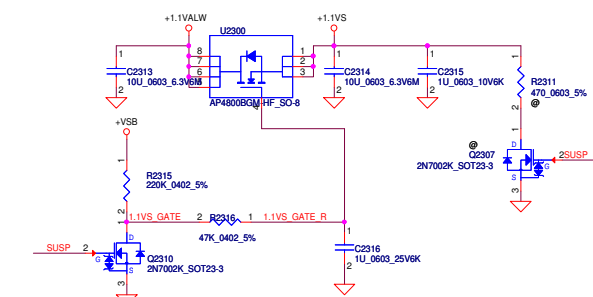
+5VALW TO +5VS



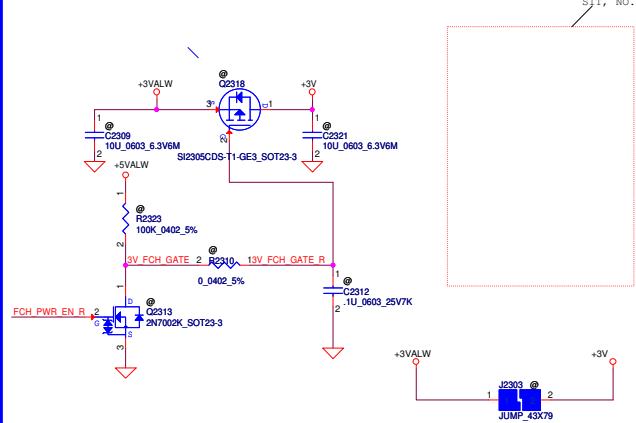
+1.5V to +1.5VS



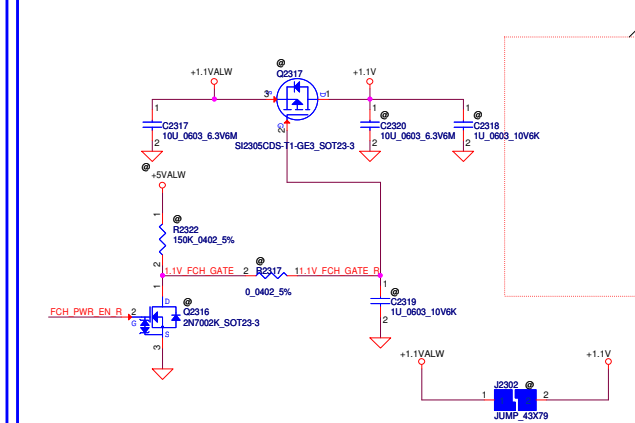
+1.1VALW to +1.1VS



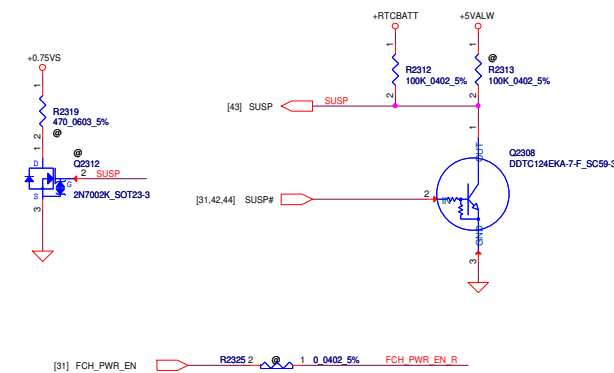
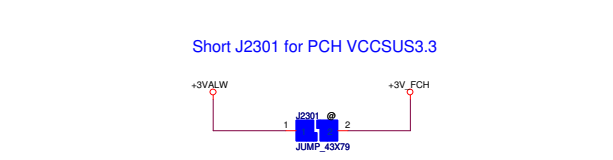
+3VALW TO +3V



+1.1VALW to +1.1V



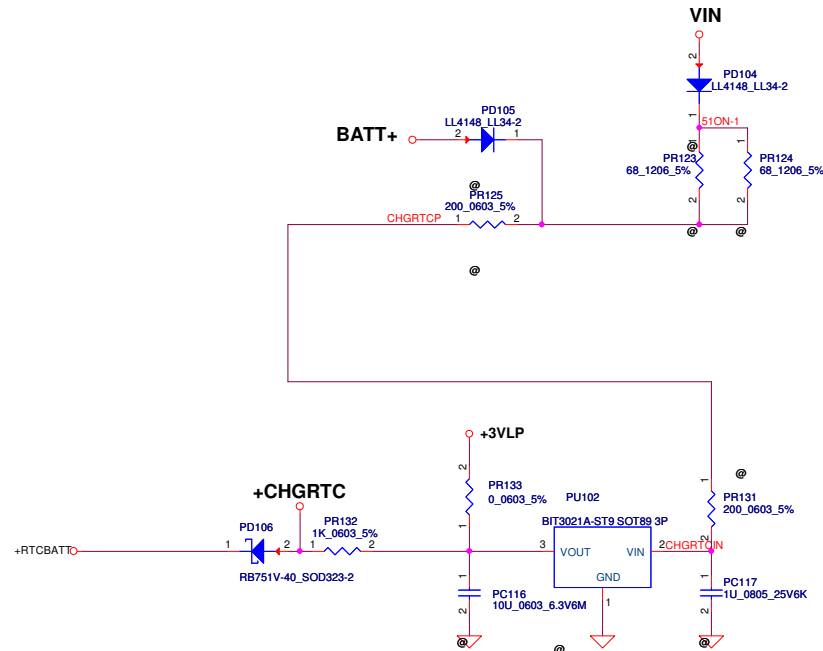
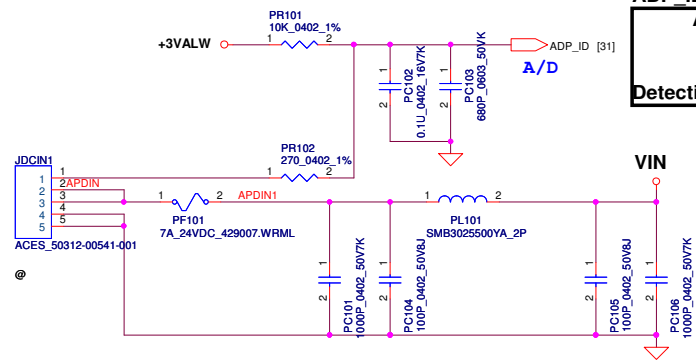
+3VALW TO +3V_FCH



Short J2301 for PCH VCCSUS3.3

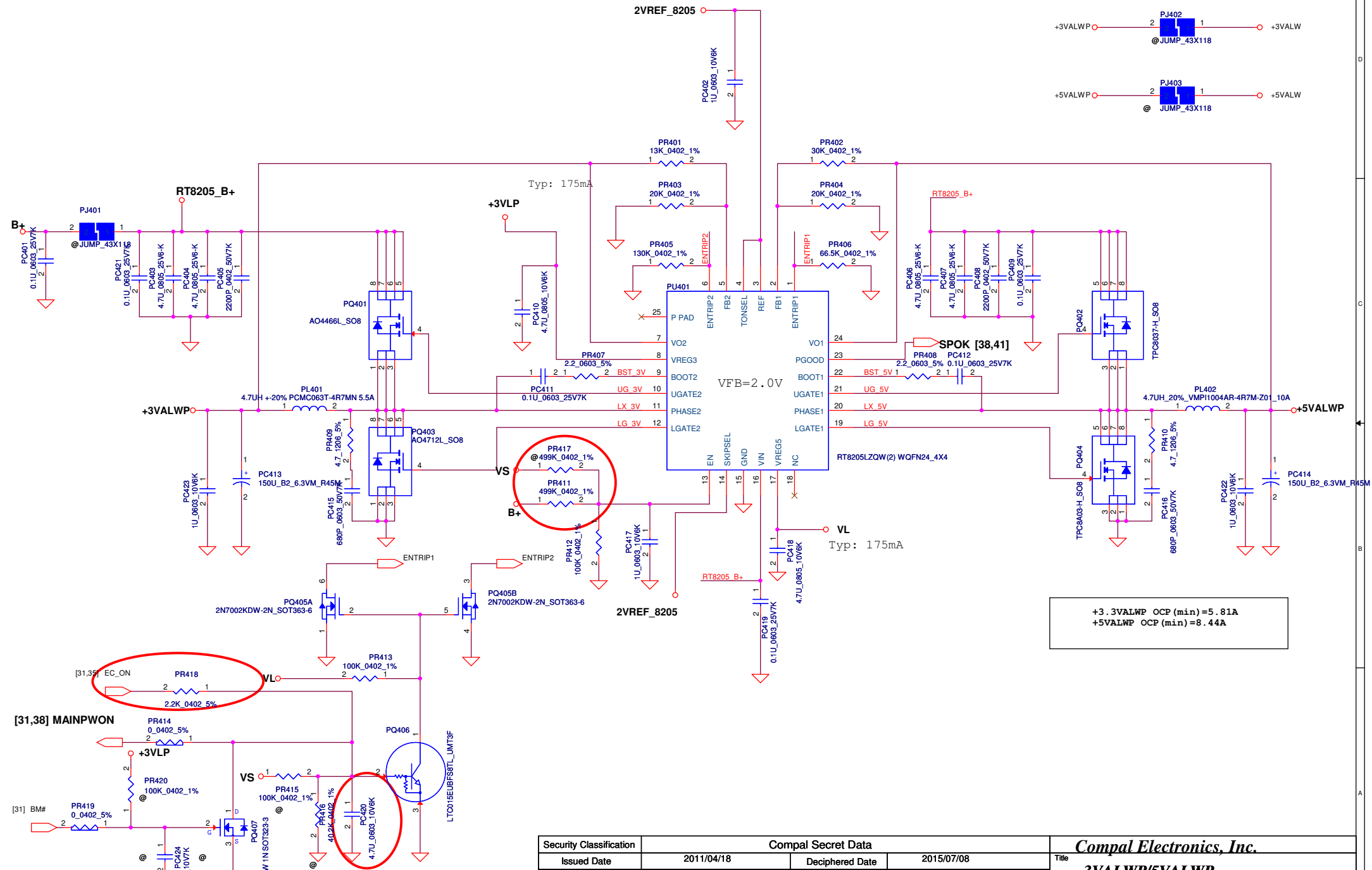
ADP_ID

AC Adapter	135W	90W	65W
R(K ohm)	0	open	10
ADP_ID(V)	0	3.3	1.65
Detection voltage	<0.33	>2.64	1.32~1.98



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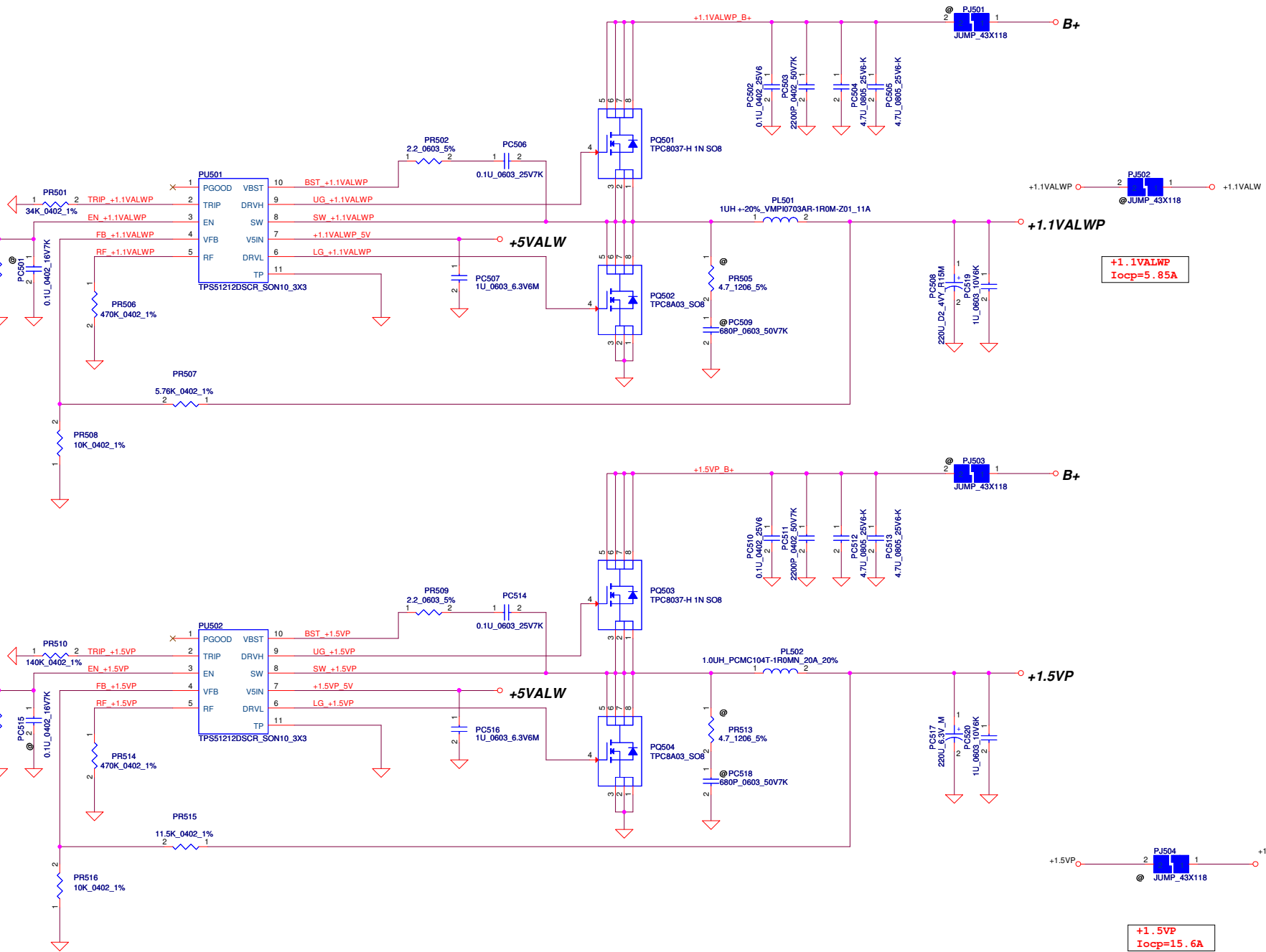
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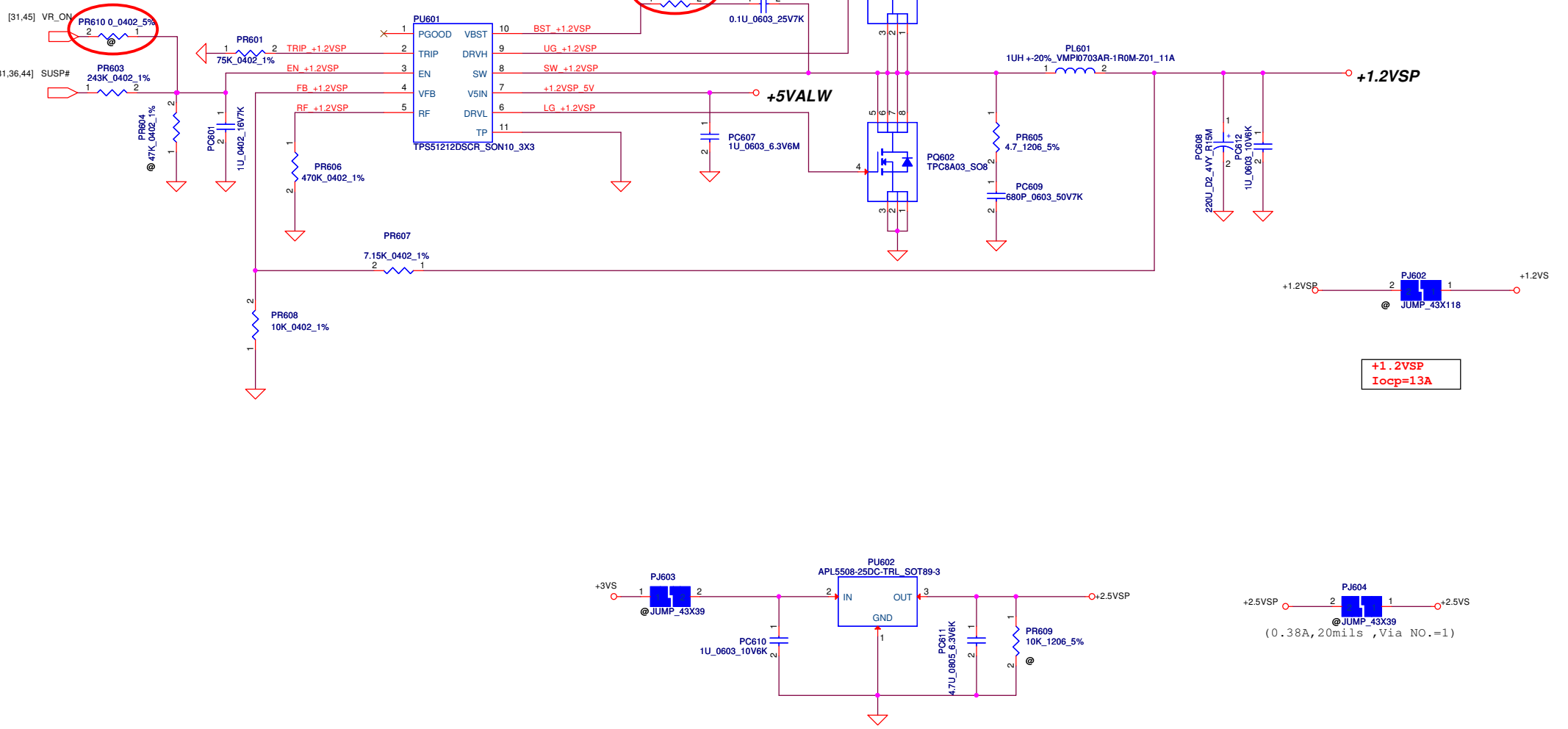
[38,40] SPOK

[31,43] SYSON

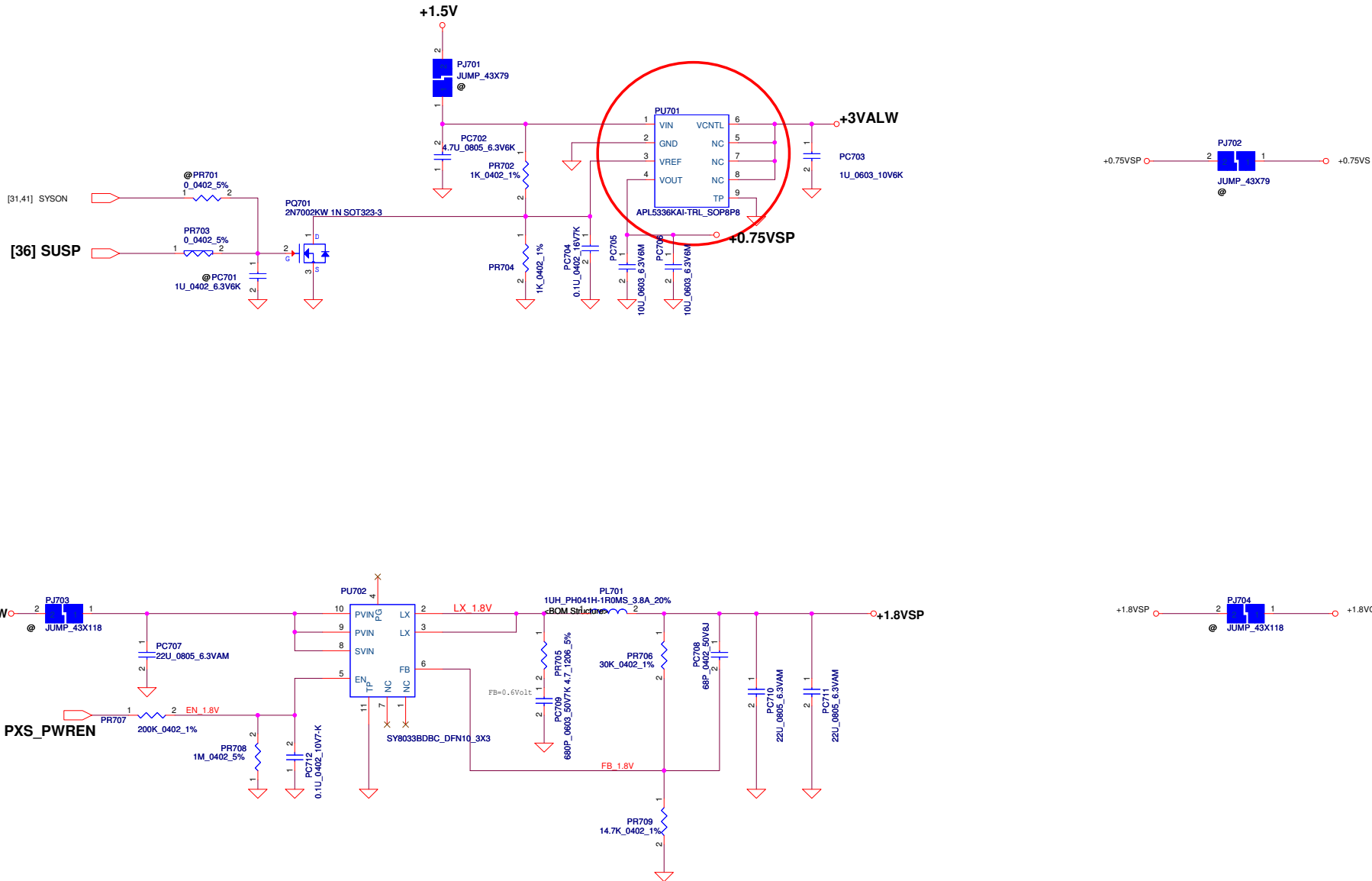


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+1.1VALWP/+1.5VP



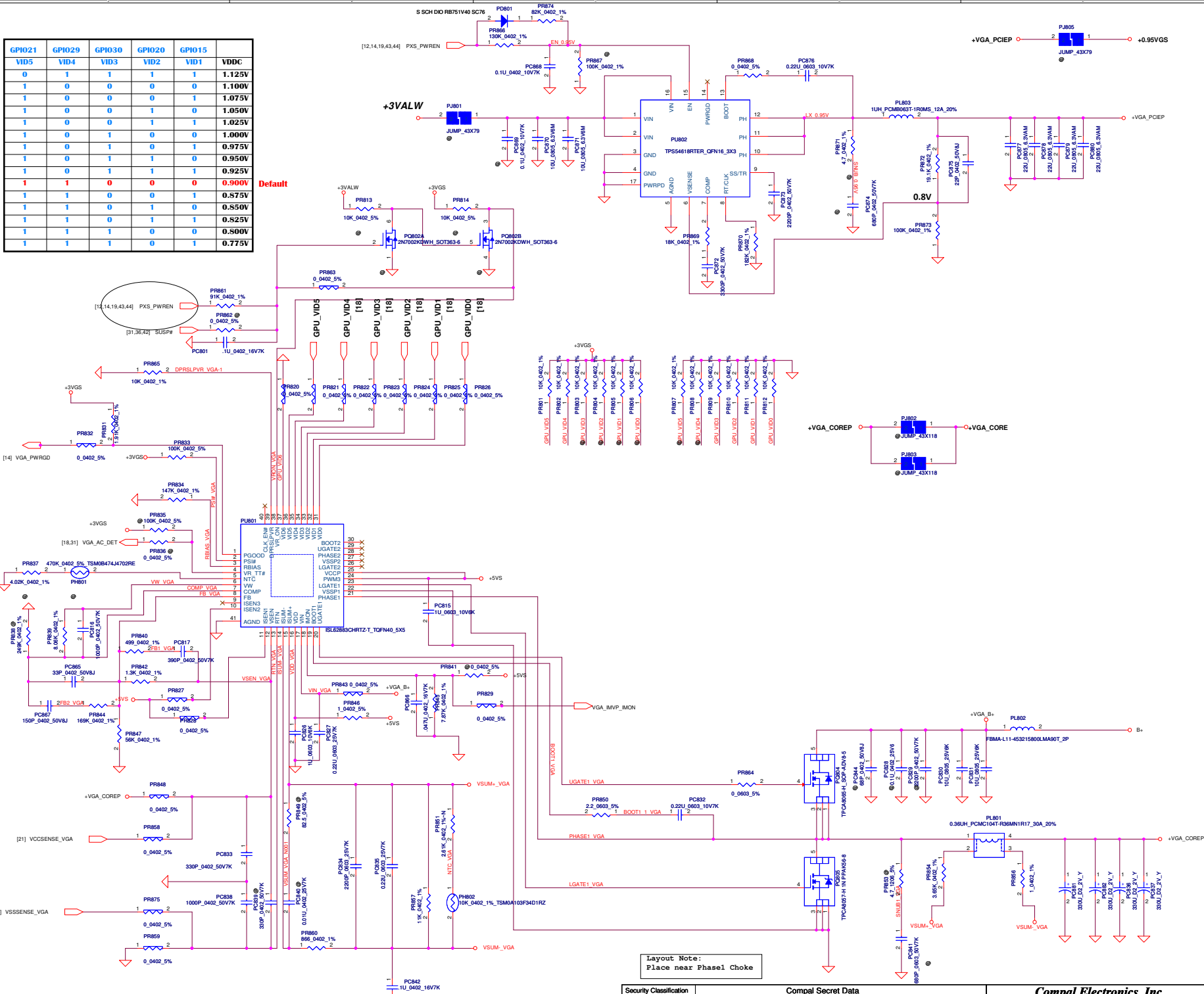
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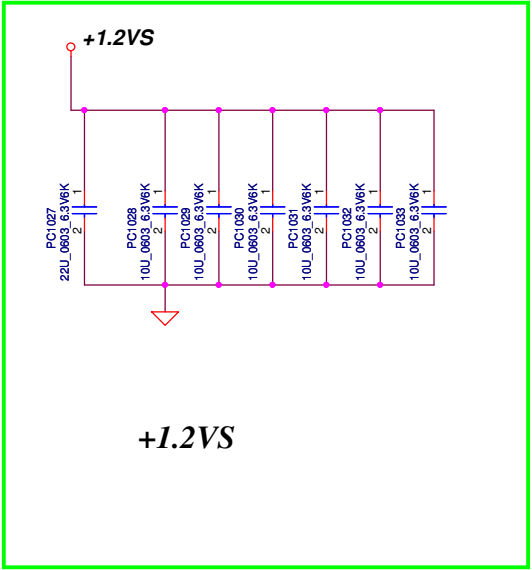
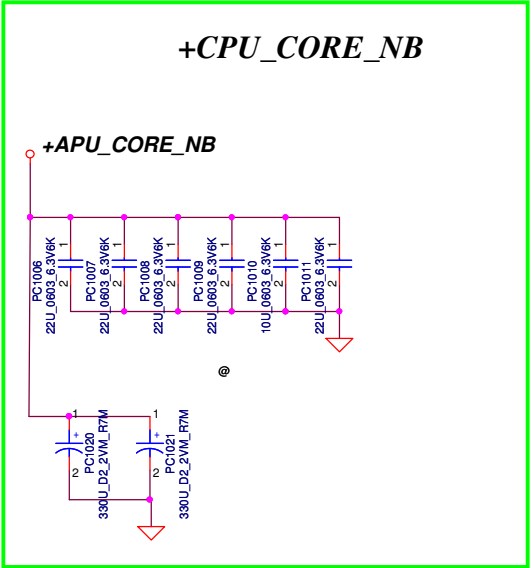
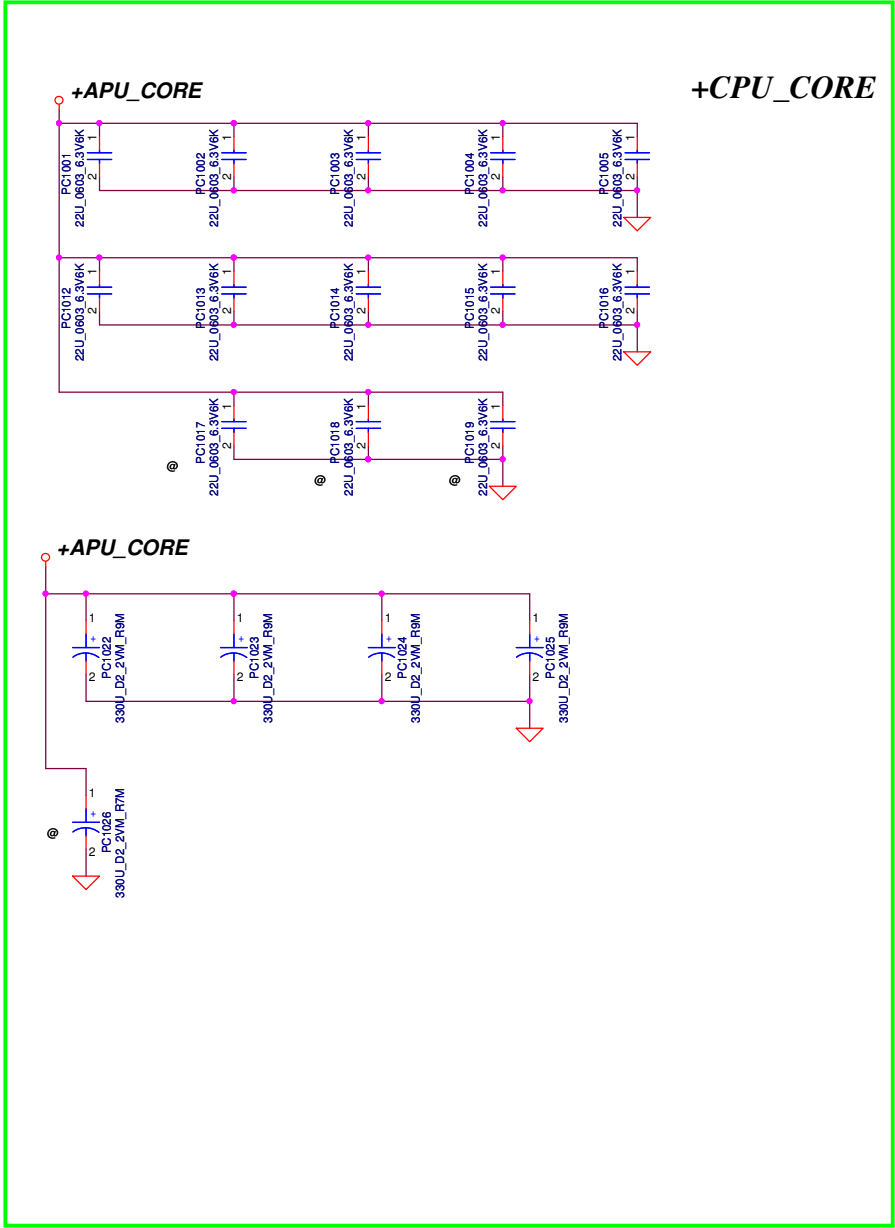
GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	VDDC
VID5	VID4	VID3	VID2	VID1	
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default



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Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Base on EE's request for fine tune power sequence.	P44	Change PR866 from 2.49k to 130k.	2013.1.11	From 0.1 to 0.2
2	For fine tune OCP set up point of VGA core.	P44	Change PR860 from 604ohm to 866ohm.	2013.1.11	From 0.1 to 0.2
3	Base on EE's request for fine tune power sequence.	P44	Change PR861 from 47k to 91k.	2013.1.11	From 0.1 to 0.2
4	Base on must meet EUP spec, change power design.	P37	Remove PR110, PC108, PR114, PC109, PR109, PC107, PU101, PR111, PD101, PR138, PR116, PR112, PD105, PR125, PR128, PC114, PR129, PQ101, PD104, PR123, PR124, PC115, PR131, PC117, PR103, PR104, PR105, PD102, PQ102, PR106, PR107, PQ103, PQ104, PR108, PR118, PR121, PC113, PR127, PQ106, PQ105, PR120, PR115, PC110, PC112, PR126, PR119, PR122, PD103.	2013.1.11	From 0.2 to 0.3
5	Base on must meet EUP spec, change power design.	P39	Remove PQ315, PR328, PR329, PQ316, PD304, PD301, PD302, PQ303, PR303, PR304, PQ306, PQ309.	2013.1.11	From 0.2 to 0.3
6	Base on must meet EUP spec, change power design.	P39	Add PR336, PR338, PR337, PR339, PQ319.	2013.1.11	From 0.2 to 0.3
7	Base on must meet EUP spec, change power design.	P40	Remove PR417, PC420, PQ407, PR420, PC424. Add PR411. Change PR418 from 47K to 2.2K.	2013.1.11	From 0.2 to 0.3
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							5	4	3	2	1
Phase	Date	No.	BOM	Sch	Layout	Description					
SDV/FVT	2012/11/22	No.1	V	V	V	Page 5, Delete for Sun Pro M2 C17,C18,C19,C20,C21,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C32 Delete PCIE_CRX_GTX_P8~15 PCIE_CTX_C_GRX_P8~15 PCIE_CTX_GRX_P8~15 PCIE_CRX_GTX_N8~15 PCIE_CTX_C_GRX_N8~15 PCIE_CTX_GRX_N8~15					
SDV/FVT	2012/11/22	No.2	V	V	V	Page 17, Delete for Sun Pro M2 C1400,C1417,C1418,C1419,C1420,C1421,C1422,C1423,C1424,C1425,C1426,C1427,C1428,C1429,C1430,C1431 Delet PCIE_CRX_C_GTX_P8~15 PCIE_CRX_C_GTX_N8~15					
SDV/FVT	2012/11/22	No.3	V	V	V	Page 17 ,U1401 change Part Number from SA000047H50 to SA00006BA30 for Sun Pro M2					
SDV/FVT	2012/11/22	No.4	V	V	V	Page 24, Delete for Sun Pro M2 no Channel B C1621,C1622,C1623,C1624,C1625,C1626,C1627,C1628,C1629,C1630,C1631,C1632,C1633,C1634,C1635,R1462,R1463 C1636,C1637,C1638,C1639,C1640,C1641,C1642,C1643,C1644,C1645,C1646,C1647,C1648,C1649,C1650,R1464,R1465 C1651,C1652,C1653,C1654,C1655,C1656,C1657,C1658,C1659,C1660,C1661,C1662,C1663,C1664,C1665,C1569 C1666,C1667,R1504,R1504,R1505,R1505,R1506,R1507,R1508,R1509,R1510,R1510,R1511,R1511,R1512,C1570 R1513,R1514,R1515,R1516,R1517,R1518,R1519,R1520,R1521,R1522,R1523,R1524,R1525,R1526,R1527,U1409,U1410,U1411,U1412					
SDV/FVT	2012/11/22	No.5		V	V	Page 19, Reserved Tl406,Tl407 for Sun Pro M2					
SDV/FVT	2012/11/22	No.6	V	V	V	Page 18, Reserved D1401 for Sun Pro M2 PX5.5					
SDV/FVT	2012/11/22	No.7	V	V	V	Page 19, Delete PX4.0 and PX5.0 schematic C1459,C1460,C1461,C1462,C1463,D1400,Q1401,Q1402,Q1403A,Q1403B,Q1404,Q1405,Q1406,R1401,R1438,R1439,,R1440, R1442,R1460,R1461,U1402,U1403					
SDV/FVT	2012/11/22	No.8	V	V	V	Page 20, Delete DGPU Display Power not need reserved C1472,C1473,C1474,C1475,C1477,C1478,C1479,C1480,C1481,C1482,C1483,C1484,C1487,C1488					
SDV/FVT	2012/11/22	No.9	V	V	V	Page 20, L1405 change Part Number from SM010009U00 to SM01000AX00 for Sun Pro M2 Spec Suggetion 120 to 220 ohm					
SDV/FVT	2012/11/22	No.10	V	V	V	Page 20, Delete R1457,R1458 ,Because the Sun Pro M2 AW28,AW18 are NC.					
SDV/FVT	2012/11/22	No.11	V	V	V	Page 20, Delete Thames&Seymour reserved R1407,R1408,R1409,R1410,R1411,R1412,R1413,R1414,R1415,R1416,R1417,R1466,R1467,R1468,R1469,R1471					
SDV/FVT	2013/1/10	No.12	V	V	V	Page 12 U2 change Part Number from SA000066K10 to SA000066K60					
SDV/FVT	2013/1/10	No.13		V	V	Page 31, for Power Eulot 6 modfiy Delete net FSTCHG,BATT_LEN#					
SDV/FVT	2013/1/11	No.14	V	V	V	Page 18, for fine tune VGA Power saving Stuff C1441					
SDV/FVT	2013/1/11	No.15	V	V	V	Page 19, for fine tune VGA Power Sequence R1445 change value from 20K to 470K R1446 change value from 20K to 10K					

Phase	Date	No.	BOM	Sch	Layout	Description
SIT	2013/1/10	No.1	v	v	v	Page 35, for Power Eulot 6 modfiy Un-Stuff @ Q2408,R2463
SIT	2013/1/10	No.2	v	v	v	Page 33, for Touch Pad Module requirment Stuff R2470
SIT	2013/2/1	No.3	v	v	v	Page 07, for APU_SID and APU_SIC voltage smothly Stuff C69
SIT	2013/2/1	No.4	v	v	v	Page 26, for Logo LED brightness change Resistor Valve from 4.99K to 1.6K
SIT	2013/2/20	No.5		v	v	Page 36, for delete Discharge circuit ,remove R2324,Q2314,R2321,Q2309
SIT	2013/3/05	No.6		v	v	Page 32, for Factory issue ,remove JBT1
SIT	2013/3/12	No.7	v	v	v	Page 25, for cost down ,not need reserved for EC ,non-stuff Q2107,R2177,R2178
SIT	2013/3/12	No.8	v	v	v	Page 36, for customer request , Stuff R2302,R2303,Q2300,Q2302

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