


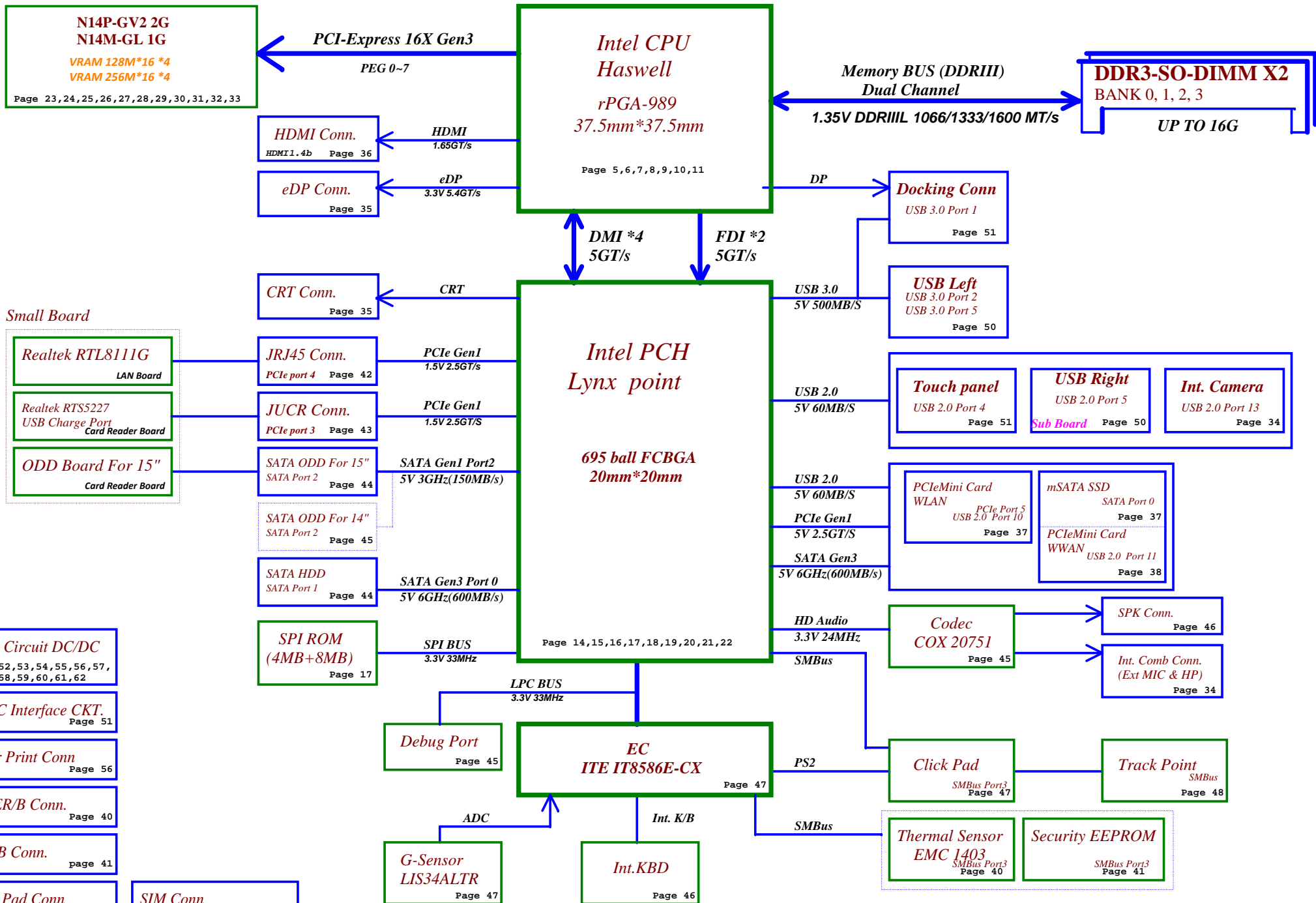
E540

NM-A161 Rev1.0 Schematic

*Intel Haswell Processor with DDRIII + Lynx point PCH
nVIDIA N14P-GV2/ N14M-GL*

2013-07-11 Rev 1.0

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Voltage Rails (0 --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC Only	0	0	X	X
S5 S4 Battery only	0	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
		0	Camera
	XHCI 1	1	USB Port (Right Side)
		2	USB Port (Left Side)
		3	
		4	
		5	USB Port (Right Side)
		6	
		7	
	EHCI 2	8	
		9	
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS sensor support part
8171@	QCA8171 LAN part
8171S@	QCA8171 LAN surge part
SURGE@	QCA8171&8172 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop
EDP@	Support EDP panel function
daul@	Support daul channel panel function

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
PM_SMBCLK PM_SMBDATA	PCH +3V_PCH	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

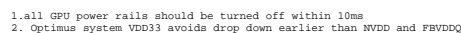
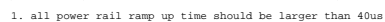


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Title	Notes List	LCFC
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GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	HPD_IRQ


[illegible]

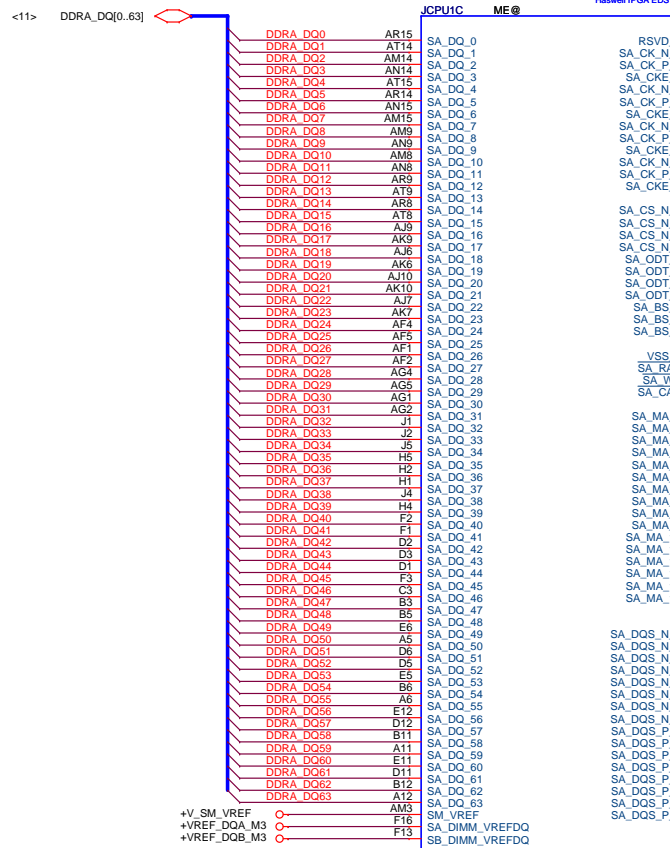
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID		setting	I2C Slave addresses
N13P-GT (28nm)	0x0FDB	SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
			1	0x9C

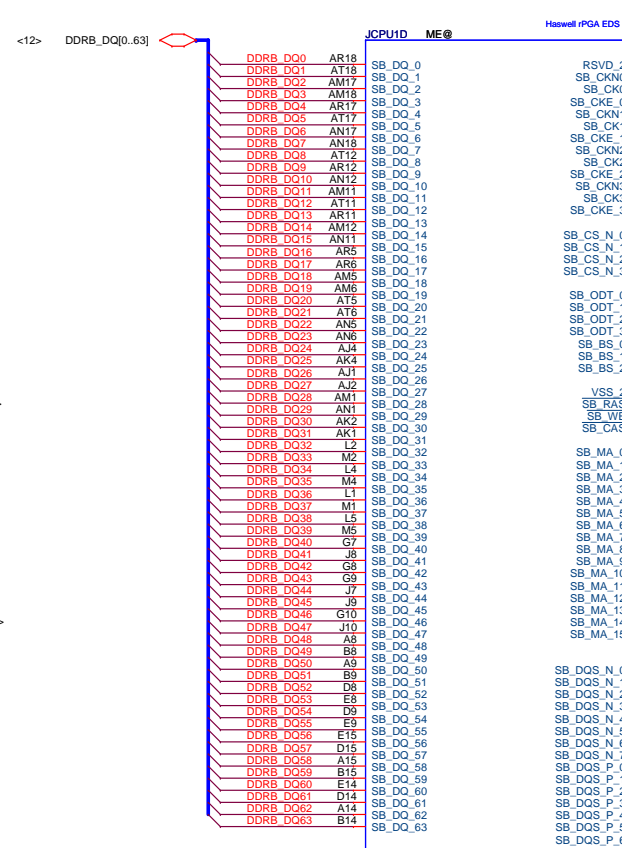
GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N13P-GT		
FB Memory (GDDR5)		ROM_S1		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

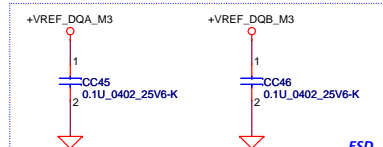
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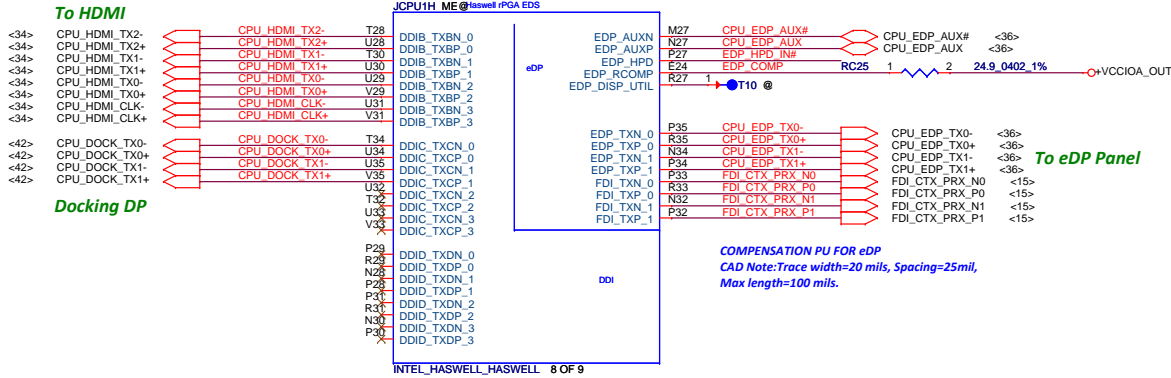
ESD

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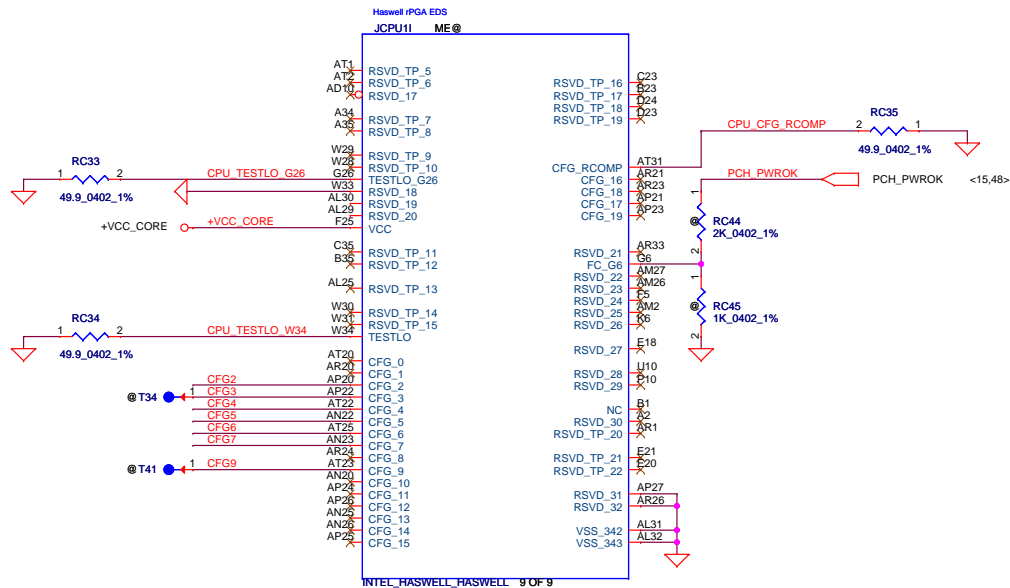


E440 NM-A151

Rev 1.0



CFG STRAPS For CPU (CFG[17:0] internal pull high 5 ~15K to VCCIO)



PEG Static Lane Reversal - CFG2 is for the 16x

CFG2

1: (Default) Normal Operation;
Lane# definition matches socket pin map definition
0: Lane Reversed

Display Port Presence Strap

CFG4

1: Disabled
No Physical Display Port attached to Embedded Display Port
0: Enabled;
An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps

CFG[6:5]

11: Func 1 Disabled, Func 2 Disabled (x16,---,---)
10: Func 1 Enabled, Func 2 Disabled (x8,x8,---)
01: Func 1 Disabled, Func 2 Enabled
00: Func 1 Enabled, Func 2 Enabled (x8,x4,x4)

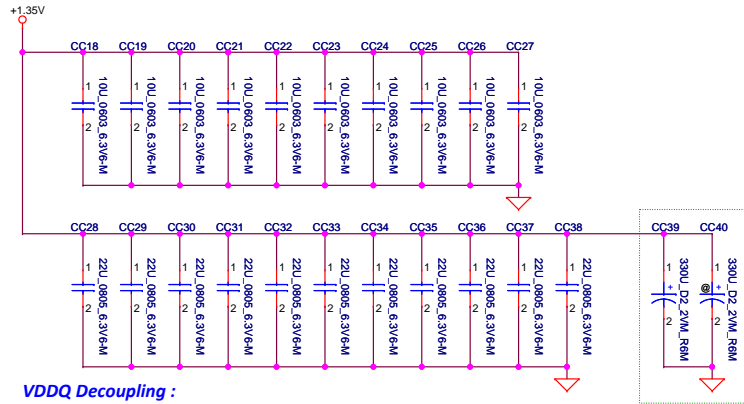
PEG DEFER TRAINING

CFG7

1: (Default)
PEG Train Immediately Following XXRESETB Deassertion
0: PEG Wait for BIOS for Training

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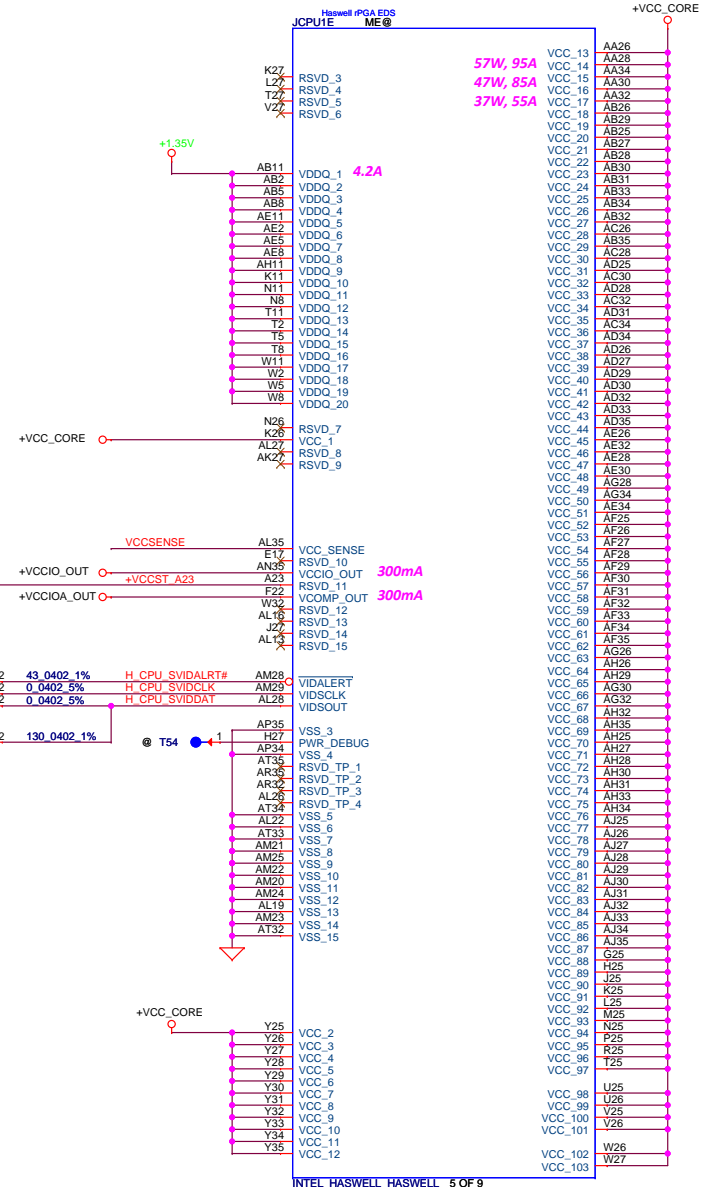
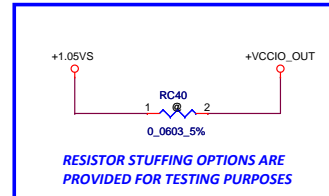
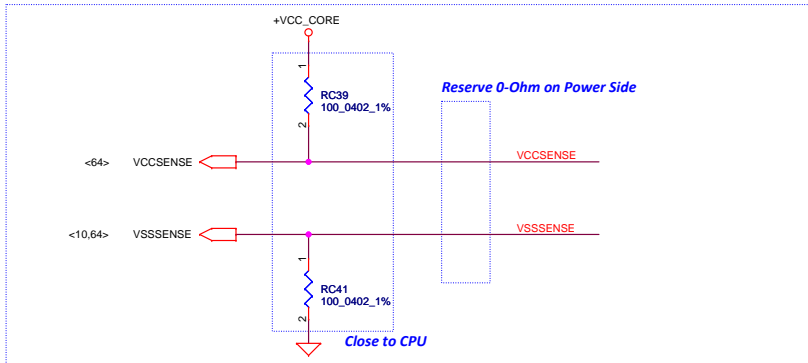
CPU VDDQ DECOUPLING



VDDQ Decoupling :

1. MB Bottom Socket Edge --> 2* 330uf, 6mΩ
2. 6x MB Bottom Socket Cavity --> 11* 22 μF (0805), 3mΩ
5x MB Top Socket Cavity
3. 5x MB Bottom Socket Cavity --> 10 x 10 μF (0805), 3mΩ
5x MB Top Socket Cavity

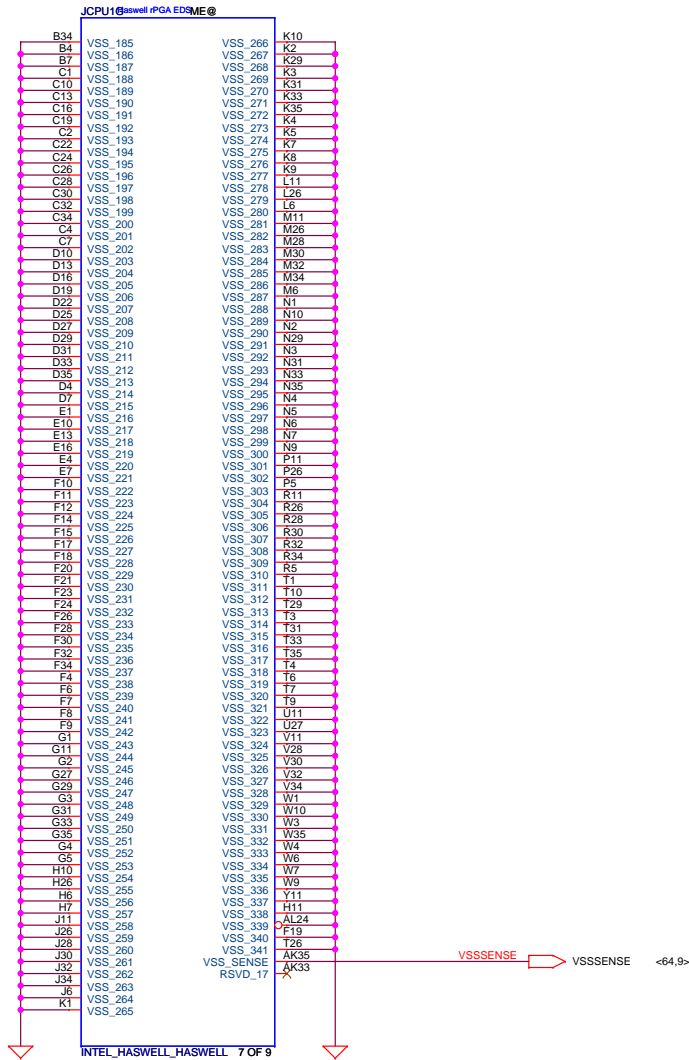
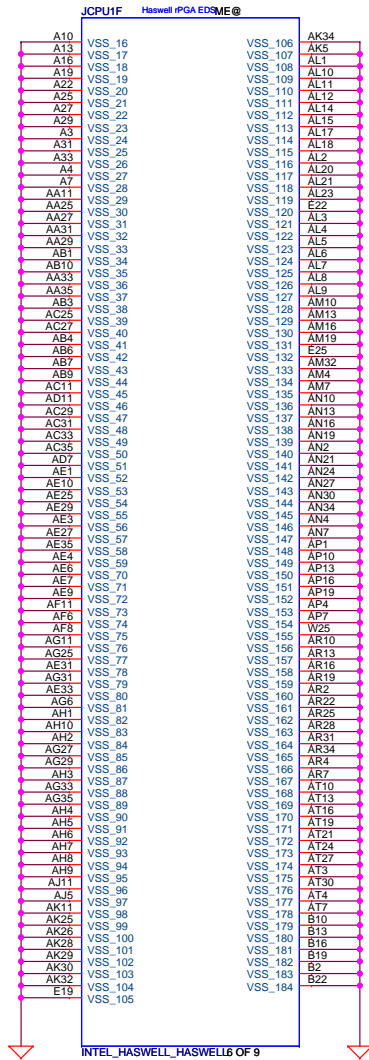
VCC/VSS SENSE



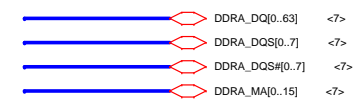
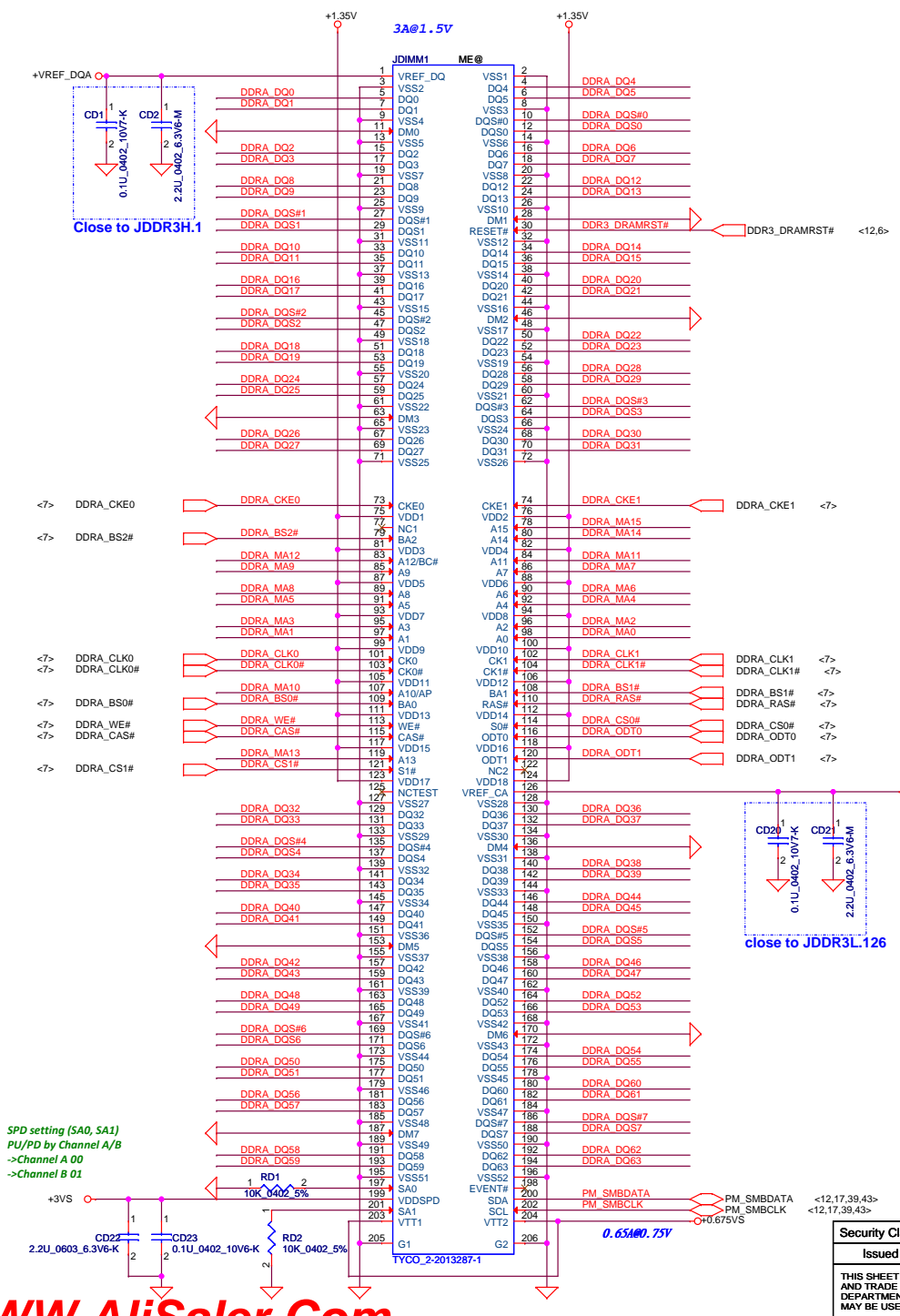
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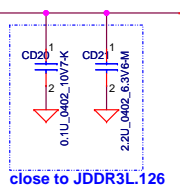
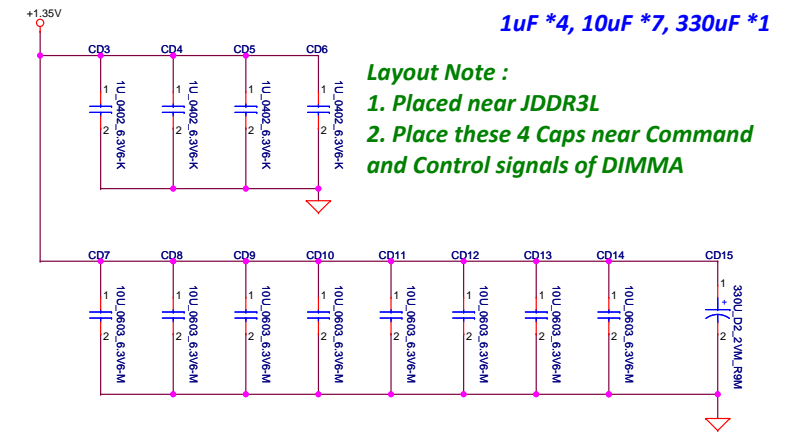




DDR3 SO-DIMM A







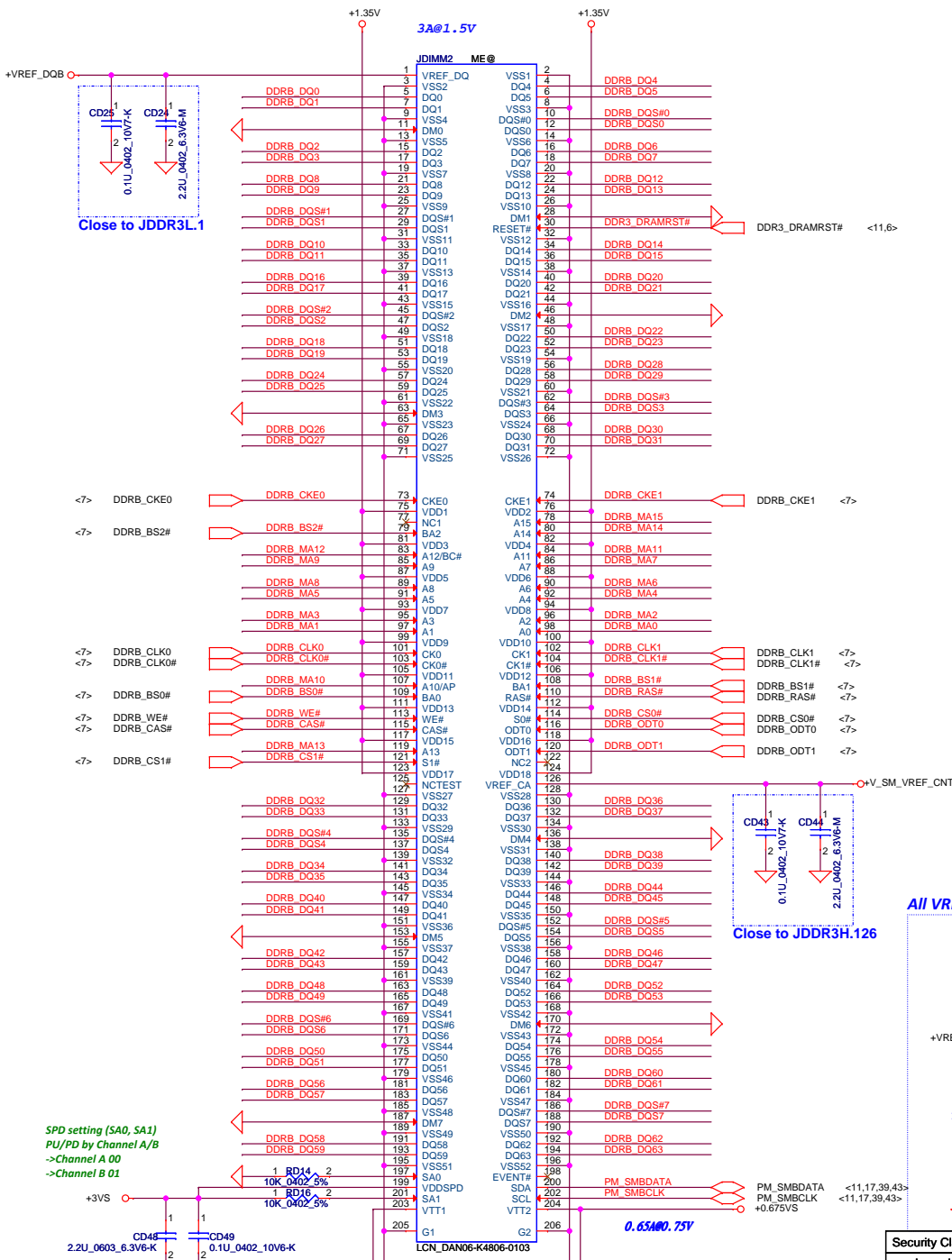
DDR Decoupling



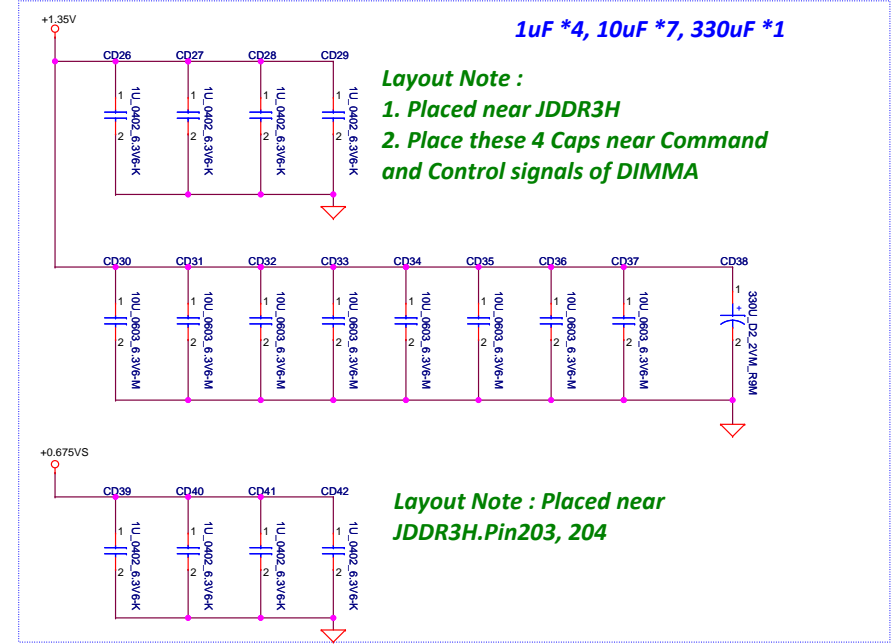
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DDR3 SO-DIMM B

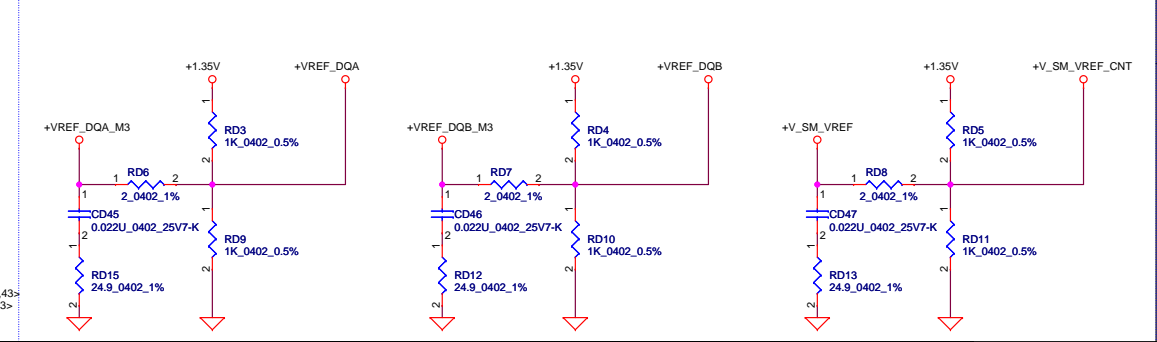
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 DDRB_DQS[0..7] <7>
 DDRB_DQS#0..7 <7>
 DDRB_MA[0..15] <7>



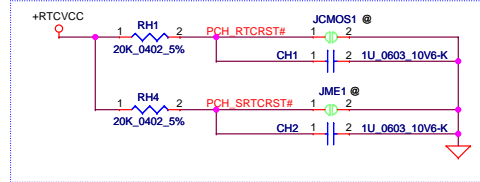
DDR Decoupling



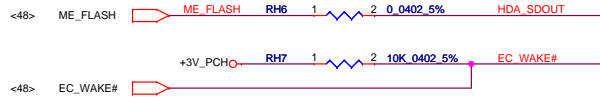
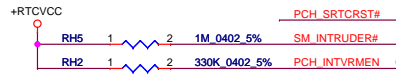
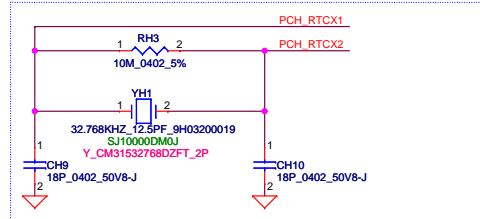
All VREF traces should have 20 mil trace width



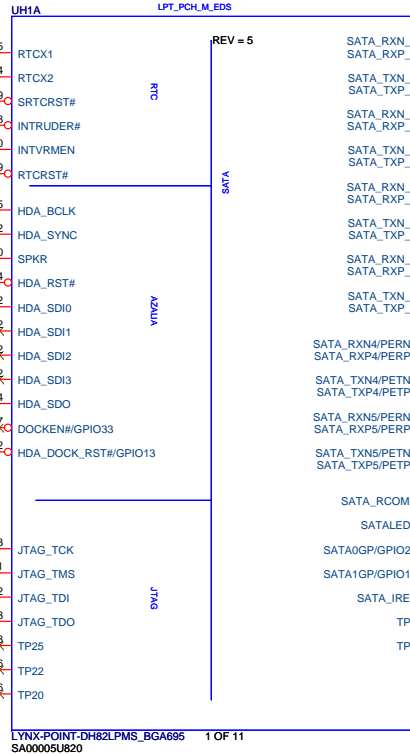
JCMOS, JME Setting, Need Under DDR Door



1. INTVRMEN, should always be pull high
H : Integrated VRM enable (Default)
L : Integrated VRM disable
2. Internal Voltage Regulator Enable:
This signal enables the internal 1.05 V regulators.

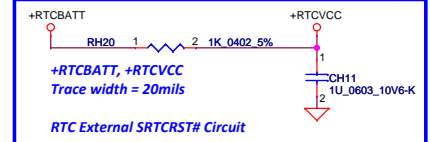


During Reset", Immediately after Reset and S3/S4/S5
1. JTAG_TDI, JTAG_TMS --> Int. PU 20K
2. JTAG_TCK --> Int. PD 20K
3. JTAG_TDO --> High-Z



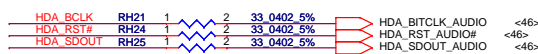
SATA Impedance Compensation :
--> Place the resistor within 500 mils of the PCH.
Avoid routing next to clock pins.

RTCVCV Circuit

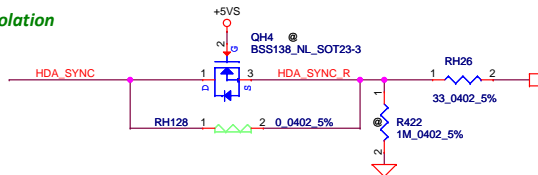


HDA AUDIO SIGNAL

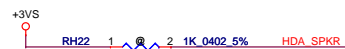
HDA AUDIO For Codec



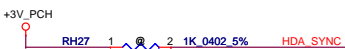
Isolation



HDA STRAP



- * HIGH= Enable (No Reboot)
- * LOW= Disable (Default)
- 1. The internal pull-down is disabled after PLTRST# deasserts.
- 2. When Sampled : Rising edge of PWROK

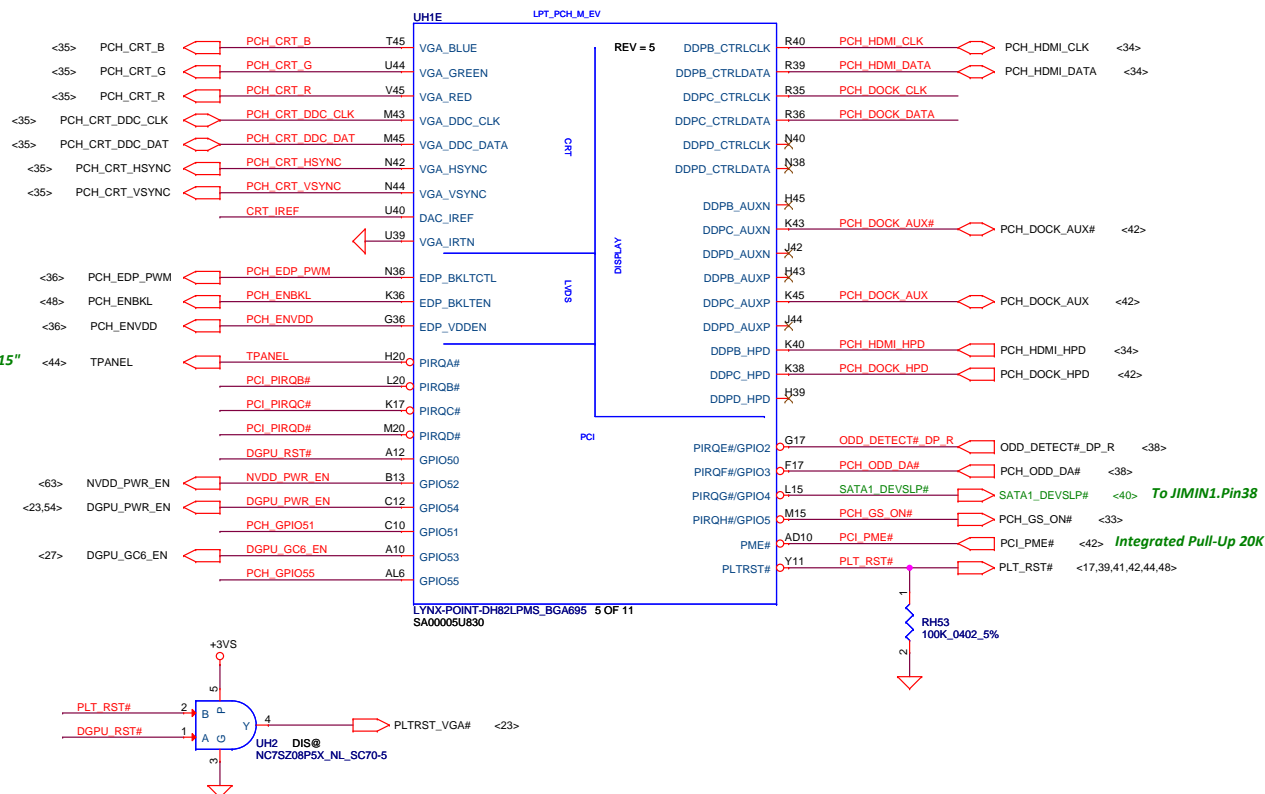
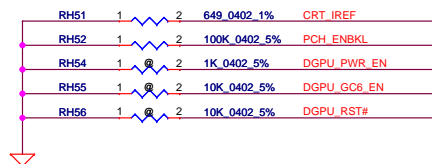


- 1. This signal has a weak internal pull-down 15K
- 2. The internal pull-down on AZA_SYNC and AZA_SDO are enabled during reset.

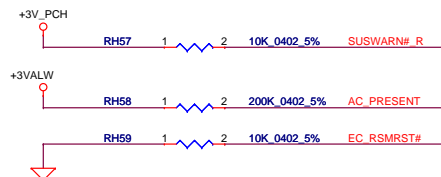
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Title	Size	Document Number	Rev
PCH_RTC/HDA/SATA	Custom	E440 NM-A151	1.0
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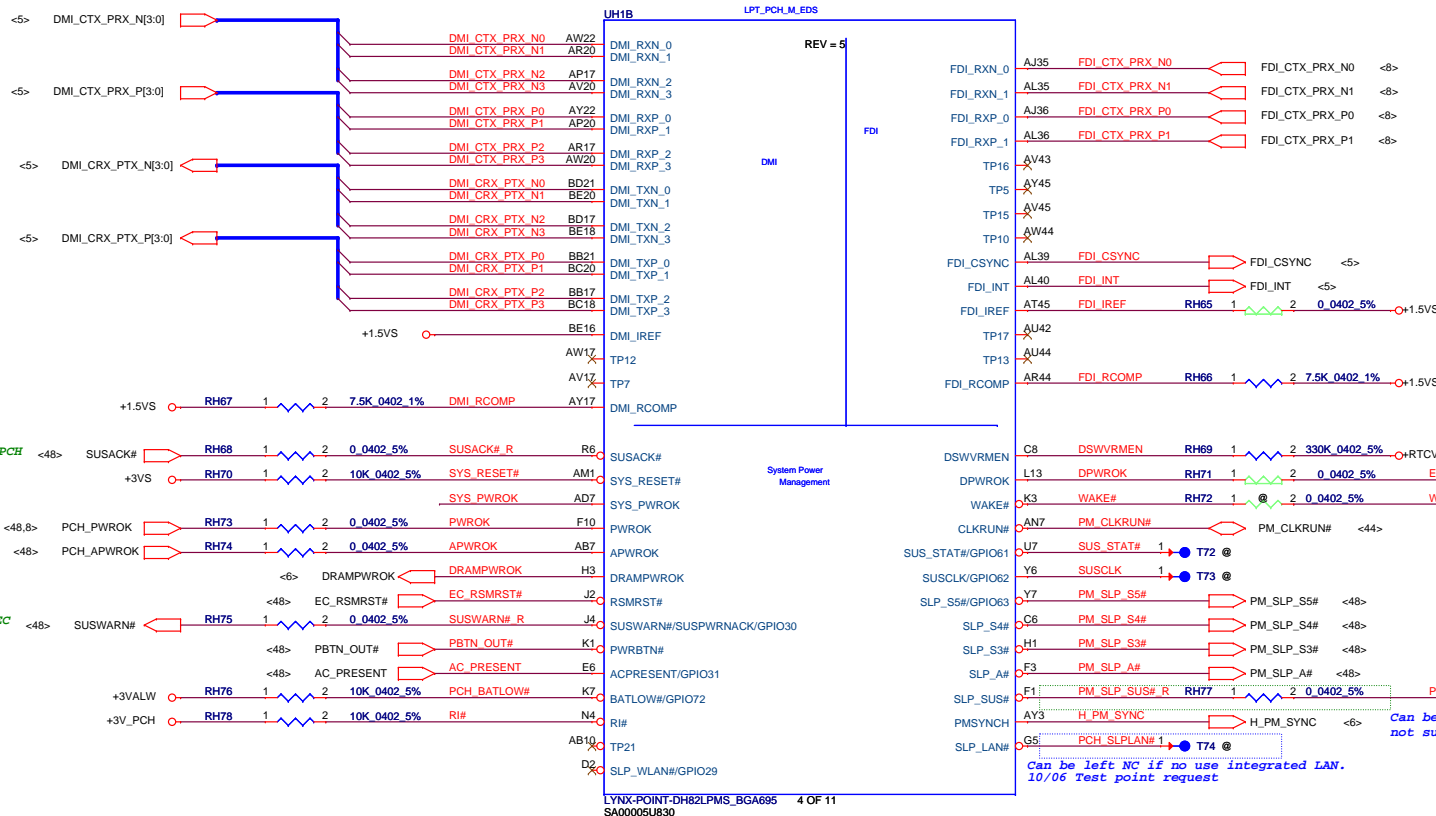
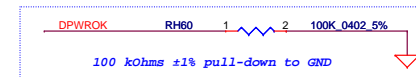
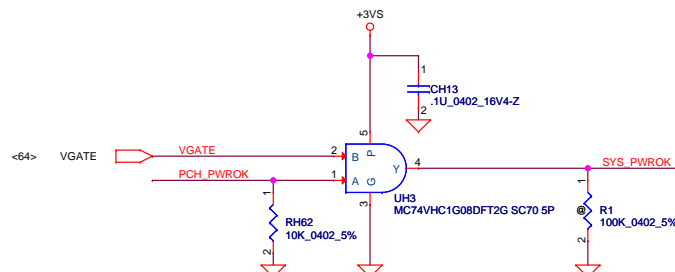




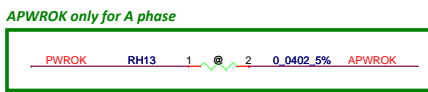
WWW.AliSaler.Com



SUSACK# R RH61 1 0.0402 5% SUSWARN# R
 Stuff RH289 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit

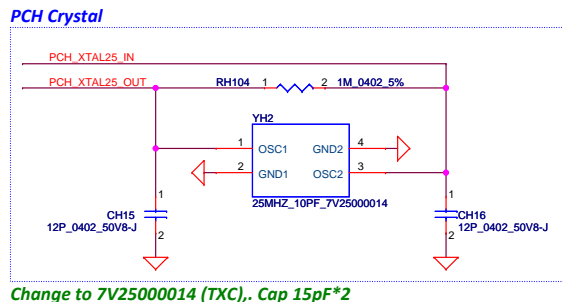
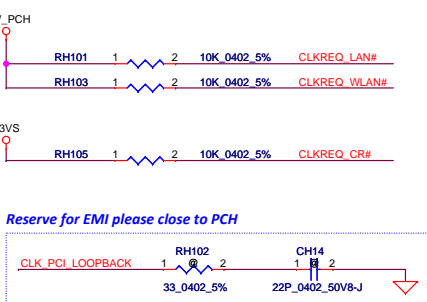
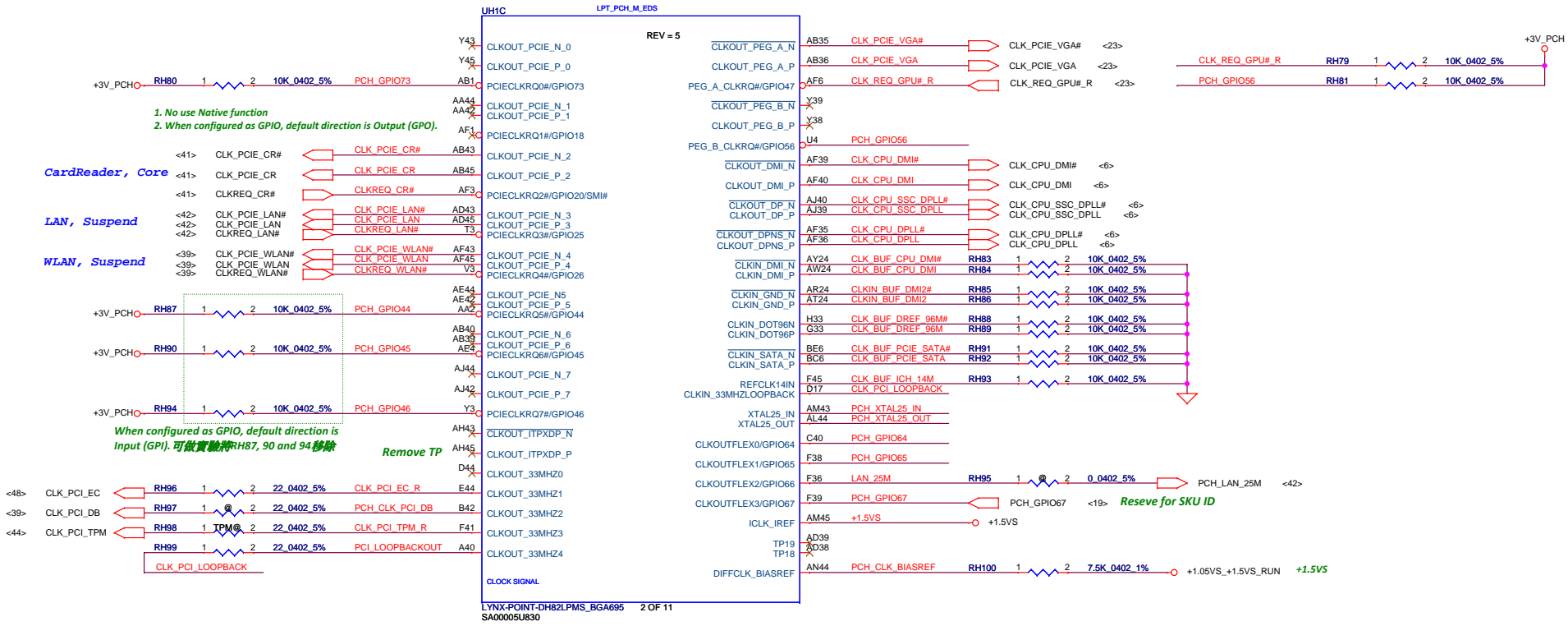


DSWVRN must be always pulled high to +RTCVCC
 DSWVRN - Internal Deep Sleep 1.05V regulator
 ***H : Enable
 L : Disable

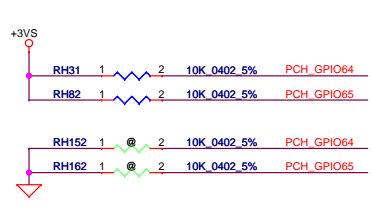


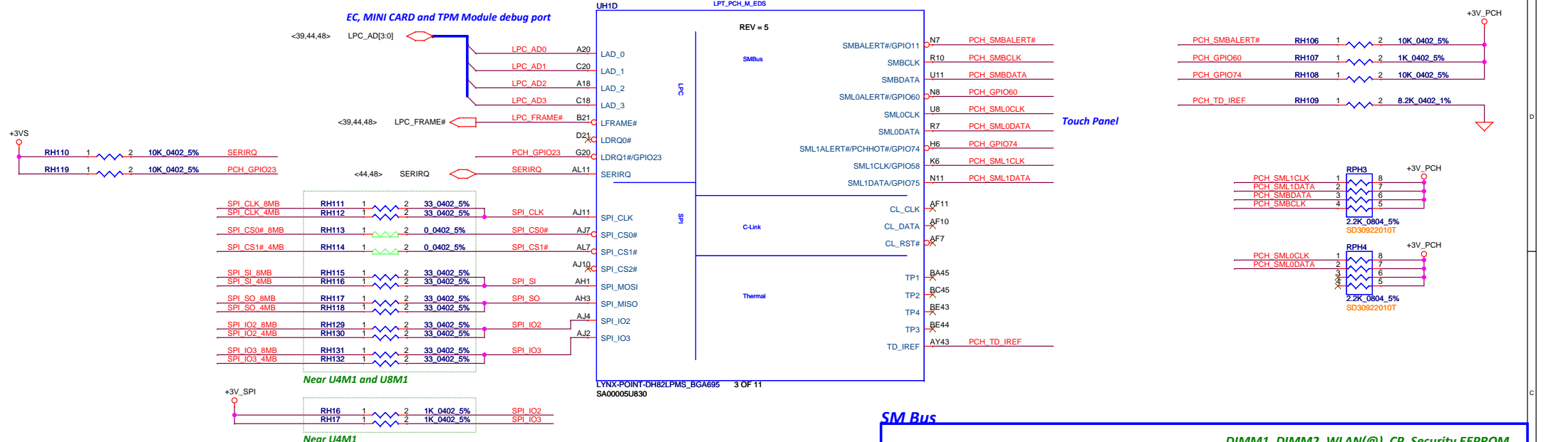
SUSCLK#/GPIO62
 This signal has a weak internal pull-up.
 0 = Disable PLL On-Die voltage regulator.
 * 1 = Enable PLL On-Die voltage regulator.
 NOTES:
 1. The internal pull-up is disabled after RSMRST# deasserts.
 2. This signal is in the Suspend well.

Security Classification				LC Future Center Secret Data				Title	
Issued Date				2012/12/05				PCH_DMI/FDI/PM	
Deciphered Date				2014/12/05				E440 NM-A151	
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				Sheet				15 of 57	

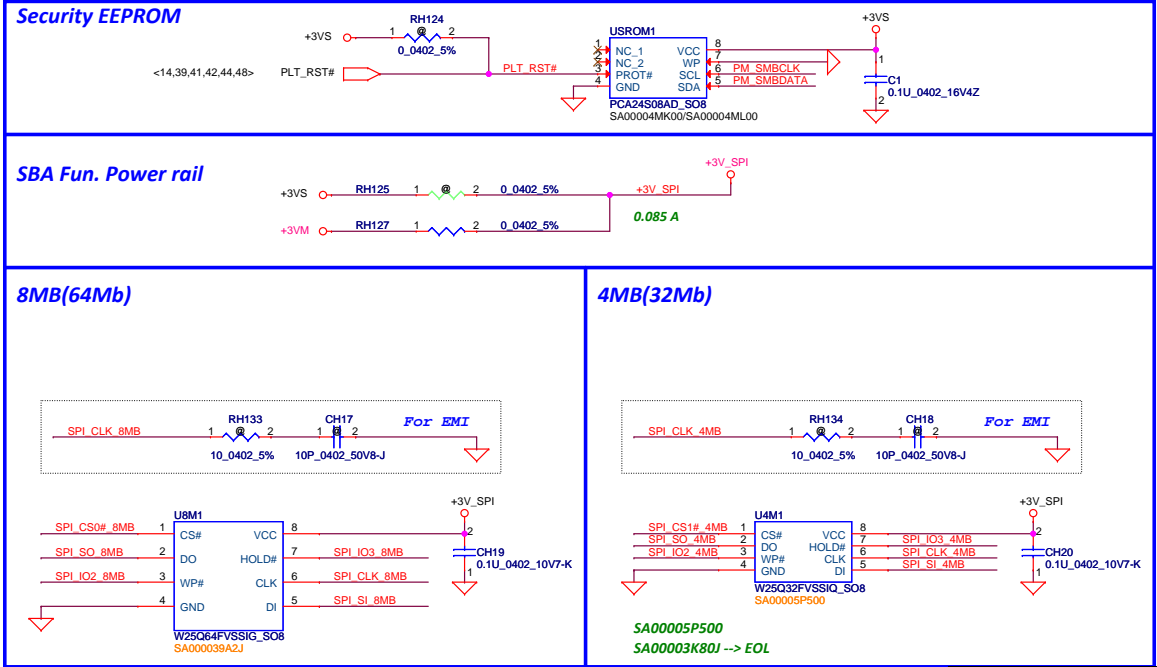


Project Phase ID		
Project Phase	PCH_GPIO64	PCH_GPIO65
SDV, FVT	0	0
SIT2 (R 0.5)	0	1
SIT (R 0.4)	1	0
* SVT	1	1

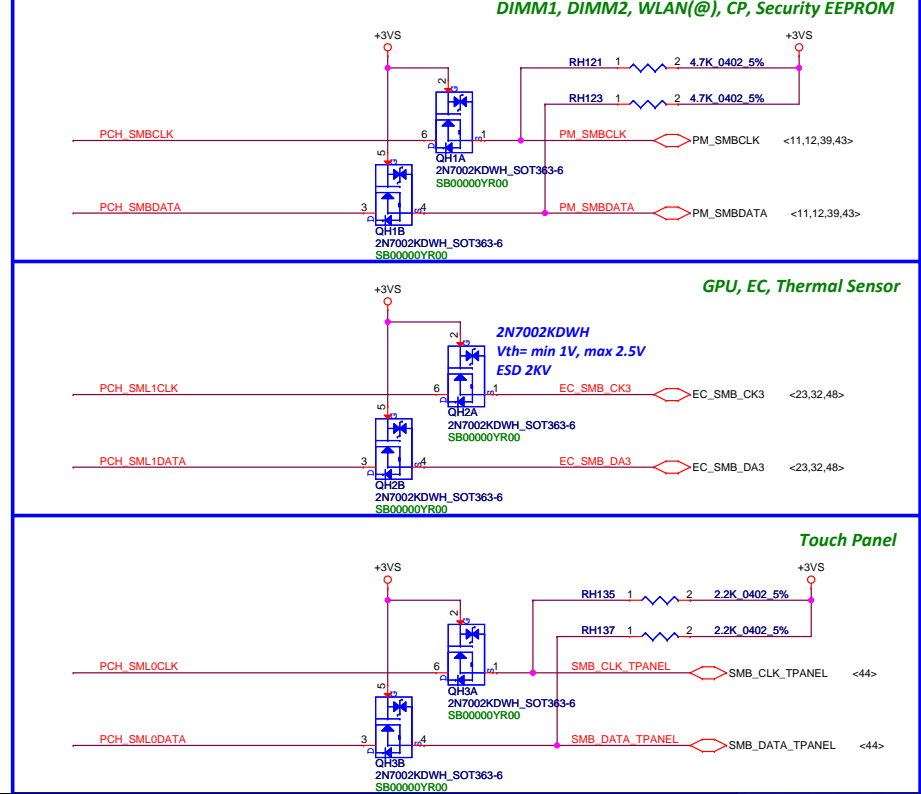




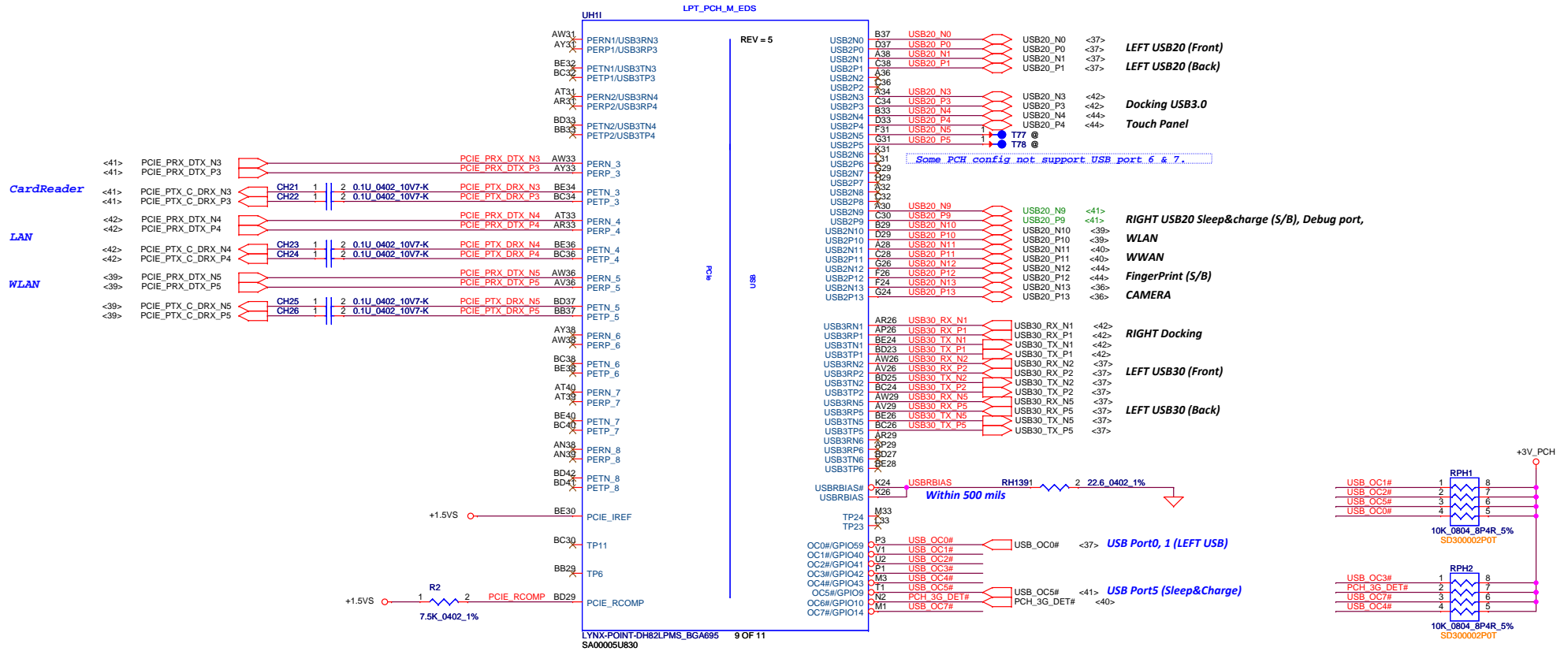
8MB + 4MB SPI ROM, 5MB ME(SBA), Security EEPROM



SM Bus



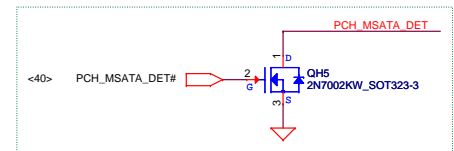
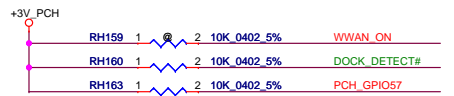
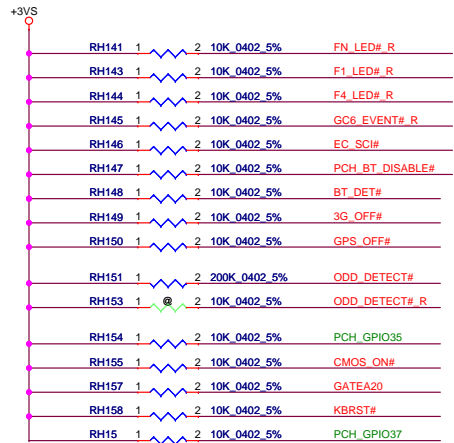
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Issued Date	2012/12/05	Deciphered Date	2014/12/05	PCH_LPC/SPI/SM BUS	
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				Date: Thursday, July 11, 2013	Rev 1.0
				Sheet 17 of 57	



USB2.0 :
OC#0-3 --> Port 0-7
OC#4-7 --> Port 8-13

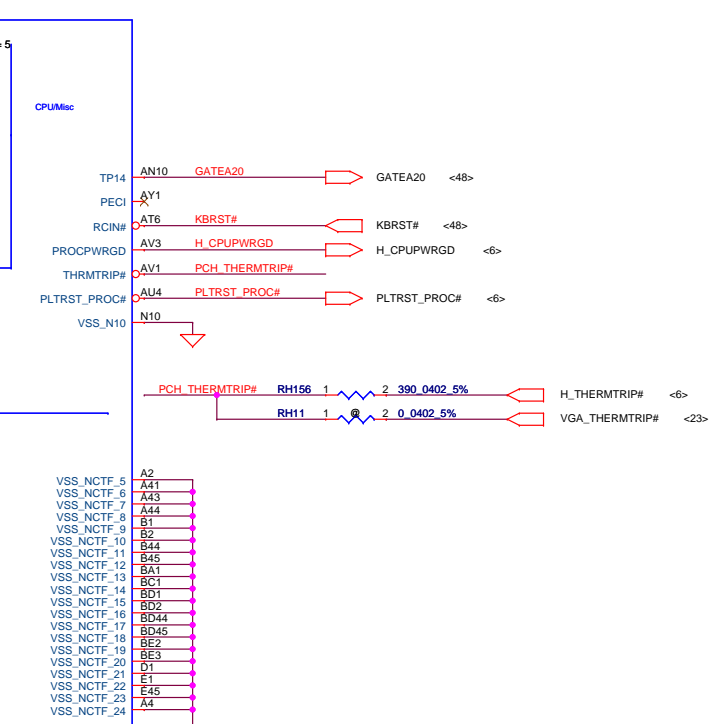
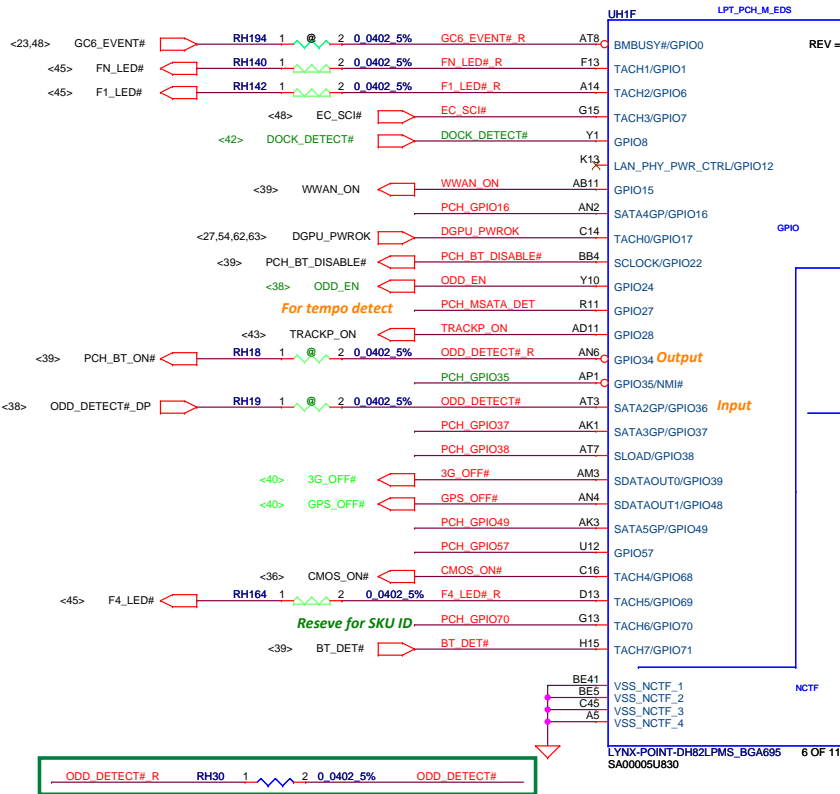
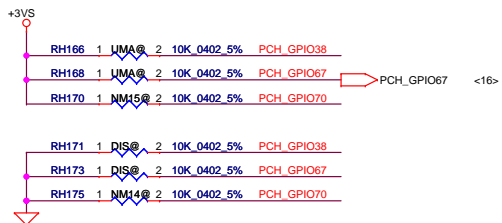
OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.

USB3.0	USB2.0	OC#	Note
Port1	Port3	X	Docking (Right)
Port2	Port0	OC0#	LEFT USB (Front)
Port5	Port1	OC0#	LEFT USB (Back)
X	Port9	OC5#	Sleep&Charge (Right)

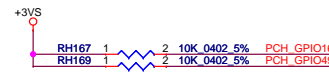


SKU ID

Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
* Optimus	0	0	
Reserve	0	1	
DIS	1	0	
* UMA	1	1	
* 14"			0
* 15"			1

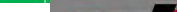


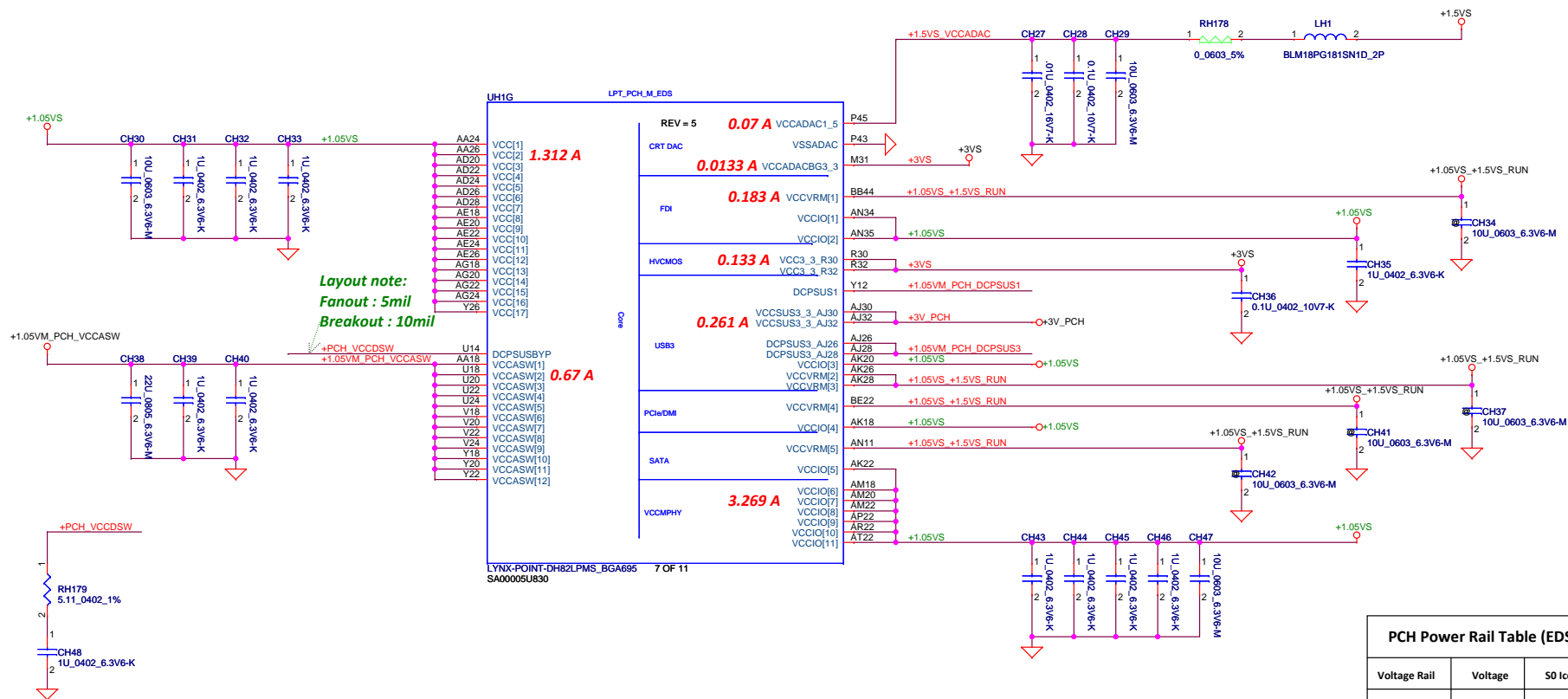
CONFIG	GPIO16, 49
* USB X4,PCIEX8,SATAx6	11
USB X6,PCIEX8,SATAx4	01



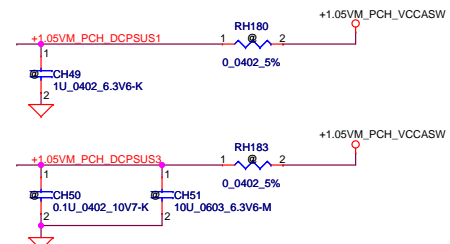
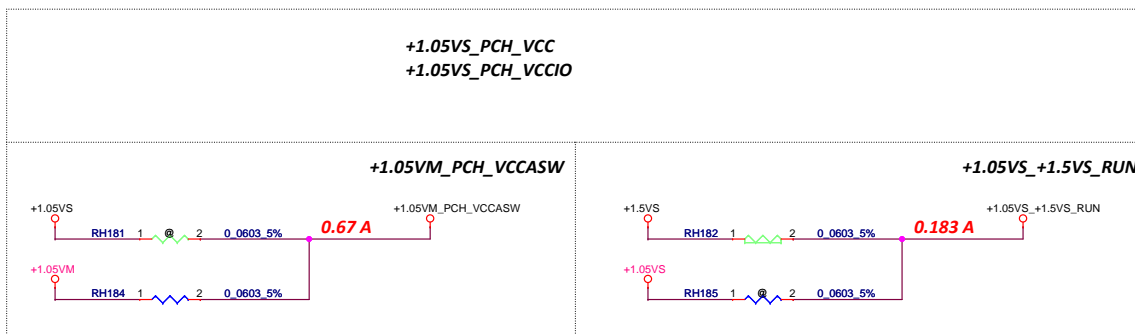
No use Flexible I/O pin, delete RH172, RH174

Fixed Signals				Muxed Signals		Fixed Signals								Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1	PCIE 2	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4	SATA 5	SATA 0	SATA 1	SATA 2	SATA 3		
				(00)	(00)							(00)	(00)						
				USB3 3	USB3 4							PCIE 1	PCIE 2						
				(01)	(01)							(01)	(01)						

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Issued Date		2012/12/05		Deciphered Date		2014/12/05				PCH_GPIO/CPU-MISC	
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Size		Custom		Document Number		E440 NW-A151					
Date:		Thursday, July 11, 2013				Sheet		19 of 57			

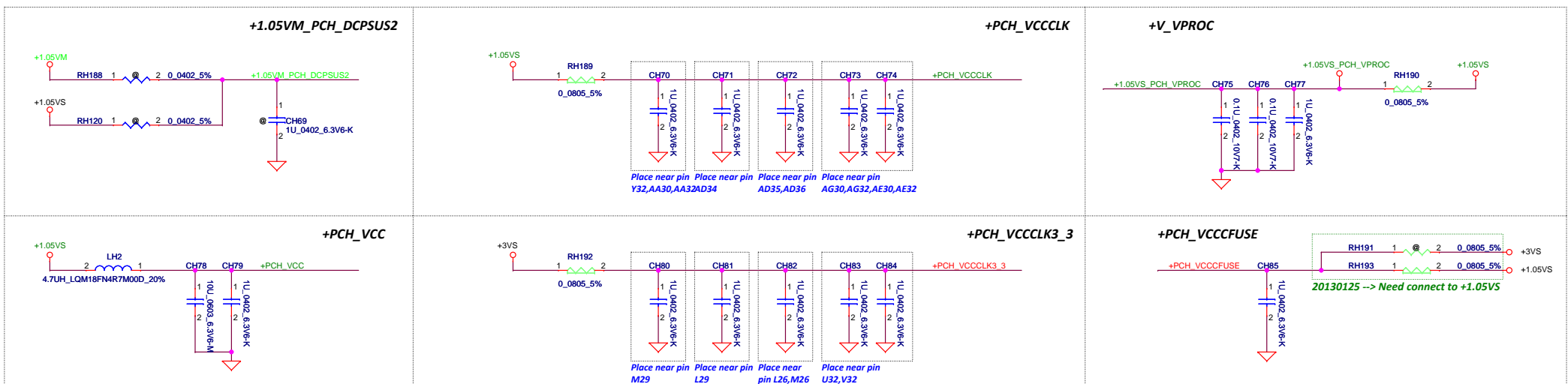
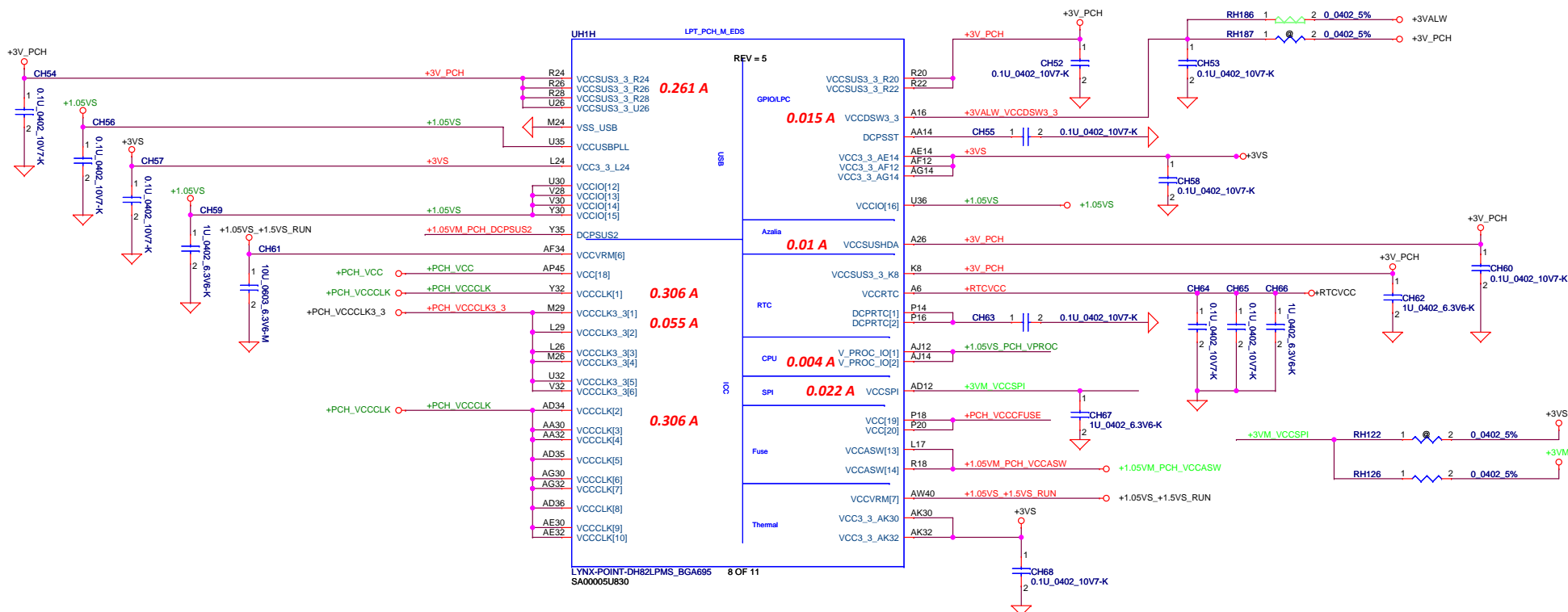


PCH Power Rail Table (EDS Rev1.0)		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.312 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.07 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.183 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

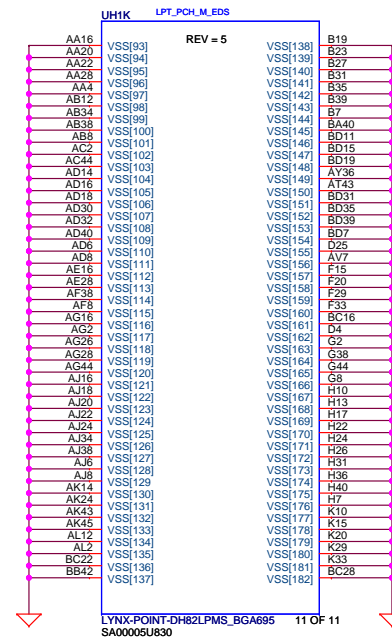
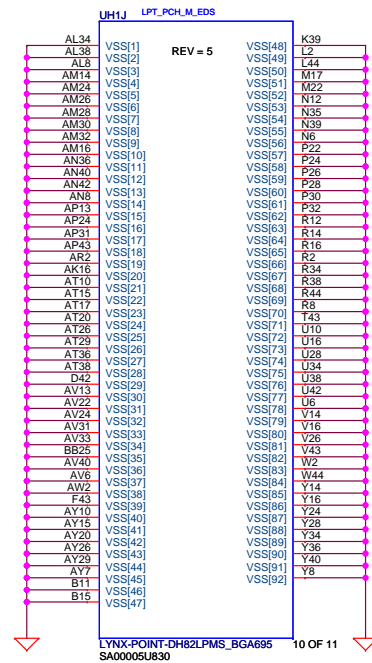


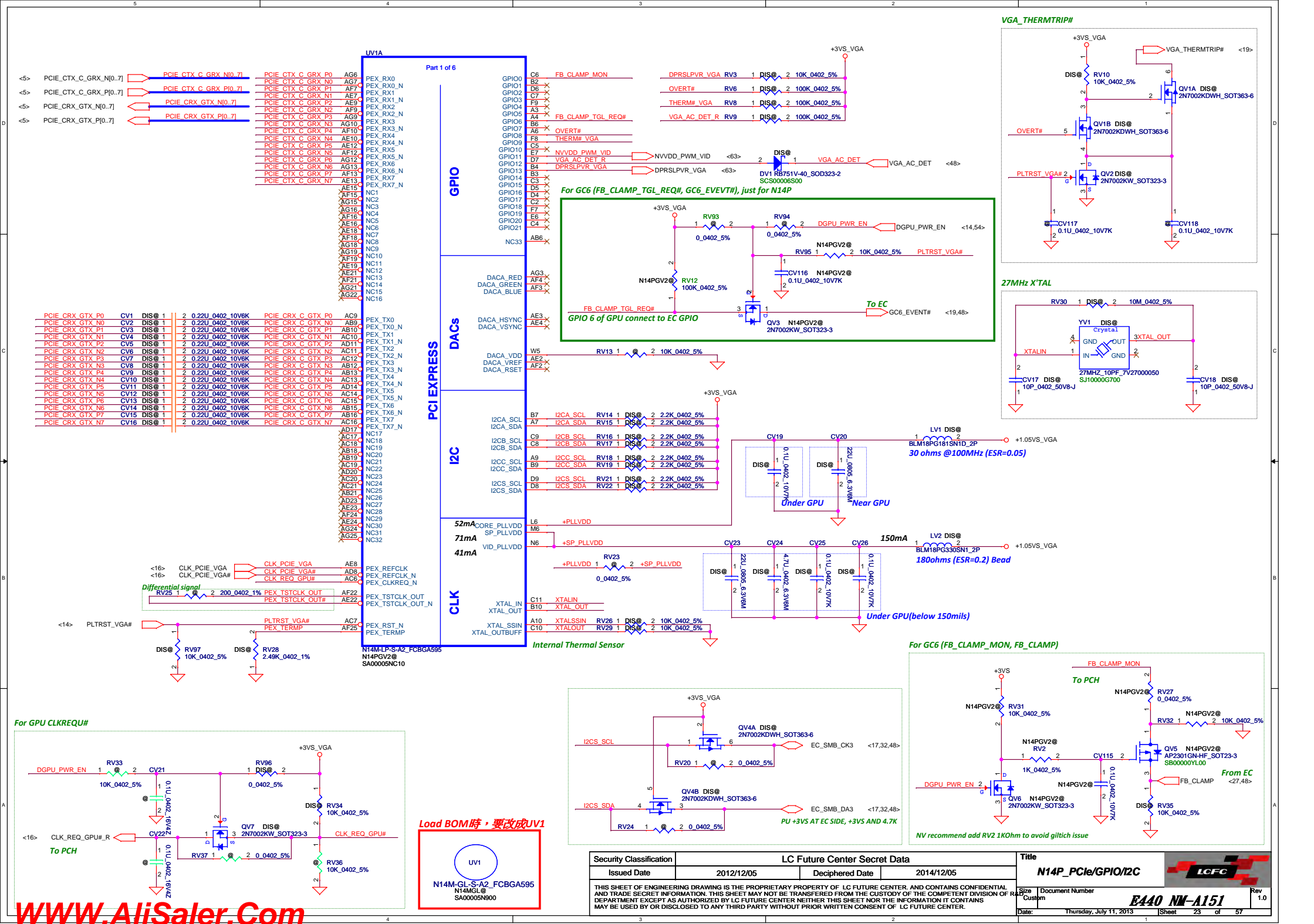
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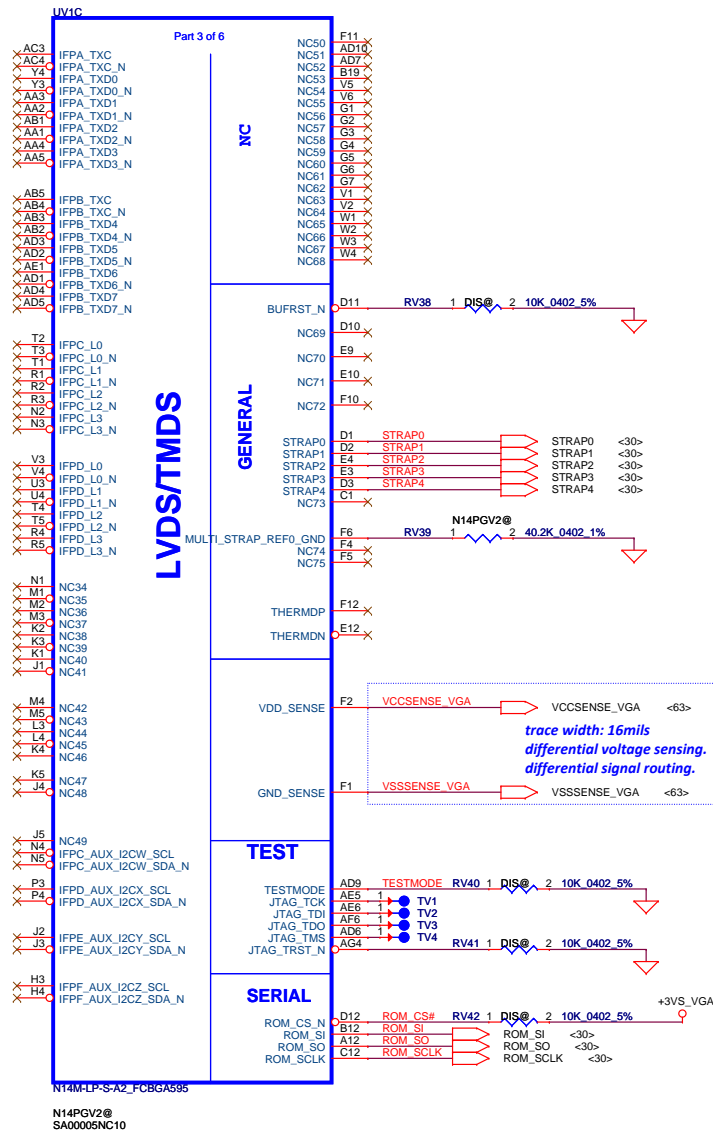
Title	Size	Document Number	Date	Thursday, July 11, 2013	Sheet	20	of	57
PCH_POWER-1	Custom	E440 NM-A151	Rev	1.0				

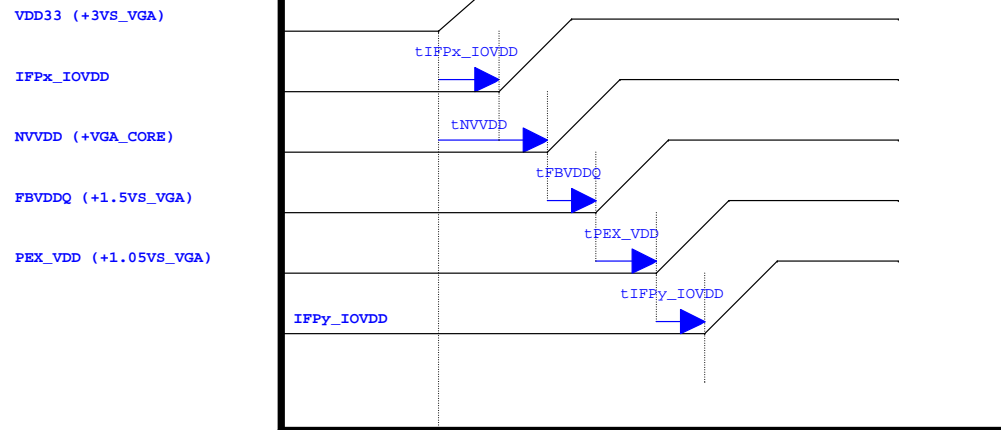
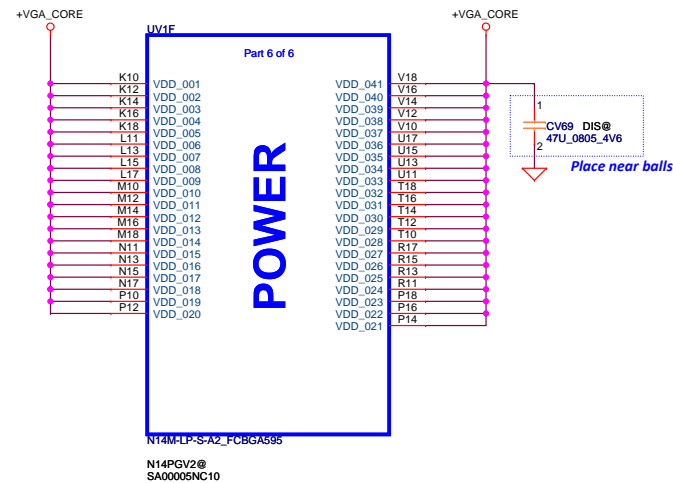
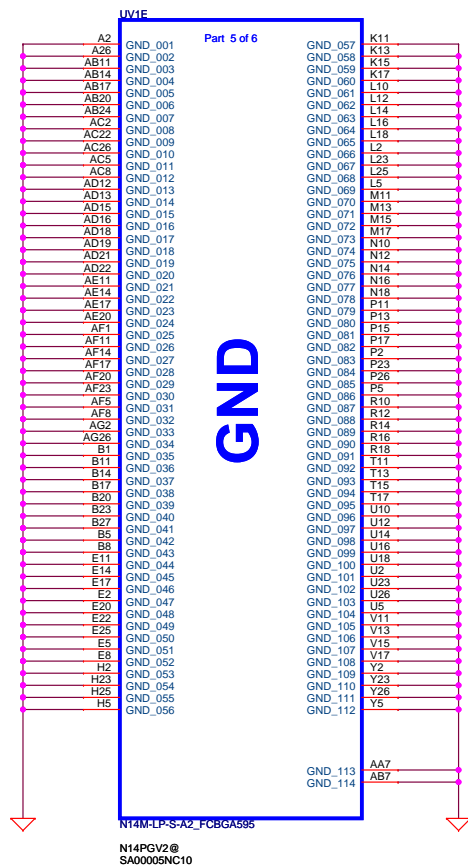


LC Future Center Secret Data				Title	
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				Sheet	21 of 57










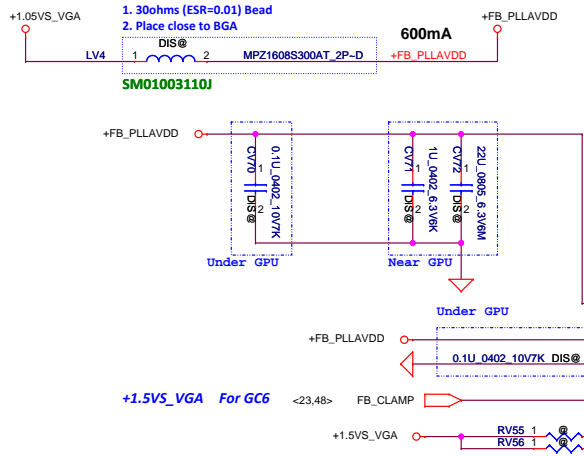
NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F

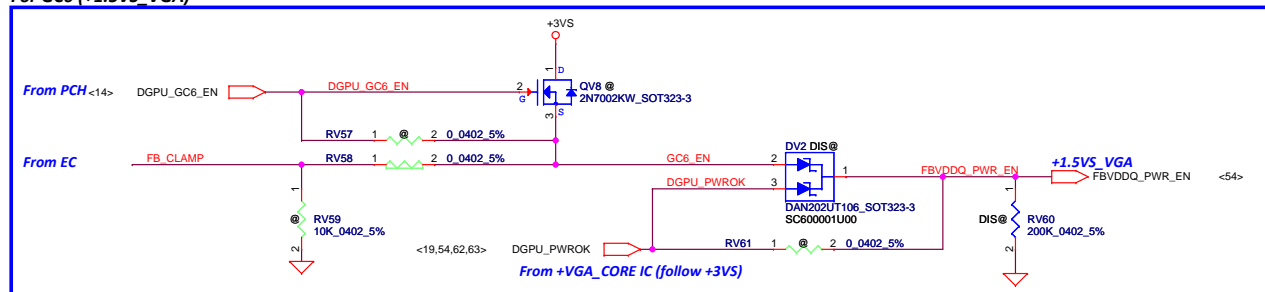
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Issued Date	2012/12/05	Deciphered Date	2014/12/05	N14P_VDD/GND	
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<28,29> FBA_D[0..63] FBA_D[0..63]
 <28,29> FBA_DQM[7..0] FBA_DQM[7..0]
 <28,29> FBA_DQS[7..0] FBA_DQS[7..0]
 <28,29> FBA_DQS[7..0] FBA_DQS[7..0]

FBA_MA[15..0] FBA_MA[15..0] <28,29>
 FBA_BA[2..0] FBA_BA[2..0] <28,29>



For GC6 (+1.5V_VGA)



UV18
 Part 2 of 6

FBA_D0 E18 FBA_D00
 FBA_D1 F18 FBA_D01
 FBA_D2 E16 FBA_D02
 FBA_D3 F17 FBA_D03
 FBA_D4 D21 FBA_D04
 FBA_D5 D21 FBA_D05
 FBA_D6 F20 FBA_D06
 FBA_D7 E21 FBA_D07
 FBA_D8 F16 FBA_D08
 FBA_D9 D15 FBA_D09
 FBA_D10 F15 FBA_D10
 FBA_D11 F13 FBA_D11
 FBA_D12 C13 FBA_D12
 FBA_D13 B13 FBA_D13
 FBA_D14 E13 FBA_D14
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 FBA_D16 B15 FBA_D16
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 FBA_D18 A13 FBA_D18
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 FBA_D21 A18 FBA_D21
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 FBA_D24 B24 FBA_D24
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 FBA_D26 A25 FBA_D26
 FBA_D27 A24 FBA_D27
 FBA_D28 A21 FBA_D28
 FBA_D29 B21 FBA_D29
 FBA_D30 C20 FBA_D30
 FBA_D31 C21 FBA_D31
 FBA_D32 R22 FBA_D32
 FBA_D33 R24 FBA_D33
 FBA_D34 T22 FBA_D34
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 FBA_D59 R27 FBA_D59
 FBA_D60 V26 FBA_D60
 FBA_D61 V27 FBA_D61
 FBA_D62 W27 FBA_D62
 FBA_D63 W25 FBA_D63

MEMORY
 INTERFACE A

FBA_CMD0 C27 FBA_CS0#_L <28>
 FBA_CMD1 C26 FBA_ODT_L <28>
 FBA_CMD2 E24 FBA_CKE_L <28>
 FBA_CMD3 F24 FBA_RST# <28,29>
 FBA_CMD4 D27 FBA_MA14
 FBA_CMD5 D26 FBA_MA15
 FBA_CMD6 F25 FBA_MA9
 FBA_CMD7 F26 FBA_MA7
 FBA_CMD8 F23 FBA_MA2
 FBA_CMD9 G22 FBA_MA0
 FBA_CMD10 G23 FBA_MA4
 FBA_CMD11 G24 FBA_MA1
 FBA_CMD12 F27 FBA_BA0
 FBA_CMD13 G25 FBA_WE# <28,29>
 FBA_CMD14 G27 FBA_CAS# <28,29>
 FBA_CMD15 G26 FBA_CS0#_H <29>
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 FBA_CMD17 M23 FBA_CKE_H <29>
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 FBA_CMD22 K26 FBA_MA11
 FBA_CMD23 K22 FBA_MA5
 FBA_CMD24 J23 FBA_BA3
 FBA_CMD25 J25 FBA_BA2
 FBA_CMD26 J24 FBA_BA1
 FBA_CMD27 K27 FBA_MA12
 FBA_CMD28 K25 FBA_MA10
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 FBA_DQM1 D14 FBA_DQM1
 FBA_DQM2 C17 FBA_DQM2
 FBA_DQM3 C22 FBA_DQM3
 FBA_DQM4 P24 FBA_DQM4
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 FBA_DQM6 AA25 FBA_DQM6
 FBA_DQM7 U25 FBA_DQM7
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 FBA_DQS_RN2 A16 FBA_DQS#2
 FBA_DQS_RN3 A22 FBA_DQS#3
 FBA_DQS_RN4 P25 FBA_DQS#4
 FBA_DQS_RN5 W22 FBA_DQS#5
 FBA_DQS_RN6 AB27 FBA_DQS#6
 FBA_DQS_RN7 T27 FBA_DQS#7
 FBA_DQS_WP0 E19 FBA_DQS0
 FBA_DQS_WP1 C15 FBA_DQS1
 FBA_DQS_WP2 B16 FBA_DQS2
 FBA_DQS_WP3 B22 FBA_DQS3
 FBA_DQS_WP4 R25 FBA_DQS4
 FBA_DQS_WP5 W23 FBA_DQS5
 FBA_DQS_WP6 AB26 FBA_DQS6
 FBA_DQS_WP7 T26 FBA_DQS7
 FBA_CLK0 D24 FBA_CLK0# <28>
 FBA_CLK1 D25 FBA_CLK1# <28>
 FBA_CLK2 N22 FBA_CLK1# <29>
 FBA_CLK3 M22 FBA_CLK1# <29>
 FBA_WCK0 D18
 FBA_WCK1 C18
 FBA_WCK2 D17
 FBA_WCK3 D16
 FBA_WCK4 T24
 FBA_WCK5 U24
 FBA_WCK6 V24
 FBA_WCK7 V25

Mode D - Mirror Mode Mapping

Address	DATA Bus
FBx_CMD0	0..31 CS0#_L
FBx_CMD1	CS0#_L
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	ODT_H
FBx_CMD18	CKE_H
FBx_CMD19	A13 A13
FBx_CMD20	A8 A8
FBx_CMD21	A6 A6
FBx_CMD22	A11 A11
FBx_CMD23	A5 A5
FBx_CMD24	A3 A3
FBx_CMD25	BA2 BA2
FBx_CMD26	BA1 BA1
FBx_CMD27	A12 A12
FBx_CMD28	A10 A10
FBx_CMD29	RAS# RAS#

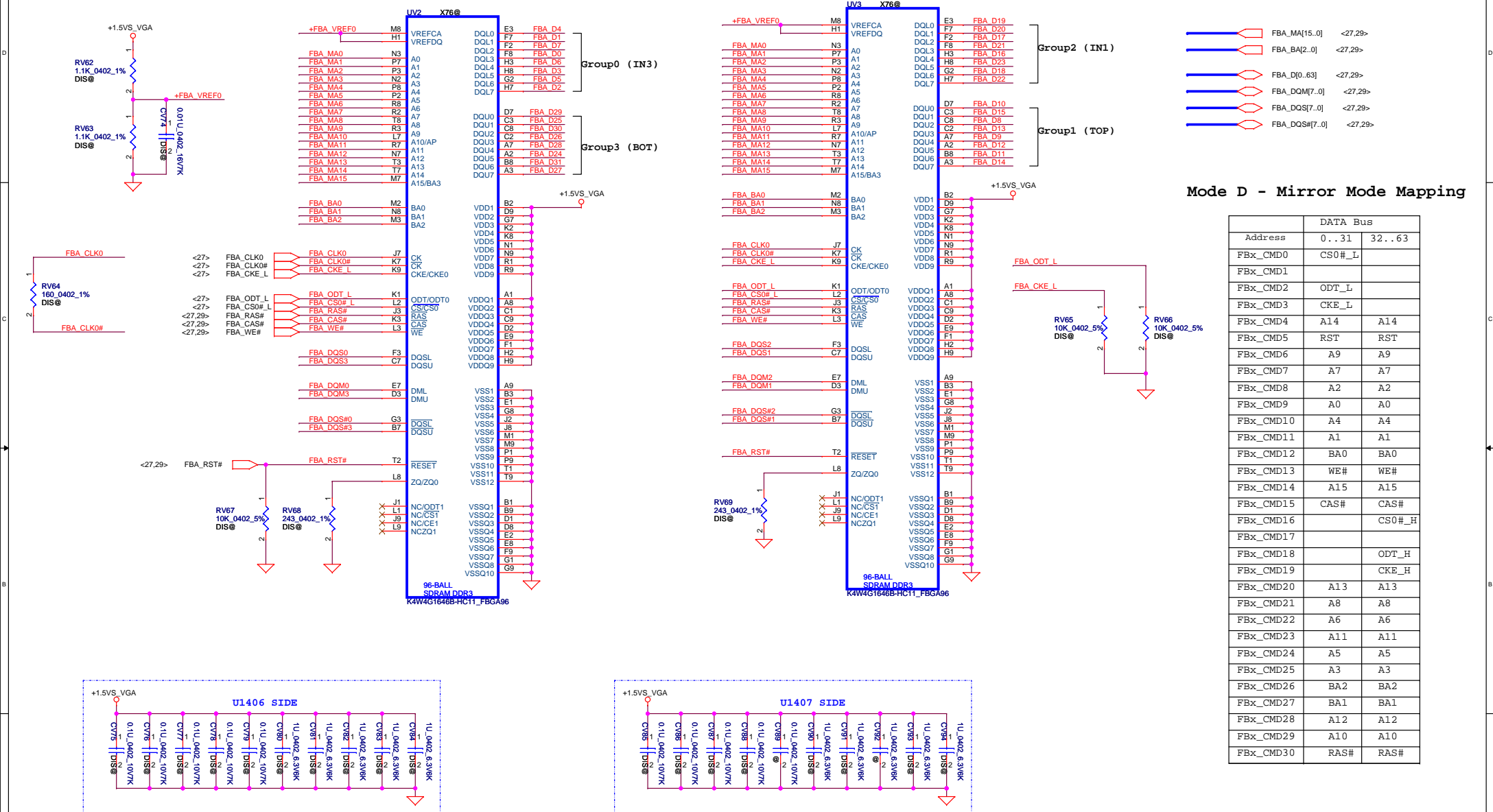
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 Issued Date 2012/12/05 Deciphered Date 2014/12/05
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Title N14P_MEM IF/FB CLAMP
 Size Custom Document Number E440 NM-A151
 Date Thursday, July 11, 2013 Sheet 27 of 57



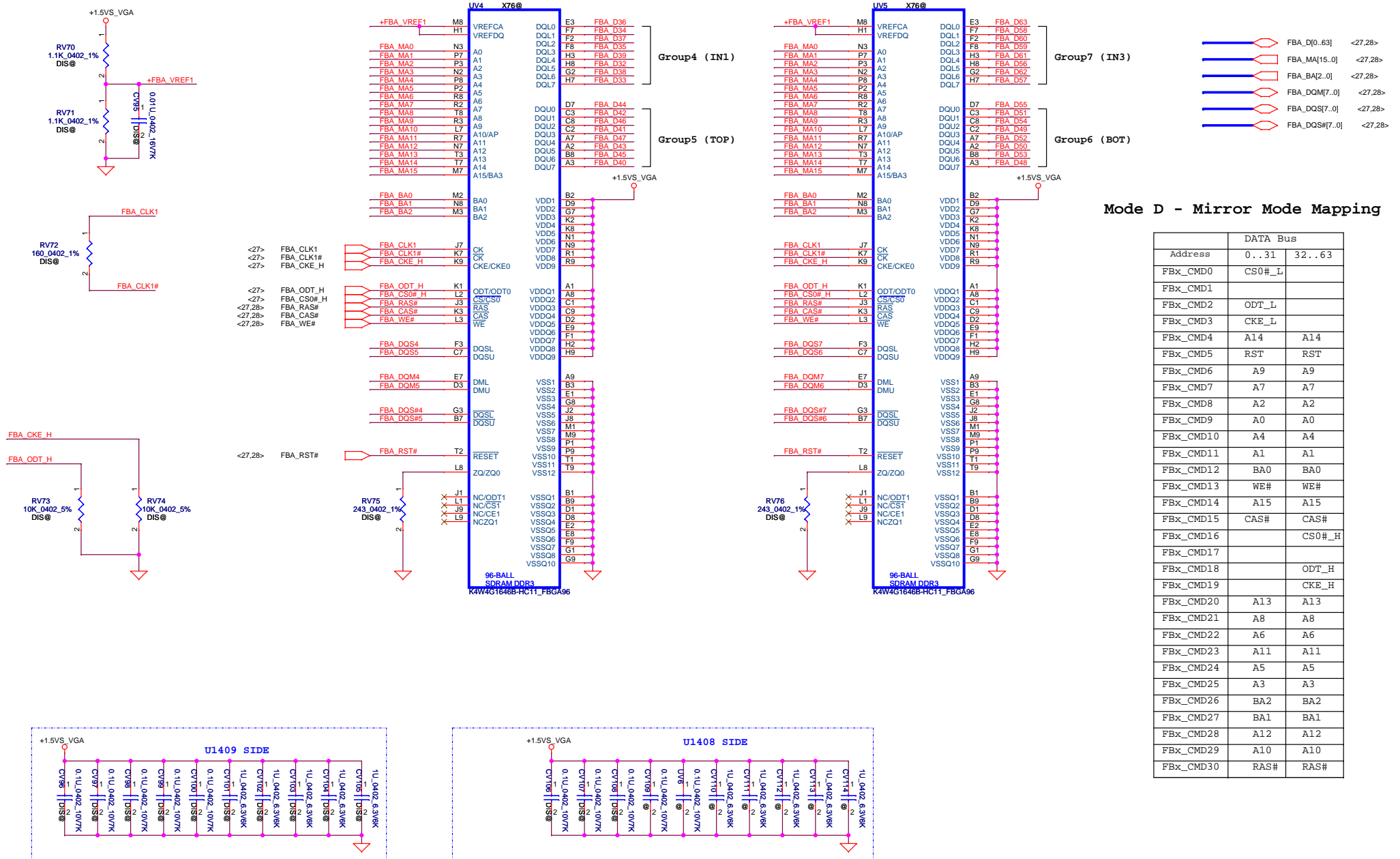
Rev 1.0

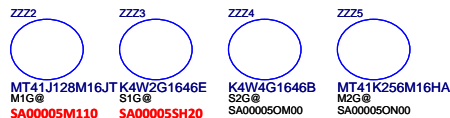
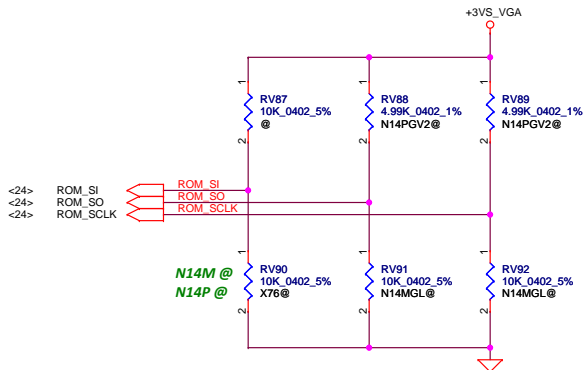
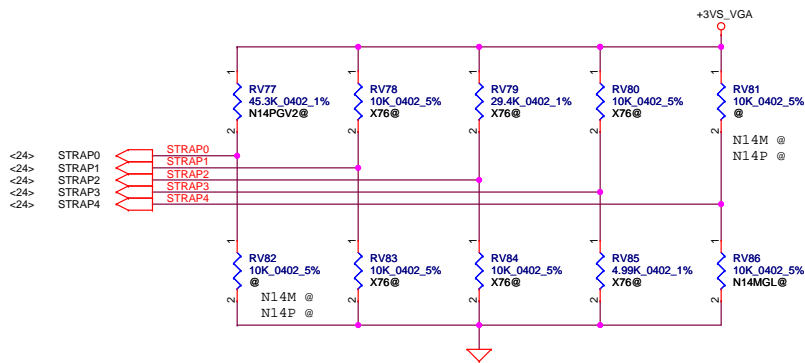
Memory Partition A - Lower 32 bits



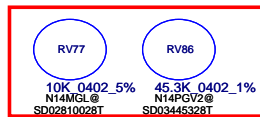
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Memory Partition A - Upper 32 bits

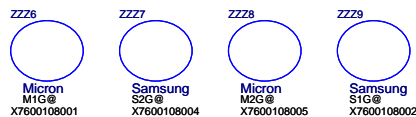




For N14P-GV2 QS Sample
 ROM_SO change from PU 10K to PU 5K
 ROM_SCLK change from PD 15K to PU 5K
 STRAP1 change from PD 5K to PD 45K
 STRAP2 change from PU 30K to PD 15K
 STRAP4 change from PD 5K to PD 45K



Load BOM時，要改成RV86, RV77



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG[3:0]	
0110	Gen1/Gen2 support only
0000	Gen3 support

FB[1:0]	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

PCIE_MAX_SPEED	
0	Limit booting to PCIe Gen1
1	Allow booting to PCIe Gen 2/3

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

USER Straps	
User[3:0]	
1000-1100	Customer defined

PCIE_SPEED_CHANGE_GEN3	
0	Disable PCIe Gen3 operation
1	Enable PCIe Gen3 operation

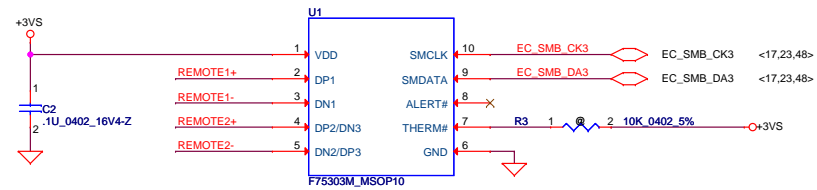
DP_PLL_VDD33V	
0	Reserved
1	Default

					X76 RV90	RV77	PU, RV78 PD, RV83	PU, RV79 PD, RV84	PU, RV80 PD, RV85	PD, RV86		
	GPU	FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
S2G, X76~04 SA00005OM00 M2G, X76~05 SA00005ON00	N14P-GV2	Samsung 1000MHz	K4W2G1646E-BC1A	PU 5K	PD 45K		PU 45.3K	PD 45.3K	PD 15K	PD 5K	PD 45.3K	
			128Mx16									
		Micron 1000MHz	MT41J128M16JT-093G									PD 30K
			128Mx16									
		*Samsung 900MHz	K4W4G1646B-HC11									PD 20K
			256Mx16									
		*Micron 900MHz	MT41K256M16HA-107G									PD 10K
			256Mx16									

						PU, RV78	PU, RV79	PU, RV80	PD, RV83	PD, RV84	PD, RV85	PD, RV86
						RV77	PD, RV83	PD, RV84	PD, RV85	PD, RV86		
GPU		FB Memory GDDR3		ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
S1G, X76~02 SA00005SH20	N14M-GL	*Samsung 1000MHz	K4W2G1646E-BC1A	PD 10K			PU 10K	PD 10K	PU 10K	PD 10K	PD 10K	
			128Mx16									
Hynix 1000MHz		H5TQ2G63DFR-N0C	PD 10K				PU 10K	PU 10K	PD 10K			
		128Mx16										
*Micron 1000MHz		MT41J128M16JT-093G	PU 10K				PD 10K	PD 10K	PD 10K			
		128Mx16										
Samsung 900MHz		K4W4G1646B-HC11	PU 10K				PU 10K	PU 10K	PU 10K			
		256Mx16										
Hynix 900MHz		H5TQ4G63MFR-11C	PU 10K				PU 10K	PD 10K	PD 10K			
		256Mx16										
Micron 900MHz		MT41K256M16HA-107G	PD 10K				PD 10K	PU 10K	PU 10K			
		256Mx16										

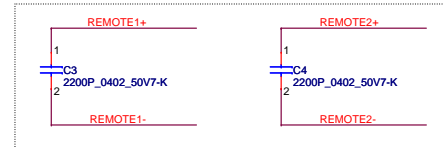
Thermal Sensor

**Thermal Sensor
placed near by VRAM**

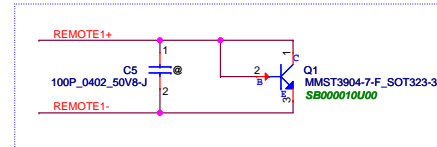


Address 1001_101xb
Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

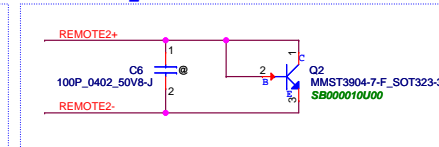
Close to U2



Close to BOTTOM DDR3



Close to +CPU_CORE

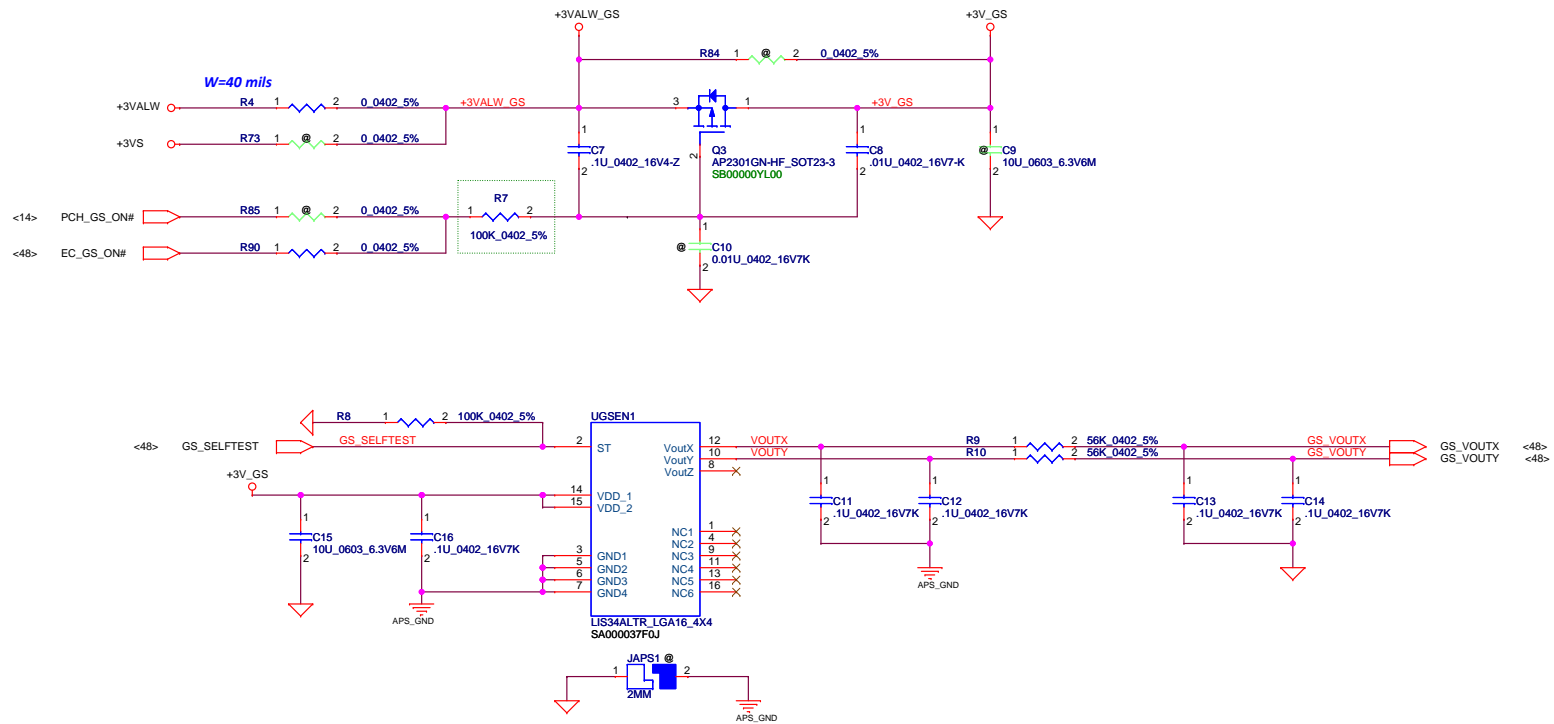


REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

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Issued Date	2012/12/05	Deciphered Date	2014/12/05	THERMAL SENSOR
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				Document Number E440 NM-A151
				Date: Thursday, July 11, 2013
				Sheet 32 of 57
				Rev 1.0



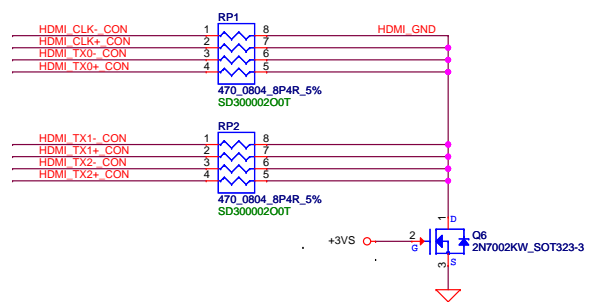
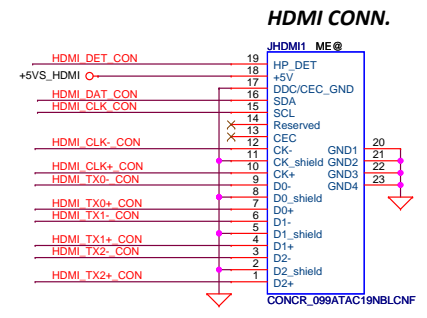
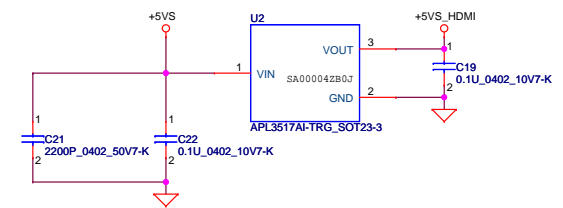
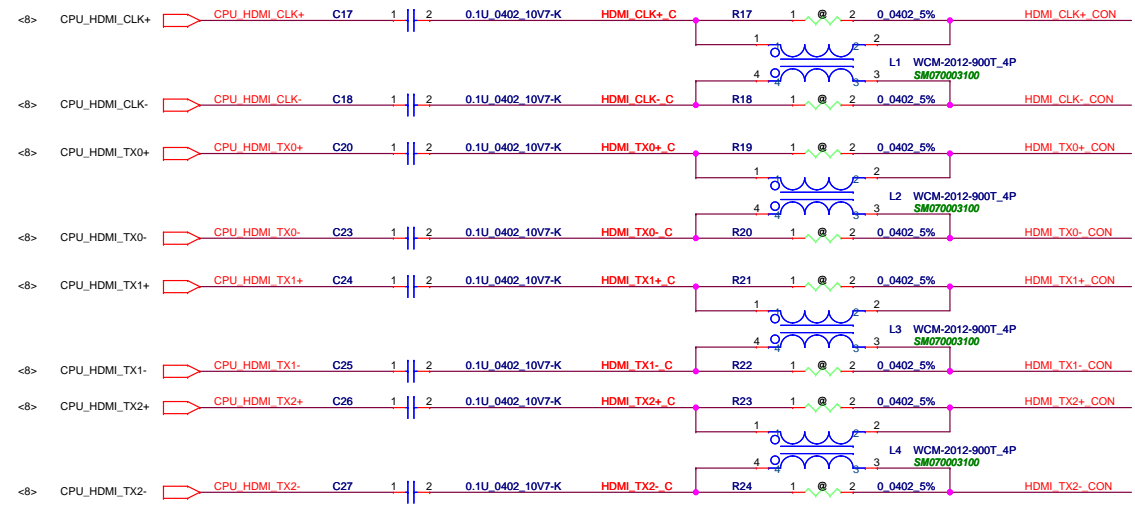
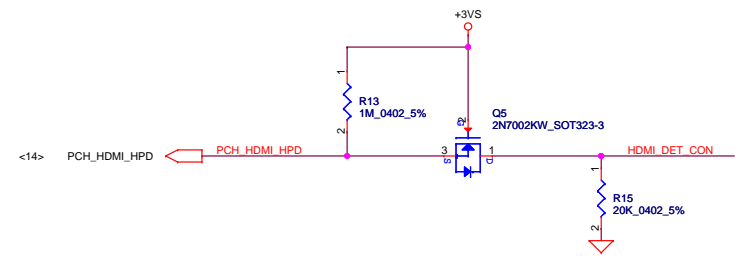
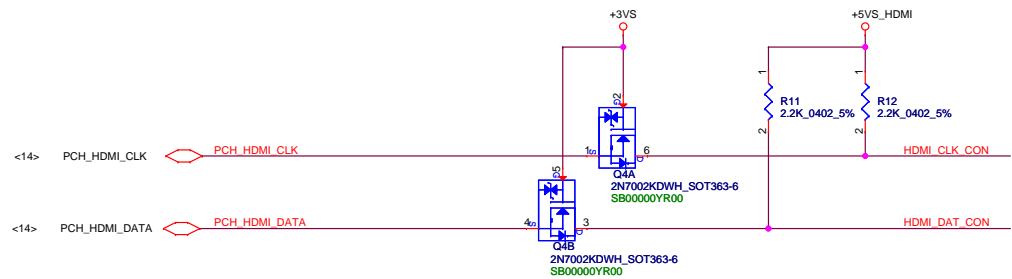
APS G-Sensor



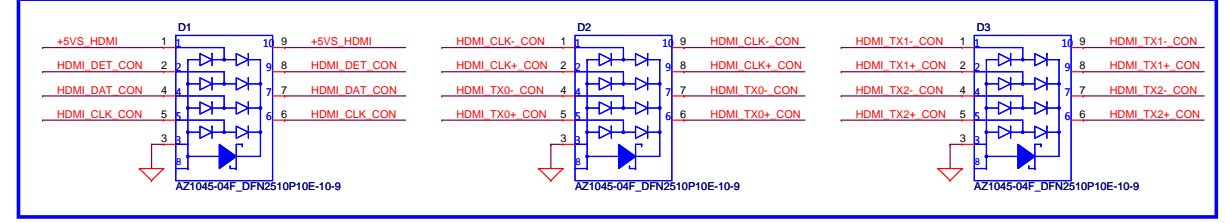
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Issued Date	2012/12/05	Deciphered Date
		2014/12/05
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Title		APPS G-SENSOR	
Size	Document Number	E440 NM-A151	
Custom			
Date:	Thursday, July 11, 2013	Sheet	33 of 57
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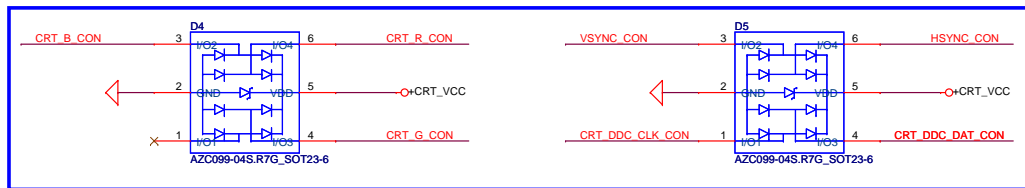




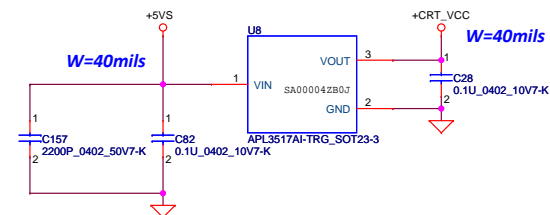
For ESD



Security Classification	LC Future Center Secret Data			Title	HDMI CONN.	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	Size	Document Number	Rev
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				Date:	Thursday, July 11, 2013	Sheet 34 of 57

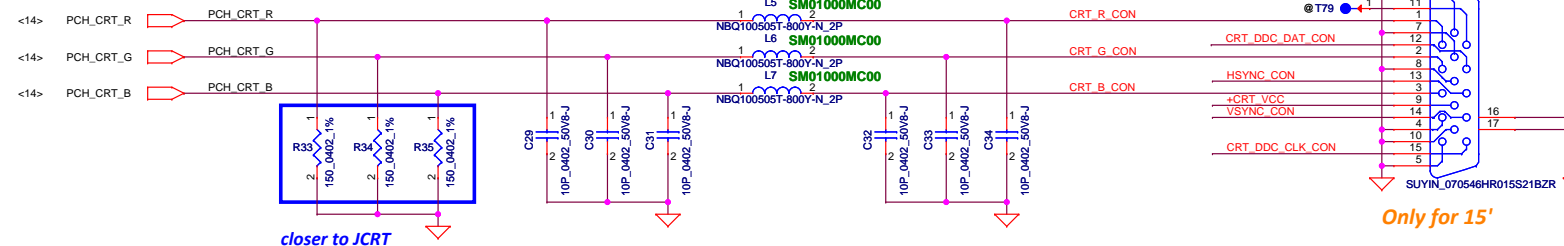


closer to JCRT



CRT Connector

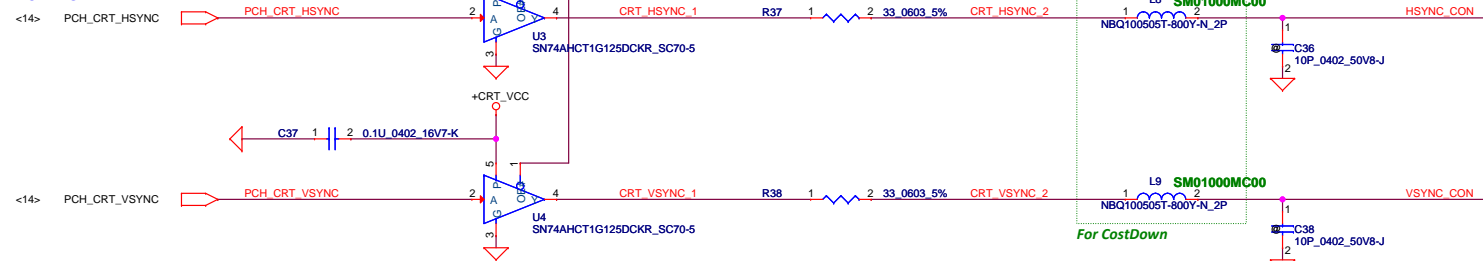
From PCH



closer to JCRT

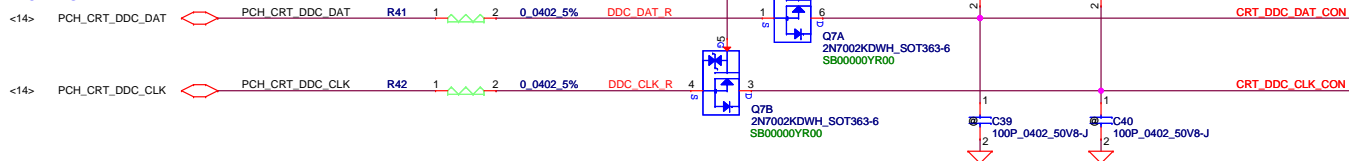
Only for 15'

From PCH



For CostDown

From PCH

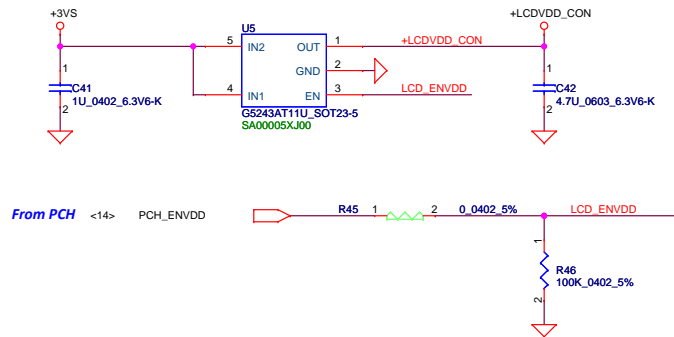


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Issued Date	2012/12/05	Deciphered Date
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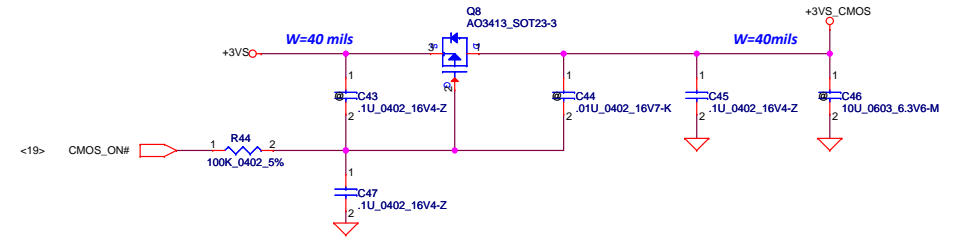
Title	Size	Document Number	Rev
CRT CONN.	Custom	E540 NM-A161	1.0
Date:	Thursday, July 11, 2013	Sheet	35 of 57



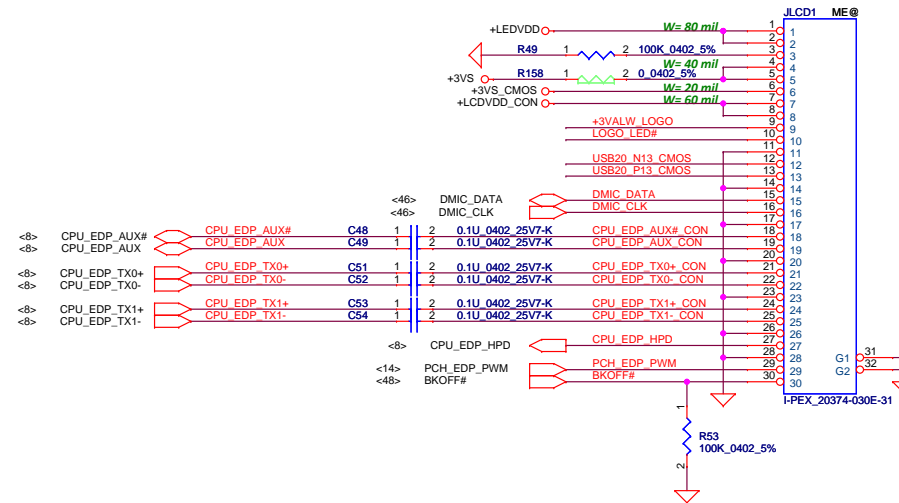
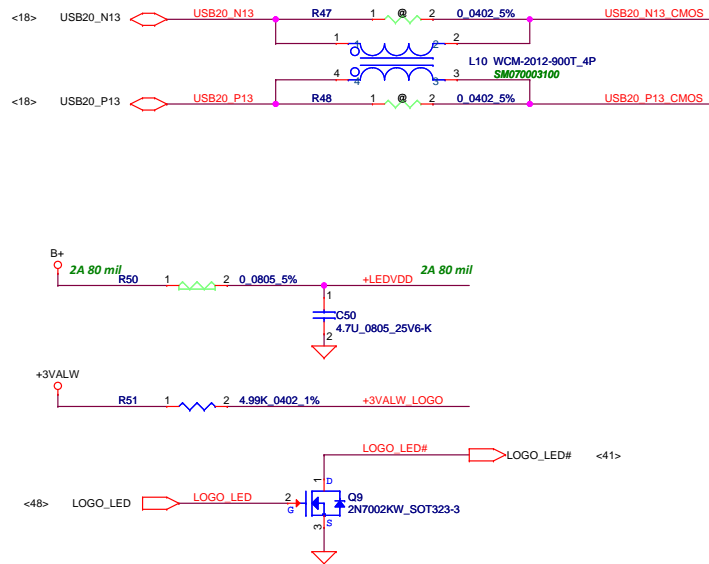
LCDVDD Circuit



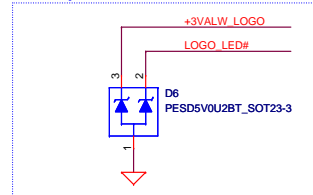
CMOS Camera



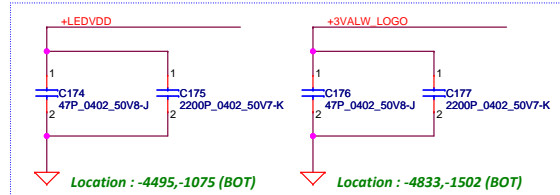
CMOS USB Port10



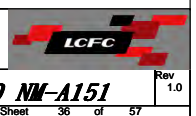
ESD request

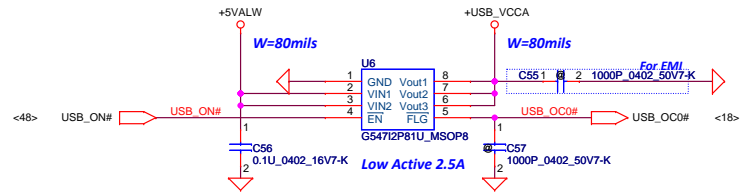


EMI

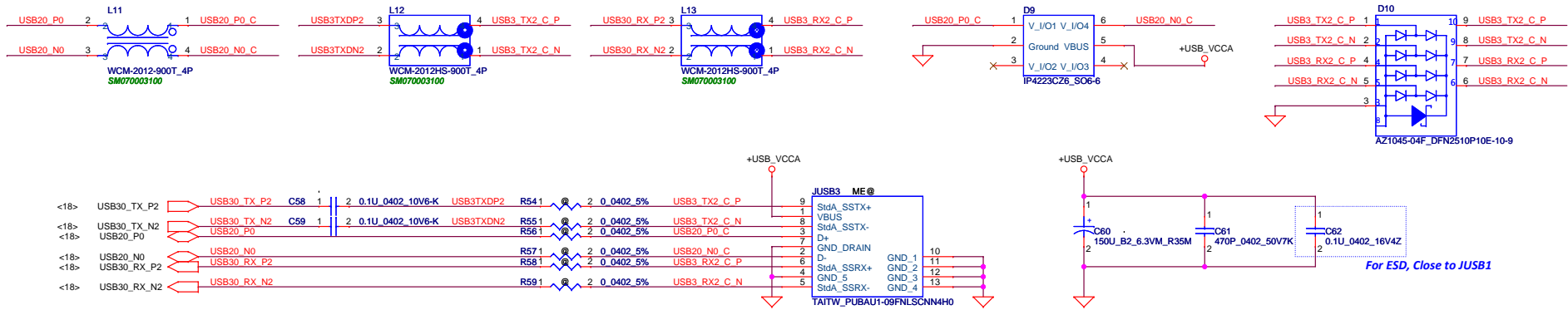


Security Classification	LC Future Center Secret Data		Title	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	LCD/CMOS CONN.
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Size	Document Number	Date	Thursday, July 11, 2013	Rev 1.0
Custom	E440 NM-A151	Sheet	36	of 57

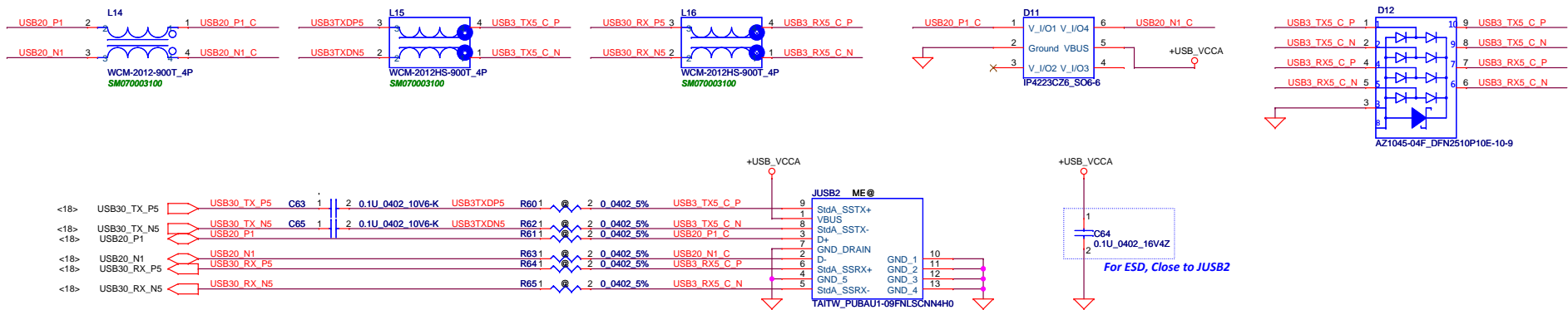





USB30 Front

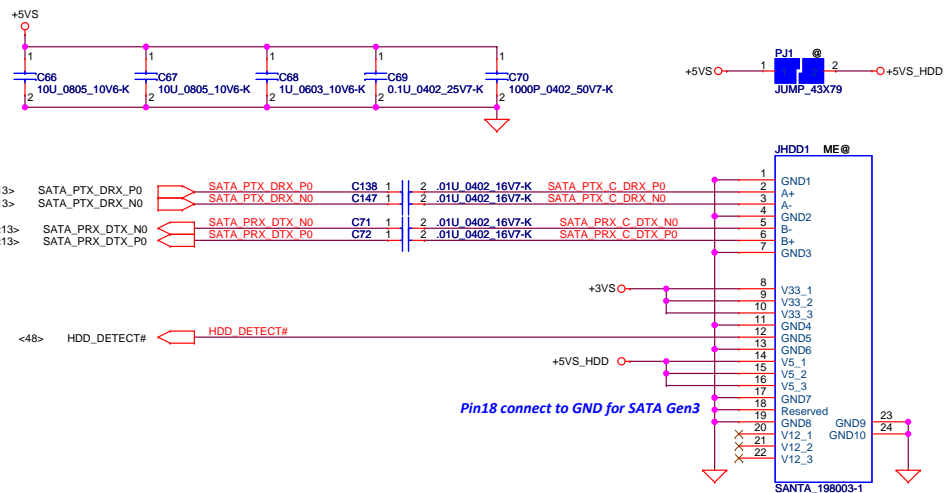


USB30 Back



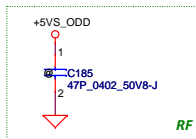
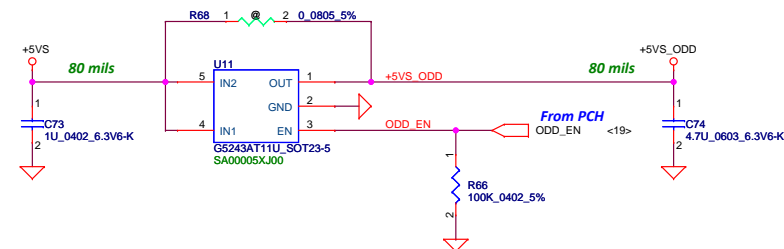
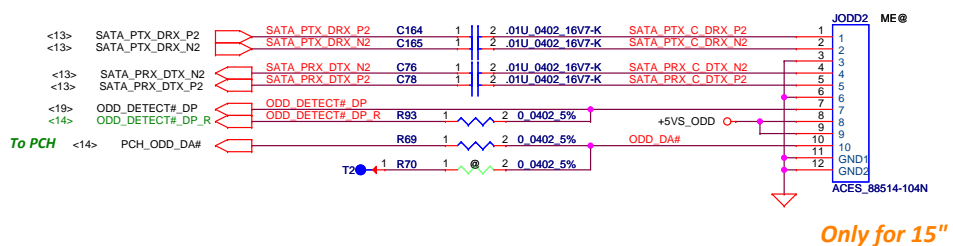
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Issued Date		2012/12/05	Deciphered Date	2014/12/05		
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Size Custom		Document Number		E440 NM-A151		Rev 1.0
Date:		Thursday, July 11, 2013		Sheet 37 of 57		

SATA HDD CONN.

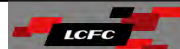


SATA ODD CONN & ODD Power Control

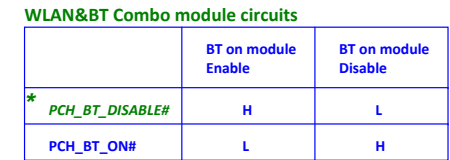
+5VS TO +5VS_ODD



Security Classification				LC Future Center Secret Data		Title		Document Number		Rev	
Issued Date				2012/12/05		Deciphered Date		2014/12/05		1.0	
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								E540 NM-A161			

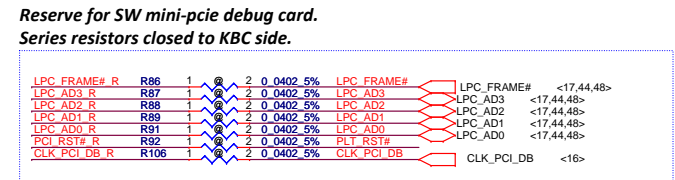


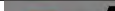
WWW.AliSaler.Com



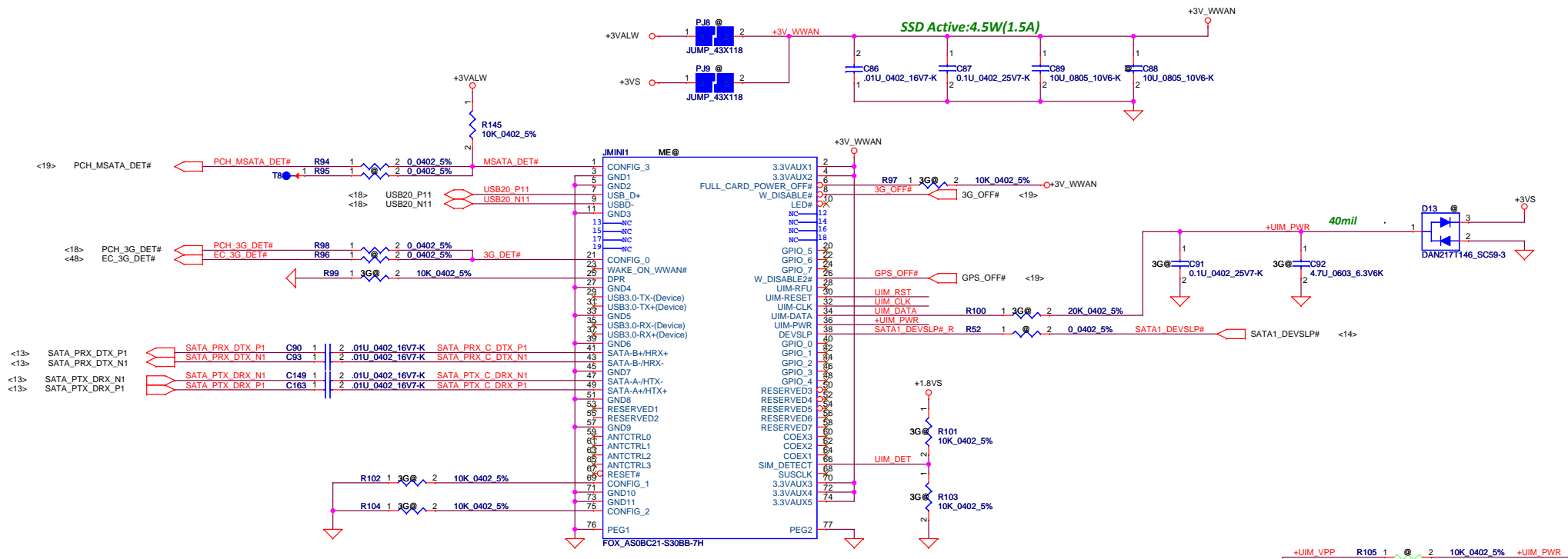
+3VALW To +3V_WLAN
+3VALW To +3V_WWAN

1. softstart (RC) will check on EVT PCB
2. if AOAC enable +3V_WLAN always ON
if AOAC disable +3V_WLAN is same as +3VS



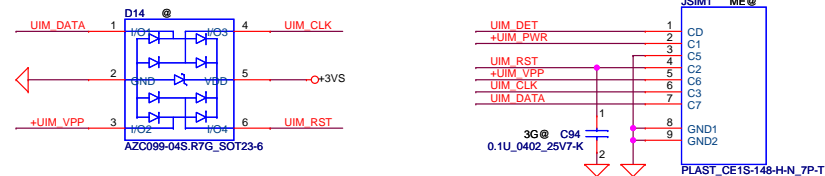
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2012/12/05	Deciphered Date	2014/12/05	PCle-WLAN SLOT		
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				Date:	Thursday, July 11, 2013	Rev 1.0
				Sheet	39 of 57	

NGFF(SSD) & SIM CARD CONN.



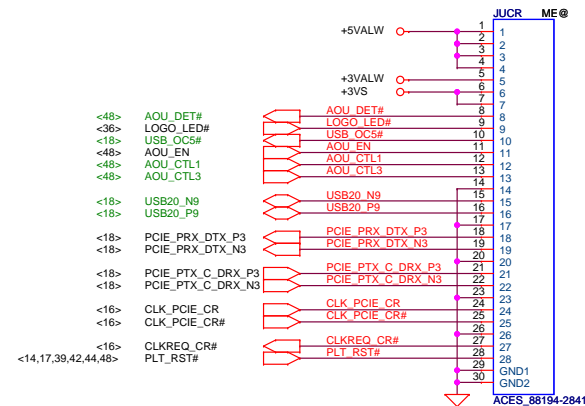
Only for 15"

1. PCH_MSATA_DET# --> +3V_PCH
EC_MSATA_DET# --> +3VL
2. PCH_3G_DET# --> +3VS
EC_3G_DET# --> +3VL
需小心EC漏電到PCH
3. EC don't have GPIO pin for DET# pin as below
 - a. PCH_3G_DET#
 - b. PCH_MSATA_DET#



NGFF Detect Desc.		
	MSATA_DET#	3G_DET#
No Card	1	1
WWAN CARD	1	0
SSD CARD	0	0

USB2.0, CR & LOGO Board

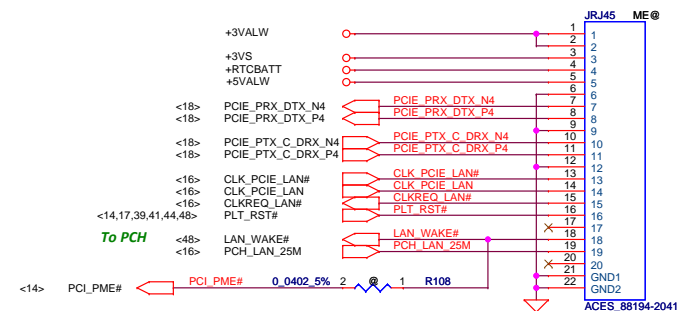


Security Classification	LC Future Center Secret Data			Title	PCle-CR/USB-Charge CONN.	
Issued Date	2012/12/05	Deciphered Date	2014/12/05	Size	Document Number	Rev
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				Date:	Thursday, July 11, 2013	Sheet 41 of 57

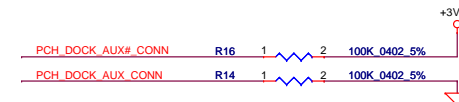
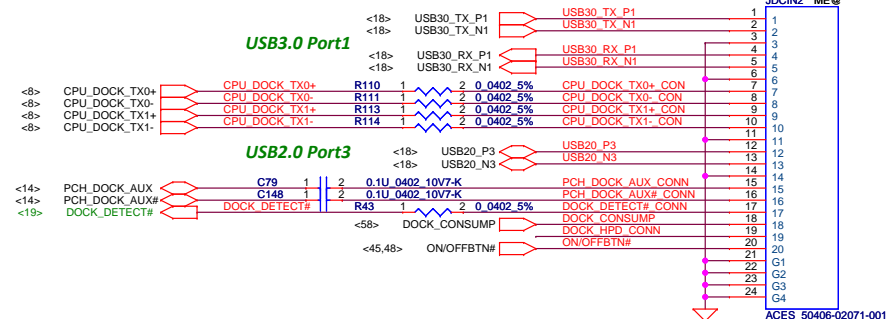
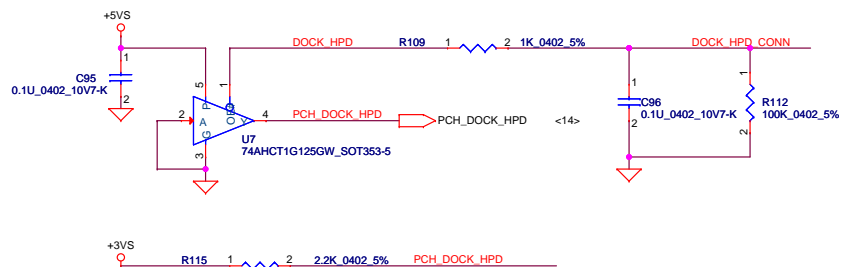


LAN (Port4)
USB3.0/2.0 (Port1/3)
DP(DDIC)

LAN CONN. (FFC)

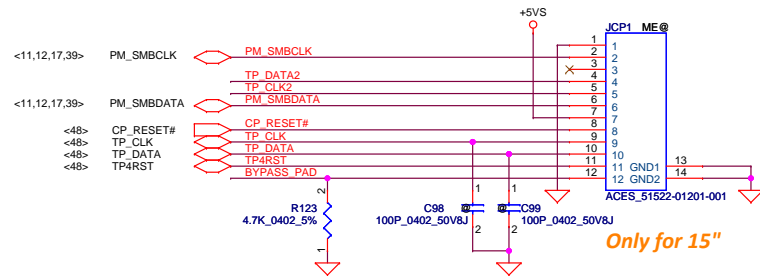


DCIN CONN. (Coaxial)

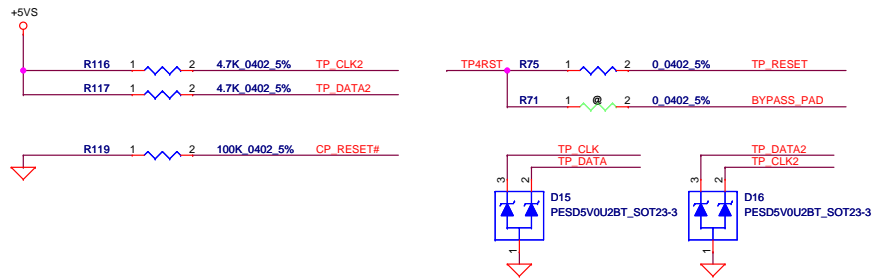


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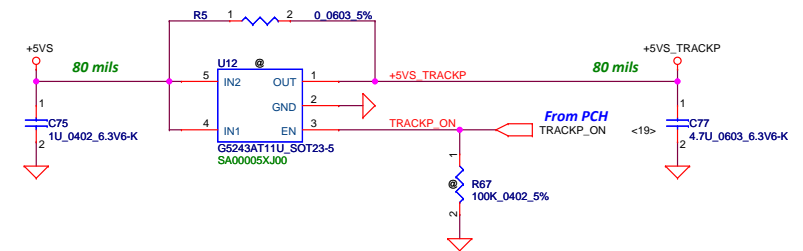
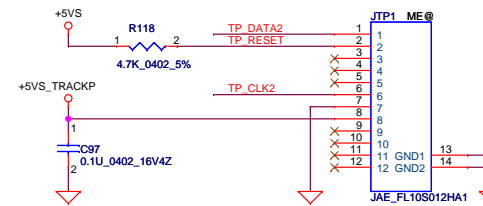
Click Pad



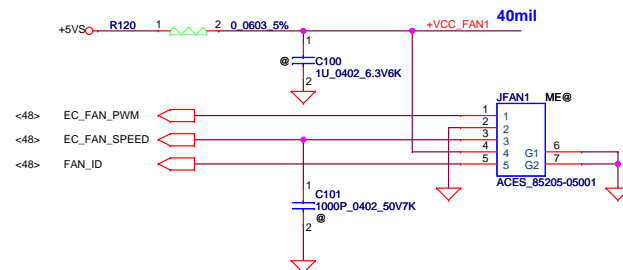
Only for 15"

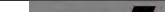


Track point

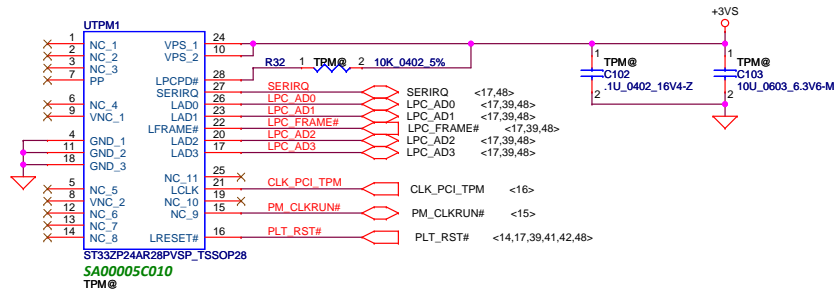


FAN CONN.

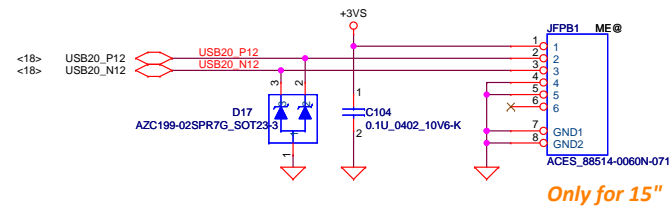


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				Date:	Thursday, July 11, 2013	Sheet 43 of 57 Rev 1.0

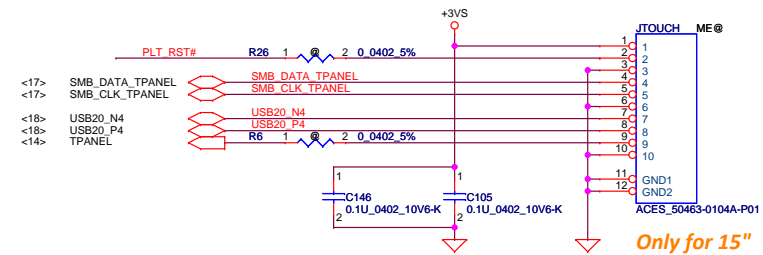
TPM IC



FingerPrint CONN.



Touch Panel CONN.



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				Document Number E540 NM-A161
				Rev 1.0
				Date: Thursday, July 11, 2013
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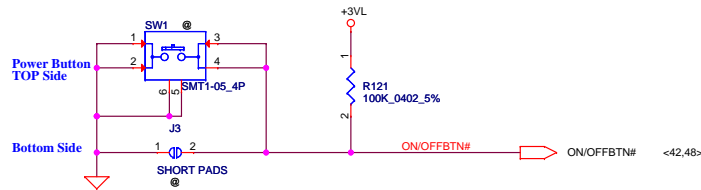


E540 NM-A161

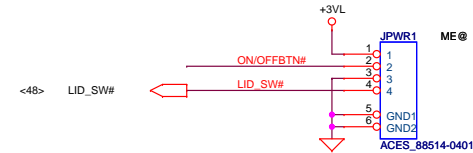
Rev 1.0

PWR BTN/LID SW CONN.

ON/OFF switch

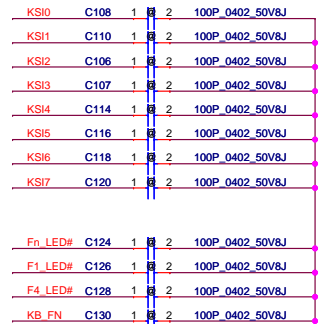


1. Power Button/B link to Function/B Conn. 10pin
2. Lid Switch

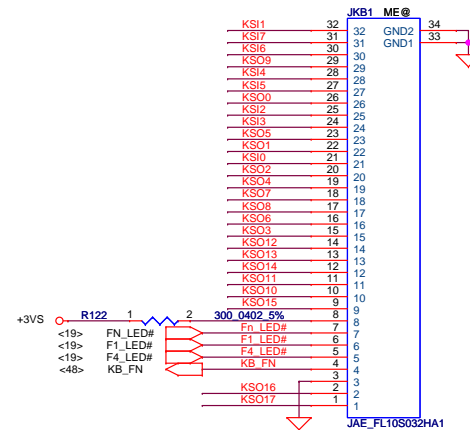
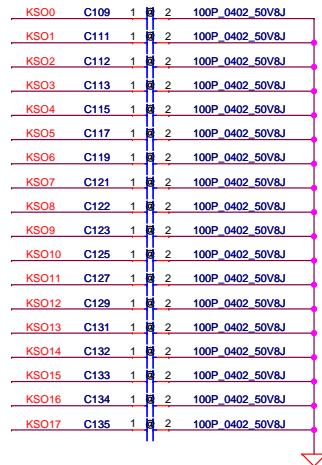



KeyBoard CONN.(14")

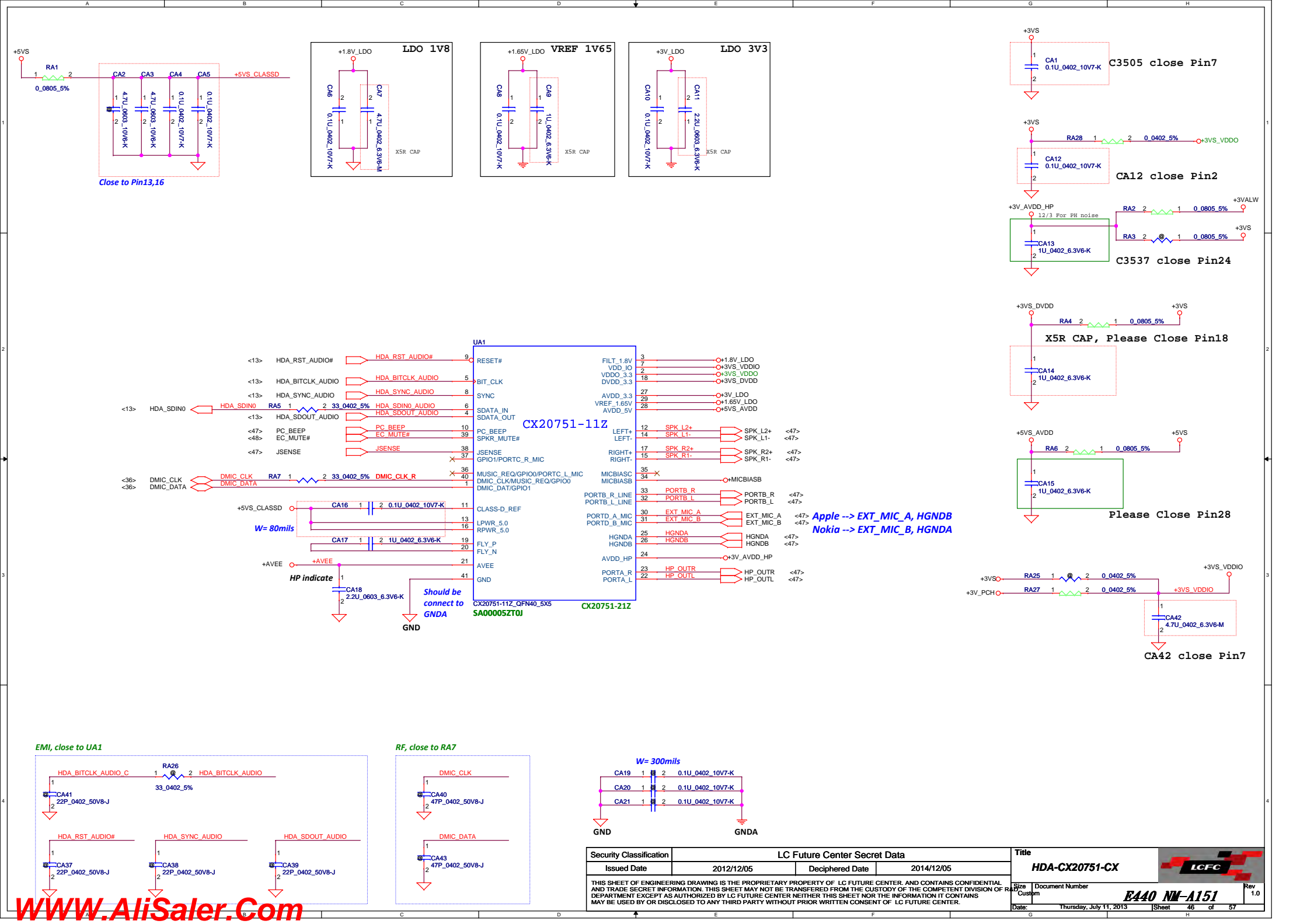
KSI[0..7] <48>
KSO[0..17] <48>



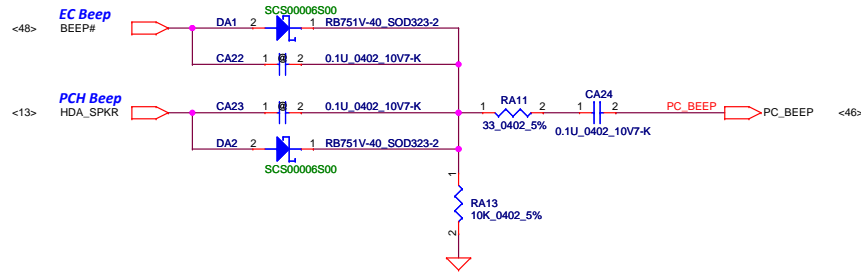
CONN PIN define need double check



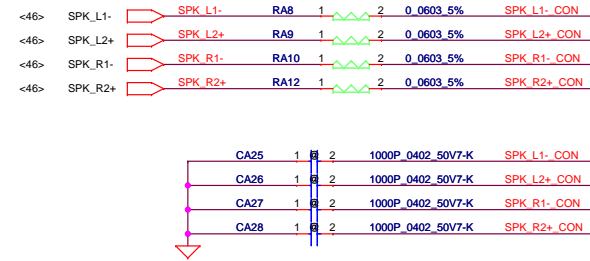
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Size		Document Number		E540 NM-A161				Rev	
Custom								1.0	
Date:		Thursday, July 11, 2013				Sheet		45 of 57	



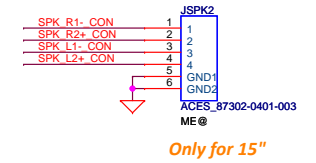
PC BEEP



Speaker OUT

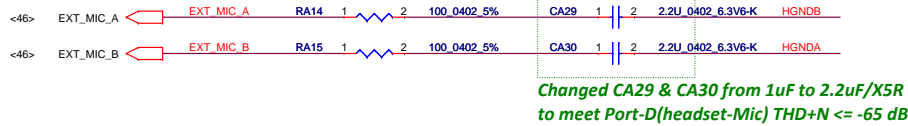


SPK CONN.

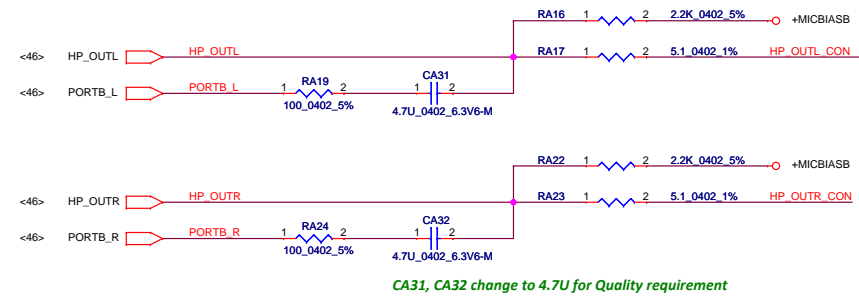


EXT. MIC/LINE IN

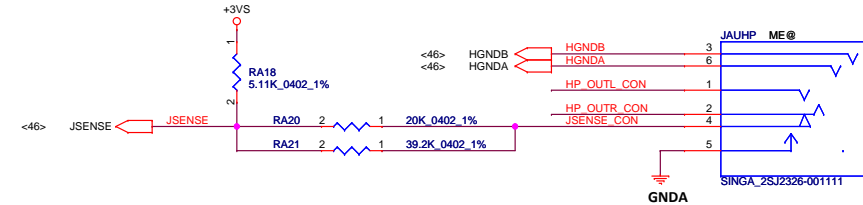
Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A



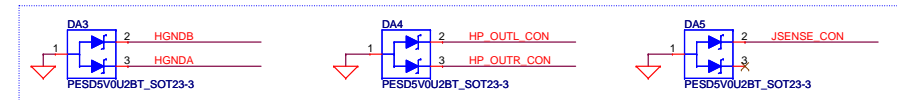
HeadPhone/LINE OUT



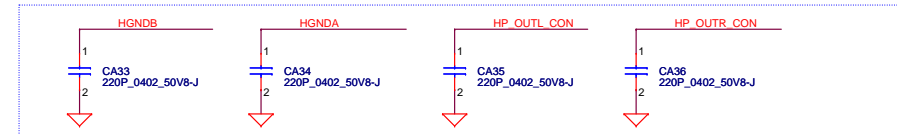
Audio Jack




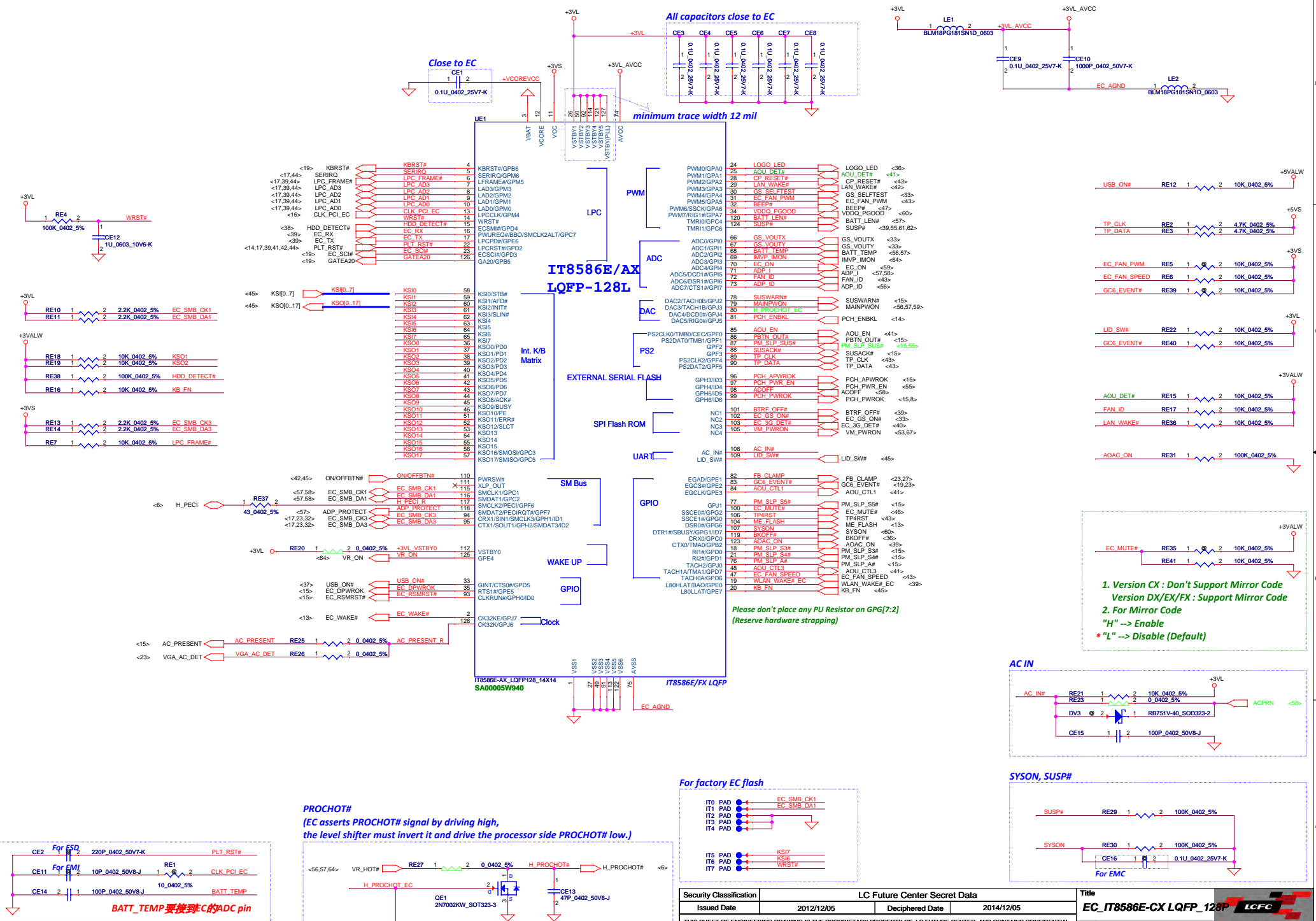
ESD Diode, close to JAUHP



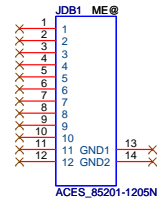
EMI, close to JAUHP




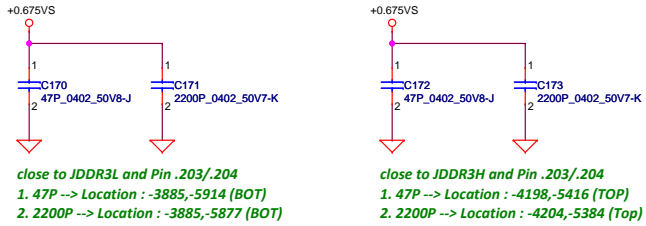
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								Custom		E540 NM-A161	1.0				
								Date:		Thursday, July 11, 2013		Sheet	47	of	57




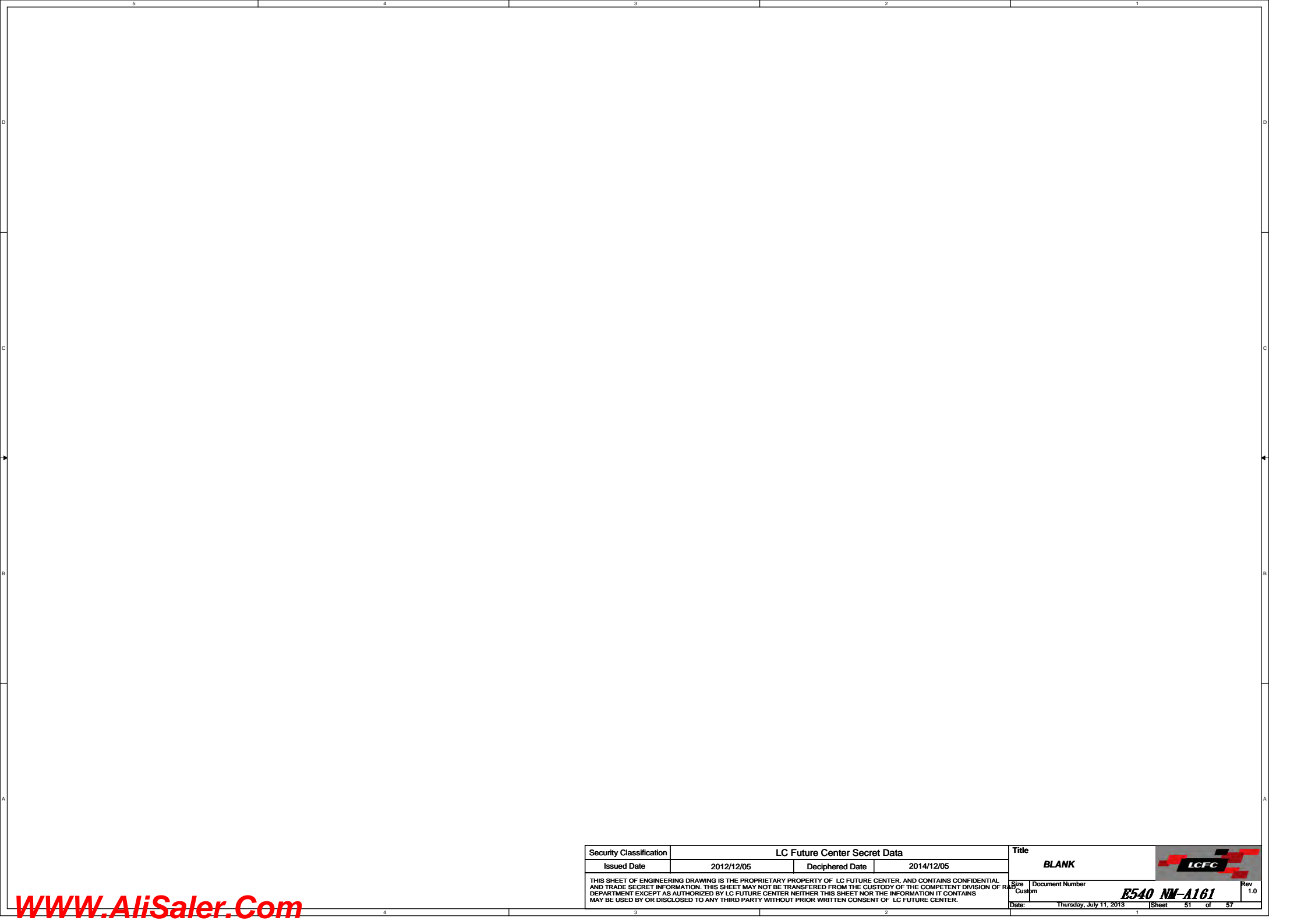
- 1. Version CX : Don't Support Mirror Code
- Version DX/EX/FX : Support Mirror Code
- 2. For Mirror Code
- "H" --> Enable
- "L" --> Disable (Default)




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				Date:	Thursday, July 11, 2013	Sheet 49 of 57

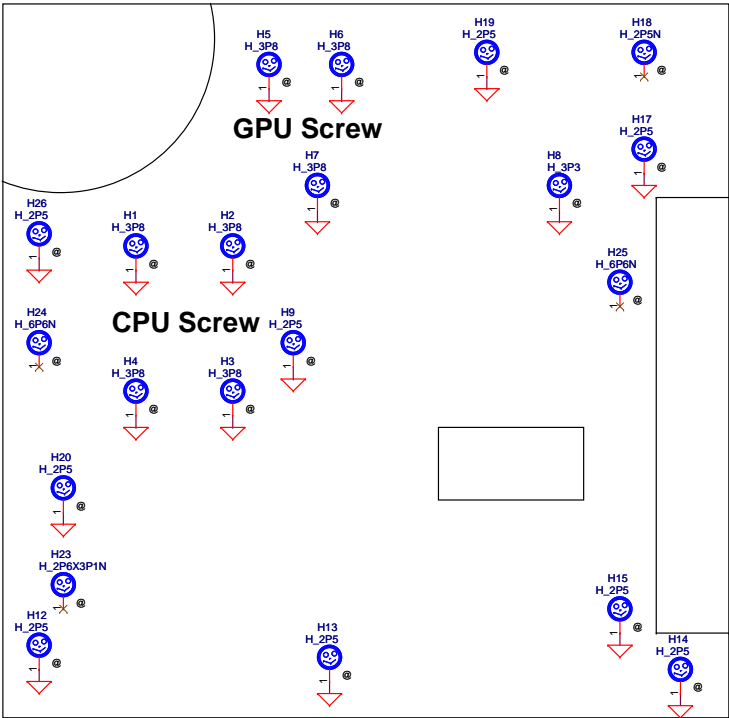


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Issued Date	2012/12/05	Deciphered Date	2014/12/05			
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				Date:	Thursday, July 11, 2013	Sheet 51 of 57

Screw Hole



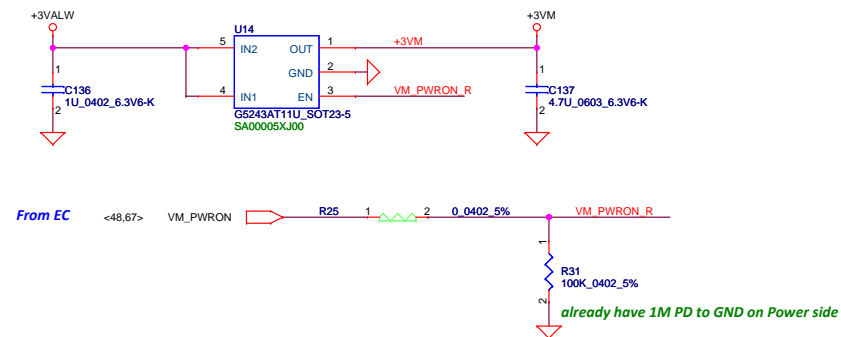
PCB Fedical Mark PAD




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				Date: Thursday, July 11, 2013	Rev 1.0
				Sheet 52	of 57

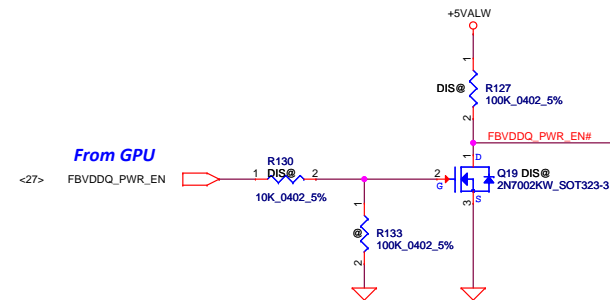
+3VALW to +3VM

FOR SBA Function POWER(always mount)

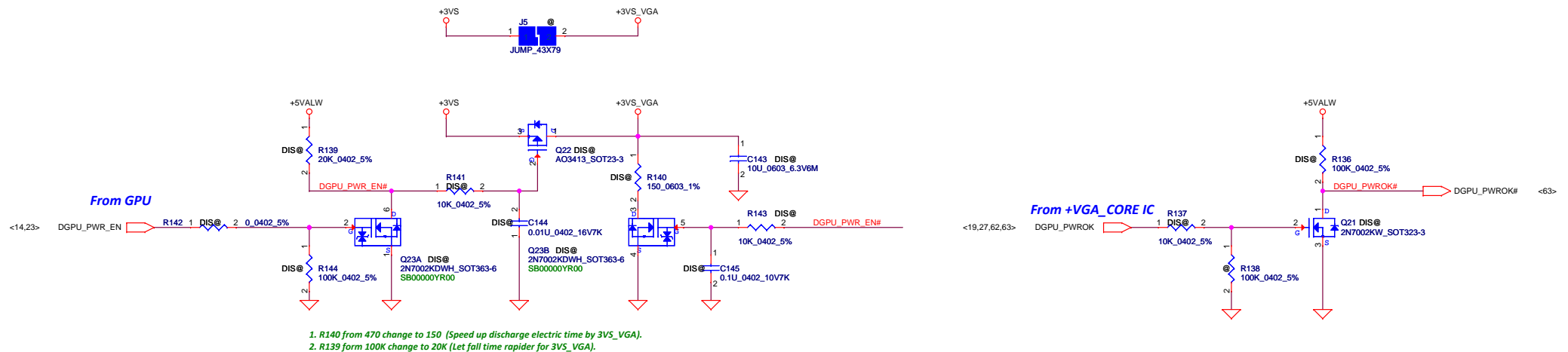


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				Rev 1.0 Sheet 53 of 57

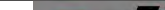
+3VS to +3VS_VGA



+3VS to +3VS_VGA



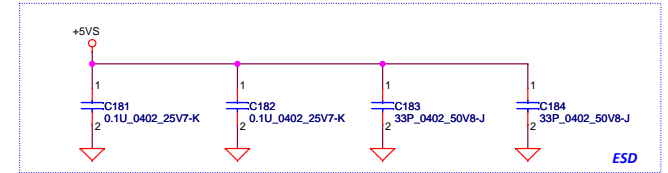
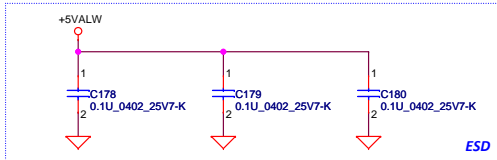
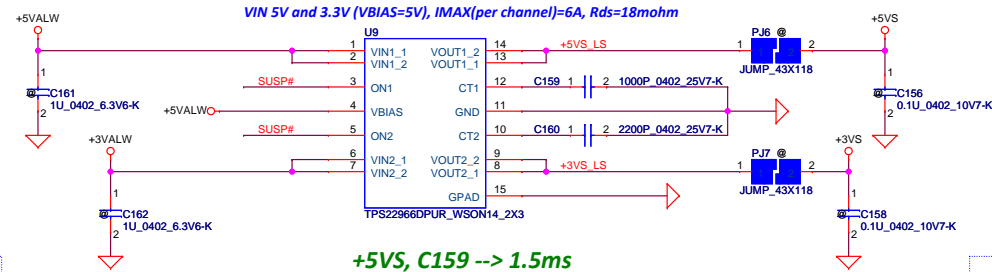
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+3VS_VGA (En:DGPU_PWR_EN)
+VGA_CORE (En:NVDD_PWR_EN, POK:DGPU_PWROK)
+1.5VS_VGA (En:FBVDDQ_PWR_EN# = FB_CLAMP and DGPU_PWROK)
+1.05VS_VGA (En:DGPU_PWROK#)
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Size	Document Number	E440 NW-A151		Rev	1.0
Date:	Thursday, July 11, 2013	Sheet	54 of 57		

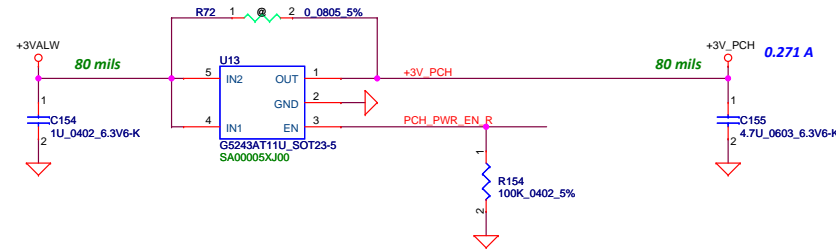
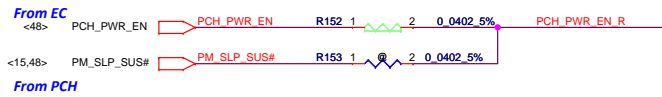
Load Switch

+5VALW To +5VS

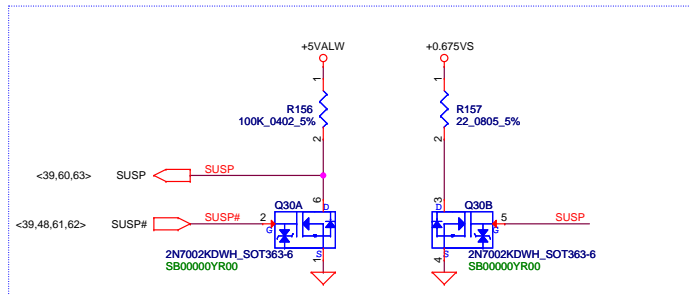
+3VALW To +3VS



+3VALW To +3V_PCH



For DisCharge

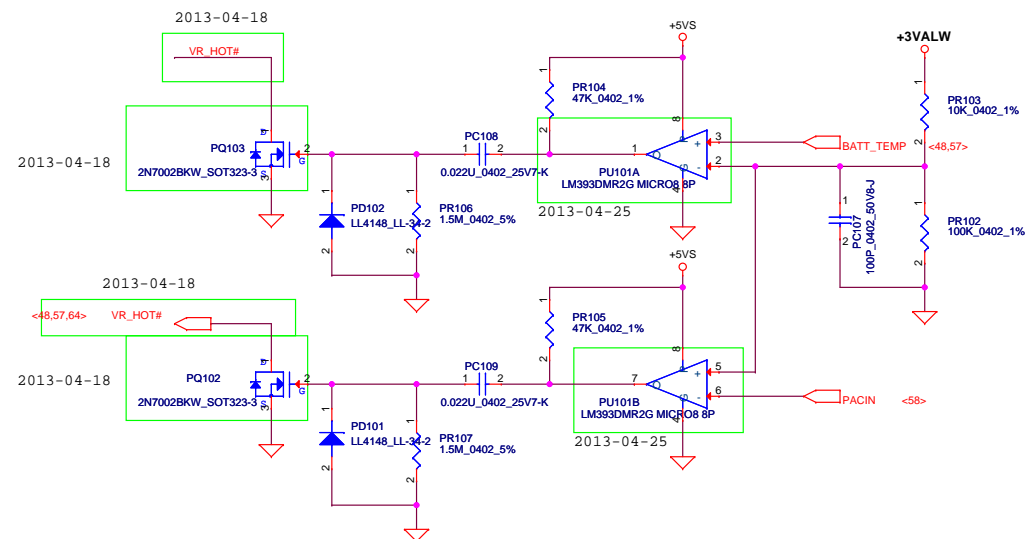
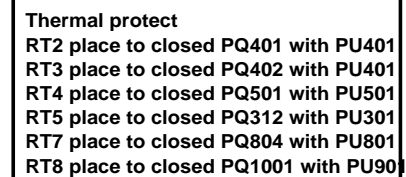
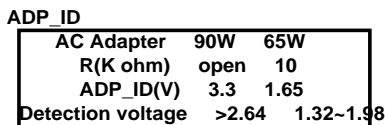


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				Date: Thursday, July 11, 2013	Rev 1.0

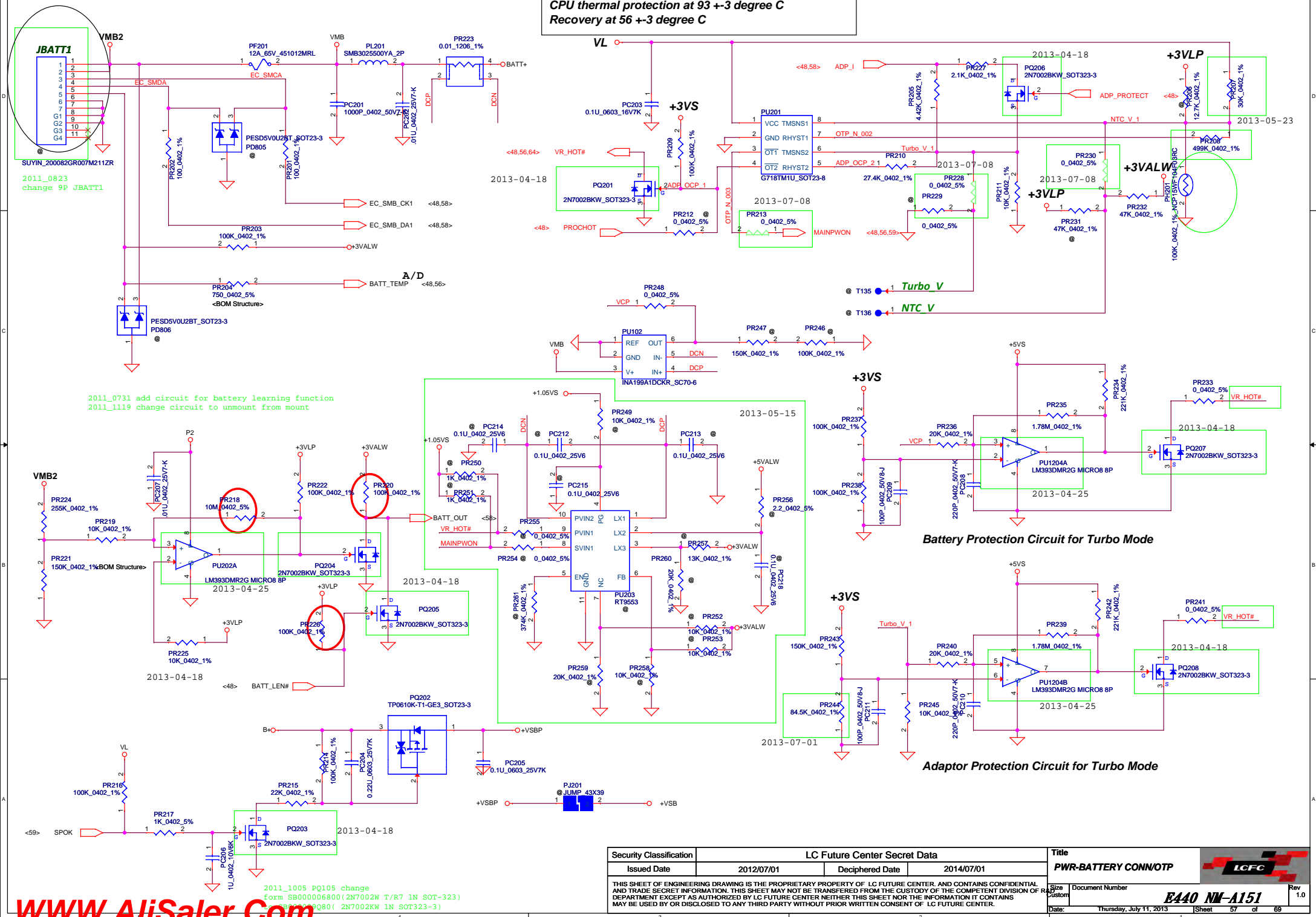


E440 NM-A151


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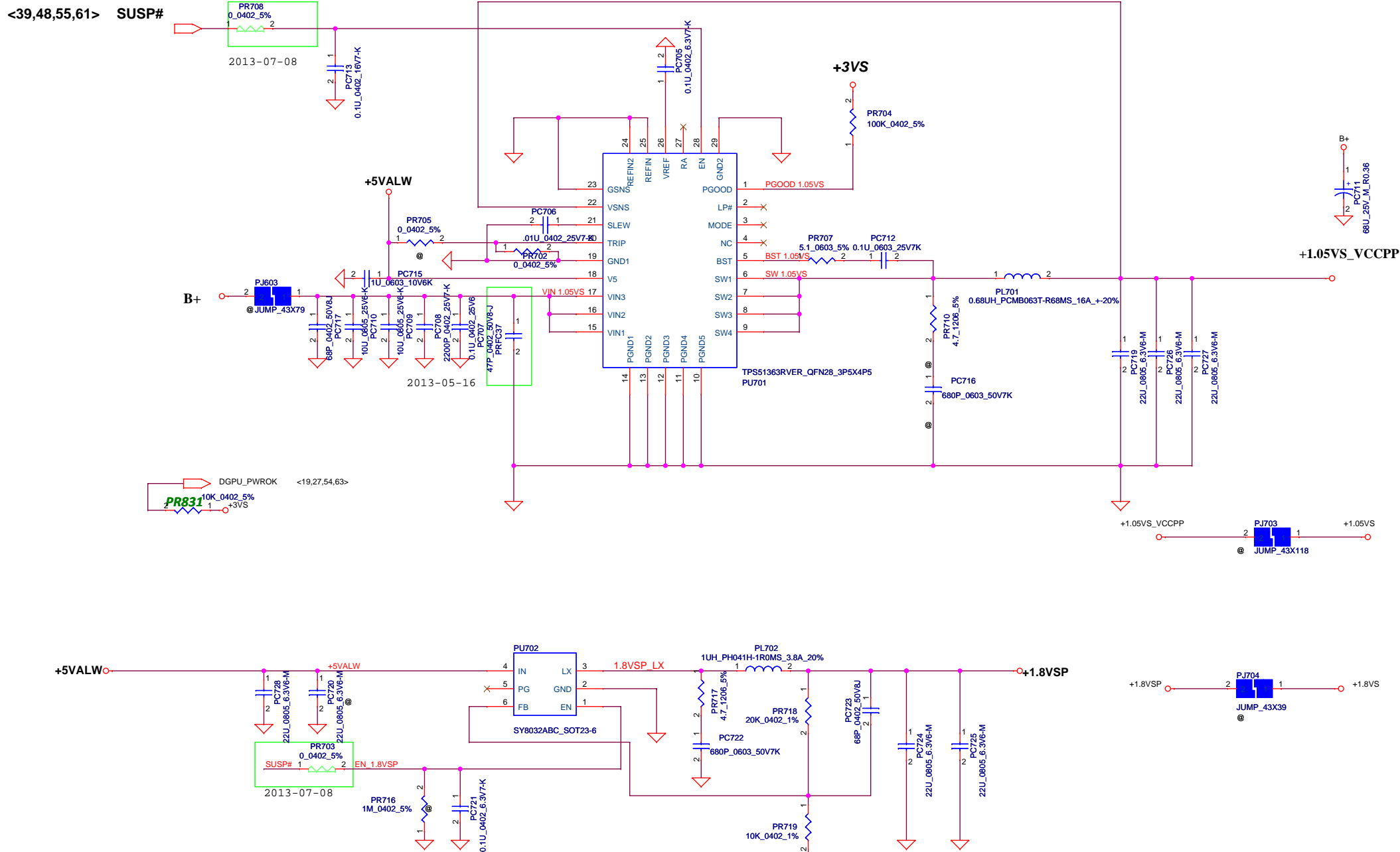



PH1 under CPU bottom side :
CPU thermal protection at 93 \pm 3 degree C
Recovery at 56 \pm 3 degree C





AL OF F	Title PWR-CHARGER-BQ24737			
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Rev 1.0

Place close to
phase 1 inductor

CPU_B+

2013-07-08

37W=10K
47W=15.4K
PR917
10K_0402_1%

37W=43K
47W=66.5K

81103_PWM

2013-07-08

Mount for 37W

2013-07-08

+5VALW

PR951
0.0402_5%

SW1

SW3

PC908

2.2U_0603_10V7-K

PR918
2.2_0803_5% 0.22U_0402_10V6-K

PC909

2.2U_0603_10V7-K

PR928
45.3K_0402_1%

PR929
52.3K_0402_1%

PR930
1.9K_0402_1%

PR931
0.0402_5%

PR932
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PR933
0.0402_5%

PR934
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PR935
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PR994
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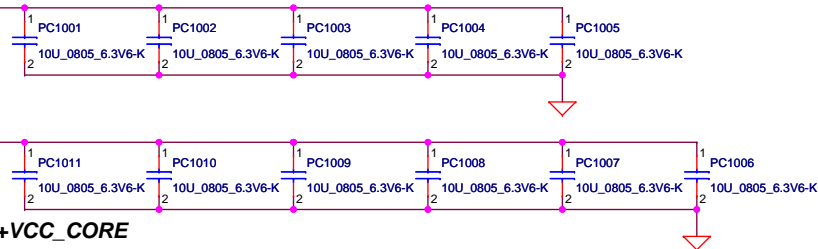
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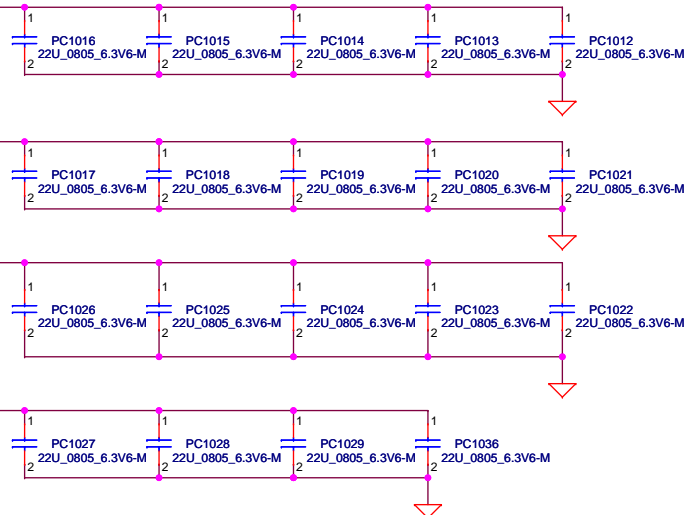
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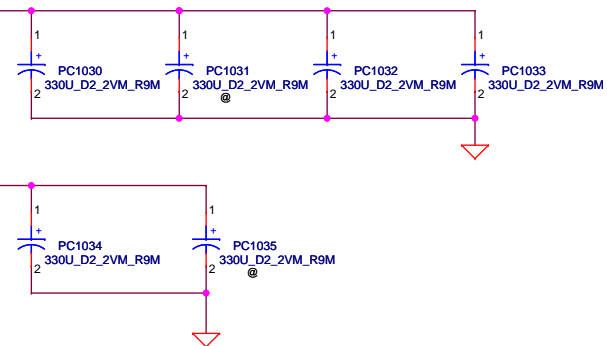
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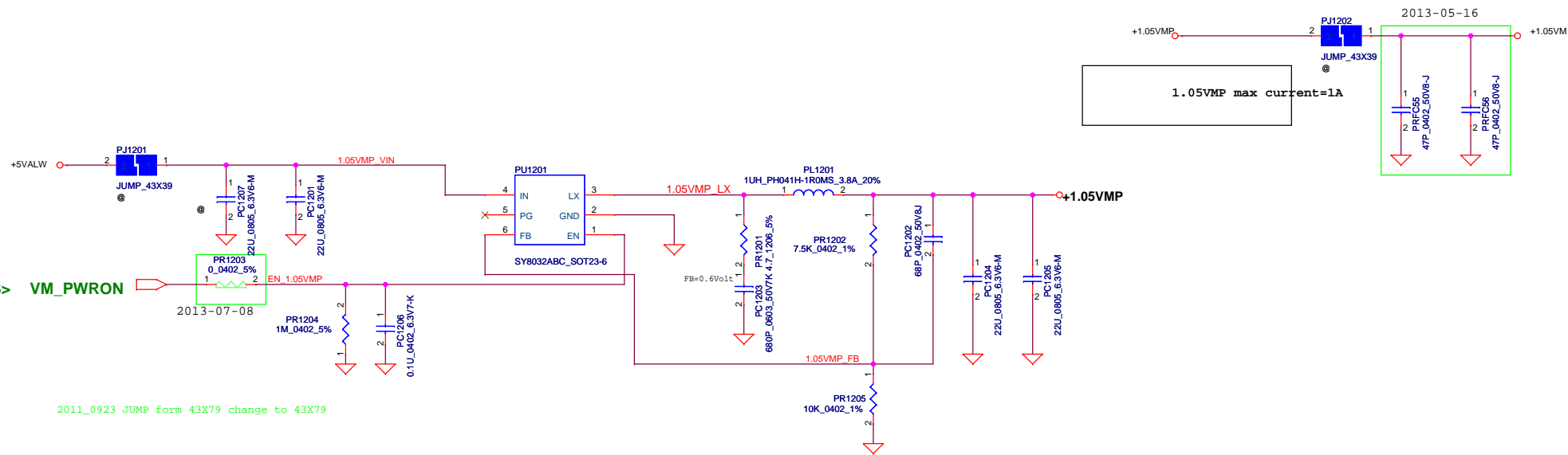
Security Classification		LC Future Center Secret Data		Title	
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E440 NM-A151 Rev 1.0

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2011_0923 JUMP form 43X79 change to 43X79

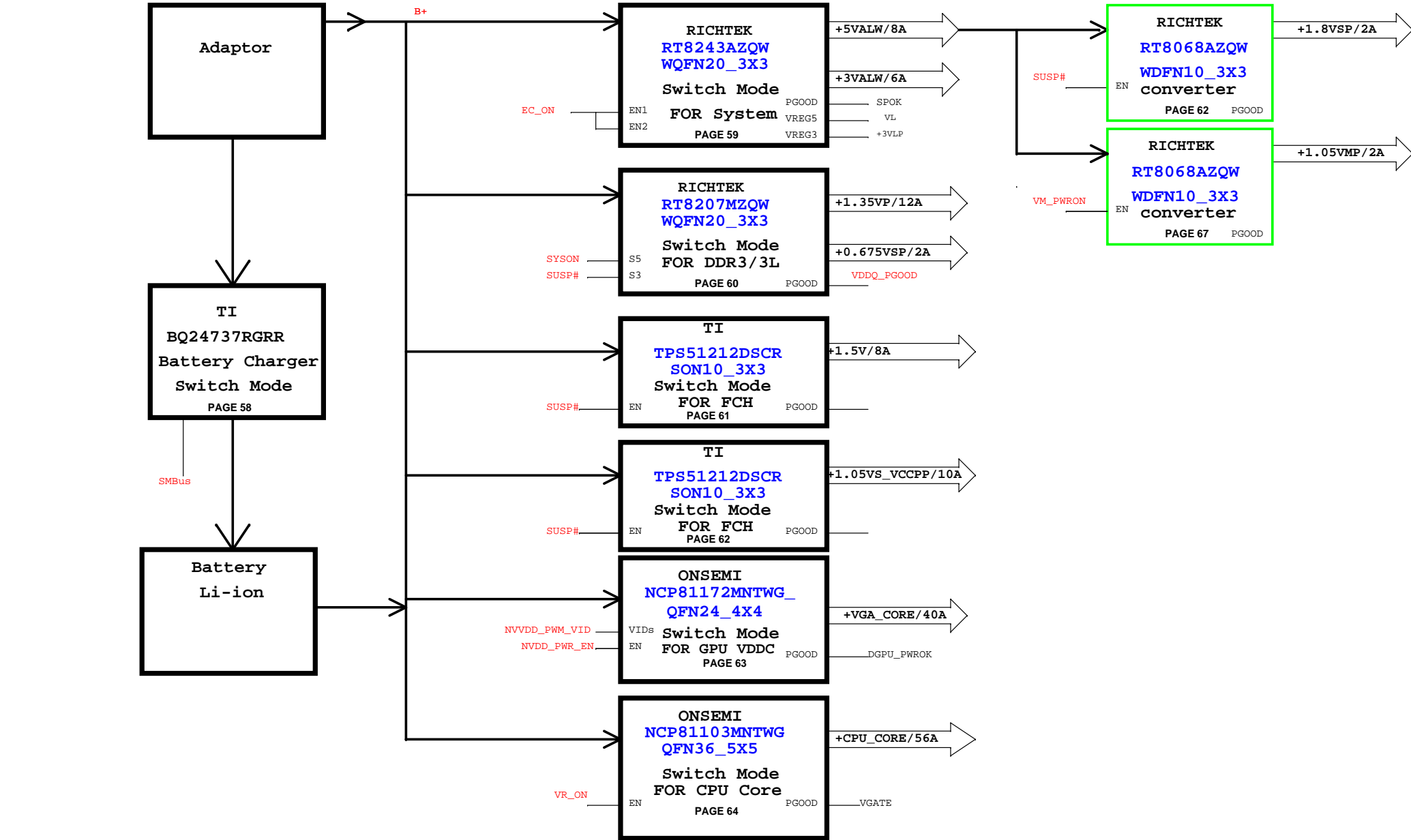


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POWER PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO DATE PAGE MODIFICATION LIST PURPOSE



HW PIR (Product Improve Record)

AILE1 NM-A151 SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/01/16

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "@" to "DS3@"
				For Deep S3 Function

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2012/12/05	Deciphered Date	2014/12/05	Title	PIR (PWR)	
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				Date:	Thursday, July 11, 2013	Sheet 69 of 69