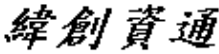


Hades_840M_ULT
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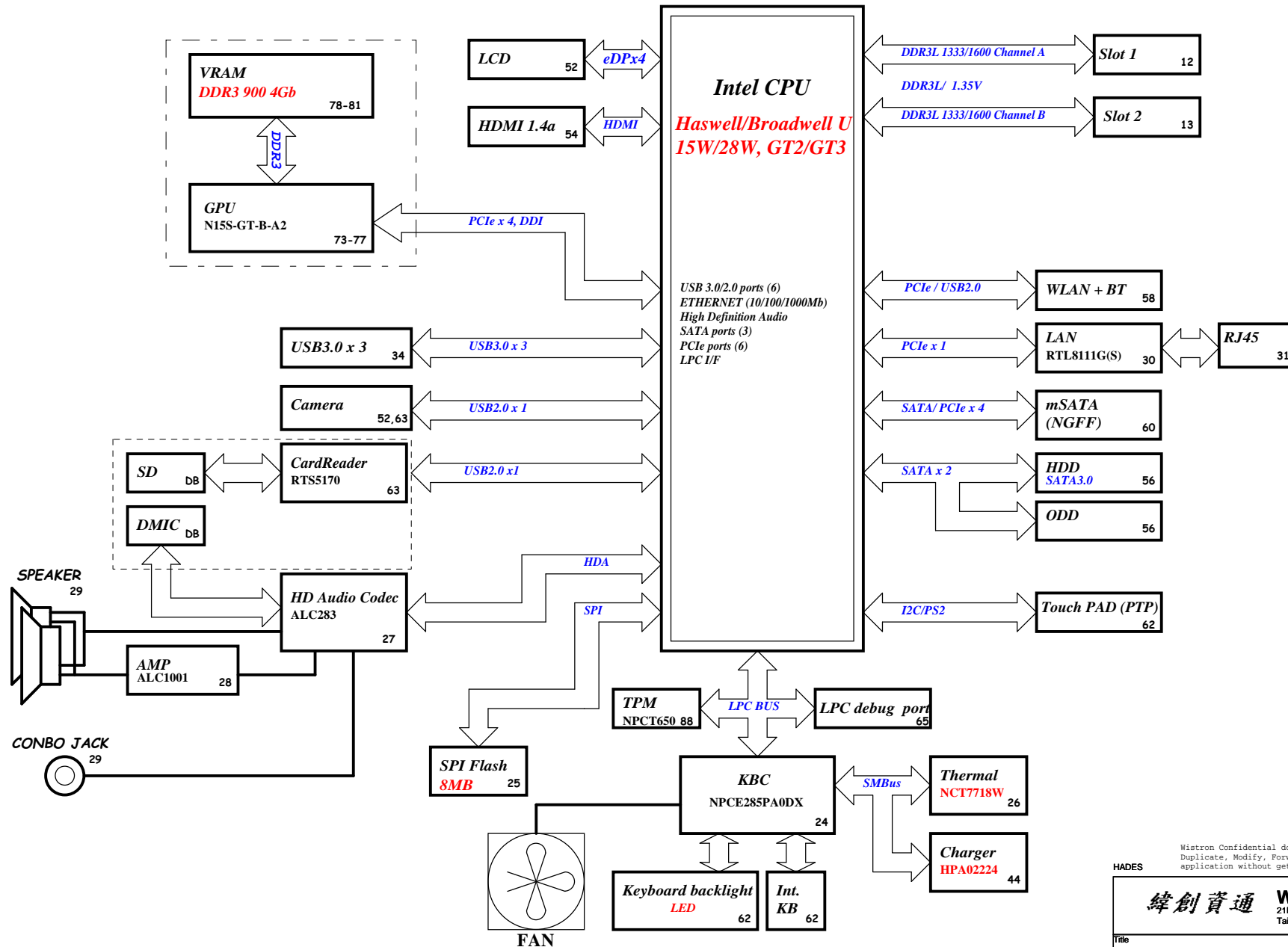
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Title			
Cover Page			
Size A4	Document Number Hades 840M ULT		Rev -1
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Hades ULV Board Block Diagram


Project code : 4PD02F010001

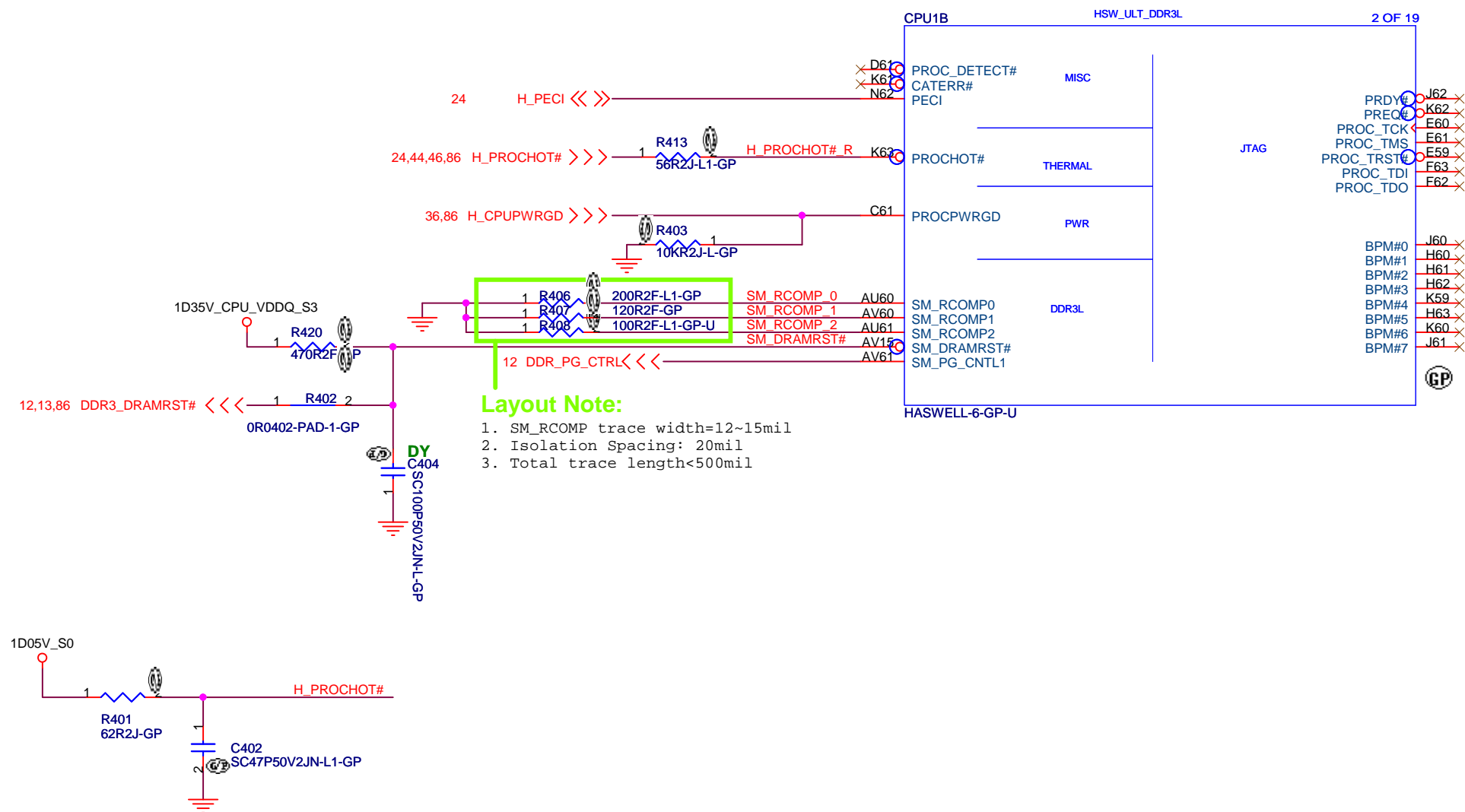
PCB P/N : 14205

Revision : -1



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CPU (THERMAL/CLOCK/PM)Size
A4

Document Number

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Rev	-1
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Date: Wednesday, April 30, 2014

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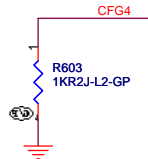


SSID = CPU

Pin Name	System Pull-up/Pull-down	Schematic Notes	✓
CFG[19:0]		Please refer to the <i>Crescent Bay and (??) Platforms - Debug Port Design Guide (DPDG)</i> .	

Note: Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

eDP Enable	
CFG4	1:Disable
	0:Enable



Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	<p>Configuration Signals:</p> <p>The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none"> • CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes. • PCI Express® Static x16 Lane Numbering Reversal. — — • • CFG[4]: eDP enable <ul style="list-style-type: none"> — 1 = Disabled — 0 = Enabled • [19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands. 	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

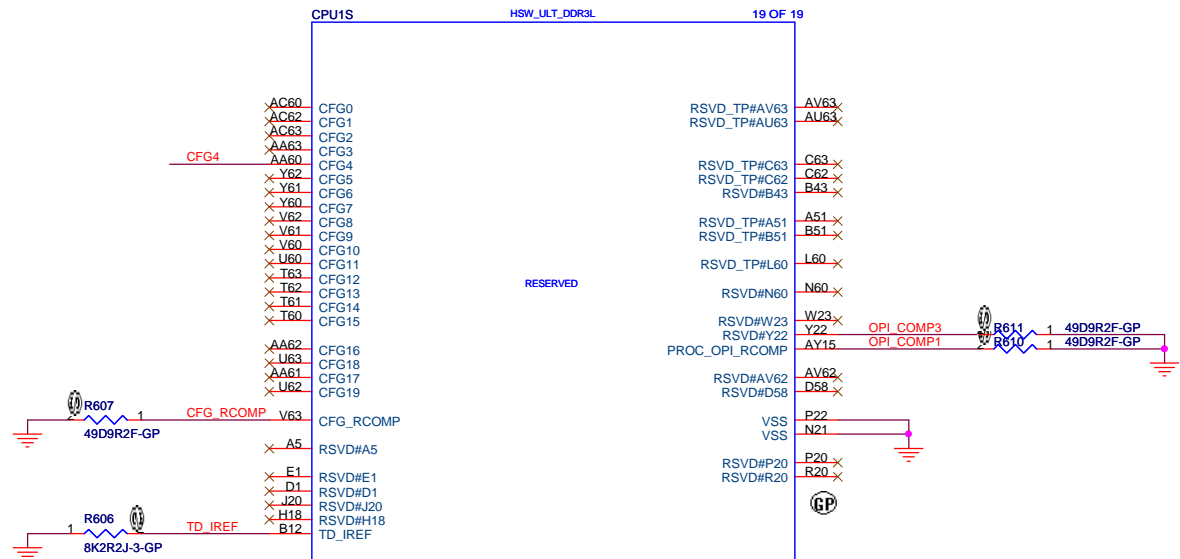
continued...

continued...

7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected

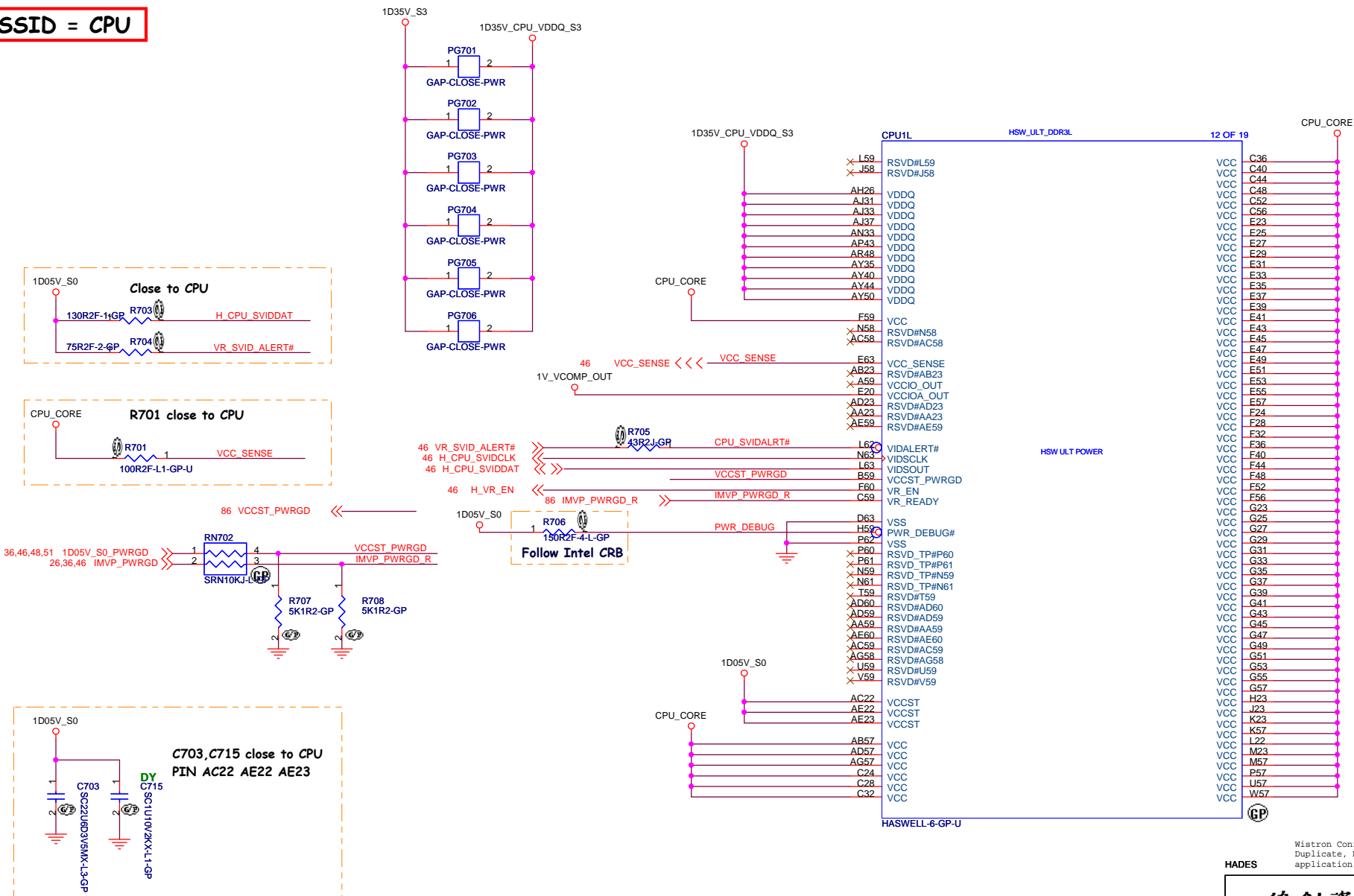


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SSID = CPU



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Size

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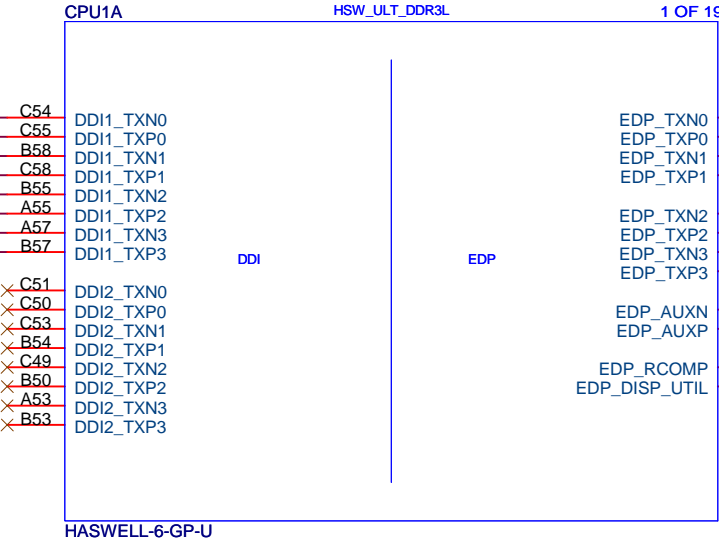
Date: Wednesday, April 30, 2014

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SSID = CPU

HDMI

54 HDMI_DATA_CPU_N2 <<
54 HDMI_DATA_CPU_P2 <<
54 HDMI_DATA_CPU_N1 <<
54 HDMI_DATA_CPU_P1 <<
54 HDMI_DATA_CPU_N0 <<
54 HDMI_DATA_CPU_P0 <<
54 HDMI_DATA_CPU_N3 <<
54 HDMI_DATA_CPU_P3 <<



C45 EDP_TXN0 >>> eDP_TX_CPU_N0 52
B46 EDP_TXP0 >>> eDP_TX_CPU_P0 52
A47 EDP_TXN1 >>> eDP_TX_CPU_N1 52
B47 EDP_TXP1 >>> eDP_TX_CPU_P1 52

C47 EDP_TXN2 >>> eDP_TX_CPU_N2 52
C46 EDP_TXP2 >>> eDP_TX_CPU_P2 52
A49 EDP_TXN3 >>> eDP_TX_CPU_N3 52
B49 EDP_TXP3 >>> eDP_TX_CPU_P3 52

A45 EDP_AUXN >>> eDP_AUX_CPU_N 52
B45 EDP_AUXP >>> eDP_AUX_CPU_P 52

eDP
eDP x4 reserve

Layout Note:
Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

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CPU (DDI/EDP)

Size A4

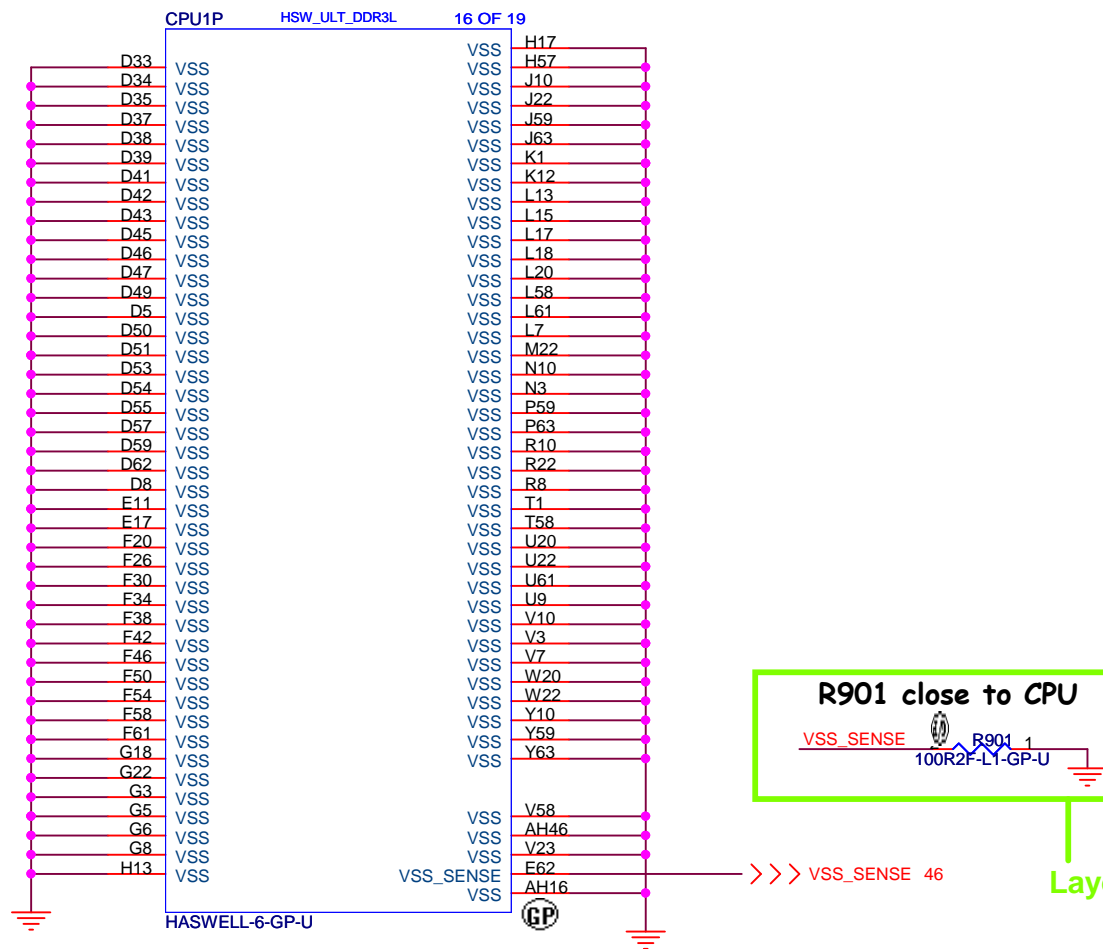
Document Number

Rev -1

Date: Wednesday, April 30, 2014

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SSID = CPU



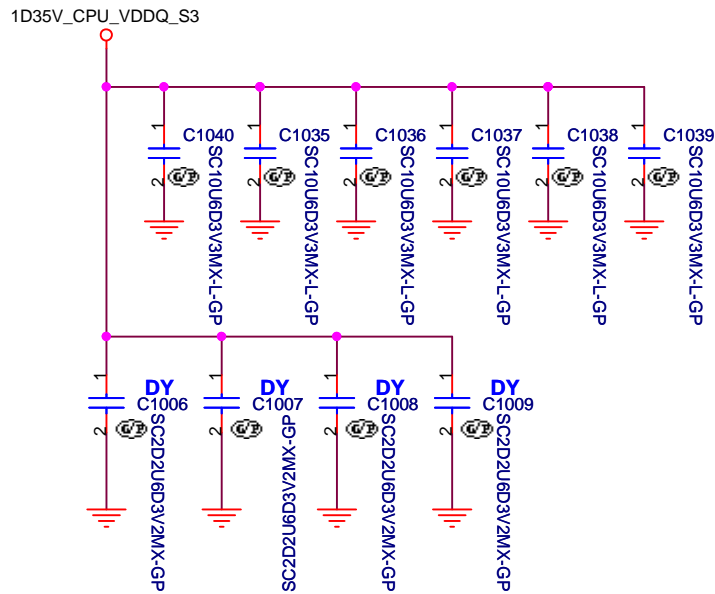
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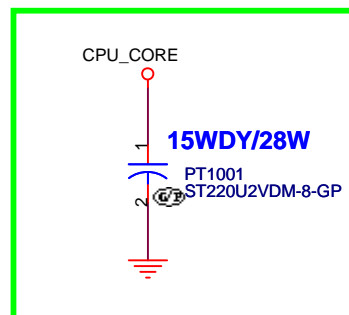
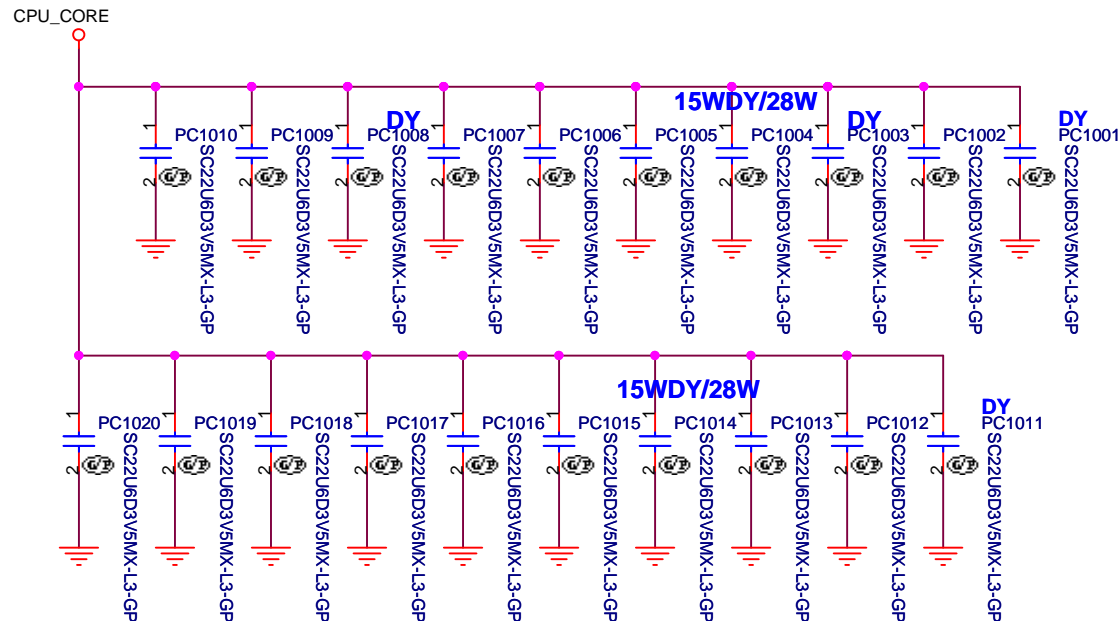
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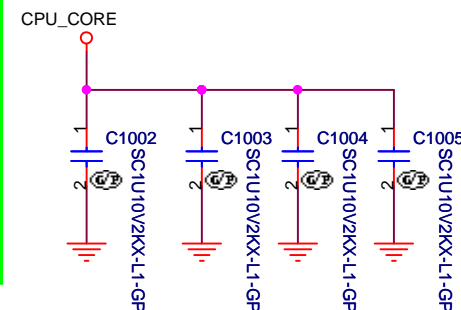
Title		
CPU (VSS)		
Size A4	Document Number Hades 840M ULT	Rev -1
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For Intel Recommend EE Part



SB 20140402



For Intel Recommend EE Part

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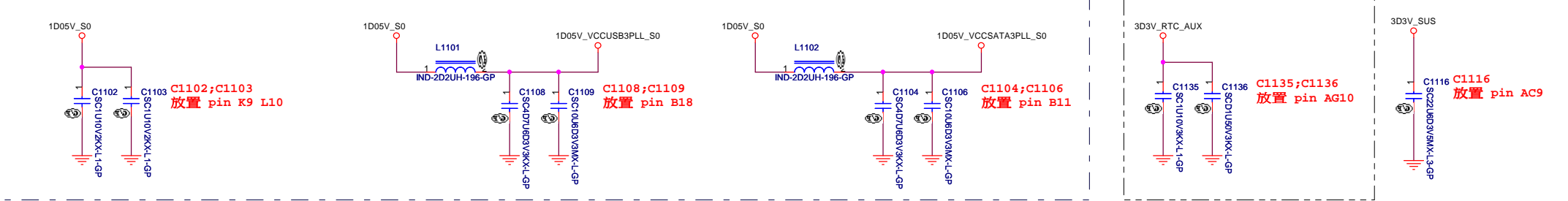
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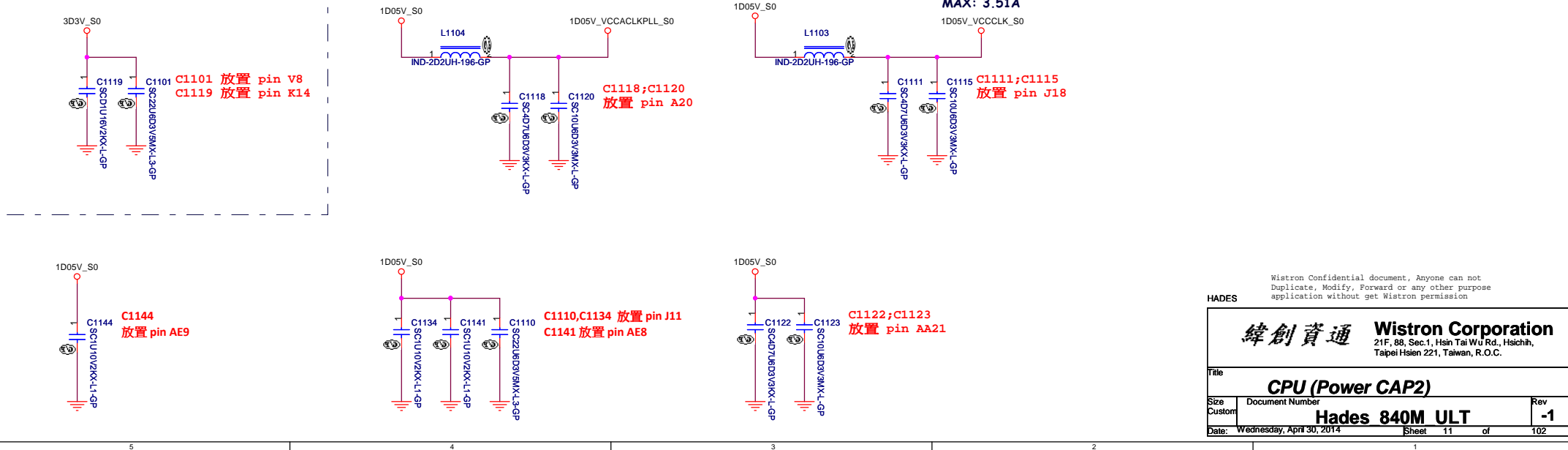
Title		
CPU (Power CAP1)		
Size	Document Number	Rev
A4	Hades 840M ULT	-1
Date:	Wednesday, April 30, 2014	Sheet 10 of 102

擺放電容的位置請參考 Page 21,每個位置如下

MAX: 1.92A



MAX: 0.285A

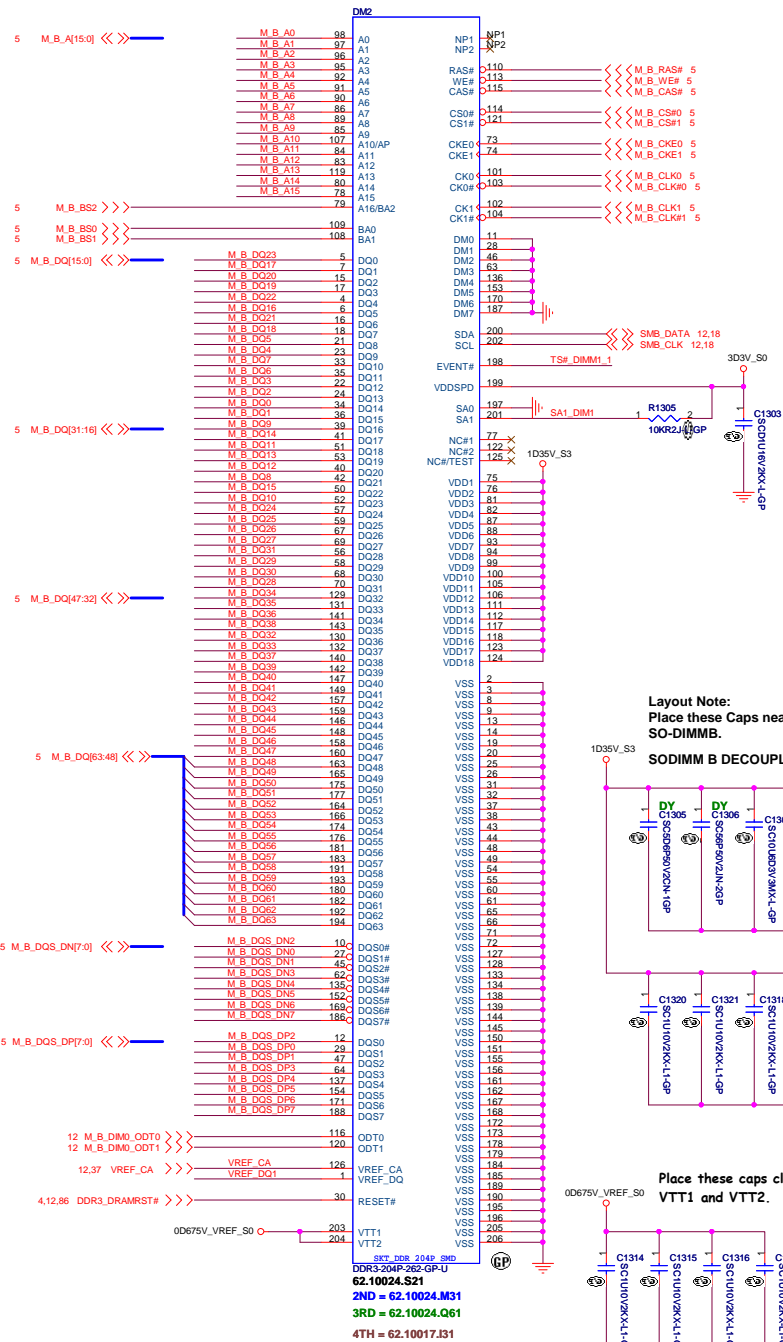


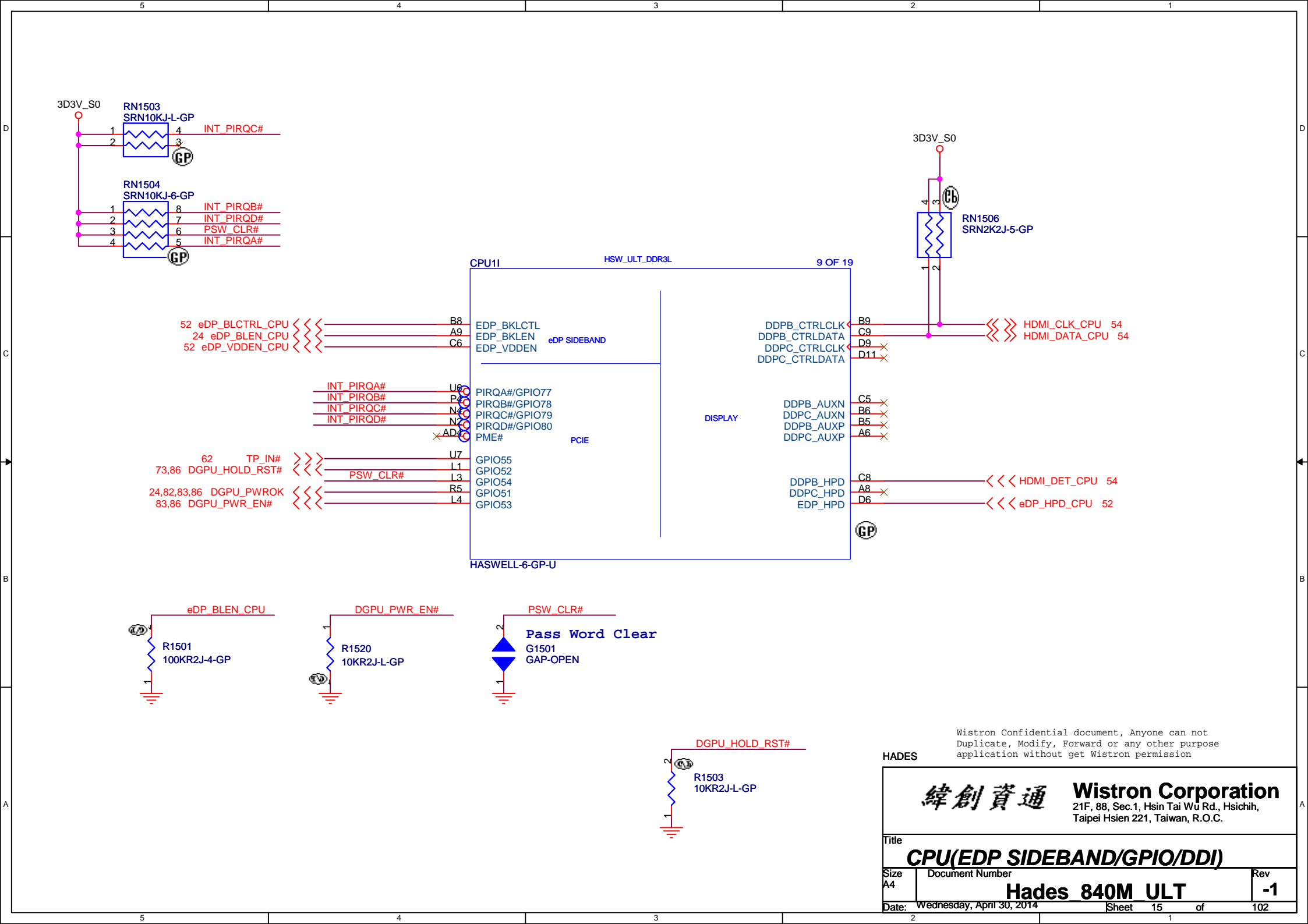
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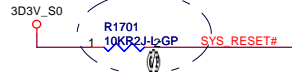
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Title		
CPU (Power CAP2)		
Size	Document Number	Rev
Custom	Hades 840M ULT	-1
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SSID = MEMORY



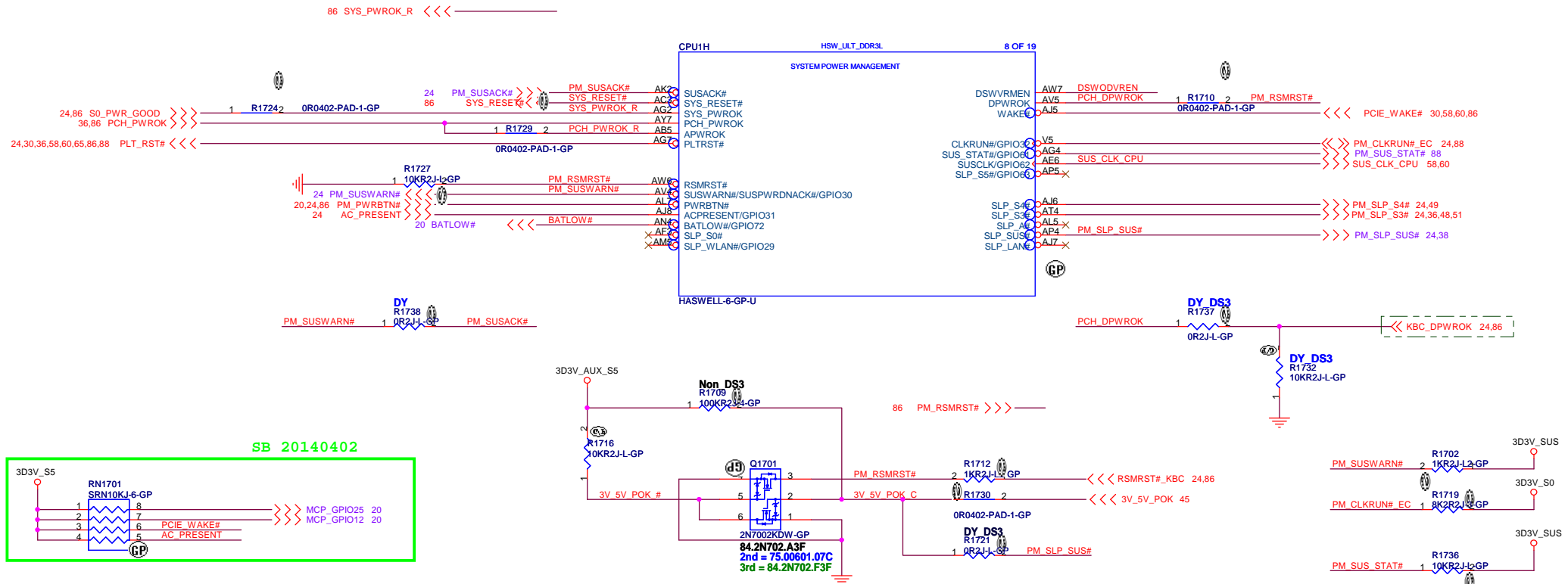




Bit	Description
31:3	Reserved
2	<p>WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN) - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0':</p> <ul style="list-style-type: none"> Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. <p>NOTE: Deep Sx disabled configuration must leave this bit at '0'.</p>

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

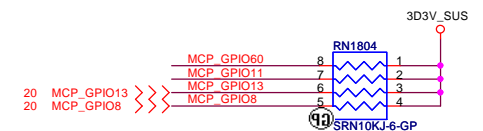
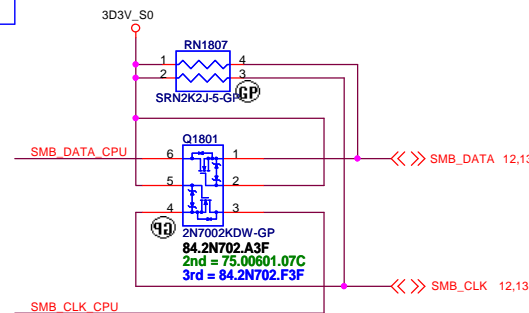
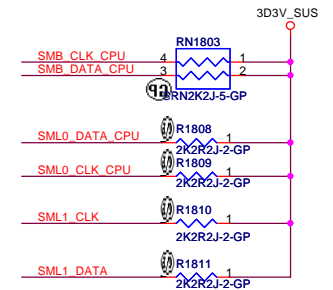
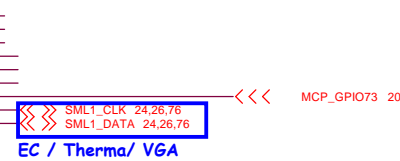
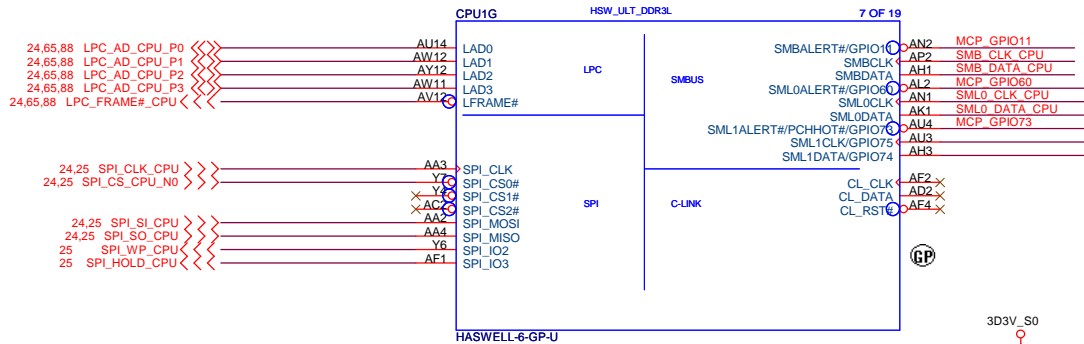
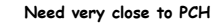
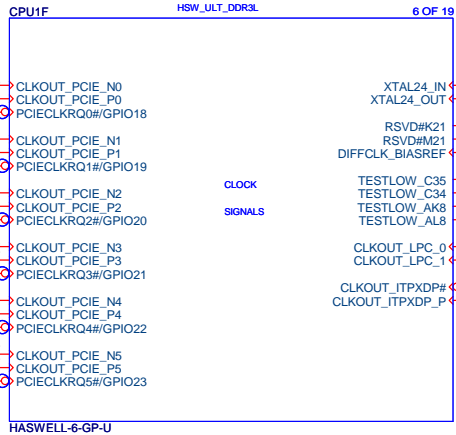
The diagram illustrates the connection of the DSWODVREN pin to the 330KR2JH-GP component. The DSWODVREN pin is connected to the R1718 pin of the component, which is also connected to ground. The R1717 pin of the component is connected to the 3D3V_RTC_AUX pin.



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CPU (DMI/FDI/PM)			
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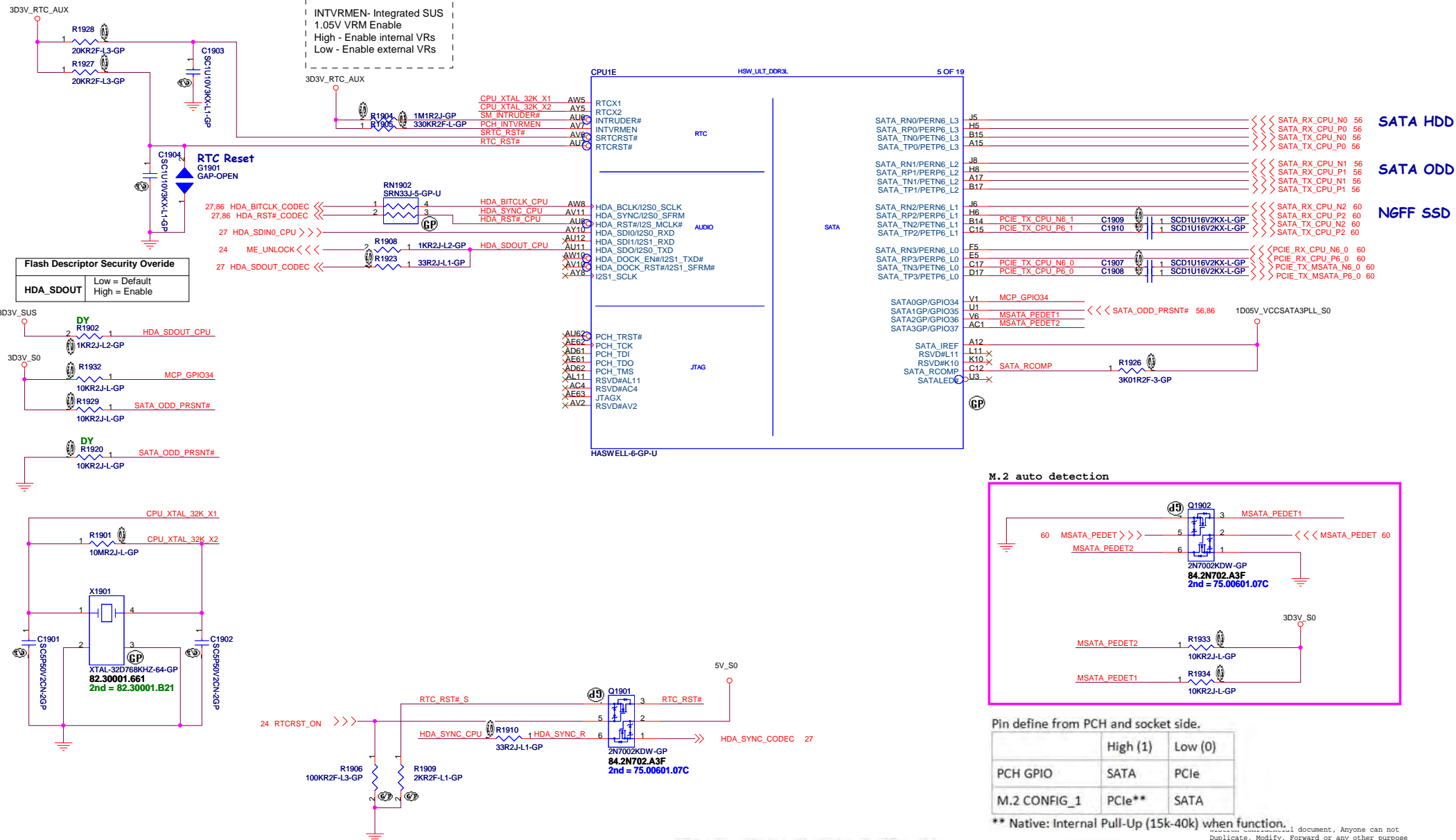
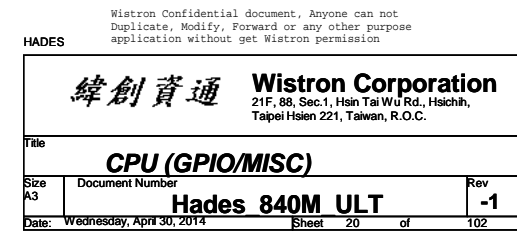
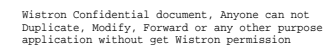


Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes				Module Type and Main Host Interface ¹	Port Configuration ²
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	N/C	GND	GND	SSD - PCIe	N/A



1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to [Section 41.3, "Loop Inductance Reduction Decoupling" on page 532](#).



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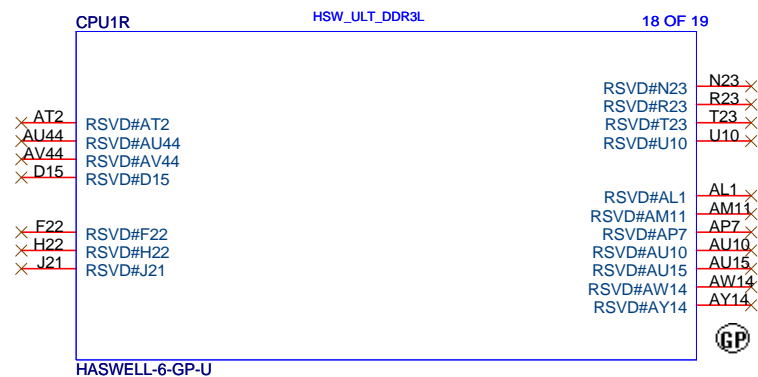
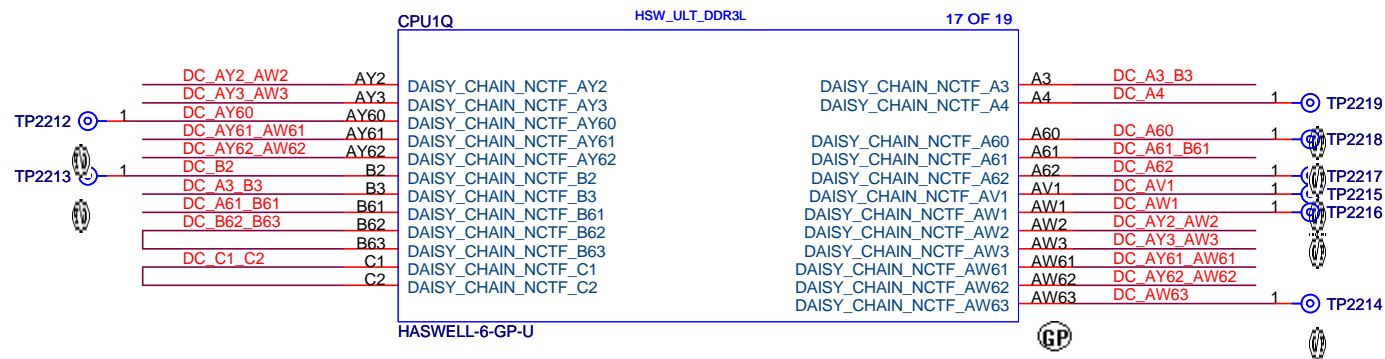
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CPU (POWER1)

Hades 840M ULT

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Title

CPU (RSVD)

Size Custom

Document Number

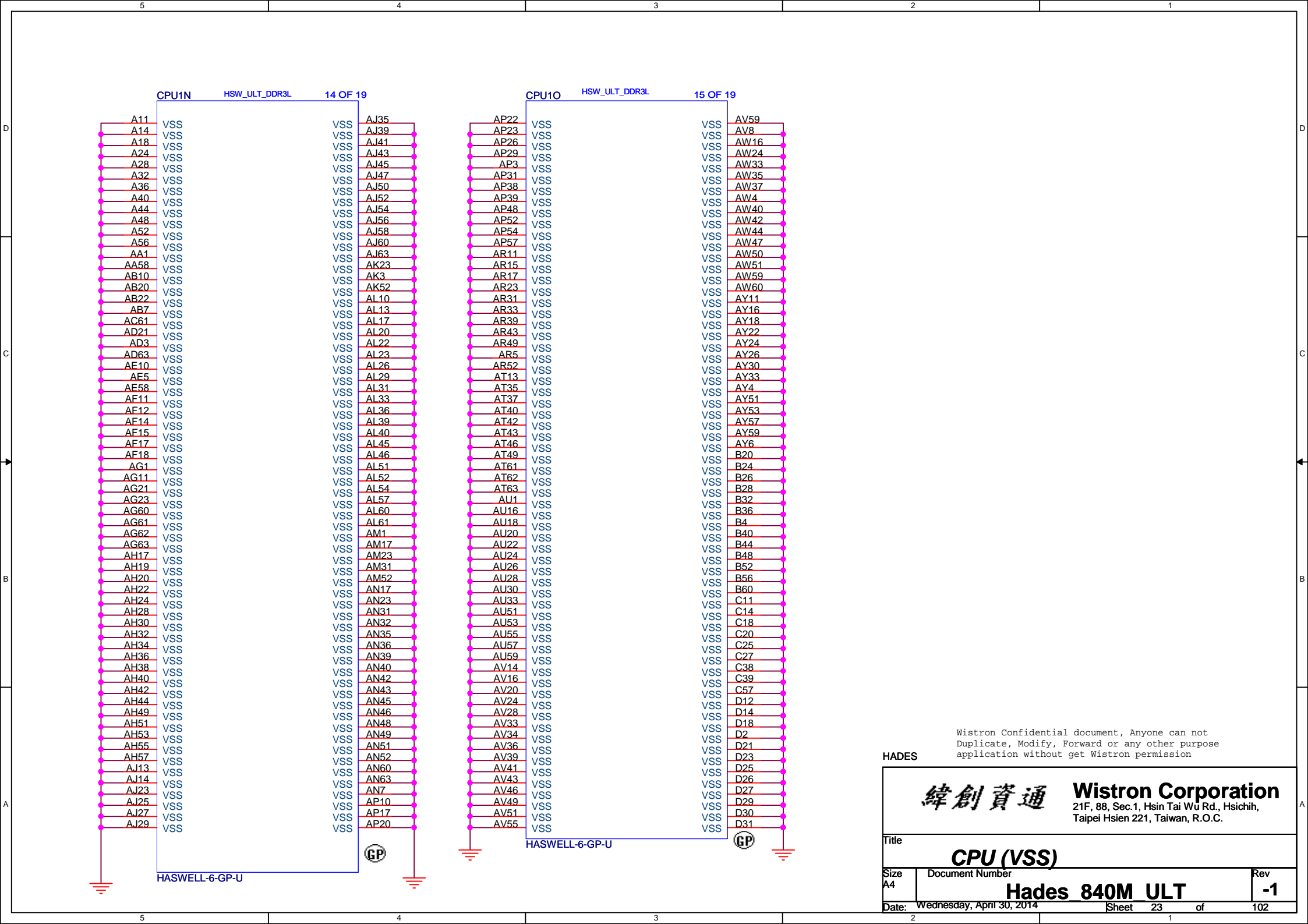
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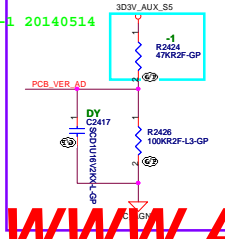
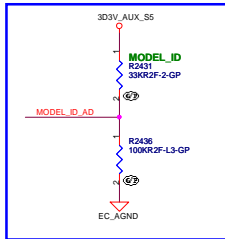
Sheet 23 of 102

SSID = KBC

BATTER /CHARGER---->
Thermal/eDP/GPU---->

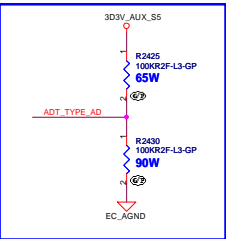
Touch Pad----

20K : 64.20025.LOL



Model ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
VA30	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V
Hades UNA	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V
Hades DIS 840	100.0 K	33.0 K	2.481 V	2.4935	< 2.616 V
Hades DIS 850	100.0 K	47.0 K	2.245 V	2.2592	< 2.363 V
Hades DIS 860	100.0 K	64.9 K	2.001 V	2.0169	>= 1.934 V
Posidon DIS 840	100.0 K	76.8 K	1.867 V	1.8827	>= 1.758 V
Posidon DIS 860	100.0 K	100.0 K	1.650 V	1.6665	>= 1.504 V
Posidon DIS 870	100.0 K	143.0 K	1.358 V	1.3740	>= 1.281 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	>= 1.126 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	>= 0.524 V

Model ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	>= 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591	>= 2.616 V
SC	100.0 K	33.0 K	2.481 V	2.4935	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.2592	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	>= 1.934 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	>= 1.758 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	>= 1.504 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	>= 1.281 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	>= 1.126 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	>= 0.524 V



Model ID	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting
65W	N/A	100.0 K	3.300 V		>= 3.000 V
89W	100.0 K	N/A	0.000 V		< 0.150 V
30W	100.0 K	100.0 K	0.300 V	0.3055	>= 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.5592	>= 0.684 V
120W	33.0 K	100.0 K	0.812 V	0.8312	>= 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.0695	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.3146	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.6665	>= 1.542 V

WWW.AliSaler.Com

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

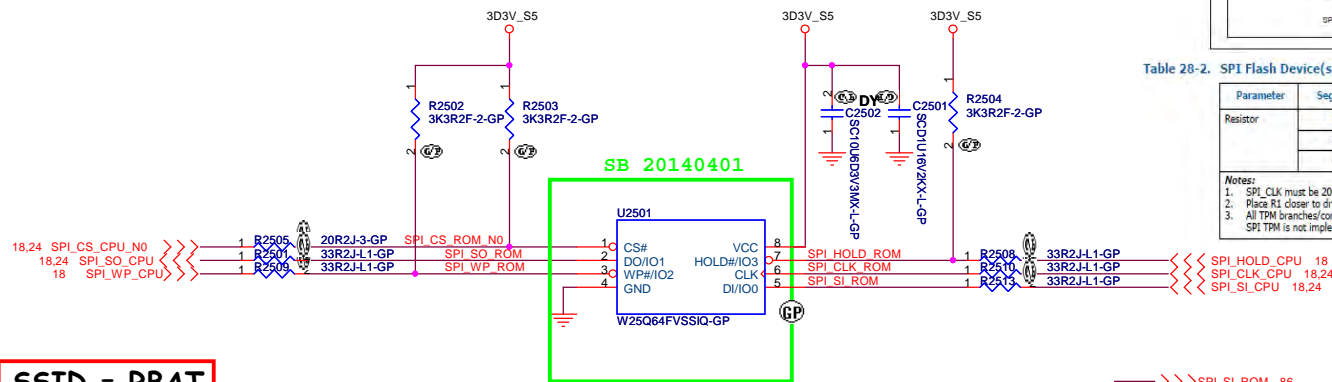
SPI FLASH ROM (8M byte)

```
1ST= 072.02564.0001(AMIC A25LQ64M)
```

2ND=072.25B64.0001(Gigadevice GD25B64BSIGR)

purge=72.25Q64.K01 (WINBOND W25Q64FVSSIQ)

72.25647.00A (MXIC MX25L6473EM2I)



SSID = RBAT

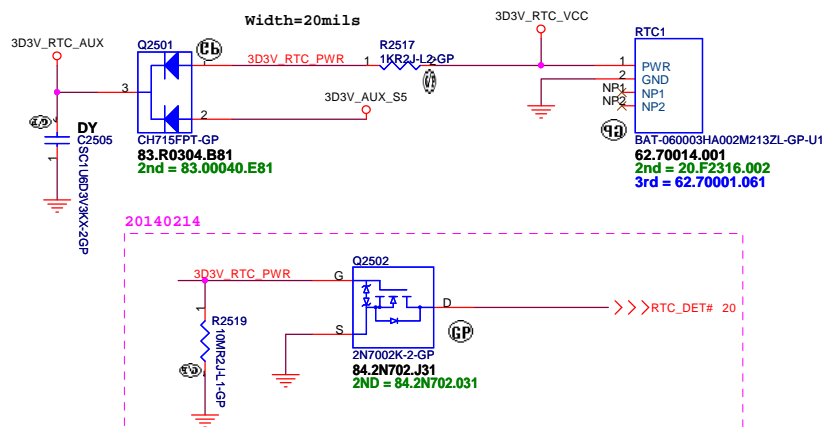


Figure 28-1. SPI Topology (Single Device)

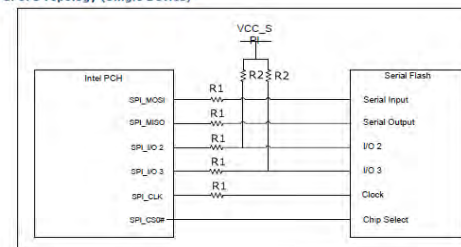


Table 28-2. SPI Flash Device(s) and TPM Routing Guideline (Sheet 2 of 2)

Parameter	Segment	Stackup	Unit	Routing Recommendation
Resistor	R1		ohm	15
	R2		ohm	1k
	R3		ohm	33

Notes:

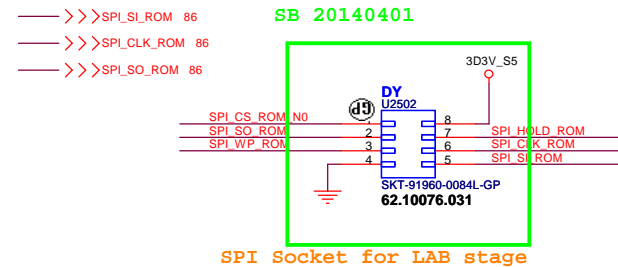
- SPL_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.
- Place R1 closer to driver side to effectively dampen undershoot and overshoots.
- All TPM branches/connections (TPM_MOST, TPM_MISO, TPM_CLK, and PCH_CS2#) can be left as NC since SPL TPM1 is not implemented.

Notes

1. SPI_CLK must be 20 mils spacing from any other high frequency (>1 GHz) signal.
2. Place R1 closer to driver side to effectively dampen the undershoot and overshoot.

3. All TPM branches/connections (TPM_MOSI, TPM_MISO, TPM_CLK, and PCH_CS2#) can be left as NC.

SPI TPM is not implemented.



SPI Socket for LAB stage

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Title

Flash(KBC+PCH)/RTC

Size

	Document Number
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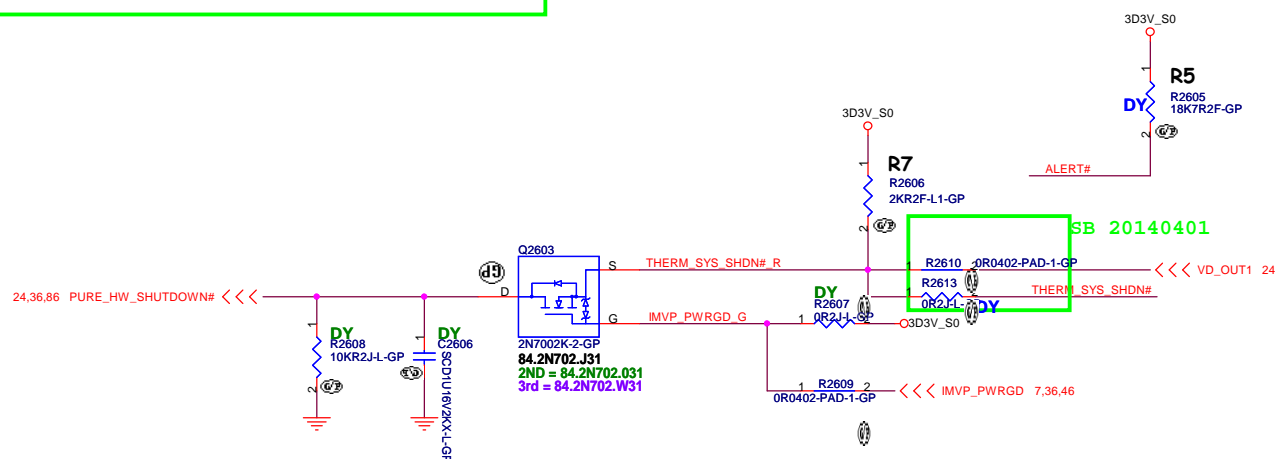
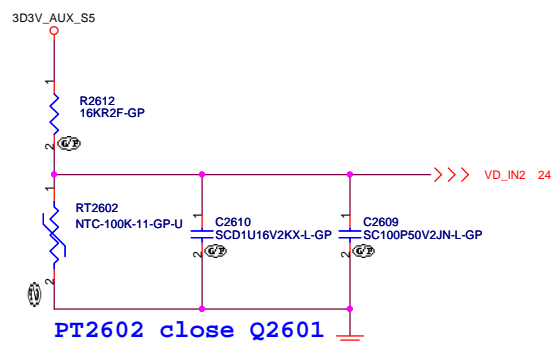
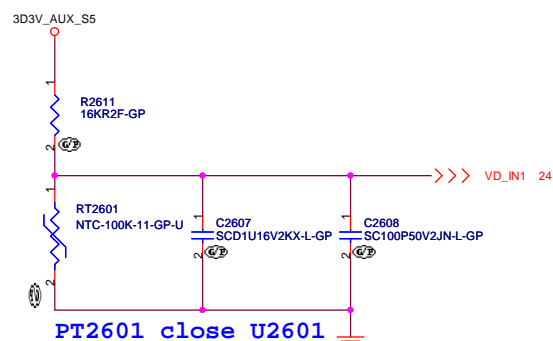
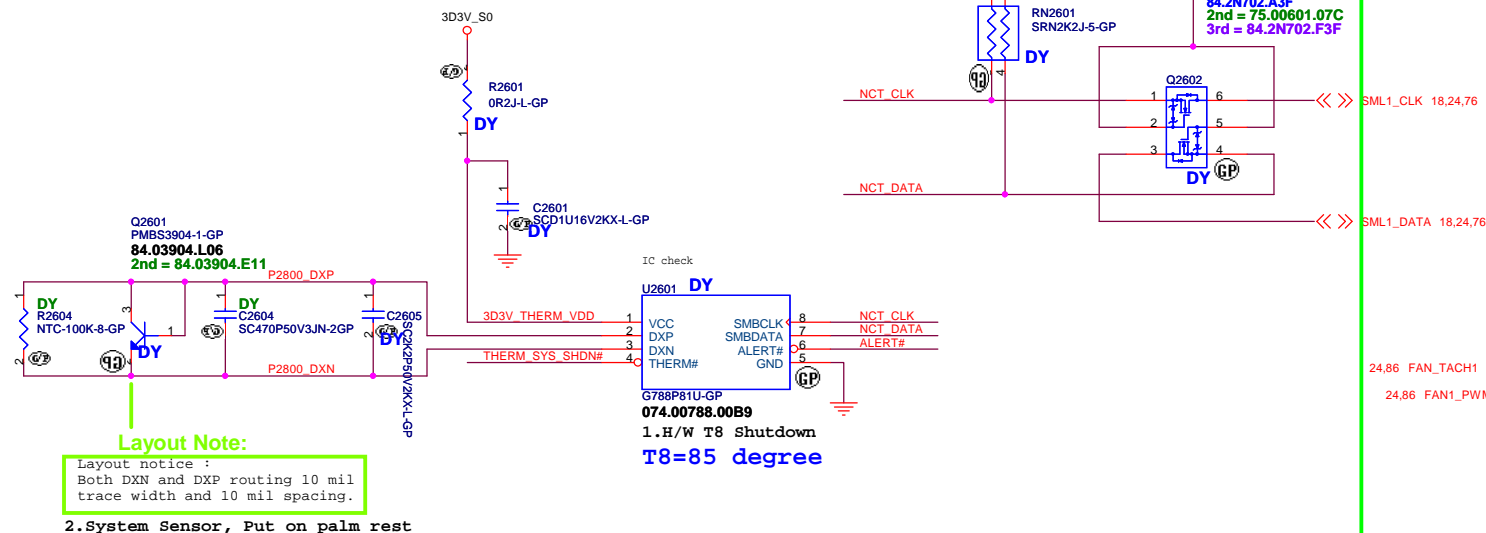
Hades_840M_ULT

Date: Wednesday, April 30, 2014

Sheet 25 of 102

Rev

Thermal sensor G788



ALERT# /T CRIT#
Pull-up Resistor

	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

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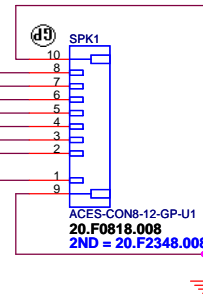
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Size	Document Number	Hades 840M ULT	
A3		Rev	-1
Date: Wednesday, May 14, 2014	Sheet	26	of 102

SSID = AUDIO

Speaker

Layout Note:
Trace width=40mil

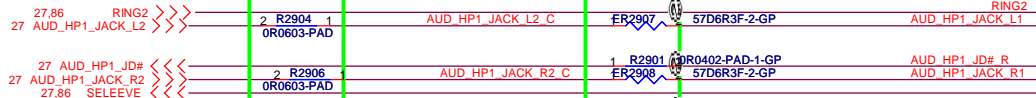
28,86 AMP_SPK1_L- >>>
28,86 AMP_SPK1_L+ >>>
27,86 AUD_SPK1_L- >>>
27,86 AUD_SPK1_L+ >>>
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27,86 AUD_SPK1_R+ >>>



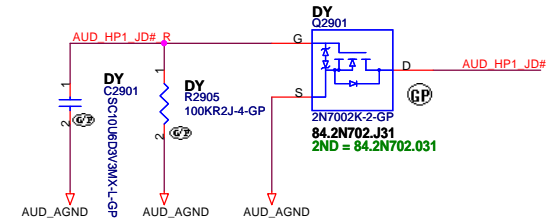
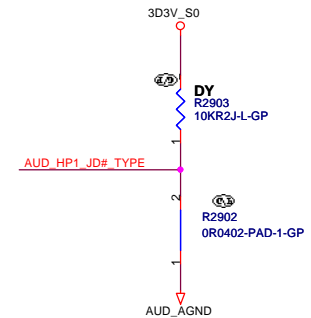
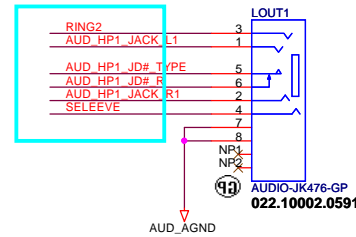
Combo Jack

SB 20140410

SB 20140410



-1 20140522



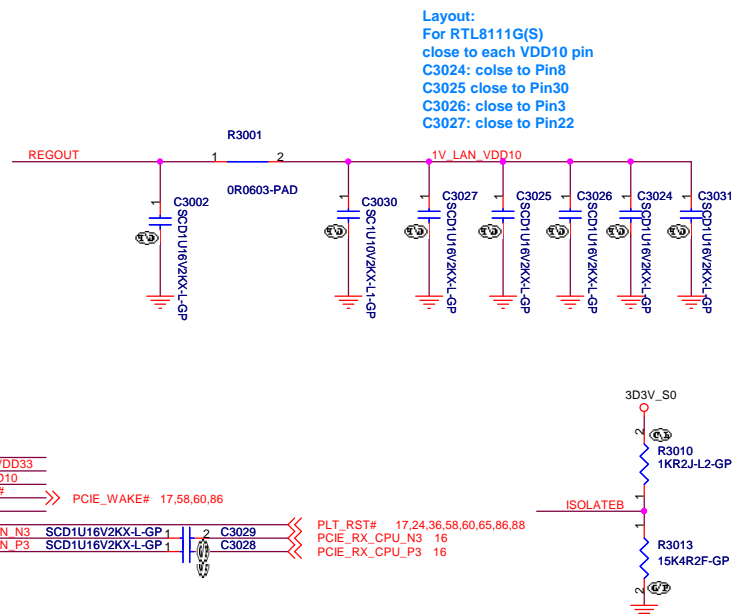
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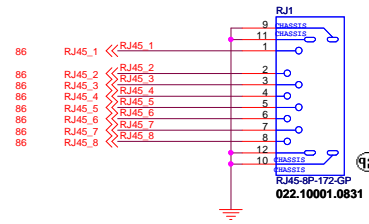
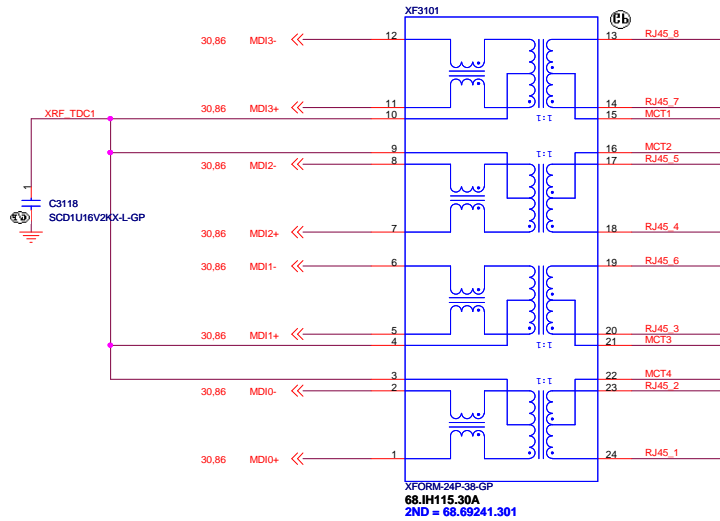
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Size	Document Number	Rev
Custom	Hades 840M ULT	-1
Date:	Thursday, May 22, 2014	Sheet 29 of 102

C3008: close to Pin32
C3007: close to Pin11 (RTL8111 only)

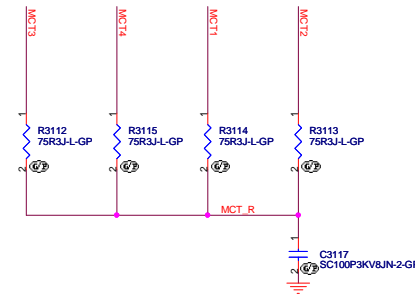
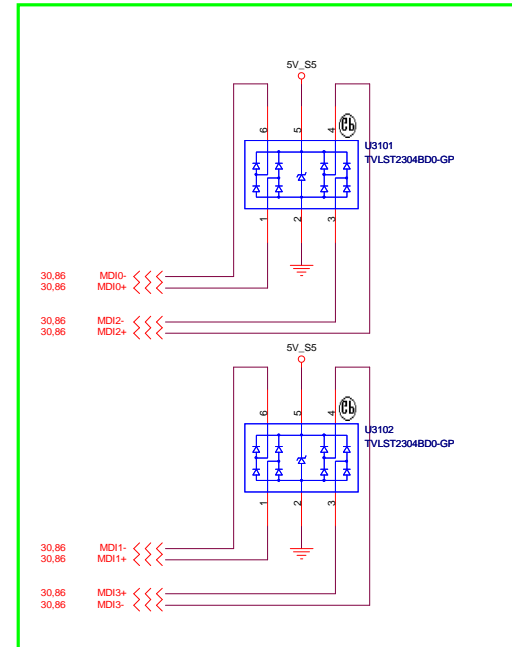


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Size A3	Document Number		Rev
	Hades 840M ULT		-1
Date:	Wednesday, April 30, 2014	Sheet 30 of	102

SSID = LAN

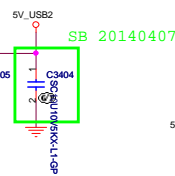
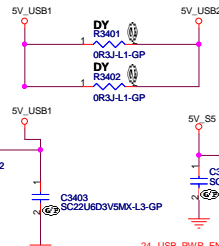


SB 20140328 FOR POE ISSUE

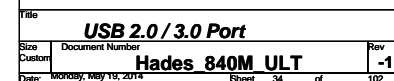
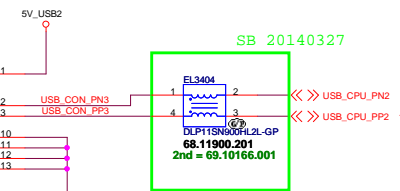
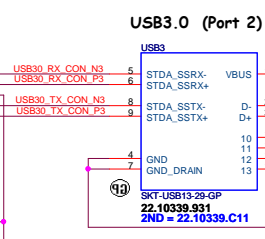
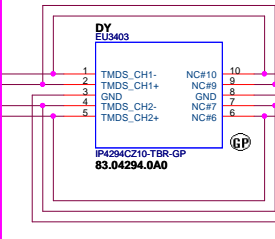
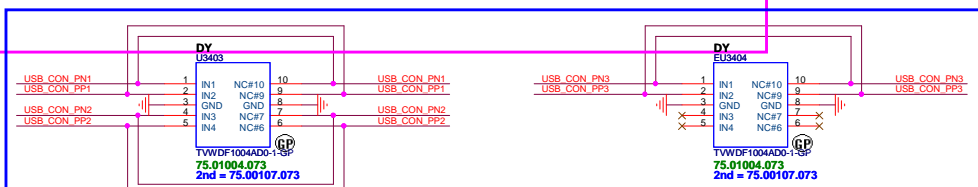


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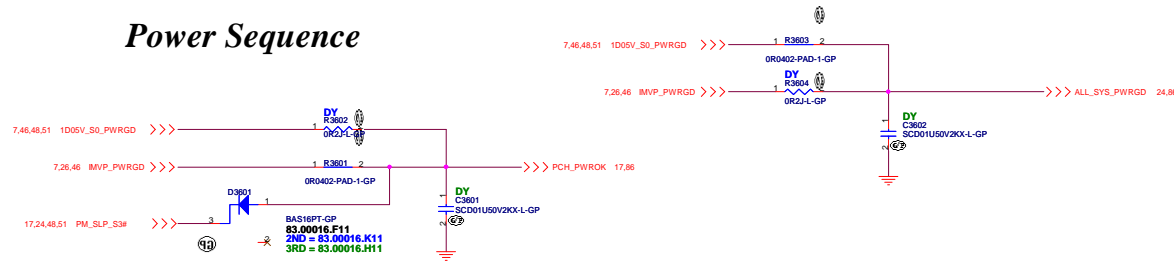
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(LAN+VGA) CONNECTOR		
Size	Document Number	Rev
Custom	Hades 840M ULT	-1
Date	Wednesday, April 30, 2014	Sheet 31 of 102



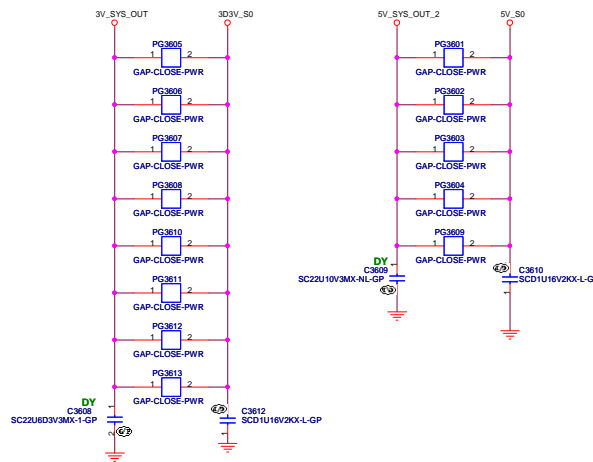
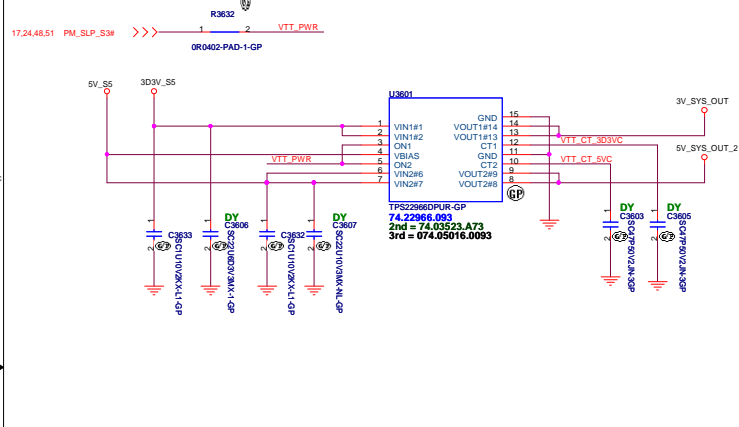
1	<i>POWER</i>	
2	<i>USB 2.0 D-</i>	
3	<i>USB 2.0 D+</i>	
4	<i>GND</i>	
5	<i>StdA_SSRX-</i>	<i>SuperSpeed RX</i>
6	<i>StdA_SSRX+</i>	
7	<i>GND</i>	
8	<i>StdA_SSTX-</i>	<i>SuperSpeed TX</i>
9	<i>StdA_SSTX+</i>	



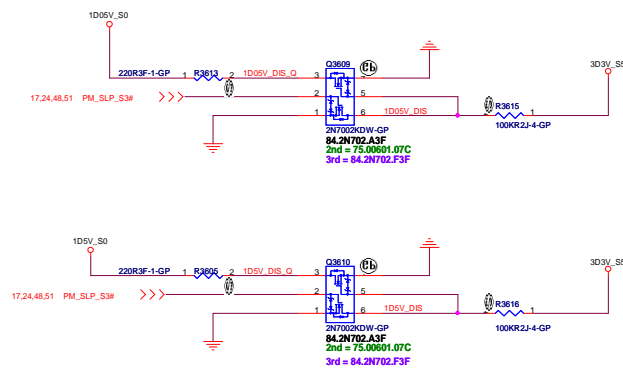
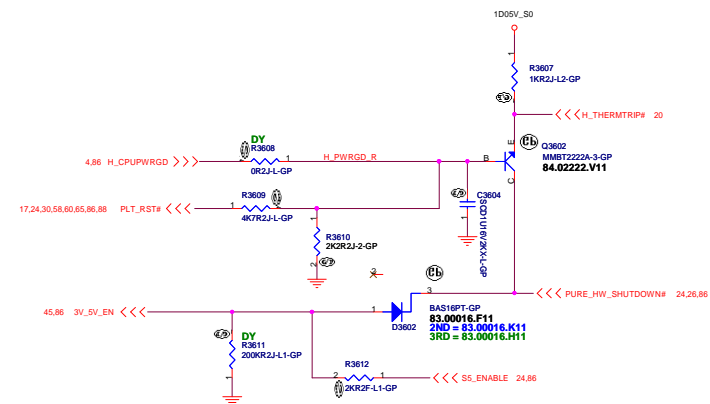
Power Sequence

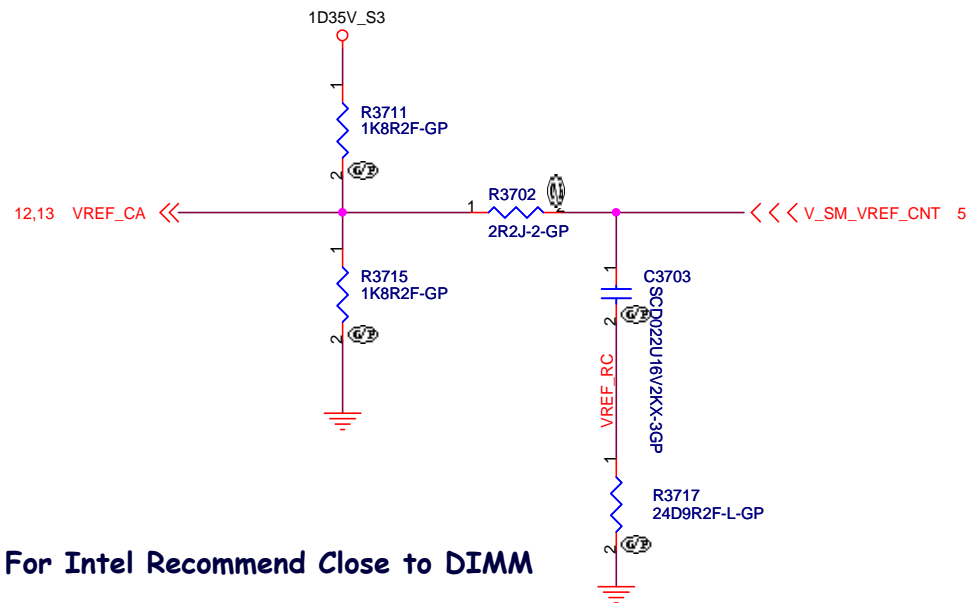


ANNIE Run Power



Discharge circuit





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Title

ADAPTER OCP / S3 reduction

Size
Custom

Document Number

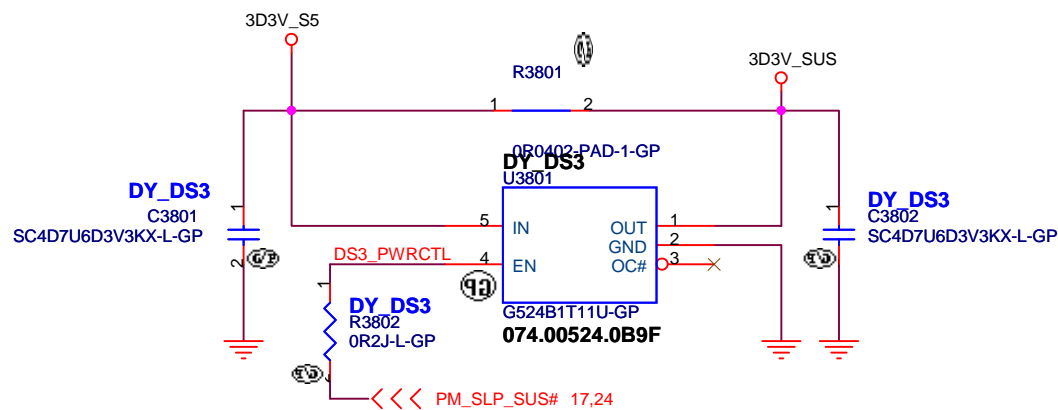
Hades 840M ULT

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-1

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Title

DS3

Size
A4

Document Number

Hades 840M ULT

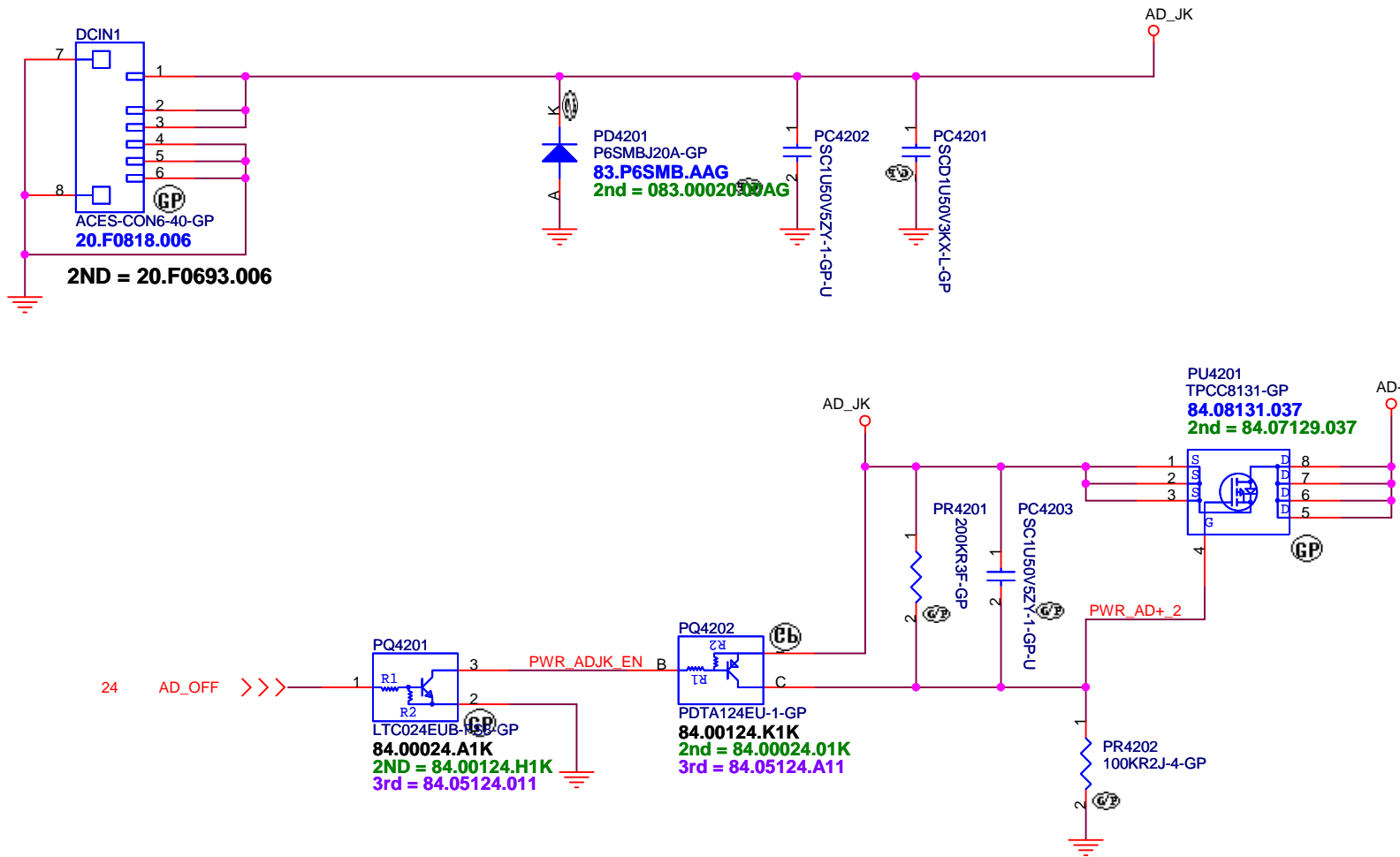
Rev
-1

Date: Wednesday, April 30, 2014

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ANNIE solution

Adaptor in to generate DCBATOUT



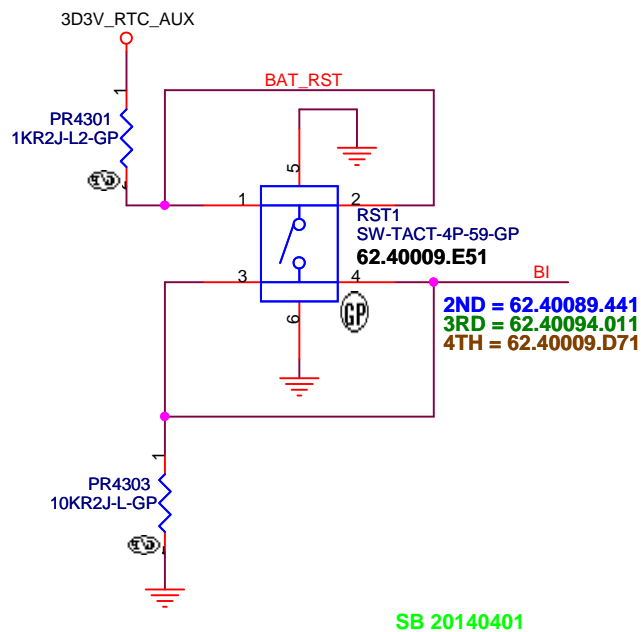
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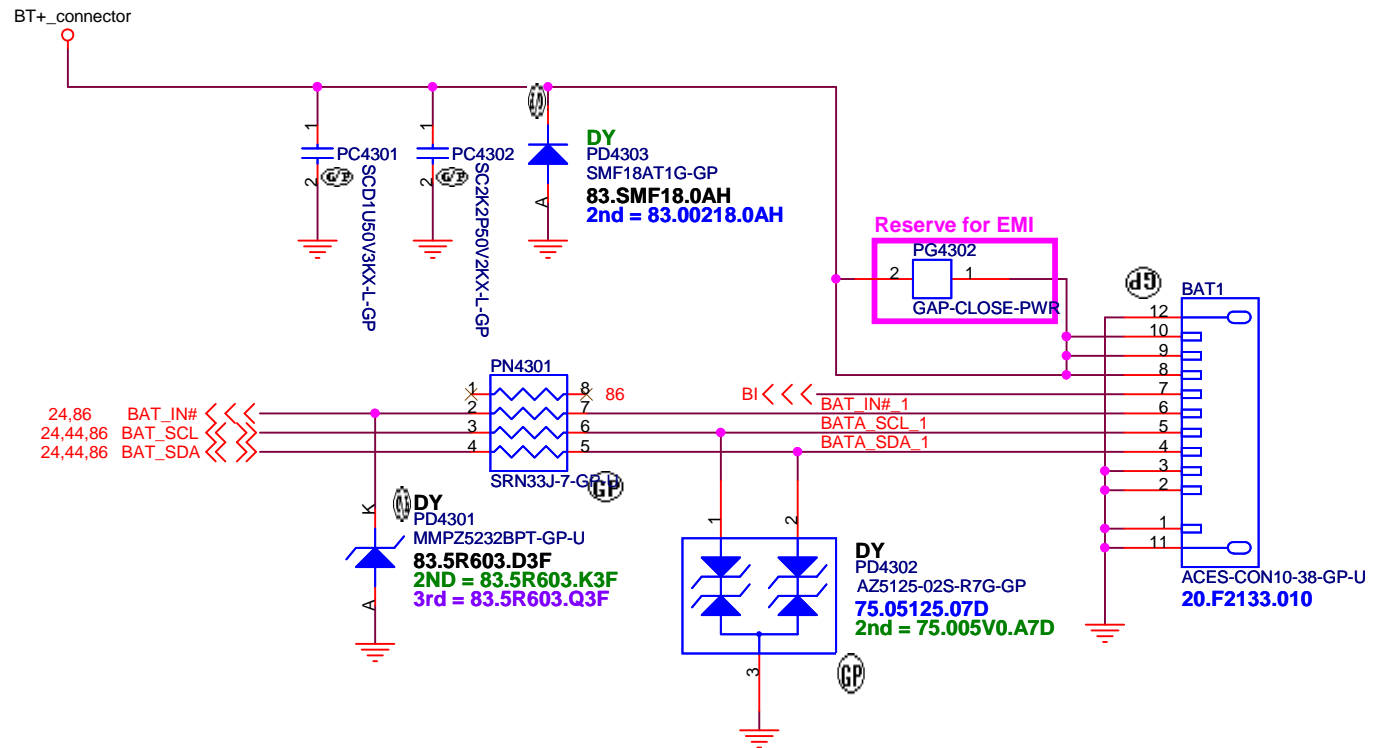
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DCIN JACK		
Size	Document Number	Rev
A4	Hades 840M ULT	-1
Date:	Friday, May 16, 2014	Sheet 42 of 102

Battery Reset



Battery Insert

Battery Connector



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Title

BATT CONN

Size
A4

Document Number

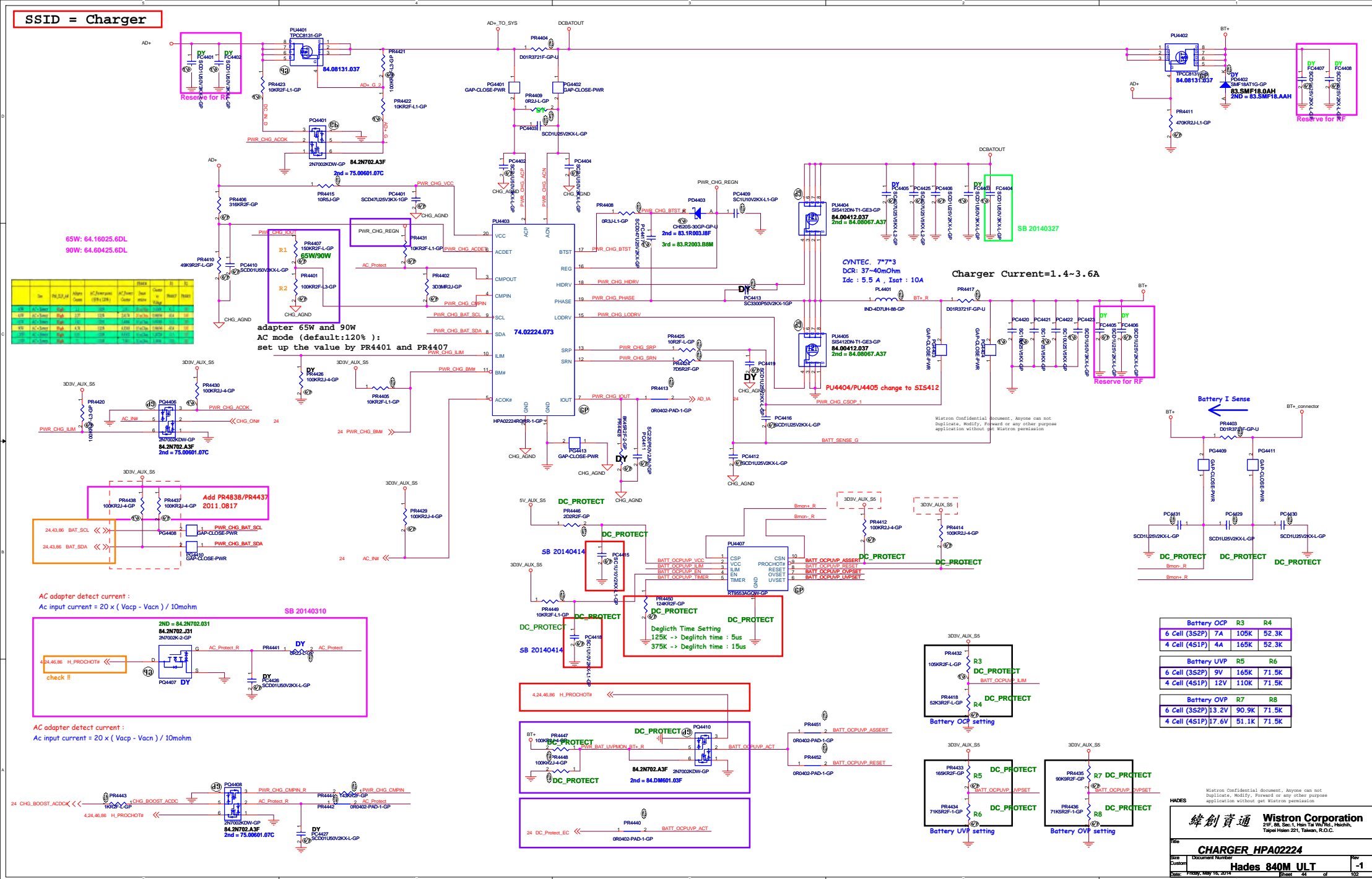
Hades 840M ULT

Rev
-1

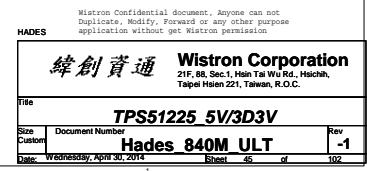
Date: Wednesday, April 30, 2014

Sheet 43 of 102

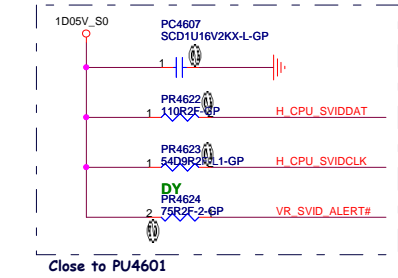
WWW.AliSaler.Com



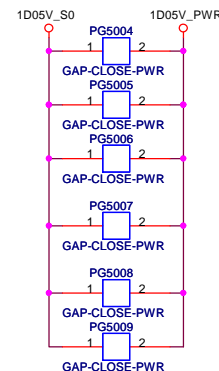
High Side	Low Side	Choke
84.00412.037 SIS412	84.00412.037 SIS412	MagLayers, 7x7x3, 2R2
Vgs @ 4.5V,	Vgs @ 4.5V,	Dcr : 18 ~ 20 mOhm
Id = 12A,	Id = 12A,	Idc : 8A Isat : 14 A
Rds(on) = 24 ~ 30mohm	Rds(on) = 24 ~ 30mohm	



	15W	28W	note
PR4614	680K	523K	Setting IMAX
PR4617	100K	100K	Freq=1.2M Hz
PR4611	475K	383K	15W
PR4612	75K	75K	OCF
PR4607	2K87	2K87	LL
PT1001	DY	Mount	POS-CAP



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Title			
TPS51624 CPUCORE(1/2)			
Size	Document Number		Rev
Custom		Hades 840M ULT	-1
Date:	Thursday, May 15, 2014	Sheet 46 of	102

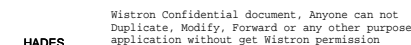


High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

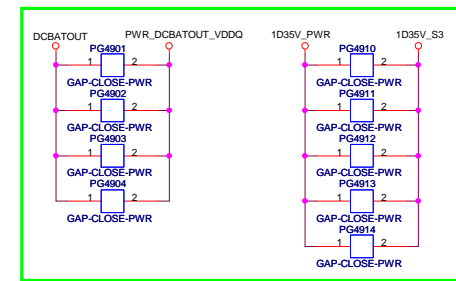


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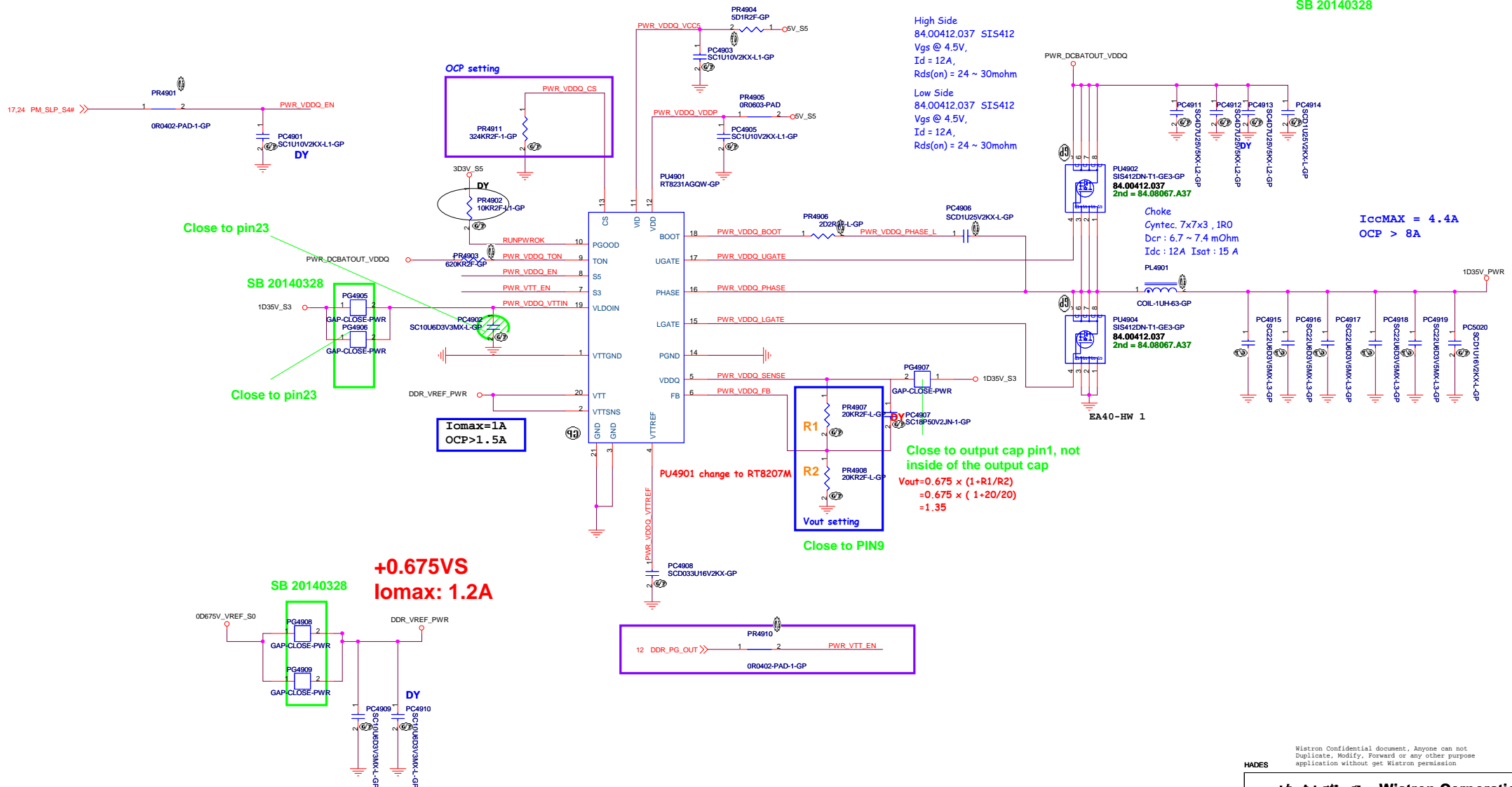
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Size A3	Document Number		Rev
	Hades 840M ULT		-1
Date:	Friday, May 16, 2014	Sheet 48 of	102


```
SSID = PWR.Plane.Regulator_1p2v0p6v
```

RT8231 for VDDQ



SB 20140328

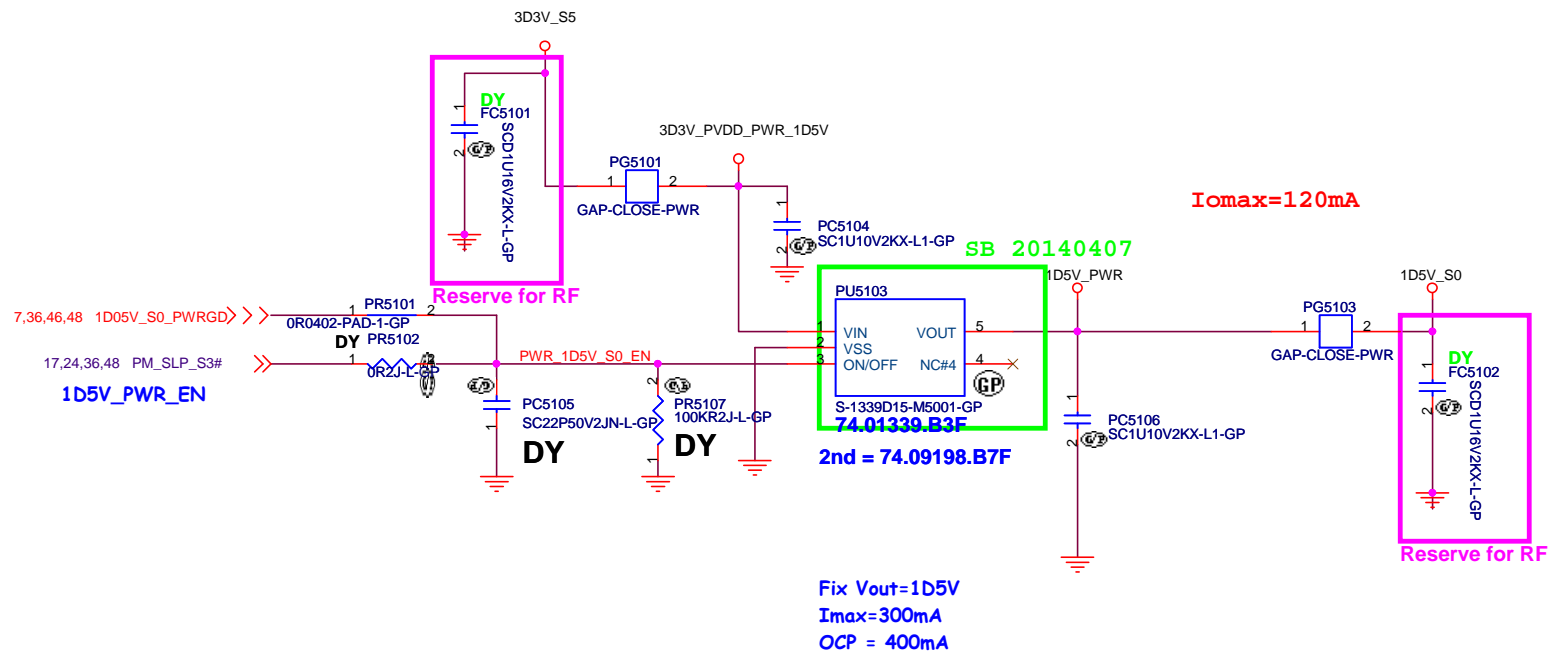


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Title			
RT8231(VDDQ_VTT)			
Size	Document Number		Rev
Custom	Hades 840M ULT		-1
Date:	Wednesday, April 30, 2014	Sheet 49 of	102

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V



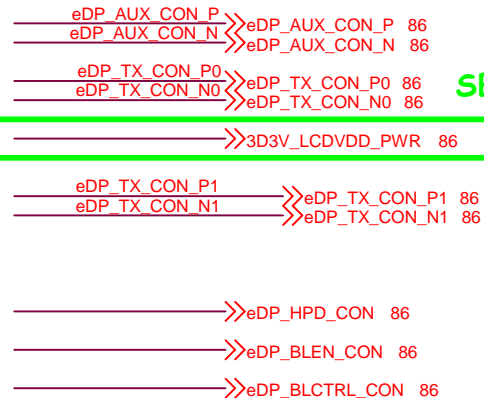
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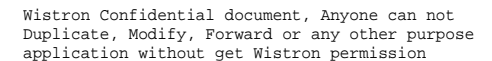
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Size Custom	Document Number	Rev
Hades 840M ULT		-1
Date: Thursday, May 15, 2014	Sheet 51 of	102

SSID = VIDEO



SB 20140401

Inverter Power



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Title

LCD Connector

Size
A4

Document Number

Hades_840M_ULT

Rev 1

Date: Wednesday, April 30, 2014

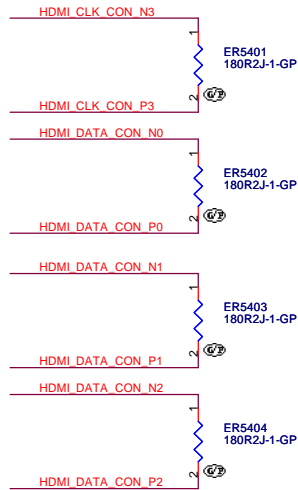
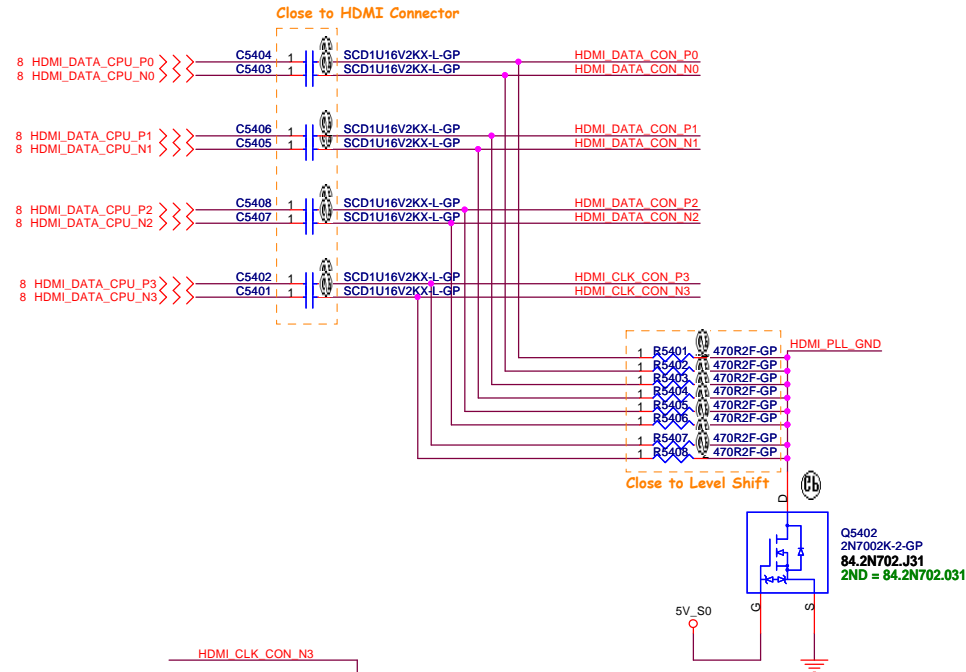
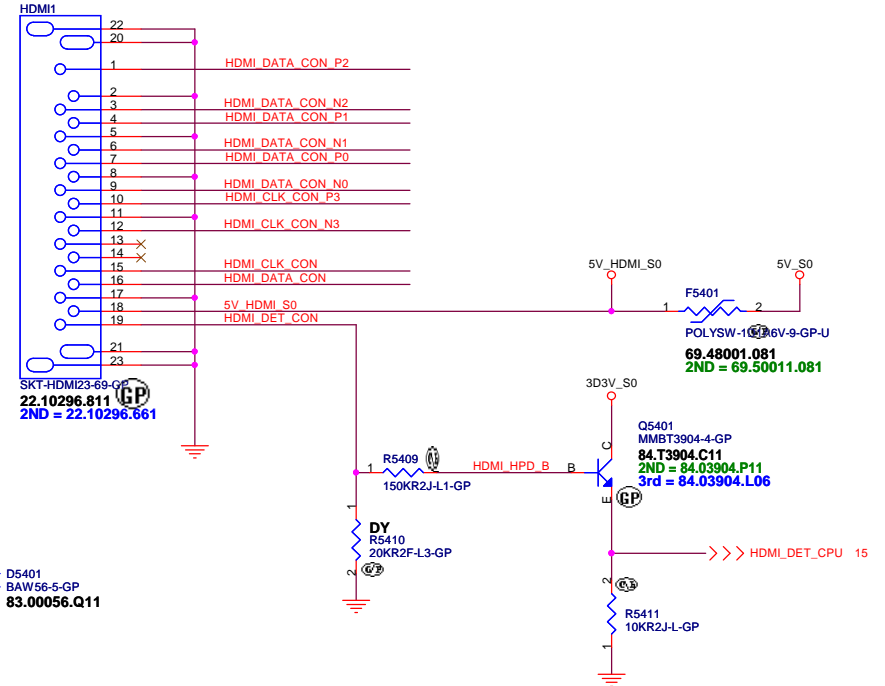
Sheet 52 of 102

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

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HDMI CONN



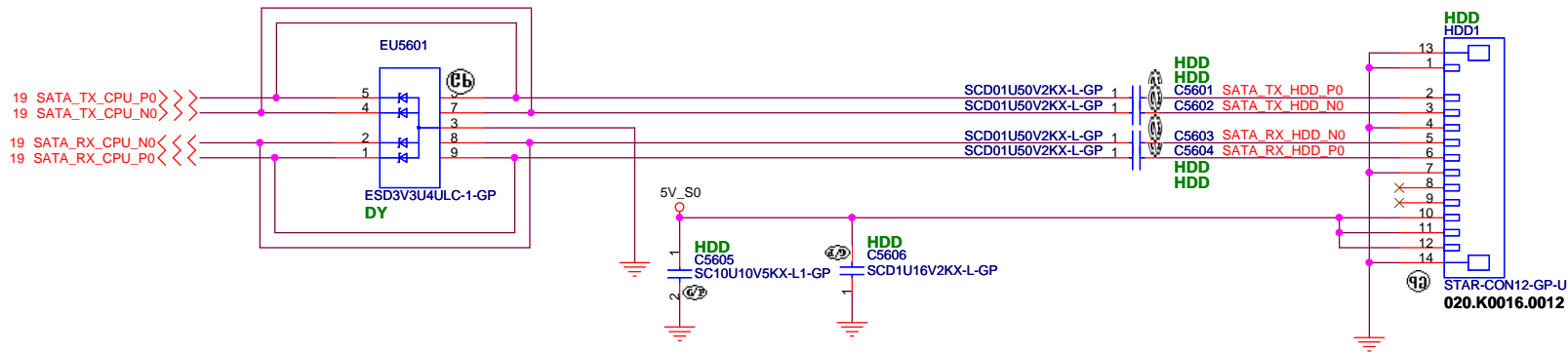
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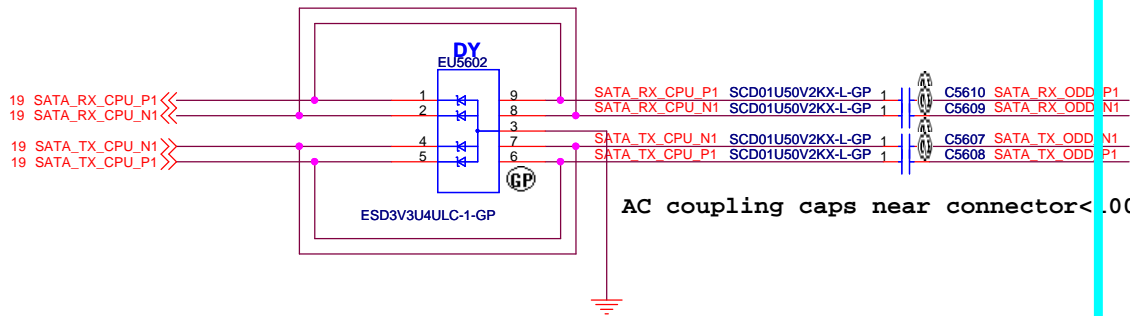
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Size	Document Number	Hades_840M_ULT		Rev
A3				-1
Date:	Friday, May 09, 2014	Sheet	54	of 102

SATA HDD Connector



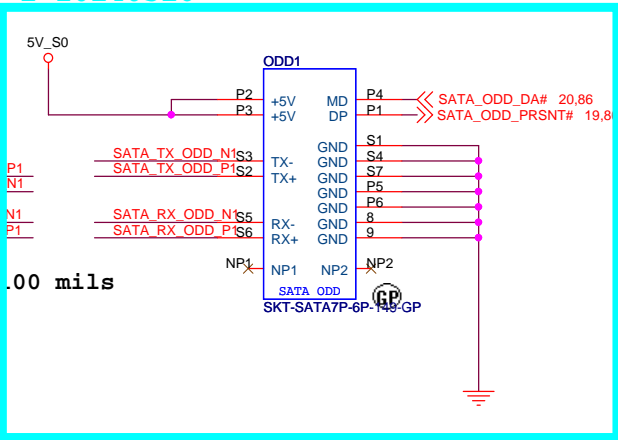
AC coupling caps near connector<100 mils

SATA ODD Connector



AC coupling caps near connector<.00 mils

-1 20140516



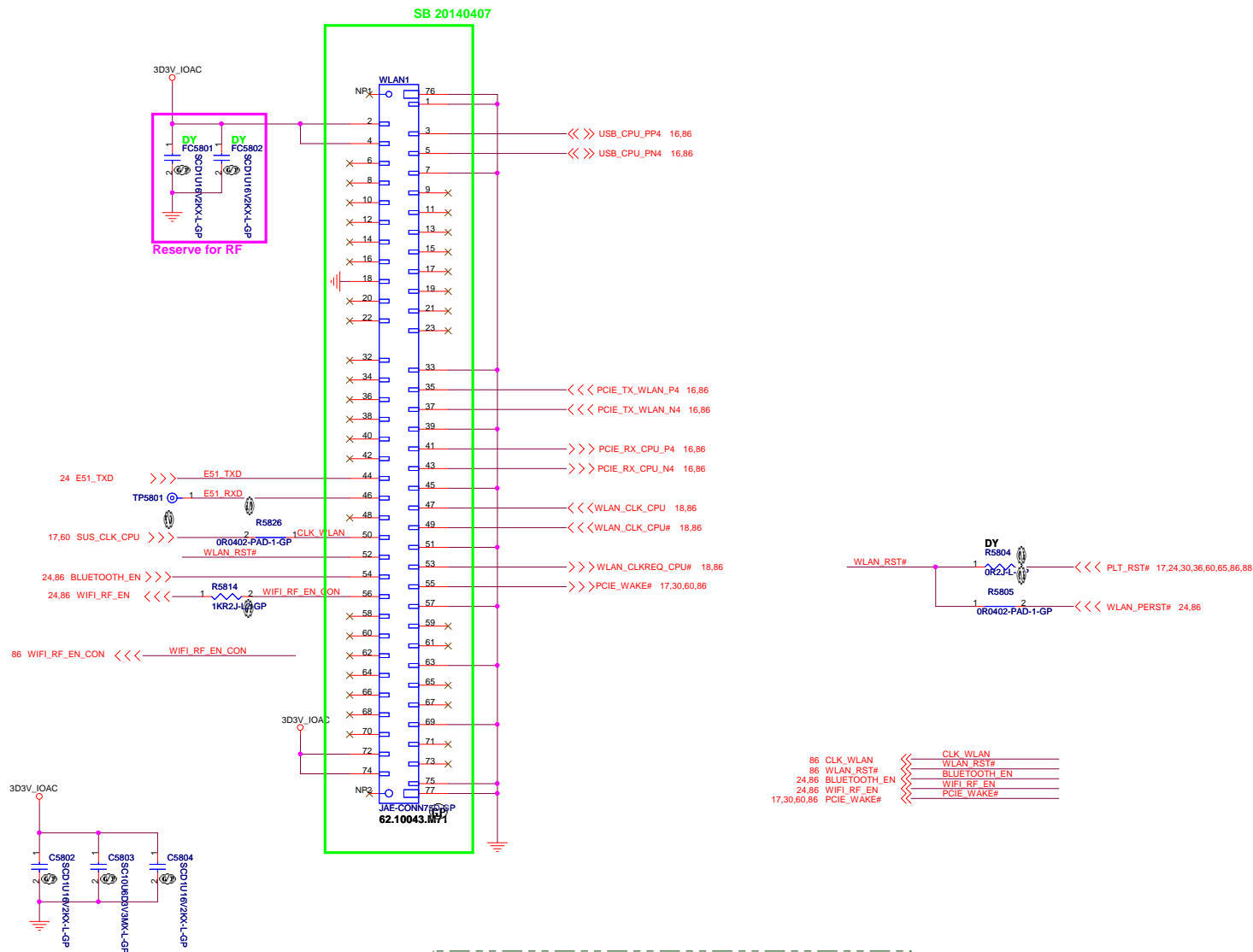
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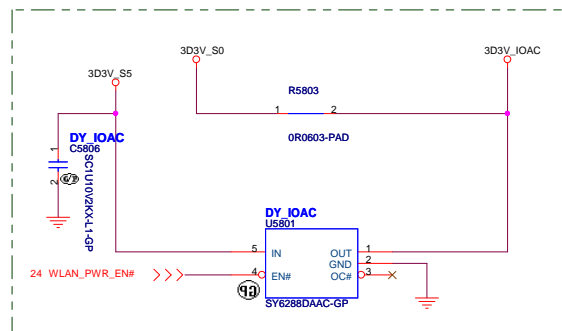
Title		HDD / ODD	
Size	Document Number	Rev	
Custom	Hades 840M ULT	-1	
Date:	Friday, May 16, 2014	Sheet	56 of 102

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



86 CLK_WLAN <<< CLK_WLAN
86 WLAN_RST# <<< WLAN_RST#
24,86 BLUETOOTH_EN <<< BLUETOOTH_EN
24,86 WIFI_RF_EN <<< WIFI_RF_EN
17,30,60,86 PCIE_WAKE# <<< PCIE_WAKE#



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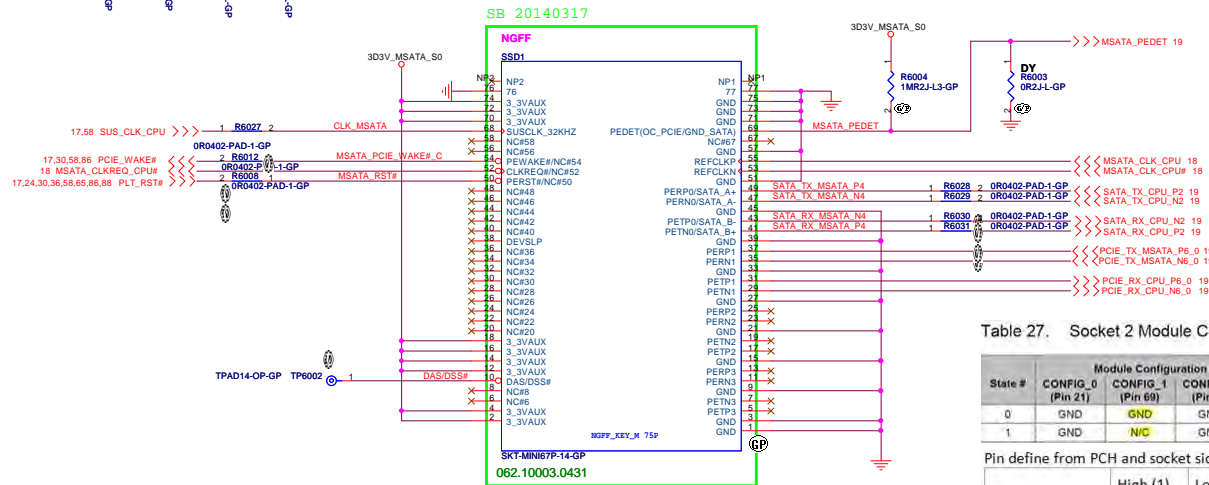
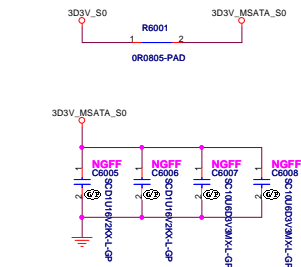
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Title: MINICARD(WLAN)

Size: Custom Document Number: Hades 840M ULT Rev: -1

Date: Wednesday, May 14, 2014 Sheet: 58 of 102

Mini Card Connector (NGFF m-SATA)



17.2.6 General Guidelines for mSATA (Gen 2 and Gen 3) Routing on SATA/PCIe muxed Ports

The below table summarizes the AC cap requirements on the motherboard when using the SATA/PCIe muxed ports.

Table 17-6. SATA/PCIe Gen 2 and Gen 3 Capacitor Values

Condition	PCIe Only	SATA Only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF ²	None ¹

Notes:

- For PCIe only application, please refer to the PCIe guidelines for details.
- For SATA only application, both PCH Tx and PCH Rx channels need to have 10 nF caps on the motherboard. This option supports all SATA devices. However, the PCH Rx 10 nF capacitor can be removed if DC coupled ODDs/devices are NOT used.
- For PCIe/SATA muxed application, a 100 nF AC cap is required on motherboards for PCH Tx channel and NO AC cap is required on motherboard for the PCH Rx channel. This option DOES NOT support DC coupled ODDs/Devices.

Table 27. Socket 2 Module Configuration

State #	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface ¹	Port Configuration ²
0	GND	GND	GND	GND	SSD - SATA	N/A
1	GND	N/C	GND	GND	SSD - PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

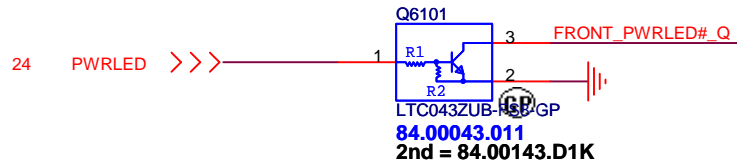
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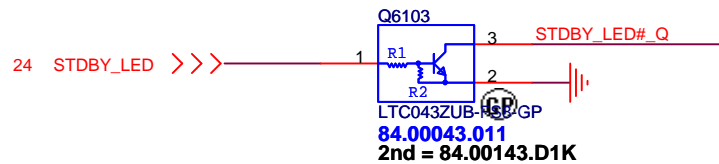
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Size	Document Number
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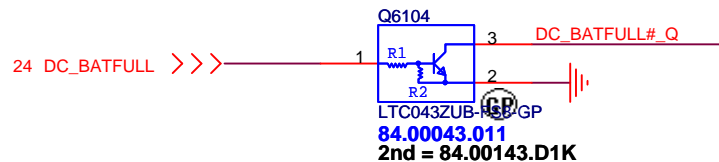
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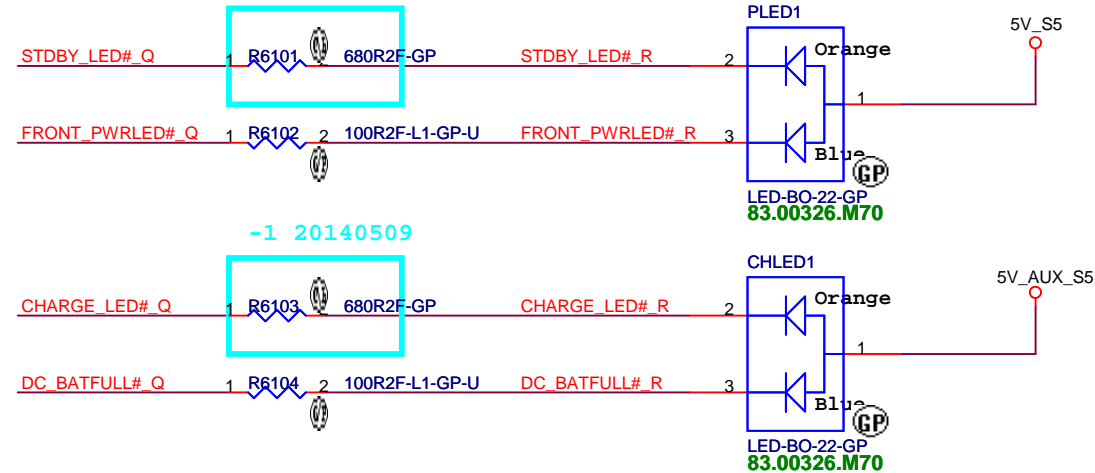
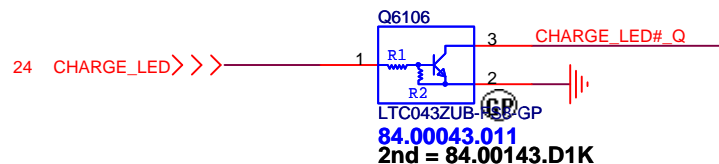
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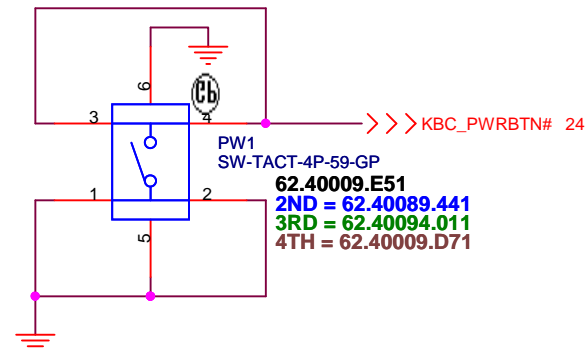
Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)



Power Button



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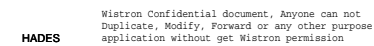
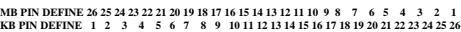
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I2C Addr. = 0X2C (Synaptics)

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Key Board/Touch Pad

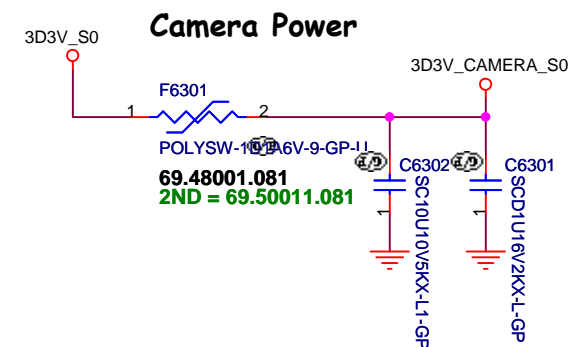
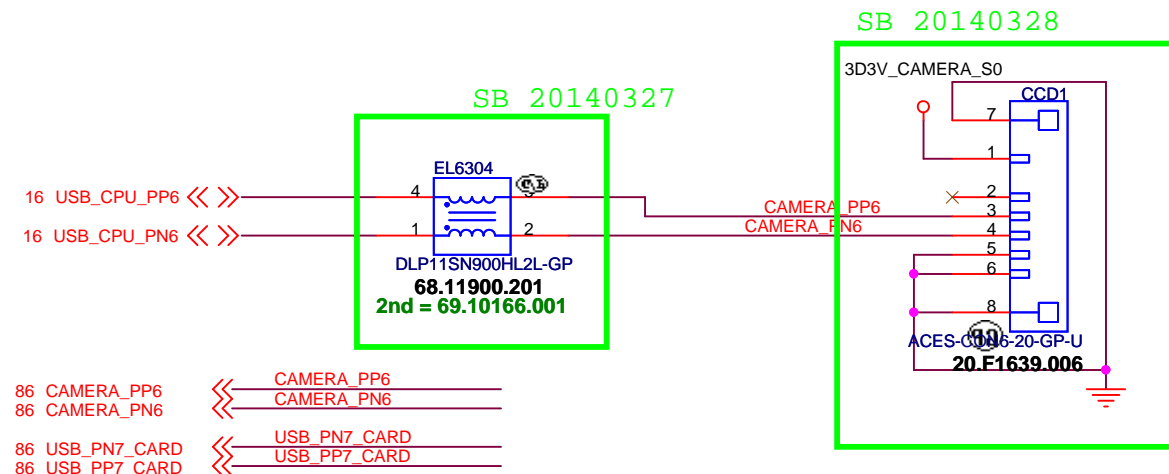
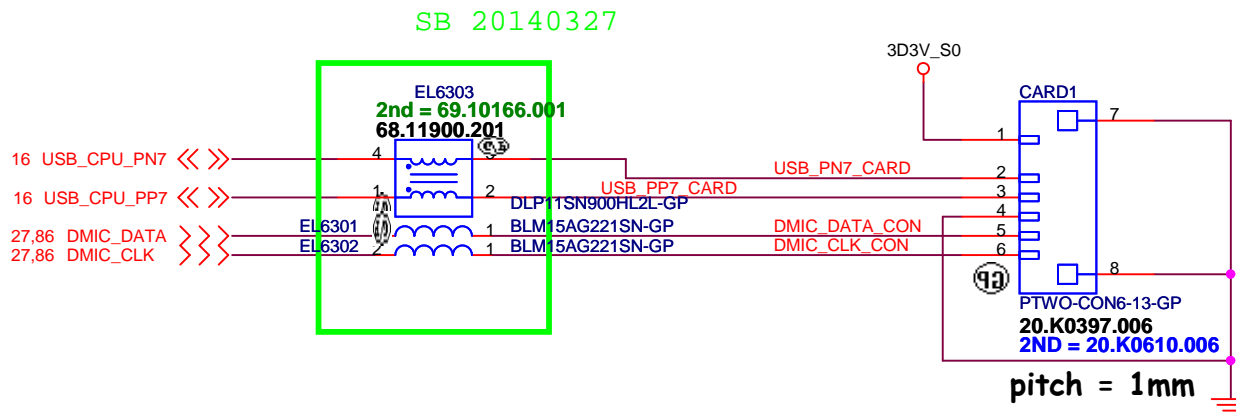
Key Board/Touch Pad

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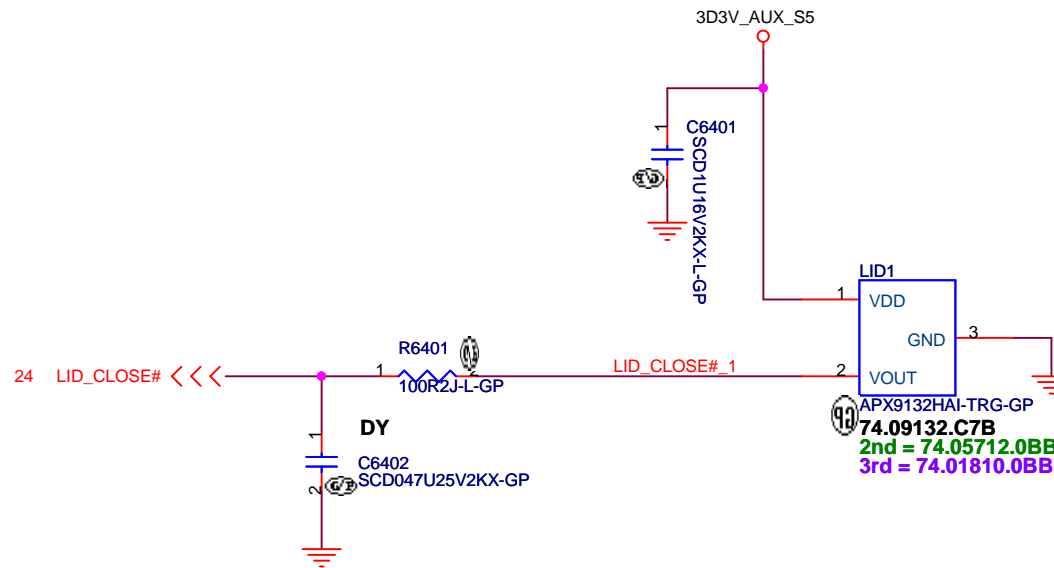


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Document Number

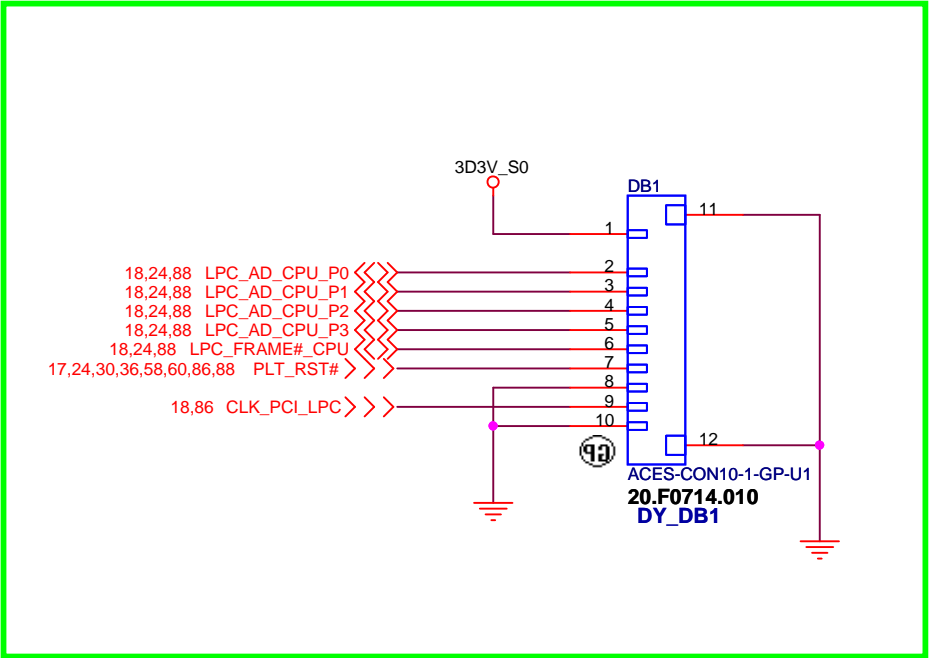
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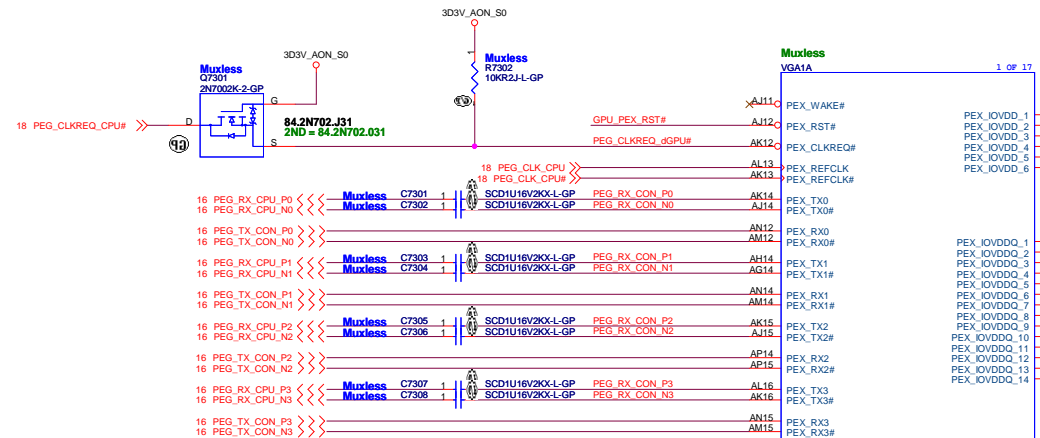
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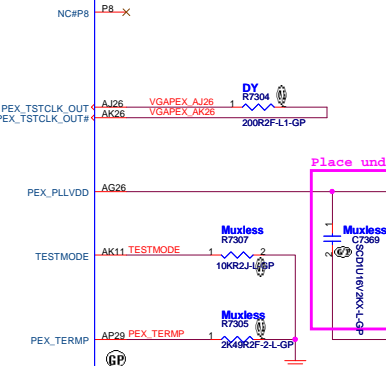
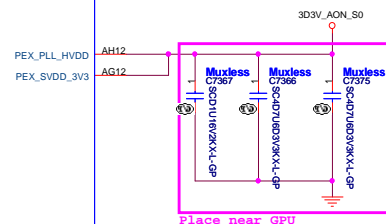
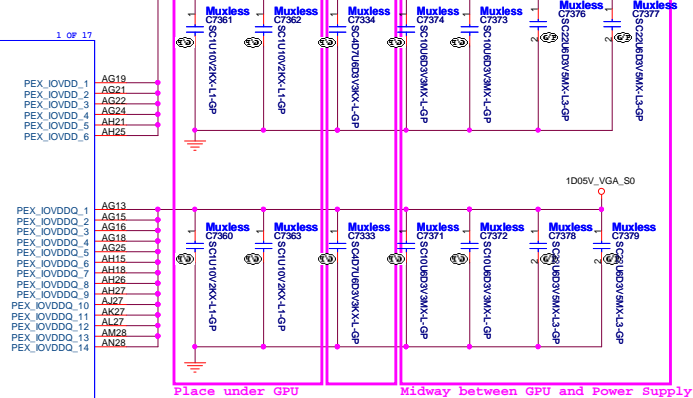
3.4.2 PCI Express Power Decoupling and Filtering

Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0 μ F	X6S 0402	1	Under GPU
	4.7 μ F	X6S 0603	1	Near GPU
	10 μ F	X5R 0805	1	Midway between GPU and Power Supply
	22 μ F	X5R 0805	1	Midway between GPU and Power Supply
GB4B-128 GB3-256	1.0 μ F	X6S 0402	4	Under GPU
	4.7 μ F	X6S 0603	2	Near GPU
	10 μ F	X5R 0805	4	Midway between GPU and Power Supply
	22 μ F	X5R 0805	4	Midway between GPU and Power Supply

Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

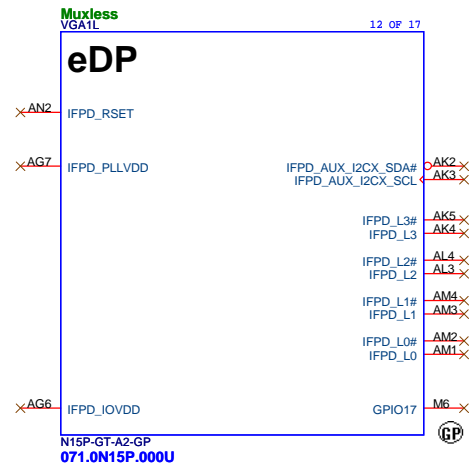
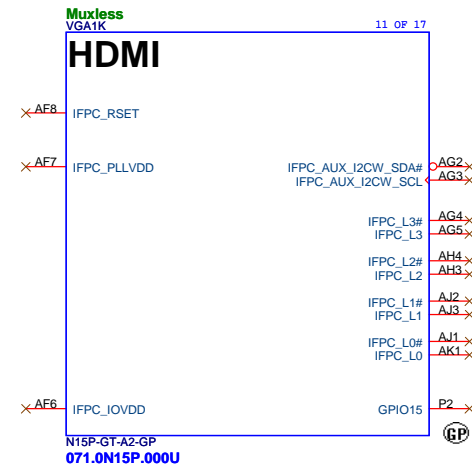
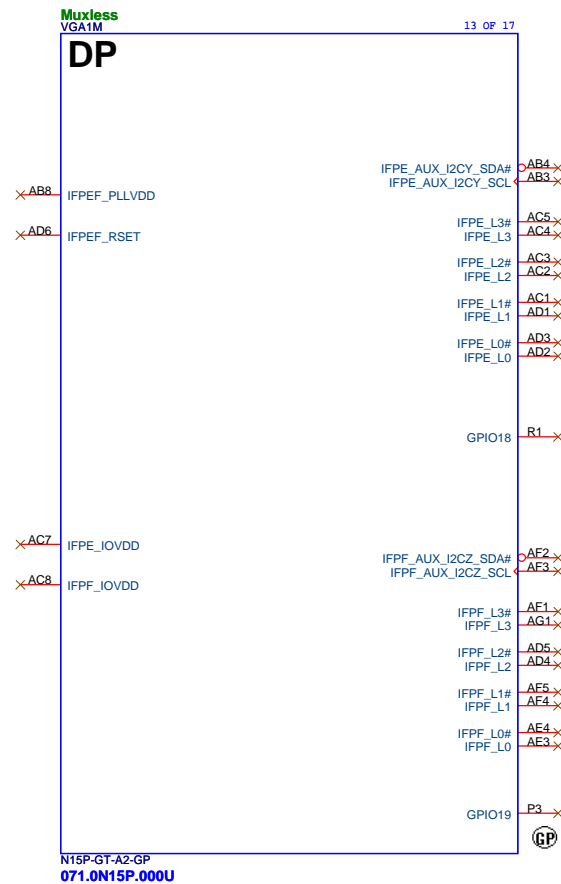
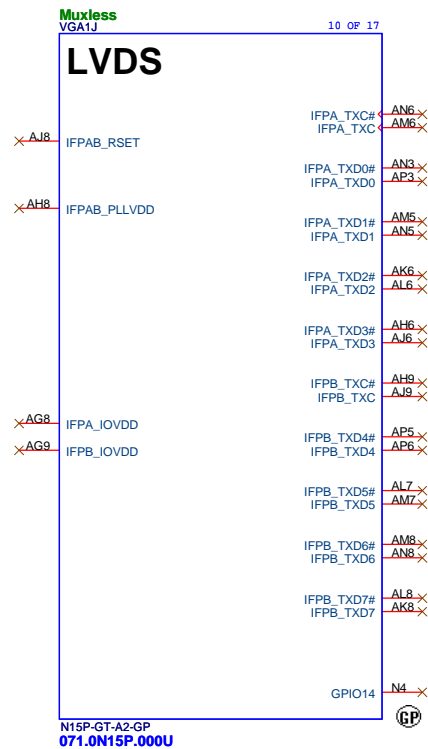
Capacitor Type	Footprint	Population	Location
0.1 μ F	X5R 0402	1	Near GPU
4.7 μ F	X5R 0603	2	Near GPU



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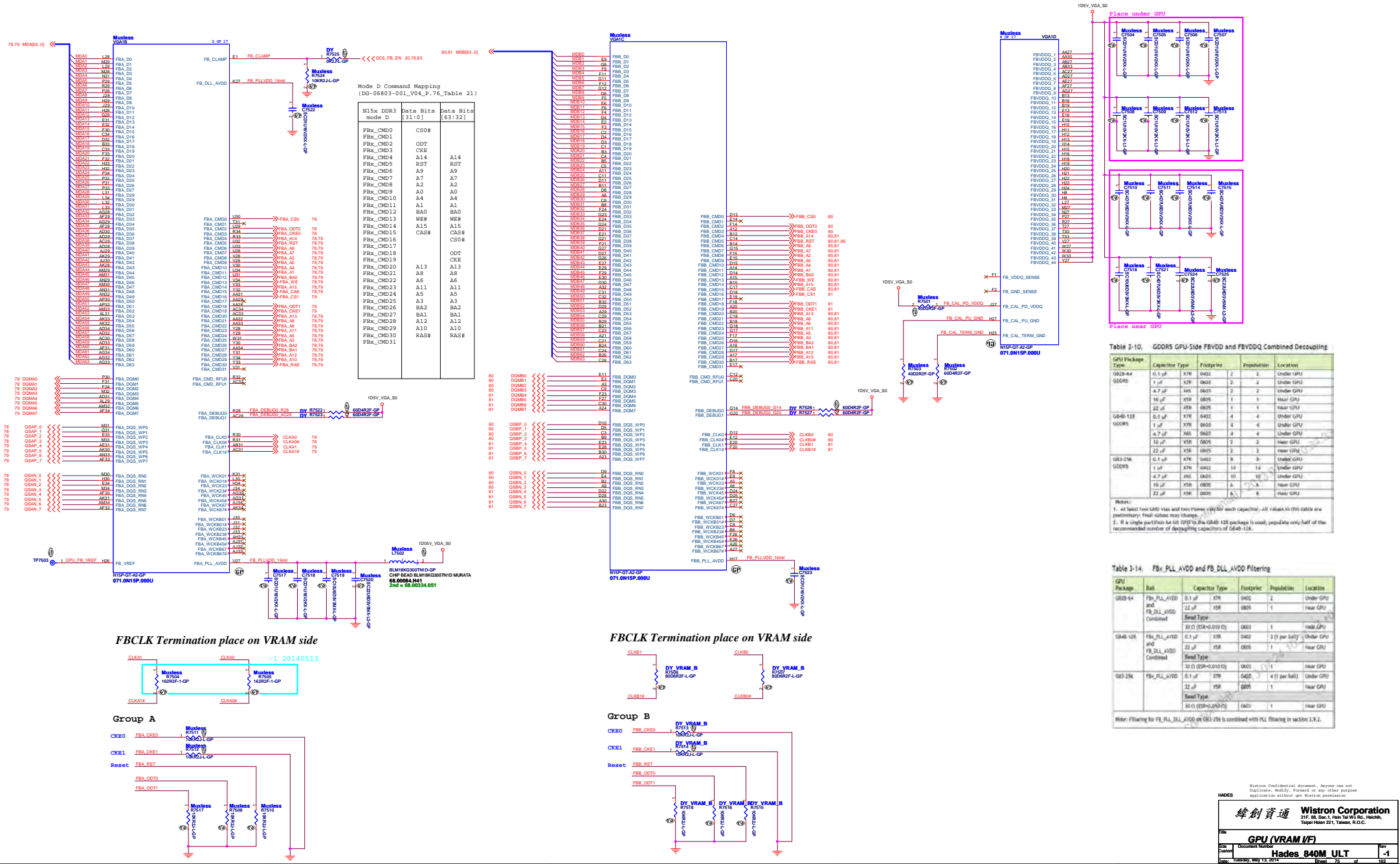


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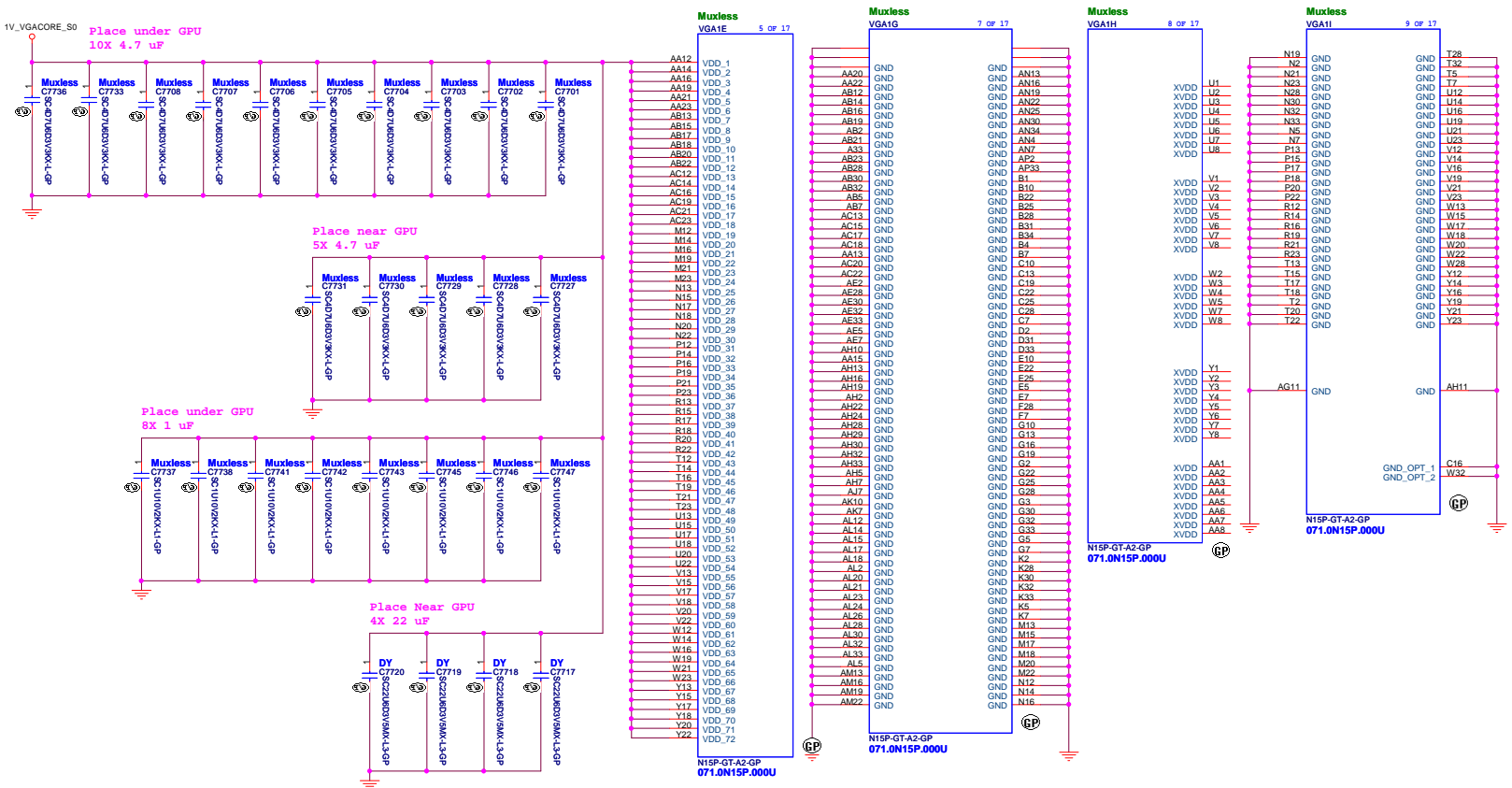


Table 3-b. HVDD Decoupling Footprint and Population

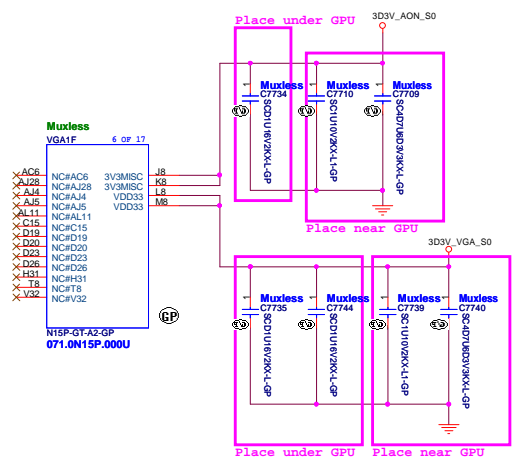
GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GB2B-64	4.7 μ F	X85 0603	10	Under GPU	
	1 μ F	X85 0402	4	Under GPU	
	4.7 μ F	X58 0805	1	Hear GPU	
	22 μ F	X58 0805	1	Hear GPU	
	4.7 μ F	X58 0805	5	Hear GPU	
GB4B-128	330 μ F	P05 7343	1	Hear GPU	ESR \leq 6 m Ω
	4.7 μ F	X85 0603	15	Under GPU	
	1 μ F	X85 0402	8	Under GPU	
	22 μ F	X58 0805	14	Hear GPU	See Note 2
GB3-256	330 μ F	P05 7343	2	Hear GPU	ESR \leq 6 m Ω
	0.1 μ F	X78 0402	20	Under GPU	
	4.7 μ F	X85 0603	40	Under GPU	
	10 μ F	X58 0805	4	Hear GPU	
	22 μ F	X58 0805	11	Hear GPU	
	470 μ F	X58 1206	4	Hear GPU	
	330 μ F	P05 7343	4	Hear GPU	ESR \leq 6 m Ω

Notes:
 1. Generally the decoupling capacitor footprint requirement will remain the same but the population may get updated or may differ per GPU SKU. Always refer to the latest PDM for any HVDD decoupling requirement update for specific GPU SKU.
 2. Continue / no layout two (2) footprints into each of the PDS-CAP footprint. So a total of four (4) footprints should be placed inside the two PDS-CAP footprints, allocating fourteen (14) footprints total.

Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	SV3_I/AAB1	0.1 μ F	X85 0402	2	Under GPU
GB4B-128		1 μ F	X58 0603	1	Hear GPU
GB3-256		4.7 μ F	X58 0603	1	Hear GPU
GB2B-64	SV3_AON1	0.1 μ F	X85 0402	1	Under GPU
GB4B-128		1 μ F	X58 0603	1	Hear GPU
GB3-256		4.7 μ F	X58 0603	1	Hear GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.



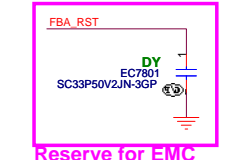
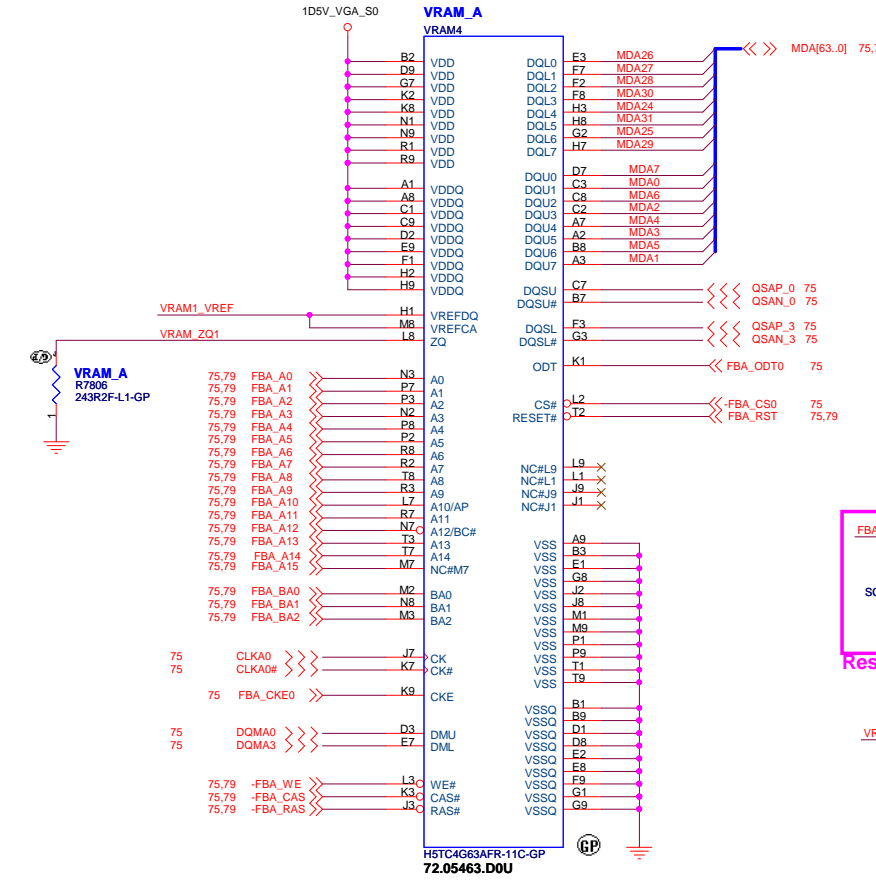
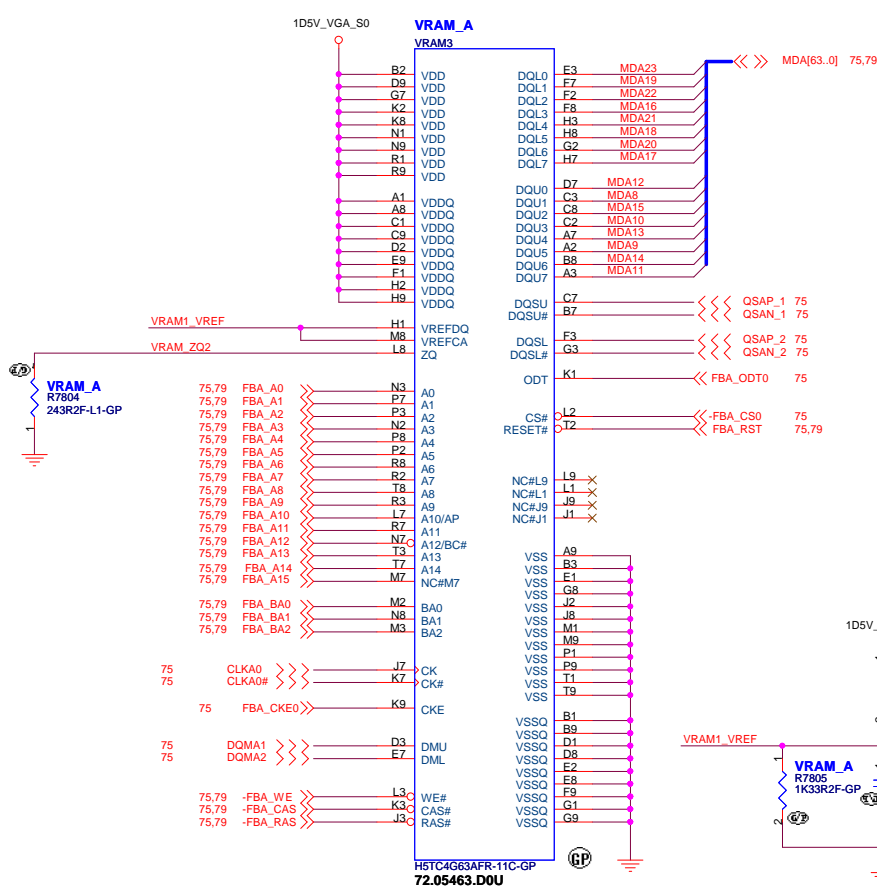
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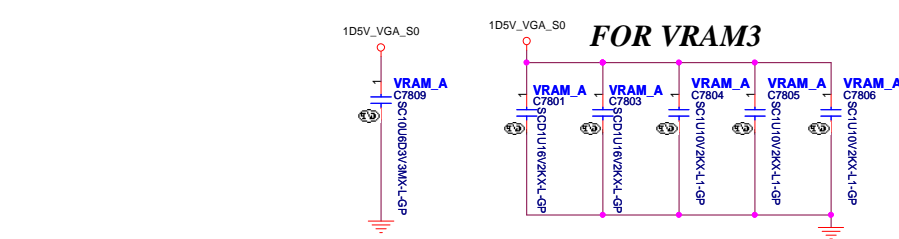
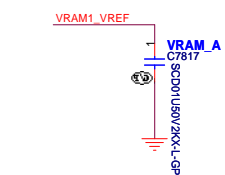
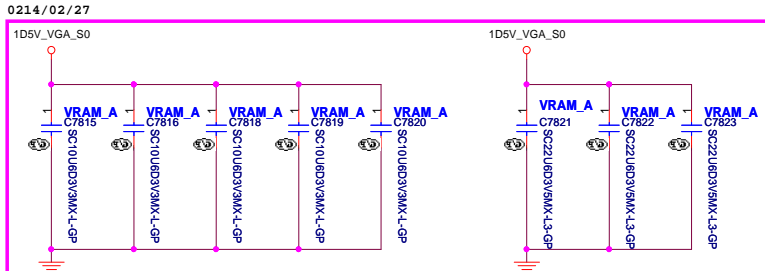
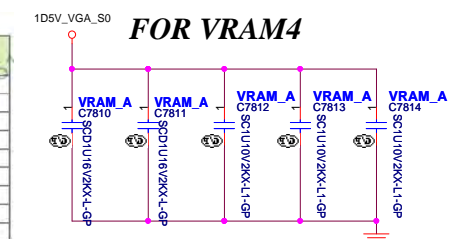


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type	Population			Location
	FBVDDQ	FBVDD		
FBVDD/Q Combined				
0.1 μF	X7R	0402	2	Under DRAM
1.0 μF	X7R	0603	4	Under DRAM
10 μF	X5R	0805	0	Close to DRAM
FBVDD/Q Separate				
0.1 μF	X7R	0402	4	Under DRAM
1.0 μF	X7R	0603	3	Under DRAM
10 μF	X5R	0805	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



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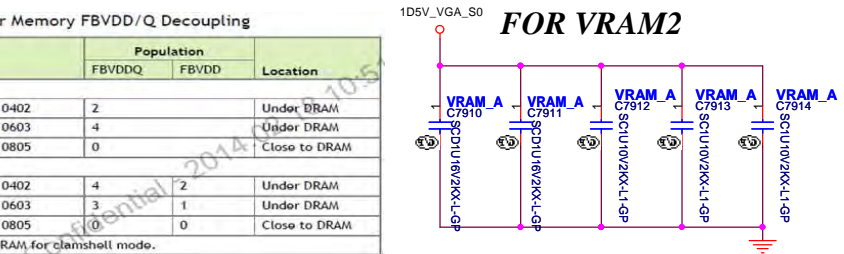
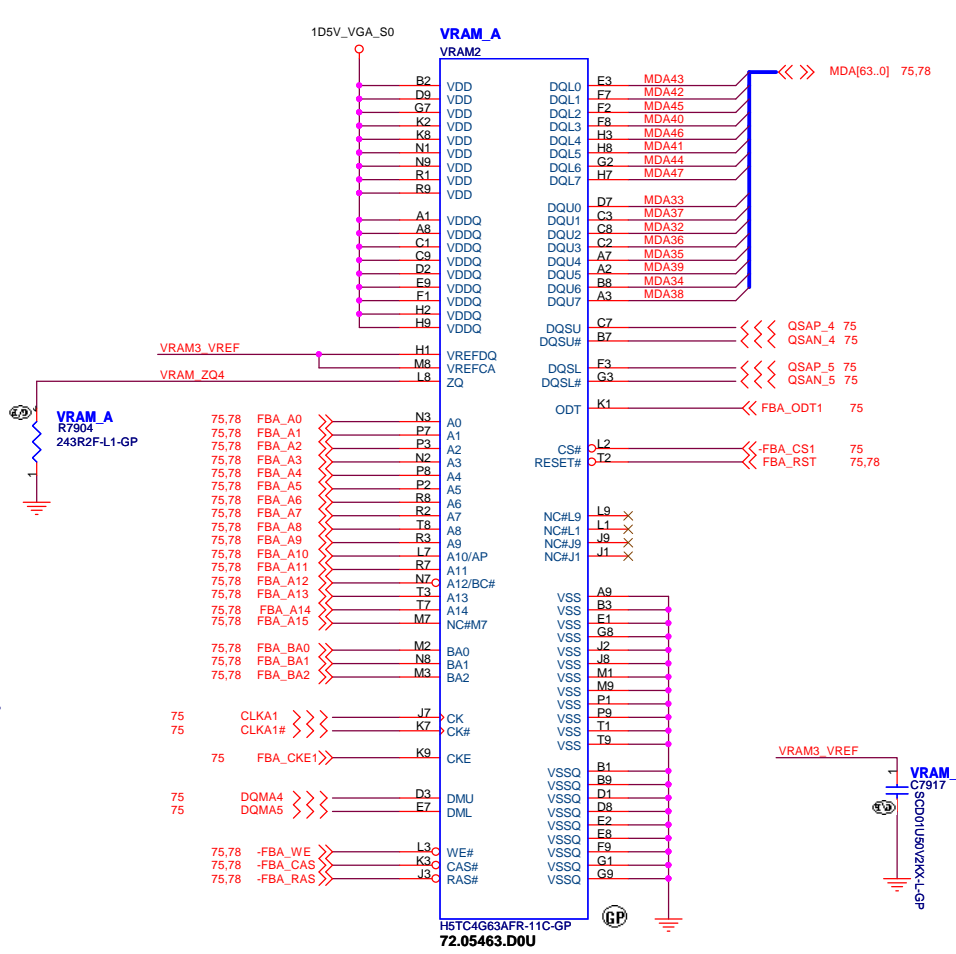
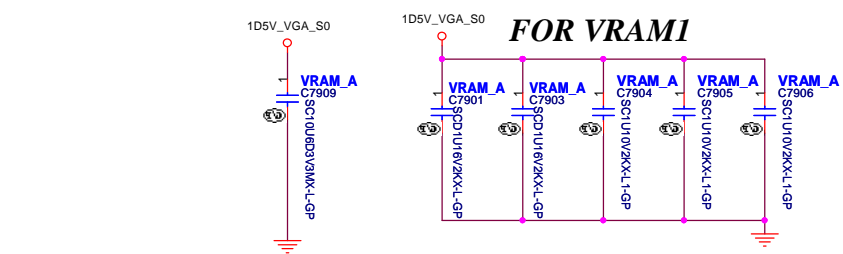
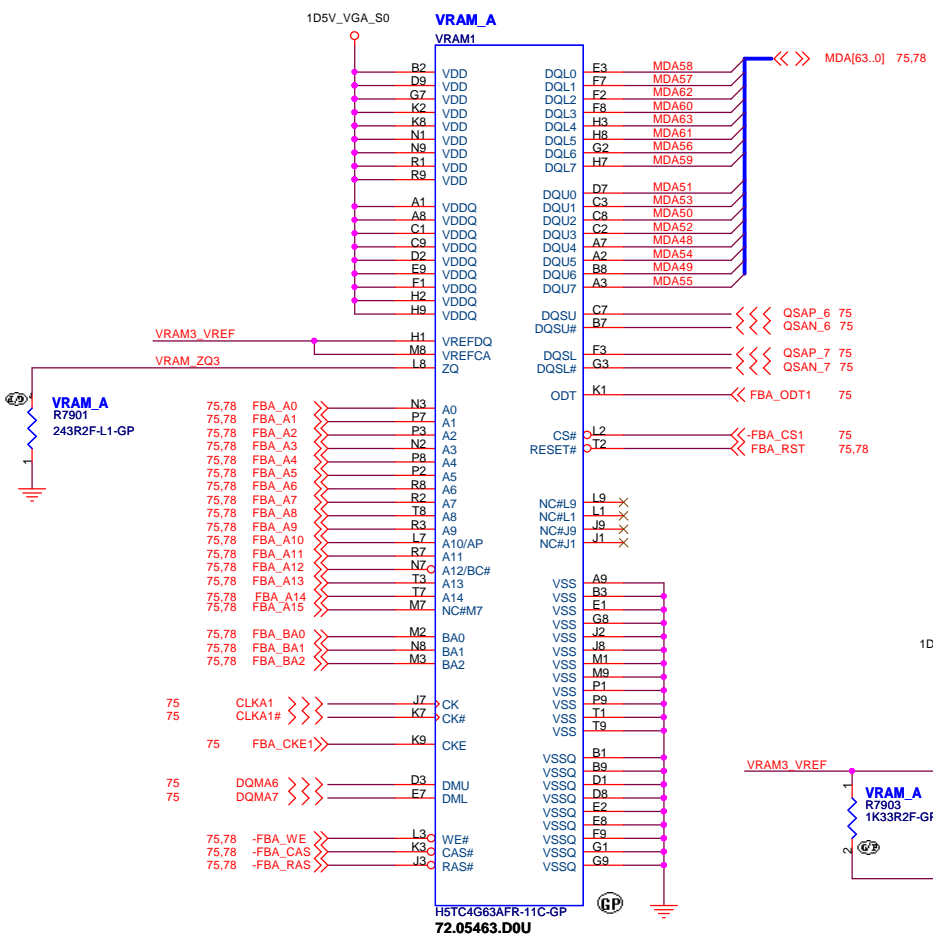


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type	Population			Location	
	FBVDDQ	FBVDD			
FBVDD/Q Combined					
0.1 μF	X7R	0402	2	Under DRAM	
1.0 μF	X7R	0603	4	Under DRAM	
10 μF	X5R	0805	0	Close to DRAM	
FBVDD/Q Separate					
0.1 μF	X7R	0402	4	2	Under DRAM
1.0 μF	X7R	0603	3	1	Under DRAM
10 μF	X5R	0805	0	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.

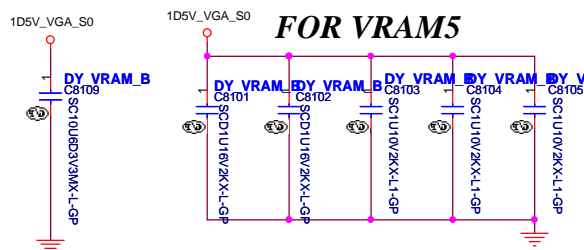
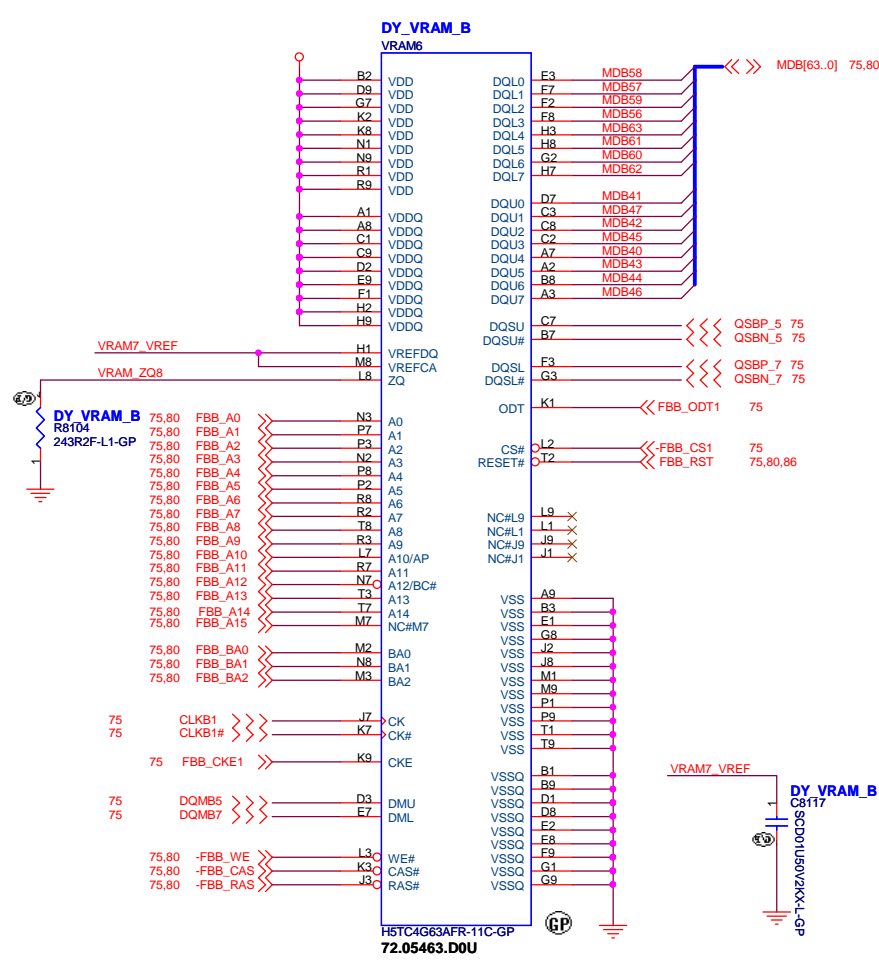
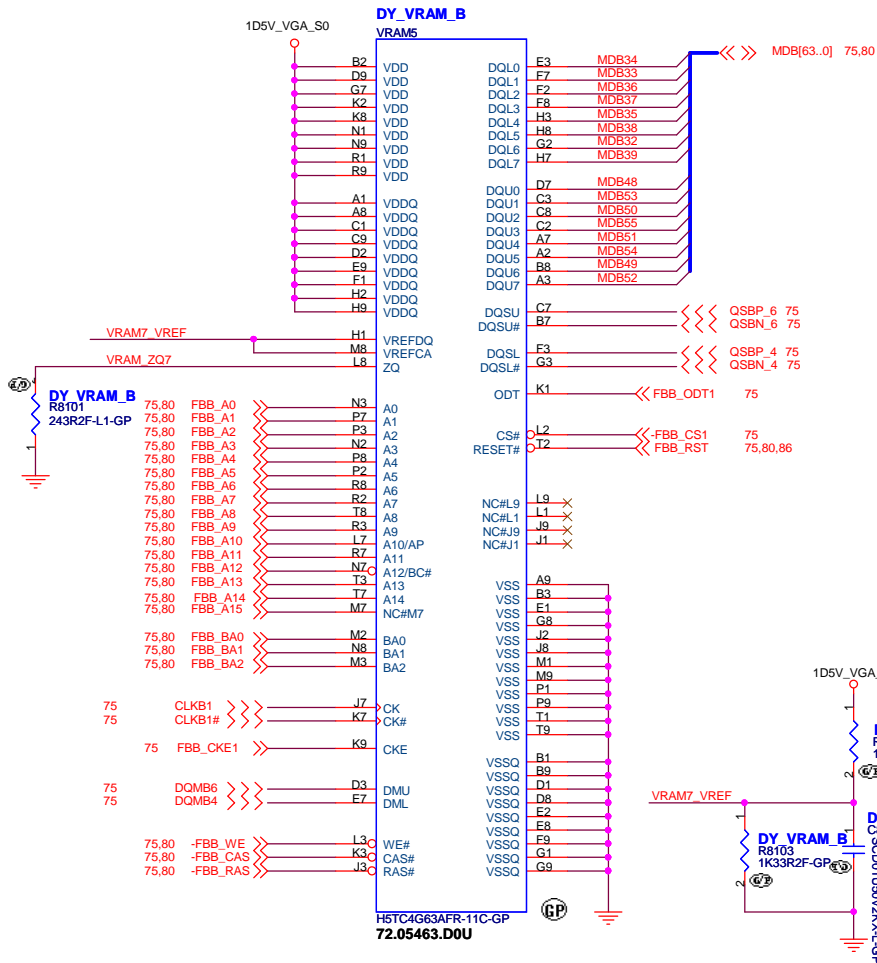
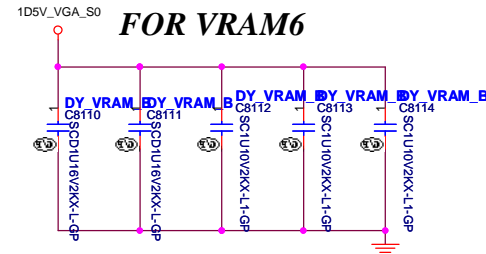


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type	Population			Location
	FBVDDQ	FBVDD		
0.1 μF	X7R	0402	2	Under DRAM
1.0 μF	X7R	0603	4	Under DRAM
10 μF	X5R	0805	0	Close to DRAM
FBVDD/Q Separate				
0.1 μF	X7R	0402	4	Under DRAM
1.0 μF	X7R	0603	3	Under DRAM
10 μF	X5R	0805	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



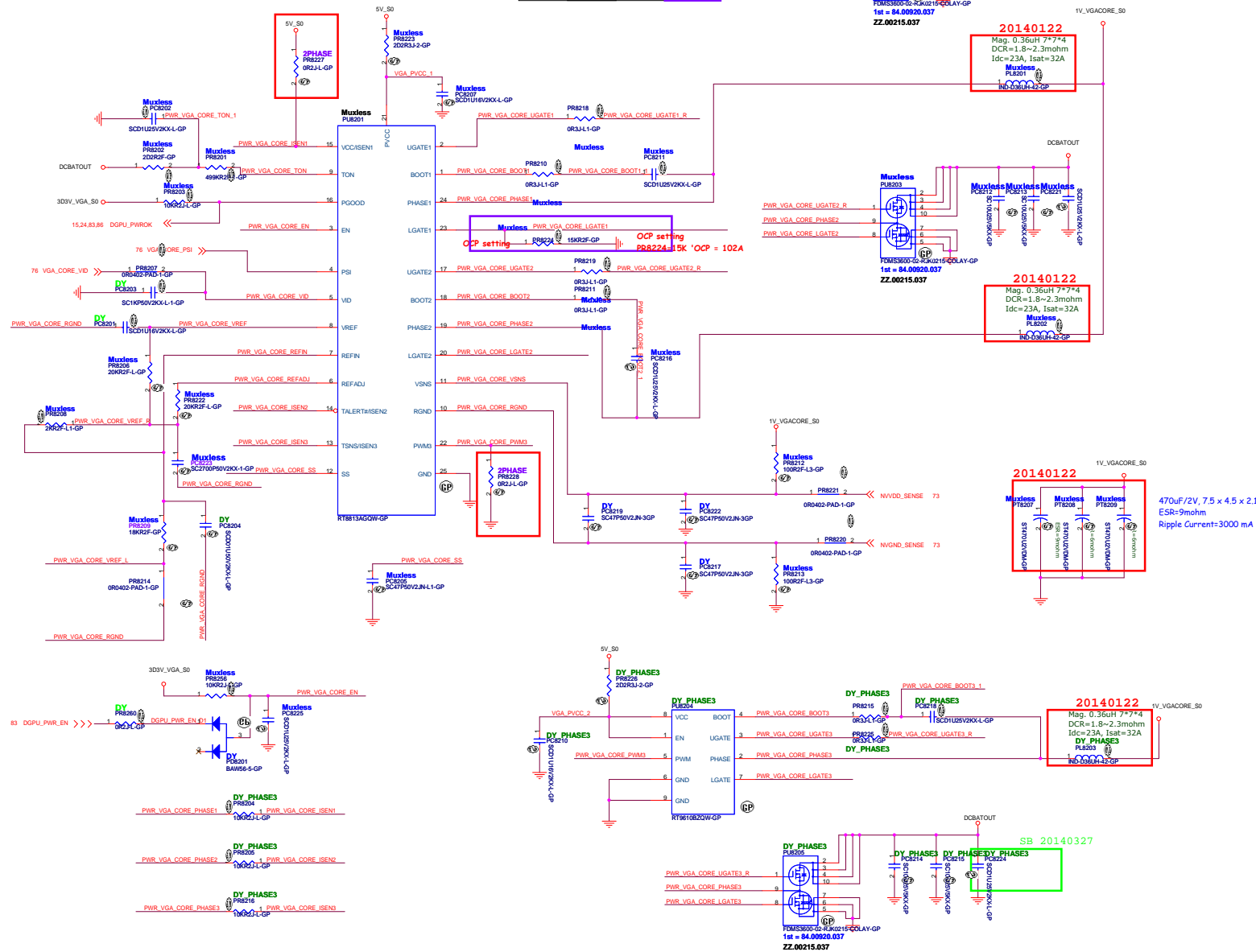
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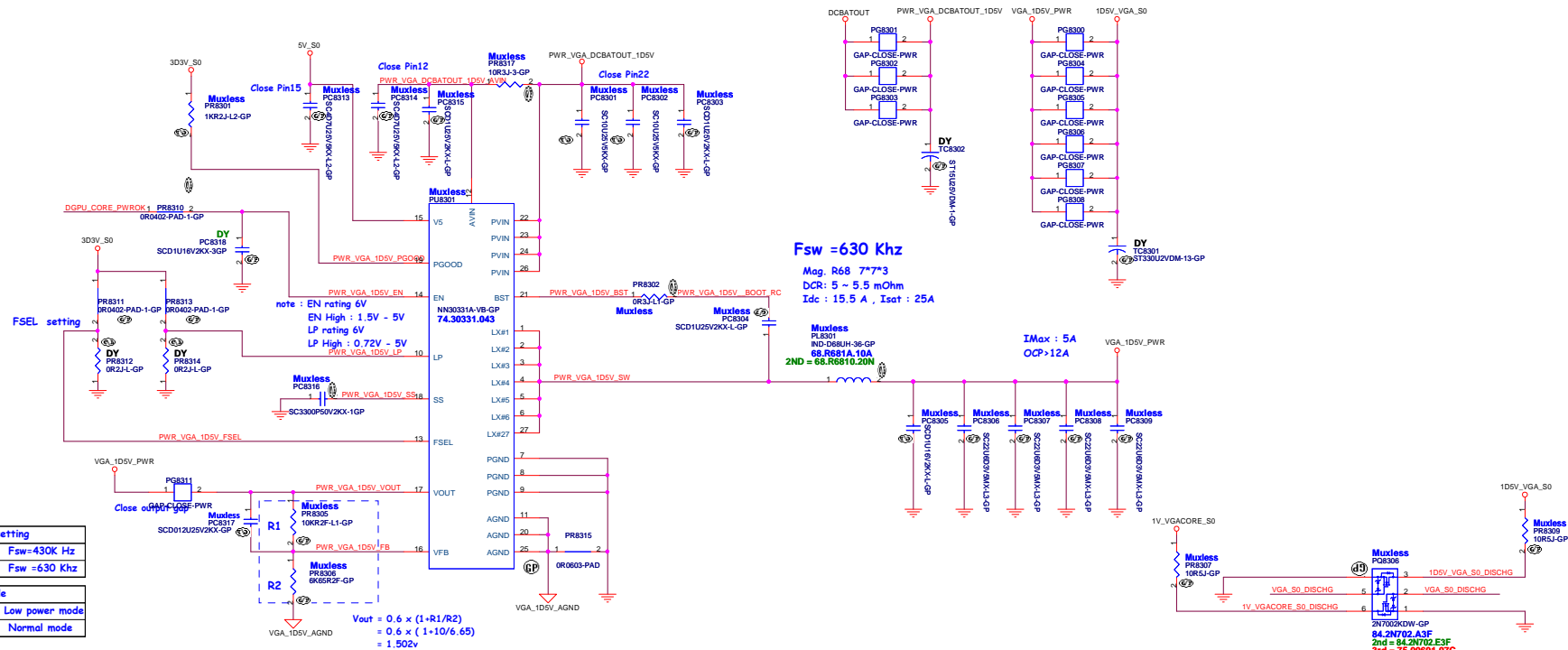
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Config : B
EDP-Continuous : 49A
EDP-Peak : 76A

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EDP-Peak	51.5 A	40.89 A	80 A
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PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
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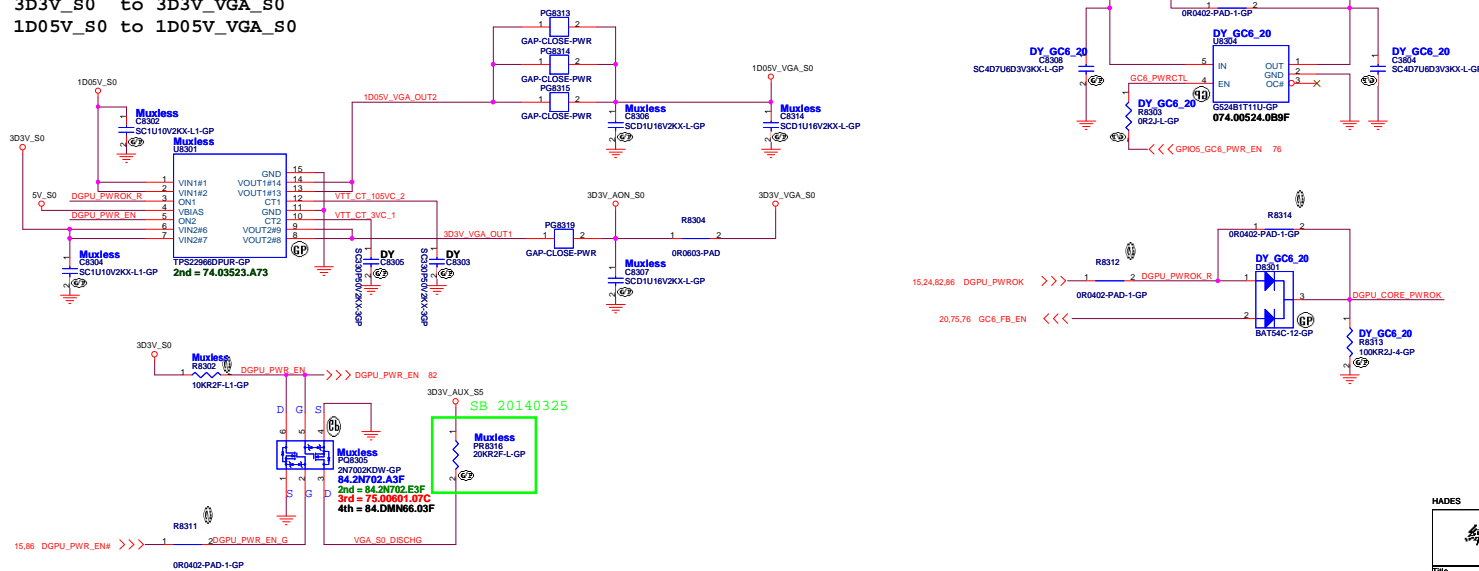


NN30331A for VGA_1D5V(For VRAM DDR3)

VGA_CORE&1D05V_VGA_S0 Discharge Circuit



3D3V_S0 to 3D3V_VGA_S0
 1D05V_S0 to 1D05V_VGA_S0

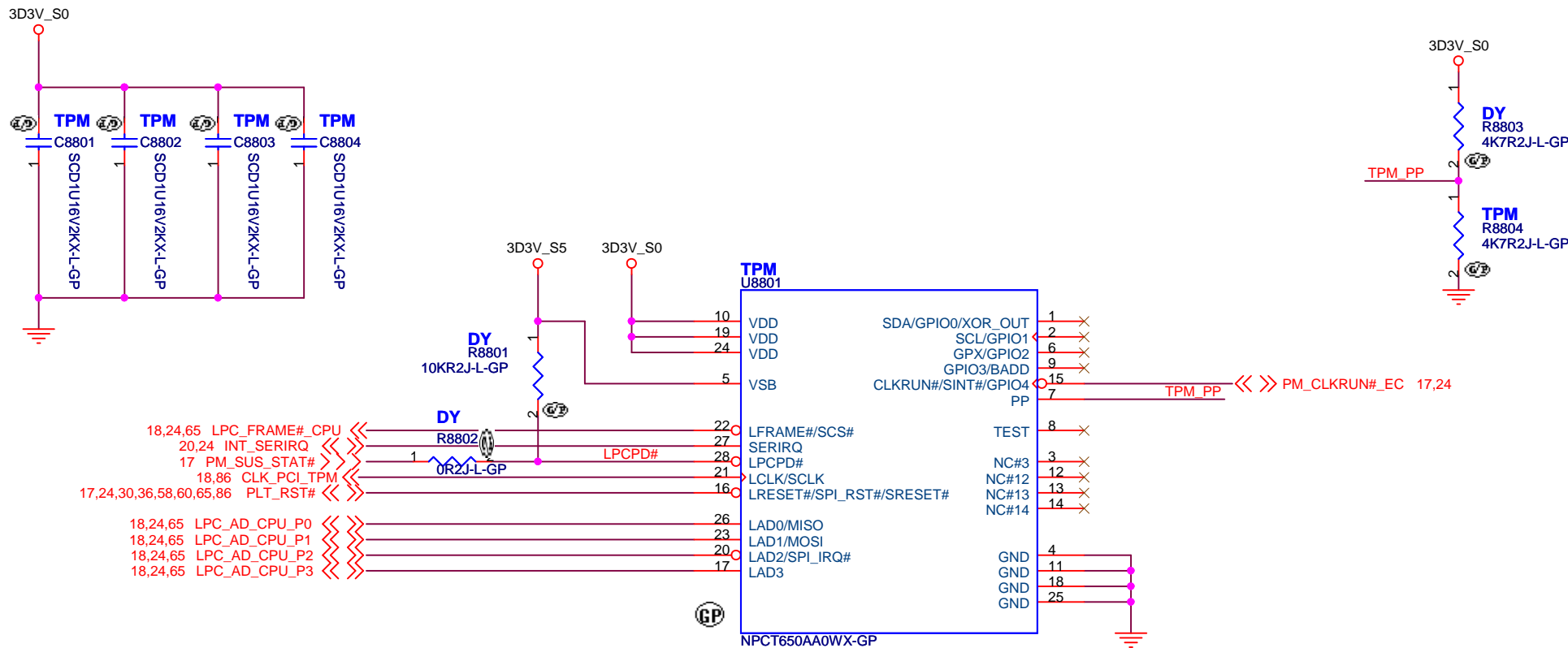


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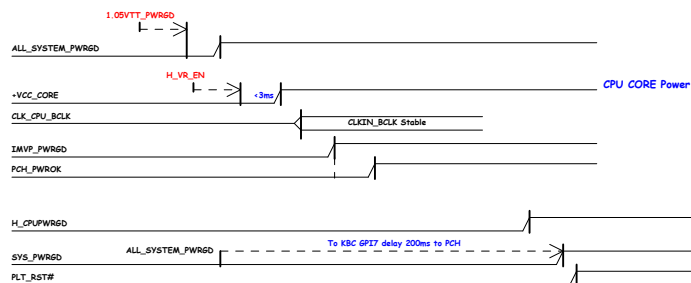
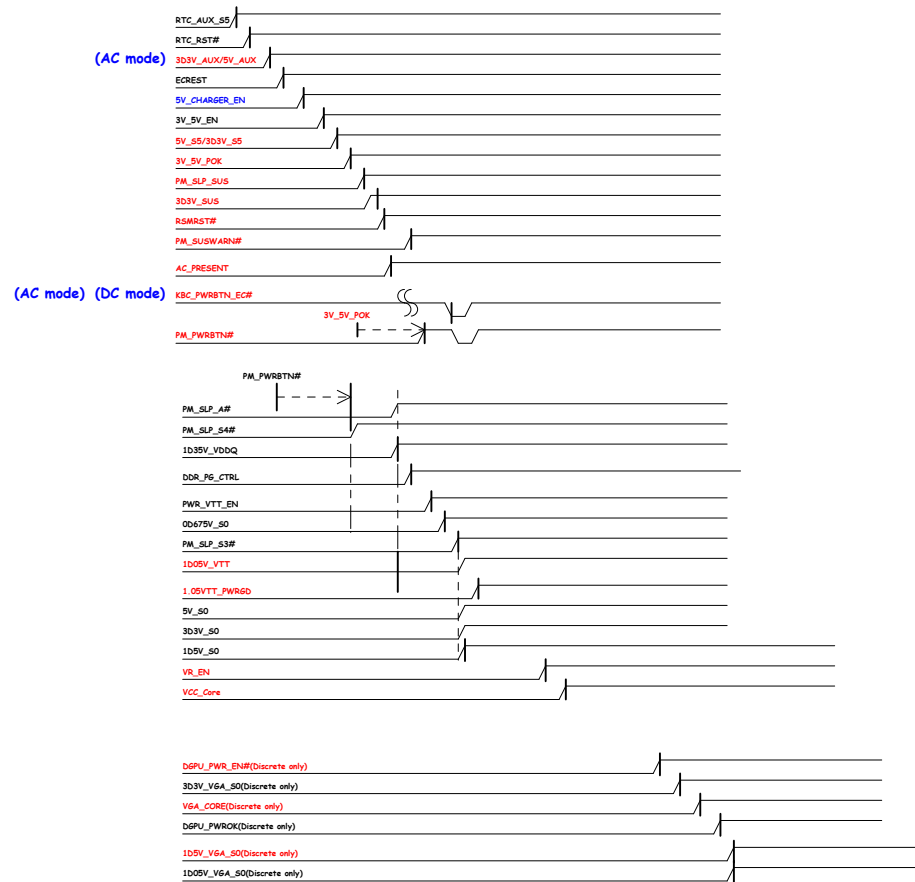
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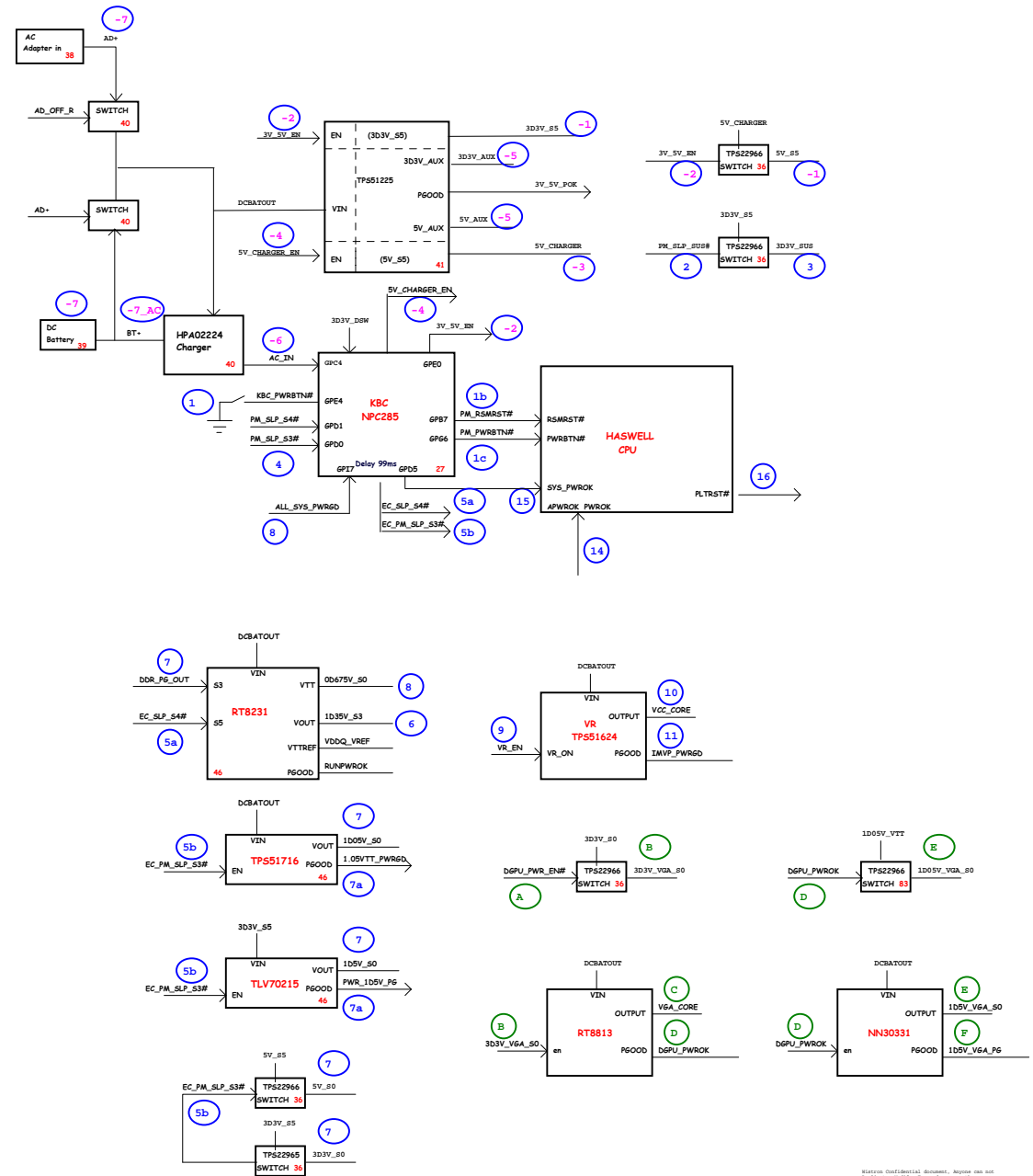
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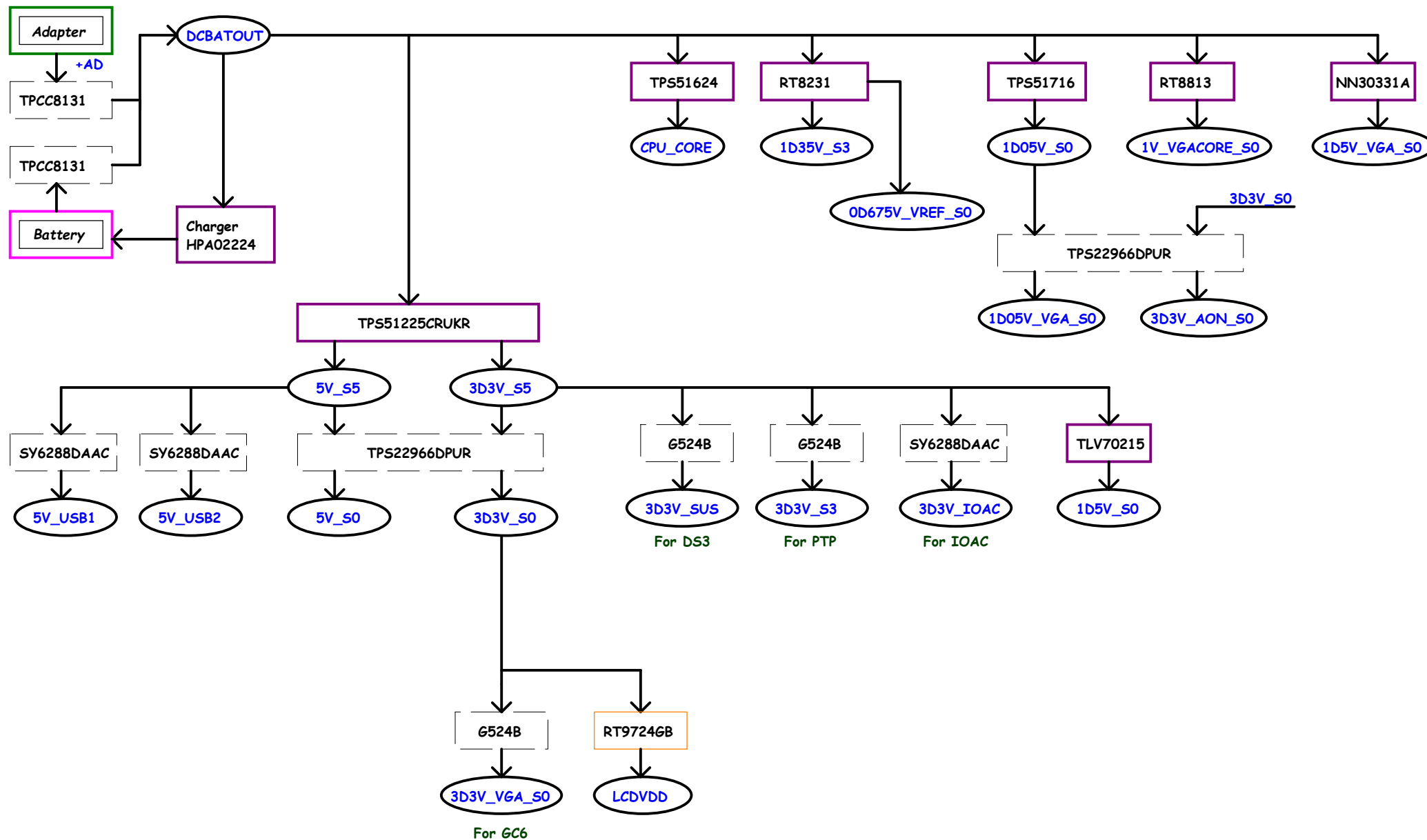
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Intel-Power Up Sequence



HASWELL POWER UP SEQUENCE DIAGRAM





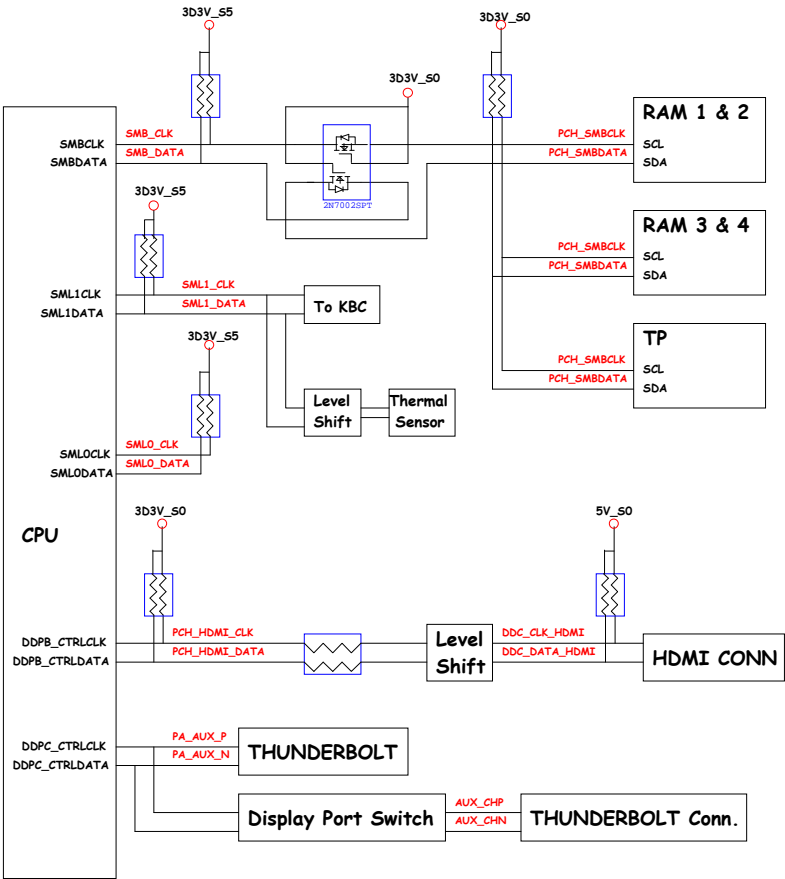
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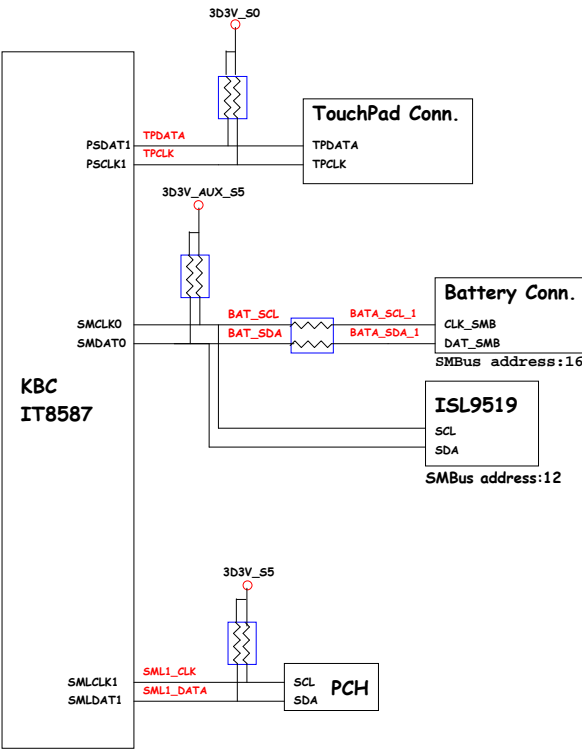
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PCH SMBus Block Diagram



KBC SMBus Block Diagram



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