

Poseidon

Schematics Document

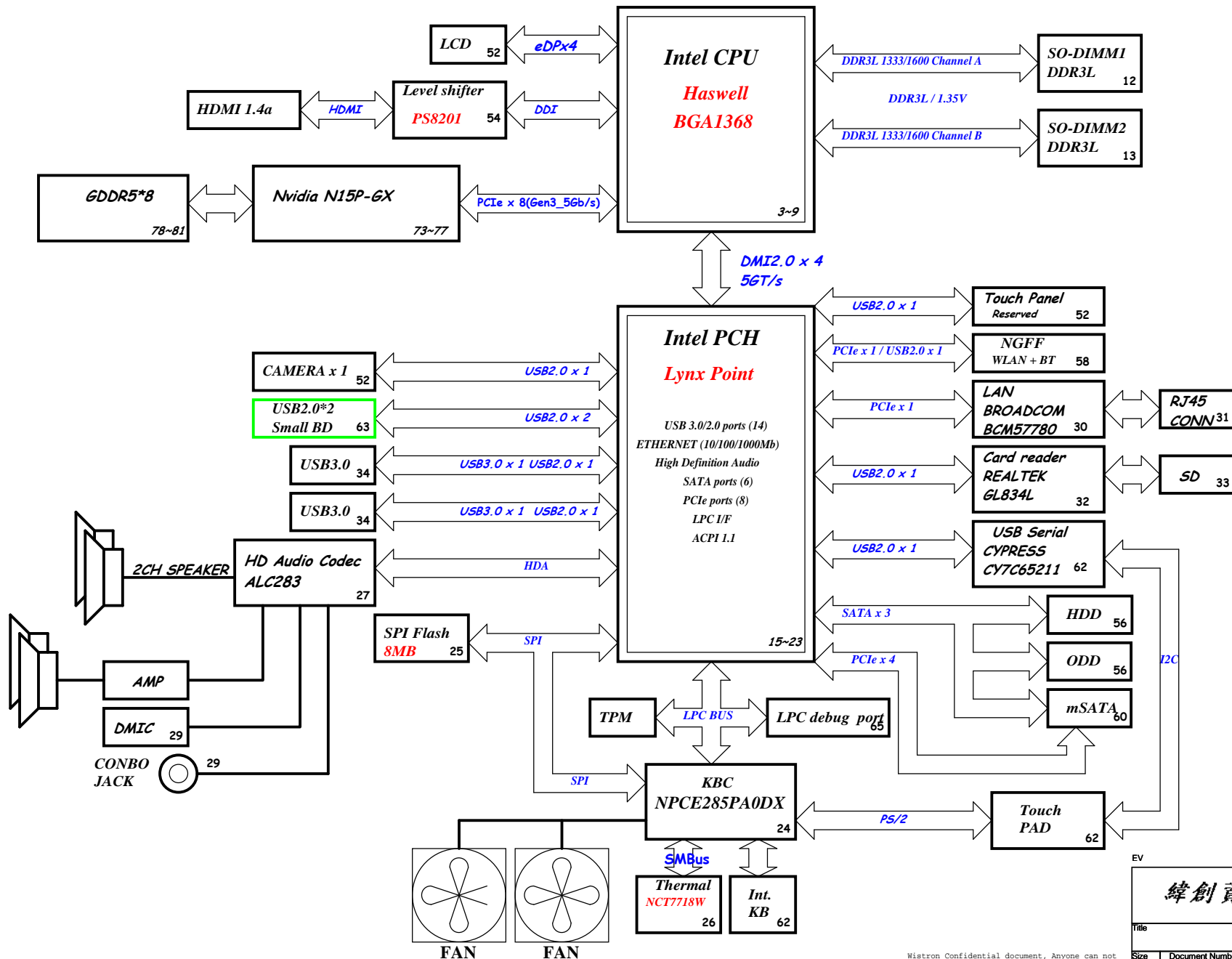
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Title			
Cover Page			
Size A3	Document Number		Rev -1
Date: Tuesday, June 17, 2014	Sheet	1	of 102

Poseidon Board Block Diagram

Project code : 4PD02G010001
PCB NO : 14203
Revision : -2



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Block Diagram

Size
Custom

Document Number

Rev
-1

Date: Tuesday, June 17, 2014

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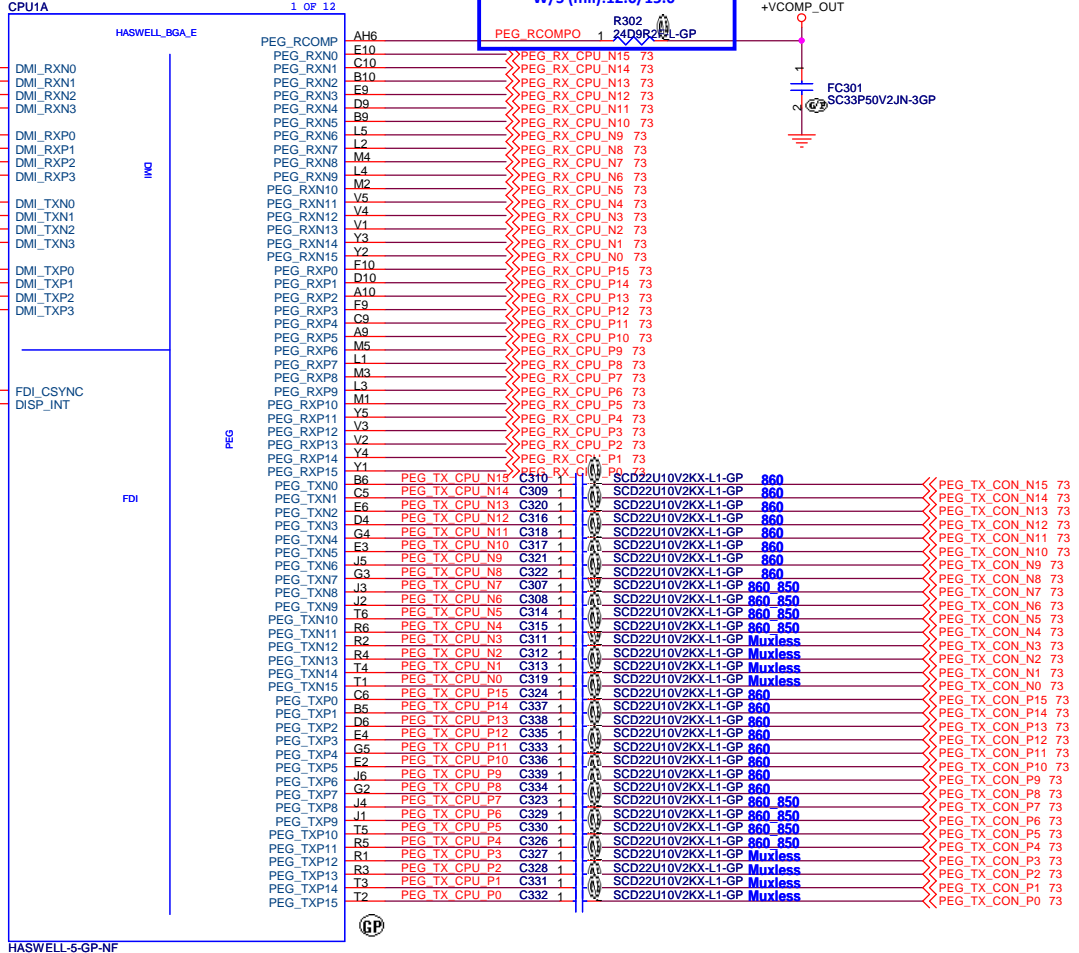
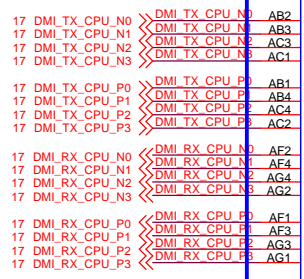
SSID = CPU

Layout Note:

Max Length : 400 Mil
W/S (mil):12.0/15.0

Max Length : 1000~8000 Mil
Max Via : 3

Layout Note:



71.HASWE.D0U

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Pro- cessor	Physical Lanes													
				0	1	2	3	4	5	6	7	8	9	10	11	12	13
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1
x16	Off	Off	Reverse	1	2	3	4	5	6	7	8	9	10	11	12	13	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2

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Title

CPU (PCIe/DMI/FDI)

Size A3

Document Number

Rev

Date

102

Sheet

3

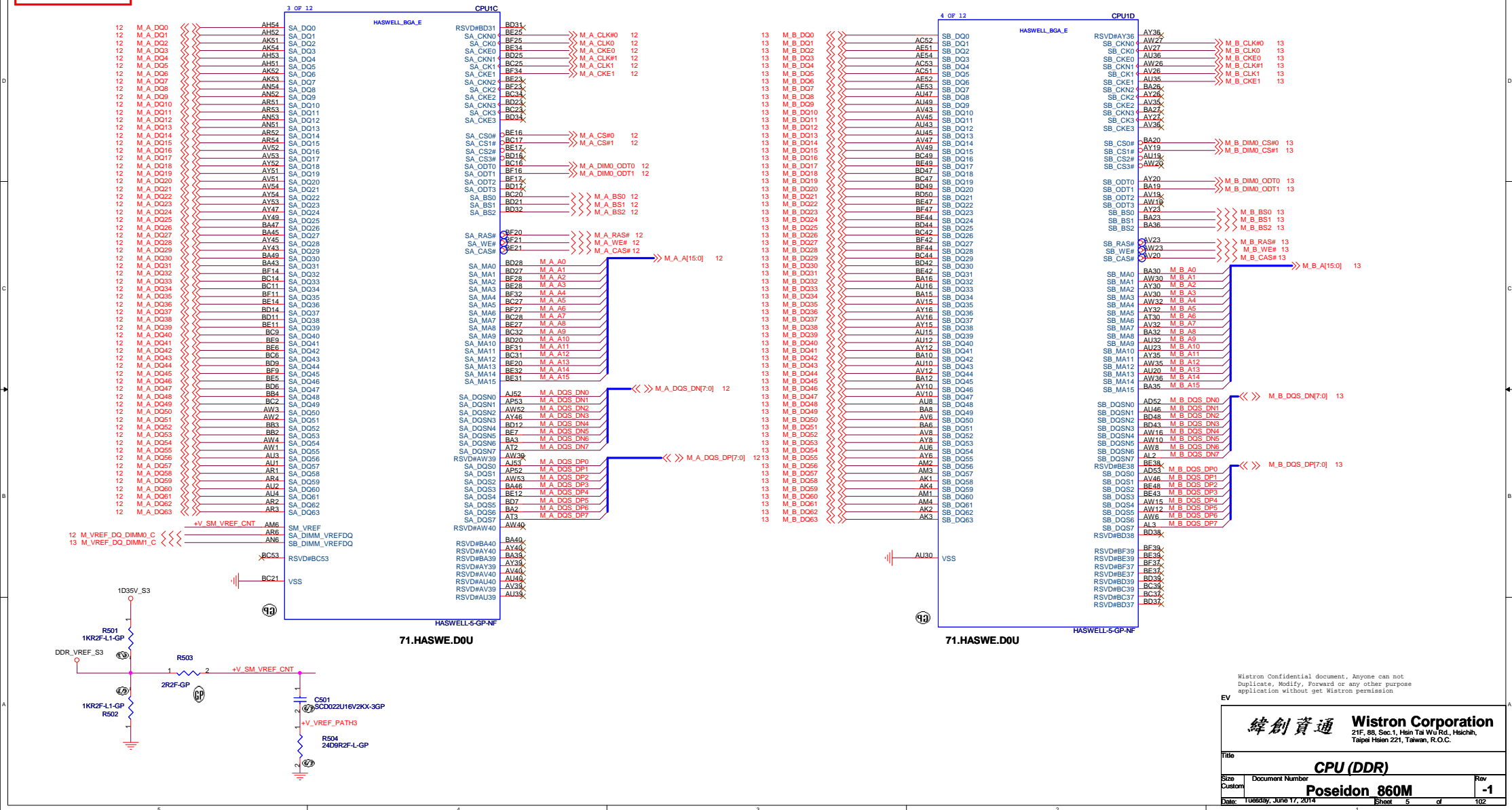
of

102

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SSID = CPU



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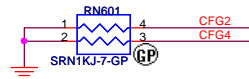
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Title			
CPU (DDR)			
Size	Document Number	Rev	
Custom	Poseidon 860M	-1	
Date:	Tuesday, June 17, 2014	Sheet	5 of 102

SSID = CPU

PEG Static Lane Reversal

CFG2 1: Normal Operation; Lane # definition matches socket pin map definition
0: Lane Reversed

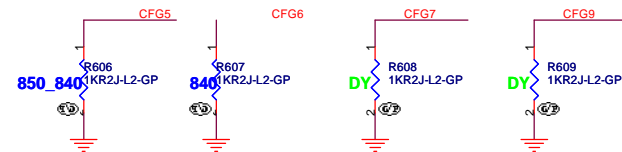


eDP Enable

CFG4 1: Disable
0: Enable

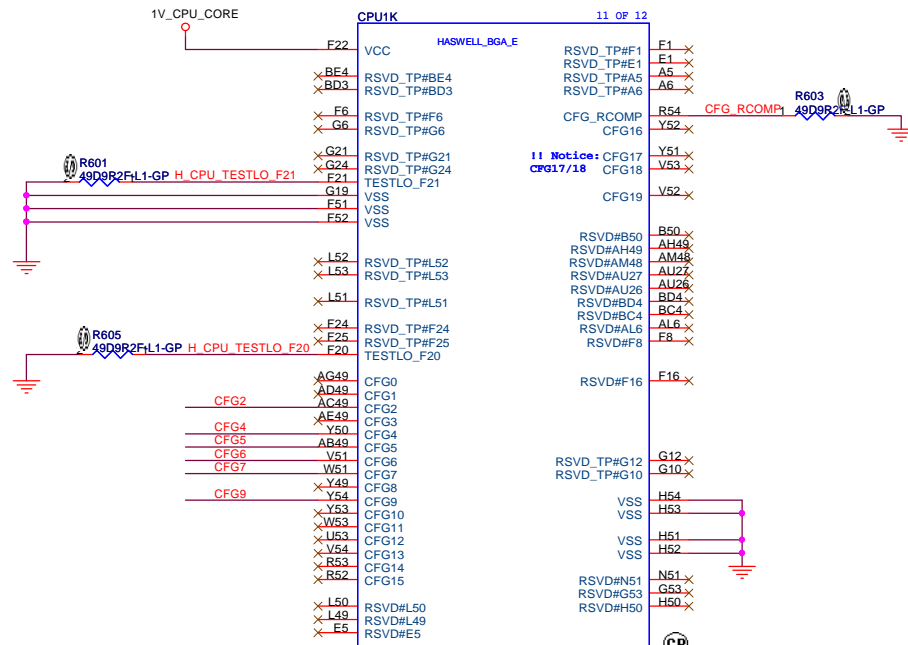
PCIe Port Bifurcation Straps

CFG[6:5] 11: x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

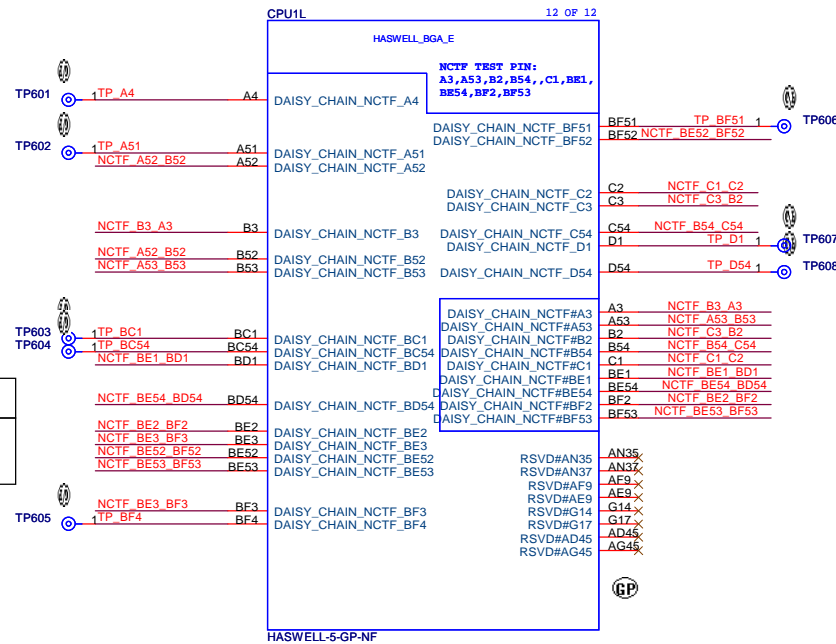


Reserved configuration lanes. A test point may be placed on the board for these lands.

CFG[19:7]



71.HASWE.D0U



HASWELL-5-GP-NF

71.HASWE.D0U

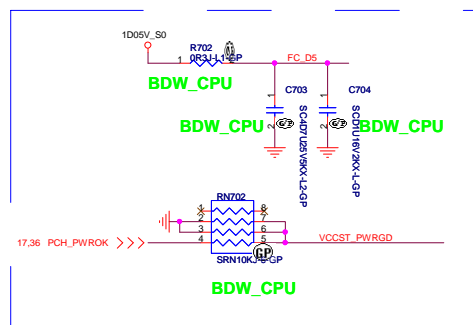
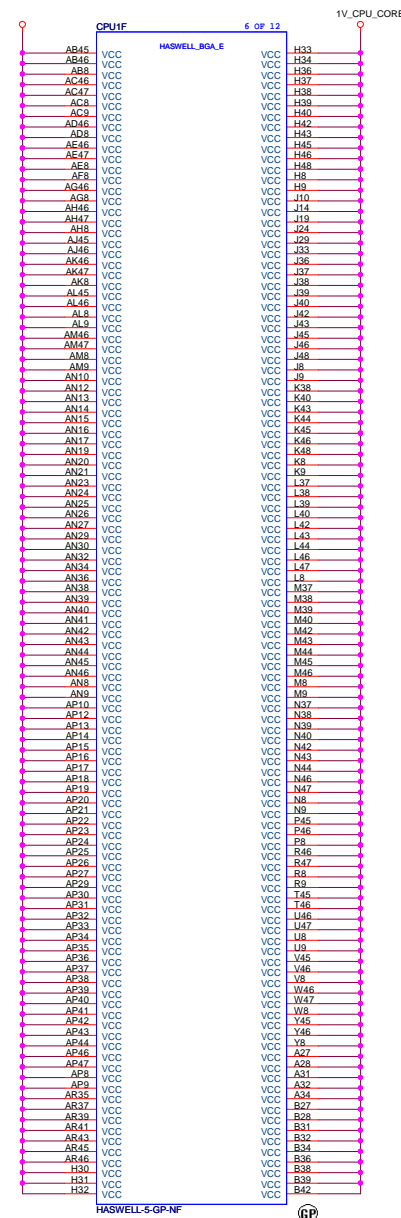
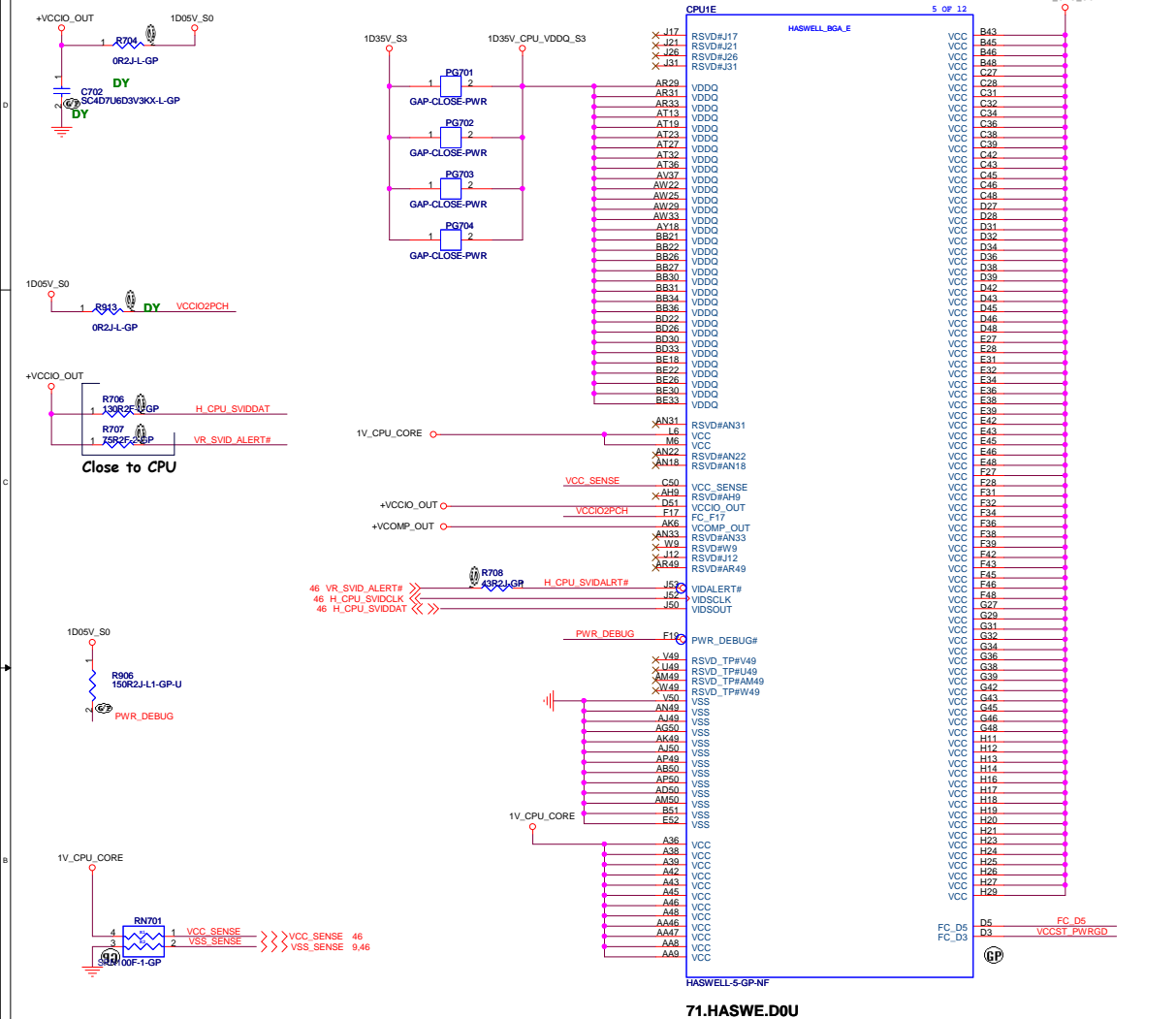
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CPU (CFG)		
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SSID = CPU



For Broadwell Processor Compatibility

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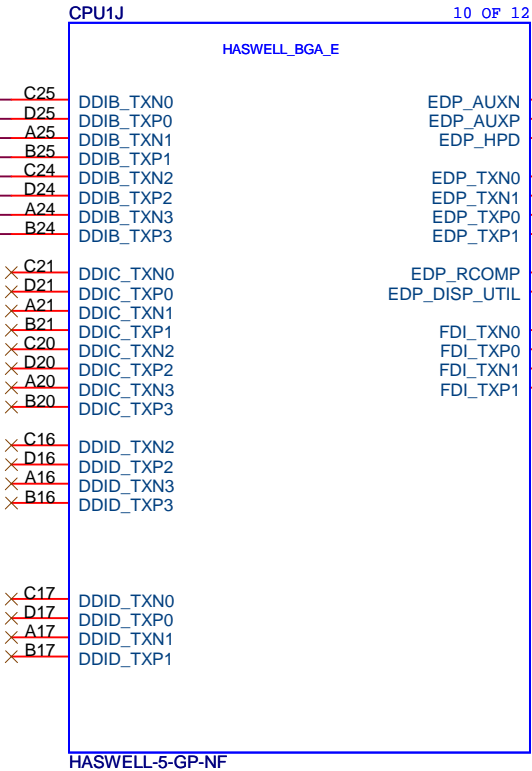
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Title			
CPU (VCC CORE)			
Size	Document Number		Rev
Custom	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet 7 of	102

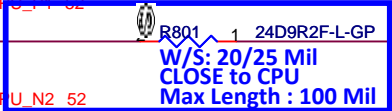
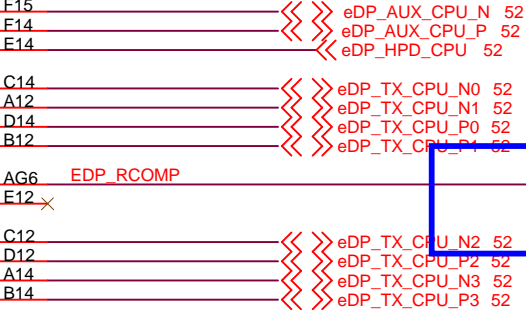
SSID = CPU

HDMI

54 HDMI_DATA_CPU_N2
54 HDMI_DATA_CPU_P2
54 HDMI_DATA_CPU_N1
54 HDMI_DATA_CPU_P1
54 HDMI_DATA_CPU_N0
54 HDMI_DATA_CPU_P0
54 HDMI_DATA_CPU_N3
54 HDMI_DATA_CPU_P3



71.HASWE.D0U

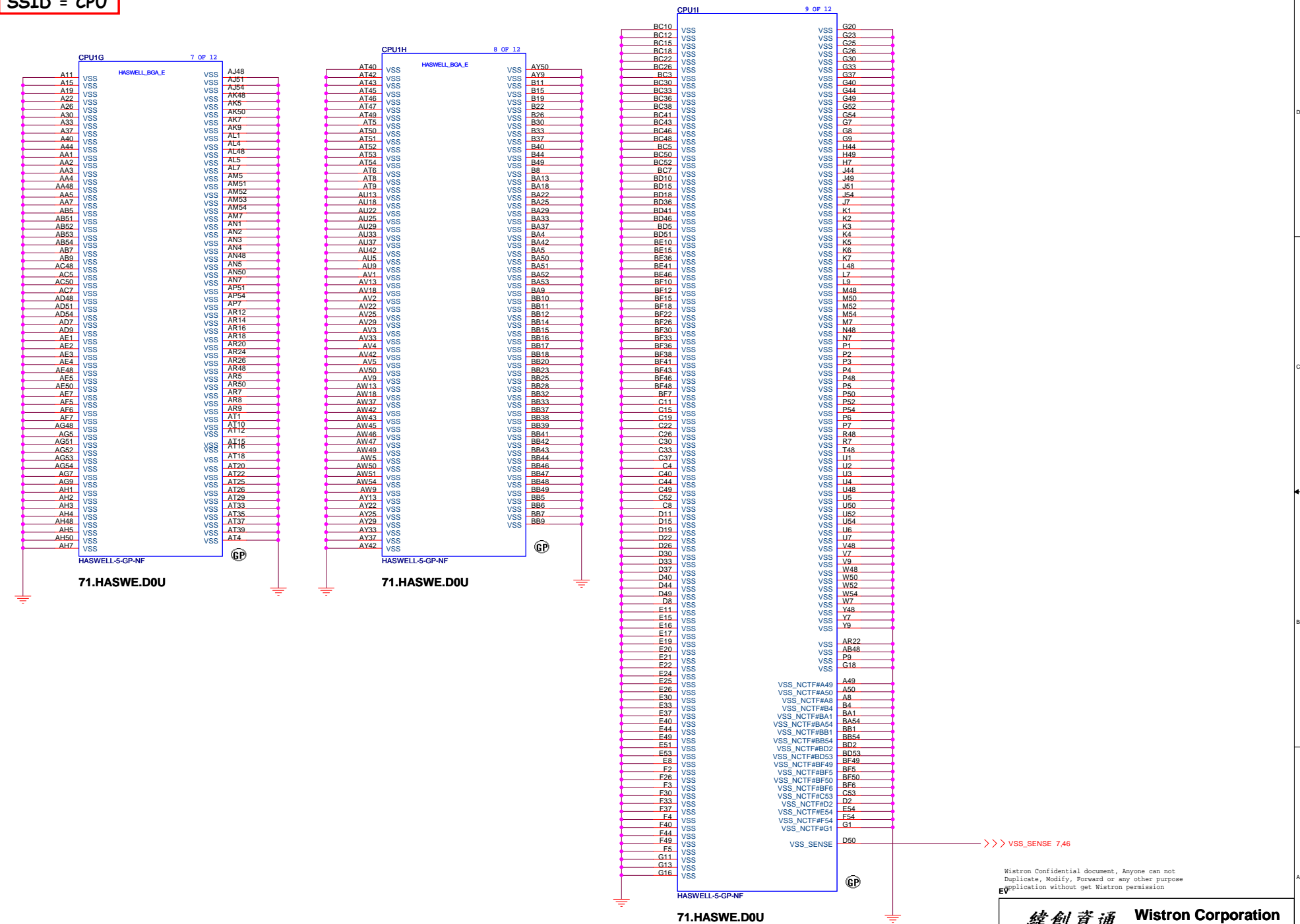


+VCOMP_OUT

Layout Note:

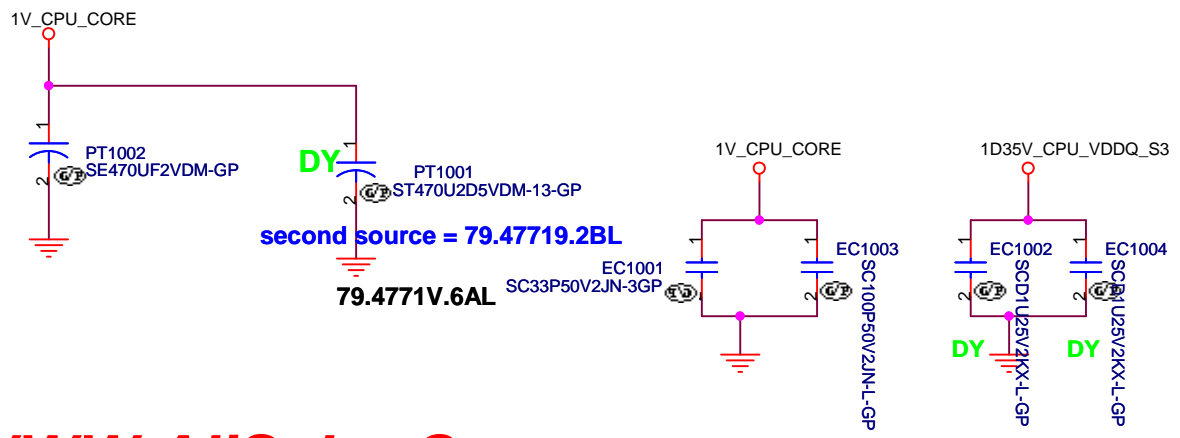
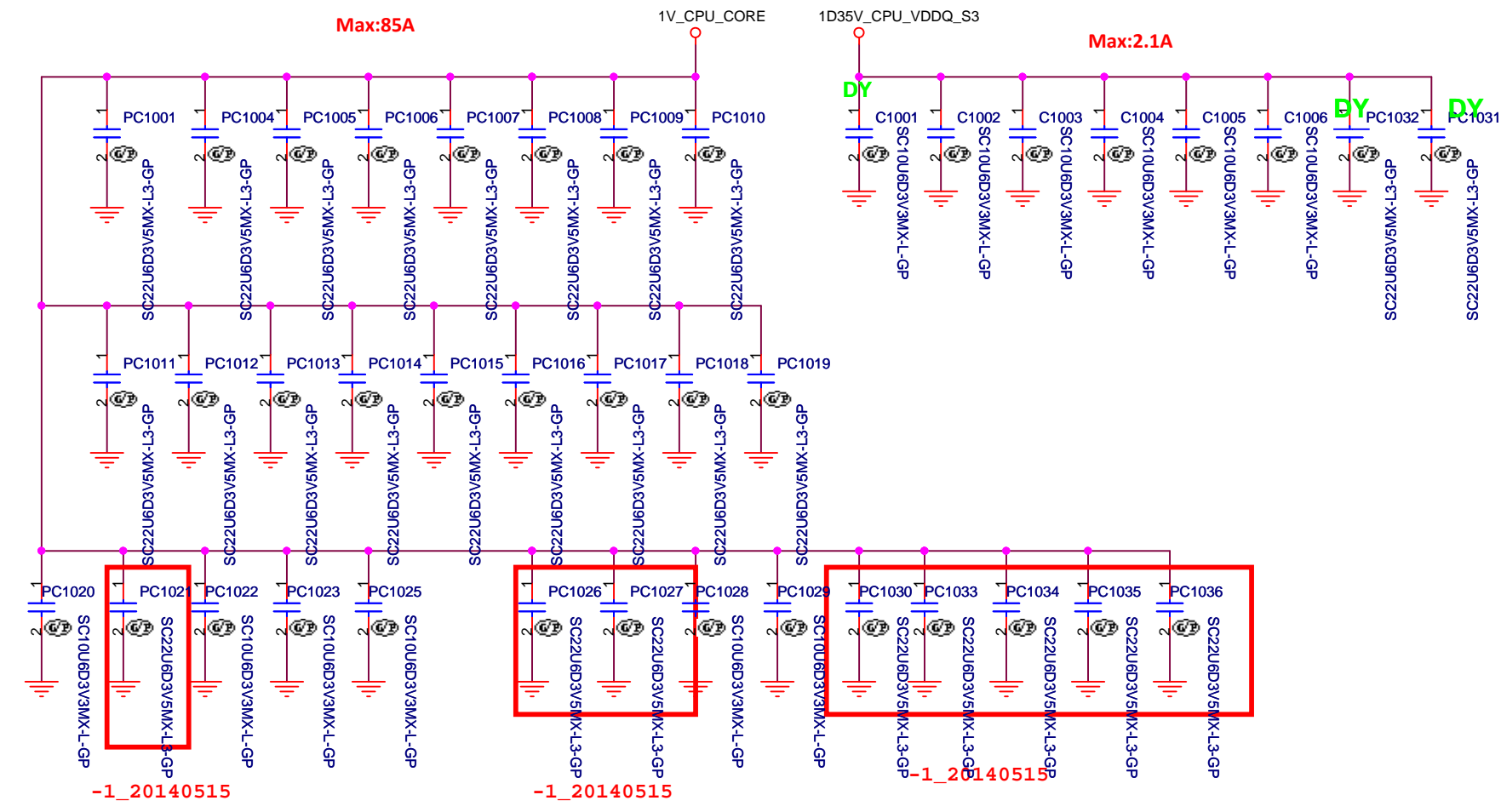


SSID = CPU



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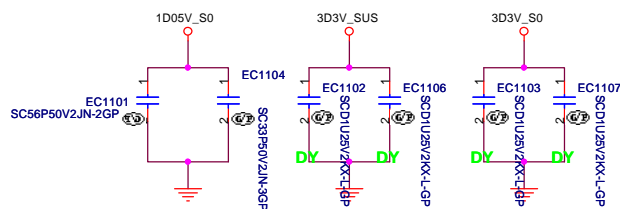
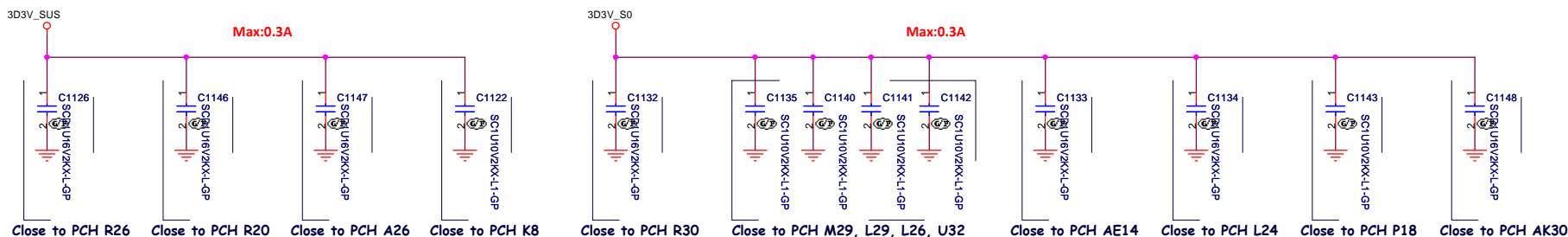
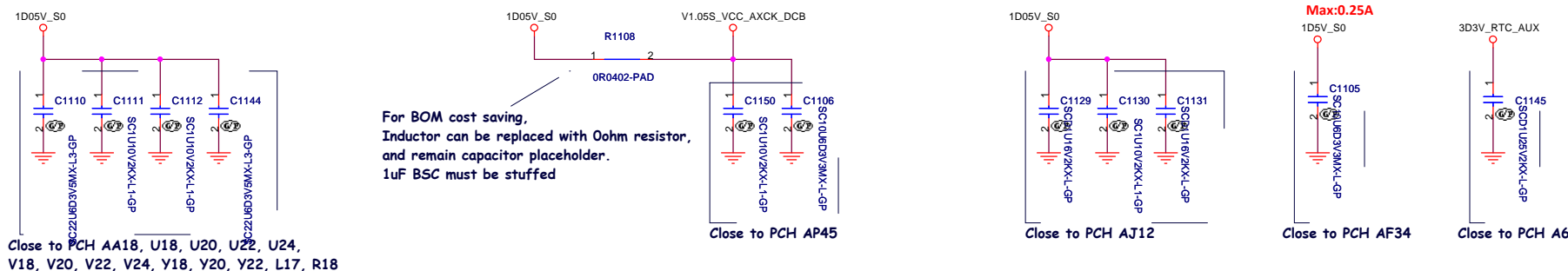
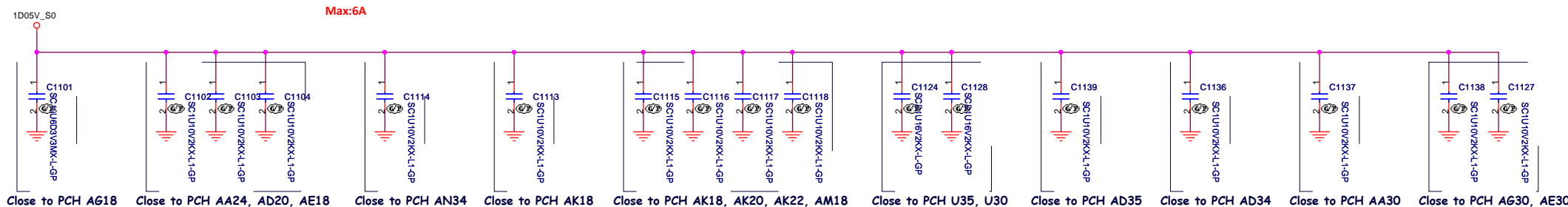
Title		
CPU (VSS)		
Size	Document Number	Rev
Custom	Poseidon 860M	-1
Date:	Tuesday, June 17, 2014	Sheet 9 of 102



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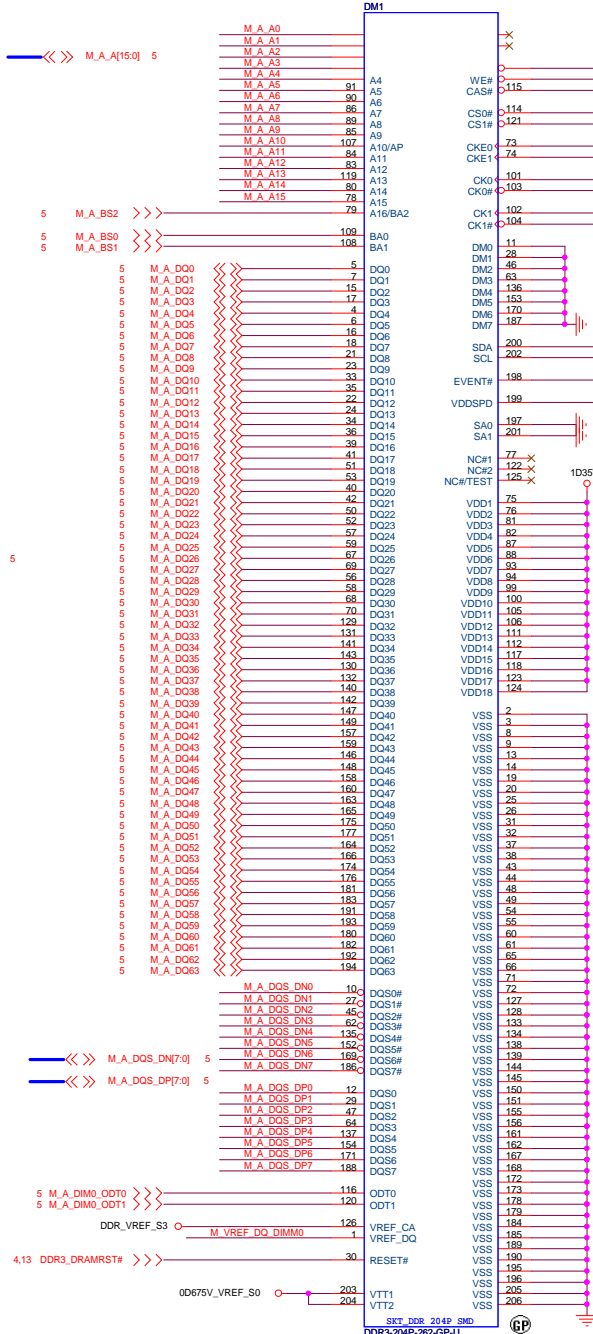
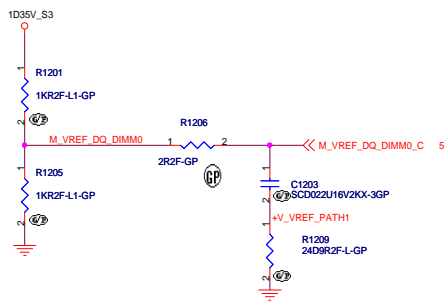
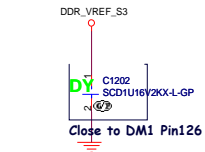
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Title CPU (Power CAP1)		
Size A4	Document Number Poseidon 860M	Rev -1
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SSID = MEMORY



62.10024.S21

2nd = 62.10024.M31

3rd = 62.10024.Q61

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

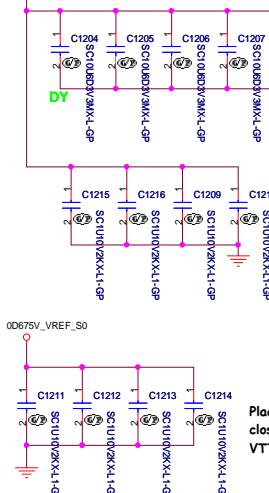
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT



Layout Note:
Place these Caps near
SO-DIMMA.

SODIMM A DECOUPLING

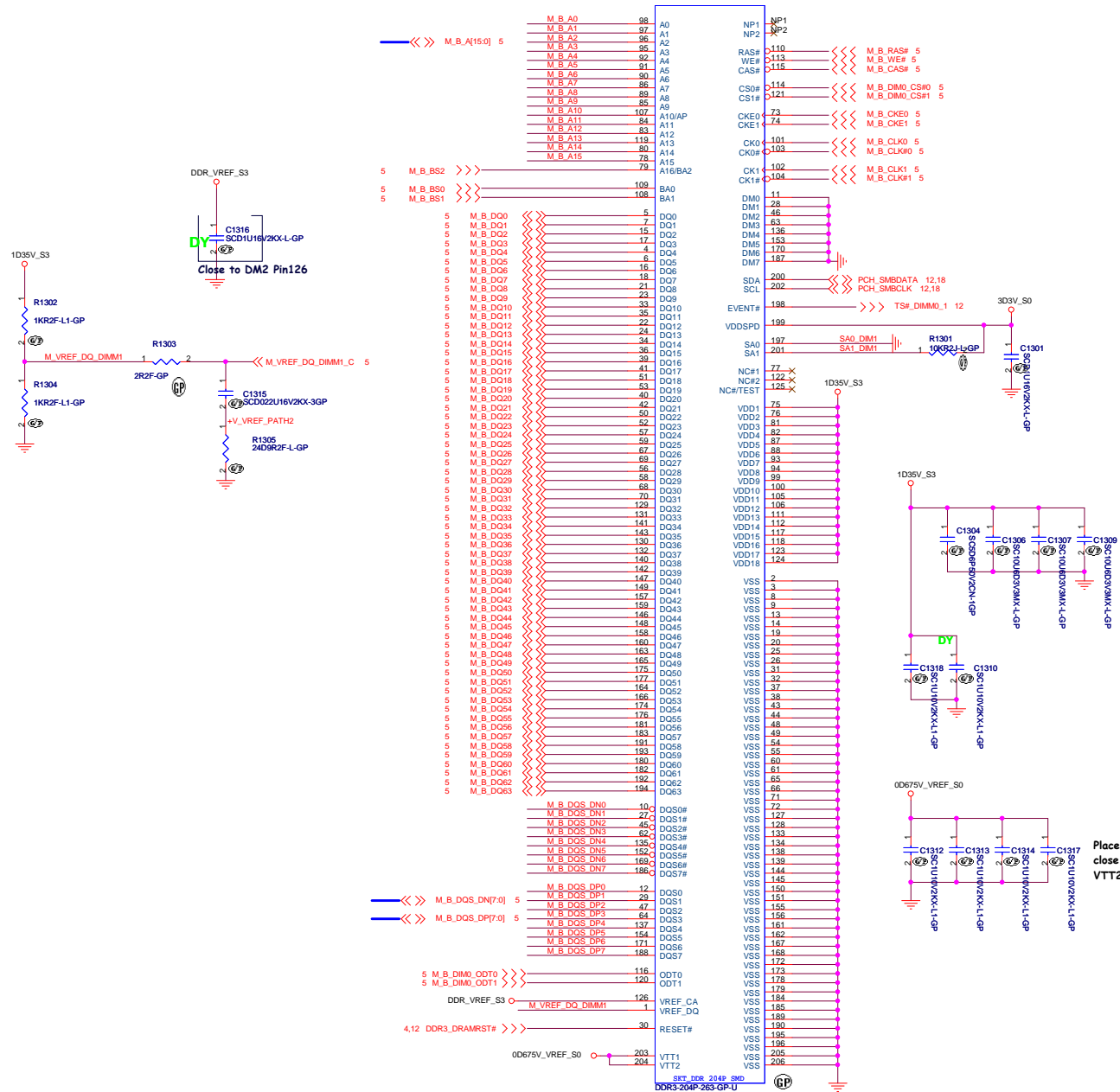


Place these caps
close to VTT1 and
VTT2.

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Title		
DDR3-SODIMM1		
Size	Document Number	Rev
Custom	Poseidon 860M	-1
Date:	106530, June 17, 2014	Sheet 12 of 102

SSID = MEMORY

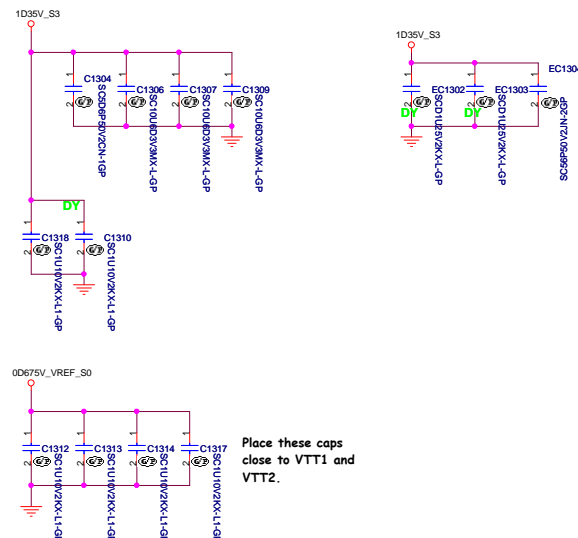


Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Layout Note:
Place these Caps near
SO-DIMMB.

SODIMM B DECOUPLING



Place these caps close to VTT1 and VTT2.

62.10024.S61

2nd = 62.10024.M51

3rd = 62.10024.Q71

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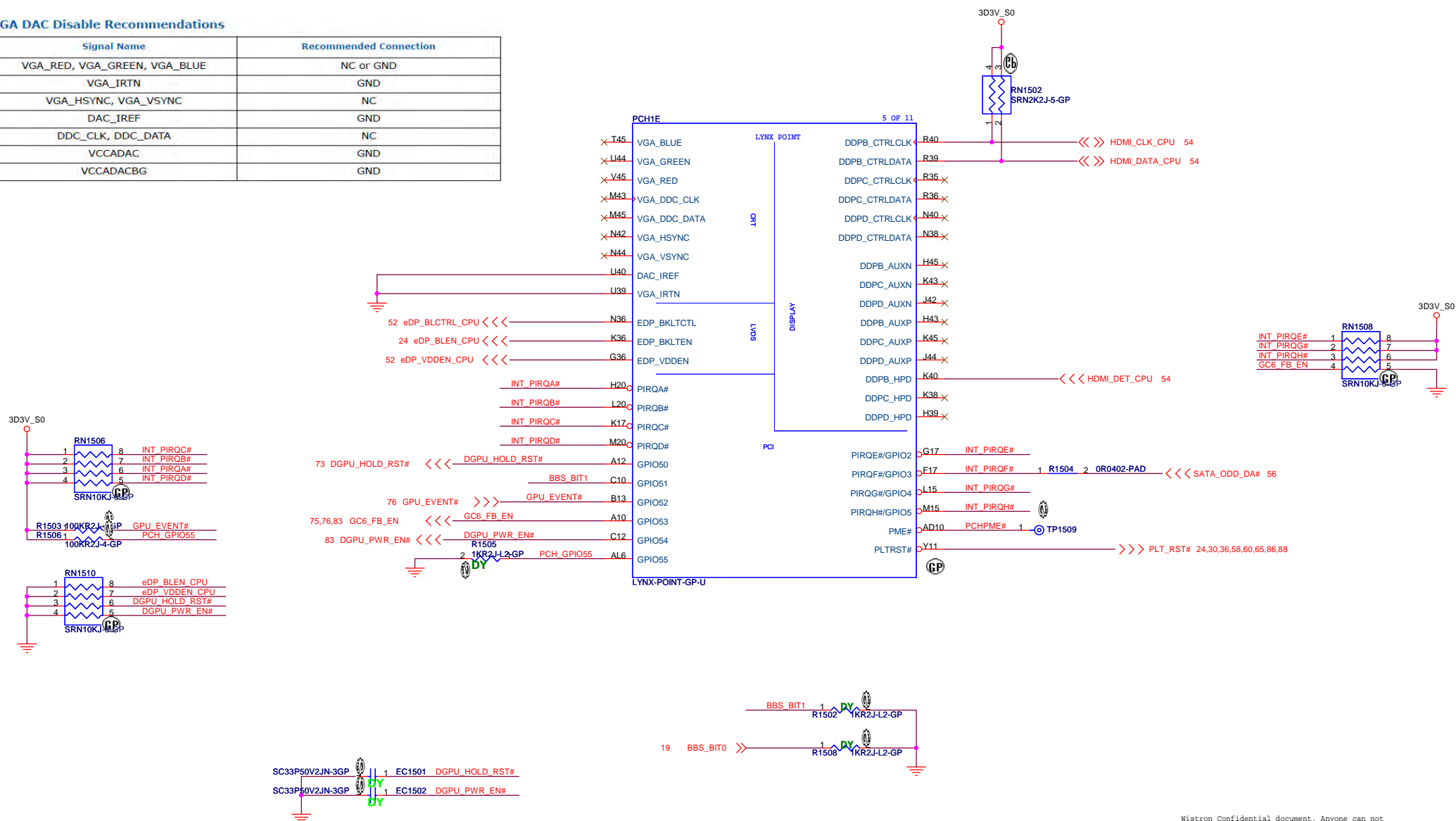
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Title			
DDR3-SODIMM2			
Size	Document Number		Rev
Customr	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014	Sheet 13 of	102

SSID = CPU

VGA DAC Disable Recommendations

Signal Name	Recommended Connection
VGA_RED, VGA_GREEN, VGA_BLUE	NC or GND
VGA_IRTN	GND
VGA_HSYNC, VGA_VSYNC	NC
DAC_IREF	GND
DDC_CLK, DDC_DATA	NC
VCCADAC	GND
VCCADACBG	GND



BOOT BIOS Strap		
GPI051	SATA1GP/GPI019	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

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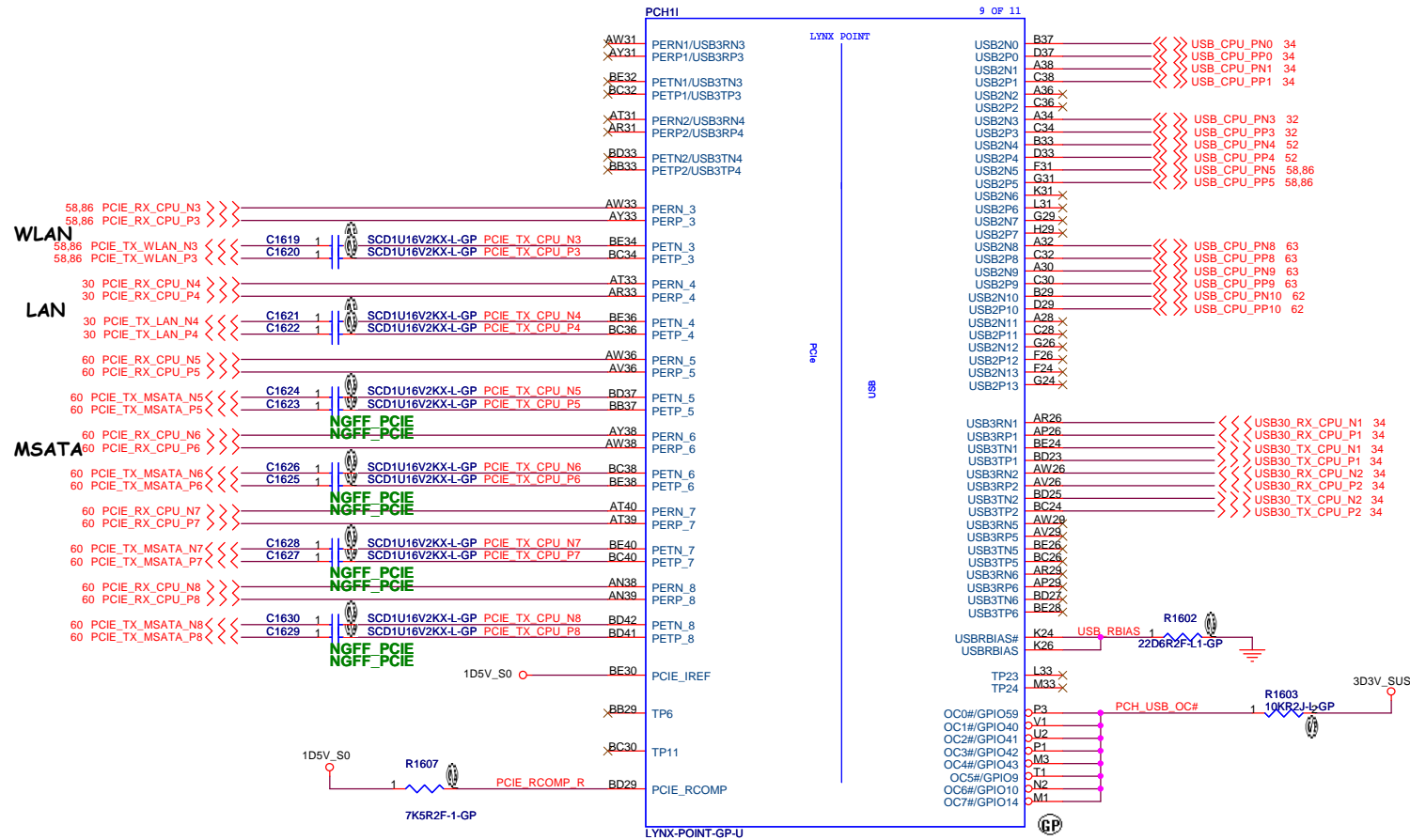
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Title			
CPU(EDP SIDEBAND/GPIO/DDI)			
Size A3	Document Number		Rev
	Poseidon 860M		-1
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SSID = PCH

USB Table

Pair	Device
0	USB3.0(port0)
1	USB3.0(port1)
2	
3	Card Reader
4	CCD
5	Mini Card1 (WLAN)
6	TOUCH PANEL
7	
8	USB2.0
9	USB2.0
10	TOUCH PAD
11	
12	
13	



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Title

CPU (PCI/USB)

Size

Size	Document Number
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Custom	Poseidon_860M
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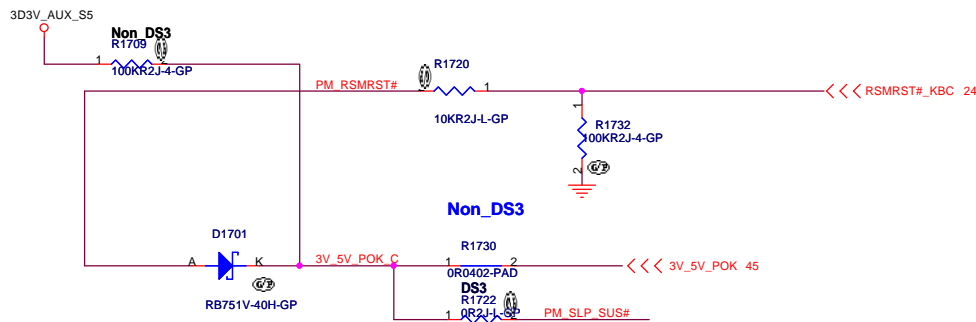
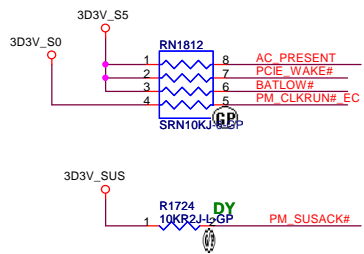
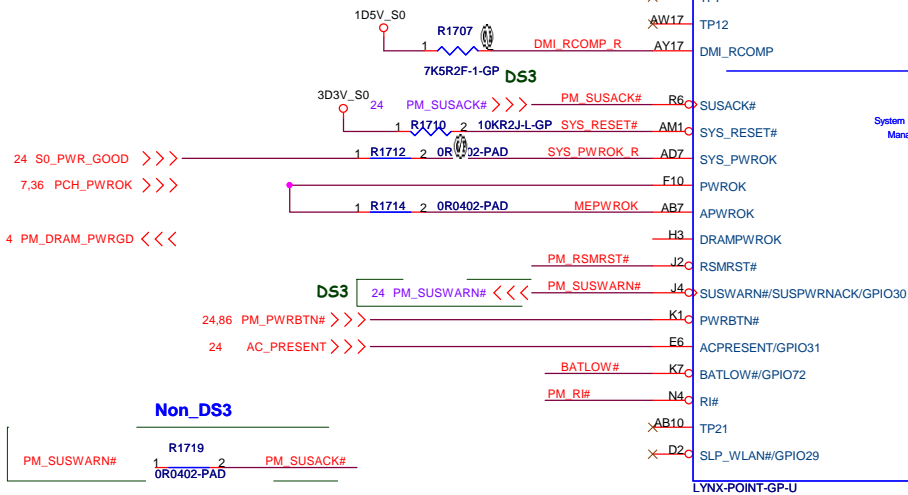
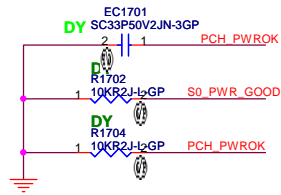
Date: Tuesday, June 17, 2014

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Rev

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SSID = PCH

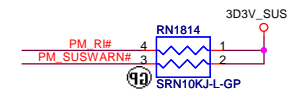
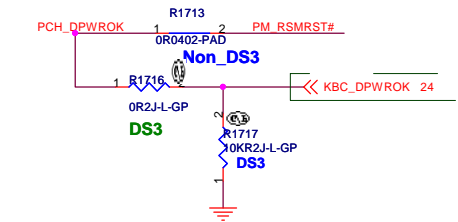


DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

The schematic shows two pins of component R1706. Pin 1 is labeled "DSWODVREN" and has a red wire extending from it. Pin 2 is labeled "GP". A blue triangle symbol connects pin 2 to the label "3D3V_RTC_AUX".

Intel® FDI Signal Disabling and Termination Guidelines

Signal	Description	Disable Guidelines
FDI_RXP[0:1] FDI_RXN[0:1]	Intel FDI Receive Differential Pair on PCH	Float
FDI_TXP[0:1] FDI_TXN[0:1]	Intel FDI Transmit Differential Pair on Processor	Float
FDI_CSYN	Intel FDI Composite Sync	Connect to Processor and PCH
DISP_INT	Intel FDI Hot Plug Interrupt	Connect to Processor and PCH
FDI_RCOMP	FDI Resistor Compensation	Float
FDI_IREF	FDI Reference Voltage	Float



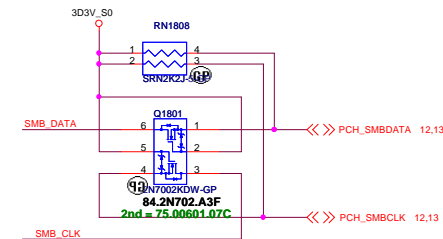
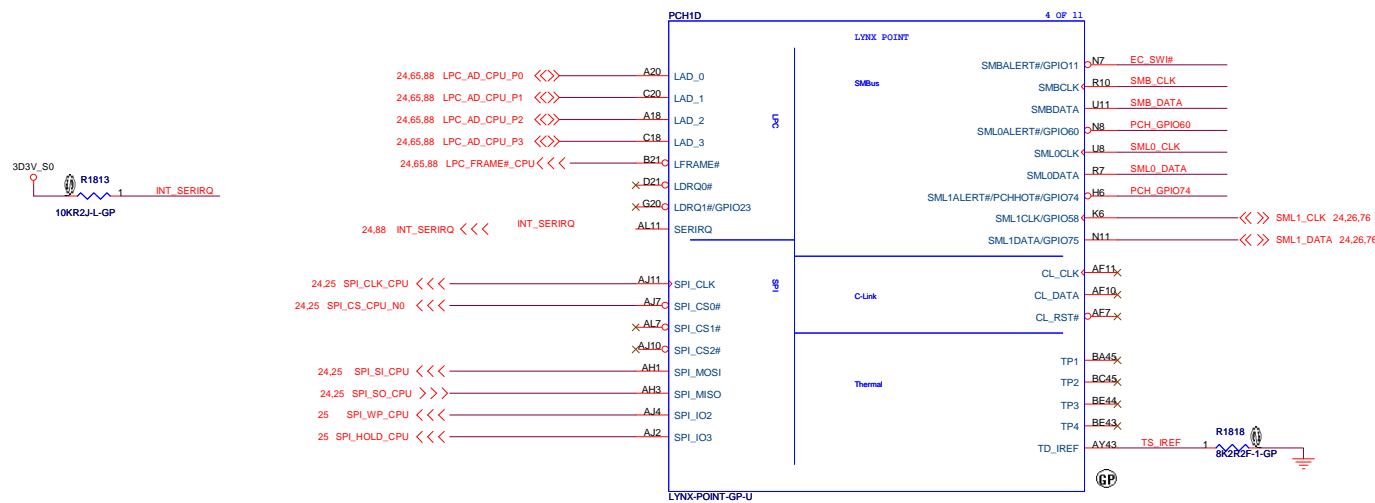
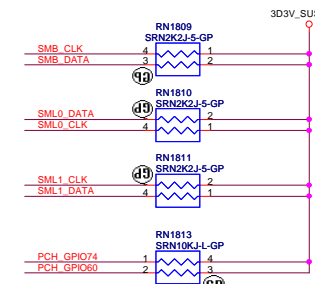
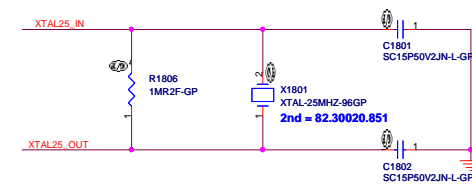
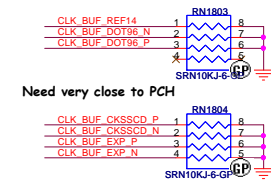
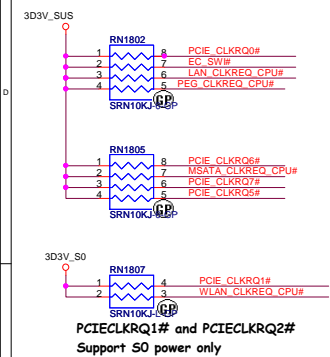
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Title			
CPU (DMI/FDI/PM)			
Size A3	Document Number		Rev
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SSID = PCH

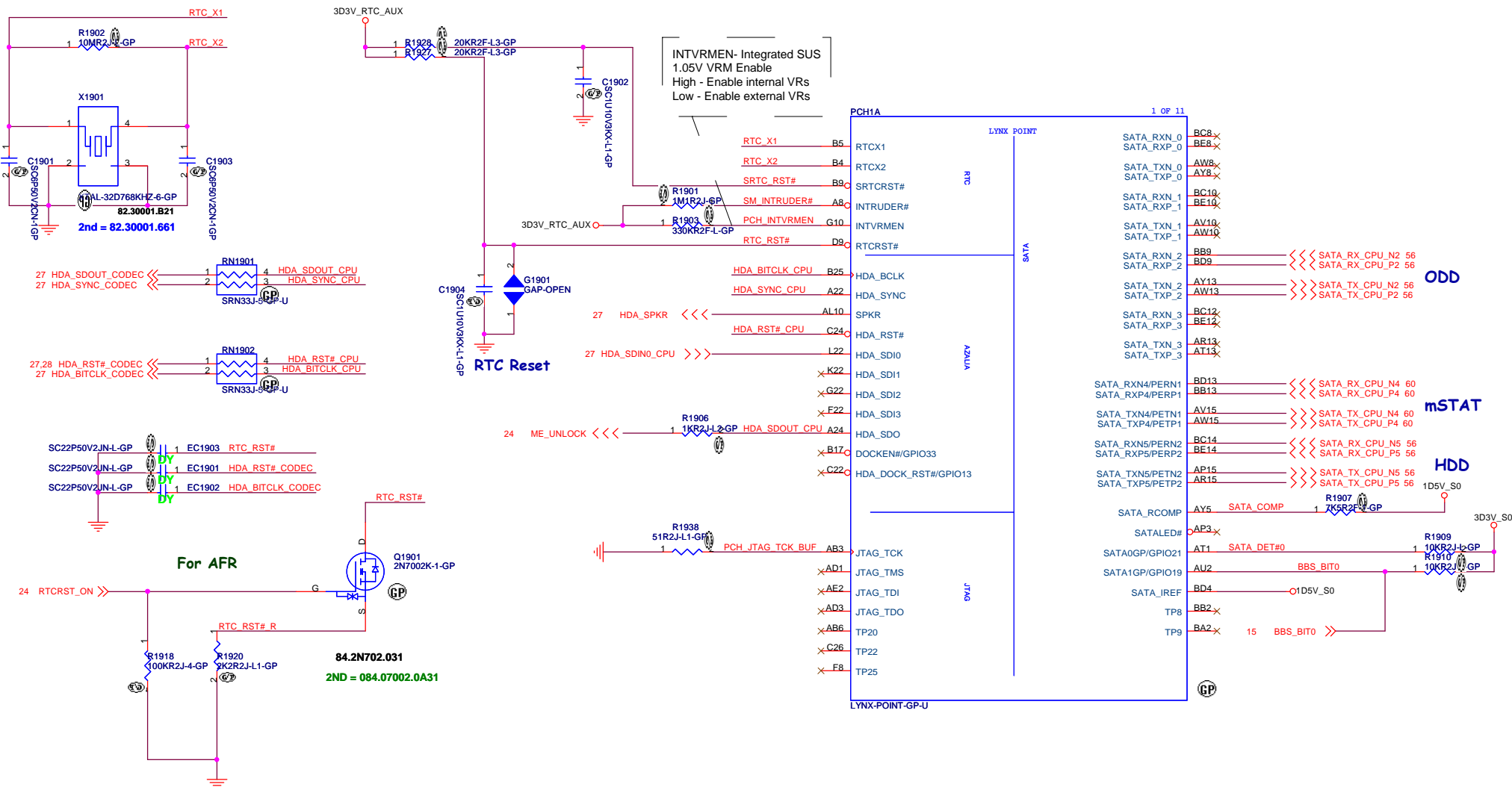


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Title		
CPU (PCI-E/SMBUS/CLOCK/CL)		
Size	Document Number	Rev
Custom	Poseidon 860M	-1
Date	Wednesday, June 17, 2014	Sheet 18 of 102

SSID = PCH



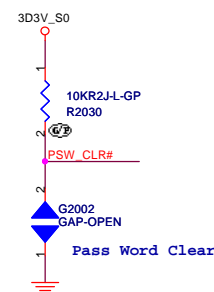
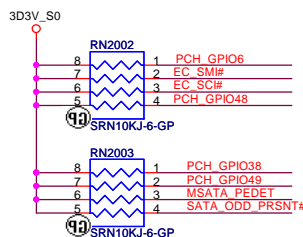
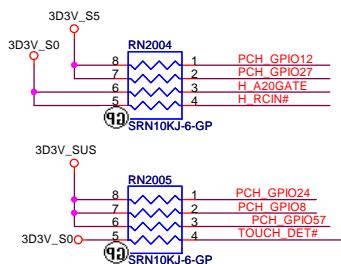
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

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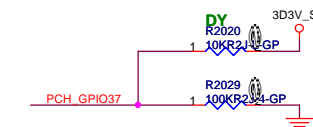
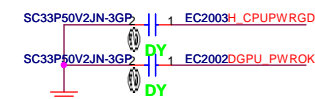
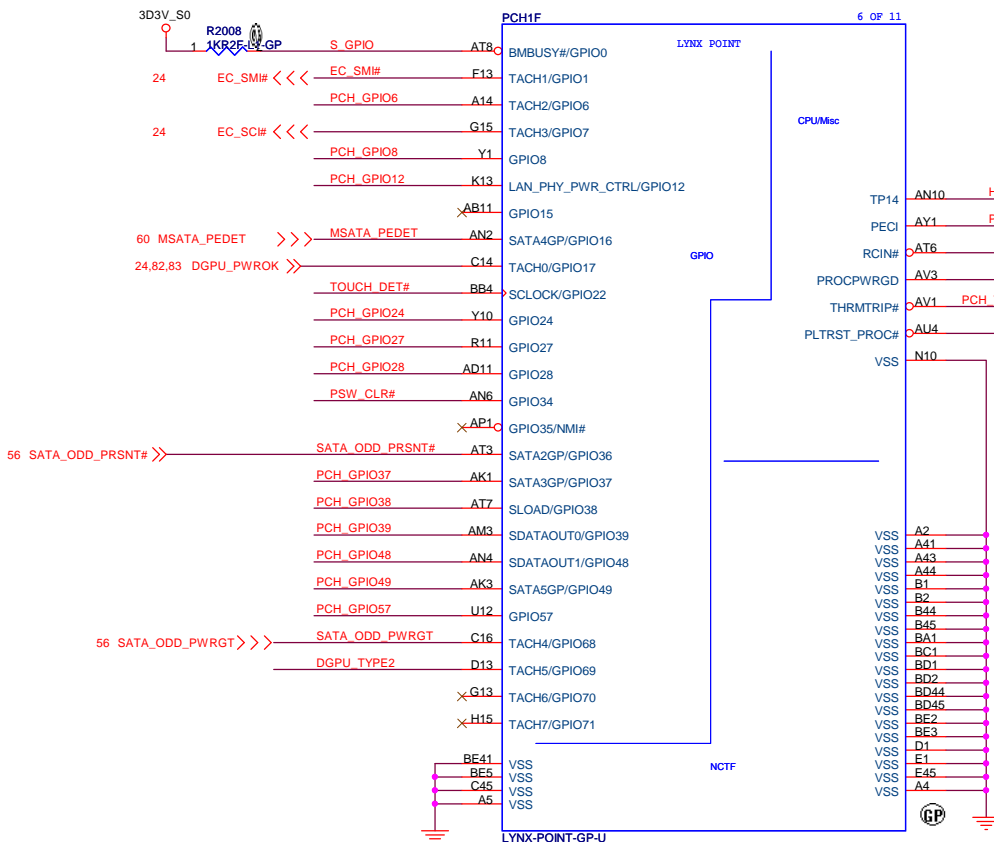
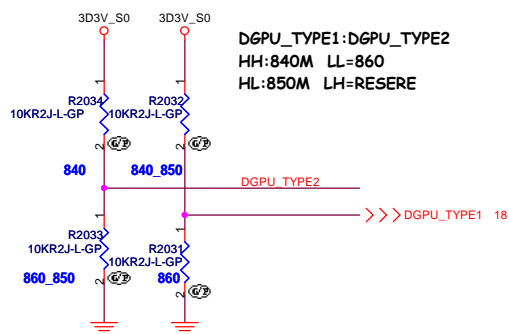
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Title		
CPU (RTC/LPC/SATA/HDA)		
Size	Document Number	Rev
Custom	Poseidon 860M	-1
Date:	Tuesday, June 17, 2014	Sheet 19 of 102

SSID = PCH

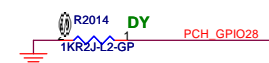


DGPU_TYPE1:DGPU_TYPE2
HH:840M LL=860
HL:850M LH=RESERE



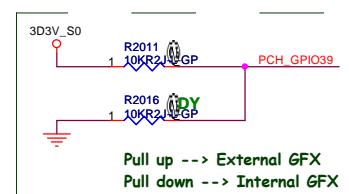
TLS Confidentiality

0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality)



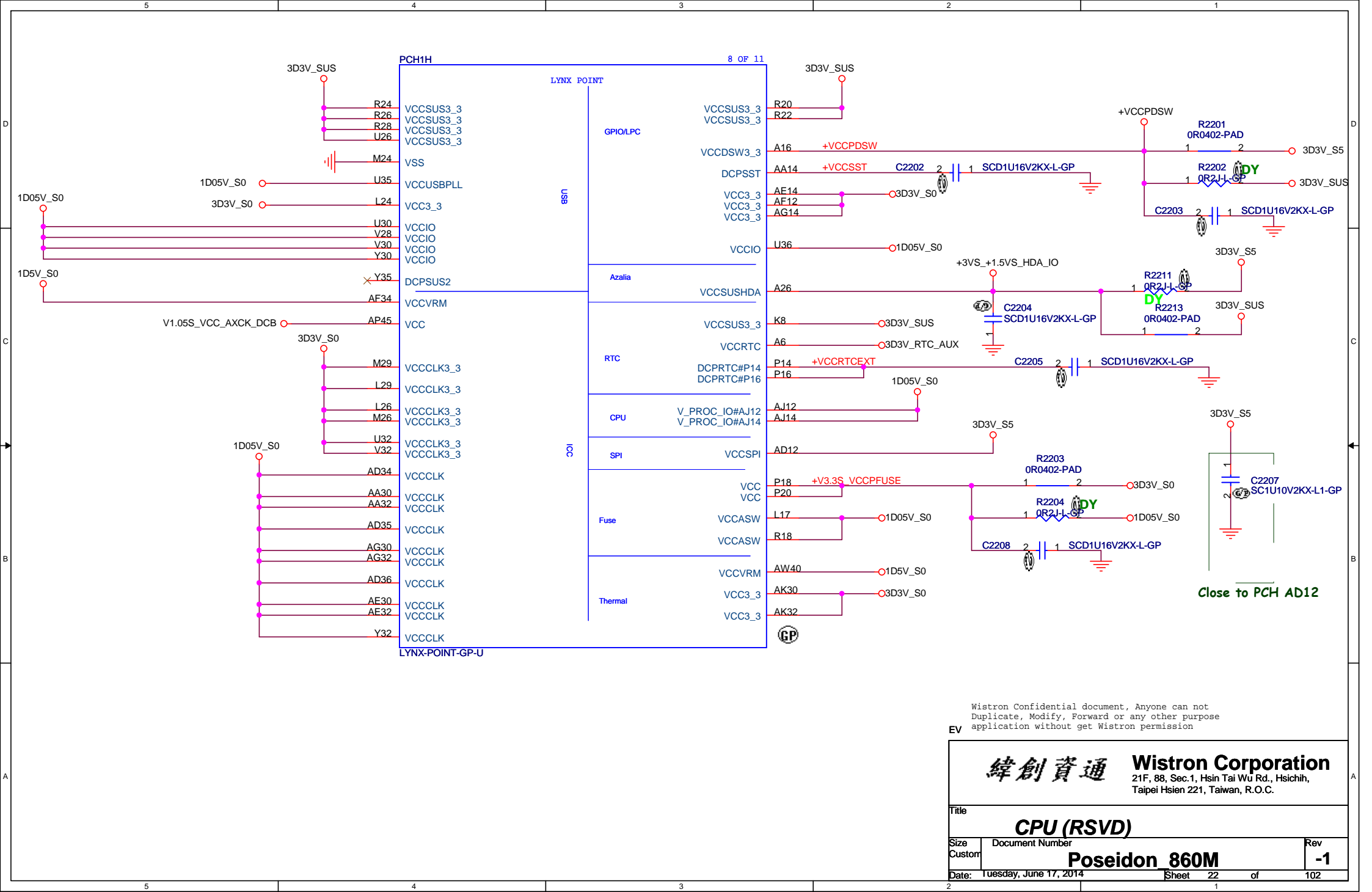
PLL ON DIE VR ENABLE

ENABLED -- HIGH (R2013 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2013 STUFFED)



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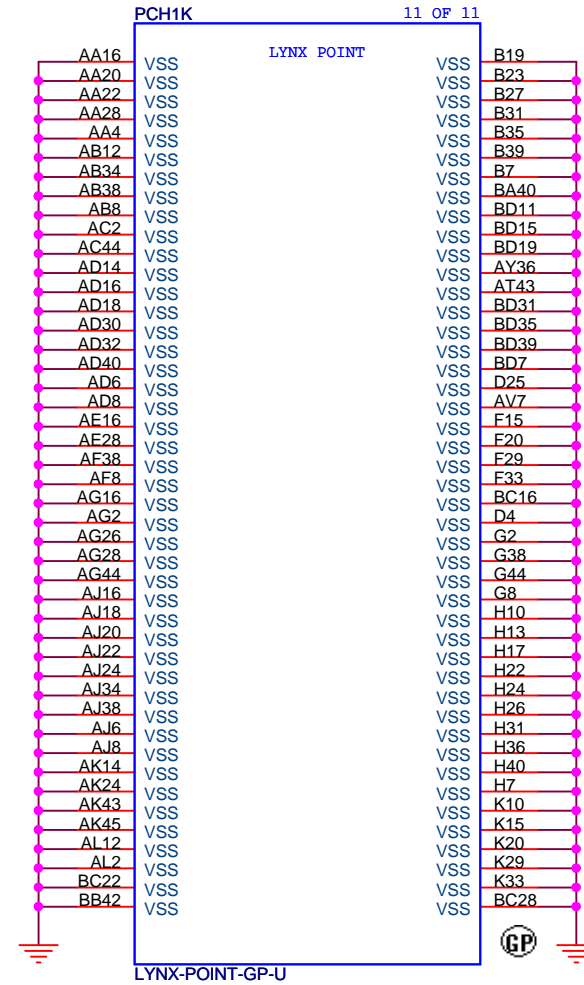


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EV

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Title			
CPU (RSVD)			
Size	Document Number		Rev
Custom	Poseidon 860M		-1
Date:	Tuesday, June 17, 2014		Sheet 22 of 102

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緯創資通

CPU (VSS)

Poseidon 860M

Sheet 23 of 102

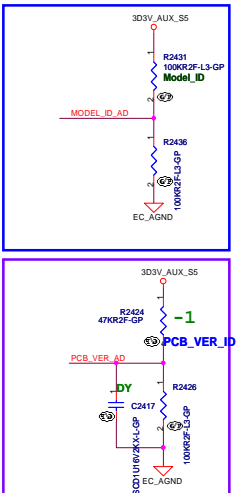
SSID = KBC

D

C

B

A

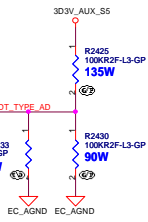


Model_AU	Pull-Low Register	Pull-High Register	Typical Voltage
VA30	100.0 K	10.0 K	3.000 V
Hades UMA	100.0 K	20.0 K	2.750 V
Hades DIS 840	100.0 K	33.0 K	2.481 V
Hades DIS 850	100.0 K	47.0 K	2.245 V
Poseidon UMA	100.0 K	64.9 K	2.001 V
Poseidon DIS 840	100.0 K	76.8 K	1.867 V
Poseidon DIS 860	100.0 K	100.0 K	1.650 V
Poseidon DIS 850	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V

PCB_Ver_AU	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
SA	100.0 K	10.0 K	3.000 V	3.0054	2.9945	>= 2.875 V
SB	100.0 K	20.0 K	2.750 V	2.7591	2.7408	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.4935	2.4688	>= 2.363 V
-1	100.0 K	47.0 K	2.245 V	2.2592	2.2305	< 2.363 V
Reserved for project use	100.0 K	64.9 K	2.001 V	2.0169	1.9854	>= 1.934 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.8827	1.8503	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.504 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.3740	1.3421	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.2197	1.1891	>= 1.126 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.0620	1.0334	< 1.126 V

3

3



ADT_Type_AU	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	Min Voltage	KBC Firmware Setting
85W	N/A	100.0 K	3.300 V			>= 3.000 V
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.3055	0.2946	>= 0.150 V
40W	20.0 K	100.0 K	0.550 V	0.5592	0.5409	>= 0.425 V
120W	33.0 K	100.0 K	0.819 V	0.8312	0.8065	< 0.884 V
130W	47.0 K	100.0 K	1.055 V	1.0695	1.0408	>= 0.937 V
150W	64.9 K	100.0 K	1.299 V	1.3146	1.2831	>= 1.177 V
Reserved	76.8 K	100.0 K	1.433 V	1.4497	1.4173	>= 1.366 V
Reserved	100.0 K	100.0 K	1.650 V	1.6665	1.6335	>= 1.542 V

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File		KBC NPCE285PA0DX	
Size	Document Number	Rev 1	
Customer		Poseldon 860M	
Date	10/25/2017, June 17, 2011	Sheet	24 of 102

5

4

2

1

SPI FLASH ROM (8M byte) for PCH

3D3V_S5

R2502 KR2F-L1-GP

R2503 3K3R2F-2-GP

R2504 KR2F-L1-GP

U2501 A25LQ64M-FF-Q-GP 072.02564.0001

2nd = 072.25B64.0001

3D3V_S5

20R2J-3-GP

15R2J-GP

15R2J-GP

33R2J-L1-GP

15R2J-GP

C2502 SCD1U3M-XL-GP

C2501 SCD1U16V2KX-L-GP

SPI_CS_ROM_N0

SPI_SO_ROM

SPI_WP_ROM

SPI_HOLD_ROM

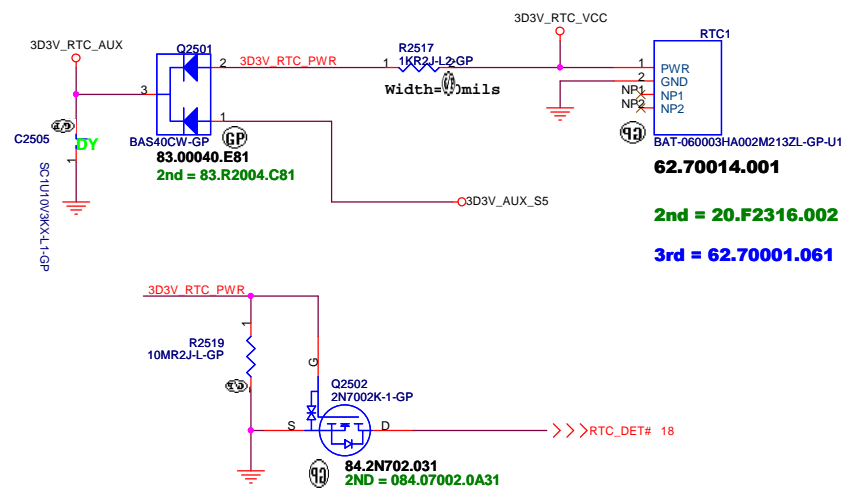
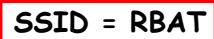
SPI_CLK_ROM

SPI_SI_ROM

SPI_HOLD_CPU

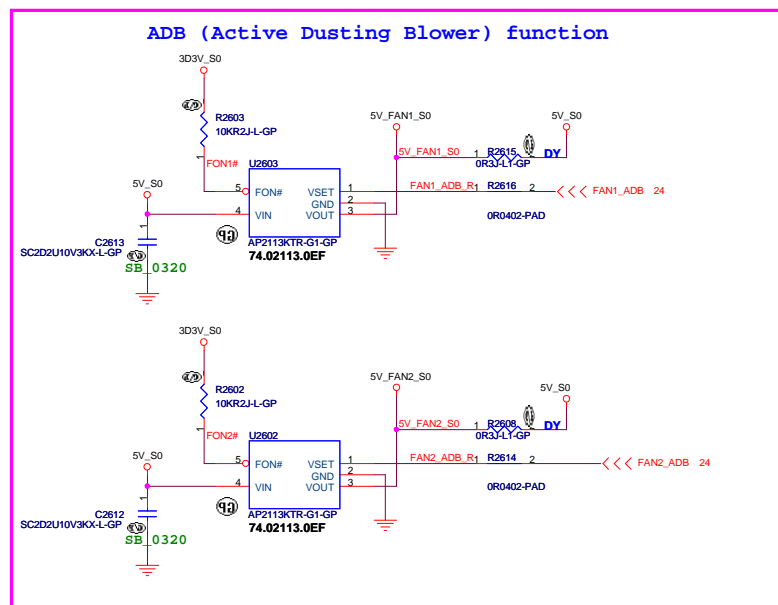
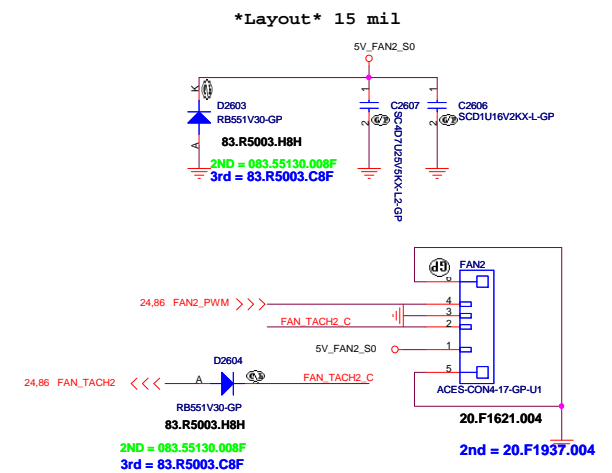
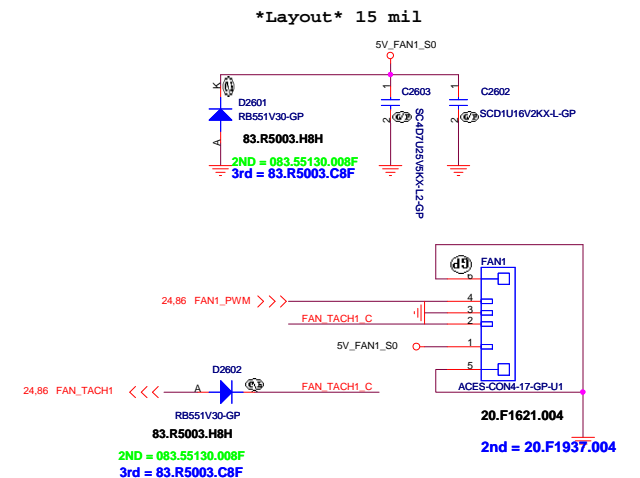
SPI_CLK_CPU

SPI_SI_CPU



Title			
Flash(KBC+PCH)/RTC			
Size A3	Document Number		Rev
	Poseidon 860M		-1
Date:	tuesday, June 17, 2014	Sheet 25 of	102

Thermal sensor NCT 7718W

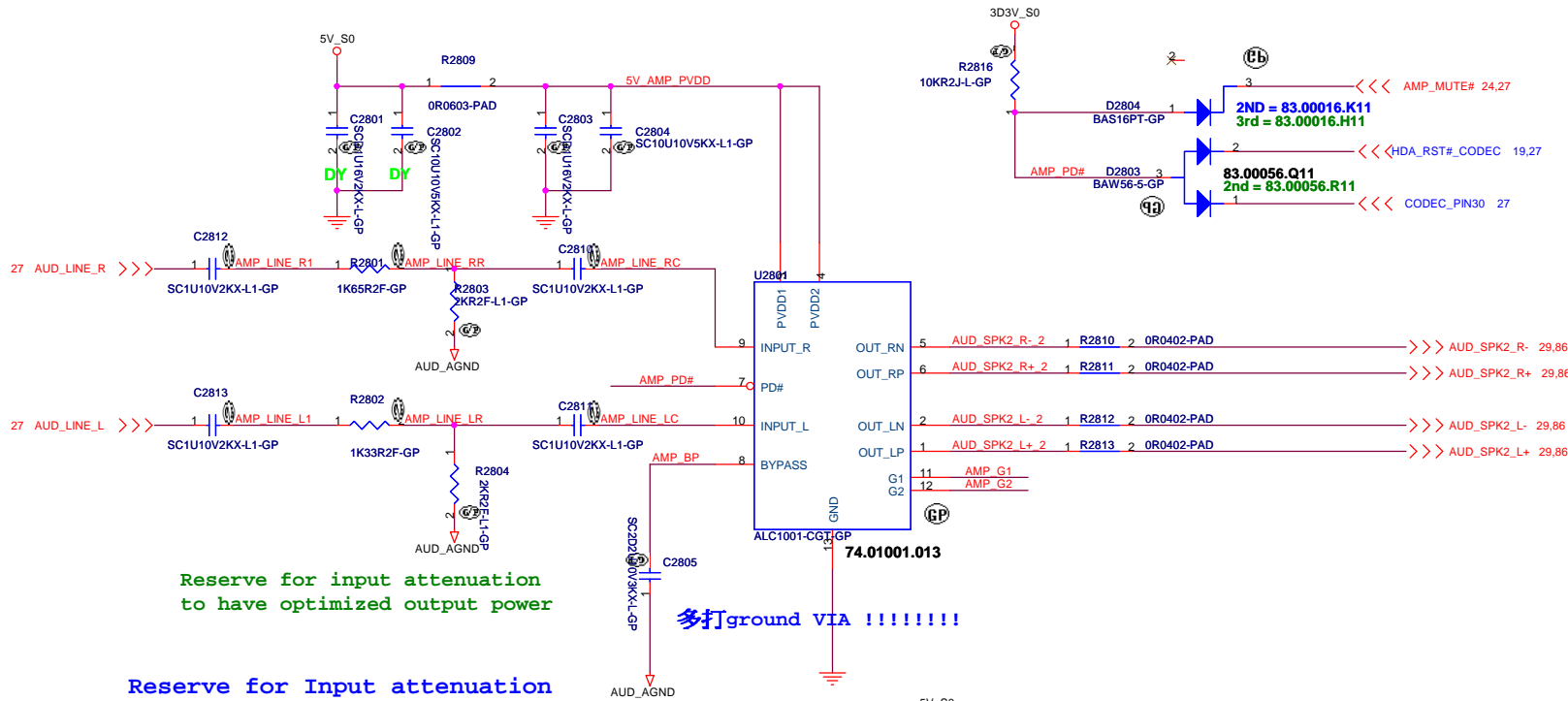


ALERT# /T CRIT#
Pull-up Resistor

	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5					
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

```
T8=85 degreeT_CRIT temperature strapping point
```

 緯創資通		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai-Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Thermal 7718/Fan Controller P2793			
Size	Document Number		Rev
Customer			-1
Poseidon 860M			
Date:	100909, June 17, 2014	Sheet	26 of 102



Reserve for input attenuation
to have optimized output power

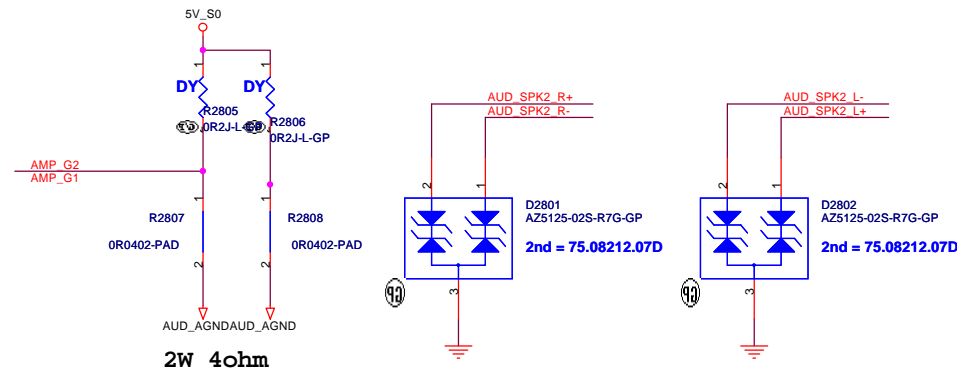
多打ground VIA !!!!!!!

Reserve for Input attenuation
To have optimization output power

Table 6. Amplifier Gain

G2	G1	Gain
0	0	11dB
0	1	14dB
1	0	19dB
1	1	25dB

*Condition is at 5V/40hm

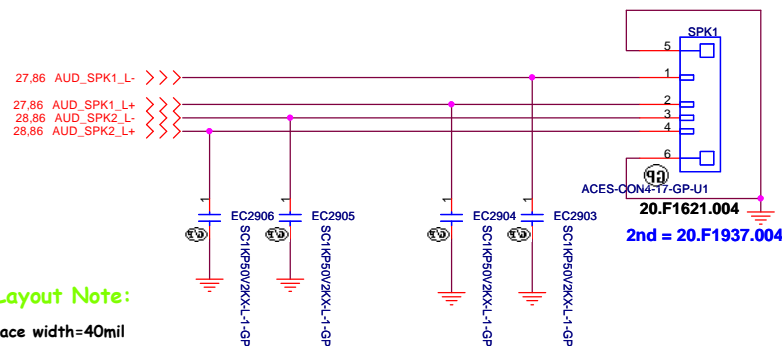
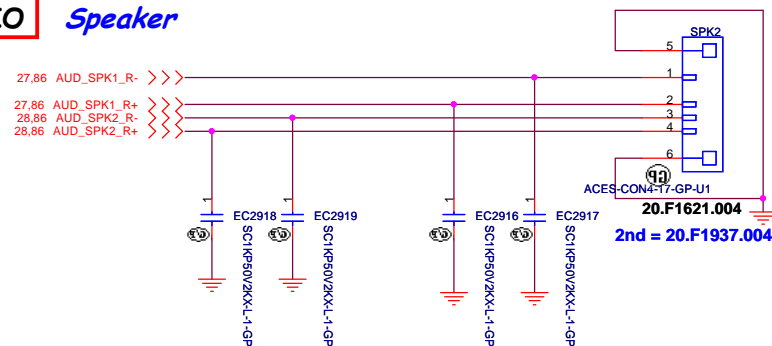


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EV

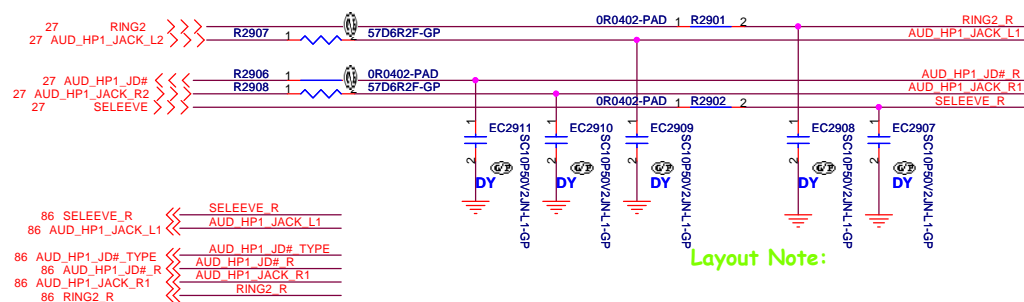
SSID = AUDIO

Speaker

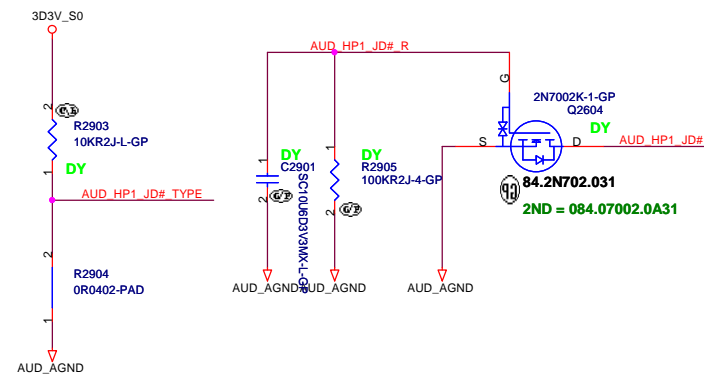
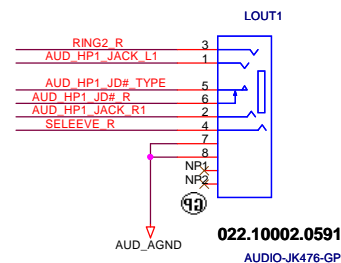


Layout Note:
Trace width=40mil

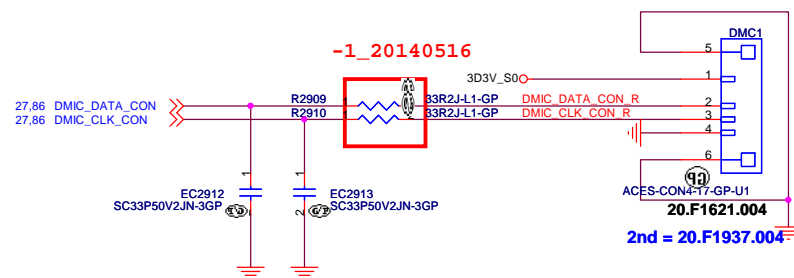
Combo Jack



Layout Note:

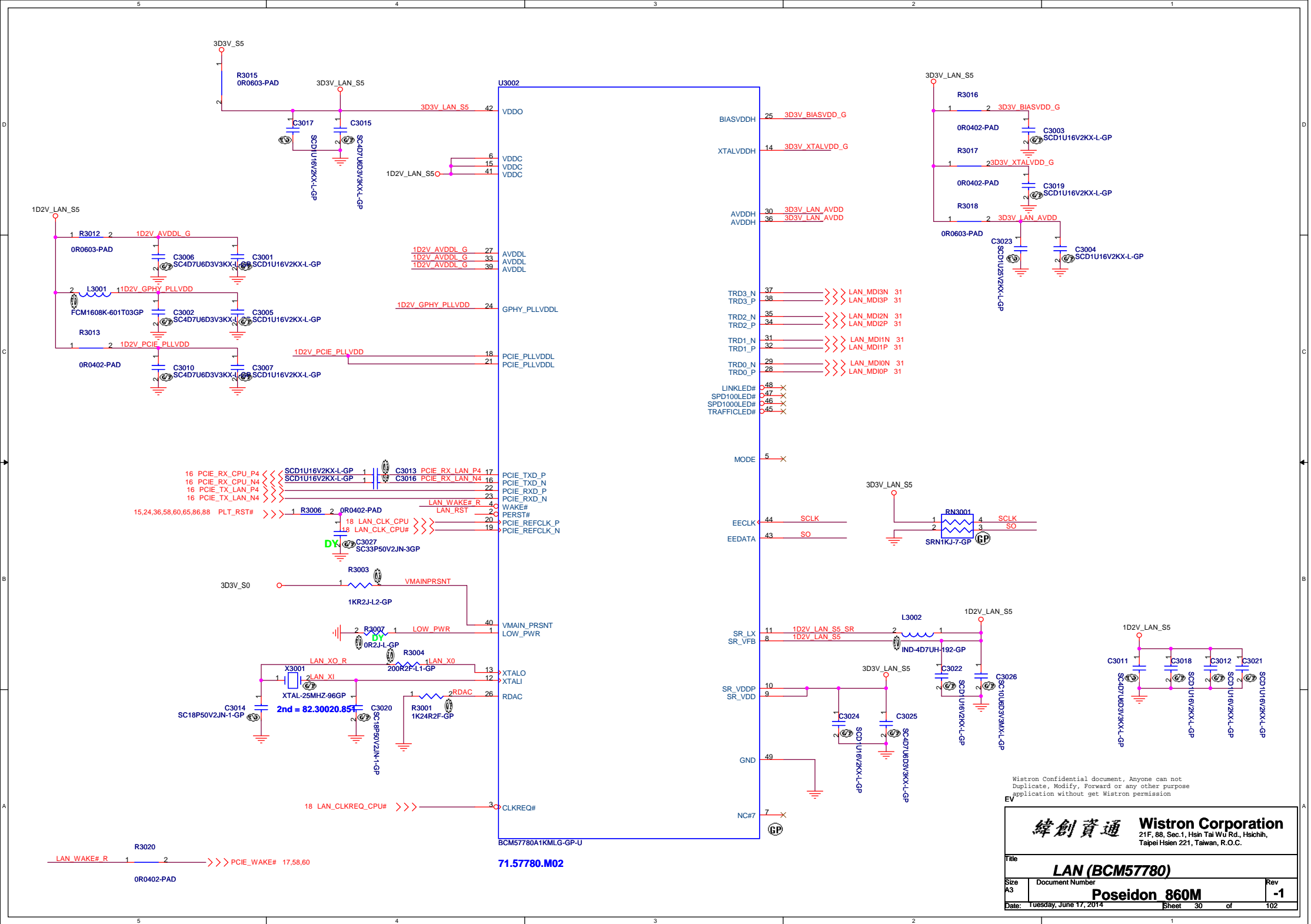


DMIC

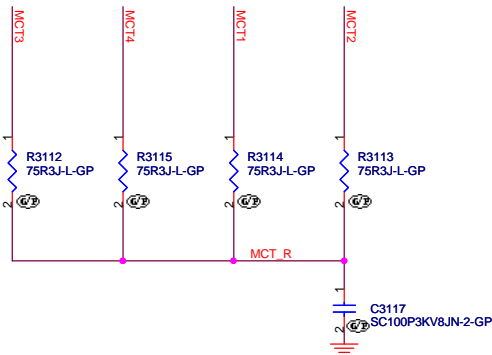
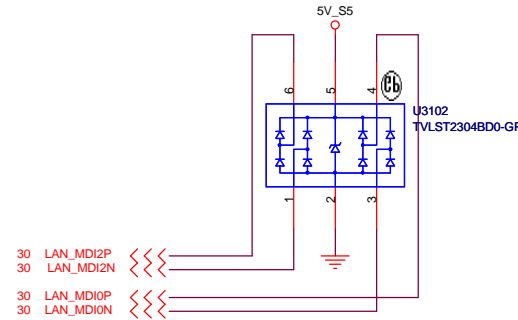
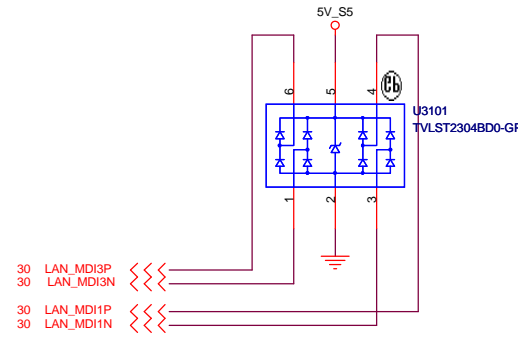
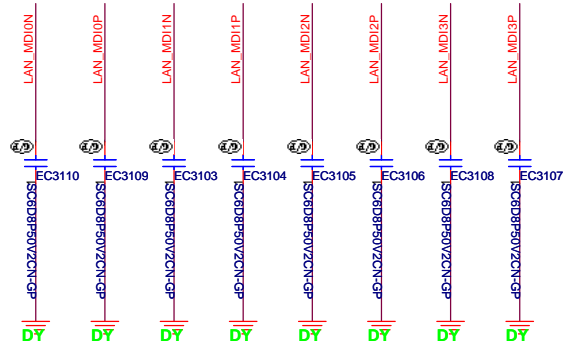
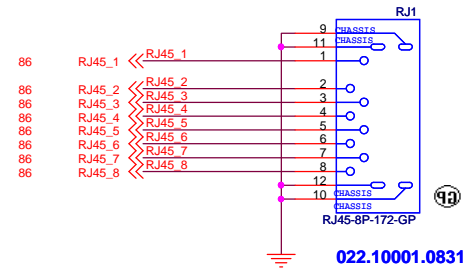
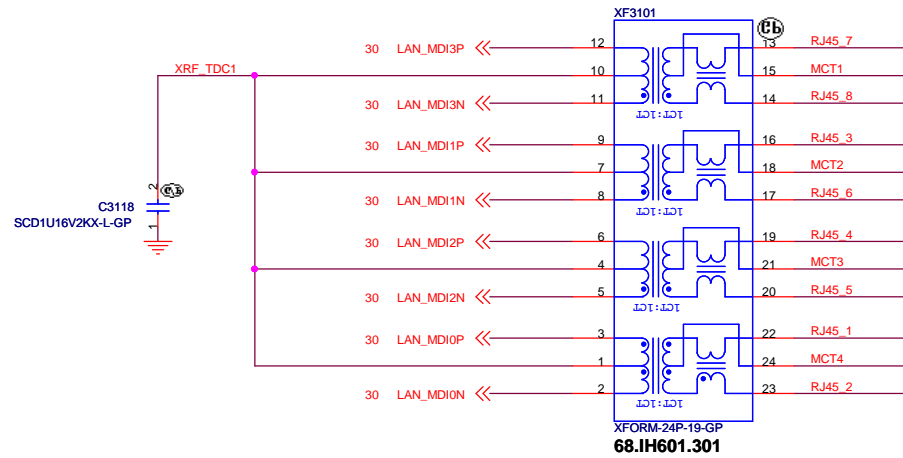


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<p>Title Audio Jack</p>		
Size Custom	Document Number Poseidon 860M	Rev -1
Date: Tuesday, June 17, 2014	Sheet 29	of 102

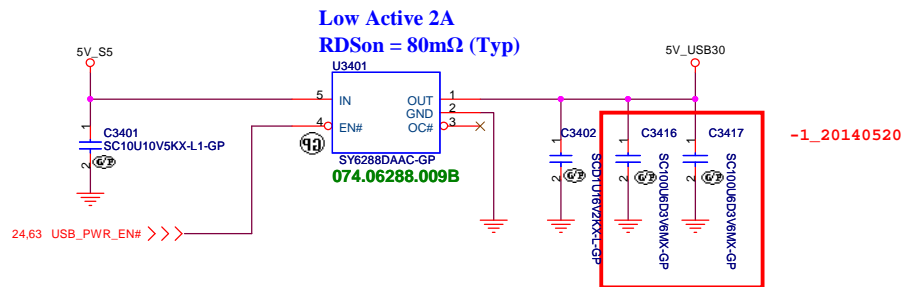


SSID = LAN



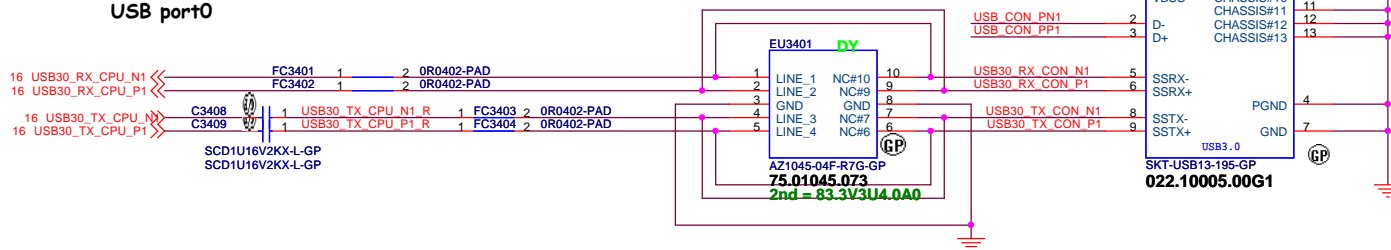
EV

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
(LAN+VGA) CONNECTOR	
Title Size Custom	Document Number Poseidon 860M
Date: Tuesday, June 17, 2014	Sheet 31 of 102

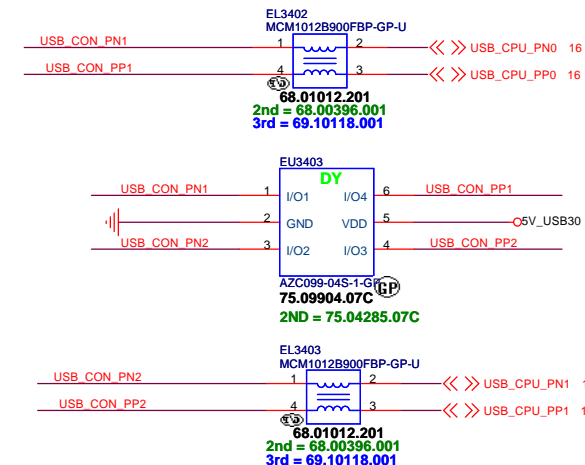
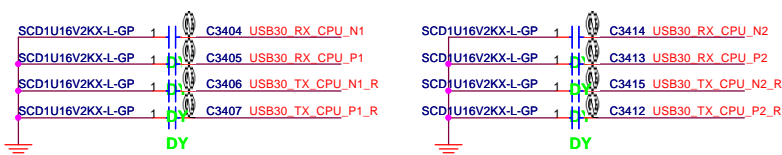
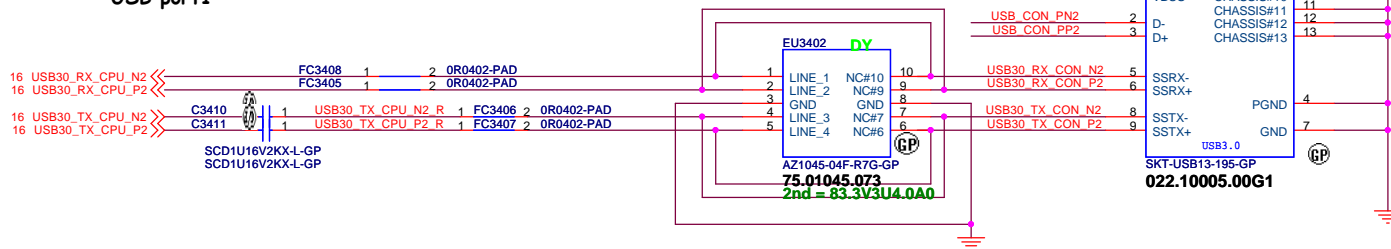


USB 3.0 Connector	
Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB port0



USB port1

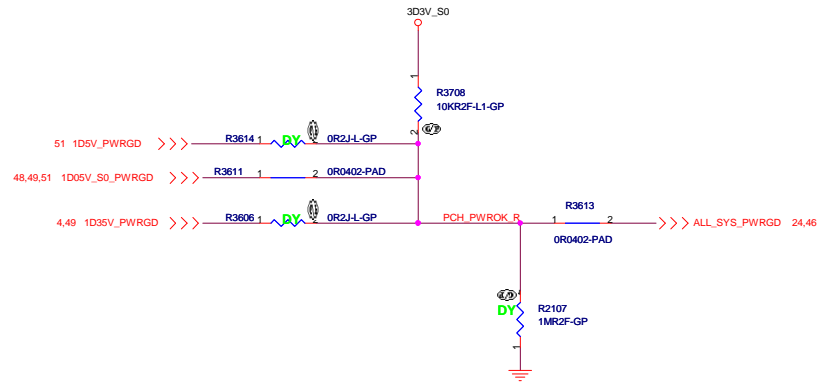
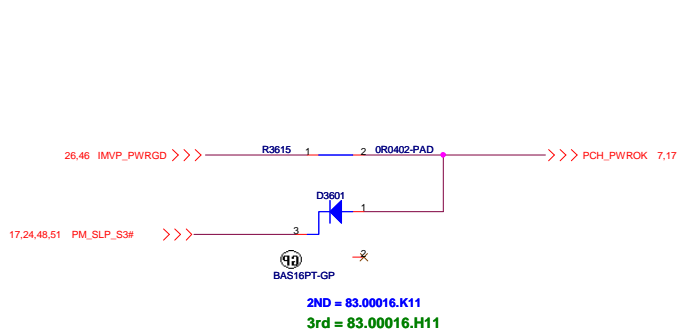


EV

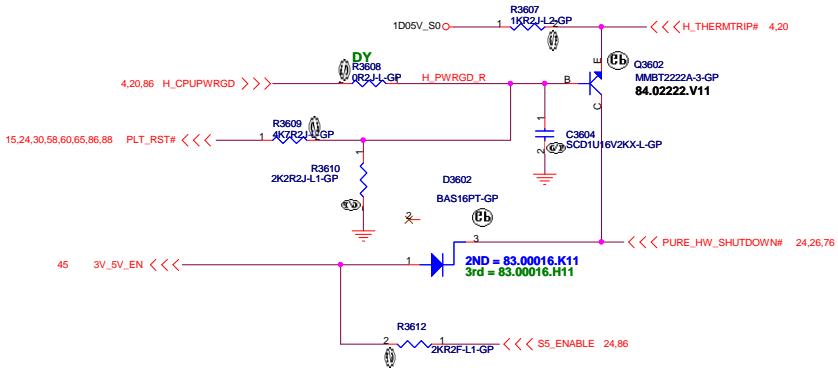
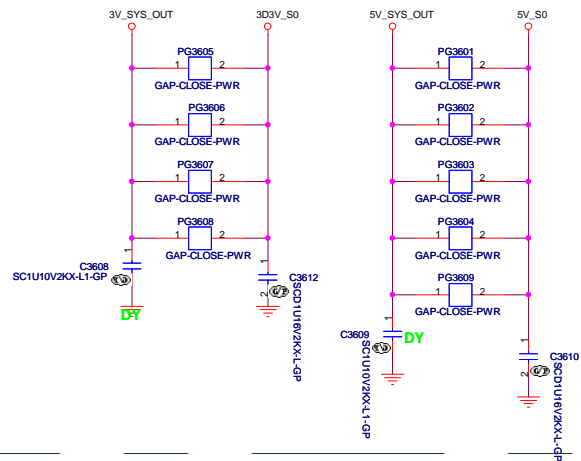
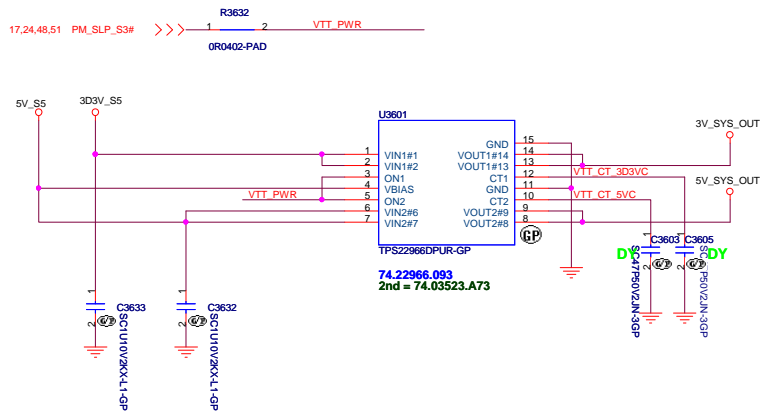
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 Taipei Hsien 221, Taiwan, R.O.C.

Title		USB 2.0 / 3.0 Port	
Size	Document Number	Poseidon 860M	
A3		-1	
Date:	Tuesday, June 17, 2014	Sheet	34 of 102

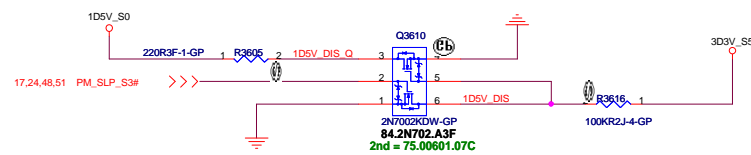
Power Sequence



ANNIE Run Power



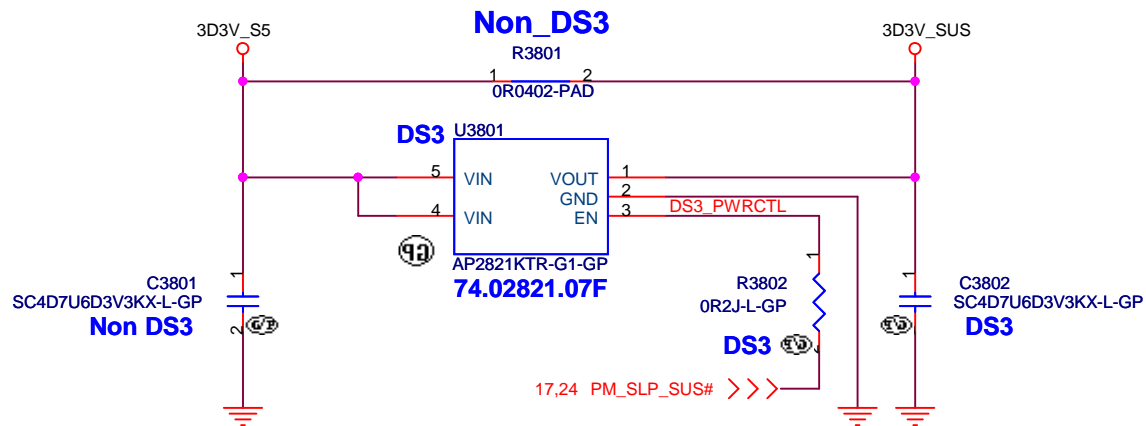
Discharge circuit



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Title			
Power Plane Enable & SEQUENCE			
Size	Document Number	Rev	
Custom	Poseidon 860M	-1	
Date:	Tuesday, June 17, 2014	Sheet	36 of 102



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EV

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Title

DS3

Size
A4

Document Number

Poseidon 860M

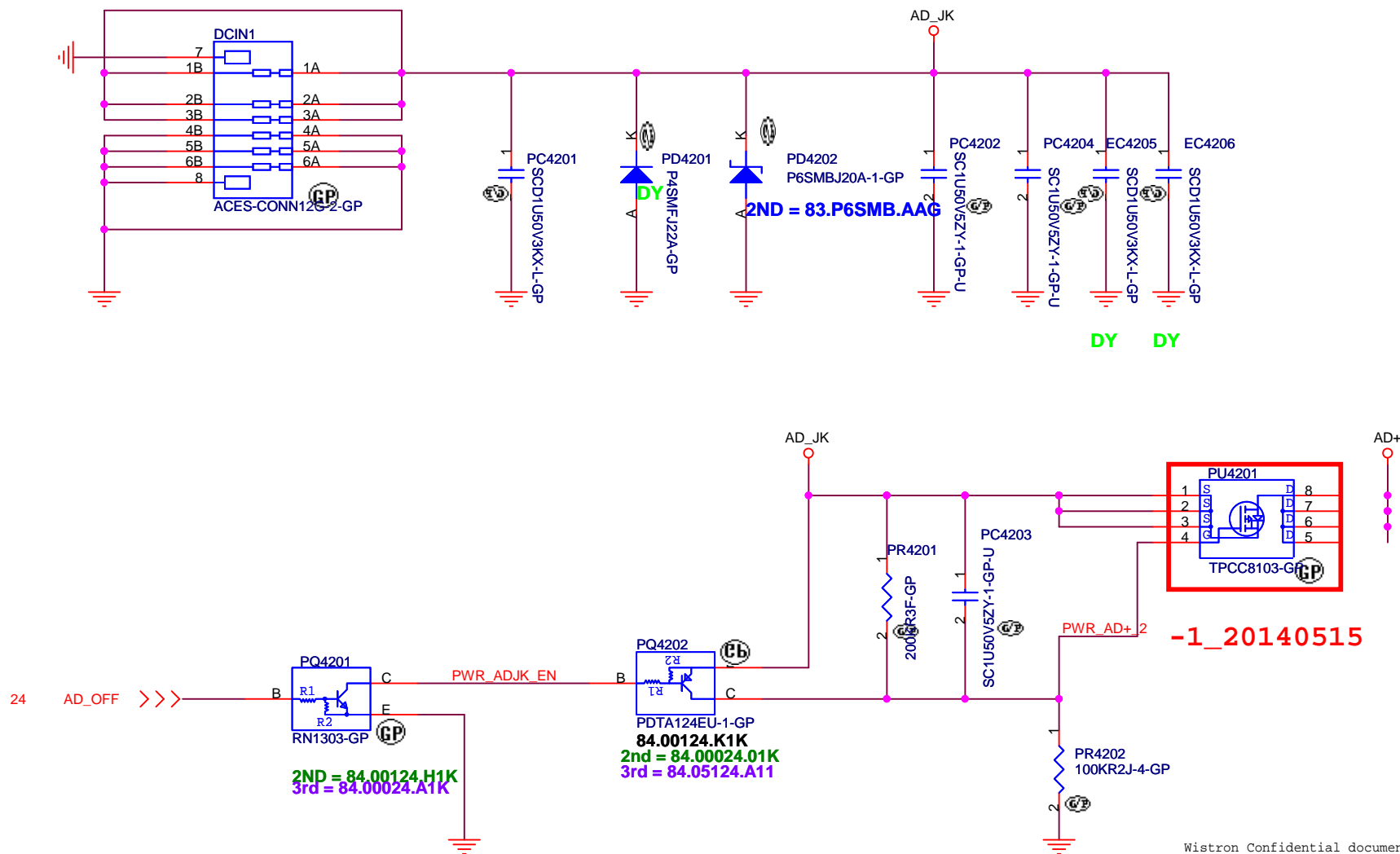
Rev
-1

Date: Tuesday, June 17, 2014

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ANNIE solution

Adaptor in to generate DCBATOUT



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Taipei Hsien 221, Taiwan, R.O.C.

Title

DCIN JACK

Size

Document Number

A4

Poseidon 860M

Rev

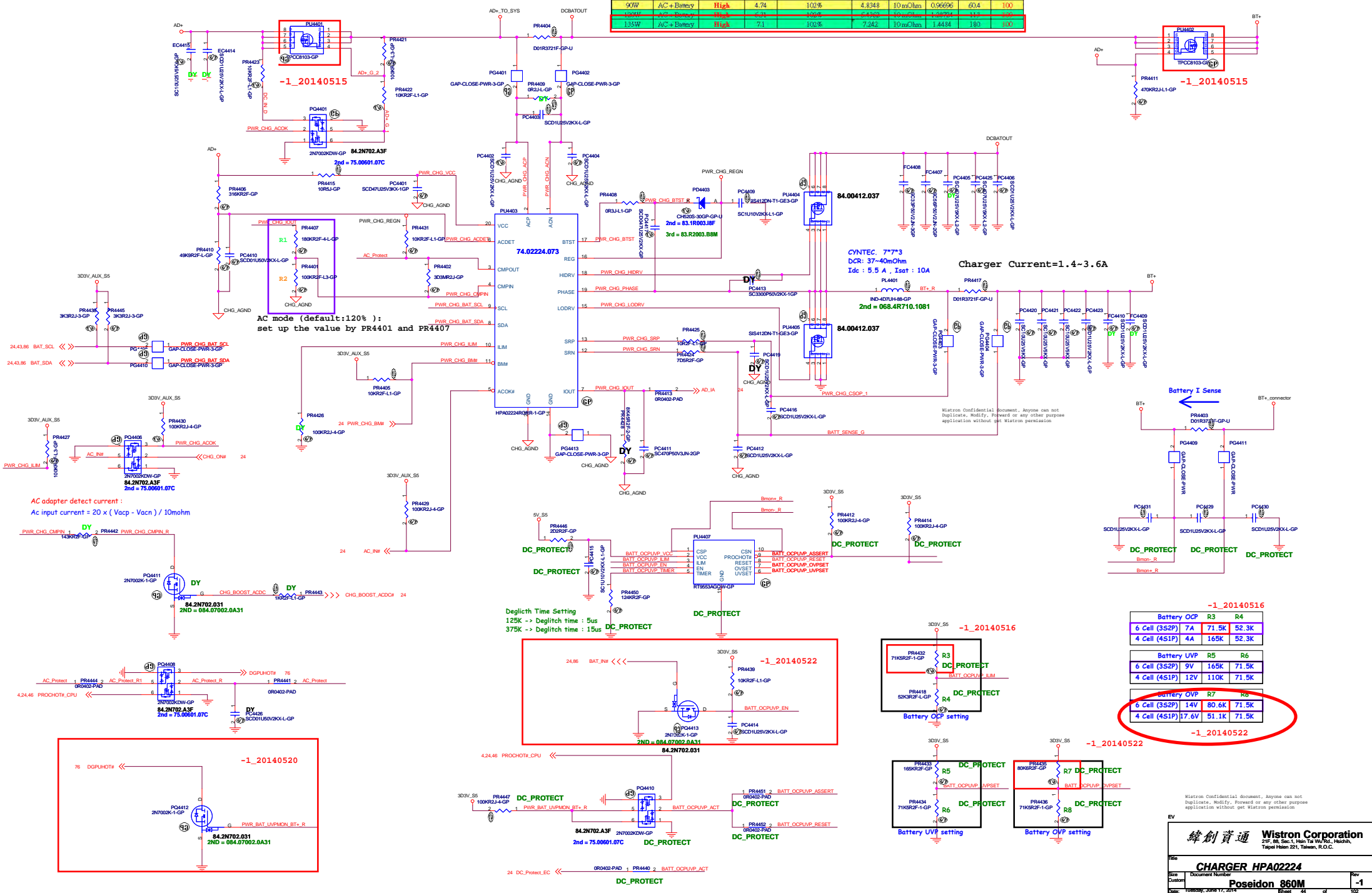
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Date: Tuesday, June 17, 2014

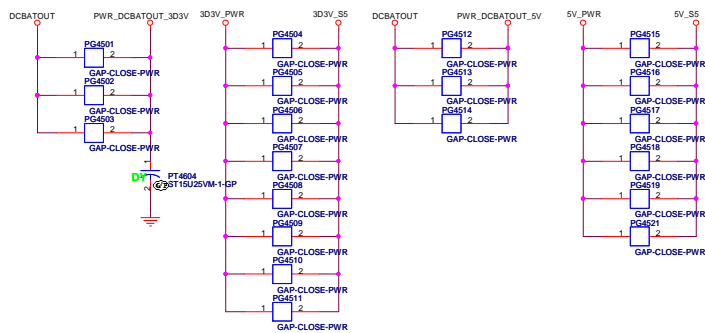
Sheet 42 of 102

SSID = Charger

						PR4404		R1	R2
	Stat	PM_SLP_A#	Adaptive Current	AC_Protect percent (85% ± 120%)	AC_Protect Current	Sense resistor	Current to Voltage	PR4407	PR4408
40W	AC + Battery	High	2.1	102%	2.142	21mΩ/2W	0.8563	61.4	509
45W	AC + Battery	High	2.37	102%	2.4174	20mΩ/2W	0.96696	40.2	100
65W	AC + Battery	High	3.42	102%	3.4884	19mΩ/2W	0.69763	16.2	100
90W	AC + Battery	High	4.74	102%	4.834	19mΩ/2W	0.96696	40.2	100
120W	AC + Battery	High	6.3	106%	6.5762	16mΩ/2W	1.21974	11.8	100
135W	AC + Battery	High	7.1	102%	7.242	16mΩ/2W	1.4484	18.0	100



SSID = PWR.Plane.Regulator_3p3v5v



High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

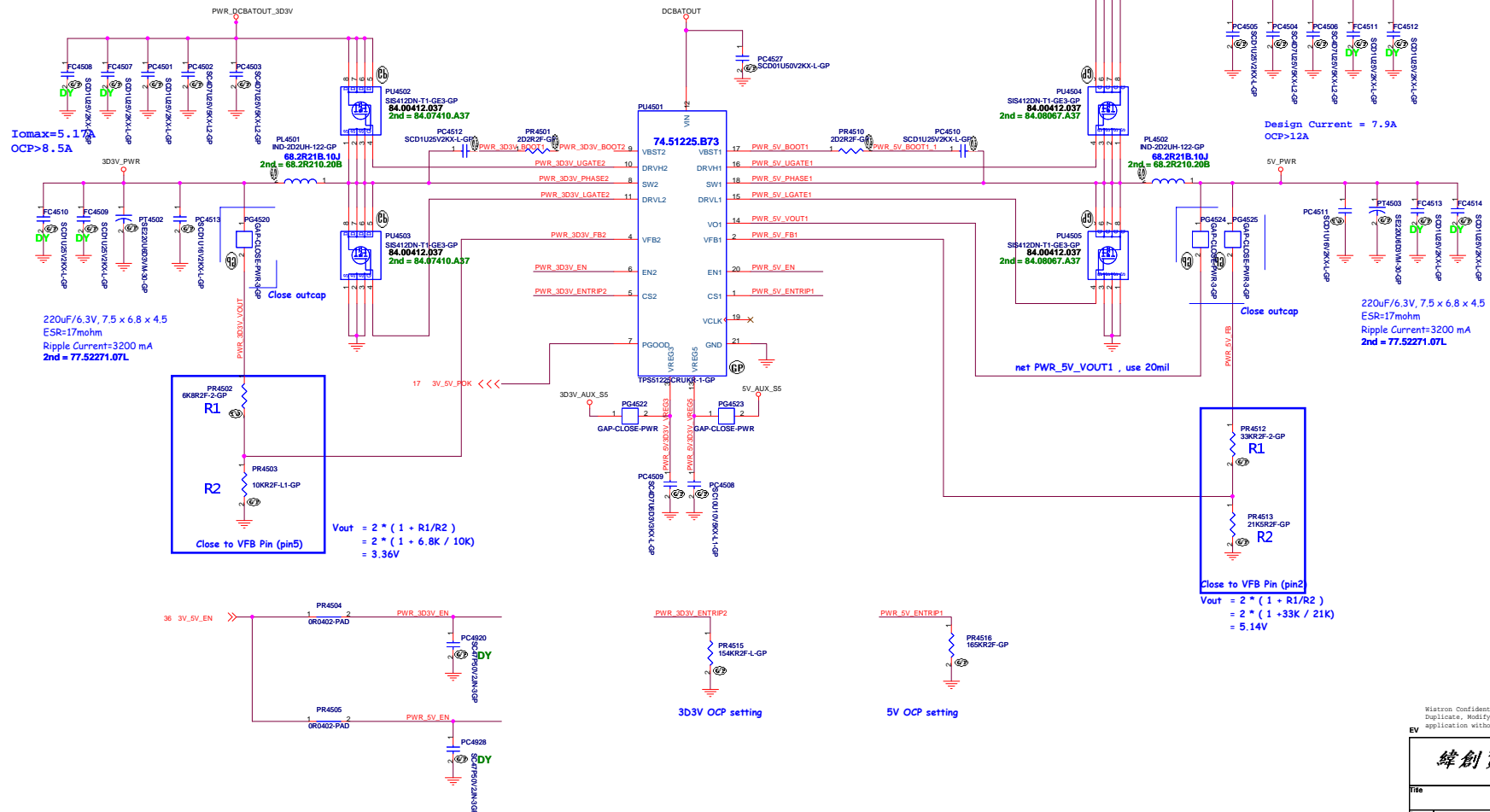
Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Choke
MagLayers. 7x7x3 , 2R2
Dcr : 18 ~ 20 mOhm
Idc : 8A Isat : 14 A

High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

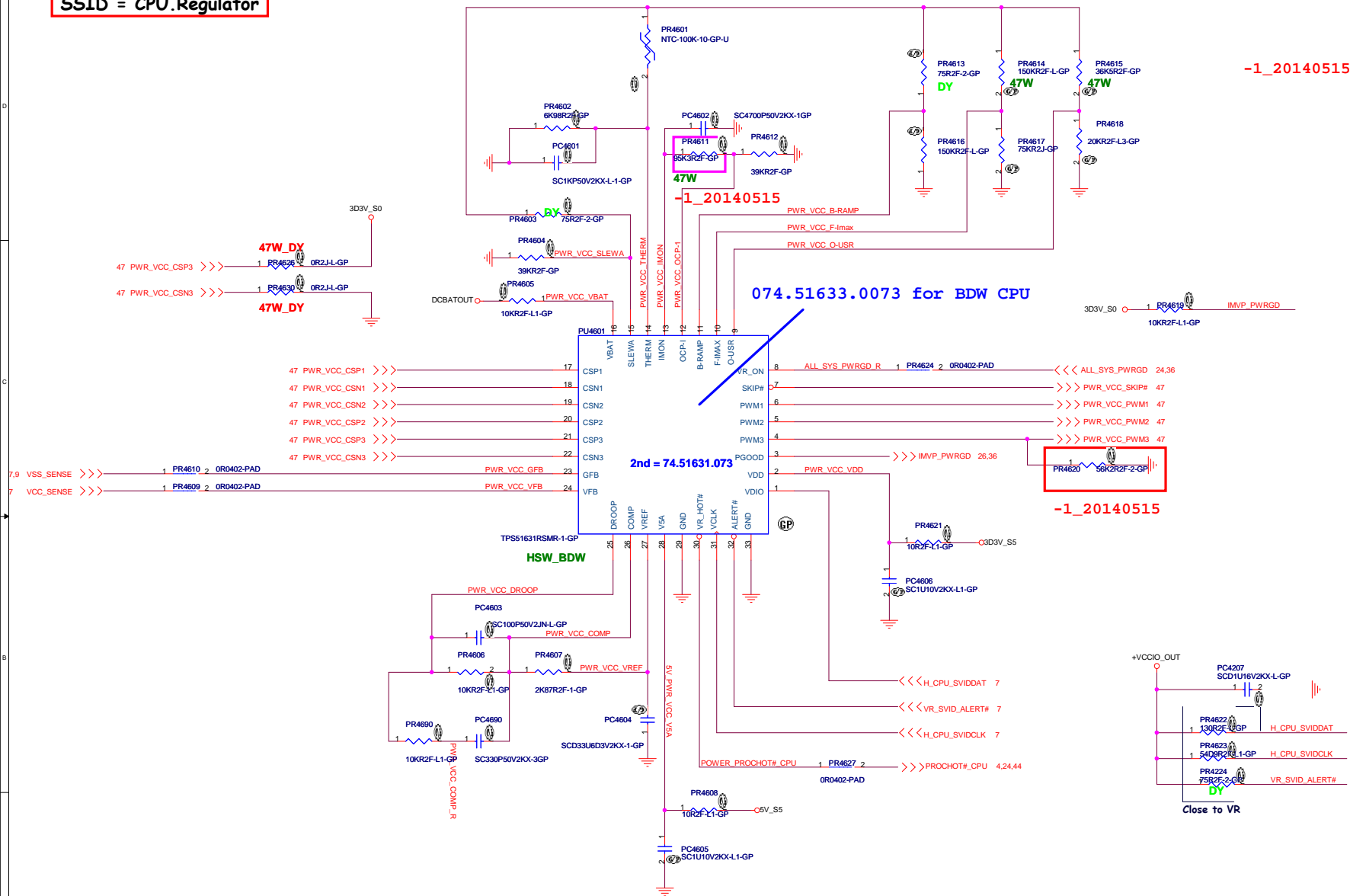
Choke
MagLayers. 7x7x3 , 2R2
Dcr : 18 ~ 20 mOhm
Idc : 8A Isat : 14 A



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File		TPS51225 5V/3D3V	
Size	Document Number	Rev	-1
Custom	Poseidon	860M	
Date	Tuesday, June 17, 2014	Sheet	45 of 102

SSID = CPU.Regulator

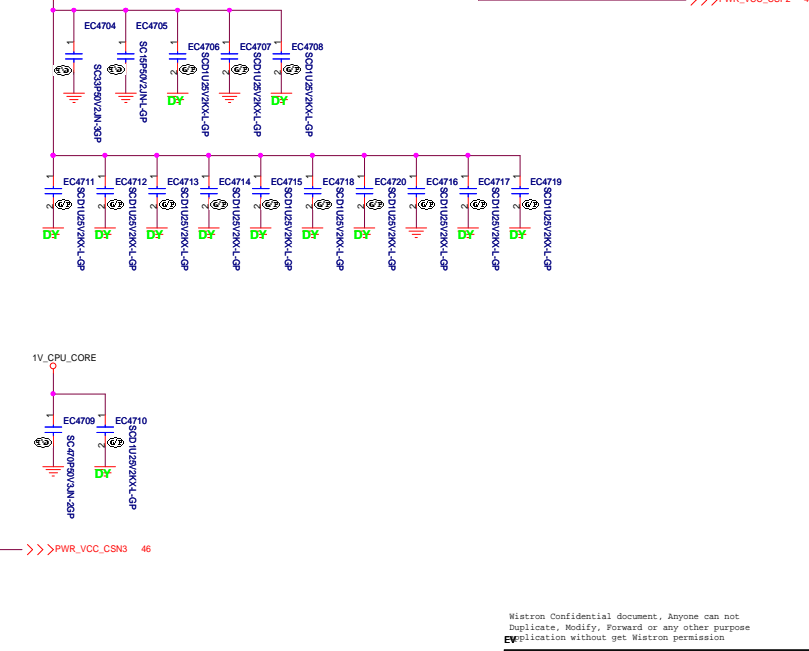
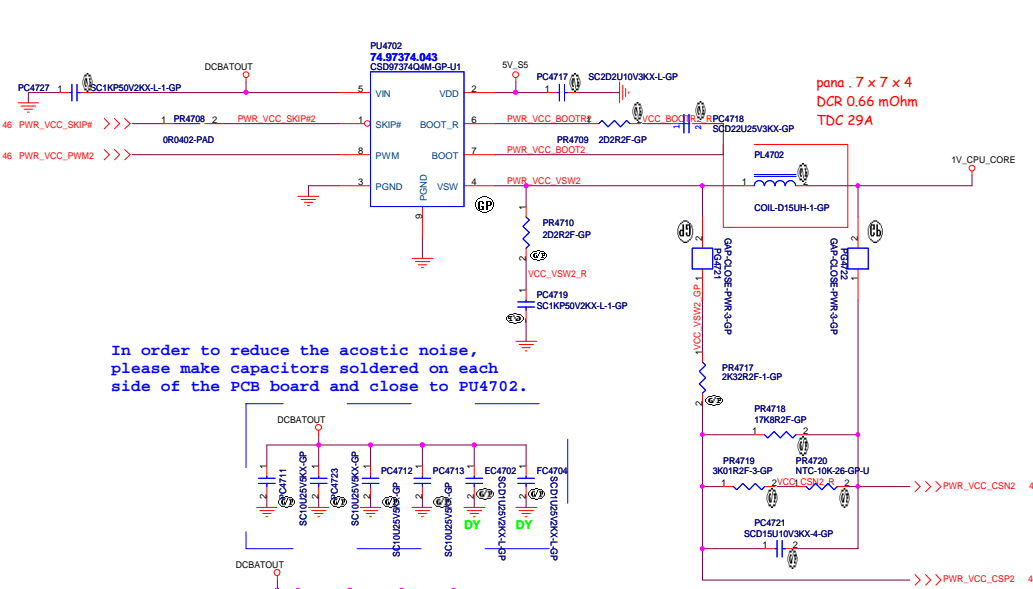


	47W
PC4602	4.7nF 78.47224.2FL
PR4611	95.3k 64.95325.6DL
PR4614	150k 64.15035.6DL
PR4617	75k 63.75334.1DL
PR4615	36.5k 64.36525.6DL
PR4618	20k 64.20025.6DL
PR4626	DY
PR4630	DY
PR4602	6.98k 64.69815.6DL
PR4607	2.87k 64.28715.6DL

EV application without get Wistron permission

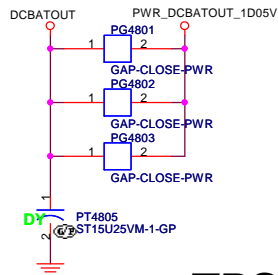
緯創資通 **Wistron Corporation**
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Title			
TPS51361 CPUCORE(1/2)			
Size	Document Number	Rev	
Custom	Poseidon 840M	-1	
Date:	Tuesday, June 17, 2014	Sheet 46 of	102



緯創資通 **Wistron Corporation**
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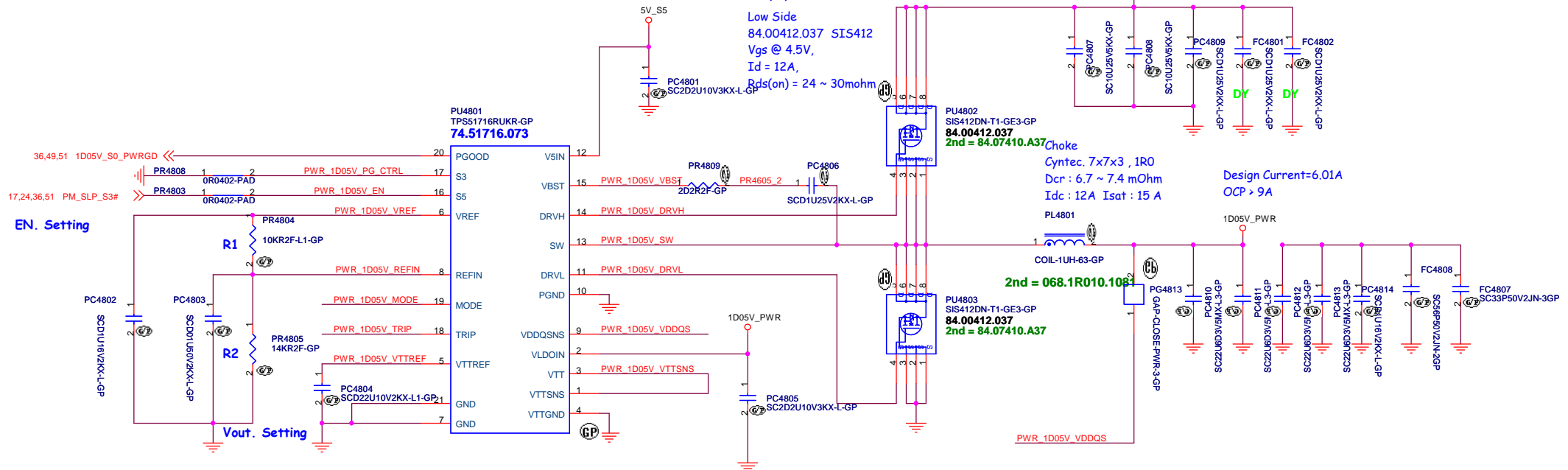
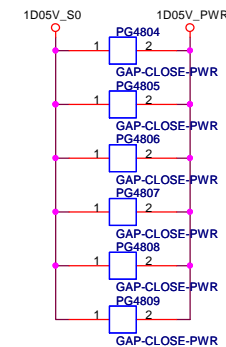
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TPS51716 for 1D05V

High Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm

Low Side
84.00412.037 SIS412
Vgs @ 4.5V,
Id = 12A,
Rds(on) = 24 ~ 30mohm



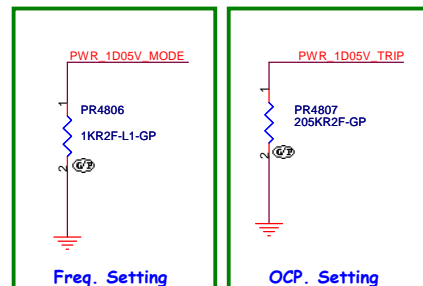
EN. Setting

Vout. Setting

MODE

PR5006	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



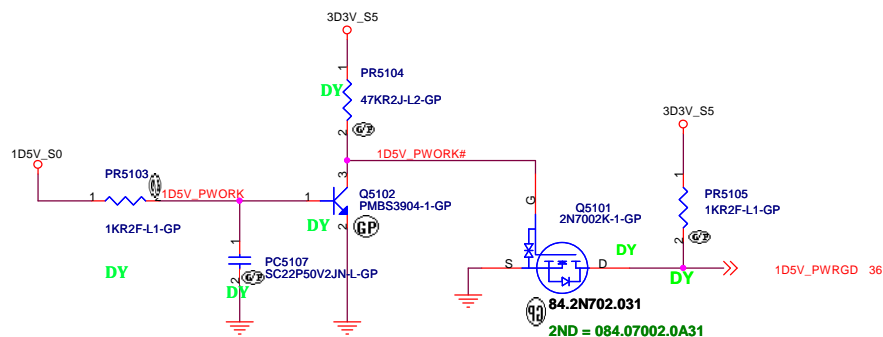
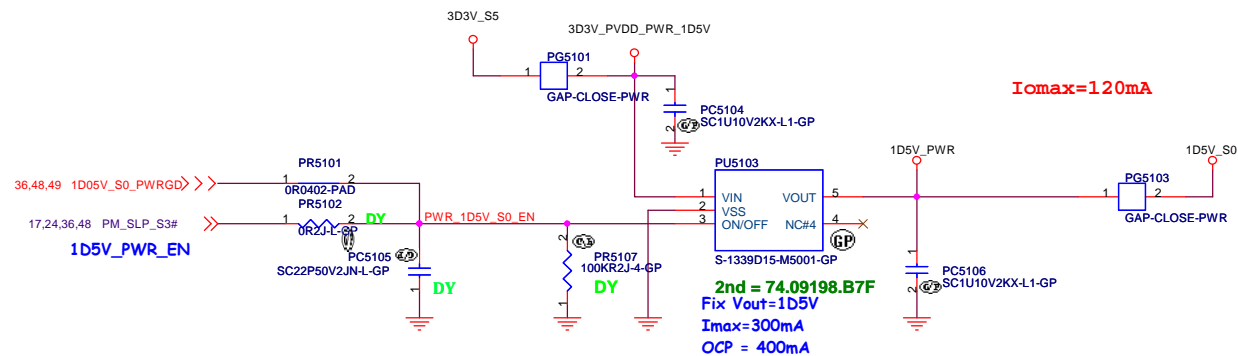
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Title DC to DC 1D05V(TPS51716)	
Size A3	Document Number Poseidon 860M
Date: Wednesday, June 18, 2014	Sheet 48 of 102

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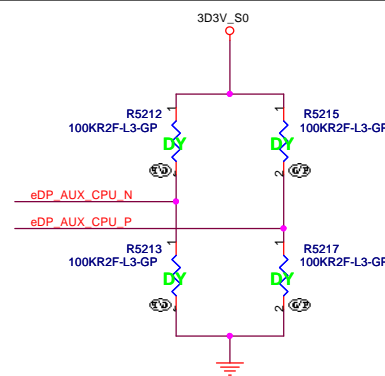
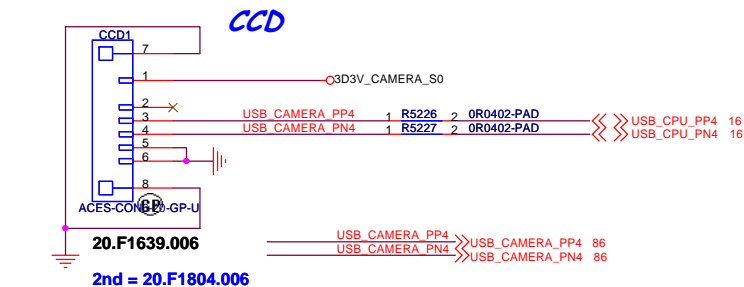
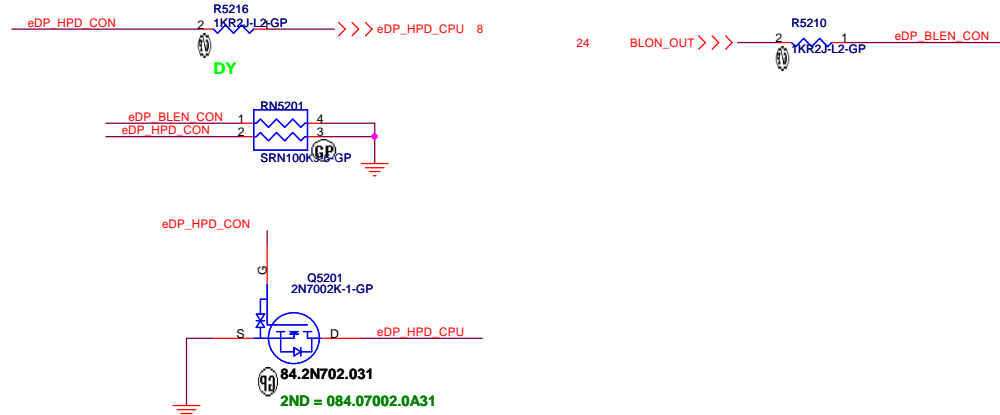
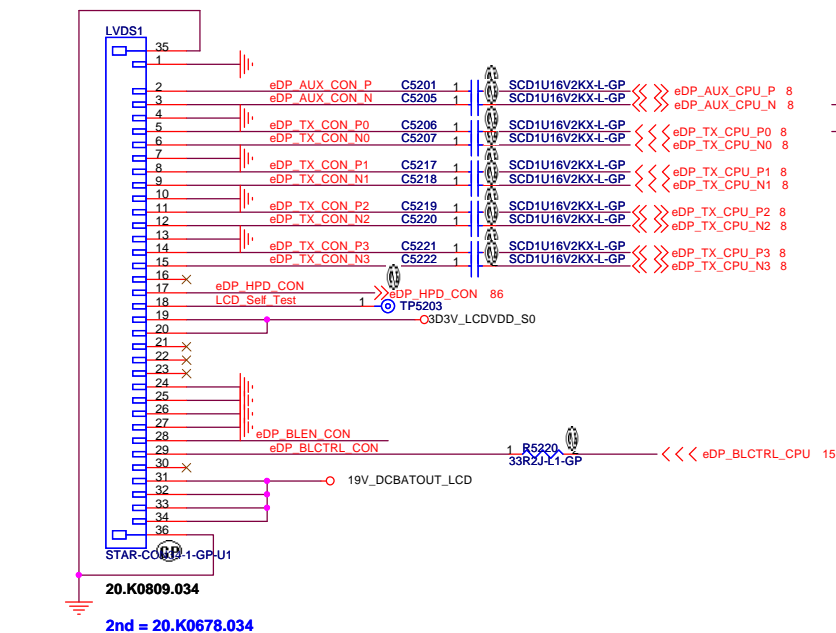
TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V



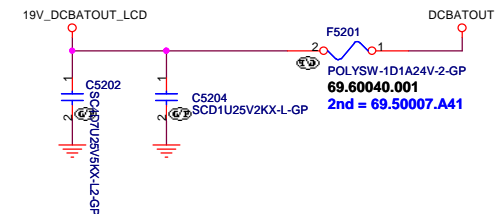
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Title 1D5V_S0 TLV70215		
Size A3	Document Number Poseidon 860M	Rev -1
Date: Tuesday, June 17, 2014	Sheet 51	of 102

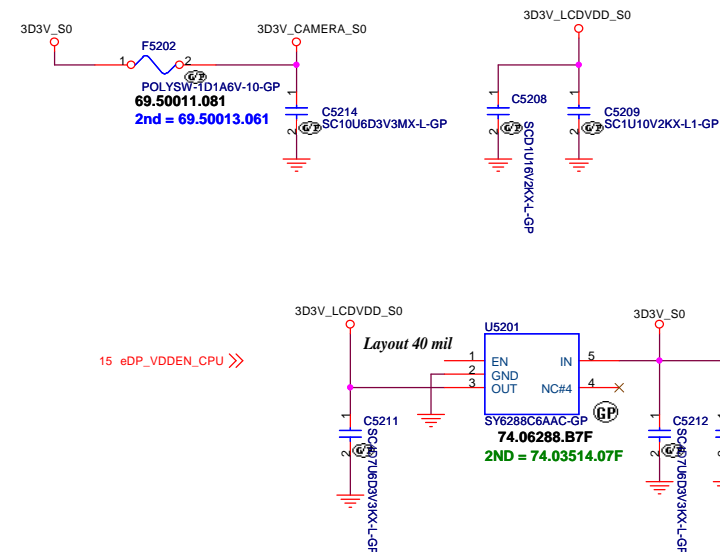
SSID = VIDEO



INVERTER POWER



Camera Power



eDP_AUX_CON_P >>> eDP_AUX_CON_P 86

eDP_AUX_CON_N >>> eDP_AUX_CON_N 86

eDP_TX_CON_P0 >>> eDP_TX_CON_P0 86

eDP_TX_CON_N0 >>> eDP_TX_CON_N0 86

eDP_TX_CON_P1 >>> eDP_TX_CON_P1 86

eDP_TX_CON_N1 >>> eDP_TX_CON_N1 86

eDP_TX_CON_P2 >>> eDP_TX_CON_P2 86

eDP_TX_CON_N2 >>> eDP_TX_CON_N2 86

eDP_TX_CON_P3 >>> eDP_TX_CON_P3 86

eDP_TX_CON_N3 >>> eDP_TX_CON_N3 86

>>> eDP_HPDCON 86

>>> eDP_BLENCON 86

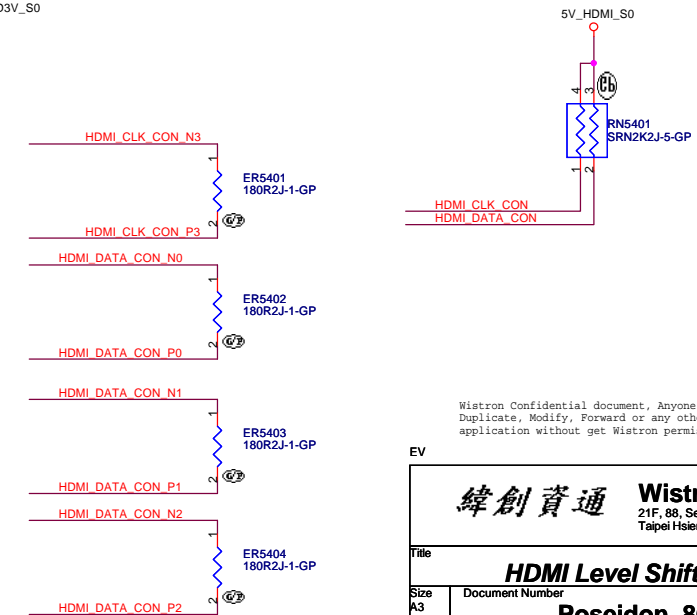
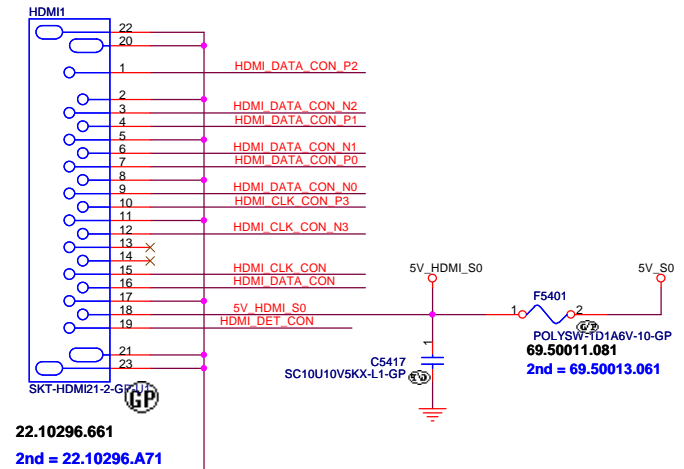
>>> eDP_BLCCTRL_CON 86

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Title LCD Connector		
Size A3	Document Number Poseidon 860M	Rev -1
Date: Tuesday, June 17, 2014	Sheet 52	of 102

HDMI Level Shifter & CONNECTOR

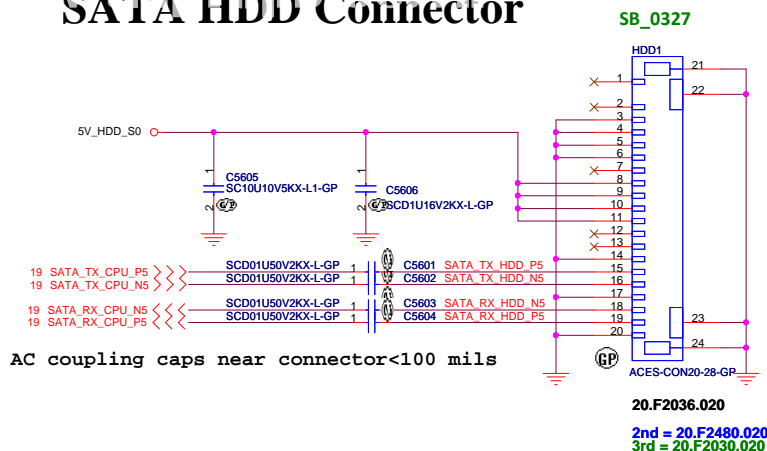
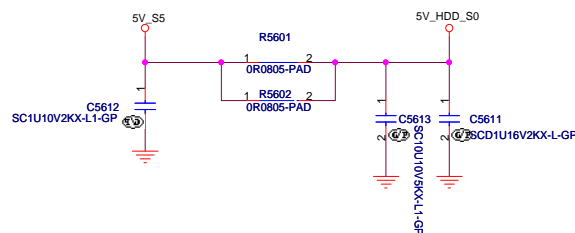


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Taipei Hsien 221, Taiwan, R.O.C.

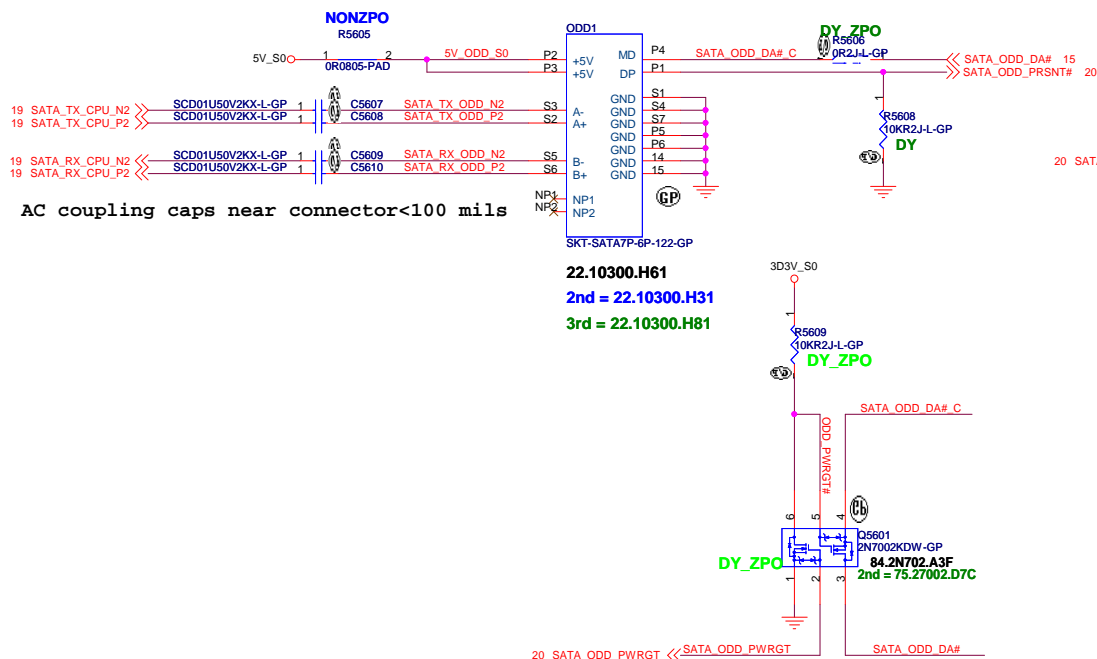
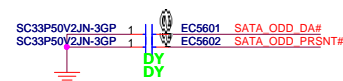
Title			
HDMI Level Shifter/Connector			
Size A3	Document Number		Rev
	Poseidon 860M		-1
Date:	tuesday, June 17, 2014	Sheet 54 of	102

SSID = SATA

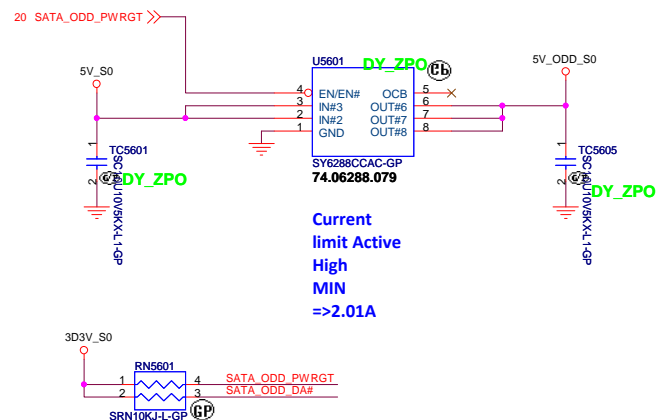
SATA HDD Connector



ODD Connector



SATA Zero Power ODD



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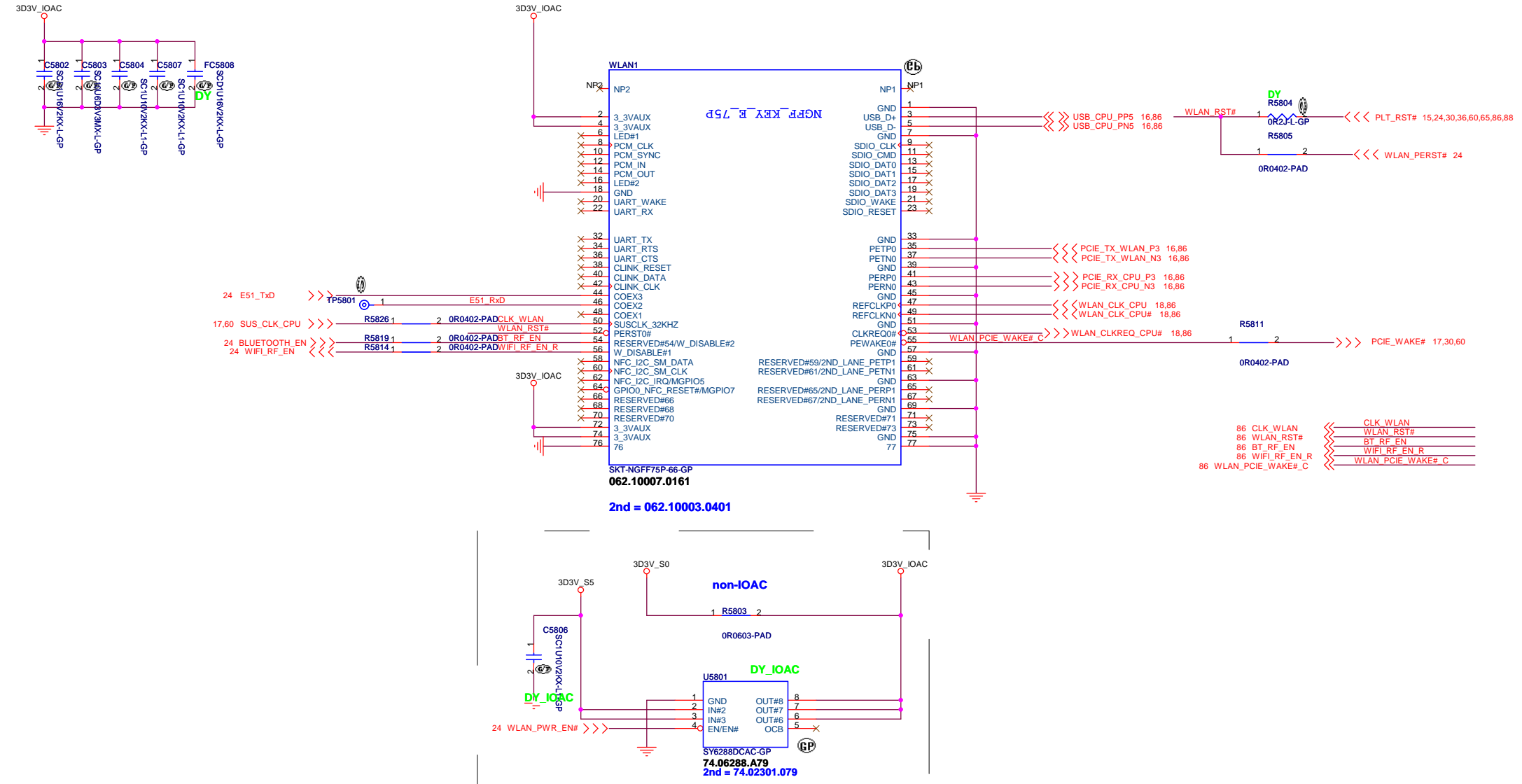
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Title			
HDD / ODD / NGFF SSD			
Size	Document Number	Rev	
Custom	Poseidon 860M	-1	
Date:	Tuesday, June 17, 2014	Sheet	56 of 102

SSID = Wireless

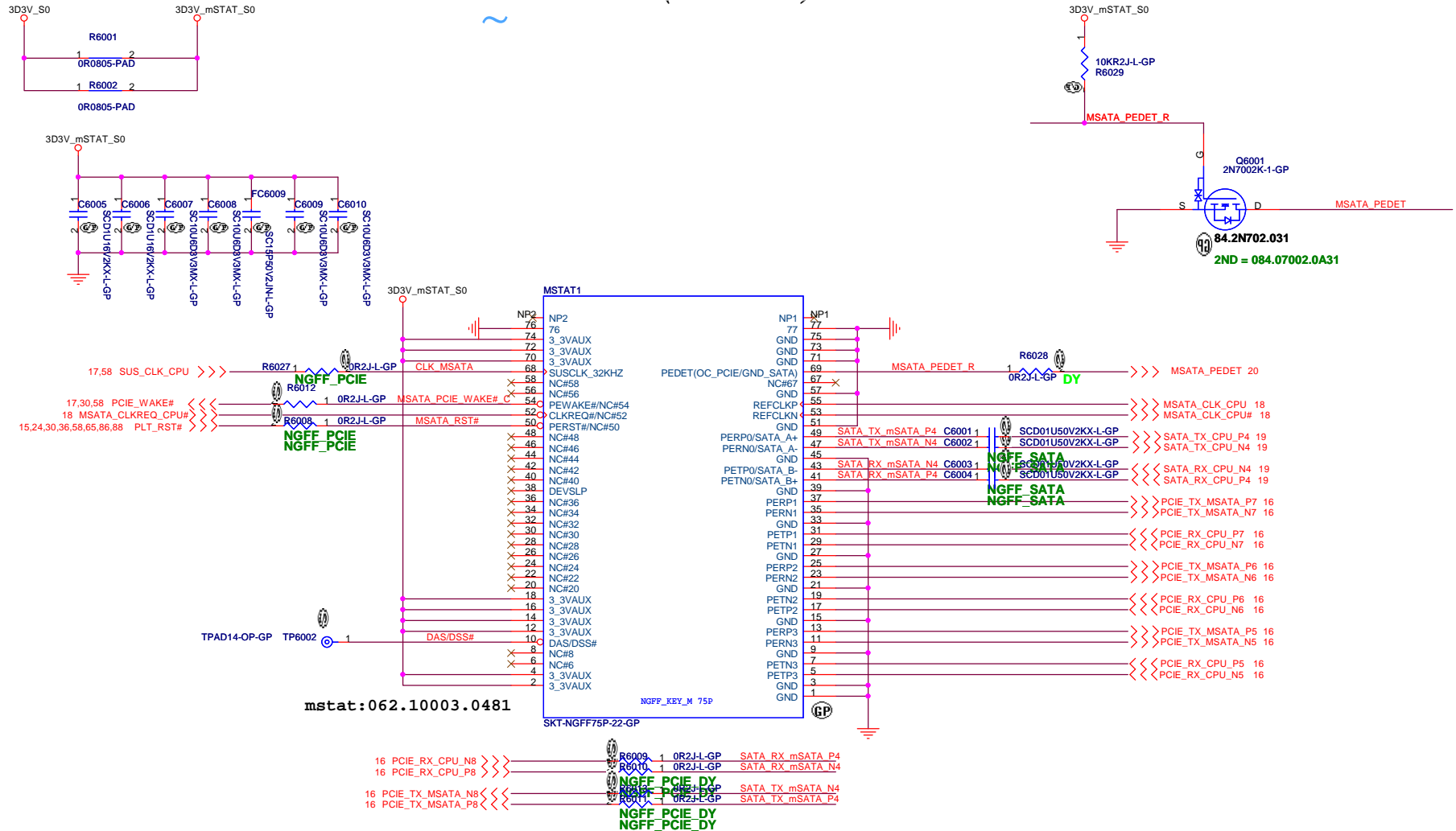
Mini Card Connector(802.11a/b/g/n)



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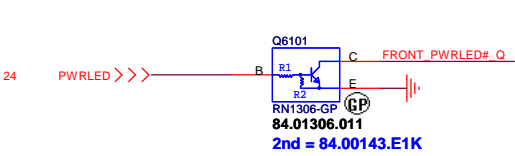
SSID = mSATA

Mini Card Connector(mSATA)

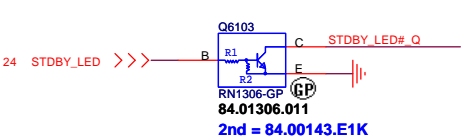


SSID = User.Interface

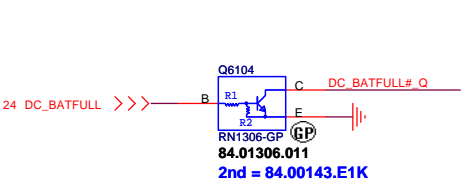
Power button LED



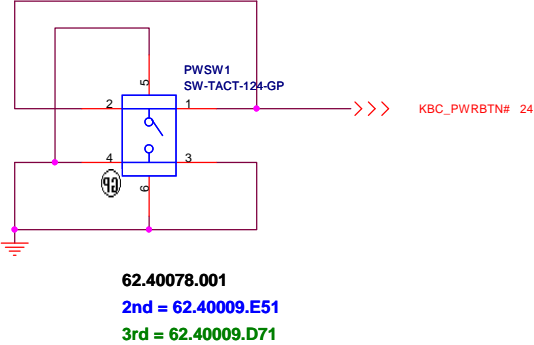
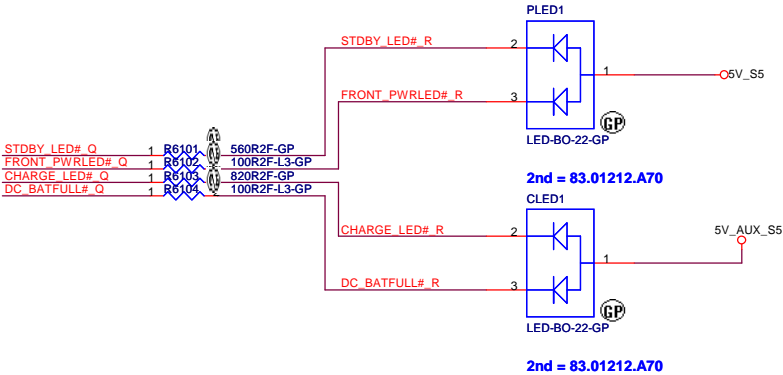
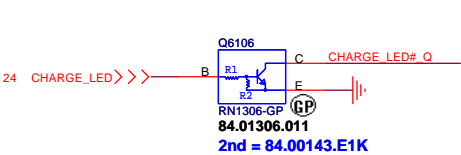
Power STDBY_LED



Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)

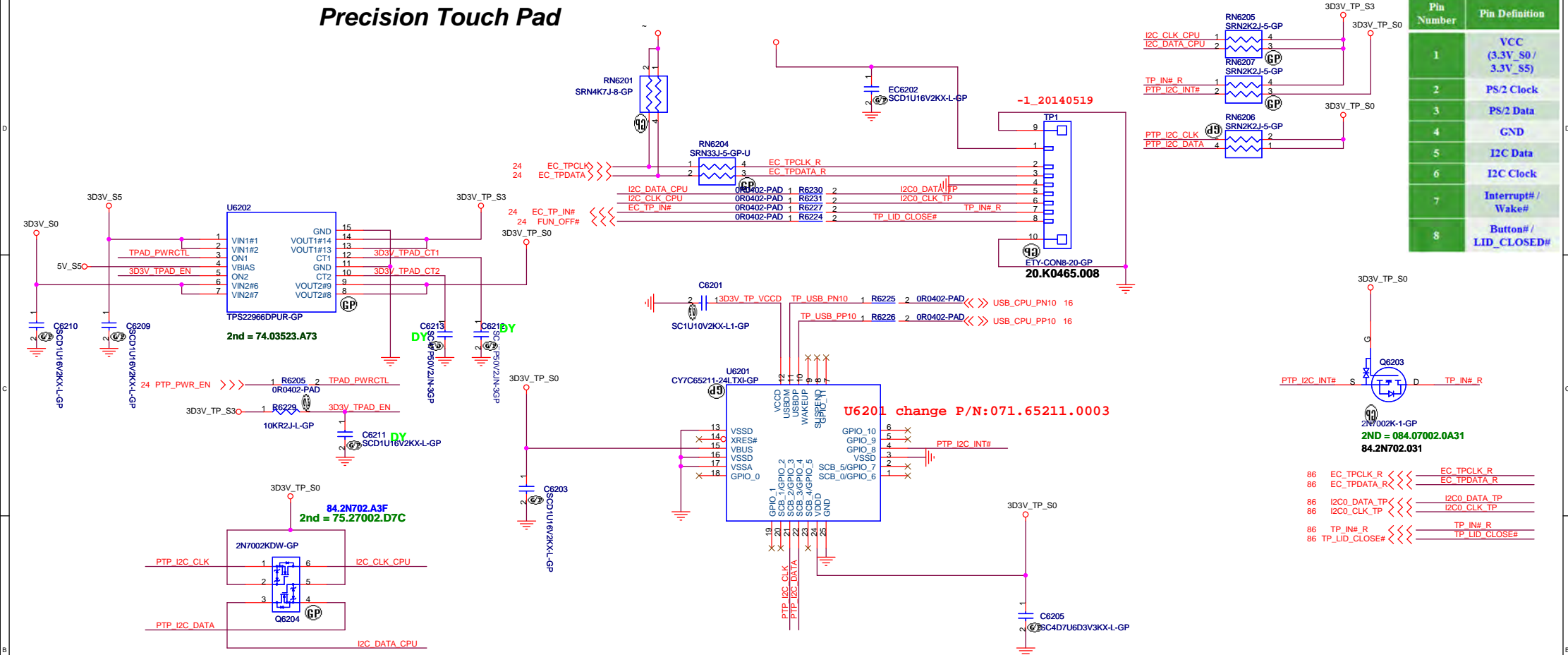


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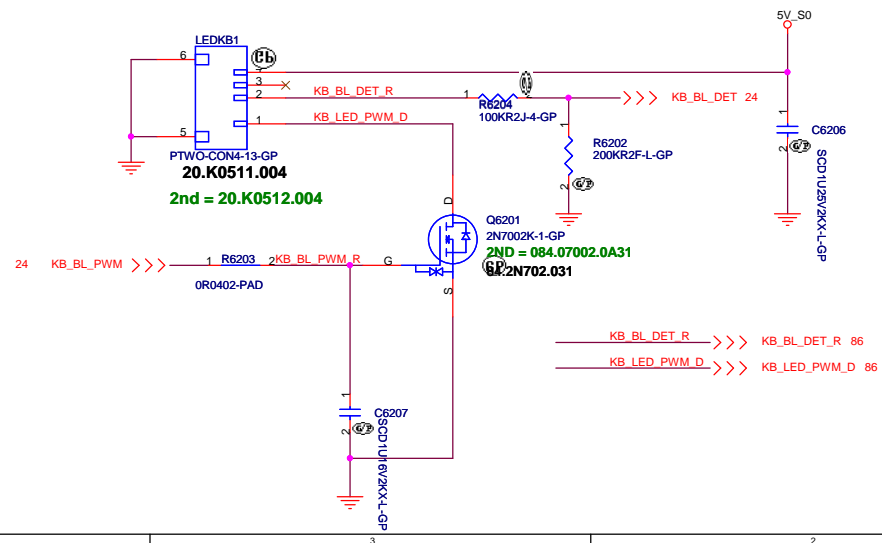
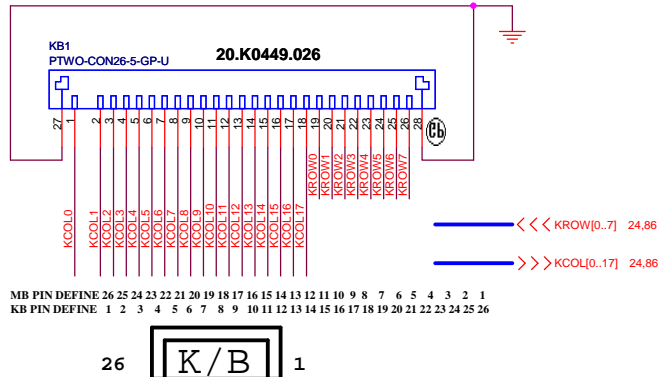
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Title		LED Bard/Power Button	
Size	Document Number	Rev	
A3	Poseidon 860M	-1	
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Precision Touch Pad



Internal KeyBoard Connector

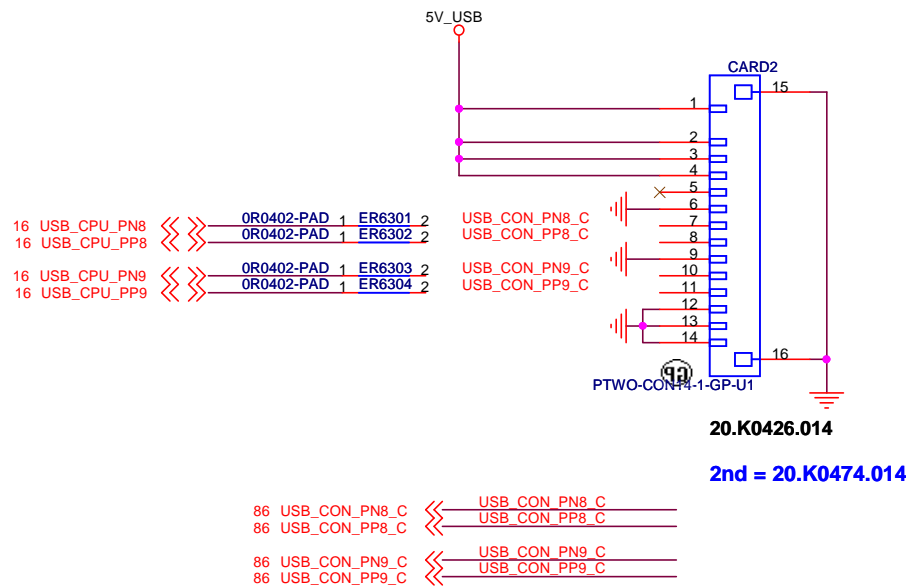
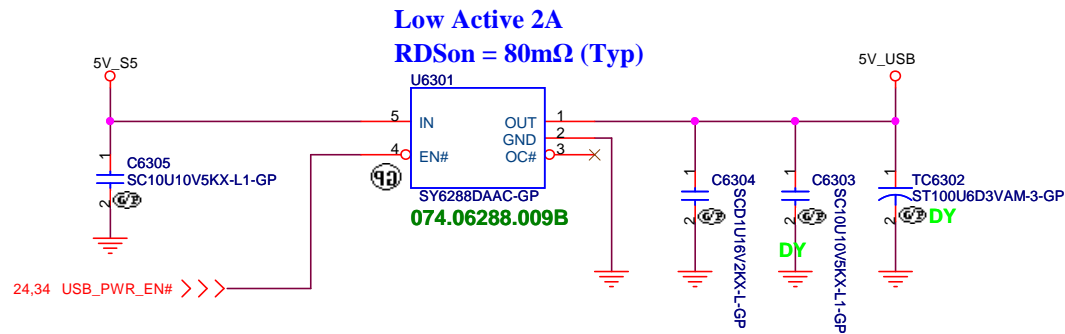


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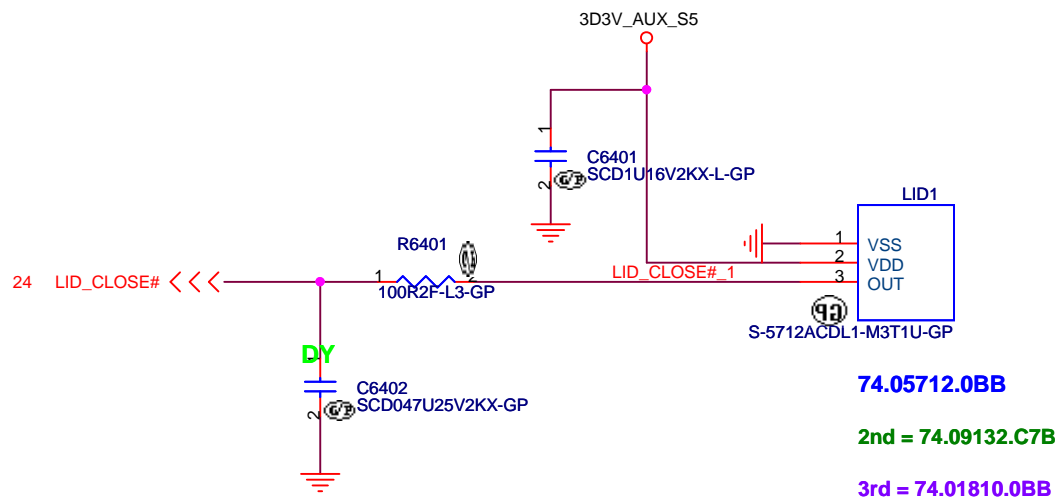
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Key Board/Touch Pad			
Size	Document Number	Rev	
Custom	Poseidon 860M	-1	
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<p>Title IO Board Connector</p>	
<p>Size Custom</p>	<p>Document Number Poseidon 860M</p>
<p>Date: Tuesday, June 17, 2014</p>	<p>Rev -1</p>
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Title

Hall Sensor

Size
A4

Document Number

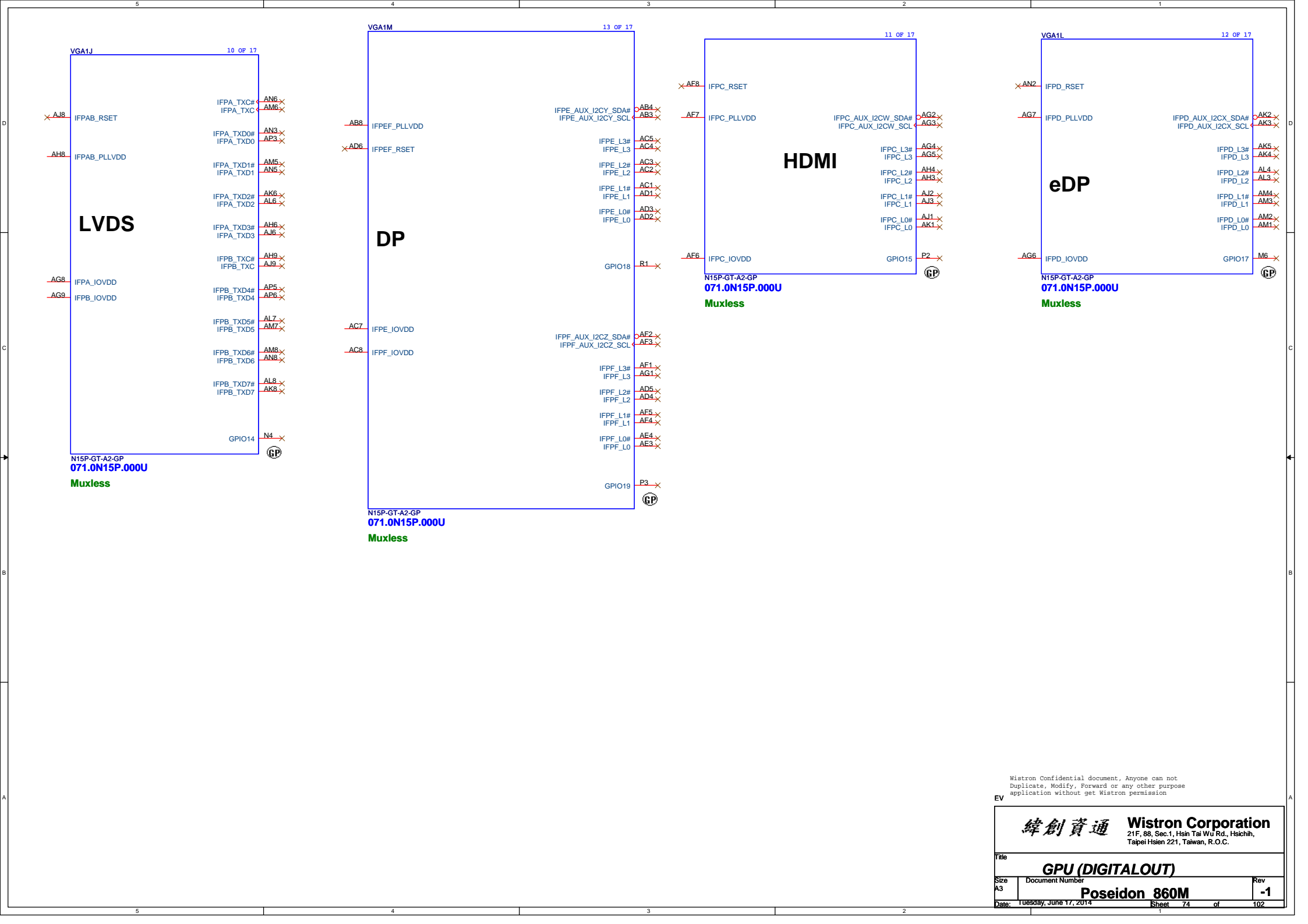
Poseidon 860M

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Title		
GPU (DIGITALOUT)		
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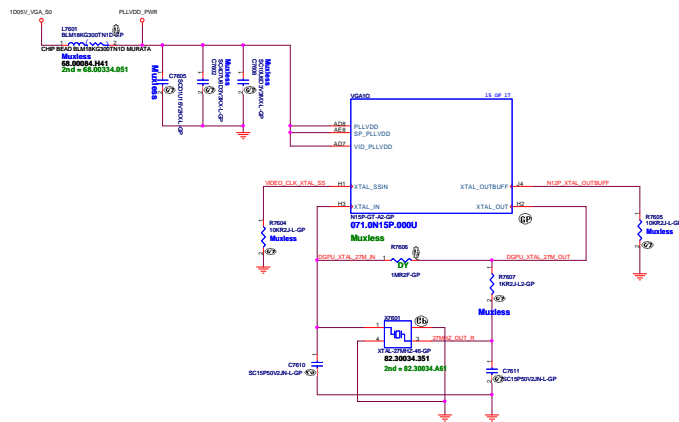
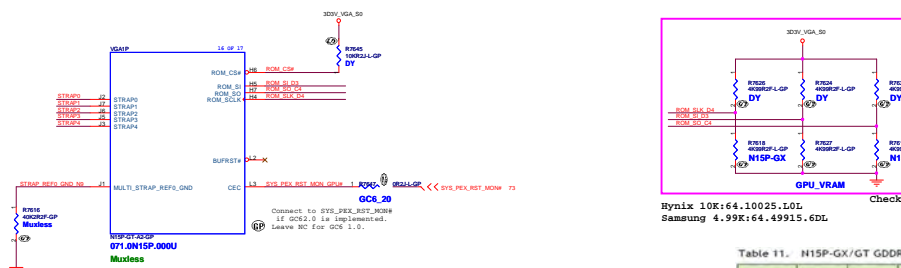
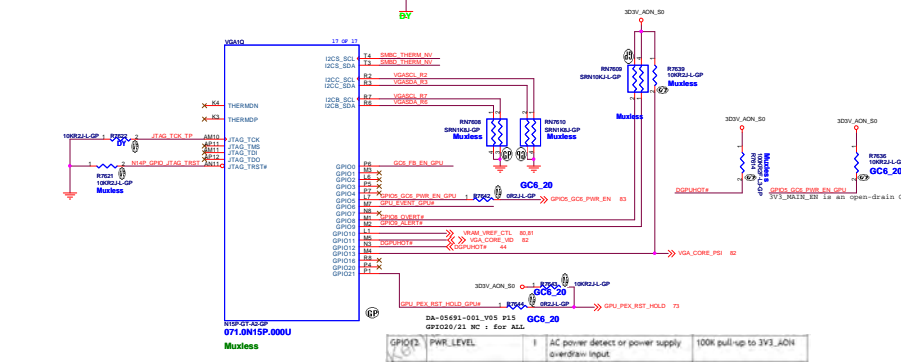
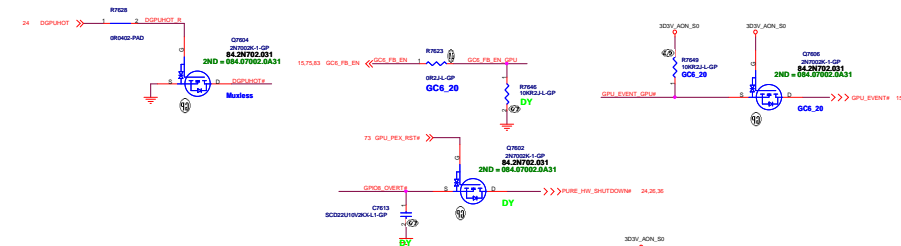
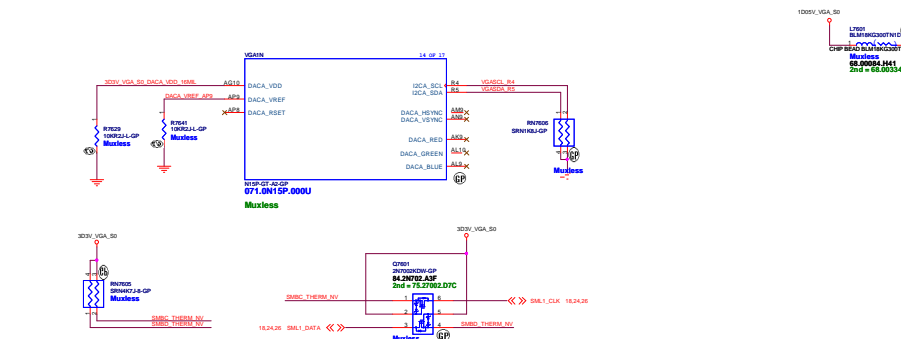


Table 2. Memory Configurations for Testing

Products	Type	VRAM Voltage	Vendor	Qty	Memory Bus Width	Density	Speed Bin (MHz)	Part Number
H155-GX	DDR3	1.5V	Hynix	8	128 bits	256MX16	1000	H5TC4G63AFR-11C
H15P-GT	DDR3	1.5V	Hynix	8	128 bits	256MX16	1000	H5TC4G63AFR-11C
H15P-GX	DDR5	1.35V	Hynix	8	128 bits	256MX16	2500	H5GC4H24NFR-T2C
H15P-GX	DDR5	1.35V	Hynix	8	128 bits	256MX16	2500	H5GC4H24NFR-T2C

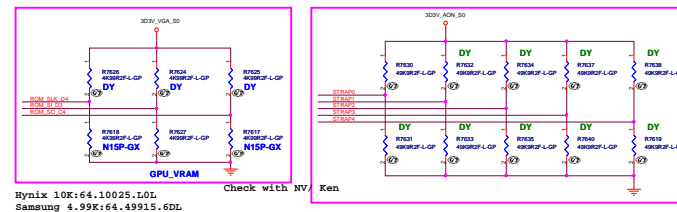
Table 15.3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bin 3	Logical Strapping Bin 2	Logical Strapping Bin 1	Logical Strapping Bin 0
ROM_SCLK	S0R3_EXPOSED	S0R2_EXPOSED	S0R1_EXPOSED	S0R0_EXPOSED
ROM_SI	RAM_CFG[0]	RAM_CFG[1]	RAM_CFG[2]	RAM_CFG[3]
ROM_SO	DEVID_SEL	PCIE_CFG	SWB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to V33_A0H and pull-down to GND and stuff S0M0 pull-up.			
STRAP1	Keep foot print for pull-up to V33_A0H and pull-down to GND for forward compatibility.			
STRAP2				
STRAP3				
STRAP4				

Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD13	Pull-down to GND
4.99k	1000	0000
10.0k	1001	0001
15.0k	1010	0010
20.0k	1011	0011
24.9k	1100	0100
30.1k	1101	0101
34.8k	1110	0110
45.3k	1111	0111

4.99Kohm 64.49915.6DL
10Kohm 64.10025.L0L
15Kohm 64.15025.6DL
20Kohm 64.20025.6DL
24.9Kohm 64.24925.6DL
30.1Kohm 64.30125.6DL
34.8Kohm 64.34825.6DL
45Kohm 64.45325.6DL



Hynix 10K:64.10025.L0L
Samsung 4.99K:64.49915.6DL

Table 11. N15P-GX/GT GDDR5 Recommended Memories

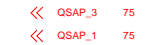
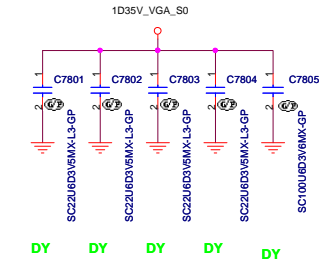
Memory Type	FBVDD/FBVDQ	Memory Density	Vendor	Manufacturer Part Number	Die Size	Strap	Memory Speed (MHz)
GDDR5	1.35V/1.35V	128MX16	Samsung	K4G20325FD-FC03	D-die	0x0	2500
			Hynix	H5GC2H24BFR-T2C	B-die	0x1	2500
			Microtron	EDV2032B8G-6A-F	B-die	0x0	2500
		256MX16	Hynix	H5GC4H24NFR-T2C	D-die	0x2	2500
			Samsung	K4G41325F-C4C03	C-die	0x3	2500
			Microtron	EPH4032B8G-60-F	A-die	0x4	2500

72.05224.A0U

72.20325.B0U

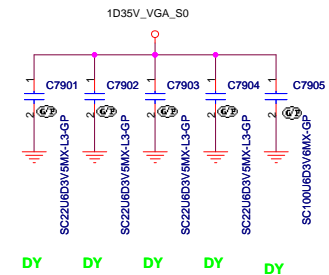
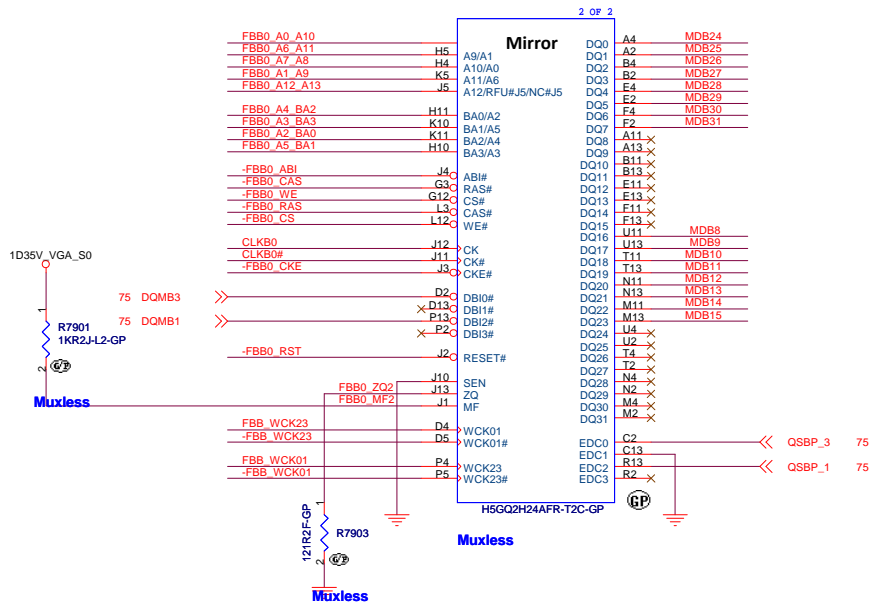
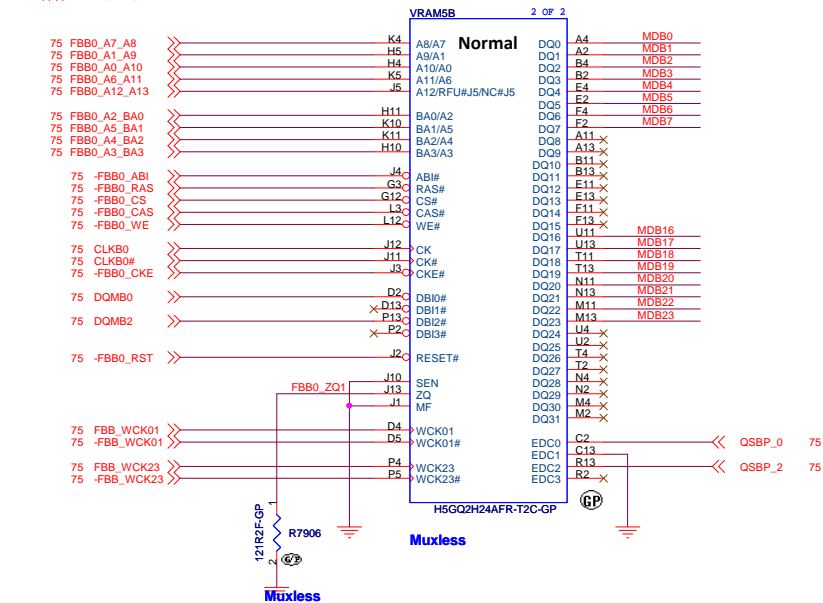
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LOGIC

LOGIC



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Title			
VRAM A			
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VRAM B

Size Custom

Document Number

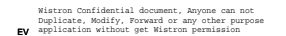
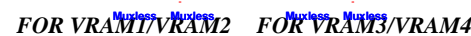
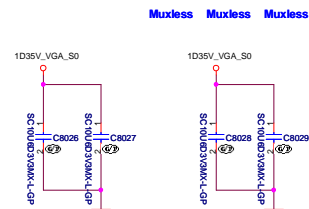
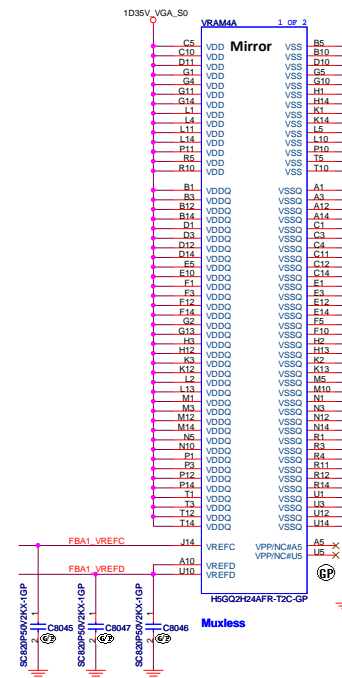
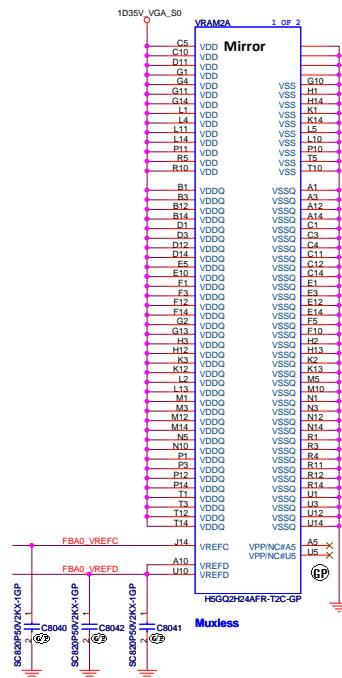
Rev

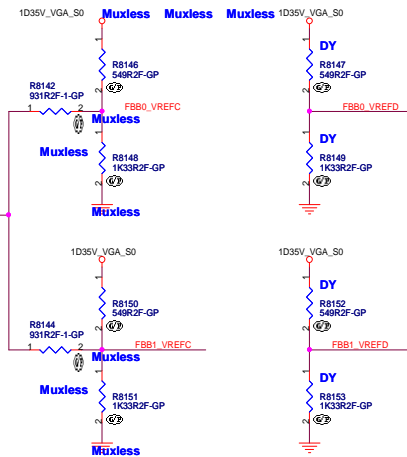
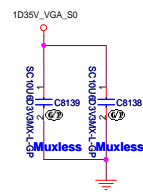
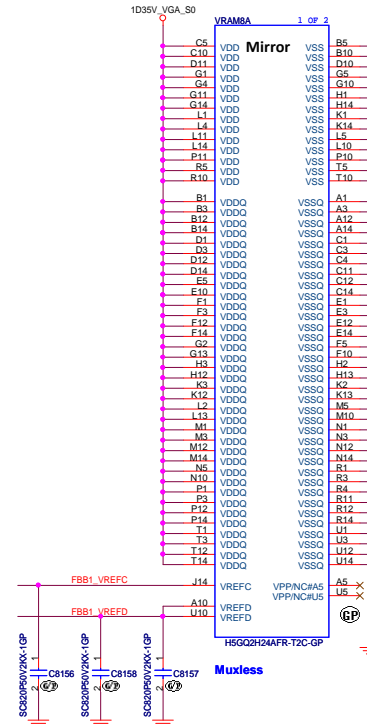
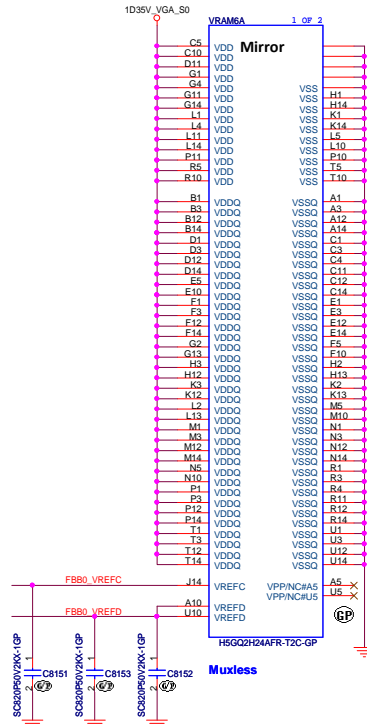
Poseidon 860M

-1

Date: Tuesday, June 17, 2014

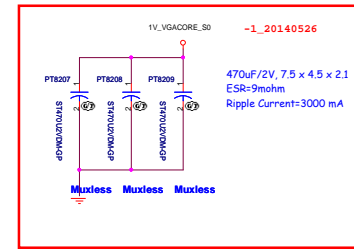
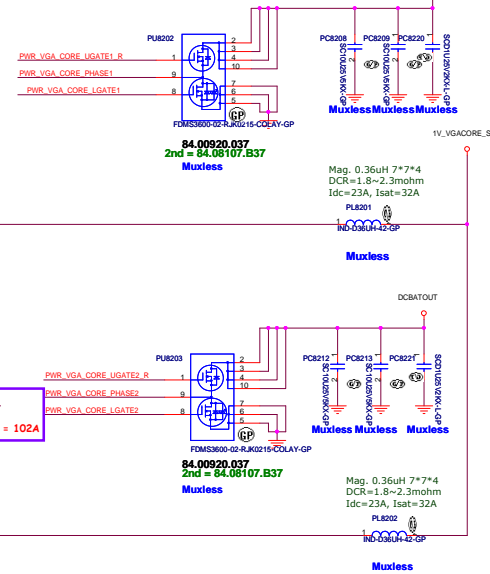
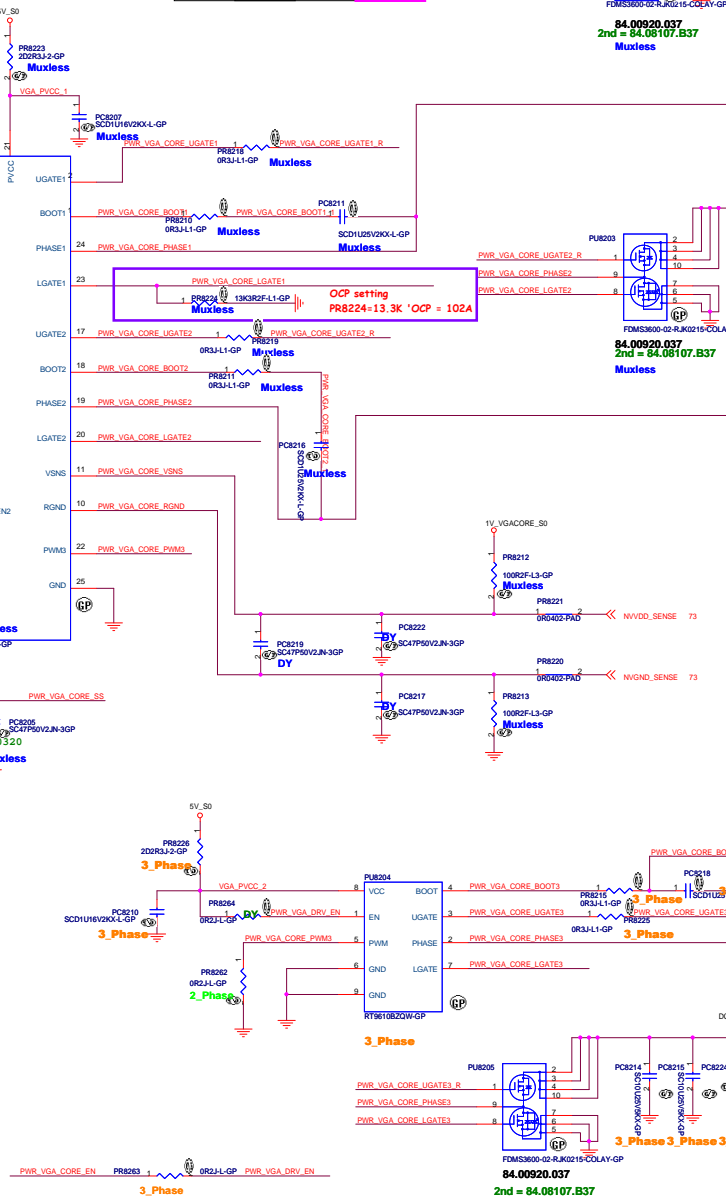
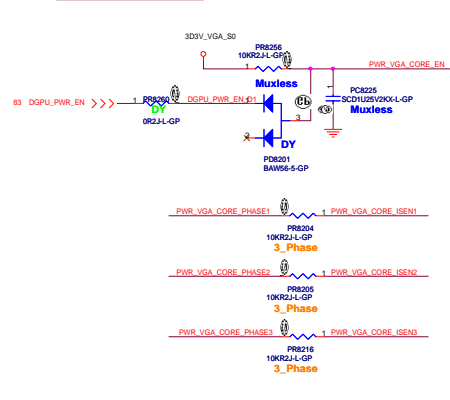
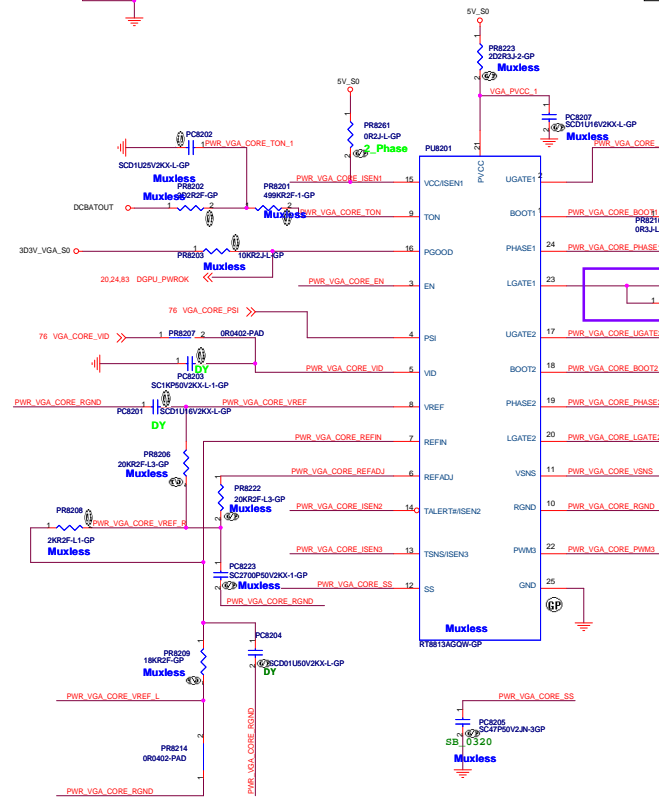
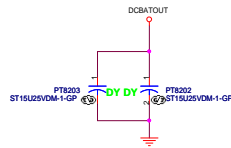
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Title			
VGA POWER B			
Size	Document Number	Rev	
Custom	Poseidon 860M	-1	
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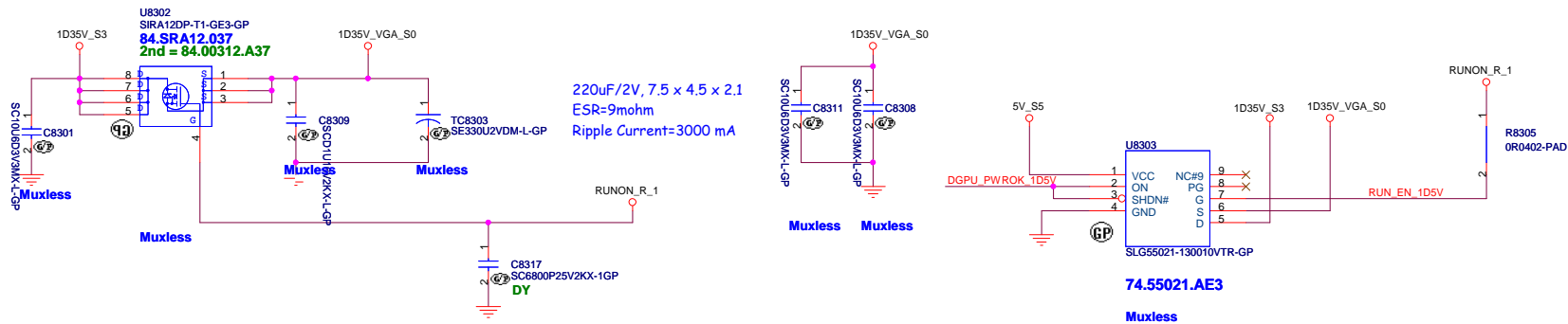
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EDP-Cont.	33.5 A	35 A	43 A
EDP-Peak	51.5 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF



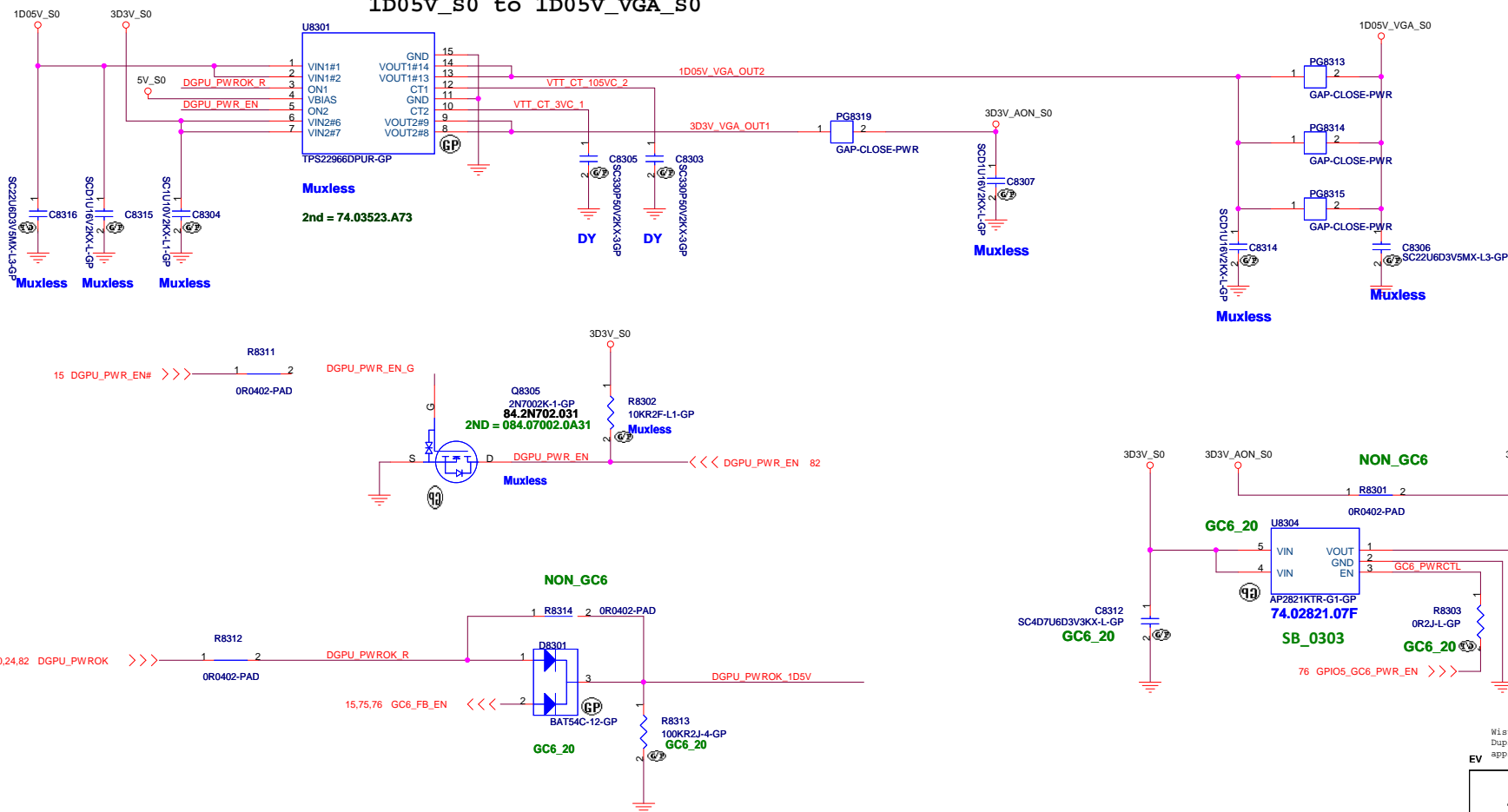
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84.00916.037
2nd:84.03660.037
PU8202/PU8203/PU8205

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TPS22966 for VGA_1D35V(For VRAM GDDR5)



```
3D3V_S0    to 3D3V_VGA_S0
1D05V_S0   to 1D05V_VGA_S0
```

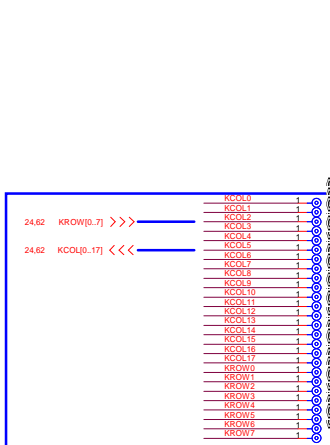
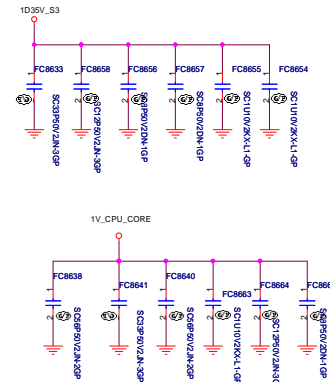
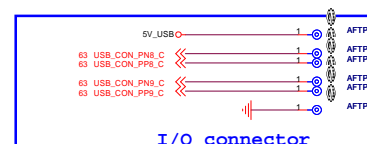
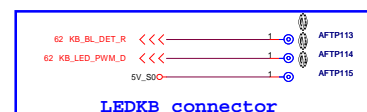
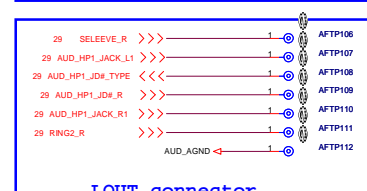
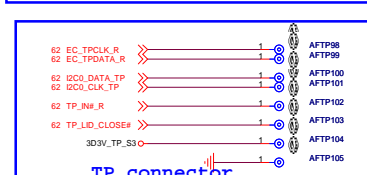
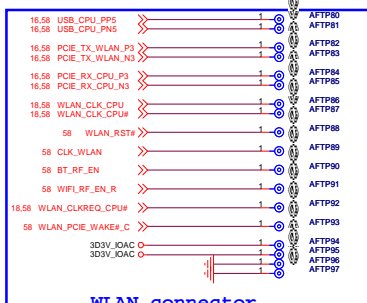
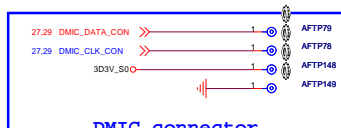
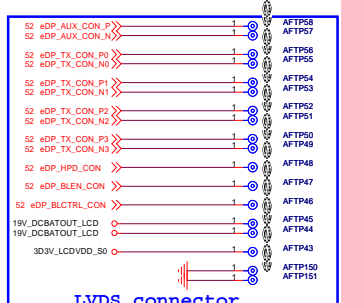
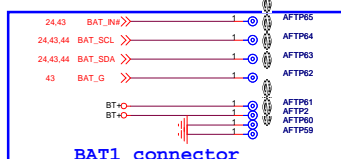
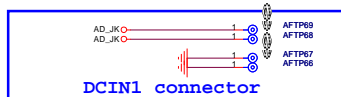
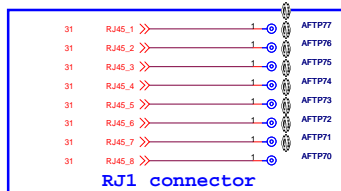
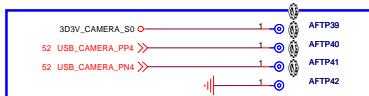
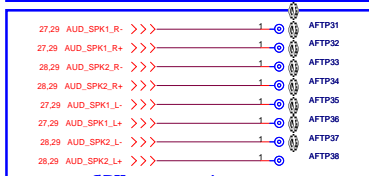
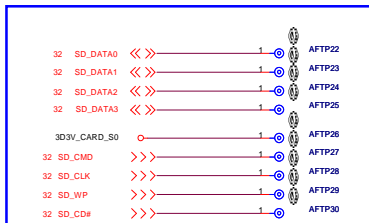
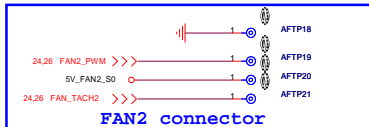
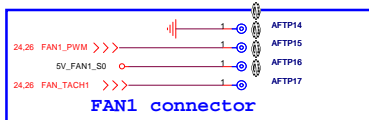
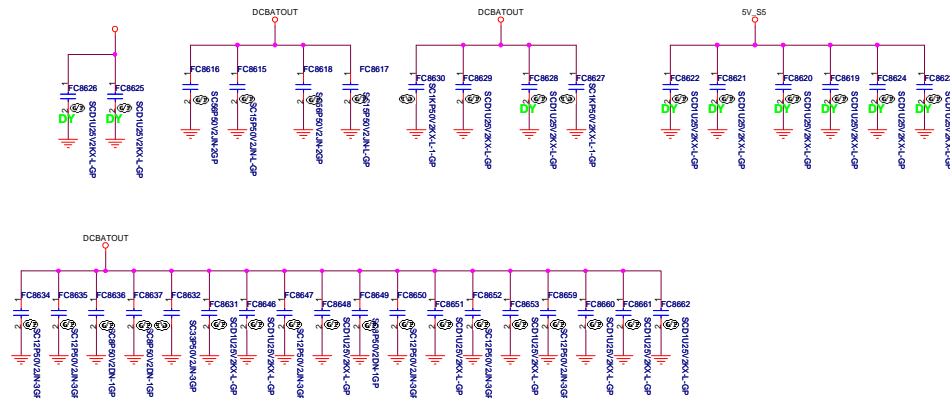
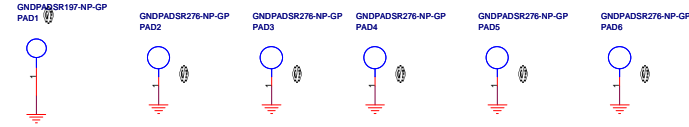


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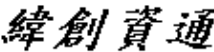
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Size	Document Number	Rev	
Custom	Poseidon 860M	-1	
Date:	Tuesday, June 17, 2014	Sheet 83 of	102



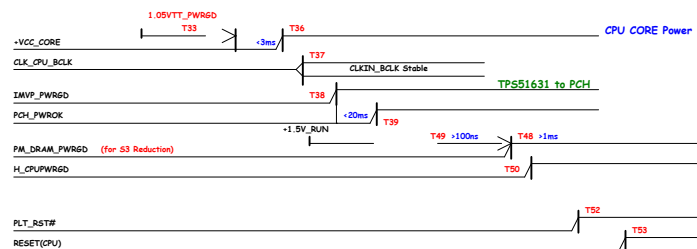
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3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

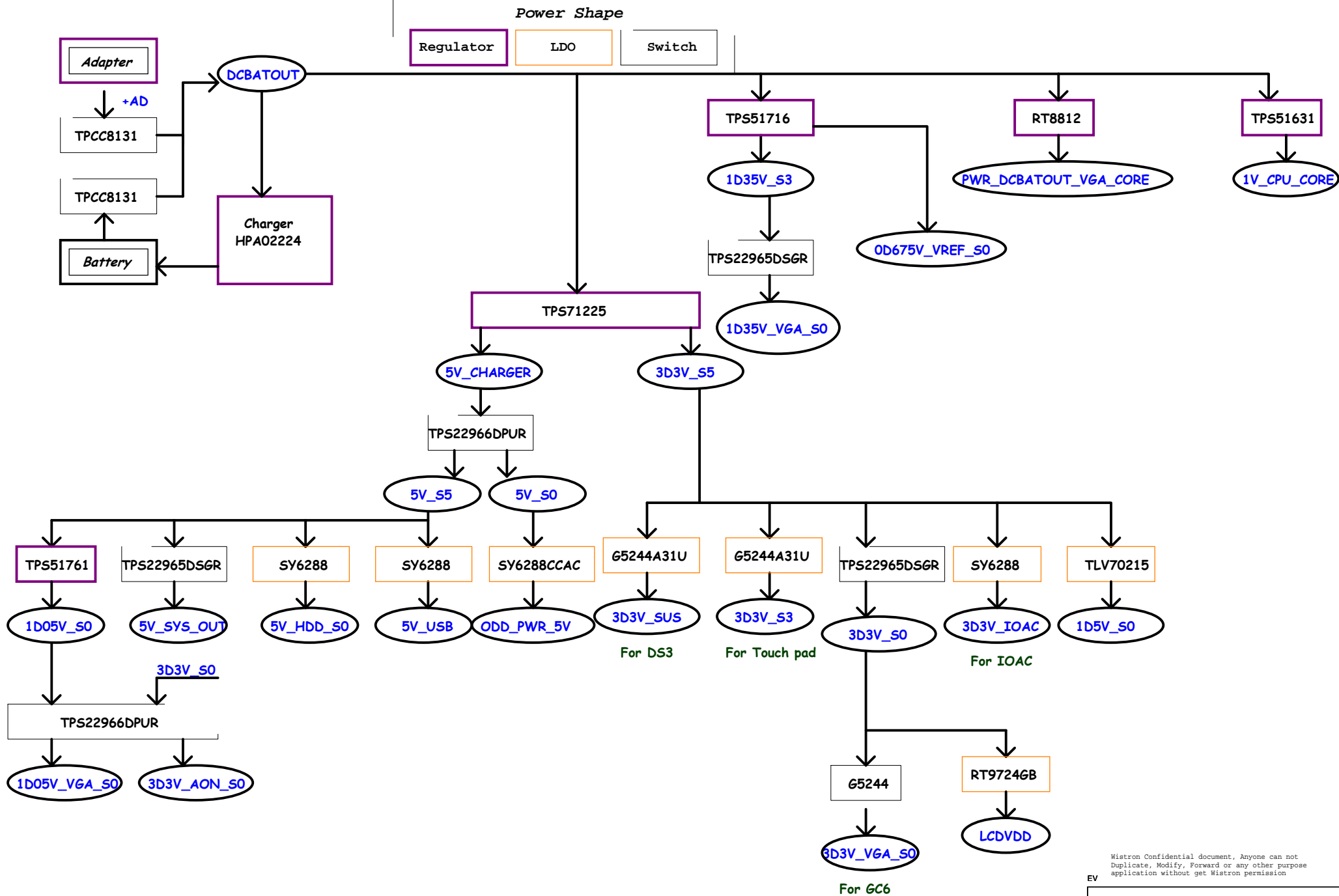
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Size A4	Document Number		Rev -1
Poseidon 860M			
Date: Tuesday, June 17, 2014		Sheet 96	of 102

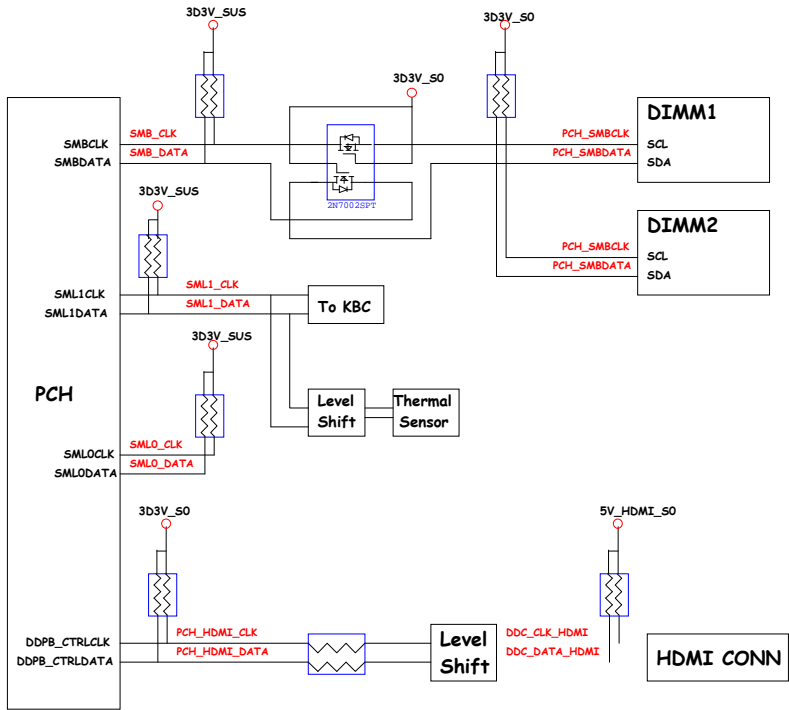
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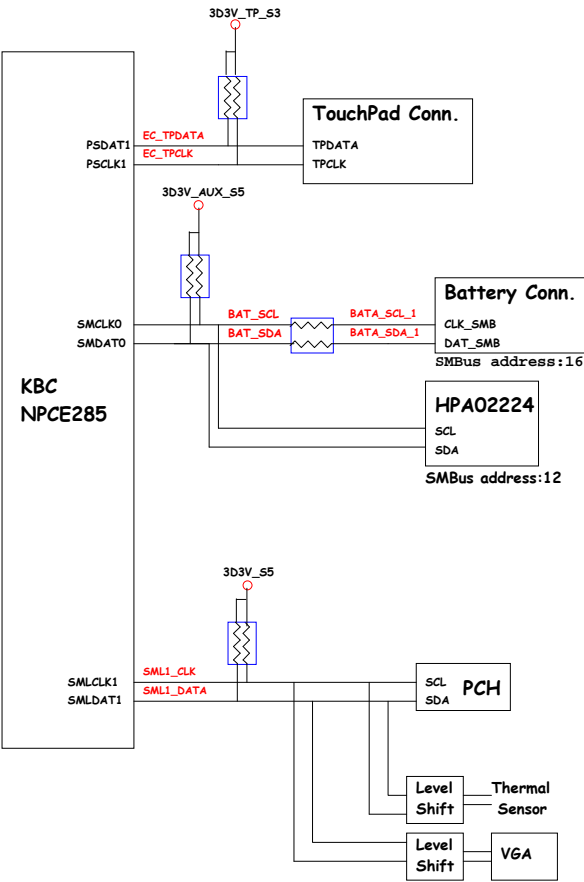


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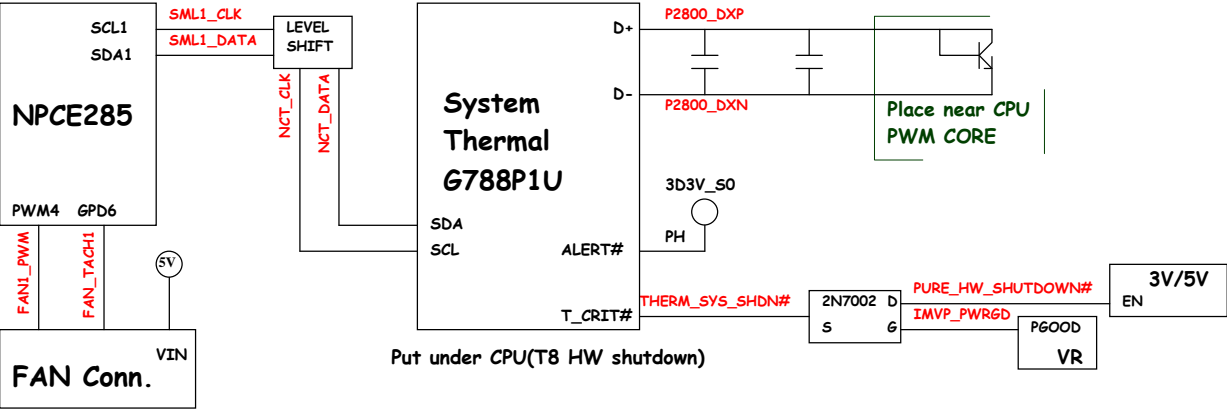
PCH SMBus Block Diagram



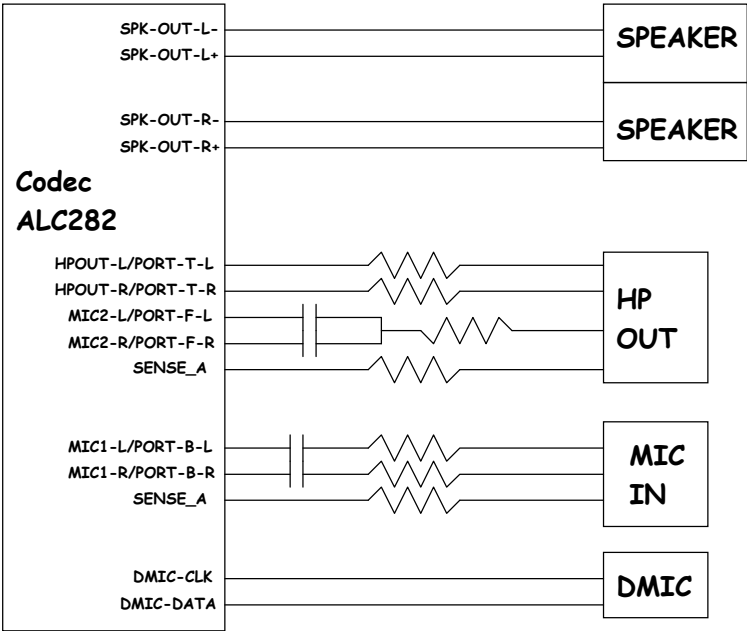
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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