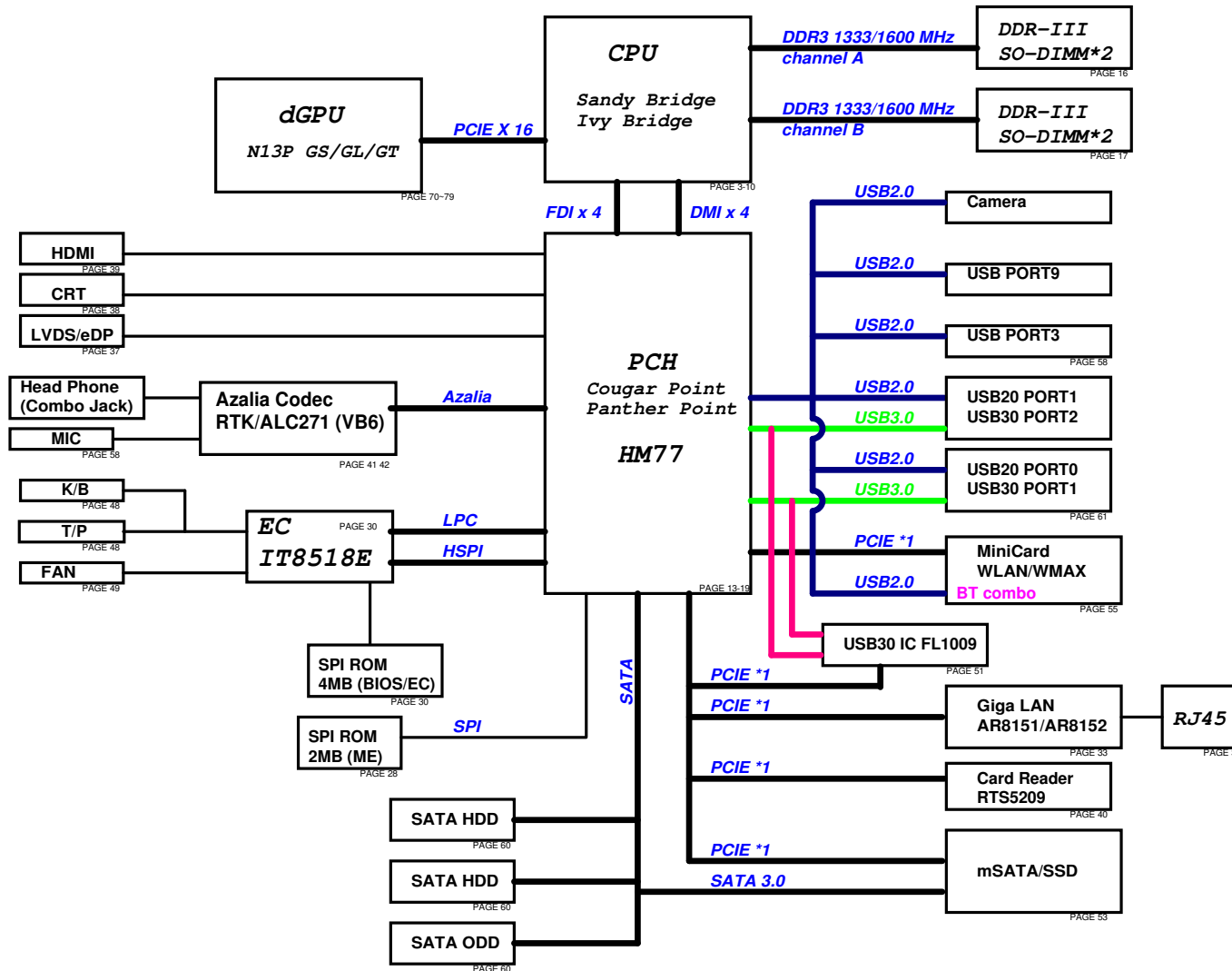


# VA70 BLOCK DIAGRAM



## POWER

CPU VCORE	PAGE 80
SYSTEM, +3V, +5V	PAGE 81
+VCCP & +VCCP_VT	PAGE 82
DDR & VTT	PAGE 83
2.5V & 1.5VS & 1.1VS	PAGE 84
SMART CHARGER	PAGE 88
POWER DETECT	PAGE 90
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

## VGA POWER

GPU VCORE	PAGE 80
+1.05VS_VGA	
+1.5VS_VGA	
+3VS_VGA	
+12VS_VGA	
LOAD SWITCH	PAGE 91
POWER PROTECT	PAGE 92

## Power Rails

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
S5/ AC	ON	ON	ON	OFF	OFF
S5/ DC	ON	ON	OFF	OFF	OFF

## PCIe Port

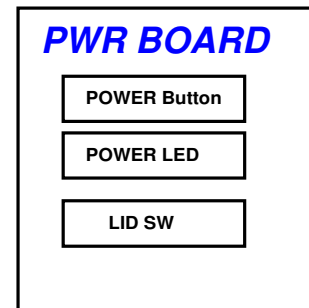
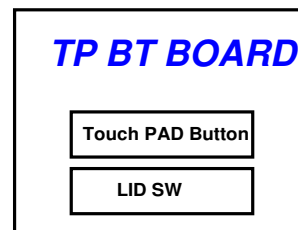
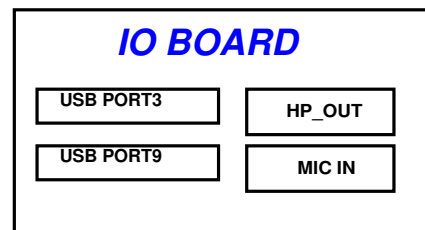
PCIe_P1	CARDREADER
PCIe_P2	Mini CARD (WLAN)
PCIe_P3	mSATA
PCIe_P4	USB30
PCIe_P5	
PCIe_P6	LAN

## USB20 PORT

USB P00	External MB
USB P01	External MB
USB P02	
USB P03	External DB
USB P04	
USB P05	BT
USB P08	Camera
USB P09	External DB
USB P10	
USB P11	SSD
USB P12	
USB P13	

## SATA PORT

SATA P0	HDD 1
SATA P1	HDD 2
SATA P2	ODD 3
SATA P3	mSATA
SATA P4	
SATA P5	



**PEGATRON**

Title : BLOCK DIAGRAM

BU1-RD Div.1-HW RD Dept.1

Engineer: Wing\_Cheng

Size Custom

Project Name

BA52HR/CR

Rev 1.0

Date: Friday, February 03, 2012

Sheet 1 of 77

BOM optional	Remark
N/A	For 上件
/ABCT	For ABCT，上件
/niAMT	For no iAMT，上件
/HOME	For 上件
/HR	For Huron River，上件
/Non_HSPI	For ROM SETTING，上件
Entry	For 上件
Main	For 上件
/USB20	For USB 2.0，上件
/HSPI	For 不上件
/HDMI	For HDMI用，不上件
/TP1_AUD	For power control，不上件
/TP1_BT	For power control，不上件
/TP1_CAMERA	For power control，不上件
/TP1_CR	For power control，不上件
/TP1_LAN	For power control，不上件
/TP1_ODD	For power control，不上件
/TP1_WLAN	For power control，不上件
/THERM	For Palm Rest溫度，不上件
/usb30	For USB 3.0，不上件
/ZPODD	For ODD battery saving使用Mount R5108，不上件
@	For 不上件
@/MP	For debug port, MP不上件
/BT270	視keypat list而定
/COMBO_BT	視keypat list而定
/SATA+	For Sata Repeater, SR先上件

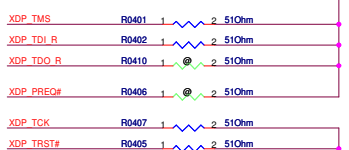
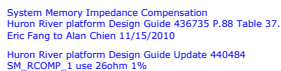
<b>PEGATRON</b>		Title : <b>System Setting</b>	
PEGATRON COMPUTER INC		Engineer: <b>Wing_Cheng</b>	
Size <b>A</b>	Project Name <b>BA52HR/CR</b>		Rev <b>1.0</b>
Date: <b>Friday, February 03, 2012</b>		Sheet <b>2</b>	of <b>94</b>



do not remove because POWER removed thier PU R. Joyoung0613



0506 EVERST check

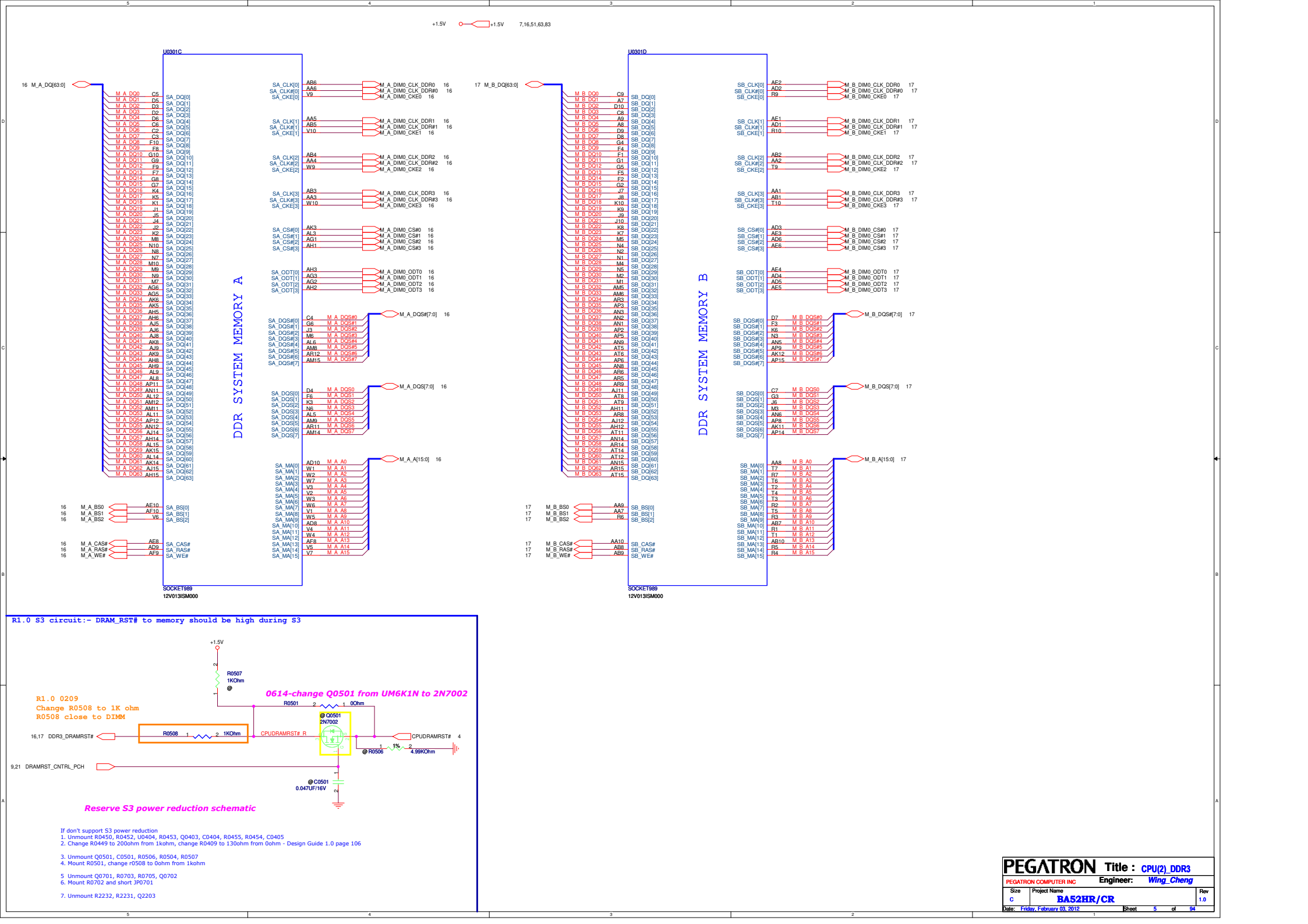


Unmount Q0501, C0501, R0506, R0504, R0507  
Mount R0501, change r0508 to 0ohm from 1kohm

Unmount Q0701, R0703, R0705, Q0702  
Mount R0702 and short JP0701

Unmount R2232, R2231, Q2203





## SENSE LINES

Frank  
20110516 Remove R0601 and R0604, because Power is already reserved

```
Decoupling guide for Everest (EE)
+VCC_CORE 22uF * 16pcs (8 nostuff)
           10uF * 10pcs (3 nostuff)
           470uF * 1pcs=>JE31HR/CR power support
```

Close to VR R0608  
1300hm

Close to VR R0605  
54.90%

+VCCP

1300nm  
1%

□ R0402

---

C	<b>BA52HR/CR</b>		
Date:	Friday, February 03, 2012	Sheet	6 of 94

SV-QC ICMAX\_VA\_XG 33A  
SV-DC ICMAX\_VA\_XG 33A  
+VGFX\_CORE

Graphics core voltage  
Voltage range: 0 - 1.52V

0622-Remove CE0705(powre schematic reserve)

HR\_Decoupling guide from Intel (POWER + EE)

+VGFX\_CORE 22uF \* 12pcs  
470uF \* 2pcs

EIH31/30

+VCCP 22uF \* 16 pcs (6 unmount)  
330uF \* 1pcs (power support)  
470uF \* 1pcs (EIH31 Del 470uF For Layout)

CR\_Decoupling guide from Intel (POWER + EE)

+VGFX\_CORE 22uF \* 12pcs  
470uF \* 2pcs

Decoupling guide for Everest (EE)

+VGFX\_CORE 22uF \* 12pcs (2 nostuff)  
470uF \* 1pcs (JE31HR/CR power support)

PLL supply voltage (DC + AC  
specification)

ICMAX\_VCCPLL 1.2A

HR\_Decoupling guide from Intel (POWER + EE)

+1.8VS 1uF \* 2pcs  
10uF \* 1pcs  
330uF \* 1pcs

EIH31/30

+1.8VS 1uF \* 2pcs  
10uF \* 1pcs  
2.2uF\*1pcs  
4.7uF\*1pcs  
22uF \* 1pcs (un-mount)

CR\_Decoupling guide from Intel (POWER + EE)

+1.8VS 1uF \* 2pcs  
10uF \* 1pcs  
330uF \* 1pcs

Decoupling guide from Everest (EE)

+1.8VS 1uF \* 2pcs  
10uF \* 1pcs  
100uF \* 1pcs

## POWER

U0301G

VAXG1  
VAXG2  
VAXG3  
VAXG4  
VAXG5  
VAXG6  
VAXG7  
VAXG8  
VAXG9  
VAXG10  
VAXG11  
VAXG12  
VAXG13  
VAXG14  
VAXG15  
VAXG16  
VAXG17  
VAXG18  
VAXG19  
VAXG20  
VAXG21  
VAXG22  
VAXG23  
VAXG24  
VAXG25  
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VAXG30  
VAXG31  
VAXG32  
VAXG33  
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VAXG40  
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VAXG42  
VAXG43  
VAXG44  
VAXG45  
VAXG46  
VAXG47  
VAXG48  
VAXG49  
VAXG50  
VAXG51  
VAXG52  
VAXG53  
VAXG54

VCCPLL1  
VCCPLL2  
VCCPLL3  
VCCSA1  
VCCSA2  
VCCSA3  
VCCSA4  
VCCSA5  
VCCSA6  
VCCSA7  
VCCSA8  
VCCSA\_SENSE  
VCCSA\_SEL0  
VCCSA\_SEL1  
VCCSA\_VDD1

SOCKET988  
12V013ISM000

SENSE  
LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

MISC

1.8V RAIL

R1.0 Add net name, Joyoung 0621  
0614-Add SP0701,SP0702

VCCGT\_SENSE R  
VSSGT\_SENSE R  
SP0701 2  
SP0702 2  
R0402 1  
R0402 1

Close to CPU

+V\_SM\_REF 10mV  
+V\_SM\_VREF CNT

R0702 1 2 00hm  
R0703 100K0hm  
Q0701 SI2308DS-T1-E3

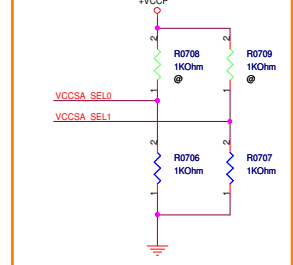
VDDQ1  
VDDQ2  
VDDQ3  
VDDQ4  
VDDQ5  
VDDQ6  
VDDQ7  
VDDQ8  
VDDQ9  
VDDQ10  
VDDQ11  
VDDQ12  
VDDQ13  
VDDQ14  
VDDQ15

VCCSA1  
VCCSA2  
VCCSA3  
VCCSA4  
VCCSA5  
VCCSA6  
VCCSA7  
VCCSA8  
VCCSA\_SENSE  
VCCSA\_SEL0  
VCCSA\_SEL1

H23  
C22  
C24

R0704 1 2 00hm  
VCCSA\_SEL0 85  
VCCSA\_SEL1 85

R1.0 0209  
Intel Comments



DDR3 Reference Voltage

Reserve S3 power reduction schematic

+1.5V\_VCCDDQ

+V\_SM\_VREF

PS\_S3CNTRL 1.5V\_R 2

R0705 00hm

R0706 470PF/50V

+1.5V

ICCMAX\_VDDQ 5A Joyoung 0613

Reduce to 5A (EDS R2.1)

Processor I/O supply  
voltage for DDR3  
(DC + AC specification)

0614-Change JP(3MM\_OPEN\_5MIL)

3MM\_OPEN\_5MIL  
JP0701

SUSB\_EC#

+1.5V\_VCCDDQ

+1.5V\_VCCDDQ Power Good  
(U0404 pin 4)

+0.75VS

>100 ns

R1.3

+VCCP 3,4,6,25,26,27,37,47,63,82  
+1.5V 5,16,51,63,83  
+VCCSA 85  
+1.8VS 25,26,63,84  
+VGFX\_CORE 63,80  
+1.5V\_VCCDDQ 4  
+V\_SM\_VREF 18

HR\_Decoupling guide from Intel (POWER + EE)

+VDDQ 10uF \* 6pcs  
330uF \* 1pcs

EIH31

+VDDQ 10uF \* 6pcs (3 nostuff)  
220uF \* 1pcs

CR\_Decoupling guide from Intel (POWER + EE)

+VDDQ 10uF \* 6pcs  
330uF \* 1pcs

Decoupling guide for Everest (EE)

+VDDQ 10uF \* 6pcs (3 nostuff)  
220uF \* 1pcs

+VCCSA_SEL0	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

HR\_Decoupling guide from Intel (POWER + EE)

+VCCSA 10uF \* 3pcs  
330uF \* 1pcs

EIH31/30

+VCCSA 10uF \* 4pcs (2 nostuff)  
100uF \* 1pcs

CR\_Decoupling guide from Intel (POWER + EE)

+VCCSA 10uF \* 3pcs  
330uF \* 1pcs

Decoupling guide for Everest (EE)

+VCCSA 10uF \* 3pcs (1 nostuff)  
100uF \* 1pcs

PEGATRON Title : CPU(4)\_PWR

PEGATRON COMPUTER INC Engineer: Wing Cheng

Size C Project Name BA52HR/CR Rev 1.0

Date: Friday, February 03, 2012 Sheet 7 of 94

U0301H

AT35	VSS1	AJ22
AT32	VSS2	AJ19
AT29	VSS3	AJ16
AT27	VSS4	AJ13
AT25	VSS5	AJ10
AT22	VSS6	AJ7
AT19	VSS7	AJ4
AT16	VSS8	AJ3
AT13	VSS9	AJ2
AT10	VSS10	AJ1
AT7	VSS11	AH35
AT4	VSS12	AH32
AT3	VSS13	AH30
AR25	VSS14	AH29
AR22	VSS15	AH28
AR19	VSS16	AH26
AR16	VSS17	AH25
AR13	VSS18	AH19
AR10	VSS19	AH18
AR7	VSS20	AH16
AR4	VSS21	AH14
AR2	VSS22	AH13
AP34	VSS23	AH10
AP31	VSS24	AH9
AP28	VSS25	AH8
AP25	VSS26	AG4
AP22	VSS27	AG3
AP19	VSS28	AG2
AP16	VSS29	AG1
AP13	VSS30	AG0
AP10	VSS31	AG0
AP7	VSS32	AG0
AP4	VSS33	AG0
AP1	VSS34	AG0
AN30	VSS35	AG0
AN27	VSS36	AG0
AN25	VSS37	AG0
AN22	VSS38	AG0
AN19	VSS39	AG0
AN16	VSS40	AG0
AN13	VSS41	AG0
AN10	VSS42	AG0
AN7	VSS43	AG0
AM4	VSS44	AG0
AM29	VSS45	AG0
AM25	VSS46	AG0
AM22	VSS47	AG0
AM19	VSS48	AG0
AM16	VSS49	AG0
AM13	VSS50	AG0
AM10	VSS51	AG0
AM7	VSS52	AG0
AM4	VSS53	AG0
AM3	VSS54	AG0
AM2	VSS55	AG0
AM1	VSS56	AG0
AL34	VSS57	AG0
AL31	VSS58	AG0
AL28	VSS59	AG0
AL25	VSS60	AG0
AL22	VSS61	AG0
AL19	VSS62	AG0
AL16	VSS63	AG0
AL13	VSS64	AG0
AL10	VSS65	AG0
AL7	VSS66	AG0
AL4	VSS67	AG0
AL2	VSS68	AG0
AK33	VSS69	AG0
AK30	VSS70	AG0
AK27	VSS71	AG0
AK25	VSS72	AG0
AK22	VSS73	AG0
AK19	VSS74	AG0
AK16	VSS75	AG0
AK13	VSS76	AG0
AK10	VSS77	AG0
AK7	VSS78	AG0
AK4	VSS79	AG0
AJ25	VSS80	AG0

VSS

SOCKET1989  
12V013ISM000

U0301I

T35	VSS161	VSS234
T34	VSS162	F22
T33	VSS163	F19
T32	VSS164	E30
T31	VSS165	E27
T30	VSS166	E24
T29	VSS167	E21
T28	VSS168	E18
T27	VSS169	E15
T26	VSS170	E13
T25	VSS171	E10
T24	VSS172	E9
T23	VSS173	E8
T22	VSS174	E7
T21	VSS175	E6
T20	VSS176	E5
T19	VSS177	E4
T18	VSS178	E3
T17	VSS179	E2
T16	VSS180	E1
T15	VSS181	D35
T14	VSS182	D32
T13	VSS183	D29
T12	VSS184	D26
T11	VSS185	D23
T10	VSS186	D20
T9	VSS187	D17
T8	VSS188	C34
T7	VSS189	C31
T6	VSS190	C28
T5	VSS191	C27
T4	VSS192	C25
T3	VSS193	C23
T2	VSS194	C10
T1	VSS195	C1
L4	VSS196	B22
L3	VSS197	B19
L2	VSS198	B17
L1	VSS199	B15
K35	VSS200	B13
K34	VSS201	B11
K33	VSS202	B9
K32	VSS203	B8
K31	VSS204	B7
K30	VSS205	B6
K29	VSS206	B5
K28	VSS207	B4
K27	VSS208	B3
K26	VSS209	B2
K25	VSS210	A35
K24	VSS211	A32
K23	VSS212	A29
K22	VSS213	A26
K21	VSS214	A23
K20	VSS215	A20
K19	VSS216	A17
K18	VSS217	A14
K17	VSS218	A11
K16	VSS219	A8
K15	VSS220	A5
K14	VSS221	A2
K13	VSS222	A1
K12	VSS223	A0
K11	VSS224	A0
K10	VSS225	A0
K9	VSS226	A0
K8	VSS227	A0
K7	VSS228	A0
K6	VSS229	A0
K5	VSS230	A0
K4	VSS231	A0
K3	VSS232	A0
K2	VSS233	A0
K1	VSS234	A0

VSS

SOCKET1989  
12V013ISM000

R1.0

TP YSSG DIE SENSE I T0801

## CFG strapping information:

### CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches socket pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

### CFG[4]: Embedded DisplayPort Detection

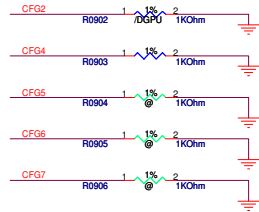
- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

### CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

### CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training



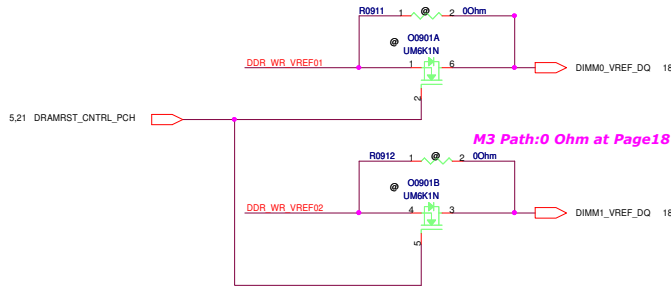
This model is UMA, unmount R0902(use Default)

Power schematic reserve 1.0V or not??

+VCCIO_SEL	
1	1.05V
0	1.00V

IVB VCCIO for Mobile and Desktop is changed from 1.0v to 1.05v, same as PPT VCCIO. (461017 WW23'11)

## PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:



Reserve S3 power reduction schematic

M3: Processor Generated SO-DIMM VREFDQ  
- New Requirement

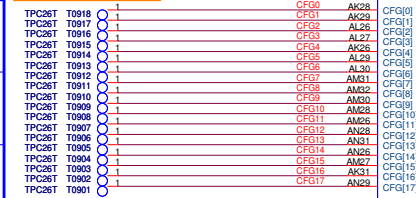
Sandy Bridge CPU Only: M1 Implementation  
Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation

R1.0

Add CFG0

Frank

0516 Remove CFG0 to XDP



VREF VAL SENSE AH31

VREF VAL SENSE AH31

VREF VAL SENSE AH31

VREF VAL SENSE AH31

VREF VAL SENSE AH31

VREF VAL SENSE AH31

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VREF VAL SENSE AH31

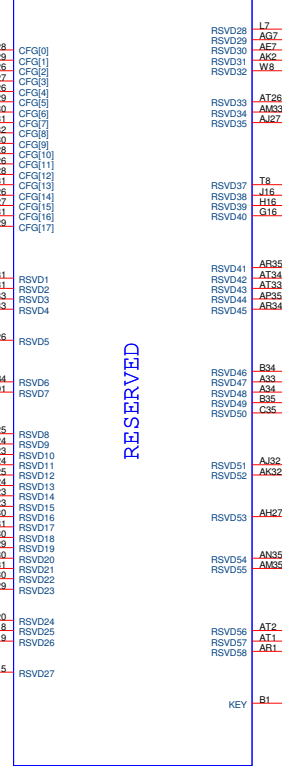
VREF VAL SENSE AH31

VREF VAL SENSE AH31

VREF VAL SENSE AH31

VREF VAL SENSE AH31

U0301E

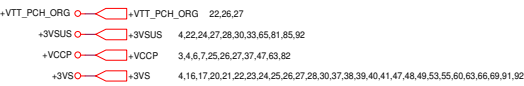


SOCKET989

12V013ISM000

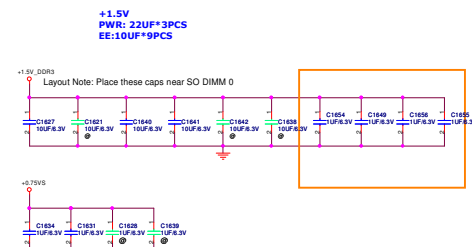
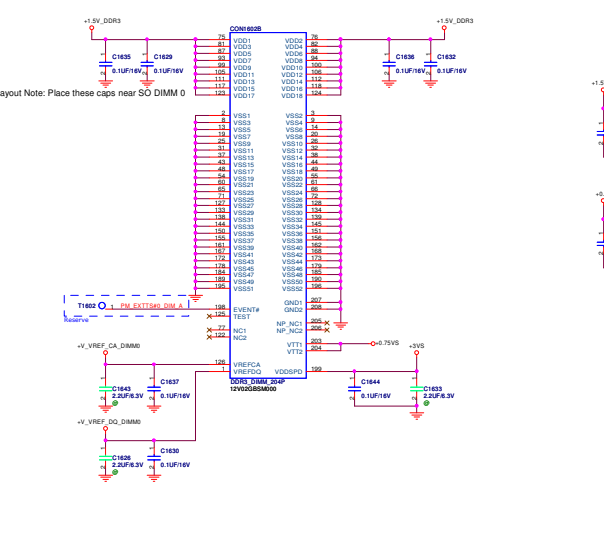
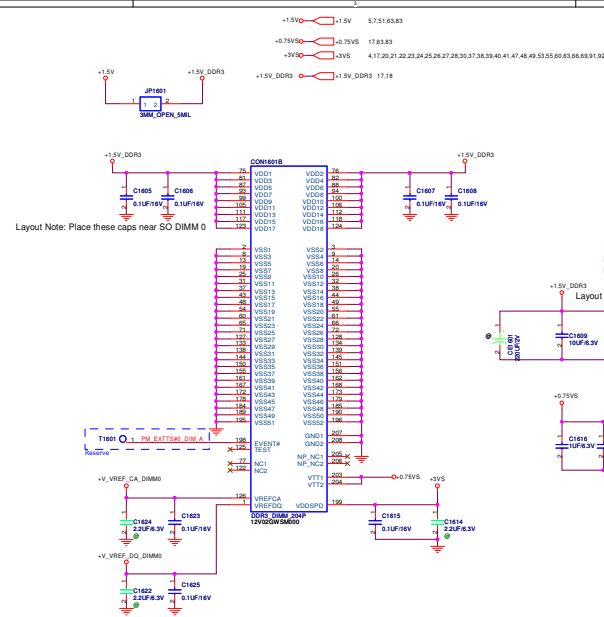
RESERVED

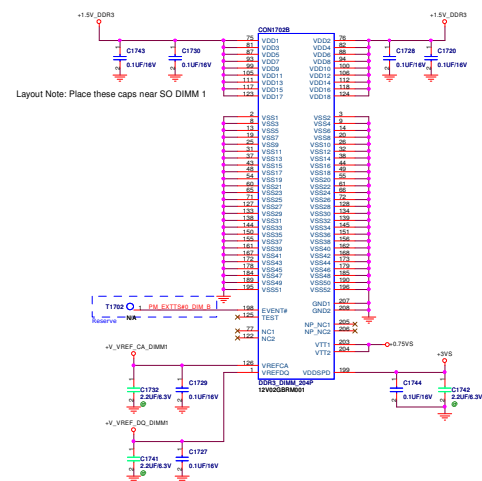
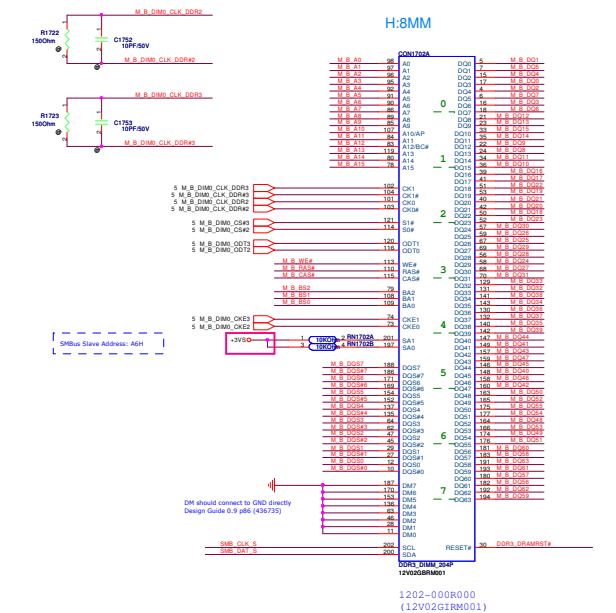
KEY



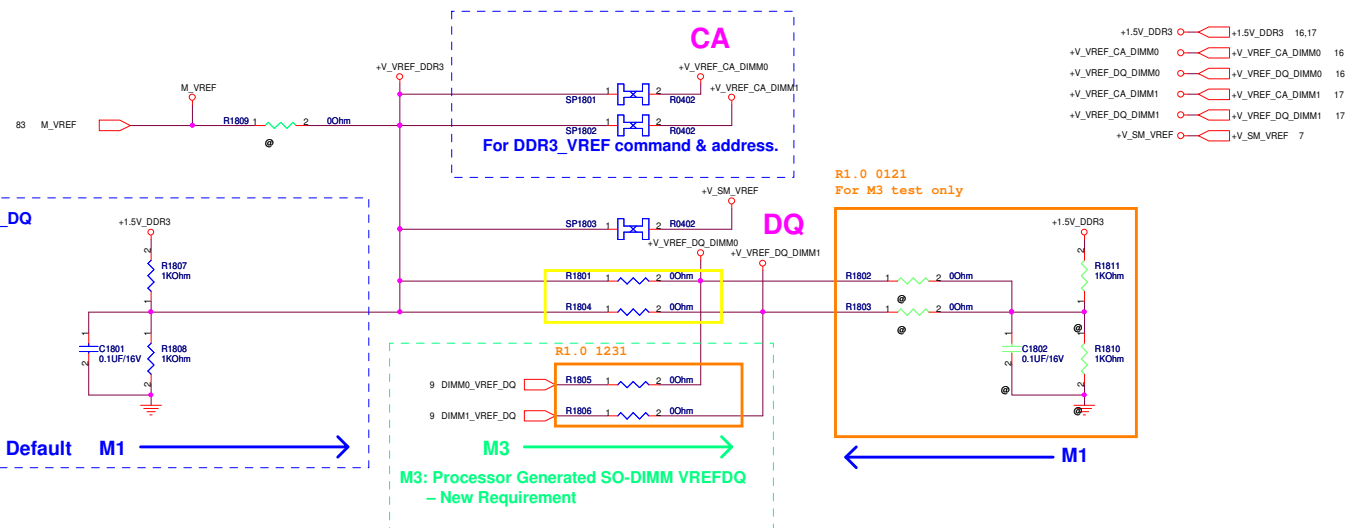
CPU XDP connector

PCH XDP connector





# DDR3 Vref



If support M1 :(Sandy Bridge CPU Only)

1. Un mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Mount R1801,R1804

==>CA and DQ are the same path

If support M1 and M3 :(Sandy Bridge/Ivy Bridge CPU)

1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
2. Un mount R1801,R1804

==> CA and DQ are separate path

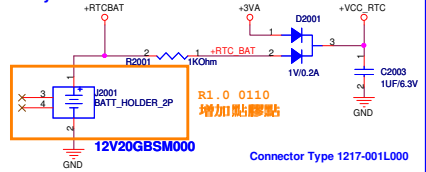
**Sandy Bridge CPU Only: M1 Implementation**  
**Sandy Bridge/Ivy Bridge CPU: M1 and M3 Implementation**

5	4	3	2	1
D				D
C				C
B				B
A				A

R1.4--2

<b>PEGATRON</b>		<b>Title : VID Controller</b>	
PEGATRON COMPUTER INC		Engineer: <i>Wing Cheng</i>	
Size	Project Name		Rev
C	BA52HR/CR		1.0
Date: Friday, February 03, 2012		Sheet	19 of 94

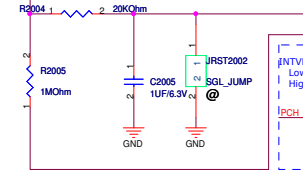
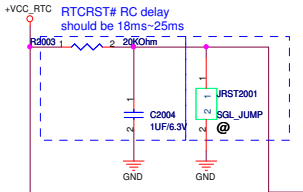
## RTC battery



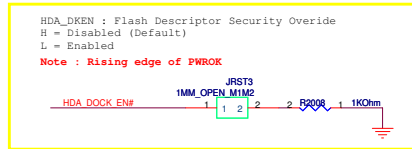
Connector Type 1217-001L000

Request by CSC  
for CMOS clear  
function

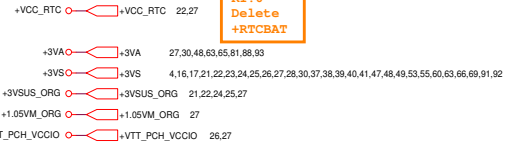
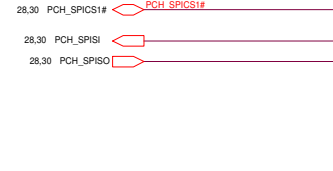
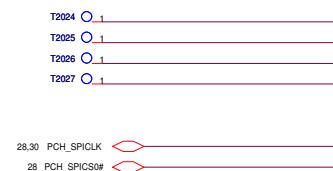
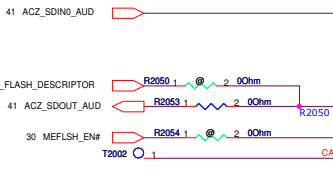
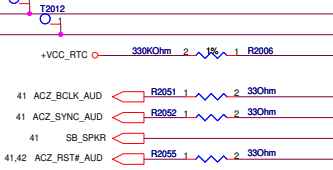
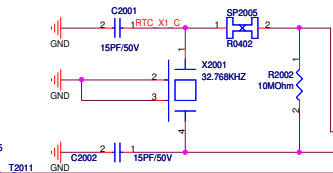
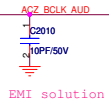
CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)



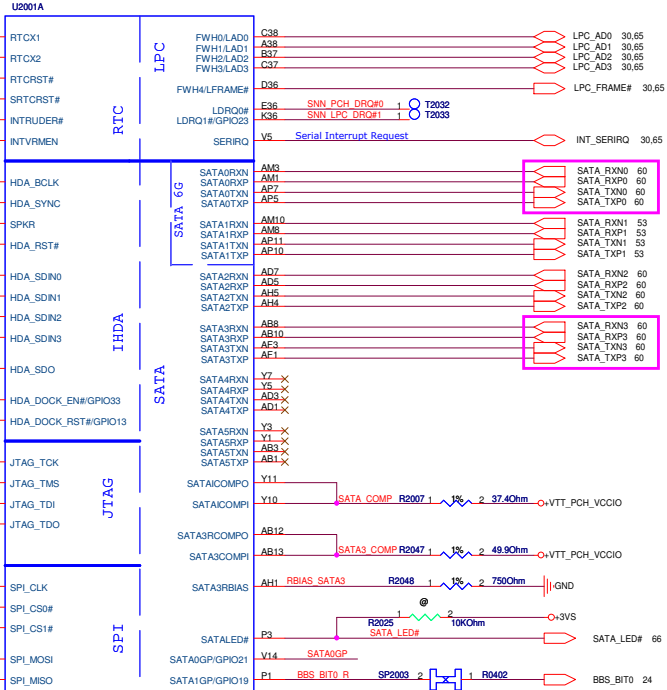
TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)



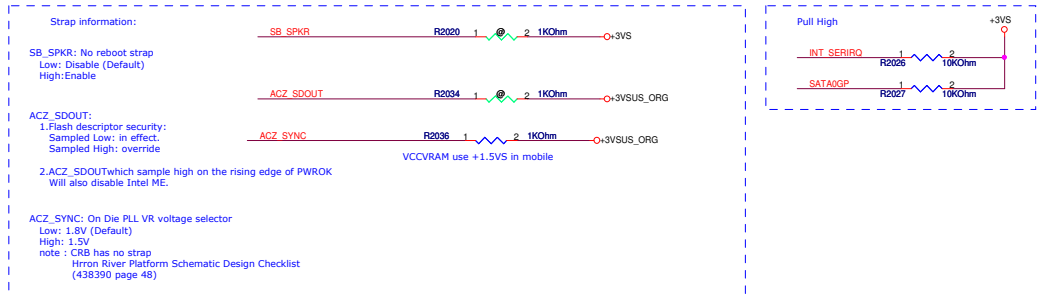
R1.0 add JRST3 to follow BIC50. Joyoung 0628



R1.0  
Delete  
+RTC\_BAT



0200-00HU000 C.5 907552 A1 QMVY BGA942 INTEL/COUGAR POINT PCH









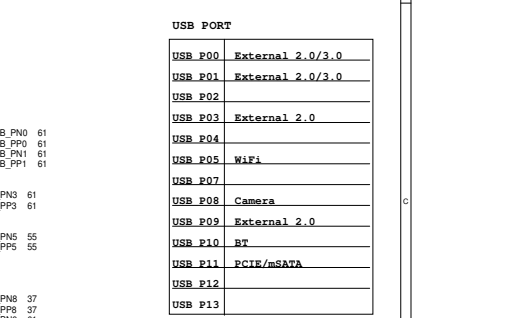
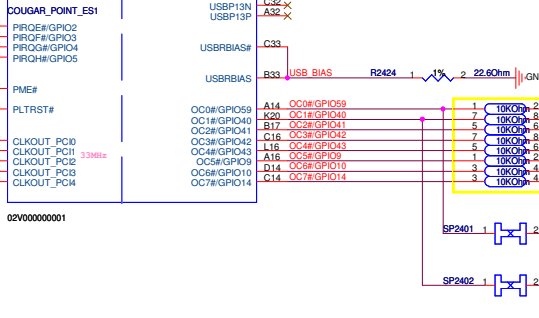
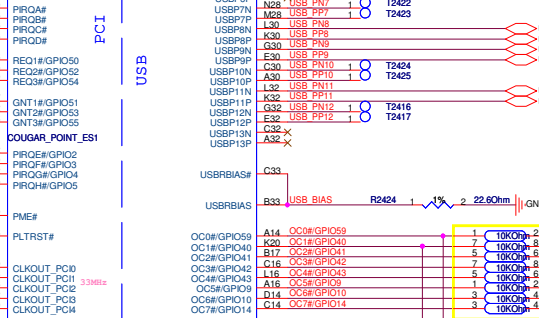
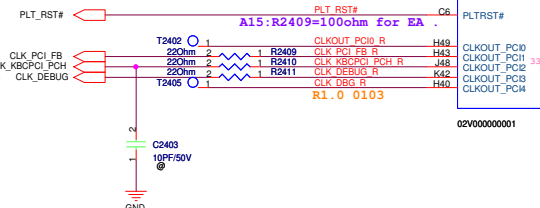
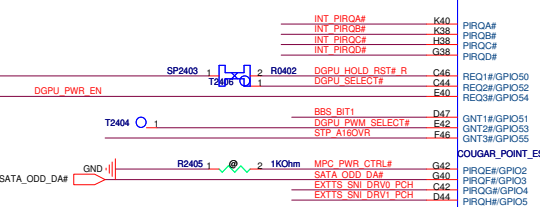
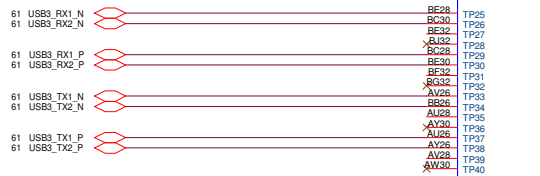
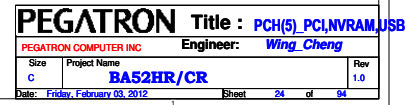


Diagram showing the connection of USB pins 61 and 62. Pin 61 is labeled +3VSUS\_ORG and is connected to a 3.3V supply. Pin 62 is labeled USB\_OC0# and is connected to a 3.3V supply. A note indicates that the pins should be placed within 500 mils of PCH.

**STP\_A16OVR:**  
**A16 swap override Strap/  
Top-Block swap override jumper**

Low=Enabled A16 swap override/ Top-Block swap override
<b>High=Default</b>

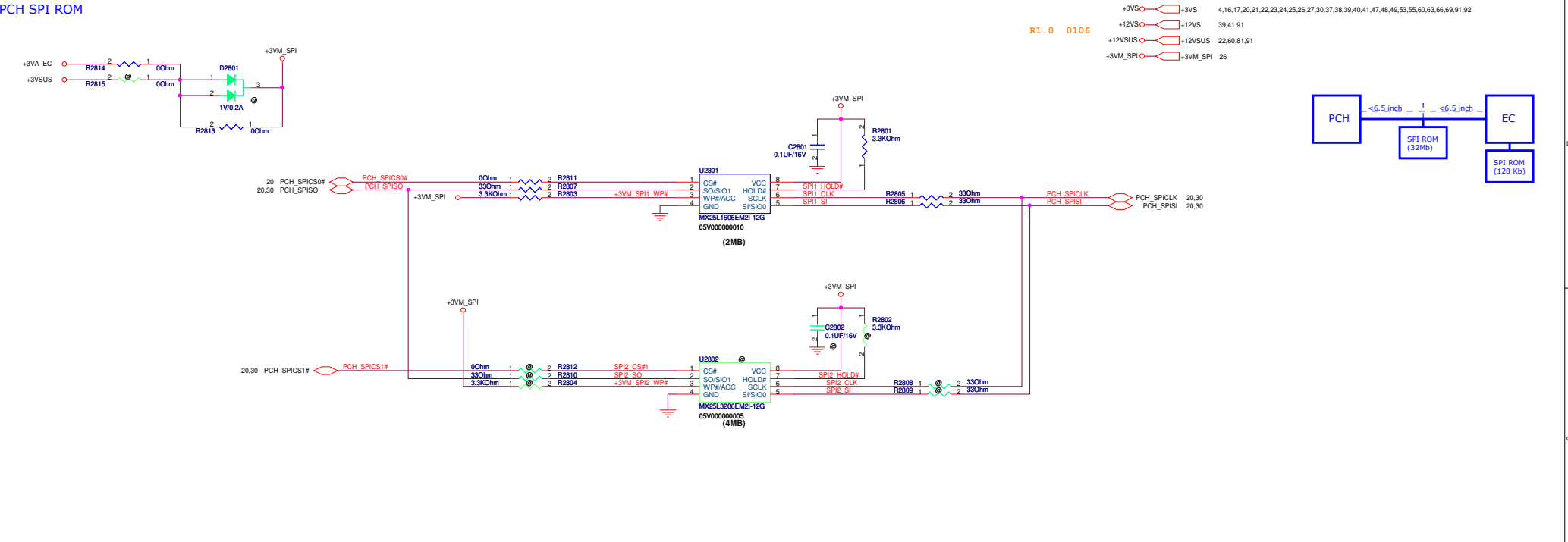




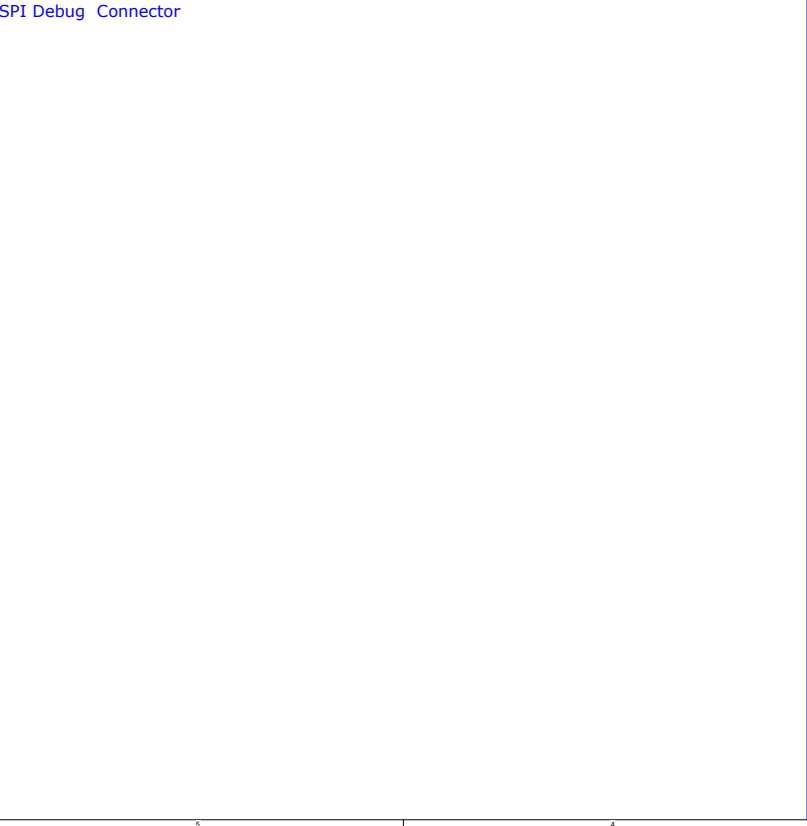




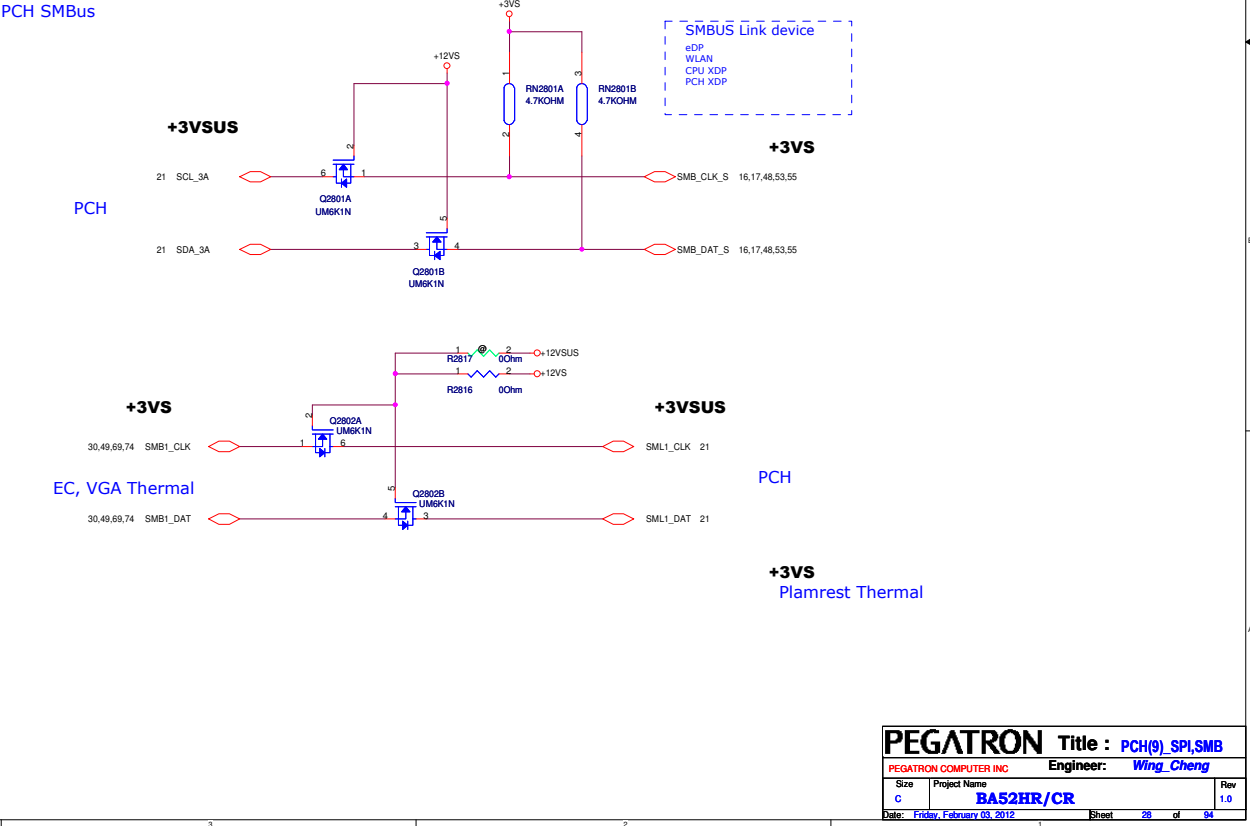
PCH SPI ROM



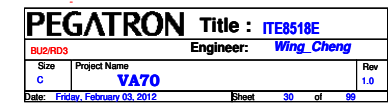
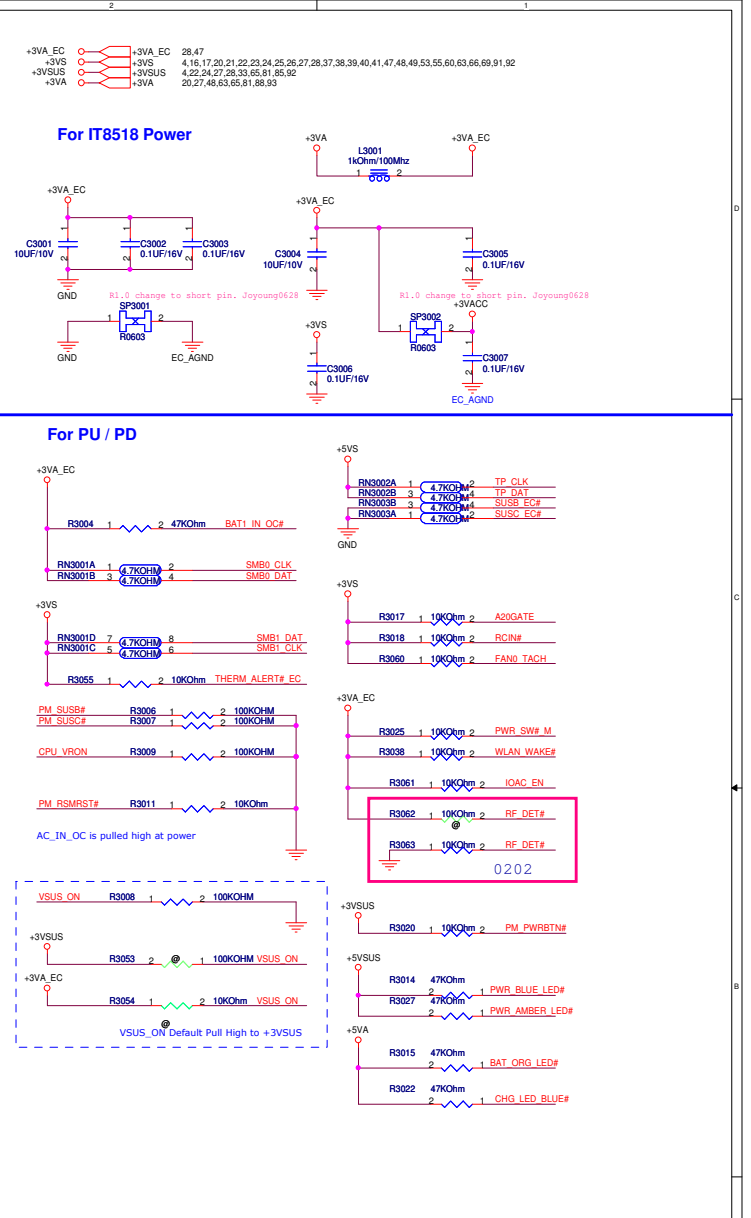
SPI Debug Connector



PCH SMBus

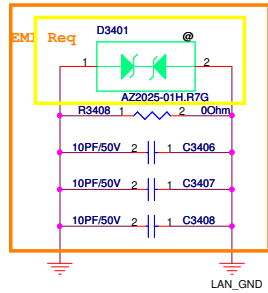
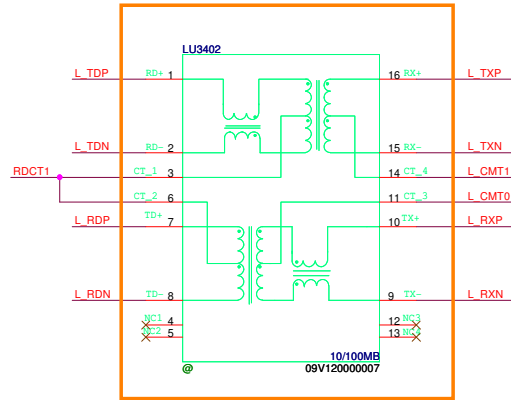


5	4	3	2	1
D				D
C				C
B				B
A				A



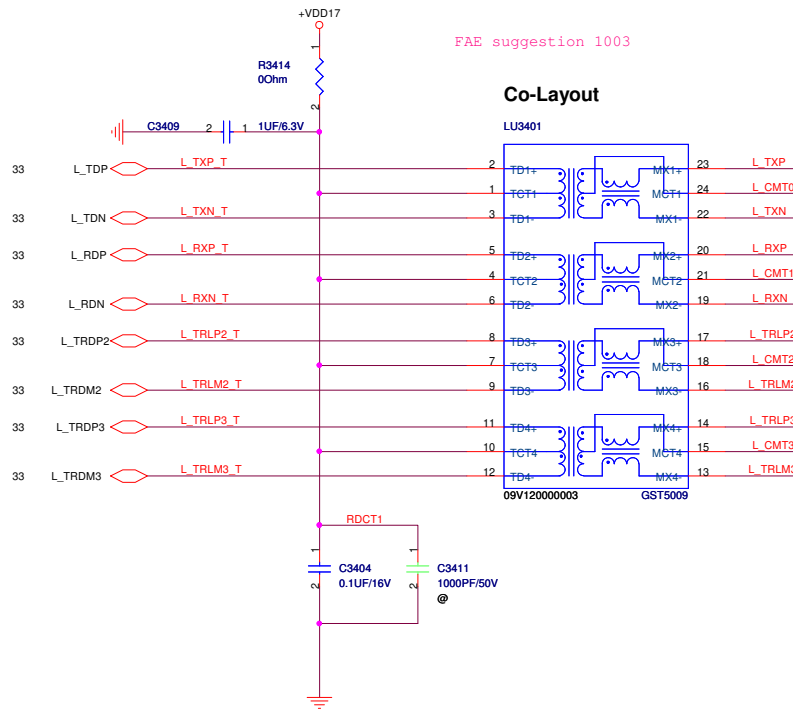


11/30 Swap for LU3401/LU3402 co-lay(Elmer)

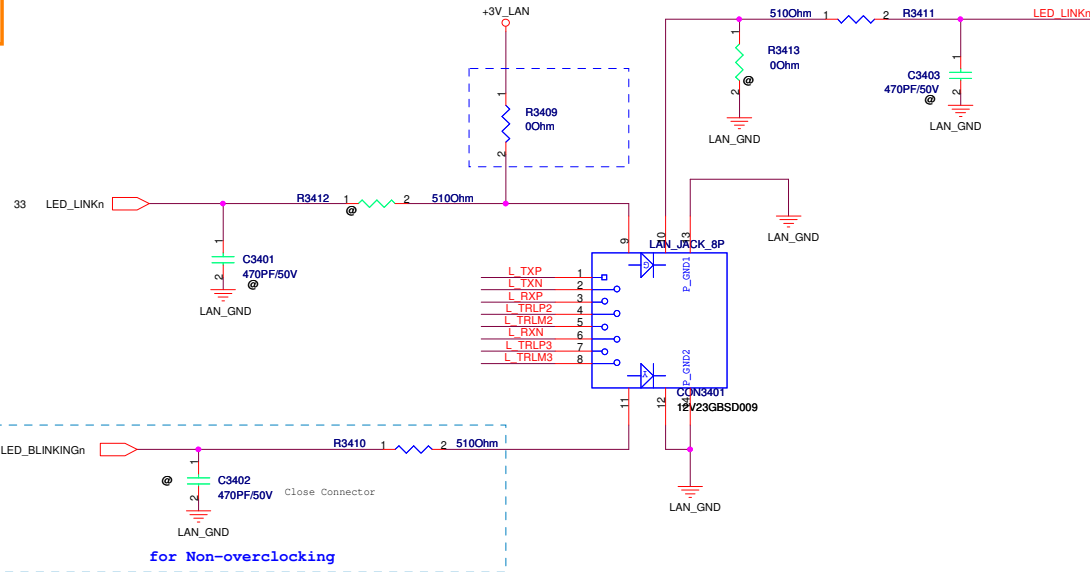
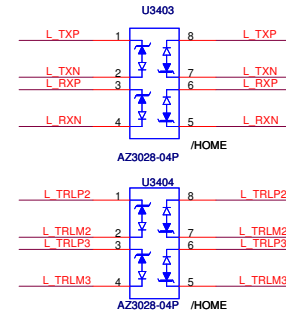
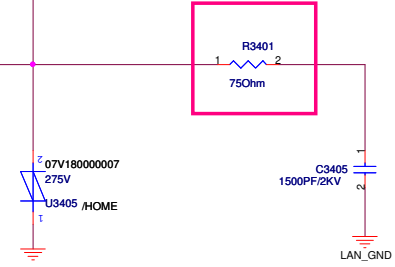


FAE suggestion 1003

### Co-Layout



EMI suggest to change 0805 size 0921

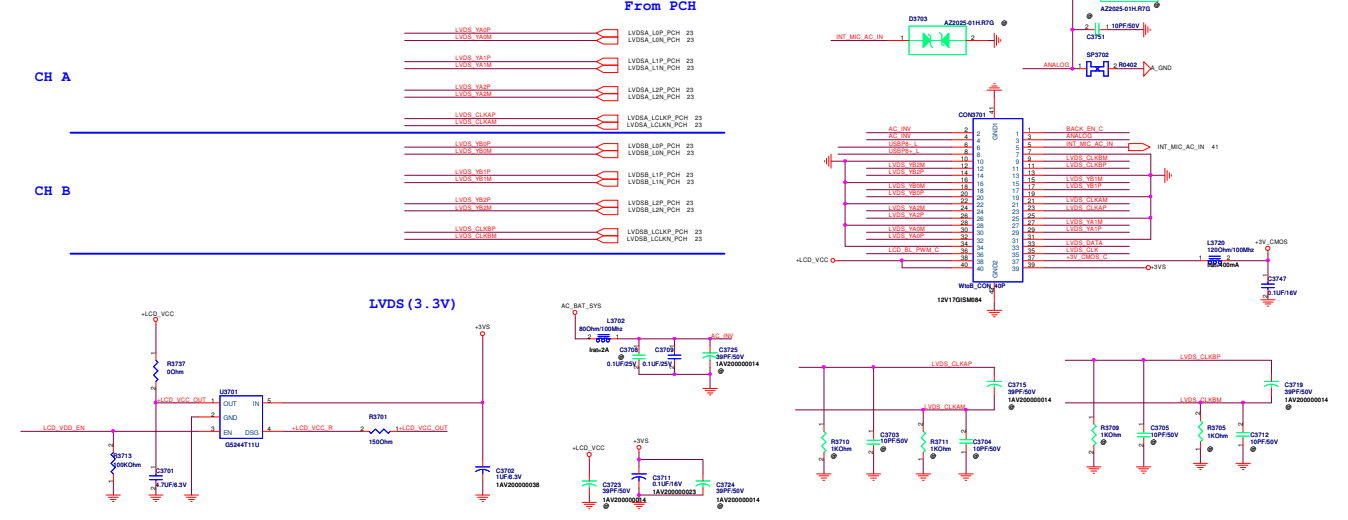


for Non-overclocking

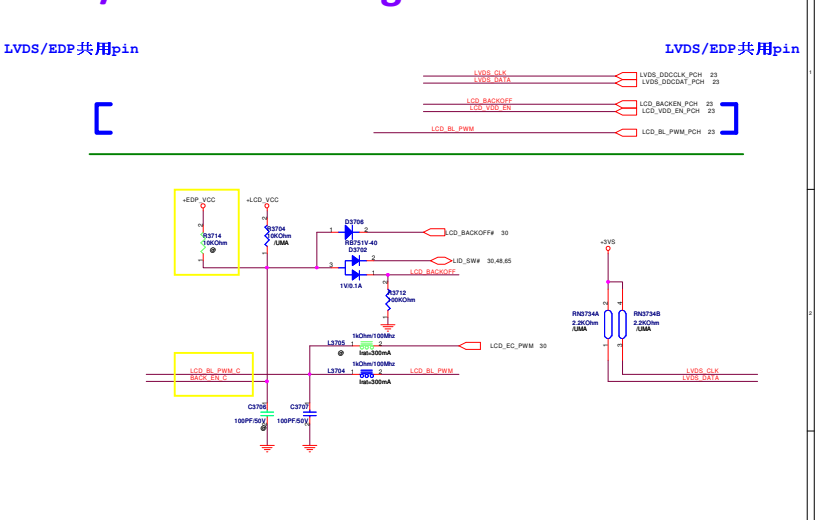
<Variant Name>

<b>PEGATRON</b> Title : RJ45/RJ11	
BG1-CSC-HW R&D Dept.5 Engineer: Ahren_chen	
Size Custom	Project Name PLFG
Date: Friday, February 03, 2012	Sheet 34 of 99

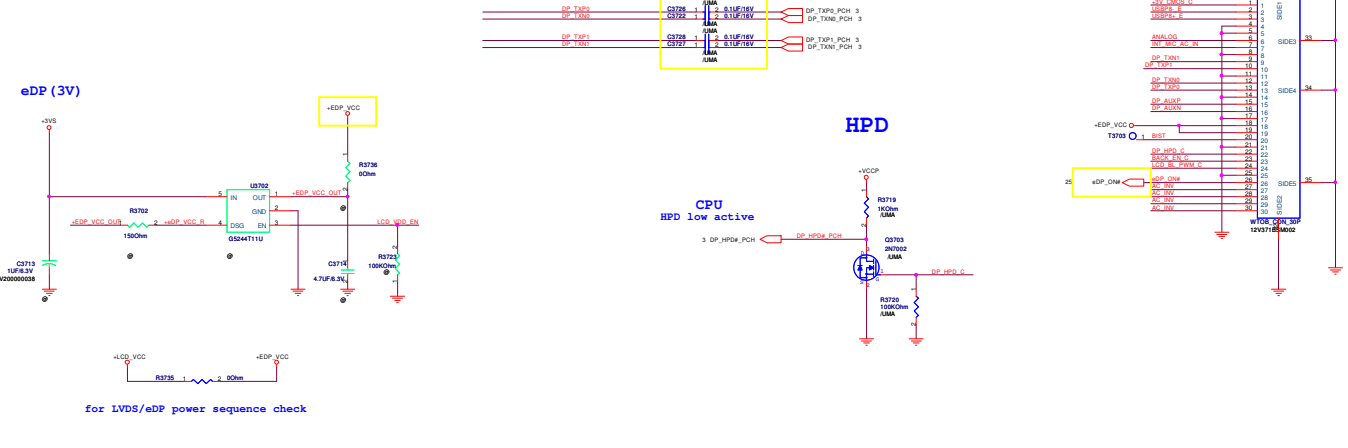
LVDS



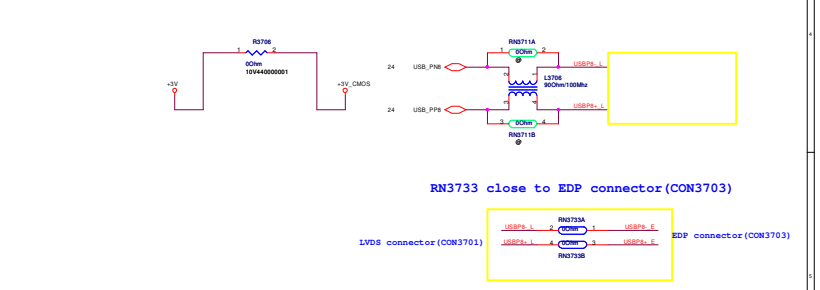
LVDS/eDP control signal



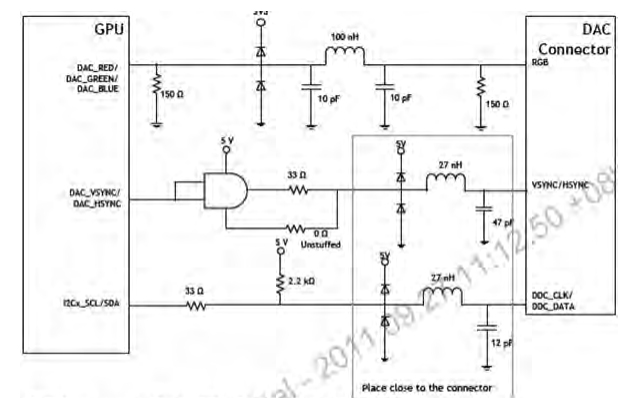
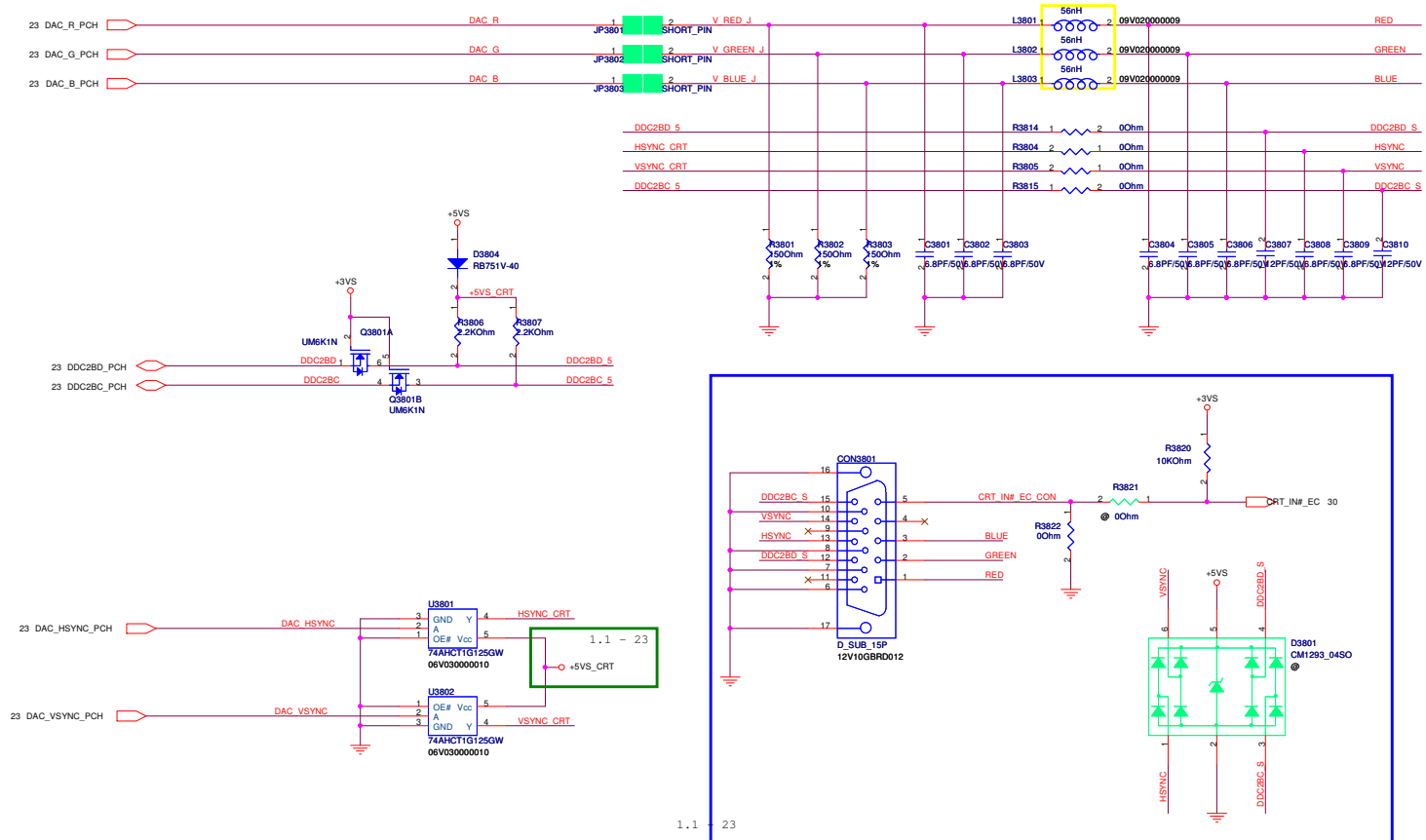
eDP



USB Camera



Check UMA and DSC inductor value



**RSET Requirements:** DACA\_RSET= 124  $\Omega$ , 1%, stuffed by default.

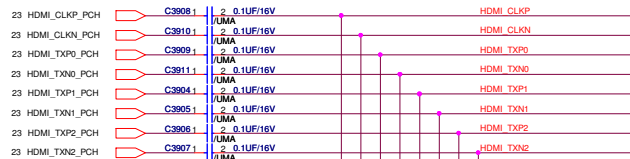
Figure 71. GPU-DAC Connections

The LC filter circuit (NV DSC only)

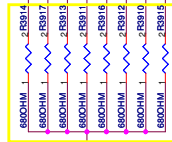
DDC :  $L=27\text{nH}$ ,  $C=12\text{PF}$

HSYNC/VSYNC:  $L=27\text{nH}$ ,  $C=47\text{PF}$ 

RGB :  $L=100\text{nH}$ ,  $C=10\text{PF}$

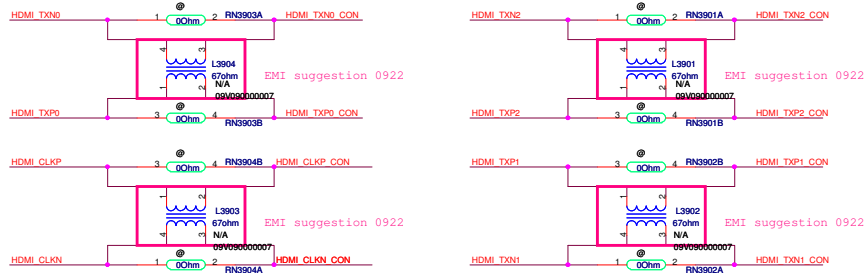
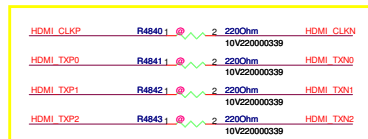


Close to connector and do T routing

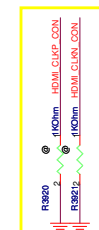
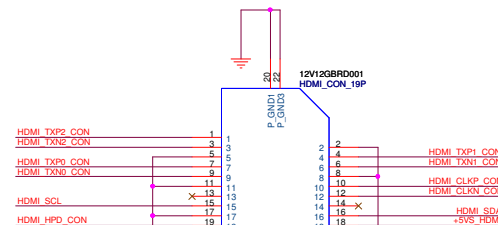


R3910, R3911, R3912, R3913, R3914, R3915, R3916, R3917  
Intel design guide : 680ohm /UMA  
NV reference schematics : 499ohm /DGPUO

### EMI solution



HDMI\_SCL & HDMI\_SDA : no via , trace length should be as short as possible

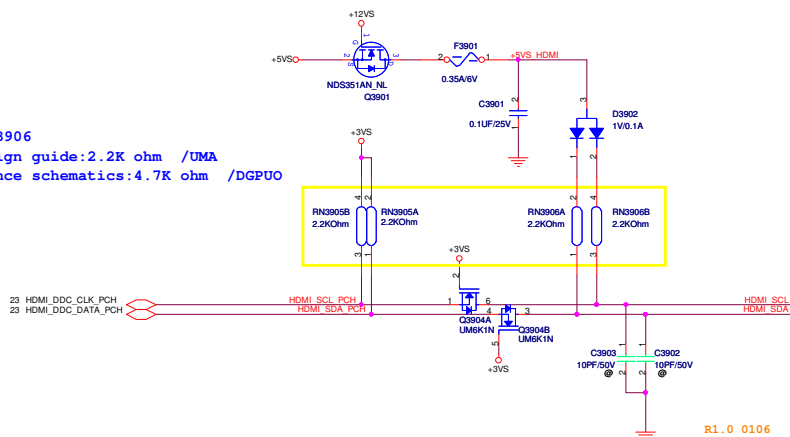


EMI solution

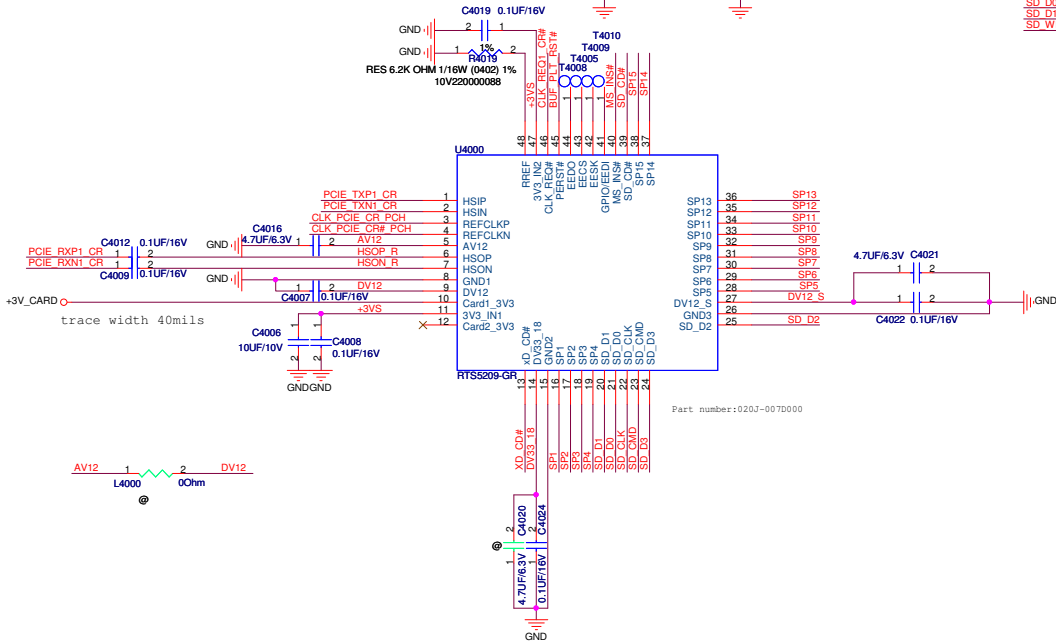
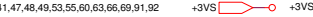
R1.0 0106  
HDMI HPD Cost Reduced Level Shifter Design Recommendation



RN3905, RN3906  
Intel design guide: 2.2K ohm /UMA  
NV reference schematics: 4.7K ohm /DGPUO



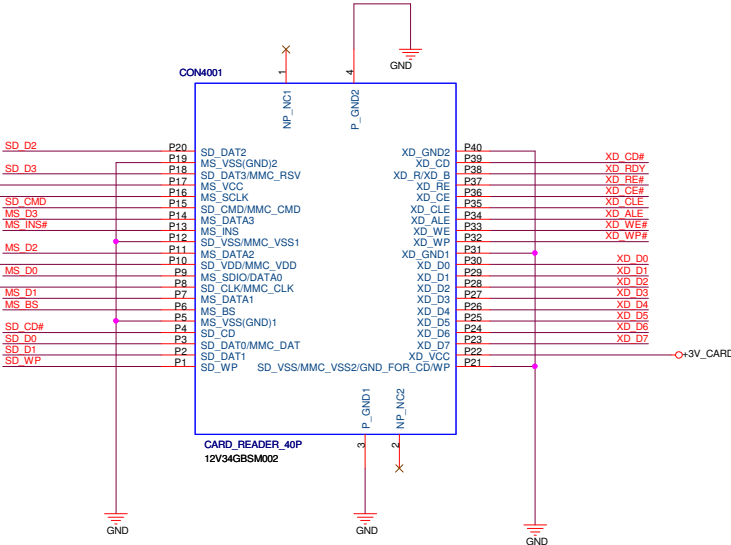
From System's PCIE interface



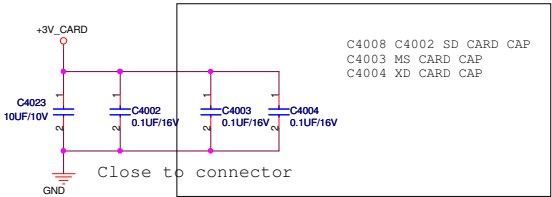
Remove Serial Flash

Reserve for BIOS boot function

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.



SD/MMC/MC plus/MS/xD



Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

SP1	SD_D7	XD_RDY
SP2	SD_D6	XD_RE#
SP3	SD_D5	XD_CE#
SP4	SD_D4	XD_WE#
SP5	MS_BS	XD_CLE
SP6	MS_D5	XD_ALE
SP7	MS_D1	XD_WP#
SP8	MS_D4	XD_D0
SP9	MS_D0	XD_D1
SP10	MS_D2	XD_D2
SP11	MS_D6	XD_D3
SP12	MS_D3	XD_D4
SP13	MS_D7	XD_D5
SP14	MS_CLK	XD_D6
SP15	SD_WP	XD_D7

Share Pin









Del Entry audio circuit

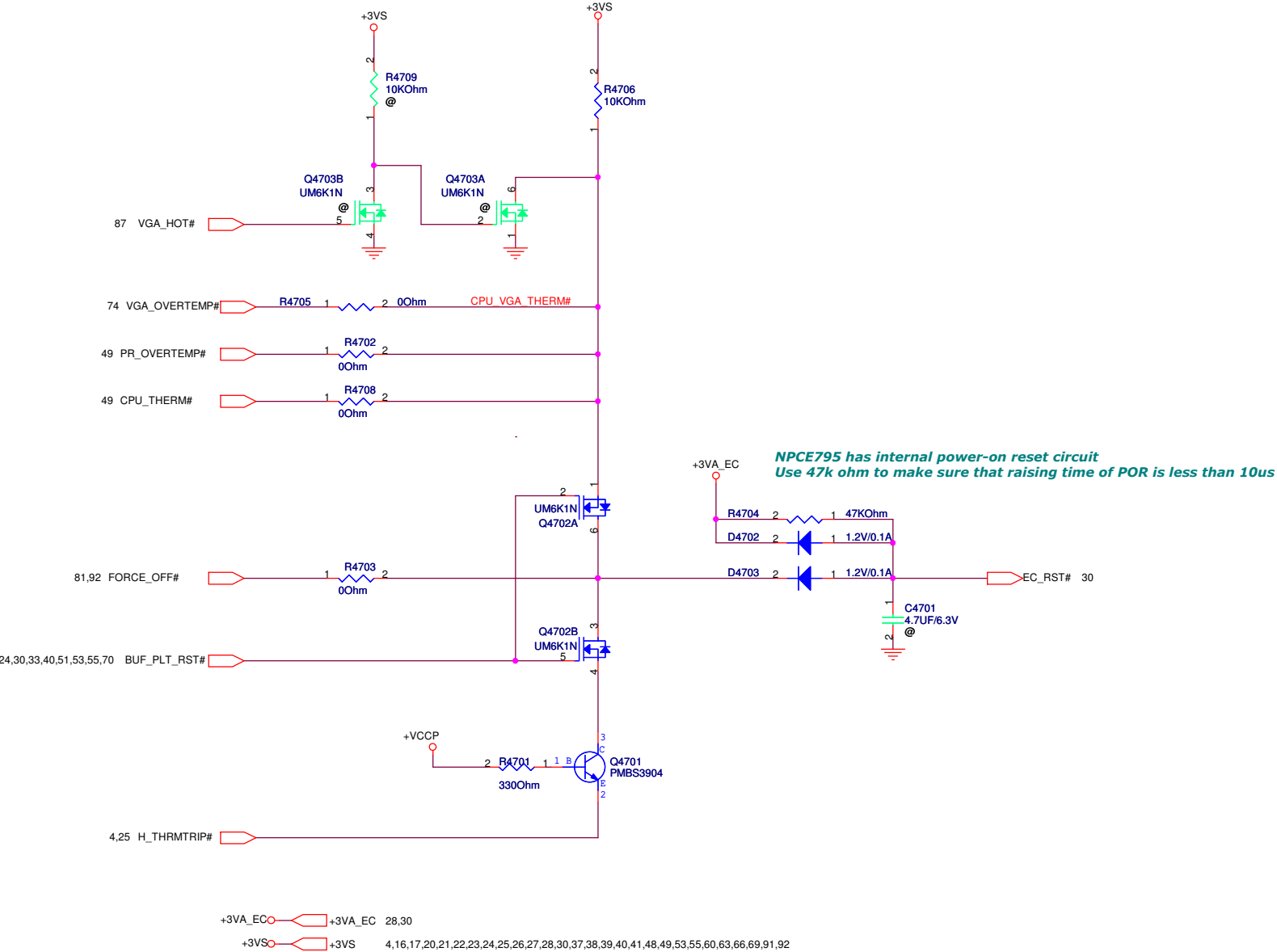
SR-8  
0121-11



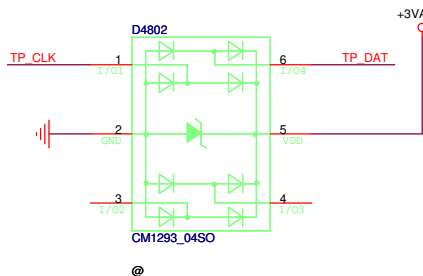
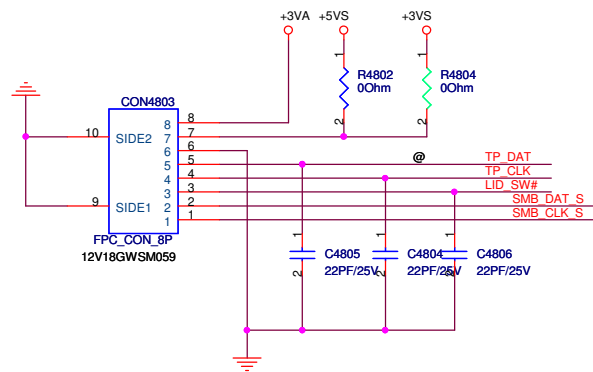
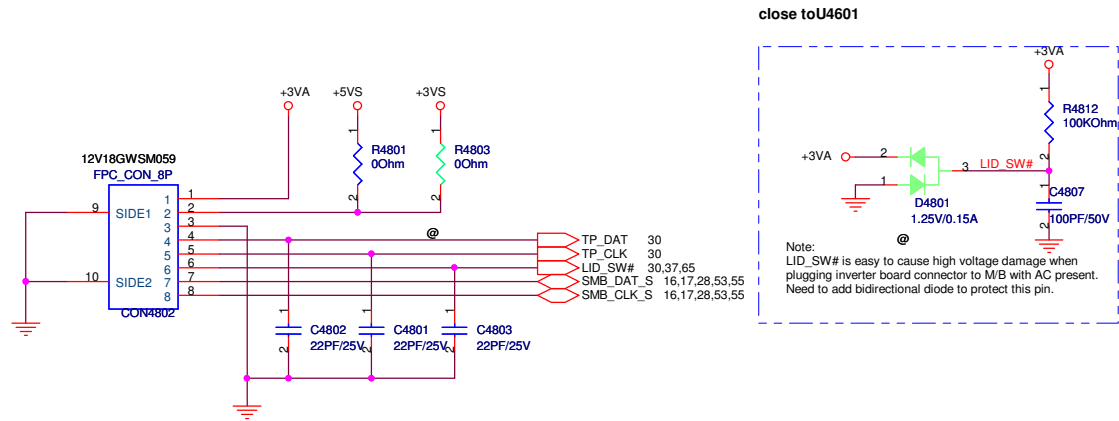
Del Entry audio circuit

SR-8  
0121-11

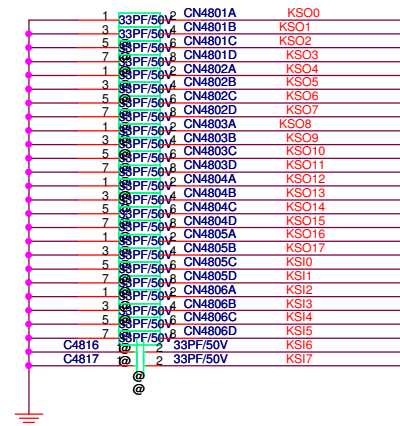
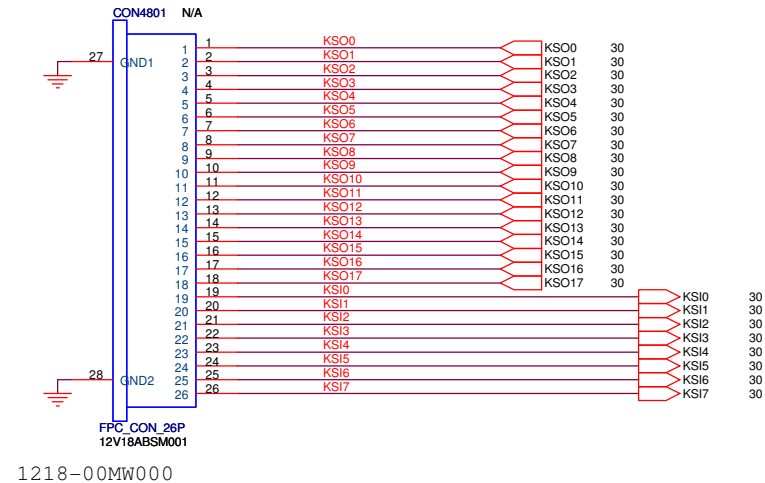
Thermal Policy



# Touch Pad Button/ Hall Sensor



# Keyboard



PEGATRON

Title : KBI/TP/FLASH

BU1-RD Div.1-HW RD Dept.1

Engineer: Wing\_Cheng

Size

Project Name

Custom

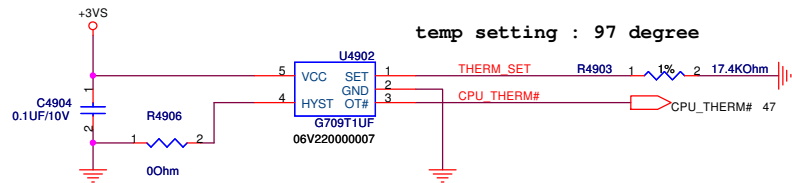
BA52HR/CR

Date: Friday, February 03, 2012

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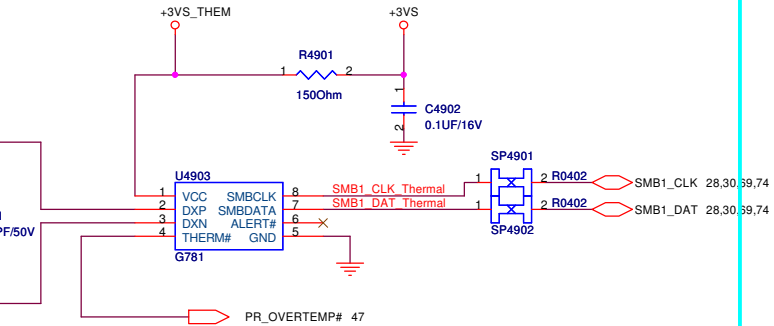
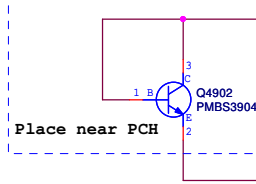
Rev 1.0

## U5001 Close to CPU



## Plam Rest Thermal Sensor

**PHILIP PMBS3904**  
Place in the center of Plamrest.



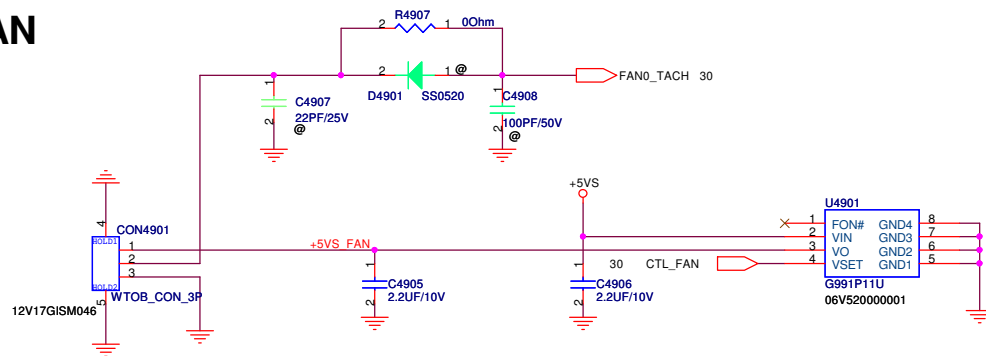
**U4903 under palmrest**

SMBUS addr=1001100x (98)

U4903: Remote(Local) thermal sensor,use remote mode.

R1.2-10

## FAN



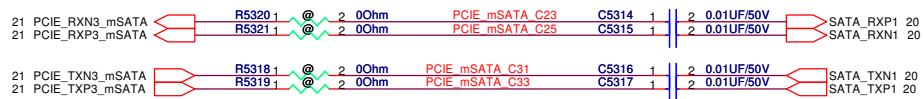






<b>PEGATRON</b>		Title : <b>PCIE NEW CARD</b>	
BU1-RD Div.1-HW RD Dept.1		Engineer: <b>Wing_Cheng</b>	
Size Custom	Project Name <b>BA52HR/CR</b>		Rev 1.0
Date: <b>Friday, February 03, 2012</b>		Sheet	52 of 77

Select PCIE or mSATA IF select mSATA(only +3VAUX)



BU1-RD Div.1-HW RD Dept.1

**Engineer:**

Size	
------	--

Project Name	
--------------	--

BA52HR/CR

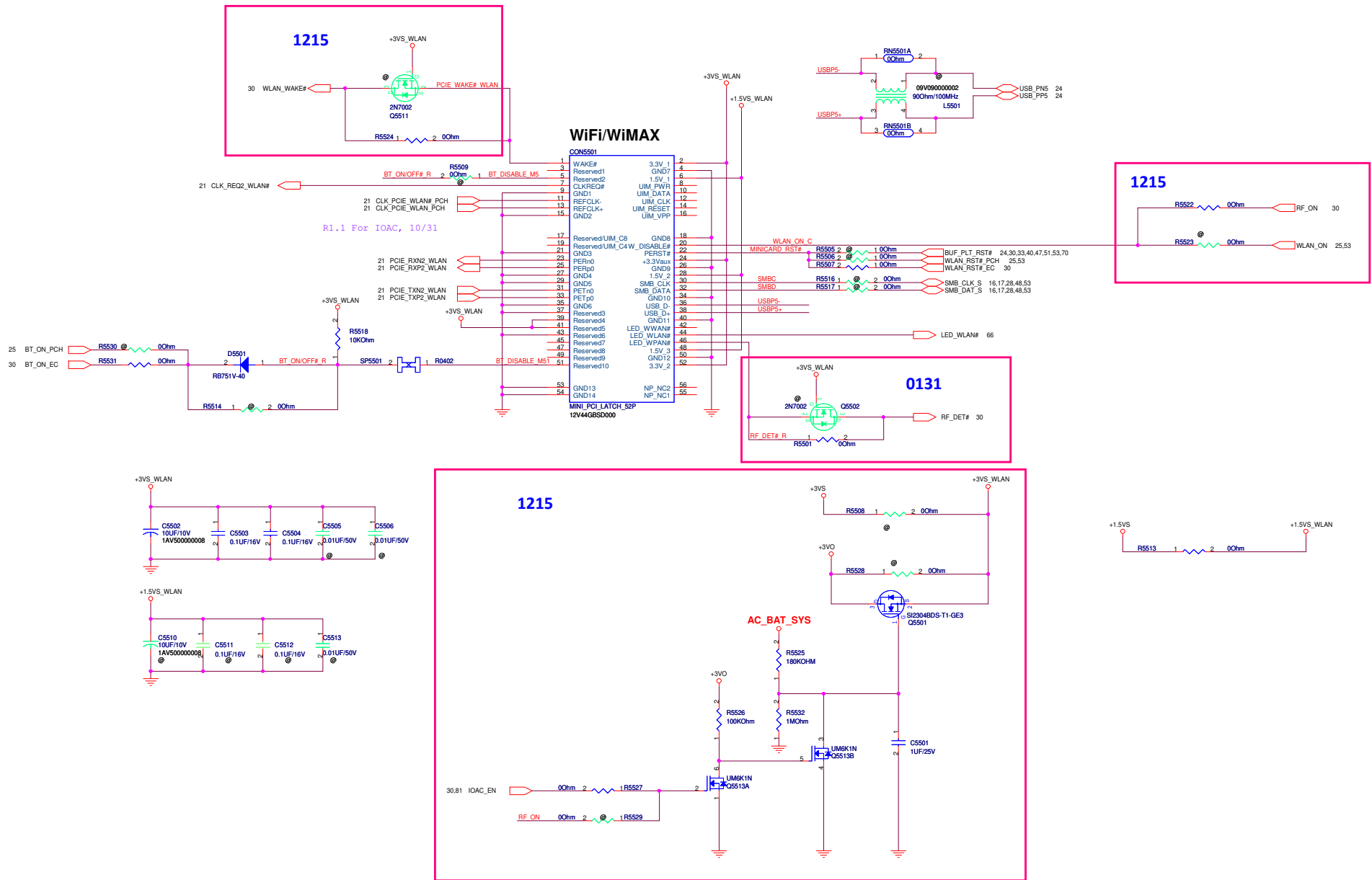
	Rev
--	-----

Date: Friday, February 03, 2012

Sheet 53 of 77

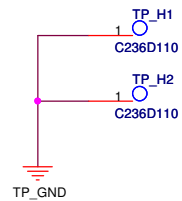


<b>PEGATRON</b>		<b>Title :</b> MINICARD (WUSB /UPCONVERT)	
BU1-RD Div.1+HW RD Dept.1		<b>Engineer:</b> <i>Wing_Cheng</i>	
Size Custom	Project Name <b>BA52HR/CR</b>		Rev 1.0
Date: Friday, February 03, 2012		Sheet	54 of 77

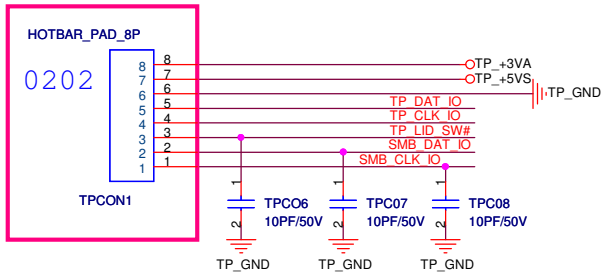
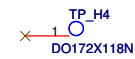
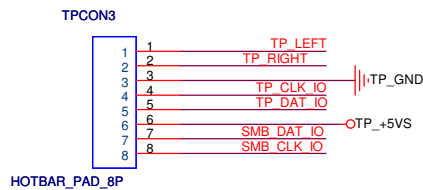
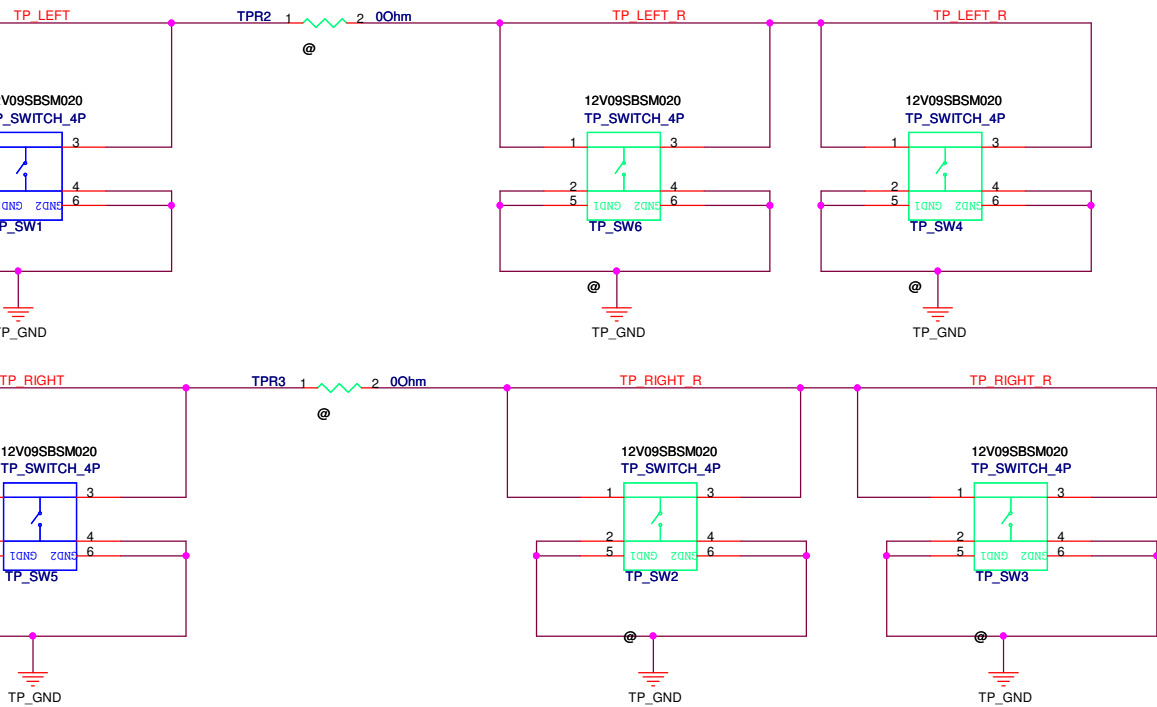
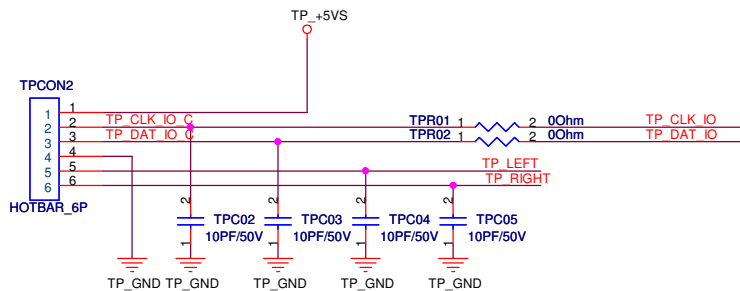


Screw M x 2

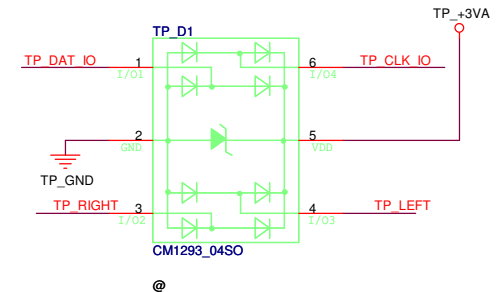
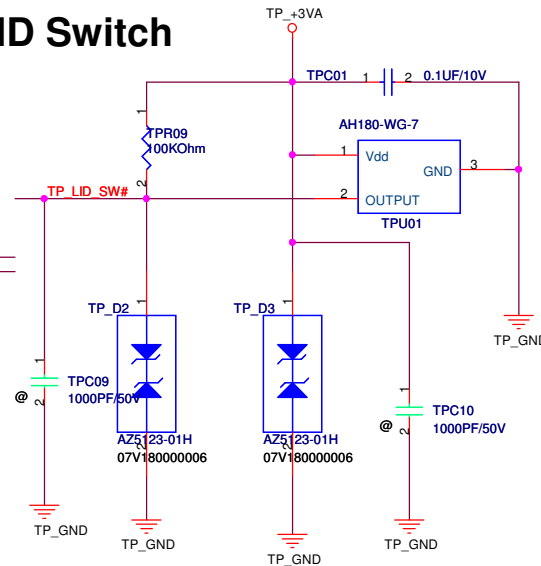
Fix Hole J x 1



Fix Hole K x 1

Touch Pad  
WIN8Touch Pad  
WIN7

LID Switch

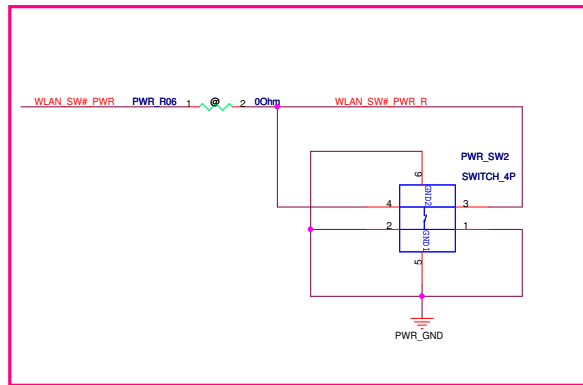
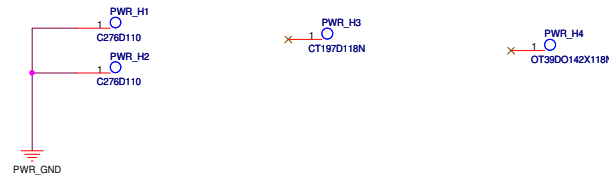


PEGATRON			Title :TP_M
BG1-HW RD Div.2-NB RD Dept.5			Engineer: Wing_Cheng
Size B	Project Name BA52HR/CR	Rev 1.0	
Date: Friday, February 03, 2012	Sheet	56	of 77

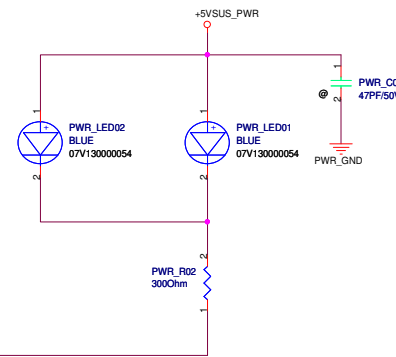
Screw G x 2

Fix Hole H x 1

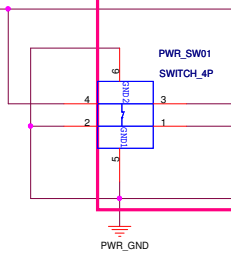
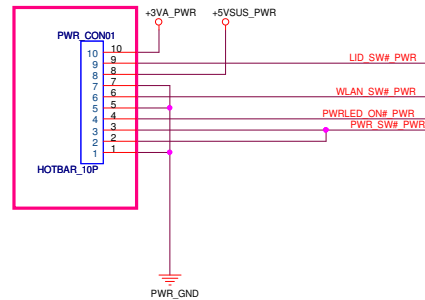
Fix Hole I x 1



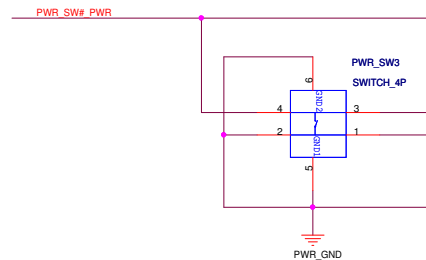
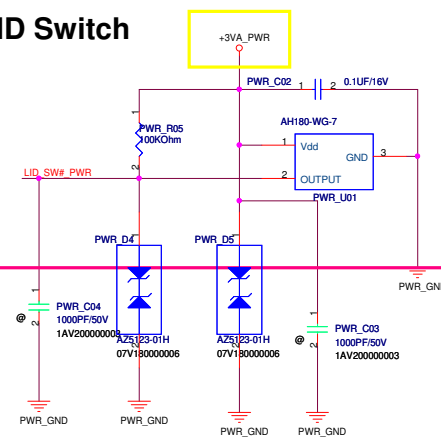
POWER Button LED

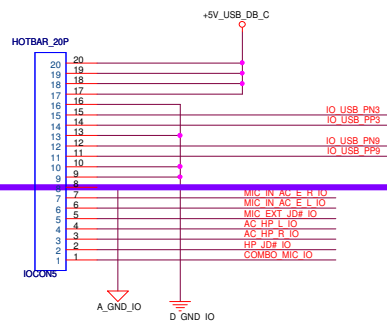


R1.1 reverse PWR\_CON01 and change pin 1~4 pin define 1024



LID Switch

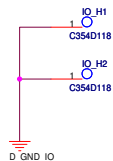




D\_GND\_IO Moat

A\_GND\_IO

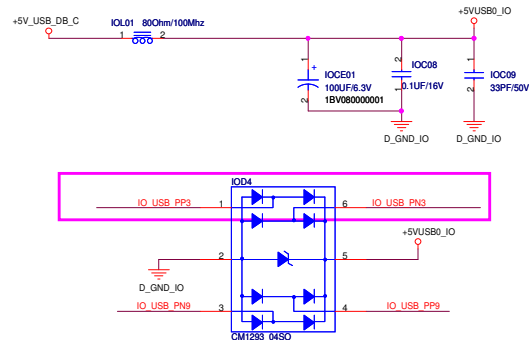
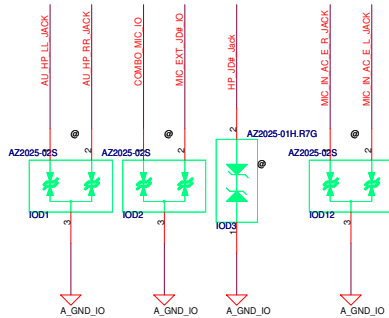
Screw L x 2



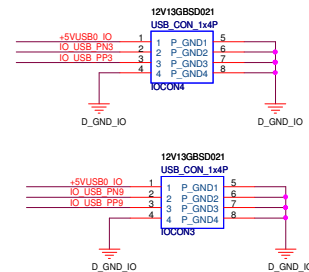
Fix Hole E x 1



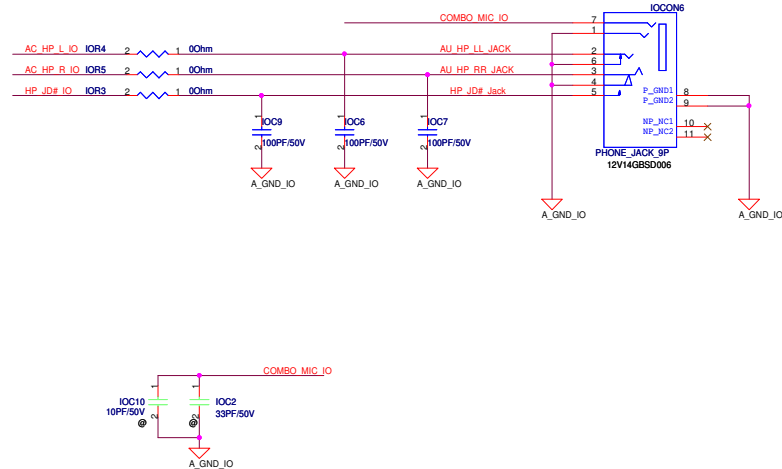
Fix Hole F x 1



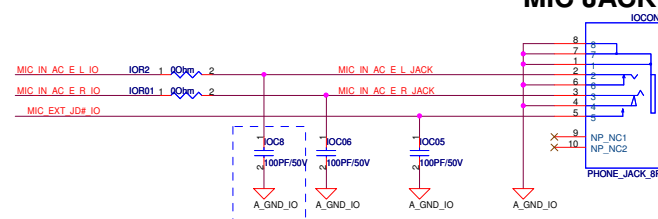
## USB 2.0



## Headphone & MIC combo Jack

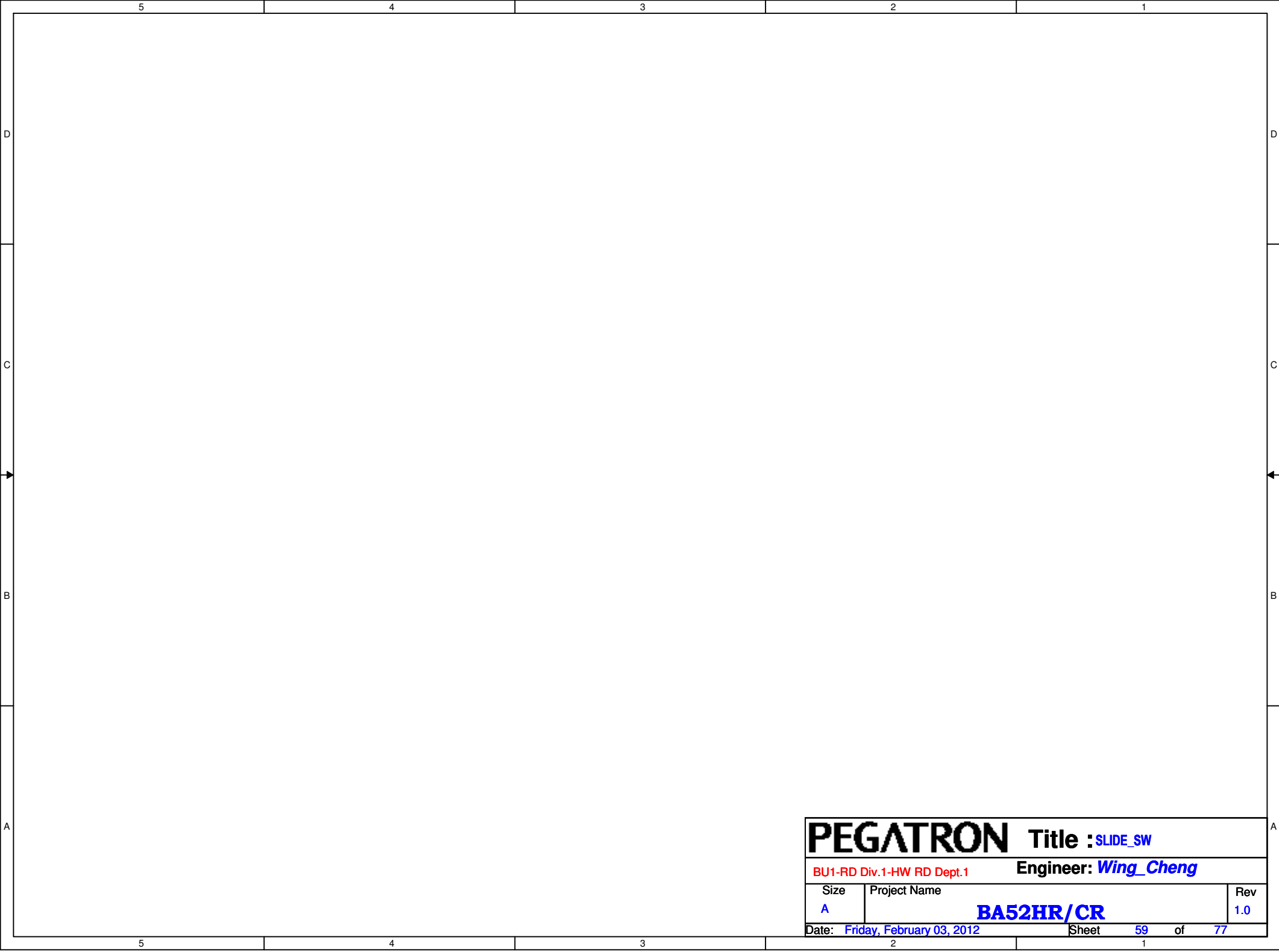


## MIC JACK



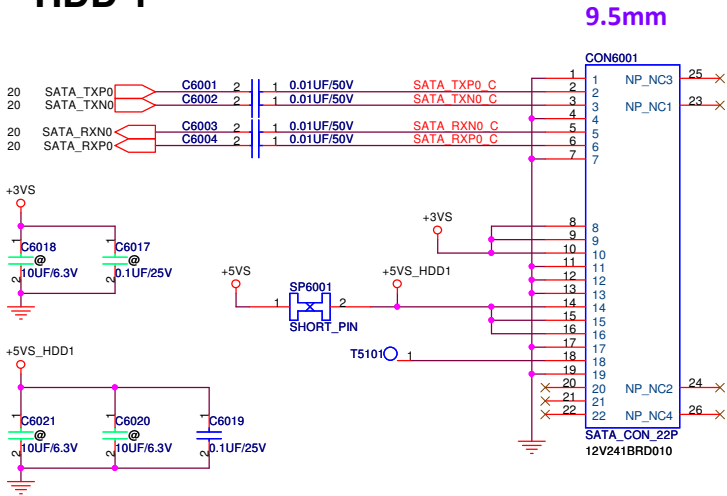
R1.1 Add 2nd MIC schematic 0804

PEGATRON Title : 0			
BG1-NB1-HW-NB5		Engineer: Wing Cheng	
Size	Project Name	BA52HR/CR	
C	Date: Friday, February 03, 2012	Sheet	58 of 77
		Rev	1.0

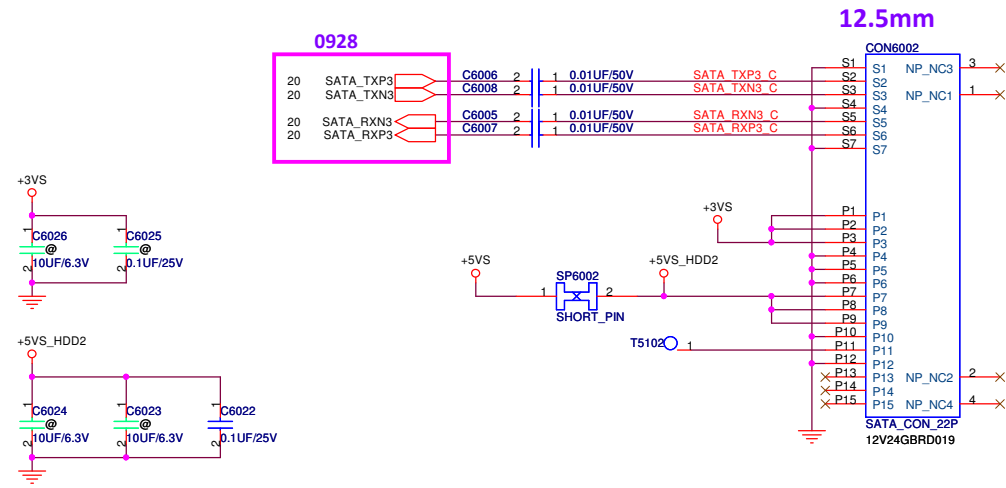


PEGATRON			Title : SLIDE_SW		
BU1-RD Div.1-HW RD Dept.1			Engineer: Wing_Cheng		
Size	Project Name				Rev
A	BA52HR/CR				1.0
Date: Friday, February 03, 2012			Sheet	59	of 77

## HDD 1



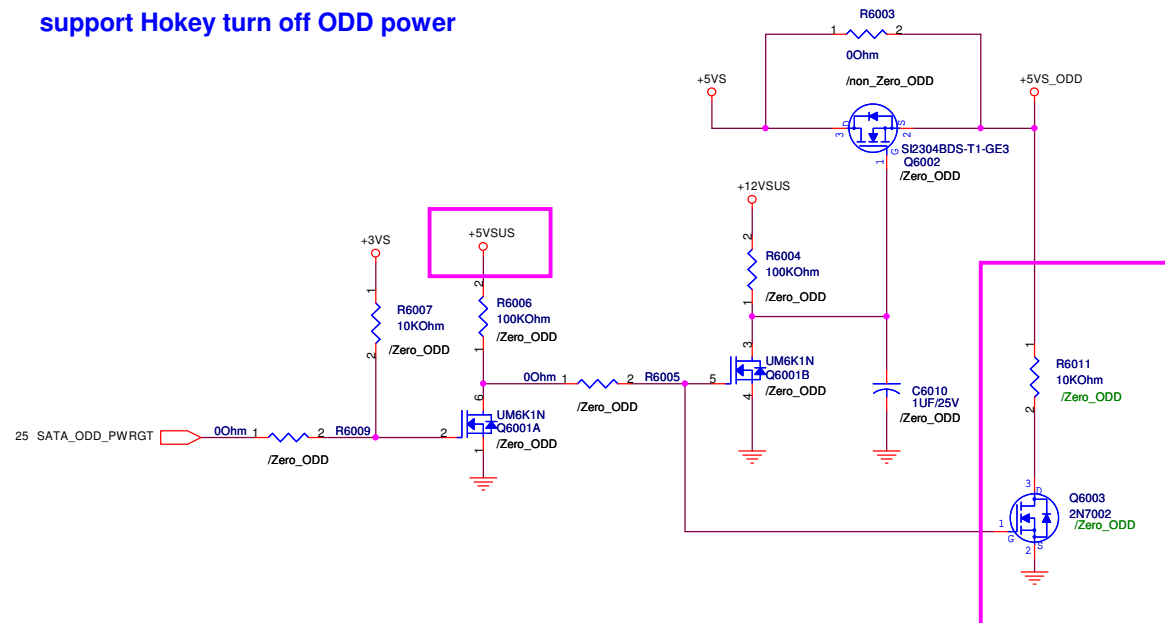
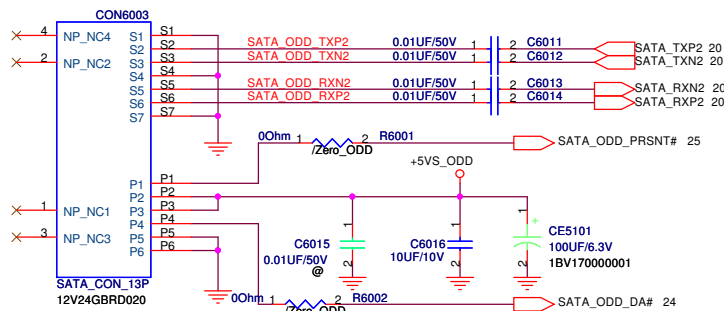
## HDD 2



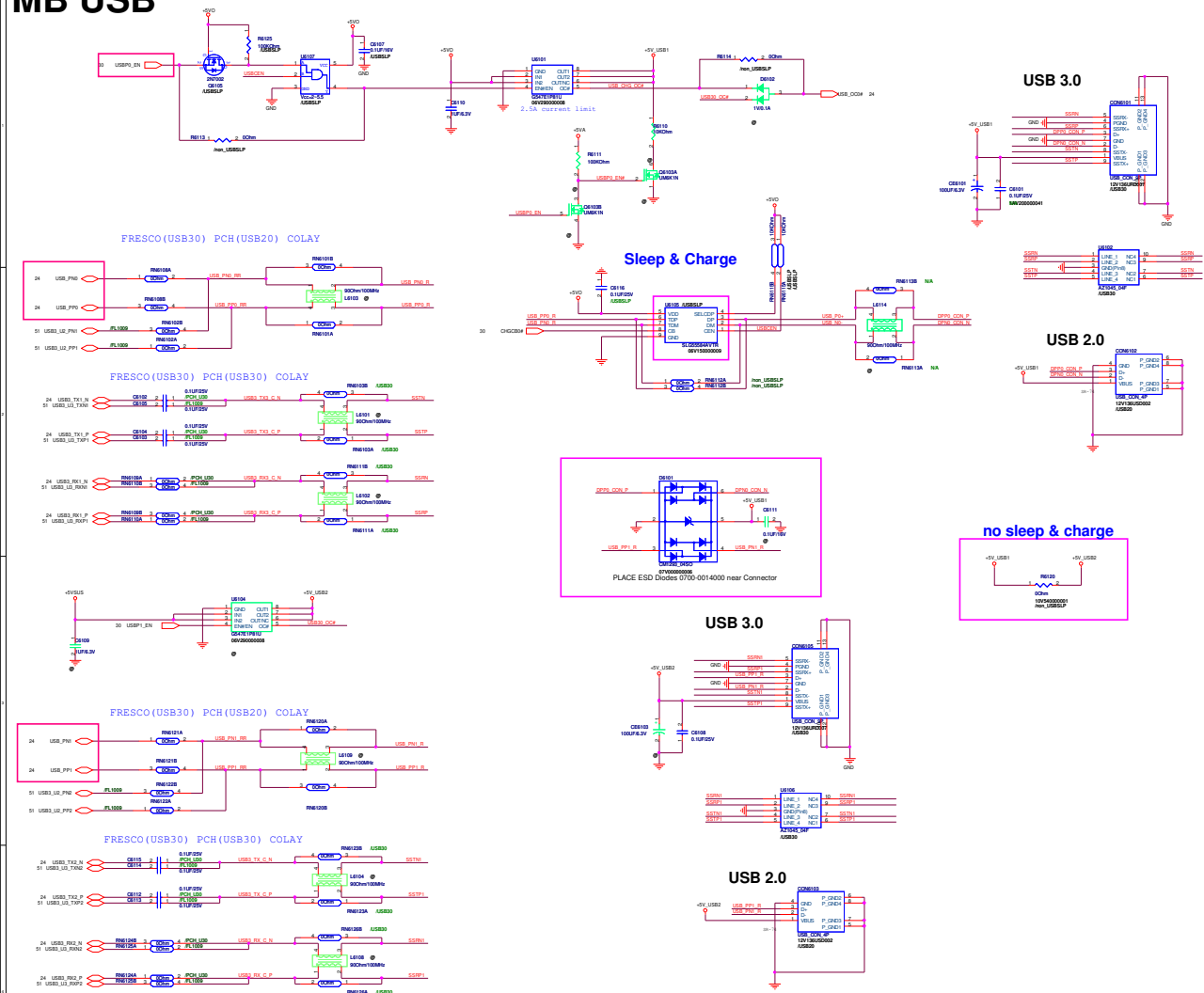
## ODD

### ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



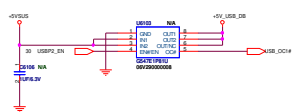
# MB USB



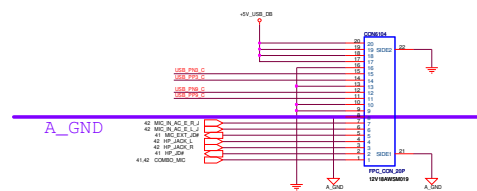
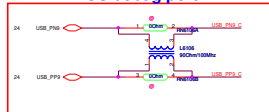
# IO Board

AUDIO BOARD/w USB2.0 x2

USB Power Switch for USB DB Main



BIOS debug port



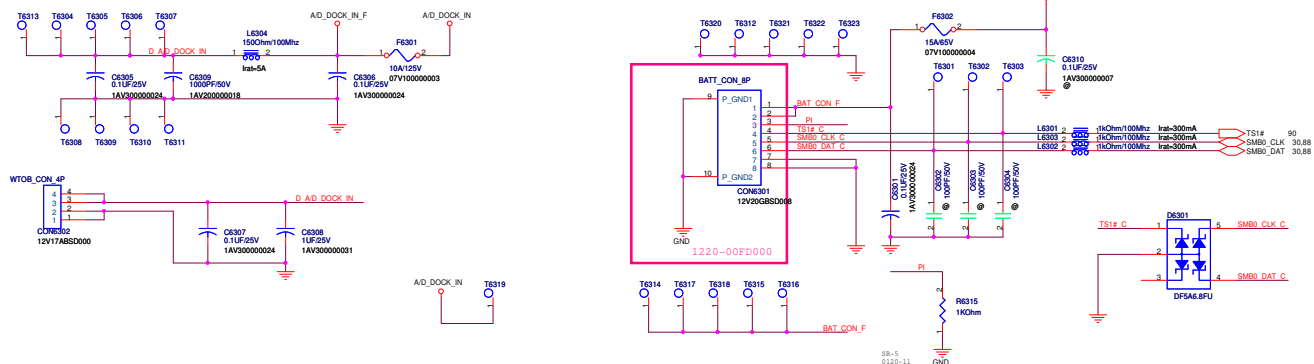


WWW.AliSaler.Com

PEGATRON		Title : Camera/ BT/ FL CONN	
BU1-RD Div.1-HW RD Dept.1		Engineer: Wing_Cheng	
Size Custom	Project Name BA52HR/CR		Rev 1.0
Date: Friday, February 03, 2012		Sheet	62 of 77

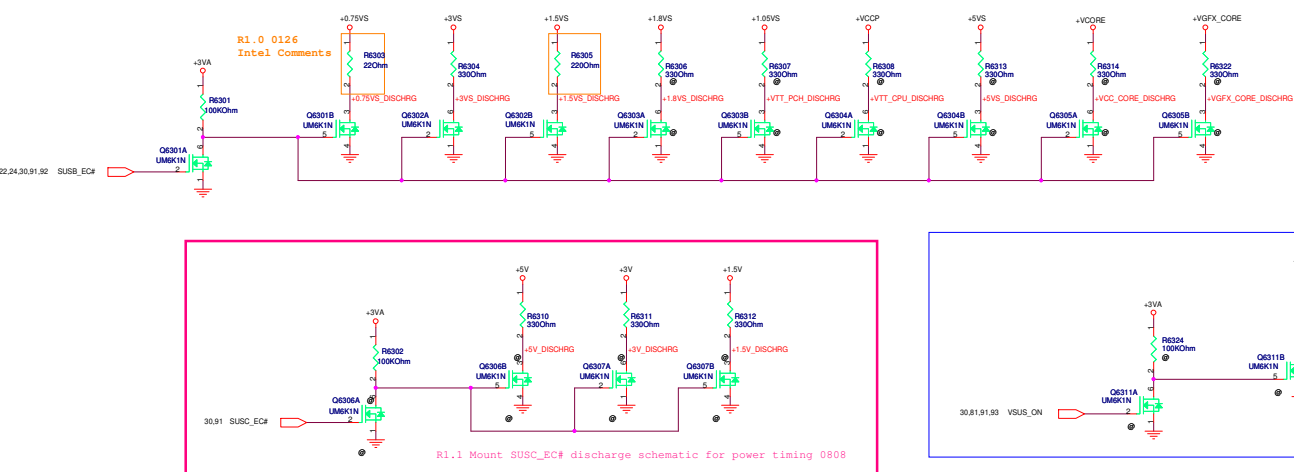
**DC IN**

## Battery Connector

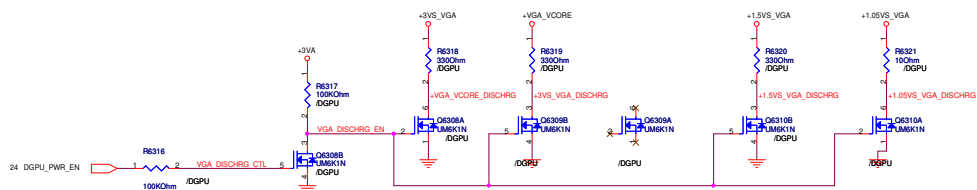


### Discharge Circuit

Frank  
0505 Follow EVEREST



### VGA Discharge Circuit



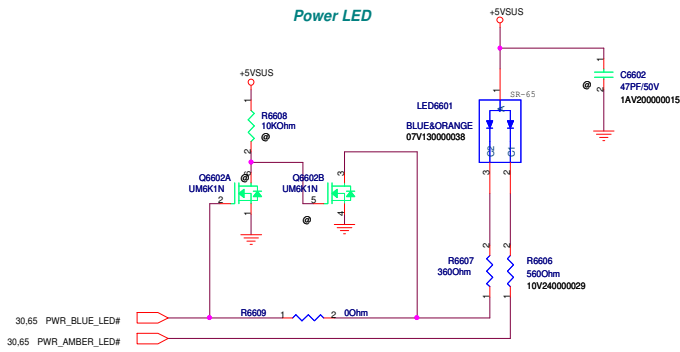
Unmount +VGA\_Vcore discharg

	5	4	3	2	1
D					
C					
B					
A					

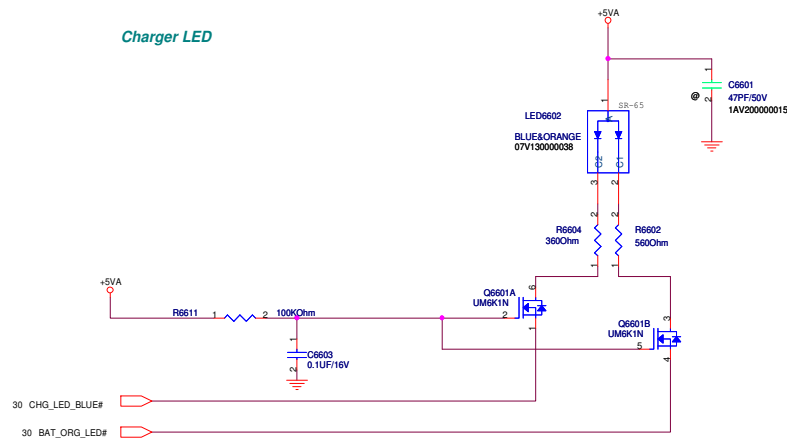
<b>PEGATRON</b>			<b>Title :USB PORTS/ eSATA</b>		
BU1-RD Div.1-HW RD Dept.1			Engineer: <i>Wing_Cheng</i>		
Size A	Project Name <b>BA52HR/CR</b>			Rev 1.0	
Date: <i>Friday, February 03, 2012</i>			Sheet	64	of 77



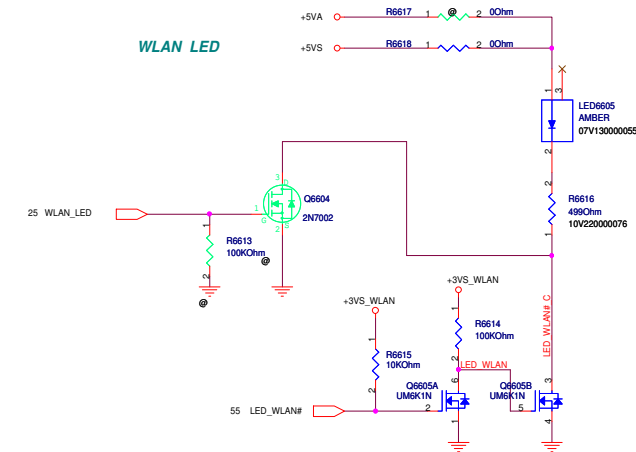
## Power LED



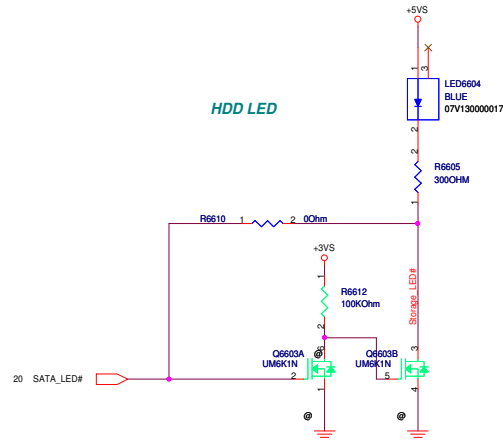
## Charger LED



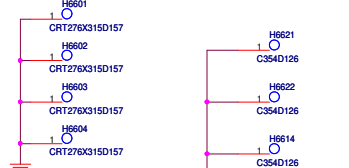
## WLAN LED



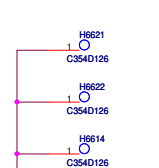
## HDD LED



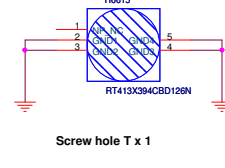
## CPU Screw B x 4



## Screw A x 4 (PTH)



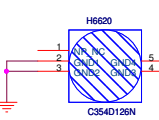
## Screw hole R x 1



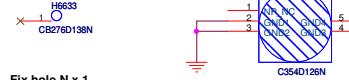
## Screw hole T x 1



## Screw A x 2 (NPTH)



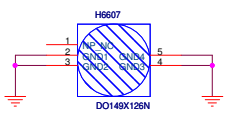
## Fix hole D x 1



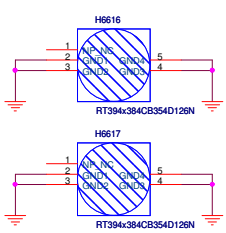
## Fix hole N x 1



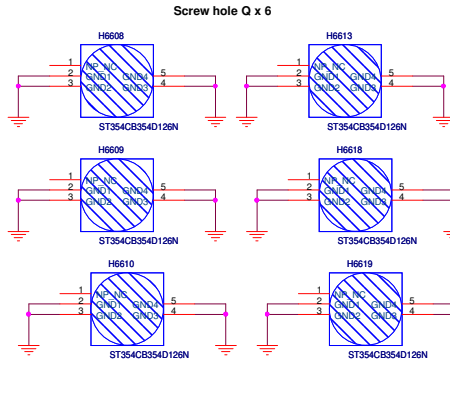
## Screw hole V x 1



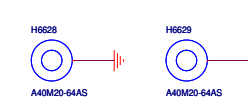
## Screw hole S x 2



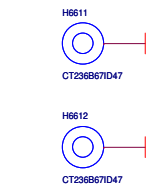
## Screw hole Q x 6



## WLAN NUT

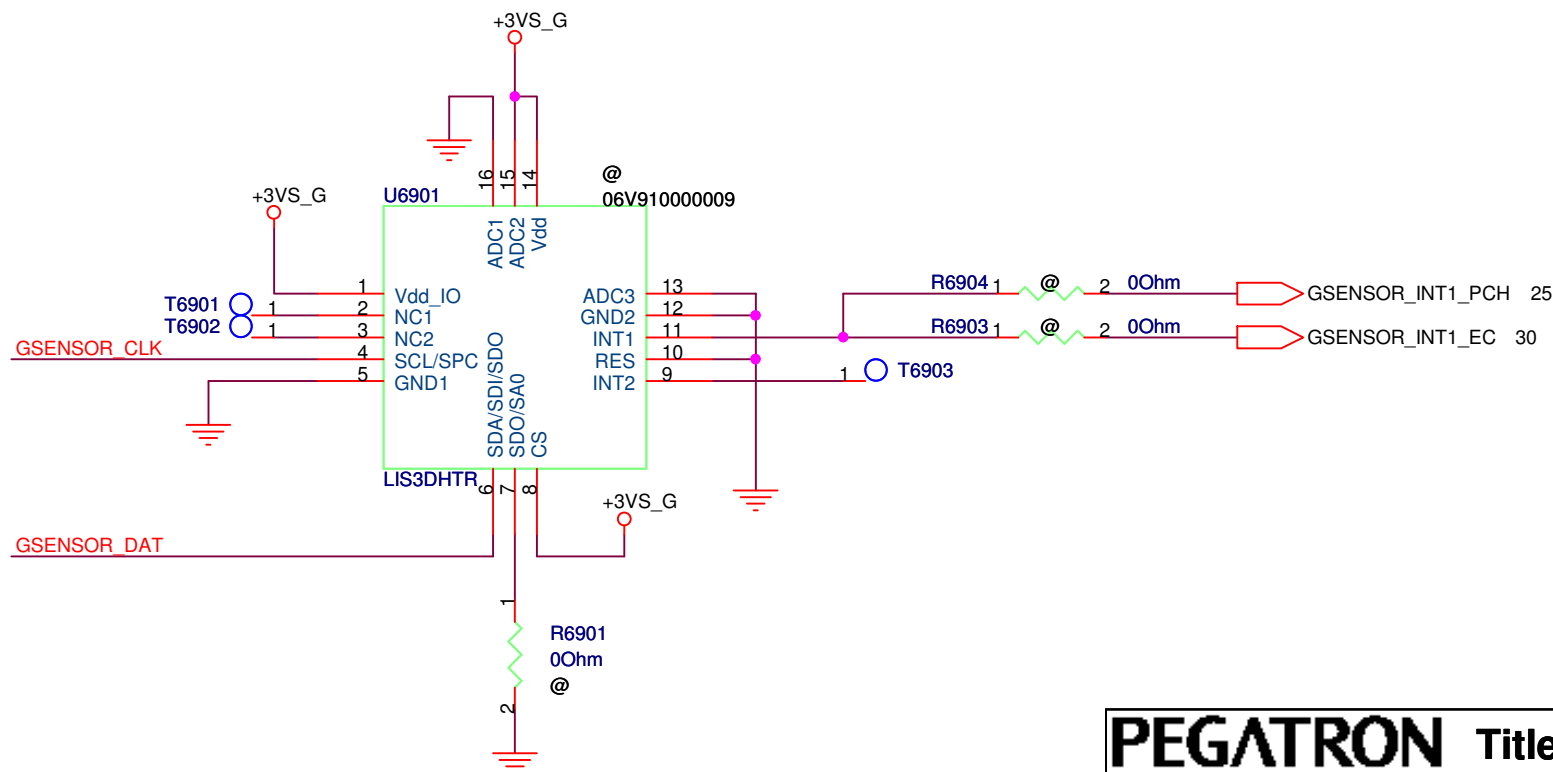
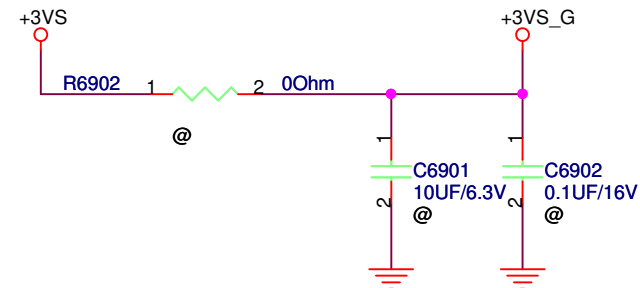
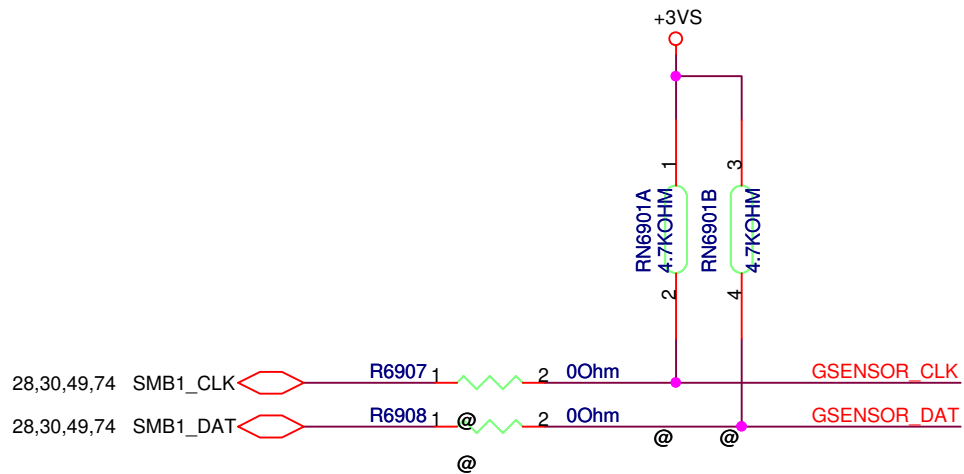


## PCH Local Side Symbol



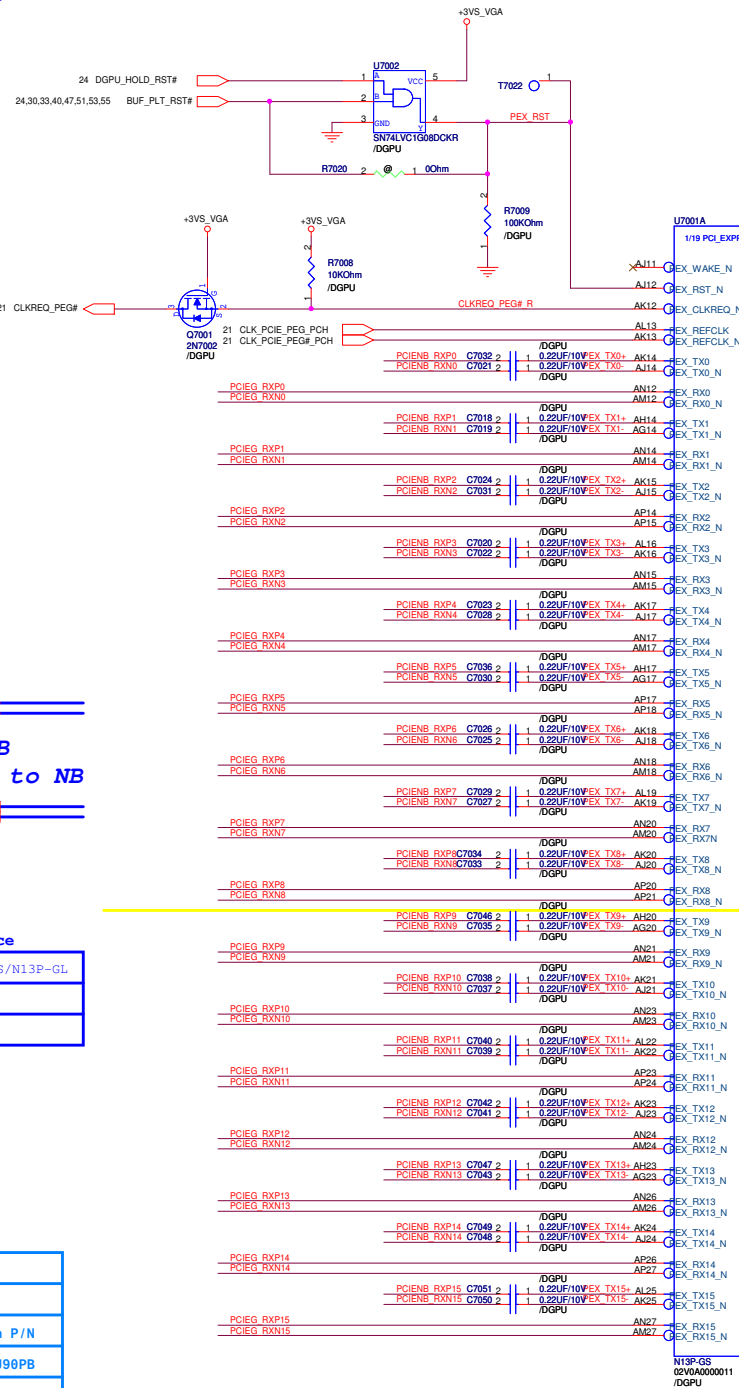






<b>PEGATRON</b>		Title : <b>G-Sensor TSH35TR</b>	
BU1-RD Div.1-HW RD Dept.1		Engineer: <b>Wing_Cheng</b>	
Size <b>A</b>	Project Name		Rev <b>1.0</b>
Date: <b>Friday, February 03, 2012</b>		Sheet <b>69</b>	of <b>77</b>

Frank  
20110513 Change N13P GPU.



PEX=> From NB  
EXP: VGA Card to NB

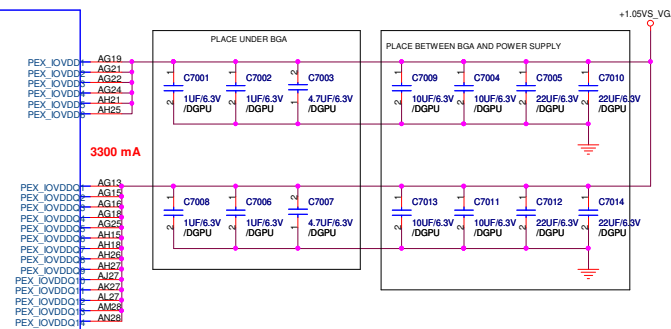
PCIe interface

	N13M-GS	N13P-GS/N13P-GL
8 Lane	V	
16 Lane		V

GPU Information		
GPU Location : U7001		
Type	Version	Pegatron P/N
N13P-GS	ES	020A-00J90PB
N13P-GL	QS	020A-00K60PB
N13M-GS	ES	020A-00J08PB

### GPU BOM Optional Definition

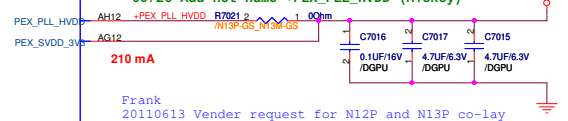
@ => Unmount.  
/DGPU => Discrete and Optimus SKU.  
/DGPU0 => Discrete SKU only.  
/OPT => Optimus SKU only.  
/N13P-GS => When N13P-GS is mounted, we need to mount this optional.  
/N13P-GL => When N13P-GL is mounted, we need to mount this optional.  
/N13P-GS\_N13M-GS => When N13P-GS or N13M-GS are mounted, we need to mount this optional.  
/N13P-GS\_N13P-GL => When N13P-GS or N13P-GL are mounted, we need to mount this optional.



PEX\_PLL\_HVDD

N13P-GL	N13P-GS/N13M-GS
NC	PEX_PLL_HVDD (3.3V)

09/26 Add net name +PEX\_PLL\_HVDD (Mickey)

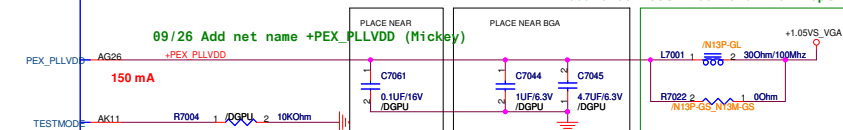


Frank  
20110613 Vender request for N12P and N13P co-lay



09/26 Change R7007 optional from @ to /DGPU (Follow NV reference schematics) (Mickey)  
09/29 Change R7007 optional from /DGPU to @ (NV FAE confirmed) (Mickey)

09/26 Correct L7001 and R7022 optional (Mickey)

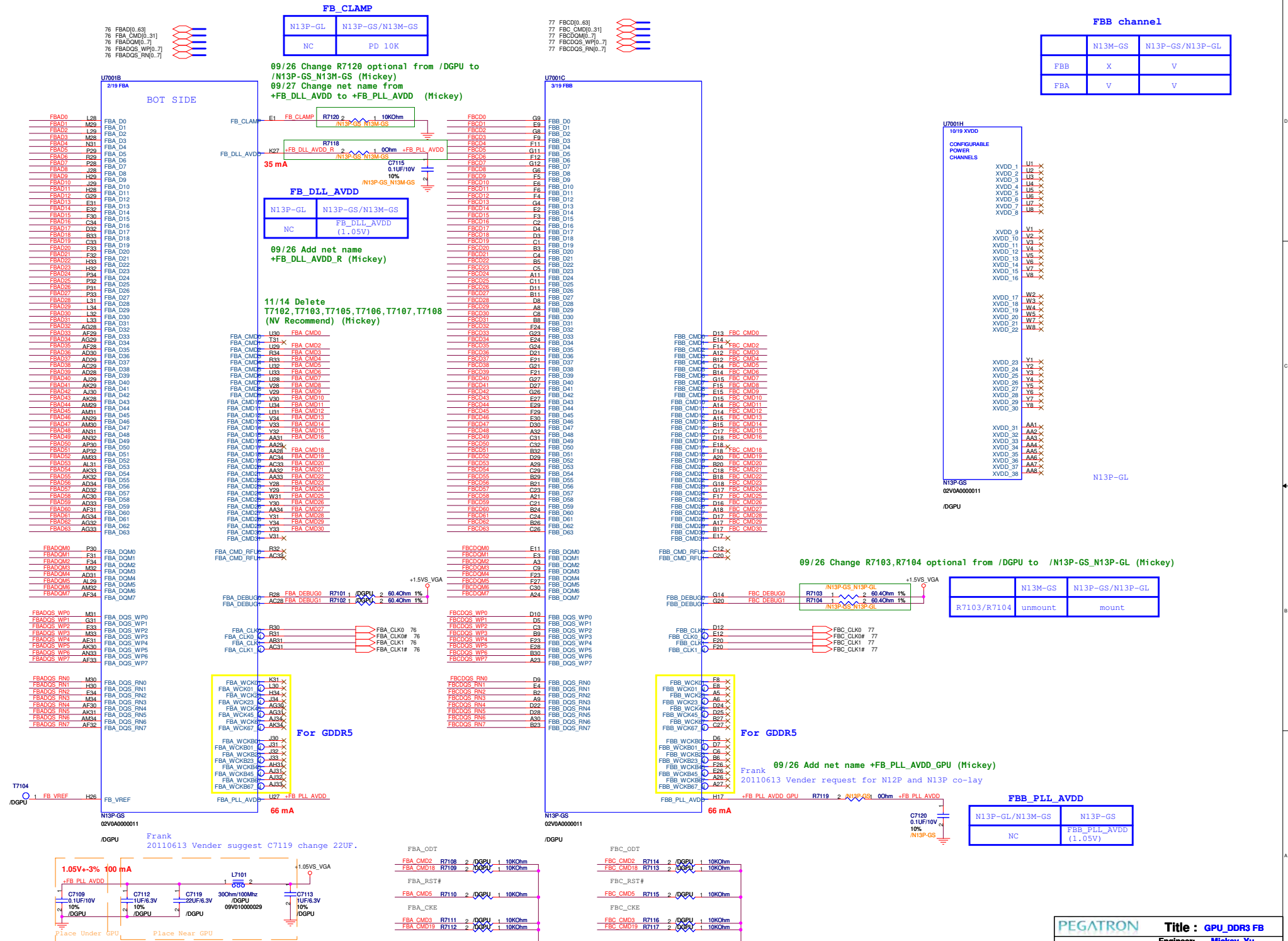


09/26 Add net name +PEX\_PLLVDD (Mickey)

PEX\_PLLVDD

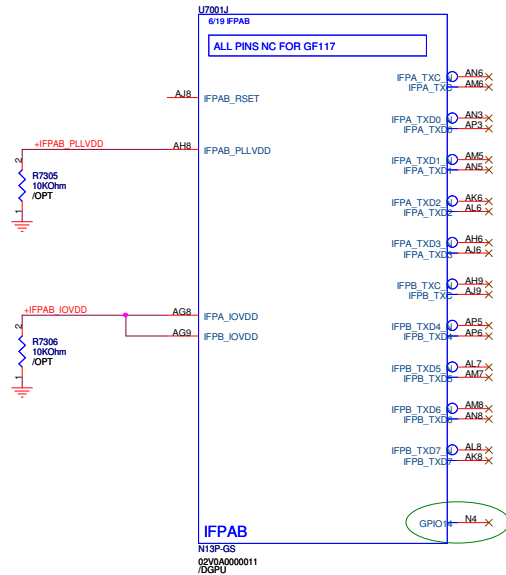
N13P-GL	N13P-GS/N13M-GS
L7001	R7022

PEGATRON		Title : GPU_PEG*16	
PEGATRON COMPUTER INC		Engineer: Mickey_Yu	
Size C	Project Name	VA79_N13P-GDDR3	Rev 1.0
Date: Friday, February 03, 2012		Sheet 70 of 99	



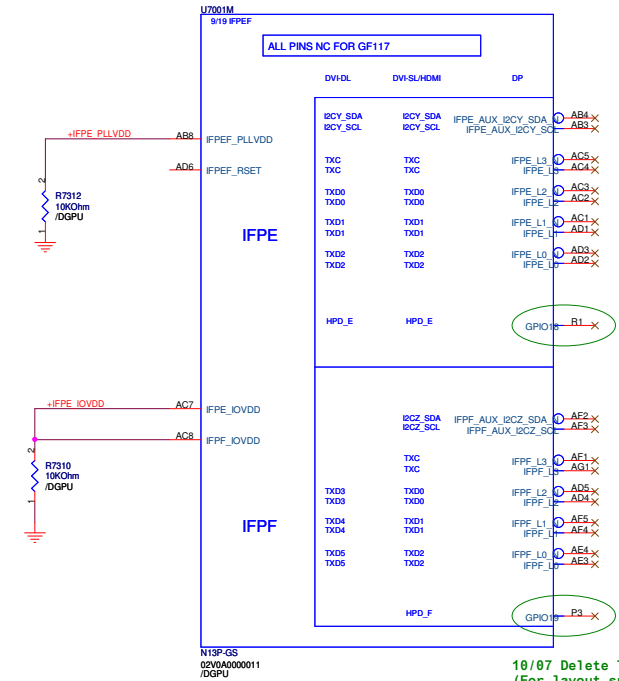
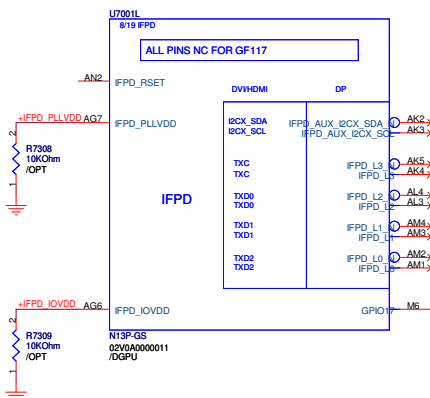
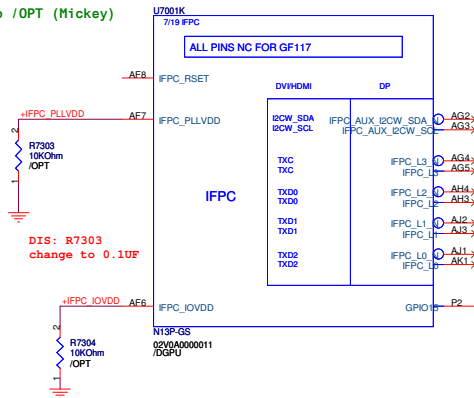


## LVDS



## HDMI

09/27 Change R7302 optional from /DGPU to /N13P-GS\_N13P-GL (Mickey)  
 09/26 Change R7303,R7304 optional from /DGPU\_ONLY to /OPT (Mickey)  
 09/26 Change C7307-7315,L7303,L7305 optional from /DGPU\_ONLY to /DGPUO (Mickey)



## GPIO

	N13M-GS	N13P-GS/N13P-GL
GPIO14	X	V
GPIO15	X	V
GPIO16	X	V
GPIO17	X	V
GPIO18	X	V
GPIO19	X	V

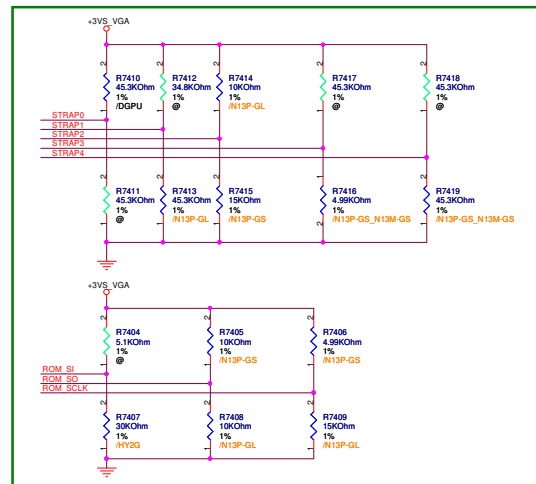
## IFPX channel

	N13M-GS	N13P-GS/N13P-GL
IFPA/B	X	V
IFPC	X	V
IFPD	X	V
IFPE/F	X	V

LVDS

HDMI

EDP



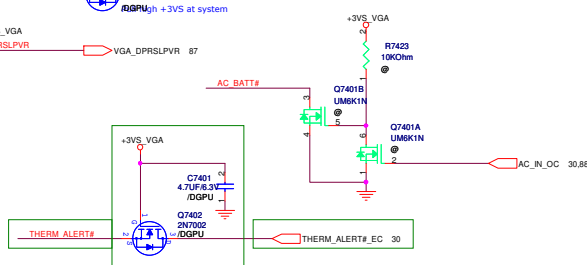
STRAP2--GPU TYPE		
N13M-GS	N13P-GL	N13P-GS

N13P-GL Q5			
DEVICE ID	0xDe9		
STRAP0	45K	PU	
STRAP1	45K	PD	
STRAP2	10K	PU	R7414
STRAP3	NC		
STRAP4	NC		
ROM_SCLK	15K	PD	
ROM_SI	Hynix 128Mx16	35K	PD
	Hynix 64Mx16	15K	PD R7487
ROM_SO	10K	PD	

ROM_SI	Hynix 128Mx16	Hynix 64Mx16
R7407	35K	15K

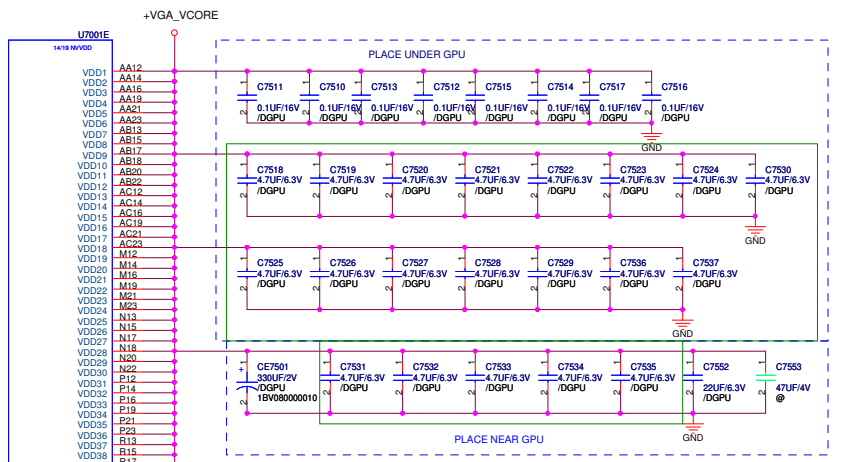


N13P-GT ES2/QS			
DEVICE ID	0xFD1		
STRAP0	45K	PU	
STRAP1	35K	PD	
STRAP2	10K	PD	
STRAP3	5K	PD	
STRAP4	10K	PD	
ROM_SCLK	5K	PU	
ROM_SI	Hynix 128Mx16	35K	PD
	Hynix 64Mx16	15K	PD R7487
ROM_SO	10K	PU	

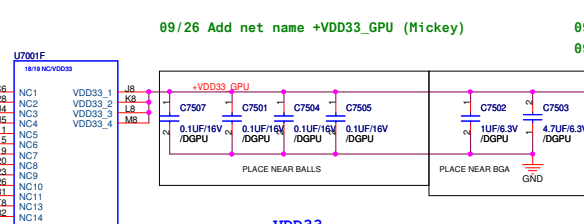
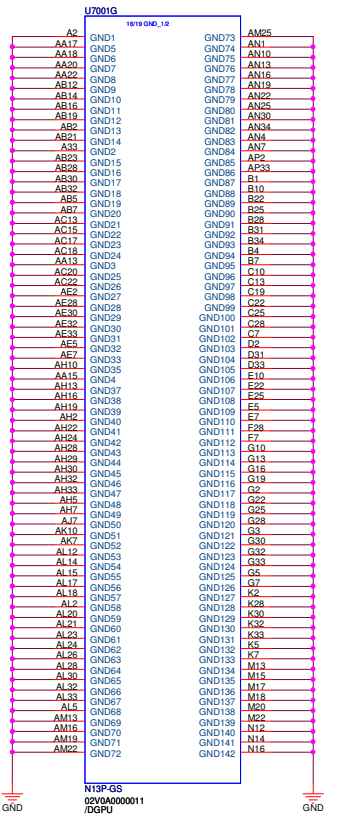
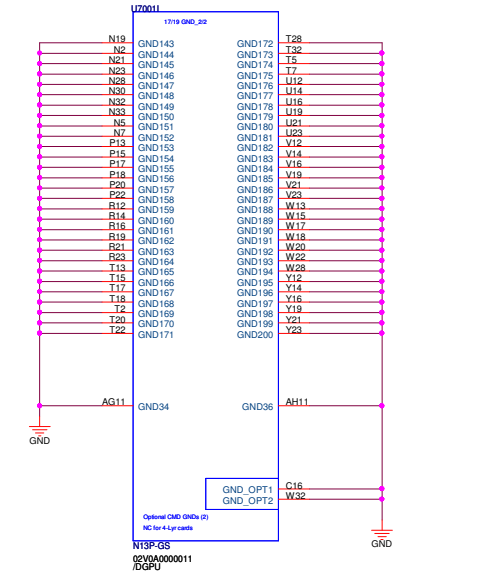


GPIO 8		
	N13P-GL	N13P-GS/N13M-GS
Q7403	unmount	NV suggestion mount

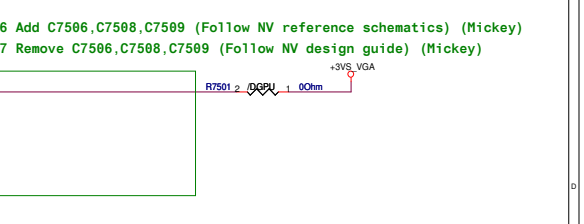
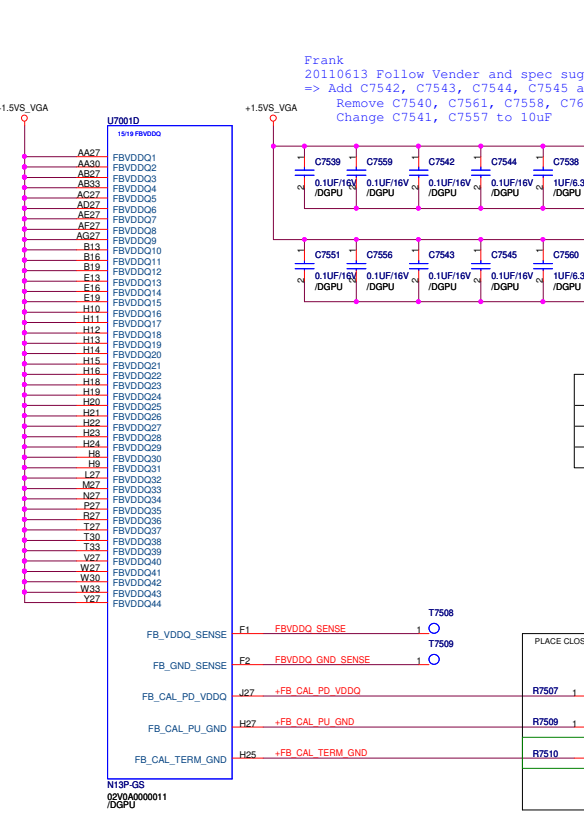
```
09/29 Change Q7401,Q7402 optional from @ to /DGPU(Mickey)
09/29 Change net name from VPS to THERM_ALERT# on Q7402.2 (Mickey)
09/29 Change net name from VPS_EC to THERM_ALERT#_EC on Q7402.3 (Mickey)
```



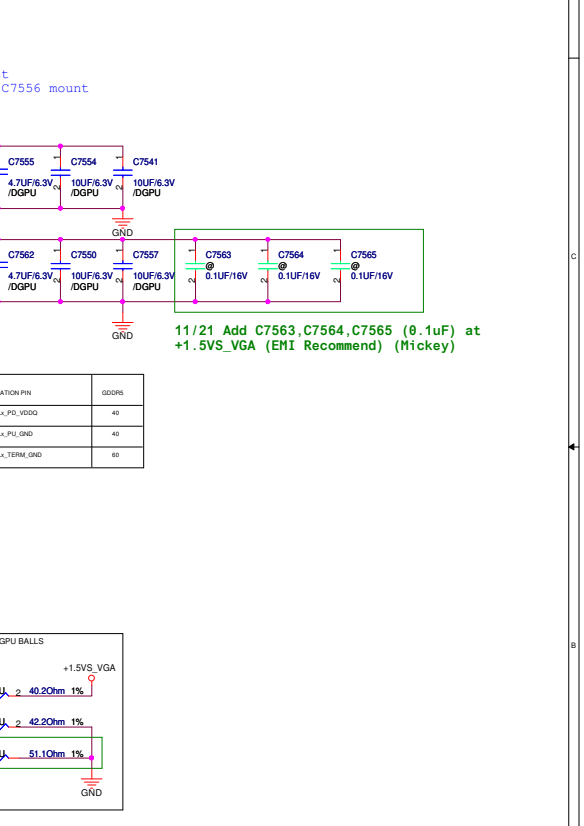
09/29 Change C7518-C7537 from 10uF to 4.7uF (Follow NV design guide) (Mickey)



VDD33	
N13P-GS	N13P-GL/N13M-GS
3V3MISC	VDD33
isolation circuitry	



VDD33	
N13P-GS	N13P-GL/N13M-GS
3V3MISC	VDD33
isolation circuitry	



check with NV==>可先不用Isolation circuitry

Frank  
20110613 Follow Vender and spec suggest  
=> Add C7542, C7543, C7544, C7545 and C7556 mount  
Remove C7540, C7561, C7558, C7649  
Change C7541, C7557 to 10uF

11/21 Add C7563,C7564,C7565 (0.1uF) at +1.5VS\_VGA (EMI Recommend) (Mickey)

09/28 Change R7510 from 60.4ohm to 51.1ohm (Follow NV design guide) (Mickey)

Frank  
20110613 Follow Vender and spec suggest=>Remove R7509 change 42.2 ohm

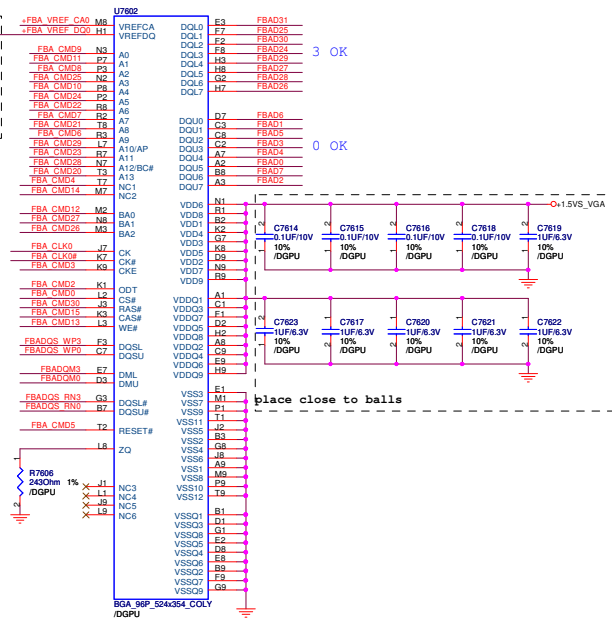
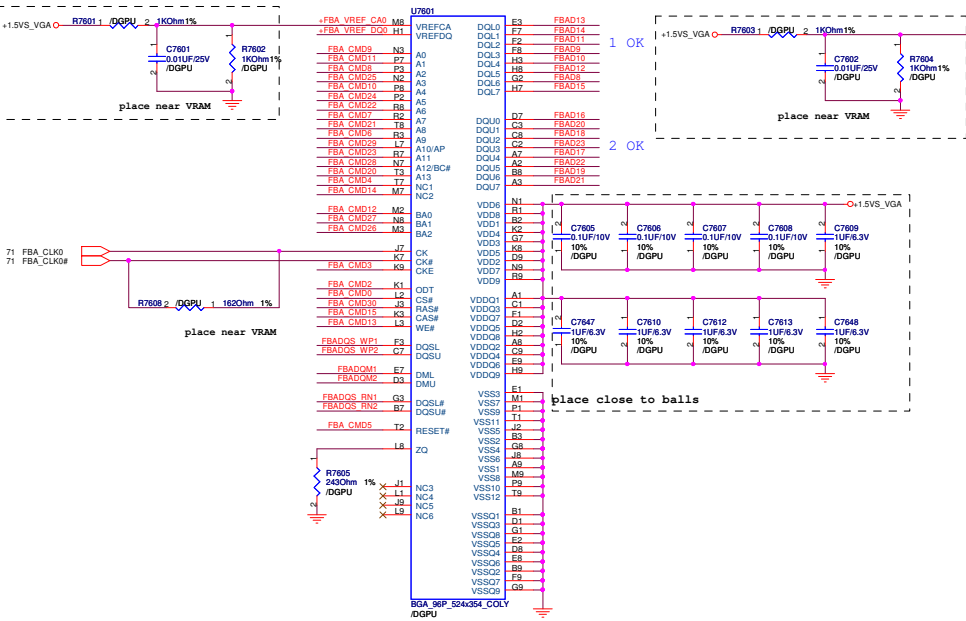
# VRAM CH A

## \*TOP SIDE\*

## \*BOT SIDE\*

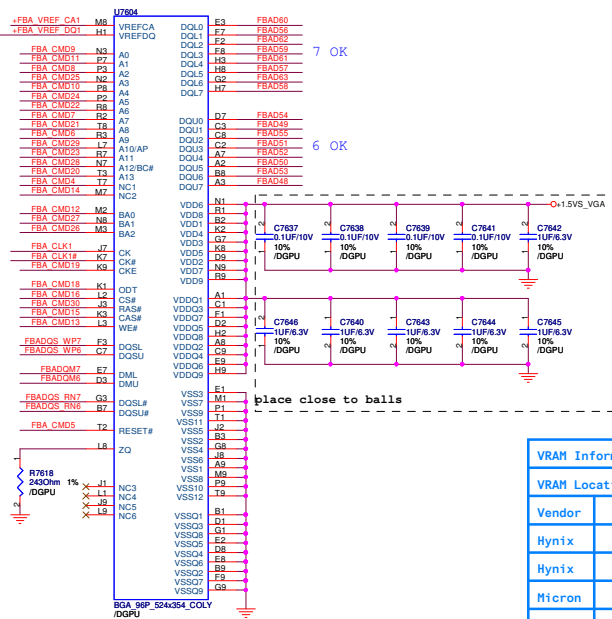
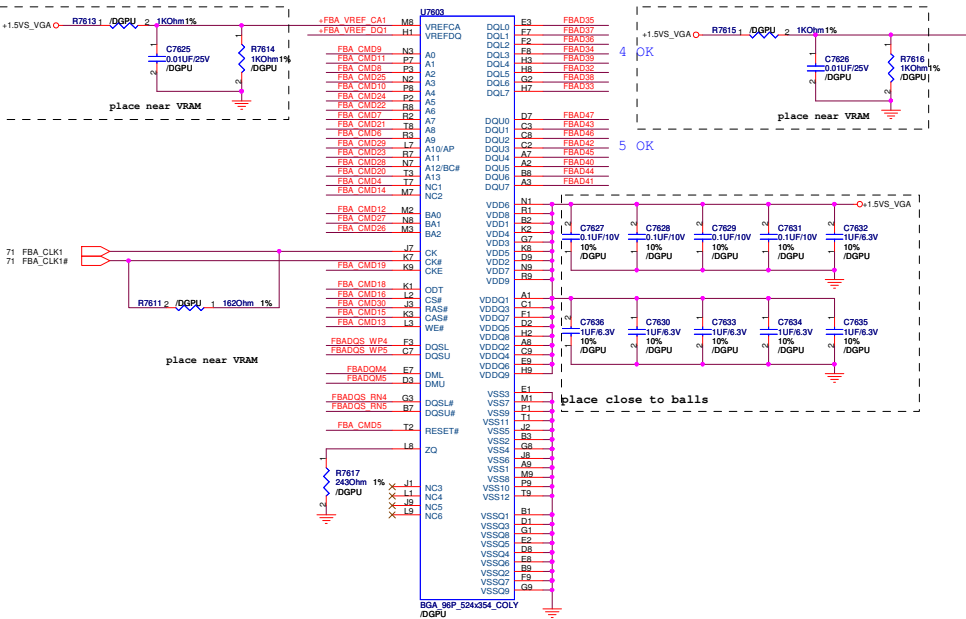
09/27 Swap VRAM data signal. (Mickey)

M13X DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16	CS0#	
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		



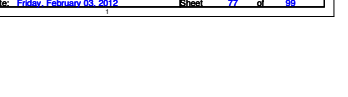
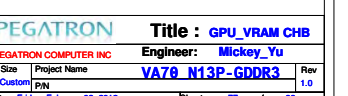
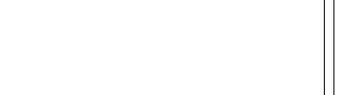
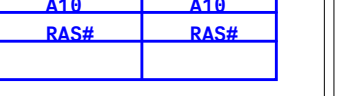
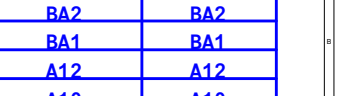
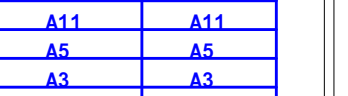
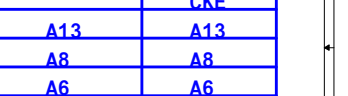
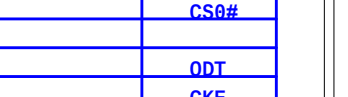
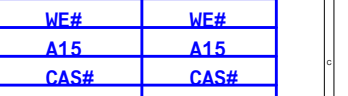
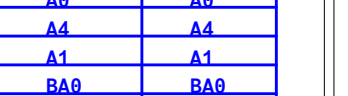
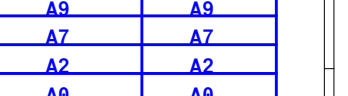
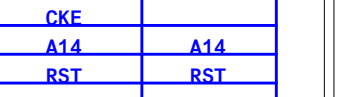
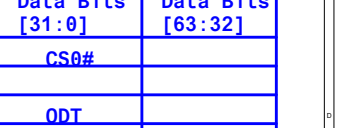
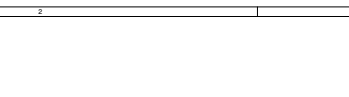
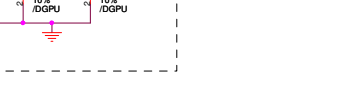
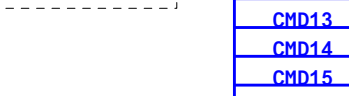
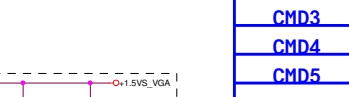
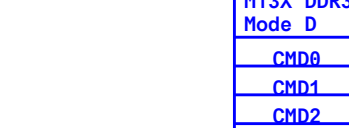
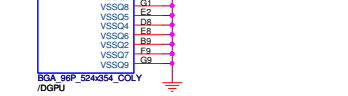
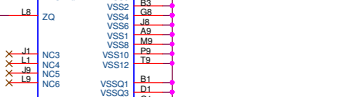
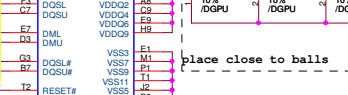
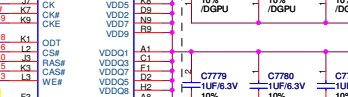
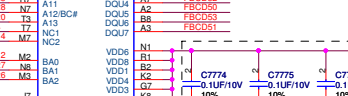
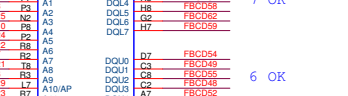
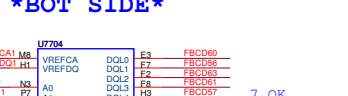
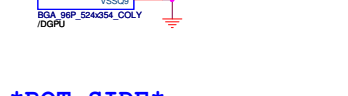
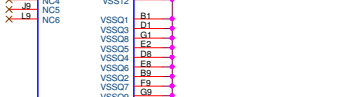
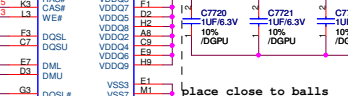
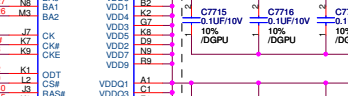
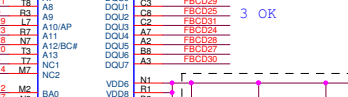
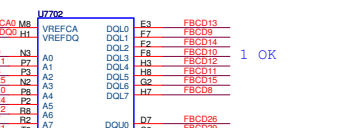
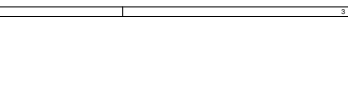
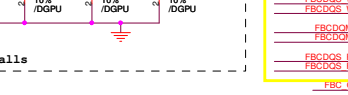
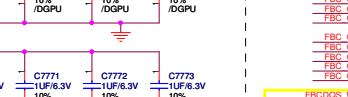
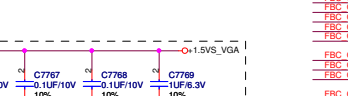
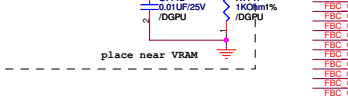
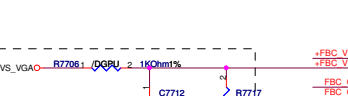
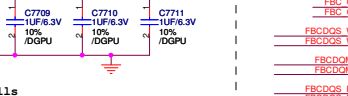
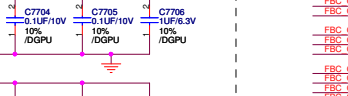
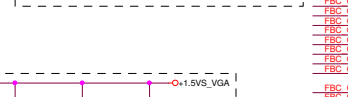
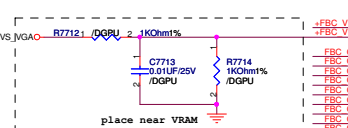
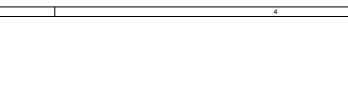
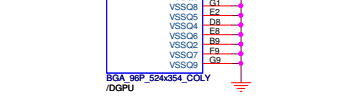
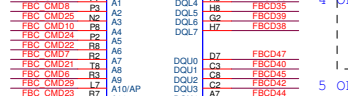
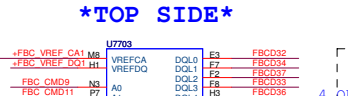
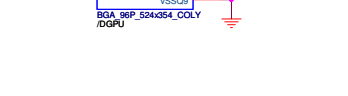
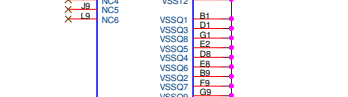
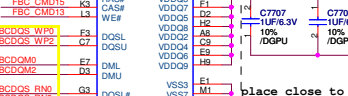
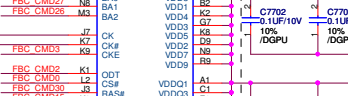
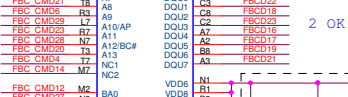
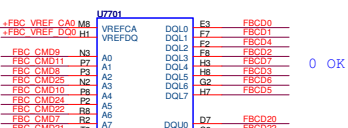
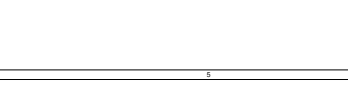
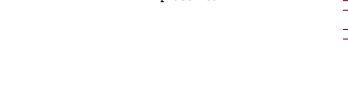
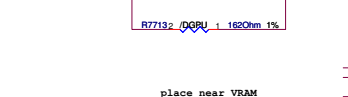
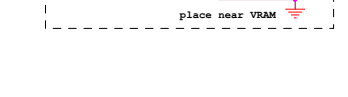
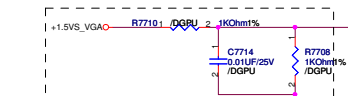
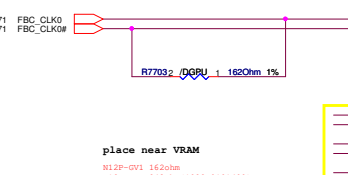
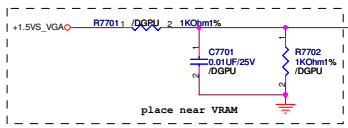
## \*TOP SIDE\*

## \*BOT SIDE\*



VRAM Information				VRAM Strap	
VRAM Location : U7601,U7602,U7603,U7604,U7701,U7702,U7703,U7704				VRAM Strap Location : R7487	
Vendor	Configuration	Pegatron P/N	Manufacturer P/N		
Hynix	128Mx16	0315-00ND0PB	H5TQ2663BFR-11C	0x6	35K
Hynix	64Mx16	0315-00NF0PB	H5TQ1G63DFR-11C	0x2	15K
Micron	128Mx16	TBD	MT41J128M16JT-107G:K	TBD	TBD
Micron	64Mx16	0315-00SG0PB	MT41J64M16JT-107G:G	TBD	TBD

VRAM CH C



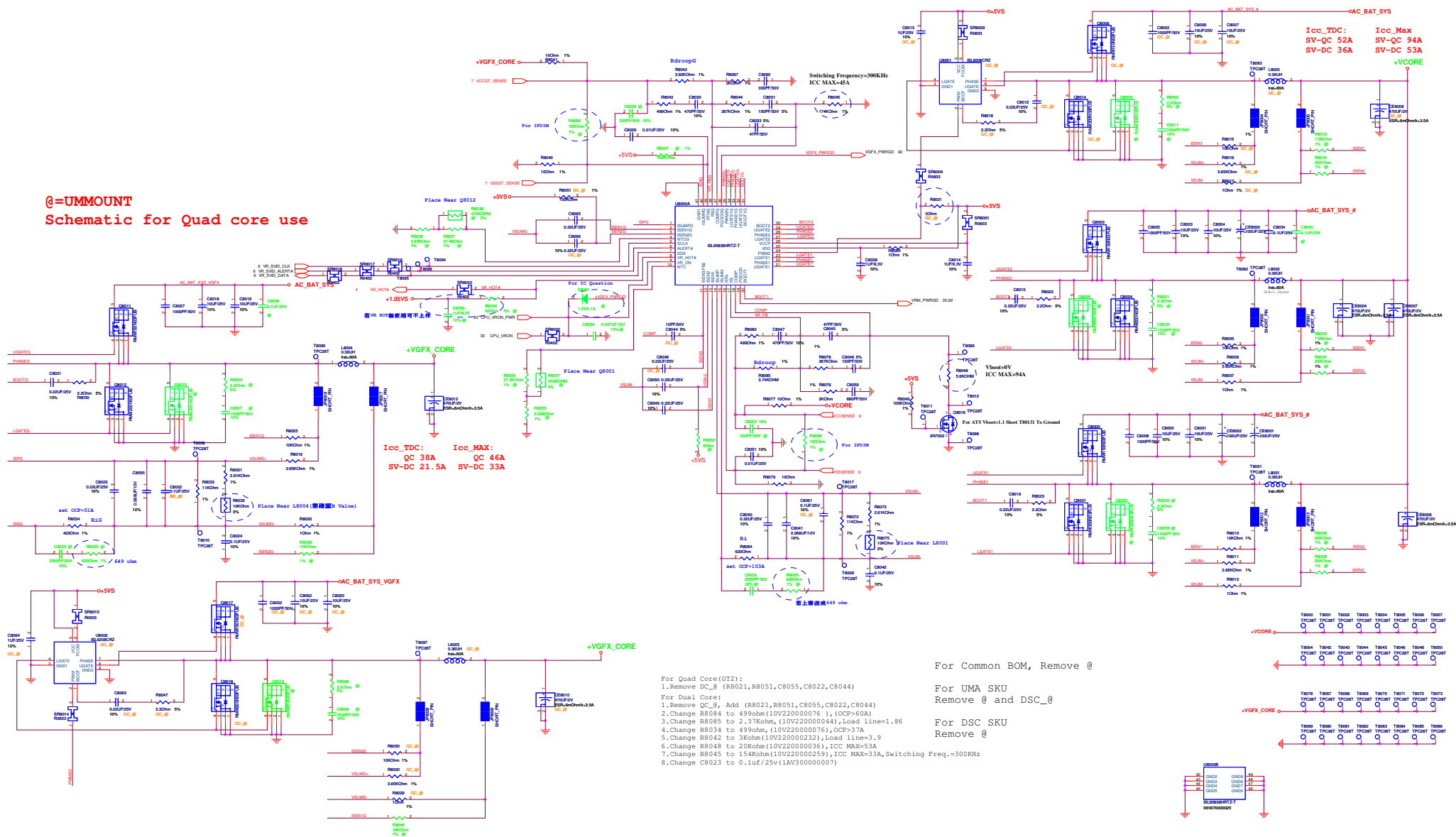
M13X DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
CMD0	CS0#	
CMD1		
CMD2	ODT	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16		CS0#
CMD17		
CMD18		ODT
CMD19		CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#
CMD31		





PEGATRON		Title : GPU_PEG*16	
PEGATRON COMPUTER INC		Engineer: Mickey_Yu	
Size	Project Name		Rev
C	P/N	VA79_N13P-GDDR3	1.0
Date: Friday, February 03, 2012		Sheet	79 of 99

@=UMMOUNT  
Schematic for Quad core use



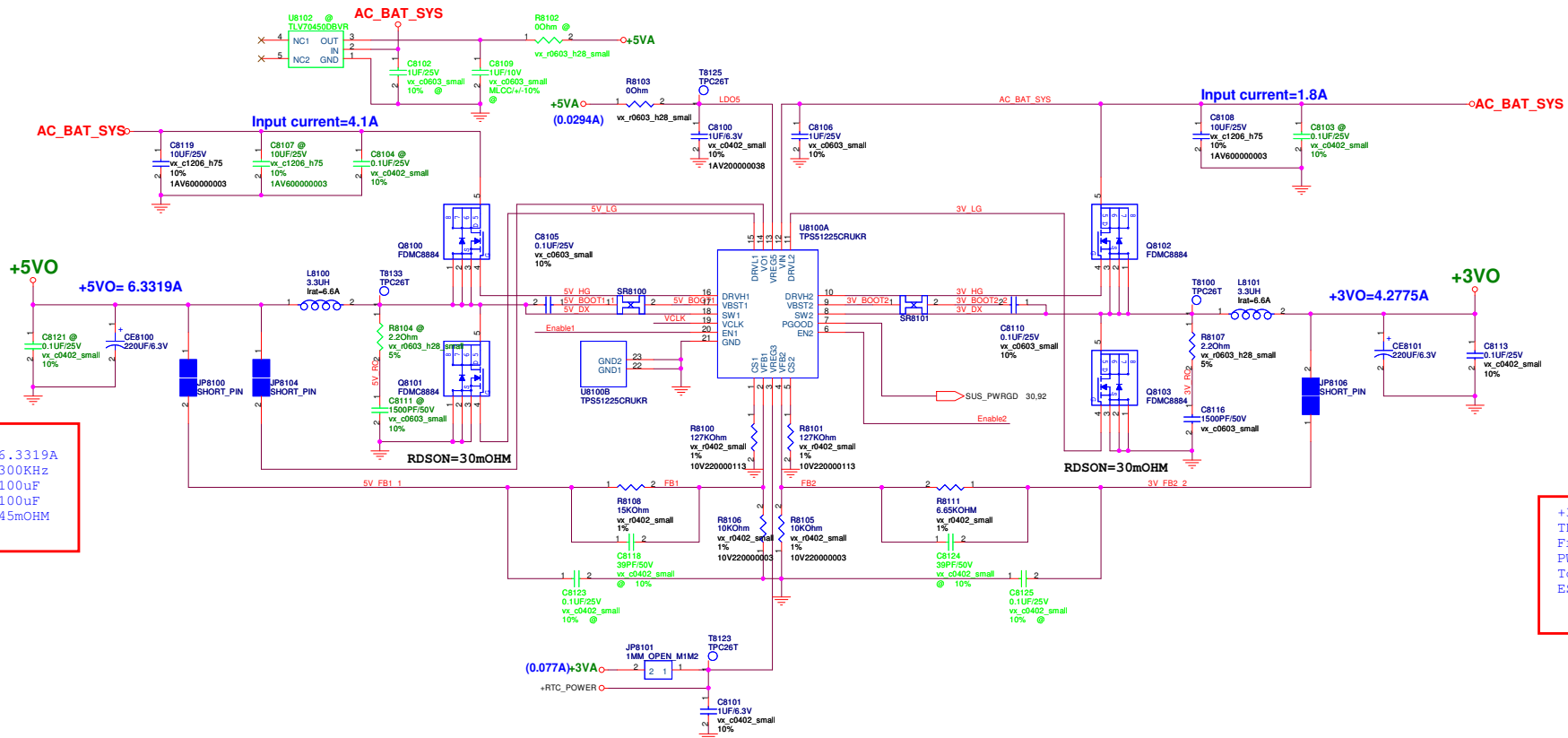
For Common BOM, Remove @

For UMA SKU  
Remove @ and DSC @

For DSC SKU  
Remove @

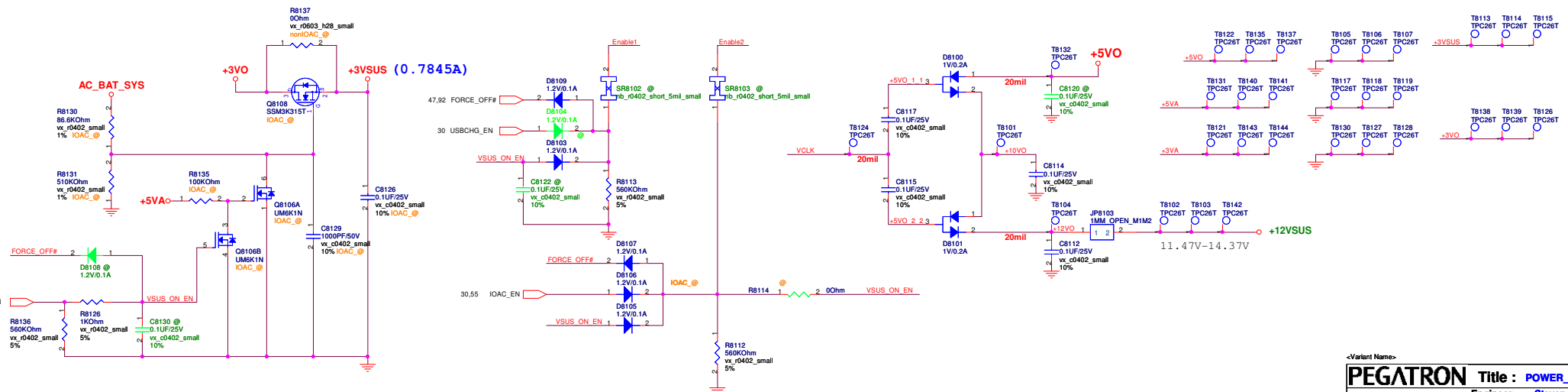
For Quad Core(GT2):	
1.Remove DC_0 (R8021,R8051,C8055,C8022,C8044)	For UMA
For Dual Core:	
1.Remove QC_0, add (R8021,R8051,C8055,C8022,C8044)	Remove
2.Change R8084 to 29970h(10V2200000074), (OCP=60A)	
3.Change R8085 to 33330h, (10V2200000006, Load line=1.86	For D3C
4.Change R8034 to 4999h, (10V2200000037), OCP=37A	
5.Change R8042 to 3040h(10V2200000023), Load line=3.9	
6.Change R8048 to 20K0h (10V2200000003), I2C MAX=53A	
7.Change R8045 to 15040h(10V2200000029), I2C MAX=33A, Switching Freq.=300KHz	
8.Change R8023 to 0.15uF/25v(1AV3300000007)	

## +5V0 & +3V0 POWER SUPPLY

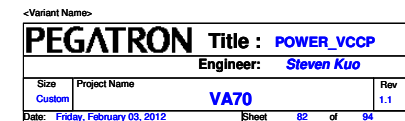


```
+5V0
TDC           :6.3319A
Frequency     :300KHz
PWR Cap.     :100uF
Total Cap.   :100uF
ESR          :45mOHM
```

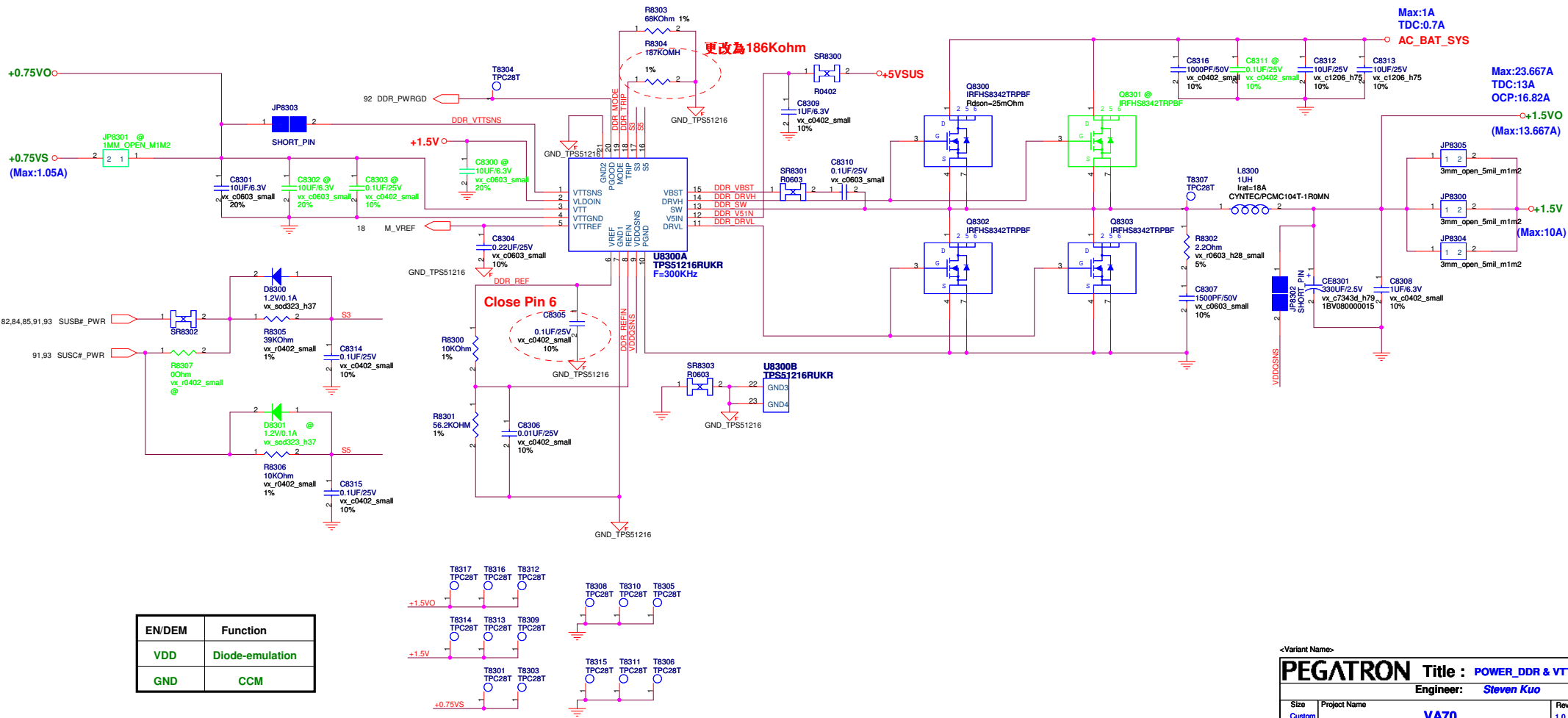
```
+3VO
TDC           :4.2775A
Frequency     :350KHz
PWR Cap.      :100uF
Total Cap.    :100uF
ESR           :45mOHM
```



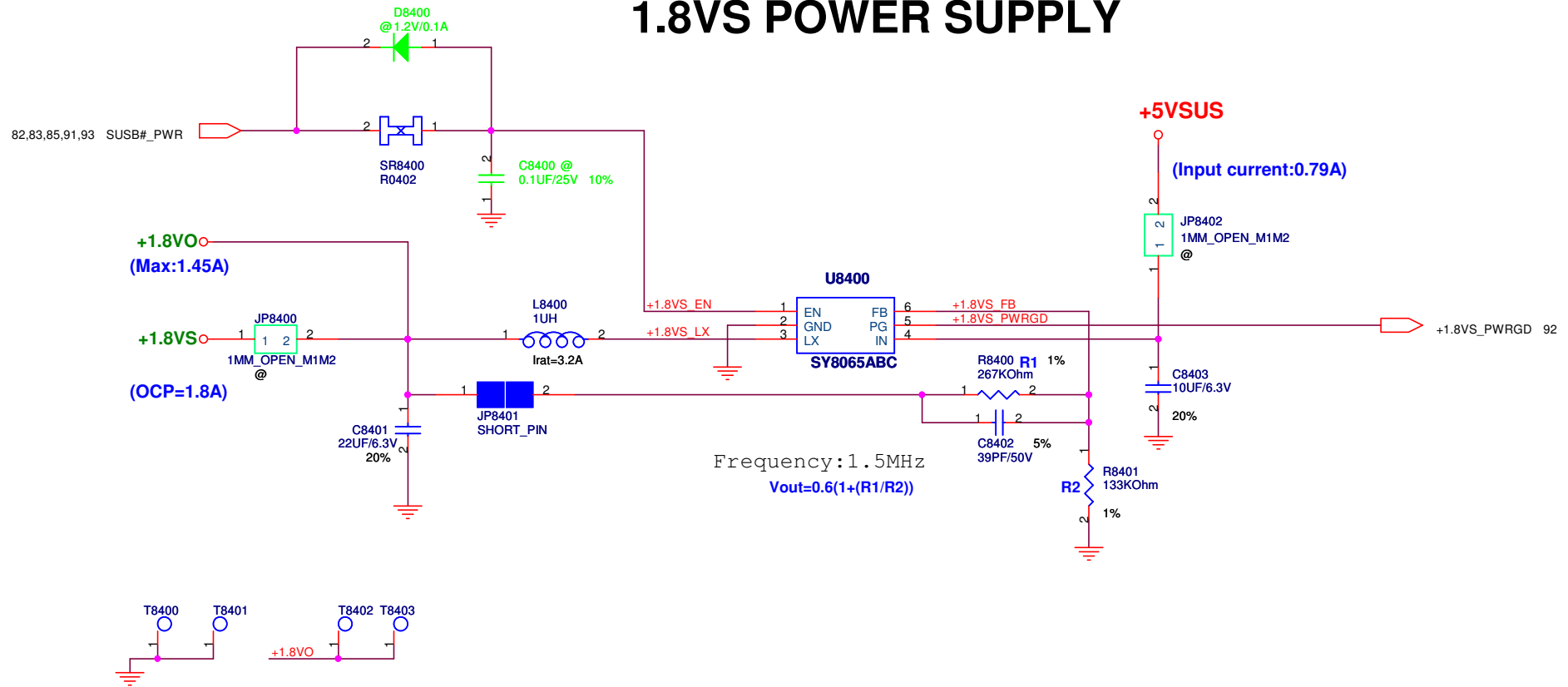
Used for testing purpose in production line.  
Pull down to GND with a resistor of 470 kΩ or less



DDR & VTT POWER SUPPLY



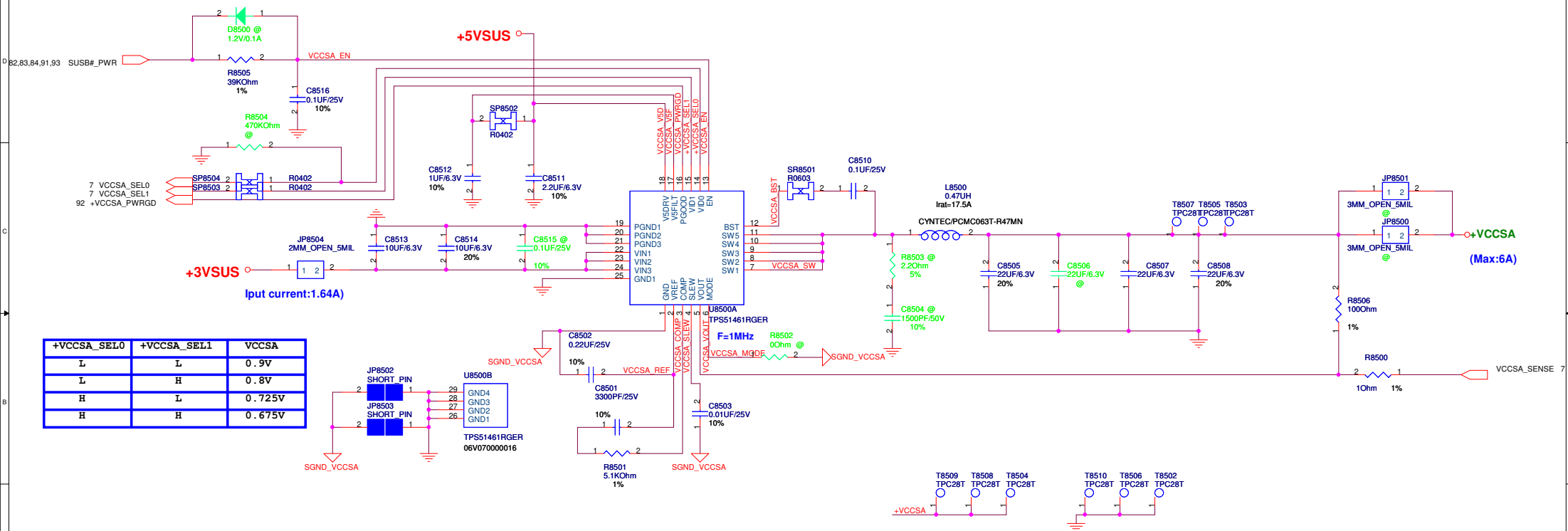
# 1.8VS POWER SUPPLY



<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_1.8VS</b>	
		Engineer: <b>Steven Kuo</b>	
Size Custom	Project Name <b>VA70</b>		Rev 1.0
Date: <b>Friday, February 03, 2012</b>		Sheet	84 of 94

## VCCSA POWER SUPPLY



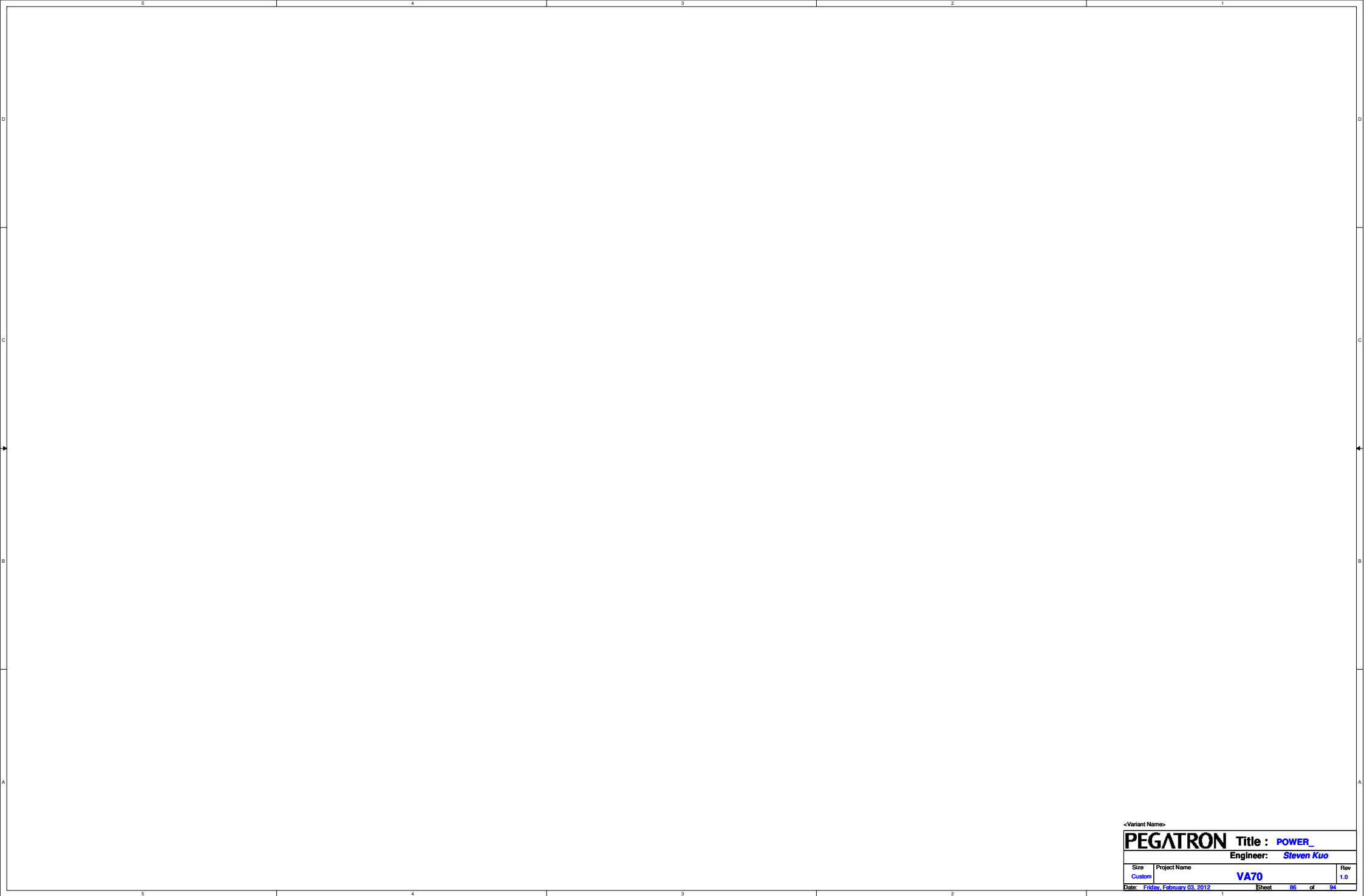
+VCCSA_SELO	+VCCSA_SEL1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

**<Variant Name>**

**PEGATRON** Title : POWER\_VCCSA

Engineer: **Steven Kuo**

Size Custom	Project Name <b>VA70</b>	Rev 1.0
Date: Friday, February 03, 2012	Sheet 85 of 94	



<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b> <b>POWER</b>	
		<b>Engineer:</b> <b>Steven Kuo</b>	
Size	Project Name		Rev
Custom	<b>VA70</b>		1.0
Date: <b>Friday, February 03, 2012</b>			
		Sheet <b>86</b> of <b>94</b>	

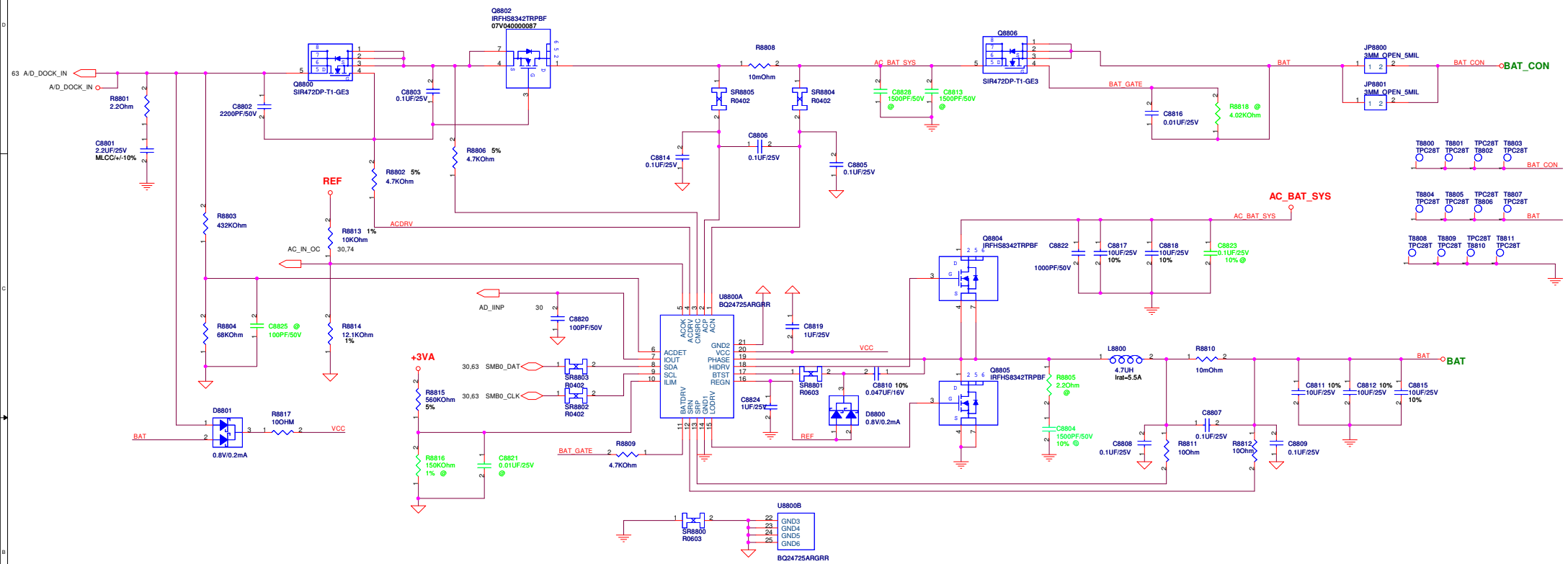
## VID Set 0.9V



Engineer: **Steven Kuo**

Date: Friday, February 03, 2012 Sheet 87 of 99

## BATTERY CHARGER



<Variant Name>

<b>PEGATRON</b>	<b>Title :</b> POWER_CHARGER
-----------------	------------------------------

Engineer: **Steven Kuo**

Size	Project Name	Rev
Custom	VA70	1.0

Date: Friday, February 03, 2012 Sheet 88 of 15

D

C

B

A

<Variant Name>

**PEGATRON** Title :POWER\_N/A

**Engineer:**

Size  
A

Project Name
--------------

Rev	1.1
-----	-----

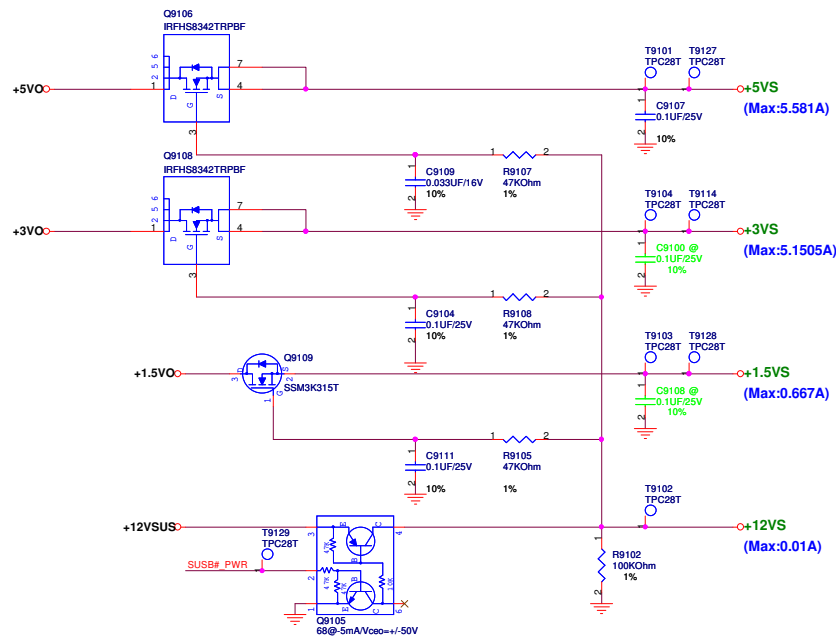
Date: Friday, February 03, 2012

Sheet 89 of 99

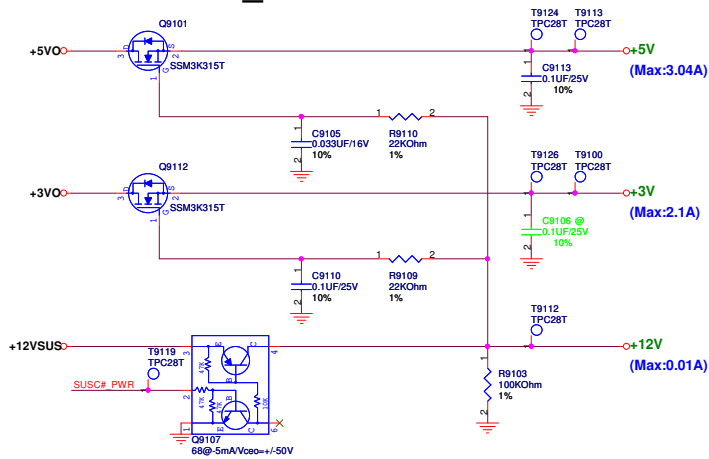
BATTERY IN DETECT



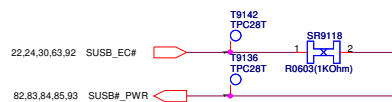
## SUSB#\_PWR POWER



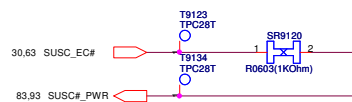
## SUSC#\_PWR POWER



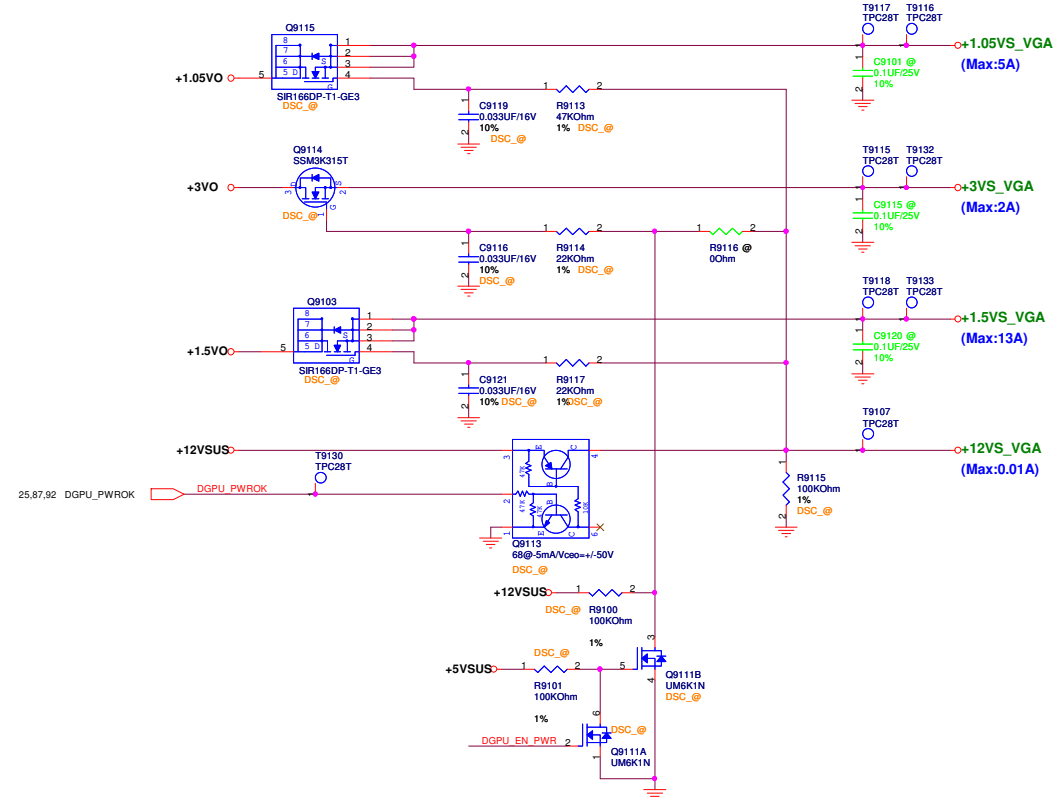
### SUSB#\_PWR POWER Control



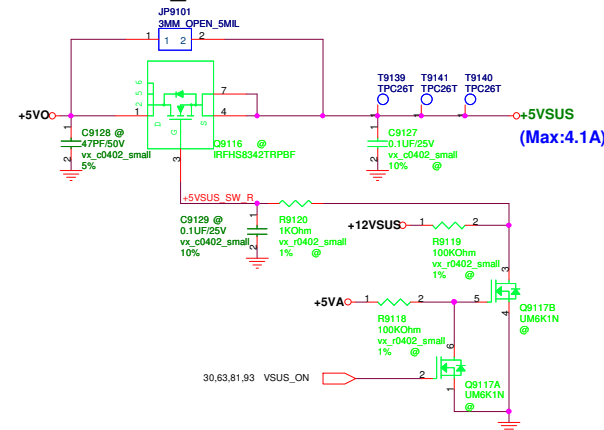
### SUSC#\_PWR POWER Control



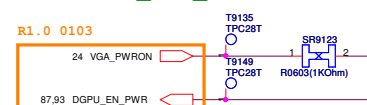
## DSC#\_PWR POWER(DGPU)



## USBCHG#\_PWR POWER

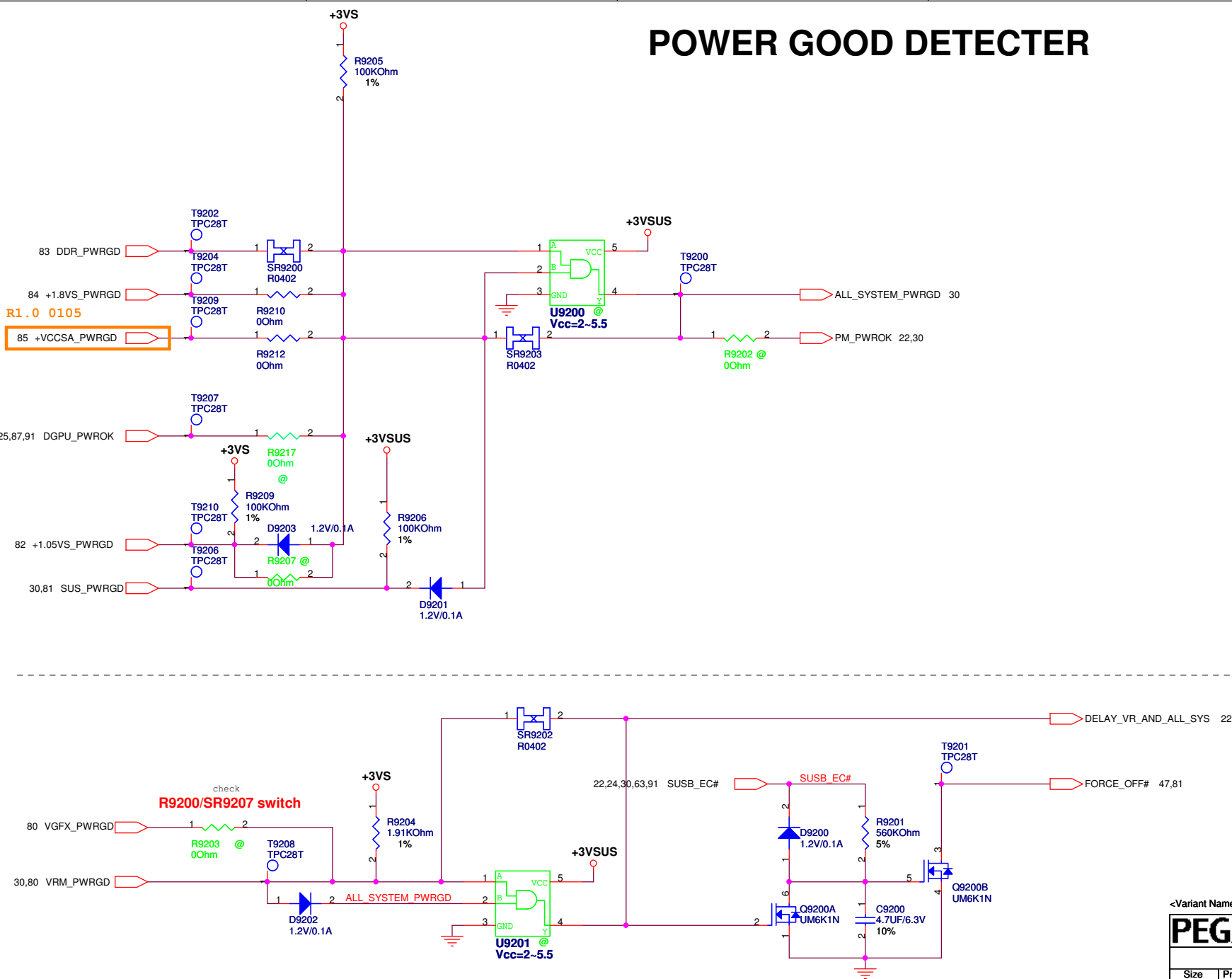


### DSC\_VGA\_PWR POWER Control



<Variant Name>		Title : POWER_LOAD SWITCH	
PEGATRON		Engineer: Steven Kuo	
Size	Project Name	Rev	1.0
Custom	VA70		
Date: Friday, February 03, 2012	Sheet	91	of 94

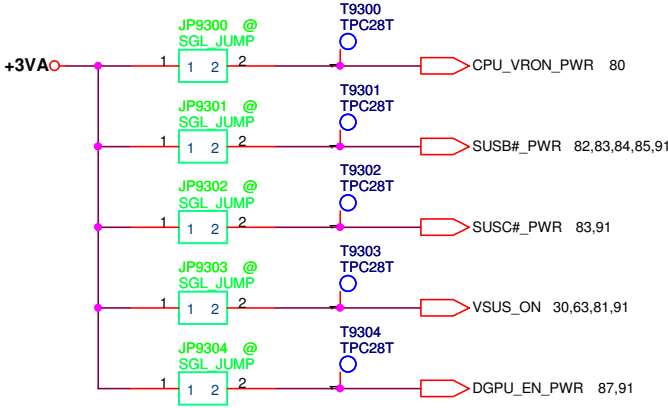
# POWER GOOD DETECTOR



<Variant Name>		
<b>PEGATRON</b> Title : <b>POWER_PROTECT</b>		
Engineer: <b>Steven Kuo</b>		
Size Custom	Project Name <b>VA70</b>	Rev 1.0
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AC_BAT_SYS		AC_BAT_SYS	37,55,80,81,82,83,87,88
BAT_CON		BAT_CON	63,88
+5VA		+5VA	30,42,61,66,81,91
+3VA		+3VA	20,27,30,48,63,65,81,88
+5VO		+5VO	61,81,91
+3VO		+3VO	55,81,91
+1.8VO		+1.8VO	84
+1.5VO		+1.5VO	83,91
+1.05VO		+1.05VO	82,91
+12VSUS		+12VSUS	22,28,60,81,91
+5VSUS		+5VSUS	22,27,30,60,61,63,65,66,82,83,84,85,91
+3VSUS		+3VSUS	4,22,24,27,28,30,33,65,81,85,92
+12V		+12V	91
+5V		+5V	51,63,91
+3V		+3V	4,24,37,51,63,65,91
+1.5V		+1.5V	5,7,16,51,63,83
+12VS		+12VS	28,39,41,91
+5VS		+5VS	27,30,38,39,41,42,48,49,60,63,66,80,87,91
+3VS		+3VS	4,16,17,20,21,22,23,24,25,26,27,28,30,37,38,39,40,41,47,48,49,53,55,60,63,66,69,91,92
+1.8VS		+1.8VS	7,25,26,63,84
+1.5VS		+1.5VS	26,53,55,63,91
+1.05VS		+1.05VS	26,27,63,80,82,87
+0.75VS		+0.75VS	16,17,63,83
+VCCSA		+VCCSA	7,85
+VCCP		+VCCP	3,4,6,7,25,26,27,37,47,63,82
+12VS_VGA		+12VS_VGA	91
+3VS_VGA		+3VS_VGA	63,70,72,74,75,87,91
+1.5VS_VGA		+1.5VS_VGA	63,71,75,76,77,91
+1.05VS_VGA		+1.05VS_VGA	63,70,71,72,91
+VGA_VCORE		+VGA_VCORE	63,75,87
+VGFX_CORE		+VGFX_CORE	7,63,80
+VCORE		+VCORE	6,63,80

# FOR POWER TEST



<Variant Name>

<b>PEGATRON</b>		<b>Title :</b> POWER_SIGNAL
<b>Size</b> Custom		<b>Engineer:</b> Steven Kuo
<b>Project Name</b> A35		<b>Rev</b> 1.0
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