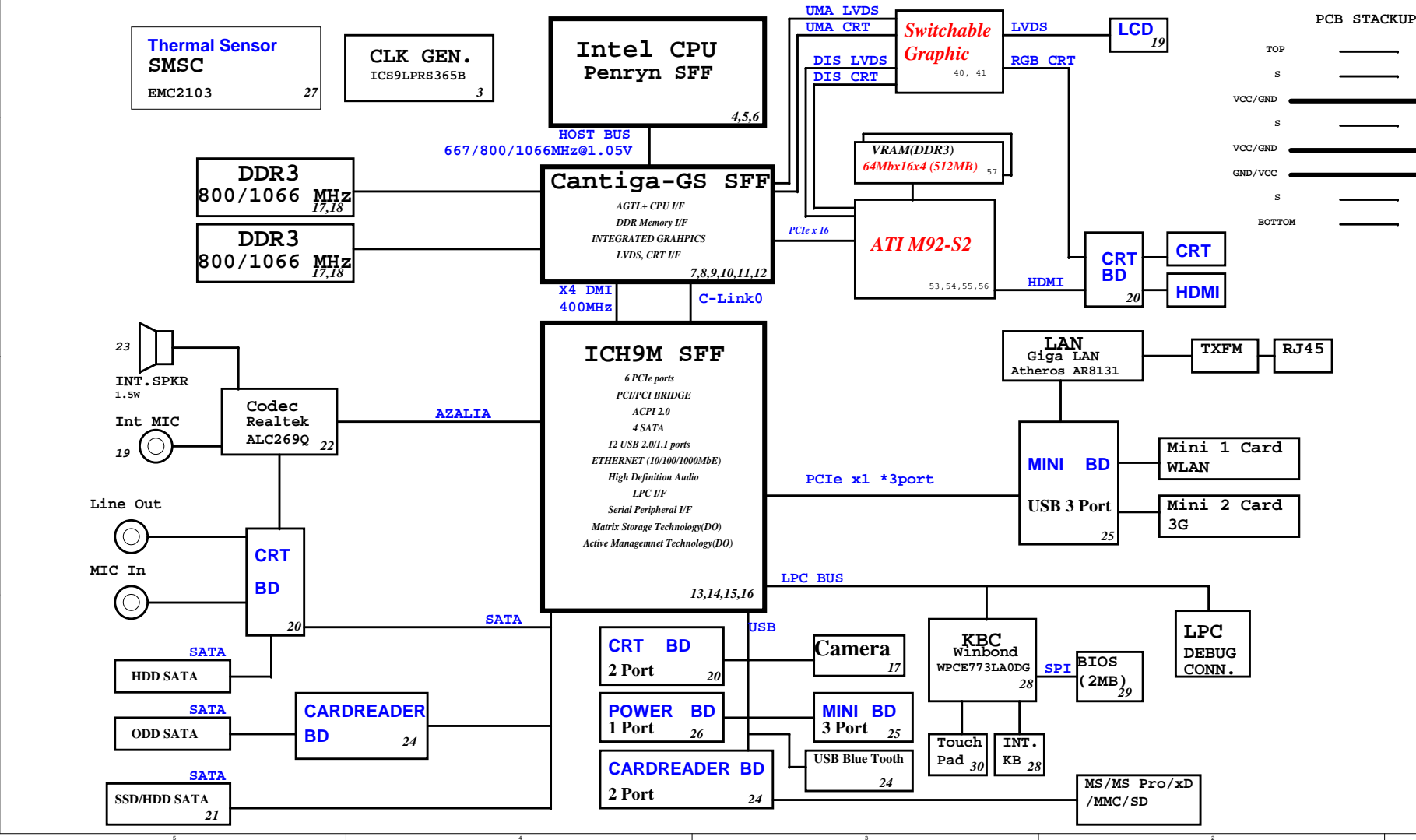


JM41/JM51 Discrete Block Diagram

Project code: 91.4CQ01.001
PCB P/N : 48.4CQ01.0SB
REVISION : 08274-1



SYSTEM DC/DC TPS51125 36	
INPUTS	OUTPUTS
5V_S5(6A)	3D3V_S5(5A)
5V_AUX_S5	3D3V_AUX_S5
RT8202 37	
INPUTS	OUTPUTS
DCBATOUT	LD05V_S0(10A)
RT8202 38	
INPUTS	OUTPUTS
DCBATOUT	LD5V_S3(11A)
RT9026 39	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3(1.2A)
CHARGER MAX8731A 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC ADP3207A 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 64A
VGA ISL6263A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC GFXCORE (7A)

PCB STACKUP	
TOP	L1
S	L2
VCC/GND	L3
S	L4
VCC/GND	L5
GND/VCC	L6
S	L7
BOTTOM	L8

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File

BLOCK DIAGRAM

Size Custom

Document Number

JM41 Discrete

Rev -2

Date: Tuesday, April 28, 2009

Sheet 1 of 48

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

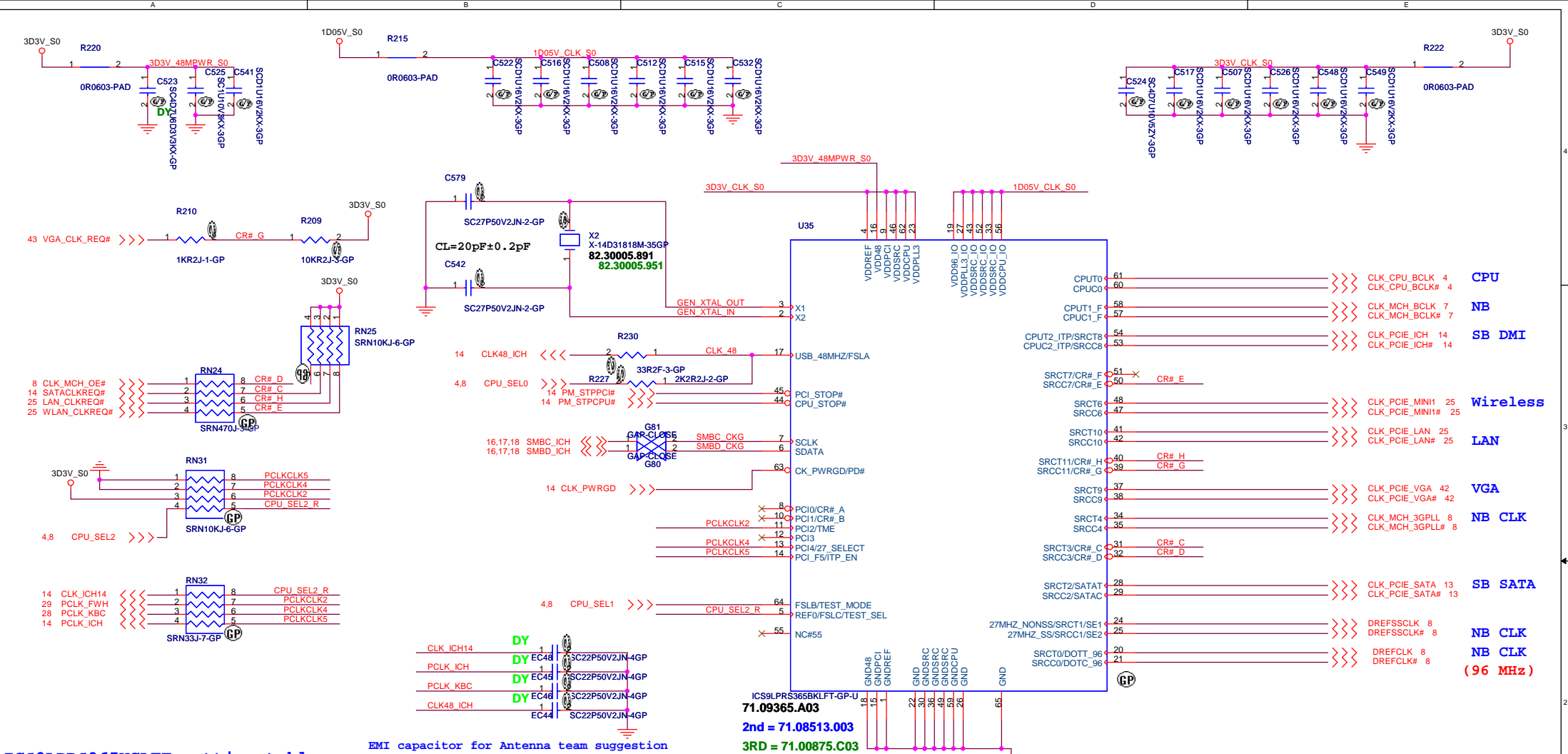
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSFPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native LAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCie are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 6 0 = CR#_B controls SRC0 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1 = CR#_C controls SRC2 pair

EMI capacitor for Antenna team suggestion

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1 = CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1 = CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1 = CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

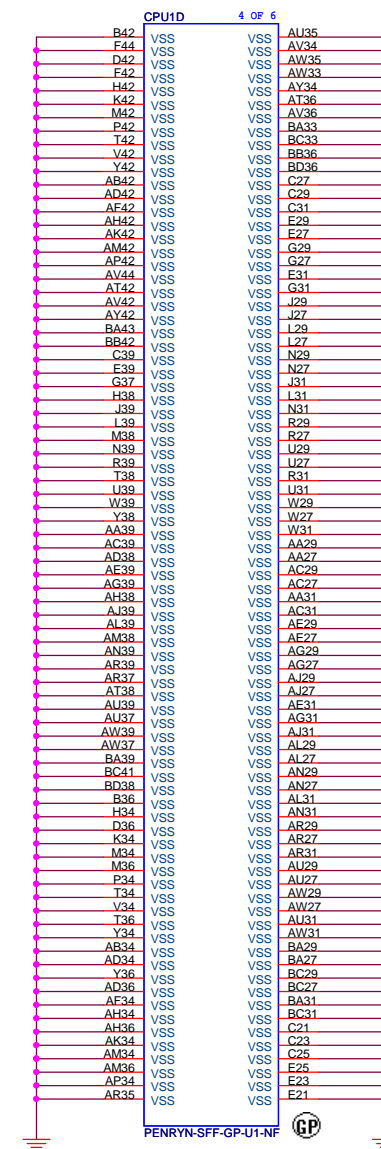
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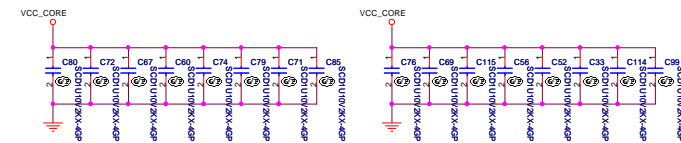
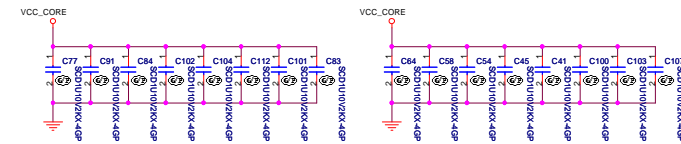
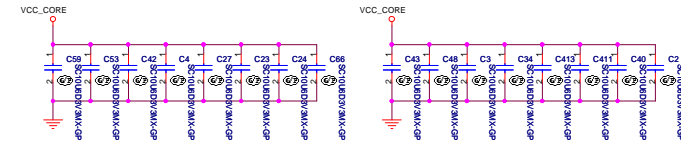
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Title: **Clock Generator**

Size: Document Number **JM41 Discrete** Rev: **-2**

Date: Tuesday, April 28, 2009 Sheet 3 of 48

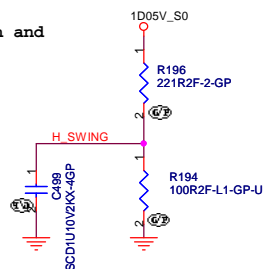




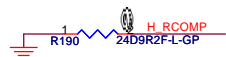
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CPU (3 of 3)			
Size	Document Number		Rev
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H_SWING routing Trace width and Spacing use 10 / 20 mil

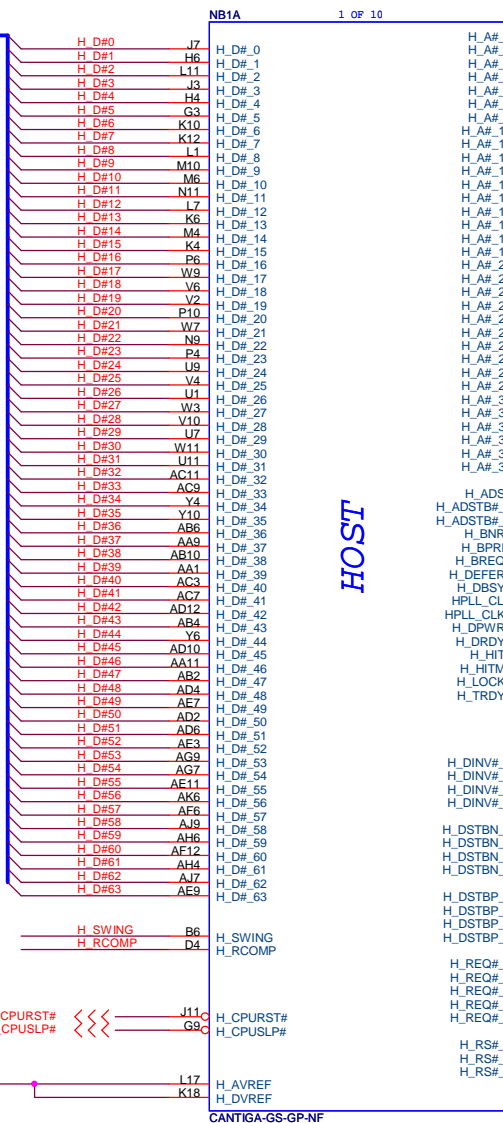
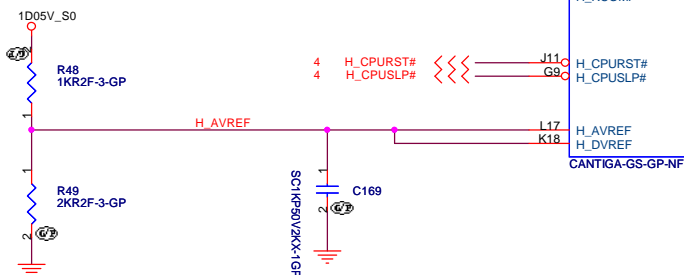
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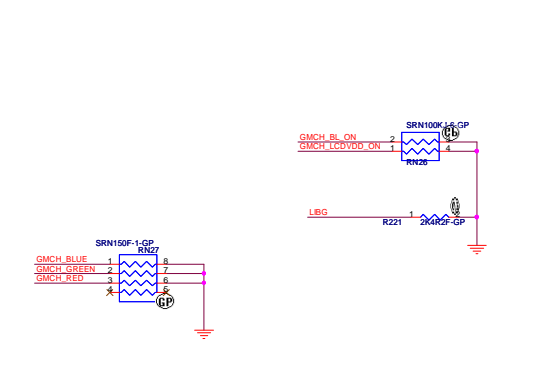
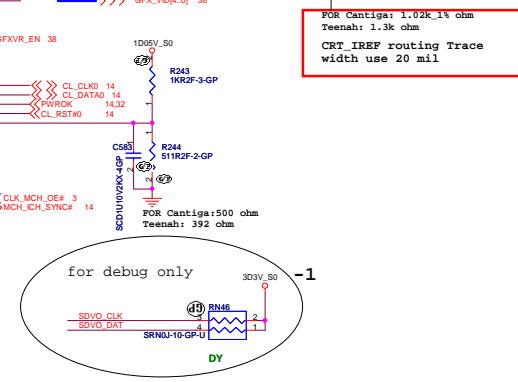
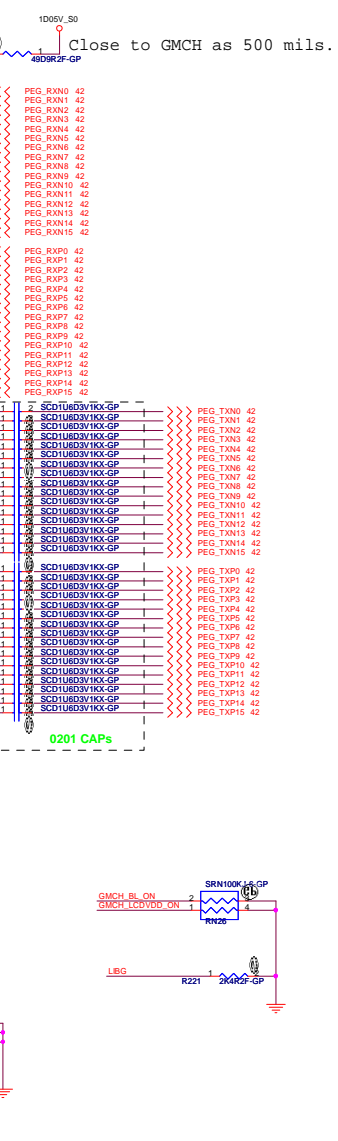
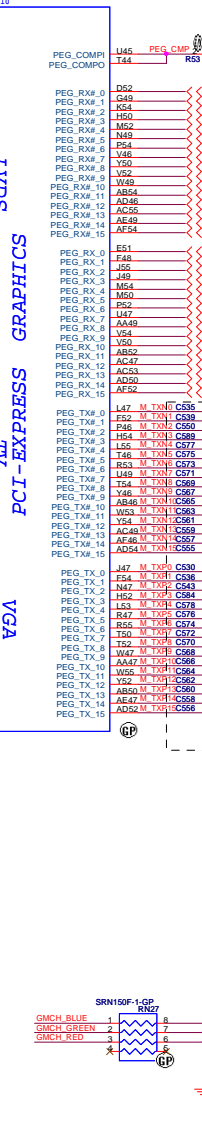
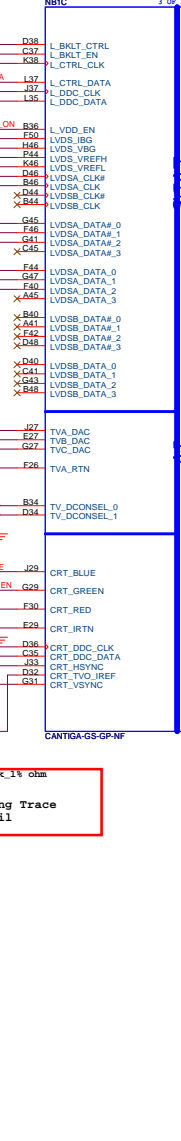
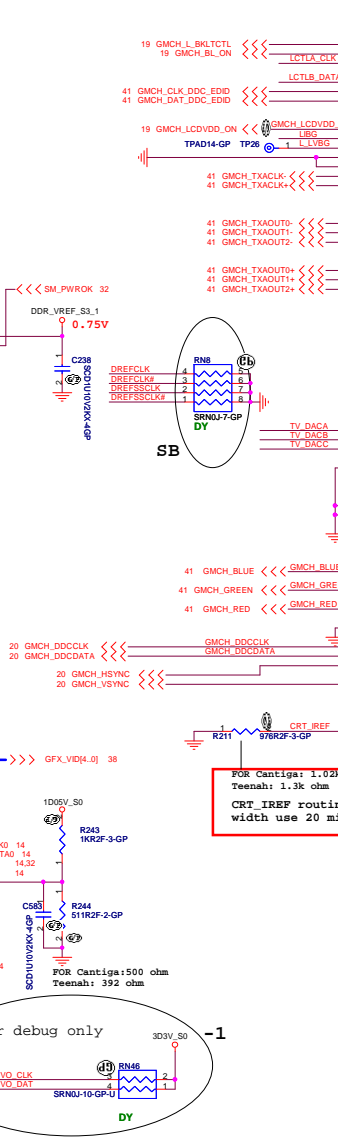
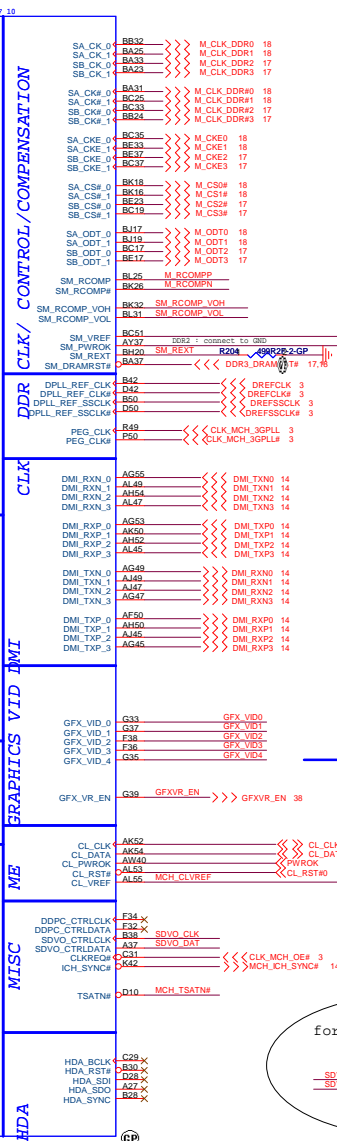
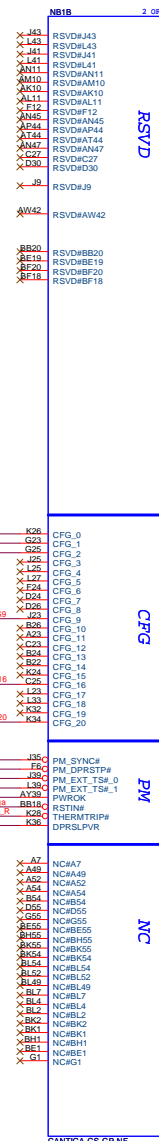
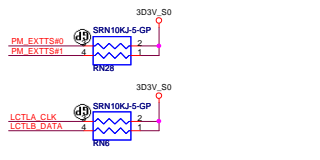
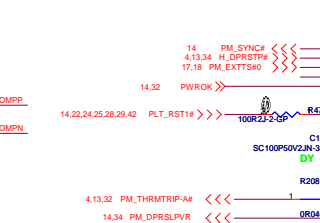
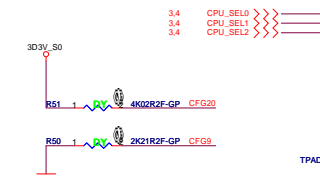
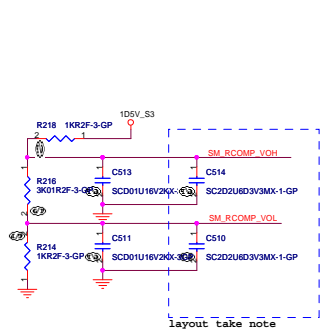
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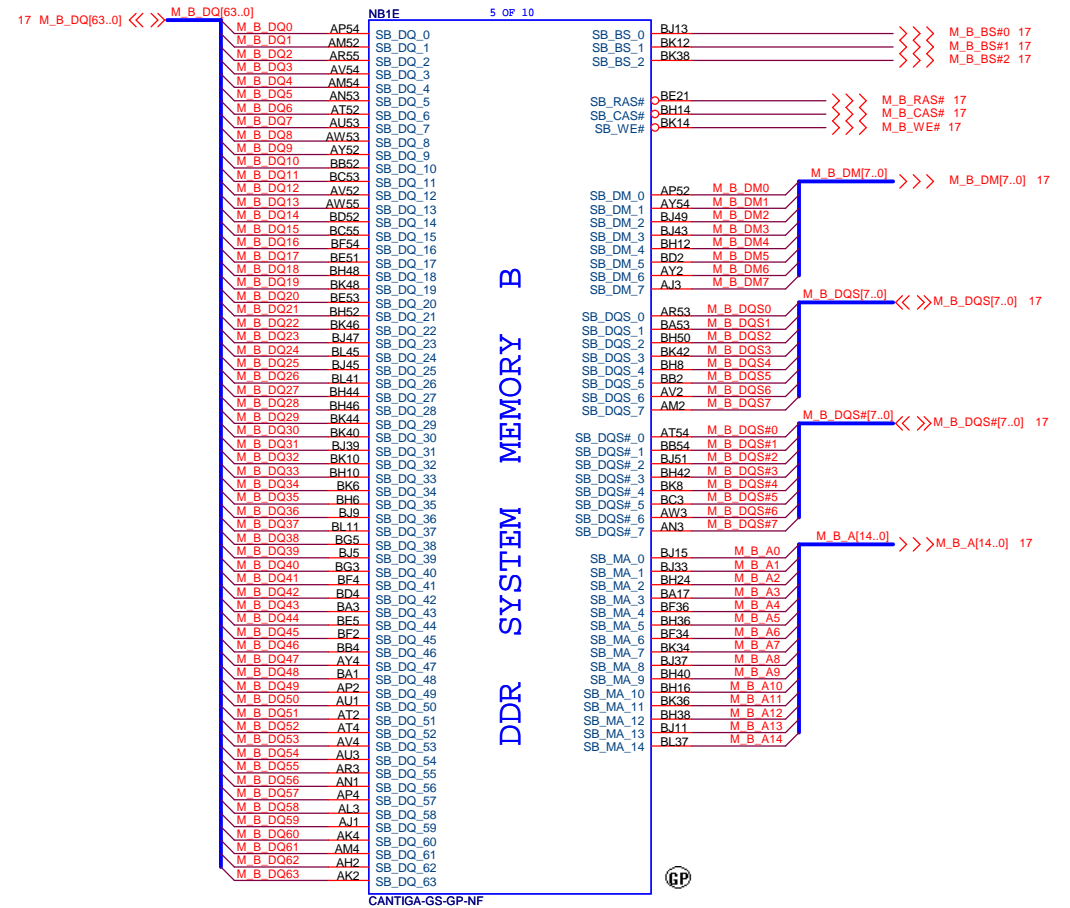
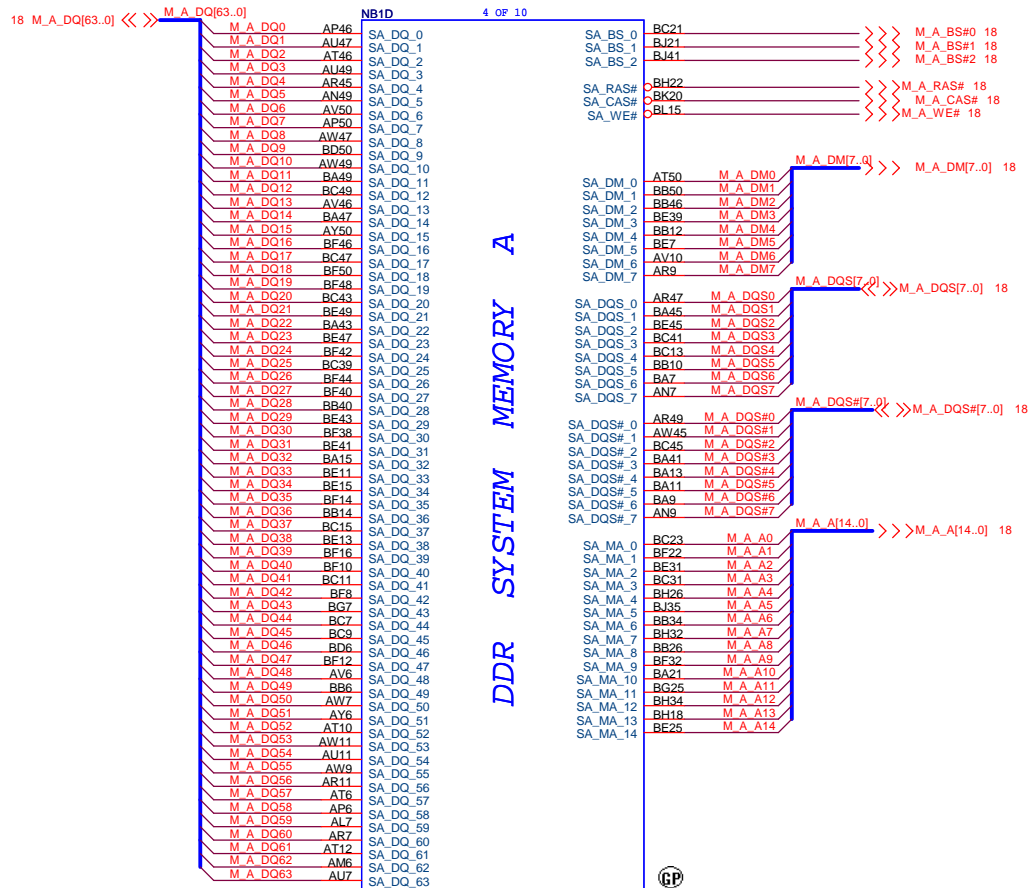


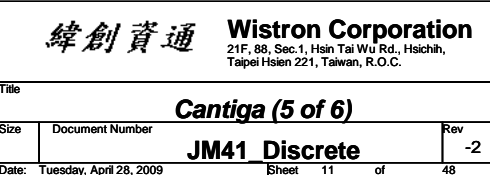
Place them near to the chip (< 0.5")

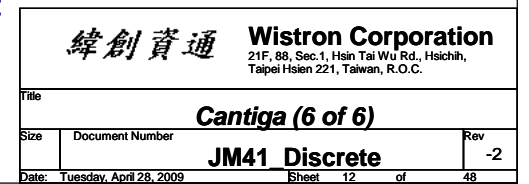


HOST











657mA

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

2mA

2mA

47mA

SATA+USB=1.56A

USBPLL=10mA

19mA in S0; 78mA in S3/S4/S5

23mA

80mA

1mA

6uA in G3

1.13A

23mA

50mA

1mA

VCC3_3=278mA

32mA

32mA

177mA

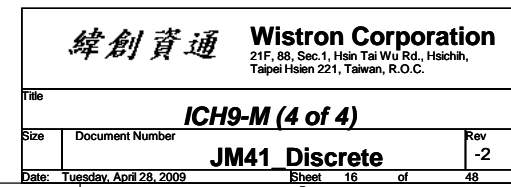
18mA

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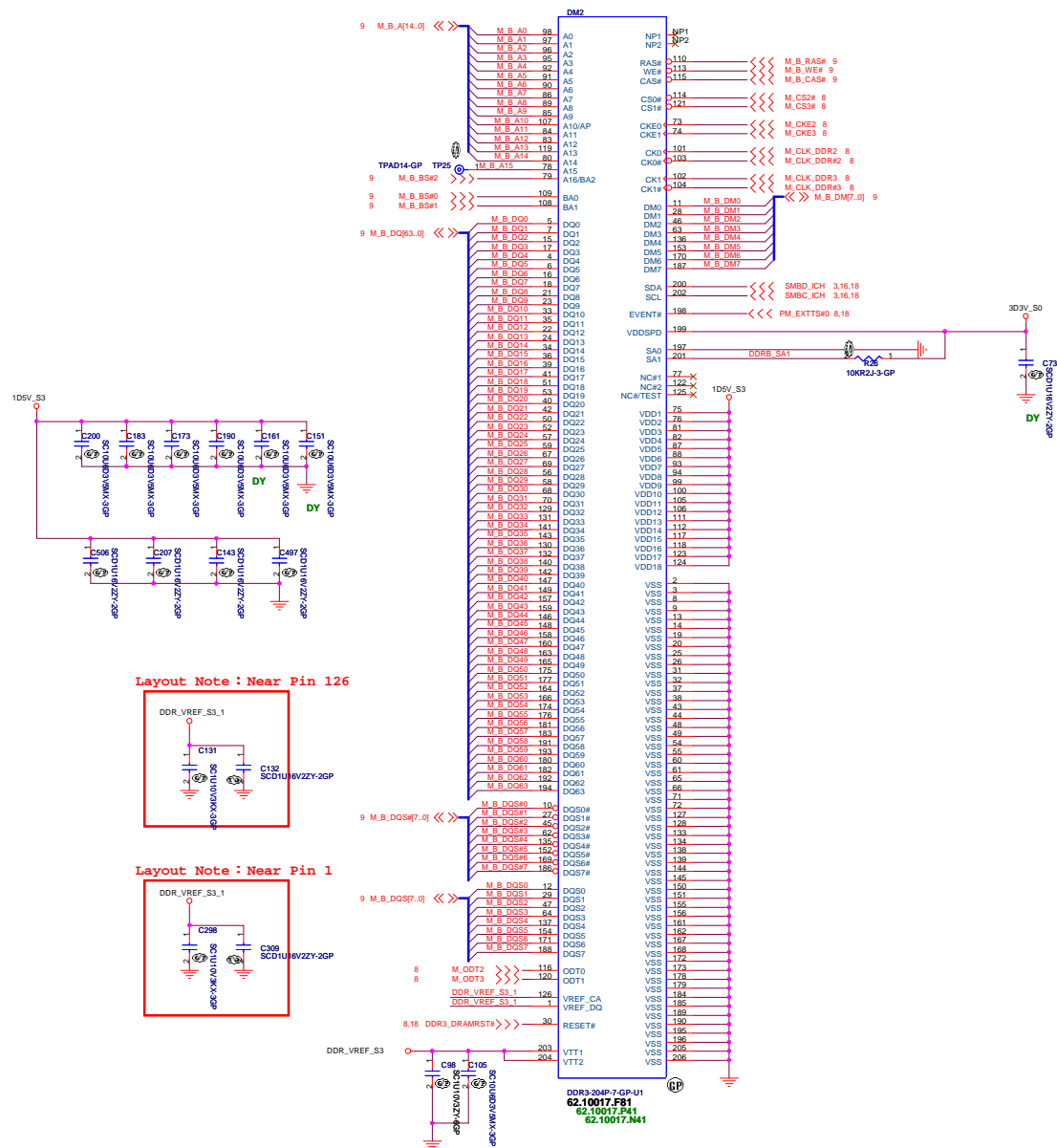
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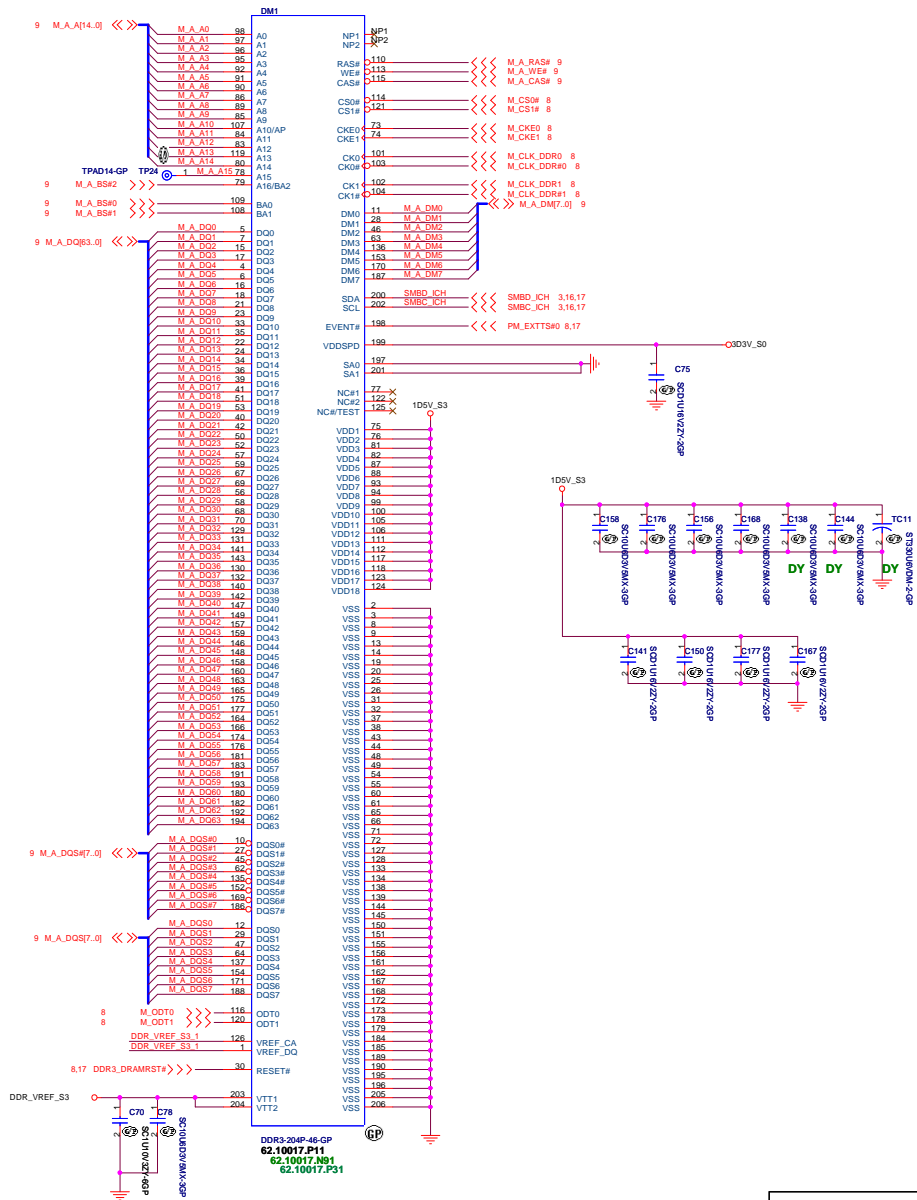
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Size	Document Number	Rev	
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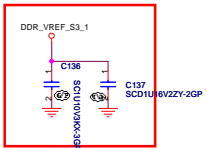
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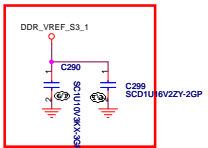
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Layout Note : Near Pin 126

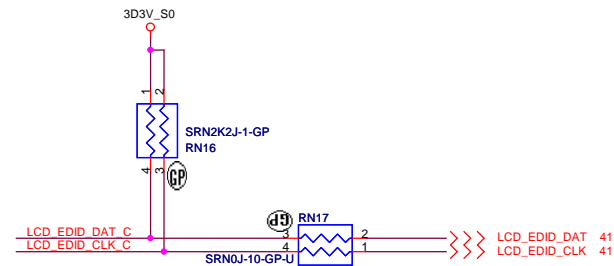
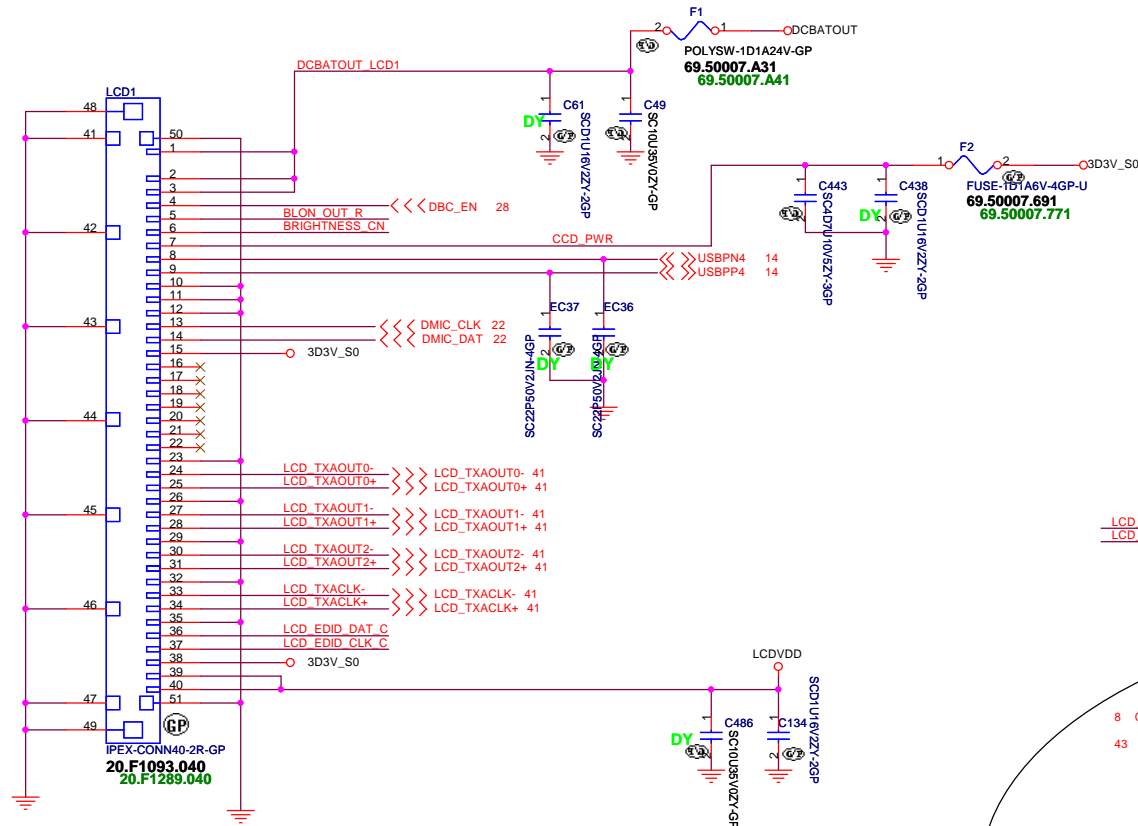


Layout Note : Near Pin 1

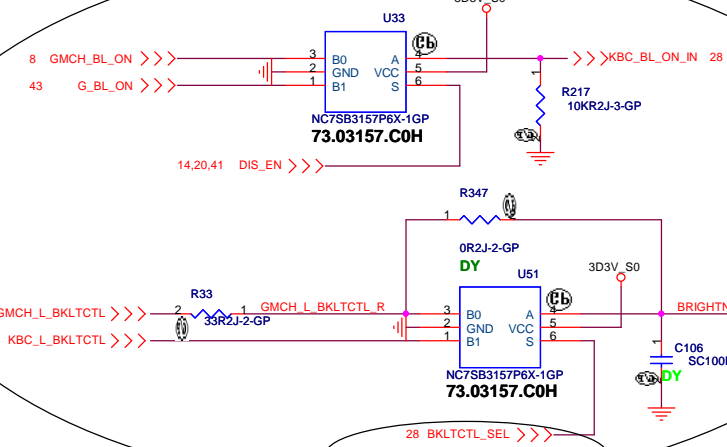


LCD/CCD CONN

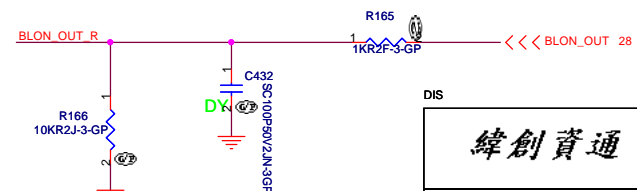
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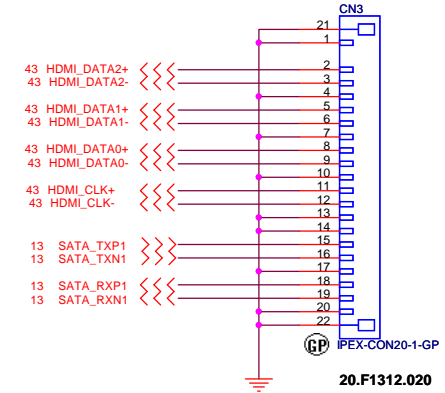
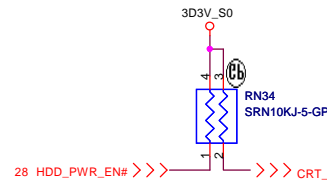
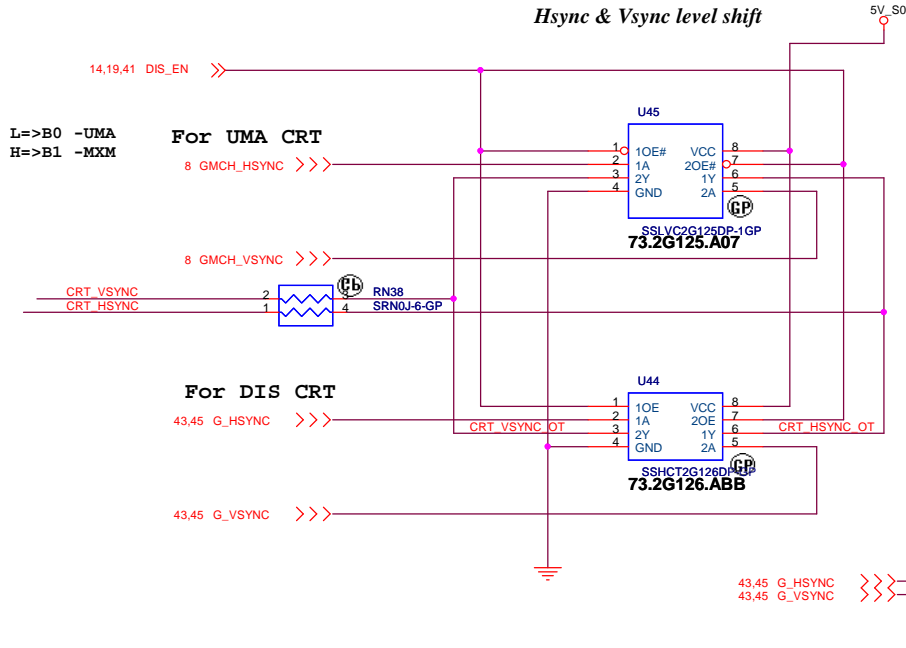
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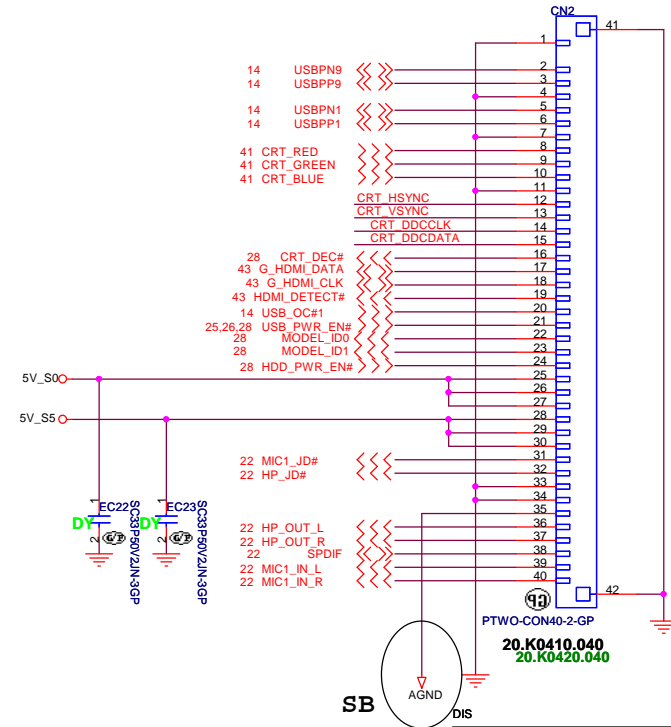
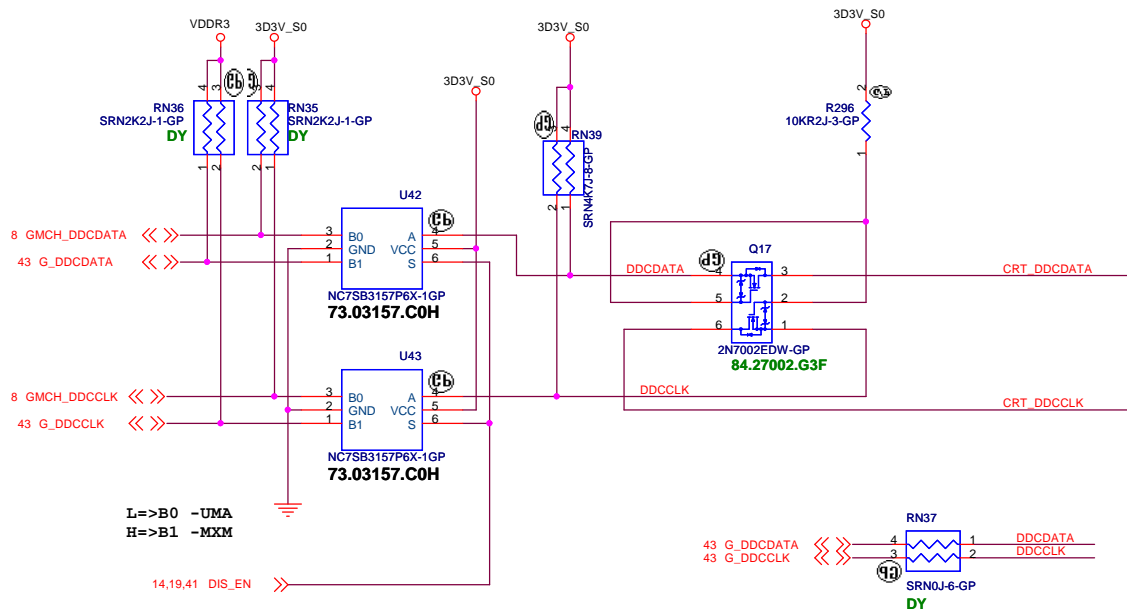
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Hsync & Vsync level shift



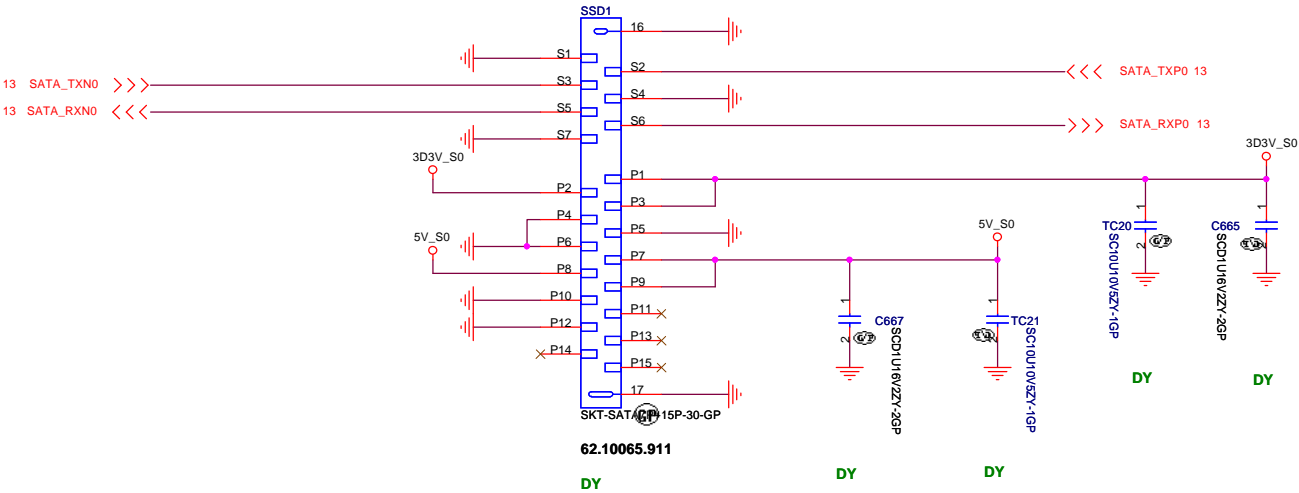
DDC_CLK & DATA level shift



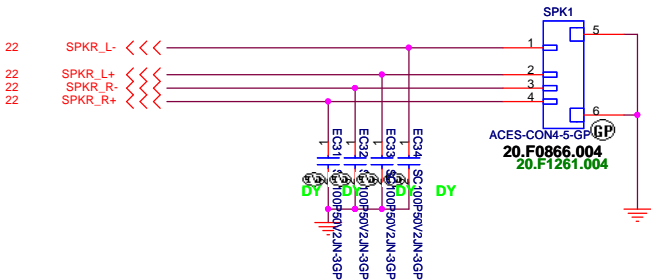
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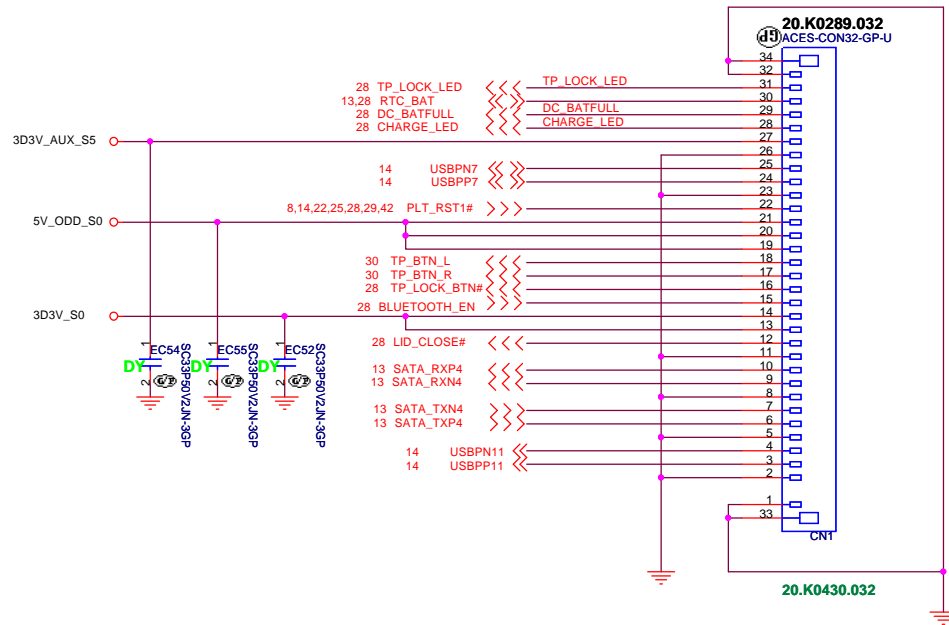
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SSD SATA Connector



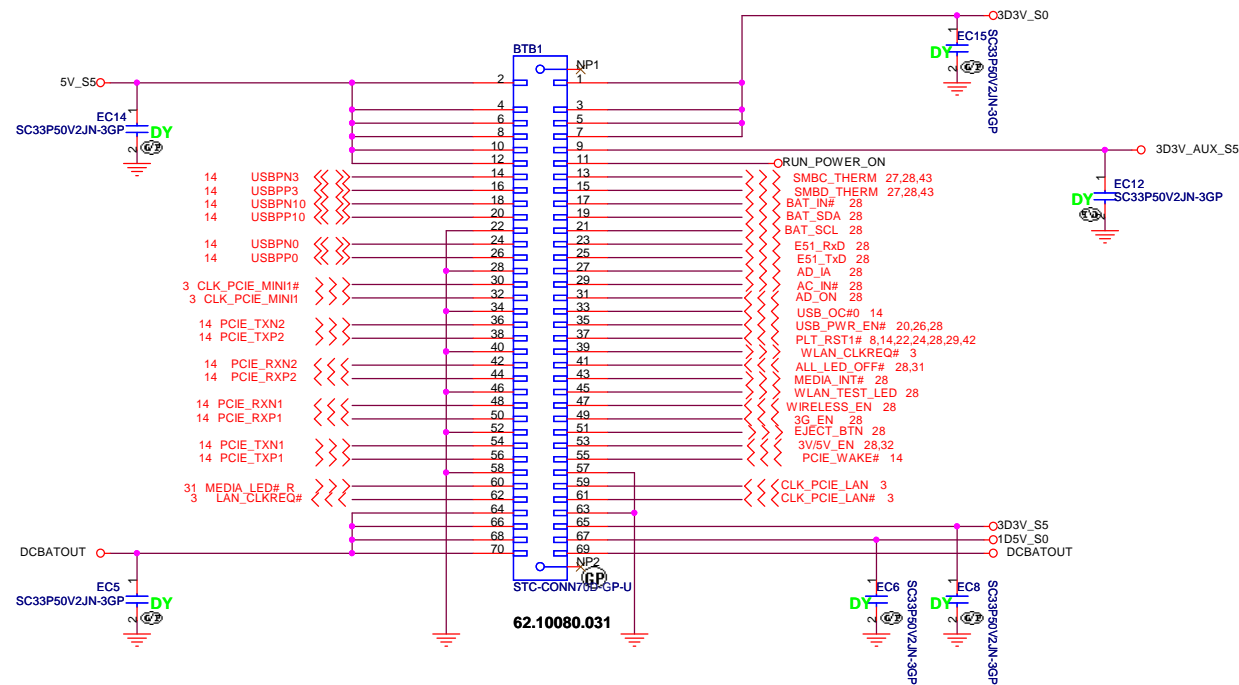
Internal Speaker





DIS

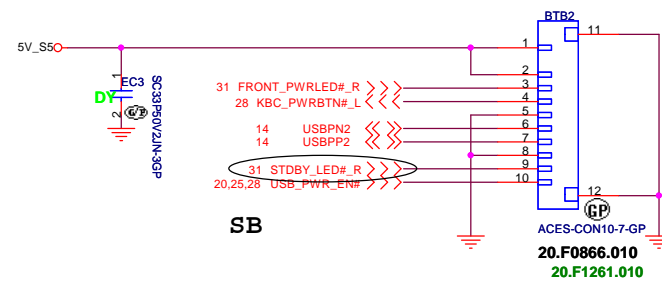
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Size	Document Number		Rev
	JM41 Discrete		-2
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Title		
MINI BD CONN		
Size	Document Number	Rev
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Date: Tuesday, April 28, 2009		
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DIS

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Title

POWER BUTTON CONN

Size

Document Number

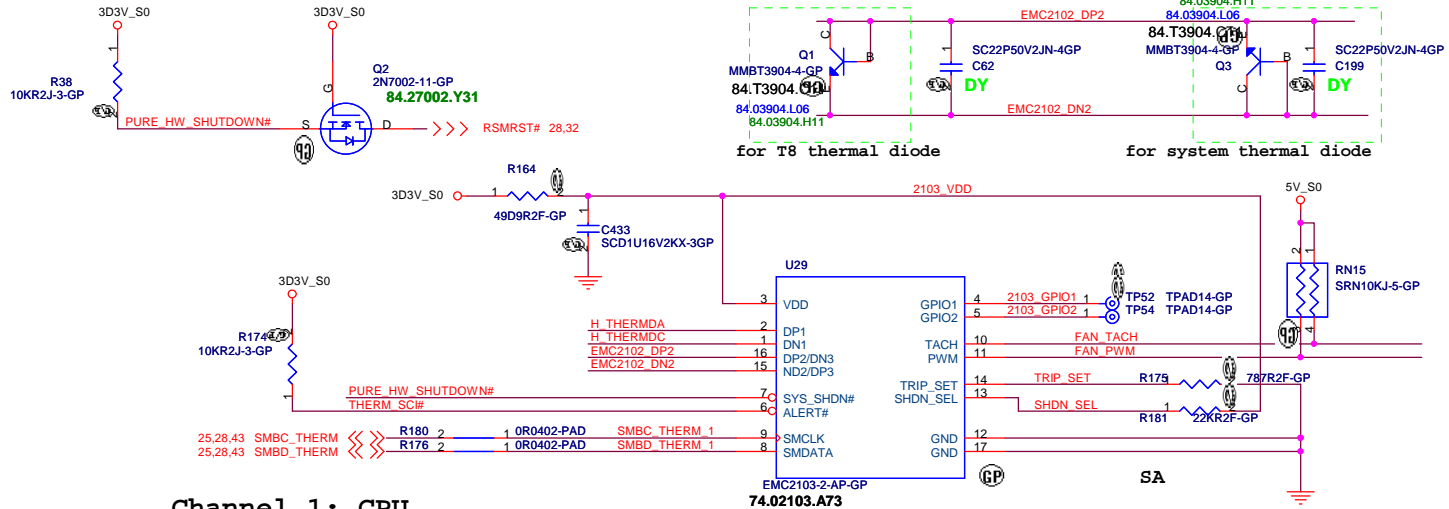
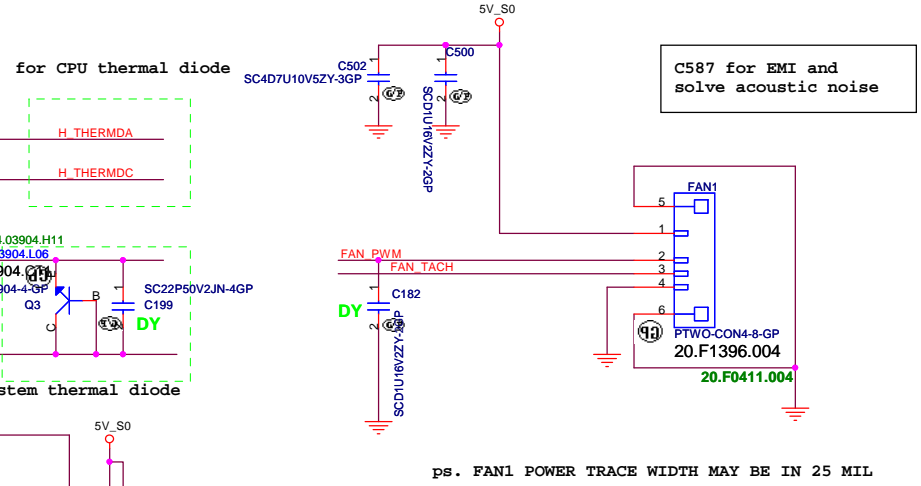
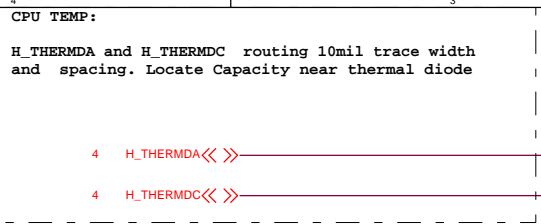
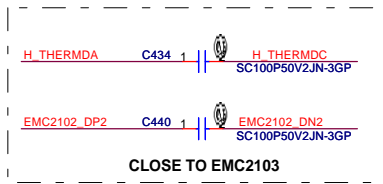
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Rev

-2

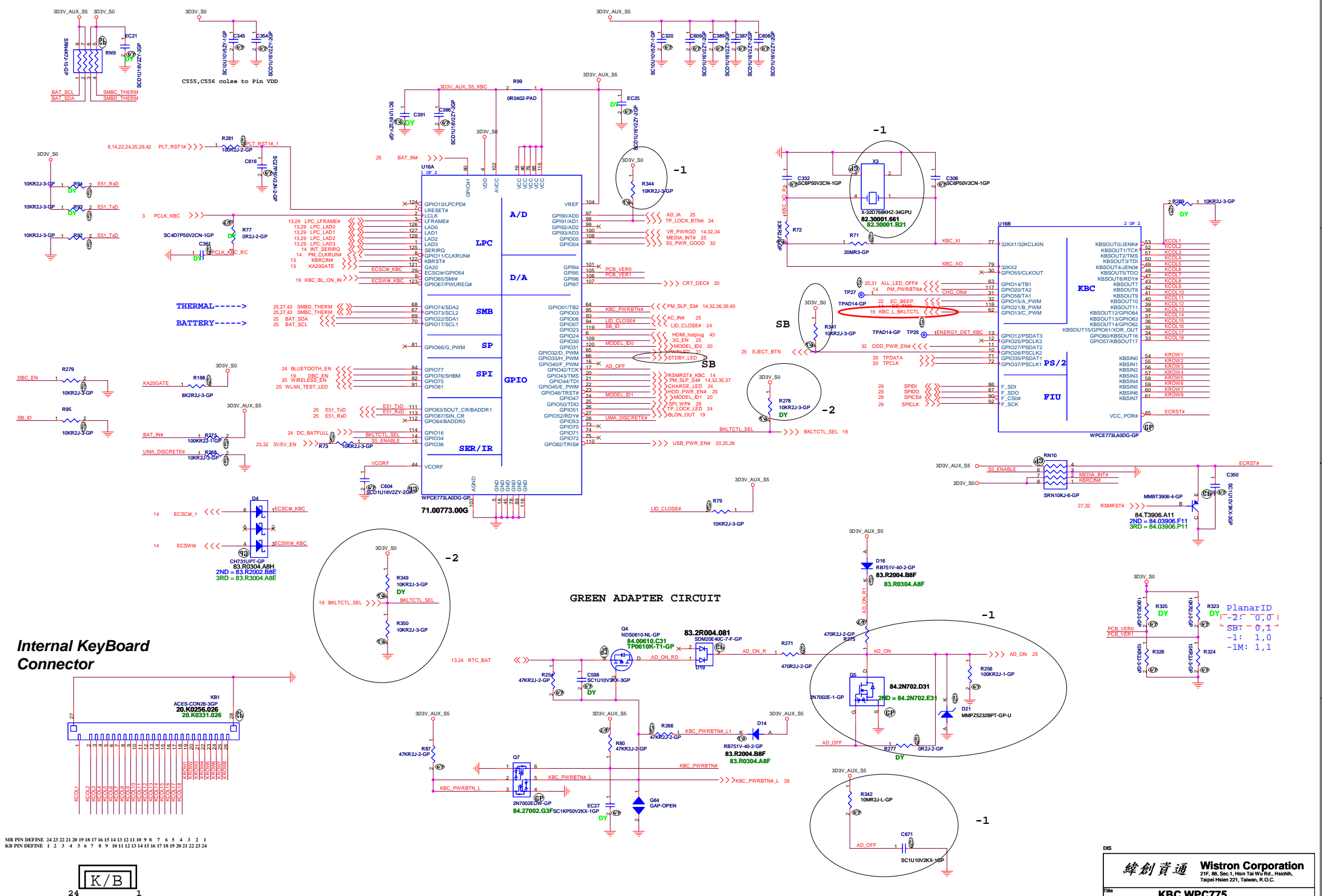
Date: Tuesday, April 28, 2009

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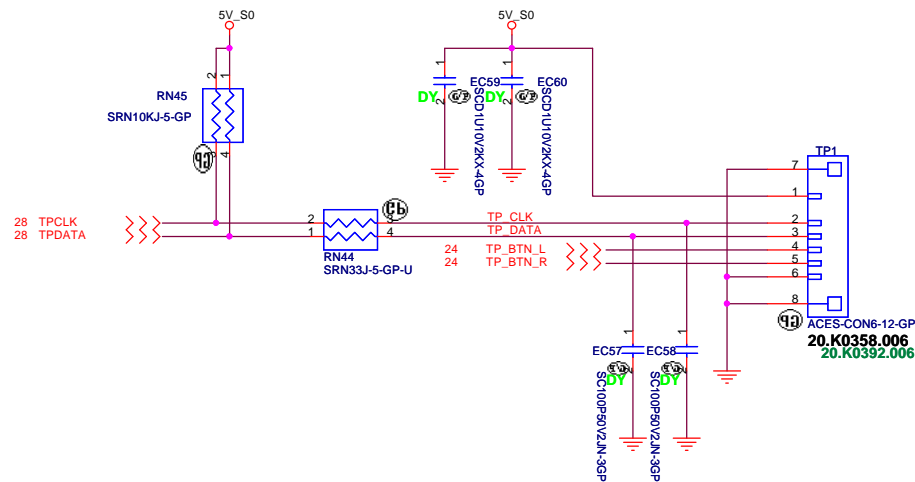


Channel 1: CPU
Channel 2: Palmrest
Channel 3: T8

SHDN_SEL		TRIP SET	
PULL UP RESISTOR	MODE OF OPERATION	Ttrip(degree)	RSET(1%)
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED,REC DISABLED	85	562
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED,REC ENABLED	86	604
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED	87	649
15K OHM	INTERNAL DIODE	88	698
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED	89	750
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED	90	787
		91	845
		92	909
		93	953
		94	1020
		95	1100

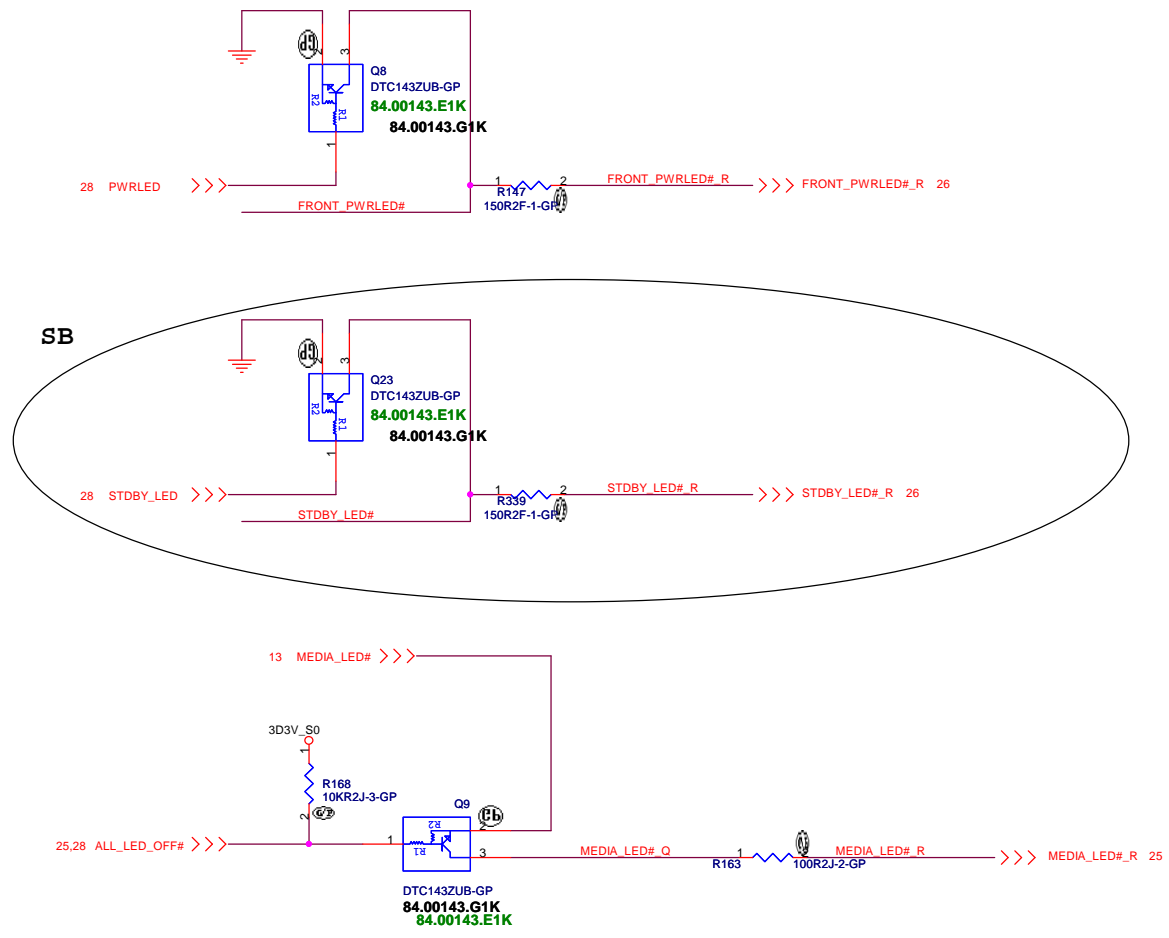


TOUCH PAD

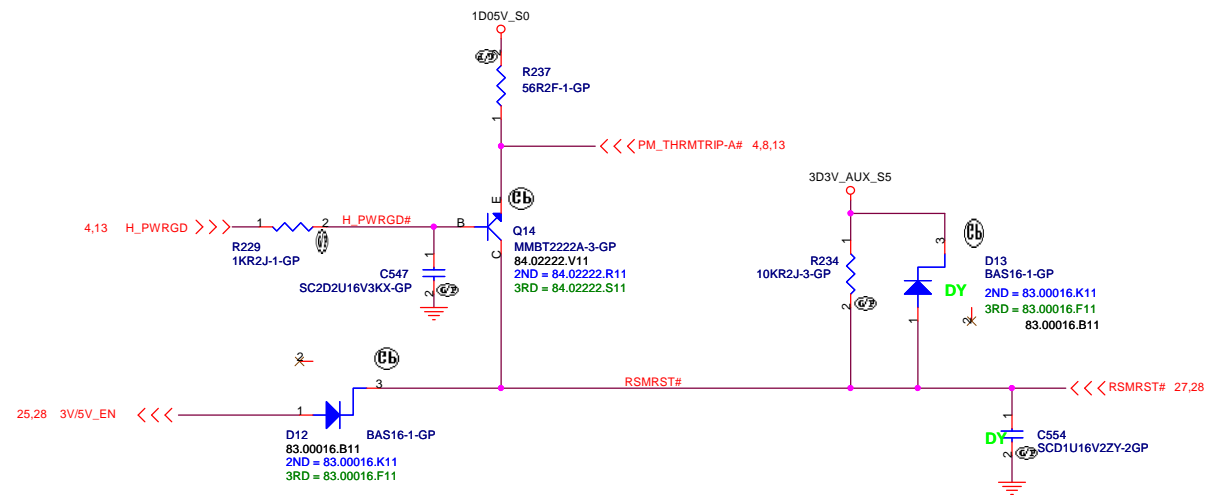
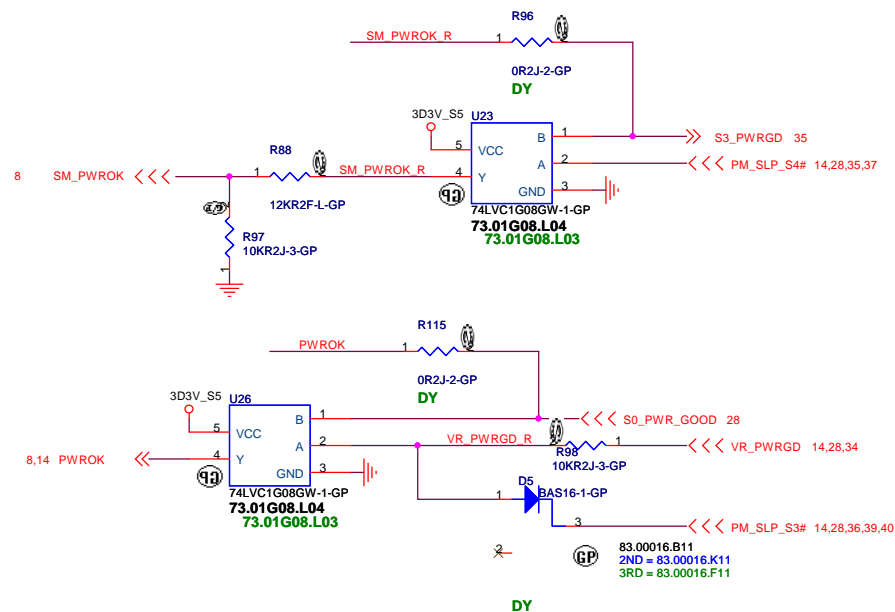
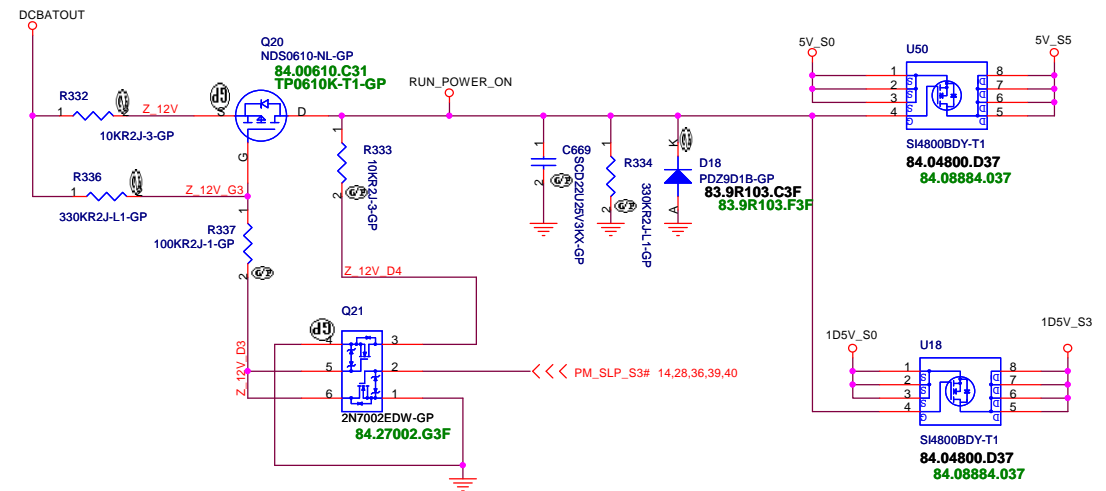
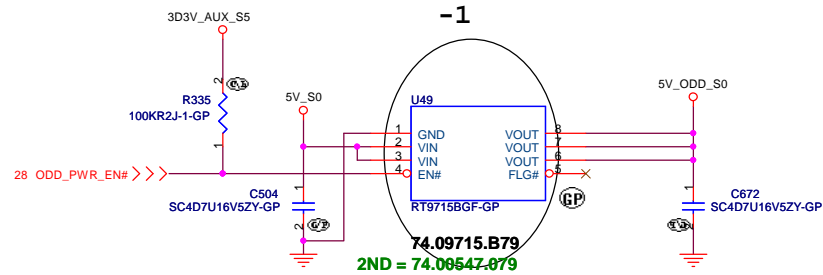


DIS

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Title			
Touch PAD			
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Run Power



DIS

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Taipei Hsien 221, Taiwan, R.O.C.

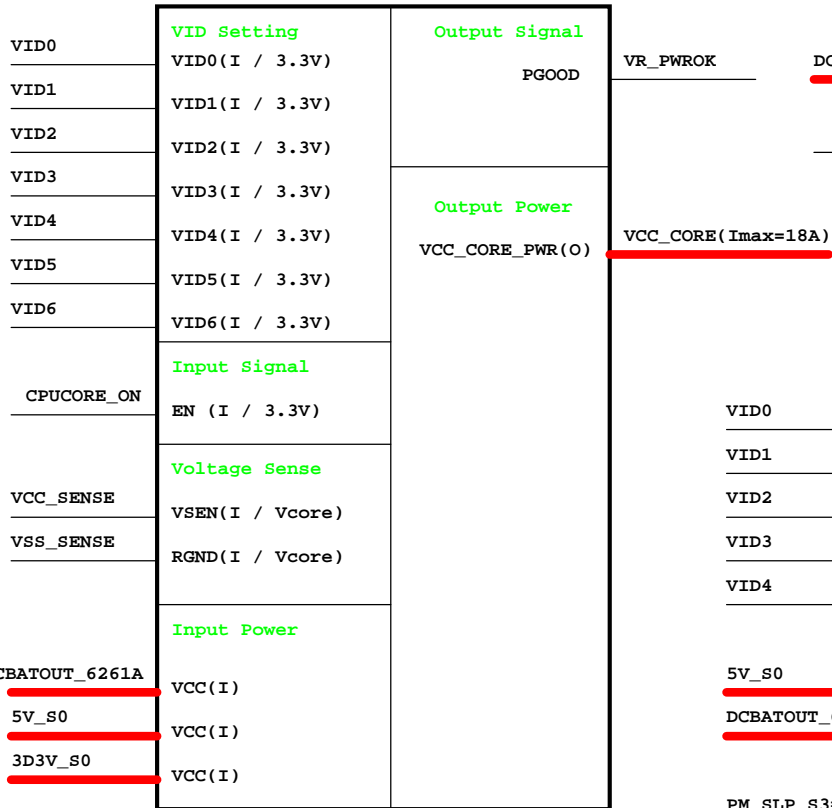
Title	RUN & ODD POWER
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Size	Document Number	Rev
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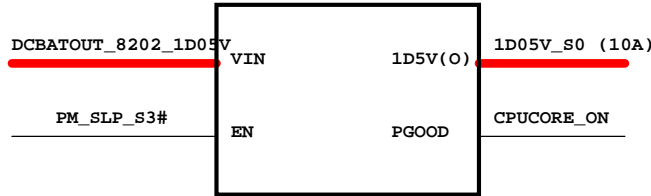
	JM41 Discrete	-2
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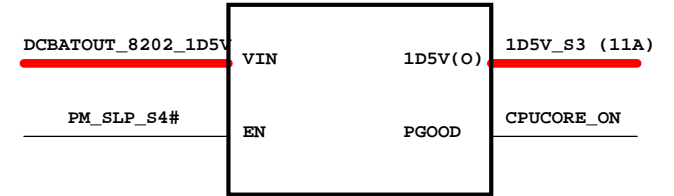
CPU_CORE
ISL6261A



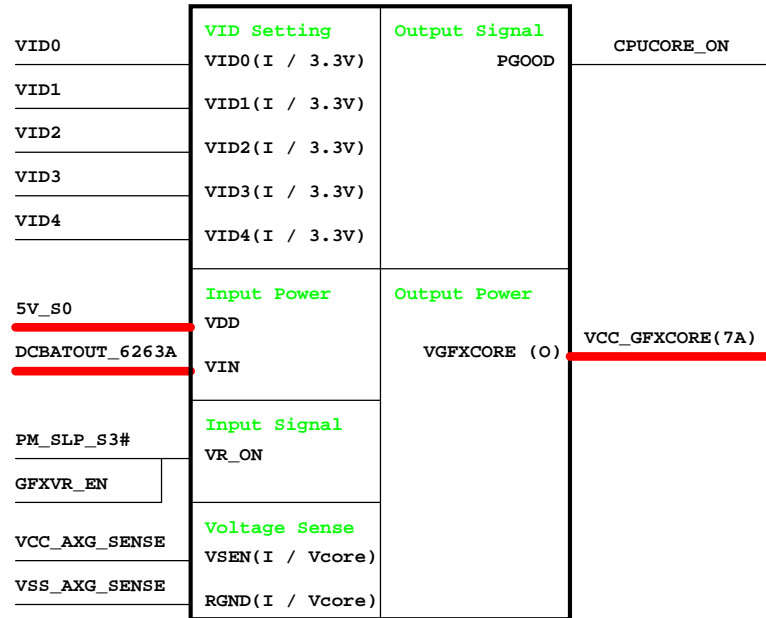
RT8202 1D05V_S0



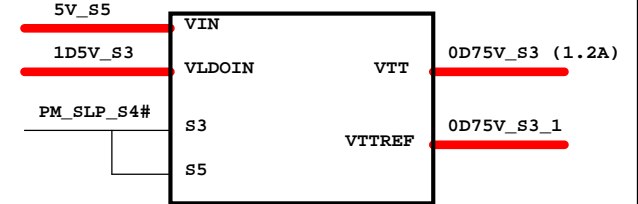
RT8202 1D5V_S3



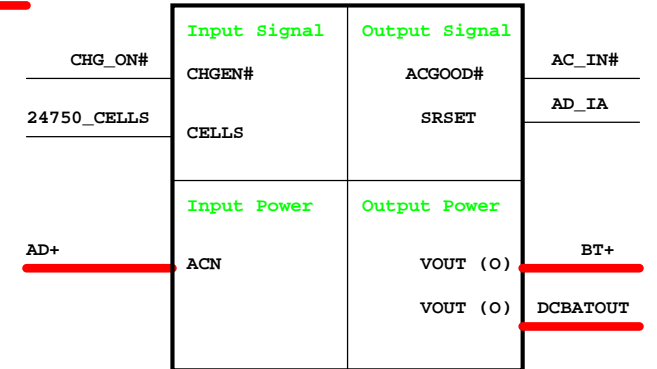
GFX_CORE
ISL6263A



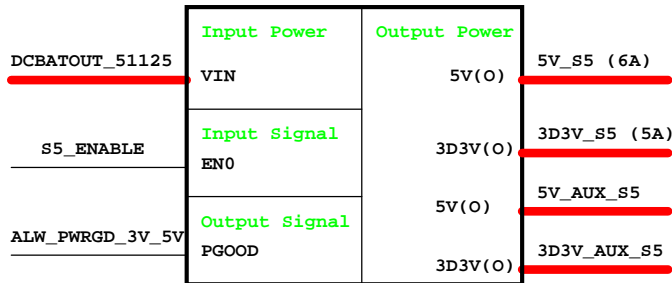
RT9026 0D9V_S0



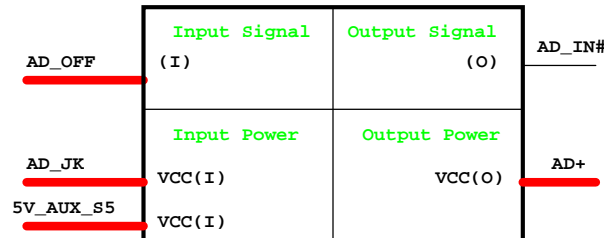
Charger MAX8731A



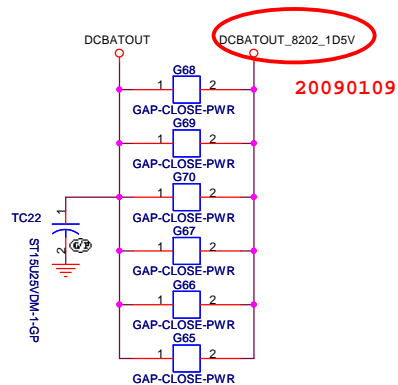
TPS51125
5V/3D3V



Adapter

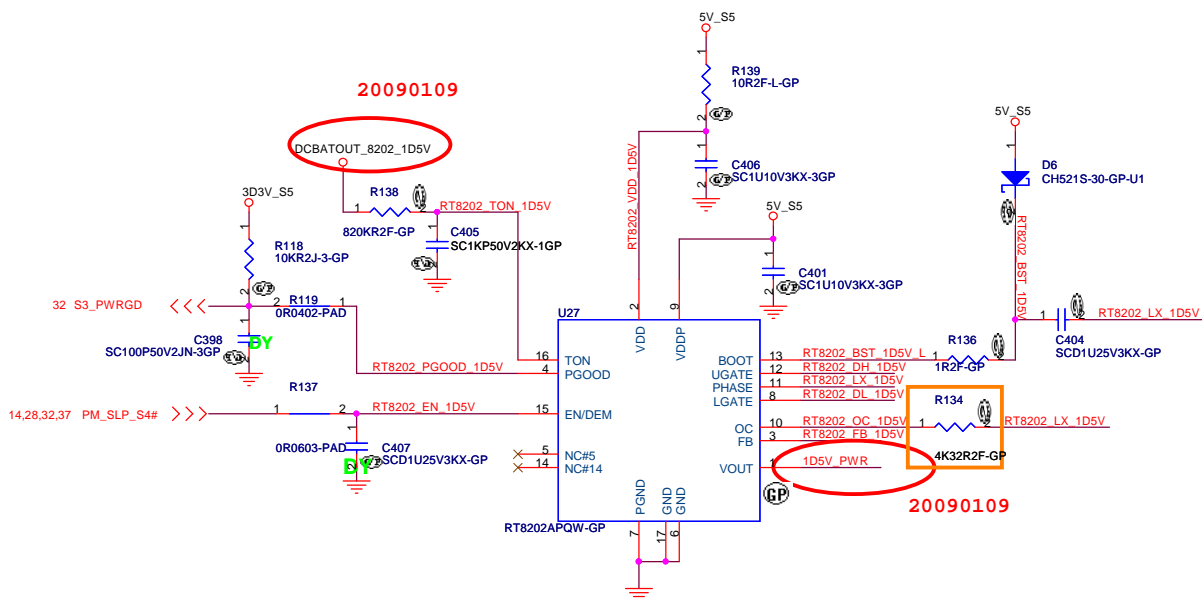


緯創資通 Wistron Corporation
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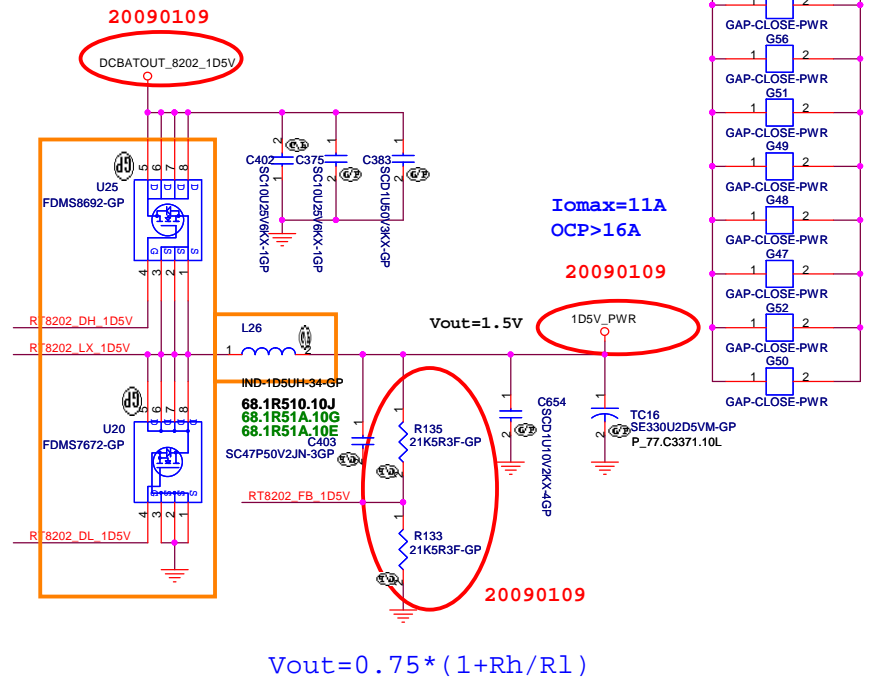


20090109

DCBATOUT_8202_1D5V



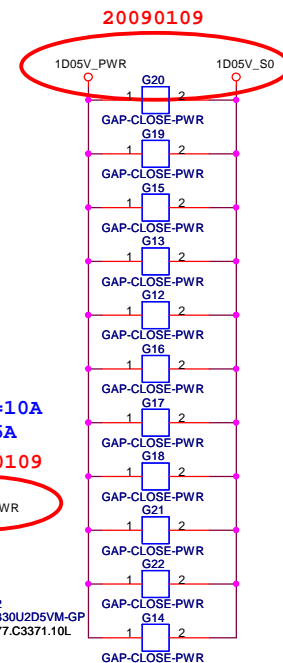
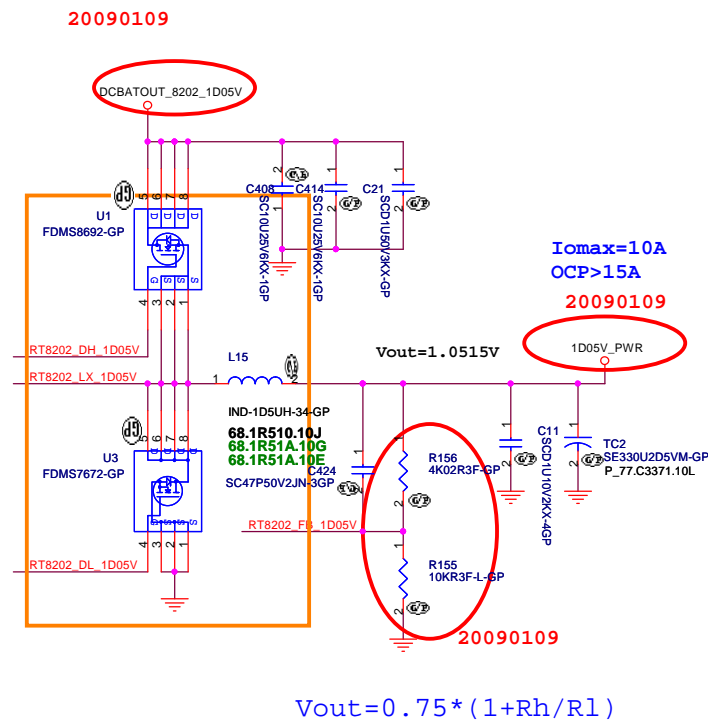
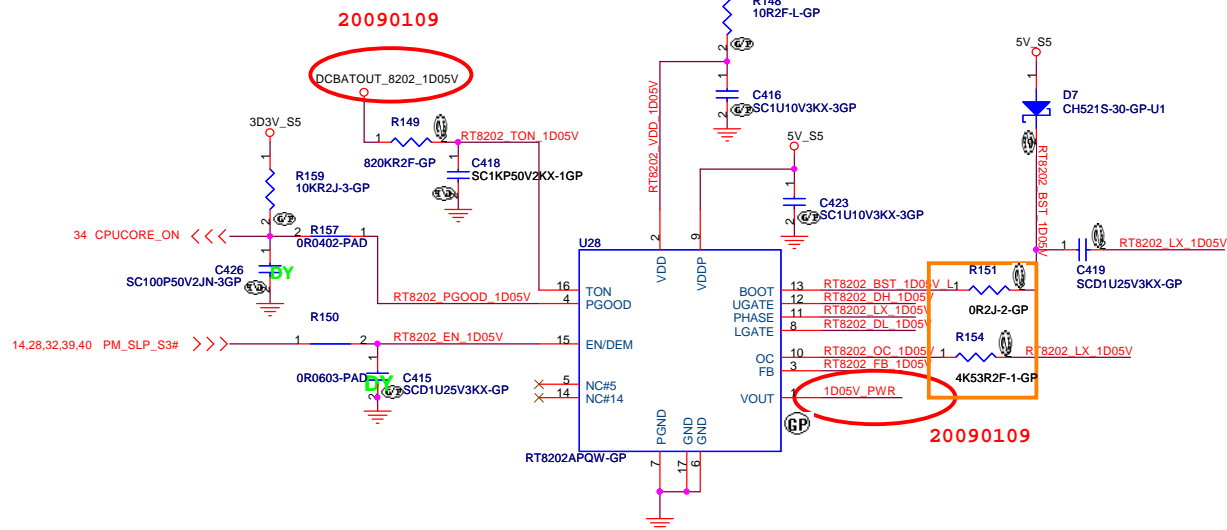
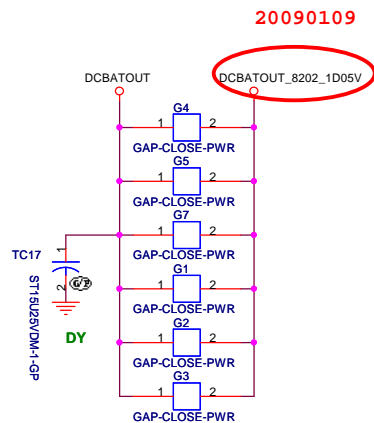
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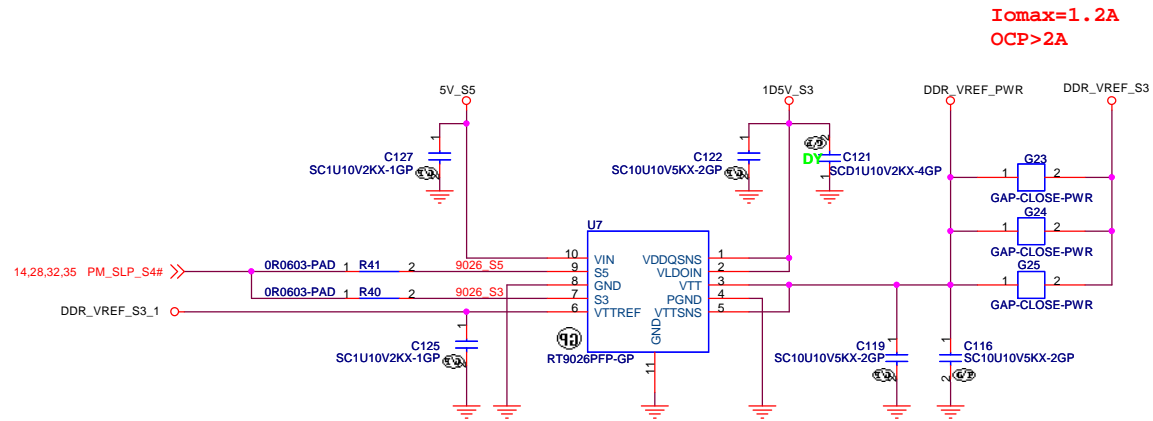


Iomax=11A
OCP>16A

20090109

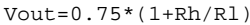
$$V_{out} = 0.75 * (1 + R_h / R_l)$$



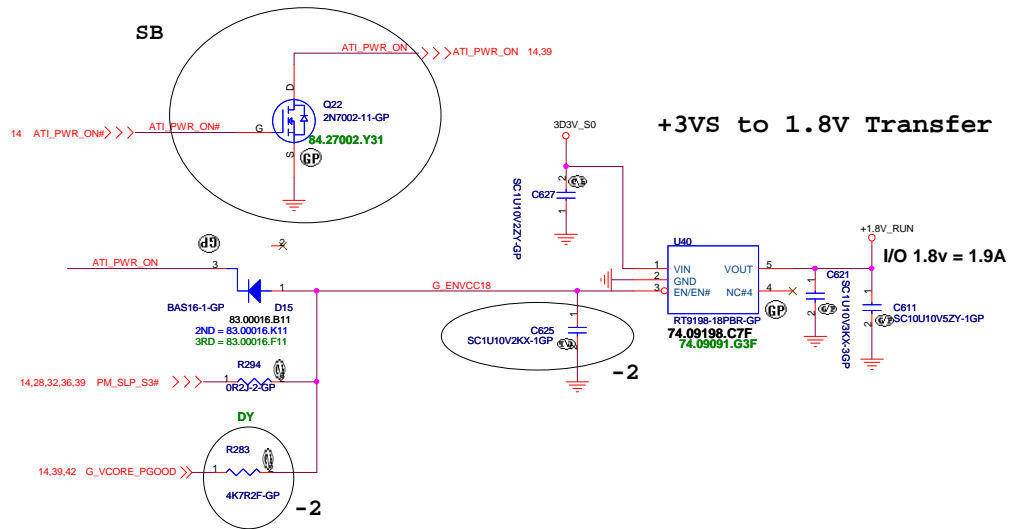


DIS

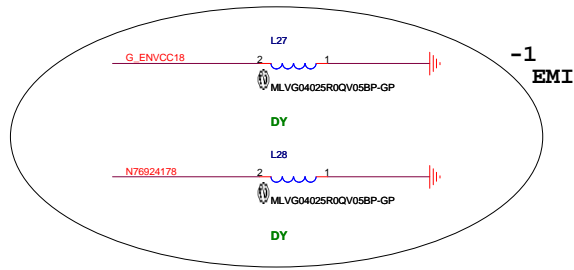
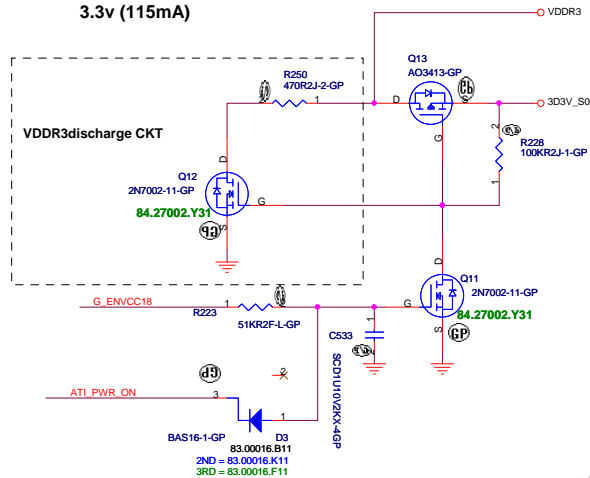
緯創資通		Wistron Corporation	
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Title			
RT9026 0D75V			
Size	Document Number	Rev	
A3	JM41 Discrete	-2	
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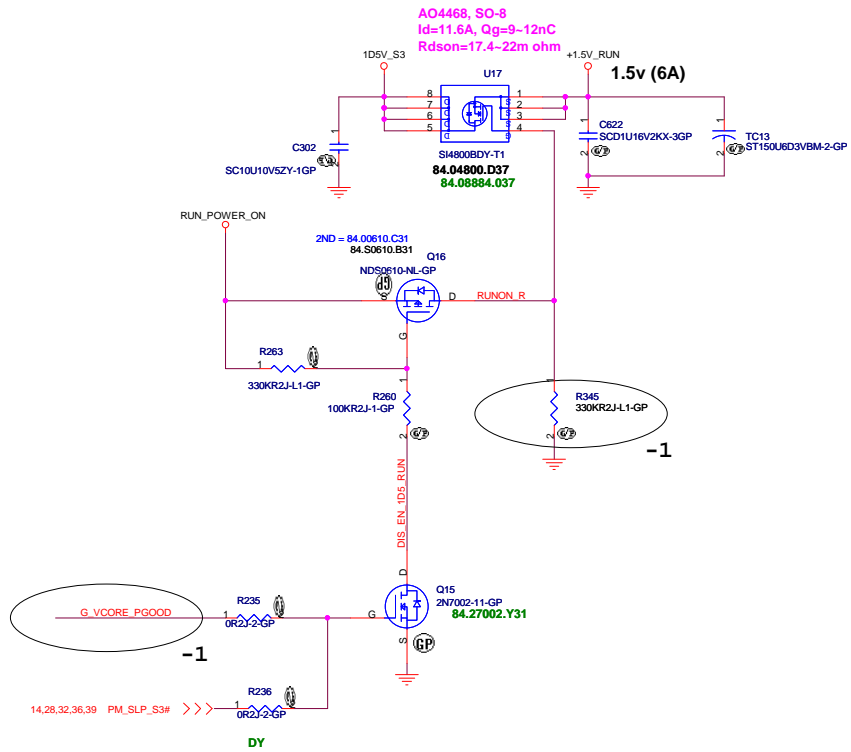
M92_LP core power			M92_XT core power		
ALTV1	ALTV0	Vout	ALTV1	ALTV0	Vout
0	0	0.90V	0	0	0.90V
0	1	1.09V	0	1	1.09V
1	0	0.95V	1	0	1.2V



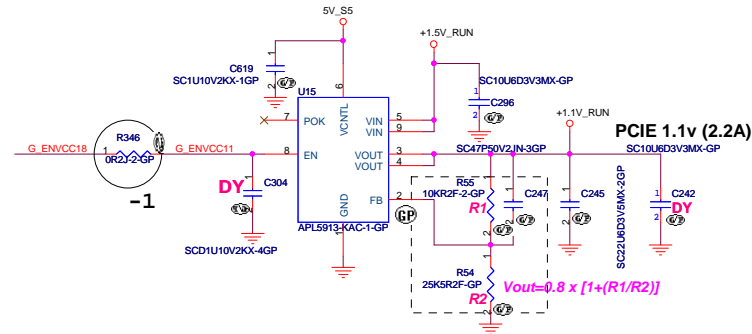
+3VS to 3.3V_DELAY Transfer
3.3v (115mA)



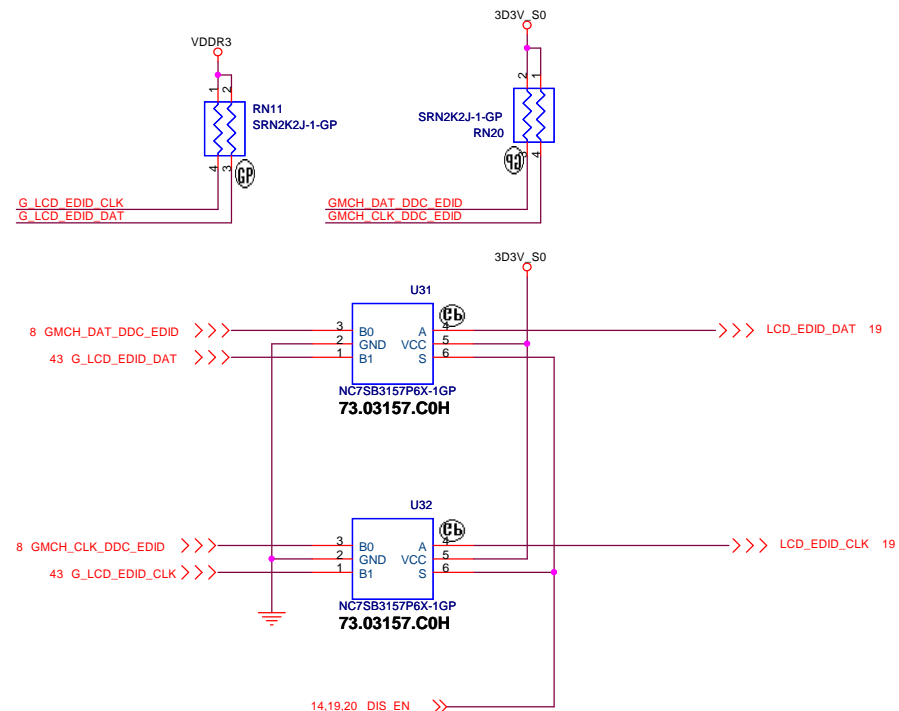
+1.5V to +1.5VS_RUN Transfer



+1.5v to PCIE 1.1V Transfer

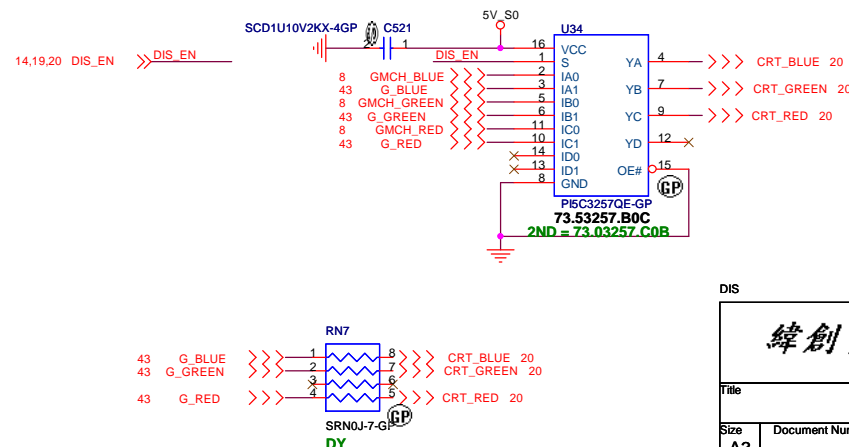


D/S			
緯創資通		Wistron Corporation	
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Title			
M92S2 power			
Size	Document Number		Rev
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\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

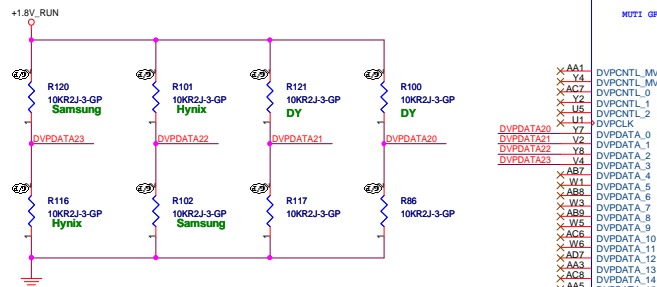
FUNCTION TABLE		
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-



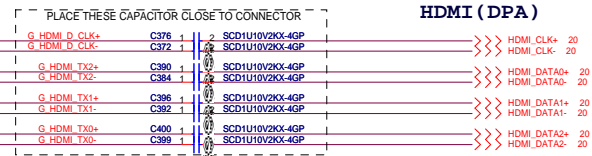
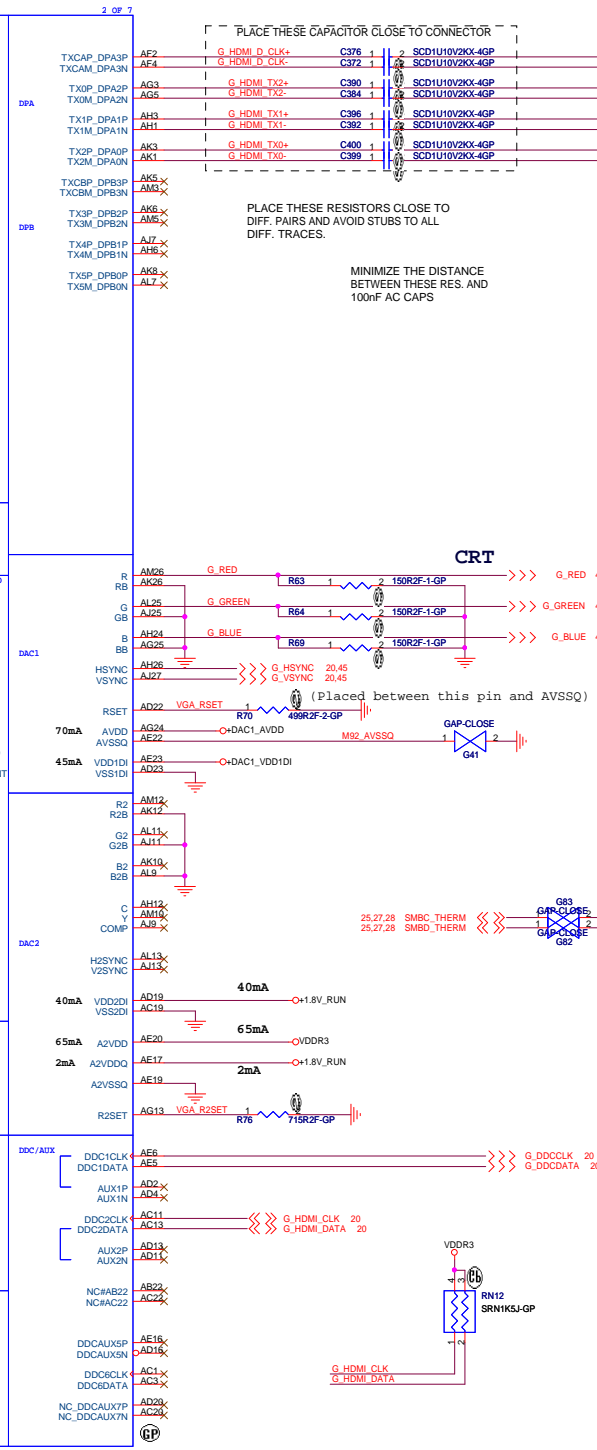
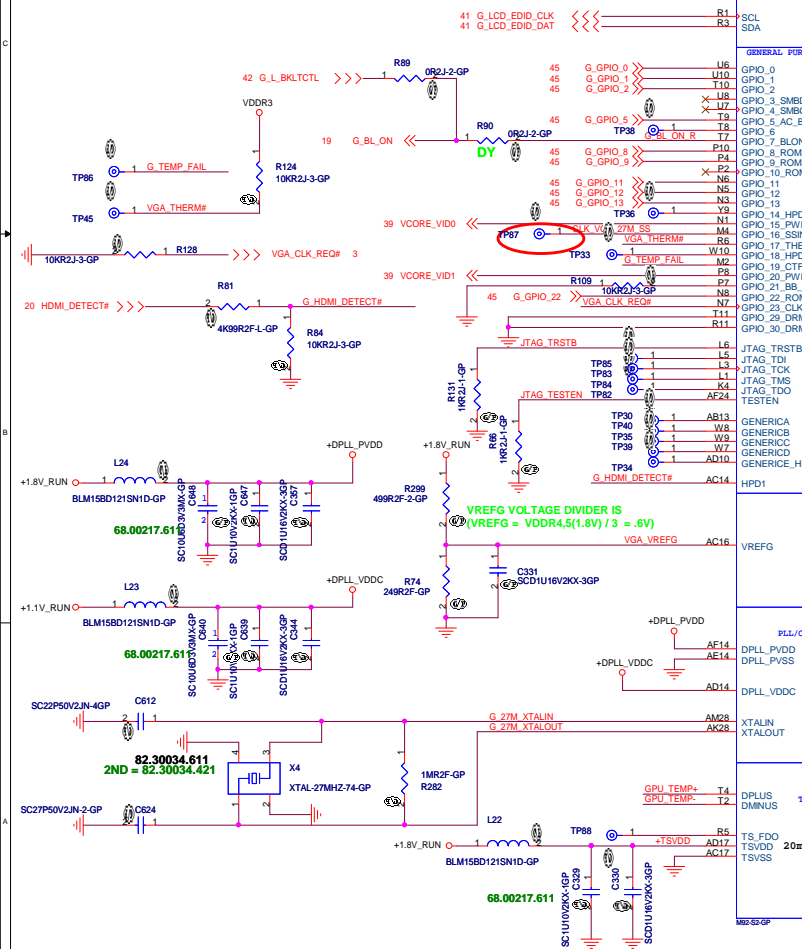


SSID = VIDEO

```
DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung
```

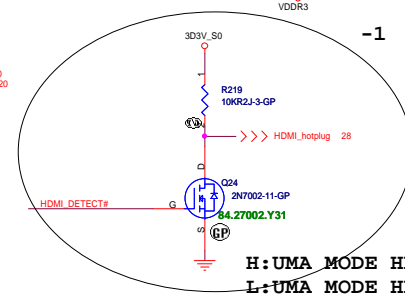
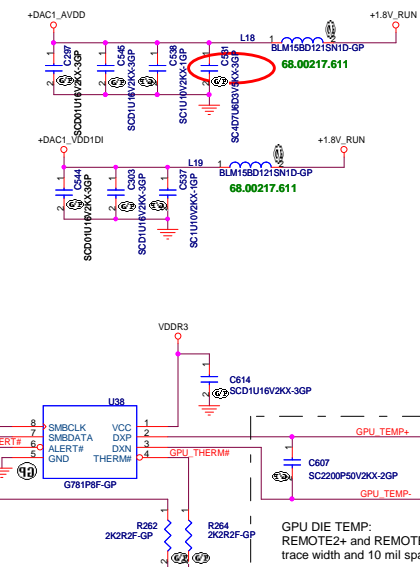


STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO 0000 - GDDR3 16Mx32 Qimonda 0001 - GDDR3 32Mx32 Hynix 0010 - GDDR3 32Mx32 Qimonda 0011 - GDDR3 32Mx32 Samsung



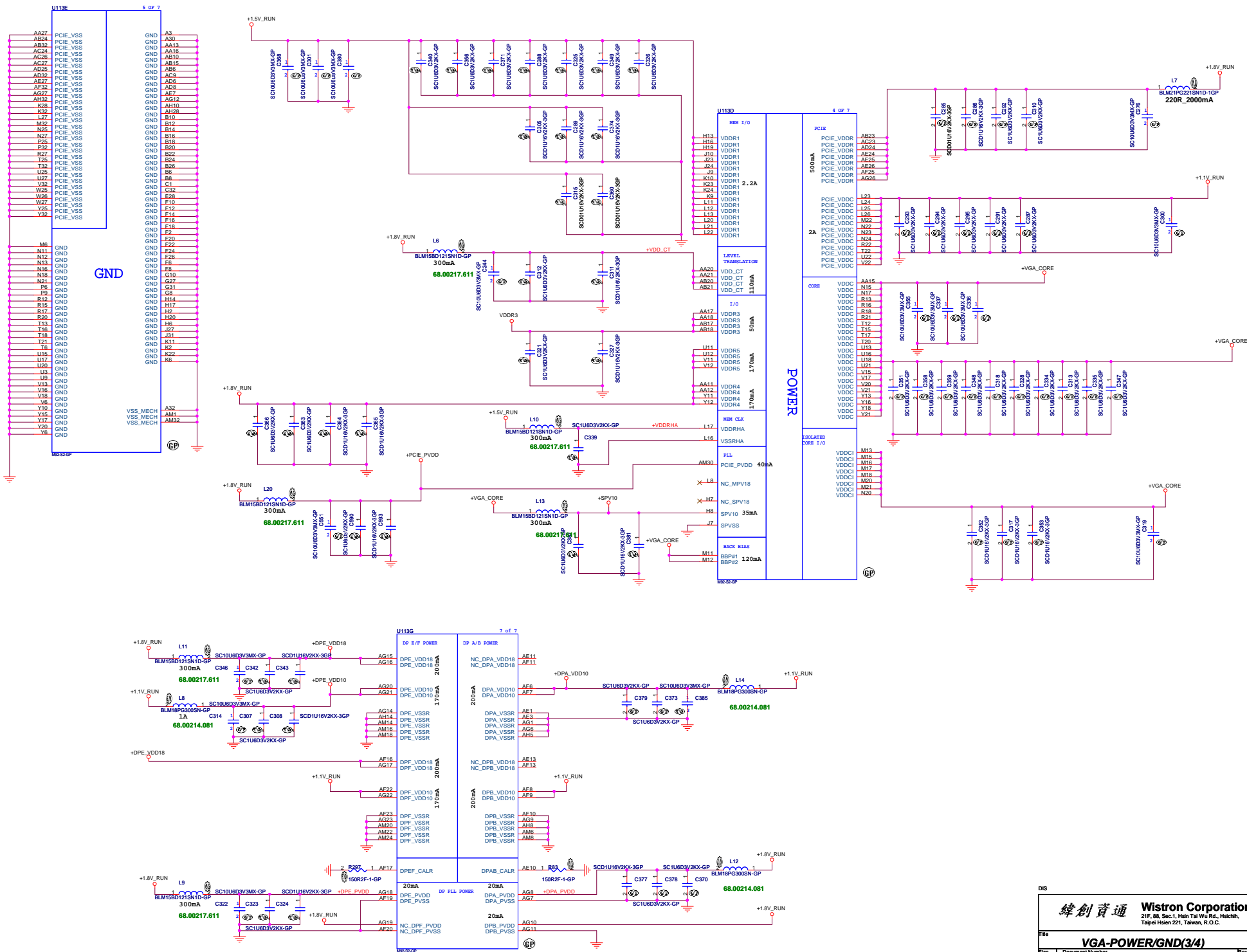
PLACE THESE RESISTORS CLOSE TO
DIFF. PAIRS AND AVOID STUBS TO ALL
DIFF. TRACES.

MINIMIZE THE DISTANCE
BETWEEN THESE RES. AND
100nF AC CAPS

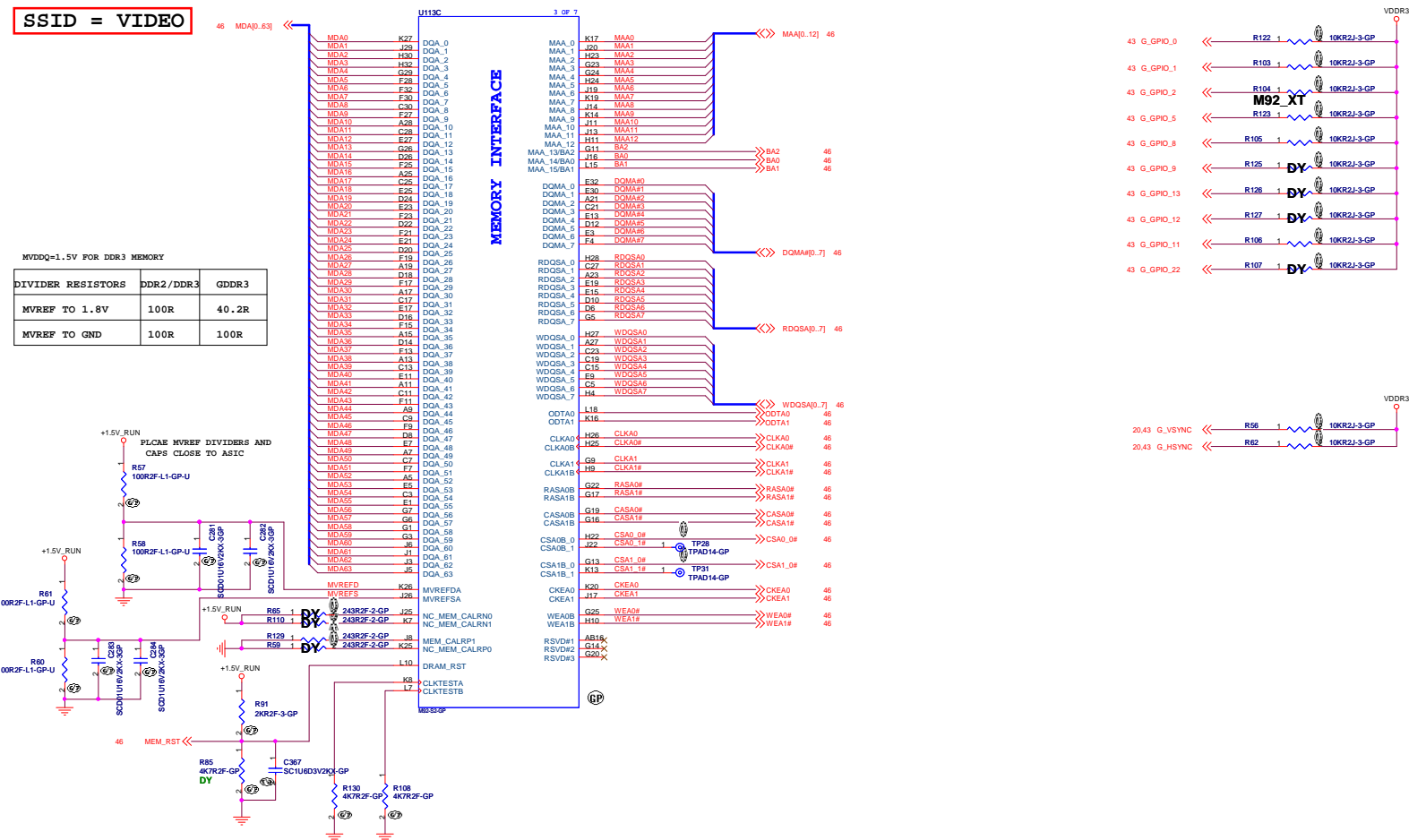


```
H:UMA MODE HDMI PLUG_OUT
L:UMA MODE HDMI PLUG IN
```

SSID = VIDEO



SSID = VIDEO



ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESE

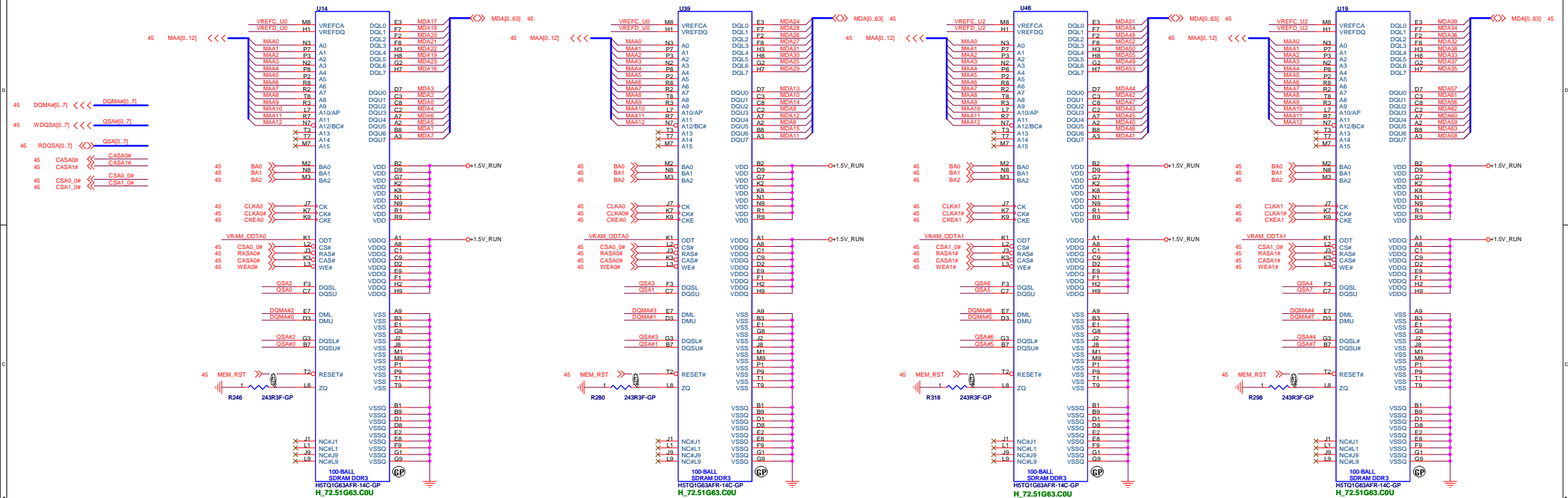
GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1			
Size of the primary memory apertures		GPIO[9,13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V	128MB	x000	ST Microelectronics	M25P05A	0100
	256MB	x001		M25P10A	0101
	64MB	x010		M25P20	0101
	32MB	x		M25P40	0101
	512MB	x		M25P80	0101
	1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
	2GB	x		Pm25LV010A	0101
	4GB	x			

STRAPS	PIN	DESCRIPTION
TX_PWR5_ENB (Internal PD)	GPIO0	Transmitter Power Savings Enable 0= 50k Tx output swing 1= Pull Tx output swing ✓
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled ✓
BIF_GEN2_EN_A	GPIO2	✓ 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	0= Disable CLKREQ# power management capability 1= Enable CLKREQ# power management capability ✓
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	✓ Enable external BIOS ROM device 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00=No audio function 01=Audio for DisplayPort and HDMI (if adapter is detected) 10=Audio for DisplayPort only 11=Audio for both DisplayPort and HDMI ✓

512MB DDR3



Samsung : K4W1G1646E-EC12

Hynix : H5TQ1G63BFR-12C





JM41/JM51 DIS Schematic EC Tracking Record

EC #/ Page / Description / Part Affected

EC SC01/11/connect NB1.A31 to GND(For power save)
EC SC02/14/net DIS_EN pull high 10K to 3D3V_S0
EC SC03/20/CN2.pin35 change to AGND
EC SC04/22/R311 change to 39.2K
EC SC05/22/U24.pin2 change to AGND
EC SC06/26/BTB2.pin9 add stand by led control signal
EC SC07/28/U16.pin66 add stand by led control signal
EC SC08/28/add circuit to support green adapter
EC SC09/28/net EJECT_BTN pull high 10K to 3D3V_S0
EC SC10/31/add circuit to stand by led control
EC SC11/40/change GPU power enable signal to ATI_PWR_ON#(low active)
EC SC12/41/change U11 power plane to 1D8V_NB_S0

DIS

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY

Size
A2

Document Number

Rev

JM41 Discrete

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