

Compal Confidential

Model Name : V5MM2_Ezel_HW

File Name : LA-A021P

Compal Confidential

M/B Schematics Document

Intel Shark Bay ULT (Hasswell + Lynx Point-LP)

nVidia N14P-GT

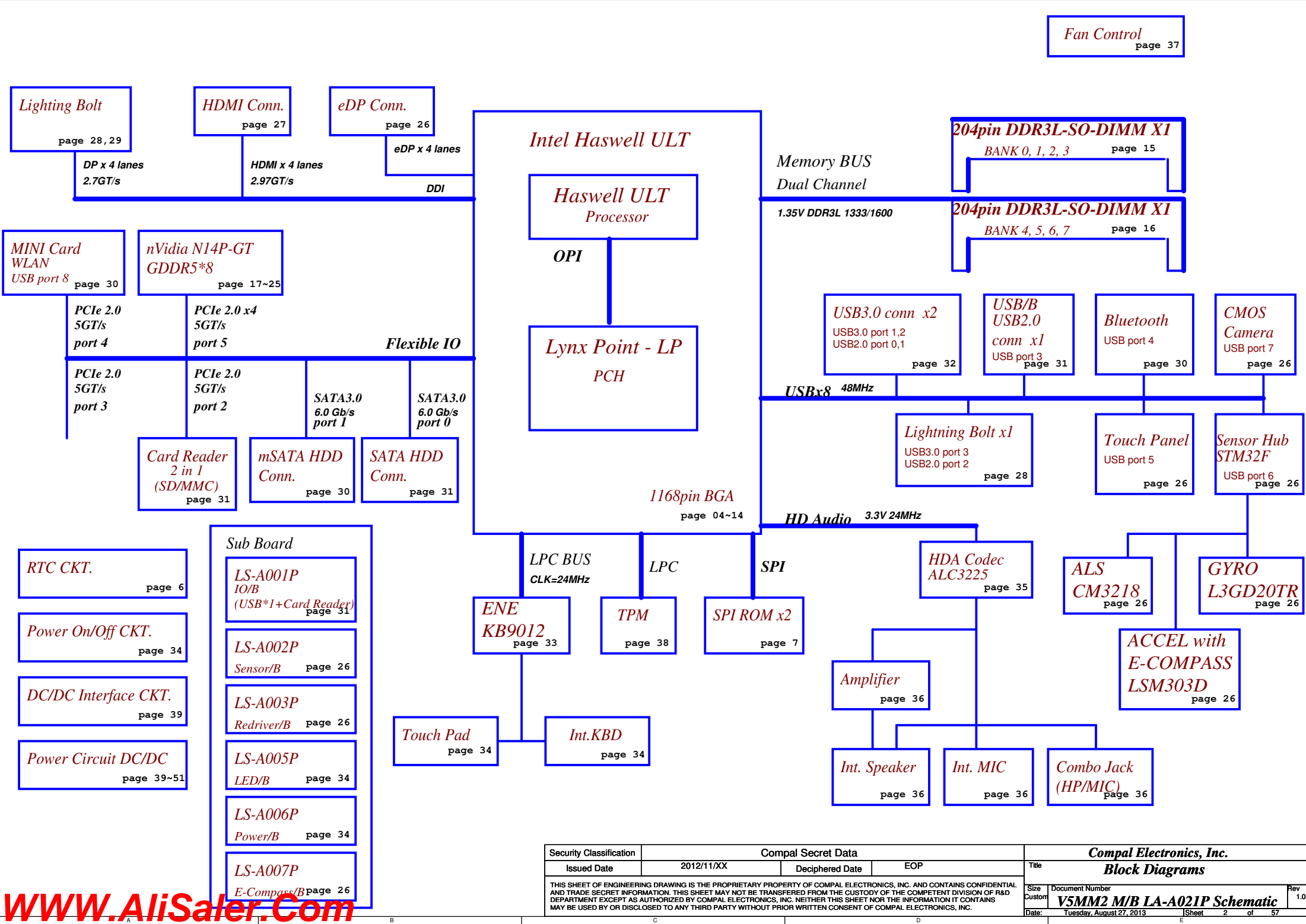
2013-08-XX

REV: 1.0

ZZZ1

| Part Number | Description |
|-------------|---|
| DAZ0YY00100 | PCB V5MM2 LA-A021P LS-A001P/A002P/A003P/A005P/A006P/A007P |

| | | | | | |
|---|--------------------|-----------------|-----|--------------------------------|---------------|
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| | | | | V5MM2 M/B LA-A021P Schematic | 1.0 |
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page 27

eDP Conn.
page 26

DP x 4 lanes
2.7GT/s

HDMI x 4 lanes
2.97GT/s

eDP x 4 lanes

DDI

MINI Card
WLAN
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nVidia N14P-GT
GDDR5*8
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PCIe 2.0
5GT/s
port 4

PCIe 2.0 x4
5GT/s
port 5

Flexible IO

PCIe 2.0
5GT/s
port 3

PCIe 2.0
5GT/s
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SATA3.0
6.0 Gb/s
port 1

SATA3.0
6.0 Gb/s
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SATA HDD
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DC/DC Interface CKT.
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Intel Haswell ULT

Haswell ULT
Processor

OPI

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LPC BUS
CLK=24MHz

LPC

SPI

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KB9012
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SPI ROM x2
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Touch Pad
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Int.KBD
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Memory BUS
Dual Channel

1.35V DDR3L 1333/1600

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204pin DDR3L-SO-DIMM X1
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CMOS
Camera
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USBx8 48MHz

Lightning Bolt x1
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USB2.0 port 2
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Touch Panel
USB port 5
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Sensor Hub
STM32F
USB port 6
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HD Audio 3.3V 24MHz

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ALC3225
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Amplifier
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Int. MIC
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GYRO
L3GD20TR
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ACCEL with
E-COMPASS
LSM303D
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| | | | | | | |
|---|--------------------|-----------------|-----|--------------------------|--------------------------|---------------|
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| Power Plane | Description | S1 | S3 | S5 |
|-------------|--|-----|-----|-----|
| VIN | Adapter power supply (19V) | N/A | N/A | N/A |
| BATT+ | Battery power supply (12.6V) | N/A | N/A | N/A |
| B+ | AC or battery power rail for power circuit. | N/A | N/A | N/A |
| +CPU_CORE | Core voltage for CPU | ON | OFF | OFF |
| +VGA_CORE | Core voltage for GPU | ON | OFF | OFF |
| +0.675VS | +0.675VSP to +0.675VS switched power rail for DDR terminator | ON | OFF | OFF |
| +1.05VSDGPU | +1.05VSDGPU switched power rail for GPU | ON | OFF | OFF |
| +1.05VS_VTT | +1.05VSP to +1.05VS_VTT switched power rail for CPU | ON | OFF | OFF |
| +1.35V | +1.35VP to +1.35V power rail for DDRIII/L | ON | ON | OFF |
| +1.5VS | +1.5V to +1.5VS switched power rail | ON | OFF | OFF |
| +1.5VSDGPU | +1.5VSDGPUP to +1.5VSDGPU switched power rail for GPU | ON | OFF | OFF |
| | | | | |
| | | | | |
| +3VALW | +3VALW always on power rail | ON | ON | ON* |
| +3VLP | B+ to +3VLP power rail for suspend power | ON | ON | ON |
| +3VS | +3VALW to +3VS power rail | ON | OFF | OFF |
| +3VSDGPU | +3VS to +3VSDGPU switched power rail for GPU | ON | OFF | OFF |
| +5VALW | +5VALWP to +5VALW power rail | ON | ON | ON* |
| +5VS | +5VALW to +5VS switched power rail | ON | OFF | OFF |
| | | | | |
| +RTCVCC | RTC power | ON | ON | ON |
| | | | | |
| | | | | |
| | | | | |

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus2 address

| Device | Address | Device | Address |
|---------------|-----------|-----------------------------|-----------|
| Smart Battery | 0001 011X | On Board Thermal Sensor | 0100 110x |
| | | VGA Internal Thermal Sensor | 0100 000x |
| | | G Sensor | 0011 000x |

| Device | | Address | |
|----------|-------|-----------|--------|
| ChannelA | DIMM0 | 1001 000x | JDIMM1 |
| ChannelB | DIMM1 | 1001 010x | JDIMM2 |

| STATE \ SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|-----------------------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1 (Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

| | | | | |
|-----------------|---------------------|-------------------------------|-------------------------------|-------------------------------|
| Vcc | 3.3V +/- 5% | | | |
| Ra/Rc/Re | 100K +/- 5% | | | |
| Board ID | Rb / Rd / Rf | V_{AD_BID} min | V_{AD_BID} typ | V_{AD_BID} max |
| 0 | 0 | 0 V | 0 V | 0 V |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V |
| 4 | 56K +/- 5% | 1.036 V | 1.185 V | 1.264 V |
| 5 | 100K +/- 5% | 1.453 V | 1.650 V | 1.759 V |
| 6 | 200K +/- 5% | 1.935 V | 2.200 V | 2.341 V |
| 7 | NC | 2.500 V | 3.300 V | 3.300 V |

| Board ID | PCB Revision |
|----------|--------------|
| 0 | 0.1 |
| 1 | 0.2 |
| 2 | 0.3 |
| 3 | 0.4 |
| 4 | 1.0 |
| 5 | |
| 6 | |
| 7 | |

| USB 2.0 | Port | |
|---------|------|--------------------------|
| EHCI1 | 0 | USB3.0 Connector (Left) |
| | 1 | USB3.0 Connector (Left) |
| | 2 | Lightning Bolt mDP Conn. |
| | 3 | USB2.0 (USB/B) |
| | 4 | Mini Card (WLAN+BT) |
| | 5 | Touch Panel |
| | 6 | Sensor Hub |
| | 7 | Camera |

| | | |
|---------|------|-----------------------|
| USB 3.0 | Port | |
| XHCI | 1 | USB Port(Left 3.0) |
| | 2 | USB Port(Left 3.0) |
| | 3 | Lightning Bolt USB3.0 |
| | 4 | |

[illegible]

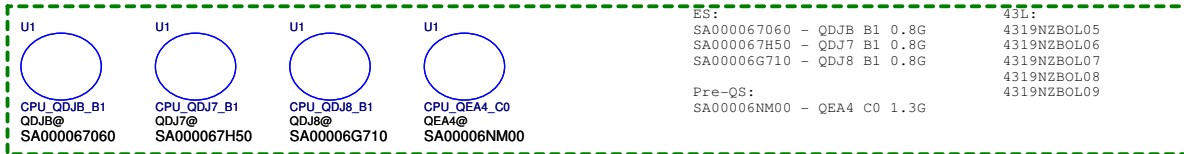
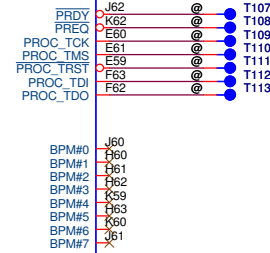
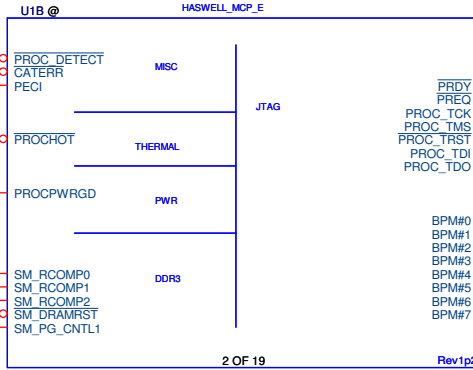
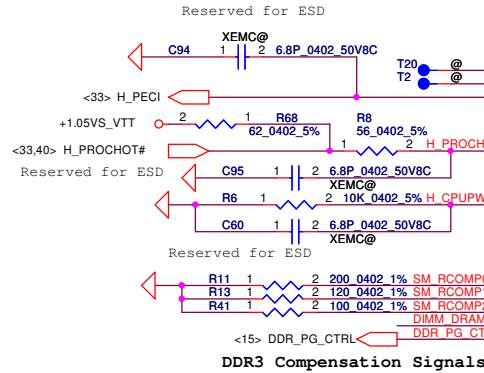
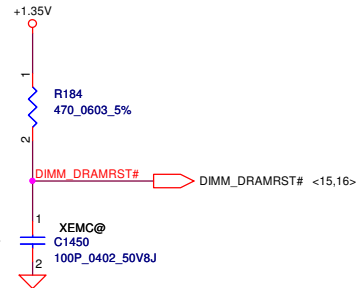
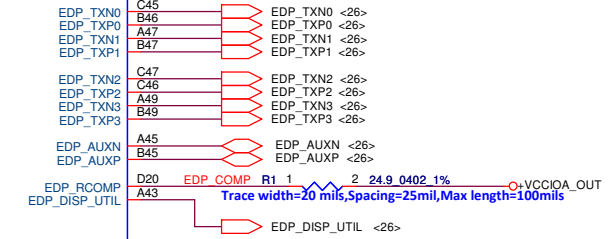
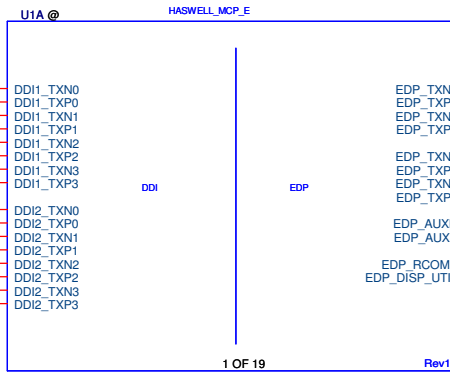
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DP for Lightning-Bolt

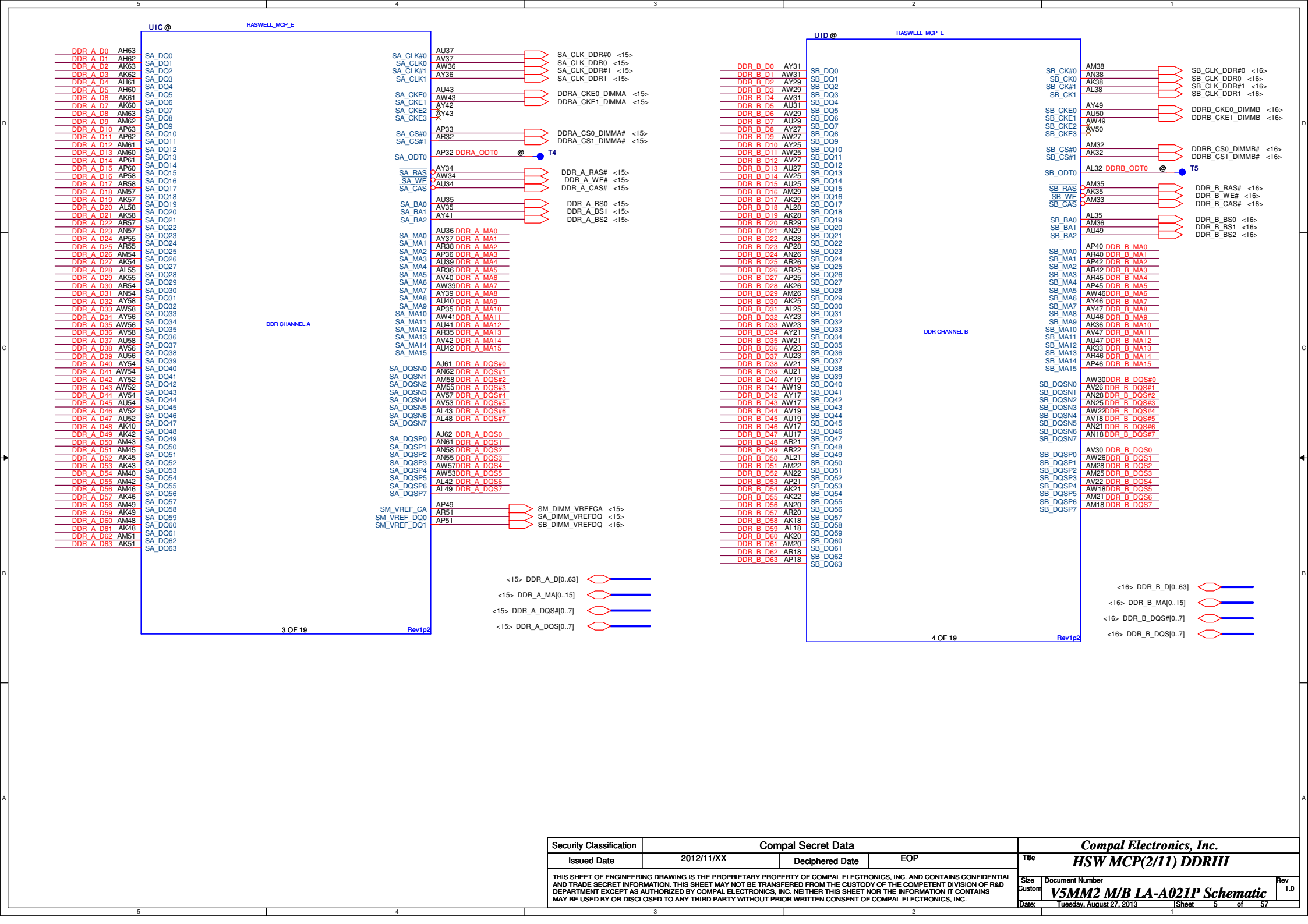
1, 0 Directly to mDP connector

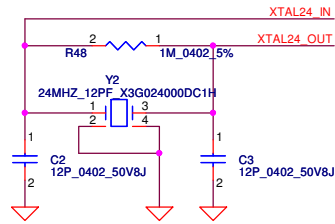
3, 2 connected to TI-HD3SS2521

HDMI

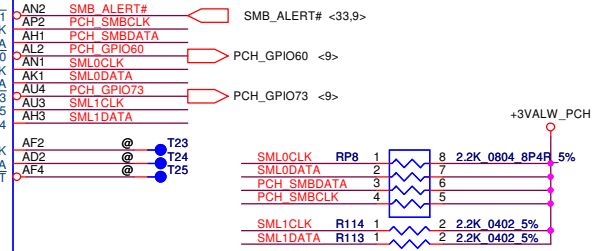
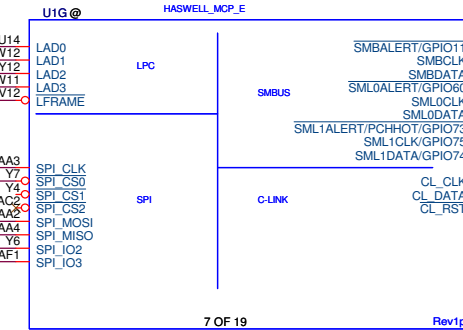
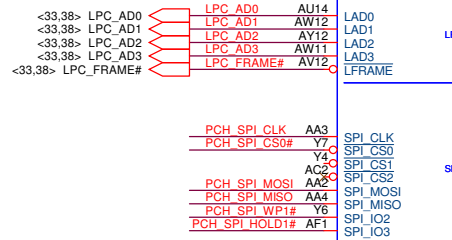
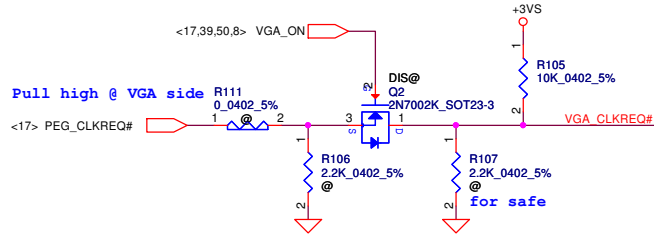
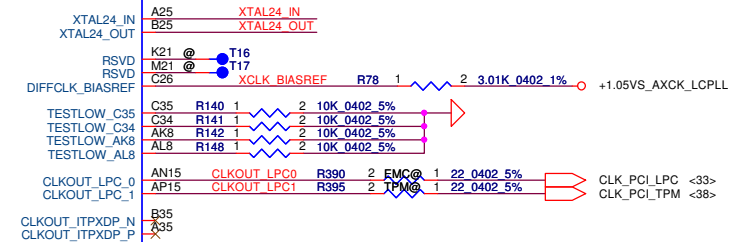
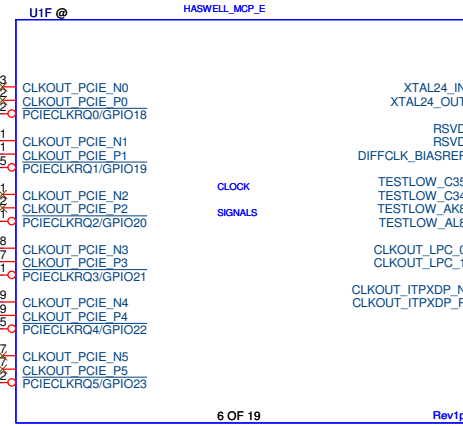
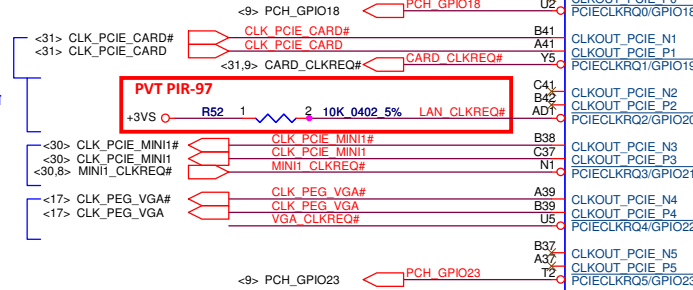


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| | | | | Date: Tuesday, August 27, 2013 | Rev 1.0 |

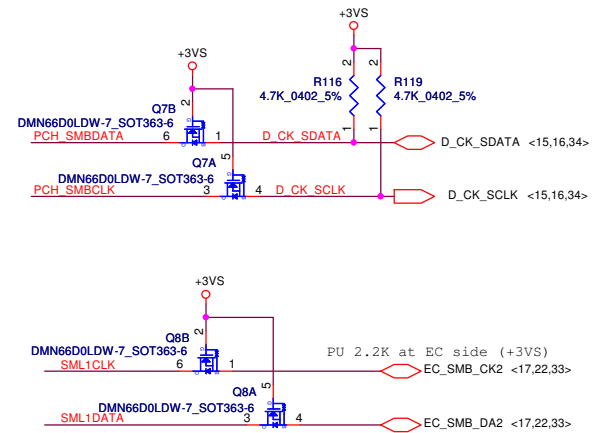
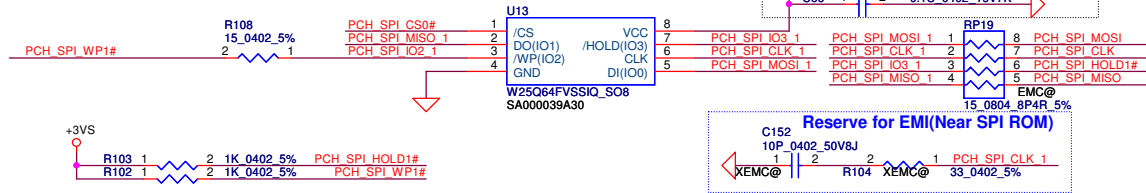




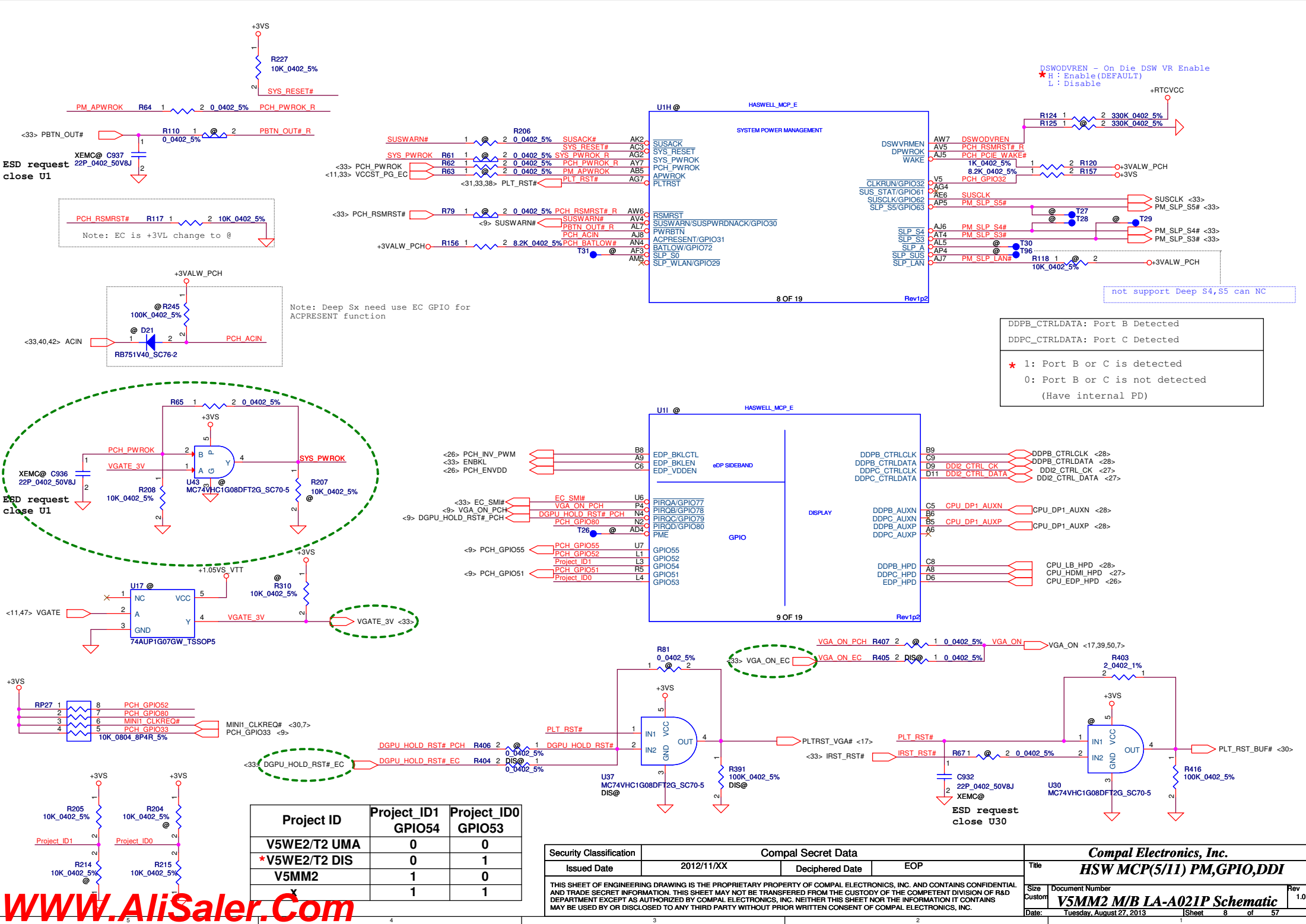
Card Reader
PCIE LAN
WLAN
VGA

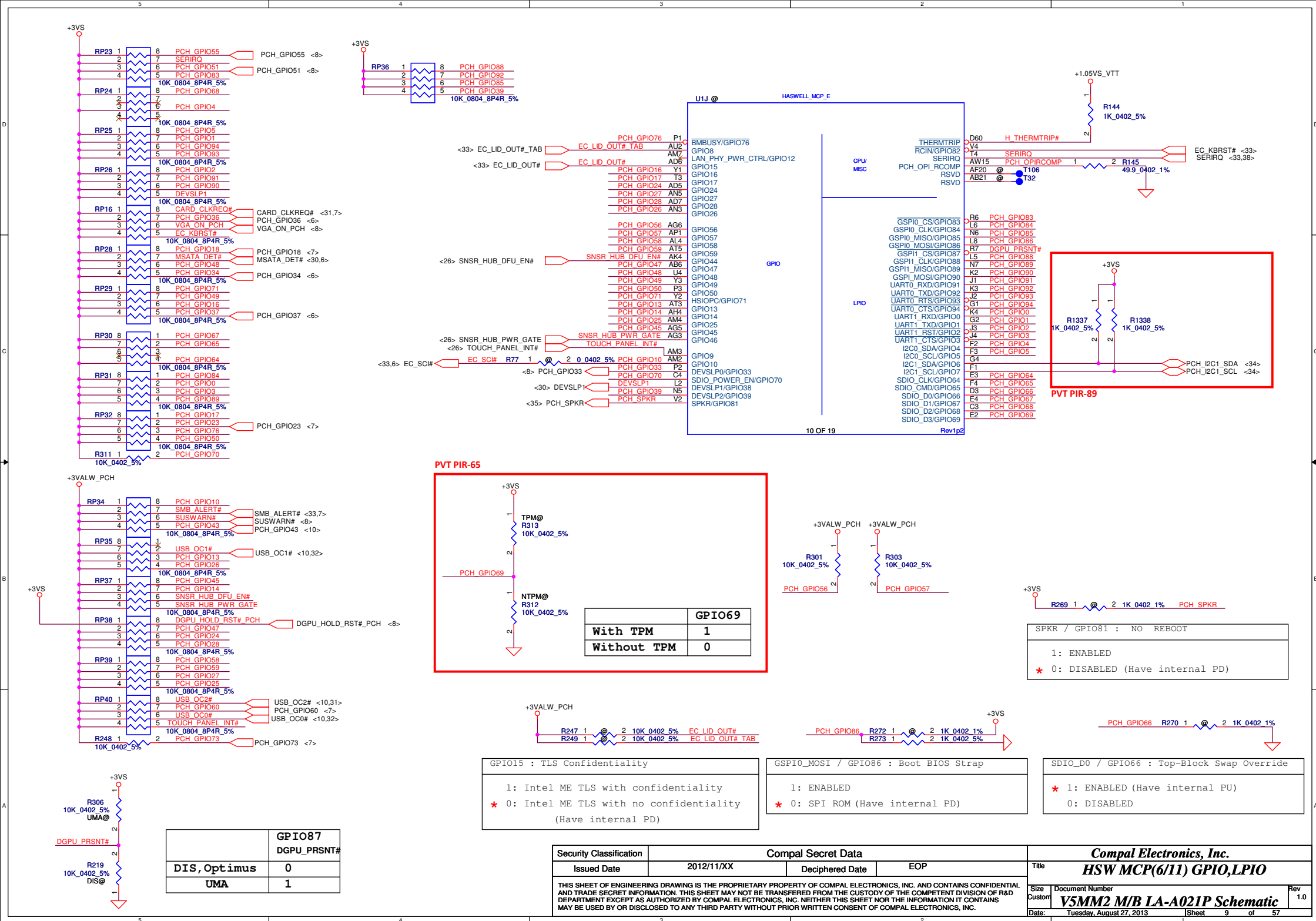


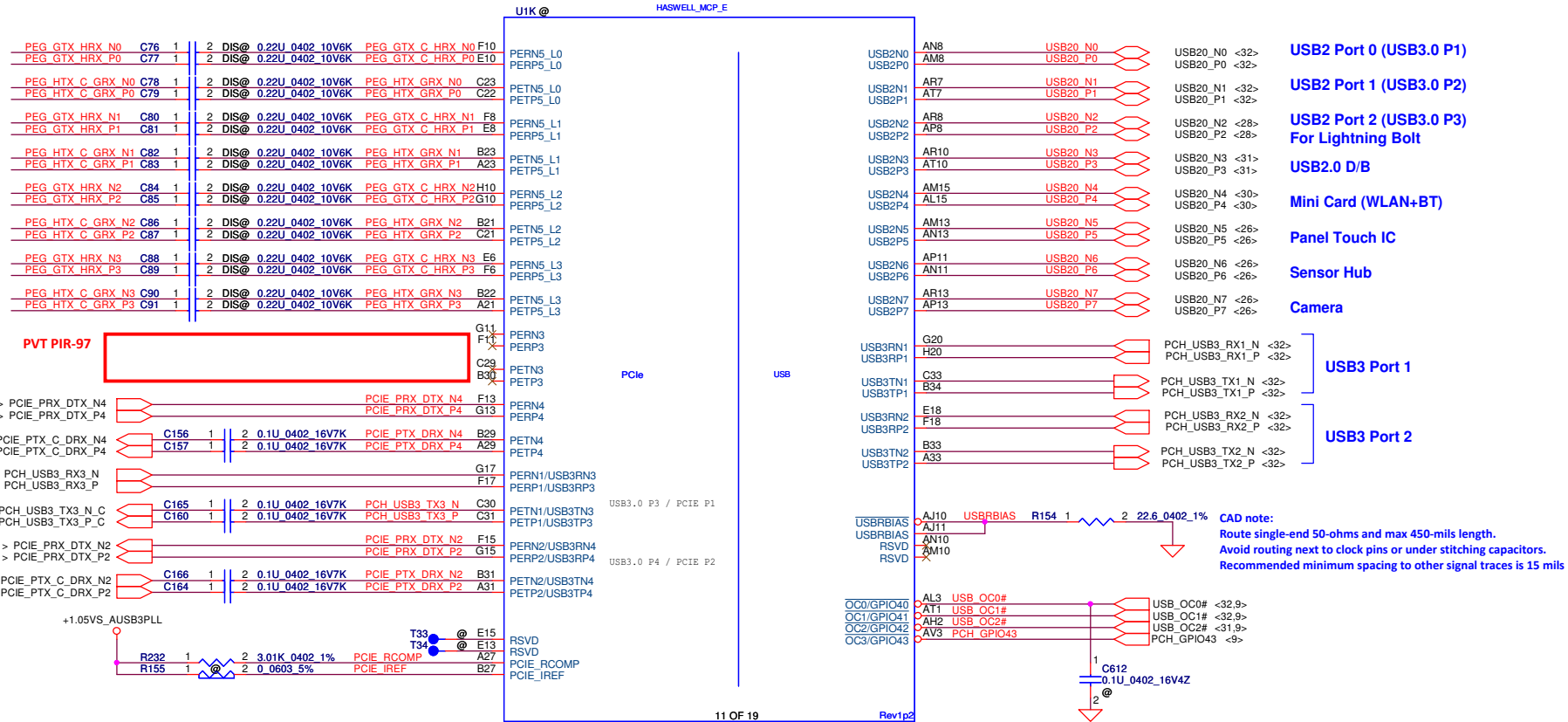
SPI ROM (8MByte)



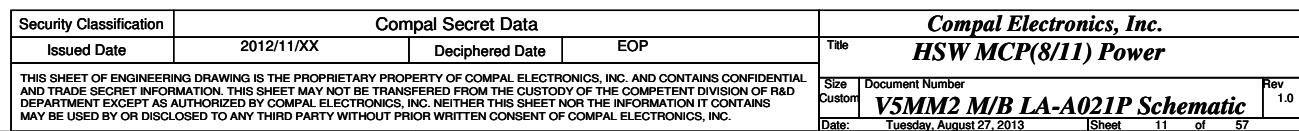
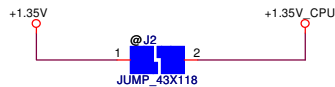
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| Size | Document Number | Date | | Sheet | Rev |
| Custom | V5MM2 M/B LA-A021P Schematic | Tuesday, August 27, 2013 | | 7 | 1.0 |
| | | | | Sheet | of |
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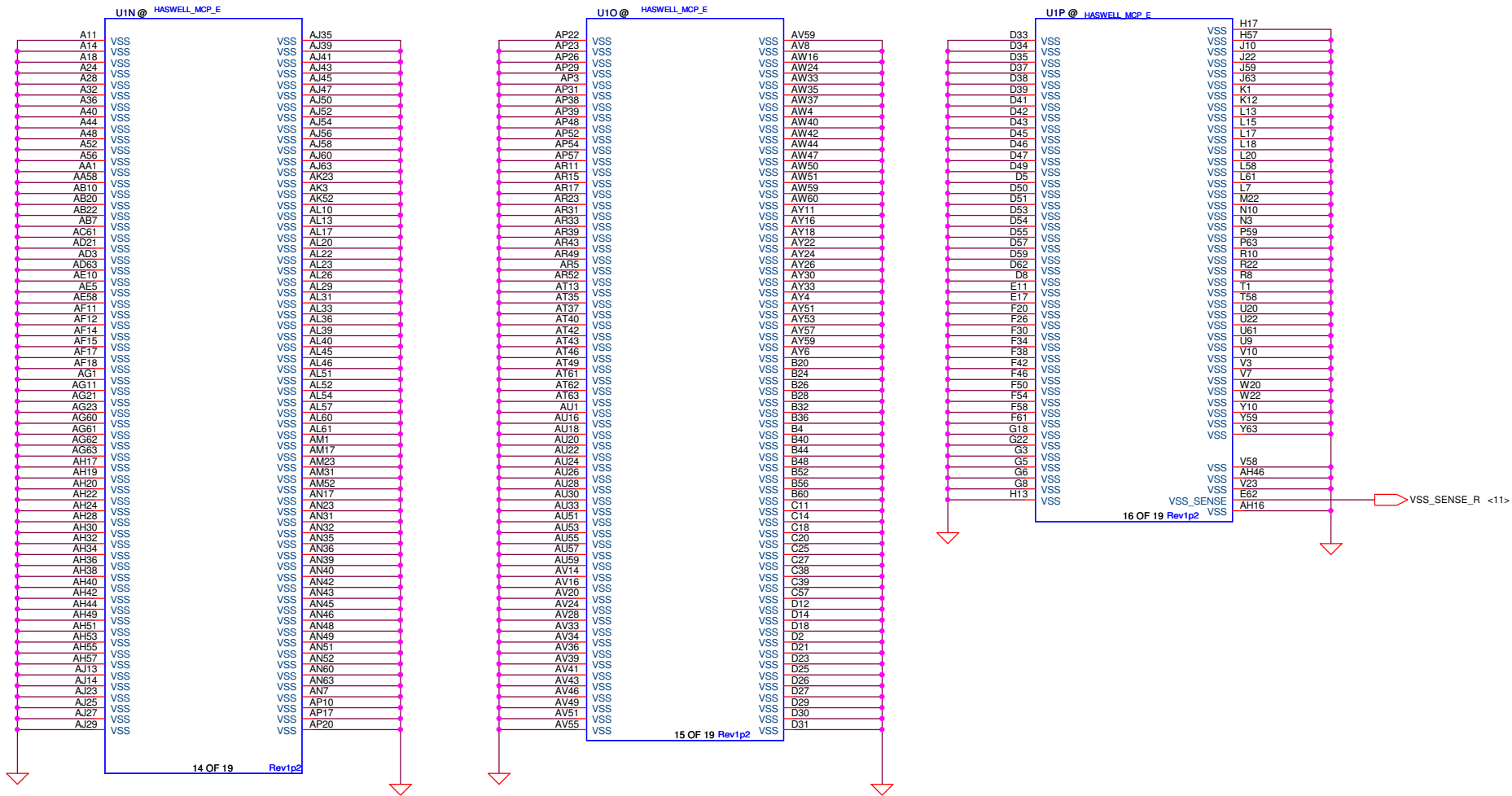




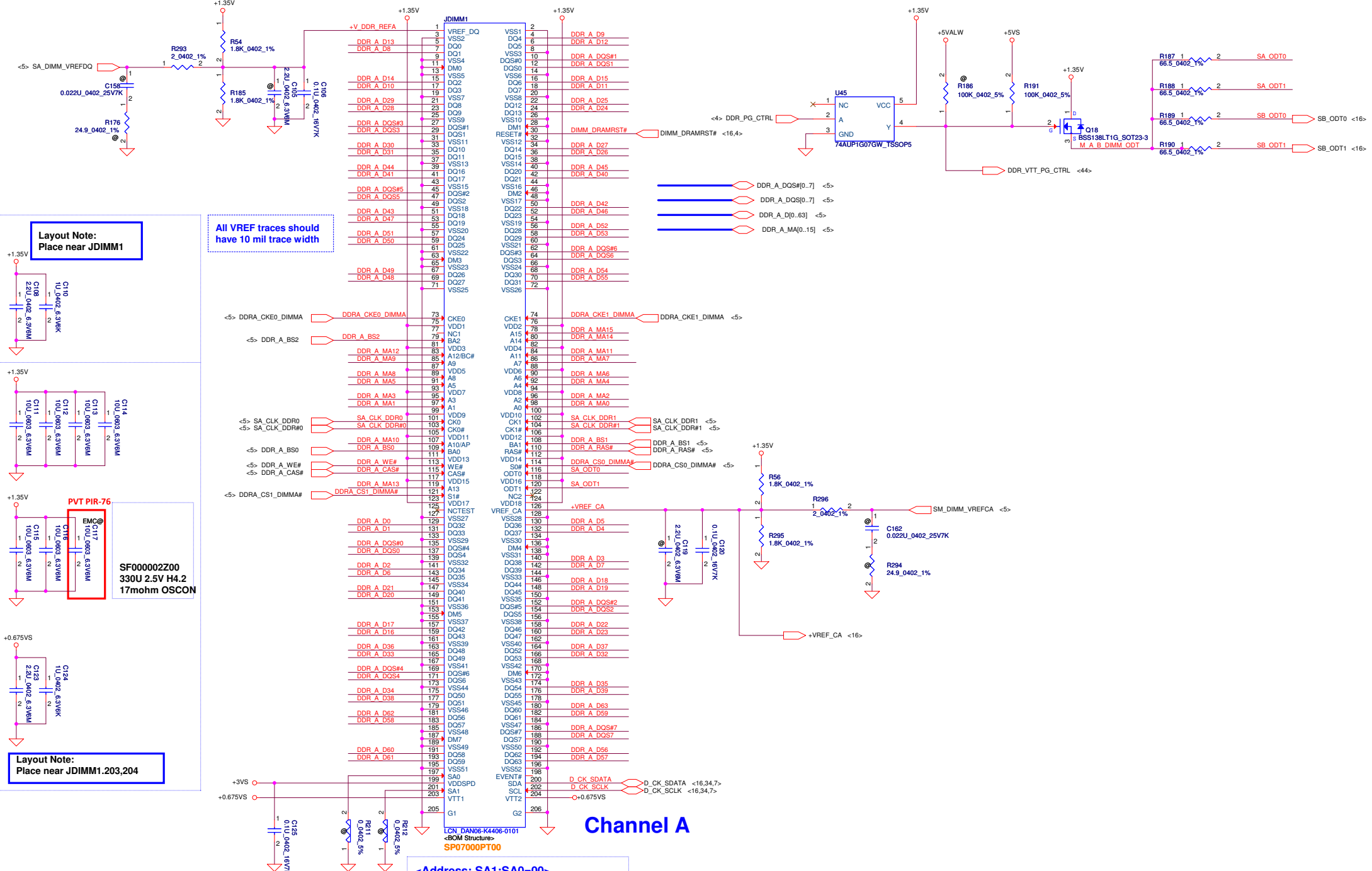


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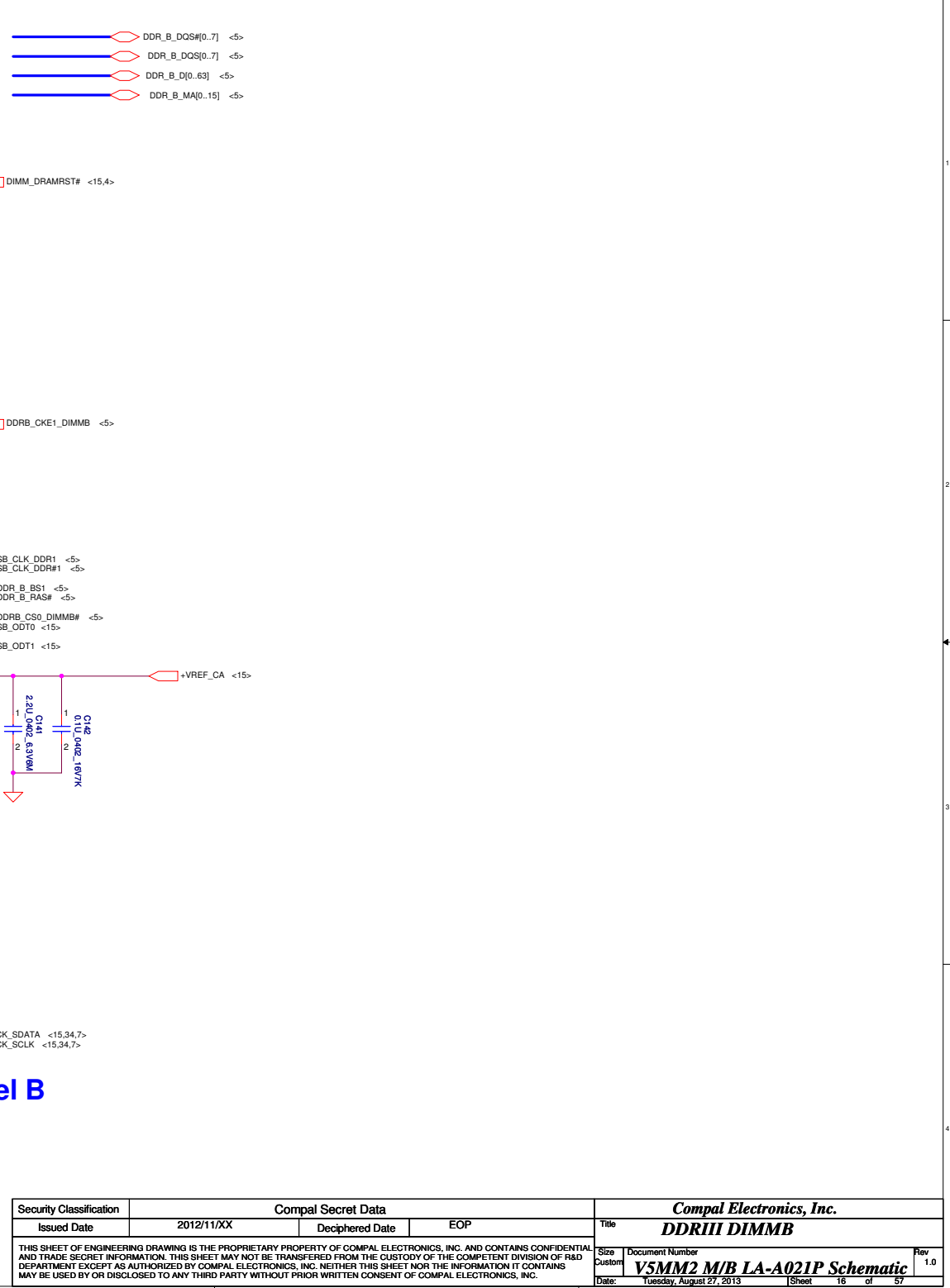
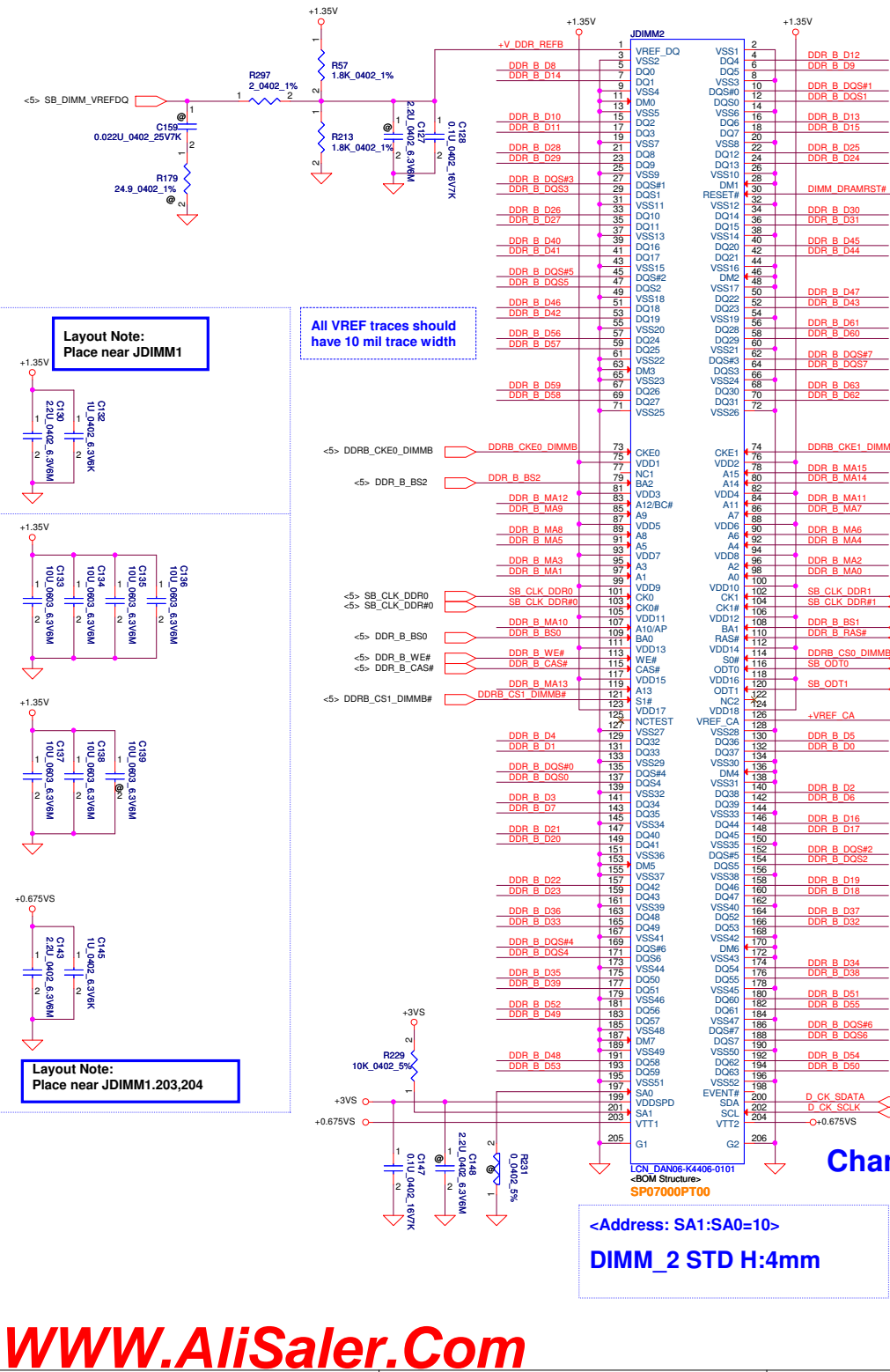
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| | | Date: Tuesday, August 27, 2013 | Sheet 13 of 57 | | |

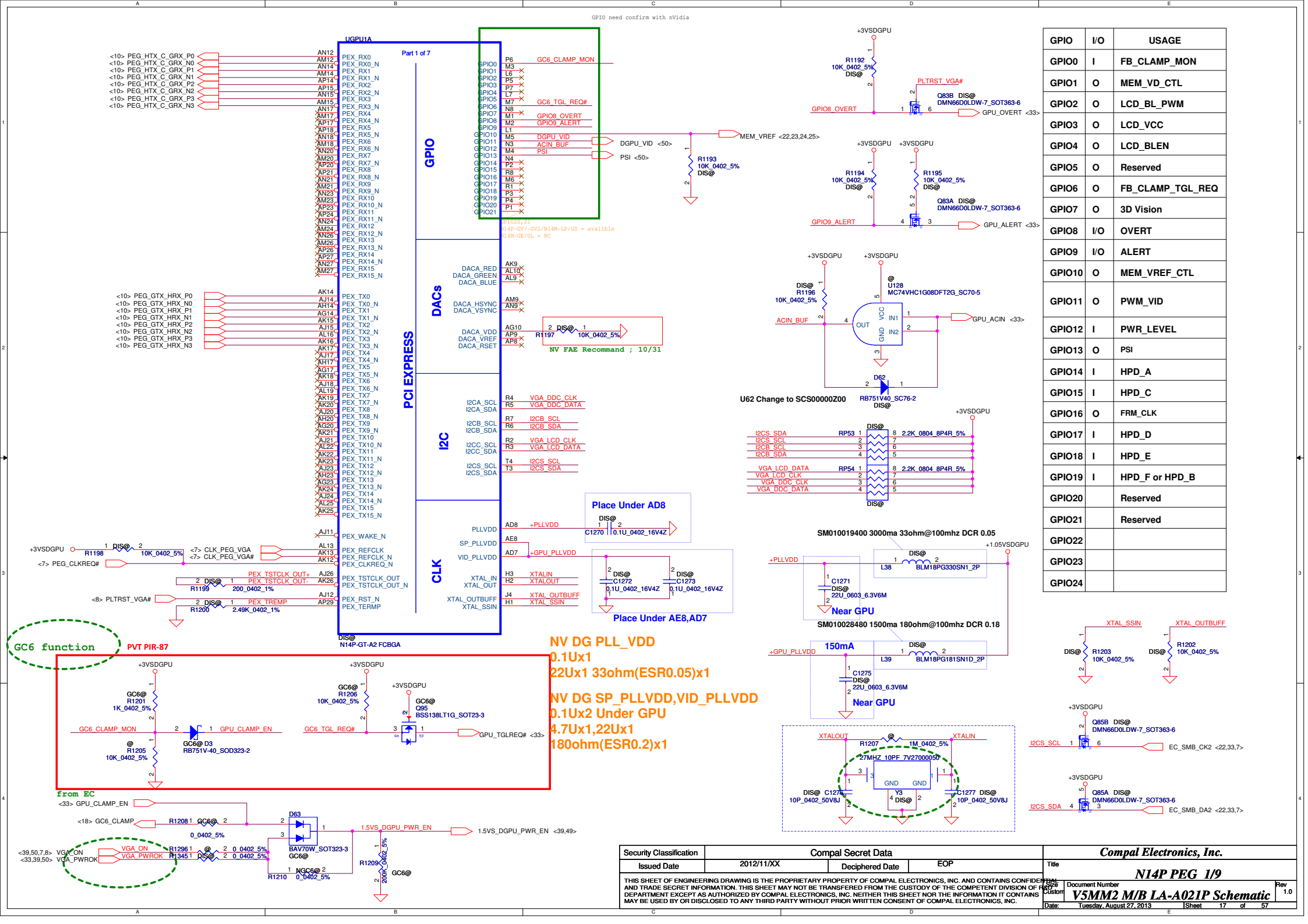


Channel A

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DIMM_1 STD H:4mm

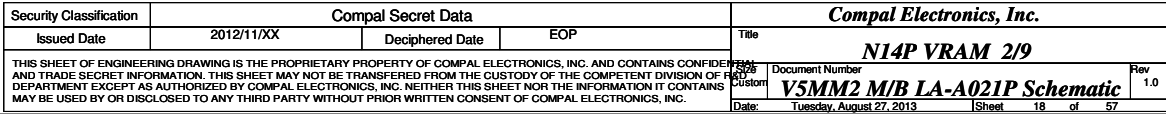
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| | | | | | | | | DDRIII DIMMA | | | | |
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| | | | | | | Date: | | Tuesday, August 27, 2013 | | | Sheet 15 of 57 | |
| | | | | | | | | | | | | |

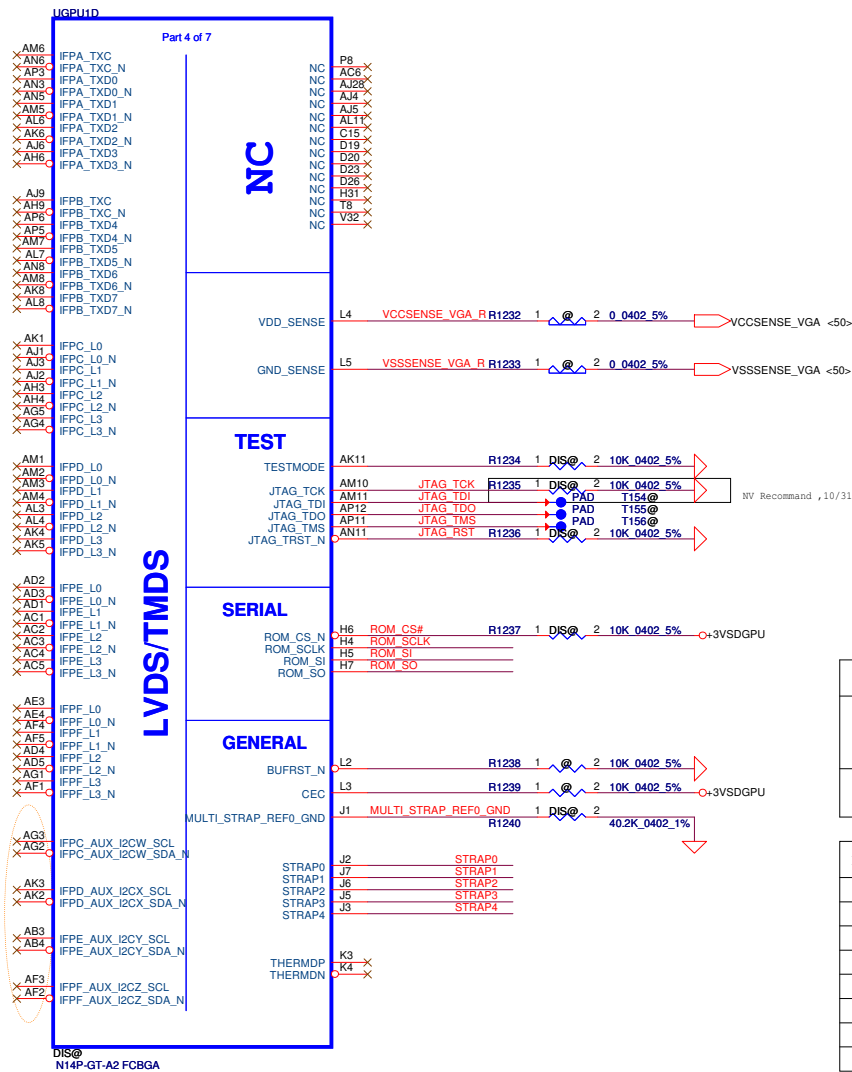




| GPIO | I/O | USAGE |
|-------|-----|------------------|
| GPI0 | I | FB_CLAMP_MON |
| GPI1 | O | MEM_VD_CTL |
| GPI2 | O | LCD_BL_PWM |
| GPI3 | O | LCD_VCC |
| GPI4 | O | LCD_BLEN |
| GPI5 | O | Reserved |
| GPI6 | O | FB_CLAMP_TGL_REQ |
| GPI7 | O | 3D Vision |
| GPI8 | I/O | OVERT |
| GPI9 | I/O | ALERT |
| GPI10 | O | MEM_VREF_CTL |
| GPI11 | O | PWM_VID |
| GPI12 | I | PWR_LEVEL |
| GPI13 | O | PSI |
| GPI14 | I | HPD_A |
| GPI15 | I | HPD_C |
| GPI16 | O | FRM_CLK |
| GPI17 | I | HPD_D |
| GPI18 | I | HPD_E |
| GPI19 | I | HPD_F or HPD_B |
| GPI20 | | Reserved |
| GPI21 | | Reserved |
| GPI22 | | |
| GPI23 | | |
| GPI24 | | |

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VRAM BOM Config

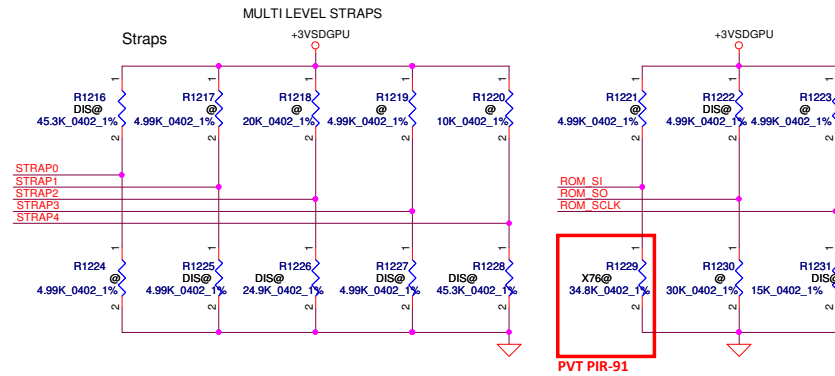
64Mx32x4

64Mx32x4

VRAM P/N

HYN 64*32 2000M SA00004GD30 (S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABOI)

HYN 64*32 2000M SA00004GD50(S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABOI)



For N14P-GT-A1 (ES2) A2 (QS) strap table Decive ID : 0x0FE4

| GDDR5 | Vendor | Strap | ROM_SI |
|-----------|----------|-------|--------|
| 128M x 16 | Hynix(M) | Ox4 | 24.9K |
| | Samsung | Ox5 | 30.1K |
| | Hynix(M) | Ox6 | 34.8K |

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---------|---------|-------------|---------------|----------|---------|----------|---------|----------|----------|---------|----------|
| N14P-GT | 900 MHZ | 128M*16 | Hynix | R PU 45K | R PD 5K | R PD 25K | R PD 5K | R PD 45K | R PD 25K | R PU 5K | R PD 15K |
| | | | Samsung | | | | | | R PD 30K | | |

| Resistor Values | Pull-up to +3V | Pull-down to Gnd |
|-----------------|----------------|------------------|
| 4.99K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 24.9K | 1100 | 0100 |
| 30.1K | 1101 | 0101 |
| 34.8K | 1110 | 0110 |
| 45.3K | 1111 | 0111 |

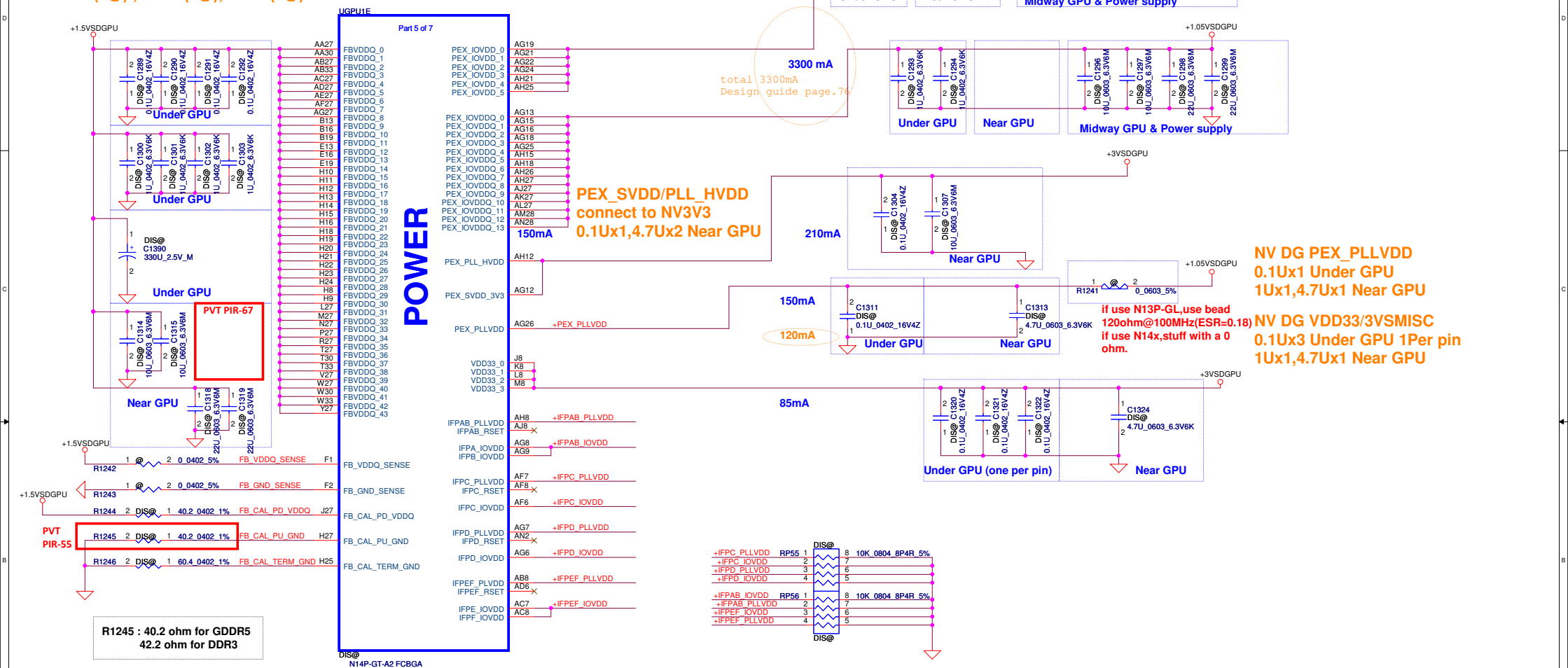
| | |
|----------|--|
| STRAP0 | USER[3:0] |
| STRAP1 | 3GIO_PADCFG_LUT_ADR[3:0] |
| STRAP2 | PCI_DEVID[3:0] |
| STRAP3 | SOR[3:0] |
| STRAP4 | PEG_SPEED_CHANGE_GEN3, PEX_MAX_SPEED,DP_PLLVDD33V |
| ROM_SCLK | PCI_DEV[4],SUB_VENDOR, PCI_DEV[5],PEX_PLL_EN_TERM |
| ROM_SI | RAM_CFG[3:0] |
| ROM_SO | FB_BAR_SIZE[1:0],SMB_ ALT_ADDR, VGA_DEVICE |

| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
|---|--------------------|-----------------|-----|--------------------------|------------------------------|----------------|
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | N14P LVDS 3/9 | |
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| | | | | Date: | Tuesday, August 27, 2013 | Sheet 19 of 57 |

4.7Ux6(3@) ,10Ux4(2@),22Ux4(2@) Near GPU

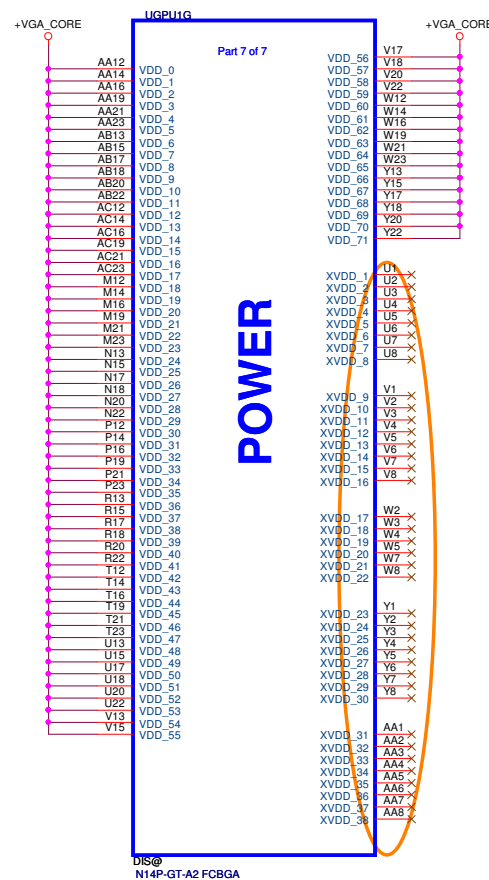
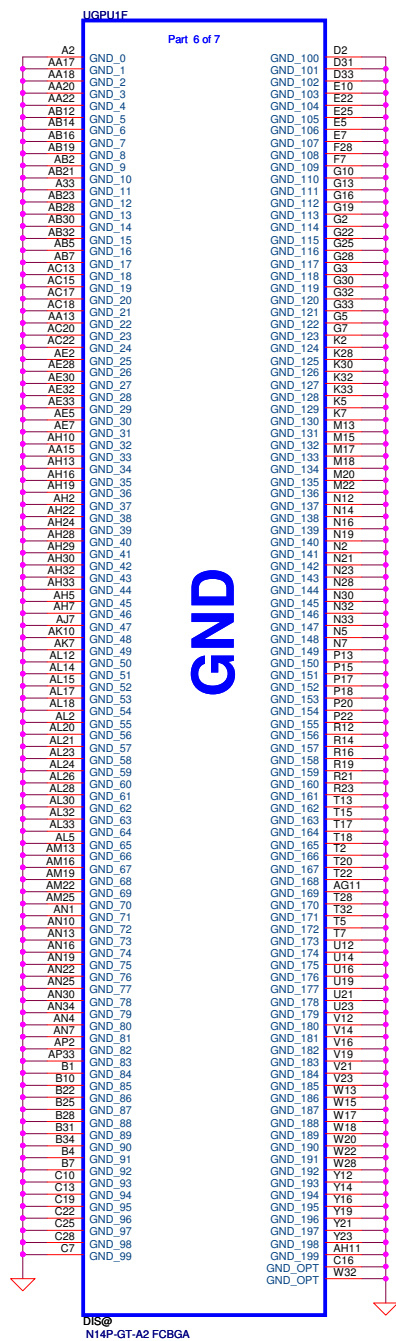
N13P-GS 10.44A
N13P-GT 10.51A

10Ux4,22Ux4 Midway GPU & Power supply



8) NV DG VDD33/3VSMISC
0.1Ux3 Under GPU 1Per pin
1Ux1,4.7Ux1 Near GPU

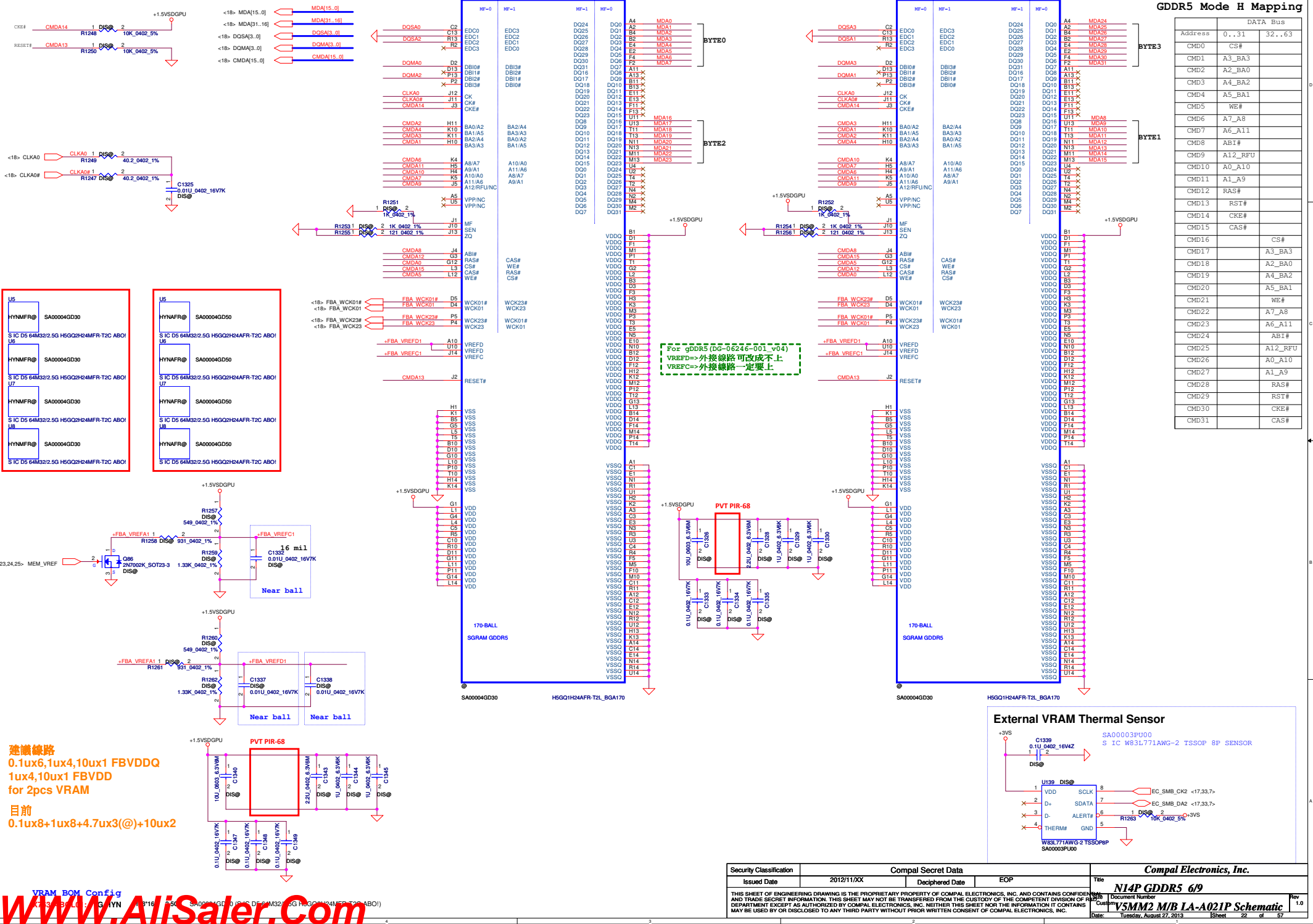
| | | | | | |
|--|------------|--------------------|-----|---|----------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | N14P POWER & GND 4/9 |
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| | | | | V5MM2 M/B LA-A021P Schematic Date: Tuesday, August 27, 2013 Sheet 20 of 57 | |



N14P-GT EDP peak 45A

| | | | | | |
|--|------------|--------------------|-----|--------------------------------|----------------|
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| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | Rev |
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| | | | | V5MM2 M/B LA-A021P Schematic | |
| | | | | Date: Tuesday, August 27, 2013 | Sheet 21 of 57 |

Memory Partition A Lower 32 Bit



[illegible]

目前
 $0.1\mu x8+1\mu x8+4.7\mu x3(@)+10\mu x2$

| | | | | | | |
|---|--------------------|-----------------|-----|--------------------------|------------------------------|----------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | N14P GDDR5 7/9 | |
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| | | | | | V5MM2 M/B LA-A021P Schematic | 1.0 |
| Date: | | | | Tuesday August 27 2013 | Sheet | 23 of 57 |

BOT / M504



| | DATA Bus | |
|---------|----------|---------|
| Address | 0...31 | 32...63 |
| CMD0 | CS# | |
| CMD1 | A3_BA3 | |
| CMD2 | A2_BA0 | |
| CMD3 | A4_BA2 | |
| CMD4 | A5_BA1 | |
| CMD5 | WE# | |
| CMD6 | A7_A8 | |
| CMD7 | A6_A11 | |
| CMD8 | AB1# | |
| CMD9 | A12_RFU | |
| CMD10 | A0_A10 | |
| CMD11 | A1_A9 | |
| CMD12 | RAS# | |
| CMD13 | RST# | |
| CMD14 | CKE# | |
| CMD15 | CAS# | |
| CMD16 | | CS# |
| CMD17 | | A3_BA3 |
| CMD18 | | A2_BA0 |
| CMD19 | | A4_BA2 |
| CMD20 | | A5_BA1 |
| CMD21 | | WE# |
| CMD22 | | A7_A8 |
| CMD23 | | A6_A11 |
| CMD24 | | AB1# |
| CMD25 | | A12_RFU |
| CMD26 | | A0_A10 |
| CMD27 | | A1_A9 |
| CMD28 | | RAS# |
| CMD29 | | RST# |
| CMD30 | | CKE# |
| CMD31 | | CAS# |

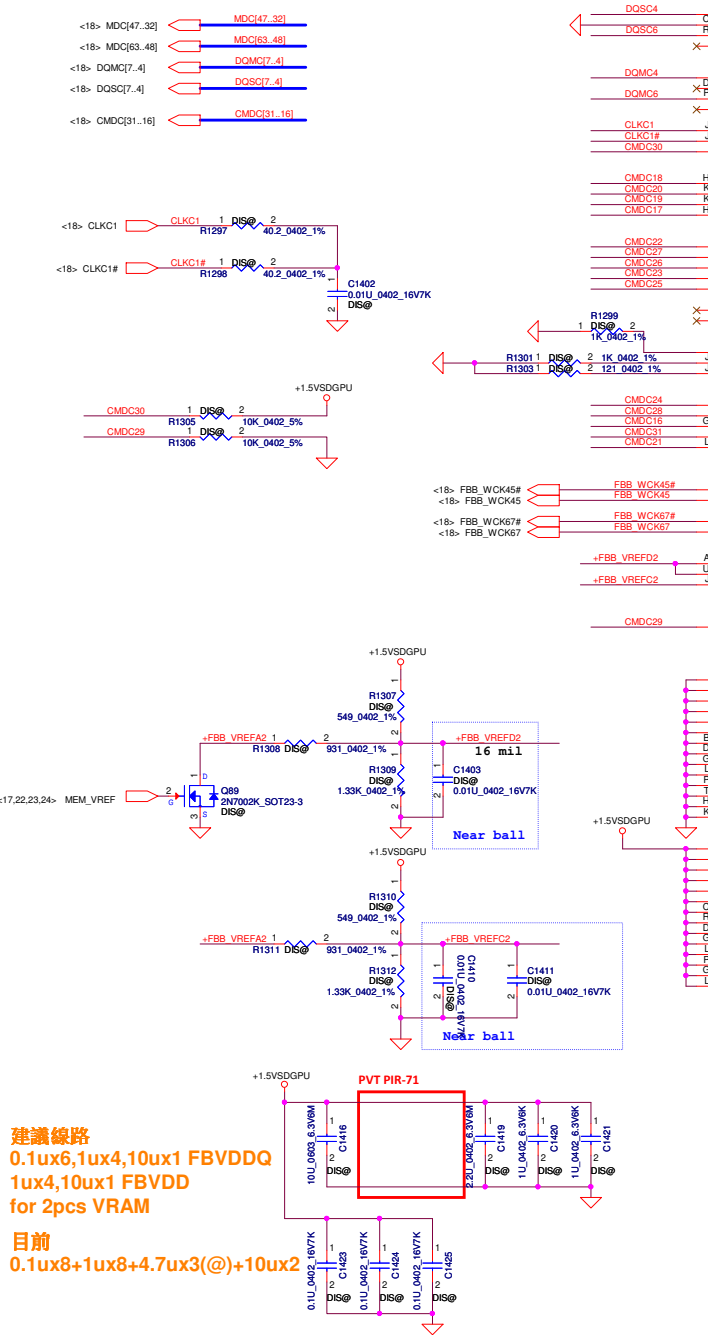
VRAM BOM Config

VRAM BOM Config

| | | | | | | |
|--|--------------------|-----------------|-----|--------------------------|------------------------------|-----------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | N14P GDDR5 8/9 | |
| <p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p> | | | | Docu. Number | V5M2M M/B LA-A021P Schematic | |
| | | | | Date | Thursday, August 27, 2014 | Sheet 5/7 |

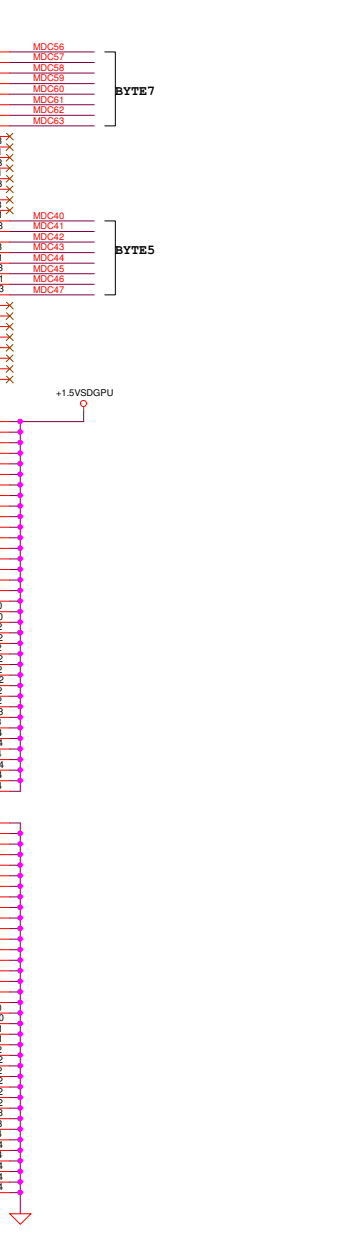
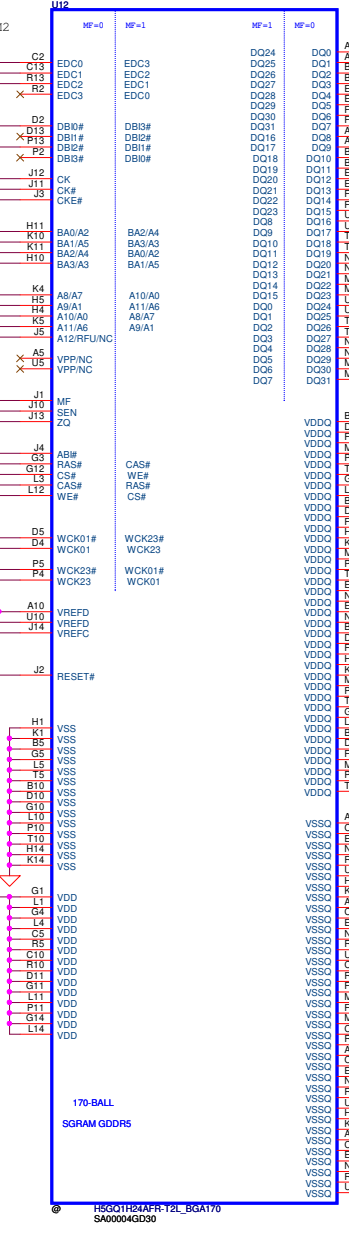
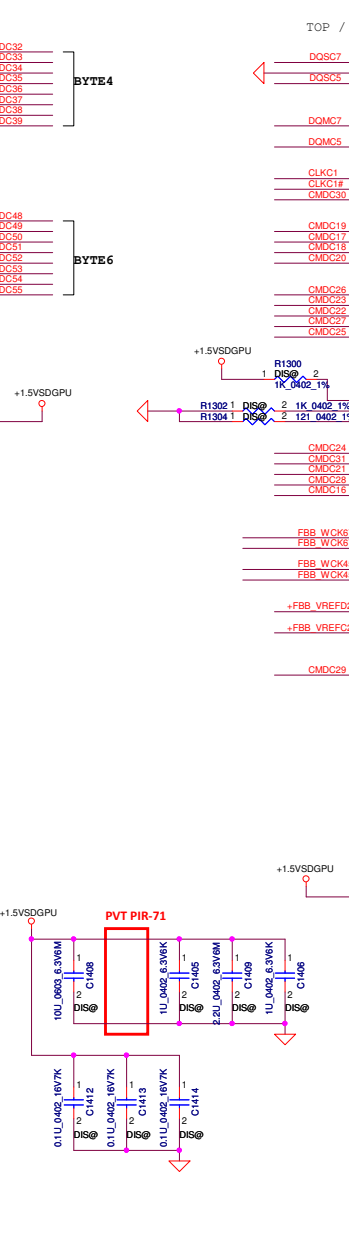
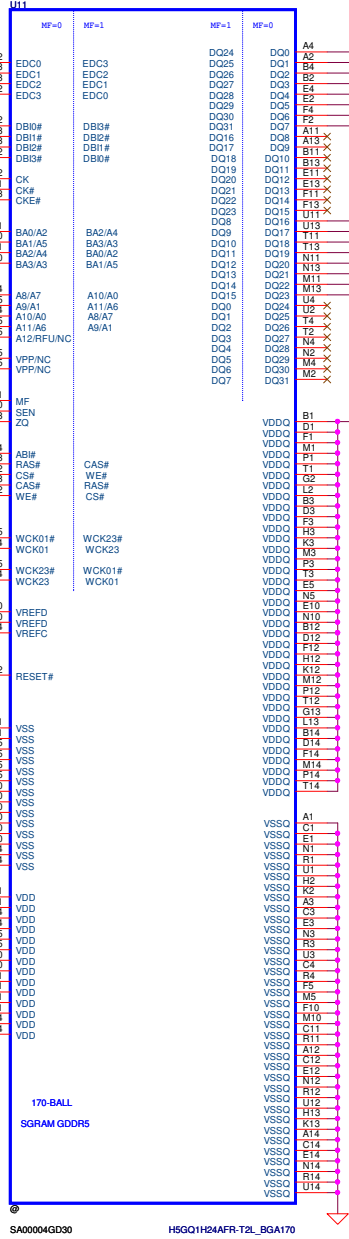
Memory Partition C Upper 32 bit

BOT / M503

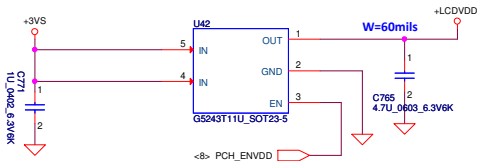


建議線路
0.1ux6,1ux4,10ux1 FBVDDQ
1ux4,10ux1 FBVDD
for 2pcs VRAM

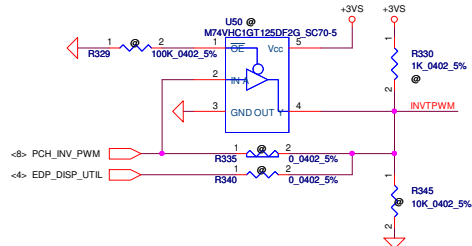
目前
0.1ux8+1ux8+4.7ux3(@)+10ux2



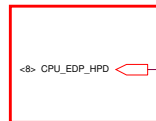
eDP Panel Power Circuit



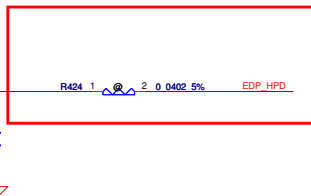
Need to check eDP panel sequence in the future.



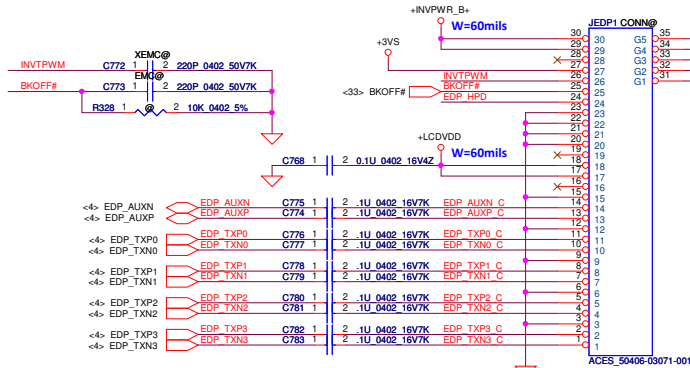
PVT PIR-54



PVT PIR-71



eDP PANEL Connector

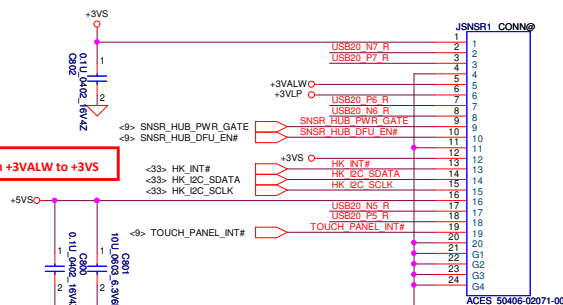


For Camera

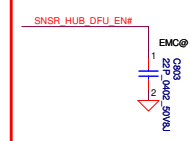
For Sensor Hub

For Touch Panel

PVT PIR-64 : JSNSR pin12 change from +3VALW to +3VS

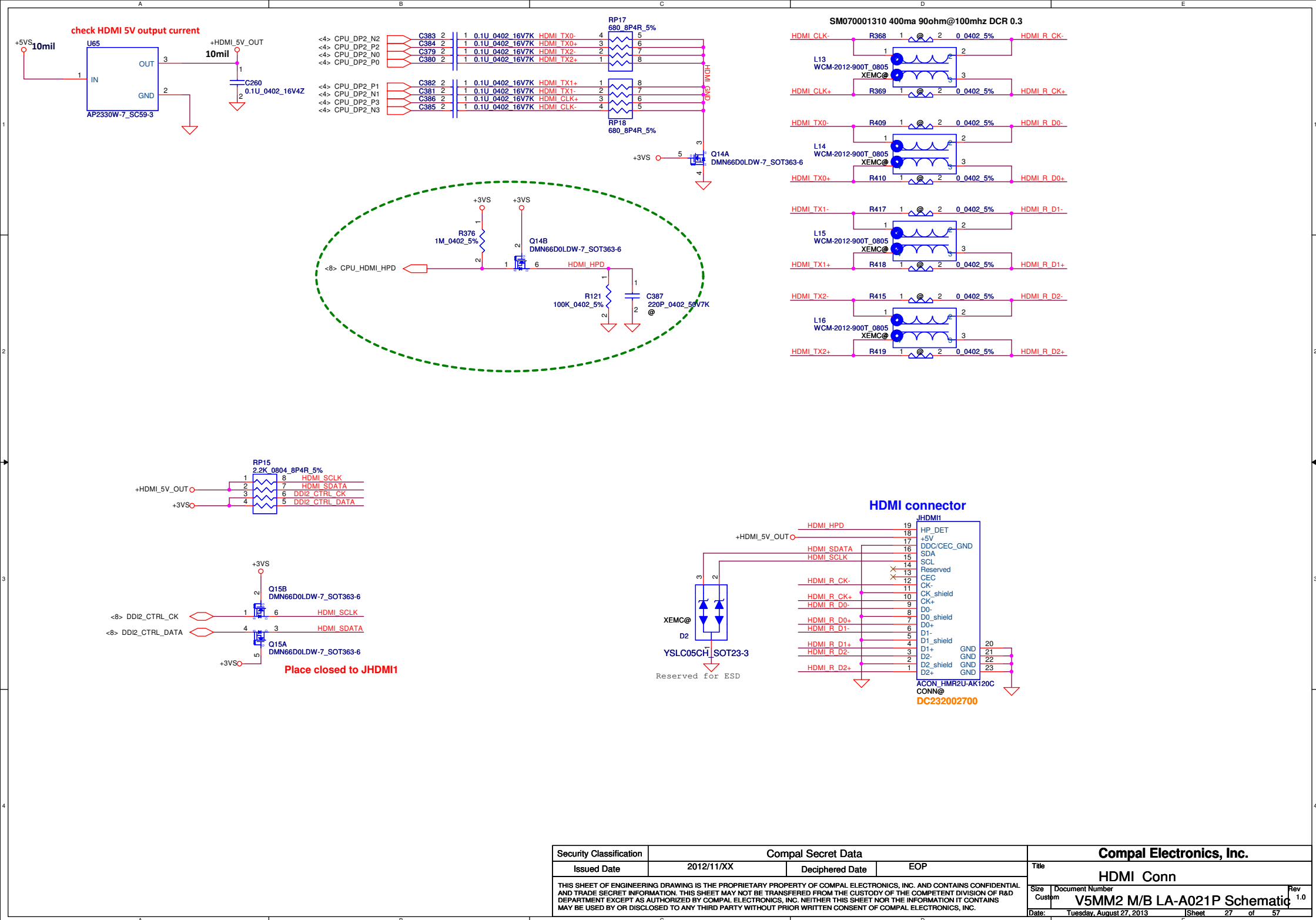


For ESD request



PVT PIR-61

| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
|---|------------|--------------------|-----|--------------------------|------------------------------|
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | eDP Connector |
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| | | | | Customer | Rev 1.0 |
| | | | | Date | Tuesday, August 27, 2013 |
| | | | | Sheet | 26 of 57 |

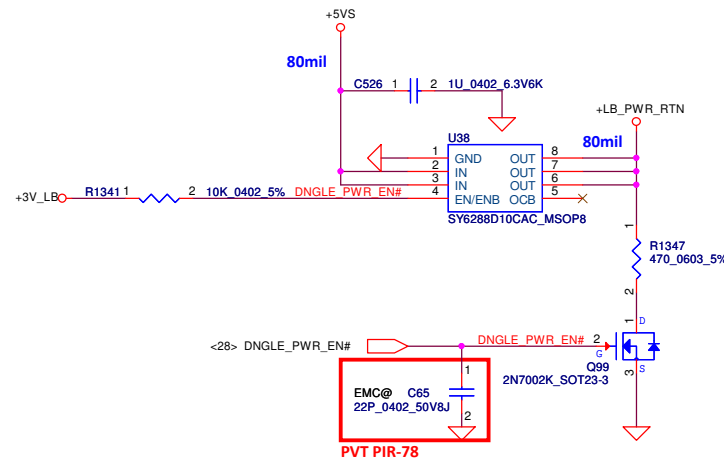


| | | | | | | |
|---|--------------------|-----------------|-----|--------------------------|------------------------------|----------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | HDMI Conn | |
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| | | | | Custom | V5MM2 M/B LA-A021P Schematic | 1.0 |
| | | | | Date: | Tuesday, August 27, 2013 | Sheet 27 of 57 |



PVT PIR-63

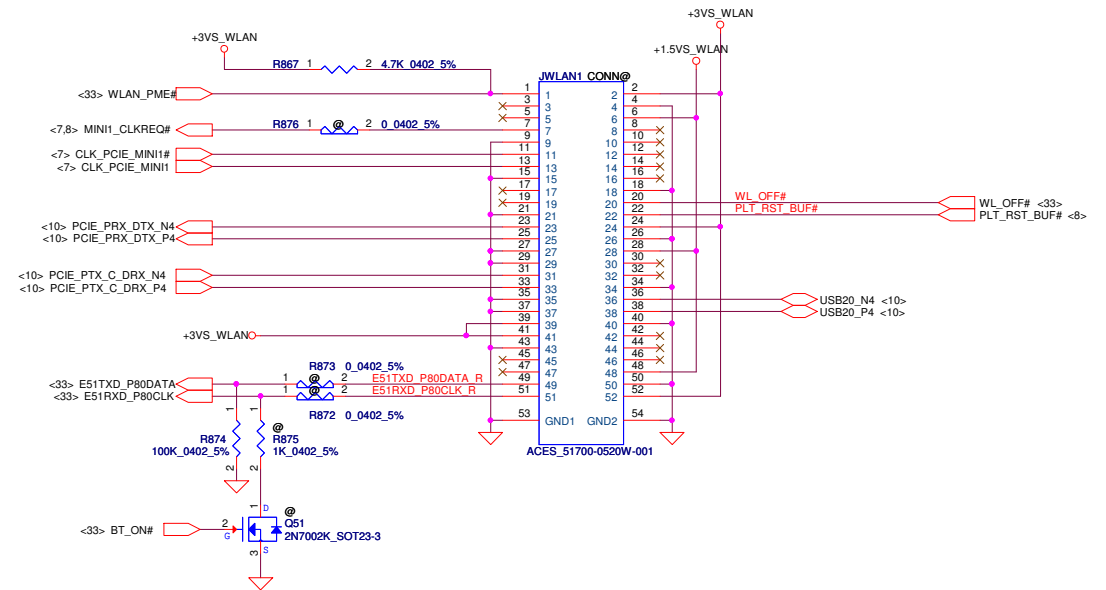
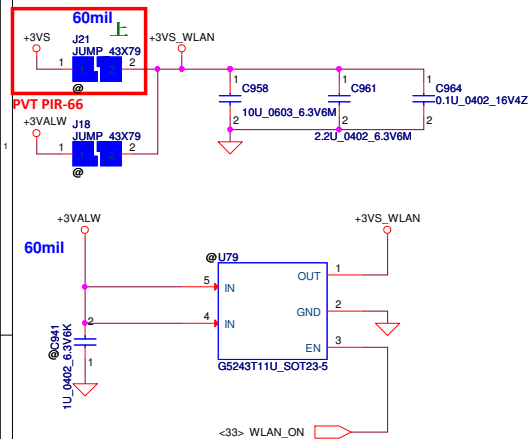
mDP Power Control Circuit for 5V Power Supply



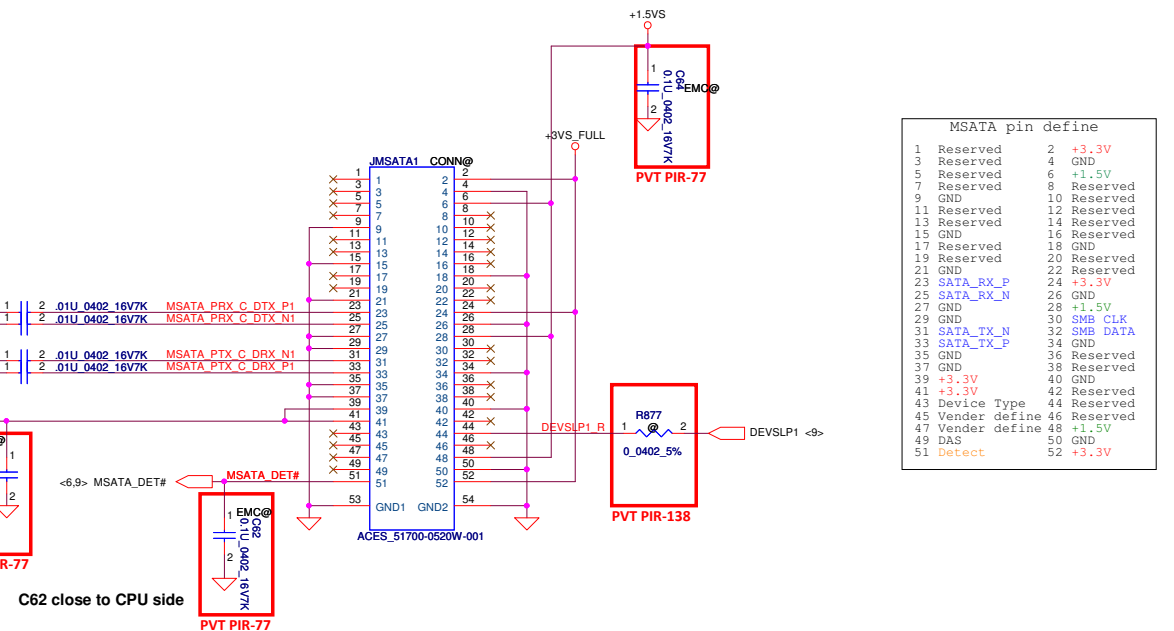
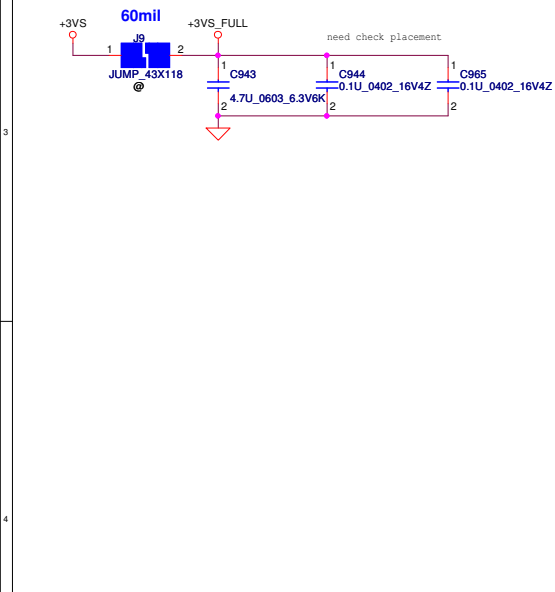
| Preliminary Power Output for mDP | | |
|----------------------------------|------------|------------|
| DNGLE_PWR_EN# | LB_PWR_RTN | LB_PWR_CNN |
| 1 | GND | 3.3V |
| 0 | 5V | 3.3V |

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| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | |
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| | | | | Date: Tuesday, August 27, 2013 | V5MM2 M/B LA-A021P Schematic |
| | | | | Sheet 29 of 57 | Rev 1.0 |

Wireless LAN



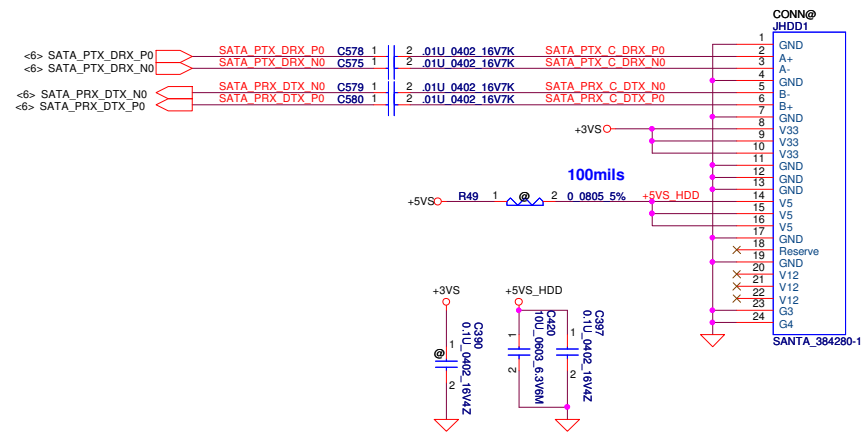
mSATA



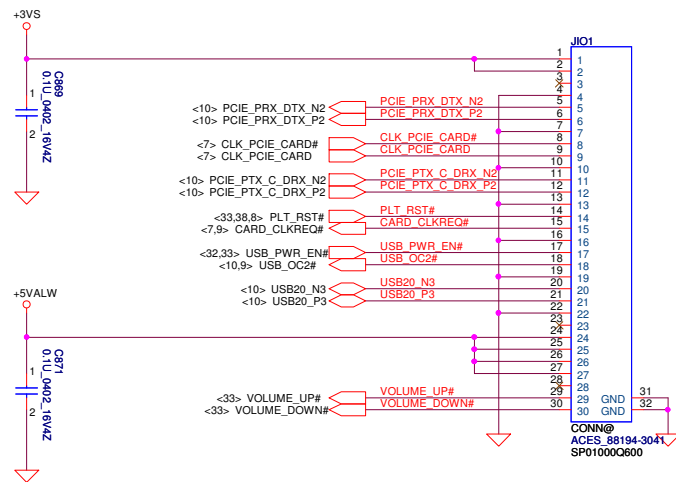
| | | | |
|----|---------------|----|----------|
| 1 | Reserved | 2 | +3.3V |
| 3 | Reserved | 4 | GND |
| 7 | Reserved | 8 | +1.5V |
| 9 | Reserved | 10 | Reserved |
| 11 | Reserved | 12 | Reserved |
| 13 | Reserved | 14 | Reserved |
| 15 | GND | 16 | Reserved |
| 17 | Reserved | 18 | GND |
| 19 | Reserved | 20 | Reserved |
| 21 | GND | 22 | Reserved |
| 23 | SATA_RX_P | 24 | +3.3V |
| 25 | SATA_RX_N | 26 | GND |
| 27 | GND | 28 | +1.5V |
| 29 | GND | 30 | SMB_CLK |
| 31 | SATA_TX_N | 32 | SMB_DATA |
| 33 | SATA_TX_P | 34 | GND |
| 35 | GND | 36 | Reserved |
| 37 | GND | 38 | Reserved |
| 39 | +3.3V | 40 | GND |
| 41 | +3.3V | 42 | Reserved |
| 43 | Device Type | 44 | Reserved |
| 45 | Vendor define | 46 | Reserved |
| 47 | Vendor define | 48 | +1.5V |
| 49 | DAS | 50 | GND |
| 51 | Detect | 52 | +3.3V |

| | | | |
|-------------------------|--------------------|-----------------|------------------------------|
| Security Classification | Compal Secret Data | Title | Compal Electronics, Inc. |
| Issued Date | 2012/11/XX | Document Number | MINI CARD/mSATA Connector |
| Deciphered Date | | Customer | V5MM2 M/B LA-A021P Schematic |
| Rev | 1.0 | Date | Tuesday, August 27, 2013 |
| | | Sheet | 30 of 57 |

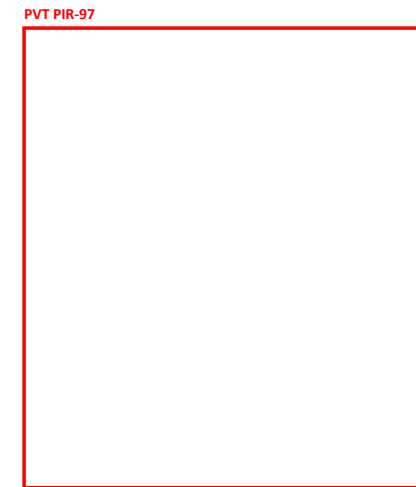
SATA HDD Connector(DIP Type)



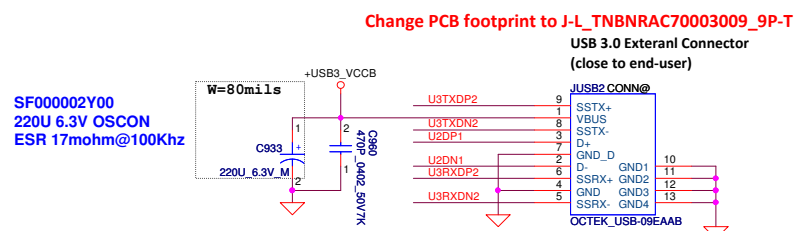
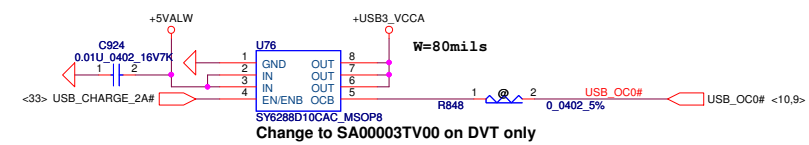
IO/B Connector

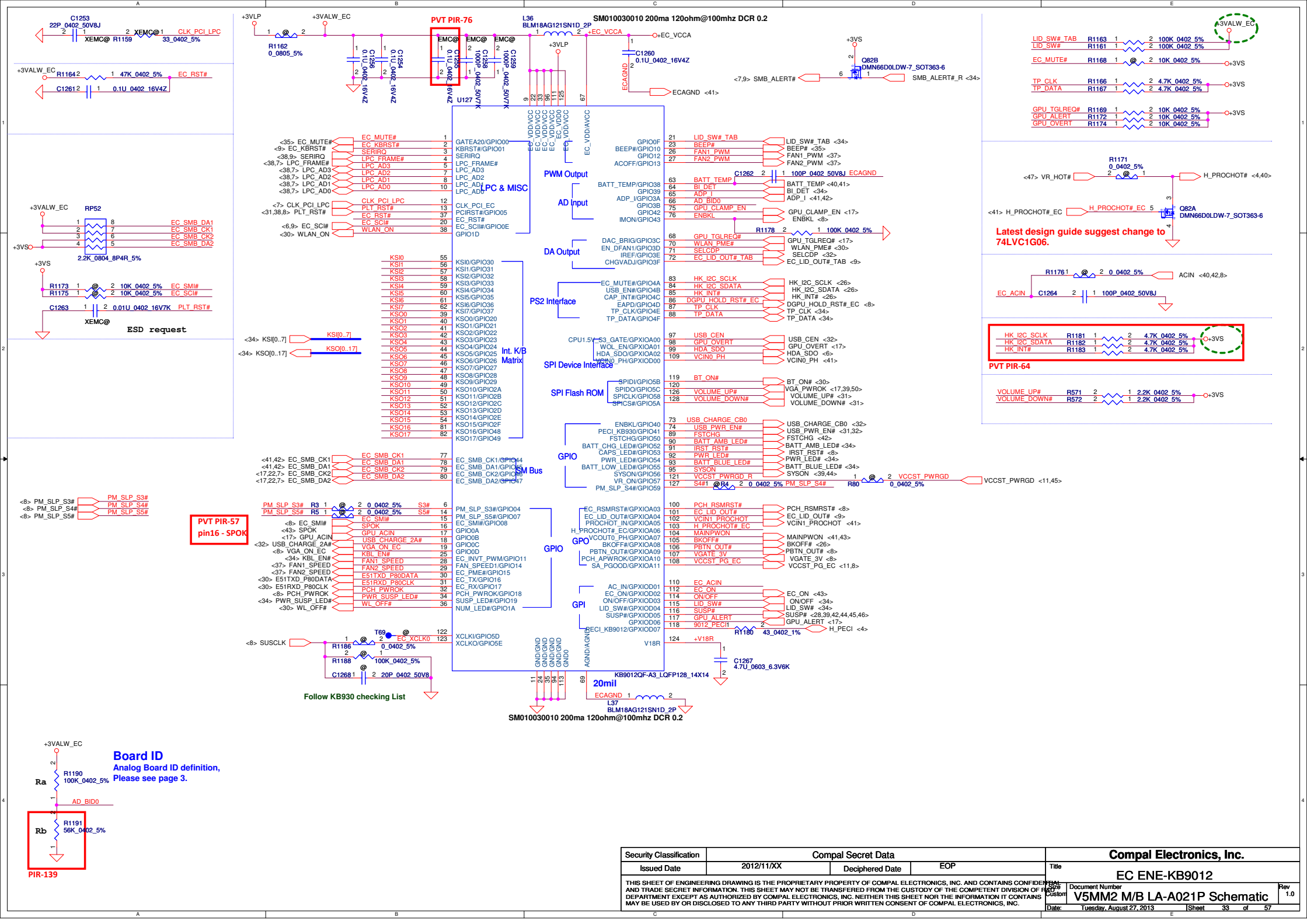


**LAN/B Connector
(Place near JPWR1)**



| | | | | | |
|---|------------|--------------------|-----|---|---------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | HDD/ODD/Debug Board |
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| | | | | V5MM2 M/B LA-A021P Schematic Date: Tuesday, August 27, 2013 Sheet 31 of 57 | |



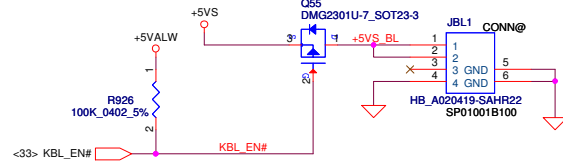
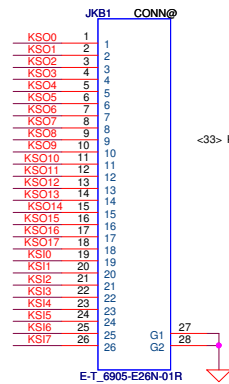
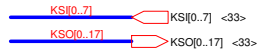


KB Conn.

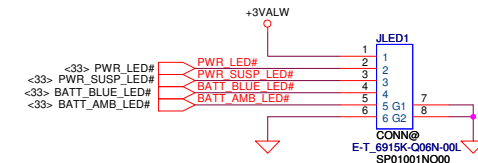
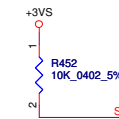
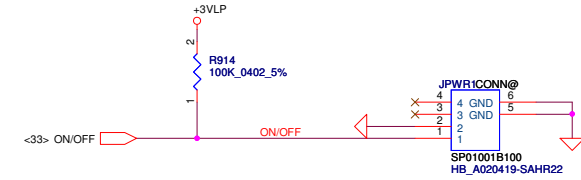
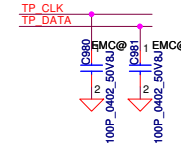
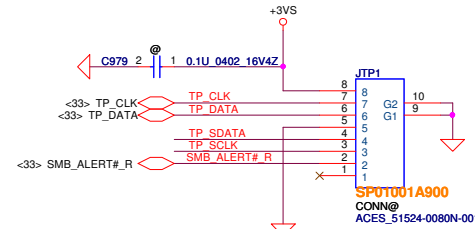
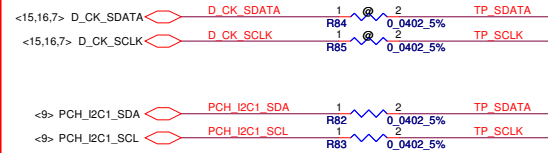
KB backlight Conn.

TP Conn.

ON/OFF BTN



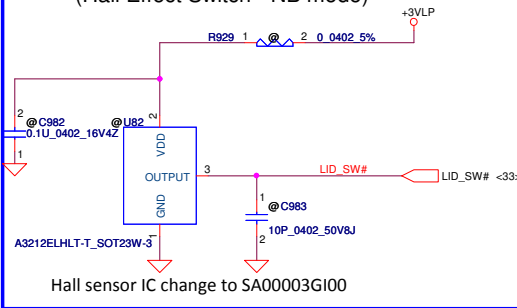
PVT PIR-89



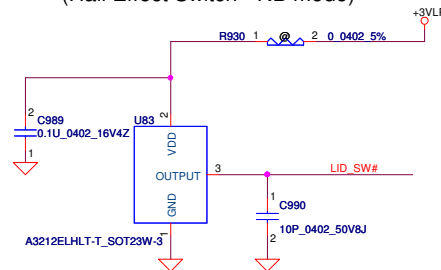
| Lid Switch solution | |
|---------------------|-----------------|
| Solution-1 | EVT, DVT, PVT-1 |
| Solution-2 | PVT-2 |

Lid switch power source need same as EC power

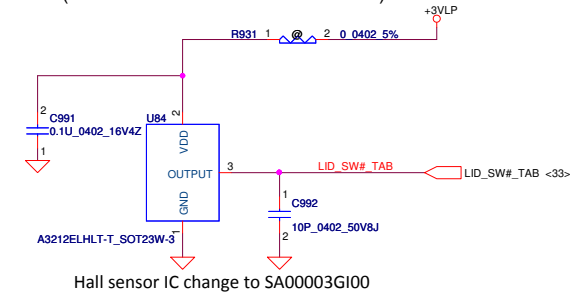
Lid Switch Solution-1 (Hall Effect Switch - NB mode)



Lid Switch Solution-2 (Hall Effect Switch - NB mode)

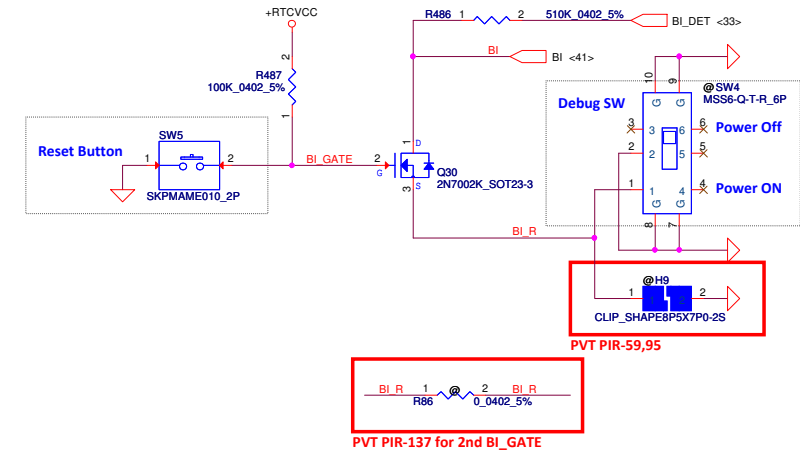


(Hall Effect Switch - Tablet mode)



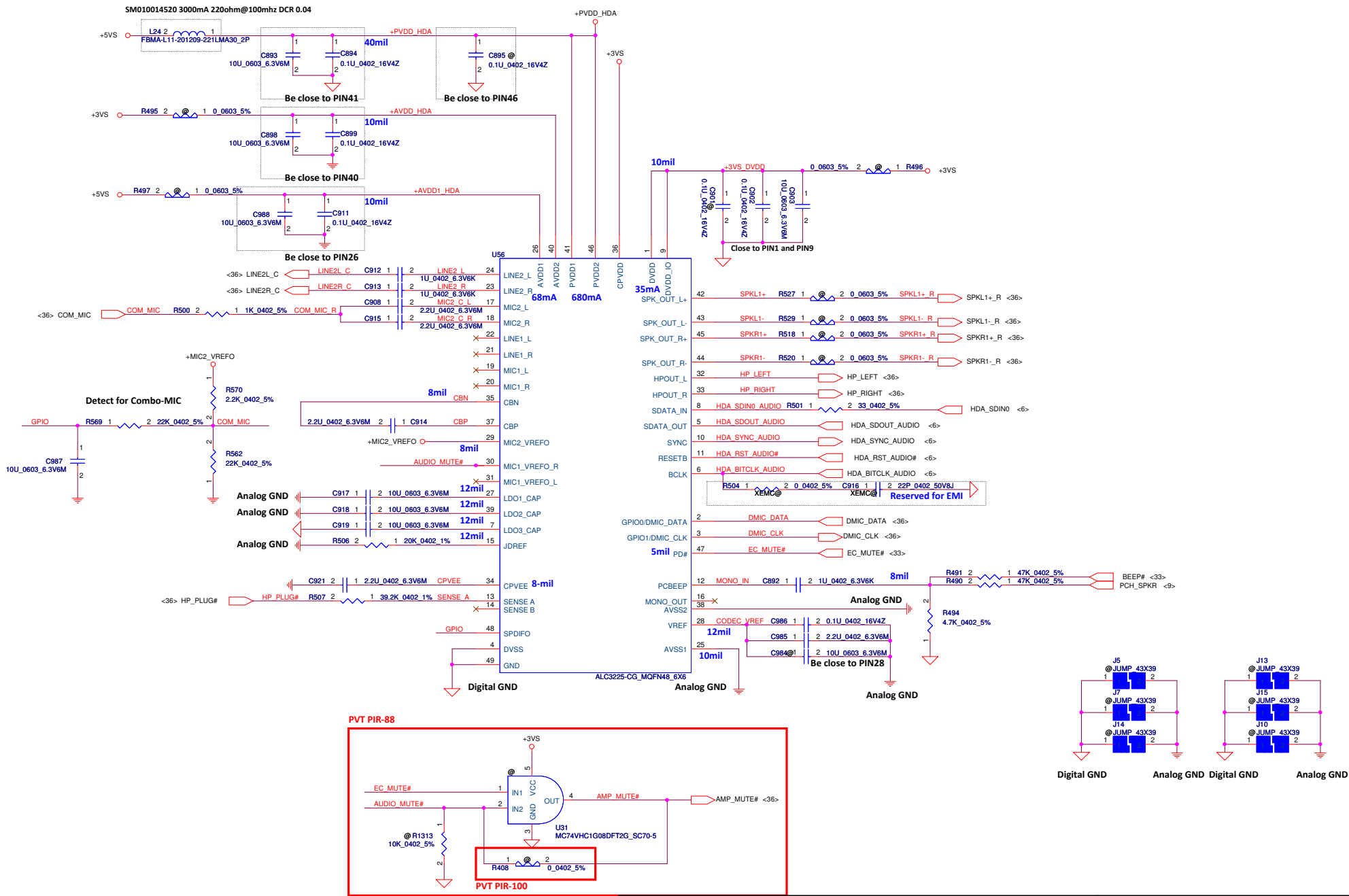
Reset Button and Debug Switch for Polymer Battery

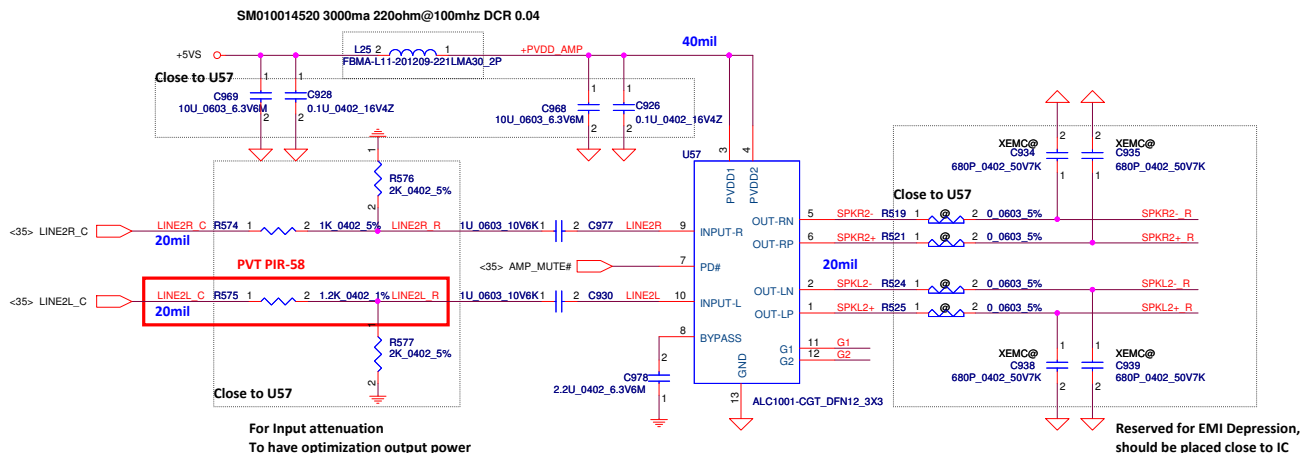
Debug switch will be removed after MP.



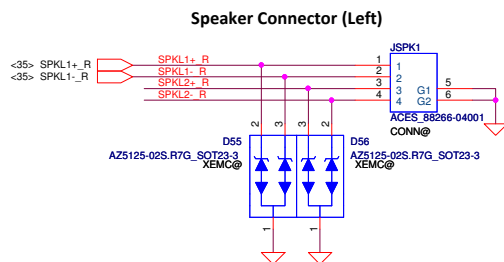
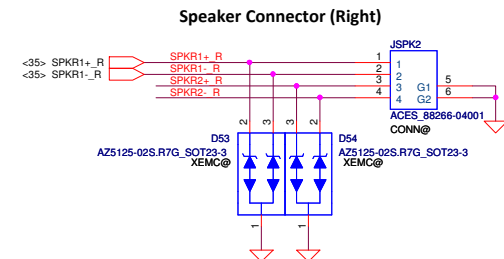
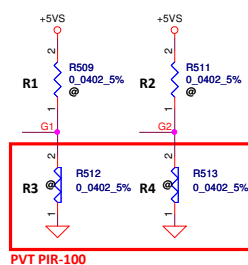
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
|--|------------|--------------------|-----|--------------------------|------------------------------|
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | User Interface |
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| | | | | Date | Tuesday, August 27, 2013 |
| | | | | Sheet | 34 of 57 |

HD Audio Codec- ALC3225 with Embedded Speaker Amplifier

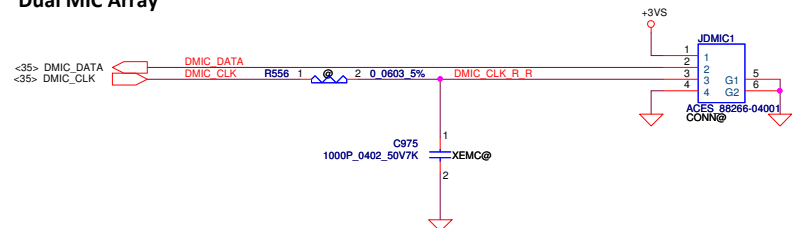




| R1 | R2 | R3 | R4 | Gain (Differential) |
|----|----|----|----|---------------------|
| NC | NC | 0 | 0 | 11dB |
| 0 | NC | NC | 0 | 14dB |
| NC | 0 | 0 | NC | 19dB |
| 0 | 0 | NC | NC | 25dB |

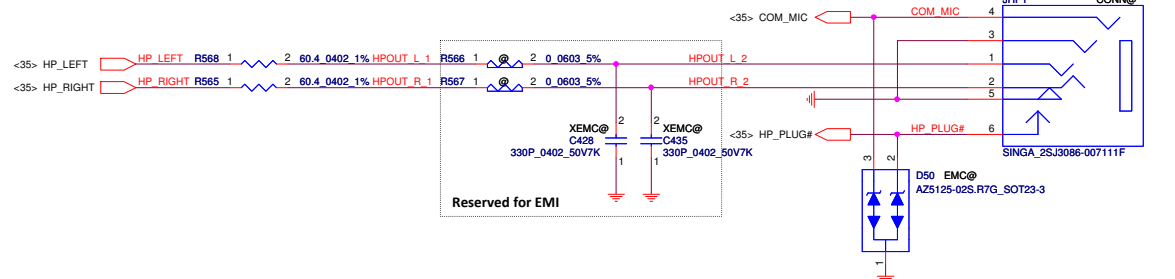


Dual MIC Array

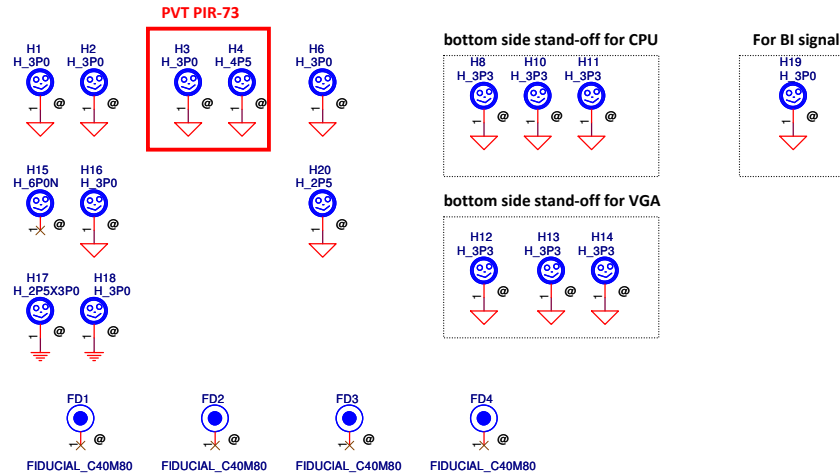
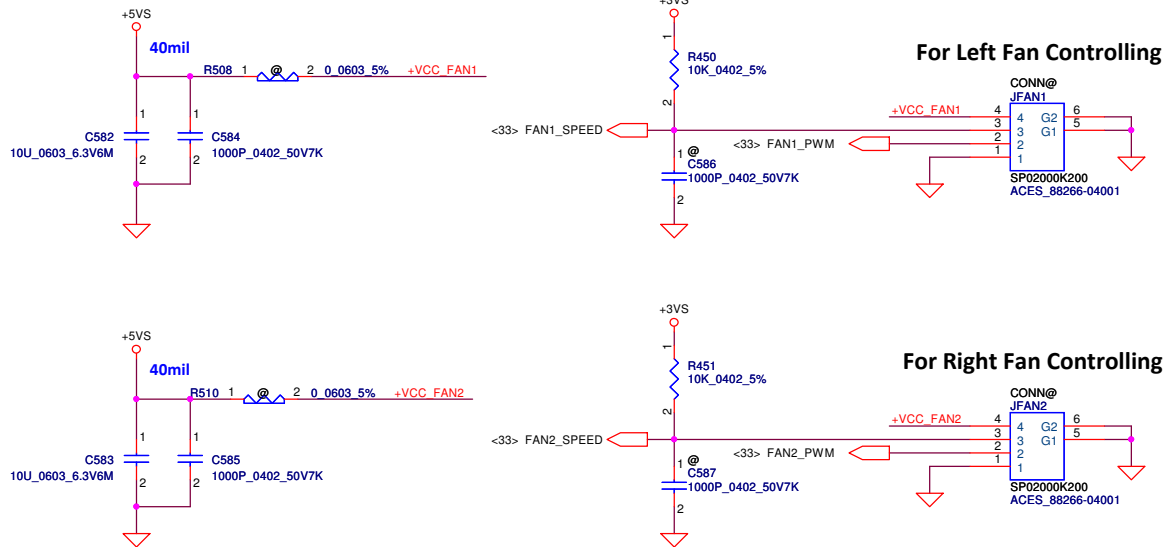


Headphone Out/Mic Combo

JACK TYPE is the same as MA51

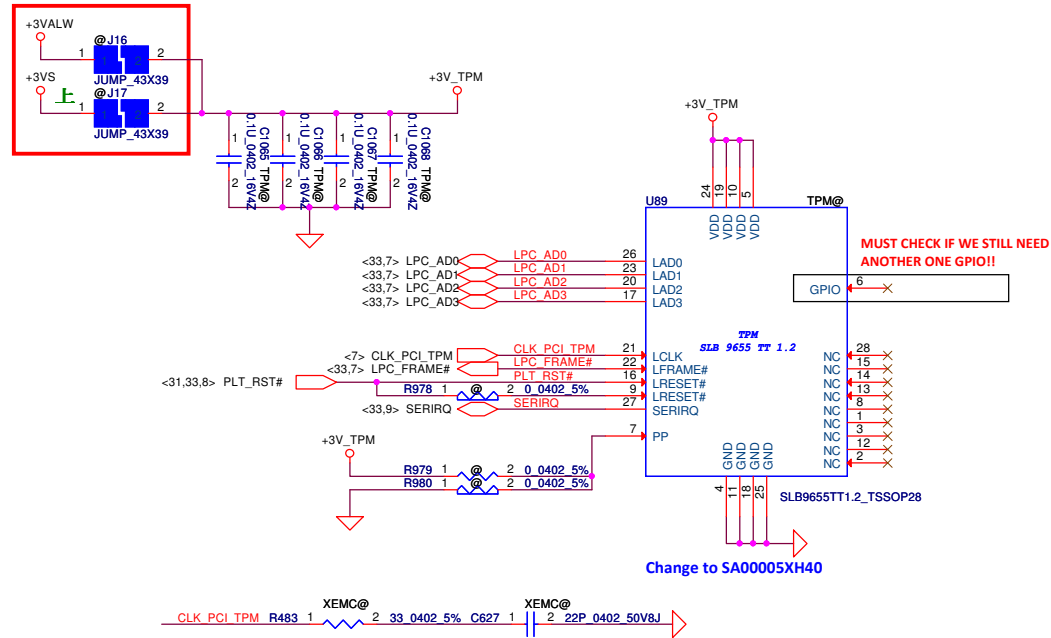


| | | | | | | |
|---|--------------------|-----------------|-----|--------------------------|------------------------------|----------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | Amplifier & I/O Ports | |
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| | | | | Customer | V5MM2 M/B LA-A021P Schematic | 1.0 |
| | | | | Date: | Tuesday, August 27, 2013 | Sheet 36 of 57 |



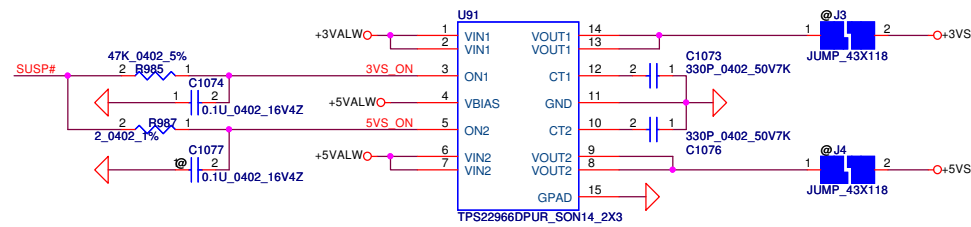
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|---|--------------------|-----------------|-----|--------------------------|------------------------------|----------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
| Issued Date | 2012/11/XX | Deciphered Date | EOP | FAN & Screw Hole | | |
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| | | | | Custom | V5MM2 M/B LA-A021P Schematic | 1.0 |
| | | | | Date: | Tuesday, August 27, 2013 | Sheet 37 of 57 |

PVT PIR-93

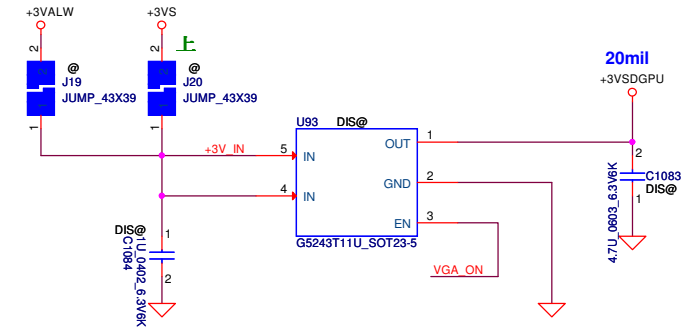


| | | | | | |
|---|--------------------------|--------------------|------------------------------|---------------------------|-----|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | |
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| Size | Document Number | Custom | V5MM2 M/B LA-A021P Schematic | Rev | 1.0 |
| Date: | Tuesday, August 27, 2013 | Sheet | 38 | of | 57 |

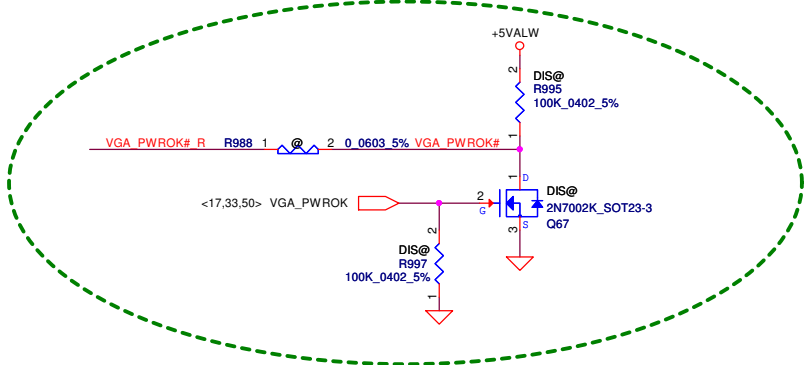
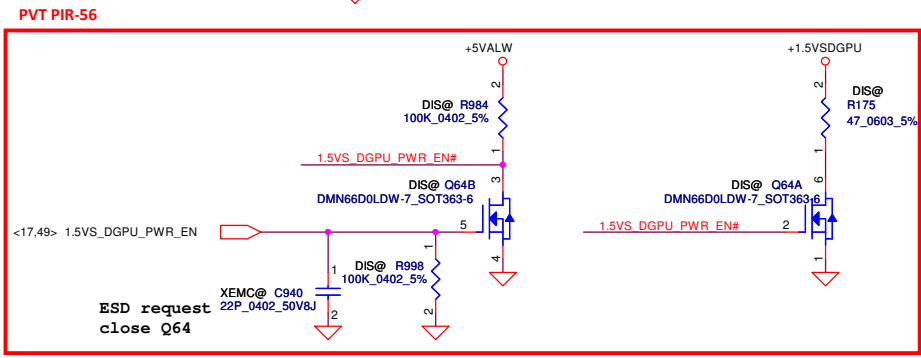
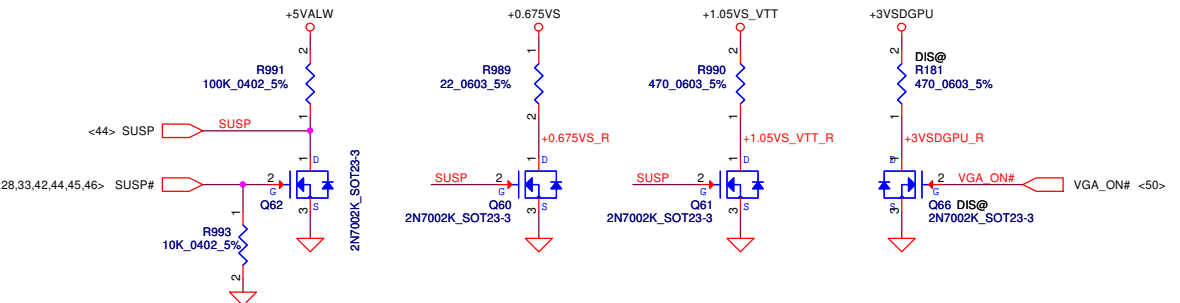
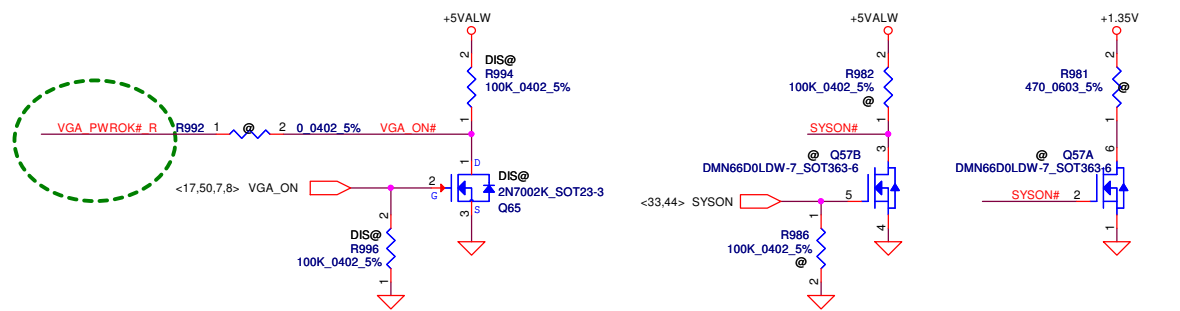
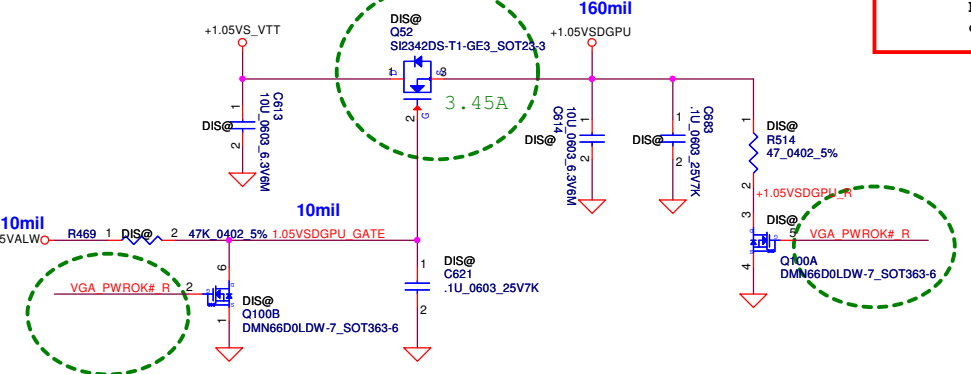
Use Dual Load Switch for +3VS/+5VS Power Supply



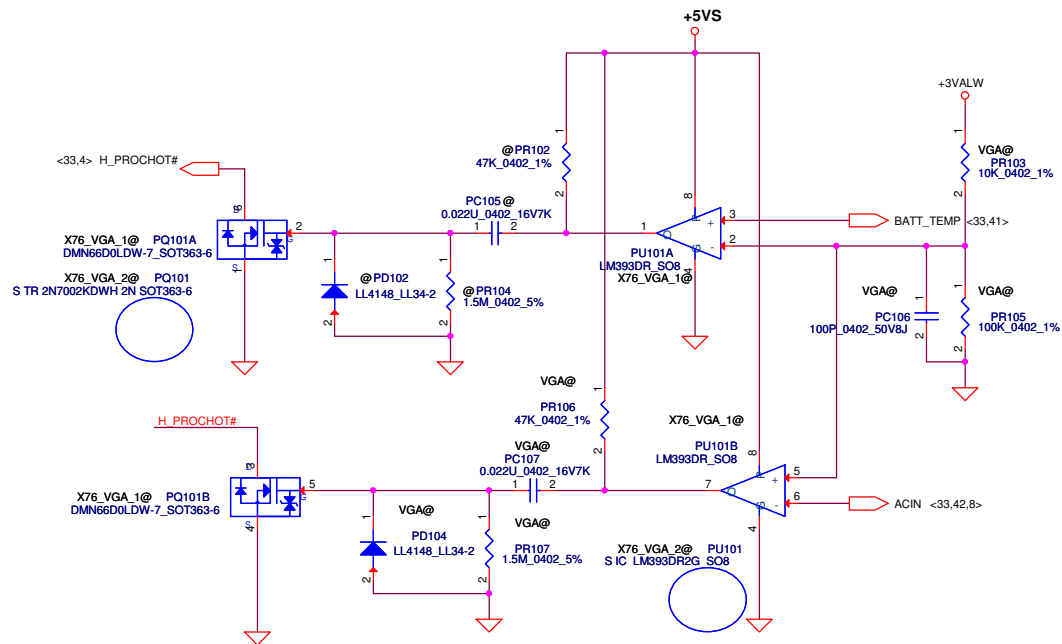
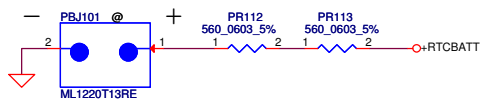
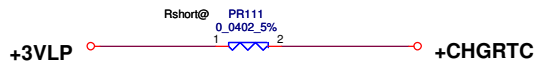
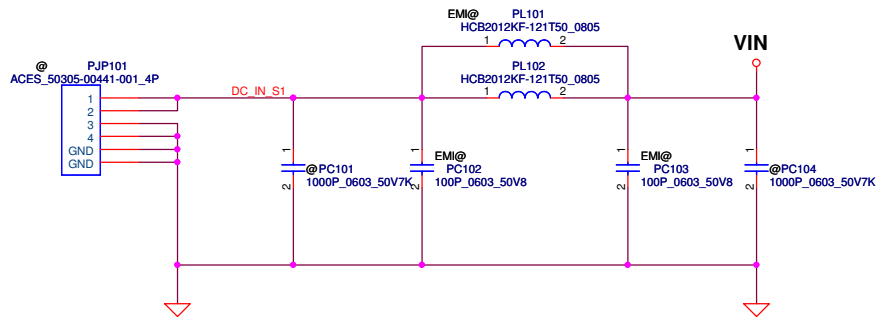
+3V source to +3VSDGPU for GPU



+1.05VS_VTT to +1.05VSDGPU



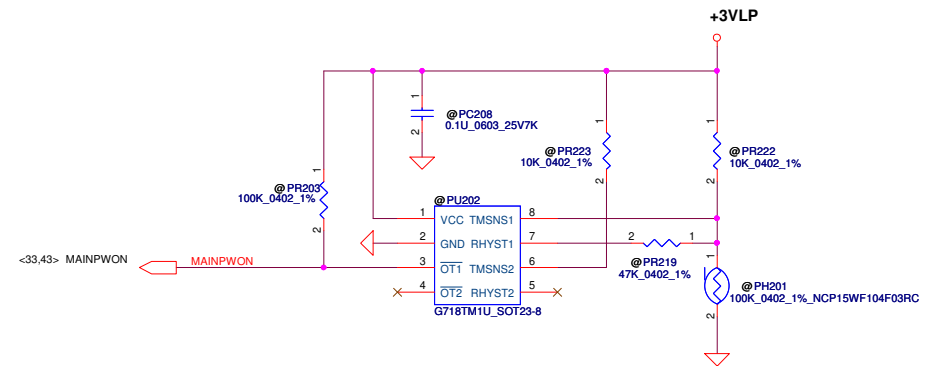
| | | | | | |
|---|------------|--------------------|-----|--------------------------|------------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2012/11/XX | Deciphered Date | EOP | Title | |
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| | | | | Custom | V5MM2 M/B LA-A021P Schematic |
| | | | | Date | Tuesday, August 27, 2013 |
| | | | | Sheet | 39 of 57 |
| | | | | Rev | 1.0 |



UMA Only :ZZZ1

DIS: ZZZ2

| | | | | | |
|--|------------|--------------------|------------|--------------------------|--------------------------|
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| | | | | Date | Tuesday, August 27, 2013 |
| | | | | Sheet | 40 of 57 |



| | |
|-------|------------------|
| VCIN0 | For KB9012 OTP |
| 92°C | 1.2V, Active |
| 56°C | 2.255V, Recovery |

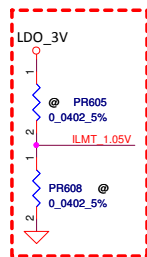
| VCIN1 For KB9012 sense 10mΩ | Active | Recovery |
|-----------------------------------|-------------|------------|
| 65W | 85W, 0.42V | 65W, 0.42V |
| 90W | 117W, 0.56V | 90W, 0.56V |
| 120W | | |

Diagram illustrating the ECAGND pin configuration and associated components:

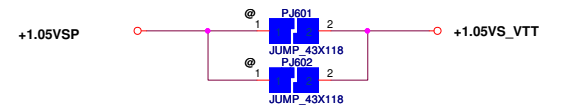
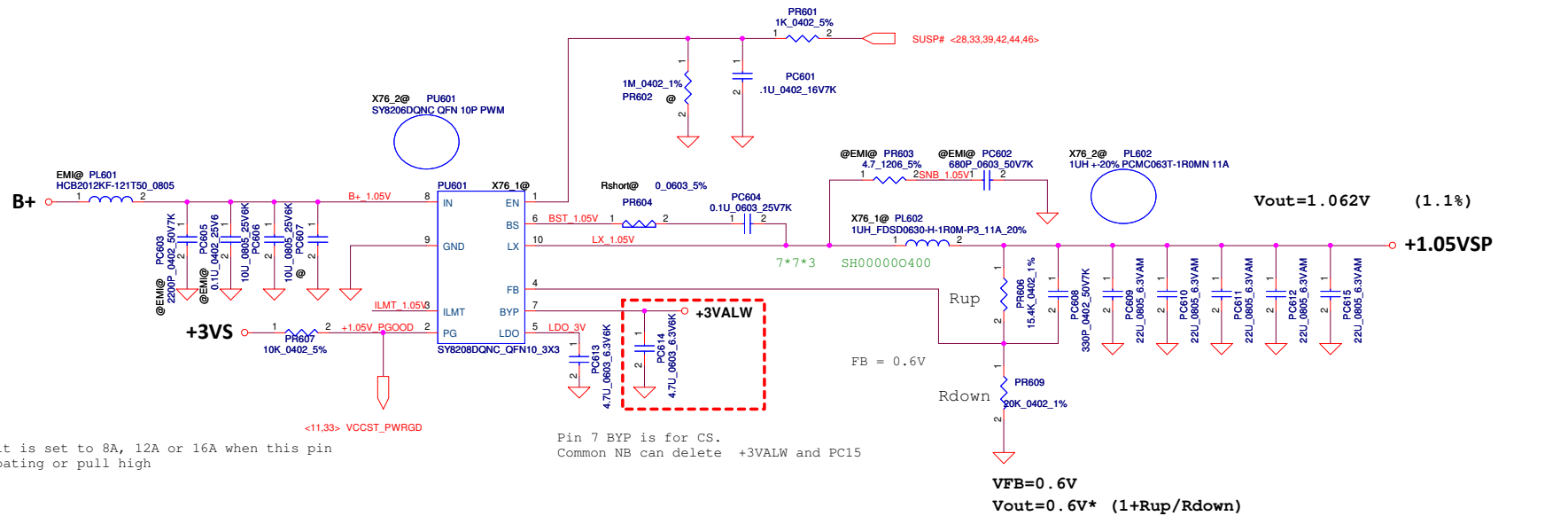
- ECAGND** (Pin 33) is connected to **EC_VCCA** through a network of resistors and a voltage source.
- Resistors:**
 - PR211** (12.4K_0402_1%)
 - PR206** (10K_0402_1%)
 - PR207** (127K_0402_1%)
 - PR225** (10.5K_0402_1%)
- Voltage Source:** **PH202** (100K_0402_1%_NCP15WF104F03RC)
- Power and Temperature Annotations:**
 - 90W@ PR225 10.5K_0402_1%**
 - 90W@ PR207 91K_0402_1%**
 - 65W@ PR225 10K_0402_1%**
 - 65W@ PR207 127K_0402_1%**
- Other Labels:**
 - ADP_I <33,42>**
 - VCIN0_PH <33>**
 - VCIN1_PROCHOT <33>**
 - H_PROCHOT#_EC <33>**

| | | | | | |
|---|------------|--------------------|------------|--------------------------|--------------------------|
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| | | | | Custom | V5MM2 SB |
| | | | | Date: | Tuesday, August 27, 2013 |
| | | | | Sheet | 41 of 57 |
| | | | | Rev | 1.0 |

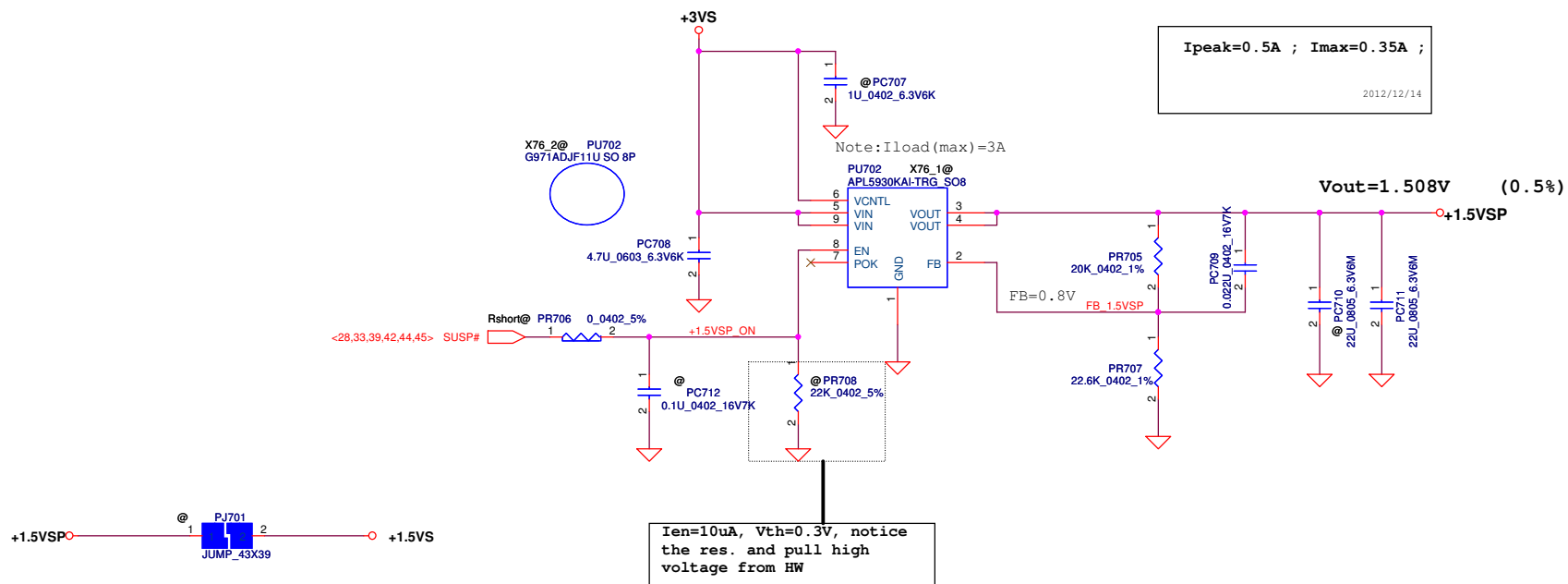
+1.05VSP Ipeak=8A ; I_{max}=5.6A ; OCP=12A
 ,F= 750K Hz (typ) (ILMT_1.05V floating)
 2012/12/14



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



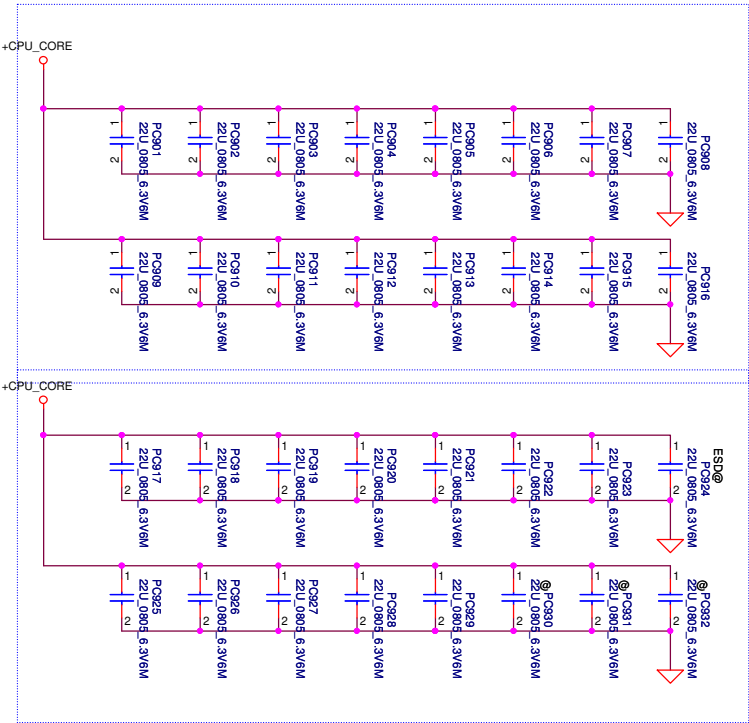
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|---|--------------------|-----------------|--------------------------|-----------------|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2012/07/10 | Deciphered Date | 2013/07/10 | Title |
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| | | | | Document Number |
| | | | | V5MM2_SB |
| | | | | Rev |
| | | | | 1.0 |
| Date: Tuesday, August 27, 2013 | | Sheet | | 45 of 57 |



| | | | | | | | | | | | |
|---|--|--------------------|--|-----------------|--|--------------------------|--|--------------------------|--|----------------|--|
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| | | | | | | Size | | Document Number | | Rev | |
| | | | | | | Custom | | | | 1.0 | |
| | | | | | | Date: | | Tuesday, August 27, 2013 | | Sheet 46 of 57 | |

PWR Rule
CPU DCLL=1.5m ohm dedign 330uF/9m *0, 22uF *30

22u *28, @*4



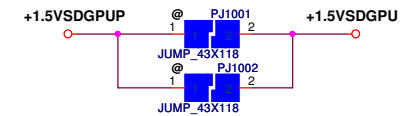
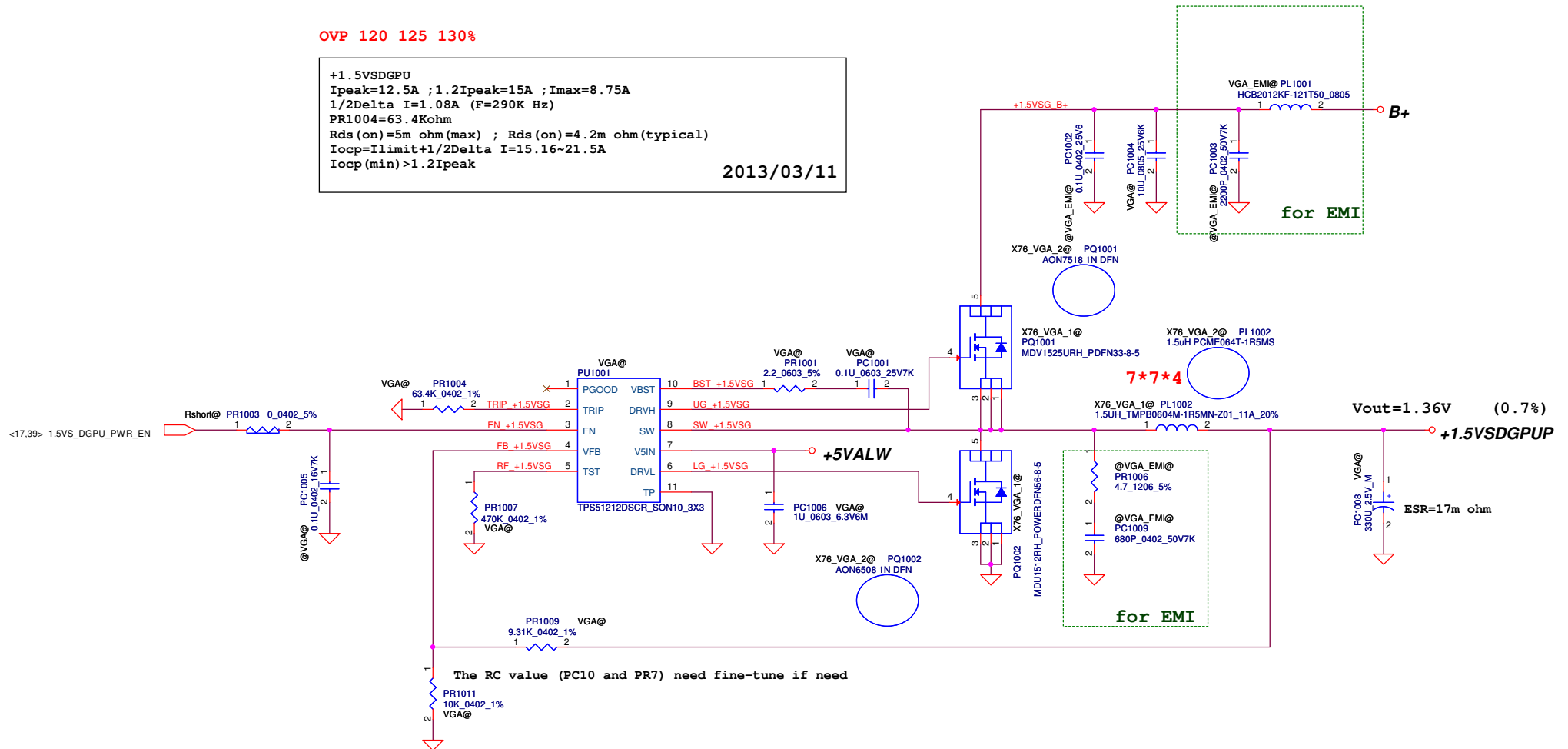
For BOT side

For TOP side

| | | | | | |
|---|------------|--------------------------|------------|--------------------------|----------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2012/07/10 | Deciphered Date | 2013/07/10 | Title | |
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| | | | | Custom V5MM2_SB | 1.0 |
| Date | | Tuesday, August 27, 2013 | | Sheet | 48 of 57 |

```
+1.5VSDGPU
Ipeak=12.5A ; 1.2Ipeak=15A ; Imax=8.75A
1/2Delta I=1.08A (F=290K Hz)
PR1004=63.4Kohm
Rds(on)=5m ohm(max) ; Rds(on)=4.2m ohm(typical)
Iocp=Ilimit+1/2Delta I=15.16~21.5A
Iocp(min)>1.2Ipeak
```

2013/03/11



| | | | | | | |
|---|--------------------|-----------------|-------------|--------------------------|--------------------------|----------------|
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| Issued Date | 2012/04/22 | Deciphered Date | Date of EOP | Title | +1.5VSDGPUP | |
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| | | | | Date: | Tuesday, August 27, 2013 | Sheet 49 of 57 |

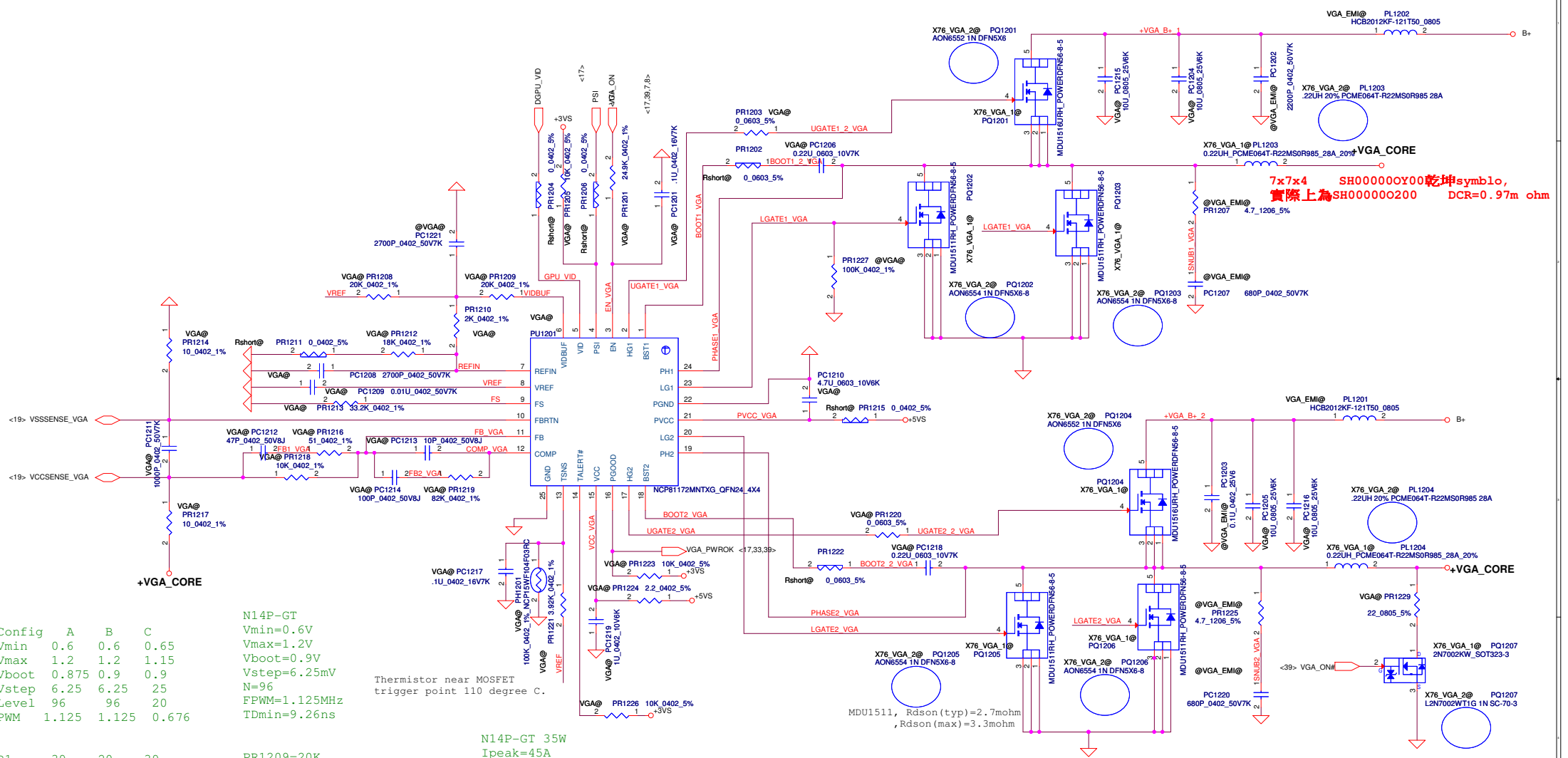
| | | | |
|--------|-------|-------|-------|
| Config | A | B | C |
| Vmin | 0.6 | 0.6 | 0.65 |
| Vmax | 1.2 | 1.2 | 1.15 |
| Vboot | 0.875 | 0.9 | 0.9 |
| Vstep | 6.25 | 6.25 | 25 |
| Level | 96 | 96 | 20 |
| PWM | 1.125 | 1.125 | 0.676 |

N14P-GT
Vmin=0.6V
Vmax=1.2V
Vboot=0.9V
Vstep=6.25mV
N=96
FPWM=1.125MHz
TDmin=9.26ns

PR1209=20K
PR1208=20K
PR1210=2K
PR1212=18K
PR1211=0K
PC1208=2.7nF

N14P-GT 35W
Ipeak=45A
Imax=31.5A
Iocp=80A
Fsw=450KHz
bulk cap 330uF 9m *3 560uF*1

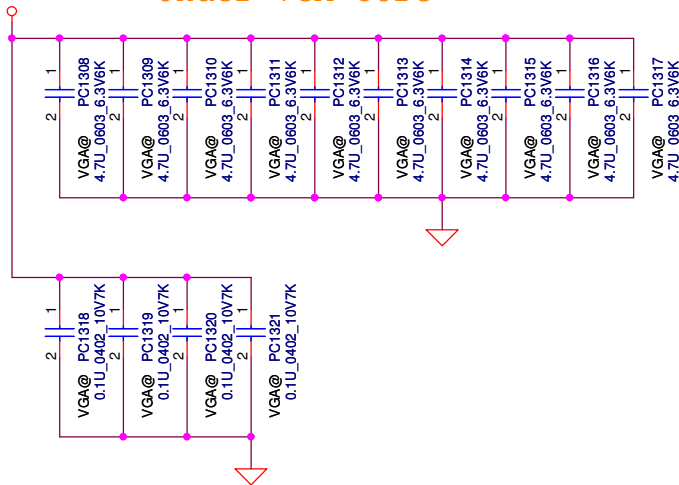
Thermistor near MOSFET
trigger point 110 degree C.



7x7x4 SH000000Y00乾坤symbolo,
實際為SH000000Z00 DCR=0.97m ohm

| | | | | | | | | | | | |
|---|--|--------------------|--|-----------------|--|--------------------------|--|-----------------|--|----------|--|
| Security Classification | | Compal Secret Data | | | | Compal Electronics, Inc. | | | | | |
| Issued Date | | 2011/12/05 | | Deciphered Date | | Date of EOP | | Title | | | |
| | | | | | | | | VGA COREP | | | |
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| | | | | | | | | | | | |
| | | | | | | | | | | | |
| Date: | | | | | | Tuesday, August 27, 2013 | | Sheet | | 50 of 57 | |

+VGA_CORE Under VGA Core



GB4-128

Under

4.7uF_0603_10pcs

0.1uF_0402_4pcs

Near

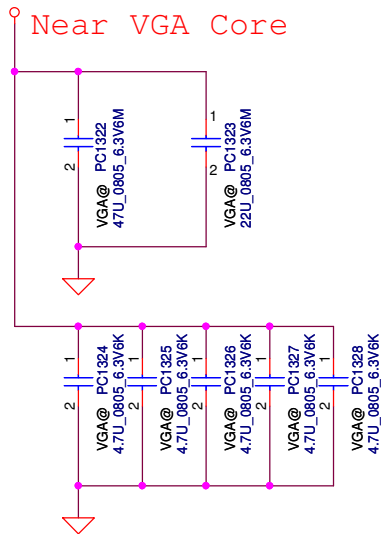
47uF_0805_1pcs

22uF_0805_1pcs

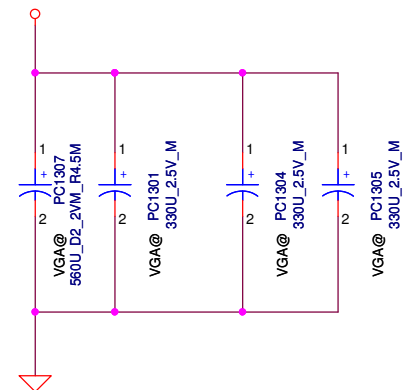
4.7uF_0805_5pcs

+VGA_CORE

Near VGA Core



+VGA_CORE



| | | | | | | |
|---|--------------------|--------------------------|-------------|--------------------------|--|----------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
| Issued Date | 2011/06/24 | Deciphered Date | Date of EOP | Title | | |
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| Size | | Document Number | | Rev | | 1.0 |
| Date: | | Tuesday, August 27, 2013 | | Sheet | | 51 of 57 |

| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | Date | Phase |
|------|-------------------------|---|------|----------|---|-------|-------|
| 1 | Acoustic noise | 3V 5V light load efficiency improvement | | 3V/5V | 1.Add 2pcs 1K_0402_5% (PR412 PR413) 1pcs 4700P_0402_25V7K (PC425) 1pcs 0.047U_0402_25V7K (PC426) 2.Add 4.7u_0402_6.3V6M (PC401) | 01/15 | EVT |
| 2 | Silergy update revision | 3V 5V enable control for Rev0.3. But un-pop. | | 3V/5V | 1.Add un-pop 2pcs 0402 resistors (PR415 PR414) 2.remove (PR207) | 01/15 | EVT |
| 3 | | Reduce part count | | VGA/CPU | Change to R-short (PR1211 PR1204 PR1206 PR1215 PR822) | 01/15 | EVT |
| 4 | | modify charger current to meet battery charge time. | | Charger | 0.02_1206_1%_SD00000S110 charger to 0.01_1206_1%_SD00000K820 (PR310) | 01/15 | EVT |
| 5 | | The modify values for CPU transition test | | CPU | 1.PR803 270K_0402_1%_SD00000G280 change to 255K_0402_1%_SD034255380 2.PR809 392K_0402_1%_SD034392380 change to 383K_0402_1%_SD034383380 3.PR831 10_0603_5%_SD013100A80 change to 22_0603_5%_SD000001R80 4.PC820 1U_0603_10V6K_SE080105K80 change to 2.2U_0402_6.3V6M_SE000008880 | 01/15 | EVT |
| 6 | | BI_GATE remove | | 3V/5V | PQ401 2N7002KW_SOT323-3_SB000009Q80 remove. | 01/16 | EVT |
| 7 | | HW VGA_sequence test | | VGA | 1.PC1201un-pop charger to 0.1U_0402_16V7K_SE076104K80 2.PR1201un-pop charger to 24.9K_0402_1%_SD034249280 3.PR12280_0402_5% charger to un-pop | 01/21 | EVT |
| 8 | | When pwm IC shutdown on S0, EC could detect SLP_S5#, but cannot detect PCH was no power. | | 3V/5V | PR416 add 100K_0402_5%_SD028100380 | 3/11 | DVT |
| 9 | | The 5VALW will fast than 3VALW and the rising time will under 2mS. | | 3V/5V | PC426 4700P_0402_25V7K_SE075472K80 change to 0.01U_0402_25V7K_SE075103K80 PC425 0.047U_0402_25V7K_SE00000MJ00 change to 6800P_0402_25V7K_SE075682K80 | 3/11 | DVT |
| 10 | | VRAM efficiency improvement | | 1.5VDGPU | 1.PQ1002 AON7702A_SB00000T600 change to MDU1512RH_POWERDFN56-8-5_SB00000SY00 2.PQ1001 AON7408L 1N DFN_SB00000H800 change to MDV1525URH 1N PDFN33-8_SB00000S600 3. PL1002 2.2uH_7*7*3_SH00000MR00 charger to 1.5uH_7*7*4_SH00000PM00 | 3/11 | DVT |
| 11 | | The discharge time may cause GC6 entry/exit quickly fail, worry about the off time too long problem cause the GC6 fail. | | VGA | PR1229 add un-pop 22_0805_5%_SD002220A80 PQ1207 add un-pop 2N7002KW_SOT323-3_SB000009Q80 | 3/11 | DVT |

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Version change list (P.I.R. List)

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for PWR

| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | Date | Phase |
|------|-------------|---|------|----------------------------|---|------|-------|
| 1 | | remove VGA enable for +3VSDGPU | | VGA_COREP | remove PR1228_0_0402_5% | 3/11 | DVT |
| 2 | | VRAM voltage change to 1.35V. | | +1.5VSDGPUP | PR1009 11.5K_0402_1%_SD034115280 change to 9.31K_0402_1%_SD034931180 PR1004 137K_0402_1%_SD034137380 change to 63.4K_0402_1%_SD03463K280 | | DVT |
| 3 | | ESD request | | CPU capacitor | Add PC924 22U_0805_6.3V6M_SE000000I10 | 3/11 | DVT |
| 4 | | VCIN1 function | | BATTERY CONN/OTP | PR225 5.1K_0402_1%_SD034510180 change to 9.76K_0402_1%_SD034976180_90W@ 1.02K_0402_1%_SD034102180 change to 9.76K_0402_1%_SD034976180_65W@ PR207 UN-pop-0K_0402_1%_SD034100280 change to 47.5K_0402_1%_SD034475280_90W@ UN-pop-0K_0402_1%_SD034100280 change to 71.5K_0402_1%_SD034715280_65W@ | | |
| 5 | | | | CHARGER | PR318 499K_0402_0.1%_SD00000U380 change to 499K_0402_1%_SD034499380 | 3/11 | DVT |
| 6 | | Material change | | CPU_CORE 1.05V | PH801 SL200000U00 change to SL200000V00 PL602 SH00000PJ00 change to SH000000400 | 4/16 | PVT-1 |
| 7 | | The discharge time may cause GC6 entry/exit quickly fail, worry about the off time too long problem cause the GC6 fail. | | VGA | Add PR1229 22_0805_5%_SD002220A80 Add PQ1207 2N7002KW_SOT323-3_SB000009Q80 | 5/14 | PVT-1 |
| 8 | | Reduce part count | | 1.35V/1.5VSP /1.5VSDGPU | SD028000080 Change to 0402_R-short (PR510 PR706 PR1003) | 5/14 | PVT-1 |
| 9 | | Reduce part count | | 3V/5V/ 1.05V/VGA | SD013000080 Change to 0603 R-short (PR405 PR408 PR604 PR1202 PR1222) | 5/14 | PVT-1 |
| 10 | | follow ON solution for VGA | | VGA | 1. PC1221_SE074272K00_2700P charger to un-pop. 2. PC1208_SE071101J80_100P charger to SE074272K00_2700P | | PVT-1 |
| 11 | | Adjust the FB voltage for 1.35V | | 1.35V | PR506_8.2K_0402_1%_SD000004100 charger to 8.06K_SD034806180. | | PVT-1 |
| 12 | | Material EOL | | 1.35V | PQ502 AON7702A SB00000T600 change to AON7506 SB000010A00 | | PVT-2 |
| 13 | | VCIN1 Recovery 85% chang to 100% | | 3V/5V BATTERY CONN /OTP | PR411 316K_0402_1%_SD034316380 change to 953K_0402_1%_SD00000X100 PR403 402K_0402_1%_SD034402380 change to 160K_0402_1%_SD034160380 PR225 9.76K_0402_1%_SD034976180 change to 10K_0402_1%_SD034100280 (65W@) change to 10.5K_0402_1%_SD034105280 (90W@) PR207 71.5K_0402_1%_SD034715280 change to 127K_0402_1%_SD034127380 (65W@) change to 91K_0402_1%_SD034910280 (90W@) | | PVT-2 |
| 14 | | Adjust the FB voltage for 1.35V | | 1.35V | PR506_8.06K_SD034806180 charger to 8.2K_0402_1%_SD000004100. | | PVT-2 |
| 15 | | Fixed system can't power on. (HW suggest delay the 3V power on sequency.) | | 3V/5V | PC426 0.01U_25V_K_X7R_0402_SE075103K80 change to 0.022U_16V_K_X7R_0402_SE076223K80 | 8/7 | PVT-3 |
| 16 | | ACER must not GC6 function. | | VGA | 1.PR1229 22_0805_5%_SD002220A80 =>un-pop 2.PQ1207 2N7002KW_SOT323-3_SB000009Q80 =>un-pop | 8/7 | PVT-3 |
| 17 | | Cancel ->ACER must not GC6 function. | | VGA | 1.PR1229 un-pop =>22_0805_5%_SD002220A80 2.PQ1207 un-pop =>2N7002KW_SOT323-3_SB000009Q80 | 8/12 | PVT-3 |

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| Item | Page# | Date | Issue Description | Solution Description | Stage |
|------|-------|-----------|---|--|-------|
| 1 | 28 | 2013/1/8 | Add DP++ Schematic | Add Q101,Q102,Q46,R336 , reserve R499,R502 | DVT |
| 2 | 28 | 2013/1/8 | Add DP++ config | Add DM@ , NDM@ | DVT |
| 3 | 28 | 2013/1/8 | Change mDP HPD Schematic from Before-IC to After-IC | | DVT |
| 4 | 28 | 2013/1/8 | for LB_RST no use | pop R1327 for LB_RST no use | DVT |
| 5 | 28 | 2013/1/8 | LB HPD issue | Change R1344 from 100K to 10K | DVT |
| 6 | 28 | 2013/1/8 | for not support LB wake function | Add R503 and unpop it | DVT |
| 7 | 28 | 2013/1/8 | for not support LB wake function | Add J24 | DVT |
| 8 | 31,34 | 2013/1/8 | Remove LAN/B from Acer request | Remove JLAN1 , Add JPWR1 (same as JBL1) | DVT |
| 9 | 31,33 | 2013/1/8 | Remove LAN/B from Acer request | 1. LAN_CLKREQ# pull-high to +3VS (R131,後面remove) 2. Remove C530,R312,R1170 3. reserve R234,R236,R237 for differential pair route space | DVT |
| 10 | 31 | 2013/1/8 | EC Board ID for Rev0.2 | Change R1191 to 8.2K pop R1190,R1191 | DVT |
| 11 | 7 | 2013/1/8 | Change SPI ROM from 4M+2M to 8M | Remove U14,RP20,R109,R402,C67,C453 | DVT |
| 12 | 26 | 2013/1/8 | 1.abnormal display via re-driver board 2. to solve the problem without any gauge increased | 1. Connect JEDP1_pin27 to +3VS, this solution is only for cable which need to pass via re-driver board 2. Add R522,C140 , unpop R421,R424 3. Change Q43 to 2N7002K | DVT |
| 13 | 8 | 2013/1/8 | incorrect gpio define | unpop R214 ,pop R205 | DVT |
| 14 | 28 | 2013/1/8 | For LightningBolt debug , will unpop in PVT | pop SW7 (後面remove) | DVT |
| 15 | 38 | 2013/1/8 | Change TPM IC P/N | Change U89 from SA00005XH00 to SA00005XH40 | DVT |
| 16 | 26,32 | 2013/1/8 | For EMI request , change EMI part P/N | Change L26 to SM01000EJ00 Change L17,L18,L20,L21,L22 to SM070001R00 | DVT |
| 17 | 30 | 2013/1/9 | some risk for OPs on factory side | Change JMINI1 and JMINI2 to JWLAN1 and JMSATA1 | DVT |
| 18 | 34 | 2013/1/9 | Pull-high 10K to +3VS for SMB_ALERT#_R | Add R452 | DVT |
| 19 | 34 | 2013/1/9 | Update KB backlight schematic | Remove Q56,R928 | DVT |
| 20 | 34 | 2013/1/9 | Battery can't detect issue (BI_GATE) | Add R530 , unpop Q30 | DVT |
| 21 | 33 | 2013/1/9 | GC6 schematic update | connect VGA_PWROK to EC_pin120 | DVT |
| 22 | 7 | 2013/1/9 | Change SPI serial resistor value | Change RP19,R108 from 22ohm to 15ohm | DVT |
| 23 | 37 | 2013/1/9 | For BI signal screw hole | Add H19 | DVT |
| 24 | 7 | 2013/1/9 | Change SPI ROM from dual to single | Remove U14,RP20,R109,R402,C67,C453 (多寫) | DVT |
| 25 | 7 | 2013/1/14 | LAN_CLKREQ# already pull-up on CPU side | Remove R313 (已有R52 pull-up) | DVT |
| 26 | 8 | 2013/1/15 | For Cost/Part count | Remove R66 unpop R67,U30 Change R403 from 0ohm to 2ohm | DVT |
| 27 | 28 | 2013/1/15 | For Cost/Part count | Remove SW7,C1443 unpop D64,D65,D66 | DVT |
| 28 | 33 | 2013/1/15 | For Cost/Part count | Remove R1160 | DVT |
| 29 | 34 | 2013/1/15 | For Cost/Part count | Remove R930,SW1 | DVT |
| 30 | 34 | 2013/1/15 | Update BI_GATE schematic | Remove D43,Q34,R489,R530,C888,C890 Q30 change from P-MOS to N-MOS R486,R487 change to 100K ohm | DVT |
| 31 | 39 | 2013/1/15 | For Cost/Part count | Change R987 to 2ohm | DVT |
| 32 | 7 | 2013/1/15 | For Cost/Part count | Change R111 to R-short 0402 | DVT |
| 33 | 27 | 2013/1/15 | For Cost/Part count | Change R368,R369,R409,R410,R417,R418,R415,R419 to R-short 0402 | DVT |
| 34 | 30 | 2013/1/15 | For Cost/Part count | Change R876,R877 to R-short 0402 | DVT |
| 35 | 31 | 2013/1/15 | For Cost/Part count | Change R49 to R-short 0805 | DVT |

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|------|--------|-----------|--|--|-------|
| 36 | 33 | 2013/1/15 | For Cost/Part count | Change R1162 to R-short 0805 | DVT |
| 37 | 34 | 2013/1/15 | For Cost/Part count | Change R929 to R-short 0402 | DVT |
| 38 | 35 | 2013/1/15 | For Cost/Part count | Change R495,R496,R497 to R-short 0603 | DVT |
| 39 | 37 | 2013/1/15 | For Cost/Part count | Change R508,R510 to R-short 0603 | DVT |
| 40 | 39 | 2013/1/15 | For Cost/Part count | Change R988 to R-short 0402 | DVT |
| 41 | 26 | 2013/1/16 | For ESD request | Add C803 | DVT |
| 42 | 34 | 2013/1/16 | Update BI_GATE schematic | Change R486 to 510K , BI_GATE power change to +RTCVCC | DVT |
| 43 | 8 | 2013/1/17 | For ESD request | Add C932,C936,C937 | DVT |
| 44 | 11 | 2013/1/17 | For ESD request | Add C920,C925 | DVT |
| 43 | 39 | 2013/1/17 | For ESD request | Add C940 | DVT |
| 44 | 6 | 2013/1/21 | Change main source on DVT only | Y1 change to SJ100004Z00 | DVT |
| 45 | 32 | 2013/1/21 | Change main source on DVT only | U76,U78 change to SA00003TV00 | DVT |
| 46 | 29 | 2013/1/21 | Change main source for AP-code | Q95,Q96 change to SB966750010 | DVT |
| 47 | 8,39 | 2013/1/21 | Update GC6 schematic | Pop R404,R405 unpop R406,R407 R469 change from 330k to 47k | DVT |
| 48 | 29 | 2013/1/21 | Update LB schematic | R1347 change from 100k to 100 ohm | DVT |
| 49 | 34 | 2013/1/21 | unpop debug switch | unpop SW4 | DVT |
| 50 | 40-53 | 2013/1/22 | update Power schematic 0121A | | DVT |
| 51 | 34 | 2013/1/22 | For X1 code | Change U82 from SA00001TC00 to SA000057Z00 | DVT |
| 52 | 26 | 2013/1/22 | For SMT 統一料 | Change L26 back to SM010014520 | DVT |
| 53 | 26 | 2013/1/23 | eDP HPD issue | Pop R421,R424 ; unpop R522 , C140 | DVT |
| 54 | 26 | 2013/2/7 | eDP HPD issue | Remove Q43 | PVT |
| 55 | 20 | 2013/2/7 | VGA schematic mistake | Change R1245 from 42.2ohm to 40.2ohm | PVT |
| 56 | 39 | 2013/2/19 | Change EN pin for +1.5VSDGPU off-current | Q64 change to Dual-N and gate pin change to 1.5VS_DGPU_PWR_EN , add R984,R998 | PVT |
| 57 | 33 | 2013/2/19 | Add SPOK to turn on/off +3,5VALW | Add EC pin_16 named SPOK | PVT |
| 58 | 36 | 2013/2/19 | Audio SPK sound not balance issue | Change R575 from 1k ohm to 1.2k ohm | PVT |
| 59 | 34 | 2013/2/19 | BI_GATE issue | Change H9 symbol | PVT |
| 60 | 32 | 2013/2/19 | Add RF frame | Add CLIP1 | PVT |
| 61 | 26 | 2013/2/19 | ESD issue | C803 change from 0.1u to 22p | PVT |
| 62 | 33 | 2013/2/19 | Board ID for Rev 0.3 PCB | R1191 change from 8.2k to 18k | PVT |
| 63 | 29 | 2013/2/19 | Change LBT 5V switch schematic | Add U38(USB power switch),C526 Remove Q95,Q96,Q97,U156,R1337,R1338,R1343,R1339.R1340 Change R1347 from 100_0402 to 470_0603 for discharge Change R1341 from 100k to 10k (follow CR) | PVT |
| 64 | 26,33 | 2013/2/19 | No need support wake by Home-Key | Change power to home key from +3VALW to +3VS (JSNSR1.pin12) Change Pull-up domain from +3VALW to +3VS (R1181,R1182,R1183) | PVT |
| 65 | 9 | 2013/2/19 | Add GPIO pin for TPM/no-TPM sku | Add R312,R313 and unpop R312 | PVT |
| 66 | 30 | 2013/2/27 | AOAC on/AOAC off co-lay | Add J21 from +3VS unpop U79,C941 | |
| 67 | 20 | 2013/2/27 | VGA part count and unpop reduce | Remove C1316,C1317 | |
| 68 | 22 | 2013/2/27 | VGA part count and unpop reduce | Remove C1341,C1342,C1327 unpop C1345,C1346,C1348,C1350,C1329,C1331,C1334,C1336 | |
| 69 | 23 | 2013/2/27 | VGA part count and unpop reduce | Remove C1366,C1367,C1355 unpop C1369,C1371,C1372,C1374,C1357,C1358,C1362,C1363 | |
| 70 | 24 | 2013/2/27 | VGA part count and unpop reduce | Remove C1392,C1393,C1378 unpop C1394,C1397,C1399,C1401,C1380,C1382,C1385,C1387 | |
| 71 | 25 | 2013/2/27 | VGA part count and unpop reduce | Remove C1417,C1418,C1404 unpop C1421,C1422,C1423,C1426,C1405,C1407,C1413,C1415 | |
| 72 | 26 | 2013/2/27 | For Cost/Part count | R424 change to R-short 0402 Remove R522,C140 | |

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|------|----------|-----------|--|--|-------|
| 73 | 37 | 2013/3/4 | ME screw change | H4 change from 3P0 to 4P5 , H3 from 2P5 to 3P0 | PVT |
| 74 | 32 | 2013/3/5 | USB charger schematic update | R853 pull-up power rail change from +3VALW to +3VALW_EC | |
| 75 | 31 | 2013/3/5 | Remove JHDD2 | Remove JHDD2 | |
| 76 | 11,15,33 | 2013/3/5 | For ESD request | pop C6,C117,C1255 (Page11,Page15,Page33) | |
| 77 | 30 | 2013/3/5 | For ESD request | Add C62,C63,C64 | |
| 78 | 29 | 2013/3/5 | For ESD request | Add C65 | |
| 79 | 11 | 2013/3/6 | For Cost/Part count | Change R167,R168 to R-short 0402 | |
| 80 | 26 | 2013/3/6 | For Cost/Part count | Change R355,R359,R366,R367,R413,R414,R335 to R-short 0402 | |
| 81 | 32 | 2013/3/6 | For Cost/Part count | Change R852,R855,R865,R866 to R-short 0402 | |
| 82 | 33 | 2013/3/6 | For Cost/Part count | Change R80 to R-short 0402 | |
| 83 | 38 | 2013/3/6 | For Cost/Part count | Change R978,R980 to R-short 0402 | |
| 84 | 20 | 2013/3/6 | For Cost/Part count | Change R1241 to R-short 0603 | |
| 85 | 35 | 2013/3/6 | For Cost/Part count | Change R518,R520,R527,R529 to R-short 0603 | |
| 86 | 36 | 2013/3/6 | For Cost/Part count | Change R519,R521,R524,R525,R556,R566,R567 to R-short 0603 | |
| 87 | 17 | 2013/3/6 | Update GC6 schematic | Add D3,Q95 Remove Q84,,Q90,R1204 Change R1201 from 10k to 1k Reserve R1205 | |
| 88 | 35,36 | 2013/3/6 | Audio PoPo issue | Add U31,R1313 and un-pop Add R408 Amp PD pin change from EC_MUSE# to AMP_MUTE# | |
| 89 | 9,34 | 2013/3/6 | Add I2C for touchpad | Add R84,R85 and unpop Add R82,R83,R1337,R1338 | |
| 90 | 28 | 2013/3/8 | Update LBT schematic (TI request) | Swap Q101A pin3 and pin4 | PVT2 |
| 91 | 19 | 2013/3/8 | Change VRAM power from 1.5V to 1.35V | Change R1229 from 24.9k to 34.8k | |
| 92 | ALL | 2013/3/11 | Combine power schematic 0311A | Combine power schematic 0311A | |
| 93 | 38 | 2013/3/13 | Change TPM power from +3VALW to +3VS | pop J17 , unpop J16 | |
| 94 | 28 | 2013/4/1 | Add F1 for LBT fuse | Add F1 | |
| 95 | 34 | 2013/4/1 | Update H9 symbol | Update H9 footprint | |
| 96 | ALL | 2013/4/1 | Update All RC*NEW footprint | | |
| 97 | 7,10,31 | 2013/5/9 | Remove LAN | Remove C168,C169,R234,R,236,R237 | |
| 98 | 34 | 2013/5/9 | Reserve one/two Lid-switch funtion | Add U83,U84,R930.R931,C989,C990,C991,C992 | |
| 99 | 6,11 | 2013/5/9 | For Cost/Part count | Change R76,R180 to R-short 0402 | |
| 100 | 35,36 | 2013/5/9 | For Cost/Part count | Change R408,R512,R513 to R-short 0402 | |
| 101 | 6,10 | 2013/5/9 | For Cost/Part count | Change R75,R155 to R-short 0603 | |
| 102 | 28 | 2013/5/9 | For Cost/Part count | Change R373,R381 to R-short 0402 | |
| 103 | 9 | 2013/5/10 | Add net for 2nd hall sensor Lid-out | Change PCH GPIO14 for EC LID_OUT TAB (LID_OUT need place between GPIO1 to GPIO15) | |
| 104 | 7,9 | 2013/5/10 | Change Card-Reader CLK from Port5 to Port1 | modify net name : GPIO19 -> CARD_CLKREQ# CARD_CLKREQ# -> GPIO23 | |
| 105 | 33 | 2013/5/16 | Add Pull-up for LID_SW#_TAB | Add R1163 | |
| 106 | 9 | 2013/5/16 | reserve Pull-up for EC_LID_OUT#_TAB | Add R249 and reserve it | |
| 107 | 16 | 2013/5/22 | pop C141 | Pop C141 | |
| 108 | 15,16 | 2013/5/22 | Change 1uF to 2.2uF | Change C108,C123,C130,C143 to 2.2uF | |
| 109 | 22,23 | 2013/5/22 | Change 1uF to 2.2uF | Change C1328,C1343,C1356,C1368 to 2.2uF | |
| 110 | 24,25 | 2013/5/22 | Change 1uF to 2.2uF | Change C1379,C1395,C1409,C1419 to 2.2uF | |
| 111 | 28 | 2013/5/22 | Co-lay LBT schematic | Remove D1 Add U66 and co-lay with F1 | |
| 112 | 12,15 | 2013/5/22 | For Cost/Part count | Remove R210,C50,C34,C126 | |
| 113 | 15,16 | 2013/5/22 | For Cost/Part count | Remove C107,C109,C121,C122,C129,C131,C144,C146 | |

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|------|--------|-----------|--|--|--------|
| 114 | 22 | 2013/5/22 | For Cost/Part count | Remove C1346,C1350,C1331,C1336 | PVT2 |
| 115 | 23 | 2013/5/22 | For Cost/Part count | Remove C1371,C1374,C1358,C1363 | |
| 116 | 24 | 2013/5/22 | For Cost/Part count | Remove C1397,C1401,C1382,C1387 | |
| 117 | 25 | 2013/5/22 | For Cost/Part count | Remove C1422,C1426,C1407,C1415 | |
| 118 | 30, 31 | 2013/5/22 | For Cost/Part count | Remove C946,C961,R869,R870,C870,C872 | |
| 119 | 33 | 2013/5/22 | For Cost/Part count | Remove C1269,C1257 | |
| 120 | 28, 29 | 2013/5/23 | Change LBT power rail to +3VS/+5VS | U38 change from +5VALW to +5VS Remove J23 (+3VALW JUMP) | |
| 121 | 22 | 2013/5/24 | Pop VGA cap | Pop C1345,C1348,C1329,C1334 | |
| 122 | 23 | 2013/5/24 | Pop VGA cap | Pop C1369,C1372,C1357,C1362 | |
| 123 | 24 | 2013/5/24 | Pop VGA cap | Pop C1394,C1399,C1380,C1385 | |
| 124 | 25 | 2013/5/24 | Pop VGA cap | Pop C1421,C1423,C1405,C1413 | |
| 125 | 33 | 2013/5/28 | Change Board ID | Change R1191 from 18K to 33K | |
| 126 | 28 | 2013/5/29 | Add cap for Lightning Bolt 3V power | Add C262 (47uF) | |
| 127 | 24 | 2013/5/30 | Add cap for VGA 1.5V (debug) | Add C1401 (0.1uF) | |
| 128 | 9 | 2013/5/30 | Change LID_OUT GPIO from GPIO14 to GPIO8 | Change GPIO8,GPIO14 net name | |
| 129 | 34 | 2013/5/31 | Update Part Number for PVT-2 SMT | Change U82,U83,U84 to SA00003G100 | |
| 130 | ALL | 2013/6/4 | Combine Power schematic 0603 | Combine Power schematic 0603 | |
| 131 | 17 | 2013/6/4 | Update Part Number for PVT-2 SMT | Change D62 to SCS00000Z00 | |
| 132 | 30 | 2013/7/2 | Update WLAN schmatic | Change C958 from 4.7uF to 10uF Add C961 | PVT3 |
| 133 | 6 | 2013/7/3 | For layout spacing | Remove R74 | |
| 134 | ALL | 2013/7/5 | Combine Power schematic 0627 | Combine Power schematic 0627 | |
| 135 | ALL | 2013/7/29 | Combine Power schematic 0729 | Combine Power schematic 0729 | |
| 136 | 34 | 2013/7/31 | Remove Buzzer schematic | Remove BUR1,Q53,R492,R493 | Pre-MP |
| 137 | 34 | 2013/7/31 | Update BI_GATE schematic (2nd BI_GATE) | Add R86 and unpop it | |
| 138 | 30 | 2013/8/1 | Update mSATA schematic for DEVSLP function | Change R877 from R-short to unpop | |
| 139 | 33 | 2013/8/4 | Change Board ID | Change R1191 from 33K to 56K | |
| 140 | ALL | 2013/8/14 | Combine Power schematic 0812A | Combine Power schematic 0812A | |
| 141 | ALL | 2013/8/27 | Combine Power schematic 0814 | Combine Power schematic 0814 | |