

Compal Confidential

Model Name : V5MM2\_Ezel\_HW

File Name : LA-A021P

Compal Confidential

M/B Schematics Document

Intel Shark Bay ULT (Hasswell + Lynx Point-LP)

nVidia N14P-GT

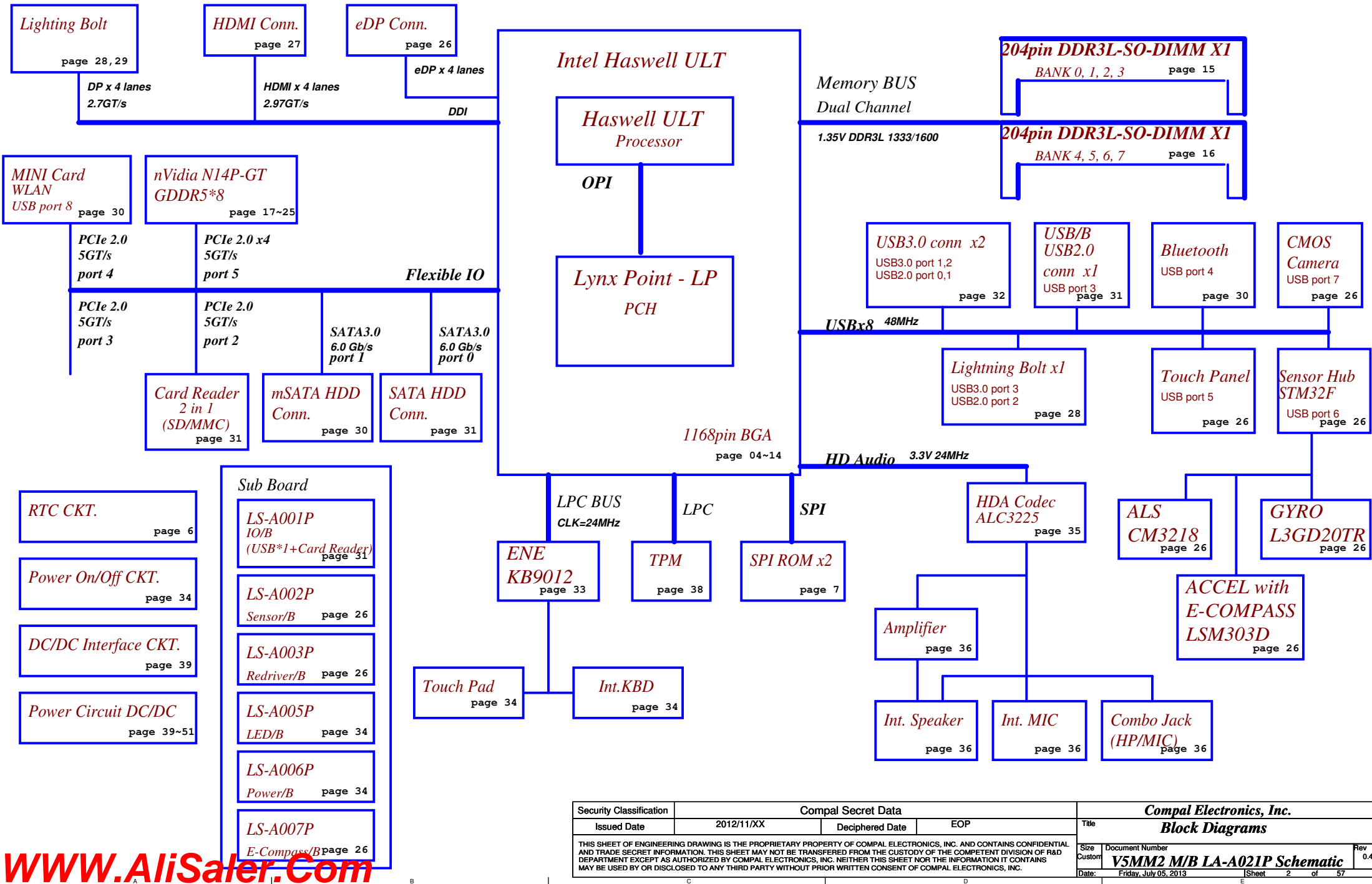
2013-06-XX

REV : 0 . 4

ZZZ1

Part Number	Description
DA6000Z3100	PCB LA-A021P REV0 M/B

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				<b>Block Diagrams</b>	
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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VSP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDRIII L	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VSDGPUP to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU switched power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

**EC SM Bus1 address**

### EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X	On Board Thermal Sensor	0100 110x
		VGA Internal Thermal Sensor	0100 000x
		G Sensor	0011 000x

## PCH SM Bus address

Device		Address	
ChannelA	DIMM0	1001 000x	JDIMM1
ChannelB	DIMM1	1001 010x	JDIMM2

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

## USB Port Table

USB 2.0	Port	
EHCI1	0	USB3.0 Connector (Left)
	1	USB3.0 Connector (Left)
	2	Lightning Bolt MDP Conn.
	3	USB2.0 (USB/B)
	4	Mini Card (WLAN+BT)
	5	Touch Panel
	6	Sensor Hub
	7	Camera

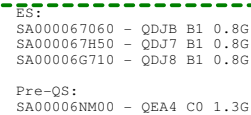
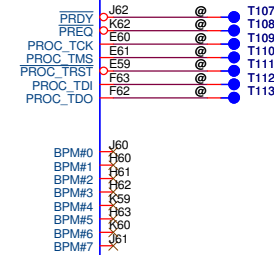
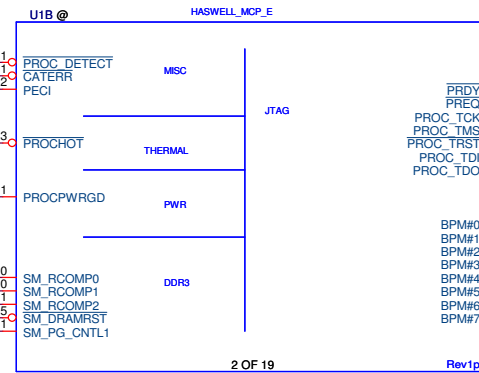
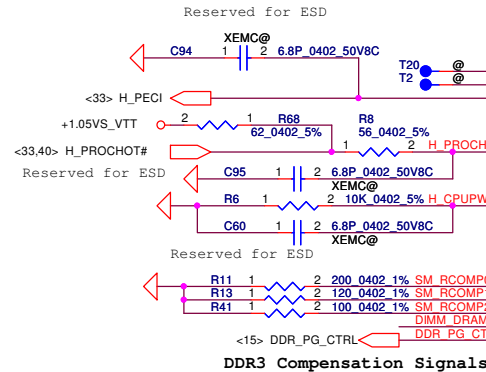
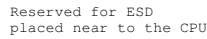
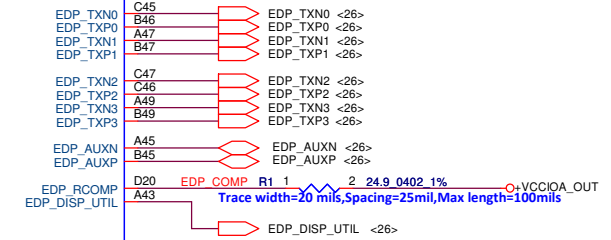
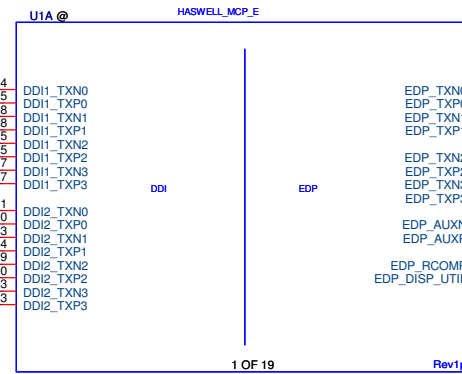
USB 3.0	Port	
XHCI	1	USB Port(Left 3.0)
	2	USB Port(Left 3.0)
	3	Lightning Bolt USB3.0
	4	

### B0M Option Table

[illegible]

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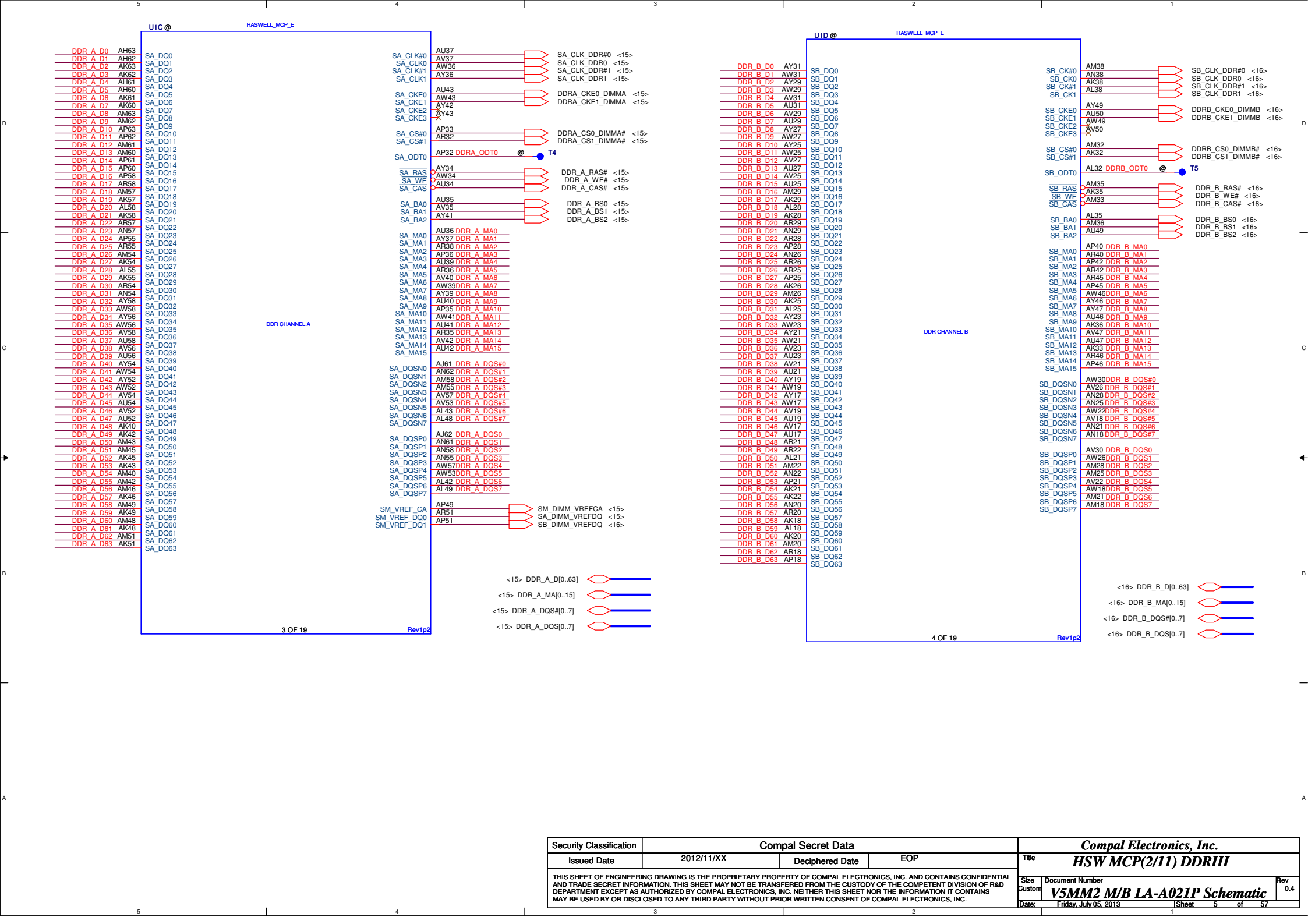
**3, 2 connected to TI-HD3SS2521**

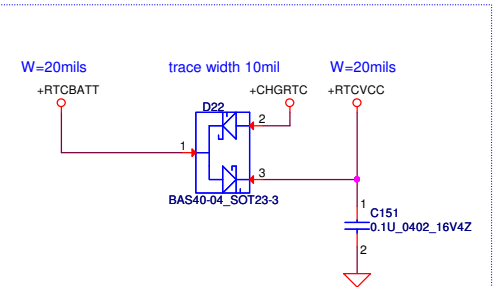
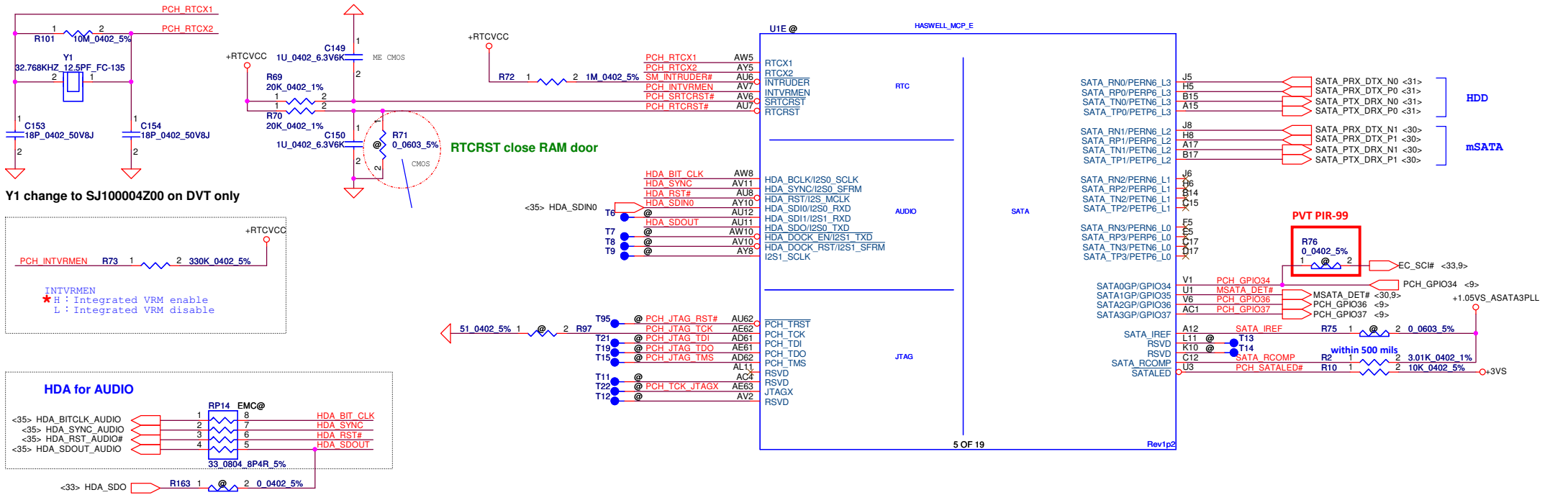


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SA000067060 SA000067H50 SA00006FY20 SA00006G120

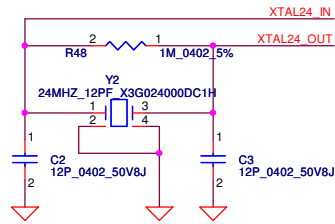
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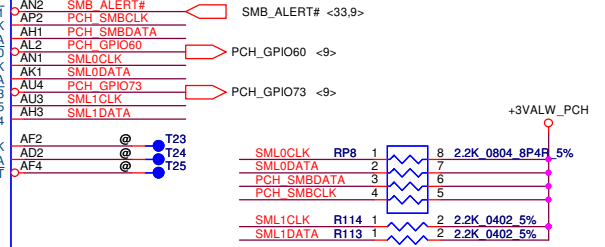
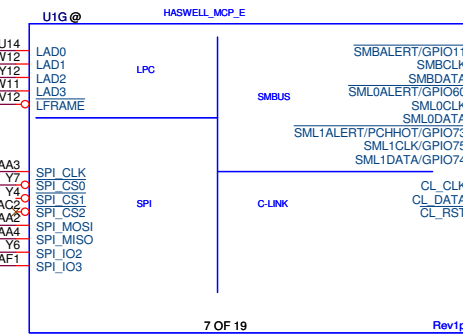
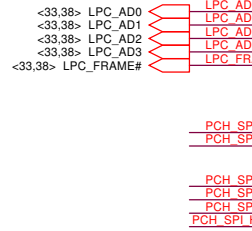
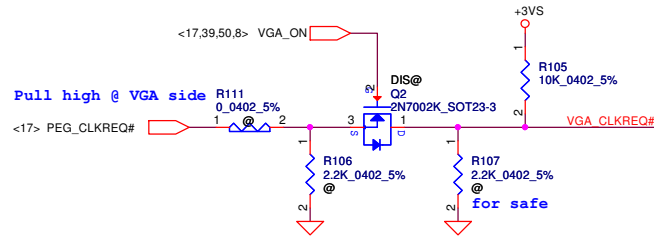
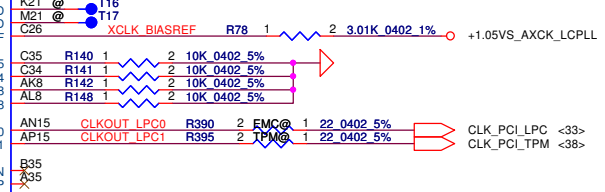
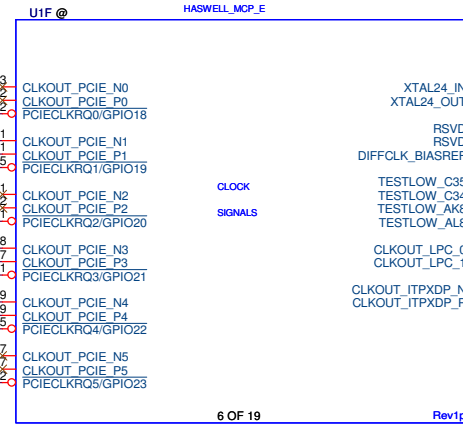
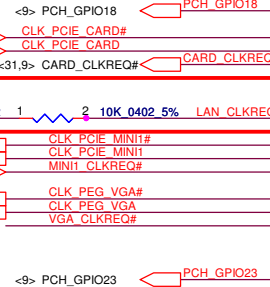


Card Reader

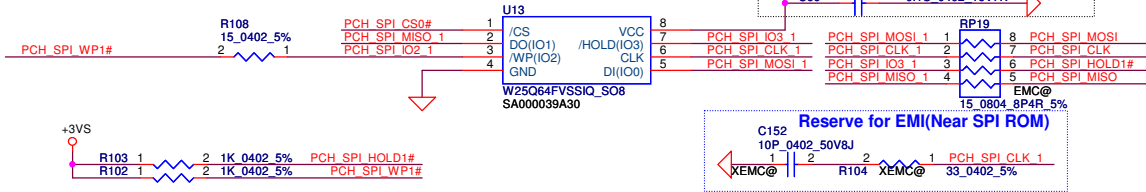
PCIE LAN

WLAN

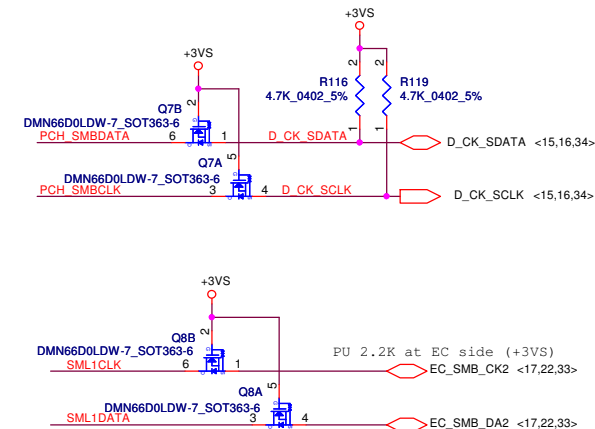
VGA



## SPI ROM ( 8MByte )

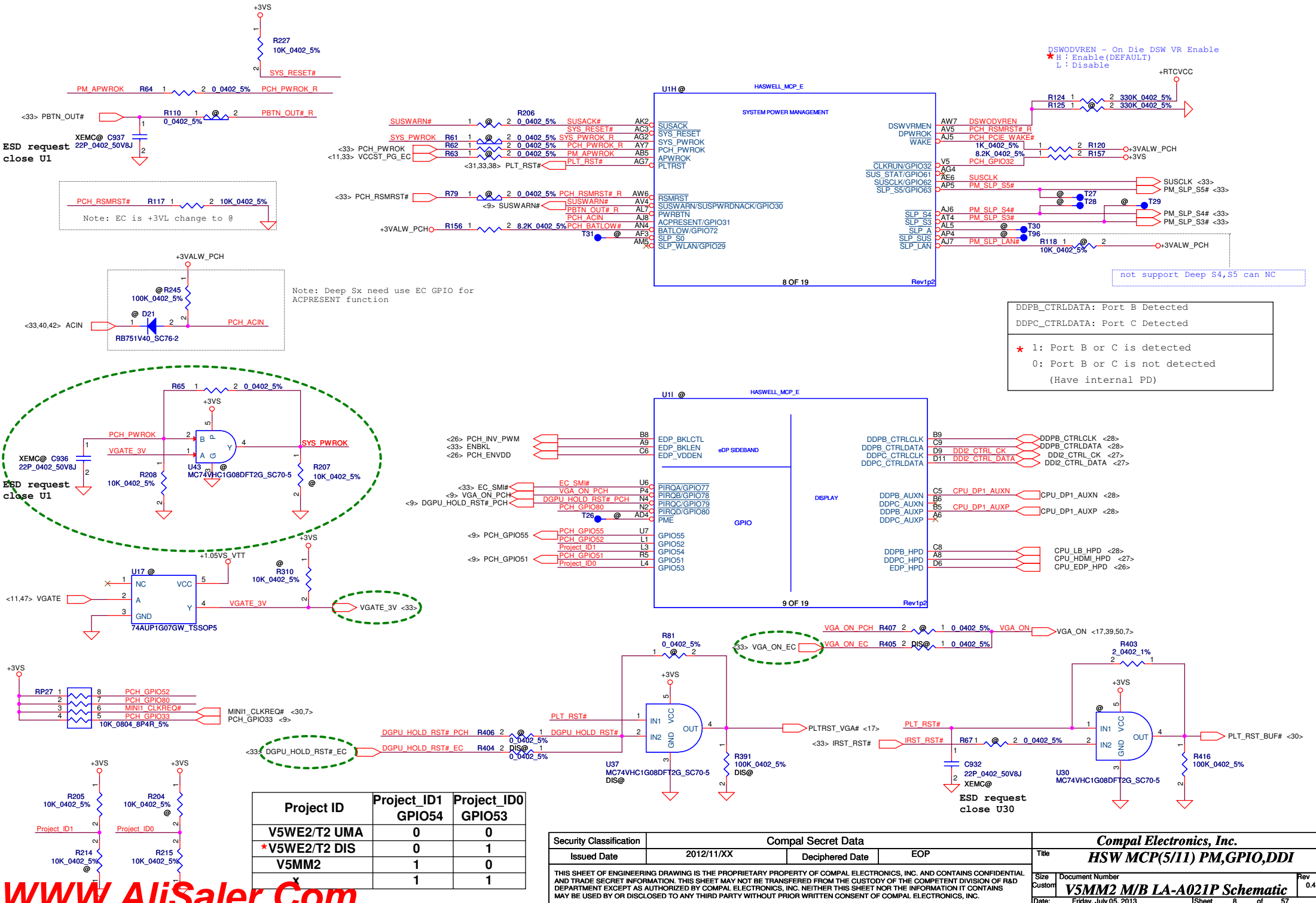


D29 design for Debug board flash SPI ROM (can be short after MP)



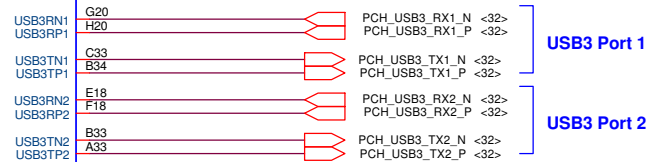
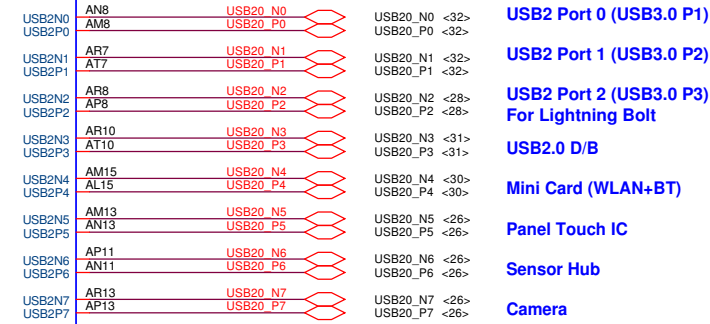
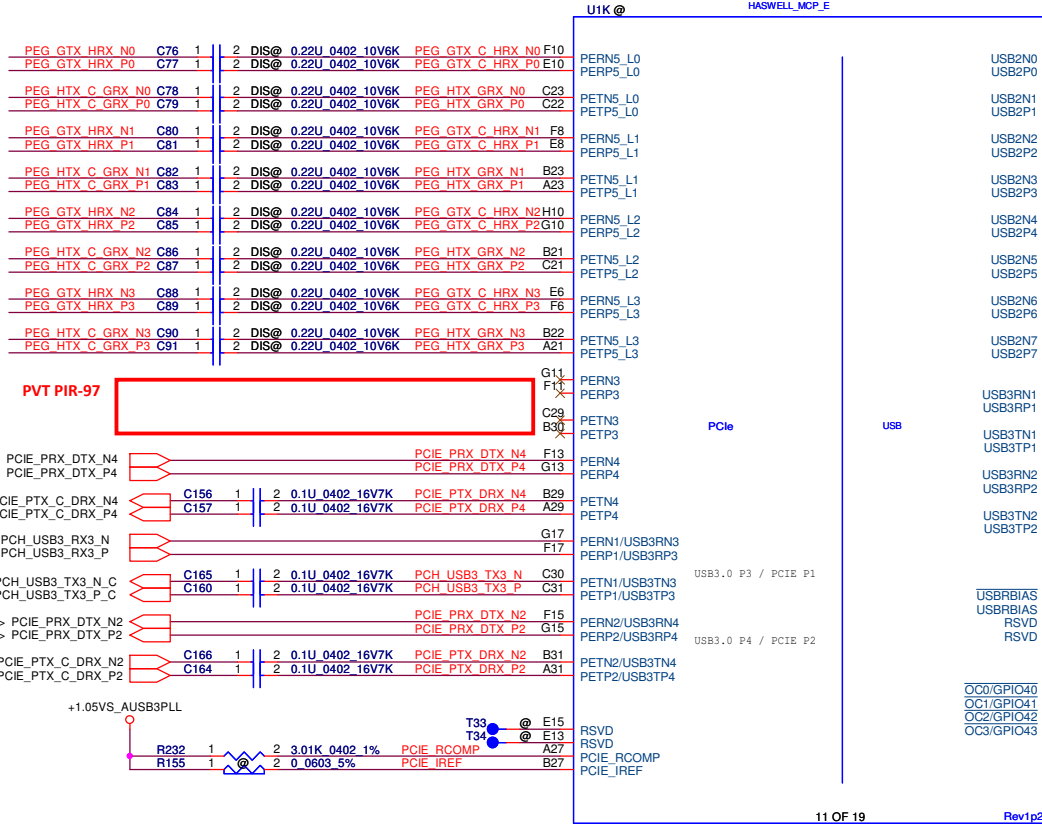
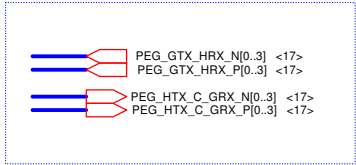
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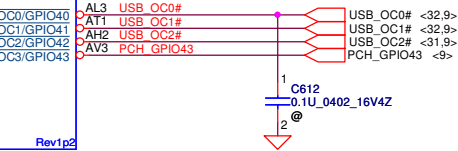




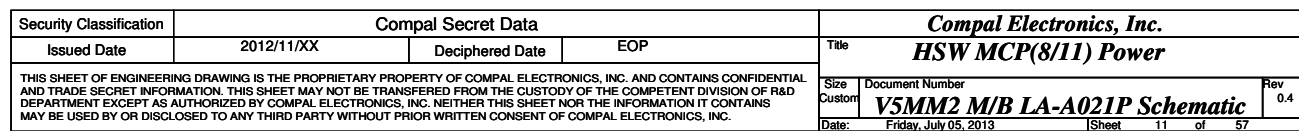
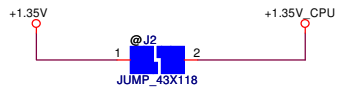




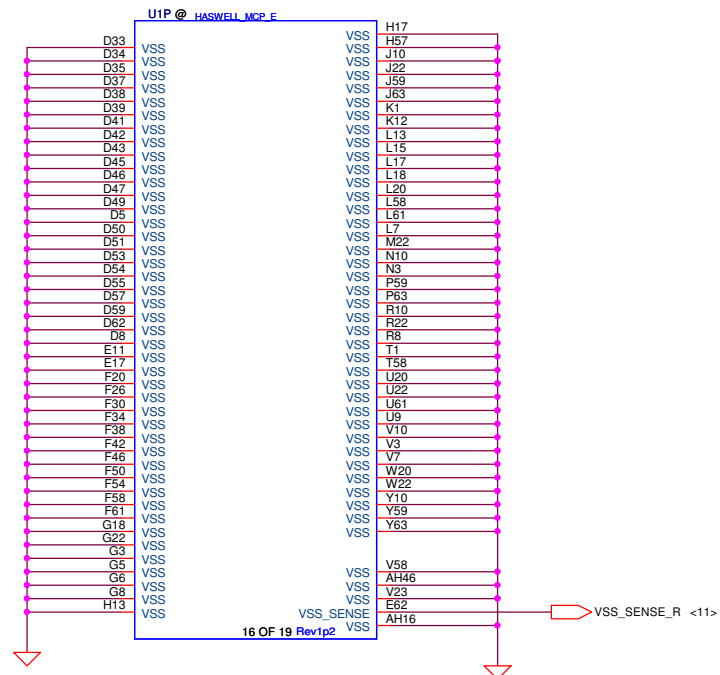
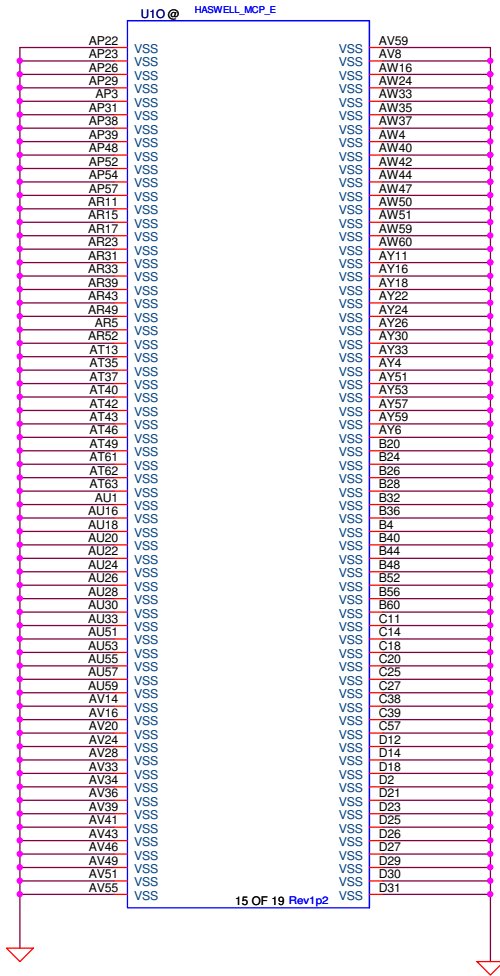
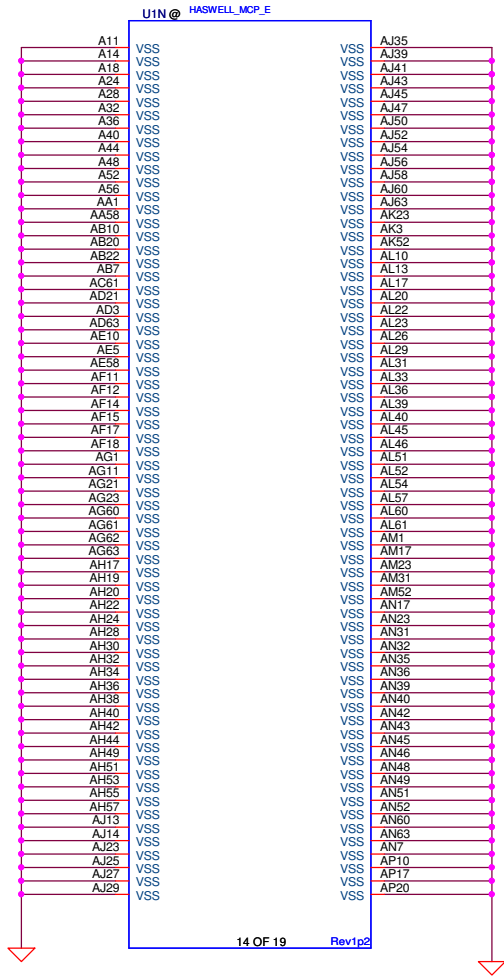
CAD note:  
Route single-end 50-ohms and max 450-mils length.  
Avoid routing next to clock pins or under stitching capacitors.  
Recommended minimum spacing to other signal traces is 15 mils

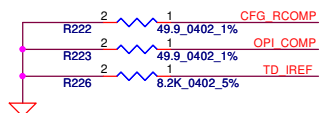
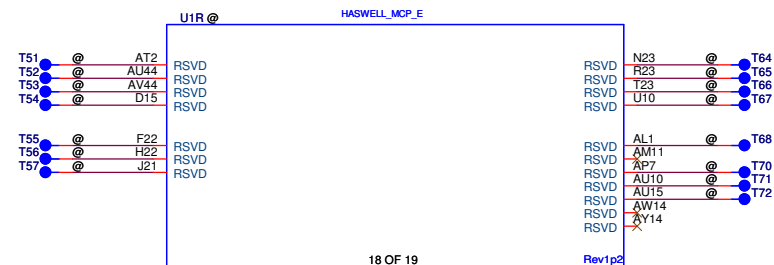


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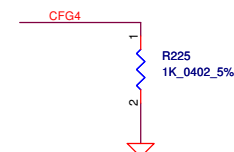




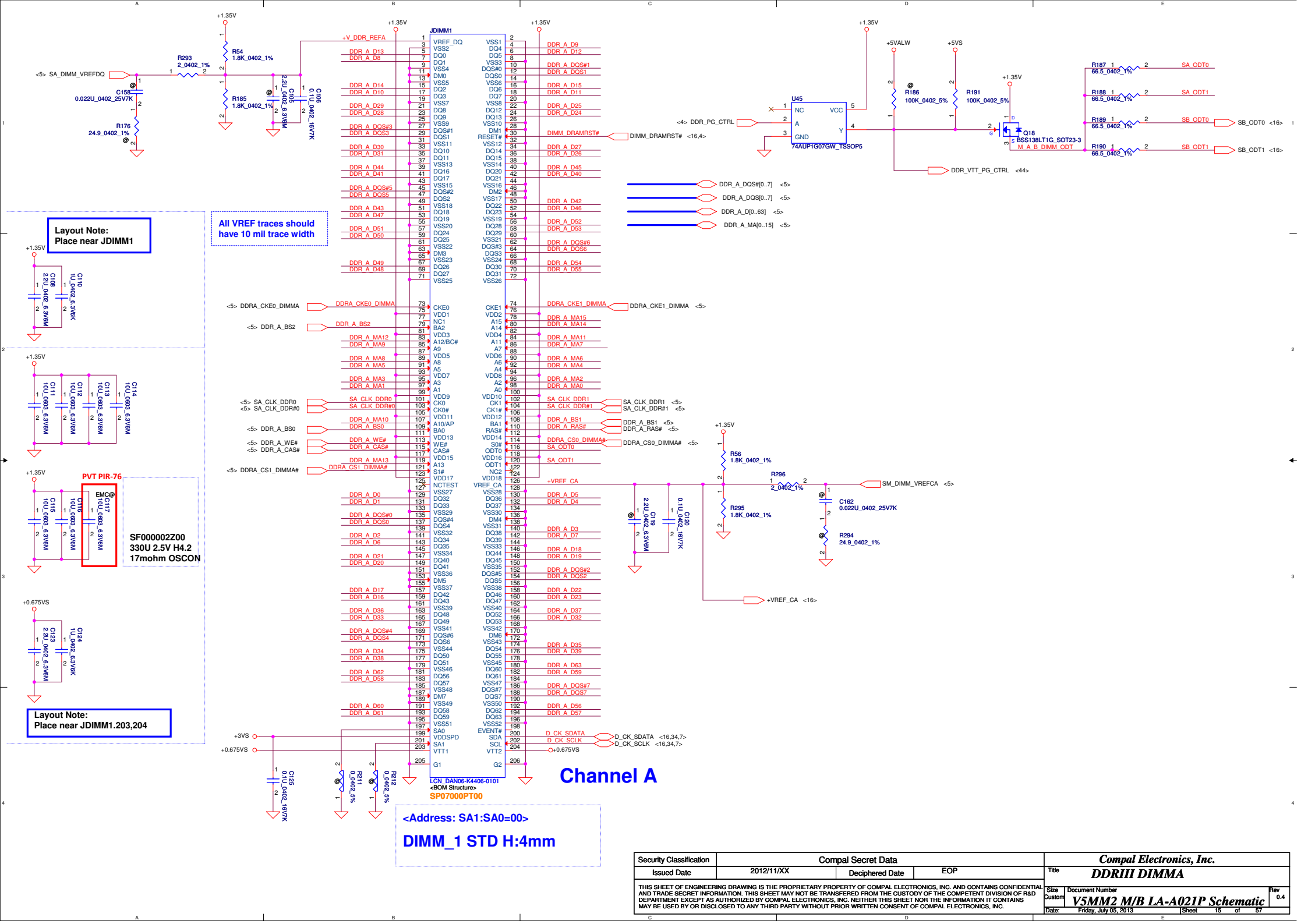


A circuit diagram showing a 1k resistor, labeled R224 1K\_0402\_1%, connected between the CFG3 pin and ground. The resistor is represented by a blue zigzag line. The CFG3 pin is labeled in red at the top. The ground connection is shown as a red triangle at the bottom. The resistor is labeled with its value and a blue '@' symbol.

Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



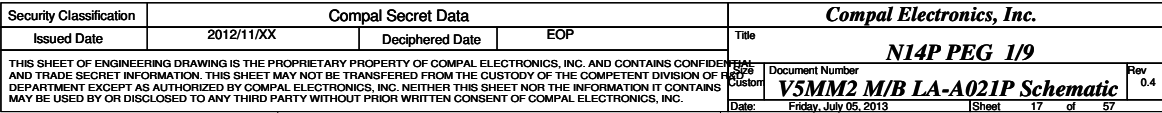
Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



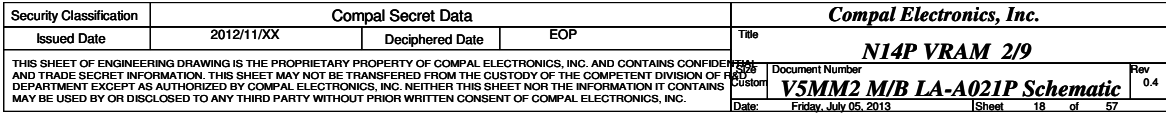


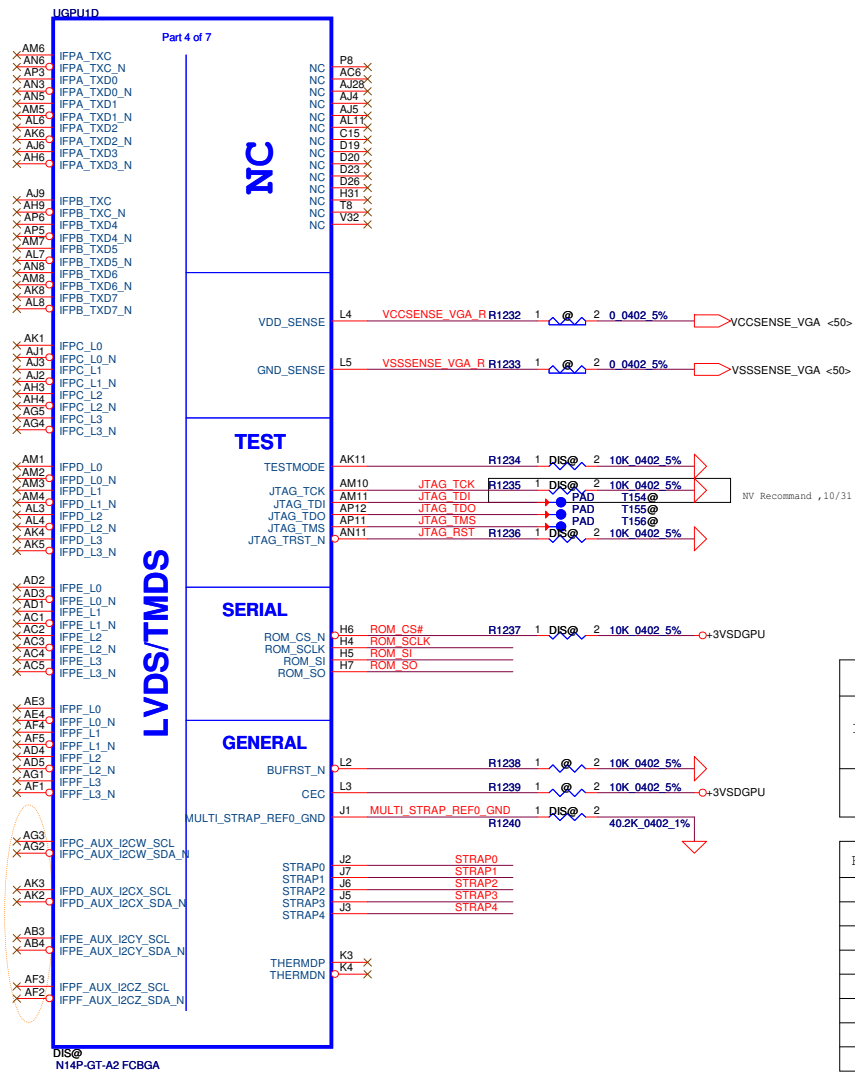


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VRAM BOM Config

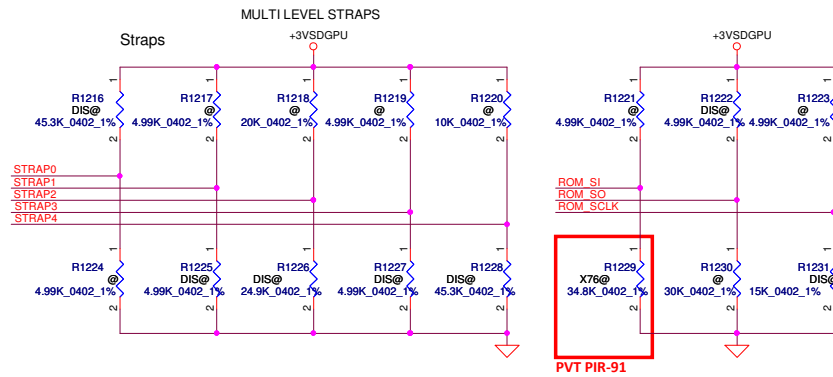
64Mx32x4

64Mx32x4

VRAM P/N

HYN 64\*32 2000M SA00004GD30 (S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABOI)

HYN 64\*32 2000M SA00004GD50(S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABOI)



For N14P-GT-A1 (ES2) A2 (QS) strap table Decive ID : 0x0FE4

GDDR5	Vendor	Strap	ROM_SI
128M x 16	Hynix (M)	Ox4	24.9K
	Samsung	Ox5	30.1K
	Hynix (M)	Ox6	34.8K

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GT	900 MHZ	128M*16	Hynix	R PU 45K	R PD 5K	R PD 25K	R PD 5K	R PD 45K	R PD 25K	R PU 5K	R PD 15K
			Samsung						R PD 30K		

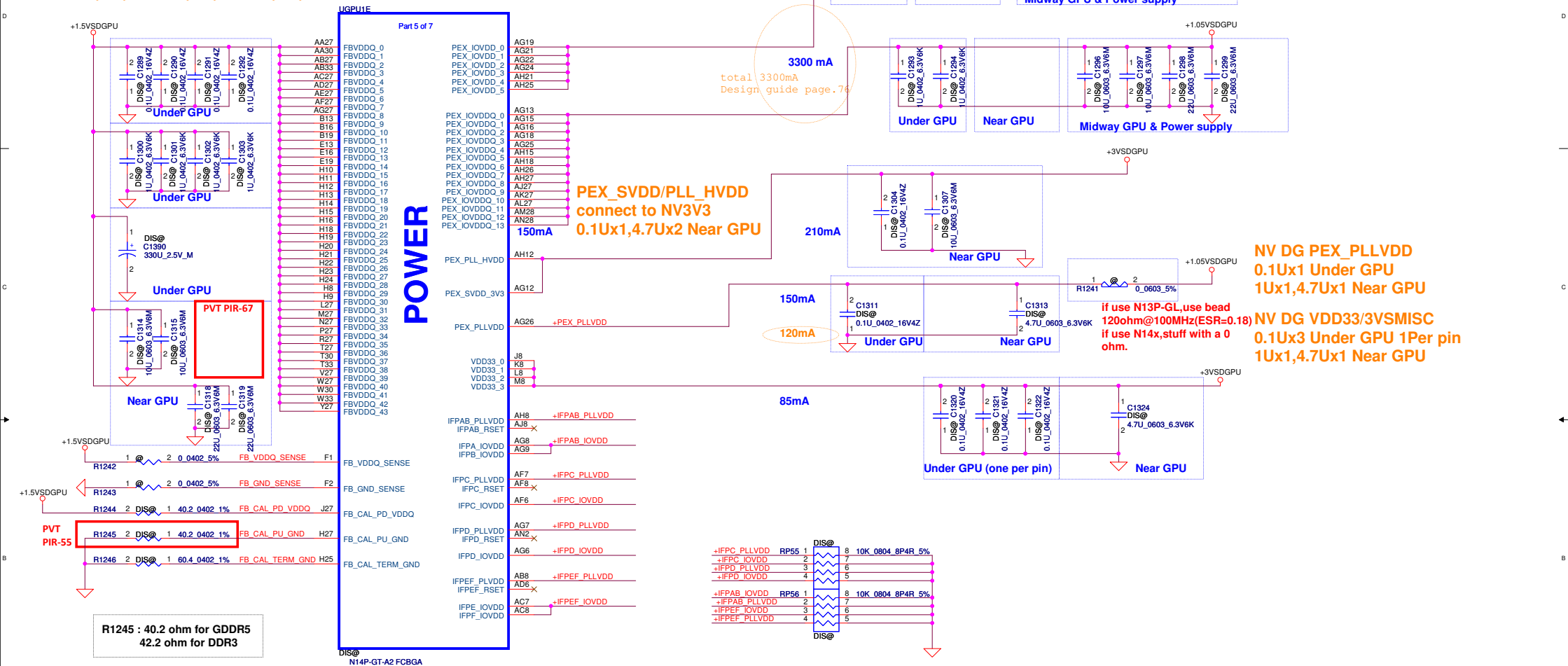
Resistor Values	Pull-up to +3V	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

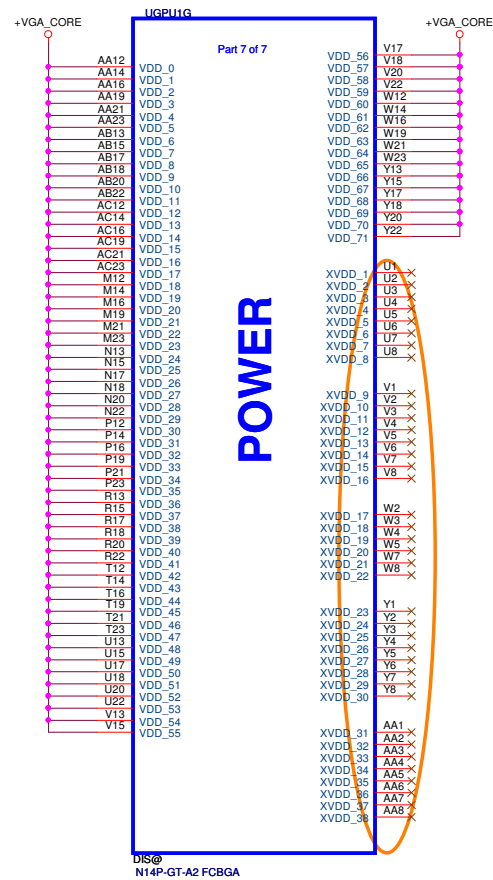
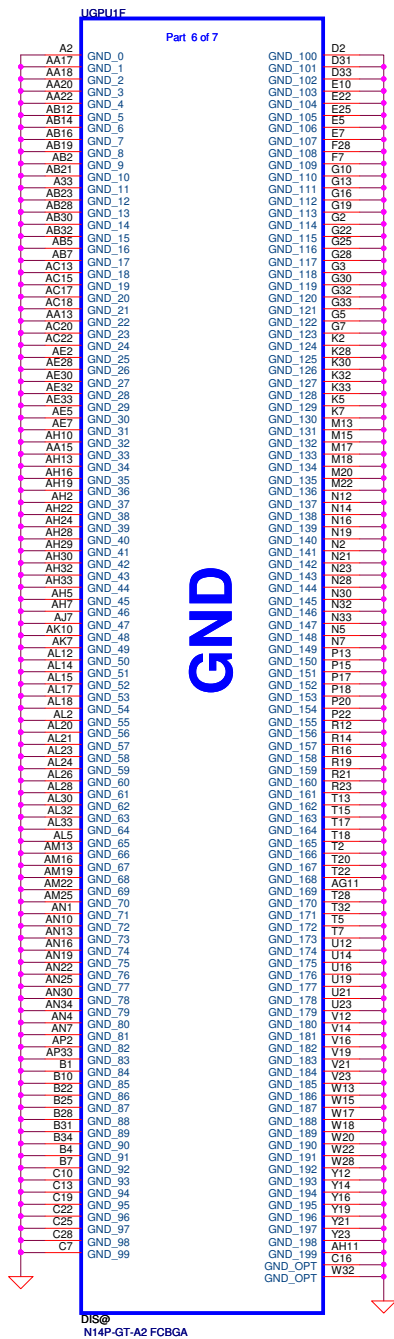
STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]
STRAP3	SOR[3:0]
STRAP4	PEG_SPEED_CHANGE_GEN3, PEX_MAX_SPEED,DP_PLLVDD33V
ROM_SCLK	PCI_DEV[4],SUB_VENDOR, PCI_DEV[5],PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3:0]
ROM_SO	FB_BAR_SIZE[1:0],SMB_ ALT_ADDR, VGA_DEVICE

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**NV DG FBVDDQ(GDDR5)**  
**0.1Ux6(3@),1Ux6(3@),Under GPU**  
**4.7Ux6(3@) ,10Ux4(2@),22Ux4(2@) Near GPU**

N13P-GS 10.44A  
N13P-GT 10.51A



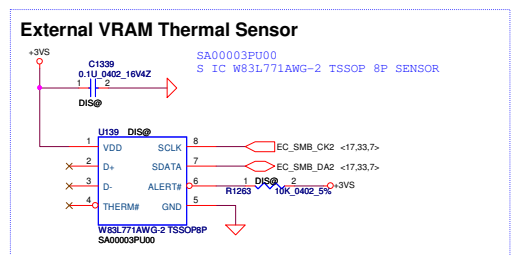


N14P-GT EDP peak 45A

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## BOT / M501

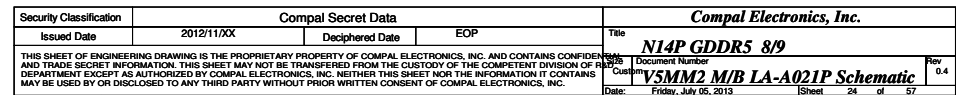


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A

## BOT / M504

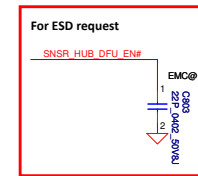
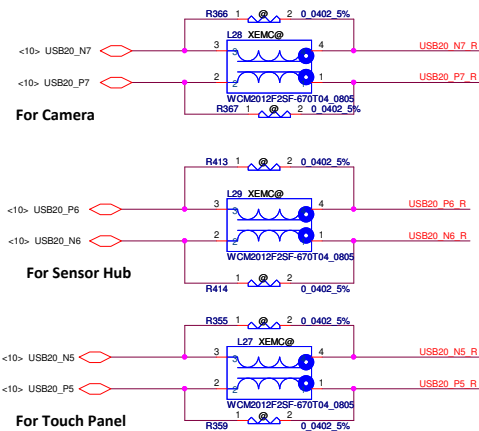
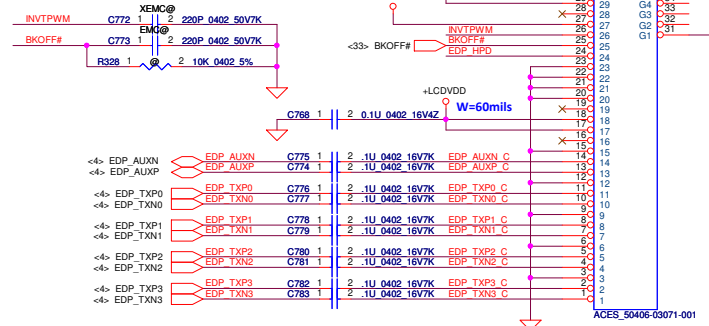
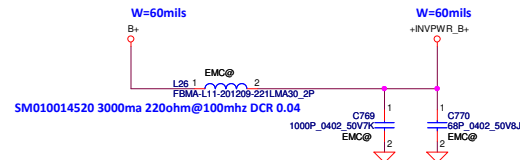


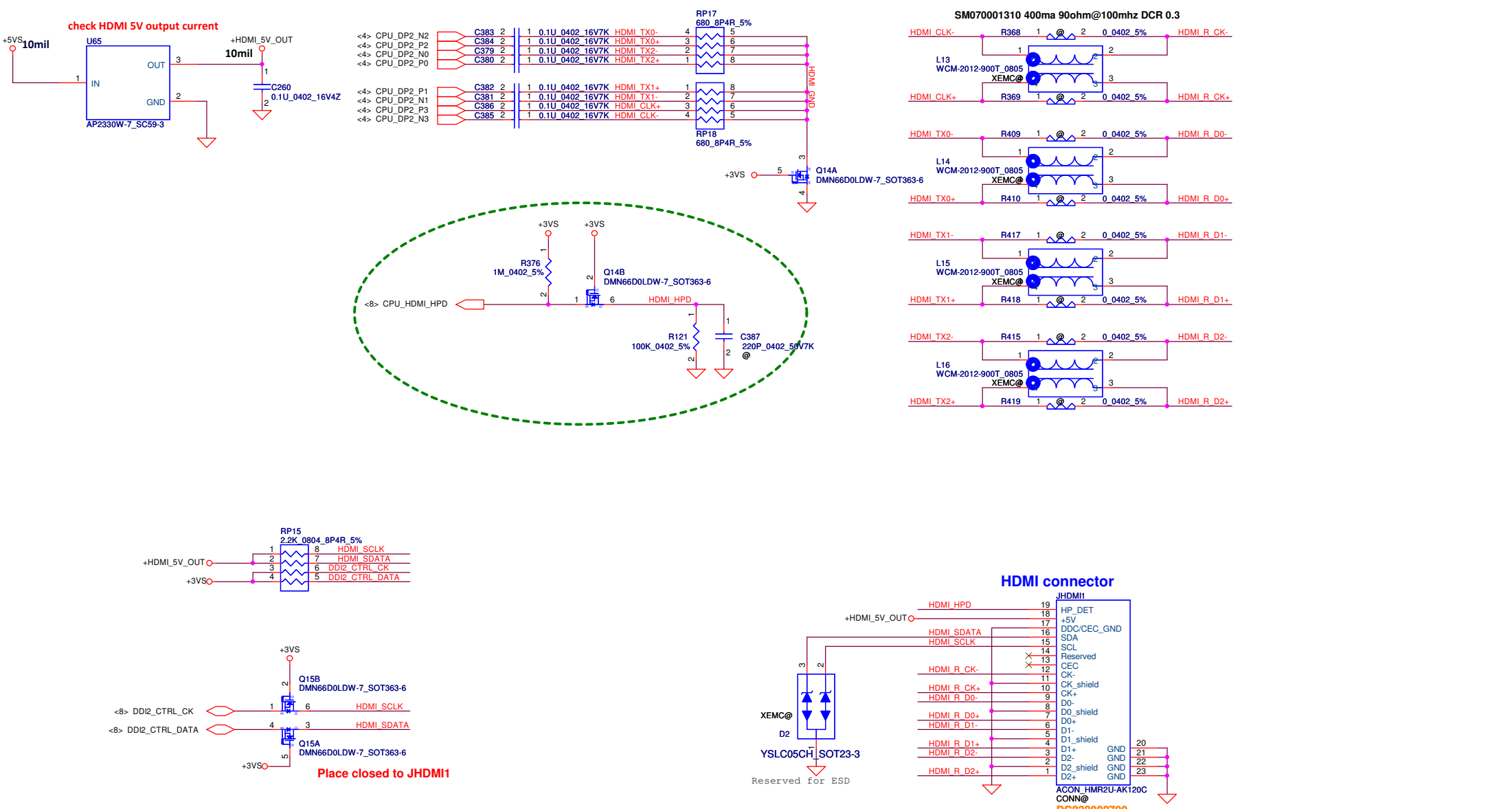
## BOT / M503



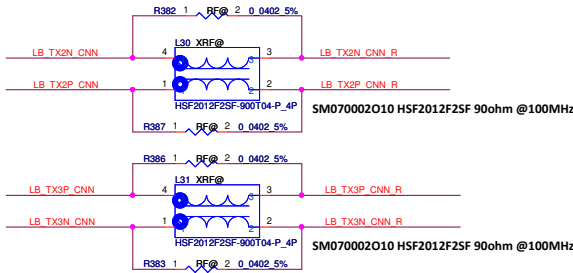
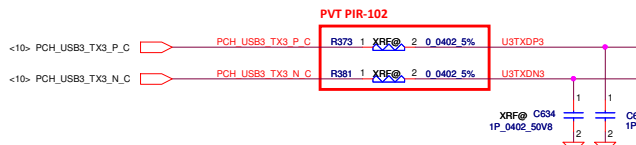
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The schematic shows an LCD driver IC U42 (G5243T11U\_S0T3-S) connected to a +3VS supply and an LCDVDD supply. The input IN is connected to +3VS through a C771 capacitor (4.7uF\_0603\_5%96K). The output OUT is connected to LCDVDD through a W=60mils trace. The GND pin is connected to ground. The EN pin is connected to ground through a C765 capacitor (4.7uF\_0603\_6.3%96K).

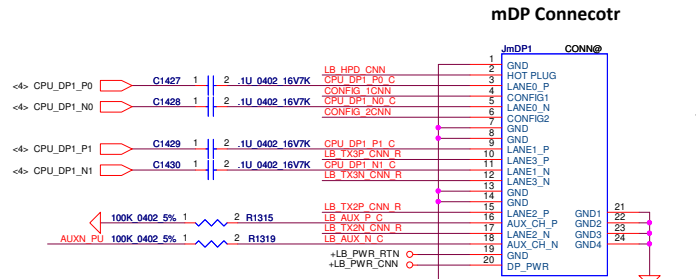




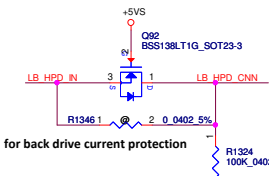
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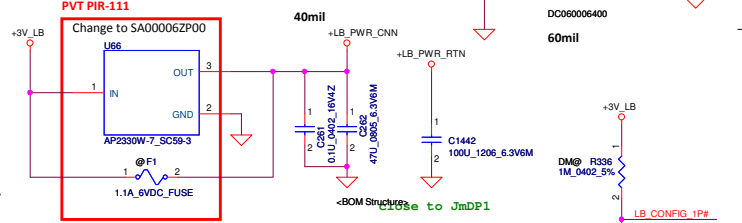
these RF solutions should be placed as close as possible JMDP1



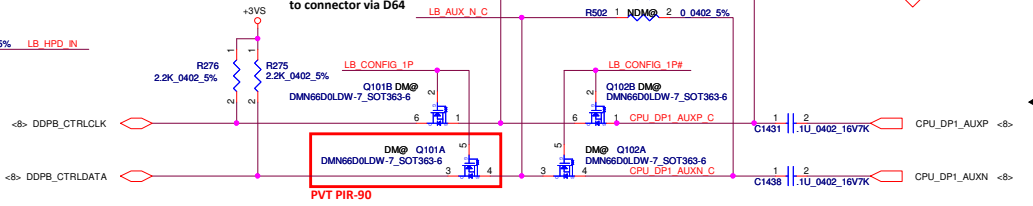
follow AE's comment, put the back drive current protection FET between IC and connector



for back drive current protection

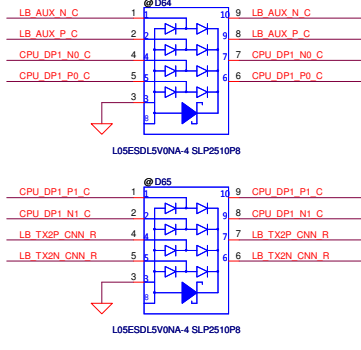


"DM+": supports Dual-Mode, such as HDMI



ESD Component

these ESD diodes should be put close to DP1



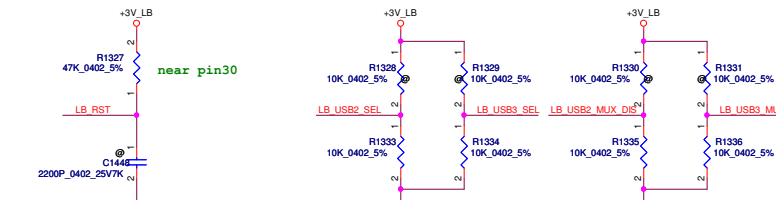
Control Signals and Miscellaneous

Pin Number	DP Mode	Lightning-Bolt Mode (2-Lane Mode)	Full DP Mode (4-Lane Mode)	Acer mDP DNGLE Mode
PIN1	GND	GND	GND	GND
PIN2	HPD	HPD	HPD	HPD
PIN3	DP_ML_0P	DP_ML_0P	DP_ML_0P	DP_ML_0P
PIN4	CONFIG1	USB20_P	CONFIG1	USB20_P
PIN5	DP_ML_0N	DP_ML_0N	DP_ML_0N	DP_ML_0N
PIN6	CONFIG2	USB20_N	CONFIG2	USB20_N
PIN7	GND	GND	GND	GND
PIN8	GND	GND	GND	GND
PIN9	DP_ML_1P	DP_ML_1P	DP_ML_1P	DP_ML_1P
PIN10	DP_ML_3P	USB30_TXP	DP_ML_3P	USB30_TXP
PIN11	DP_ML_1N	DP_ML_1N	DP_ML_1N	DP_ML_1N
PIN12	DP_ML_3N	USB30_TXN	DP_ML_3N	USB30_TXN
PIN13	GND	GND	GND	GND
PIN14	GND	GND	GND	GND
PIN15	DP_ML_2P	USB30_RXP	DP_ML_2P	USB30_RXP
PIN16	AUX_P	AUX_P	AUX_P	AUX_P
PIN17	DP_ML_2N	USB30_RXN	DP_ML_2N	USB30_RXN
PIN18	AUX_N	AUX_N	AUX_N	AUX_N
PIN19	DP_PWR_RTN	DP_PWR_RTN	DP_PWR_RTN	PWR 5V 1.5A
PIN20	PWR 3V 500mA			PWR 3V 500mA

no wake-up function supported requirement, un-stuff R324

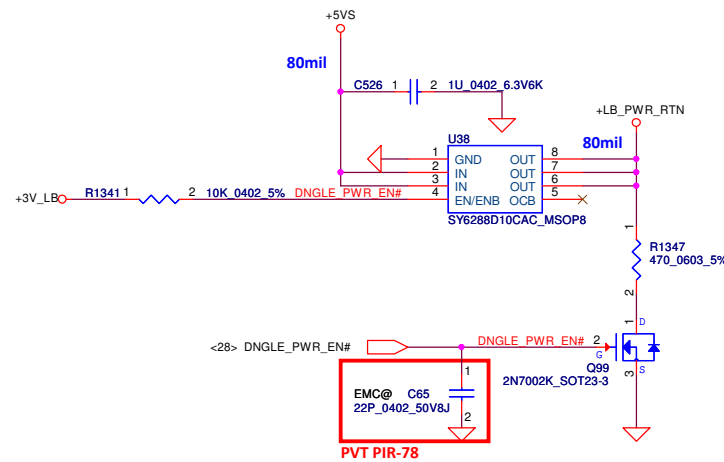
PIN22, CHRQ\_DELAY can be left NC for no battery charge mode supported.

RST: Pull up to 47K if this implementation not used  
RST/TEST: NC if this implementation not used



PVT PIR-63

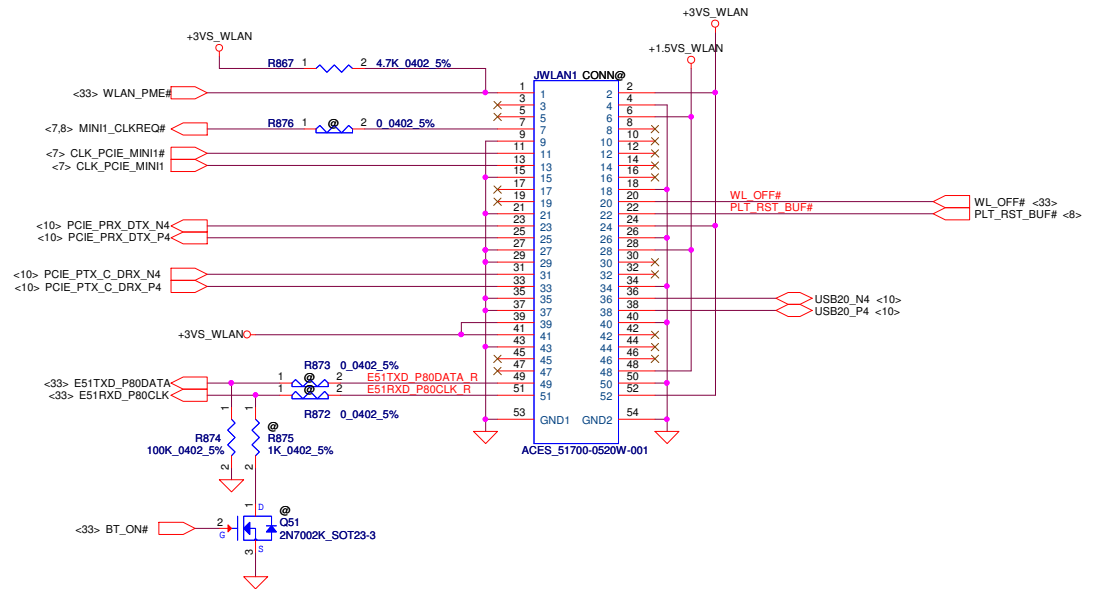
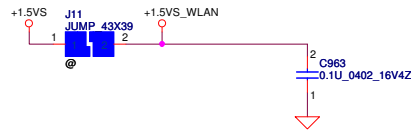
### mDP Power Control Circuit for 5V Power Supply



Preliminary Power Output for mDP		
DNGLE_PWR_EN#	LB_PWR_RTN	LB_PWR_CNN
1	GND	3.3V
0	5V	3.3V

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60mil

+3VS

JUMP\_43X118

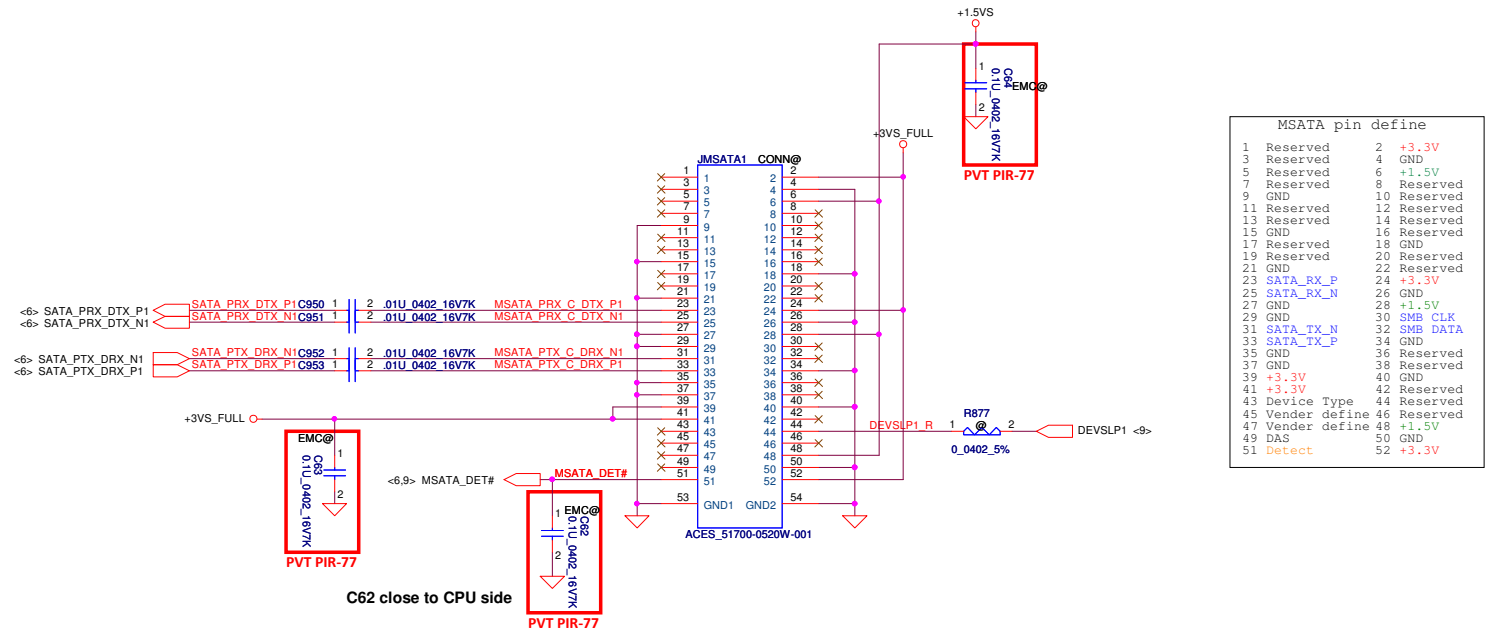
+3VS\_FULL

need check placement

C943 4.7U\_0603\_6.3V6K

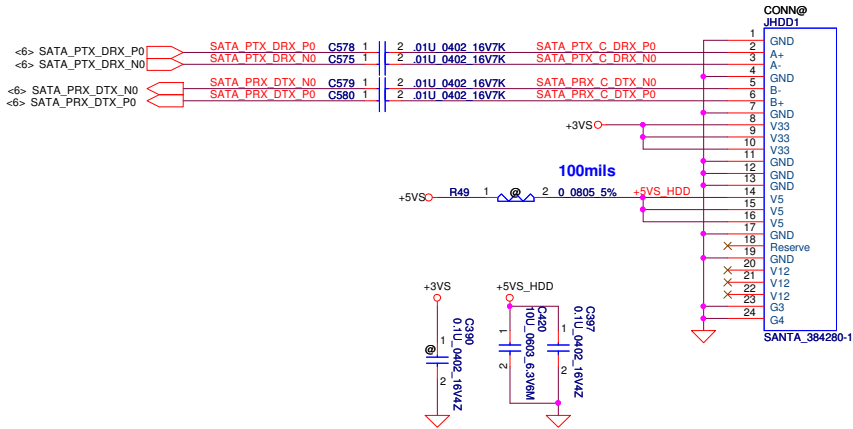
C944 0.1U\_0402\_16V4Z

C965 0.1U\_0402\_16V4Z

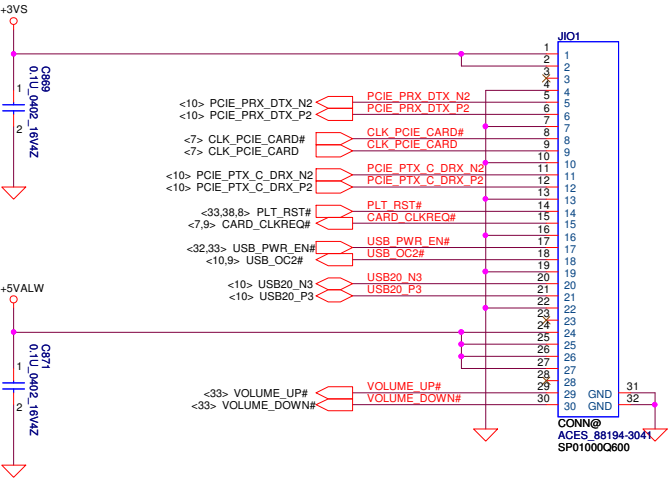


MSATA pin define			
1	Reserved	2	+3.3V
3	Reserved	4	GND
5	Reserved	6	+1.5V
7	Reserved	8	Reserved
9	GND	10	Reserved
11	Reserved	12	Reserved
13	Reserved	14	Reserved
15	GND	16	Reserved
17	Reserved	18	GND
19	Reserved	20	Reserved
21	GND	22	Reserved
23	SATA_RX_P	24	+3.3V
25	SATA_RX_N	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	SATA_TX_N	32	SMB_DATA
33	SATA_TX_P	34	GND
35	GND	36	Reserved
37	GND	38	Reserved
39	+3.3V	40	GND
41	+3.3V	42	Reserved
43	Device Type	44	Reserved
45	Vendor define	46	Reserved
47	Vendor define	48	+1.5V
49	DAS	50	GND
51	Detect	52	+3.3V

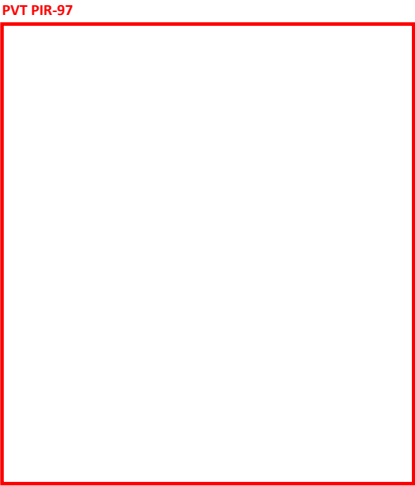
SATA HDD Connector(DIP Type)



IO/B Connector

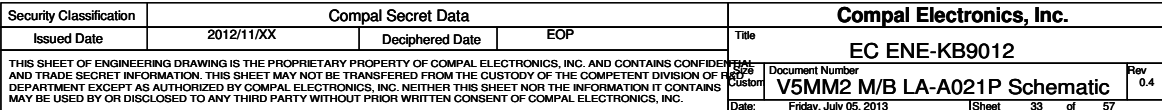


LAN/B Connector  
(Place near JPWR1)



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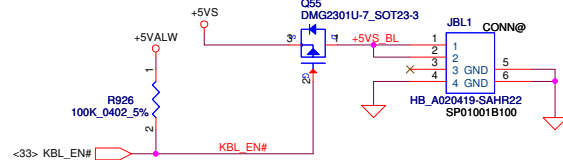
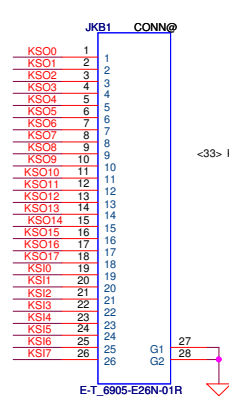
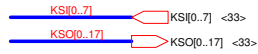


## KB Conn.

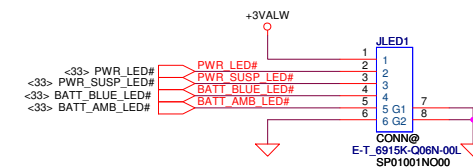
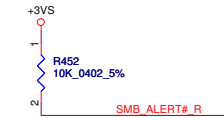
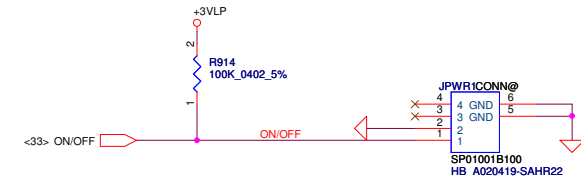
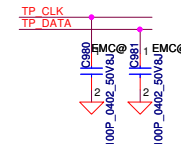
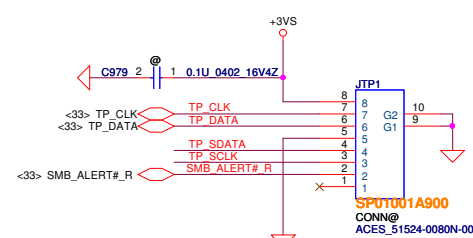
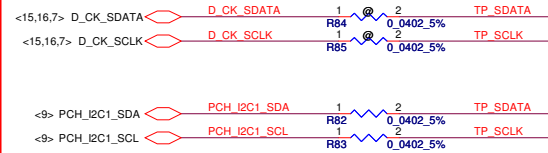
## KB backlight Conn.

## TP Conn.

## ON/OFF BTN

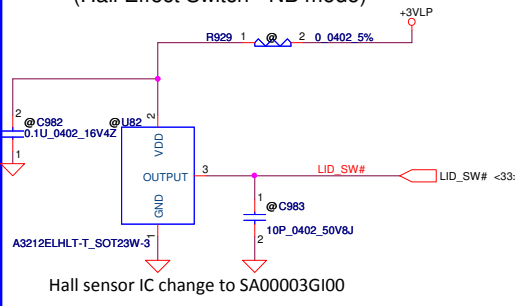
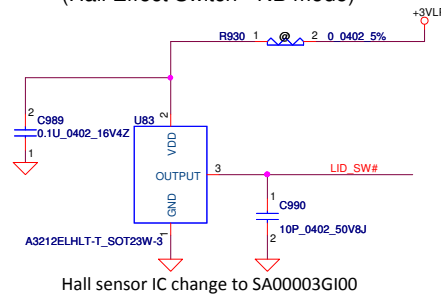


## PVT PIR-89

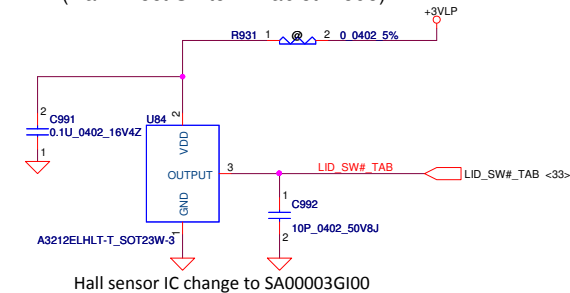


Lid Switch solution	
Solution-1	EVT, DVT, PVT-1
Solution-2	PVT-2

Lid switch power source need same as EC power

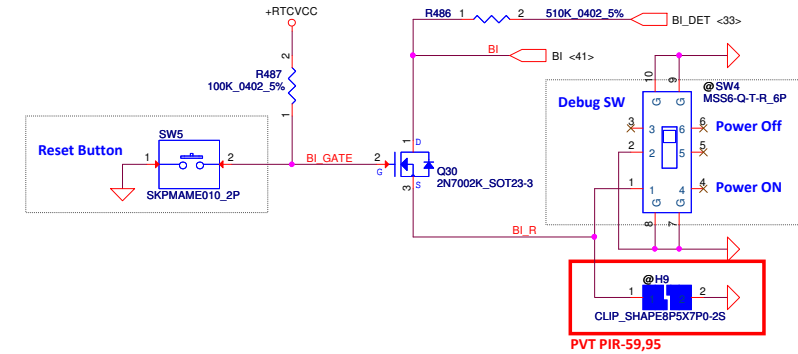
Lid Switch Solution-1  
(Hall Effect Switch - NB mode)Lid Switch Solution-2  
(Hall Effect Switch - NB mode)

## (Hall Effect Switch - Tablet mode)

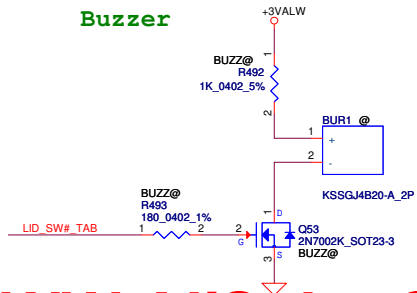


## Reset Button and Debug Switch for Polymer Battery

Debug switch will be removed after MP.

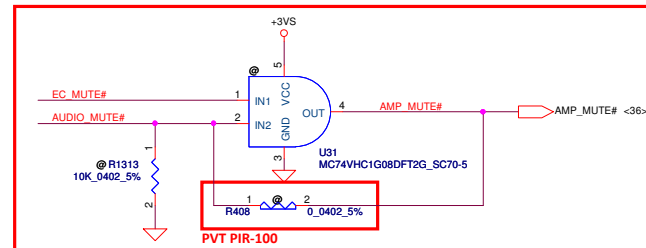
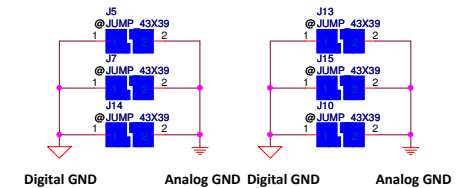


## Buzzer

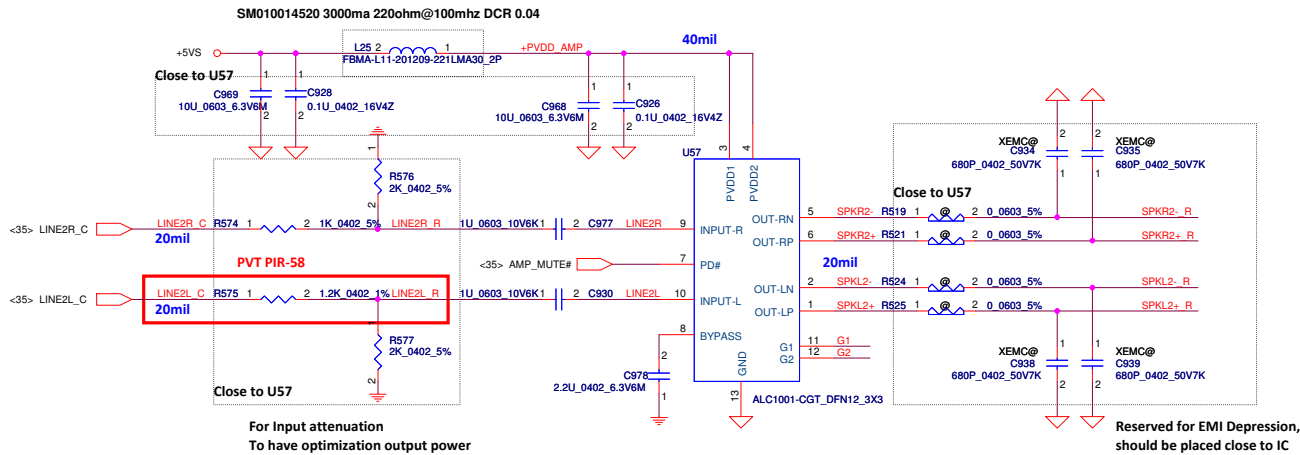


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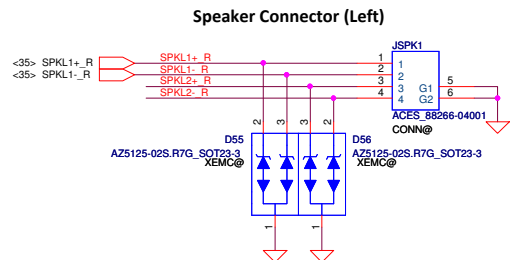
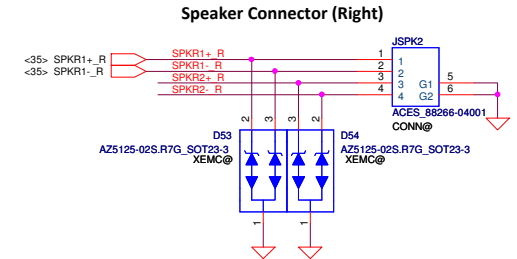
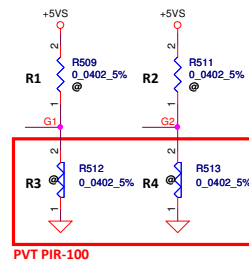
## PVT PIR-88



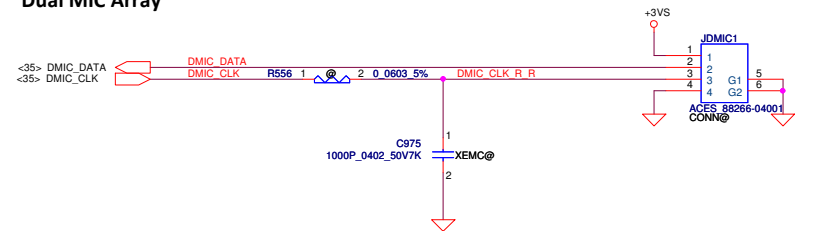
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>HD Audio Codec ALC3225X + ALC1001</b>	
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R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

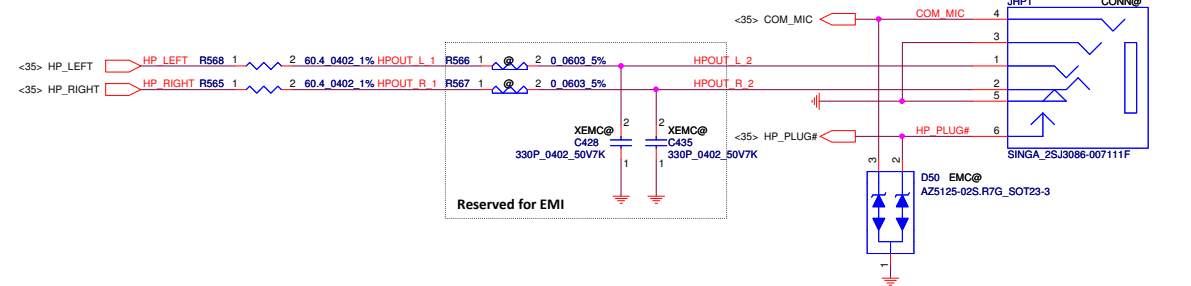


## Dual MIC Array



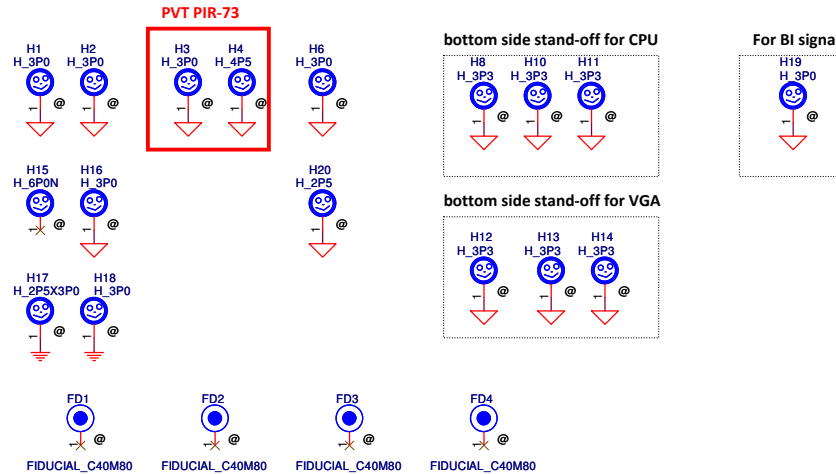
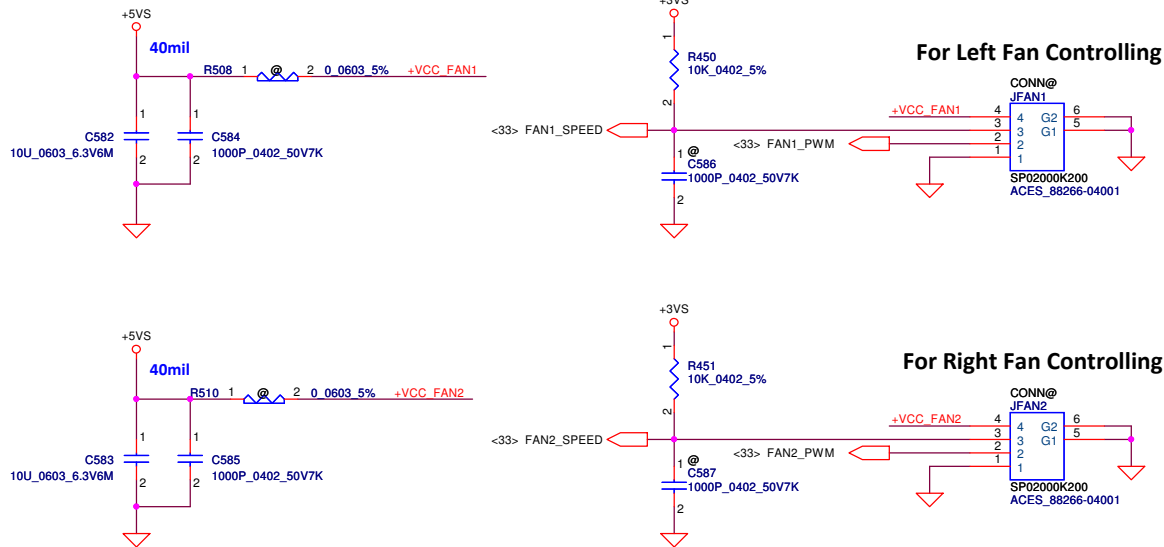
## Headphone Out/Mic Combo

JACK TYPE is the same as MA51



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								V5MM2 M/B LA-A021P Schematic			
								Rev			
								0.4			
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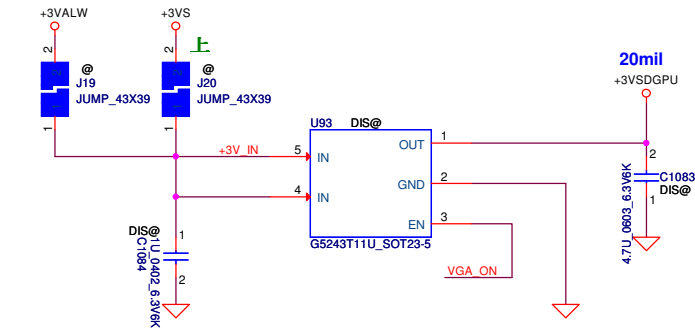




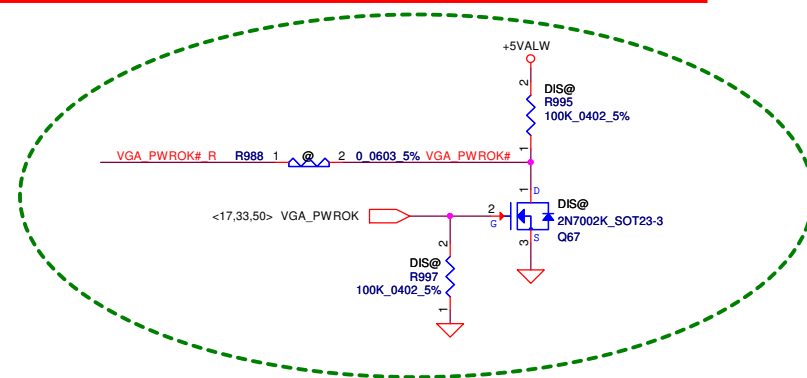
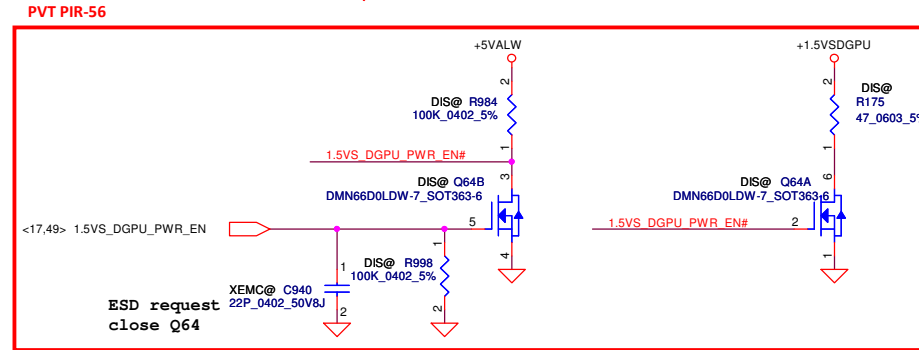
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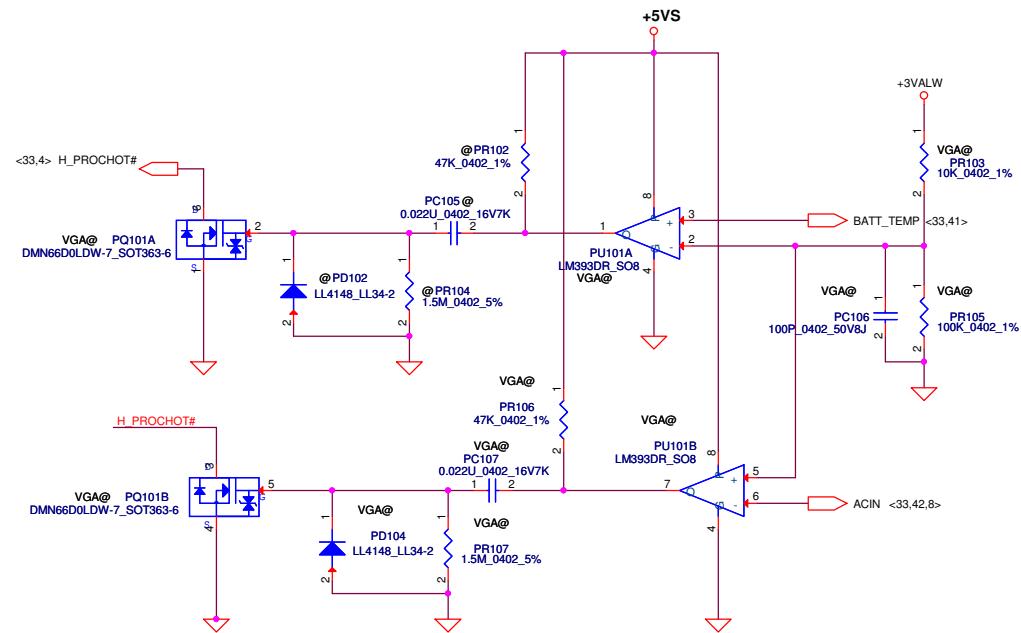
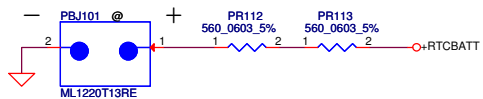
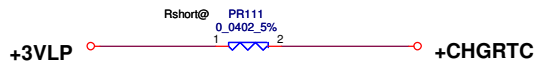
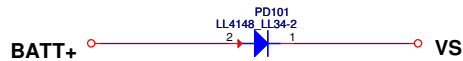
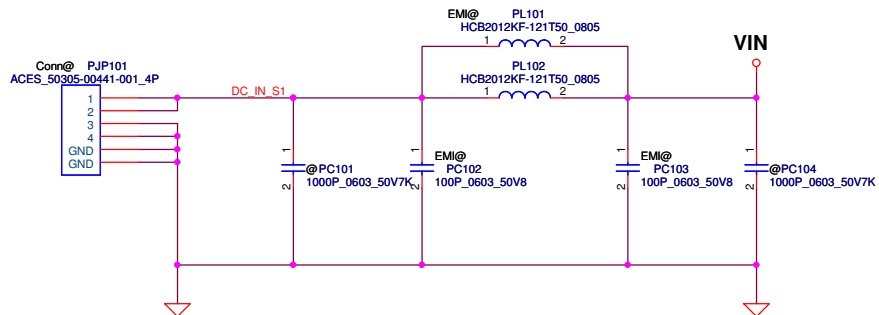
**+3V source to +3VSDGPU for GPU**



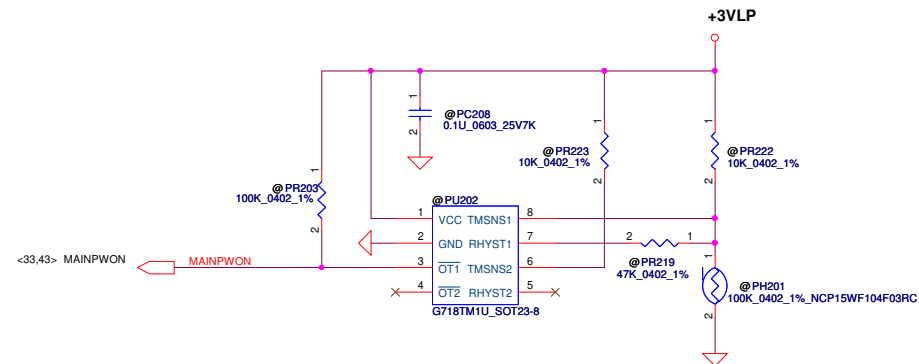
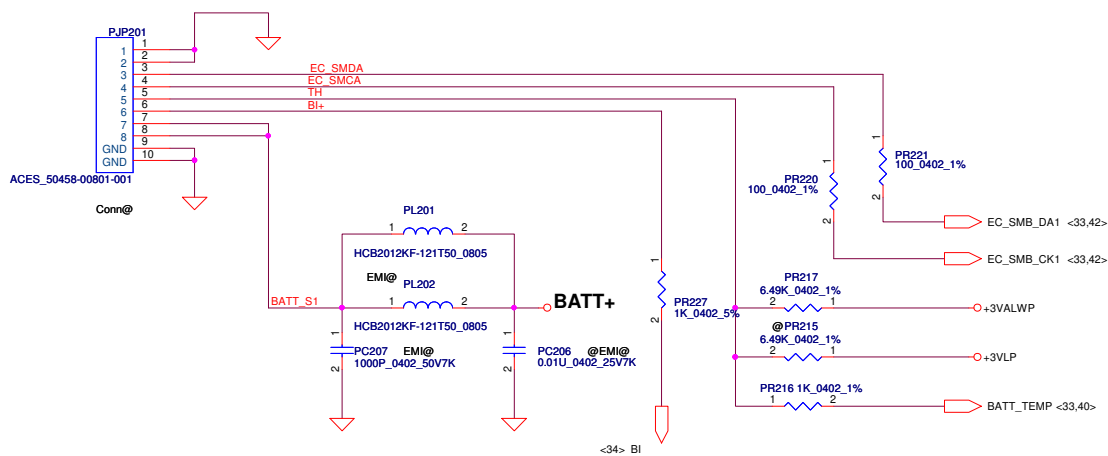
The schematic shows the internal circuitry of the VGA output driver. It includes two MOSFET drivers, Q52 and Q100B, which are part of the DMN66D0LDW-7\_SOT363-6 package. The input signal is +5VALW, which passes through a resistor R469 and a diode DIS@\_R514 to the gate of Q100B. The gate of Q100B is also connected to the gate of Q52 via a 47k resistor. The source of Q100B is connected to ground. The drain of Q100B is connected to the source of Q52. The gate of Q52 is connected to the +1.05VSDGPU\_GATE signal. The source of Q52 is connected to ground. The drain of Q52 is connected to the +1.05VSDGPU signal. The output of the driver is connected to the VGA\_PWROK# pin of the DMN66D0LDW-7\_SOT363-6 package.



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				Custom	0.4
				V5MM2 M/B LA-A021P Schematic	
Date:	Friday, July 05, 2013	Sheet	39	of	57



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				Date	Friday, July 05, 2013
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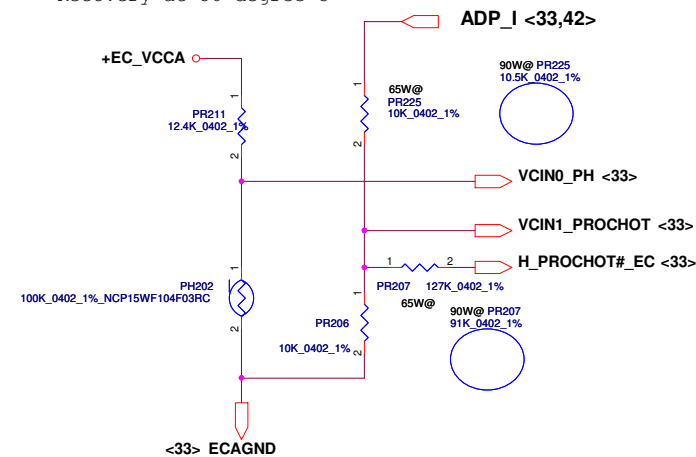


VCIN1 Recovery 85% chang to 100% \_2013/06/27

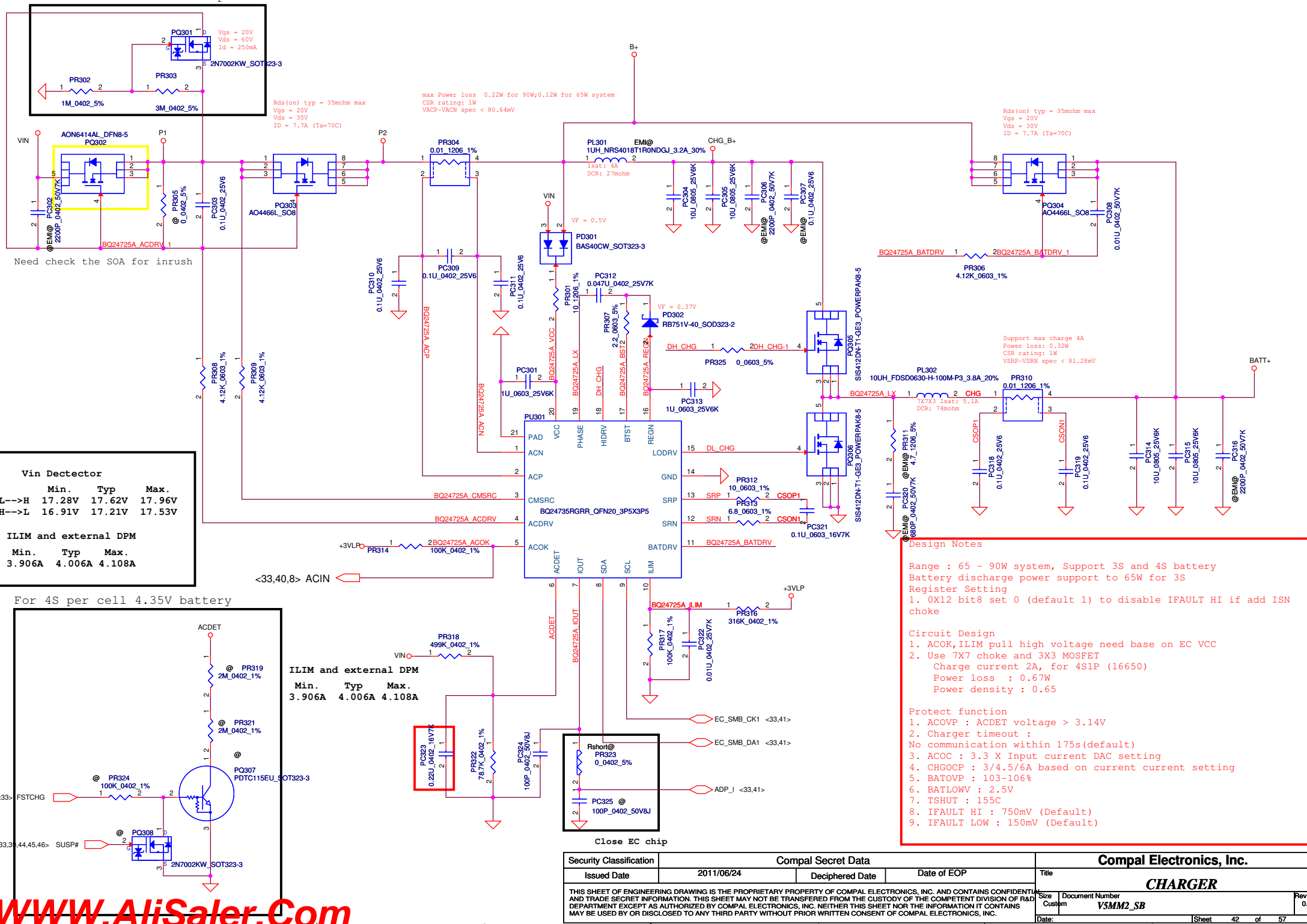
VCIN0	For KB9012 OTP
92°C	1.2V, Active
56°C	2.255V, Recovery

VCIN1 For KB9012 sense 10mΩ	Active	Recovery
65W	85W, 0.42V	65W, 0.42V
90W	117W, 0.56V	90W, 0.56V
120W		

PH202 under CPU bottom side :  
CPU thermal protection at 92 degree C ( shutdown )  
Recovery at 56 degree C



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								Size		Document Number		Rev	
								Custom		V5MM2_SB		0.	
Date:								Friday, July 05, 2013		Sheet		41 of 57	

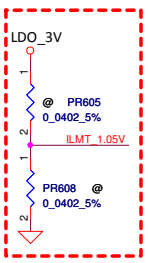
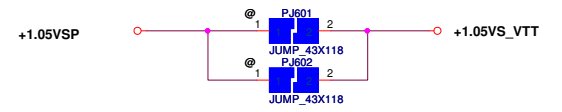




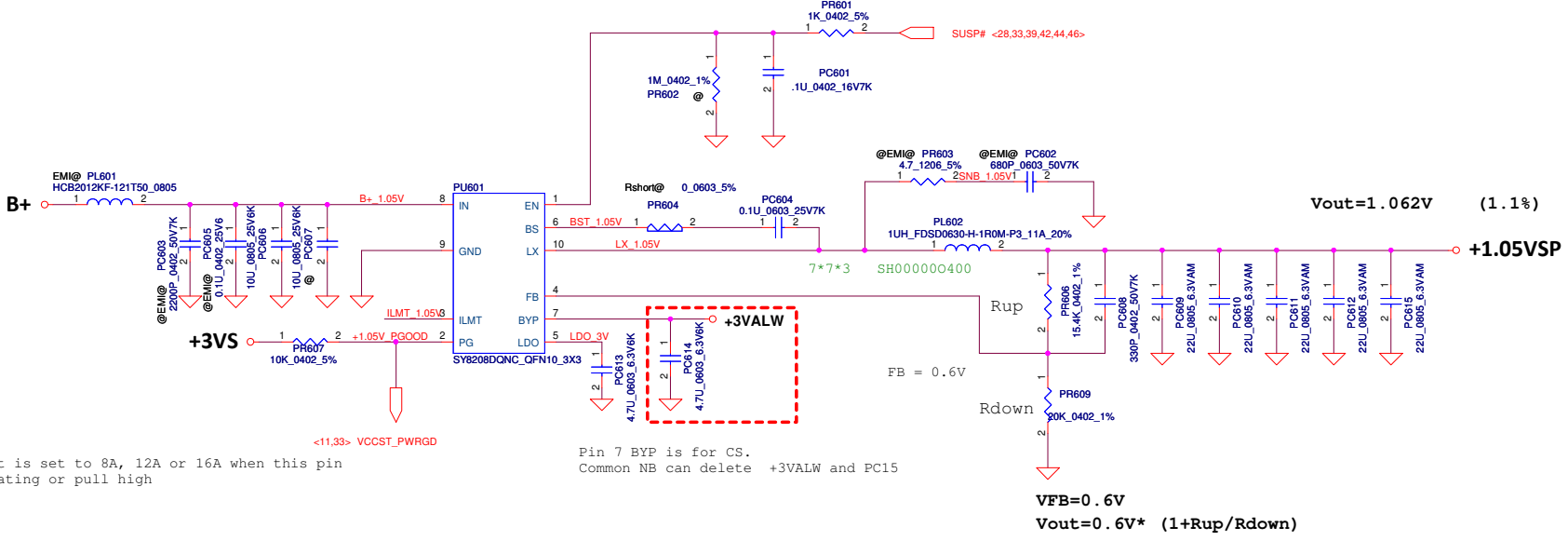




+1.05VSP Ipeak=8A ; I<sub>max</sub>=5.6A ; OCP=12A  
,F= 750K Hz (typ) (ILMT\_1.05V floating)  
2012/12/14

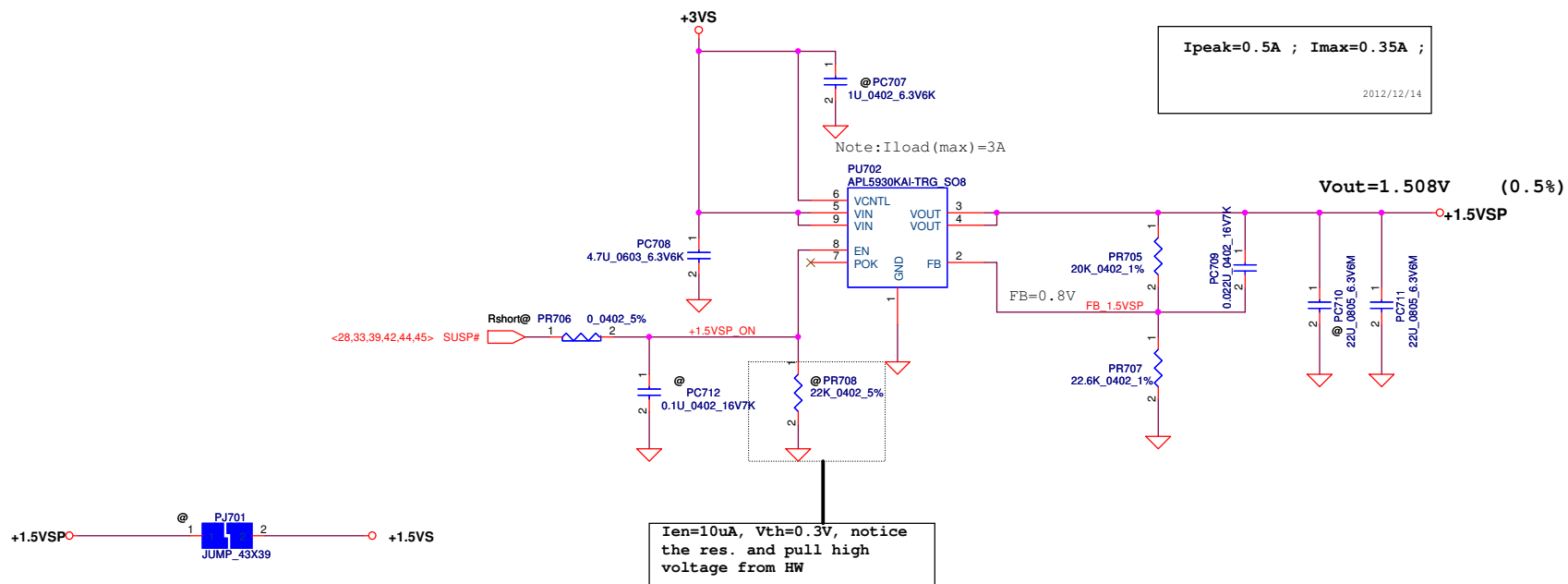


The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high



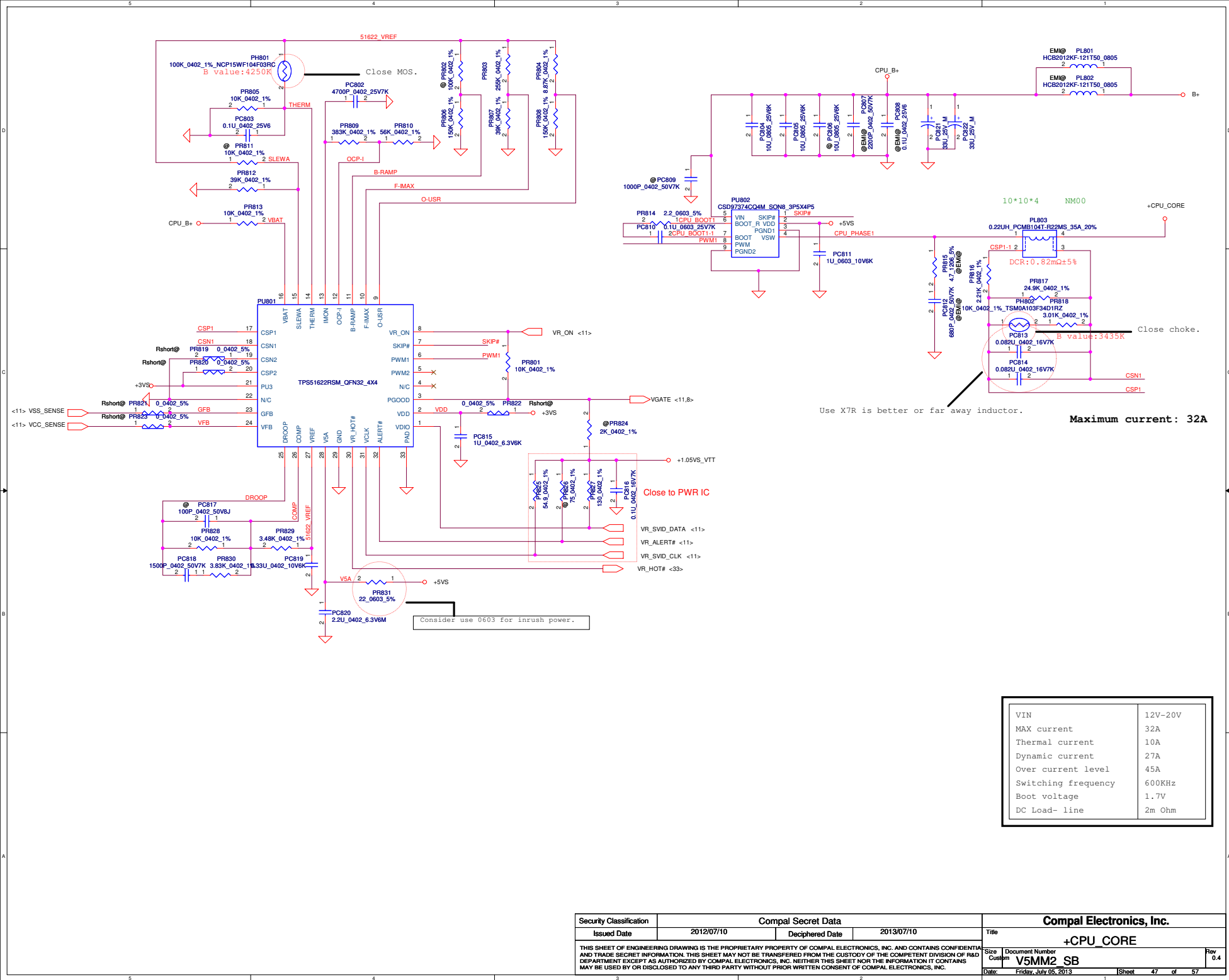
Pin 7 BYP is for CS.  
Common NB can delete +3VALW and PC15

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			V5MM2_SB	0.4
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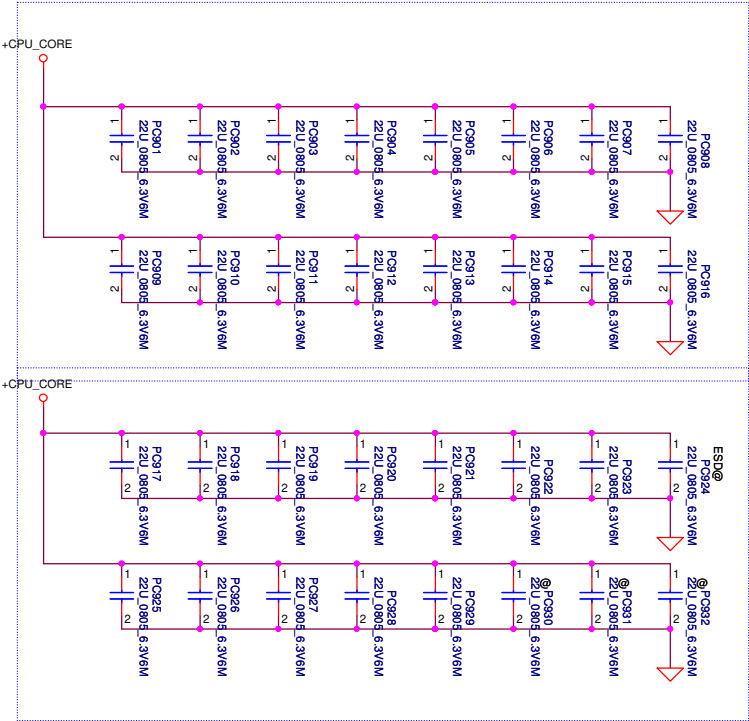
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2012/07/10		Deciphered Date		2013/07/10		Title			
								<b>+1.5VSP</b>			
Size		Document Number		Date		Friday, July 05, 2013		Sheet		46 of 57	
Custom										Rev 0.4	

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PWR Rule  
CPU DCLL=1.5m ohm dedign 330uF/9m \*0, 22uF \*30

22u \*28, @\*4



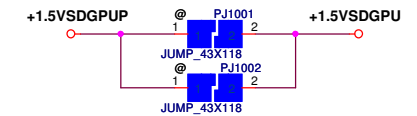
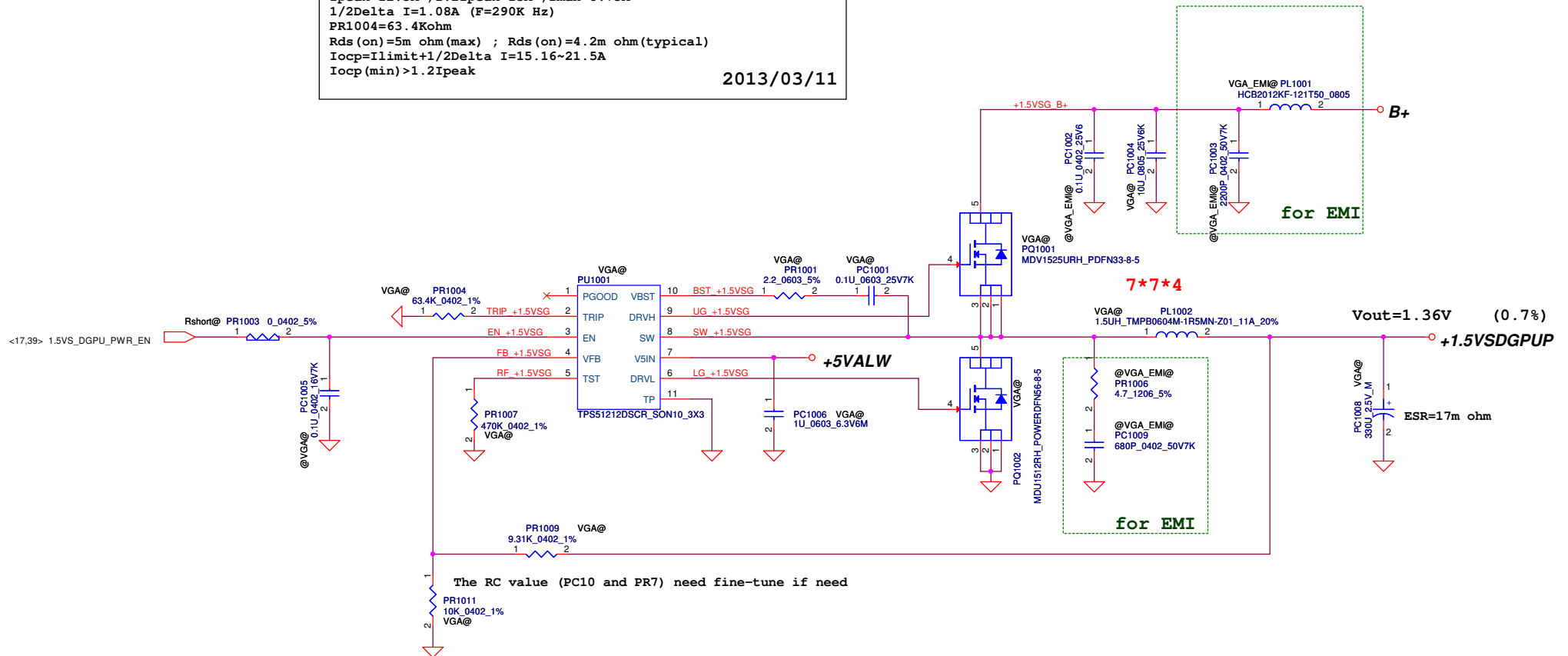
For BOT side

For TOP side

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Size		Document Number		Rev	
Customer		V5MM2_SB		0.4	
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```
+1.5VSDGPU
Ipeak=12.5A ; I2Ipeak=15A ; Imax=8.75A
1/2Delta I=1.08A (F=290K Hz)
PR1004=63.4Kohm
Rds(on)=5m ohm(max) ; Rds(on)=4.2m ohm(typical)
Iocp=Ilimit+1/2Delta I=15.16~21.5A
Iocp(min)>1.2Ipeak
```

2013/03/11

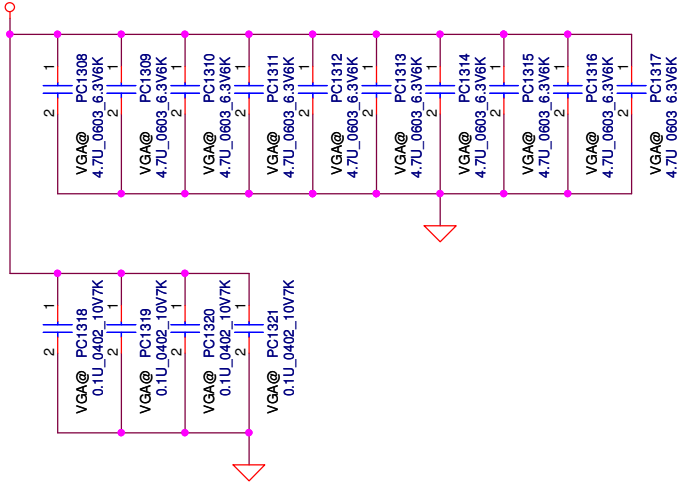


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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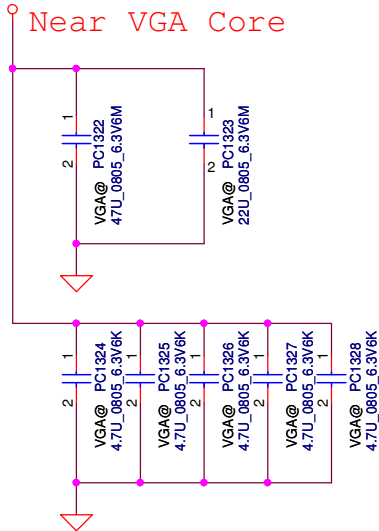


+VGA\_CORE Under VGA Core

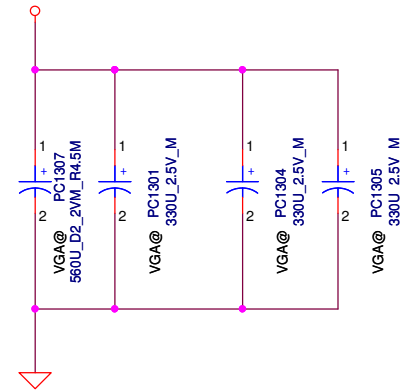


GB4-128  
Under  
4.7uF\_0603\_10pcs  
0.1uF\_0402\_4pcs  
Near  
47uF\_0805\_1pcs  
22uF\_0805\_1pcs  
4.7uF\_0805\_5pcs

+VGA\_CORE Near VGA Core



+VGA\_CORE



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Issued Date	2011/06/24	Deciphered Date	Date of EOP	Title VGA_CORE CAP		
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Acoustic noise	3V 5V light load efficiency improvement		3V/5V	1.Add 2pcs 1K_0402_5% (PR412 PR413) 1pcs 4700P_0402_25V7K (PC425) 1pcs 0.047U_0402_25V7K (PC426) 2.Add 4.7u_0402_6.3V6M (PC401)	01/15	EVT
2	Silergy update revision	3V 5V enable control for Rev0.3. But un-pop.		3V/5V	1.Add un-pop 2pcs 0402 resistors (PR415 PR414) 2.remove (PR207)	01/15	EVT
3		Reduce part count		VGA/CPU	Change to R-short (PR1211 PR1204 PR1206 PR1215 PR822 )	01/15	EVT
4		modify charger current to meet battery charge time.		Charger	0.02_1206_1%_SD00000S110 charger to 0.01_1206_1%_SD00000K820 (PR310)	01/15	EVT
5		The modify values for CPU transition test		CPU	1.PR803 270K_0402_1%_SD00000G280 change to 255K_0402_1%_SD034255380 2.PR809 392K_0402_1%_SD034392380 change to 383K_0402_1%_SD034383380 3.PR831 10_0603_5%_SD013100A80 change to 22_0603_5%_SD000001R80 4.PC820 1U_0603_10V6K_SE080105K80 change to 2.2U_0402_6.3V6M_SE000008880	01/15	EVT
6		BI_GATE remove		3V/5V	PQ401 2N7002KW_SOT323-3_SB000009Q80 remove.	01/16	EVT
7		HW VGA_sequence test		VGA	1.PC1201un-pop charger to 0.1U_0402_16V7K_SE076104K80 2.PR1201un-pop charger to 24.9K_0402_1%_SD034249280 3.PR12280_0402_5% charger to un-pop	01/21	EVT
8		When pwm IC shutdown on S0, EC could detect SLP_S5#, but cannot detect PCH was no power.		3V/5V	PR416 add 100K_0402_5%_SD028100380	3/11	DVT
9		The 5VALW will fast than 3VALW and the rising time will under 2mS.		3V/5V	PC426 4700P_0402_25V7K_SE075472K80 change to 0.01U_0402_25V7K_SE075103K80 PC425 0.047U_0402_25V7K_SE00000MJ00 change to 6800P_0402_25V7K_SE075682K80	3/11	DVT
10		VRAM efficiency improvement		1.5VDGPU	1.PQ1002 AON7702A_SB00000T600 change to MDU1512RH_POWERDFN56-8-5_SB00000SY00 2.PQ1001 AON7408L 1N DFN_SB00000H800 change to MDV1525URH 1N PDFN33-8_SB00000S600 3. PL1002 2.2uH_7*7*3_SH00000MR00 charger to 1.5uH_7*7*4_SH00000PM00	3/11	DVT
11		The discharge time may cause GC6 entry/exit quickly fail, worry about the off time too long problem cause the GC6 fail.		VGA	PR1229 add un-pop 22_0805_5%_SD002220A80 PQ1207 add un-pop 2N7002KW_SOT323-3_SB000009Q80	3/11	DVT

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## Version change list (P.I.R. List)

Page 1 of 2  
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		remove VGA enable for +3VSDGPU		VGA_COREP	remove PR1228_0_0402_5%	3/11	DVT
2		VRAM voltage change to 1.35V.		+1.5VSDGPUP	PR1009 11.5K_0402_1%_SD034115280 change to 9.31K_0402_1%_SD034931180 PR1004 137K_0402_1%_SD034137380 change to 63.4K_0402_1%_SD03463K280	3/11	DVT
3		ESD request		CPU capacitor	Add PC924 22U_0805_6.3V6M_SE000000I10	3/11	DVT
4		VCIN1 function		BATTERY CONN/OTP	PR225 5.1K_0402_1%_SD034510180 change to 9.76K_0402_1%_SD034976180_90W@ 1.02K_0402_1%_SD034102180 change to 9.76K_0402_1%_SD034976180_65W@ PR207 UN-pop-0K_0402_1%_SD034100280 change to 47.5K_0402_1%_SD034475280_90W@ UN-pop-0K_0402_1%_SD034100280 change to 71.5K_0402_1%_SD034715280_65W@		
5				CHARGER	PR318 499K_0402_0.1%_SD000000U380 change to 499K_0402_1%_SD034499380	3/11	DVT
6		Material change		CPU_CORE 1.05V	PH801 SL200000U00 change to SL200000V00 PL602 SH00000PJ00 change to SH00000O400	4/16	PVT-1
7		The discharge time may cause GC6 entry/exit quickly fail, worry about the off time too long problem cause the GC6 fail.		VGA	Add PR1229 22_0805_5%_SD002220A80 Add PQ1207 2N7002KW_SOT323-3_SB000009Q80	5/14	PVT-1
8		Reduce part count		1.35V/1.5VSP /1.5VSDGPU	SD028000080 Change to 0402_R-short (PR510 PR706 PR1003)	5/14	PVT-1
9		Reduce part count		3V/5V/ 1.05V/VGA	SD013000080 Change to 0603 R-short (PR405 PR408 PR604 PR1202 PR1222)	5/14	PVT-1
10		follow ON solution for VGA		VGA	1. PC1221_SE074272K00_2700P charger to un-pop. 2. PC1208_SE071101J80_100P charger to SE074272K00_2700P		PVT-1
11		Adjust the FB voltage for 1.35V		1.35V	PR506 8.2K_0402_1%_SD000004100 charger to 8.06K_SD034806180.		PVT-1
12		Material EOL		1.35V	PQ502 AON7702A SB00000T600 change to AON7506 SB000010A00		PVT-2
13		VCIN1 Recovery 85% chang to 100%		3V/5V BATTERY CONN /OTP	PR411 316K_0402_1%_SD034316380 change to 953K_0402_1%_SD000000X100 PR403 402K_0402_1%_SD034402380 change to 160K_0402_1%_SD034160380 PR225 9.76K_0402_1%_SD034976180 change to 10K_0402_1%_SD034100280 (65W@) change to 10.5K_0402_1%_SD034105280 (90W@) PR207 71.5K_0402_1%_SD034715280 change to 127K_0402_1%_SD034127380 (65W@) change to 91K_0402_1%_SD034910280 (90W@)		PVT-2

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				PIR (PWR)		
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Item	Page#	Date	Issue Description	Solution Description	Stage
1	28	2013/1/8	Add DP++ Schematic	Add Q101,Q102,Q46,R336 , reserve R499,R502	DVT
2	28	2013/1/8	Add DP++ config	Add DM@ , NDM@	DVT
3	28	2013/1/8	Change mDP HPD Schematic from Before-IC to After-IC		DVT
4	28	2013/1/8	for LB_RST no use	pop R1327 for LB_RST no use	DVT
5	28	2013/1/8	LB HPD issue	Change R1344 from 100K to 10K	DVT
6	28	2013/1/8	for not support LB wake function	Add R503 and unpop it	DVT
7	28	2013/1/8	for not support LB wake function	Add J24	DVT
8	31,34	2013/1/8	Remove LAN/B from Acer request	Remove JLAN1 , Add JPWR1 (same as JBL1)	DVT
9	31,33	2013/1/8	Remove LAN/B from Acer request	1. LAN_CLKREQ# pull-high to +3VS (R131,後面remove) 2. Remove C530,R312,R1170 3. reserve R234,R236,R237 for differential pair route space	DVT
10	31	2013/1/8	EC Board ID for Rev0.2	Change R1191 to 8.2K pop R1190,R1191	DVT
11	7	2013/1/8	Change SPI ROM from 4M+2M to 8M	Remove U14,RP20,R109,R402,C67,C453	DVT
12	26	2013/1/8	1.abnormal display via re-driver board 2. to solve the problem without any gauge increased	1. Connect JEDP1_pin27 to +3VS, this solution is only for cable which need to pass via re-driver board 2. Add R522,C140 , unpop R421,R424 3. Change Q43 to 2N7002K	DVT
13	8	2013/1/8	incorrect gpio define	unpop R214 ,pop R205	DVT
14	28	2013/1/8	For LightningBolt debug , will unpop in PVT	pop SW7 (後面remove)	DVT
15	38	2013/1/8	Change TPM IC P/N	Change U89 from SA00005XH00 to SA00005XH40	DVT
16	26,32	2013/1/8	For EMI request , change EMI part P/N	Change L26 to SM01000EJ00 Change L17,L18,L20,L21,L22 to SM070001R00	DVT
17	30	2013/1/9	some risk for OPs on factory side	Change JMINI1 and JMINI2 to JWLAN1 and JMSATA1	DVT
18	34	2013/1/9	Pull-high 10K to +3VS for SMB_ALERT#_R	Add R452	DVT
19	34	2013/1/9	Update KB backlight schematic	Remove Q56,R928	DVT
20	34	2013/1/9	Battery can't detect issue (BI_GATE)	Add R530 , unpop Q30	DVT
21	33	2013/1/9	GC6 schematic update	connect VGA_PWROK to EC_pin120	DVT
22	7	2013/1/9	Change SPI serial resistor value	Change RP19,R108 from 22ohm to 15ohm	DVT
23	37	2013/1/9	For BI signal screw hole	Add H19	DVT
24	7	2013/1/9	Change SPI ROM from dual to single	Remove U14,RP20,R109,R402,C67,C453 (多寫)	DVT
25	7	2013/1/14	LAN_CLKREQ# already pull-up on CPU side	Remove R313 (已有R52 pull-up)	DVT
26	8	2013/1/15	For Cost/Part count	Remove R66 unpop R67,U30 Change R403 from 0ohm to 2ohm	DVT
27	28	2013/1/15	For Cost/Part count	Remove SW7,C1443 unpop D64,D65,D66	DVT
28	33	2013/1/15	For Cost/Part count	Remove R1160	DVT
29	34	2013/1/15	For Cost/Part count	Remove R930,SW1	DVT
30	34	2013/1/15	Update BI_GATE schematic	Remove D43,Q34,R489,R530,C888,C890 Q30 change from P-MOS to N-MOS R486,R487 change to 100K ohm	DVT
31	39	2013/1/15	For Cost/Part count	Change R987 to 2ohm	DVT
32	7	2013/1/15	For Cost/Part count	Change R111 to R-short 0402	DVT
33	27	2013/1/15	For Cost/Part count	Change R368,R369,R409,R410,R417,R418,R415,R419 to R-short 0402	DVT
34	30	2013/1/15	For Cost/Part count	Change R876,R877 to R-short 0402	DVT
35	31	2013/1/15	For Cost/Part count	Change R49 to R-short 0805	DVT

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36	33	2013/1/15	For Cost/Part count	Change R1162 to R-short 0805	DVT
37	34	2013/1/15	For Cost/Part count	Change R929 to R-short 0402	DVT
38	35	2013/1/15	For Cost/Part count	Change R495,R496,R497 to R-short 0603	DVT
39	37	2013/1/15	For Cost/Part count	Change R508,R510 to R-short 0603	DVT
40	39	2013/1/15	For Cost/Part count	Change R988 to R-short 0402	DVT
41	26	2013/1/16	For ESD request	Add C803	DVT
42	34	2013/1/16	Update BI_GATE schematic	Change R486 to 510K , BI_GATE power change to +RTCVCC	DVT
43	8	2013/1/17	For ESD request	Add C932,C936,C937	DVT
44	11	2013/1/17	For ESD request	Add C920,C925	DVT
43	39	2013/1/17	For ESD request	Add C940	DVT
44	6	2013/1/21	Change main source on DVT only	Y1 change to SJ100004Z00	DVT
45	32	2013/1/21	Change main source on DVT only	U76,U78 change to SA00003TV00	DVT
46	29	2013/1/21	Change main source for AP-code	Q95,Q96 change to SB966750010	DVT
47	8,39	2013/1/21	Update GC6 schematic	Pop R404,R405 unpop R406,R407 R469 change from 330k to 47k	DVT
48	29	2013/1/21	Update LB schematic	R1347 change from 100k to 100 ohm	DVT
49	34	2013/1/21	unpop debug switch	unpop SW4	DVT
50	40-53	2013/1/22	update Power schematic 0121A		DVT
51	34	2013/1/22	For X1 code	Change U82 from SA00001TC00 to SA000057Z00	DVT
52	26	2013/1/22	For SMT 統一料	Change L26 back to SM010014520	DVT
53	26	2013/1/23	eDP HPD issue	Pop R421,R424 ; unpop R522 , C140	DVT
54	26	2013/2/7	eDP HPD issue	Remove Q43	PVT
55	20	2013/2/7	VGA schematic mistake	Change R1245 from 42.2ohm to 40.2ohm	PVT
56	39	2013/2/19	Change EN pin for +1.5VSDGPU off-current	Q64 change to Dual-N and gate pin change to 1.5VS_DGPU_PWR_EN , add R984,R998	PVT
57	33	2013/2/19	Add SPOK to turn on/off +3,5VALW	Add EC pin_16 named SPOK	PVT
58	36	2013/2/19	Audio SPK sound not balance issue	Change R575 from 1k ohm to 1.2k ohm	PVT
59	34	2013/2/19	BI_GATE issue	Change H9 symbol	PVT
60	32	2013/2/19	Add RF frame	Add CLIP1	PVT
61	26	2013/2/19	ESD issue	C803 change from 0.1u to 22p	PVT
62	33	2013/2/19	Board ID for Rev 0.3 PCB	R1191 change from 8.2k to 18k	PVT
63	29	2013/2/19	Change LBT 5V switch schematic	Add U38(USB power switch), C526 Remove Q95,Q96,Q97,U156,R1337,R1338,R1343,R1339.R1340 Change R1347 from 100_0402 to 470_0603 for discharge Change R1341 from 100k to 10k (follow CR)	PVT
64	26,33	2013/2/19	No need support wake by Home-Key	Change power to home key from +3VALW to +3VS (JSNSR1.pin12) Change Pull-up domain from +3VALW to +3VS (R1181,R1182,R1183)	PVT
65	9	2013/2/19	Add GPIO pin for TPM/no-TPM sku	Add R312,R313 and unpop R312	PVT
66	30	2013/2/27	AOAC on/AOAC off co-lay	Add J21 from +3VS unpop U79,C941	
67	20	2013/2/27	VGA part count and unpop reduce	Remove C1316,C1317	
68	22	2013/2/27	VGA part count and unpop reduce	Remove C1341,C1342,C1327 unpop C1345,C1346,C1348,C1350,C1329,C1331,C1334,C1336	
69	23	2013/2/27	VGA part count and unpop reduce	Remove C1366,C1367,C1355 unpop C1369,C1371,C1372,C1374,C1357,C1358,C1362,C1363	
70	24	2013/2/27	VGA part count and unpop reduce	Remove C1392,C1393,C1378 unpop C1394,C1397,C1399,C1401,C1380,C1382,C1385,C1387	
71	25	2013/2/27	VGA part count and unpop reduce	Remove C1417,C1418,C1404 unpop C1421,C1422,C1423,C1426,C1405,C1407,C1413,C1415	
72	26	2013/2/27	For Cost/Part count	R424 change to R-short 0402 Remove R522,C140	

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73	37	2013/3/4	ME screw change	H4 change from 3P0 to 4P5 , H3 from 2P5 to 3P0	PVT
74	32	2013/3/5	USB charger schematic update	R853 pull-up power rail change from +3VALW to +3VALW_EC	
75	31	2013/3/5	Remove JHDD2	Remove JHDD2	
76	11,15,33	2013/3/5	For ESD request	pop C6,C117,C1255 (Page11,Page15,Page33)	
77	30	2013/3/5	For ESD request	Add C62,C63,C64	
78	29	2013/3/5	For ESD request	Add C65	
79	11	2013/3/6	For Cost/Part count	Change R167,R168 to R-short 0402	
80	26	2013/3/6	For Cost/Part count	Change R355,R359,R366,R367,R413,R414,R335 to R-short 0402	
81	32	2013/3/6	For Cost/Part count	Change R852,R855,R865,R866 to R-short 0402	
82	33	2013/3/6	For Cost/Part count	Change R80 to R-short 0402	
83	38	2013/3/6	For Cost/Part count	Change R978,R980 to R-short 0402	
84	20	2013/3/6	For Cost/Part count	Change R1241 to R-short 0603	
85	35	2013/3/6	For Cost/Part count	Change R518,R520,R527,R529 to R-short 0603	
86	36	2013/3/6	For Cost/Part count	Change R519,R521,R524,R525,R556,R566,R567 to R-short 0603	
87	17	2013/3/6	Update GC6 schematic	Add D3,Q95 Remove Q84,,Q90,R1204 Change R1201 from 10k to 1k Reserve R1205	
88	35,36	2013/3/6	Audio PoPo issue	Add U31,R1313 and un-pop Add R408 Amp PD pin change from EC_MUSE# to AMP_MUTE#	
89	9,34	2013/3/6	Add I2C for touchpad	Add R84,R85 and unpop Add R82,R83,R1337,R1338	
90	28	2013/3/8	Update LBT schematic (TI request)	Swap Q101A pin3 and pin4	
91	19	2013/3/8	Change VRAM power from 1.5V to 1.35V	Change R1229 from 24.9k to 34.8k	
92	ALL	2013/3/11	Combine power schematic 0311A	Combine power schematic 0311A	
93	38	2013/3/13	Change TPM power from +3VALW to +3VS	pop J17 , unpop J16	
94	28	2013/4/1	Add F1 for LBT fuse	Add F1	PVT2
95	34	2013/4/1	Update H9 symbol	Update H9 footprint	
96	ALL	2013/4/1	Update All RC*NEW footprint		
97	7,10,31	2013/5/9	Remove LAN	Remove C168,C169,R234,R,236,R237	
98	34	2013/5/9	Reserve one/two Lid-switch funtion	Add U83,U84,R930.R931,C989,C990,C991,C992	
99	6,11	2013/5/9	For Cost/Part count	Change R76,R180 to R-short 0402	
100	35,36	2013/5/9	For Cost/Part count	Change R408,R512,R513 to R-short 0402	
101	6,10	2013/5/9	For Cost/Part count	Change R75,R155 to R-short 0603	
102	28	2013/5/9	For Cost/Part count	Change R373,R381 to R-short 0402	
103	9	2013/5/10	Add net for 2nd hall sensor Lid-out	Change PCH GPIO14 for EC LID_OUT TAB (LID_OUT need place between GPIO1 to GPIO15)	
104	7,9	2013/5/10	Change Card-Reader CLK from Port5 to Port1	modify net name : GPIO19 -> CARD_CLKREQ# CARD_CLKREQ# -> GPIO23	
105	33	2013/5/16	Add Pull-up for LID_SW#_TAB	Add R1163	
106	9	2013/5/16	reserve Pull-up for EC_LID_OUT#_TAB	Add R249 and reserve it	
107	16	2013/5/22	pop C141	Pop C141	
108	15,16	2013/5/22	Change 1uF to 2.2uF	Change C108,C123,C130,C143 to 2.2uF	
109	22,23	2013/5/22	Change 1uF to 2.2uF	Change C1328,C1343,C1356,C1368 to 2.2uF	
110	24,25	2013/5/22	Change 1uF to 2.2uF	Change C1379,C1395,C1409,C1419 to 2.2uF	
111	28	2013/5/22	Co-lay LBT schematic	Remove D1 Add U66 and co-lay with F1	
112	12,15	2013/5/22	For Cost/Part count	Remove R210,C50,C34,C126	
113	15,16	2013/5/22	For Cost/Part count	Remove C107,C109,C121,C122,C129,C131,C144,C146	

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