

KIWB3/B4

Schematics Document

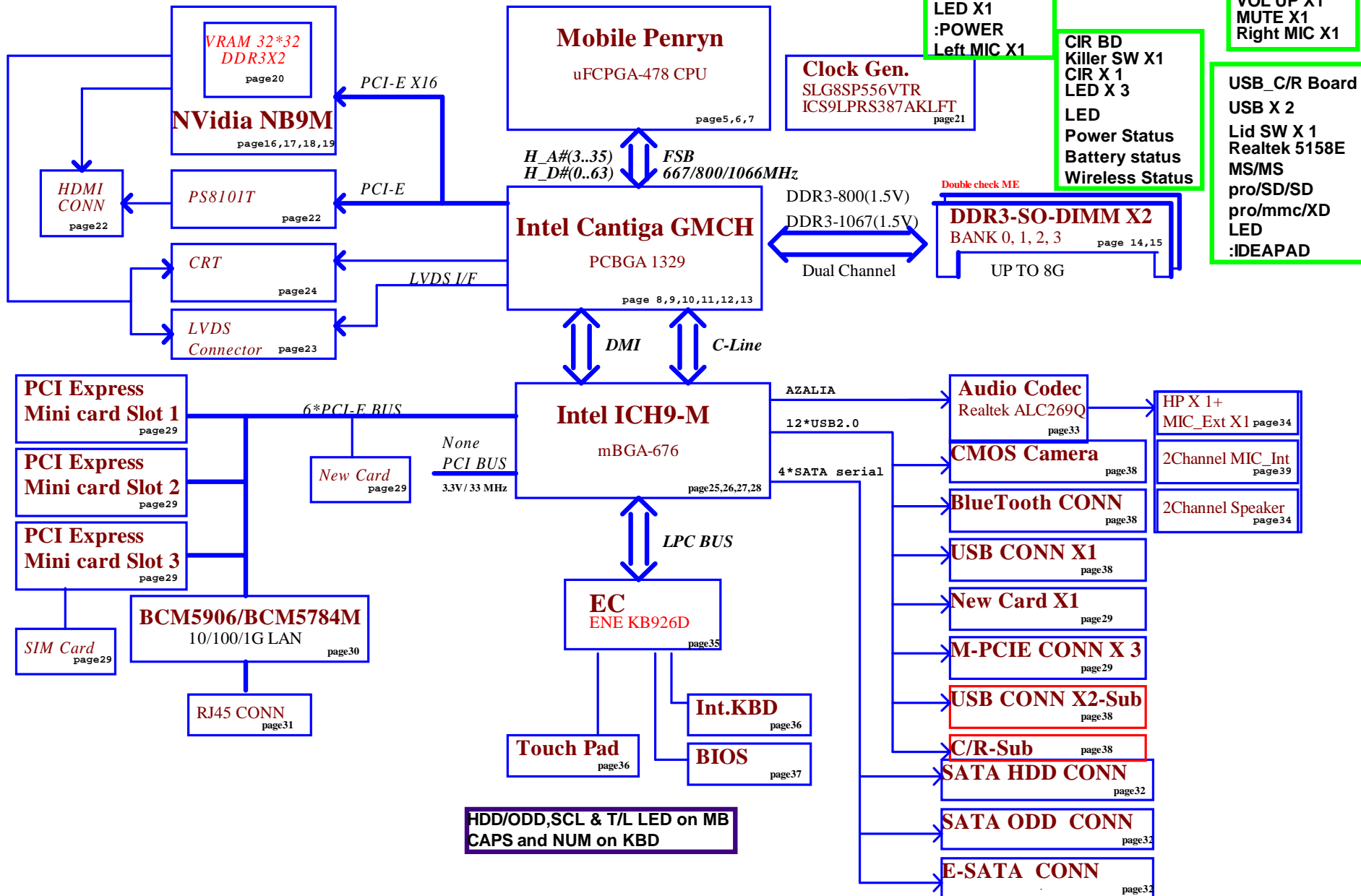
Mobile Penryn uFCPGA with Intel
Cantiga_GM/PM+ICH9-M core logic
REV:0.1

Security Classification	Compal Secret Data			Compal Electronics,Ltd.	
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Compal confidential

File Name :

ZZZ1
16W_PCB_LA4551P



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DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V +1.8V +0.75V	+5VS +3VS +1.5VS +1.1VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

PM@ , GM@ , N9@ , N10@

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	✗	✗	✗	✗	✓	✗	✗	✗	✗	✗	✓	✗	✗
EC_SMB_CK2 EC_SMB_DA2	KB926	✗	✗	✗	✗	✗	✗	✗	✓	✗	✗	✗	✓	✓
ICH_SMBCLK ICH_SMBDAT	ICH9	✗	✗	✗	✗	✗	✓	✓	✗	✓	✓	✗	✗	✗
LVDS_SCL LVDS_SDA	Cantiga	✗	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	✗	✗	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
HDMI_CLK_NB HDMI_DAT_NB	Cantiga	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
VGA_DDCCLK VGA_DDCDATA	VGA	✗	✗	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	✗	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	✓	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	✗	✗	✗	✗	✓	✗	✗	✗	✗	✗	✗	✗	✗
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	✗	✗	✗	✗	✓	✗	✗	✗	✗	✗	✗	✗	✗
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	✗	✗	✗	✗	✓	✗	✗	✗	✗	✗	✗	✗	✗

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VGA and DDR2 Voltage Rails (NB9M-GS)

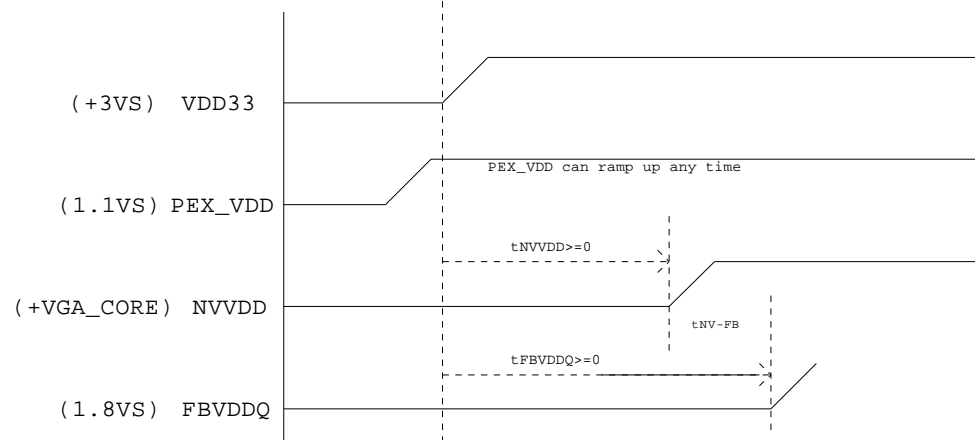
power plane State			+1.8V	+3VS +VGA_CORE +1.1VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EDP at Tj = 97C*

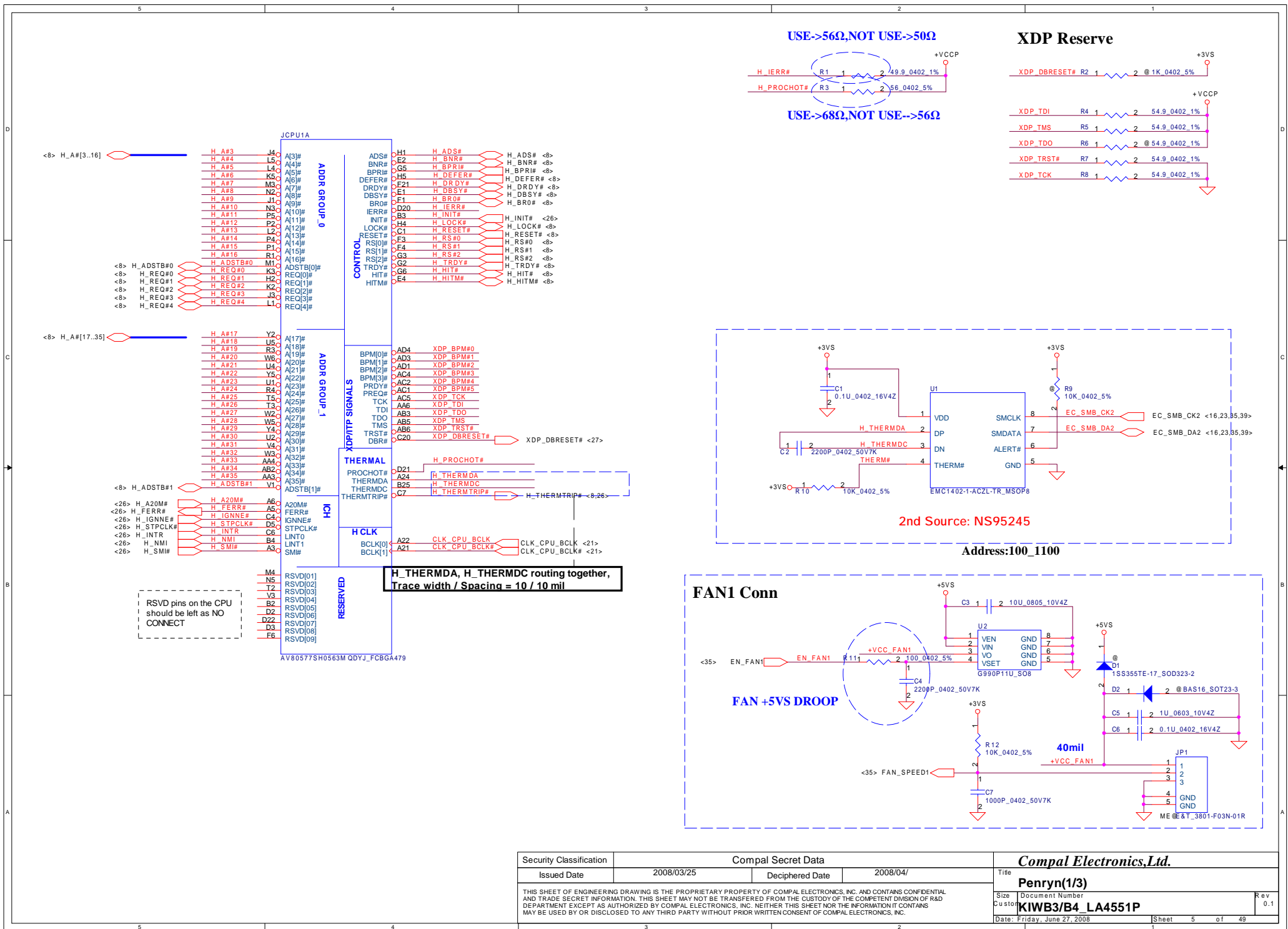
Power Supply Rail		NB9M-GS		NB9M-GE	
	(V)	GDDR3	DDR2	GDDR3	DDR2
NVVD	Variable	11.22A	10.87A	9.2A	8.88A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	165mA			
PLLVD	1.1	55mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.425A			
FBVDDQ	1.8	2.24A	1.65A	2.17A	1.63A
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	2.76A	2.17A	2.69A	2.15A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	125mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	80mA			
TOTAL	3.3	0.445A			

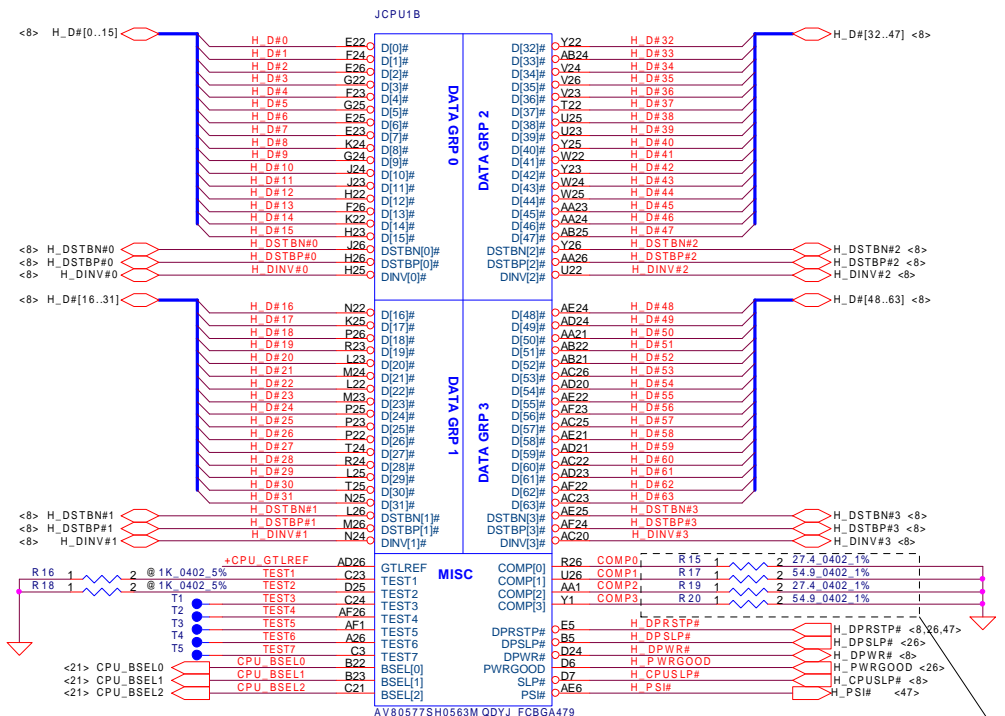
POWER SQUENCE

The ramp time for any rail must be more than 40us



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Trace Close CPU < 0.5'

Width=4 mil,
Spacing: 15mil
(550hm)

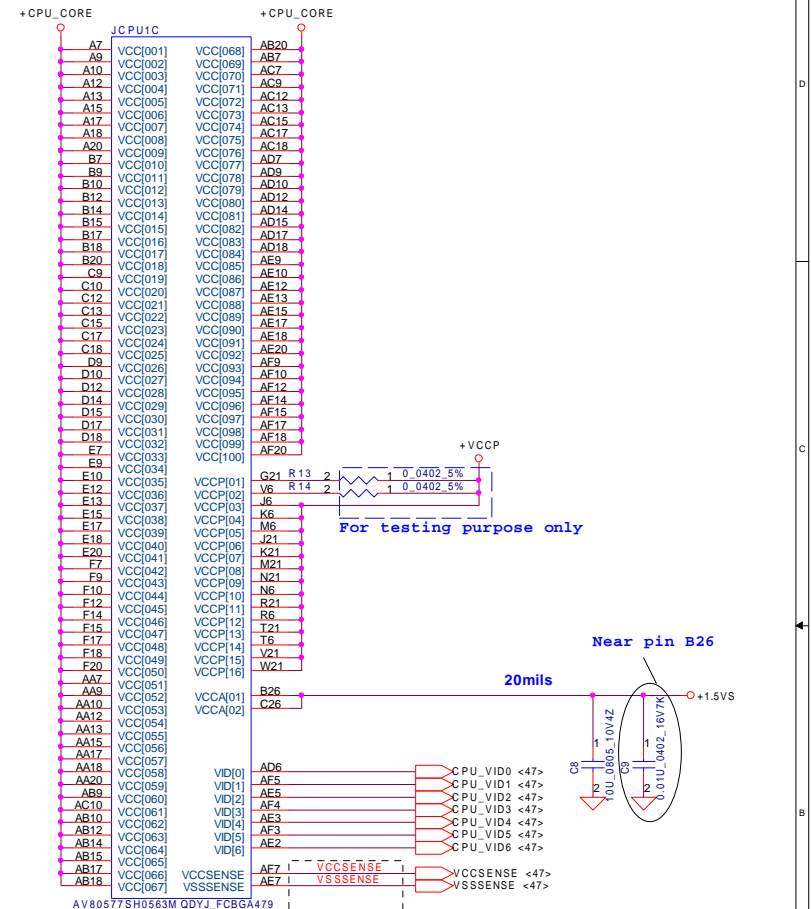
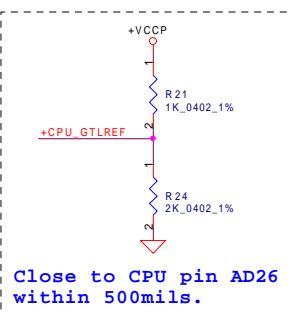
TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 5mils and Space 25mils (550hms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

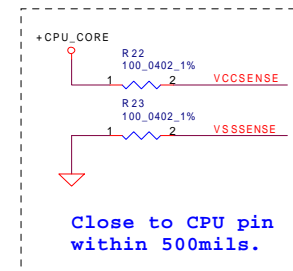
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Layout note: Z0=55 ohm
0.5" max for GTLREF.

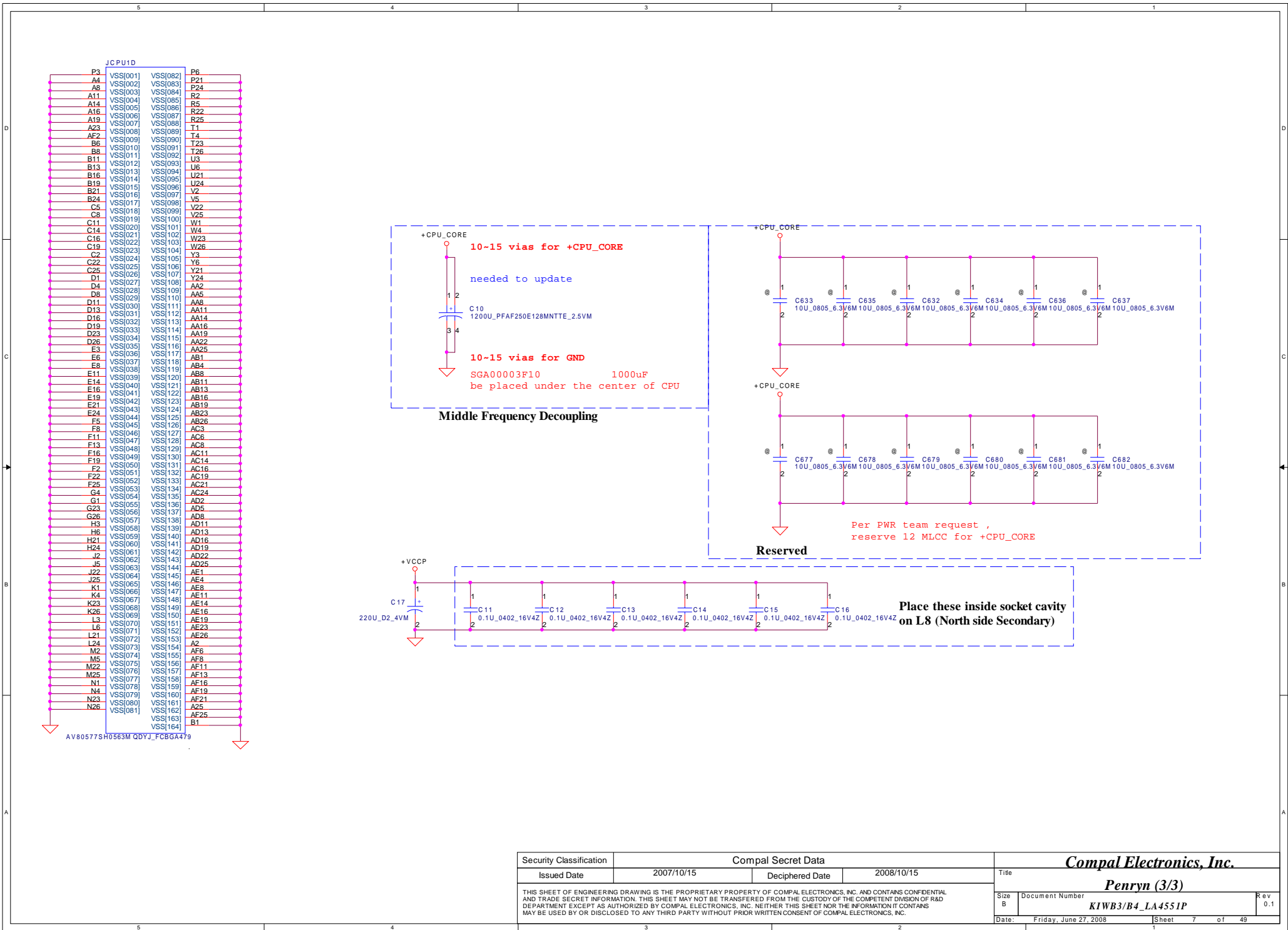


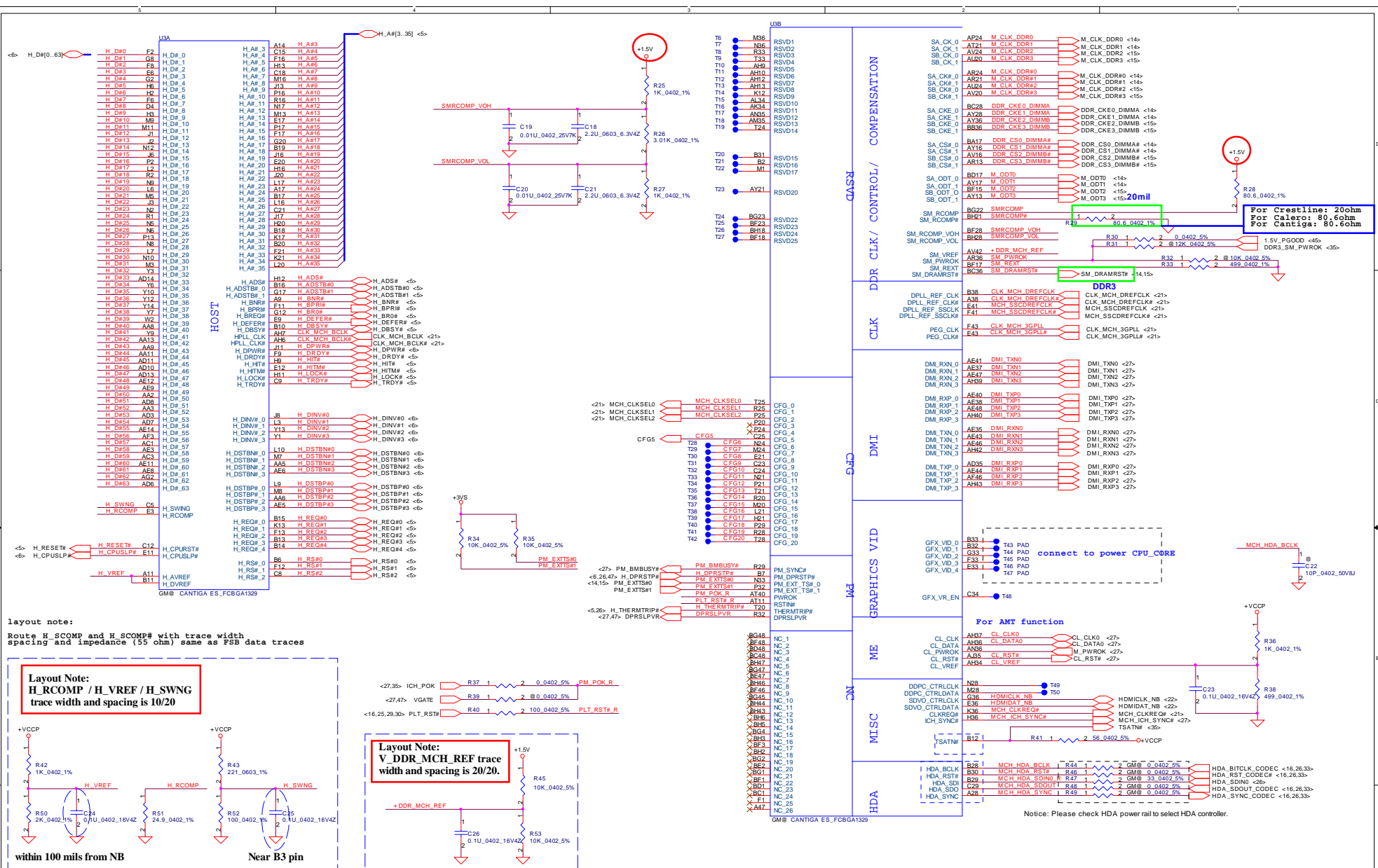
Length match within 25 mils.
The trace width/space/other is
18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at
27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

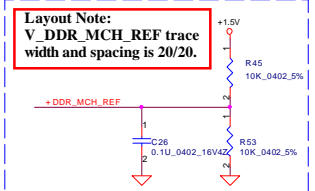
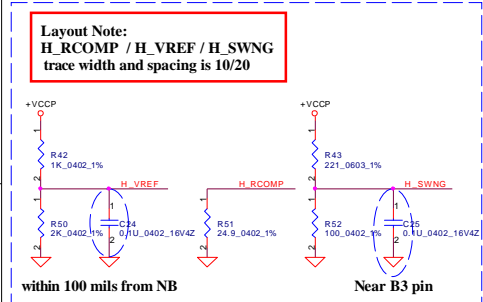


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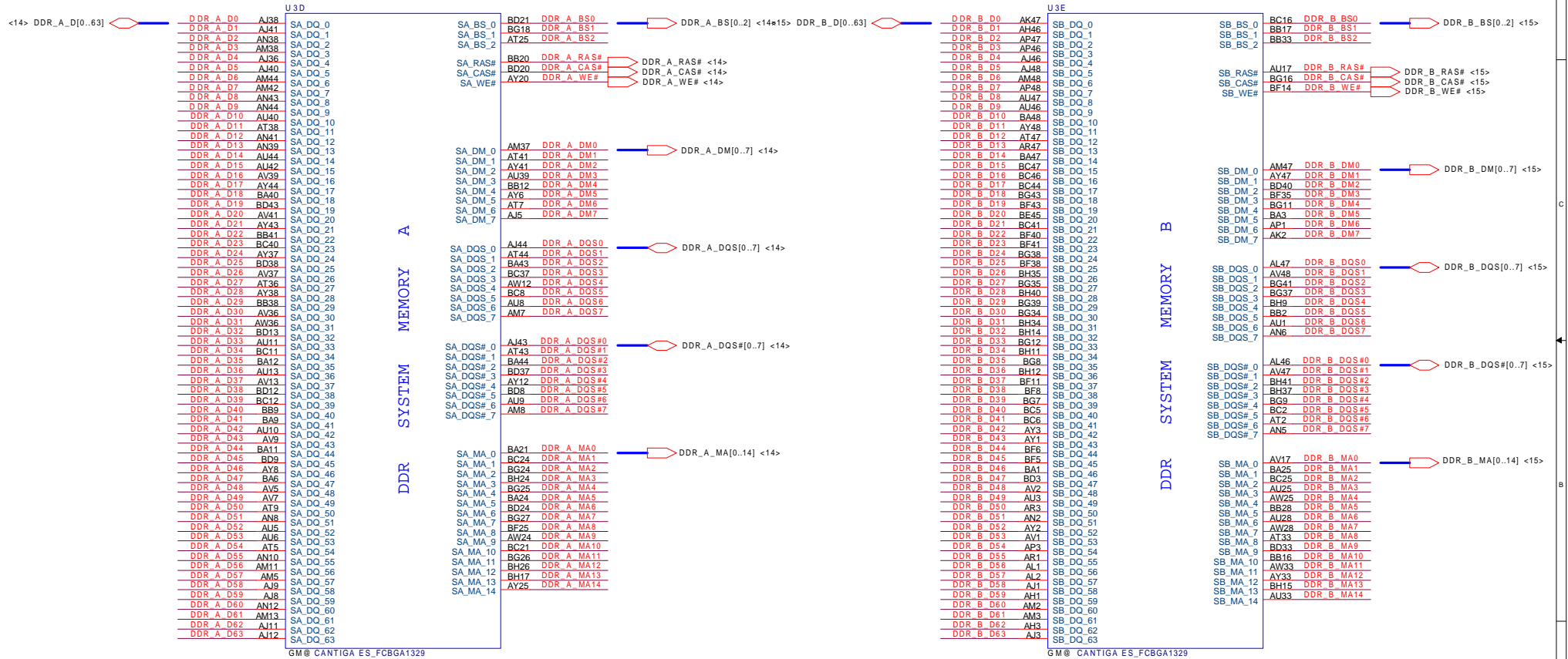
layout note:
Route H_SCMP and H_SCMP# with trace width spacing and impedance (55 ohm) same as FSB data traces



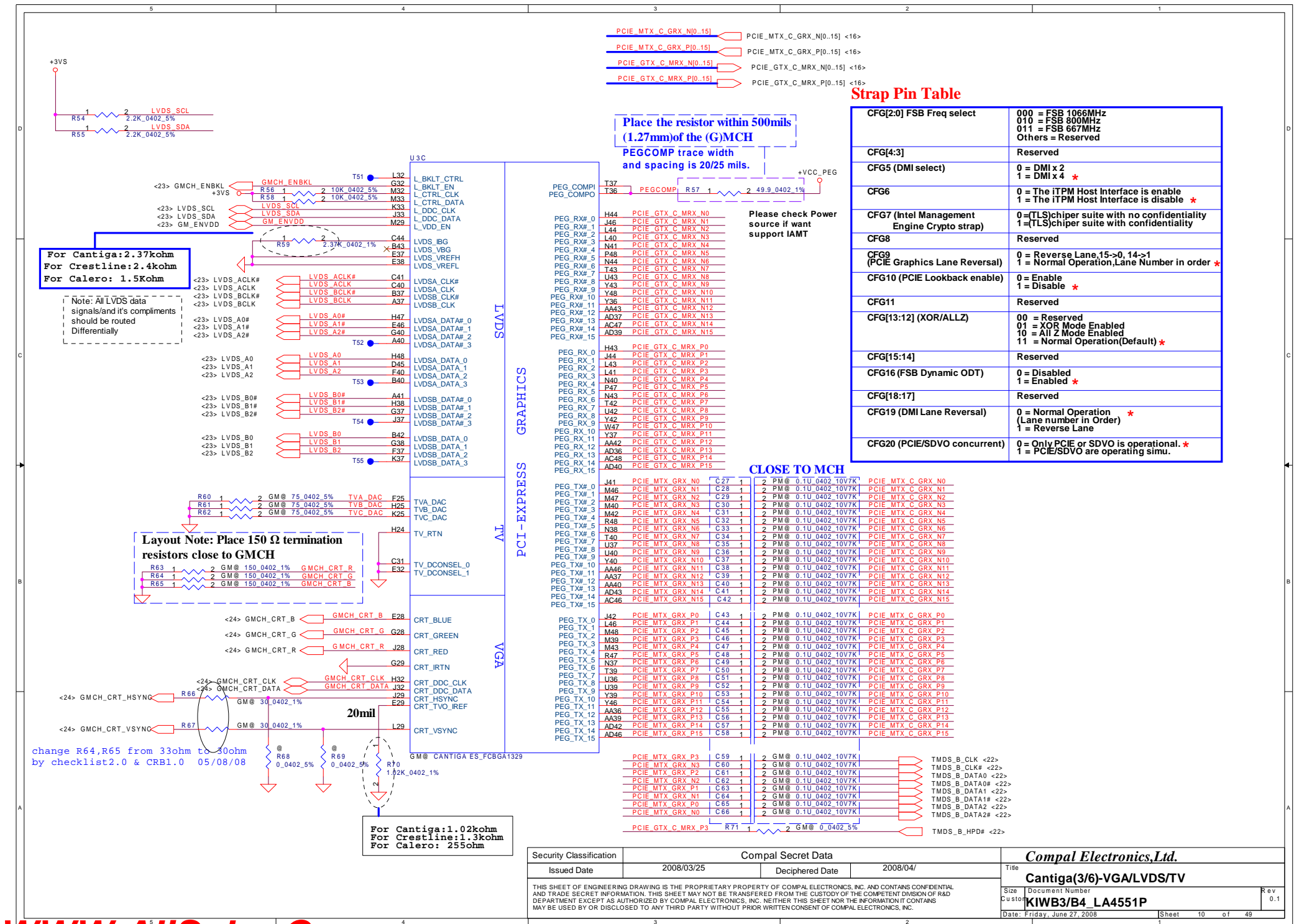
Security Classification		Compel Secret Data		Title	
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MEMORY 7-GROUPS

1. Data Bus;
 2. Data Strobe Differential Pairs;
 3. Data Mask Bits;
 4. Address Group;
 5. Bank Select Group;
 6. Command Group;
 7. CLK Group;
- *. Reset Group;



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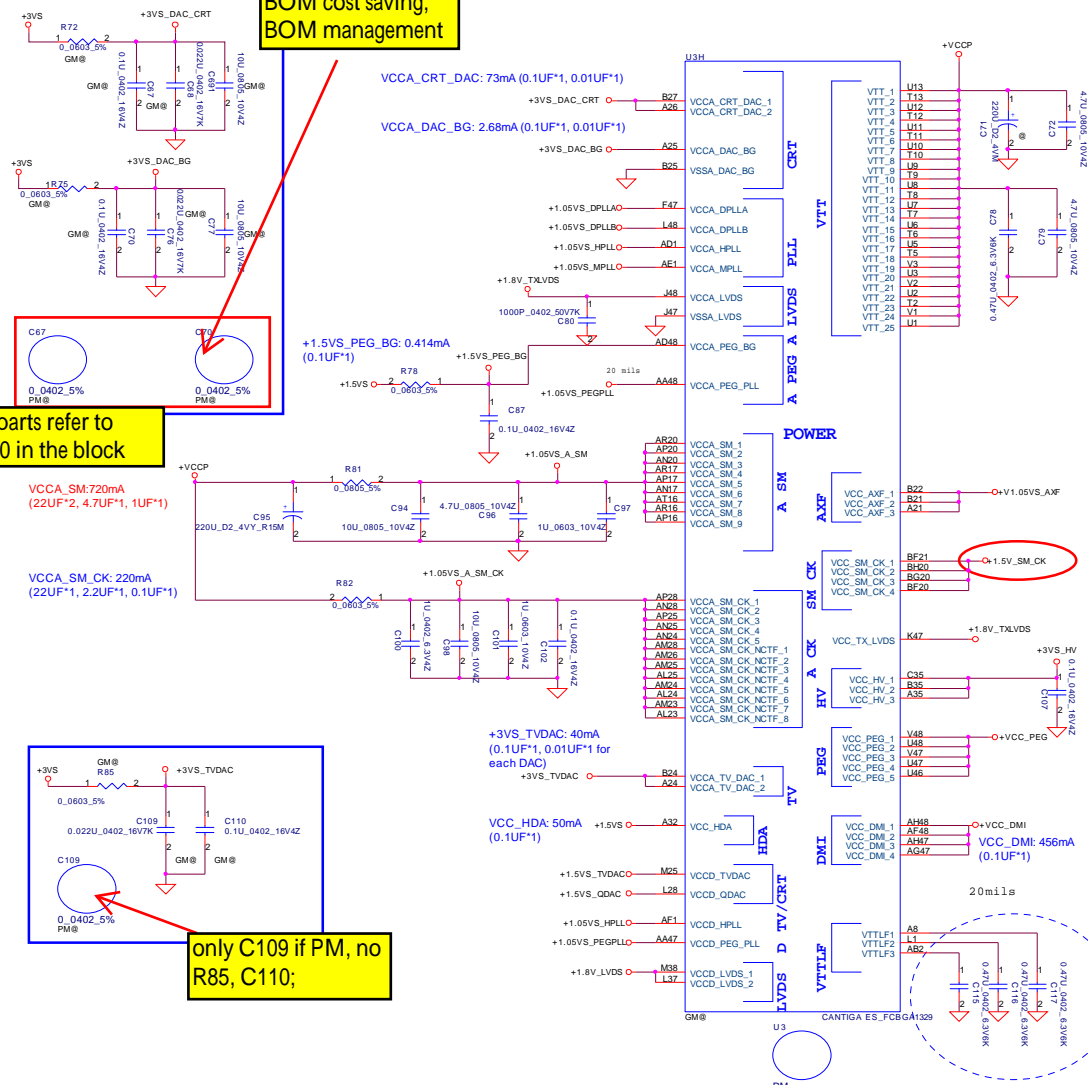


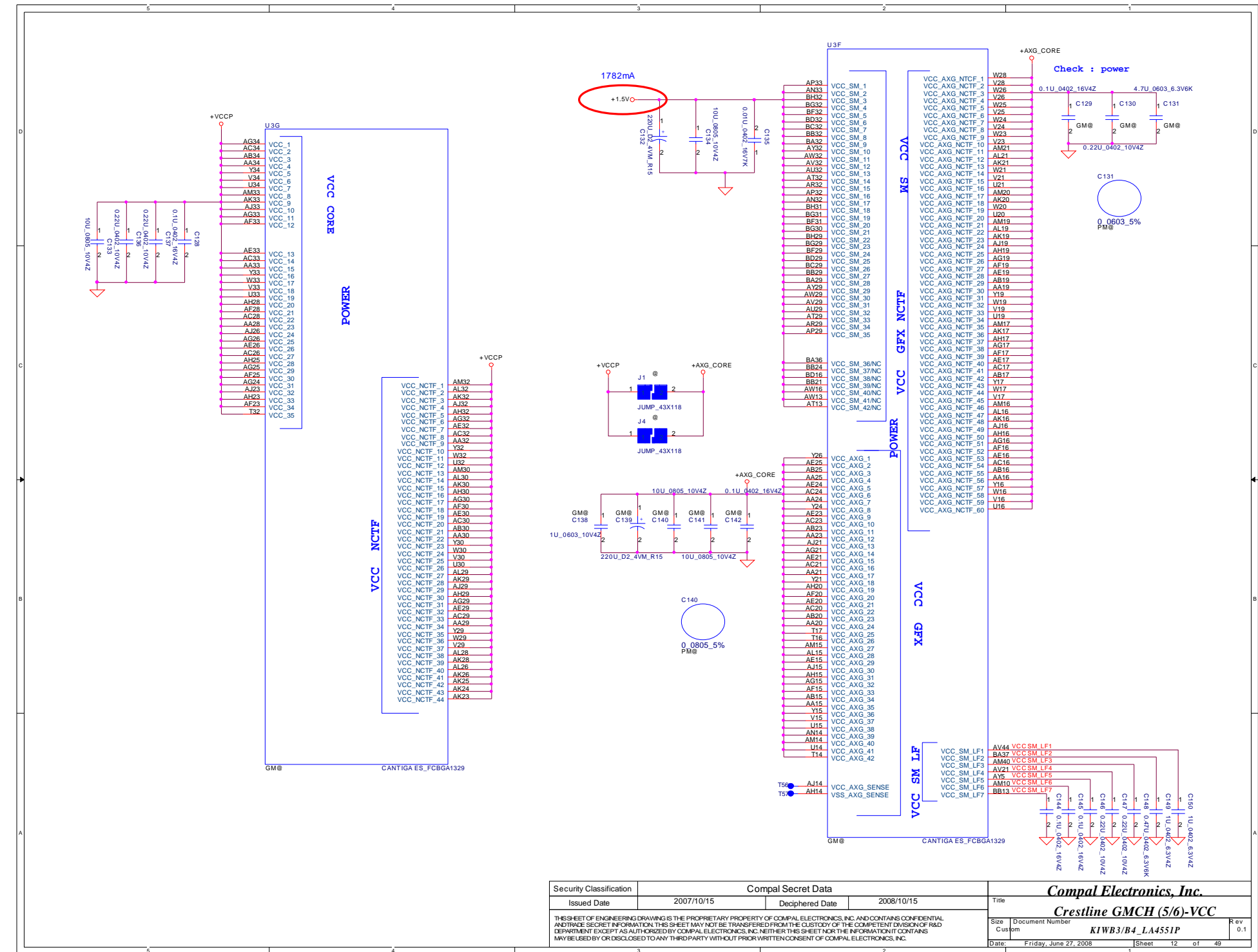
BOM cost saving,
BOM management

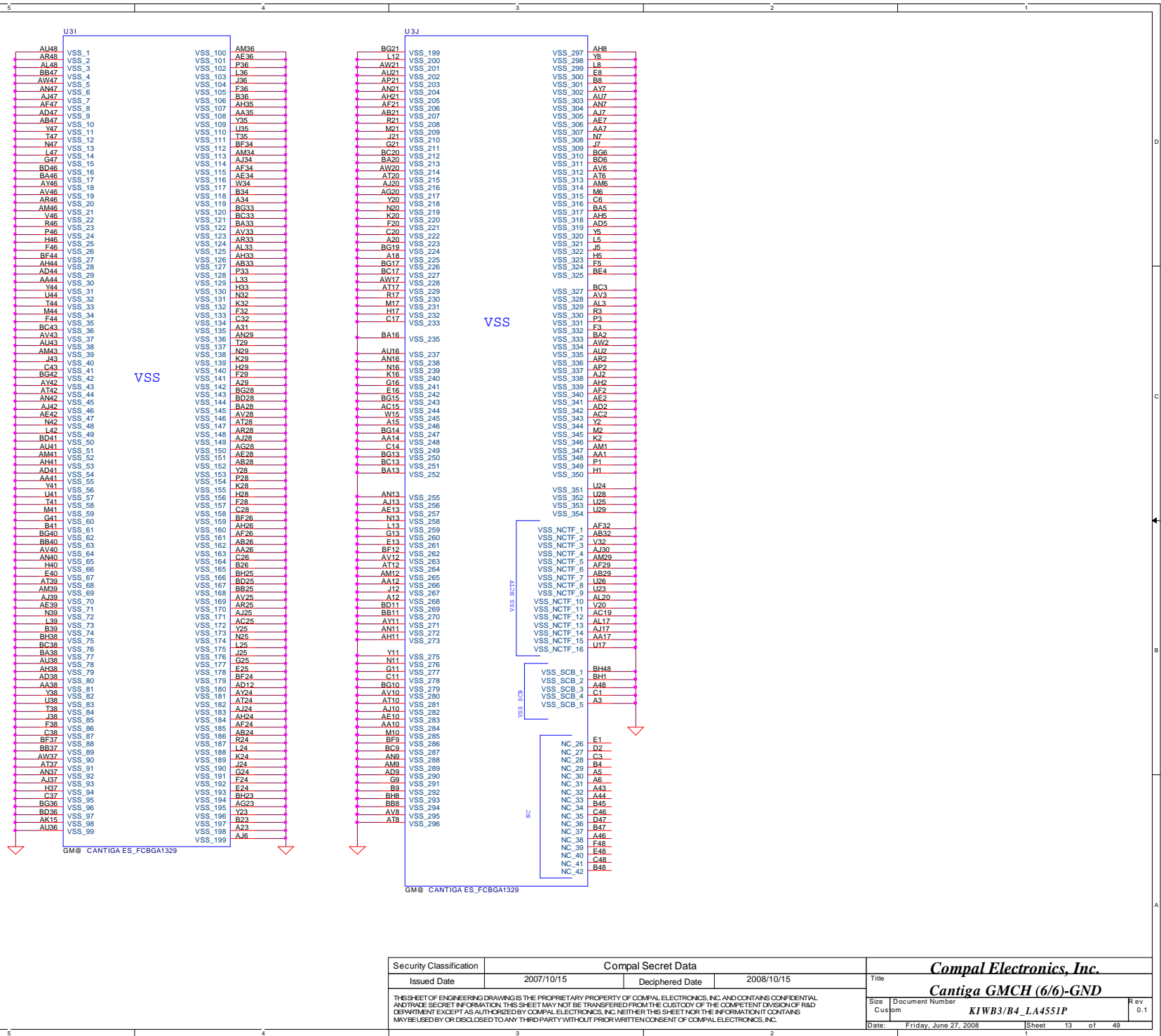
the two parts refer to
C67, C70 in the block

only C109 if PM, no
R85, C110;

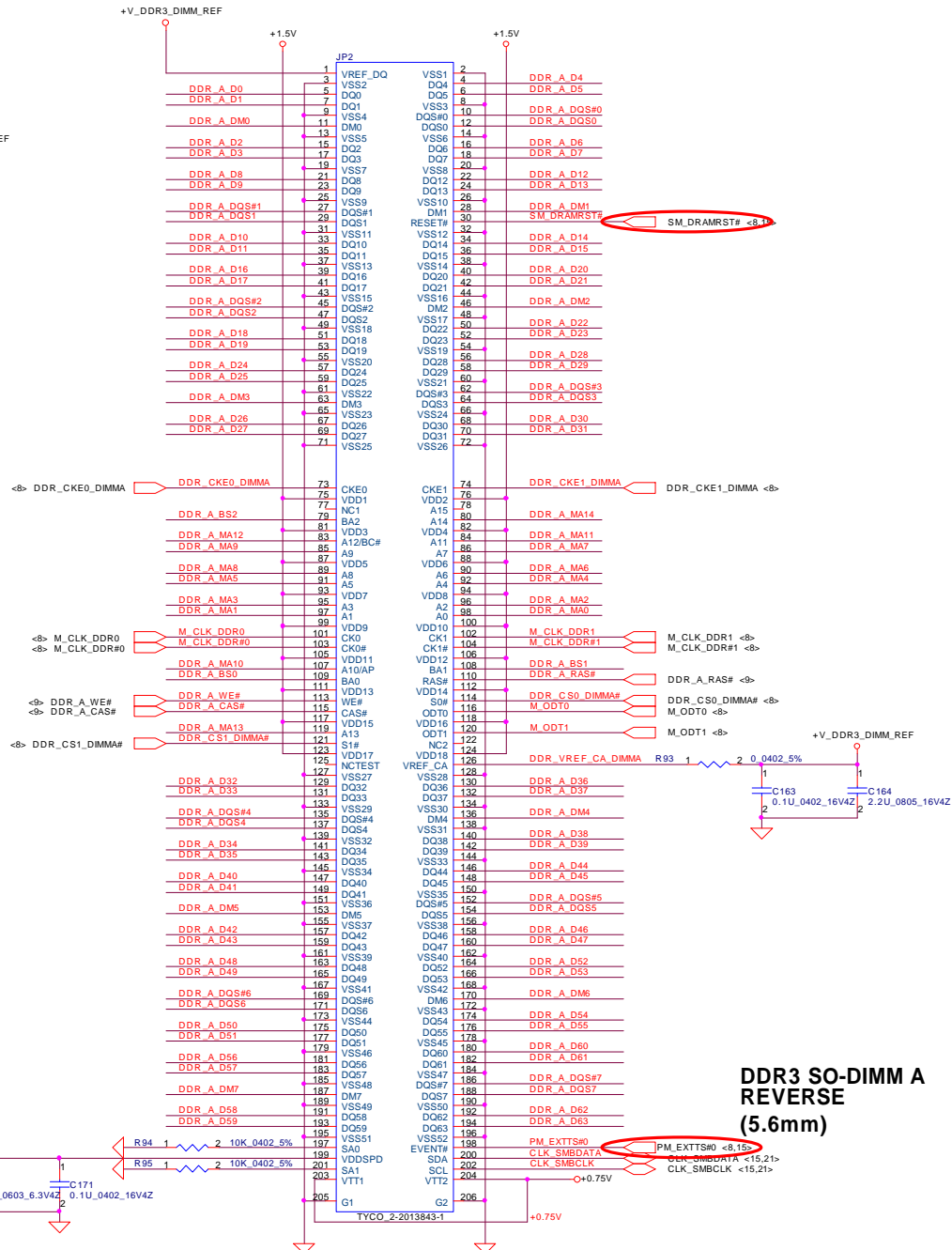
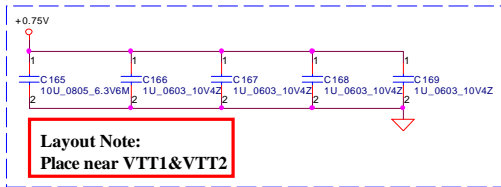
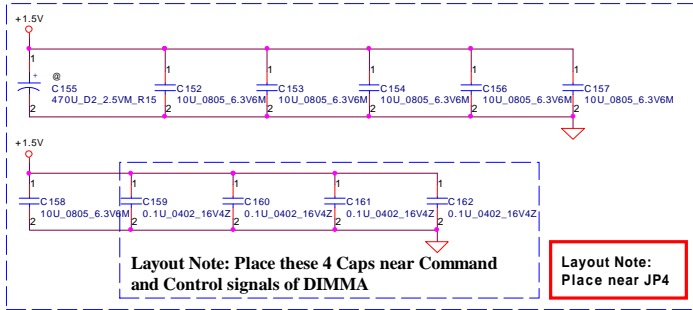
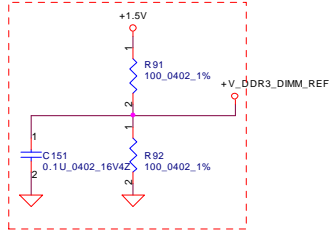
value of bypass cap. depends on the
maximum switching current and
impedance of the trace;



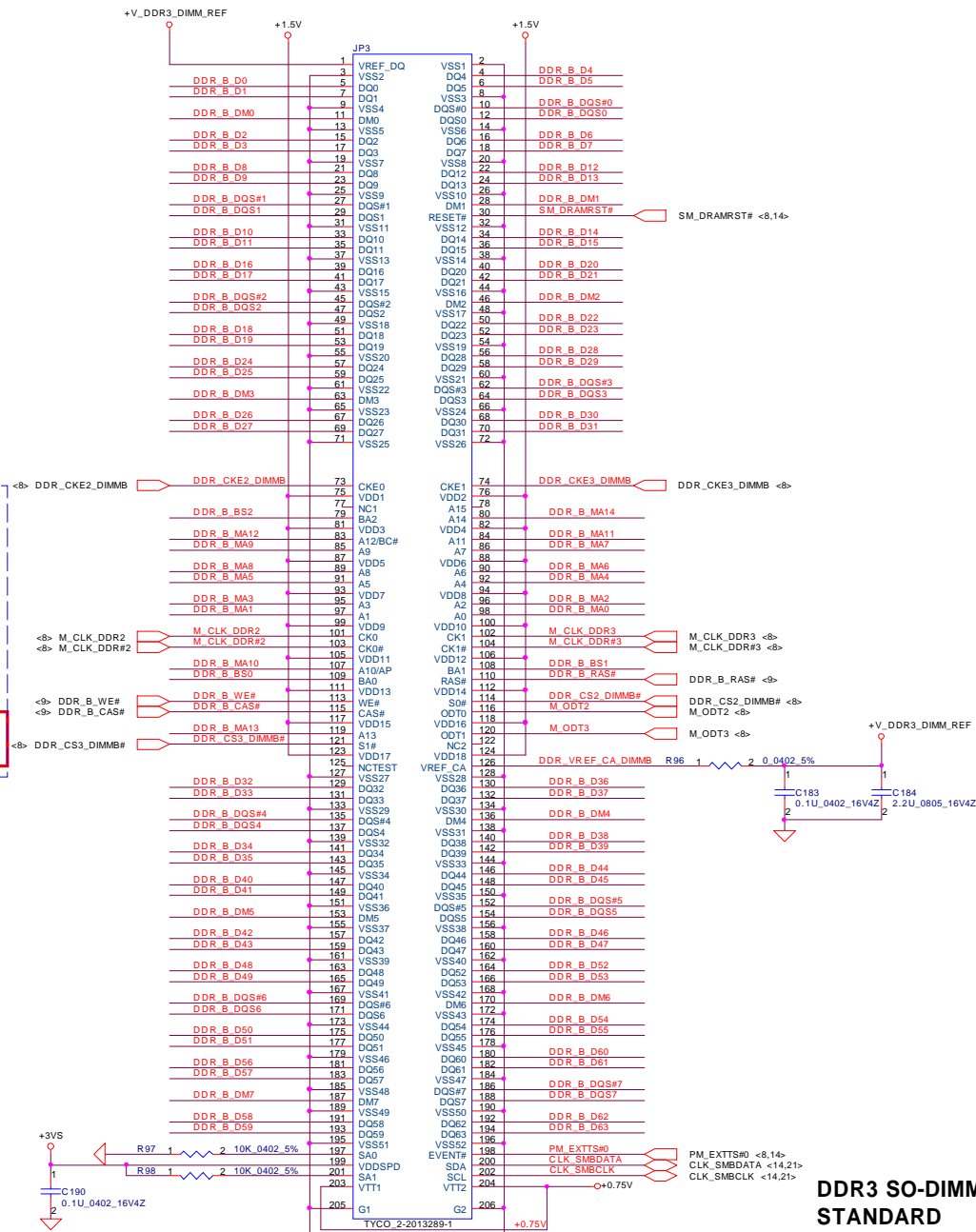




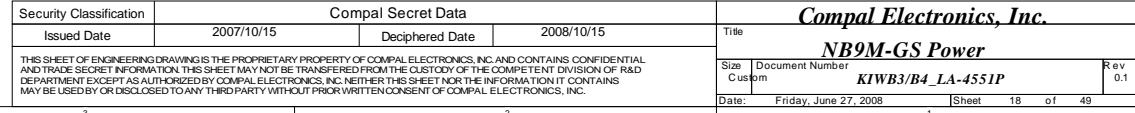
<9> DDR_A_DQS#[0..7]
 <9> DDR_A_D[0..63]
 <9> DDR_A_DM[0..7]
 <9> DDR_A_DQS[0..7]
 <9> DDR_A_MA[0..14]
 <9> DDR_A_BS[0..2]



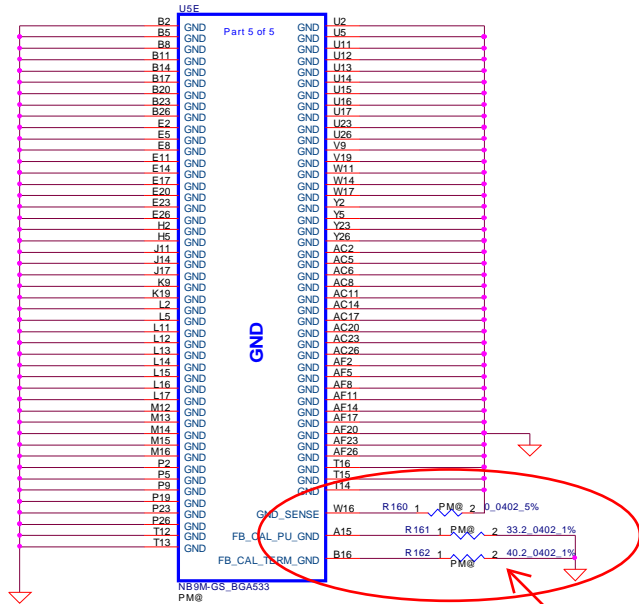
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				DDR3-SODIMM SLOT1		
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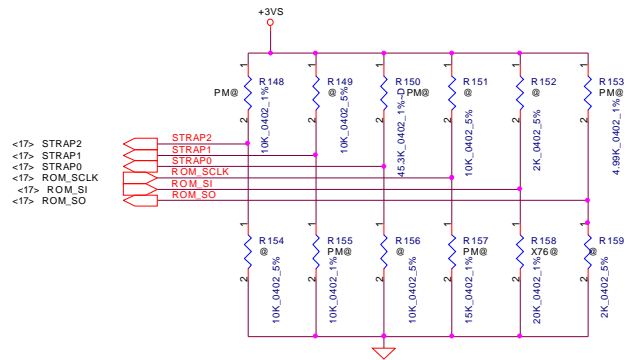


A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



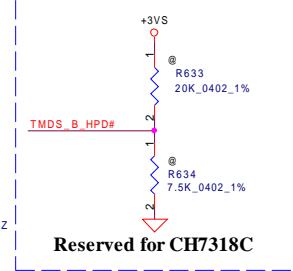
Memory/PKG	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR2	30.1ohm	30.1ohm	NC
GDDR3	33.2ohm	44.2ohm	40.2ohm

To update for NV PUN-03304-001_V06 (2008/4/01)



GB1 Family GPU Strap Options

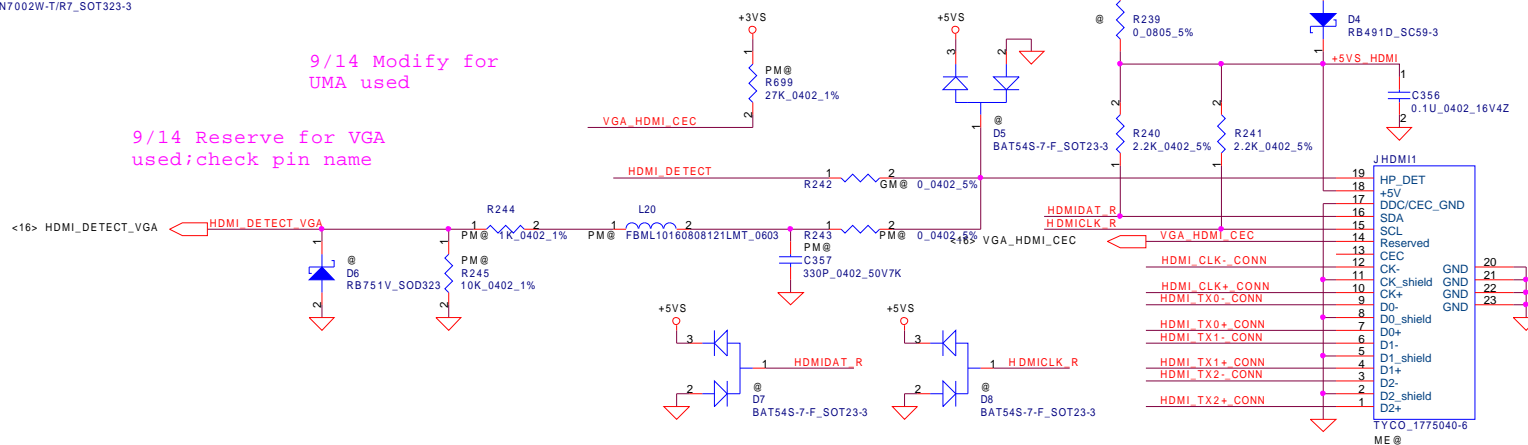
GPU	FB Memory (GDDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	16Mx32	PU 5K	PD 15K	PD 20K	PU 10K	PD 10K
		32Mx32	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K
	Hynix	16Mx32	PU 5K	PD 15K	PD 15K	PU 10K	PD 10K
		32Mx32	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K
	Qimonda	16Mx32	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K
		32Mx32	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K



NEAR CONNECTOR

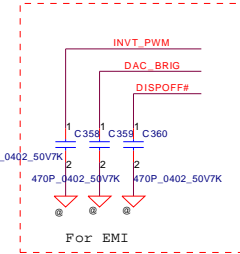
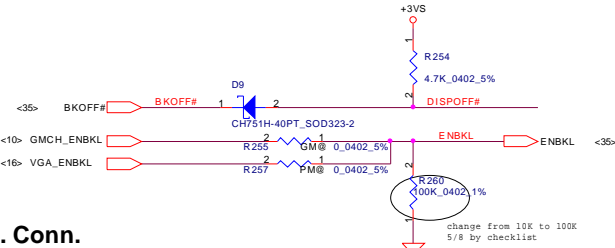
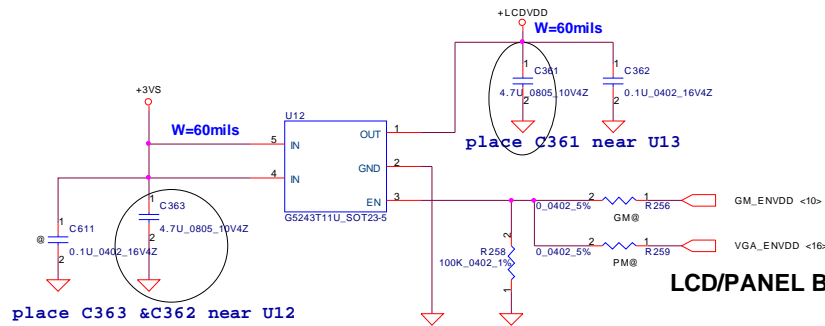


9/14 Reserve for VGA
used;check pin name

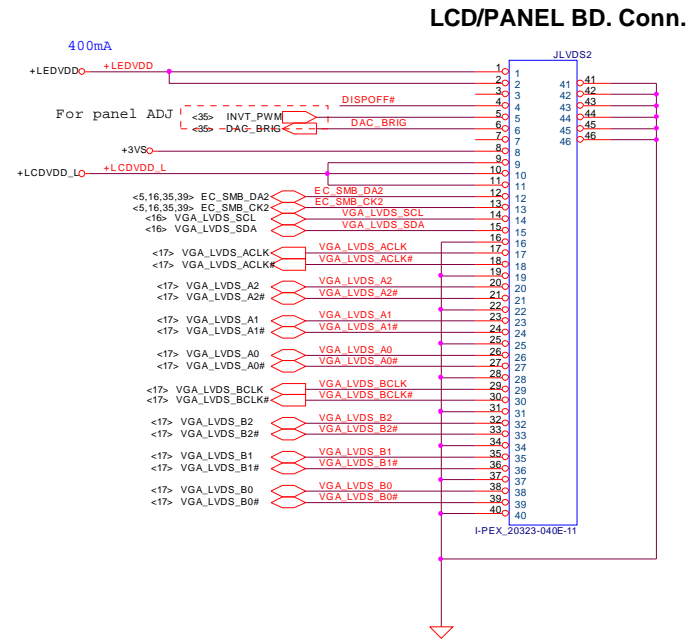
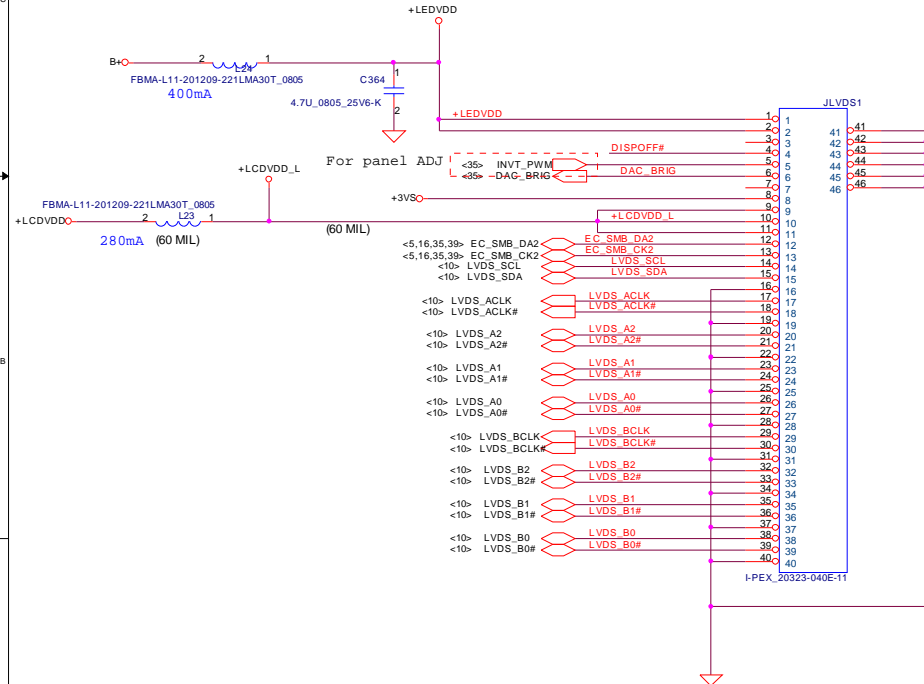


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LCD POWER CIRCUIT



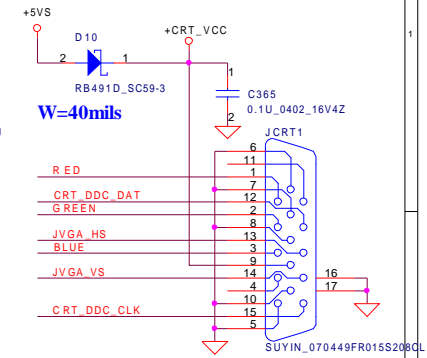
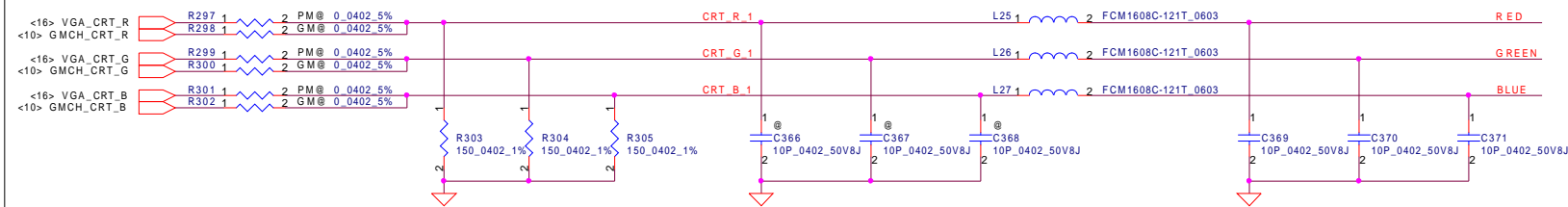
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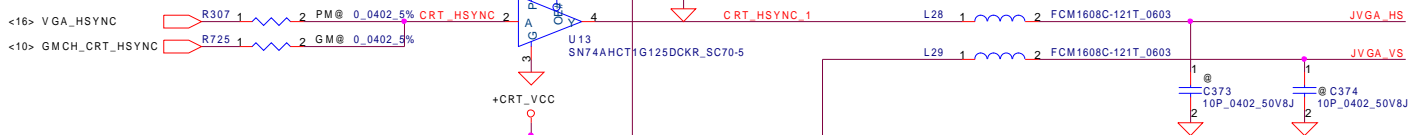
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Compal Electronics, Inc.				
LVDS & DVI Connector				
Size	Document Number	JITRI_LA-4141P		Rev 0.1
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CRT Connector

CLOSE TO CONN



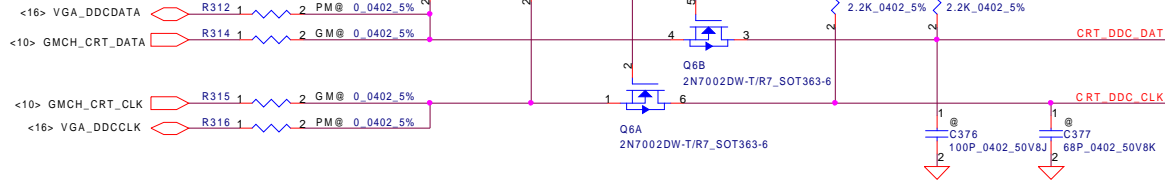
CLOSE TO CONN



CLOSE TO CONN



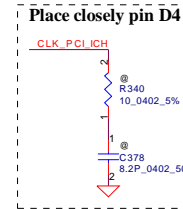
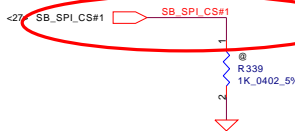
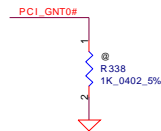
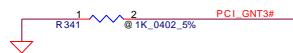
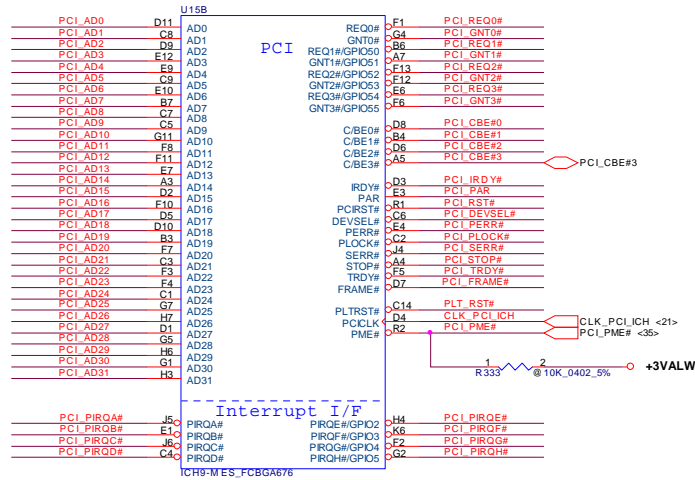
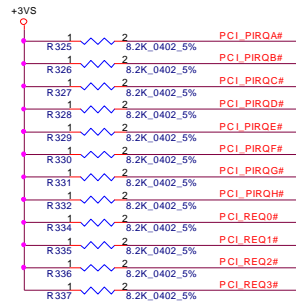
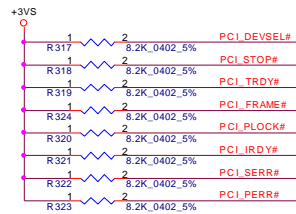
CLOSE TO CONN



PIN ASSIGMENT

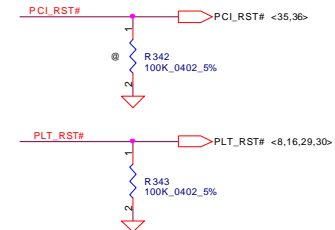
D-SUB	FUNCTION
9	+CART_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

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Size	Custom	Document Number	J1TR1_LA-4141P	Rev 0.1
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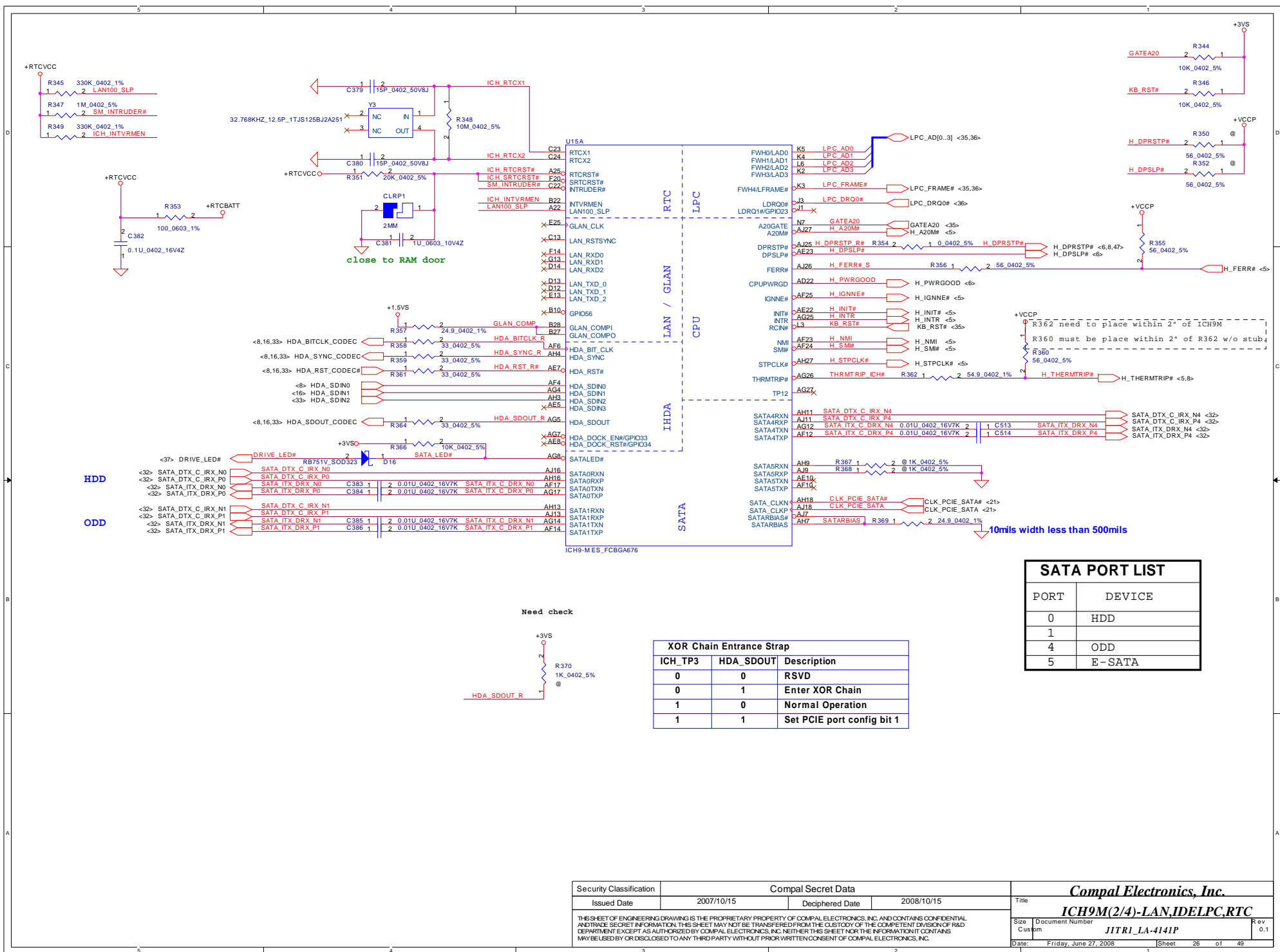


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



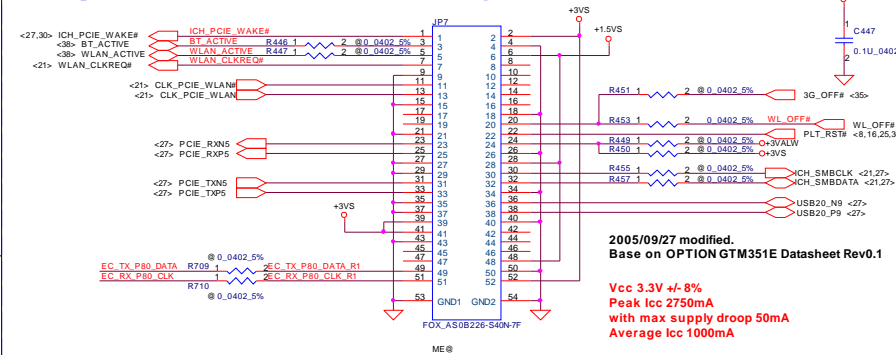
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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				Document Number
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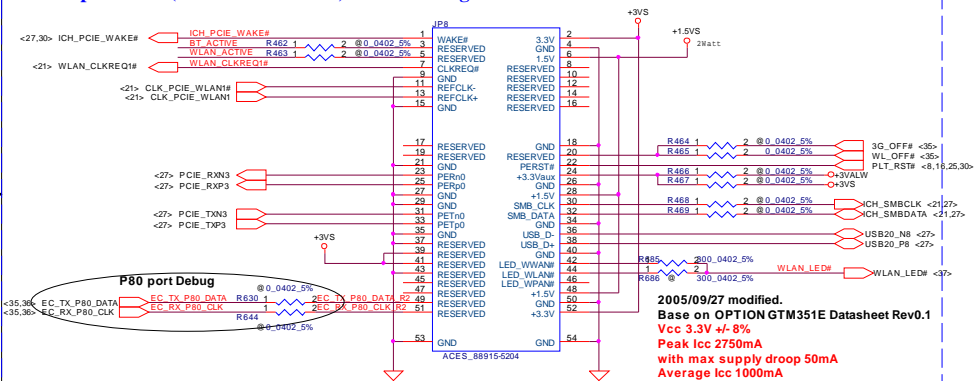


Mini-Express Card for 3G Or TV Tuner Mini-Express Card for WLAN

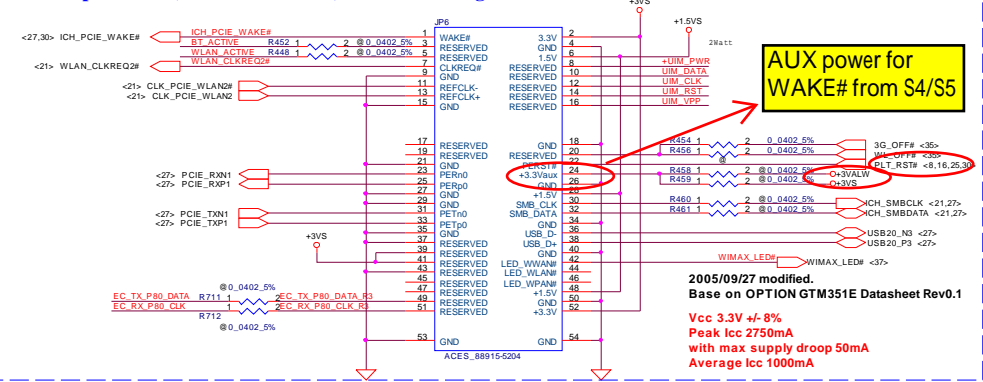
Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high



Mini-Express Card(Slot 2-WIRELESS) 5.2mm high

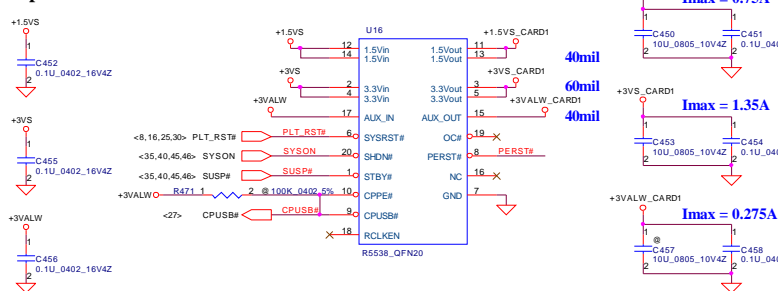


Mini-Express Card(Slot 3-WWAN 3G) 5.2mm high

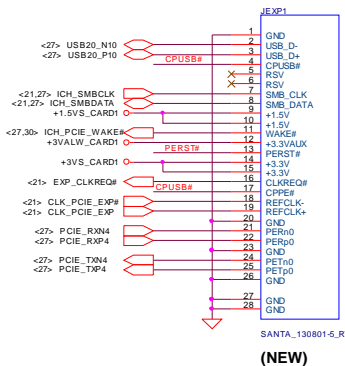


AUX power for
WAKE# from S4/S5

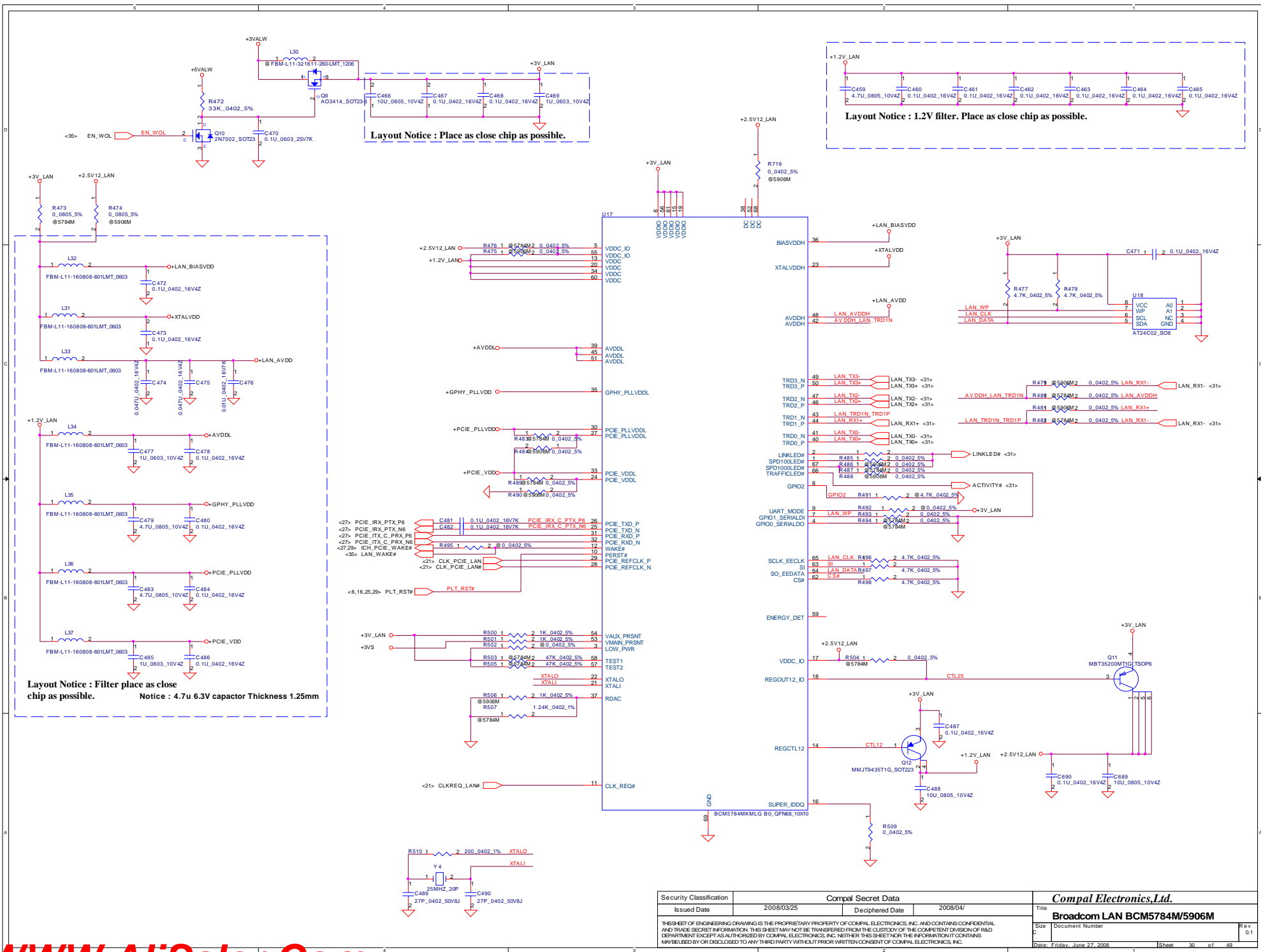
Express Card Power Switch



New Card 34mm Socket (Left/TOP)

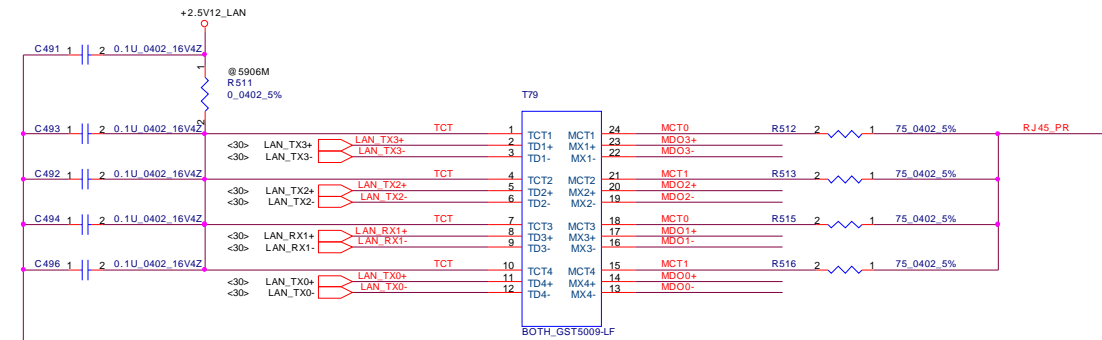


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Size	Document Number	Rev
J1TR1_LA-4141P		0.1
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29	of	69

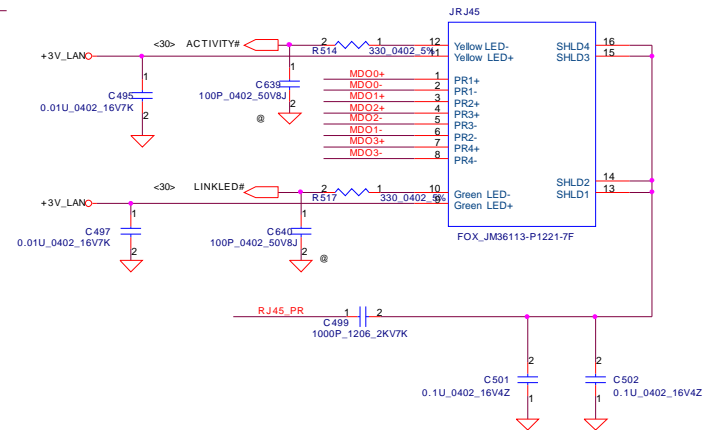
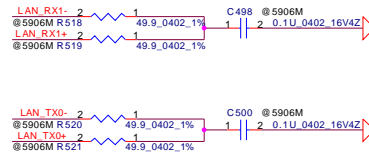


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Issued Date		Deciphered Date		Title	
2008/03/25		2008/04/		Broadcom LAN BCM5784M/5906M	
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		Date: Friday, June 27, 2008		Sheet 30 of 49	
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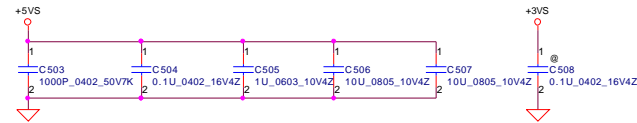
RJ45 CONN



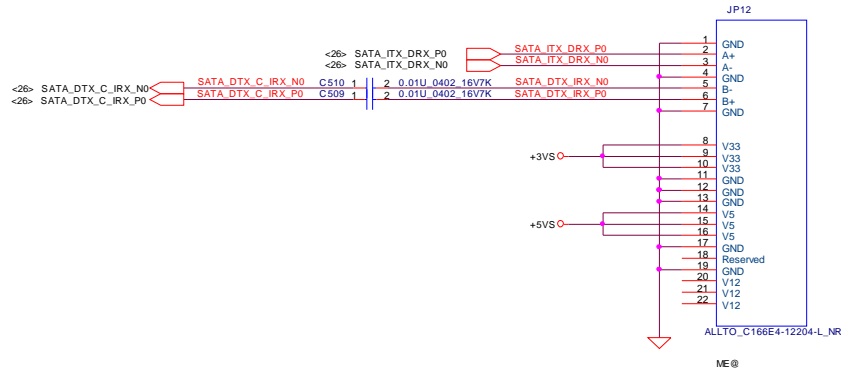
near LAN controller



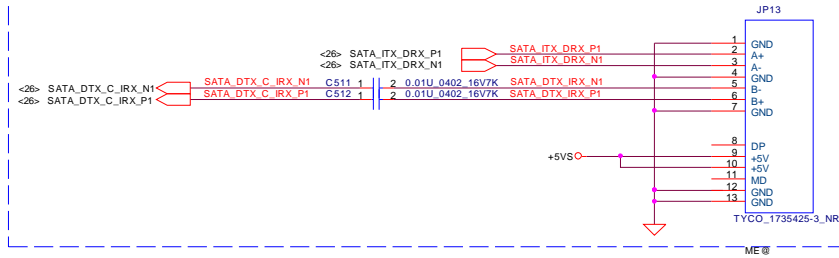
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Custom	JITRI_LA-4141P
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SATA HDD Conn.

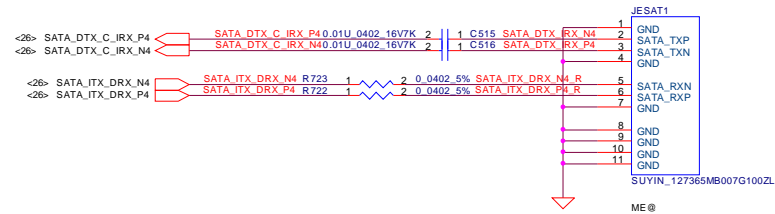


SATA ODD Conn.

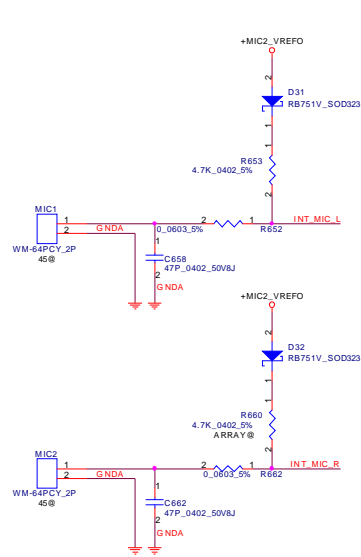
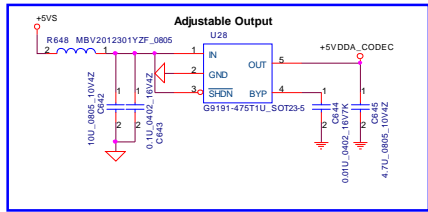


E-SATA Conn.

place R722&R723&C515&C516
near JESAT1



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				Date:	Friday, June 27, 2008	Sheet 32 of 48

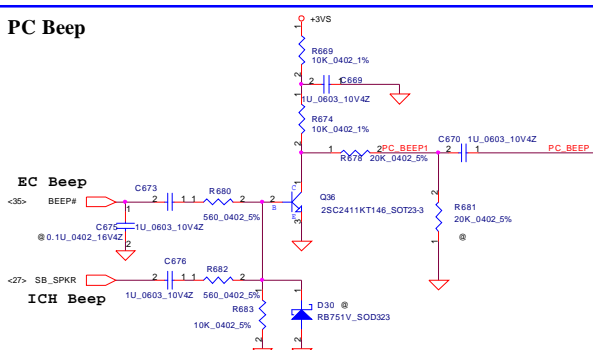
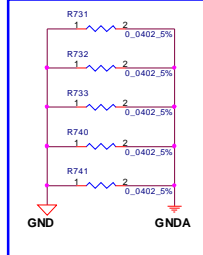


MIC Sense
R516 place near pin13
Capless HP Sense
R517 place near pin34

<38> MIC_ID
<38> PLUG_IN

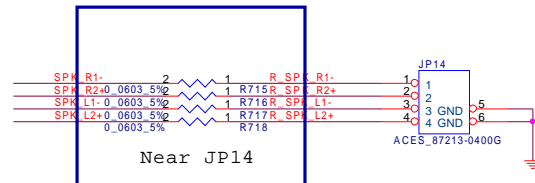


ALC272-GR_LQFP48

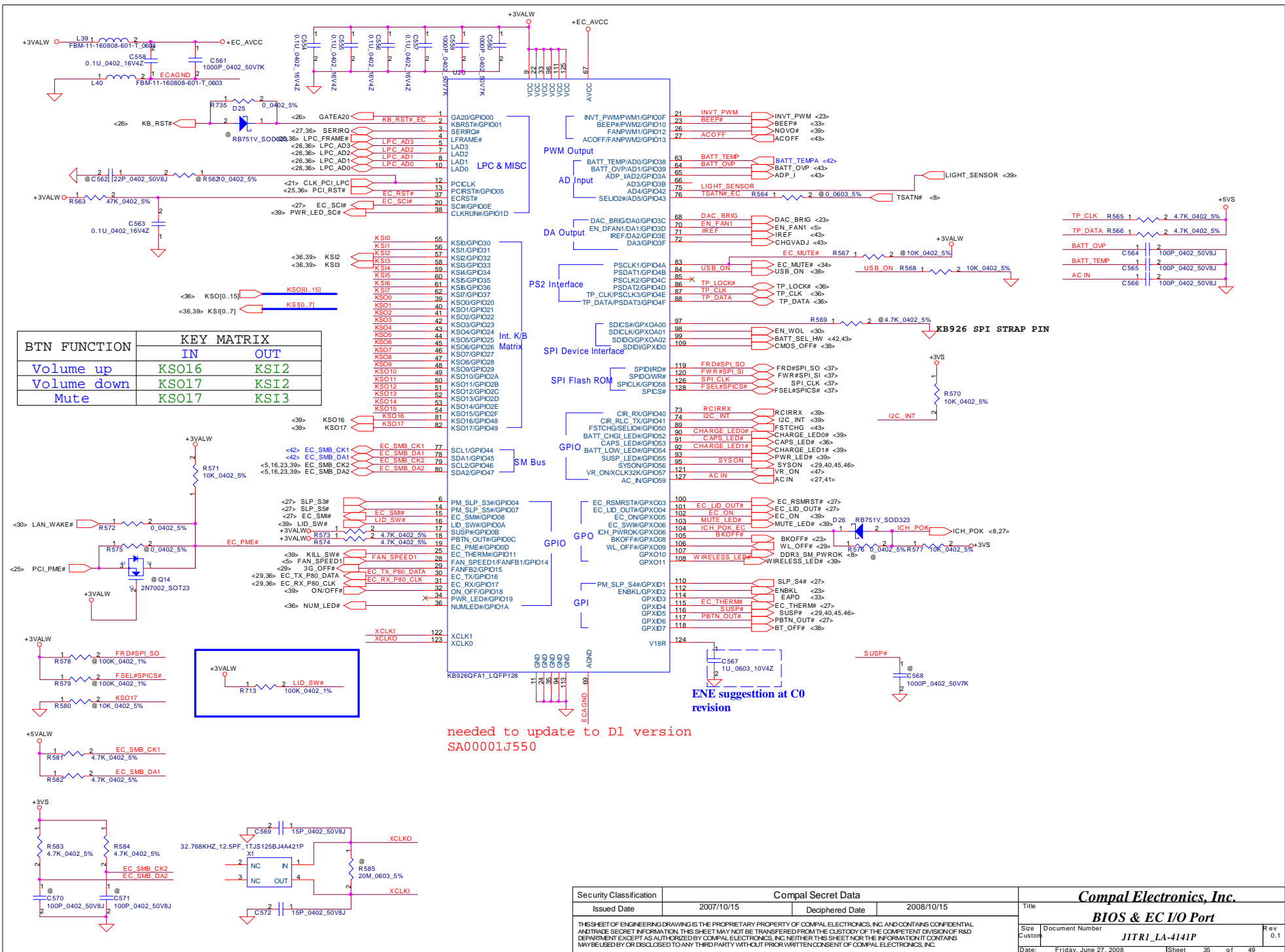


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Compal Electronics Ltd.		Title	
HD Audio Codec ALC272		Rev	
Document Number		Rev	
KTWB3/B4 LA4551P		Rev	
Date: Friday, June 27, 2008		Sheet	
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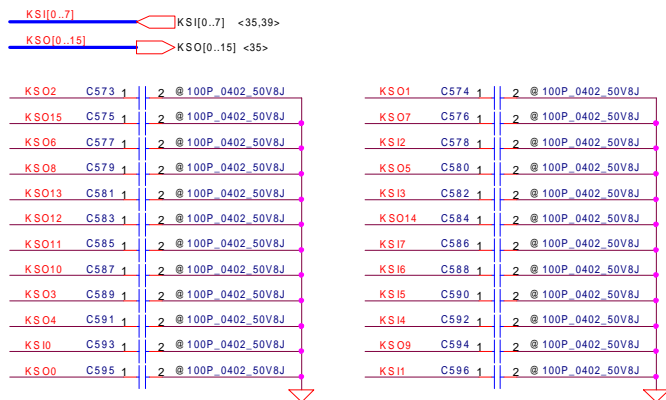
5	4	3	2	1
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WWW.AliSaler.Com

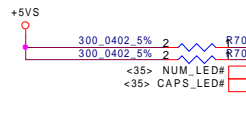
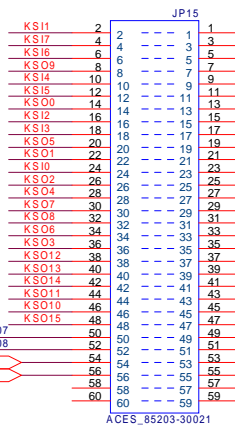


INT_KBD Conn.

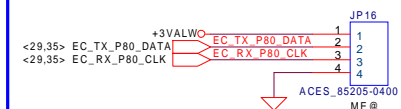


CONN PIN define need double check

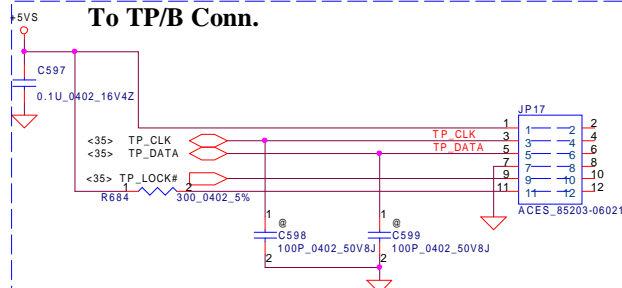
Source:SP01000IE00
2nd source:SP01000IF00
30 pin



EC DEBUG PORT

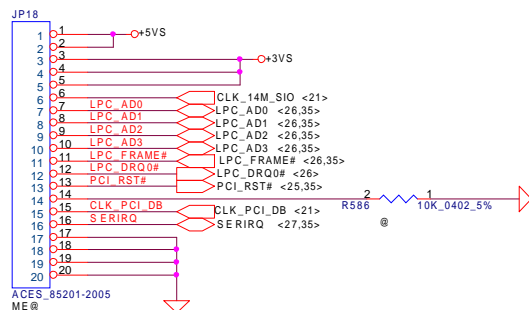


To TP/B Conn.



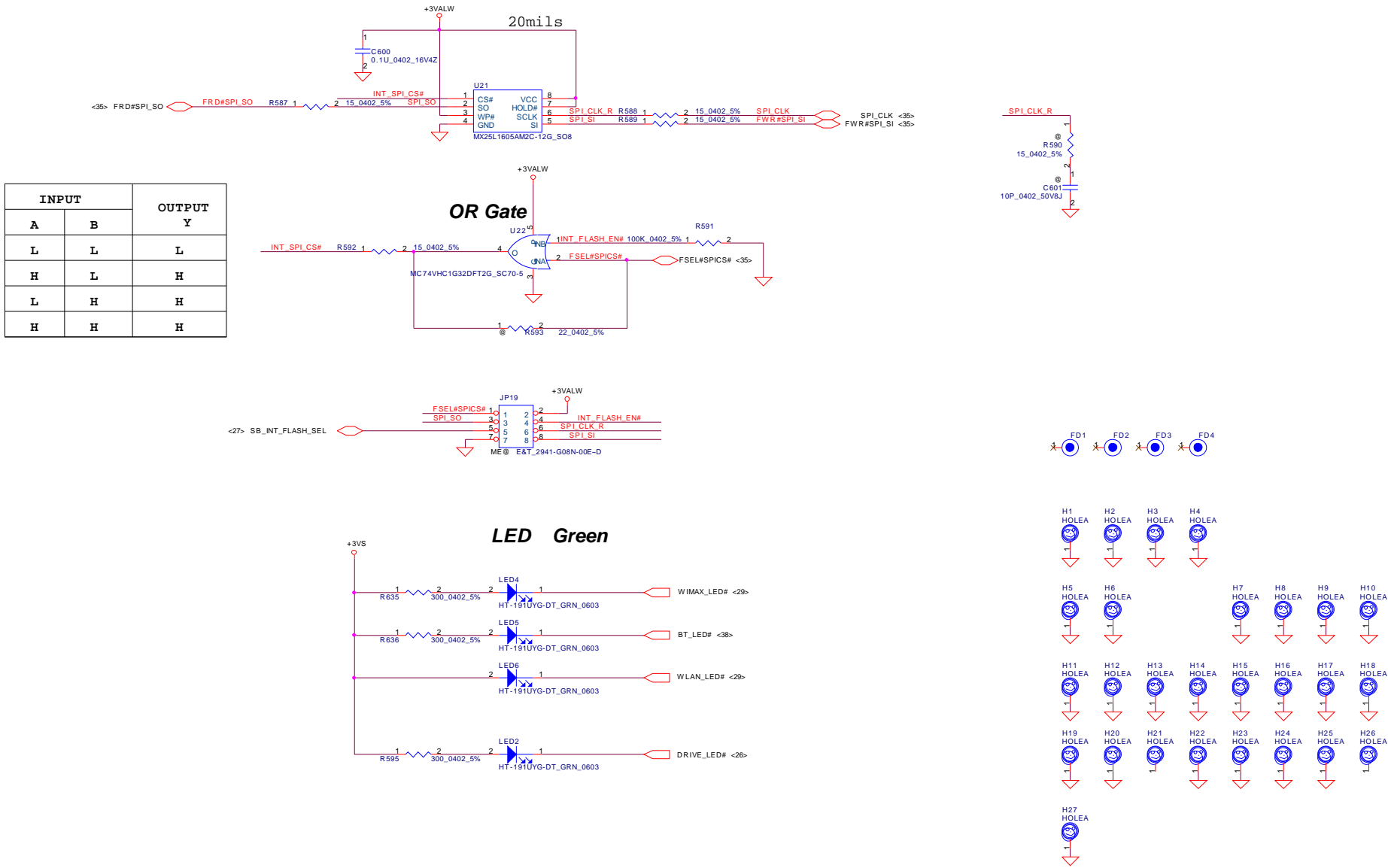
CONN PIN define need double check

FOR LPC SIO DEBUG PORT

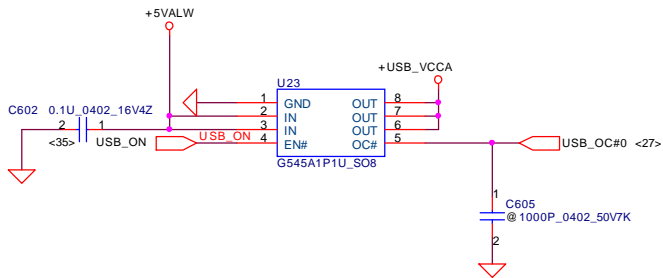


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Size	Document Number	JITR1_LA-4141P		Rev	
B				0.1	
Date:	Friday, June 27, 2008	Sheet	36	of	49

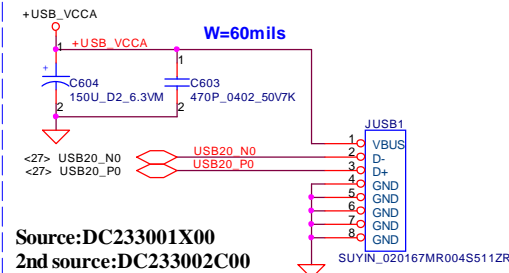
FOR EC 16M SPI ROM



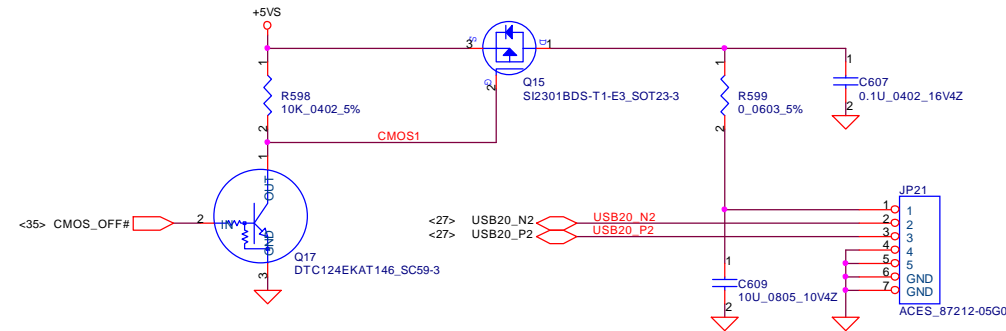
Security Classification	Compal Secret Data			Title		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	LED/EC SPI ROM		
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				Date:	Friday, June 27, 2008	Sheet 37 of 49



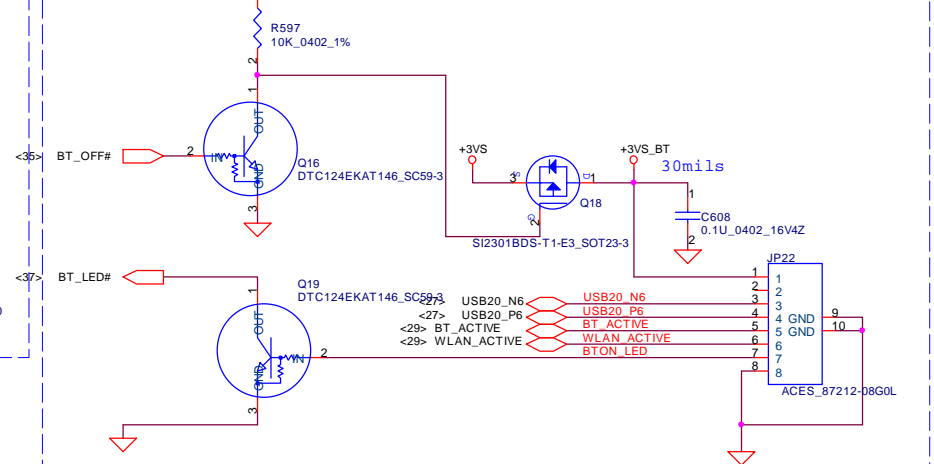
LIFT USB CONN. 1



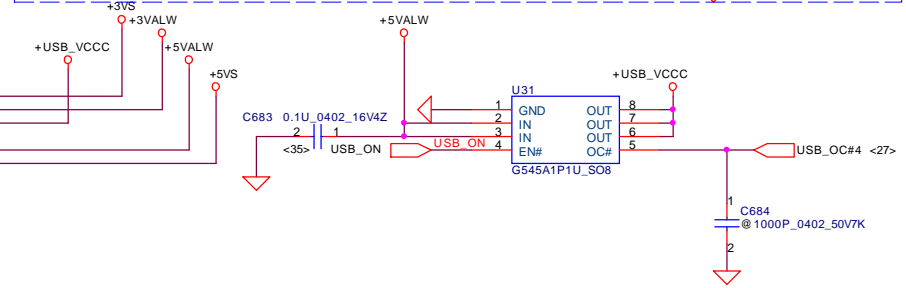
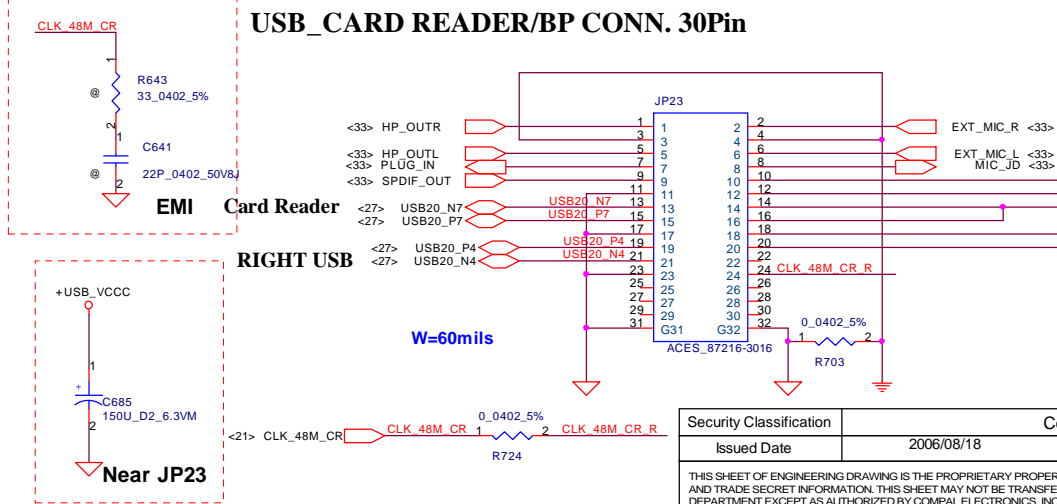
CMOS Camera Conn



BT MODULE CONN

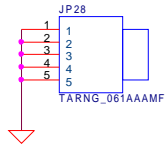


USB_CARD READER/BP CONN. 30Pin

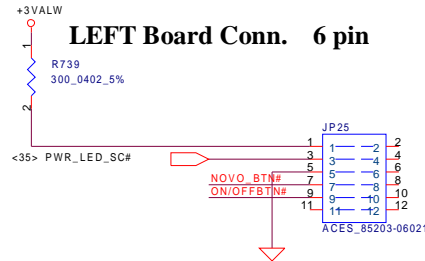


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Size		Document Number		Rev	
Custom		KIWB3/B4_LA4551P		0.1	
Date:		Friday, June 27, 2008		Sheet	
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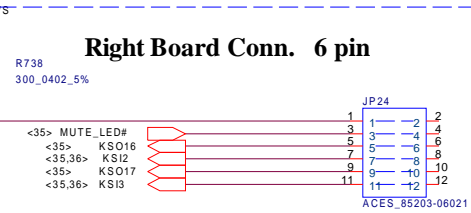
TV ANTENNA



LEFT Board Conn. 6 pin



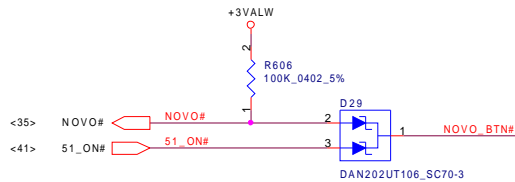
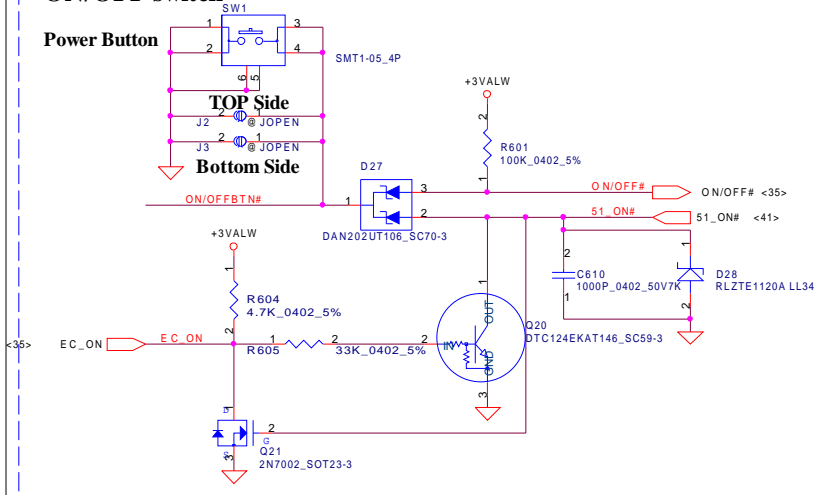
Right Board Conn. 6 pin



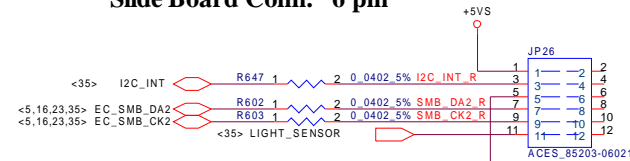
BTN FUNCTION	KEY MATRIX	
	IN	OUT
UP	KSO16	KSI2
DOWN	KSO17	KSI2
MUTE	KSO17	KSI3

ON/OFF switch

Power Button

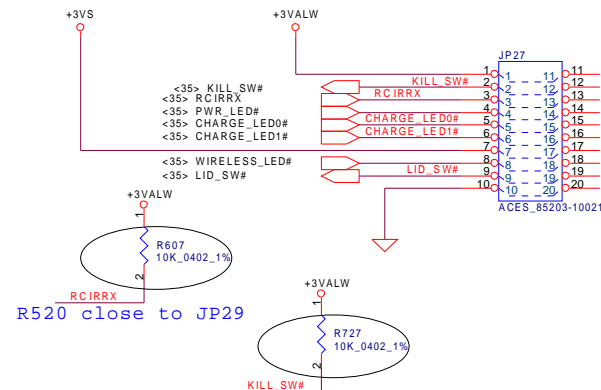


Slide Board Conn. 6 pin



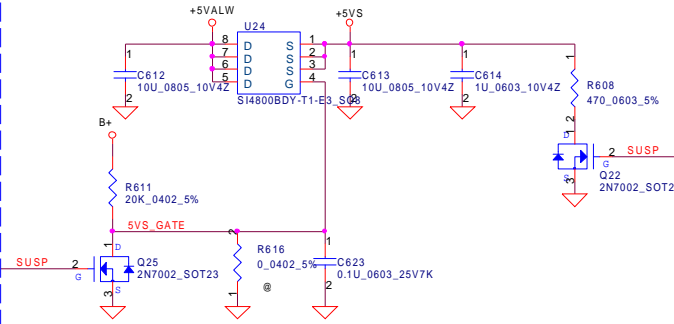
not be defined yet

CIRI Board Conn. 14 pin

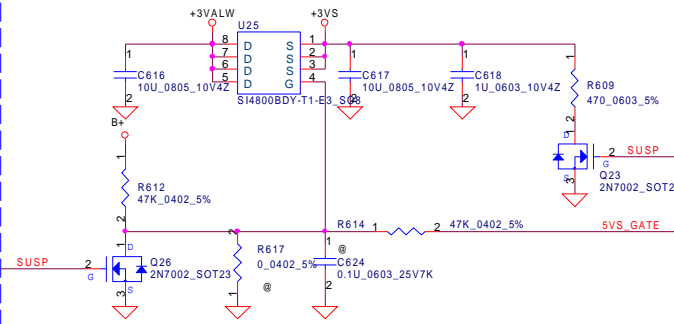


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Date: Friday, June 27, 2008				Size Custo
Sheet 39 of 49				Document Number KIWB3/B4_LA4551P Rev 0.1

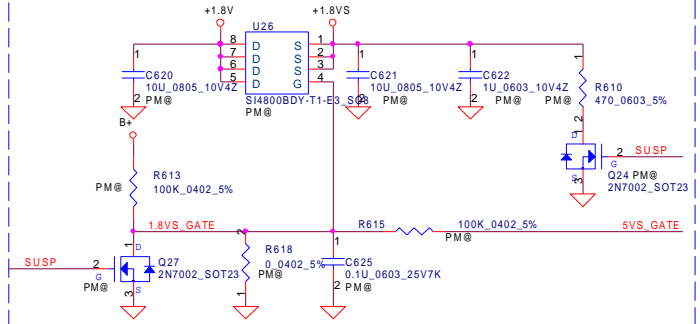
+5VALW TO +5VS



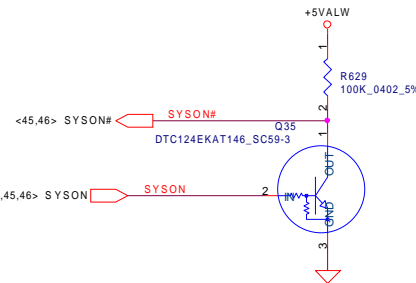
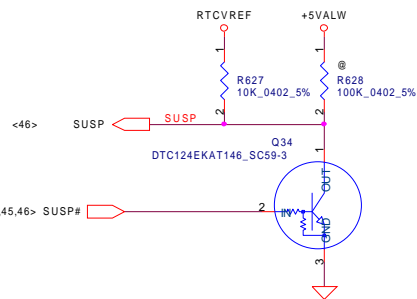
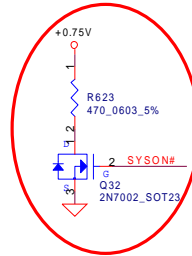
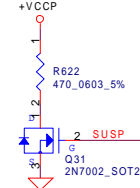
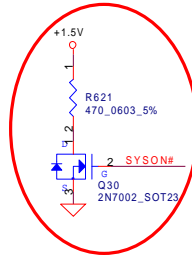
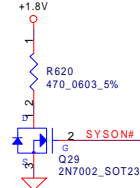
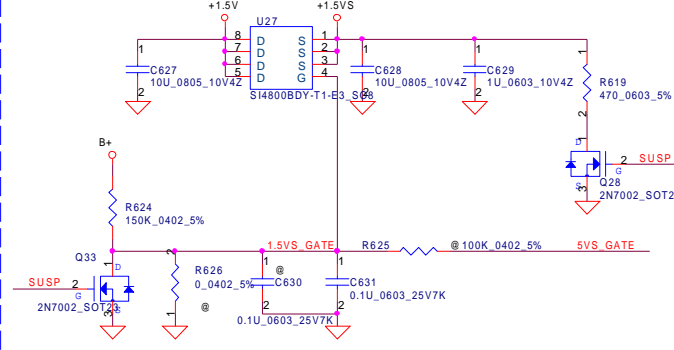
+3VALW TO +3VS



+1.8V to +1.8VS

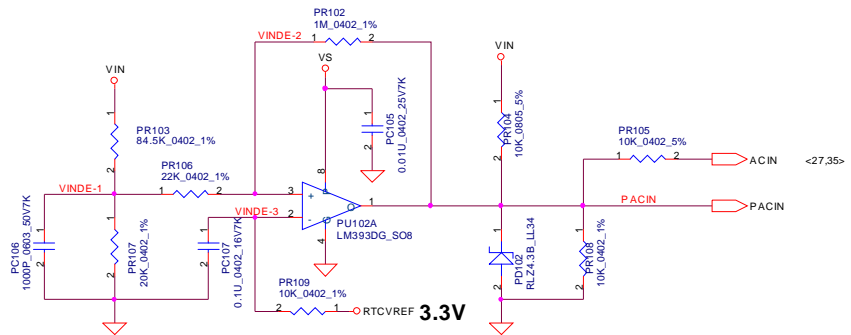
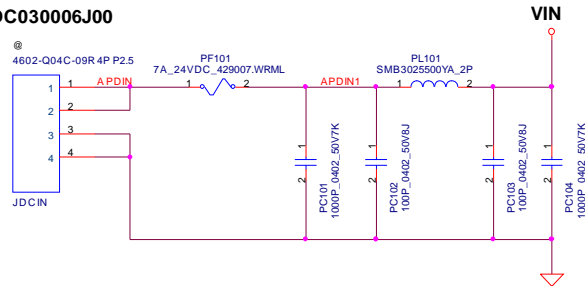


+1.5V to +1.5VS



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				Date	Friday, June 27, 2008
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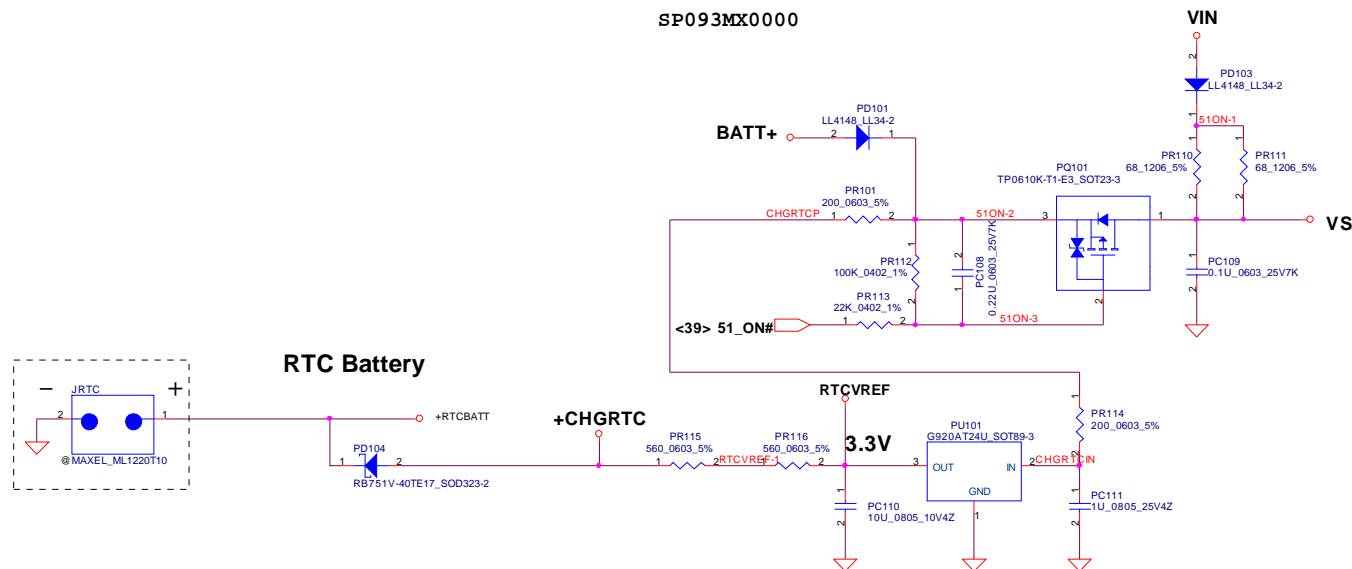
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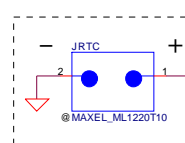
Vin Detector

High 18.384 17.901 17.430
Low 17.728 17.257 16.976

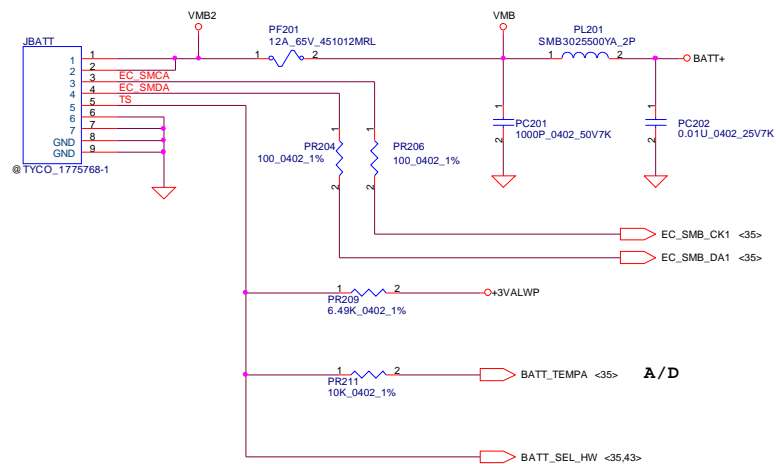
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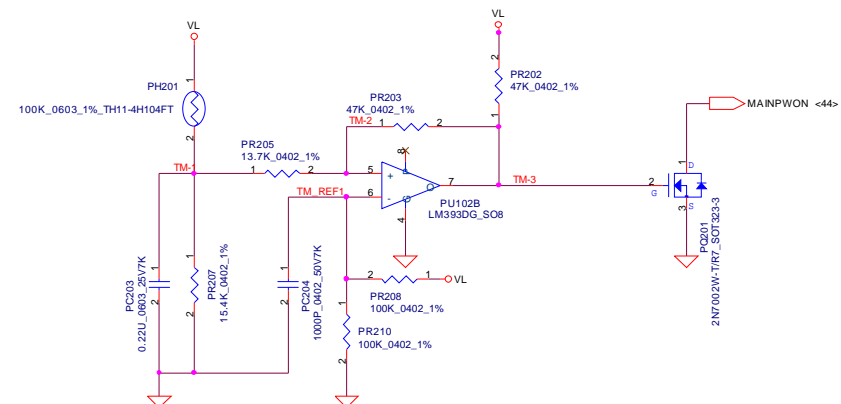
RTC Battery



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PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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1. ACDET
ACOV
CHG_PVCC
ACSET
ACOP/IADP
ACGOOD#
2. BATT_OVP
BATT_CELL
CHG_VOLT
CHG_CURT
BATT_LEARN

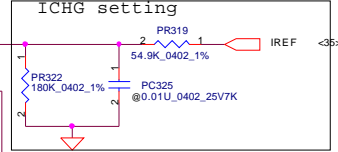
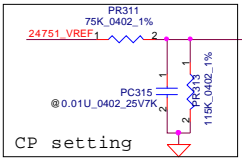
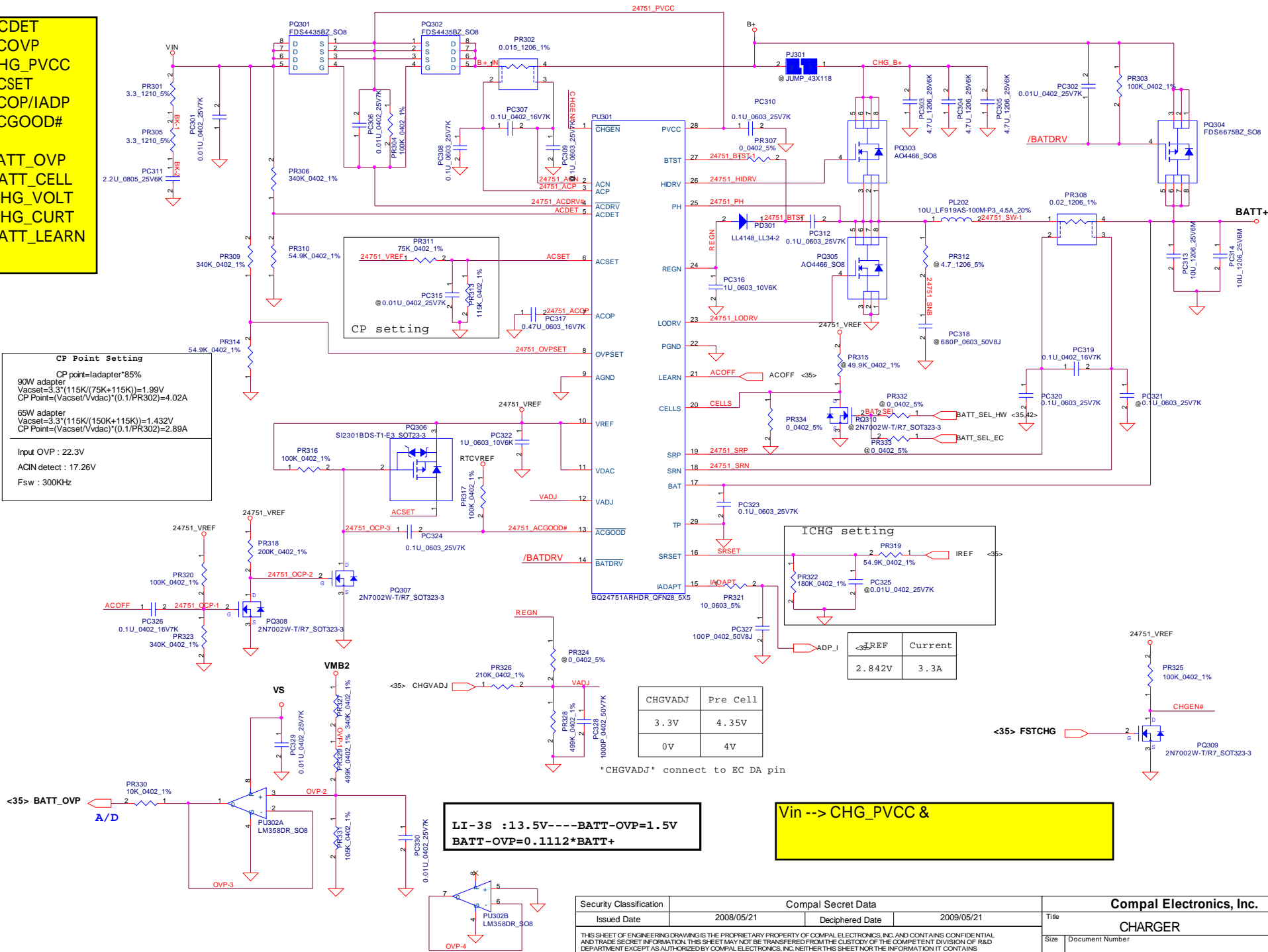
CP Point Setting

CP point=ladapter*85%

90W adapter
Vacset=3.3*(115K/(75K+115K))=1.99V
CP Point=(Vacset/Vvdac)*(0.1/PR302)=4.02A

65W adapter
Vacset=3.3*(115K/(150K+115K))=1.432V
CP Point=(Vacset/Vvdac)*(0.1/PR302)=2.89A

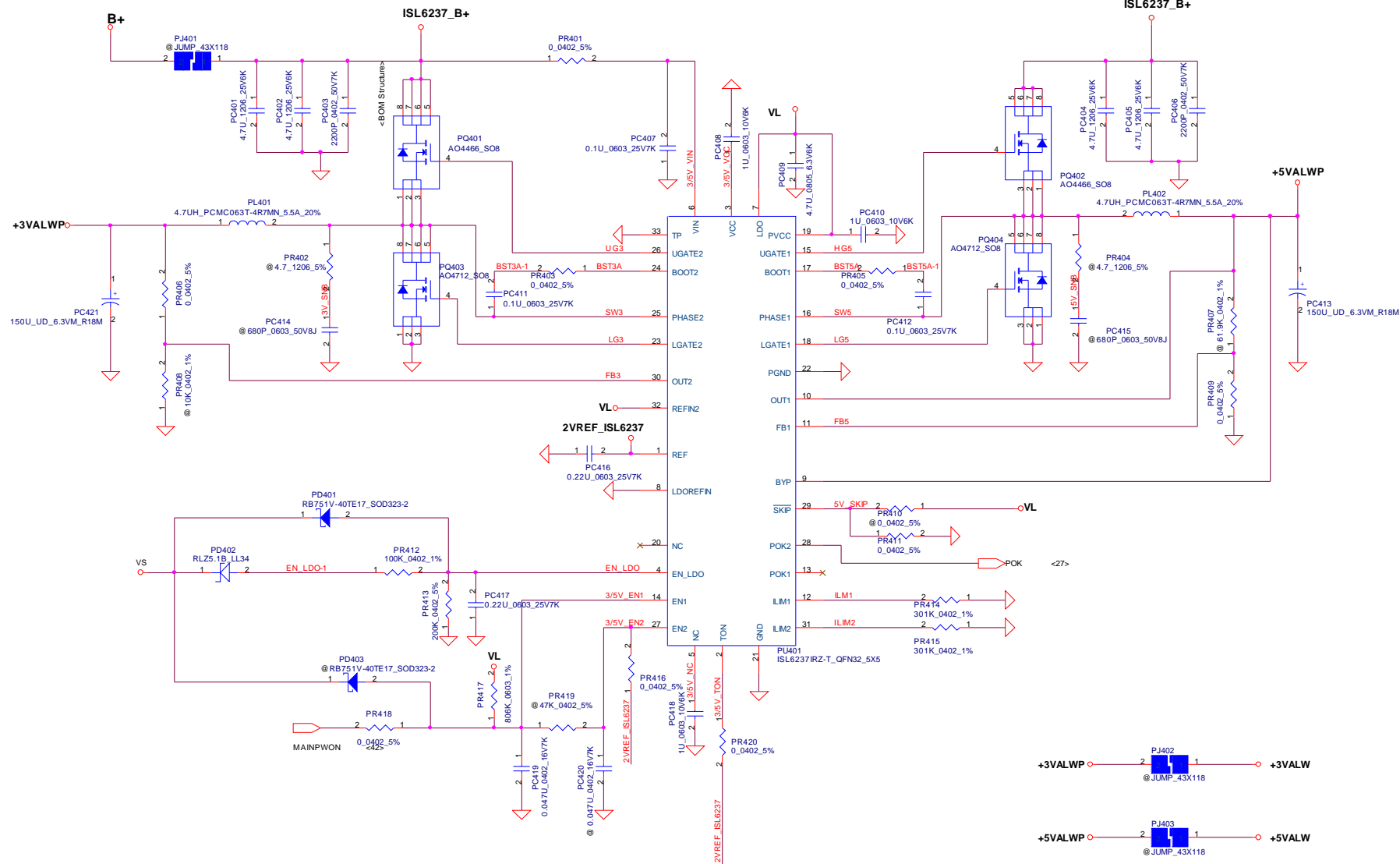
Input OVP : 22.3V
ACIN detect : 17.26V
Fsw : 300KHz



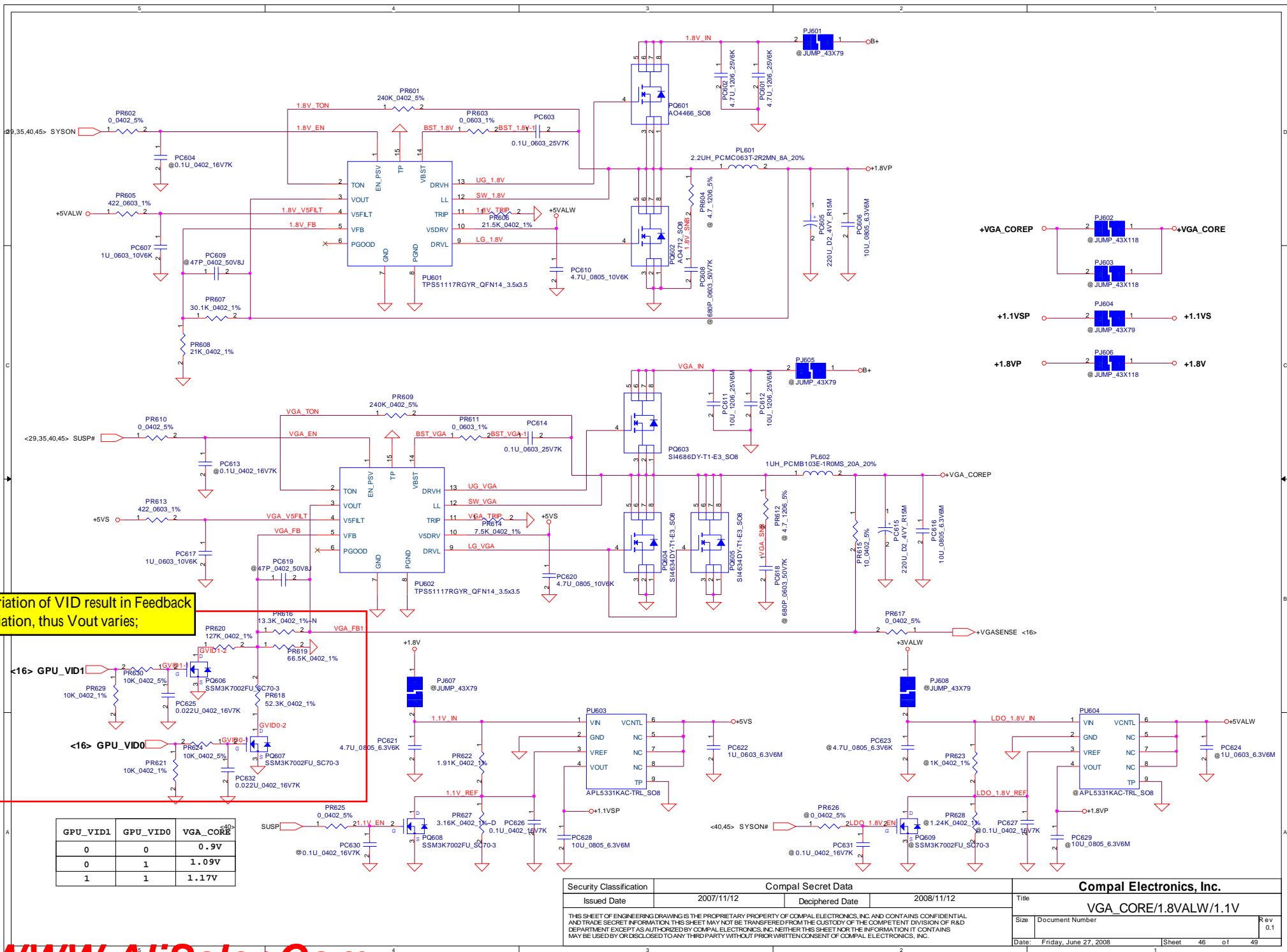
CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+

Vin --> CHG_PVCC &



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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Schematic modify	0.1	41 43 46 47	Add PR334,PR861,PR862,PR863PR864 Canel PH802 Change PR841,PR846 to 0ohm Change PC831 to 10U Change PR840,PR850 to 194K Change PR801,PR848 to 15.4K Change PR842,PR851 to 28.7K Change PC106 to 1000P Change PC829,PC835 to 0.022U Change PR622 to 1.91K Change PR627 to 3.16K Change PR628 to 1.24K PU401 main source change to TPS51427		EVT
2							
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					Security Classification	Compal Secret Data	
					Issued Date	2007/09/20	Deciphered Date 2008/09/20
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					Compal Electronics, Inc.		
					PIR (PWR)		

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