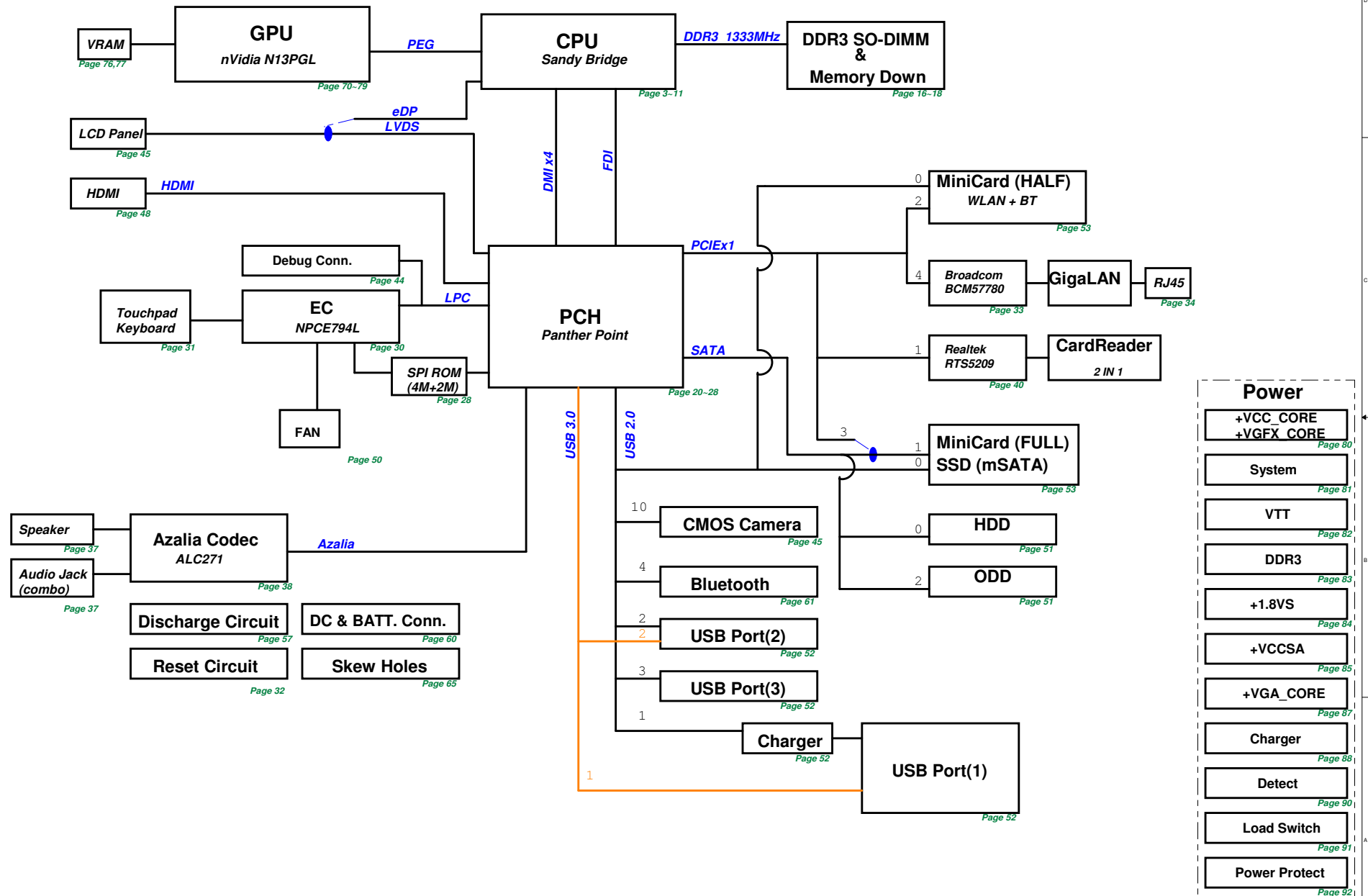


MA50 Ultrabook Block Diagram Rev 1.0



PCH_CPT
GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00				
GPIO 01				
GPIO [2:5]				
GPIO 06				
GPIO 07				
GPIO 08				
GPIO 09				
GPIO 10				
GPIO 11				
GPIO 12				
GPIO 13				
GPIO 14				
GPIO 15				
GPIO 16				
GPIO 17				
GPIO 18				
GPIO 19				
GPIO 20				
GPIO 21				
GPIO 22				
GPIO 23				
GPIO 24				
GPIO 25				
GPIO 26				
GPIO 27				
GPIO 28				
GPIO 29				
GPIO 30				
GPIO 31				
GPIO 32				
GPIO 33				
GPIO 34				
GPIO 35				
GPIO 36				
GPIO 37				
GPIO 38				
GPIO 39				
GPIO 40				
GPIO 41				
GPIO 42				
GPIO 43				
GPIO 44				
GPIO 45				
GPIO 46				
GPIO 47				
GPIO 48				
GPIO 49				
GPIO 50				
GPIO 51				
GPIO 52				
GPIO 53				
GPIO 54				
GPIO 55				
GPIO 56				
GPIO 57				
GPIO 58				
GPIO 59				
GPIO 60				
GPIO 61				
GPIO 62				
GPIO 63				
GPIO 64				
GPIO 65				
GPIO 66				
GPIO 67				
GPIO 72				
GPIO 73				
GPIO 74				
GPIO 75				

WWW.AliSaler.Com

EC
NPCE795L

EC GPIO	Use As	Signal Name
GPA0		
GPA1		
GPA2		
GPA3		
GPA4		
GPA5		
GPA6		
GPA7		
GPB0		
GPB1		
GPB2		
GPB3		
GPB4		
GPB5		
GPB6		
GPB7		
GPC0		
GPC1		
GPC2		
GPC3		
GPC4		
GPC5		
GPC6		
GPC7		
GPD0		
GPD1		
GPD2		
GPD3		
GPD4		
GPD5		
GPD6		
GPD7		
GPE0		
GPE1		
GPE2		
GPE3		
GPE4		
GPE5		
GPE6		
GPE7		
GPF0		
GPF1		
GPF2		
GPF3		
GPF4		
GPF5		
GPF6		
GPF7		
PGP0		
PGP1		
PGP2		
PGP6		
GPH0		
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GPH2		
GPH3		
GPH4		
GPH5		
GPH6		
GPI0		
GPI1		
GPI2		
GPI3		
GPI4		
GPI5		
GPI6		
GPI7		
GPJ0		
GPJ1		
GPJ2		
GPJ3		
GPJ4		
GPJ5		

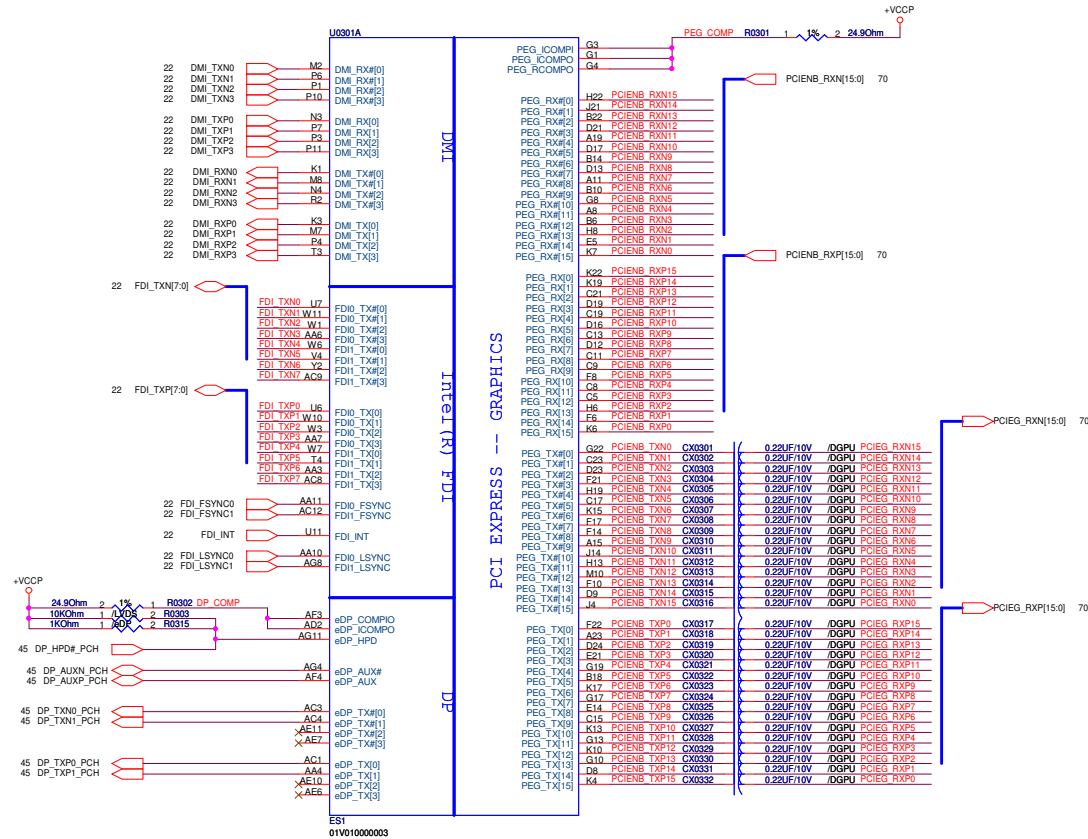
SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB 3.0 Port (3)
USB 3	USB Port (4)
USB 4	N/A
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	Card Reader
USB 11	N/A
USB 12	N/A
USB 13	N/A

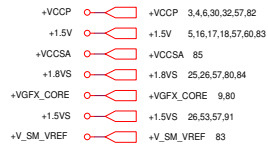
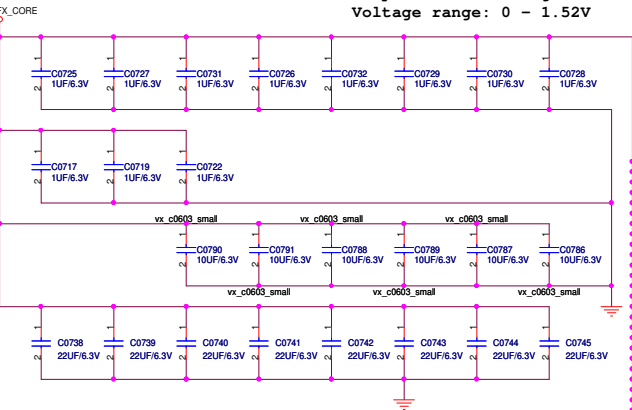


Decoupling guide from Intel PDDG R0.8

+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 6pcs

+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 8pcs(power request)

Graphics core voltage
Voltage range: 0 - 1.52V



DDR3 Reference Voltage

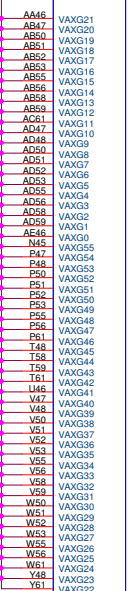
+1.5VS_VCCDDQ R1.1 add S3 power reduction

+V_SM_VREF 10mV

DDR3 - 1.5V RAILS

POWER

GRAPHICS



SM_VREF

AY43

-V SM_VREF

+V_SM_VREF

MAX: 5A

vx_c0603_small

vx_c0603_small

vx_c0603_small

vx_c0603_small

vx_c0603_small

vx_c0603_small

vx_c0603_small

vx_c0603_small

vx_c0603_small

vx_c0603_small

vx_c0603_small

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vx_c0603_small

vx_c0603_small

vx_c0603_small

vx_c0603_small

Processor I/O supply
voltage for DDR3
(DC + AC specification)

+1.5VS_VCCDDQ

ICCMAX_VDDQ 5A

JP0701

@ 9MM_OPEN_SML

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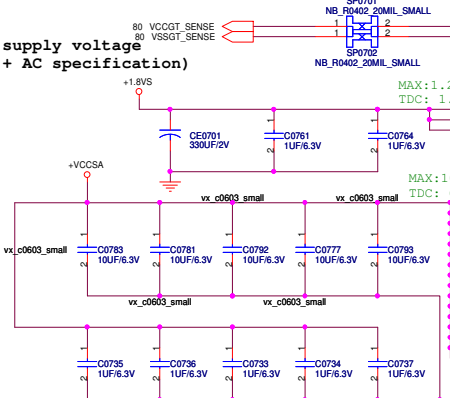
1

1

1

1

PLL supply voltage
(DC + AC specification)



Decoupling guide for A14 (EE)
+VCCSA
1uF * 5pcs
10uF * 5pcs

VAXG_SENSE

VSSAXG_SENSE

MAX: 1.2A

TDC: 1.2A

BB3

BC1

BC4

MAX: 10A

TDC: 6A

L17

N16

VCCSA15

VCCSA14

VCCSA13

VCCSA12

N20

VCCSA11

VCCSA10

VCCSA9

VCCSA8

VCCSA7

VCCSA6

VCCSA5

VCCSA4

VCCSA3

VCCSA2

VCCSA1

VCCSA0

W20

W19

W18

W17

W16

W15

W14

W13

W12

W11

W10

W9

W8

W7

W6

W5

W4

W3

W2

W1

W0

W-1

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W-106

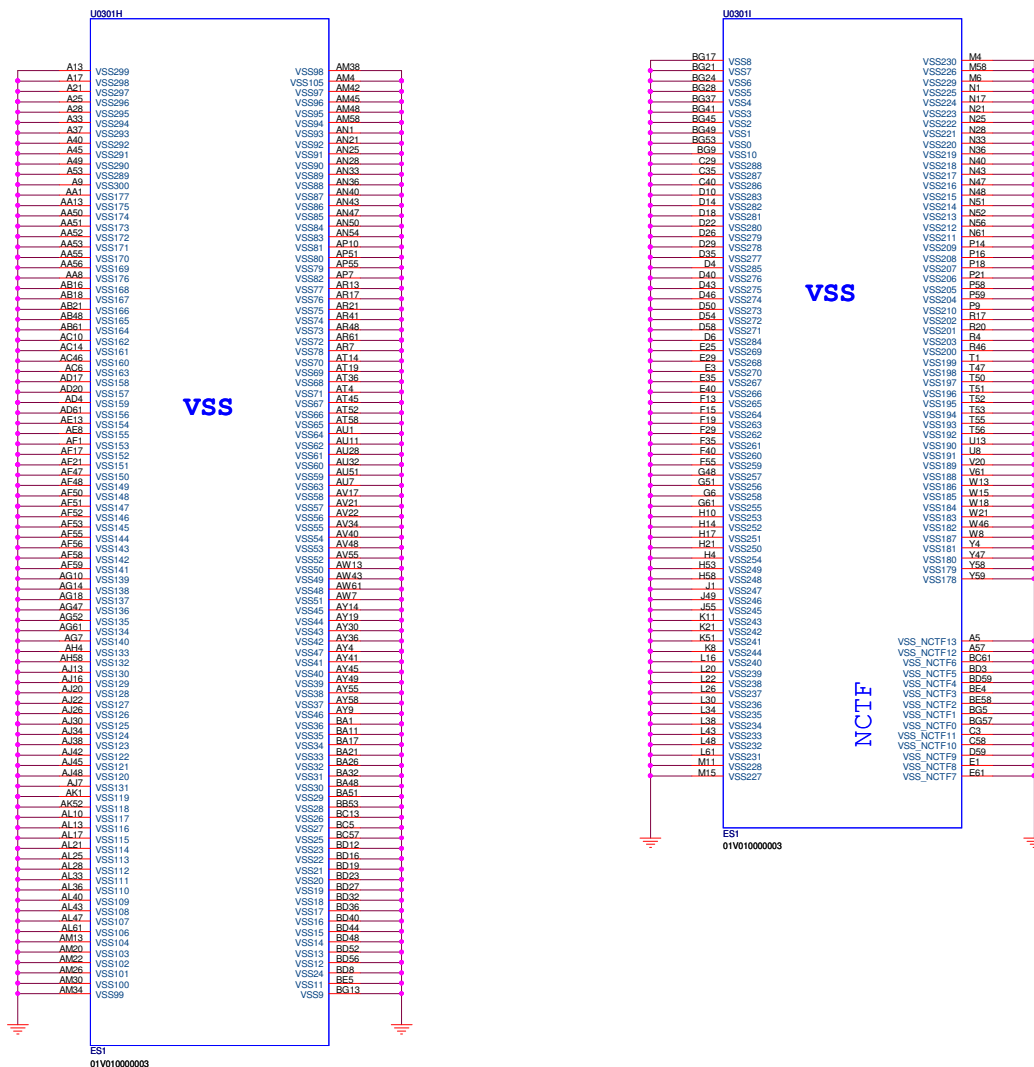
W-107

W-108

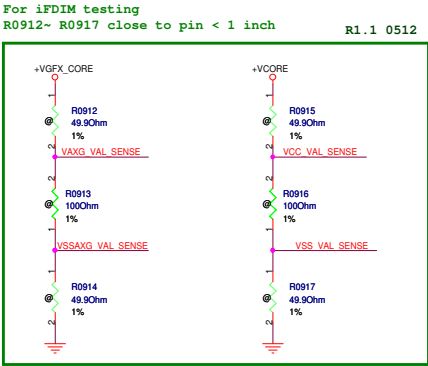
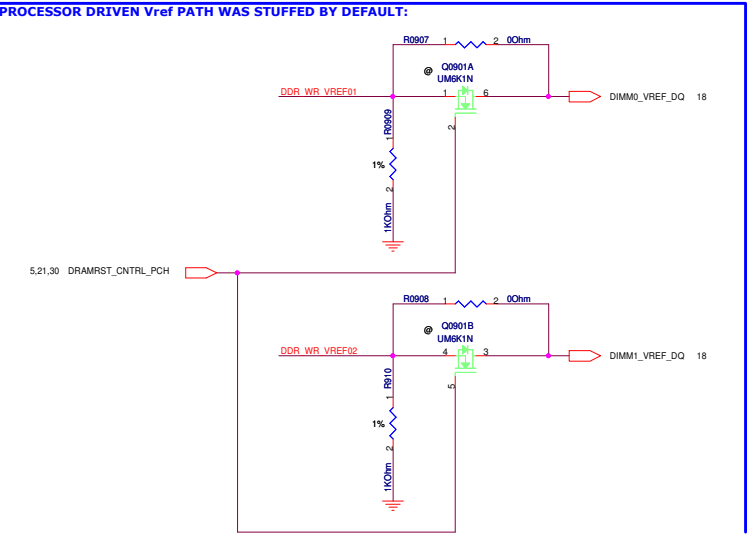
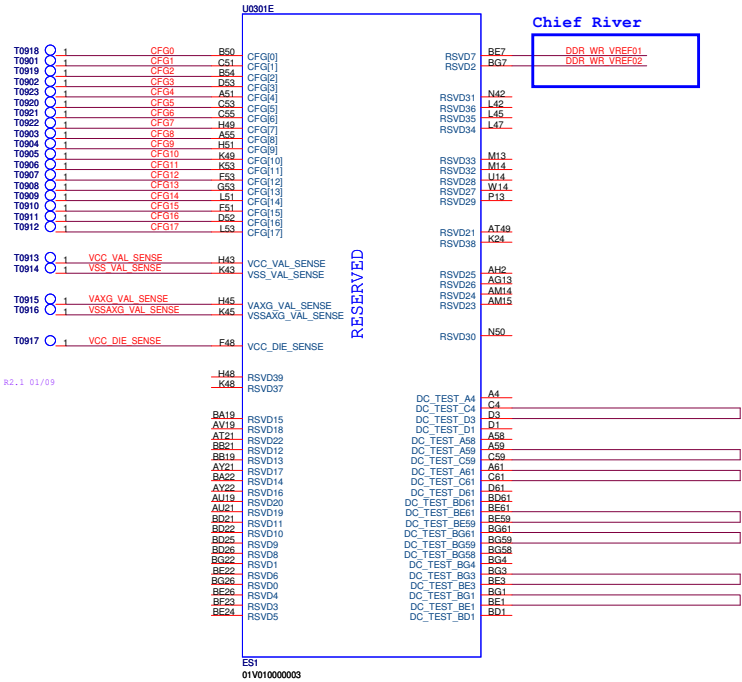
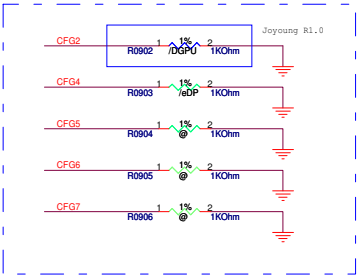
W-109

W-110

W-111



CFG strapping information:
CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x - 1: (Default) Normal Operation, Lane # definition matches socket pin map definition - 0: Lane Numbers Reversed
CFG[4]: Embedded DisplayPort Detection - 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort - 0: Enabled ; An external Display Port device is connected to the Embedded Display Port
CFG[6:5]: PCI Express Port Bifurcation Straps - 11 : (Default) x 1 6 - 10 : x 8 , x 8 - 01 : Reserved - 00 : x 8 , x 4 , x 4
CFG[7]: PEG DEFER TRAINING - 1: (Default) PEG Train immediately following xxRESETB de assertion - 0: PEG Wait for BIOS training



CPU XDP connector

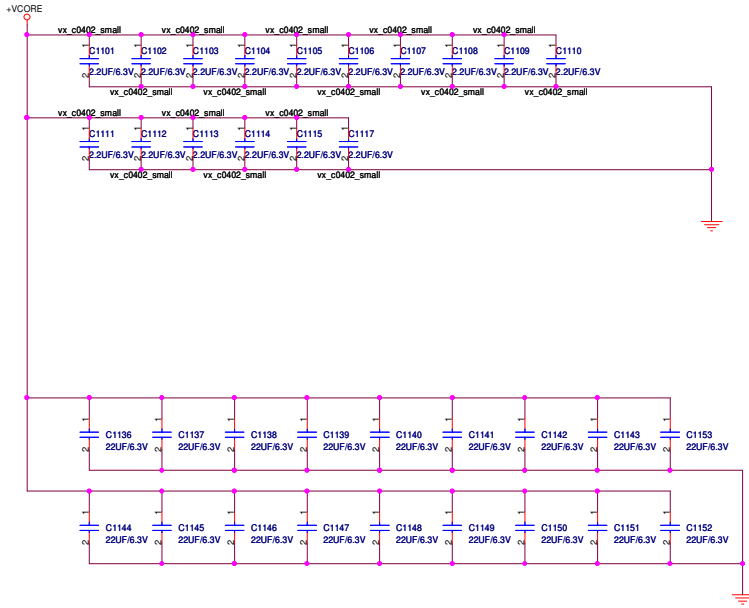
Check Connector

PCH XDP connector

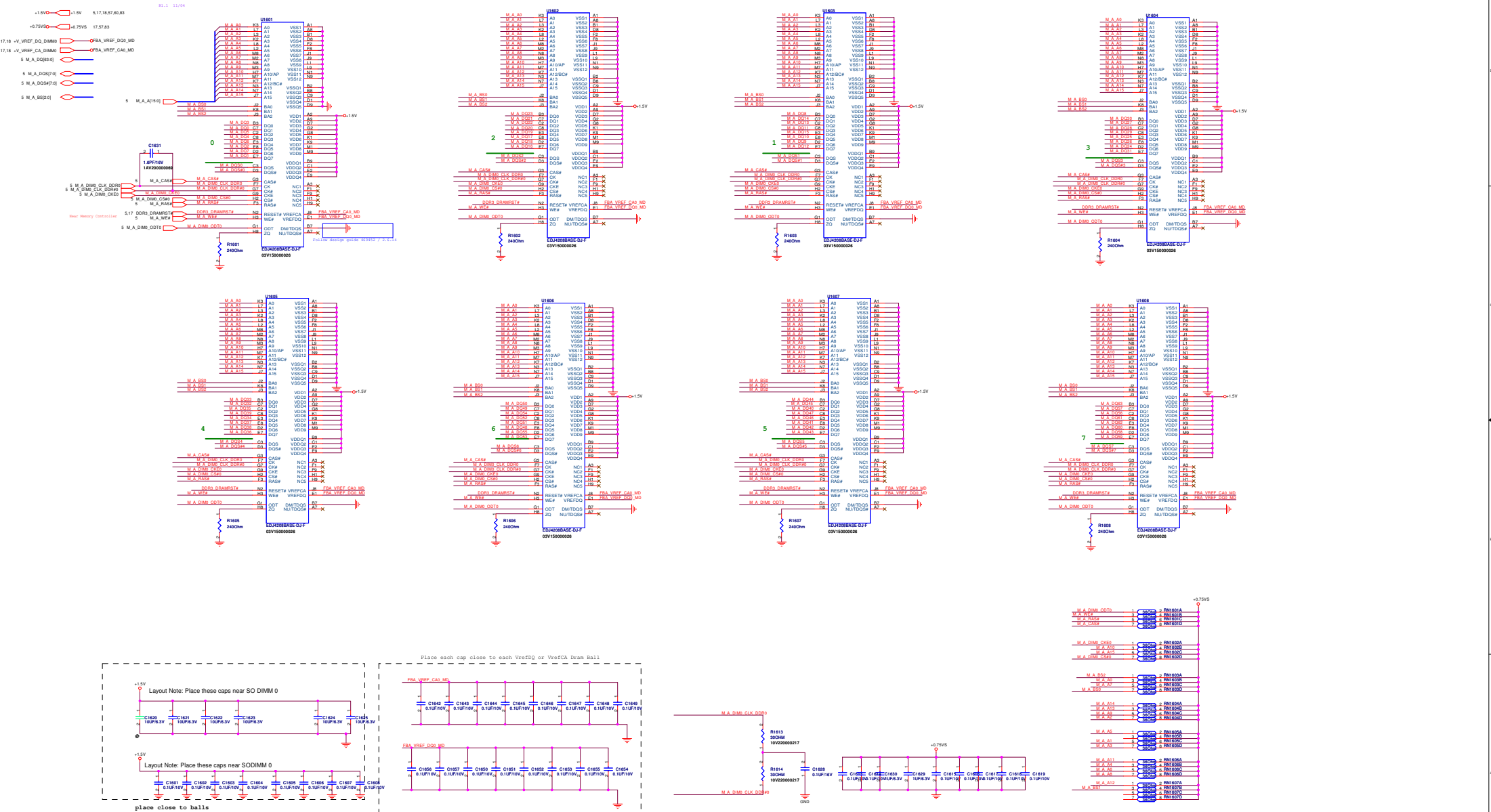
PEGATRON		Title : CPU_PCH_XDP	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
Custom	MA50		1.0
Date: Monday, February 13, 2012		Sheet	10 of 93

Chief River
Decoupling guide from Intel PDDG R0.8
+VCORE 2.2uF * 16 pcs
22uF * 12 pcs

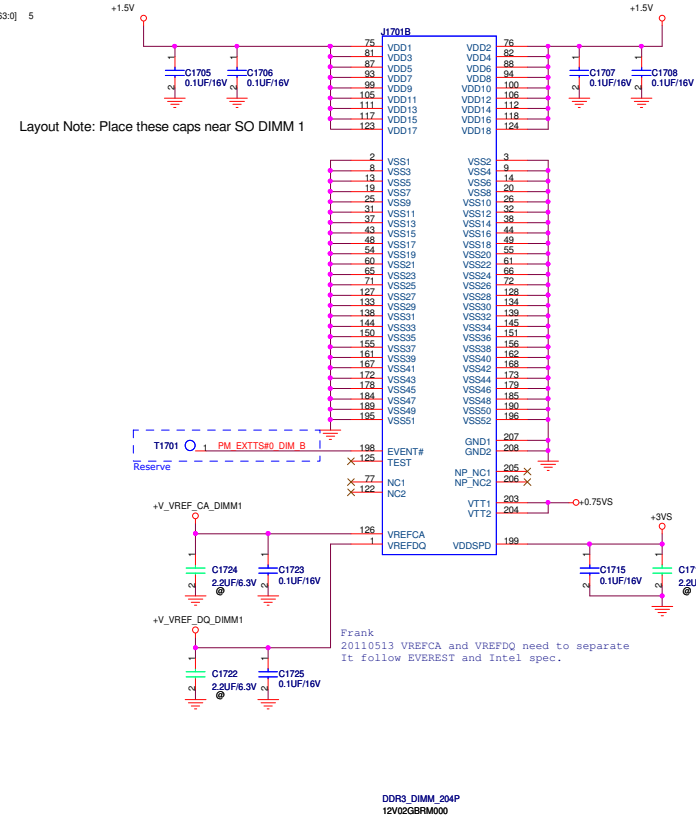
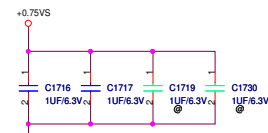
Chief River
+VCORE 2.2uF * 16 pcs
22uF * 18 pcs (power request)



Memory Down CH A

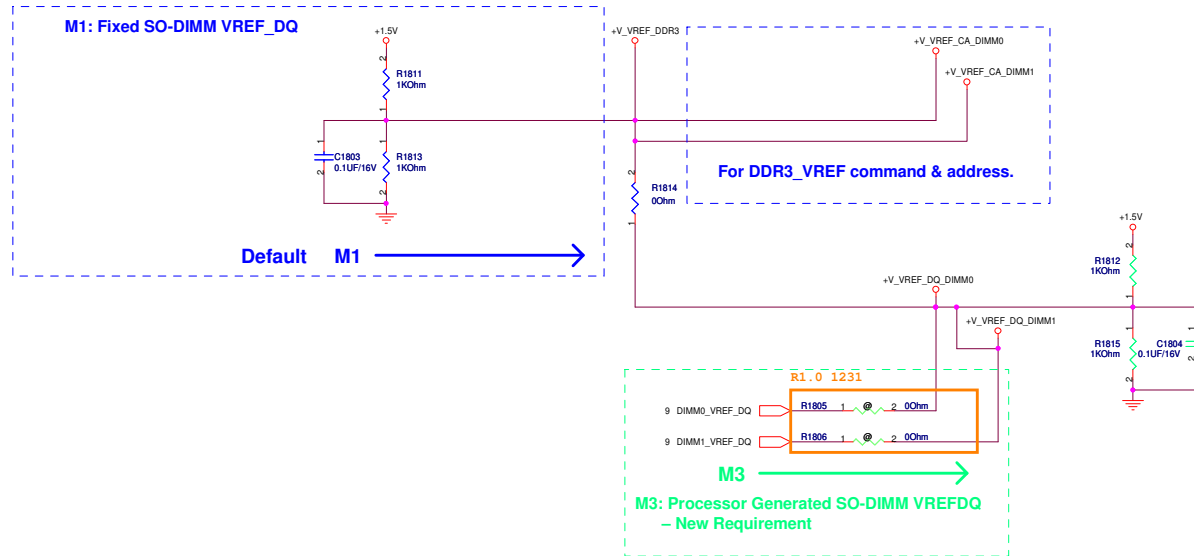


PAGATRON Title : DOR3(U) SO-DIMM	
Rev : 1	Engineer : Joyung Chhang
Date : 2019.12.10	
Page : 10 of 10	



PEGATRON		Title : <u>DDR3(2)_SO-DIMM1</u>	
PEGATRON COMPUTER INC		Engineer: <u>Joyoung_Chianhg</u>	
Size C	Project Name MA50	Rev 1.0	
Date: <u>Monday, February 13, 2012</u>	Sheet <u>17</u> of <u>93</u>		

DDR3 Vref

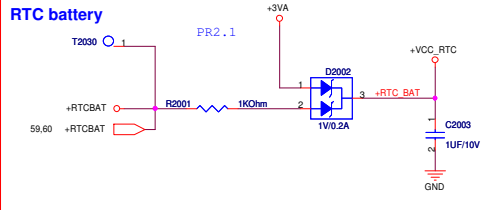


If support M3 :
 1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
 2. Un mount R1801,R1804

+1.5V 5,16,17,57,60,83
 +V_VREF_CA_DIMM0 16,17
 +V_VREF_DQ_DIMM0 16,17

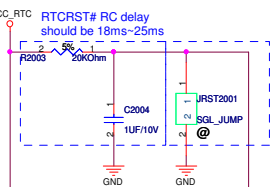
+3V 24,45,57,59,61,91
 +5VSUS 51,57,59,91
 +5VA 37,60,81,91

RTC battery

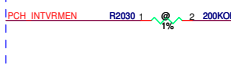


Request by CSC
for CMOS clear
function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)



INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High: Enable Internal VRs



TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

20110719 Frank
add C2006 for EMI request



Intel I:5 Design Guide, page 260

isolate schematic for ACZ_SYNC and SDOUT follow EIH31

R1.0
For JTAG to pull high and low.

Remove JTAG schematic

Strap information:

SB_SPKR: No reboot strap
Low: Disable (Default)
High: Enable

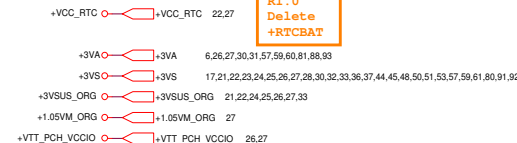
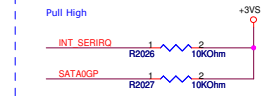
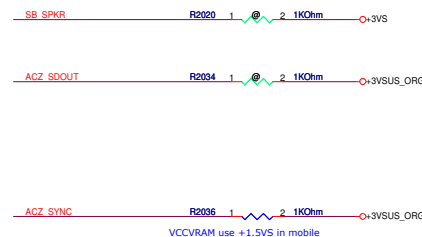
ACZ_SDOUT:

1. Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

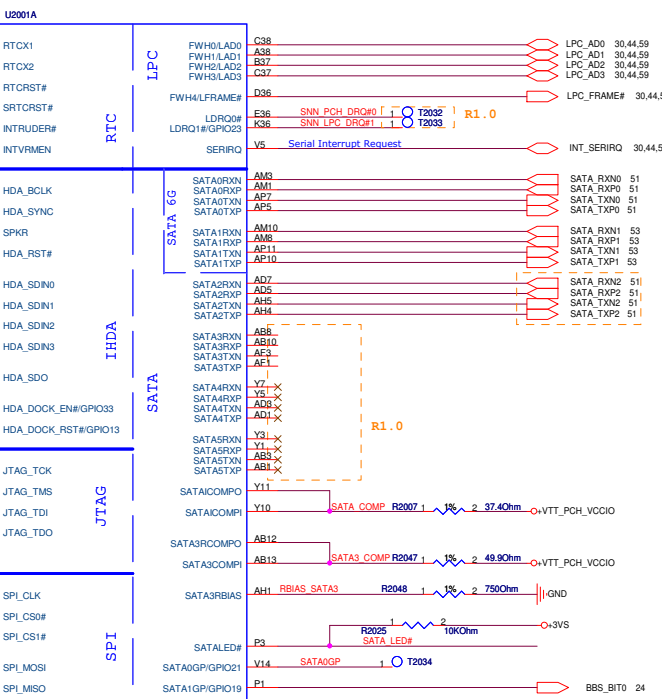
2. ACZ_SDOUT which sample high on the rising edge of PWROK
Will also disable Intel ME.

ACZ_SYNC: On Die PLL VR voltage selector

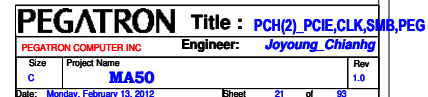
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hiron River Platform Schematic Design Checklist
(438390 page 48)

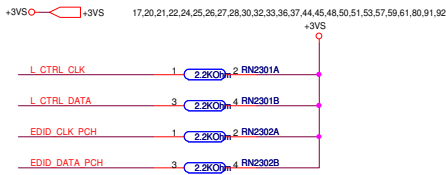


R1.0
Delete
+RTCBAT



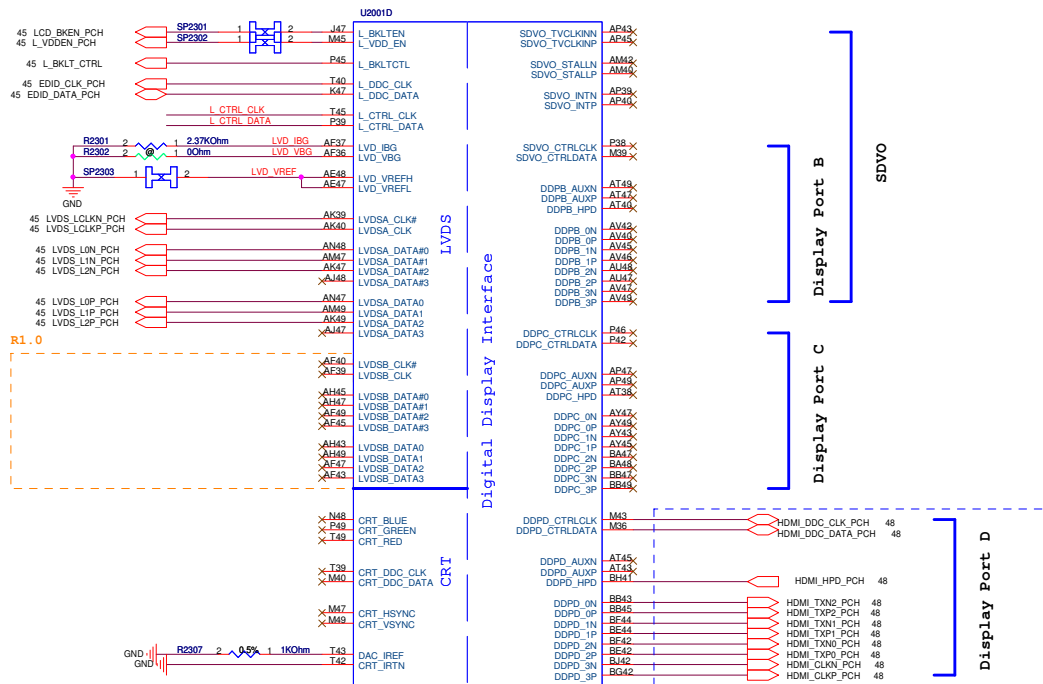
Frank
0517_Add 3G PCIE and CLKRQ in Port3.





Pull up 2.2k ohm in DDC bus for LVDS .

Remove LVDS net name and add port B.



CRT Disable: (For discrete graphic)

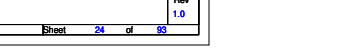
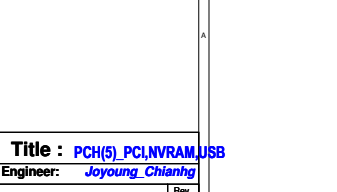
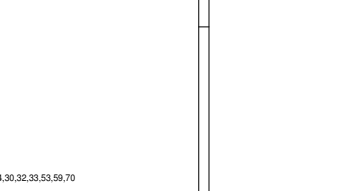
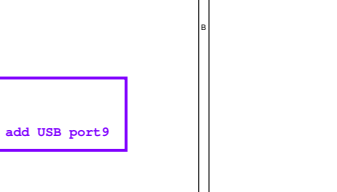
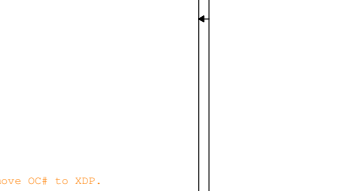
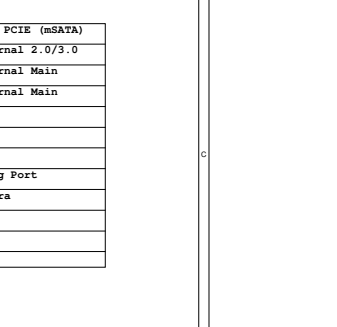
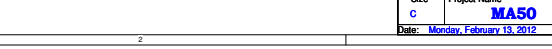
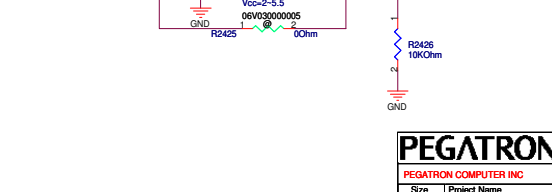
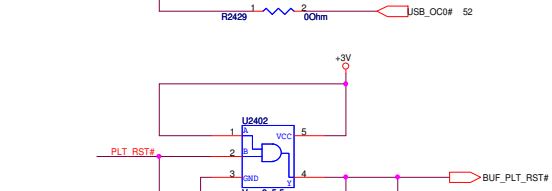
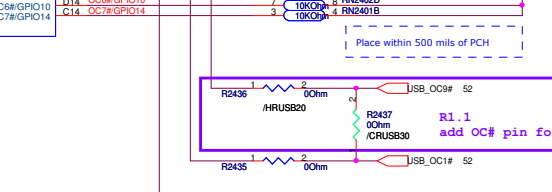
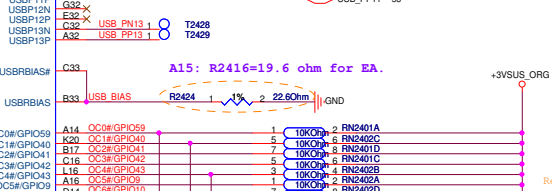
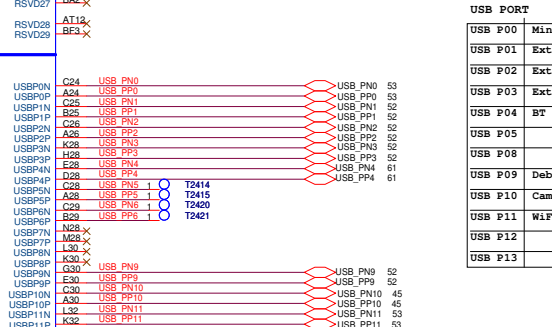
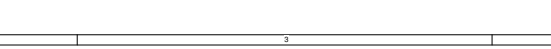
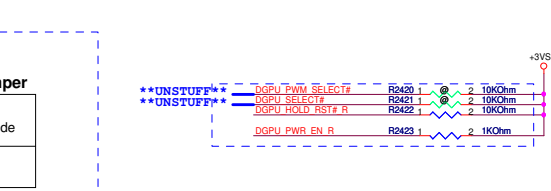
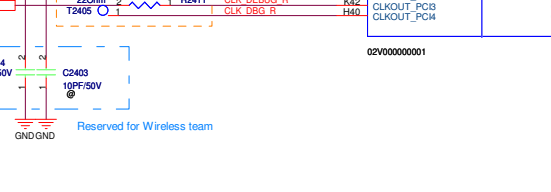
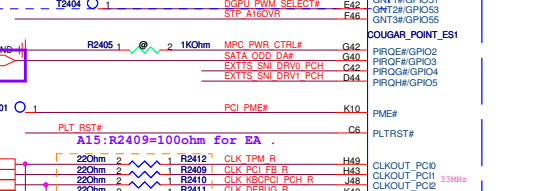
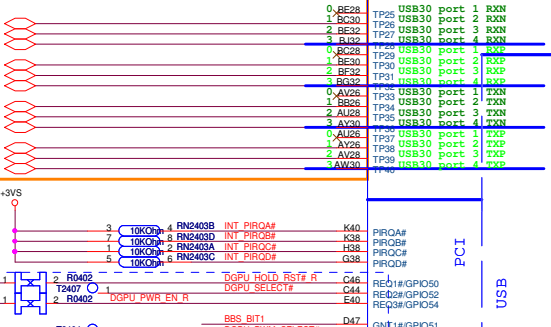
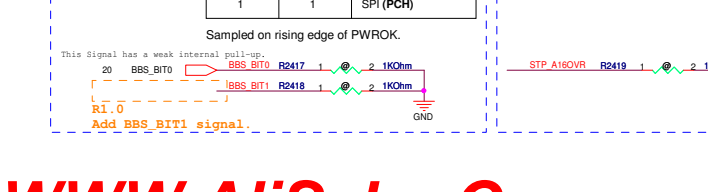
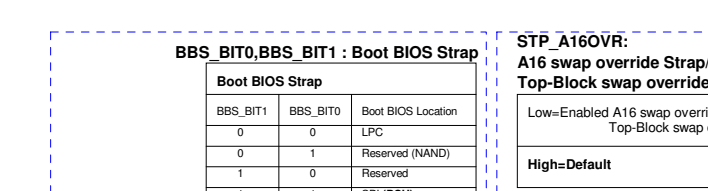
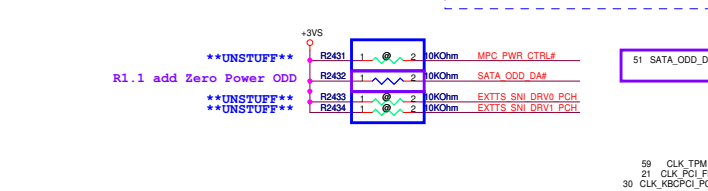
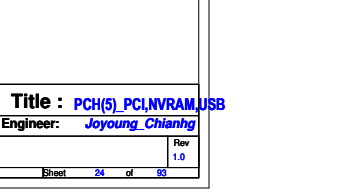
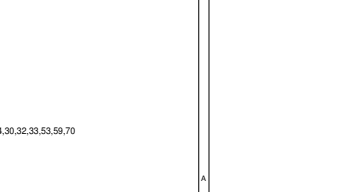
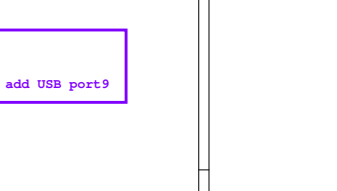
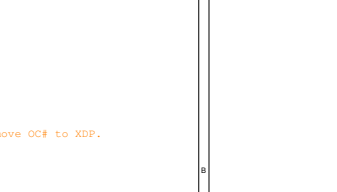
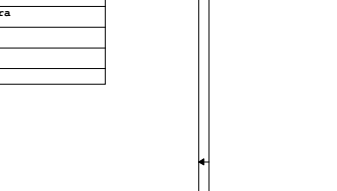
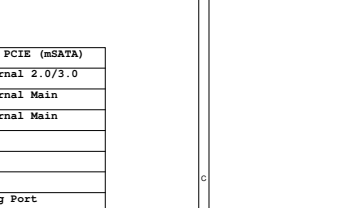
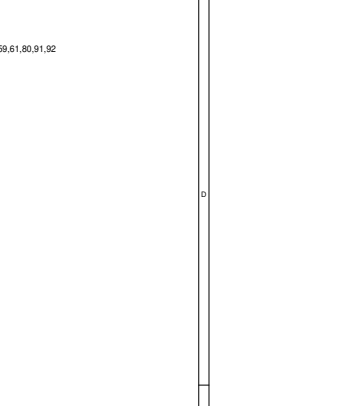
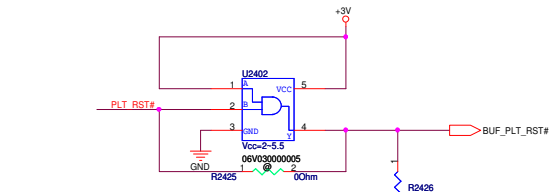
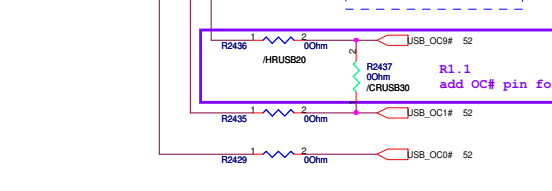
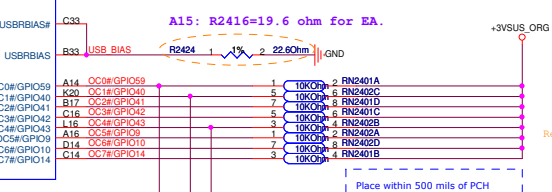
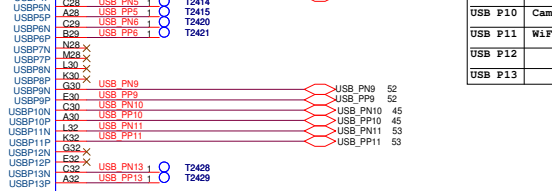
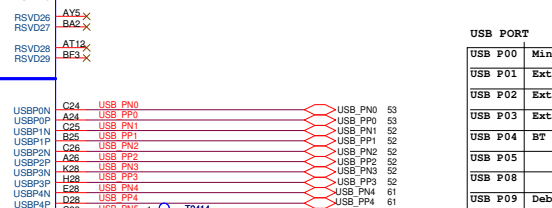
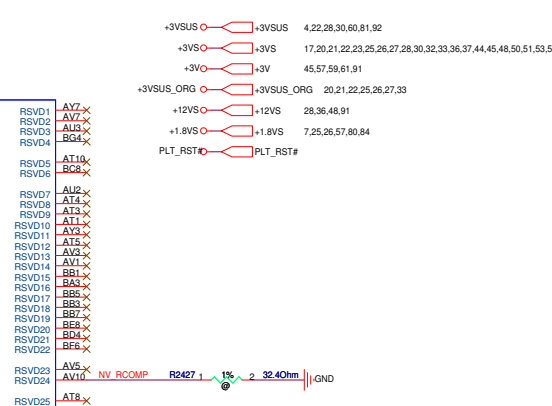
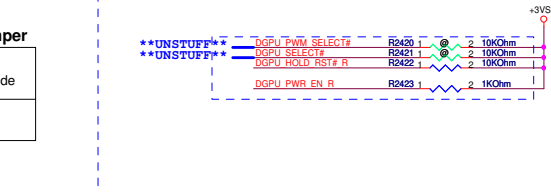
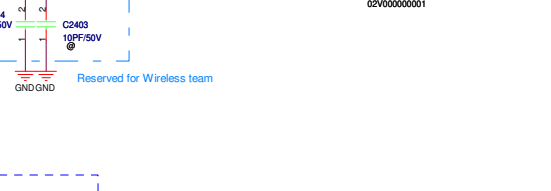
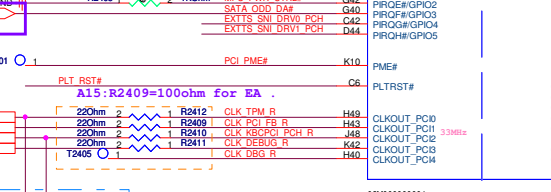
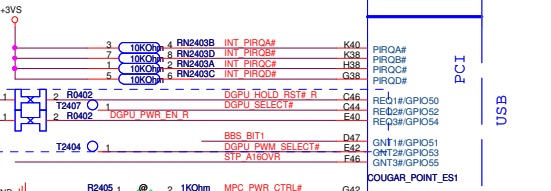
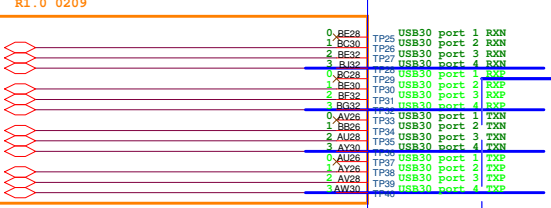
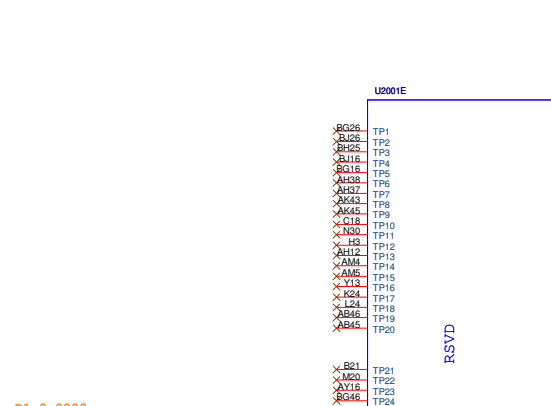
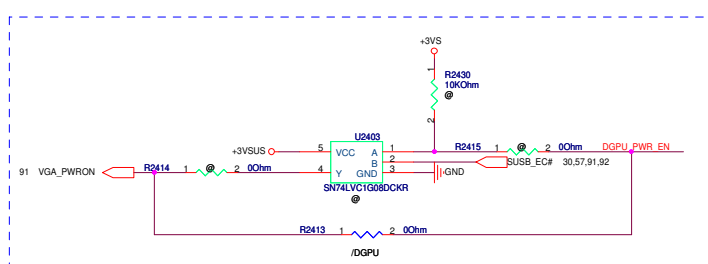
1. NC:
CRT_RED,CRT_GREEN,CRT_BLUE
CRT_HSYNC,CRT_VSYNC
2. 1-k Ω \pm 0.5% pull-down to GND:
DAC_IREF
3. Connected to GND:
CRT_ITRN
4. Connect to +V3.3:
VCCADAC

DisPlay Port Disable: (For discrete graphic)

1. NC:
ALL

LVDS Disable: (For discrete graphic)

1. NC:
LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
LVD_VREFL, LVD_IBG, LVD_VBG
2. Connected to GND:
VccALVDS,VccTX_LVDS



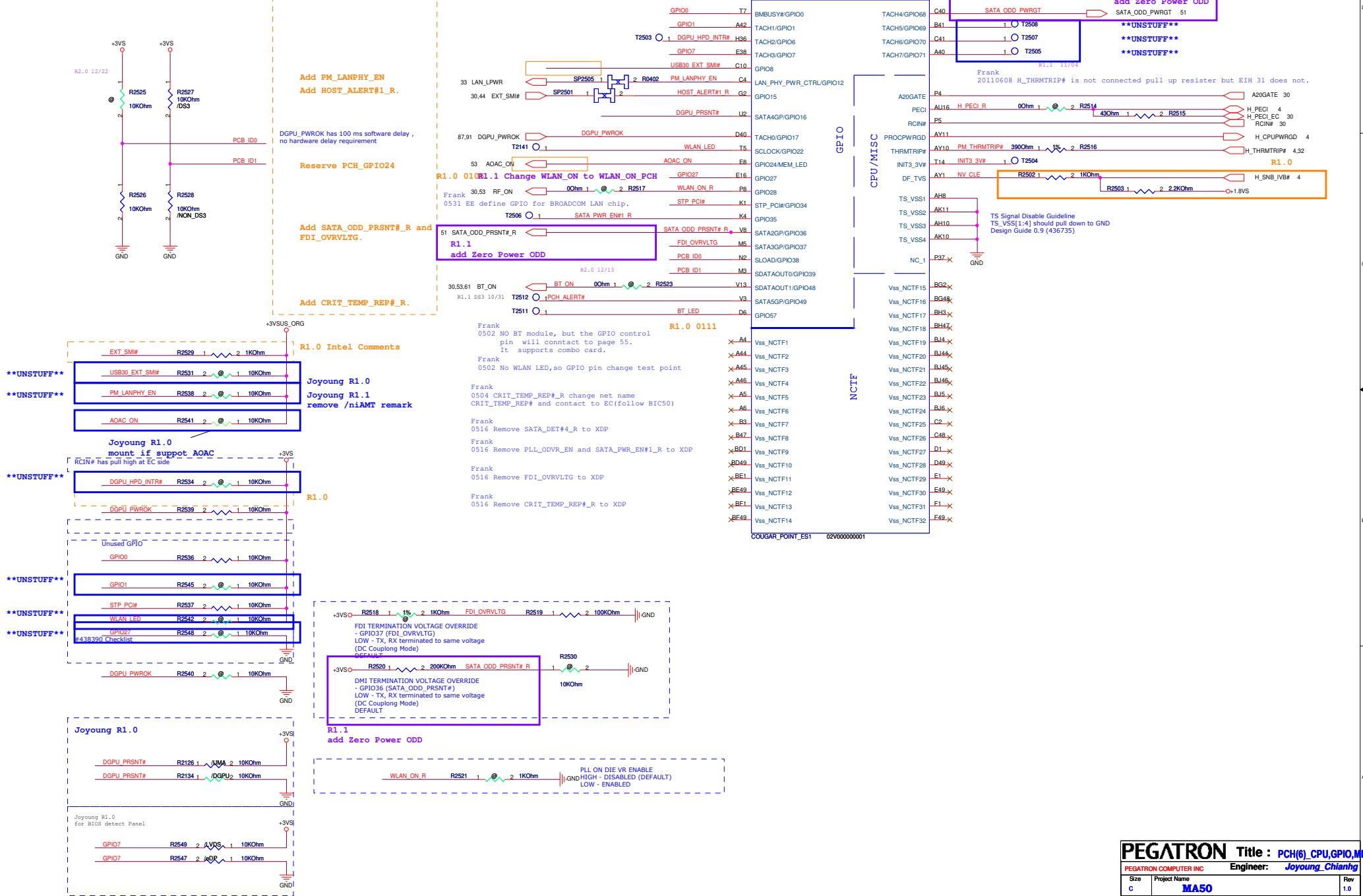
+3VSUS_O -> +3VSUS_O 17,20,21,22,23,24,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+3VSUS_O -> +3VSUS_O 4,22,24,28,30,60,81,92
+3VSUS_ORG_O -> +3VSUS_ORG_O 20,21,22,24,26,27,33

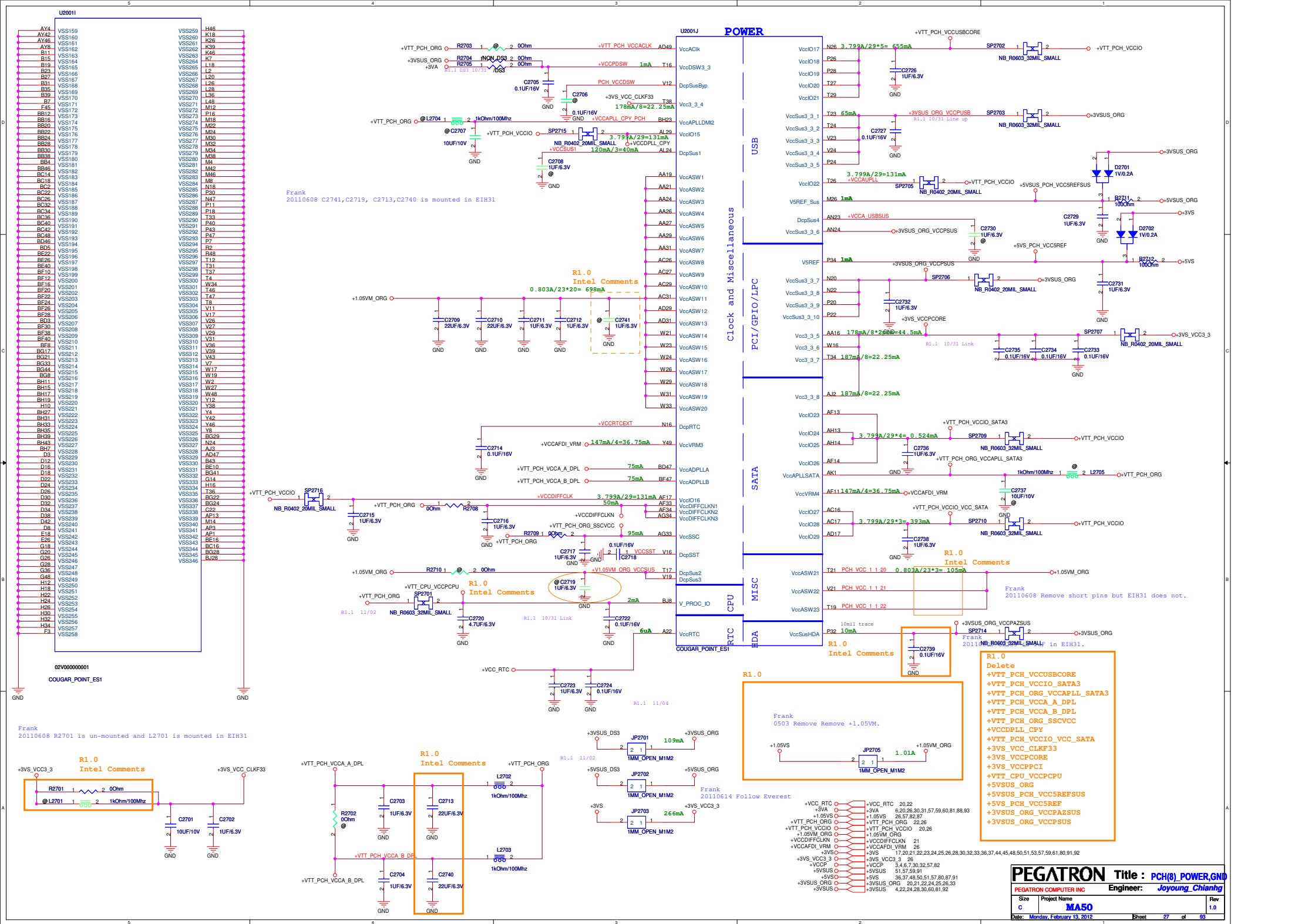
R1.0

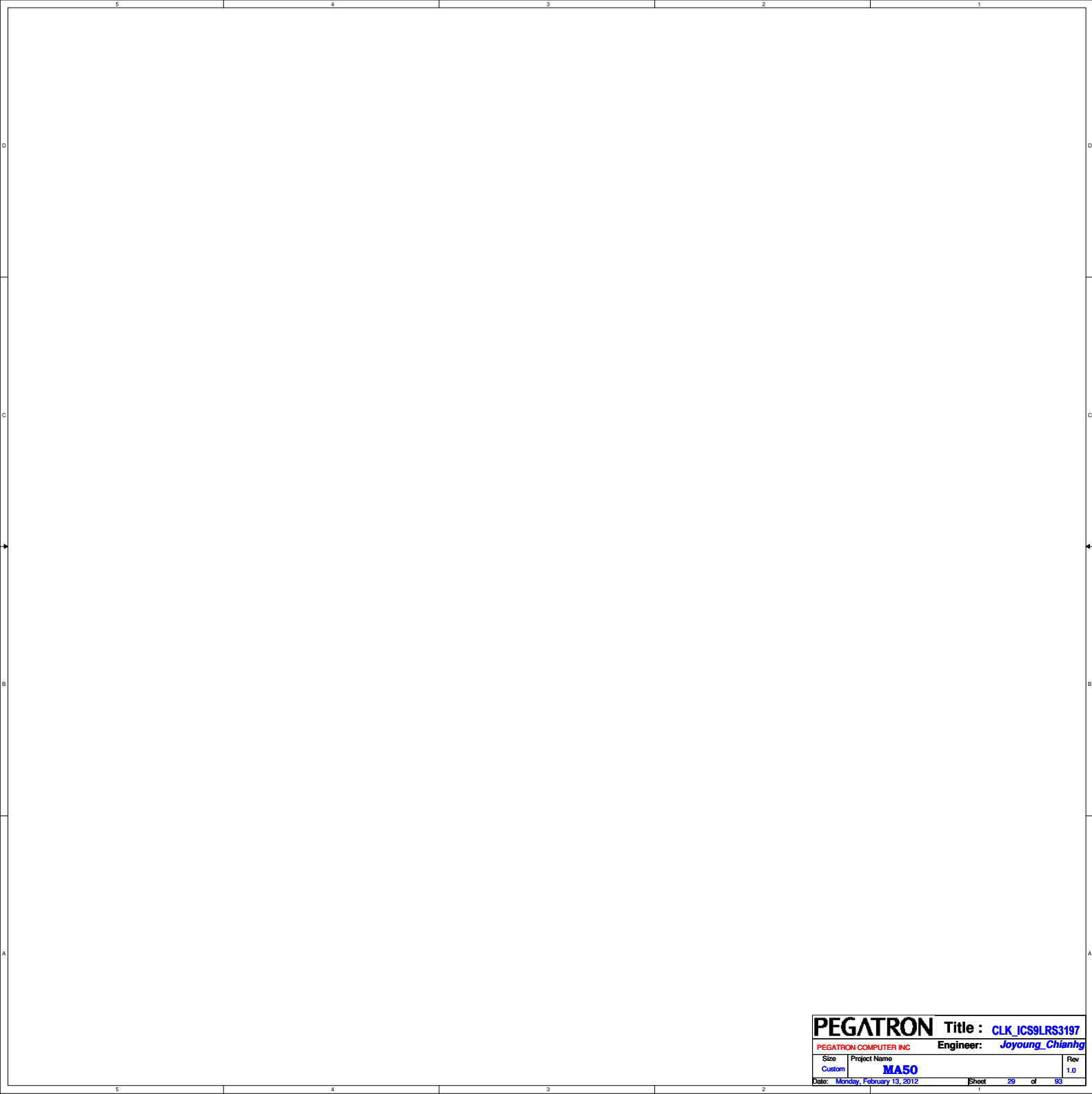
Remove CRIT_TEMP_GPIO0_R to XDP

U2001F




R1.1 add Zero Power ODD



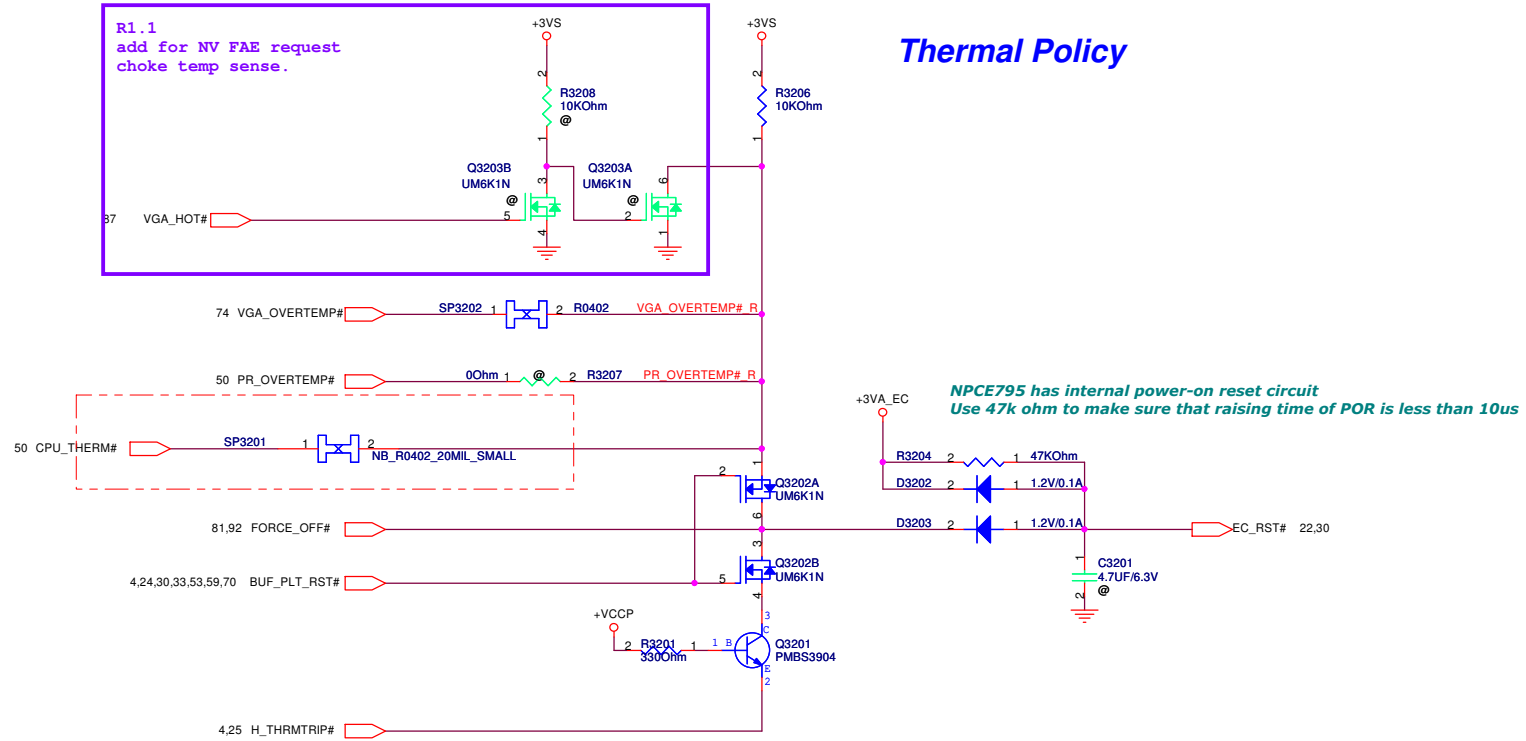


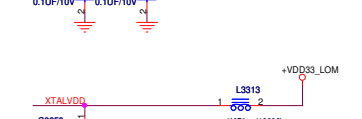
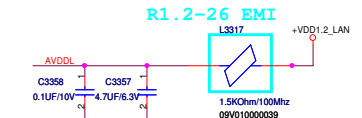
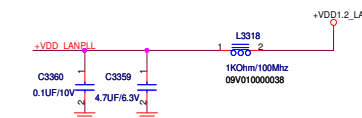
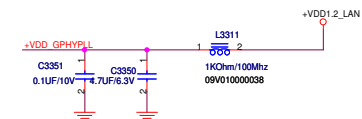
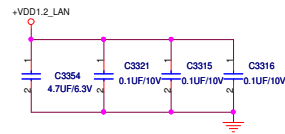
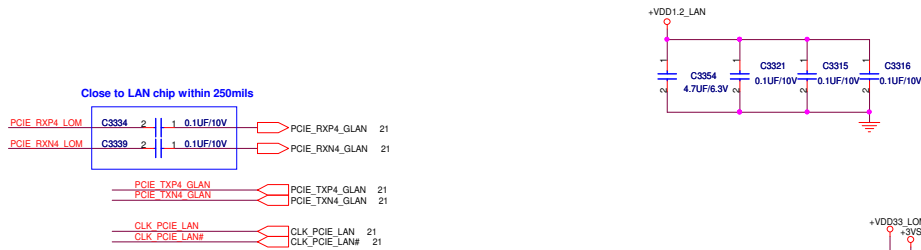




+VCCP  +VCCP 3,4,6,7,30,57,82
 +3VA_EC  +3VA_EC 28,30
 +3VS  +3VS 17,20,21,22,23,24,25,26,27,28,30,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

Thermal Policy





R1.0 Remove PU R for FAB suggestion.

R1.0 chnge VFRI.1.

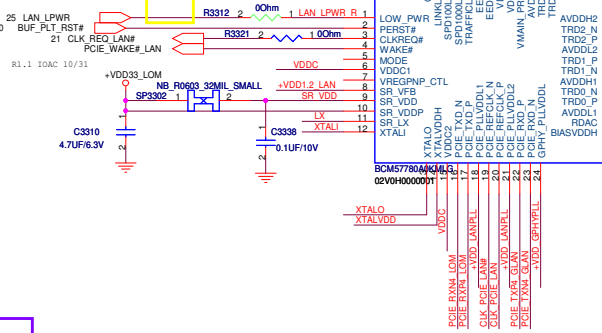
Delete R5308 for unused.

R1.1 change pin define.

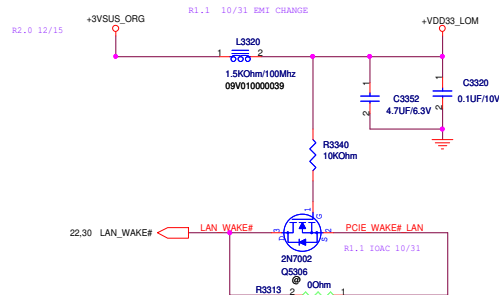
R1.1 10/31 EMI CHANGE

R1.0
OTP mode

Frank
0503 LAN_LPWR is not defined GPIO in PCH.



R1.1
change value for -R test report



Joyoung R1.0
FAE suggest common mode choke is on chip side.

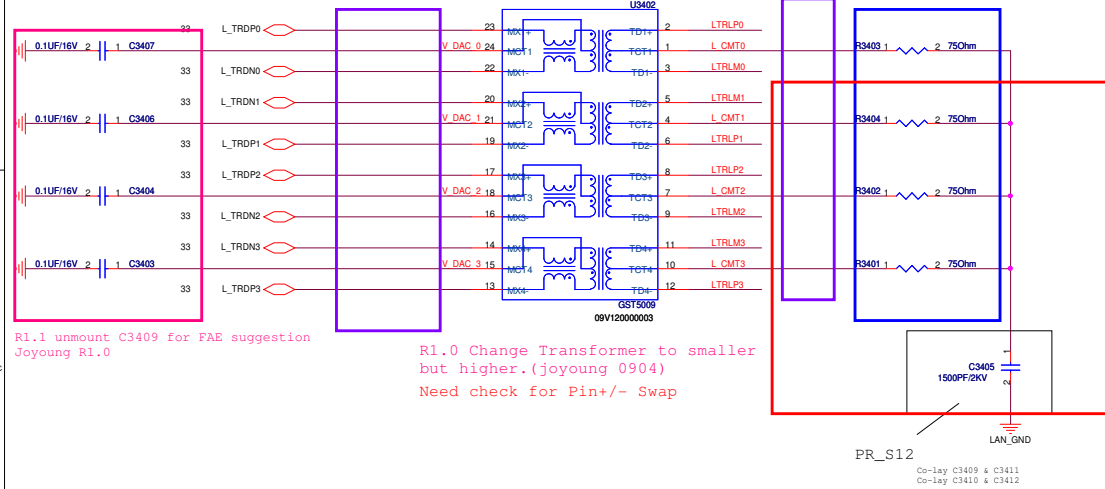
R1.1 Swap L_TRDP3 L_TRDN3 & L_TRDP1 L_TRDN1

R1.1 Add 0 OHM for FAE suggestion 0809
JM50: FAE suggest remove

R1.1 Mount R3401-R3403 for FAE suggestion 0809
R1.1 Remove R3405-R3407 & C3409

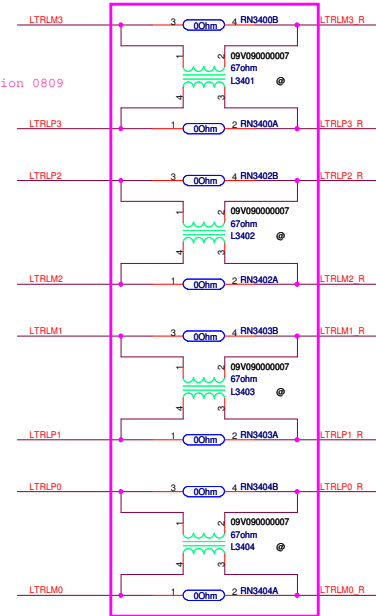
R1.1 remove CAP of V_DAC_3, V_DAC_2 and V_DAC_1 for FAE suggestion

R1.1 Remove R3405-R3407 & C3409

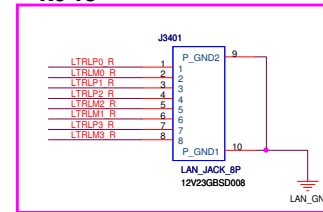


R1.1 unmount C3409 for FAE suggestion
Joyoung R1.0

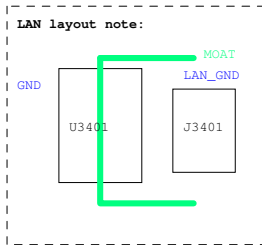
R1.0 Change Transformer to smaller
but higher.(joyoung 0904)
Need check for Pin+/- Swap



RJ45

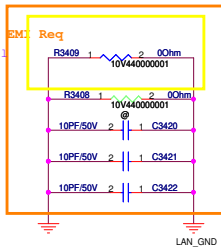


Change RJ45 CON3401

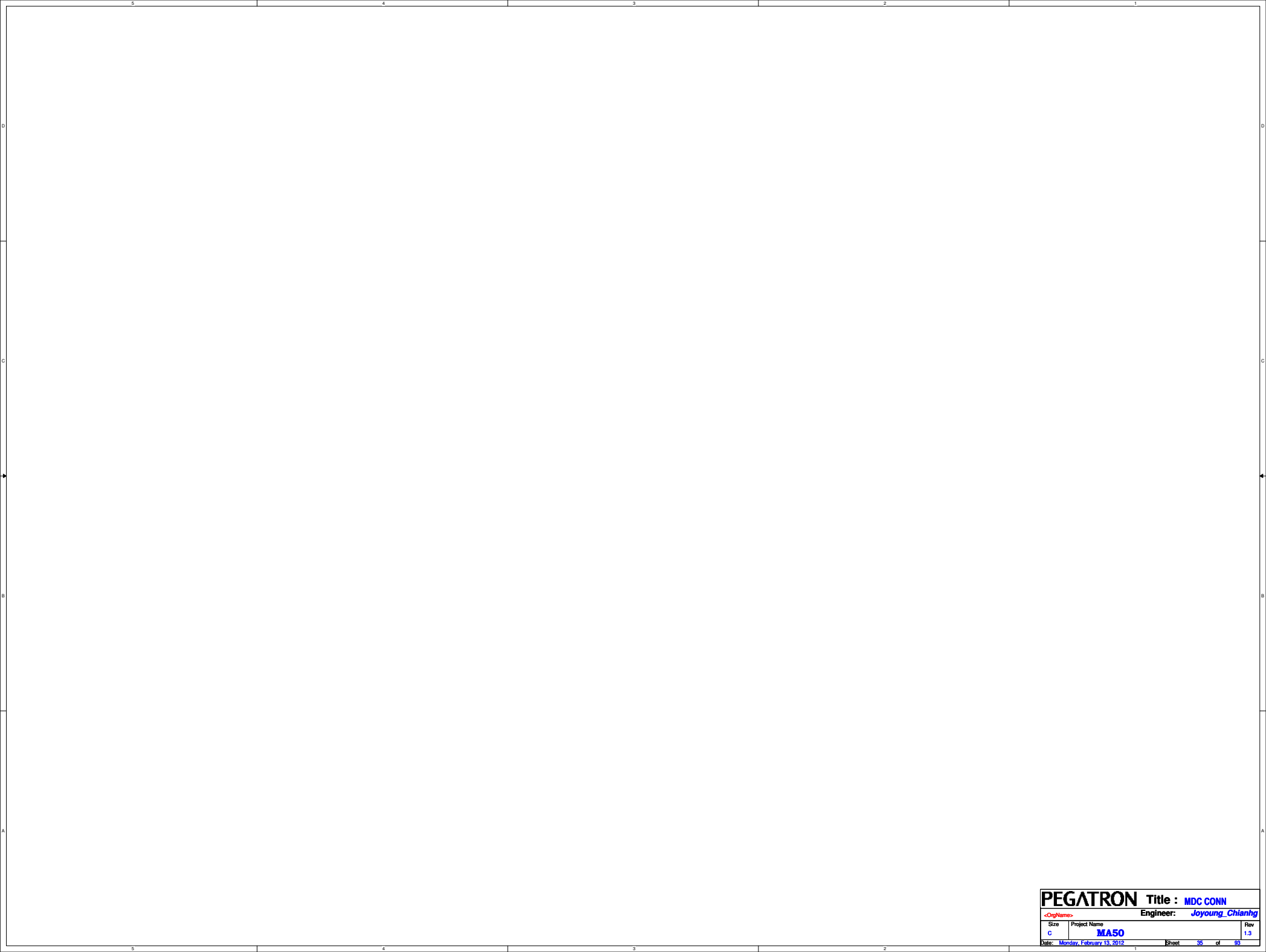


R1.0 Reserve D3401 for EMI.

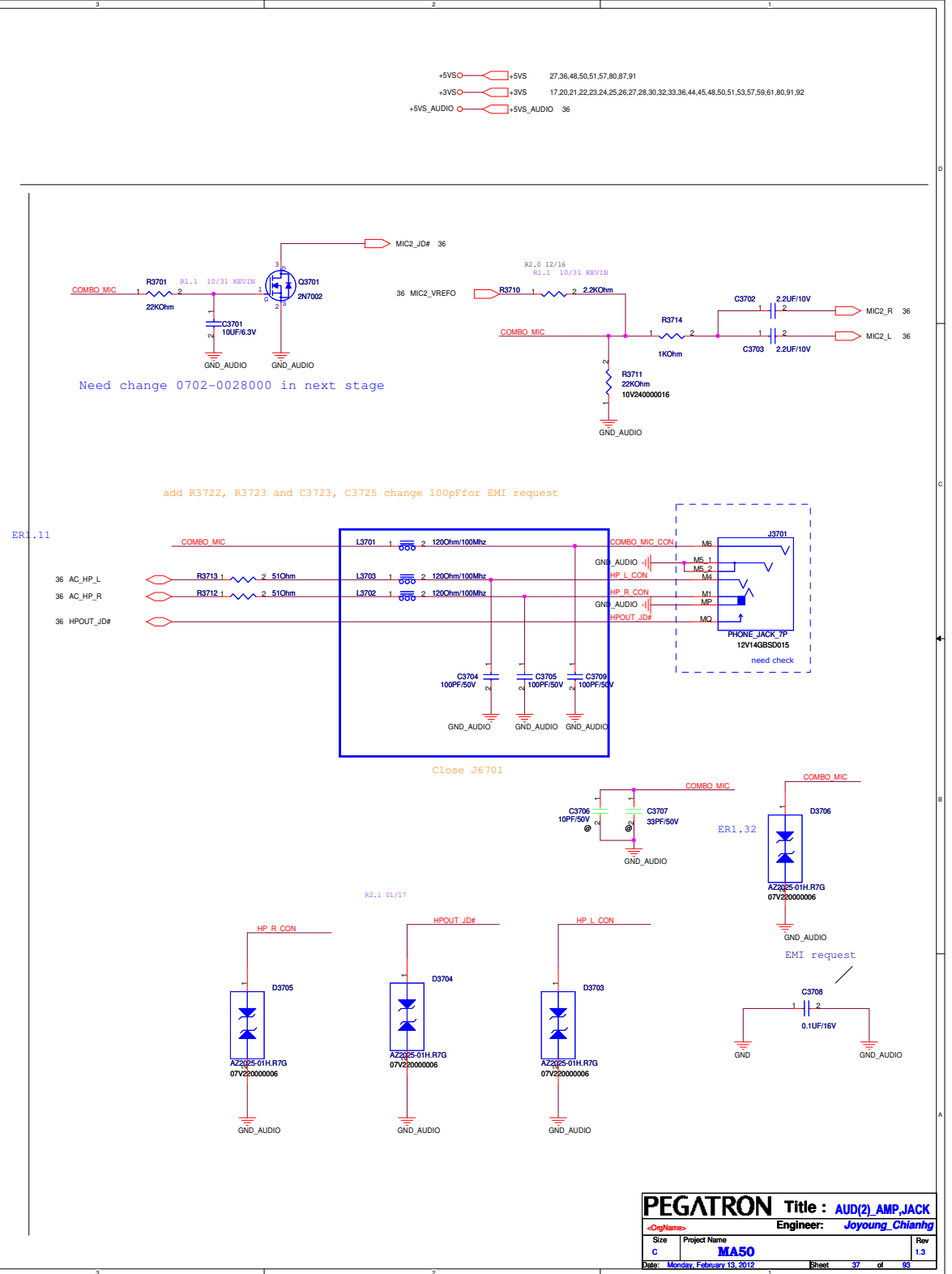
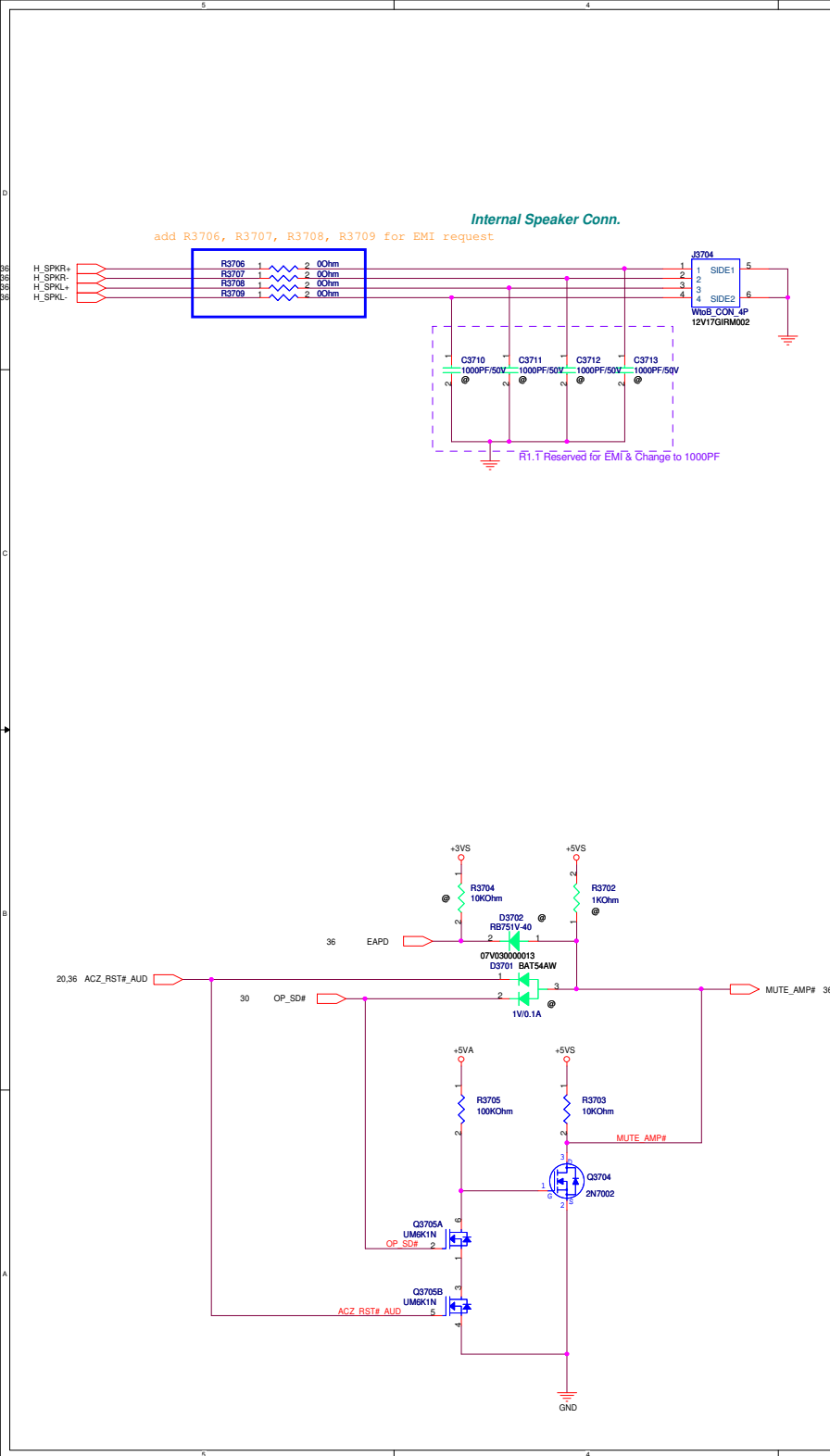
R1.0 Mount R3408 for FAE suggestion



R1.1 EMI Request 4.7PF & Set Close to Connector, then removed all





PEGATRON		Title : MDC CONN	
<OrigName>		Engineer: Joyoung Chianhg	
Size	Project Name	Rev	
C	MA50	1.3	
Date: Monday, February 13, 2012		Sheet	35 of 83






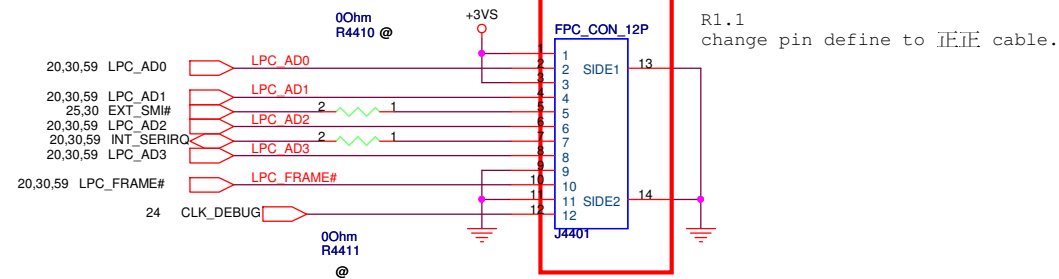


PEGATRON		Title : AUD(4)_****	
<OrgName>		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
Custom	MA50		1.3
Date: Monday, February 13, 2012	Sheet 39 of 93		

+3VS  +3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+12V  +12V 60,91

+3VS  +3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,45,48,50,51,53,57,59,61,80,91,92

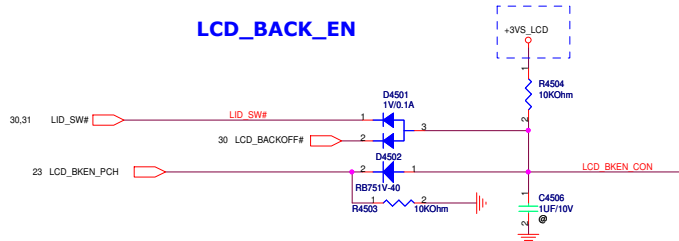
LPC Debug Port



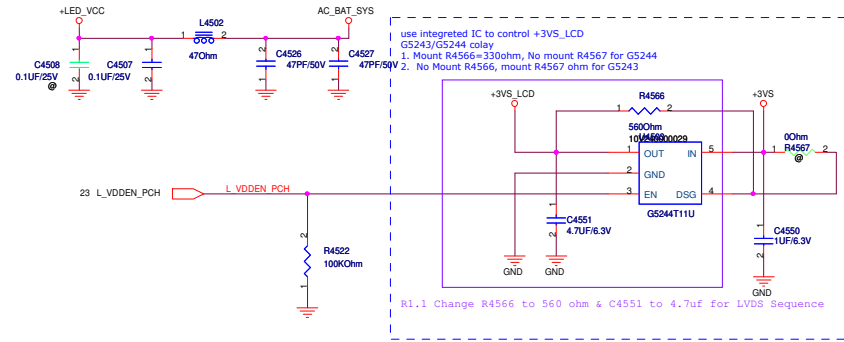
PEGATRON		Title : BUG_Debug	
<OrgName>		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
B	MA50		1.3
Date: Monday, February 13, 2012		Sheet 44	of 93

+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,48,50,51,53,57,59,61,80,91,92
+5VS	27,36,37,48,50,51,57,80,87,91
+12VS	28,36,48,91
+VCCP	3,4,6,7,30,32,57,82
AC_BAT_SYS	53,81,87,88

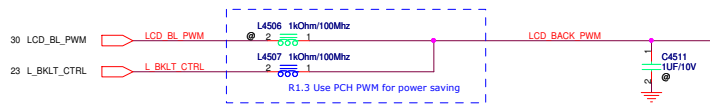
LCD_BACK_EN



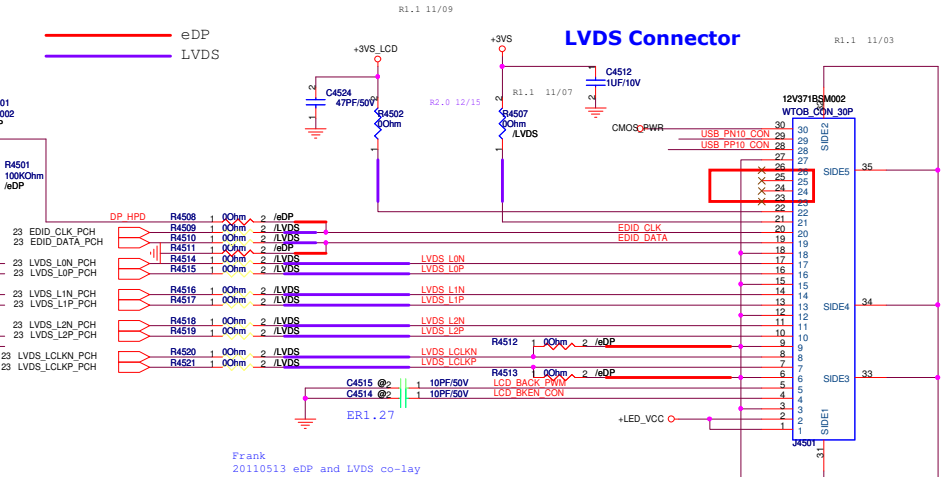
LCD VDDEN / +LED_VCC



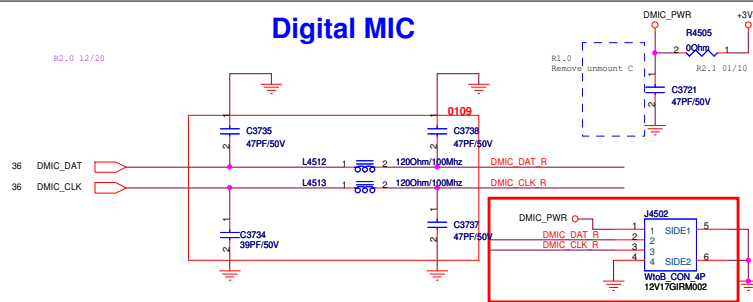
LCD_BL_PWM



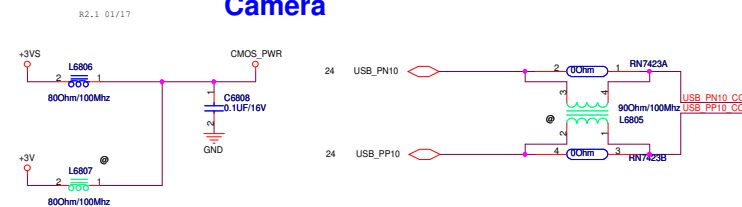
eDP
LVDS



Digital MIC

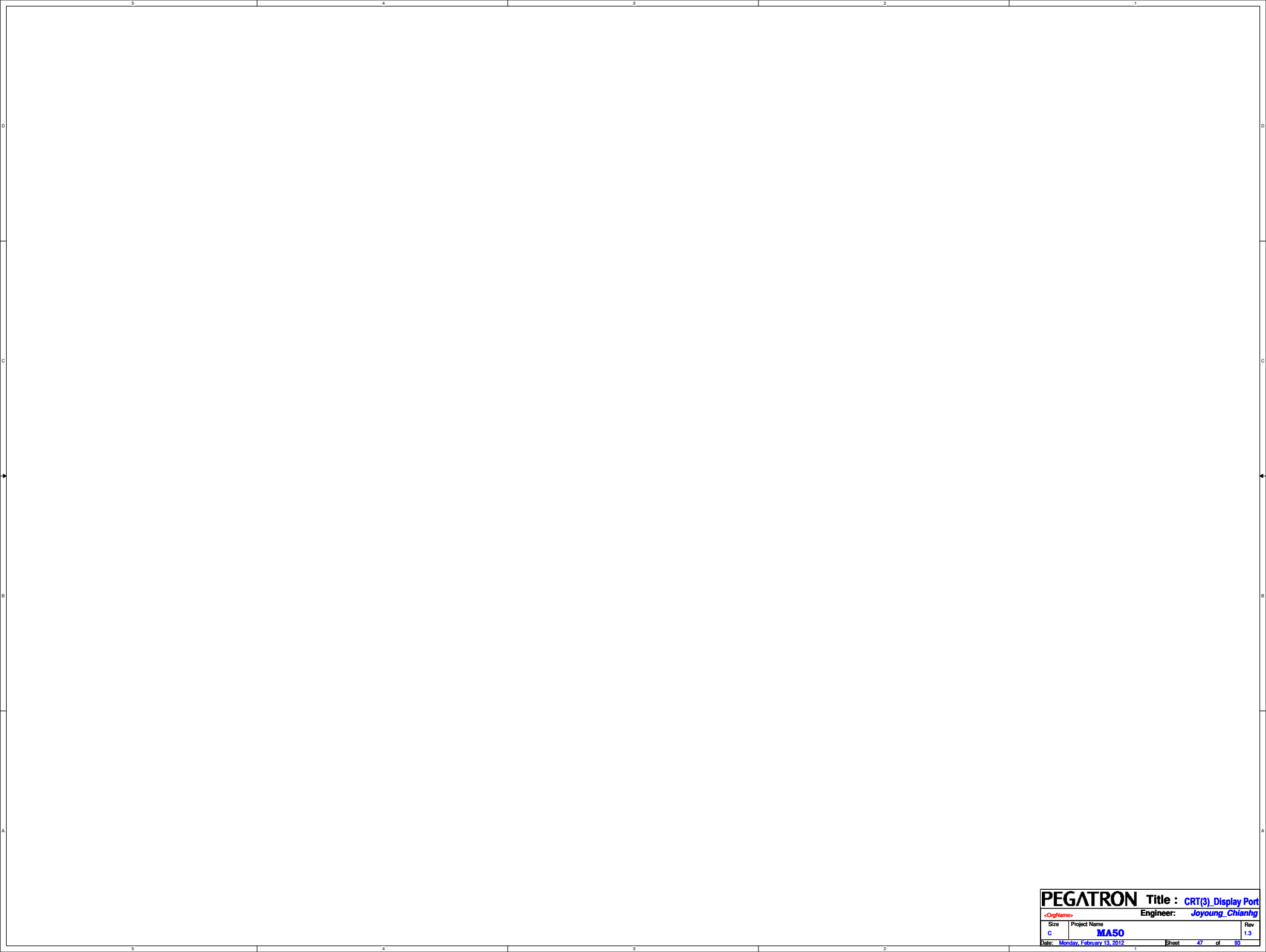


Camera

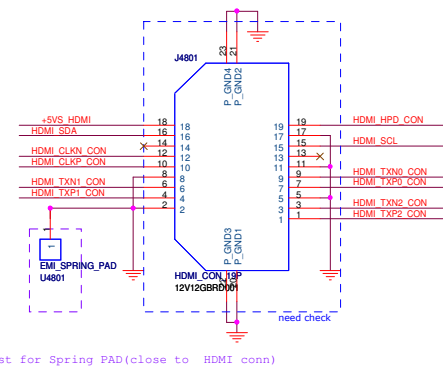
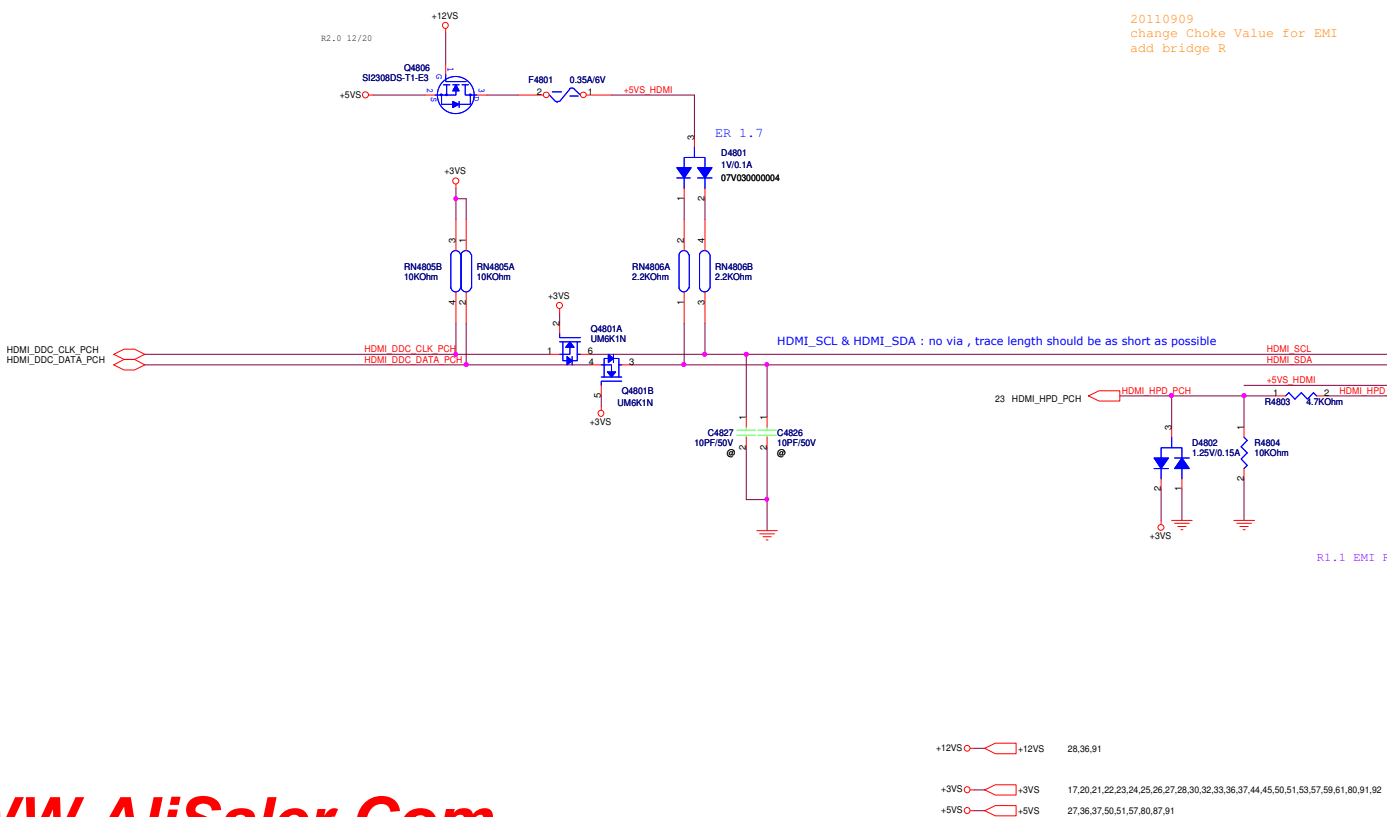


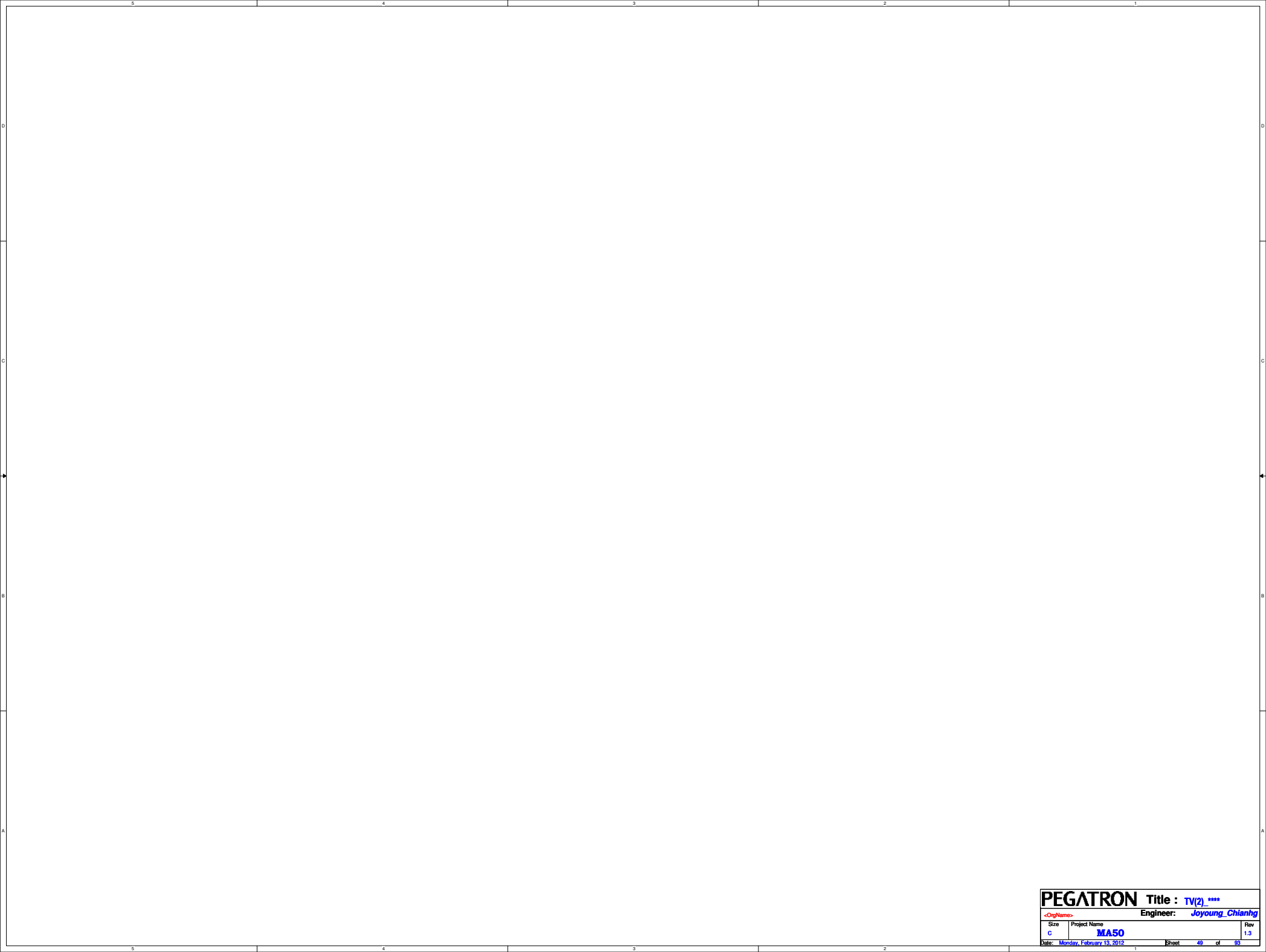


PEGATRON		Title : CRT	
BU1-RD Div.1-HW RD Dept.1		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
Custom	MA50		1.0
Date: Monday, February 13, 2012		Sheet	46 of 93



PEGATRON		Title : CRT(3)_Display Port	
<OrgName>		Engineer: Joyoung Chianhg	
Size	Project Name		Rev
C	MA50		1.3
Date: Monday, February 13, 2012		Sheet	47 of 83



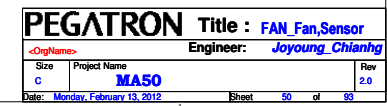


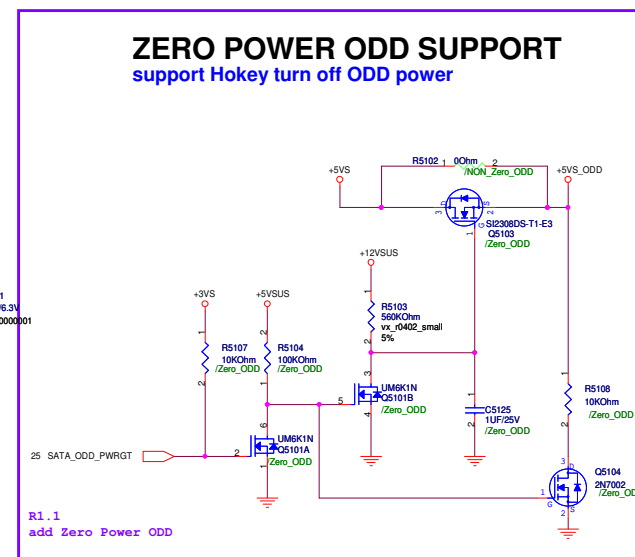
PEGATRON		Title : TV(2)_****	
<OrgName>		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
C	MA50		1.3
Date: Monday, February 13, 2012		Sheet	49 of 83

CPU Thermal Sensor



PWM Fan



[illegible]

PEGATRON		Title : <u>XDD_HDD,ODD</u>	
<OrigName>		Engineer: <u>Joyoung_Chianhg</u>	
Size C	Project Name MA50	Rev 1.3	
Date: <u>Monday, February 13, 2012</u>		Sheet	51 of 93

PEGATRON		Title : USB3.0	
<OrgName>		Engineer: Joyoung_Chianhg	
Size B	Project Name MA50	Rev 1.3	
Date: Monday, February 13, 2012		Sheet	54 of 93





+3VA 6,20,26,27,30,31,57,59,60,81,88,93
+3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+5VSUS 51,57,59,91
+5VA 37,60,81,91
+5V 57,59,60,91
+5VS 27,36,37,48,50,51,57,80,87,91
AC_BAT_SYS AC_BAT_SYS 45,53,81,87,88
+3V 24,45,57,59,61,91

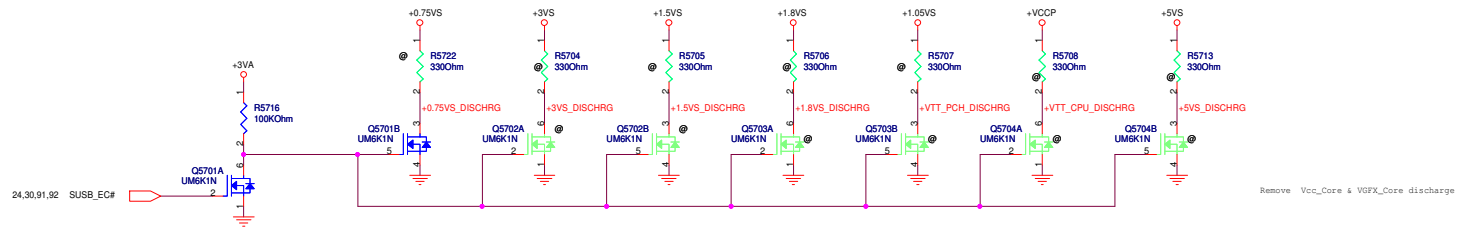
30.59 PWR_LED#

30.59 PWR_LED_standby#

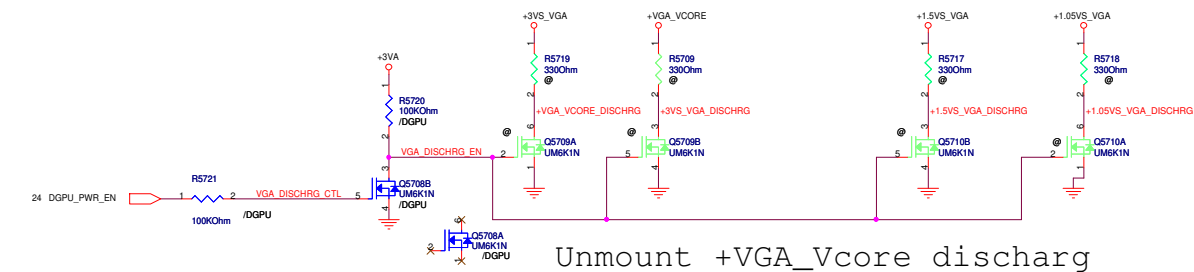
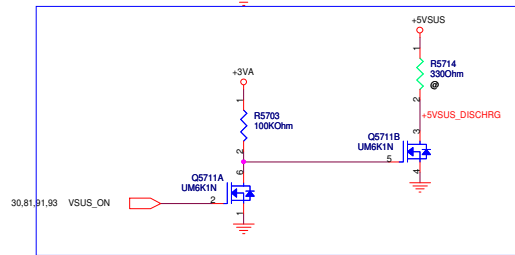
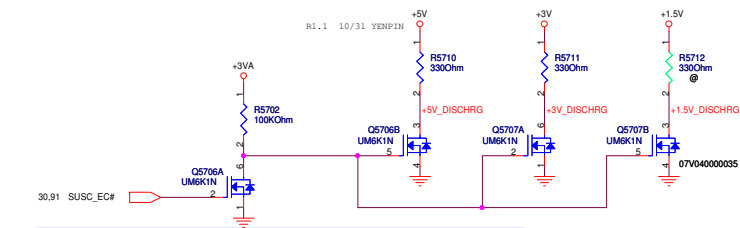
30.59 CHG_LED_BLUE#

30.59 CHG_LED_ORANGE#

+3VA	6,20,26,27,30,31,59,60,81,88,93
+VOCORE	6,9,11,80
+VGFX_CORE	7,9,80
+VCCP	3,4,6,7,30,32,82
+0.75VS	16,17,83
+1.05VS	26,27,82,87
+1.5VS	7,26,53,91
+1.8VS	7,25,26,80,84
+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,59,61,80,91,92
+5VS	27,36,37,48,50,51,80,87,91
+1.5V	5,16,17,18,60,83
+3V	24,45,59,61,91
+5V	59,60,91



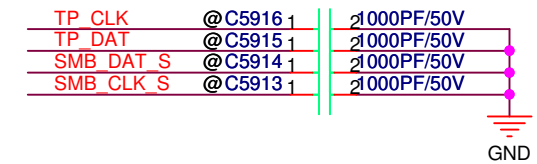
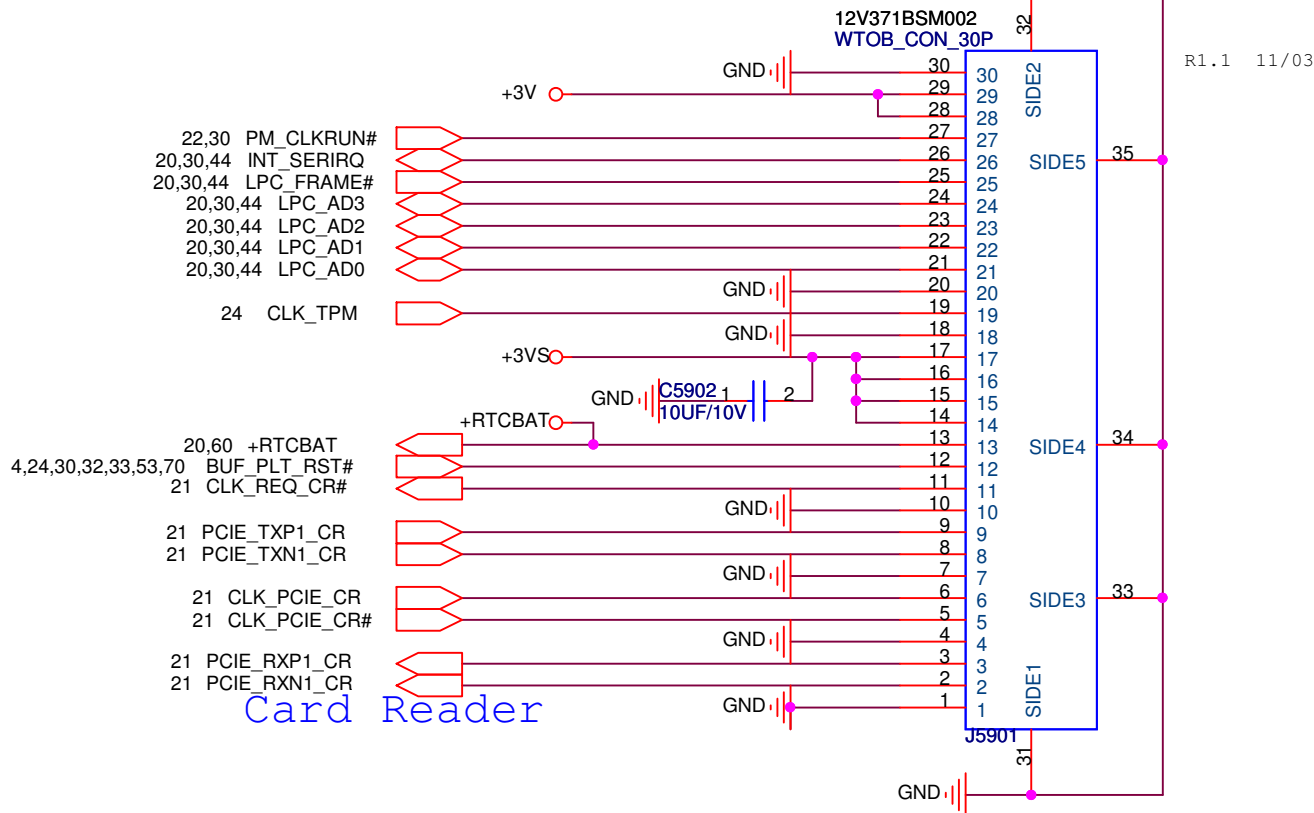
Remove Vcc_Core & VGFX_Core discharge



Unmount +VGA_Vcore discharg

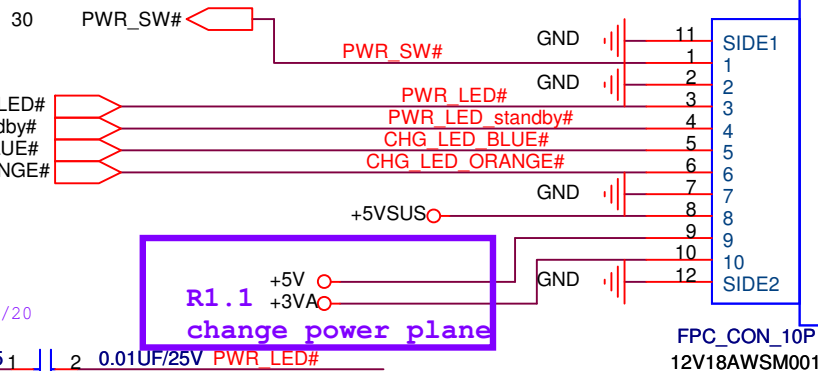
PEGATRON		Title : DSG_Discharge	
<OrgName>		Engineer: Joyoung Chianhg	
Size	Project Name	Rev	
C	MA50	1.3	
Date: Monday, February 13, 2012		Sheet	57 of 83

PEGATRON		Title : System Setting	
<OrgName>		Engineer: <i>Joyoung_Chianhg</i>	
Size	Project Name		Rev
Custom	MASO		1.3
Date: <i>Monday, February 13, 2012</i>		Sheet	58 of 93



Power BTN and LED

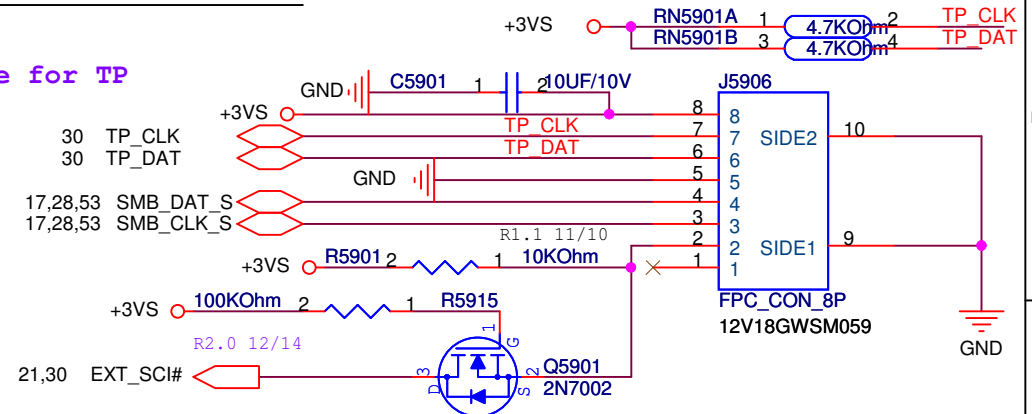
R2.0 12/19



R2.0 12/20

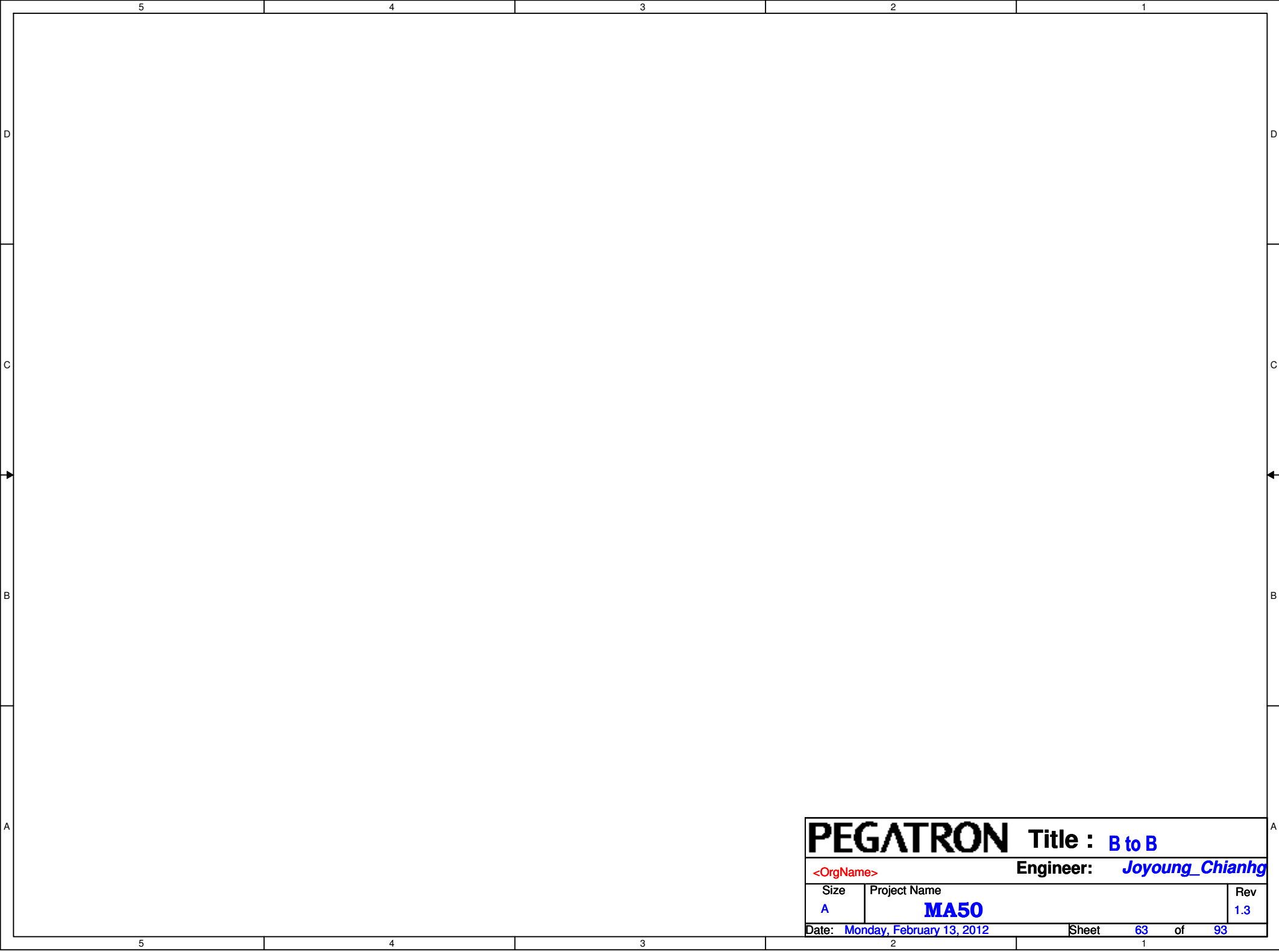
R1.1
change for TP

R2.0 12/19



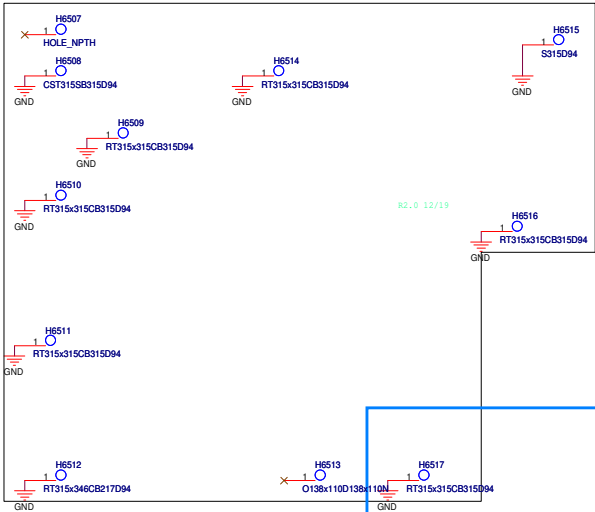
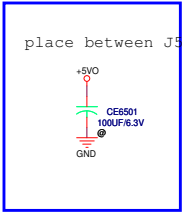
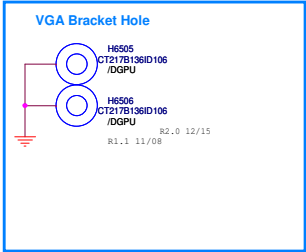
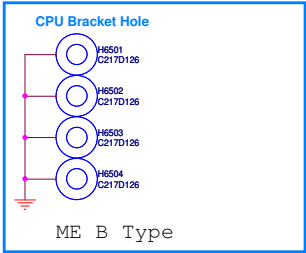
PEGATRON Title : B to B		
Engineer: Joyoung Chianhg		
Size A	Project Name MA50	Rev 1.3
Date: Monday, February 13, 2012	Sheet 59	of 93

PEGATRON		Title : System Setting	
<OrgName>		Engineer: <i>Joyoung_Chianhg</i>	
Size	Project Name		Rev
Custom	MASO		1.3
Date: <i>Monday, February 13, 2012</i>		Sheet	62 of 93

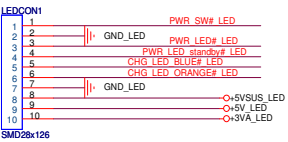


PEGATRON			Title : B to B		
<OrgName>			Engineer: Joyoung_Chianhg		
Size	Project Name				Rev
A	MA50				1.3
Date: Monday, February 13, 2012			Sheet	63	of 93

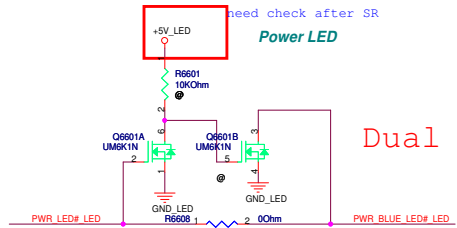
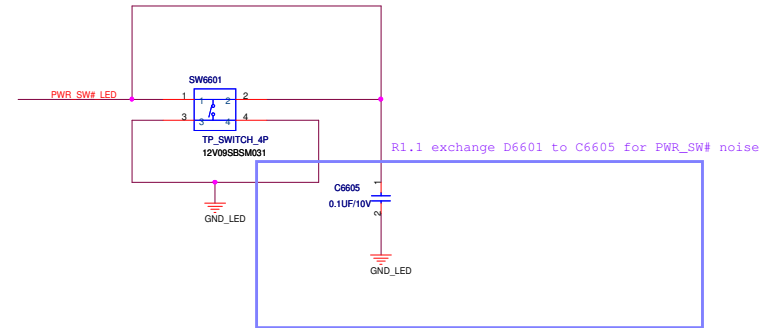




This screw hole should be Upside down(TOP and BOTTOM) .

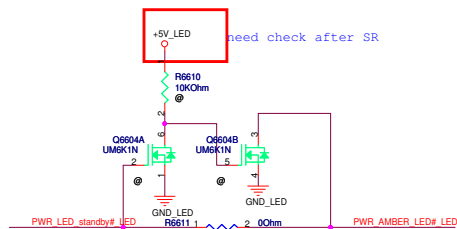


Power Button

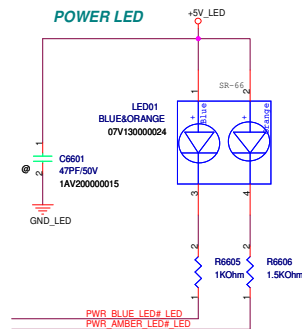


Power LED

Dual Color



need check after SR



POWER LED

LED01
BLUE&ORANGE
07V1300000024

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

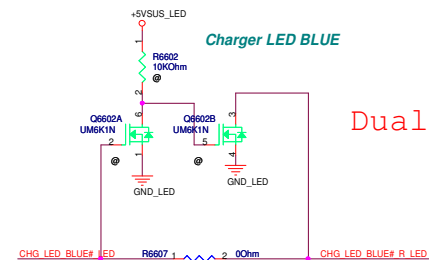
GND_LED

GND_LED

GND_LED

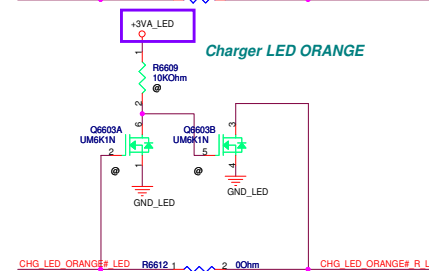
GND_LED

GND_LED

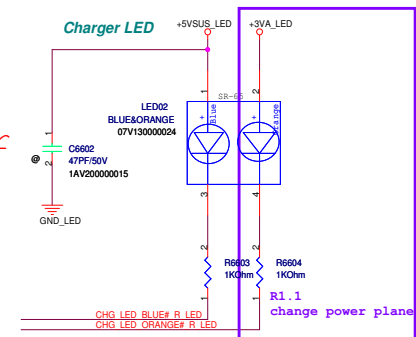


Charger LED BLUE

Dual Color



Charger LED ORANGE



Charger LED

LED02
BLUE&ORANGE
07V1300000024

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

GND_LED

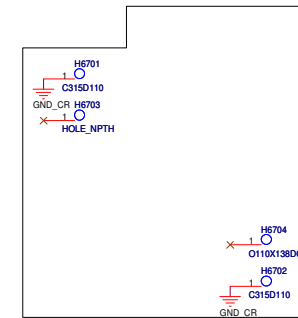
GND_LED

GND_LED

GND_LED

GND_LED

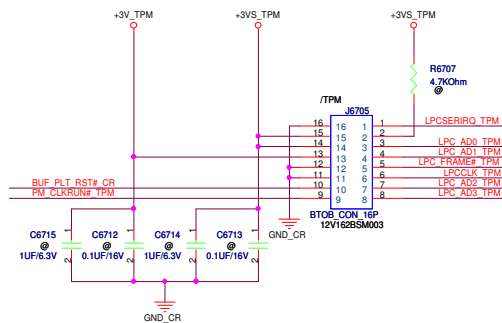
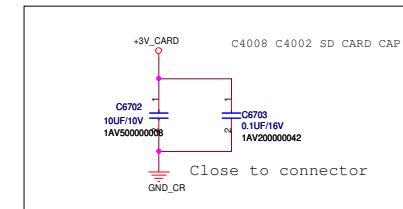
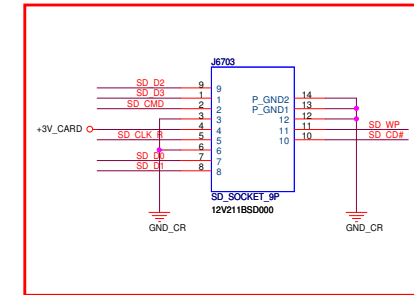
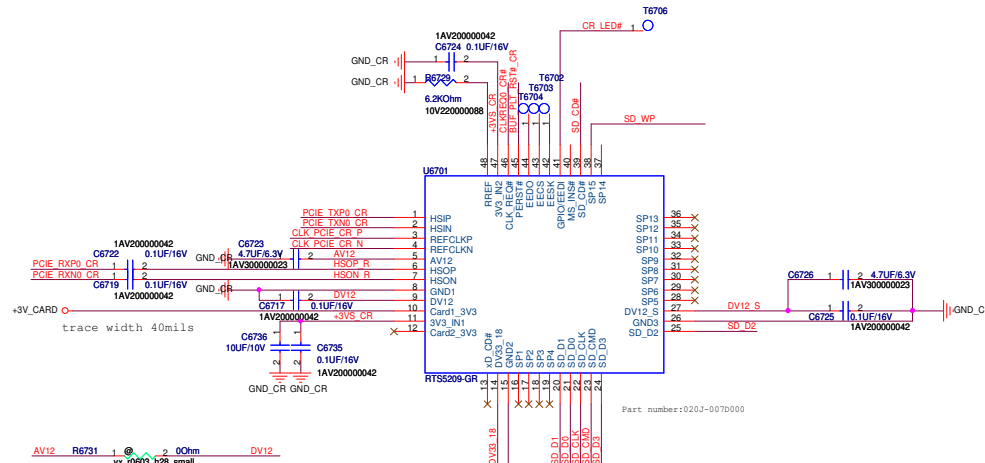
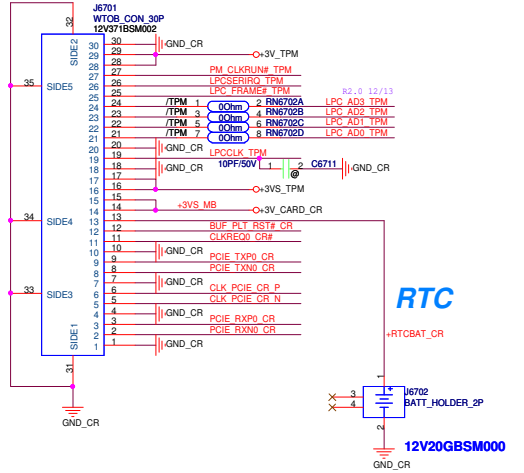
R1.1 change power plane



SDCLK trace length shorter, surround with GND.

From System's PCIe interface

R1.1 change to 30P



Remove Serial Flash

```

|-----|
| Reserve for BIOS boot function

```

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

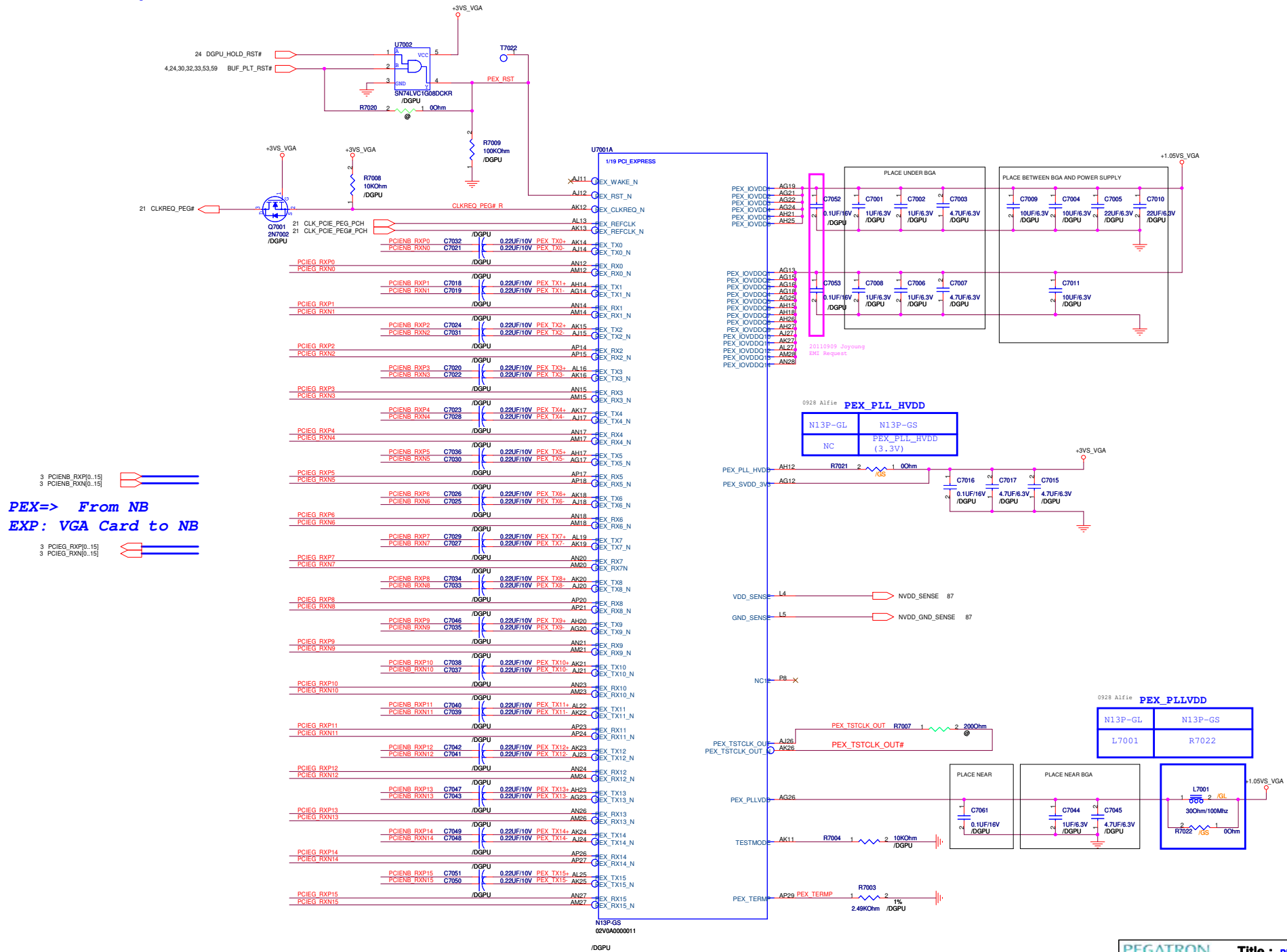
PEGATRON Title : **RTS5209**

Engineer: **JAY TSAI**

Size C	Project Name MA50	Rev 1.0
Date: Monday, February 13, 2012		Sheet 67 of 93

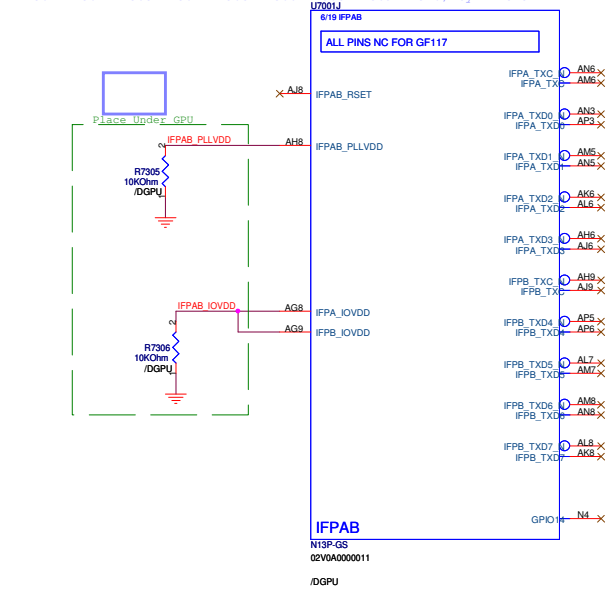
PEGATRON		Title : USB_USB Port	
<OrgName>		Engineer: Joyoung_Chianhg	
Size B	Project Name MA50	Rev 1.3	
Date: Monday, February 13, 2012		Sheet 69 of 93	

Frank
20110513 Change N13P GPU.

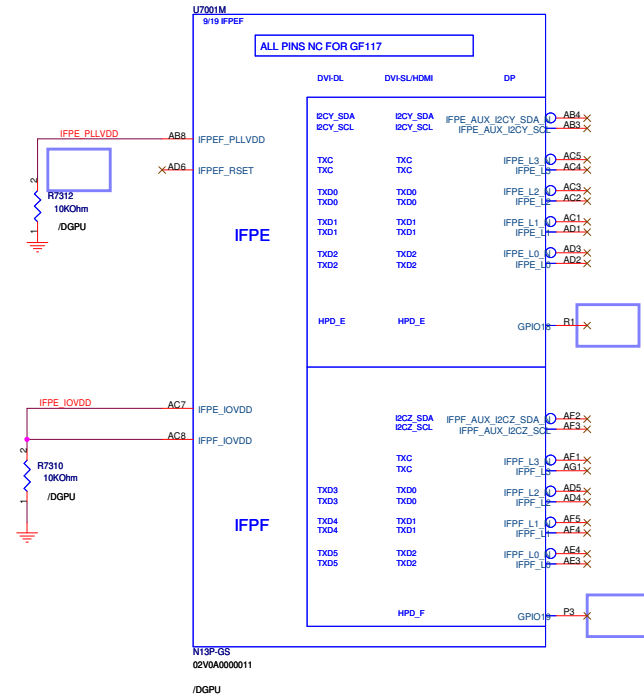
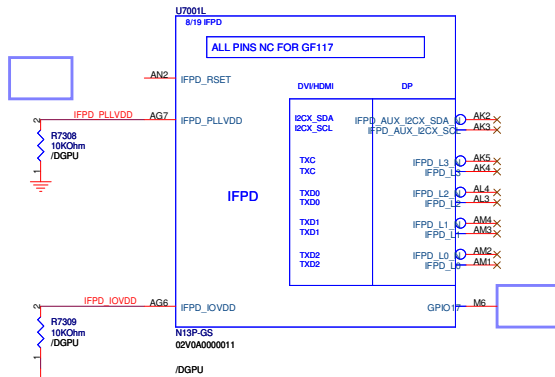
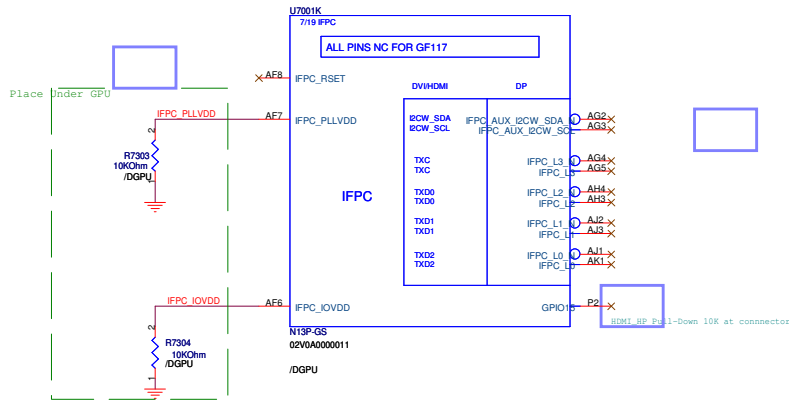




LVDS
R1.1 Remove the TP (T7301 T7311 T7302 T7307 T7303 T7304 T7305 T7306 T7308 T7309 T7310) by Nvidia

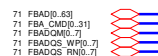


HDMI

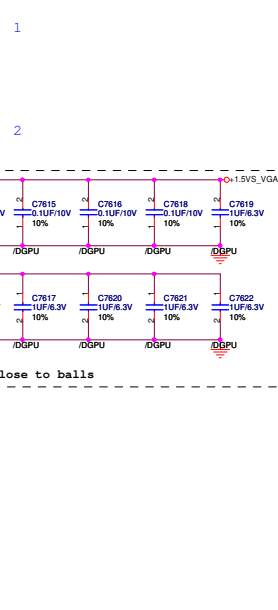
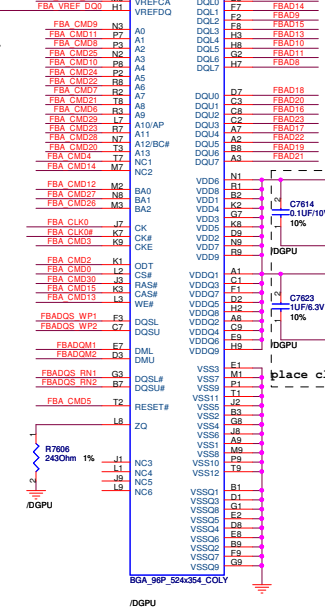


PEGATRON		Title : FRAME BUFFER A	
PEGATRON COMPUTER INC		Engineer: Jyoung Chianhg	
Size A2	Project Name MA50	Rev 1.0	
P/N	<OrgAddr>		
Date: Monday, February 13, 2012	Sheet 74	of 93	

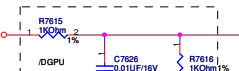
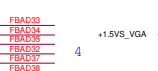
TOP SIDE



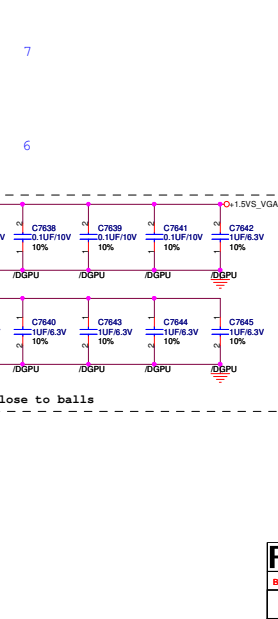
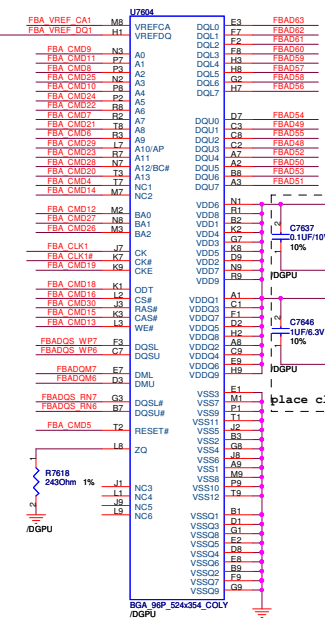
BOT SIDE



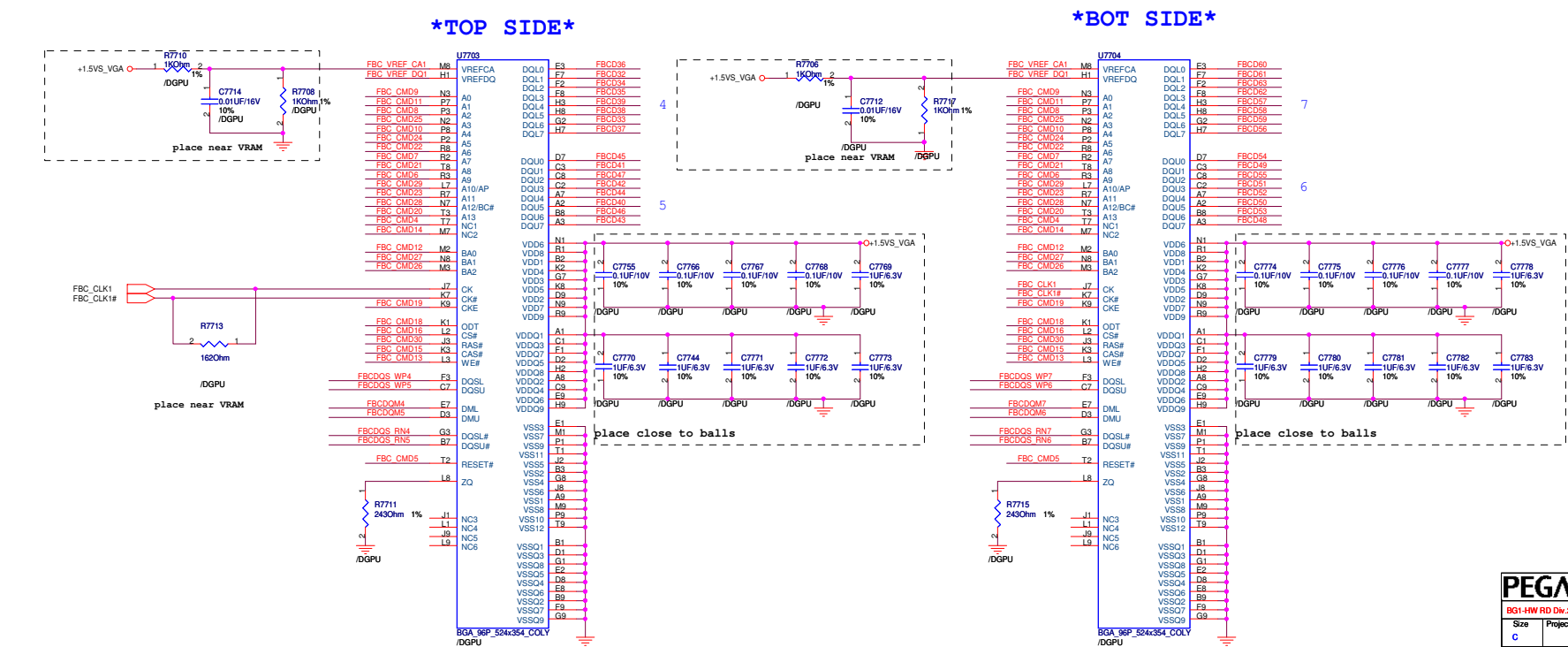
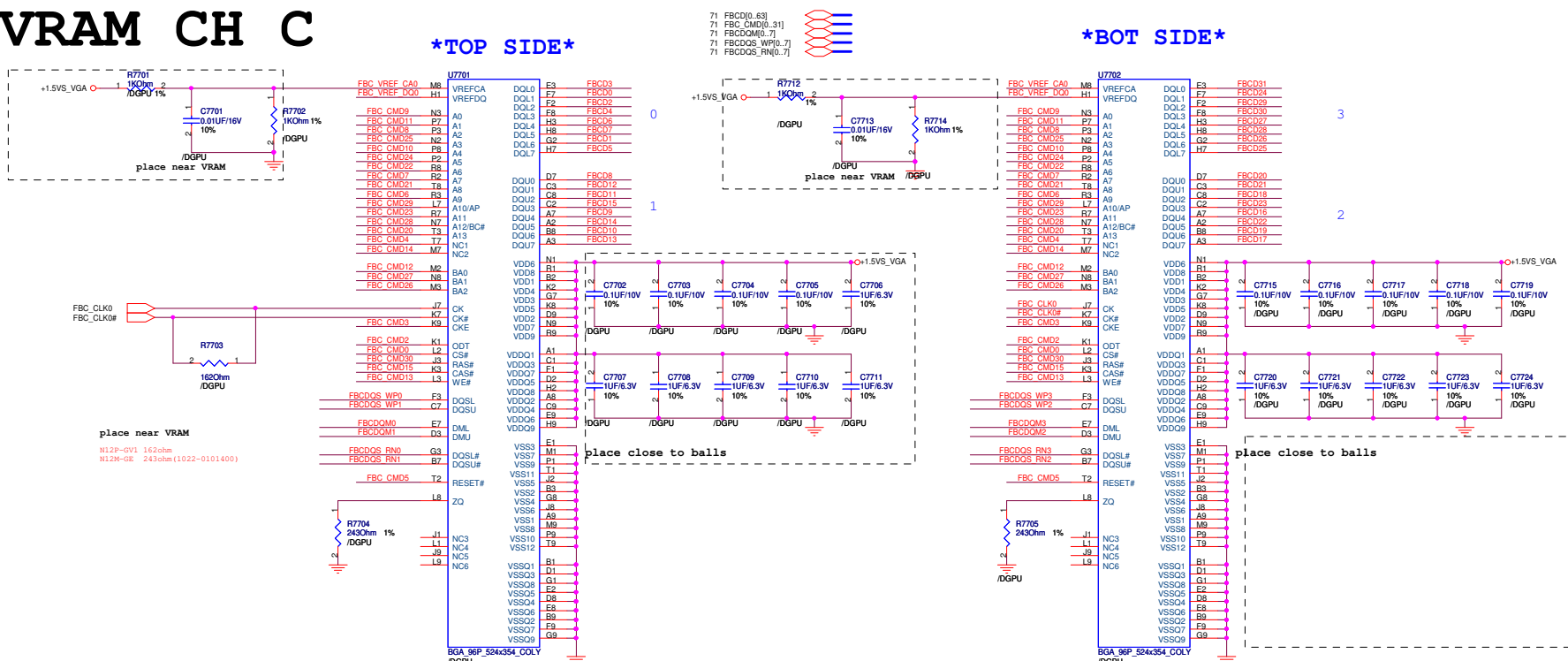
TOP SIDE



BOT SIDE



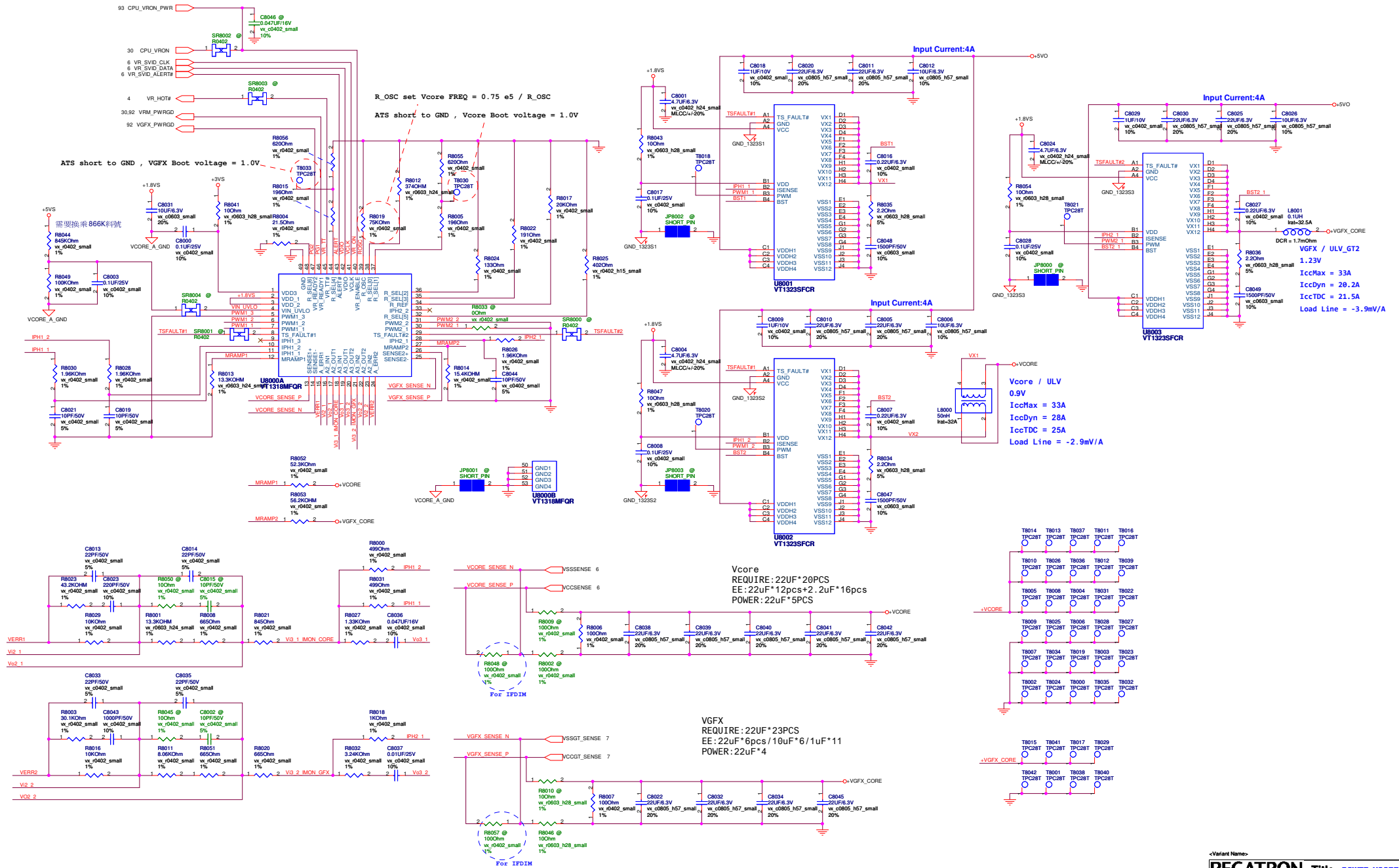
VRAM CH C



	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: Joyoung Chianhg	
Size	Project Name		Rev
C	P/N	MASO <OrgAddr2>	1.0
Date: Monday, February 13, 2012		Sheet	78 of 83

+VCORE & +VGFX POWER SUPPLY Huron River



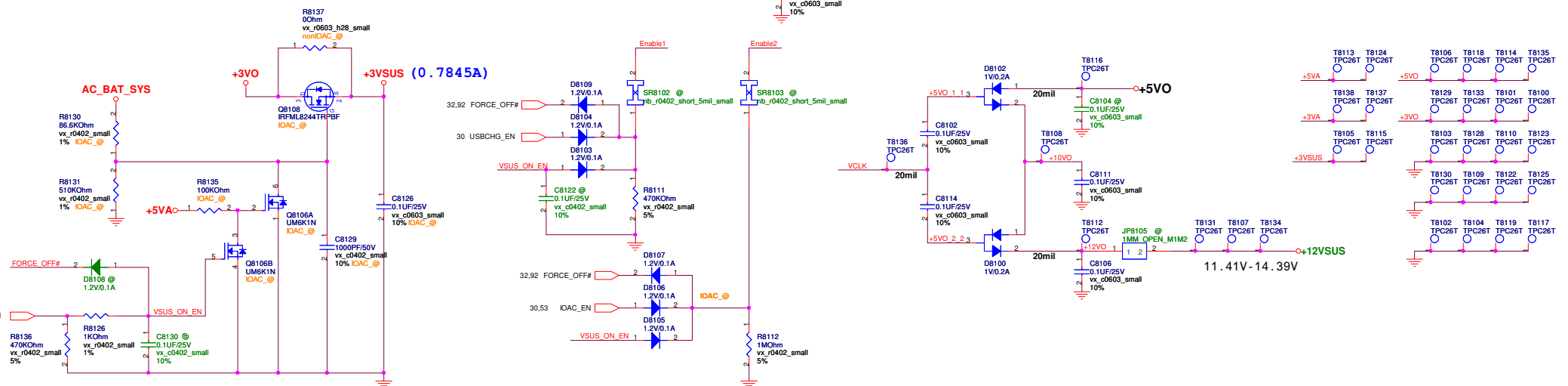
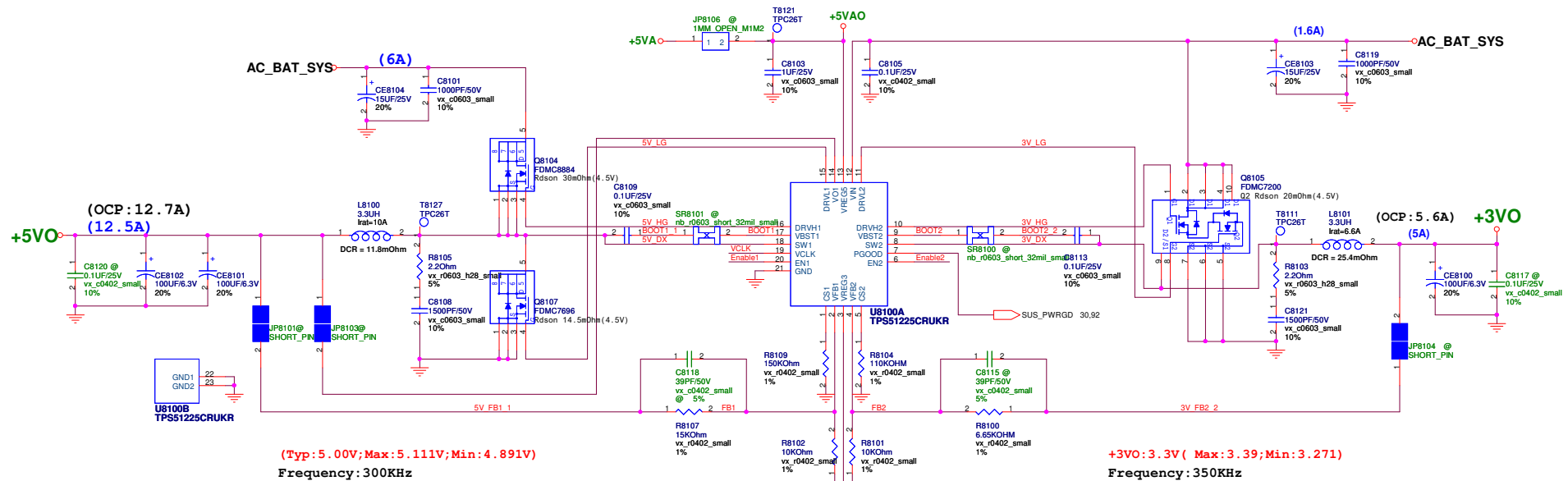
Variant Name:

PEGATRON Title: POWER_VCORE&VGFX

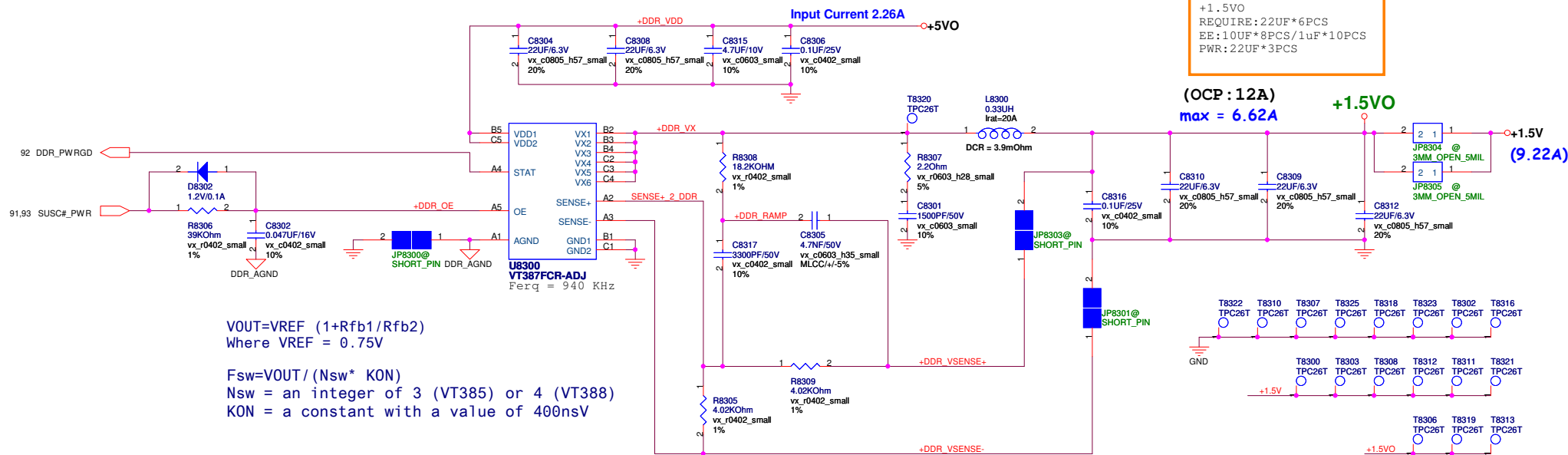
Engineer: Clark Liang

Size: Project Name: MA50

Date: Monday, February 13, 2012 Sheet: 80 of 84



11/07/21
+1.5VO
REQUIRE:22UF*6PCS
EE:10UF*8PCS/1uF*10PCS
PWR:22UF*3PCS

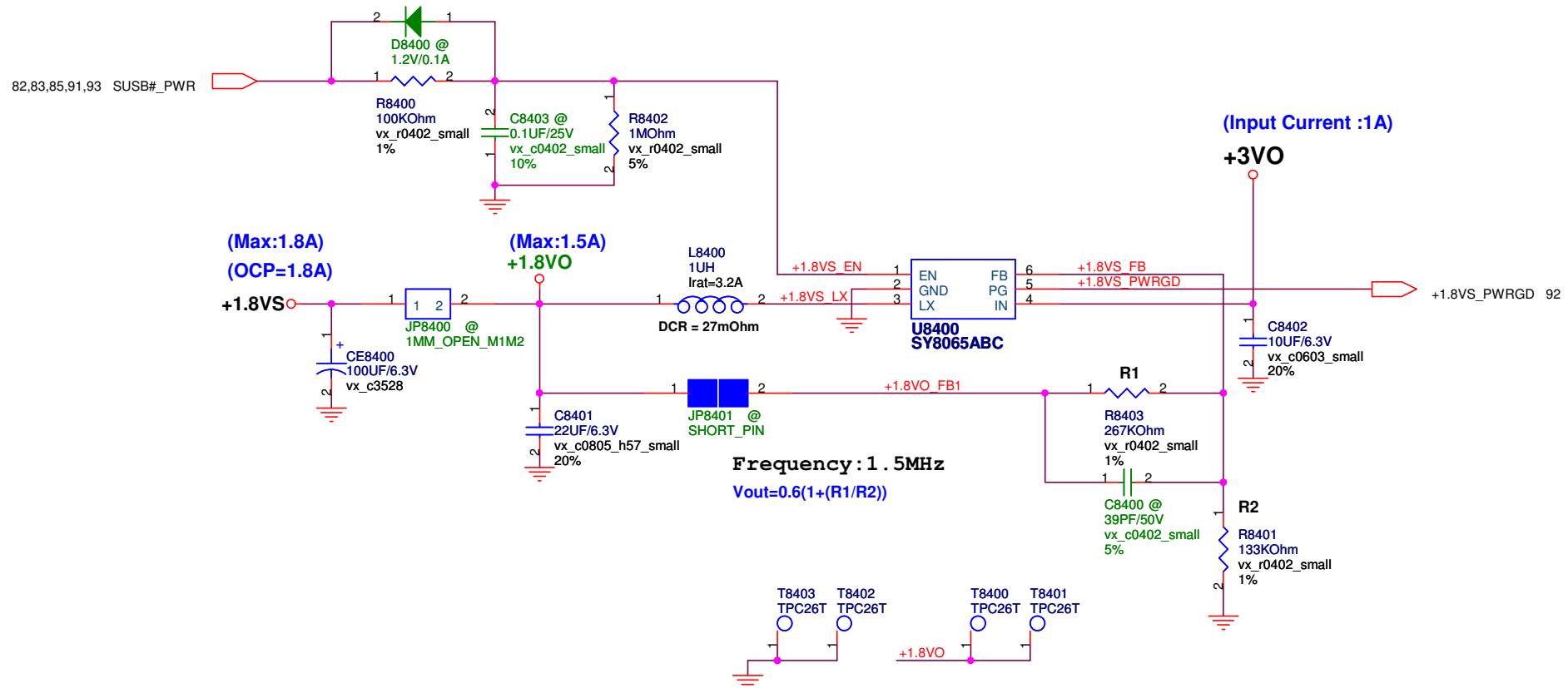


PEGATRON Title : POWER_DDR & VTT

Size	Project Name	Rev
Custom	MA50	1.0

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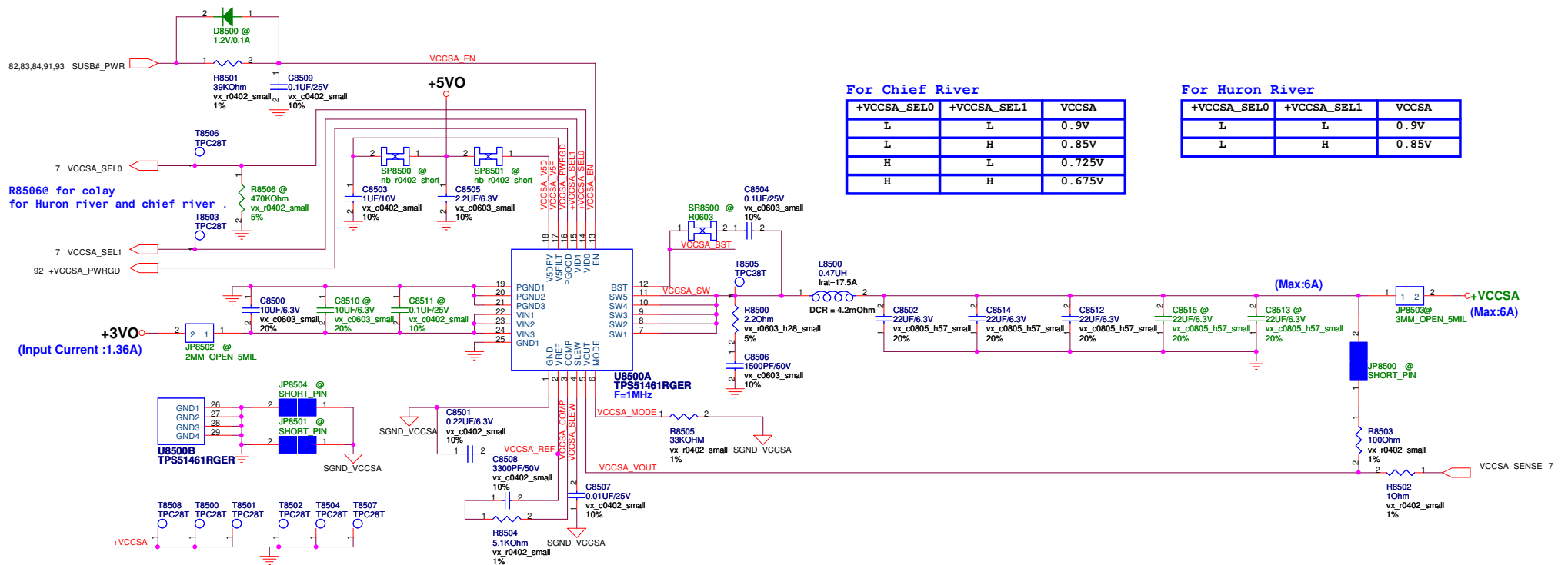
+1.8VS POWER SUPPLY



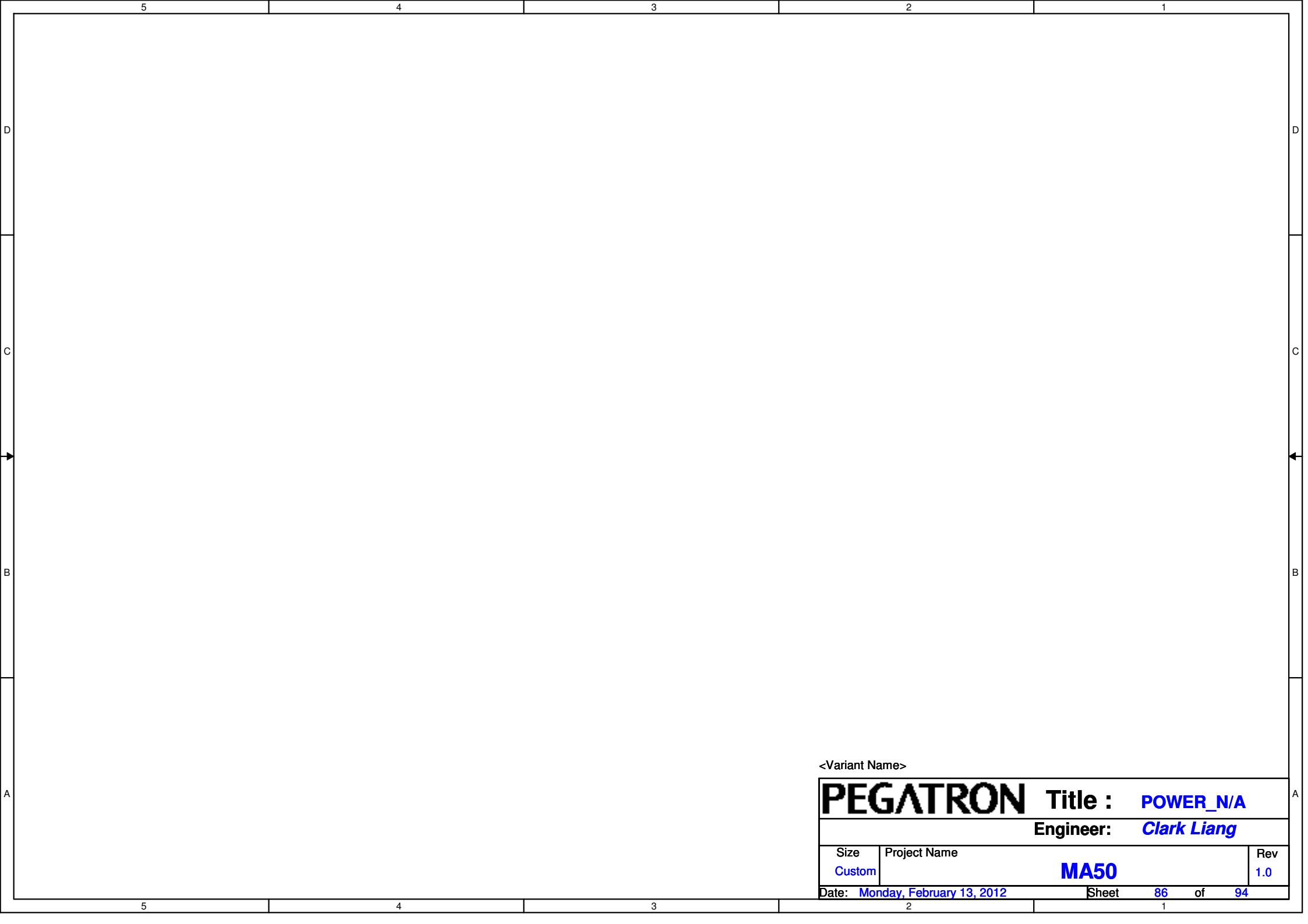
<Variant Name>

PEGATRON		Title :	POWER_+1.8VS
		Engineer:	Clark Liang
Size Custom	Project Name	MA50	
Date: Monday, February 13, 2012	Sheet	84	of 94
		Rev	1.0

IVB VCCSA POWER SUPPLY



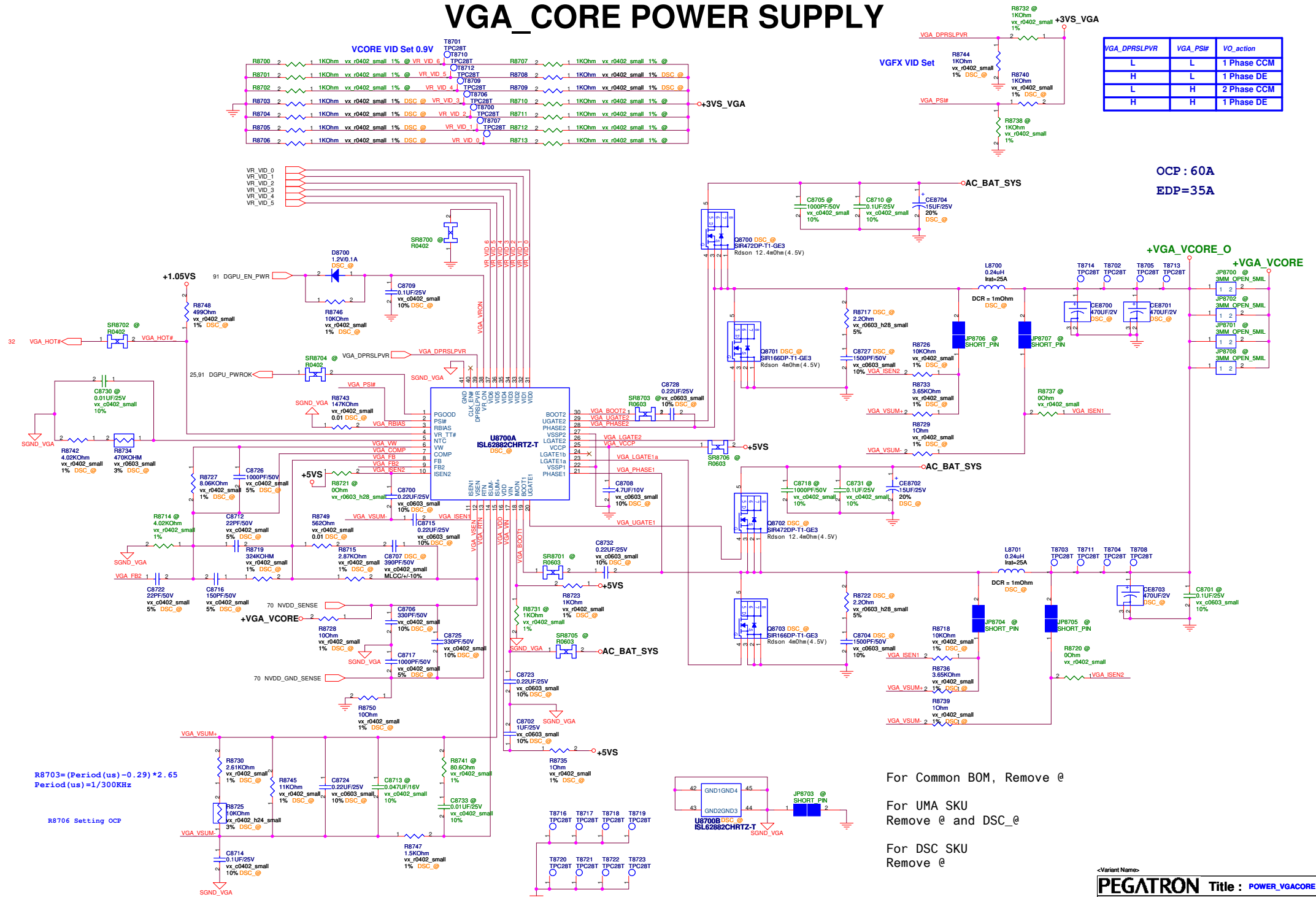
<Variant Name>



<Variant Name>

PEGATRON		Title :	POWER_N/A
		Engineer:	Clark Liang
Size	Project Name		Rev
Custom	MA50		1.0
Date: Monday, February 13, 2012		Sheet	86 of 94

VGA_CORE POWER SUPPLY



For Common BOM, Remove @

For UMA SKU
Remove @ and DSC_@

For DSC SKU
Remove @

<Variant Name>

PEGATRON Title : POWER_VGACORE

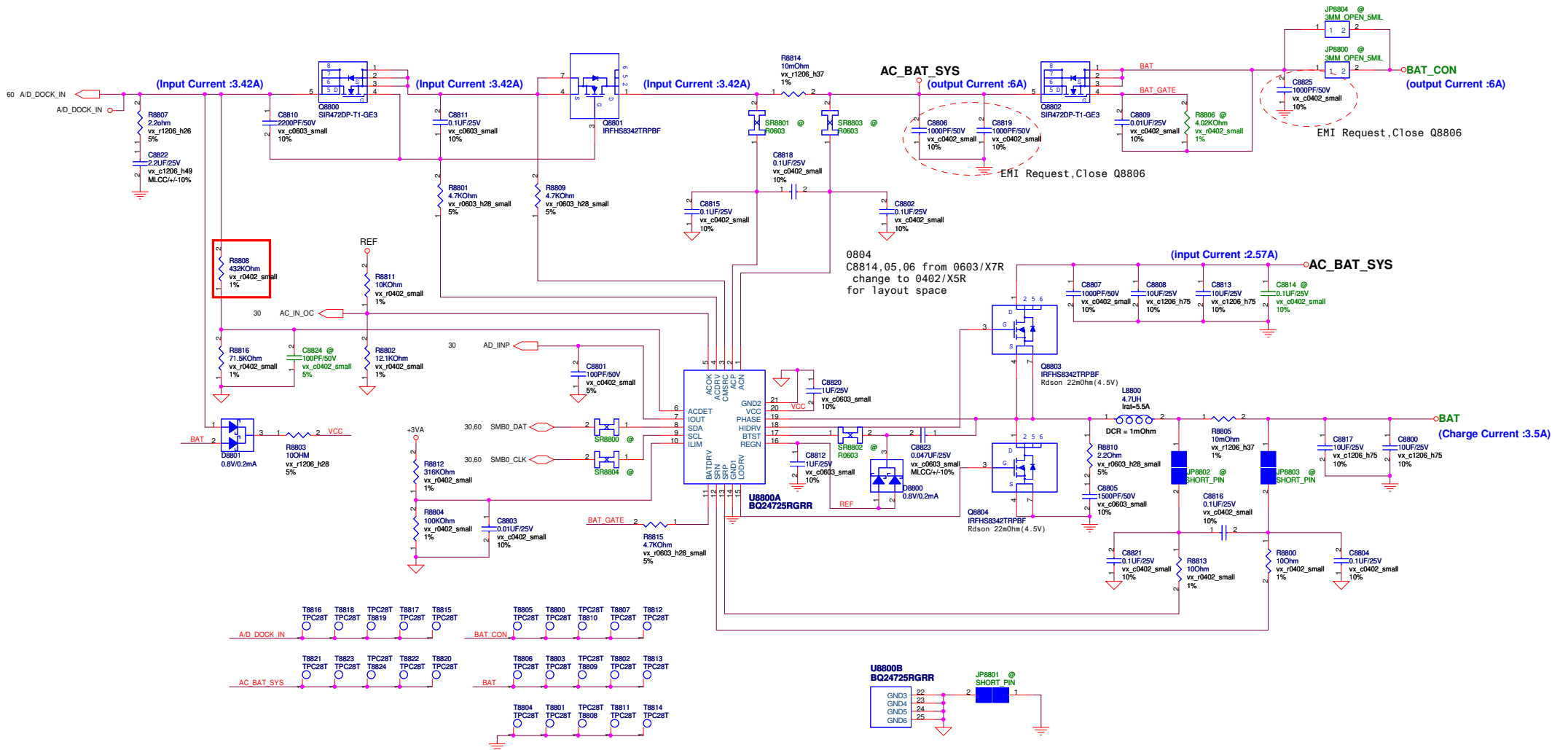
Engineer: *Clark Liang*

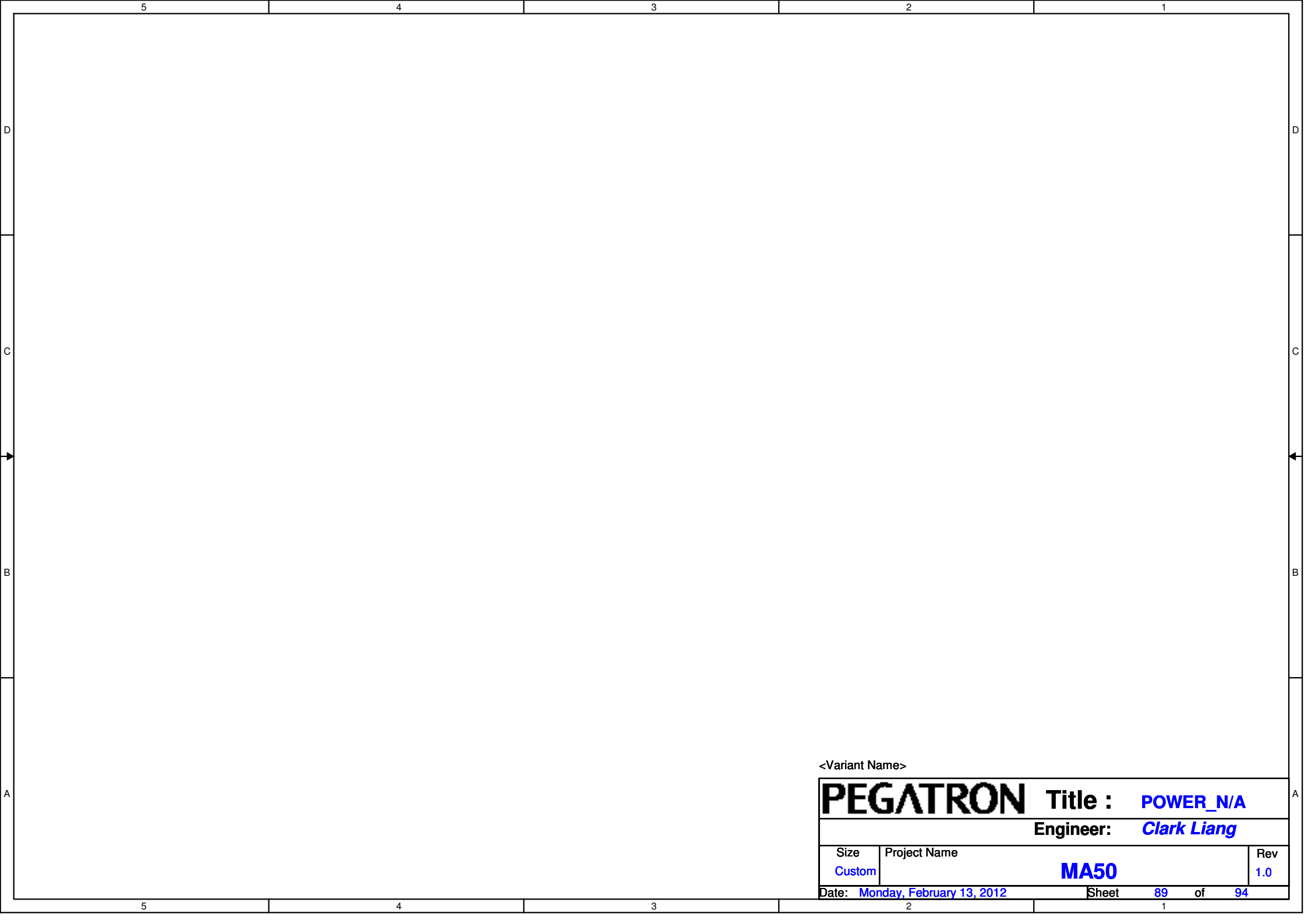
Size	Project Name	Rev
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Custom	MA50	1.0
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Date: Monday, February 13, 2012 Sheet 87 of 94

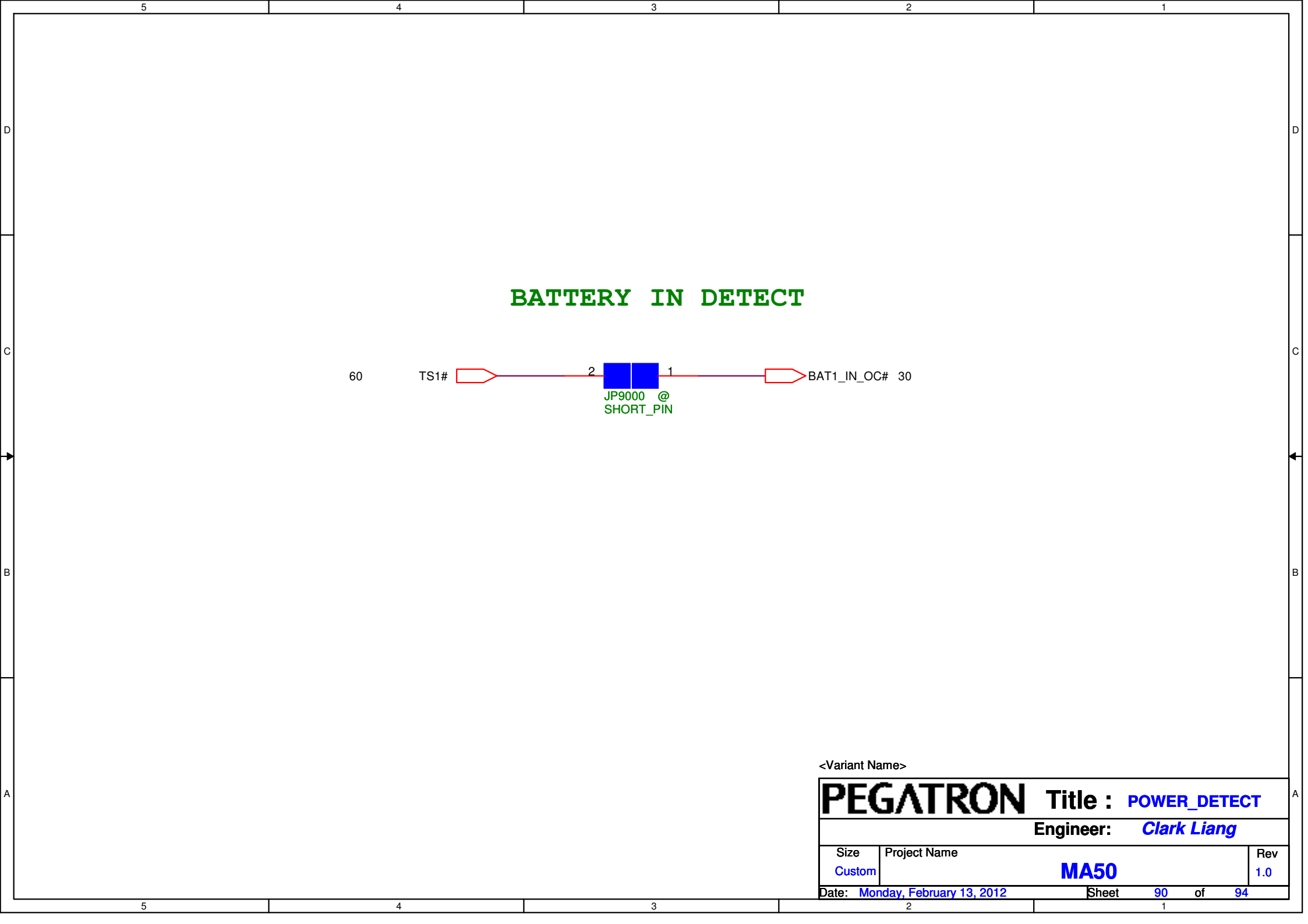
BATTERY CHARGER



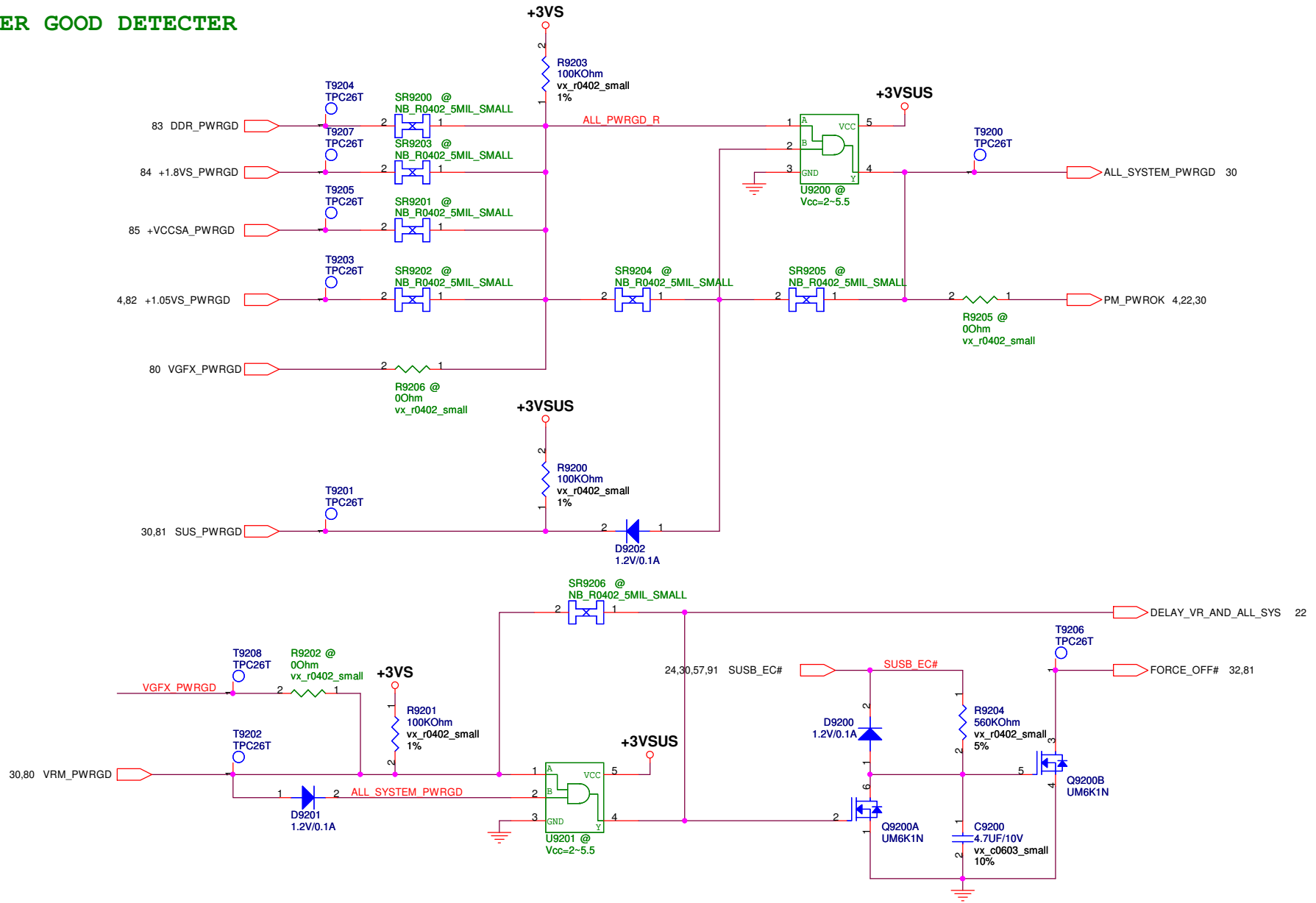


<Variant Name>

PEGATRON		Title : POWER_N/A	
		Engineer: Clark Liang	
Size	Project Name		Rev
Custom	MA50		1.0
Date: Monday, February 13, 2012		Sheet	89 of 94



POWER GOOD DETECTOR

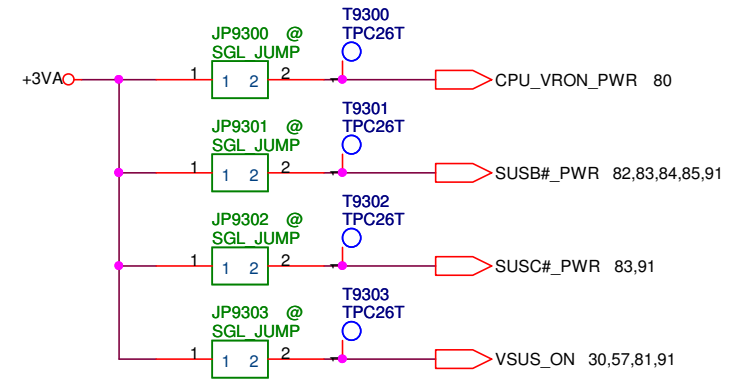


<Variant Name>

PEGATRON		Title : POWER_PROTECT	
		Engineer: Clark Liang	
Size Custom	Project Name MA50	Rev 1.0	
Date: Monday, February 13, 2012		Sheet 92 of 94	

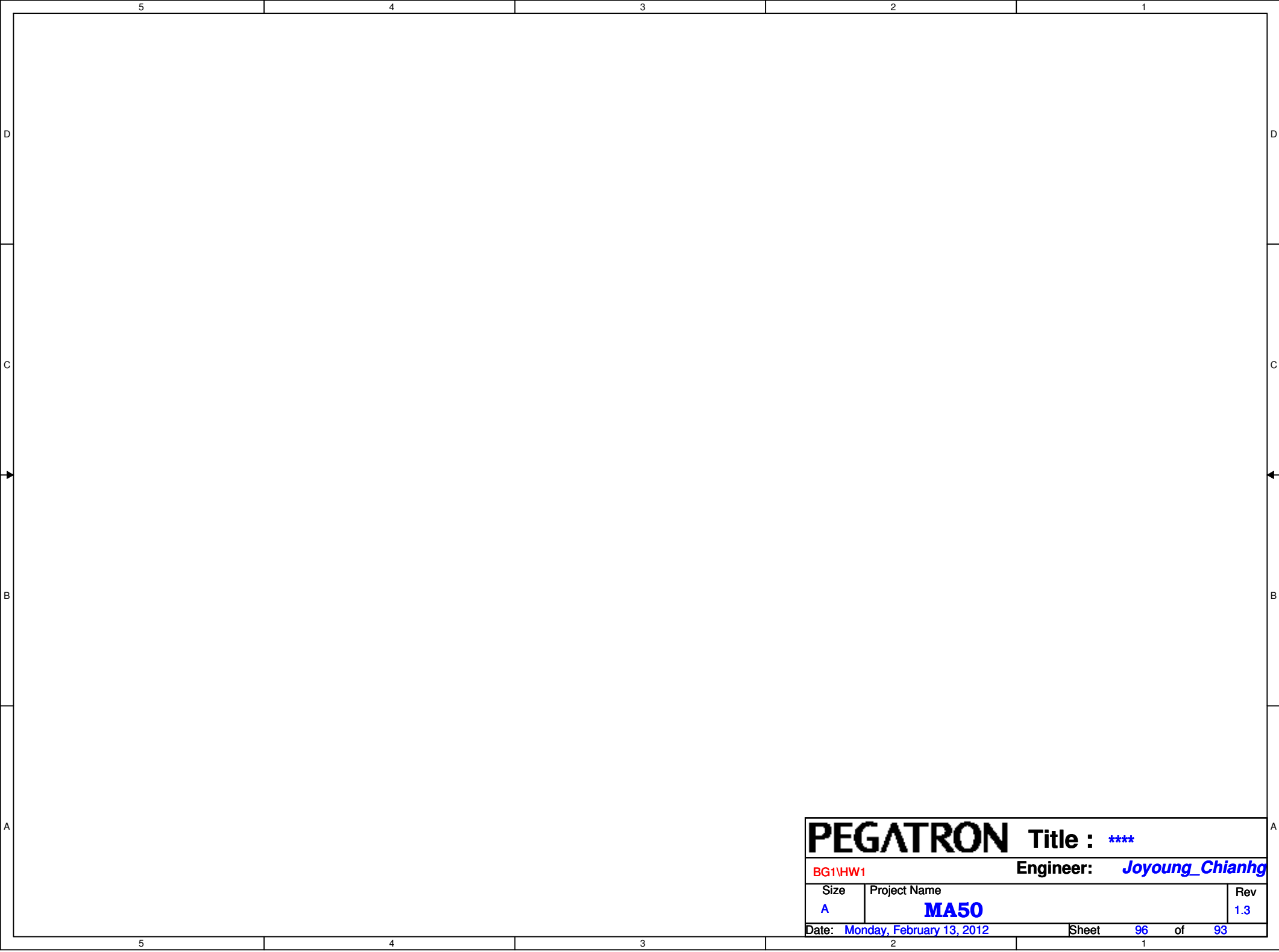
AC_BAT_SYS	AC_BAT_SYS	45,53,81,87,88
BAT	BAT	88
BAT_CON	BAT_CON	60,88
+5VA	+5VA	37,60,81,91
+3VA	+3VA	6,20,26,27,30,31,57,59,60,81,88
+5VO	+5VO	52,65,80,81,82,83,85,91
+3VO	+3VO	53,81,84,85,91
+1.8VO	+1.8VO	60,84
+1.5VO	+1.5VO	83,91
+1.05VO	+1.05VO	82,91
+0.75VO	+0.75VO	83
+12VSUS	+12VSUS	28,51,81,91
+5VSUS	+5VSUS	51,57,59,91
+3VSUS	+3VSUS	4,22,24,28,30,60,81,92
+12V	+12V	60,91
+5V	+5V	57,59,60,91
+3V	+3V	24,45,57,59,61,91
+1.5V	+1.5V	5,16,17,18,57,60,83
+12VS	+12VS	28,36,48,91
+5VS	+5VS	27,36,37,48,50,51,57,80,87,91
+3VS	+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+1.8VS	+1.8VS	7,25,26,57,80,84
+1.5VS	+1.5VS	7,26,53,57,91
+1.05VS	+1.05VS	26,27,57,82,87
+VCCSA	+VCCSA	7,85
+0.75VS	+0.75VS	16,17,57,83
+VCORE	+VCORE	6,9,11,80
+VGFX_CORE	+VGFX_CORE	7,9,80
+12VS_VGA	+12VS_VGA	60,91
+3VS_VGA	+3VS_VGA	57,70,72,74,75,87,91
+1.5VS_VGA	+1.5VS_VGA	57,71,75,76,77,91
+1.05VS_VGA	+1.05VS_VGA	57,70,71,72,91

FOR POWER TEST



<Variant Name>

PEGATRON		Title : POWER_SIGNAL	
		Engineer: Clark Liang	
Size	Project Name		Rev
Custom	MA50		1.0
Date: Monday, February 13, 2012		Sheet	93 of 94



PEGATRON			Title : ****		
BG1\HW1			Engineer: Joyoung_Chianhg		
Size	Project Name				Rev
A	MA50				1.3
Date: Monday, February 13, 2012			Sheet	96	of 93

SR BOM change

- SR1.1 Un-mount Q5602, Q5601 and mount R5323 and R5310
- SR1.2 CE5001 un-mount
- SR1.3 L3602 mount
- SR1.4 R7005 un-mount
- SR1.5 R7410 change 10K ohm
- SR1.6 R4504 change 10K ohm for LVDS backlight
- SR1.7 R7430, R7432, R7433 un-mount
- SR1.8 R7608, R7611 change 162 ohm

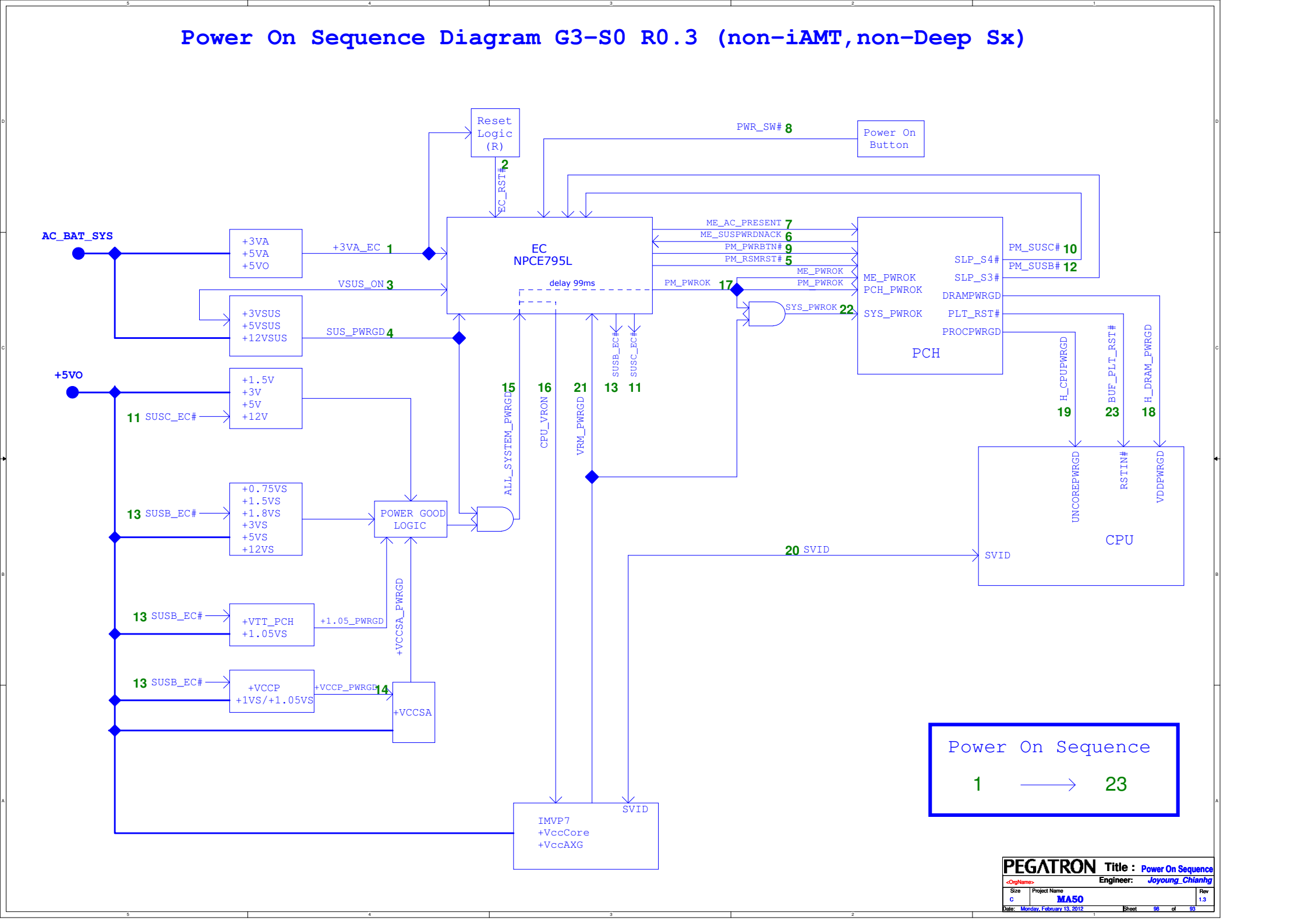
ER

- ER1.1 PI pin connect to ESD and VDD pin reserve 0.1 uF cap
- ER1.2 Add diode and reserve 0 ohm for AC adapter plug in /out voice
- ER1.3 U5201 change G547G1P81U for Desing IP
- ER1.4 Add Card Reader LED
- ER1.5 J3701, J3702, J4601, J5201, J5304,J5001 chang connector
- ER1.6 R6505~R6508 change 0603 size
- ER1.7 D4801 contact to 2.2K ohm for EA solution in HDMI issue
- ER1.8 CPU_THERM# contact to FORCE_OFF#
- ER1.9 RTC battery connector (J2001)Pin1, Pin2 swap
- ER1.10 D3707, D4618, D5201, D5301, D6502, D6503, D6802 VDD pin reserve 0.1 uF cap
- ER1.11 R3720 R3721 change 51ohm for consumer spec in HP
- ER1.12 L4601, L4602, L4603 change 27nH and add C4622, C4623, C4624 for EA solution in CRT
- ER1.13 L5301, L5302, L5306 change 0 ohm and L5305 change short pin, C5321, C5327,C5307, C5322, C5315, C5305, C5313 change umount
- ER1.14 Change R4566 from 300(0603) to 150(0402) for LVDS power sequence solution
- ER1.15 USB port 0 and port 1 swap
- ER1.16 Vcore_add CE8002&CE8006 to replace CE0601&CE0602
- ER1.17 VGFX_CORE(IGPU) add CE8007 to replace CE0705
- ER1.18 reserve M_VREF schematic
- ER1.19 Reserve C2623, C2624, C4514, C4515 for WLAN solution
- ER1.20 Reserve C4510, C4512, C4513 for 3G and L6002~L6004, L4502 change 47 ohm Bead
- ER1.21 C6007, C6006 mount for WLAN
- ER1.22 RN3002 change 2R4P
- ER1.23 LED and BT schematic change to LED board
- ER1.24 LED power change 5VSUS, so R5618, R5616, R5623 change 560 ohm
- ER1.25 VRAM change co-lay footprint
- ER1.26 Reserve C5601, C5602, C5603, C6356, C6357 to 47pF for RF request
- ER1.27 Reserve C4516, C4517 to 10pF for RF request
- ER1.28 U6504,U6505 change AZ3028 for EMI request
- ER1.29 D6401, D6501, D6502 change ESD AZ5023 in for EMI request in LAN function
- ER1.30 Add C6010 C6011 for EMI request
- ER1.31 Merge Q6704 and remove U6704
- ER1.32 D3720 change to mount for EMI request
- ER1.34 Reserve C6913(47PF), C6902(0.1uF), C6623(47PF), C6606(22uF) for 3G
- ER1.35 L6601=>0901-00HI000 FERRITE BEAD(1206)390 OHM/2A

PR

- PR2.1 RTC pin define swap

- PR_S01:Change C3627,C3626 from X5R to Y5V
- PR_S02:According with INTEL datasheet suggest.(Power circuit mount)
- PR_S03:To prevent 誤動作 PCIE Wake.
- PR_S04:To change WLAN LED control by MODULE then gate control by 3G LED.
- PR_S05:To change 3G LED control by MODULE.
- PR_S06:To prevent leakage current and mount R for cost down.
- PR_S07:RF reserve.
- PR_S08:Move P.U 10K near 3G connector.
- PR_S09:Change LED POWER rail from +5VSUS_LEDDDB(+5VSUS) to +5VA_LEDDDB(+5VA) .(To resolve Battery LL issue)
- PR_S10:Change LED POWER rail from +5VSUS_LEDDDB(+5VSUS) to +5V_LEDDDB(+5V)
- PR_S11:Del JP, +3VS_CR change Net name to +3VS
- PR_S12:ESD change solution ,Add U6512 ,Del C6509,D6501~3,U6502,U6503,D6401
- PR_S13:Change NET name to +3VS
- PR_S14:Change 10uF to 22uF for wave of CRT display.
- PR_S15:Add 10uF (C6803)for USB droop test.
- PR_S16:D5201 PIN Swap
- PR_S17:ME modify.(H6532,8,1,9,4,3,5,H6945),DEL H6944
- PR_S18:EMI add.
- PR_S19:Change to unmount for ME
- PR_S20:RF request.
- PR_S21:LED light fine-tune.
- PR_S22:BIOS request for UMA and DSC platform identifying.

[illegible]

Power On Sequence

1 → 23

Power On Sequence

1 → 23

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT, non-Deep Sx)

