

Compal Confidential

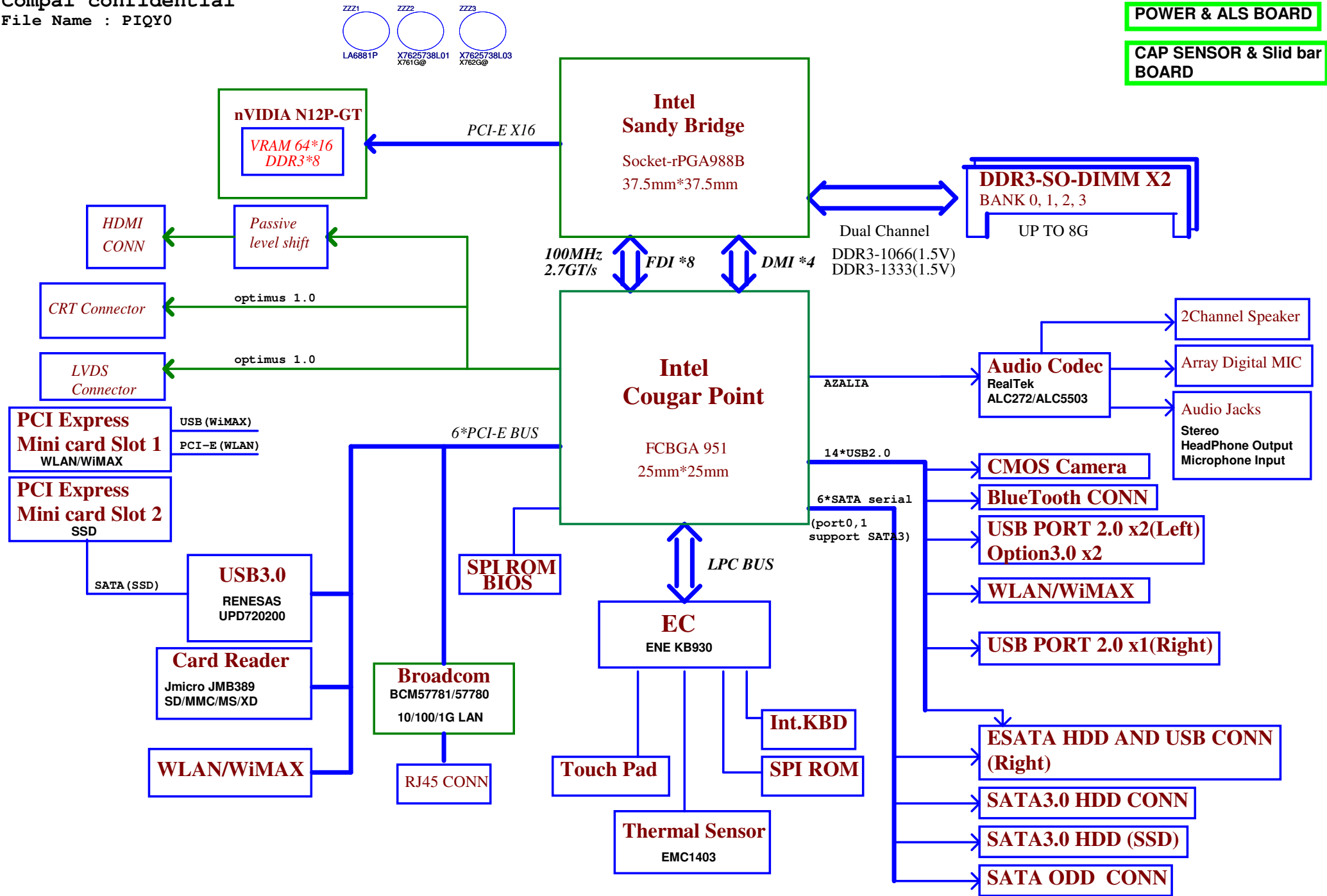
PIQY0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
nVIDIA N12P-GT

2010-11-26

REV: 0.3

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	
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				Size	Document Number
				Custom	PIQY0 LA6881P
				Date:	Monday, November 29, 2010
				Sheet	1 of 63
				Rev	0.3



Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0		○	○	○	○
S3		○	○	○	✗
S5 S4/AC		○	○	✗	✗
S5 S4/ Battery only		○	✗	✗	✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗

SMBUS Control Table

	SOURCE	VGA	BATT	KB930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	✗	✓ +3VALW	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	✗	✗	✗	✗	✗	✗	✓ +3VS
SMBCLK SMBDATA	PCH +3VALW	✗	✗	✗	✓ +3VS	✓ +3VS	✗	✗
SML0CLK SML0DATA	PCH +3VALW	✗	✗	✗	✗	✗	✗	✗
SML1CLK SML1DATA	PCH +3VALW	✓ +3VS	✗	✓ +3VS	✗	✗	✓ +3VS	✗

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
UMA	
UMA Only	UMA_ONLY@
Optimus	OPTI@
VRAM	X76@
HDMI	HDMI@
Blue Tooth	BT@
USB3.0	USB30@
ESATA	ESATA@
USB Charger	USB_CHG@
No USB Charger	NO_CHG@
Unpop	@
Codec ALC272	272@
Codec ALC5503	5503@
LAN 57781	57781@
LAN 57780	57780@
Ventura Feature	VENTURA@
Camera	CMOS@

VRAM BOM Config

X761G@: X7625738L01	Samsung 1GB
Sub: X7625738L02	Hynix 1GB
X762G@: X7625738L03	Samsung 2GB
Sub: X7625738L04	Hynix 2GB

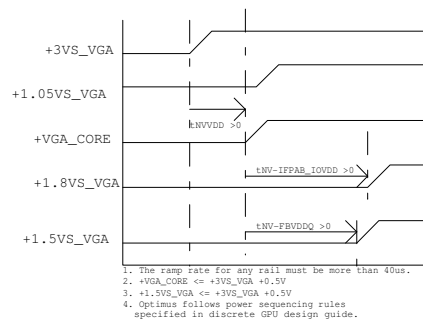
GPU BOM Config

N12P SKU:	OPTI@
GS SKU:	GS@
GT SKU:	GT@

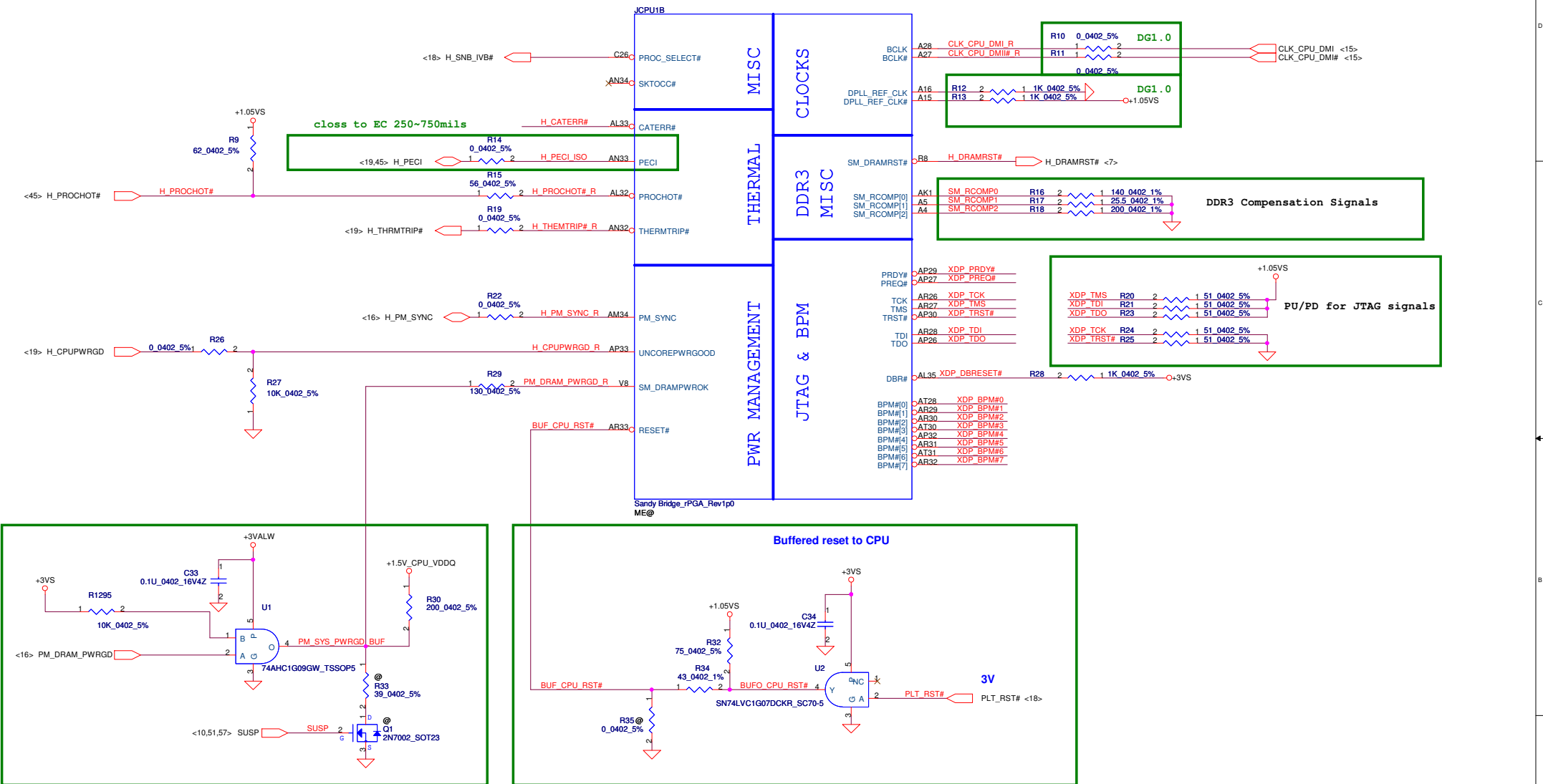
USB Port Table

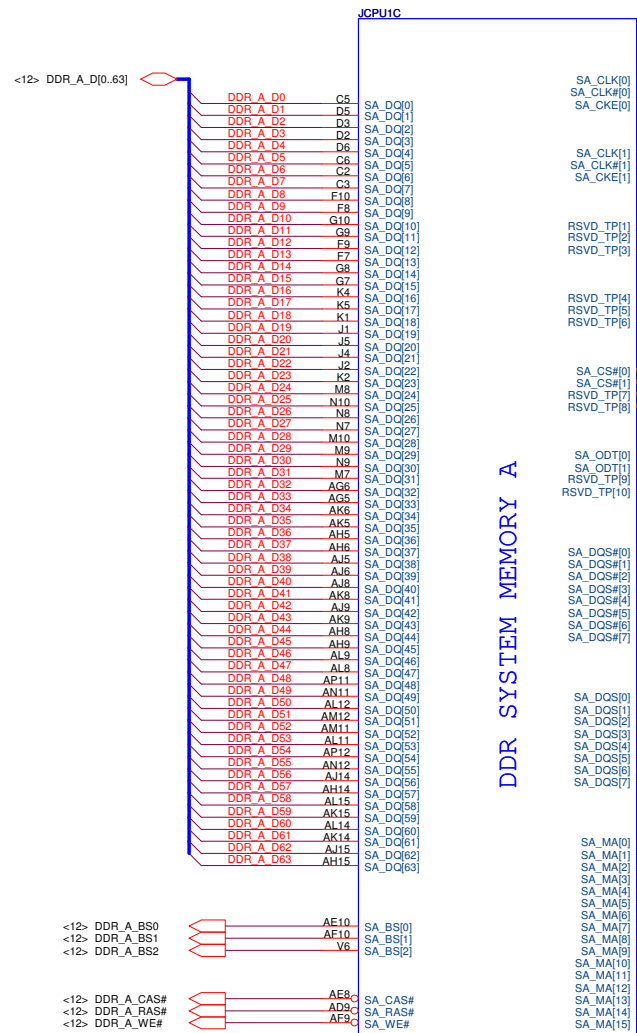
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/Cable (Right Side)
		1	USB Port (Right Side COMBO)
	UHCI1	2	USB/B (Left Side)
		3	USB/B (Left Side)
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	Blue Tooth

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				Date:	Monday, November 29, 2010
				Sheet	3 of 63
				Rev	0.3

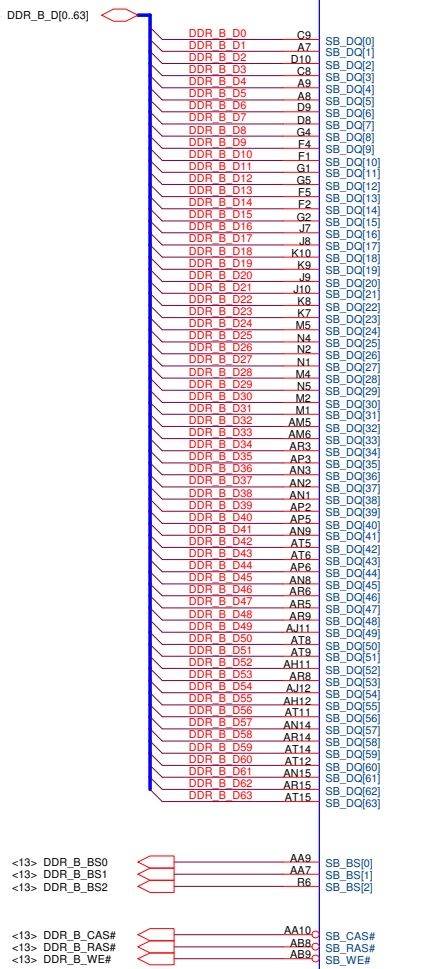
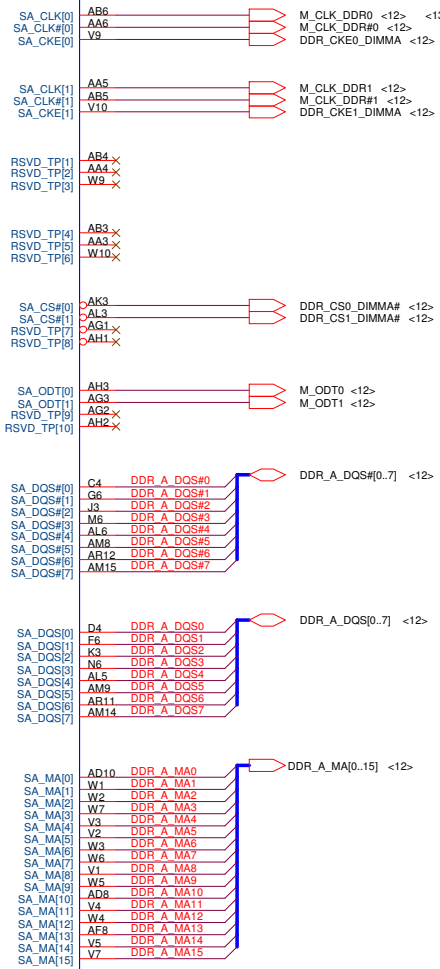


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				Document Number	0.3
				PIQY0 LA6881P	
				Date: Monday, November 29, 2010	Sheet 4 of 63

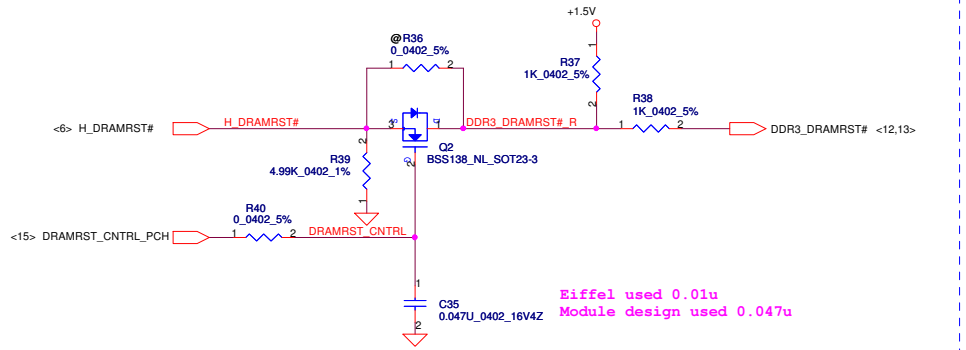
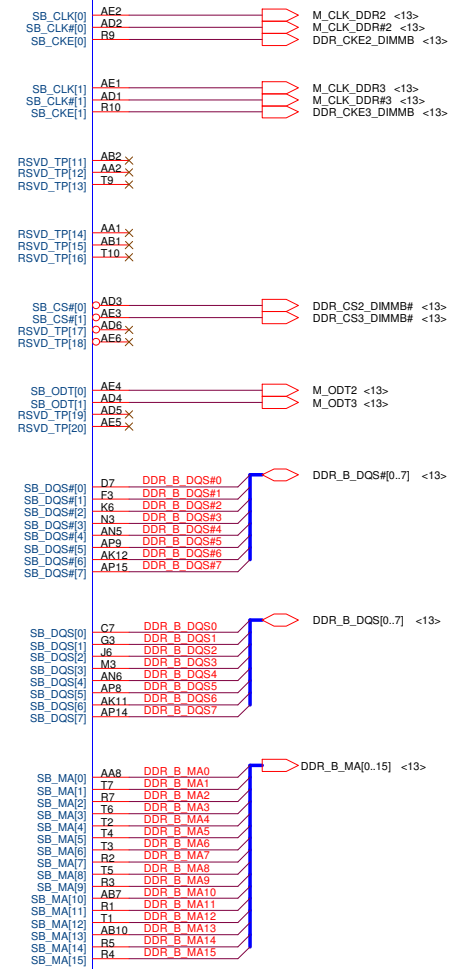




DDR SYSTEM MEMORY A



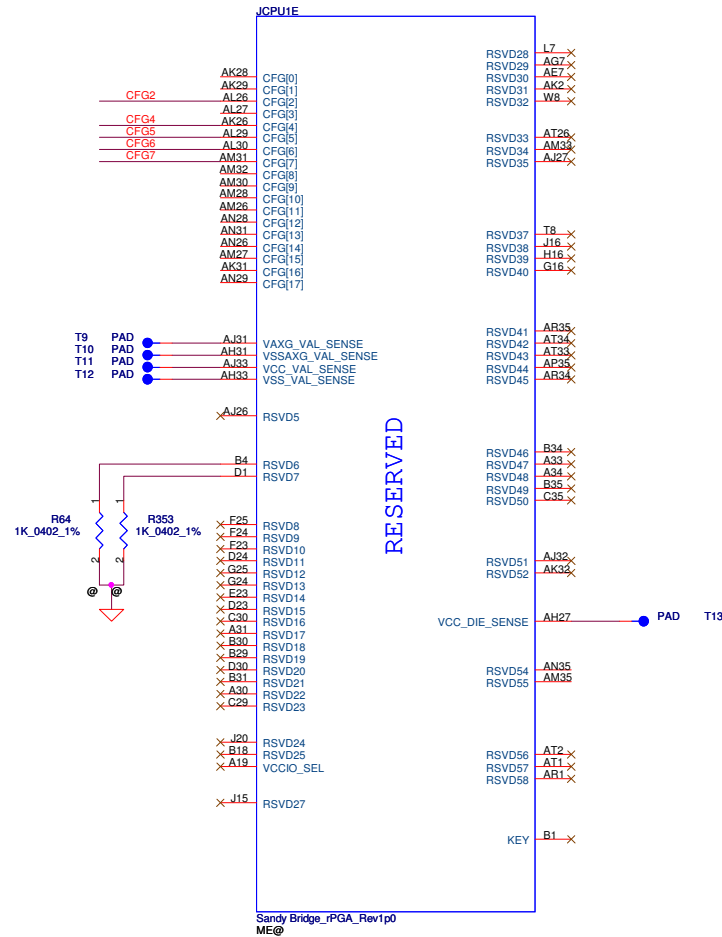
DDR SYSTEM MEMORY B



Eiffel used 0.01u
Module design used 0.047u

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		Size		Document Number						Rev	
		Customer		PIQY0 LA6881P						0.3	
		Date:		Monday, November 29, 2010		Sheet		7		of 63	

CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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				PROCESSOR(47) RSVD,CFG			
				Size		Document Number	Rev
				PIQY0 LA6881P		0.3	
Date:				Monday, November 29, 2010		Sheet 8 of 63	

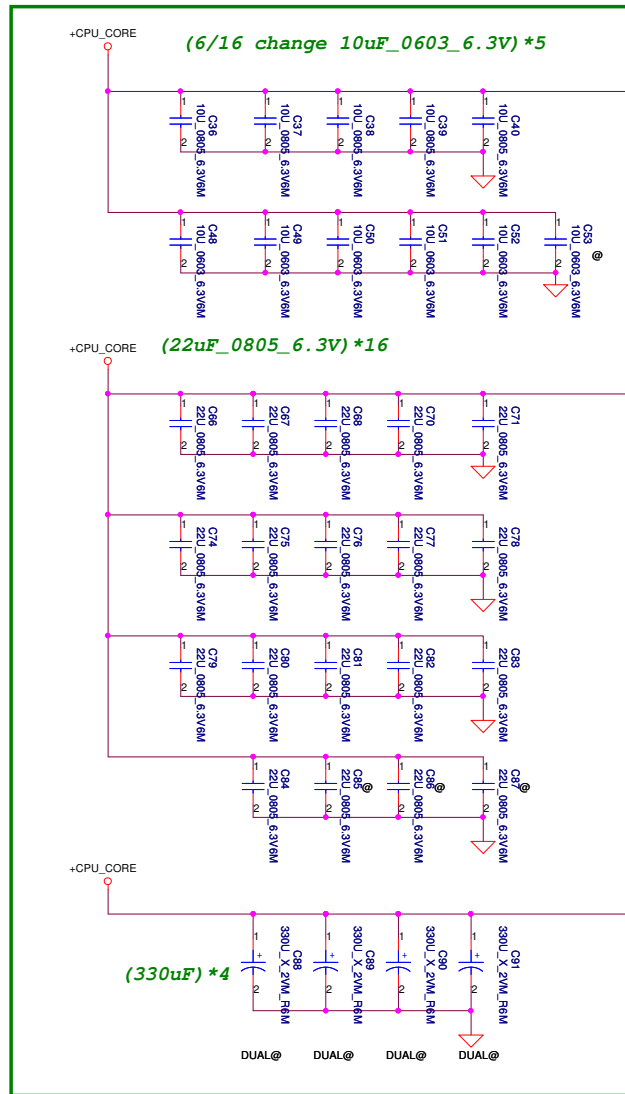
POWER

CORE SUPPLY

SVID

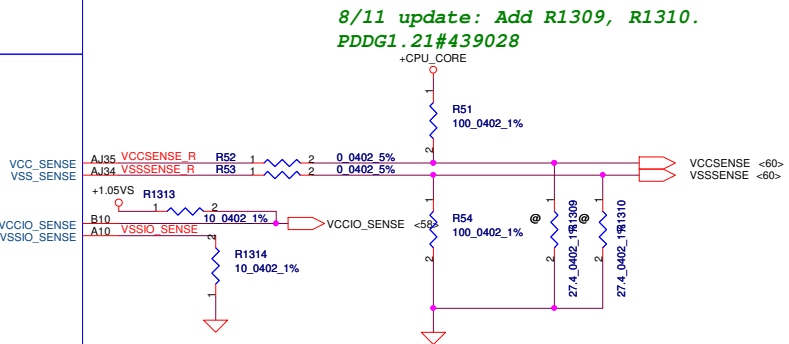
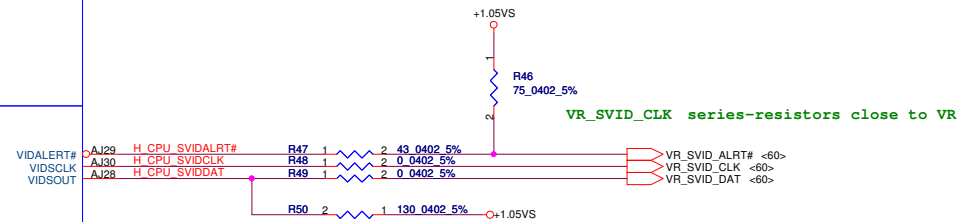
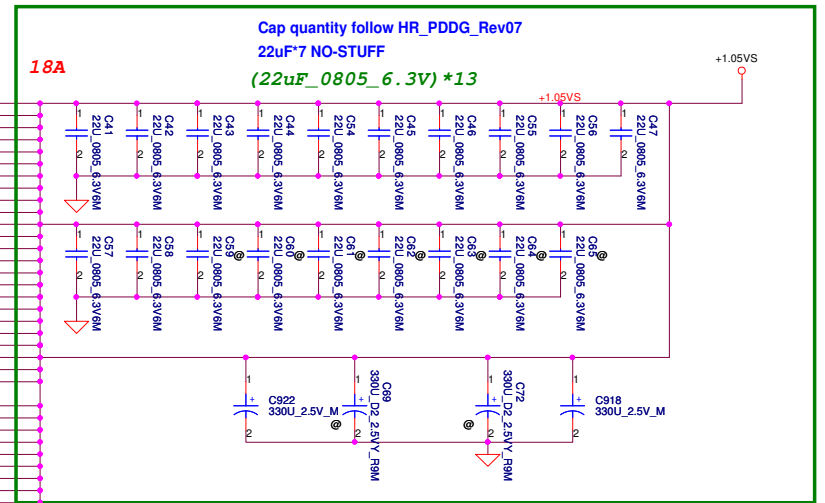
SENSE LINES

PEG AND DDR



QC=94A
DC=53A

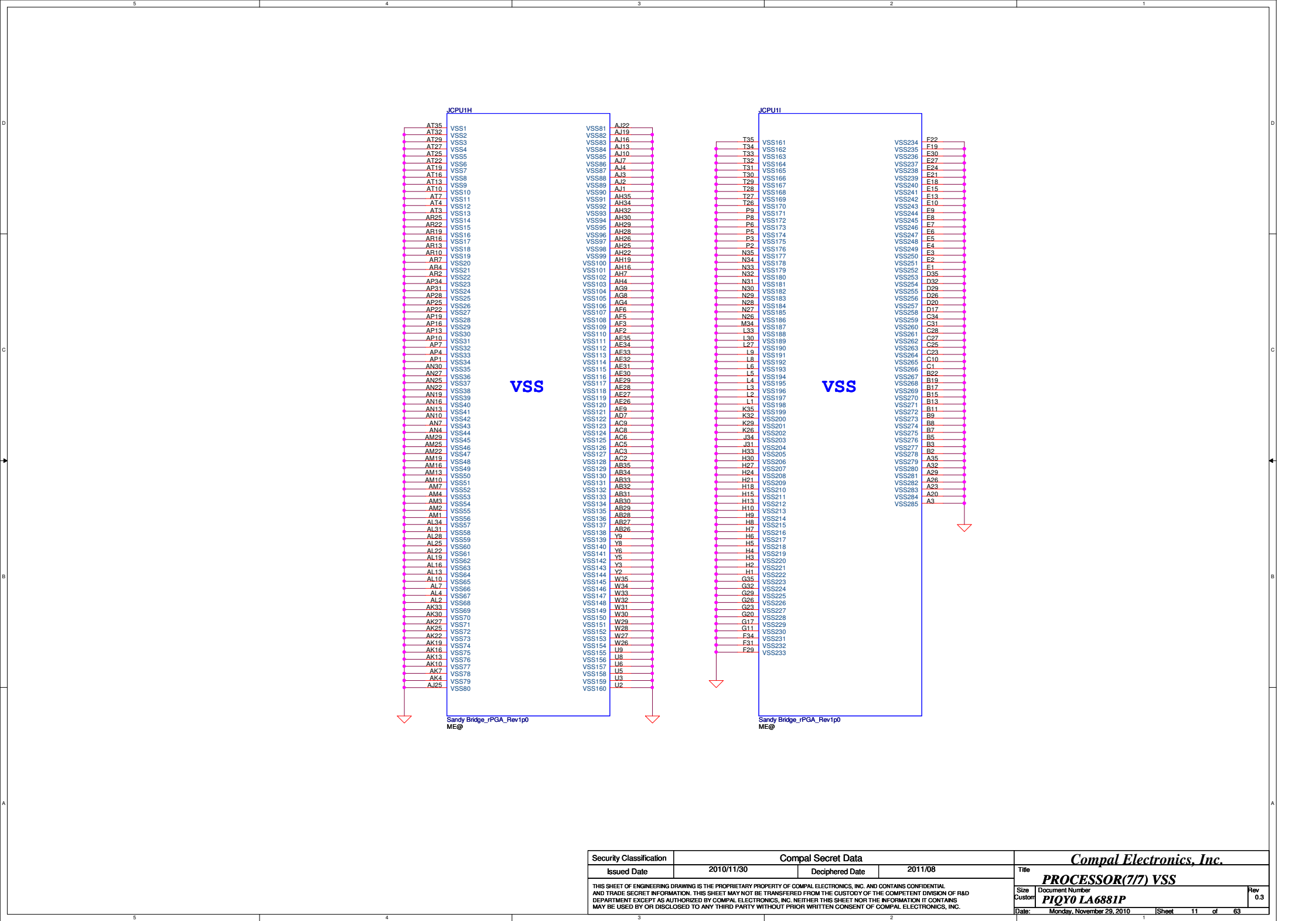
AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
Y35	VCC50
Y34	VCC51
Y33	VCC52
Y32	VCC53
Y31	VCC54
Y30	VCC55
Y29	VCC56
Y28	VCC57
Y27	VCC58
Y26	VCC59
Y25	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

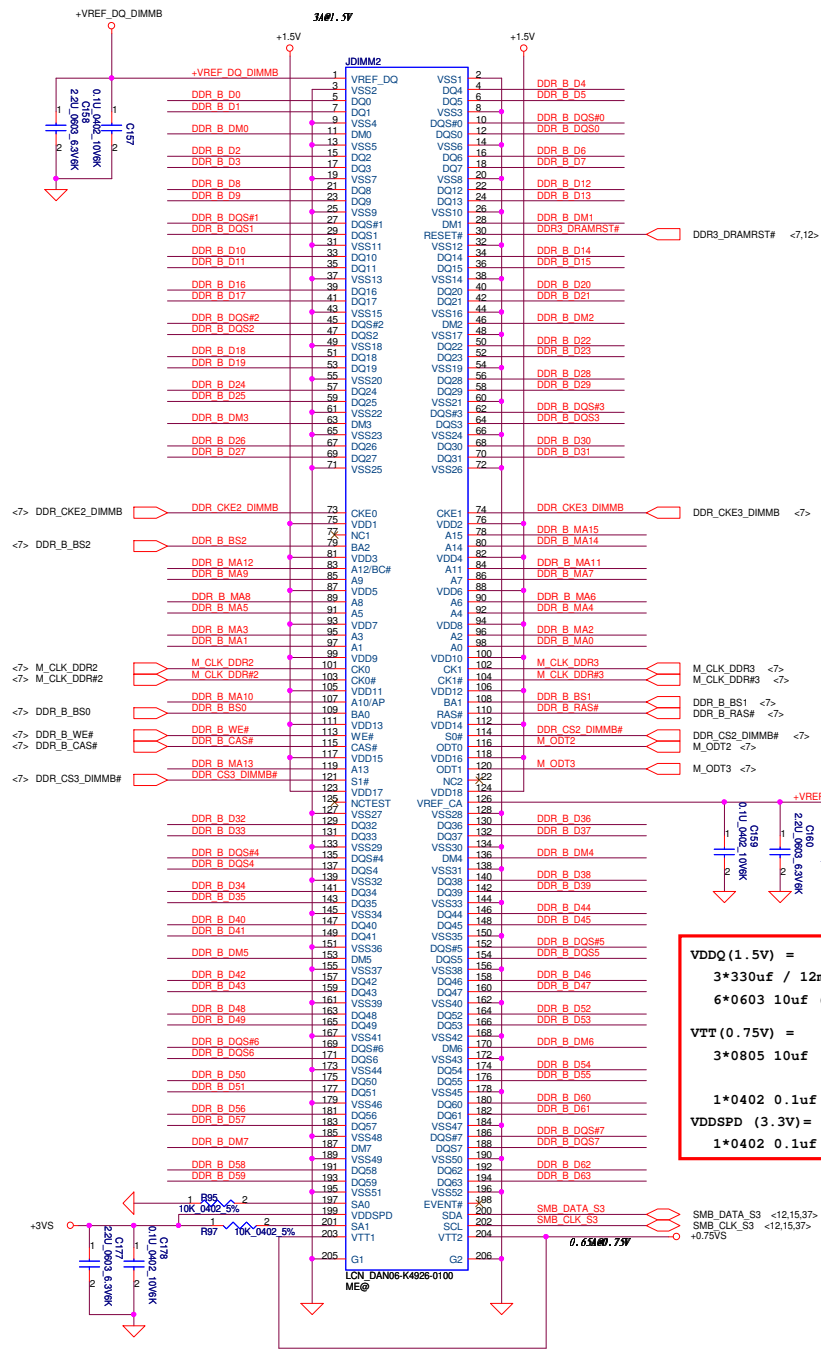


Sandy Bridge_rPGA Rev1.0
ME

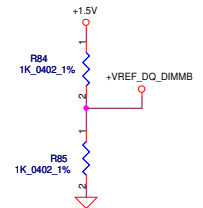
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PROCESSOR(5/7) PWR,BYPASS	
Size	Document Number
Custom	PIQY0 LA6881P
Date:	Monday, November 29, 2010
Sheet	9 of 63
Rev	0.3





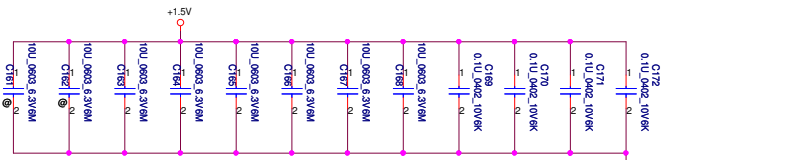
<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_DQS#0..7
<7> DDR_B_MA[0..15]



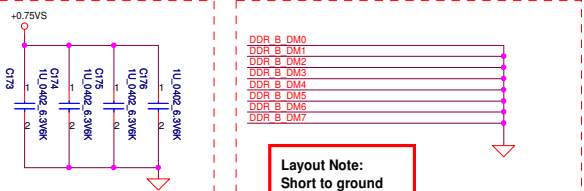
For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4



Layout Note:
Place near DIMM



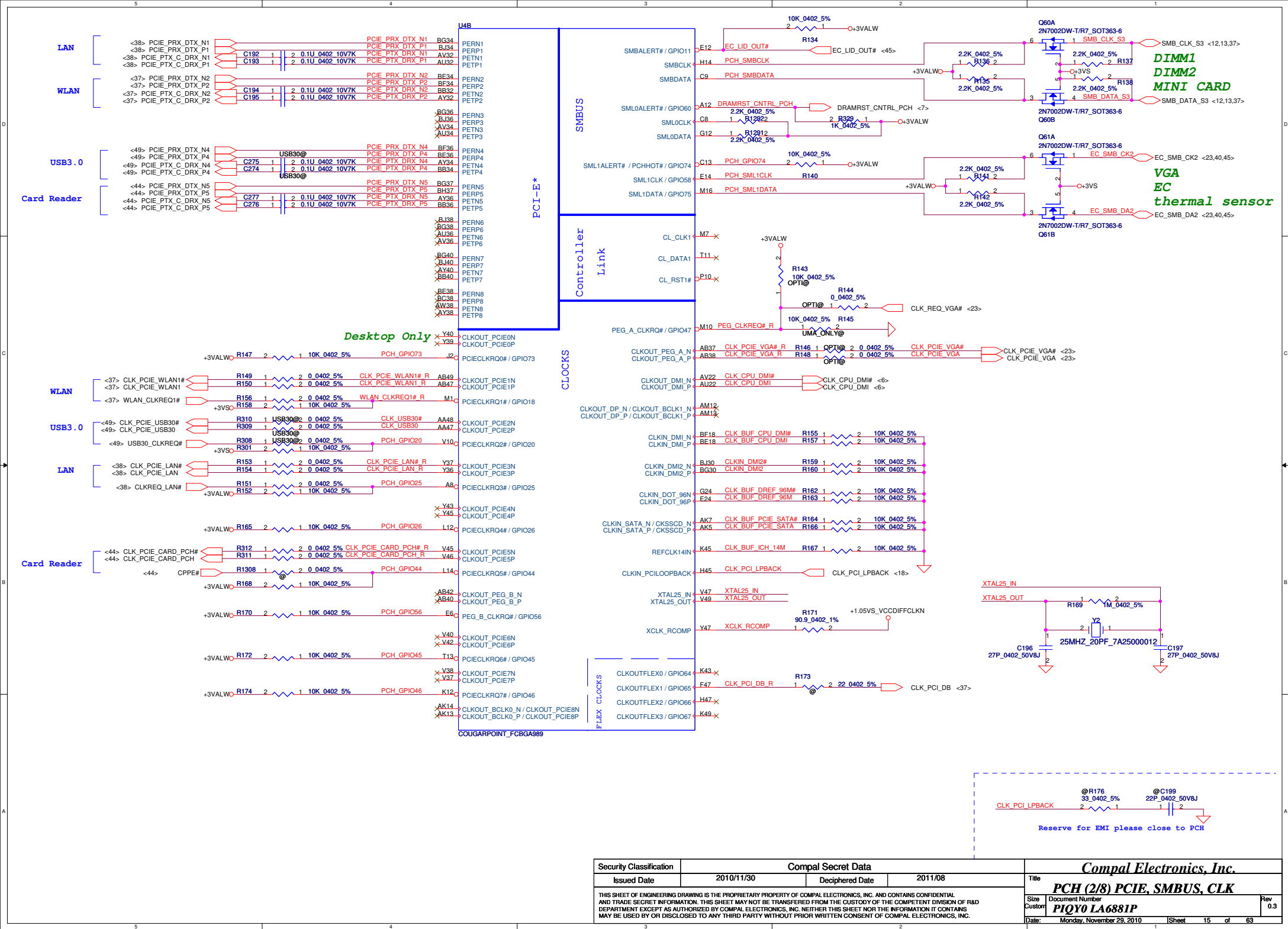
Layout Note:
Short to ground

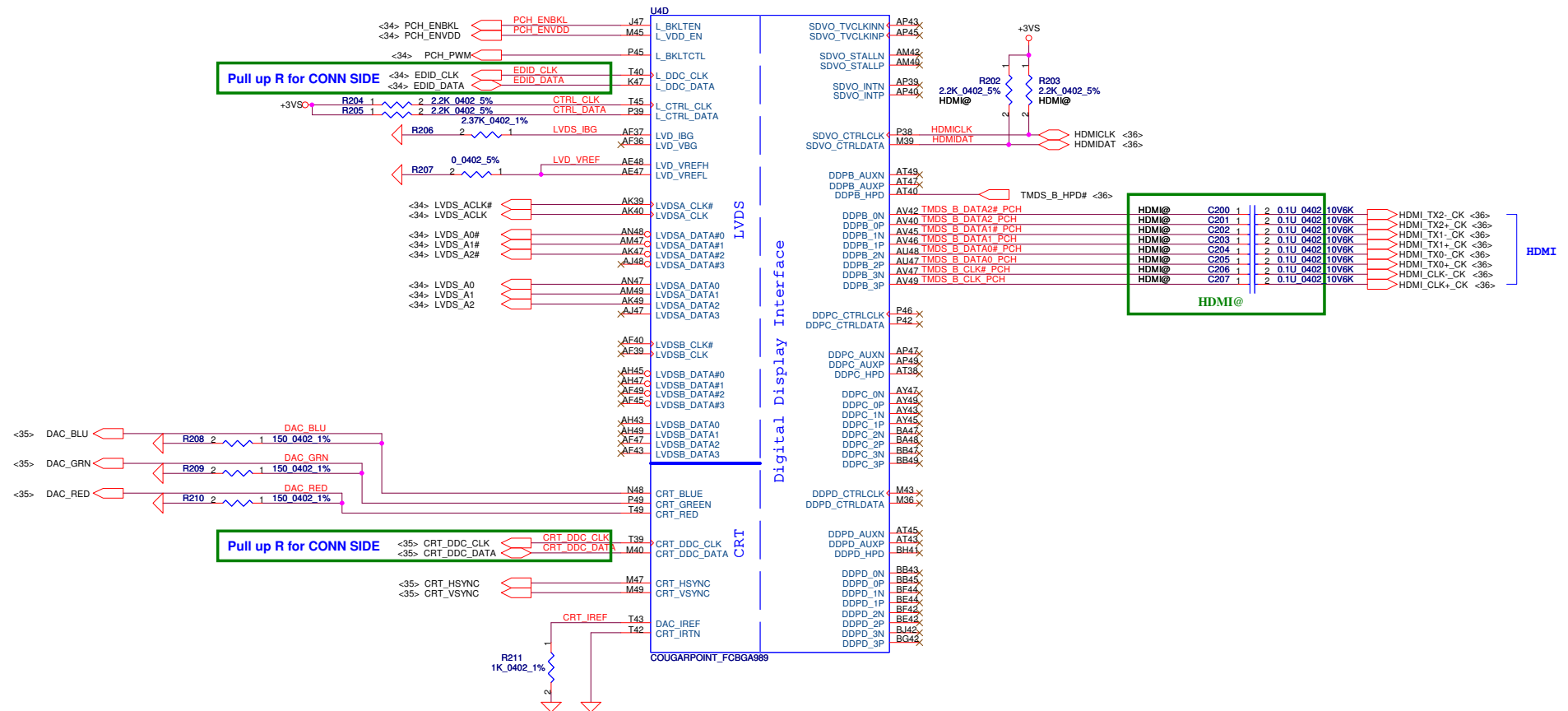
VDDQ (1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

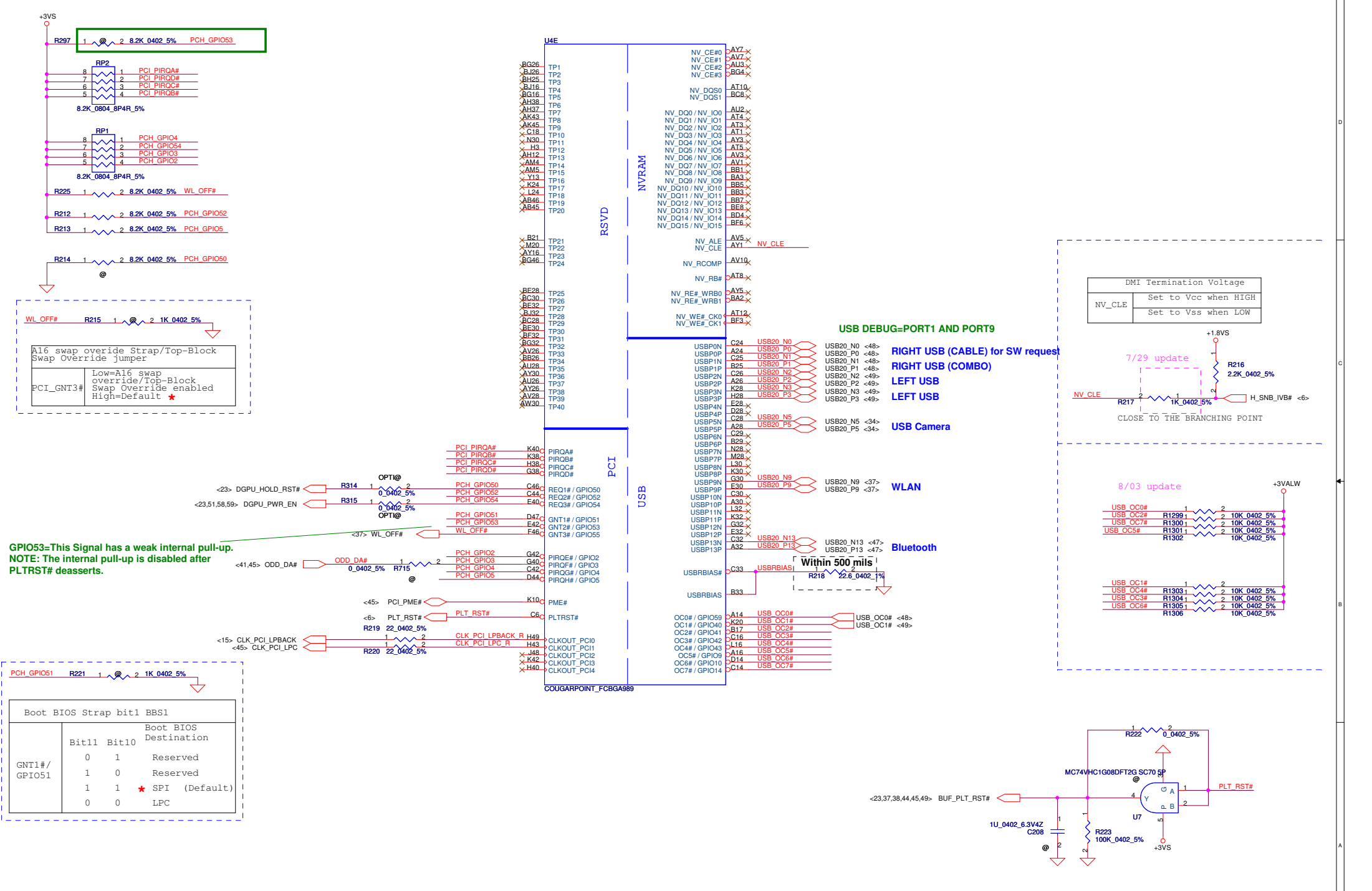
VTT (0.75V) =
3*0805 10uf 4*0402 1uf

VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf
1*0402 0.1uf 1*0402 2.2uf

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Size		Document Number		PIQY0 LA6881P	
Date		Monday, November 29, 2010		Sheet 13 of 63	
				Rev 0.3	







6/24 Change to @ follow module design and double check on module design meeting

ICC_EN#
Integrated Clock Chip Enable
H ; Disable
L ; Enable
★
R235 1 @ 2 1K 0402 5% EC_SMI# <37,38,44> DEVICE_RST#
Weak internal pull-high

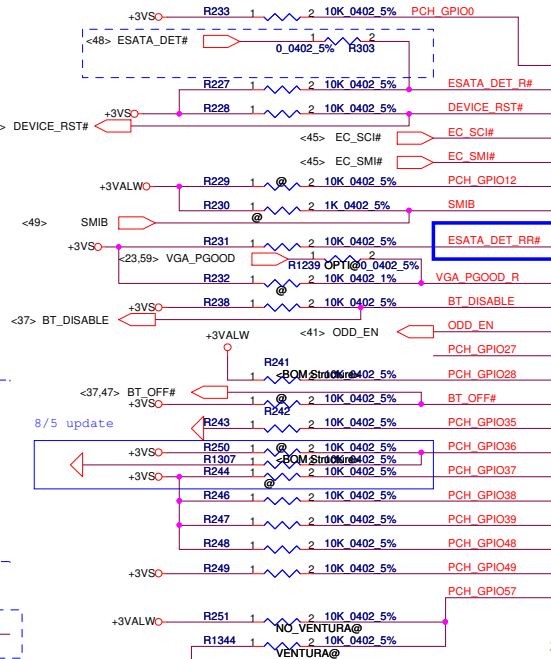
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 1 @ 2 1K 0402 5% PCH_GPIO28

PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable
R245 1 @ 2 10K 0402 5% PCH_GPIO27

7/29 update for ESATA detect
<48> ESATA_DET# 0_0402_5% ESATA_DET_RR#
R1294

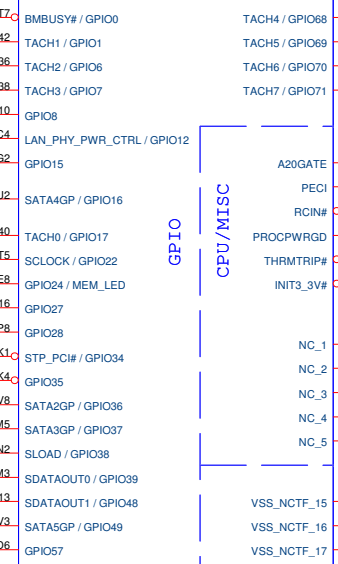
0812 Checklist Rev.1.2
When Unused as GPIO or SATA*GP - Use 8.2K-10K pull-down to ground.
R1311 1 @BOM Stock 10K 0402 5% PCH_GPIO37

7/29 update for ESATA detect



8/5 update

U4F



- × A4 VSS_NCTF_1
- × A44 VSS_NCTF_2
- × A45 VSS_NCTF_3
- × A46 VSS_NCTF_4
- × A5 VSS_NCTF_5
- × A6 VSS_NCTF_6
- × B3 VSS_NCTF_7
- × B47 VSS_NCTF_8
- × BD1 VSS_NCTF_9
- × BD49 VSS_NCTF_10
- × BE1 VSS_NCTF_11
- × BE49 VSS_NCTF_12
- × BF1 VSS_NCTF_13
- × BF49 VSS_NCTF_14

COUGARPOINT_FCBGA989

GPIO

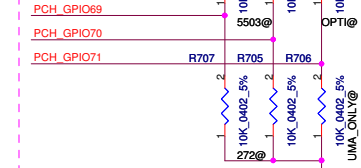
NCTF

CPU/MISC

- TACH4 / GPIO68 C40 PCH_GPIO68
- TACH5 / GPIO69 B41 PCH_GPIO69
- TACH6 / GPIO70 C41 PCH_GPIO70
- TACH7 / GPIO71 A40 PCH_GPIO71

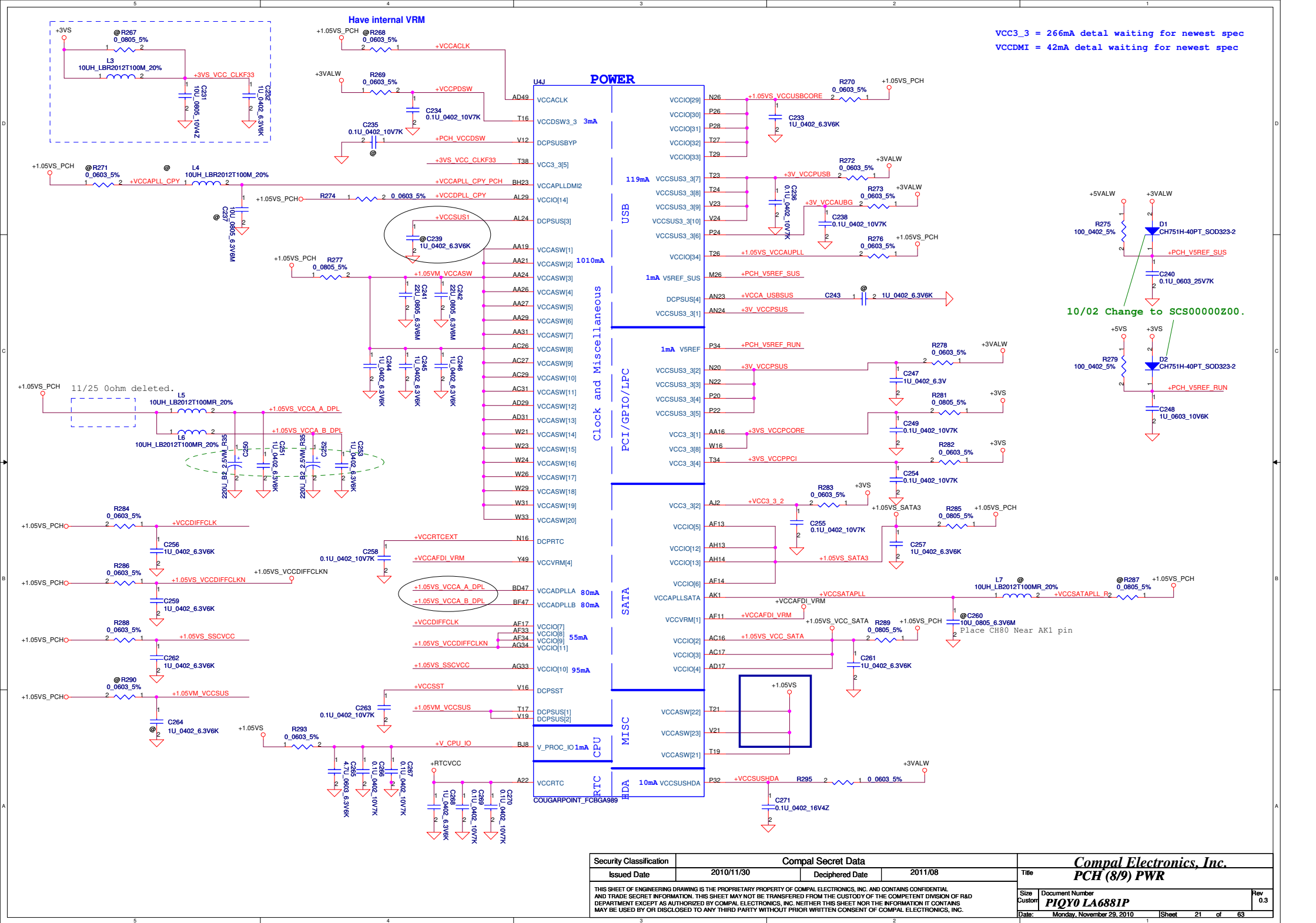
- A20GATE P4
- PECI AU16 PCH_PECI R 0_0402_5% R237 H_PECI <6,45>
- RCIN# P5 KB_RST# <45>
- PROCPWRGD AY11 H_CPUPWRGD <6>
- THRMTrip# AY10 PCH_THRMTrip# R 390_0402_5% R239 H_THRMTrip# <6>
- INIT3_3V# T14 PCH_THRMTrip#_R <23>
- NC_1 AH8
- NC_2 AK11
- NC_3 AH10
- NC_4 AK10
- NC_5 P37

- VSS_NCTF_15 BG2
- VSS_NCTF_16 BG48
- VSS_NCTF_17 BH3
- VSS_NCTF_18 BH47
- VSS_NCTF_19 BJ4
- VSS_NCTF_20 BJ44
- VSS_NCTF_21 BJ45
- VSS_NCTF_22 BJ46
- VSS_NCTF_23 BJ5
- VSS_NCTF_24 BJ6
- VSS_NCTF_25 C2
- VSS_NCTF_26 C48
- VSS_NCTF_27 D1
- VSS_NCTF_28 D49
- VSS_NCTF_29 E1
- VSS_NCTF_30 E49
- VSS_NCTF_31 F1
- VSS_NCTF_32 F49



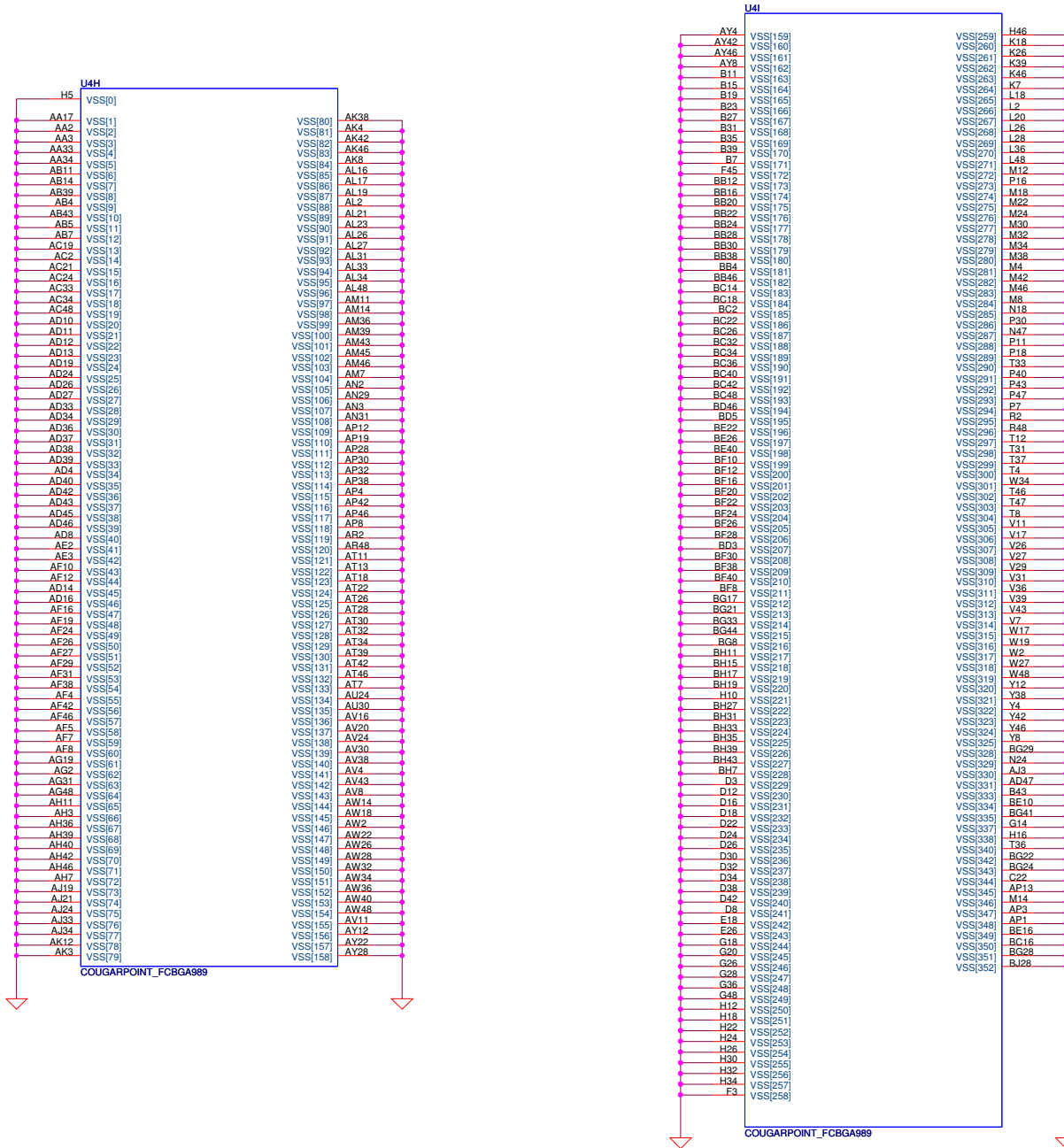
6/23 update for MB ID

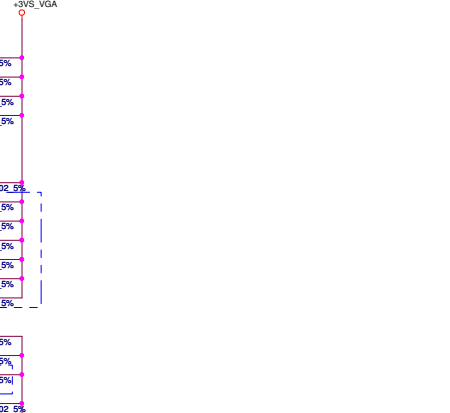
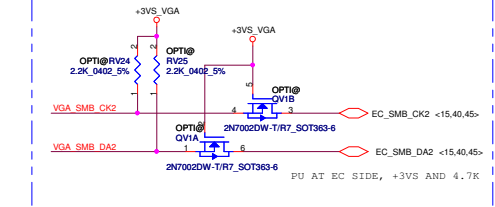
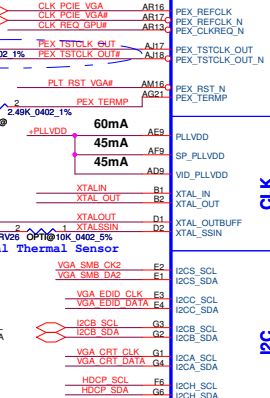
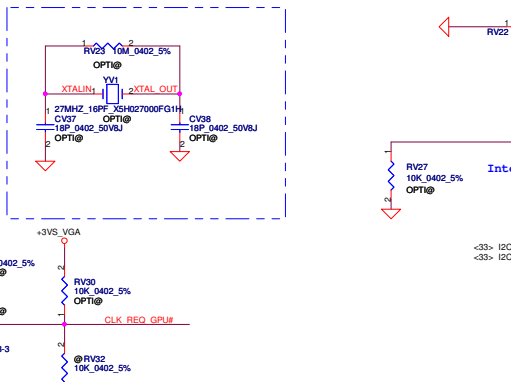
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	
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Size		Document Number		Rev	
Custom		PIQY0 LA6881P		0.3	
Date:		Monday, November 29, 2010		Sheet 19 of 63	



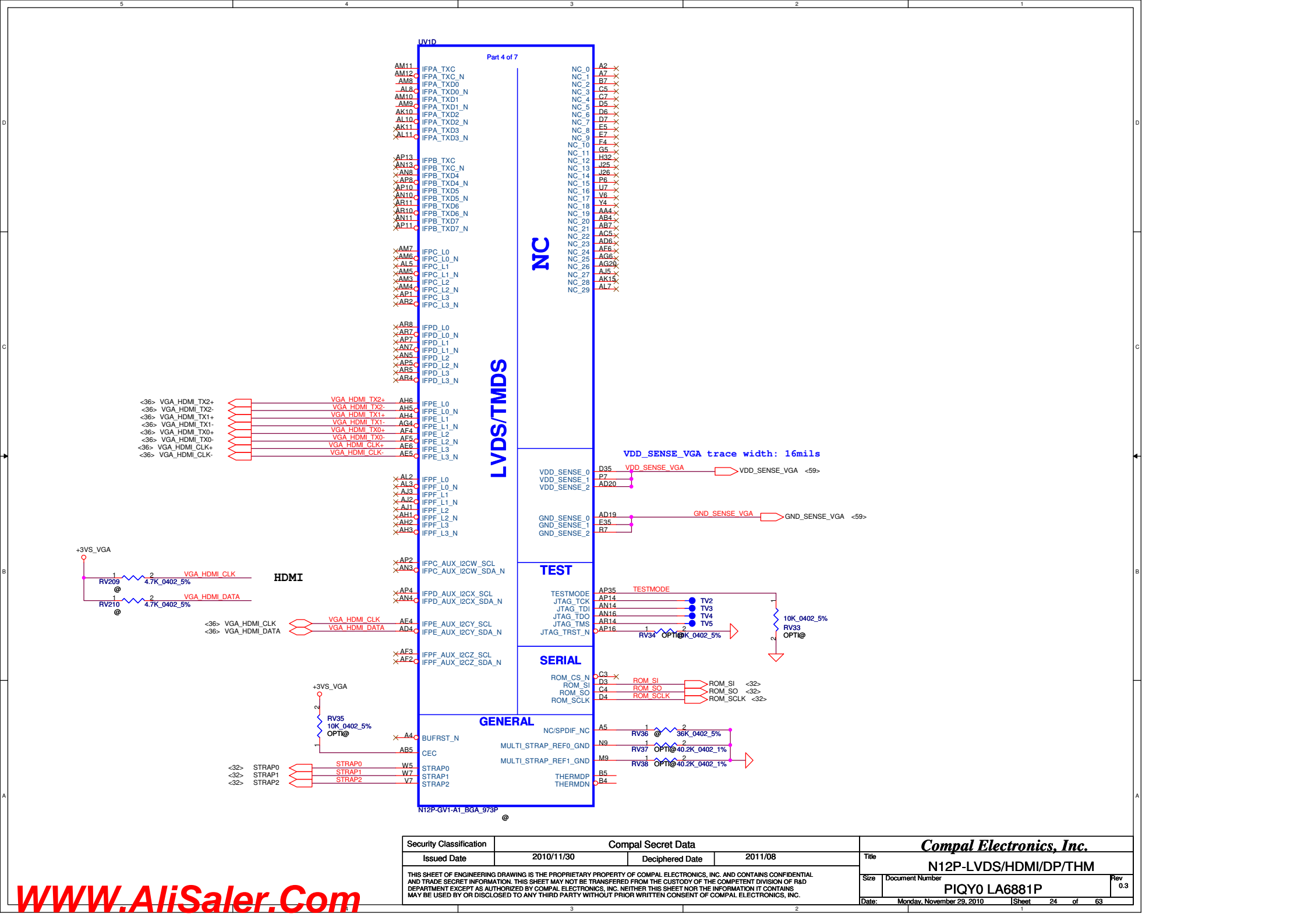
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>				
Issued Date		2010/11/30		Deciphered Date		2011/08		
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				PCH (9/9) VSS				
				Size	Document Number		Rev	
				PIQY0 LA6881P		0.3		
				Date:		Monday, November 29, 2010		Sheet 22 of 63

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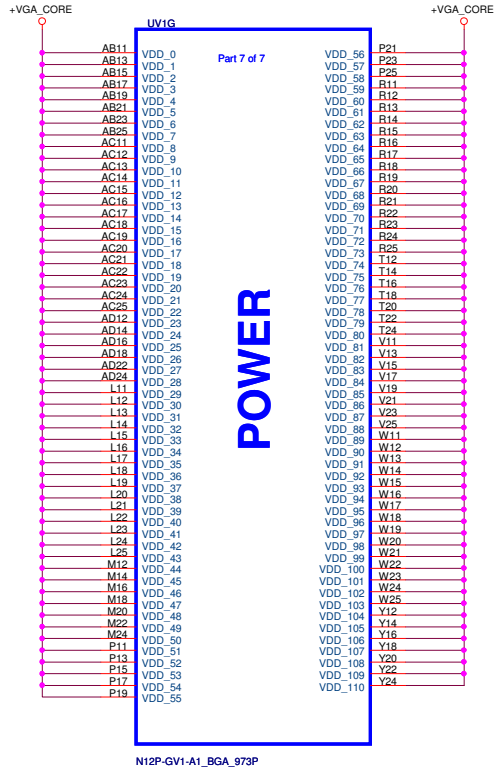




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				Document Number	0.3
				PIQYO LA68811P	
Date:		Monday, November 23, 2010		Sheet	23 of 63

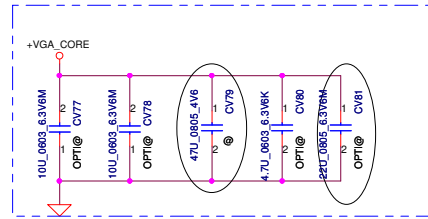


30.54A (41.02A Peak)

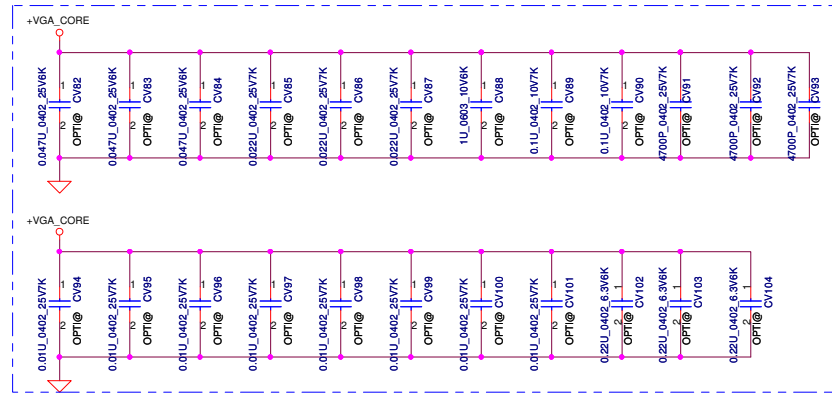


POWER

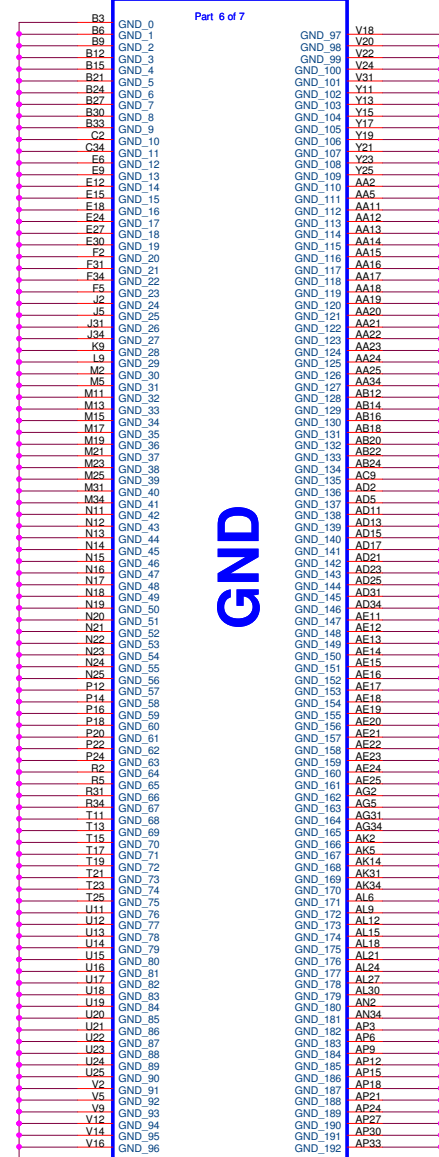
Near GPU



Under GPU



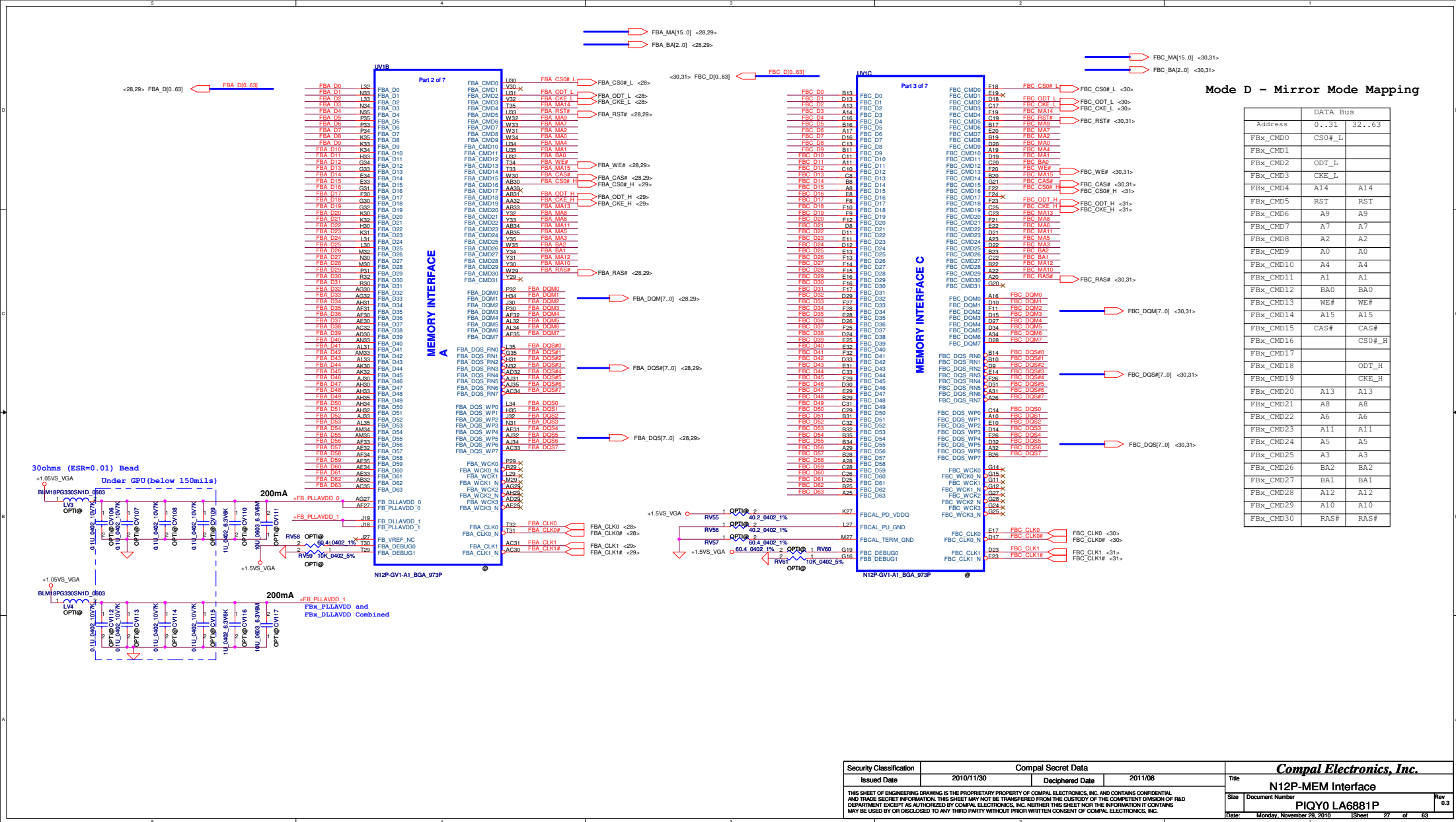
UVIF



GND

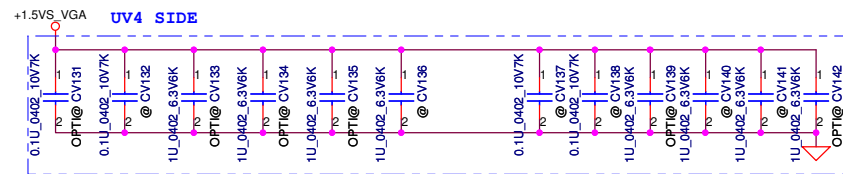
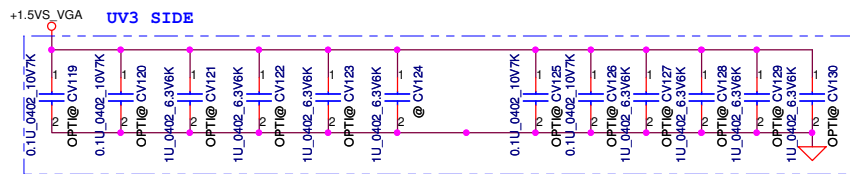
N12P-GV1-A1_BGA_973P

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				Date:	Monday, November 29, 2010



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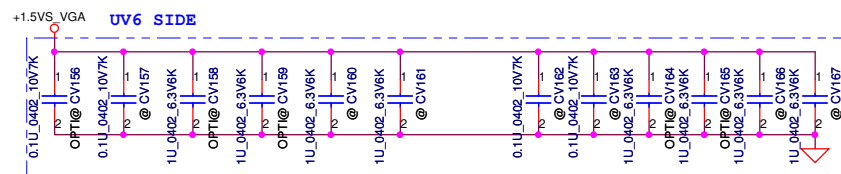
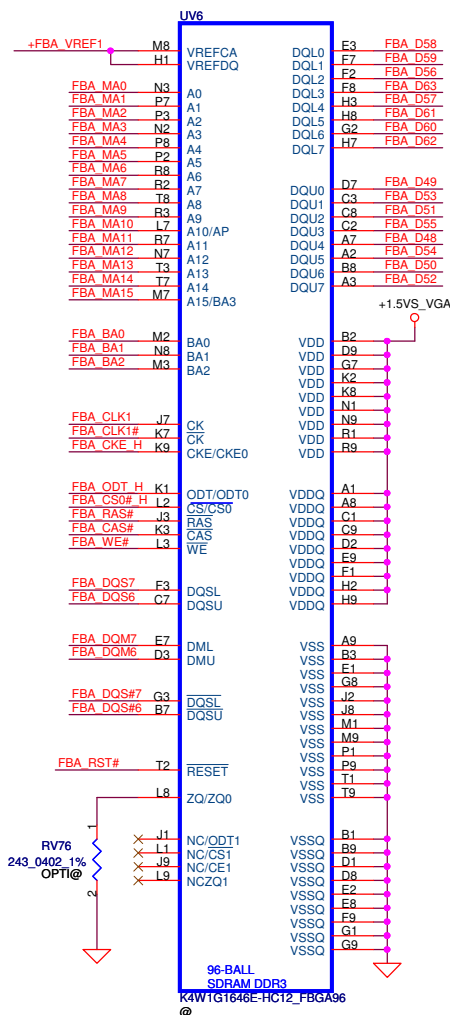
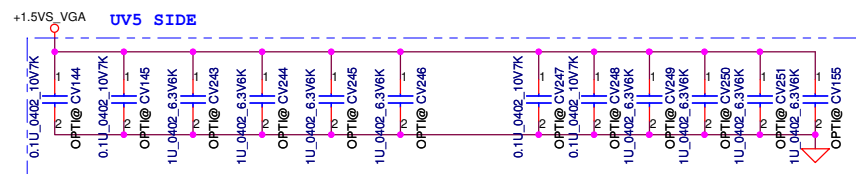
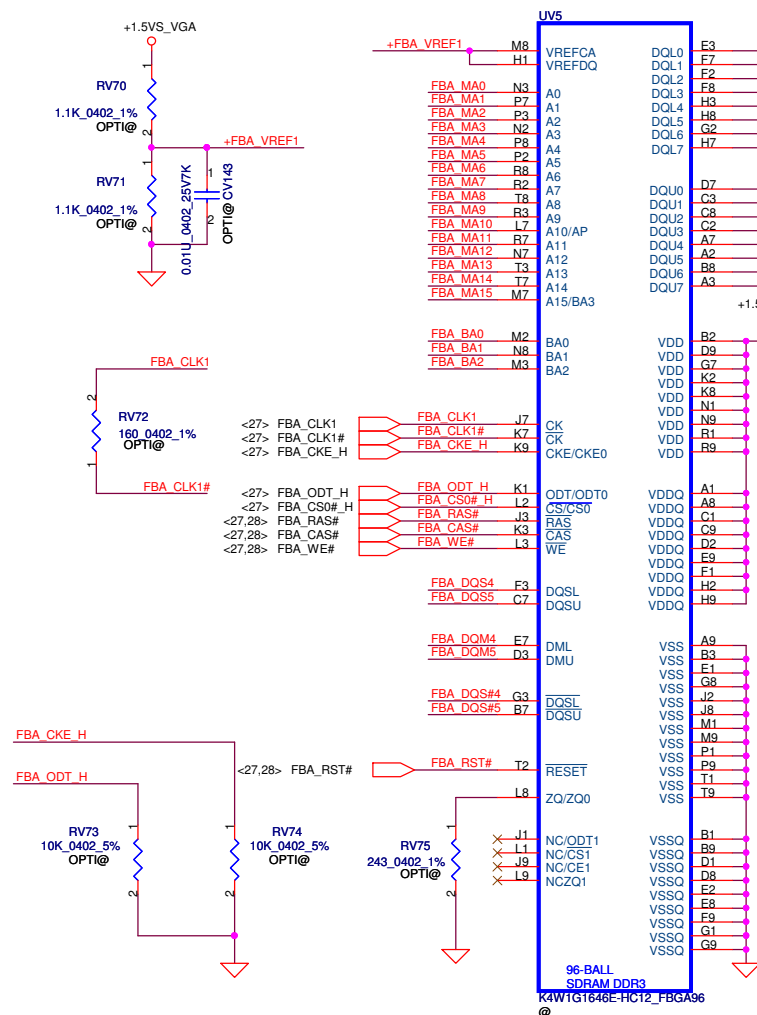
WWW.AliSaler.Com









	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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Memory Partition A - Upper 32 bits

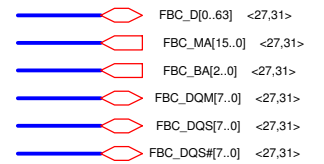
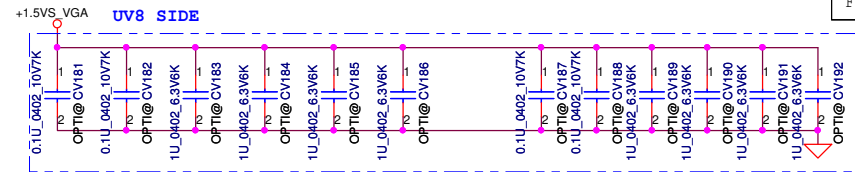
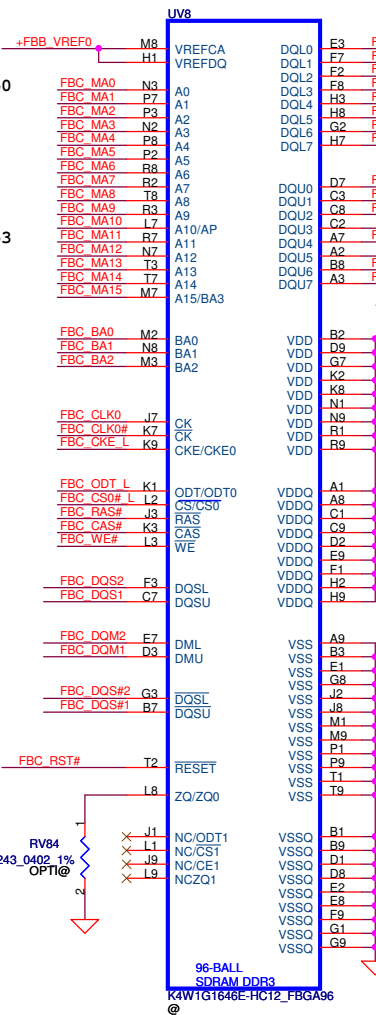
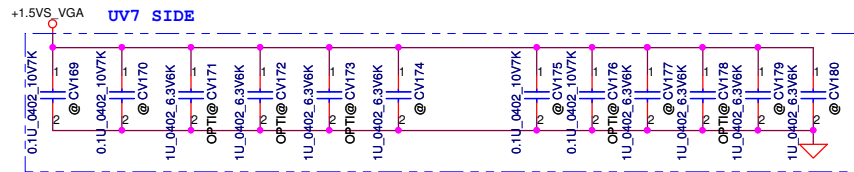
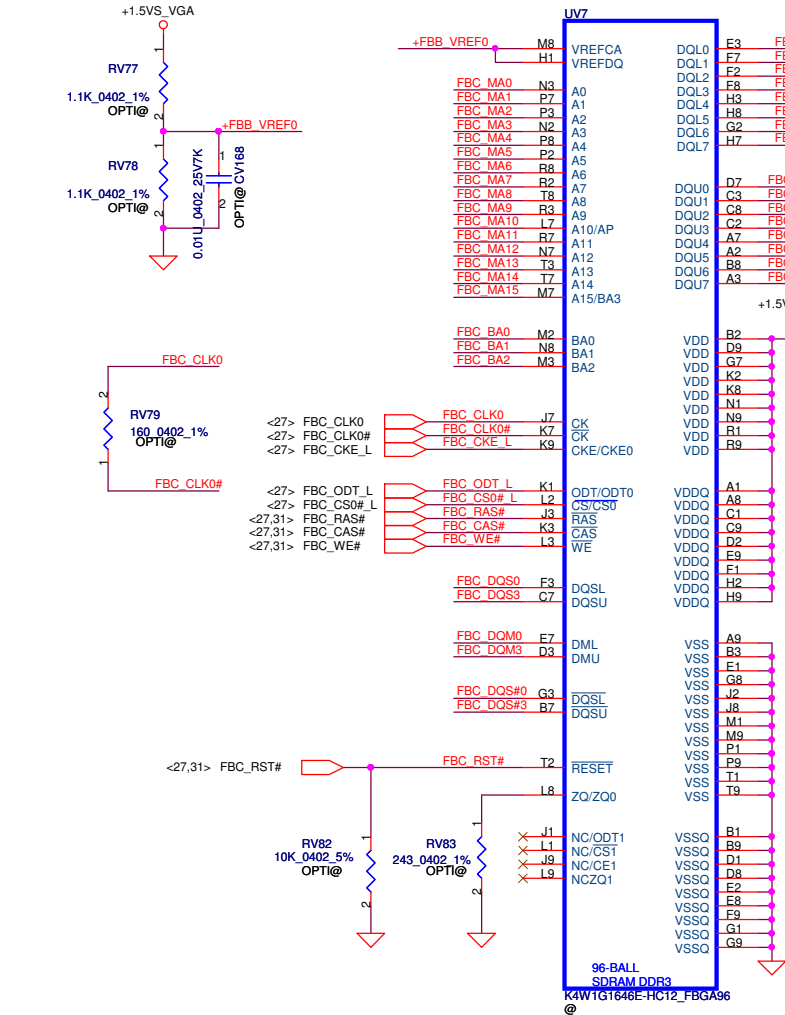


	FBA_D[0..63]	<27,28>
	FBA_MA[15..0]	<27,28>
	FBA_BA[2..0]	<27,28>
	FBA_DOM[7..0]	<27,28>
	FBA_DQS[7..0]	<27,28>
	FBA_DQS#[7..0]	<27,28>

Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Memory Partition C - Lower 32 bits

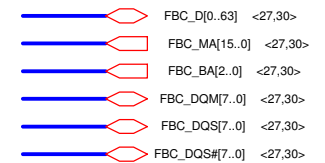
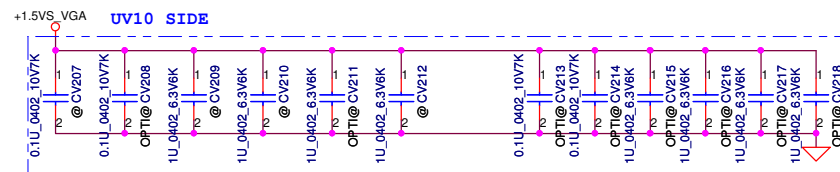
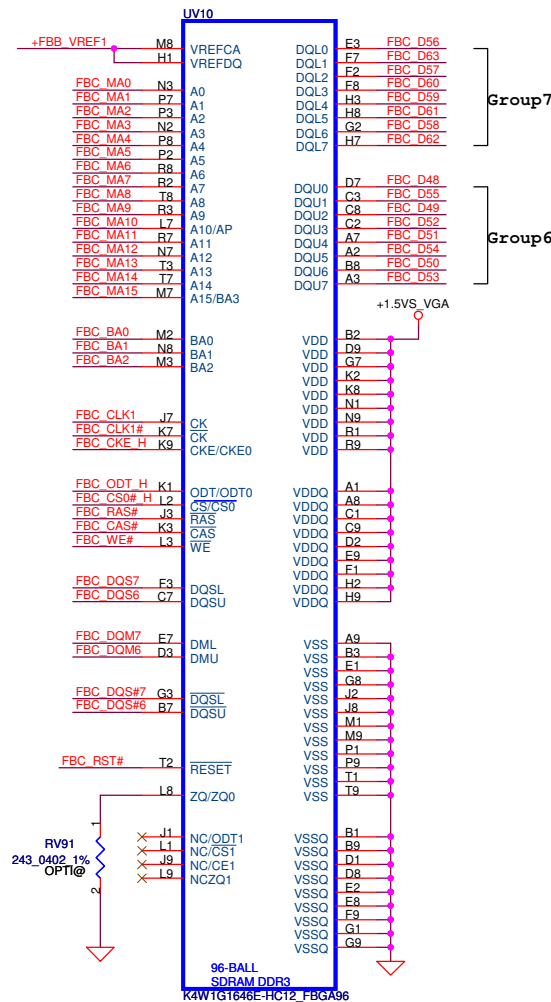
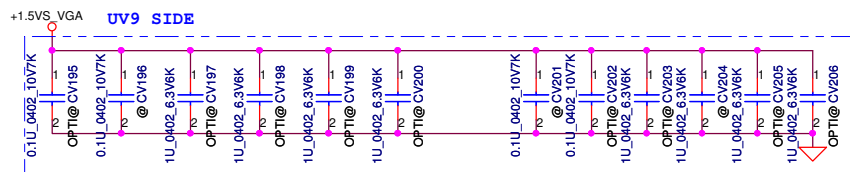
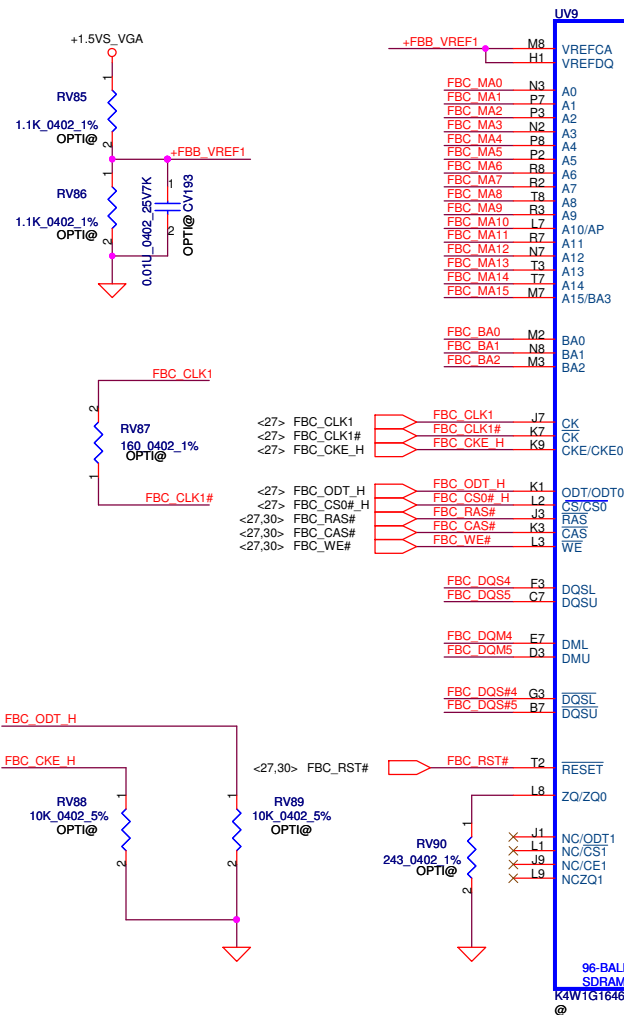


Mode D - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14
FBx_CMD5	RST
FBx_CMD6	A9
FBx_CMD7	A7
FBx_CMD8	A2
FBx_CMD9	A0
FBx_CMD10	A4
FBx_CMD11	A1
FBx_CMD12	BA0
FBx_CMD13	WE#
FBx_CMD14	A15
FBx_CMD15	CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13
FBx_CMD21	A8
FBx_CMD22	A6
FBx_CMD23	A11
FBx_CMD24	A5
FBx_CMD25	A3
FBx_CMD26	BA2
FBx_CMD27	BA1
FBx_CMD28	A12
FBx_CMD29	A10
FBx_CMD30	RAS#

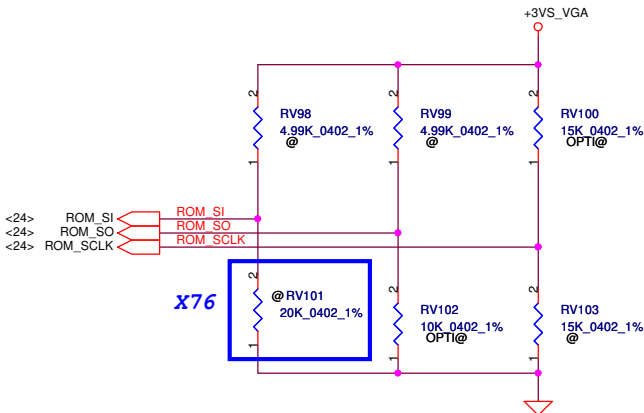
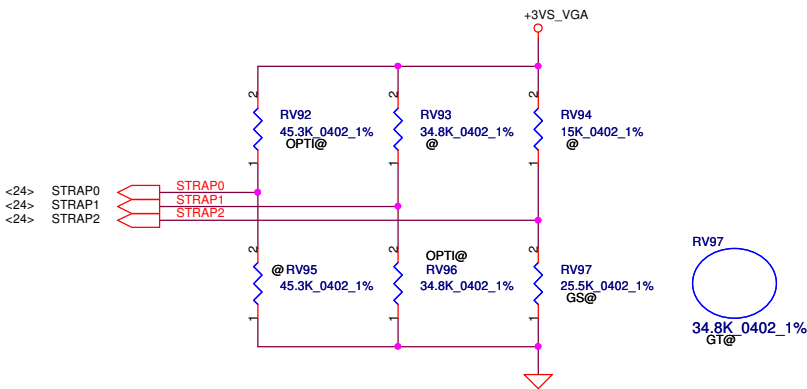
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				Date: Monday, November 29, 2010	Sheet 30 of 63

Memory Partition C - Upper 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



ROM_SO : PD-10K
 ROM_SCLK : PH-15K
 ROM_SI : PD20K (Samsung)
 Strap 2 : N12P-GS, PD-25K,
 N12P-GT, PD35K,
 Strap 1 : PD-35K
 Strap 0 : PH-45K

	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GT	0x0DF6	Pull up 15K	Pull down 35K

Hynix H5TQ1G63BFR-12C	64Mx16	0010	PD 15K	SA000041S30
	128Mx16	0110	PD 35K	SA00003YO10
Samsung K4W1G1646E-HC12	64Mx16	0011	PD 20K	SA000041T10
	128Mx16	0111	PD 45K	SA000047Q10

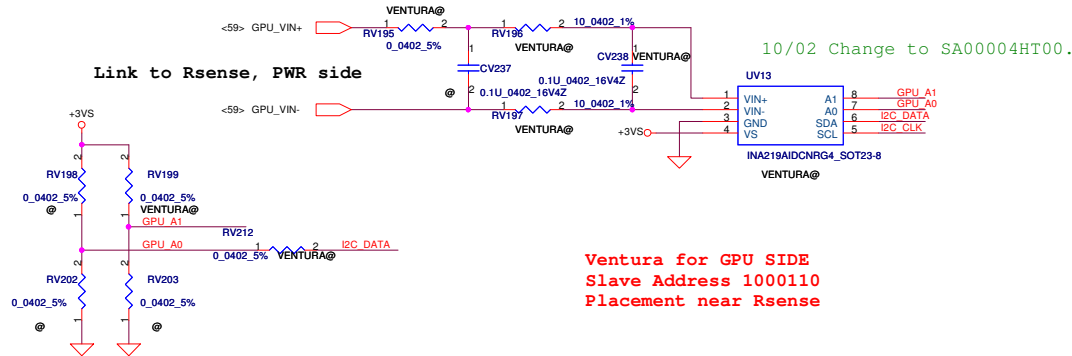
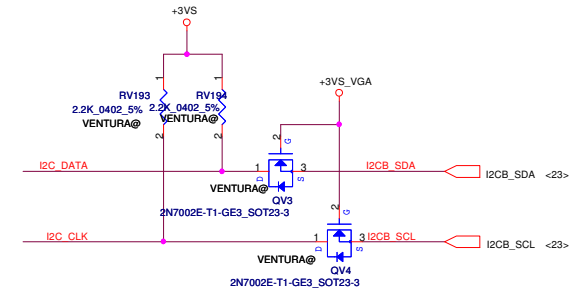
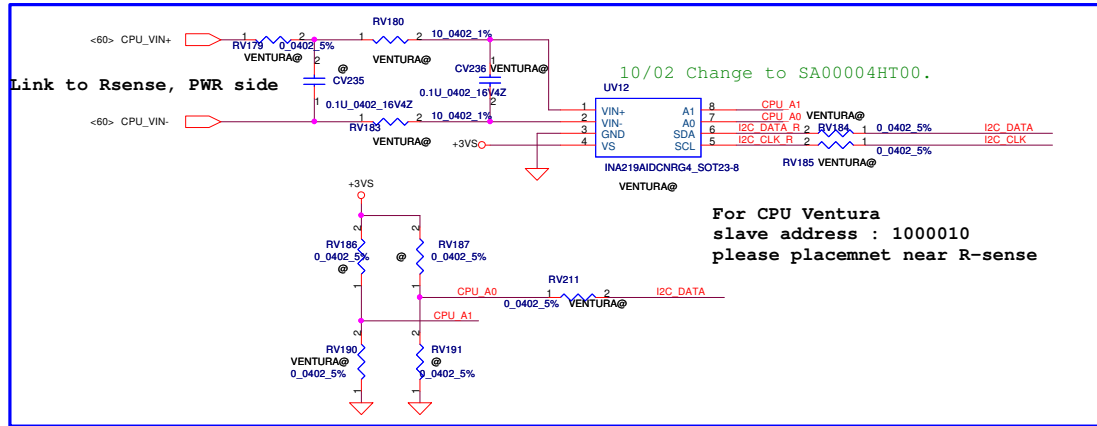
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

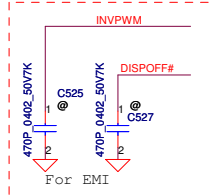
SUB_VENDOR		XCLK_417	
0	No VBIOS ROM	0	277MHz (Default)
1	BIOS ROM is present (Default)	1	Reserved
FB_0_BAR_SIZE		USER Straps	
0	256MB (Default)	User [3:0]	
1	Reserved	1000-1100	Customer defined
3GIO_PADCFG		PEX_PLL_EN_TERM	
3GIO_PADCFG[3:0]		0	Disable (Default)
0110	Notebook Default	1	Enable
SLOT_CLK_CFG			
0	GPU and MCH don't share a common reference clock		
1	GPU and MCH share a common reference clock (Default)		
SMBUS_ALT_ADDR		VGA_DEVICE	
0	0x9E (Default)	0	3D Device (Class Code 302h)
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)

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				Size Custom	Document Number	Rev 0.3
				PIQY0 LA6881P		
				Date:	Monday, November 29, 2010	Sheet 32 of 63

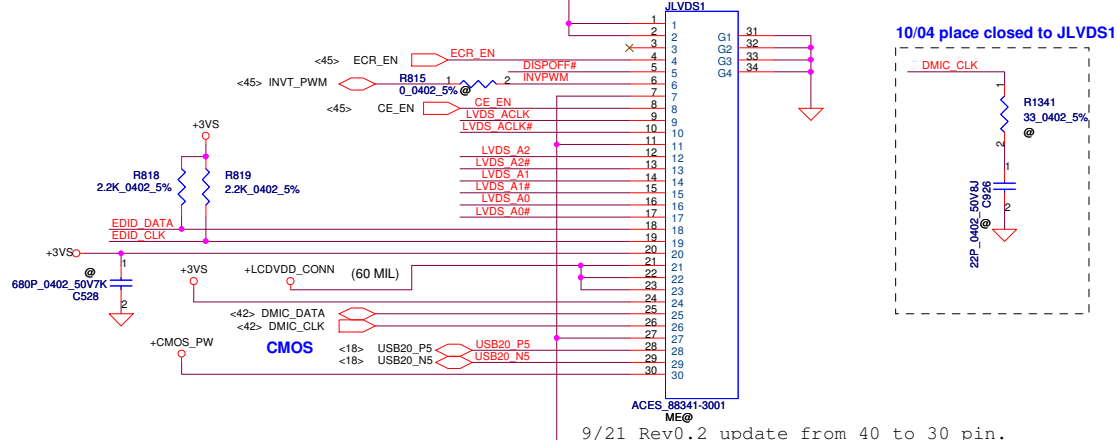
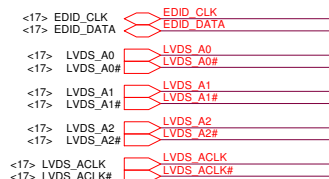
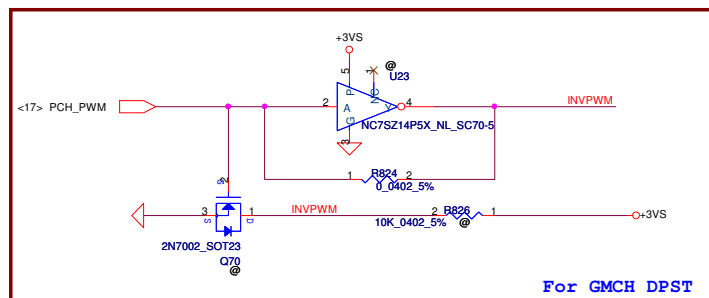
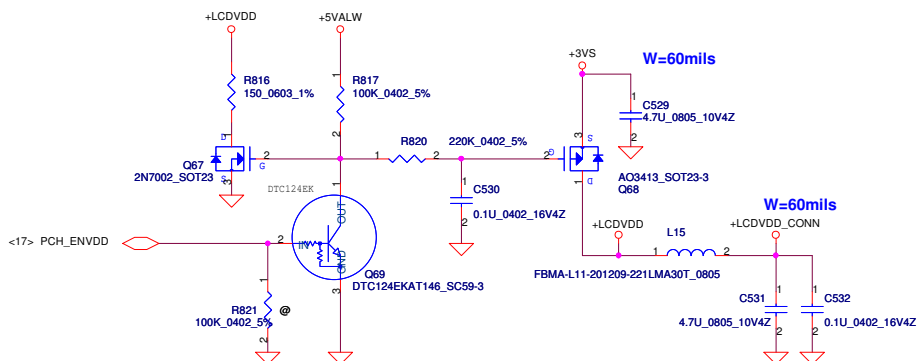
TOP side (under inductor)



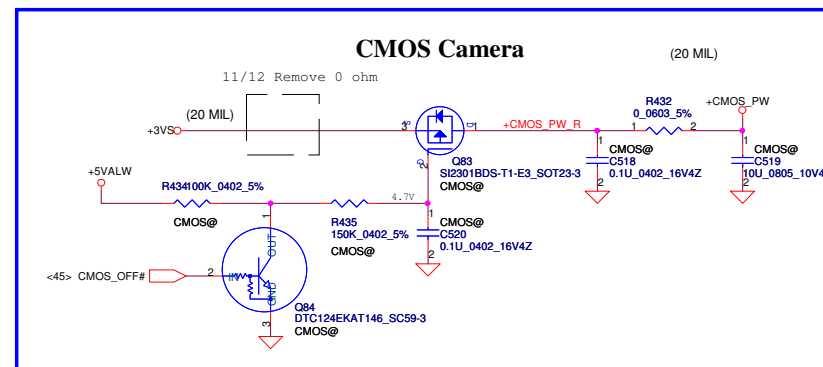
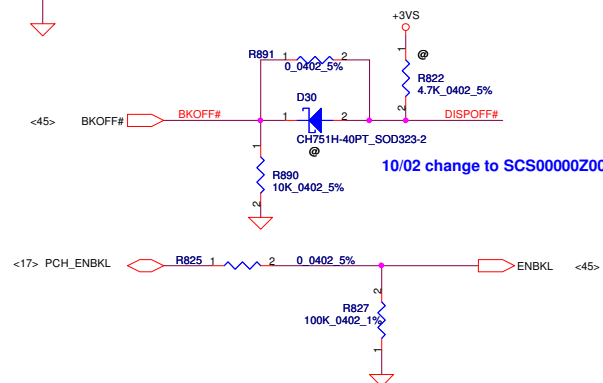
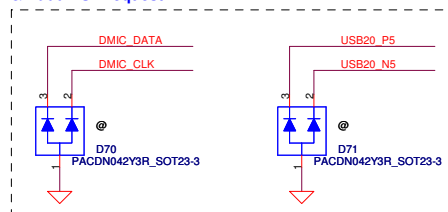
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				Size	Document Number	Rev
					PIQY0 LA6881P	0.3
				Date:	Monday, November 29, 2010	Sheet 33 of 63



LCD POWER CIRCUIT



8/4 add ESD request



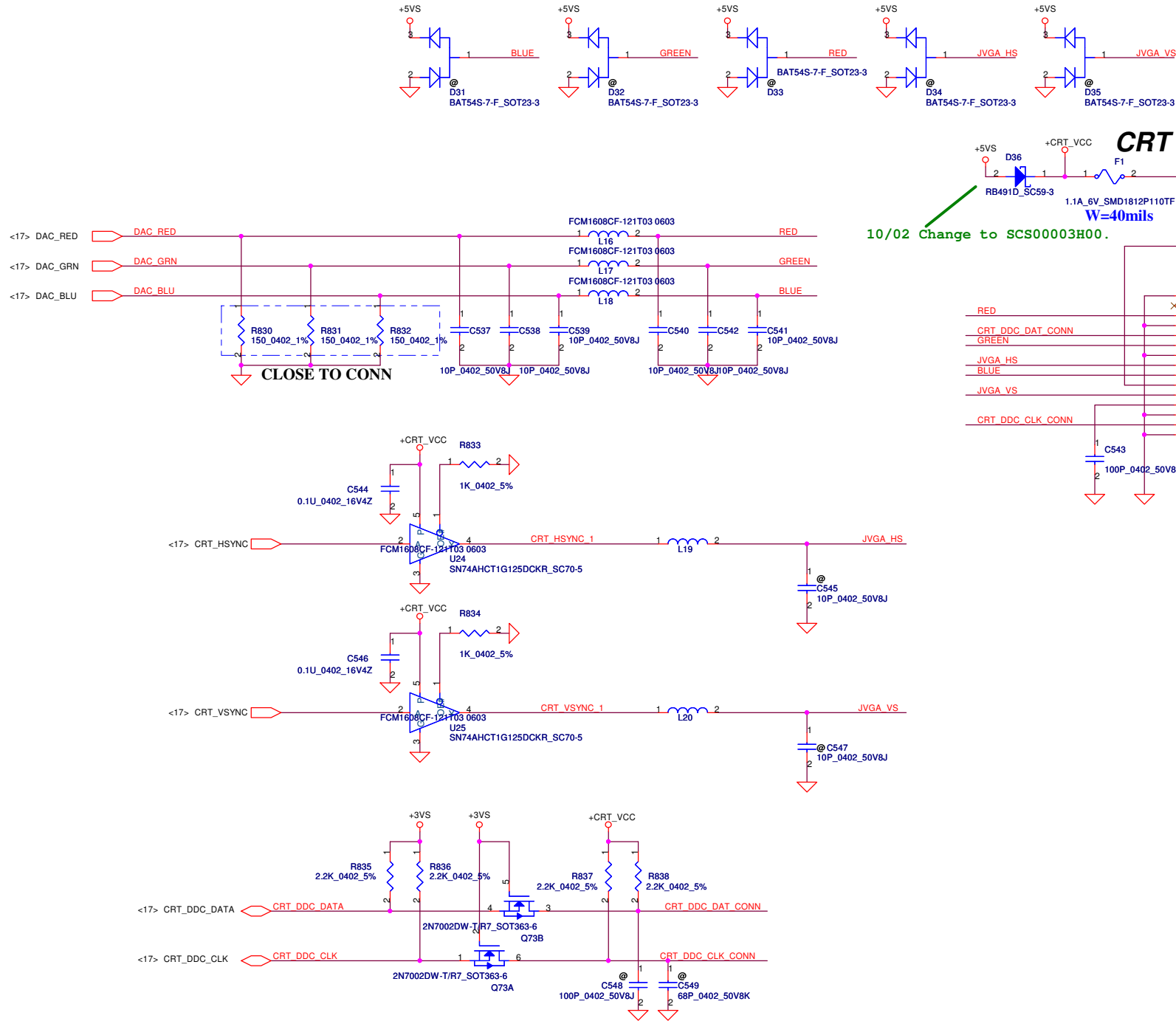
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Issued Date	2010/11/30	Deciphered Date	2011/08	Size	Document Number
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				1 Sheet 34 of 63	

Compal Electronics, Inc.

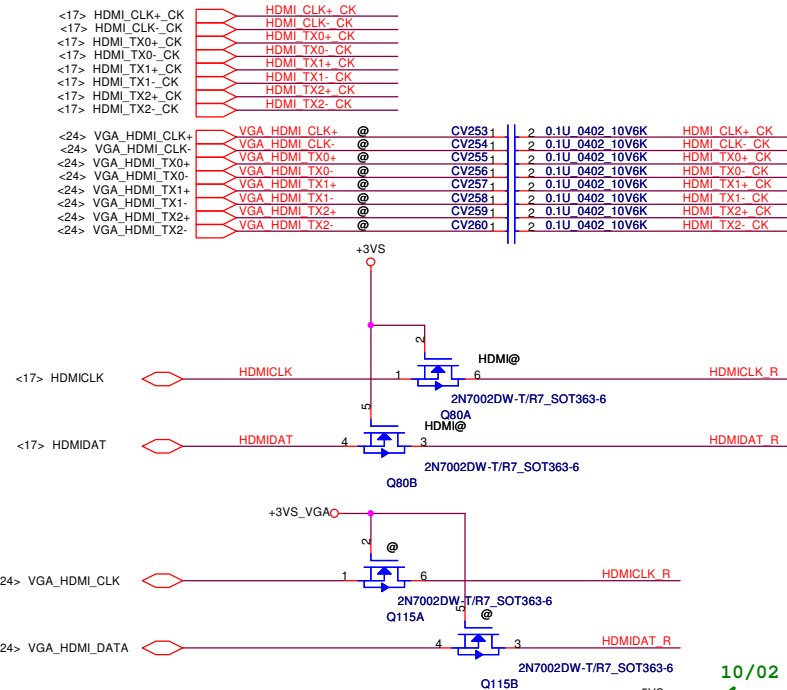
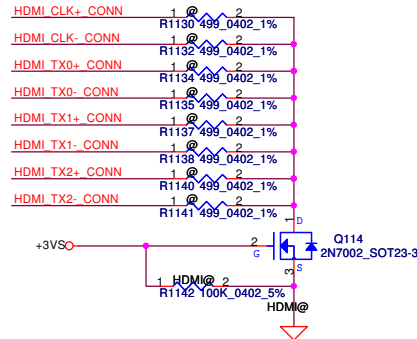
LVDS/CAMERA

PIQY0 LA6881P

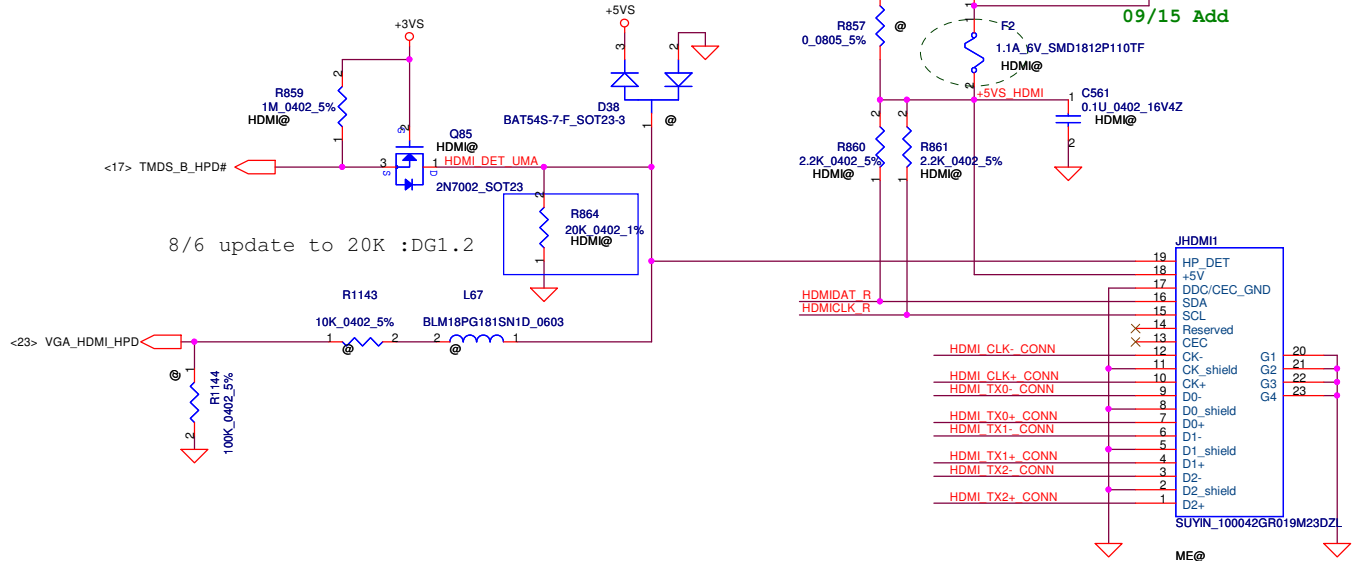
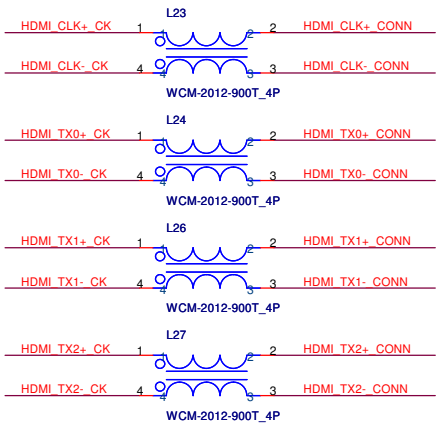
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				Custom	PIQY0 LA6881P
				Date:	Monday, November 29, 2010
				Sheet	35 of 63
				Rev	0.3



DVT, Change to SM070000I00 for EMI request.

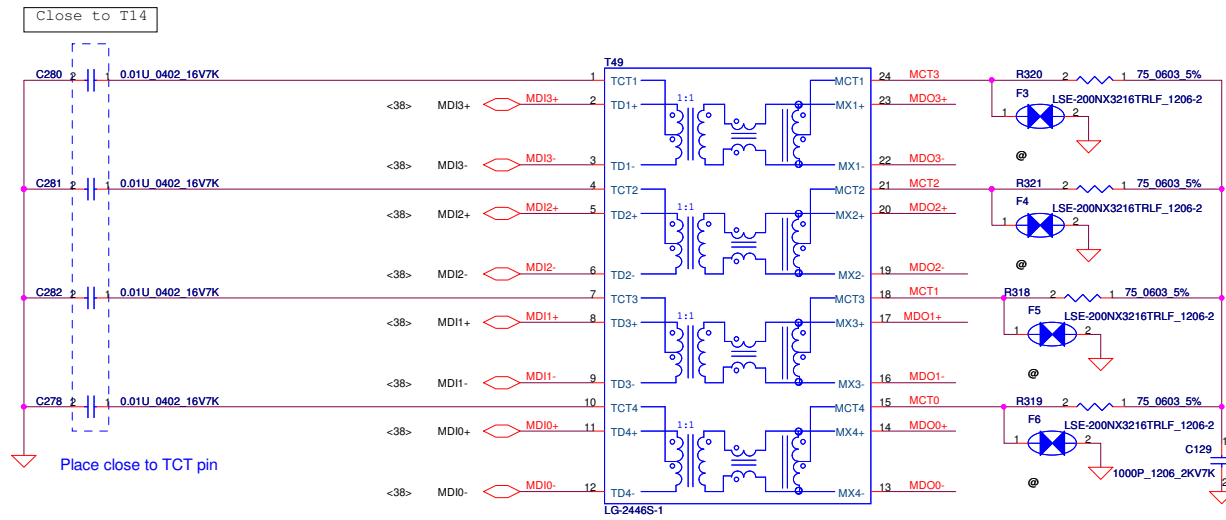


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Issued Date	2010/11/30	Deciphered Date	2011/08	HDMI CONN	
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				Custom	PIQY0 LA6881P
				Date	Monday, November 29, 2010
				Sheet	36 of 63

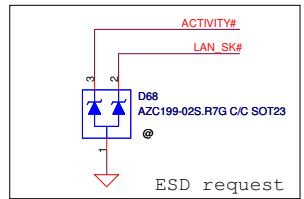
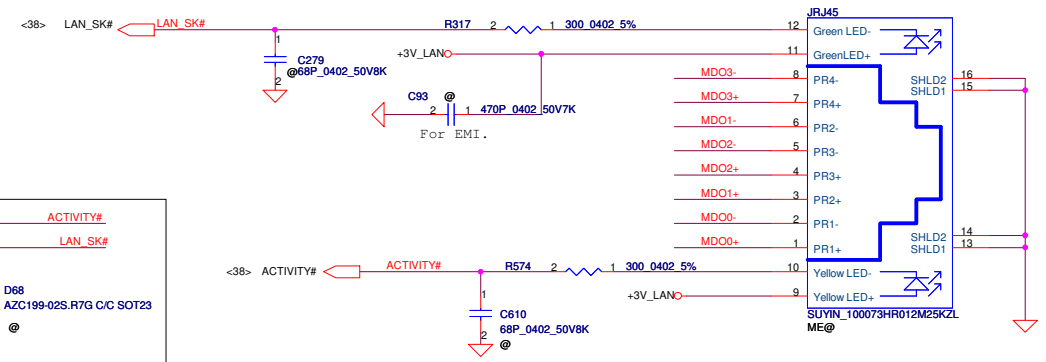
Mini-Express Card(SSD)

0.3



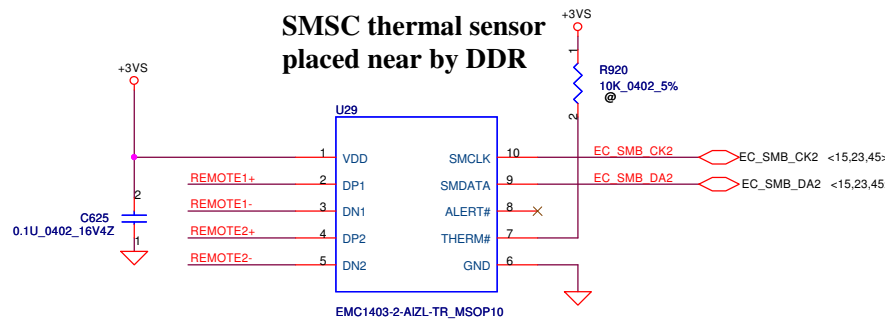
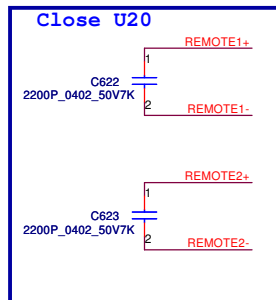


RJ45 Conn.

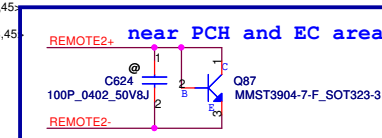
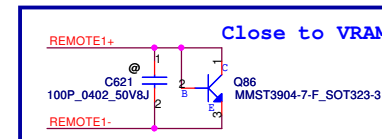


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Issued Date				2010/11/30				Title			
				Deciphered Date				LAN Magnetic & RJ45			
				2011/08				Size			
								Document Number			
								PIQY0 LA6881P			
								Rev			
								0.3			
								Date: Monday, November 29, 2010			
								Sheet 39 of 63			

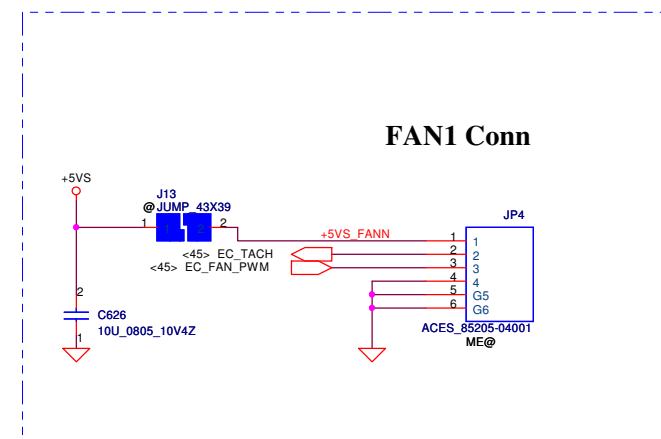
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Address 1001_101xb
8/02 Change PN to SA000046C00, Fintek.

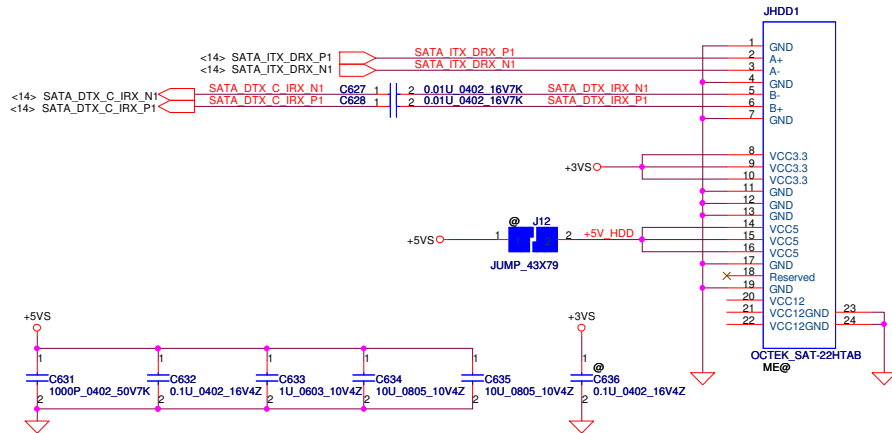


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

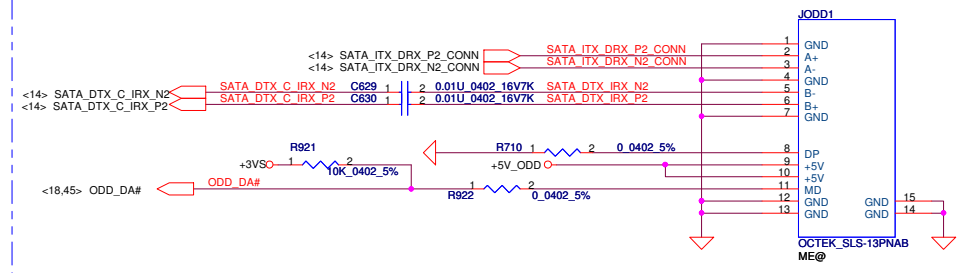


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				Date: Monday, November 29, 2010	PIQY0 LA6881P
				Sheet 40 of 63	Rev 0.3

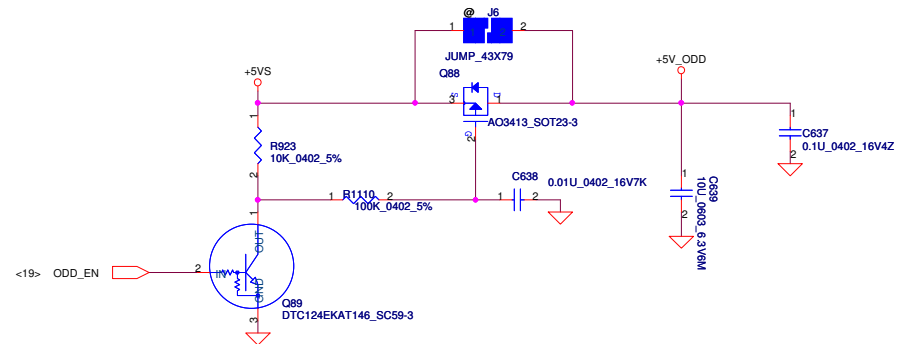
SATA HDD Conn.



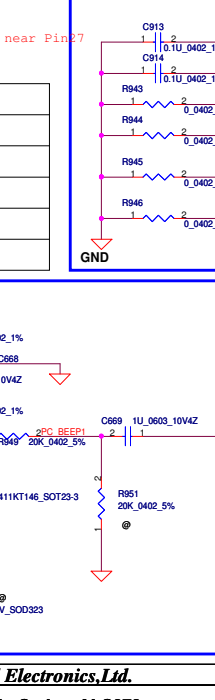
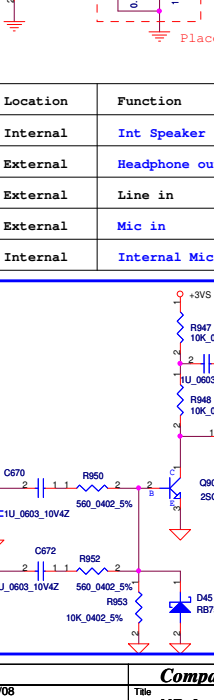
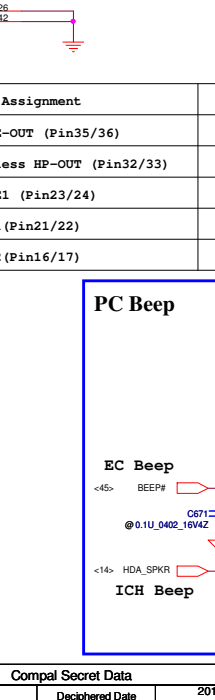
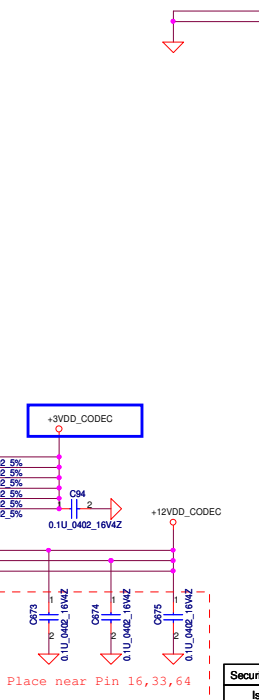
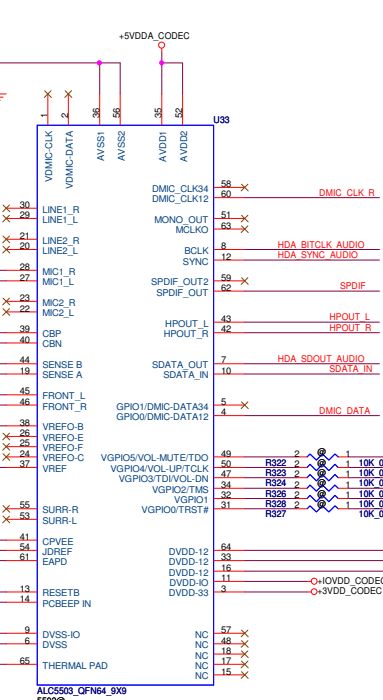
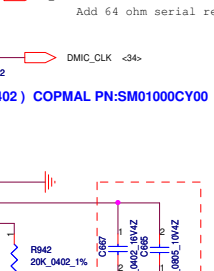
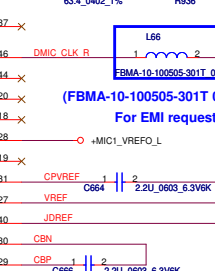
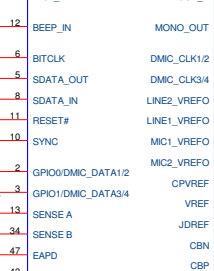
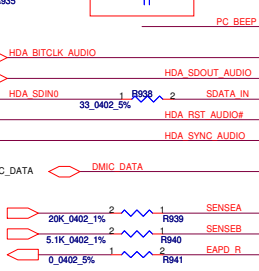
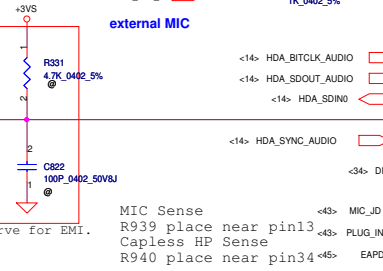
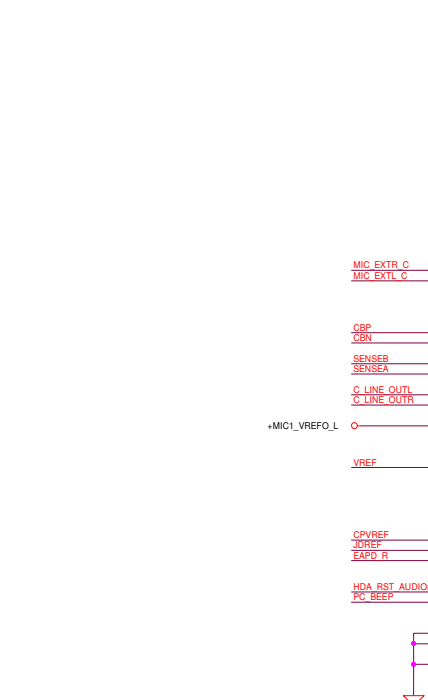
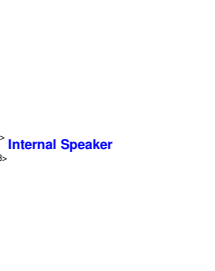
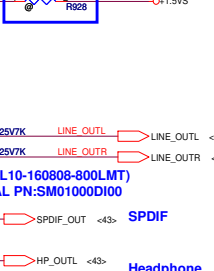
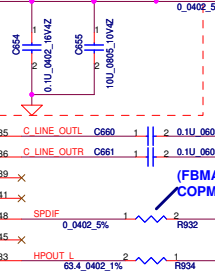
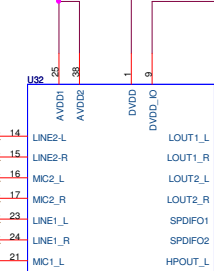
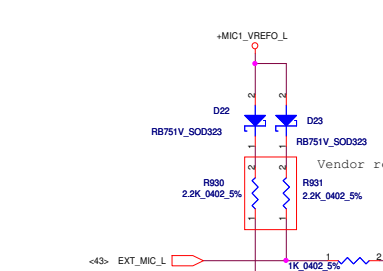
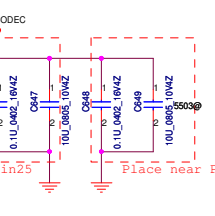
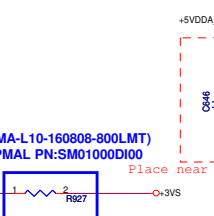
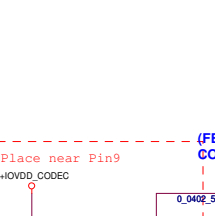
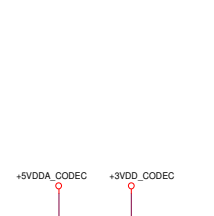
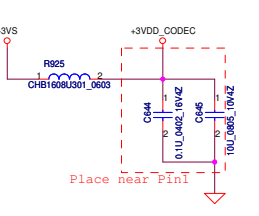
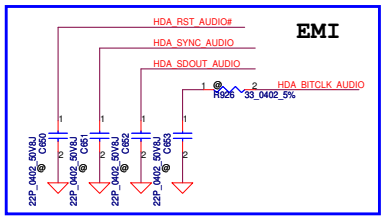
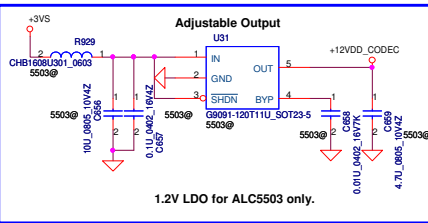
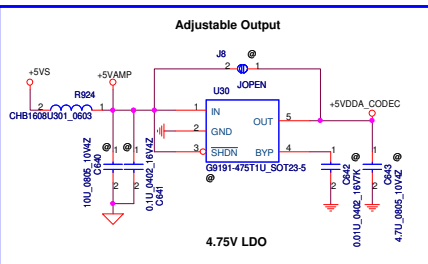
SATA ODD Conn.



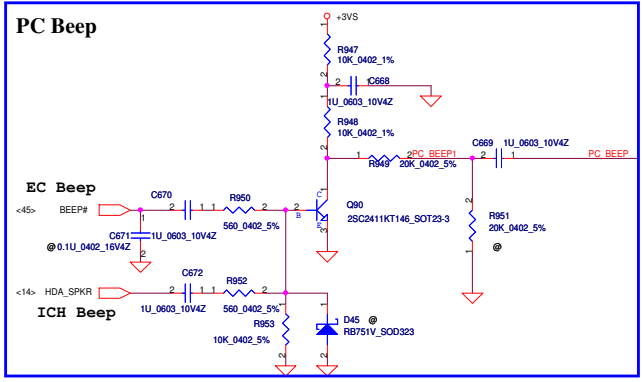
ODD Power Control



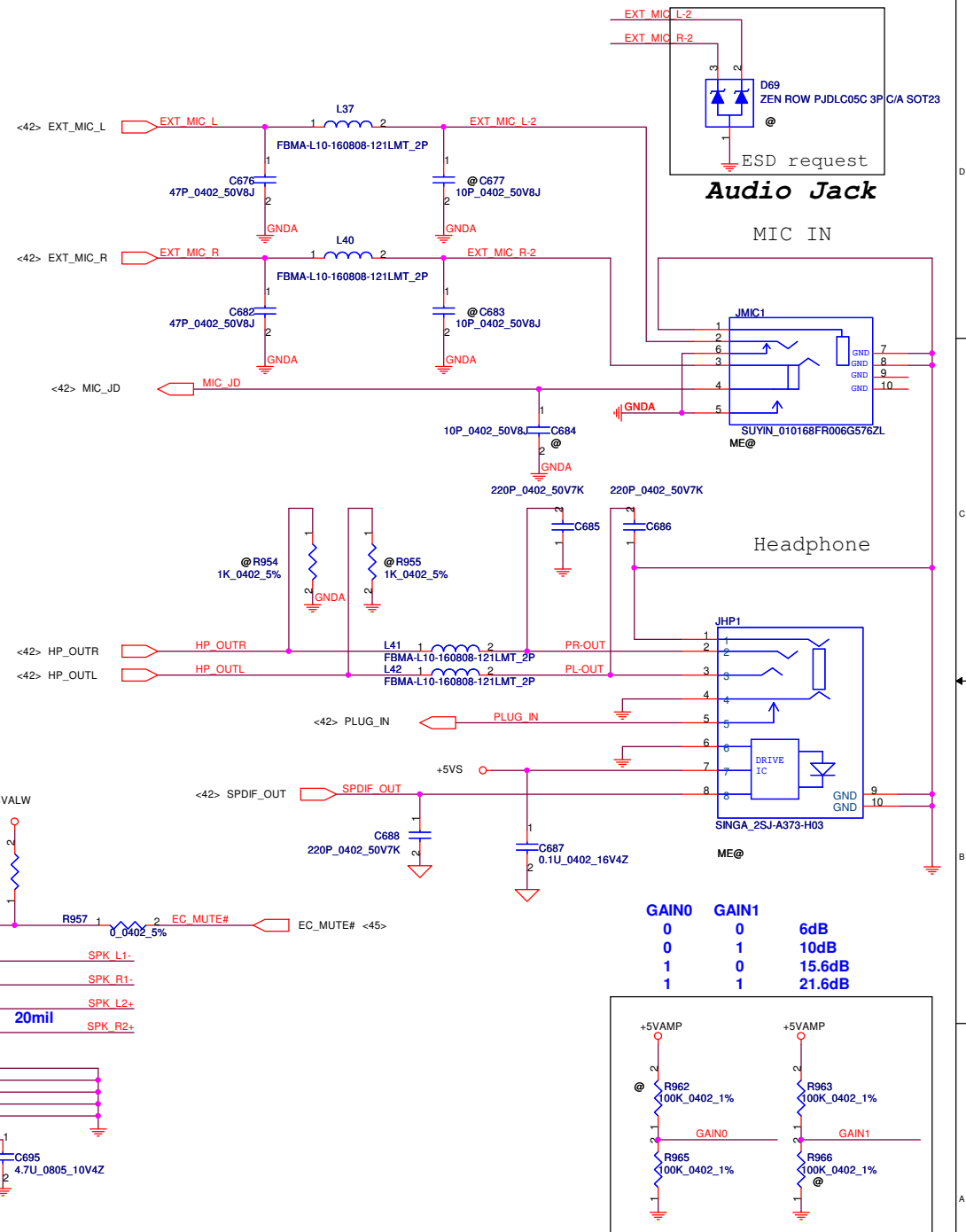
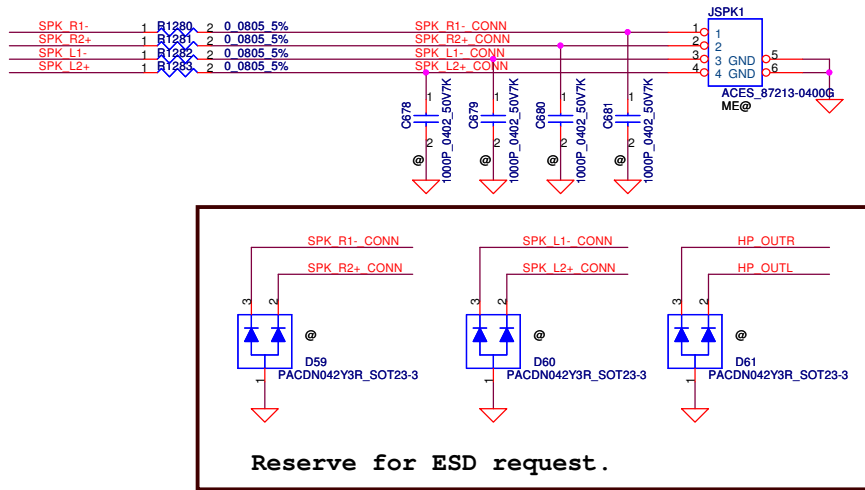
Security Classification	Compal Secret Data			Title	
Issued Date	2010/11/30	Deciphered Date	2011/08	HDD/ODD Connector	
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				PIQY0 LA6881P	
				Date: Monday, November 29, 2010	Rev 0.3
				Sheet 41	of 63



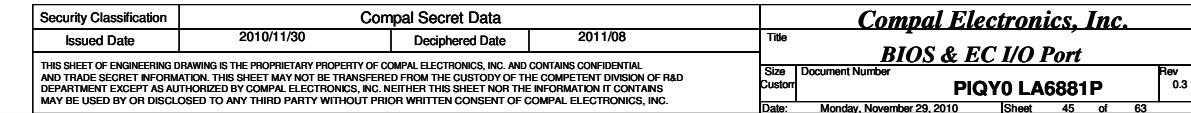
Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1 (Pin21/22)	External	Mic in
MIC2 (Pin16/17)	Internal	Internal Mic



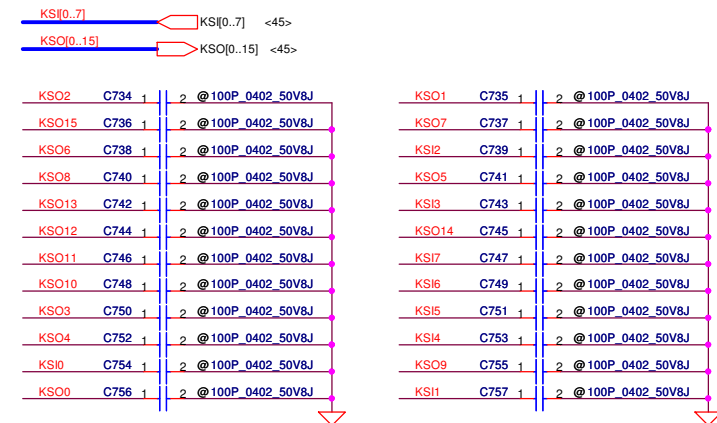
wide 20MIL



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				Date: Monday, November 29, 2010	Rev 0.3
				Sheet 43	of 63

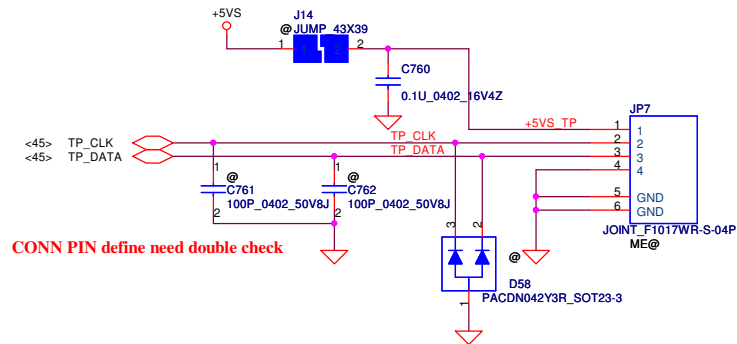


INT_KBD Conn.

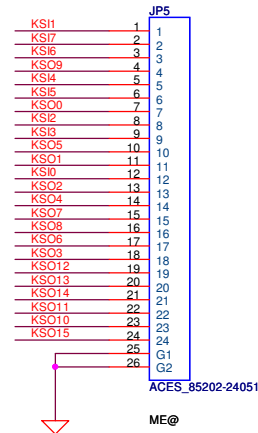


CONN PIN define need double check

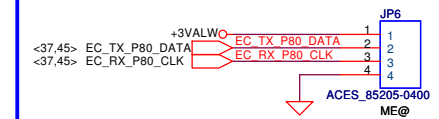
To TP/B Conn.



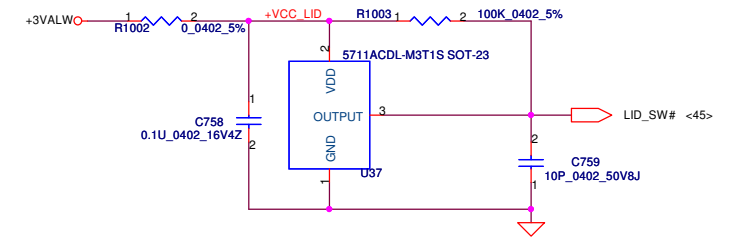
CONN PIN define need double check



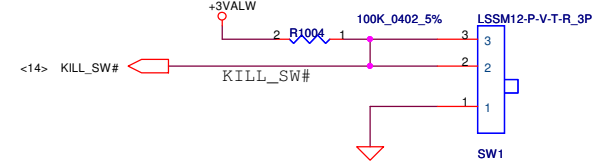
EC DEBUG PORT



Lid Switch

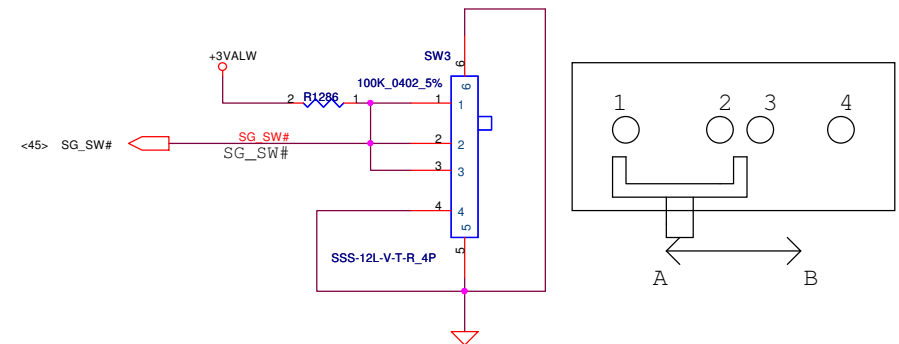


Kill Switch



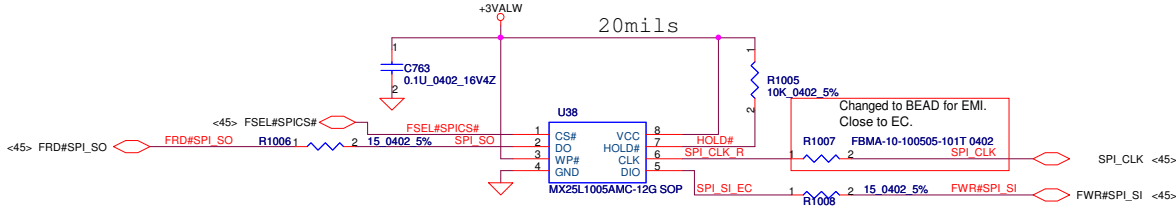
Kill

STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

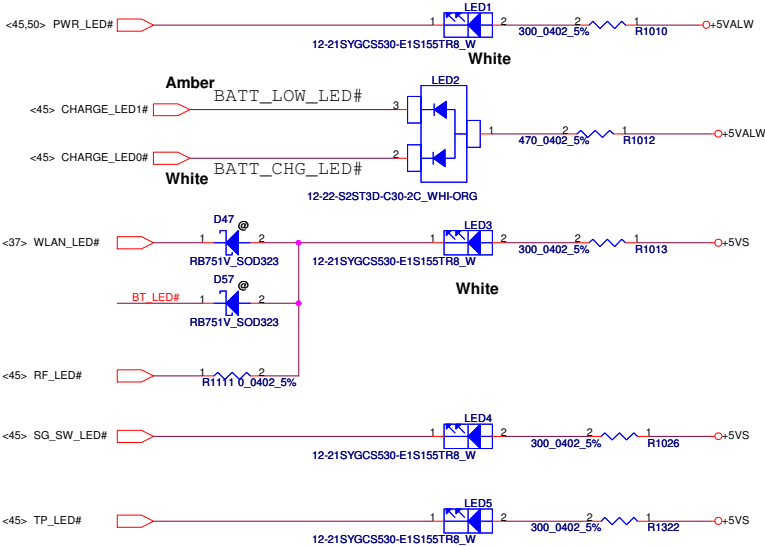


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				PIQY0 LA6881P	
				Date: Monday, November 29, 2010	Rev 0.3
				Sheet 46	of 63

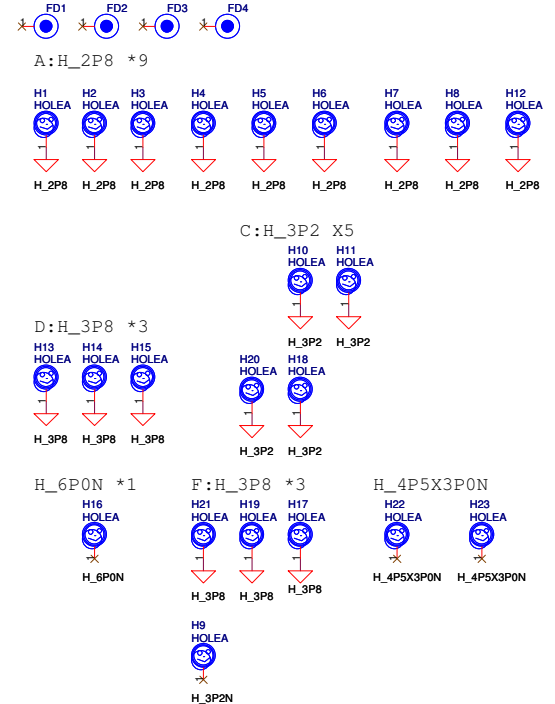
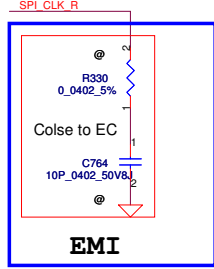
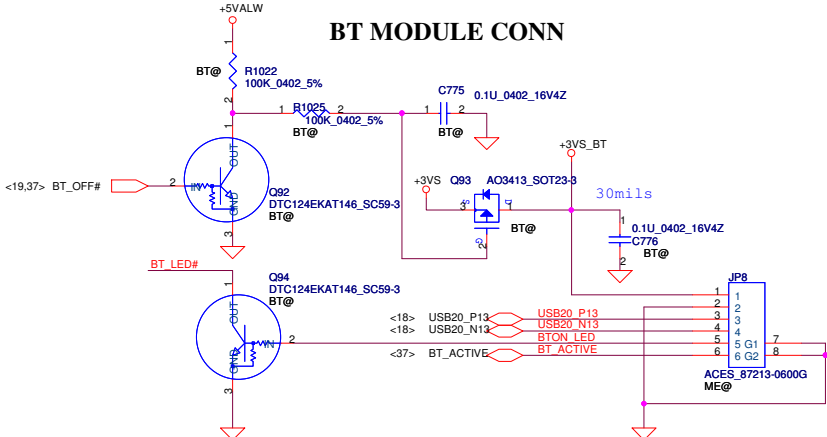
P/N : SA00002C100



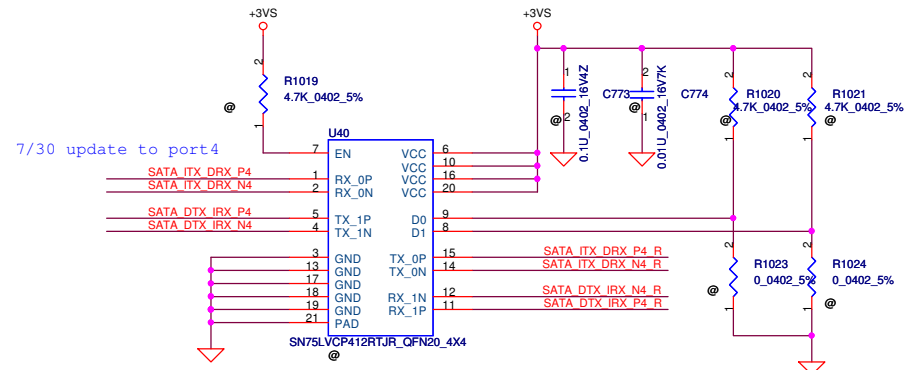
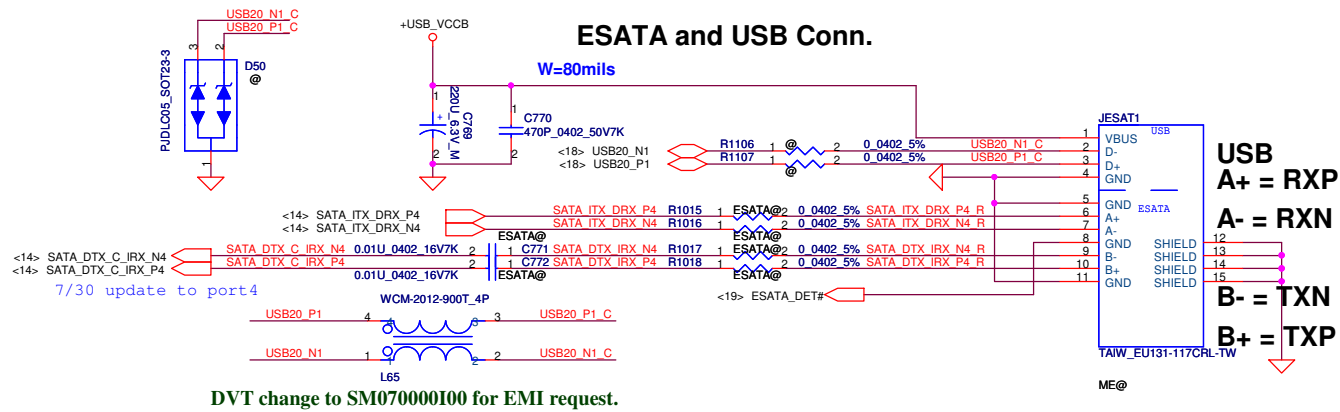
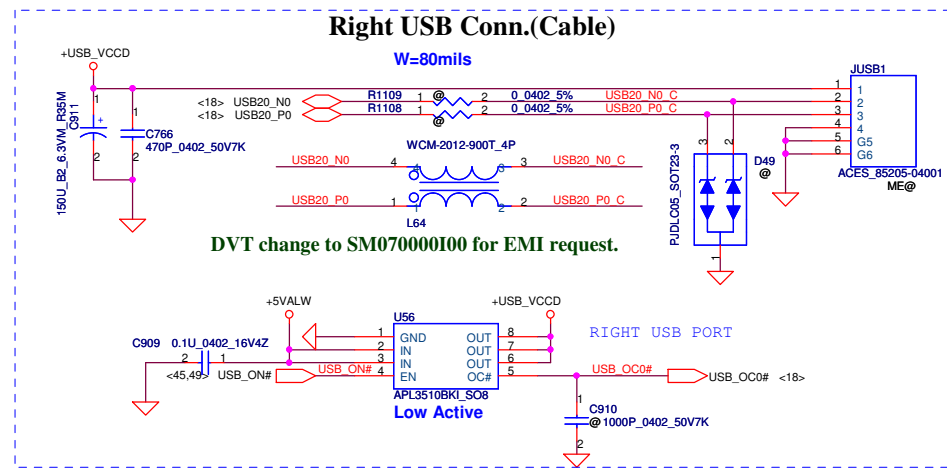
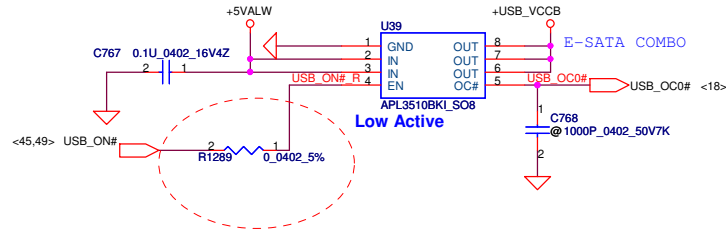
LED



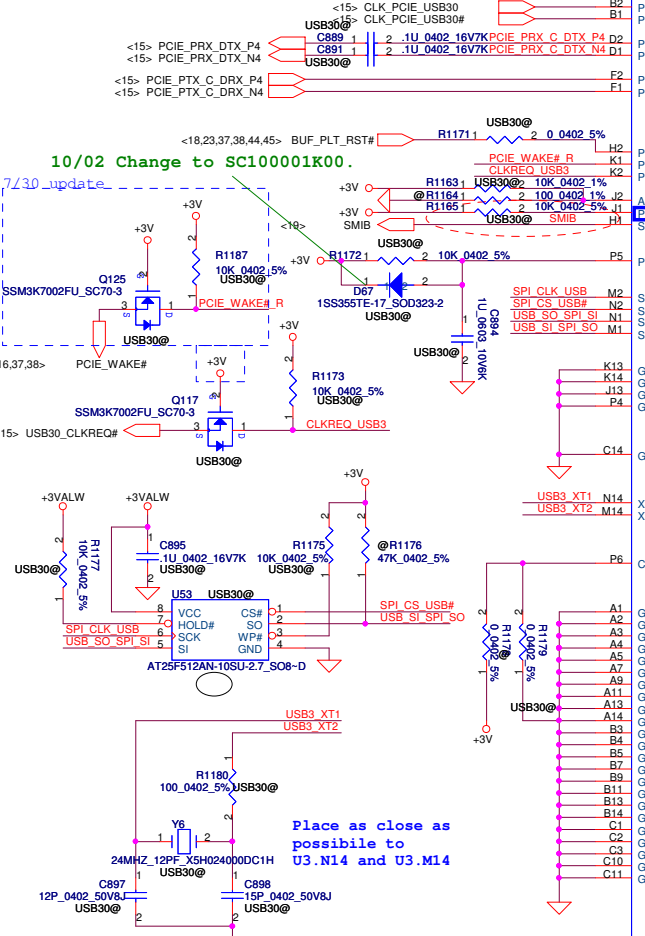
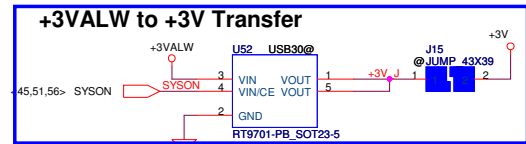
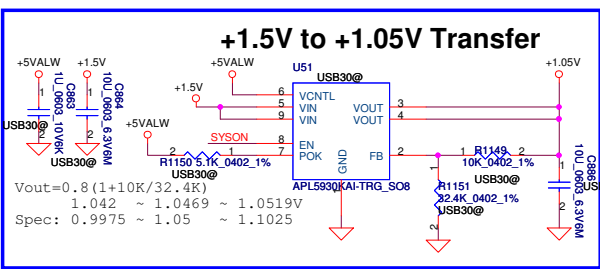
BT MODULE CONN



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					Rev 0.3
Date:	Monday, November 29, 2010	Sheet	47 of 63		

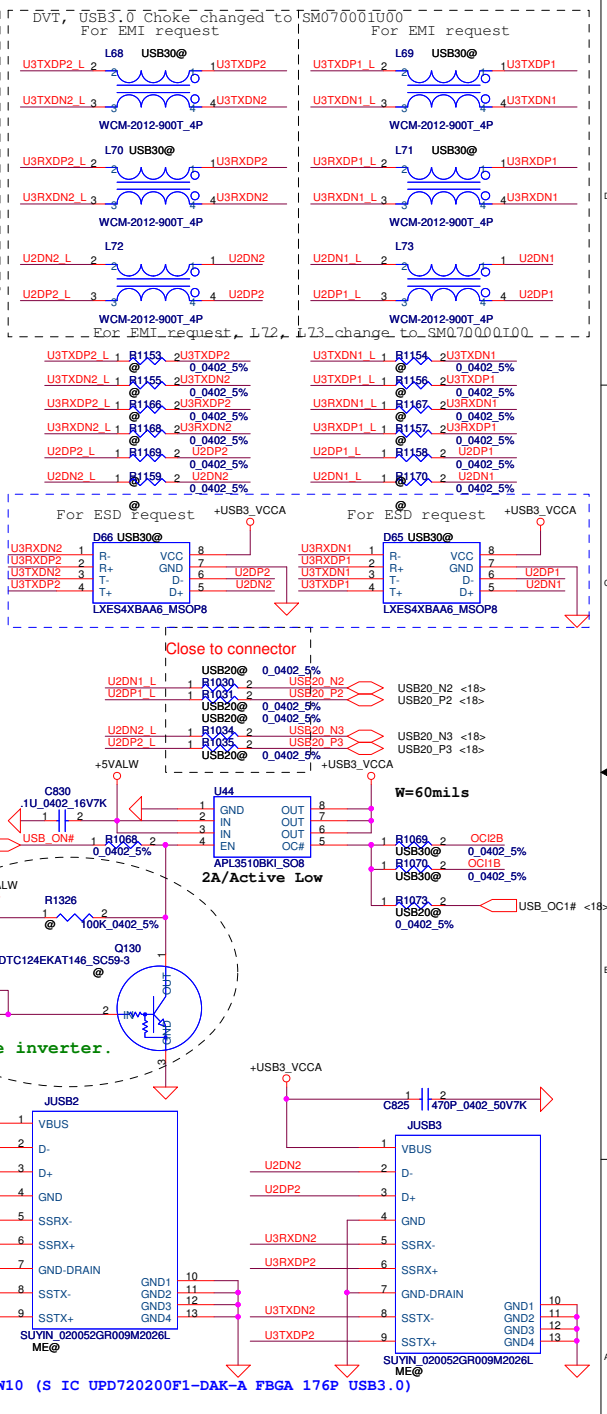
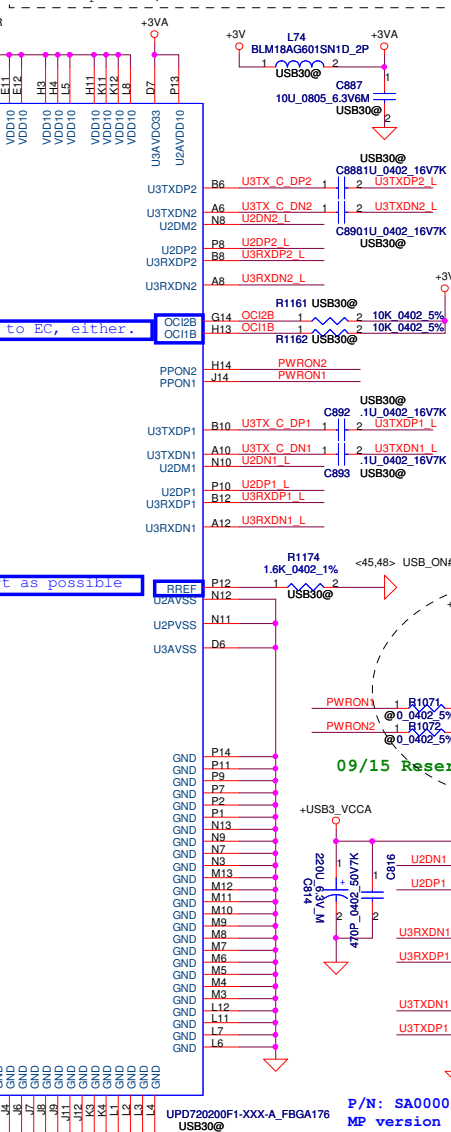
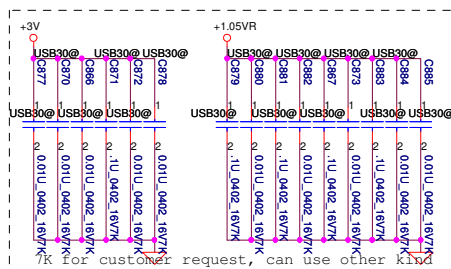
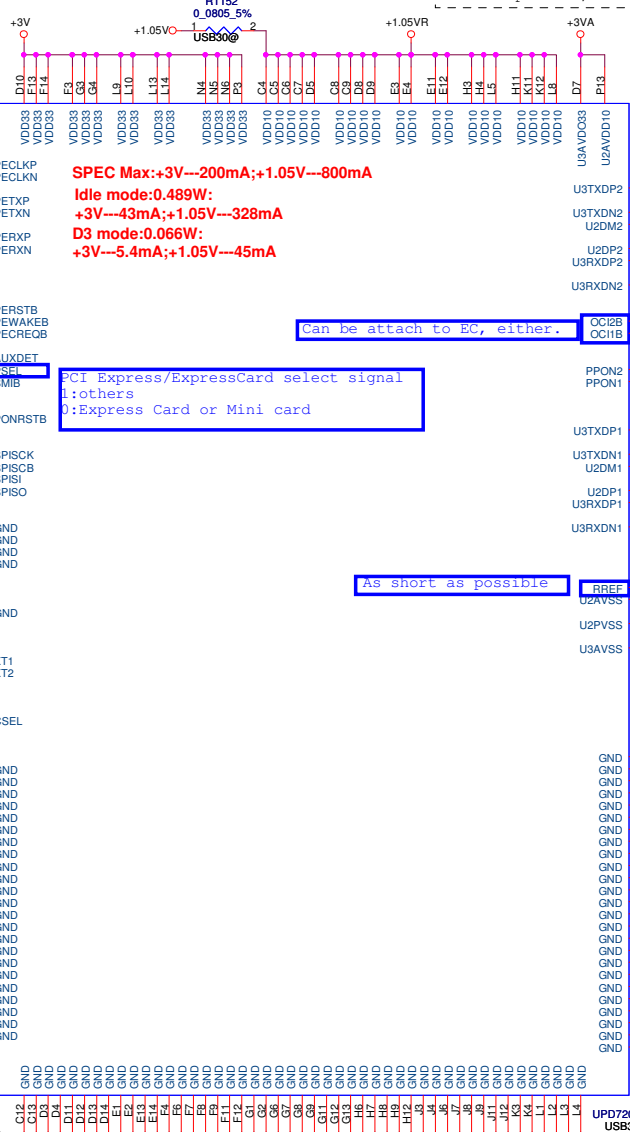
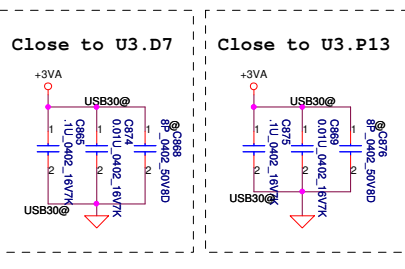


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								USB ports/E-SATA			
								Size			
								Document Number			
								PIQY0 LA6881P			
								Rev			
								0.3			
								Date:			
								Monday, November 29, 2010			
								Sheet			
								48			
								of			
								63			

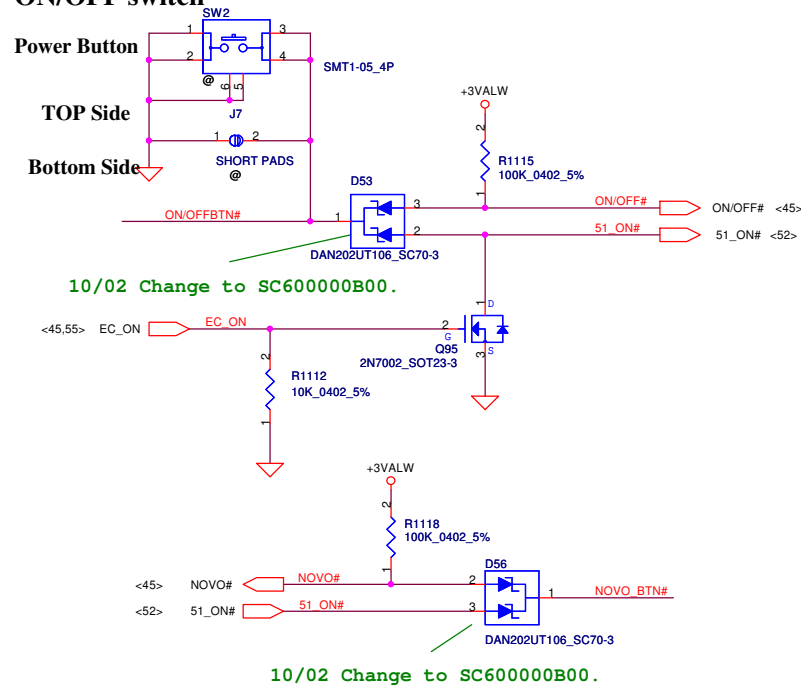


Pin compare table for support USB remote wakeup or not

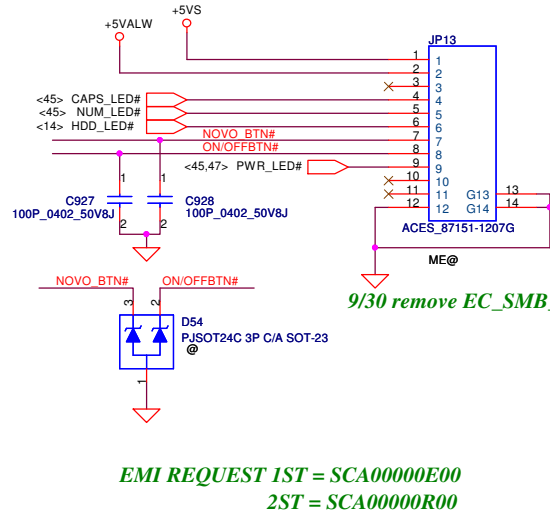
	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25



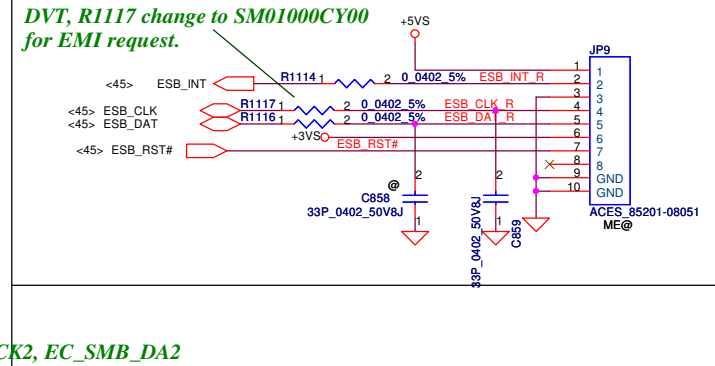
ON/OFF switch



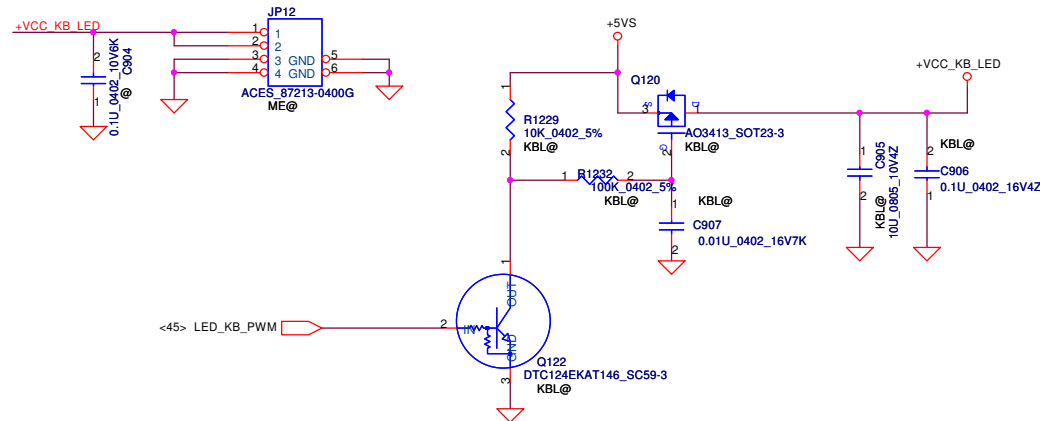
Power Bottom Board Conn. 10pin



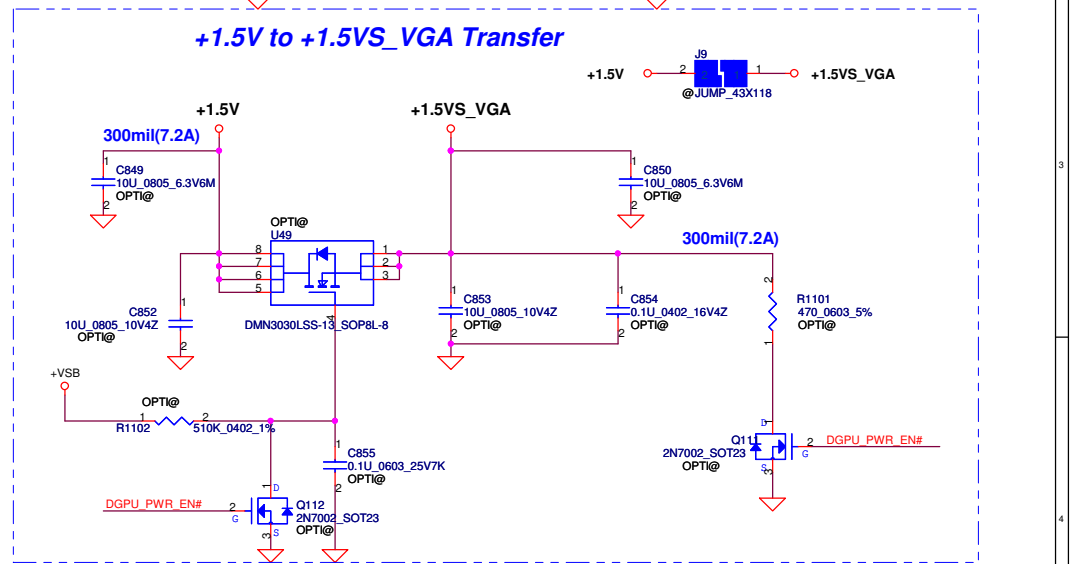
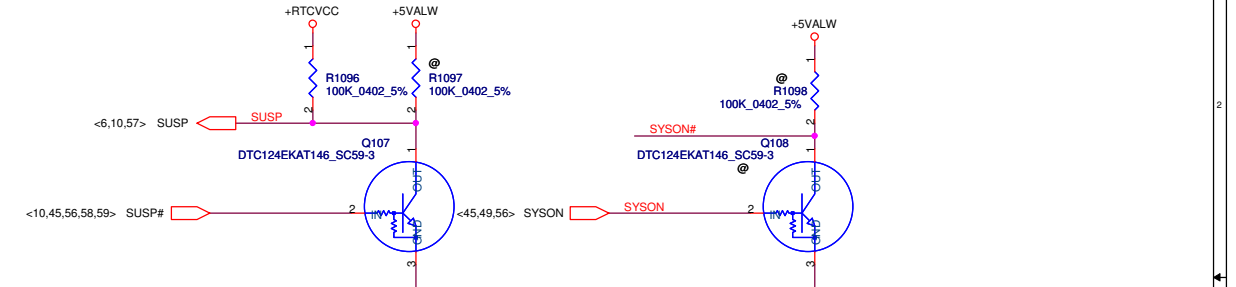
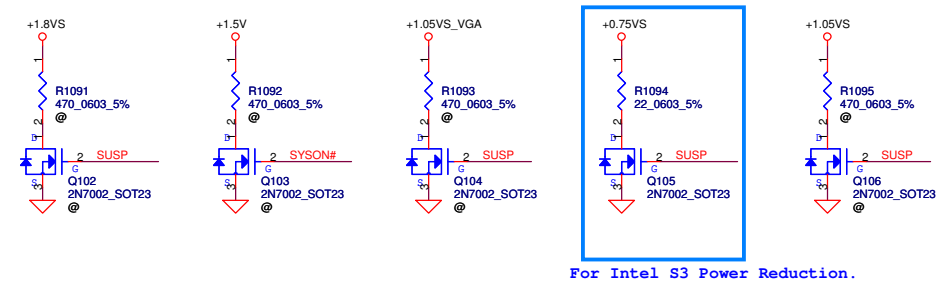
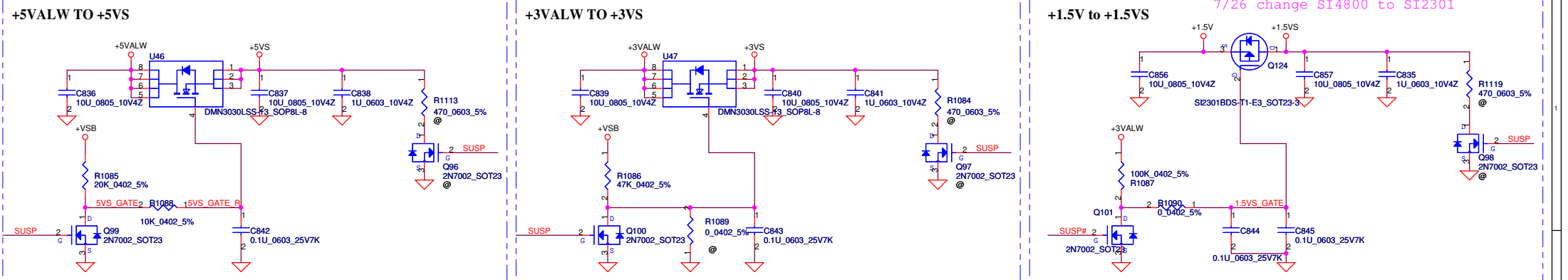
Silder Bar Board Mdule Conn. 6pin



KB Lighting CONN.4pin

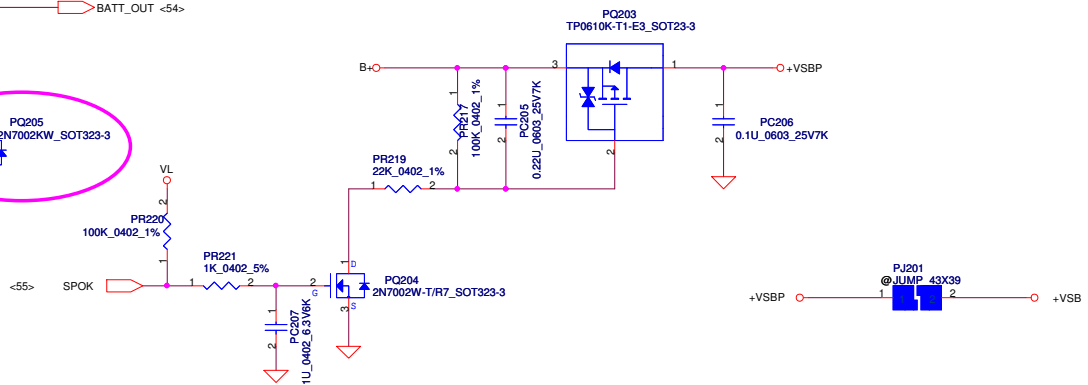
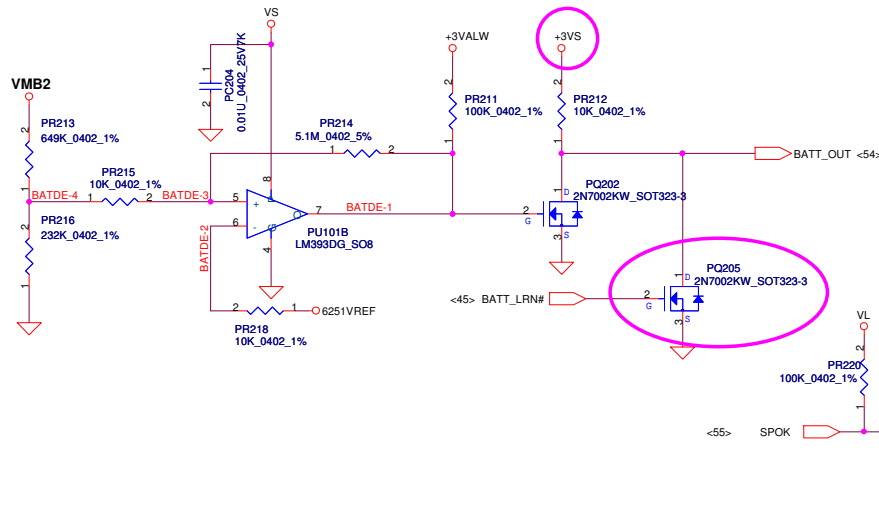
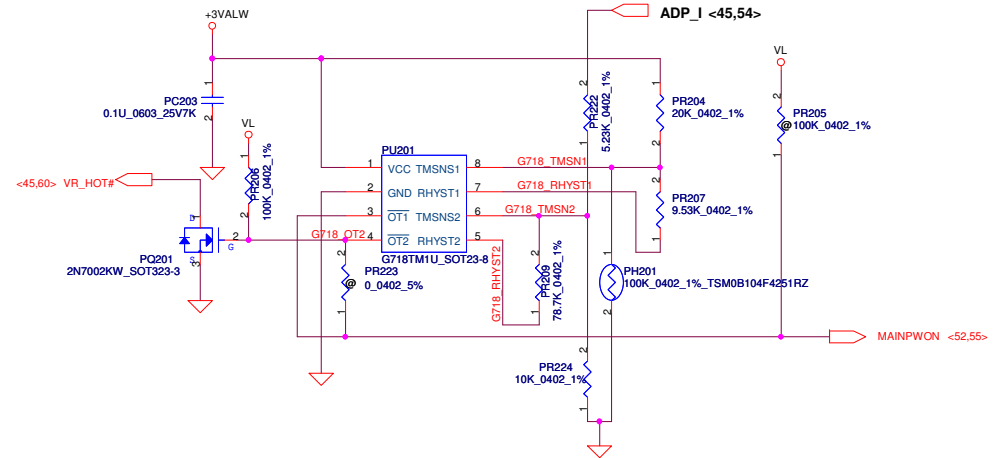
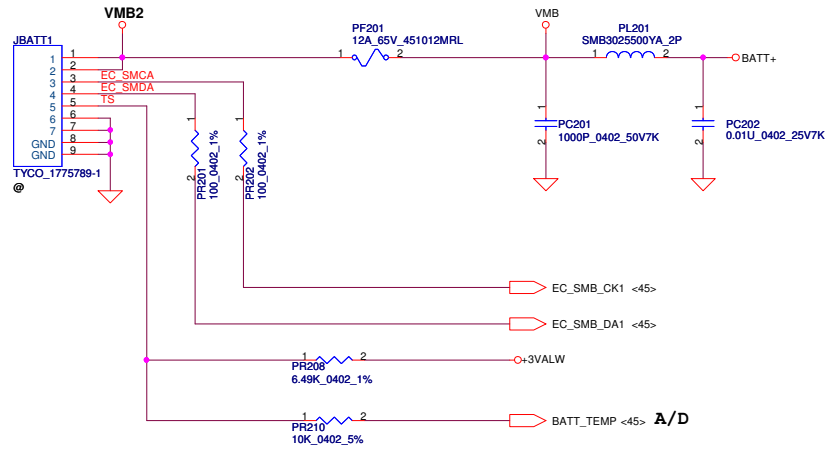


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Size Custom	Document Number	PIQY0 LA6881P		Rev 0.3
Date: Monday, November 29, 2010	Sheet	50	of	63



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				Size	Document Number	Rev
				Custm	PIQY0 LA6881P	0.3
				Date:	Monday, November 29, 2010	Sheet 51 of 63

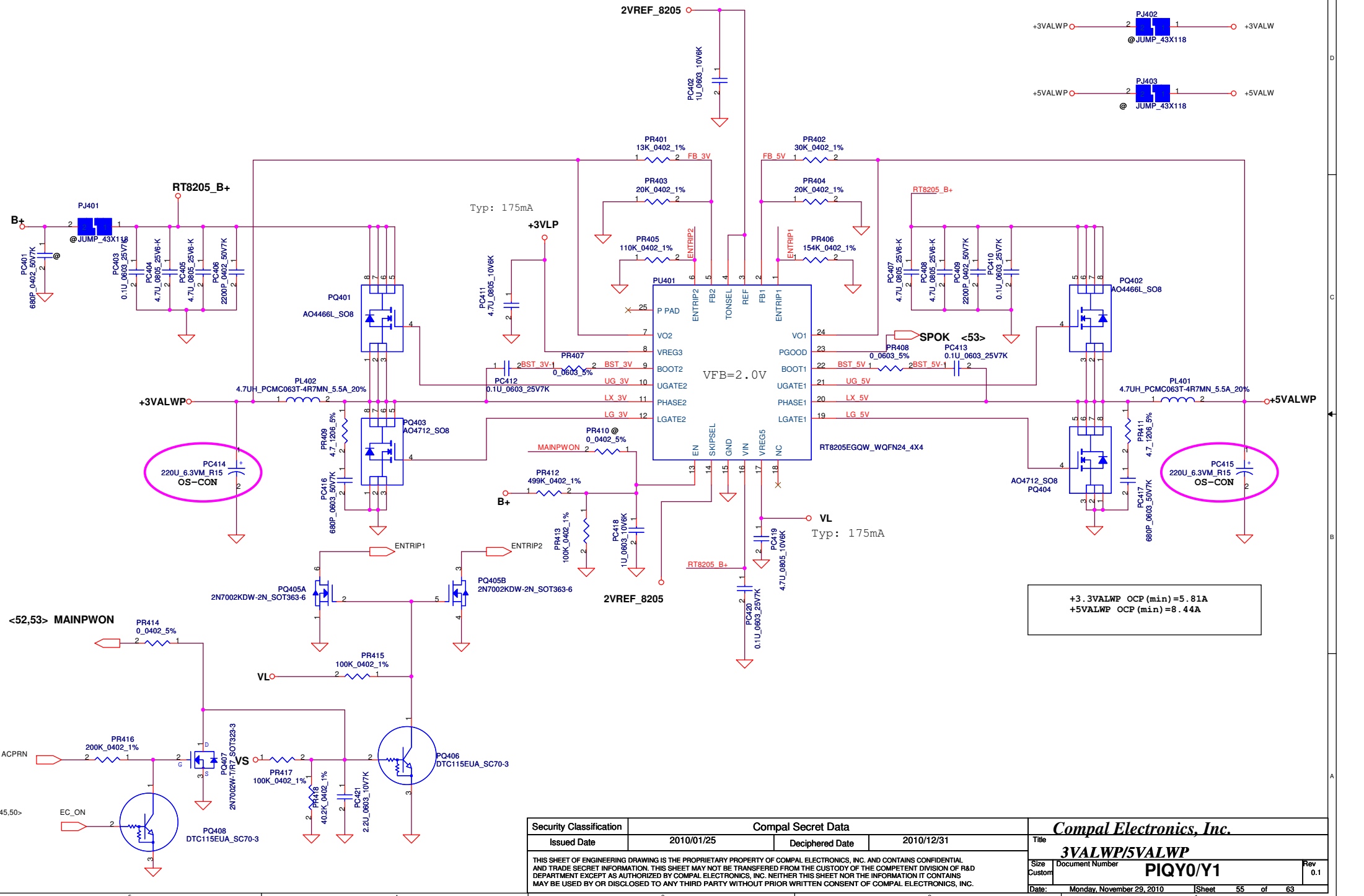
PH201 under CPU botten side :
 CPU thermal protection at 95 degree C
 Recovery at 56 degree C



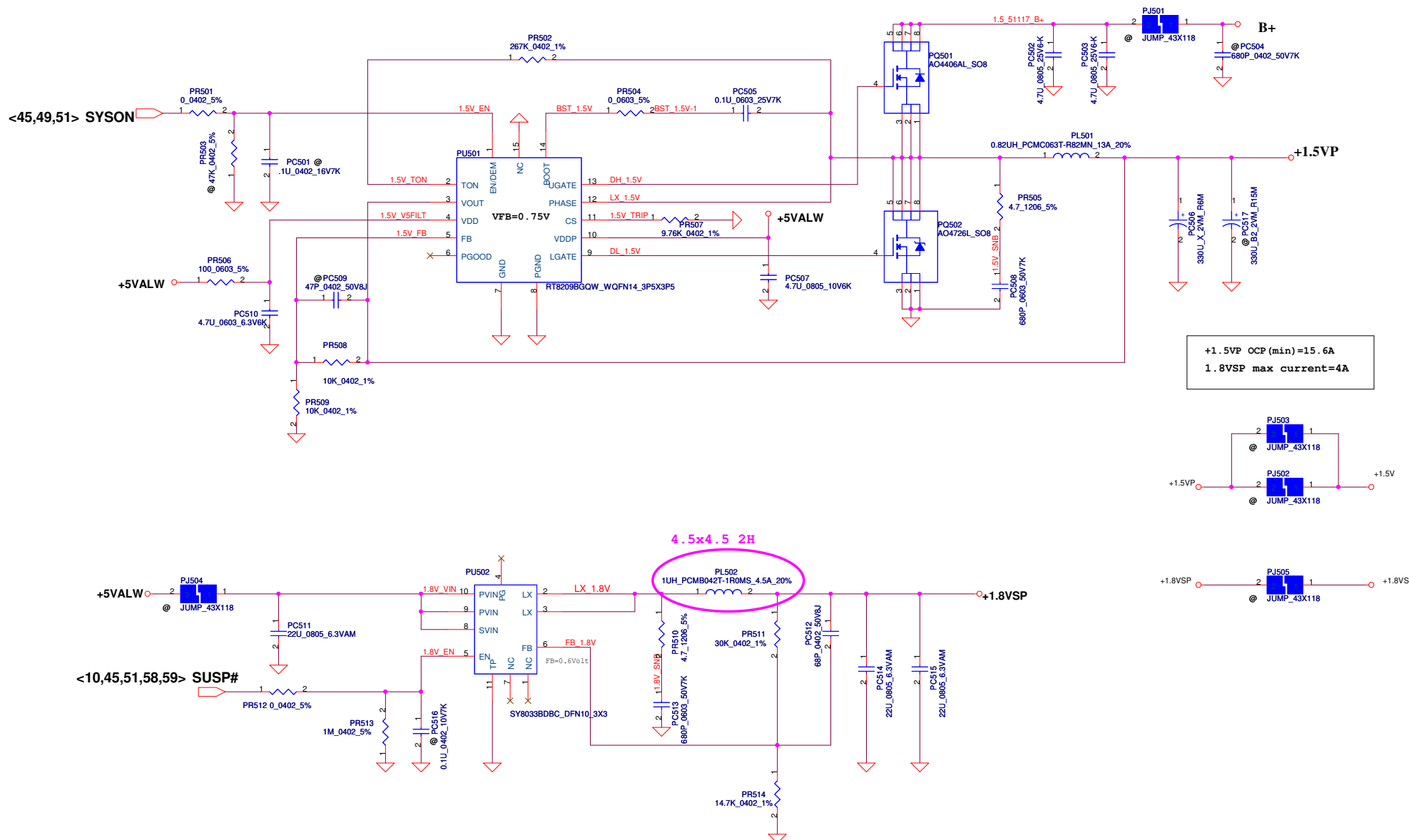
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR-BATTERY CONN/OTP
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				Date: Monday, November 29, 2010	Sheet 53 of 63



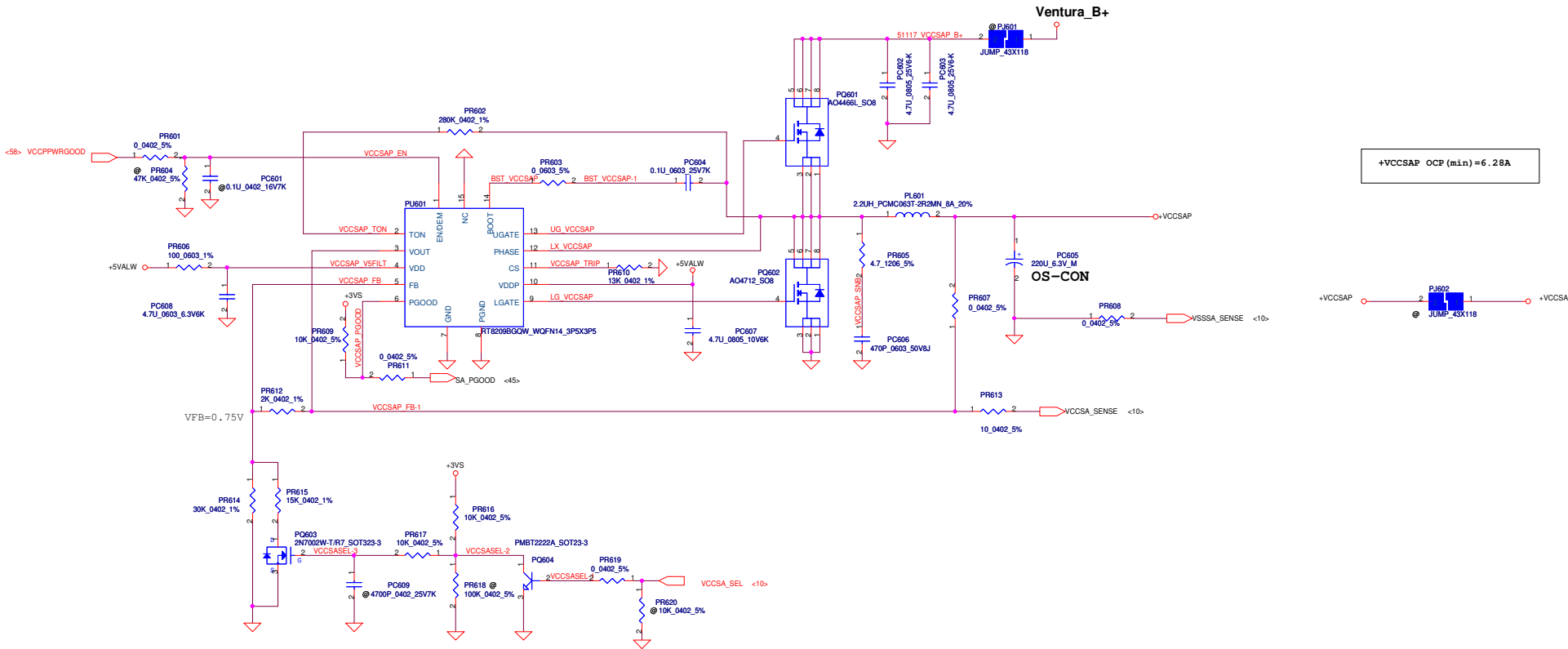
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



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				Date	Monday, November 29, 2010
				Sheet	55 of 63
				Rev	0.1

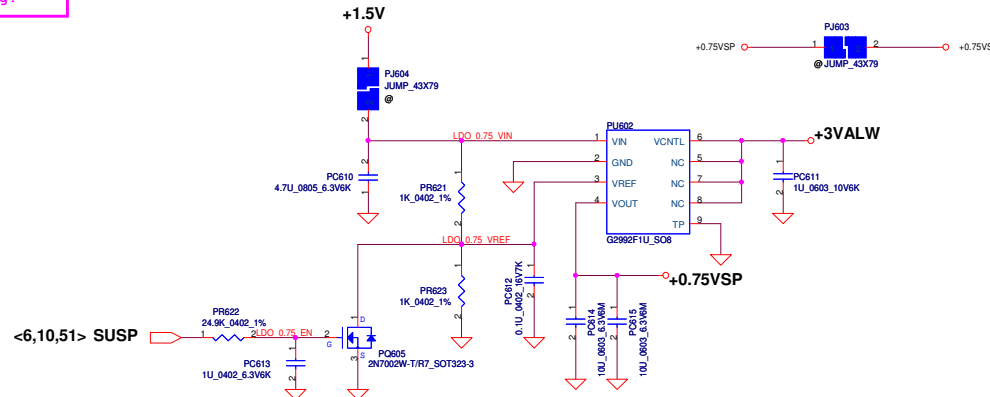


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				Customer	Rev 0.1
				Date:	Monday, November 29, 2010
				Sheet	56 of 63



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note: Use VCCSA_SEL to switch High & Low Level for VID[1] (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.



<10,45,51,56,59> SUSP#

+1.05VS_VCCPP OCP (min)=20.75A

+5VALW

Ventura_B+

B+

+1.05VS_VCCPP

VCCIO_SENSE <9>

Security Classification

Compal Secret Data

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Issued Date

2010/01/25

Deciphered Date

2010/12/31

Title

PWR +1.05VS_VCCPP/1.05VS_VGA

Size

Document Number

PIQY0/Y1

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0.1

Date:

Monday, November 29, 2010

Sheet

58

of

63

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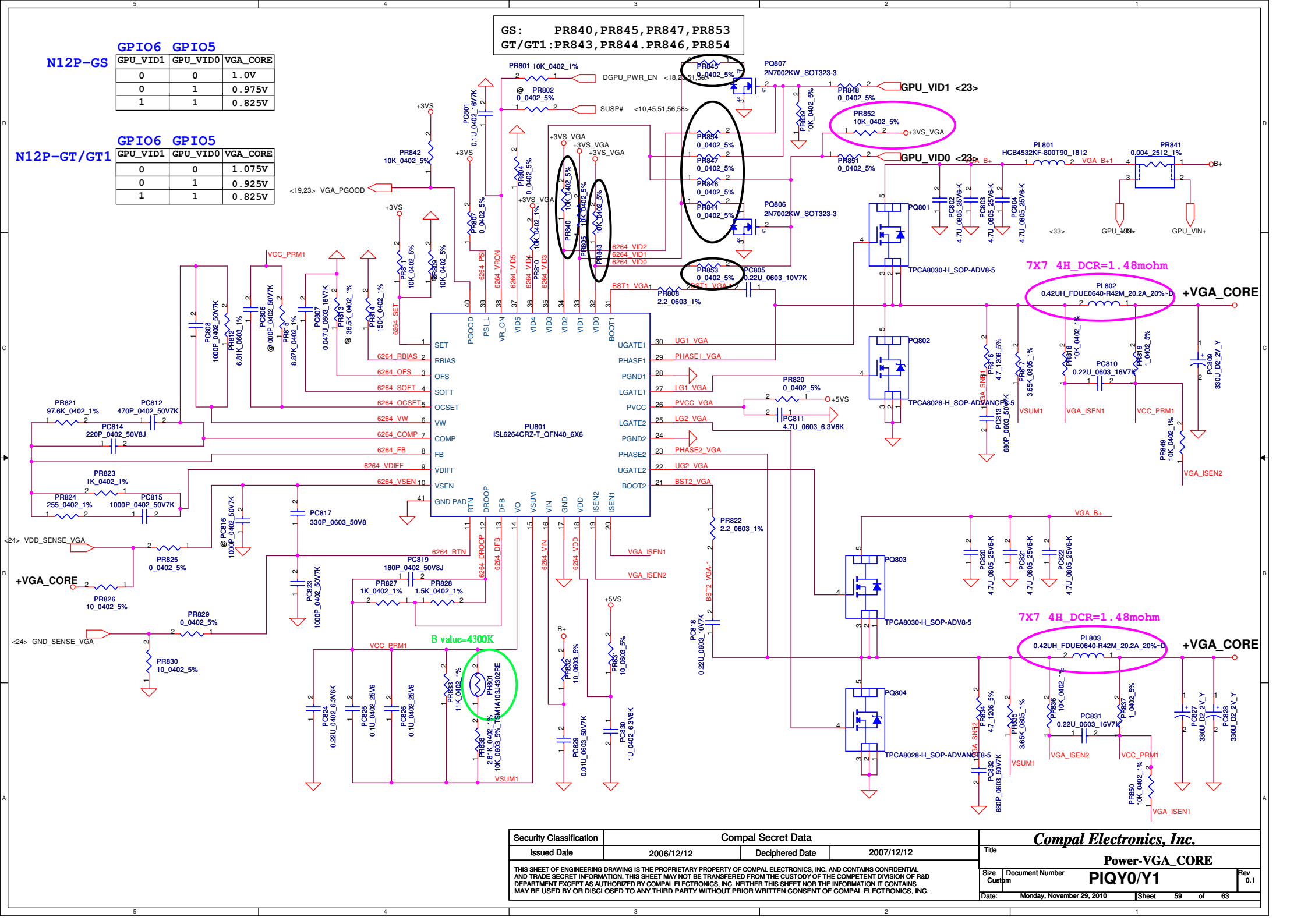
GS: PR840, PR845, PR847, PR853
GT/GT1: PR843, PR844, PR846, PR854

N12P-GS

GPIO6	GPIO5	VGA_CORE
GPU_VID1	GPU_VID0	
0	0	1.0V
0	1	0.975V
1	1	0.825V

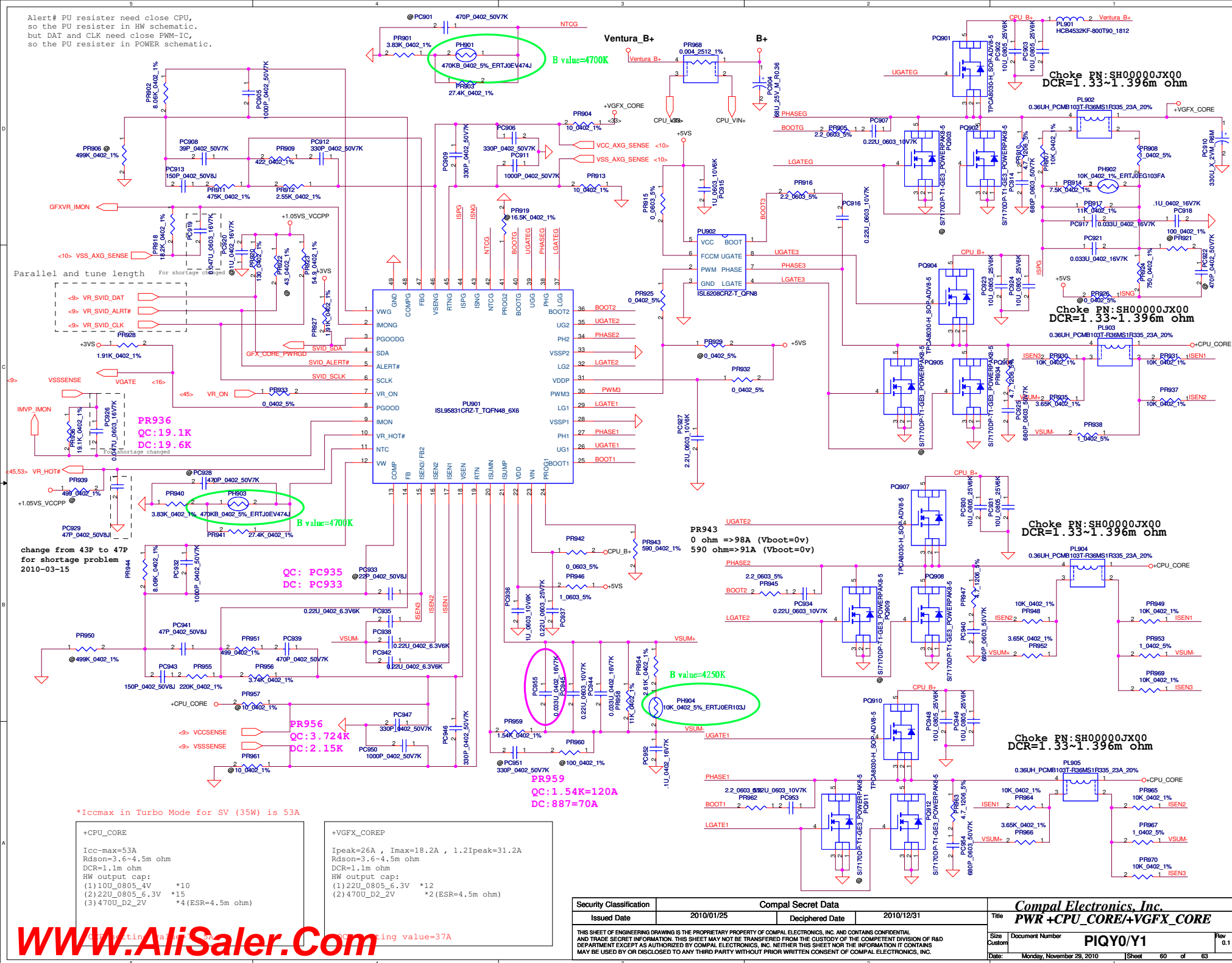
N12P-GT/GT1

GPIO6	GPIO5	VGA_CORE
GPU_VID1	GPU_VID0	
0	0	1.075V
0	1	0.925V
1	1	0.825V



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Size	Document Number	PIQY0/Y1		Rev
Custom				0.1
Date:	Monday, November 29, 2010	Sheet	59	of 63

Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.



Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				PIQY0/Y1	
				Rev 0.1	
Date: Monday, November 29, 2010				Sheet	61 of 63

PIQY0 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
----- EVT TO DVT				
1		P18	Reserve R297	Reserve pull down for PCH GP1053.
2		P18	Exchange SATA port0 & port1	For fast boot function.
3		P50	Change KB light control circuit	Change KB light control from PWM to on/off.
			Delete U55,C908,R1233,R1235,R1236, 1238, R1230, R1231, Q121	
4		P36	Add F2 (poly-fuse)	For HDMI port diode protection.
5		P19	Stuff R303, unstuff R340	Change ESATA_DET# to GP101.
6		P49	Stuff R1068, reserve R1326, Q130	Reserve USB3.0 power swith control inverter circuit.
7		P48	Add R1327	For CHG_ON# pull down.
8		P45	Stuff R996,R139,C815, unstuff R1000,C732,C733,Y5	Change EC CLK from crystal to SUSCLK.
9		P37	Add U60, Q132, C921, R1329, Q133, R1328	Add WLAN power switch circuit
10		P34	Modify JLVDS1	Modify connector from 40pin to 30pin.
11		P09	Add C922	Add C922 to place at CPU sdie.
12		P21	Add R1330	Add for INTVREN control
13		P41	Modify C639	Modify type from 0805 to 0603
14		P45	Modify TP_LED#, PCH_DPWROK and LED_KB_PWM link	Change LED_KB_PWM to U36. pin26 GP1012.
15		P18	Delete EN_CARD_PW#, EN_WOL#	Add FAST_BOOT# to replace EN_CARD_PW# and EN_WOL#
16		P48		Remove USB charger function
17		P42	Change C660, C661 from 3300p to 0.1u	For 100Hz High Pass filter
18		P43	Replace R958, R959 to C924, C925 0.033u	For 100Hz High Pass filter
19		P14	Add one more SPI-ROM circuit	For dual BIOS function
20		P50	Remove EC_SMB_CK2, EC_SMB_DA2 link to JP13	Remove light sensor function
21		P14	Add Q134, R1345, R1346	Add for Fast boot SPI ROM selection by EC.
22		P34	Add R1341, C926	Added for EMI request
23		P37, P44	Add R1342,R1343	Added for WLAN and CARD reader Reset signal.
24		P19	Add R1344	Added for VENTURA detection.
----- DVT TO PVT				
1		P10	Add R1347, Change R56 to 20K,	Modify S3 1.5V reduction sequence.
2		P45	Add Q135	Modify PROCHOT control circuit.
			Modify R980 link to +5VALW	Change USB_ON PU power rail

