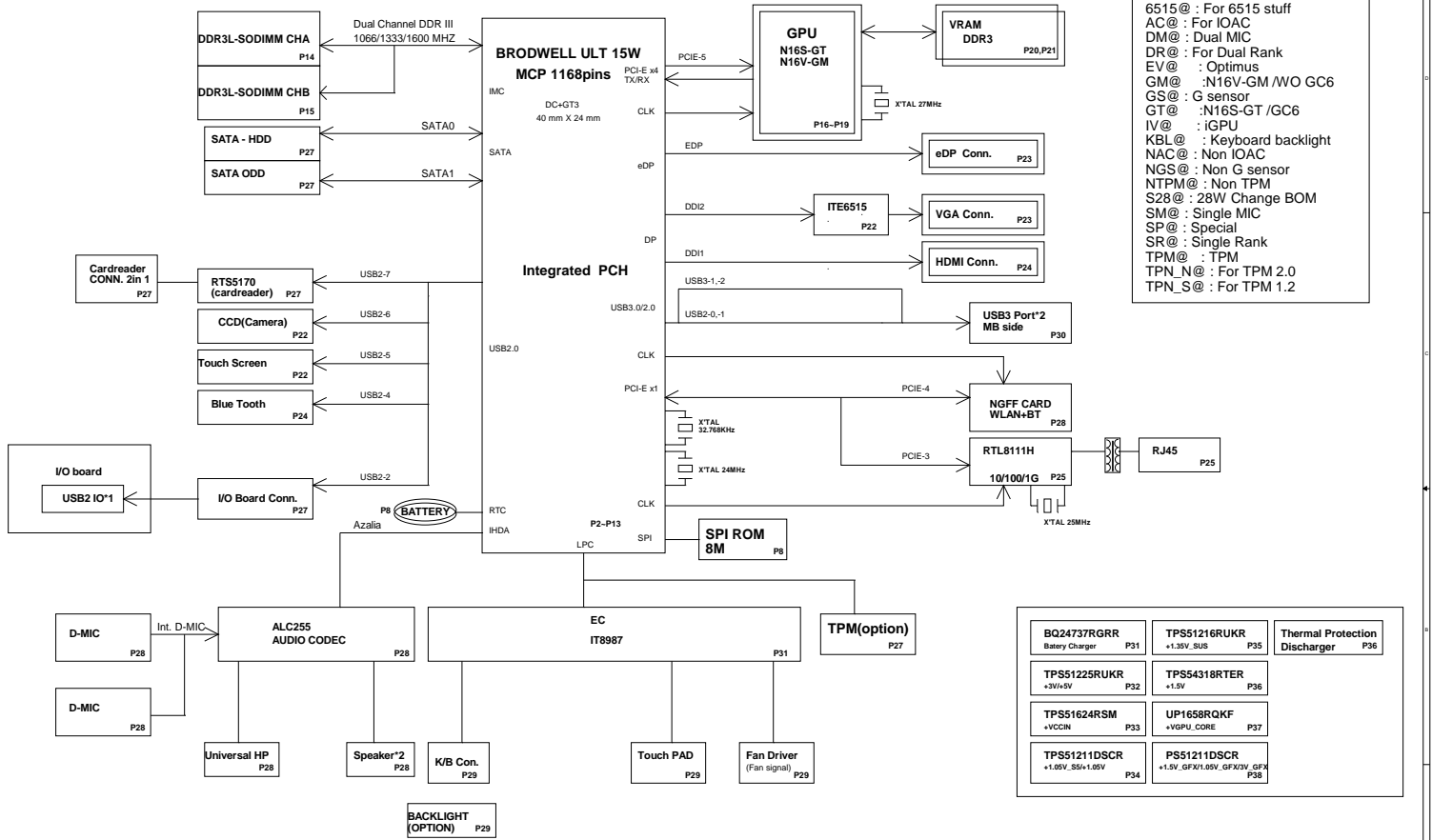
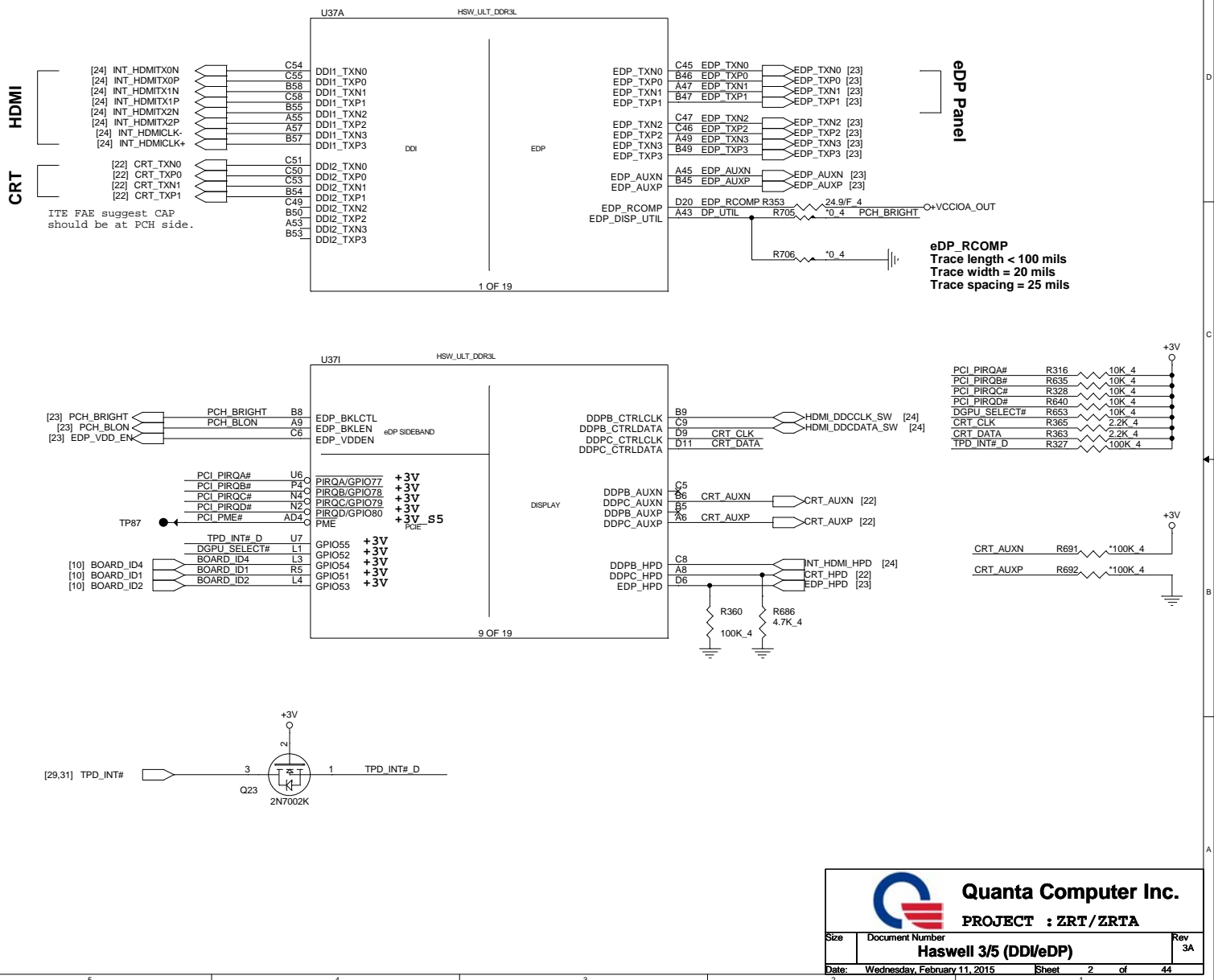


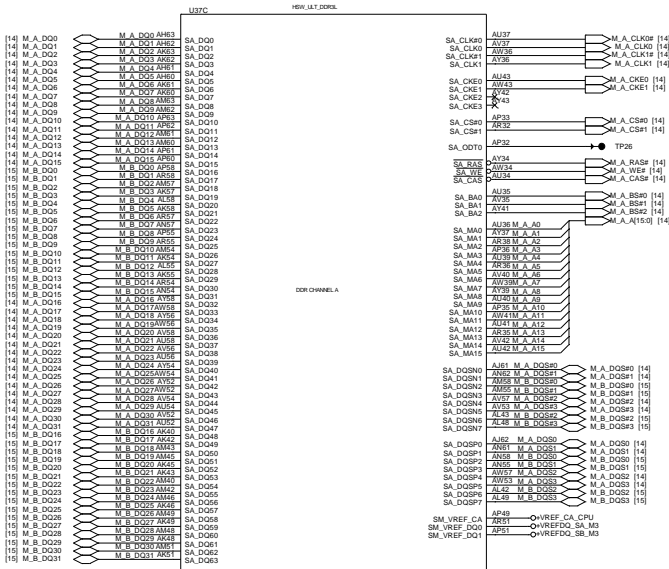
ZRT/ZRTA_GDDR3 BWD ULT SYSTEM BLOCK DIAGRAM



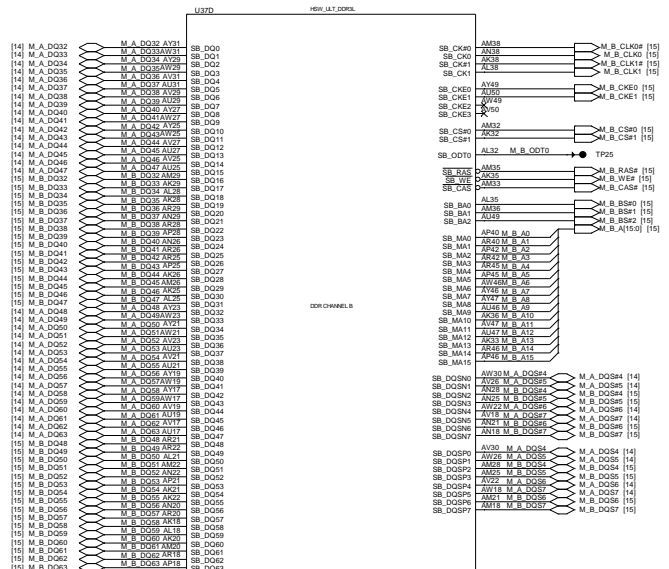
Haswell ULT (DISPLAY,eDP)



Haswell ULT (DDR3L)



Haswell Processor (DDR3)

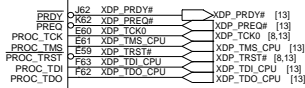
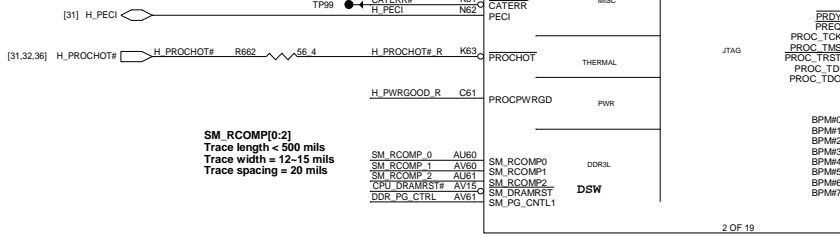


Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4-6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1-11.25 inches

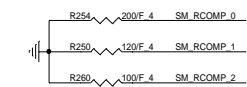
CPU_PLTRST# (50ohm)
Trace Length: 10-17 inches



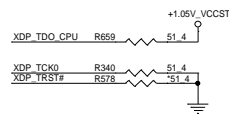
TCK.TMS
Trace Length < 9000mils

BPM#[0:7]
Trace Length 1-6 inches
Length match < 300 mils

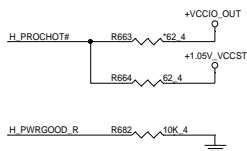
DRAM COMP



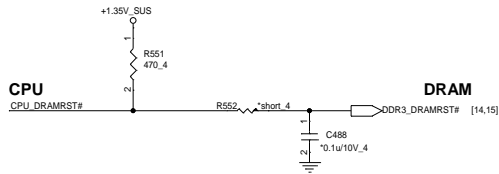
XDP PU/PD



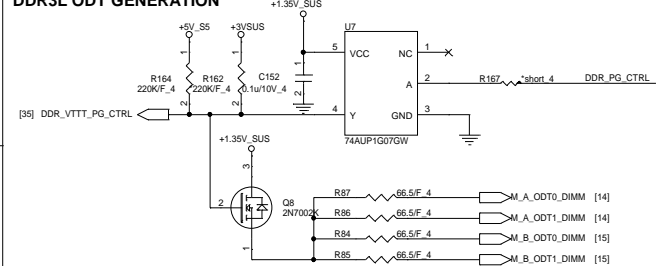
PU/PD of CPU



DRAMRST



DDR3L ODT GENERATION

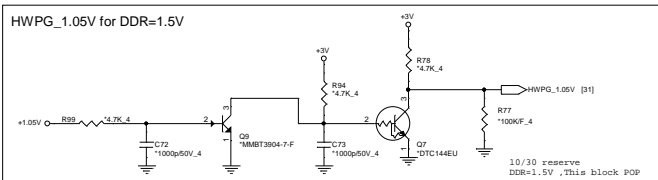


Quanta Computer Inc.
PROJECT : ZRT / ZRTA

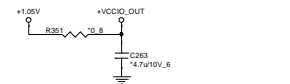
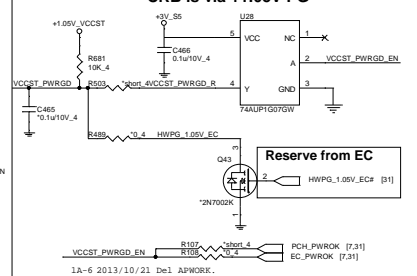
Size	Document Number	Rev
	Haswell 1/5 (PEG/DM/FDI)	3A
Date:	Wednesday, February 11, 2015	Sheet 4 of 44

Haswell ULT (POWER)

HWPG_1.05V for DDR=1.5V

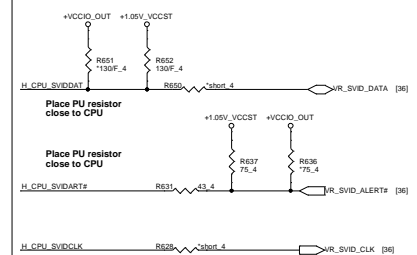


VCCST PWRGD CRB is via +1.05V PG



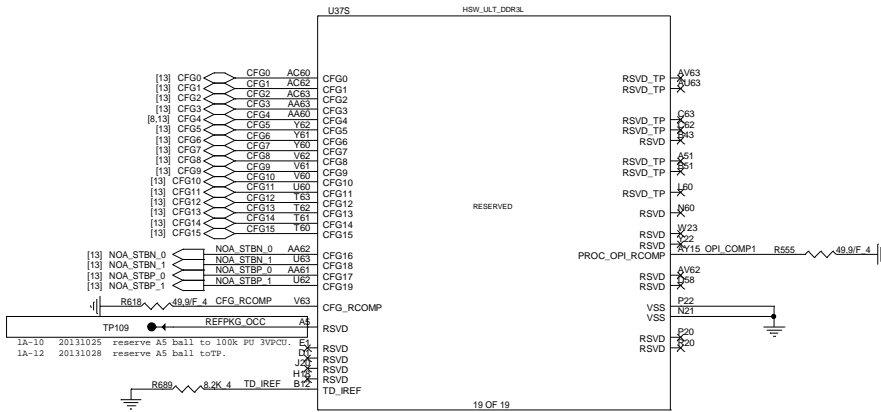
SVID

Layout note: need routing together
and ALERT need between CLK and DATA.



VCC Output Decoupling Recommendations		
470uF x4	7343	TOP socket side
22uF x8	0805	4 on TOP, 4 on BOT near socket edge
22uF x11	0805	TOP, inside socket cavity
10uF x11	0805	BOT, inside socket cavity

Haswell ULT (CFG,RSVD)



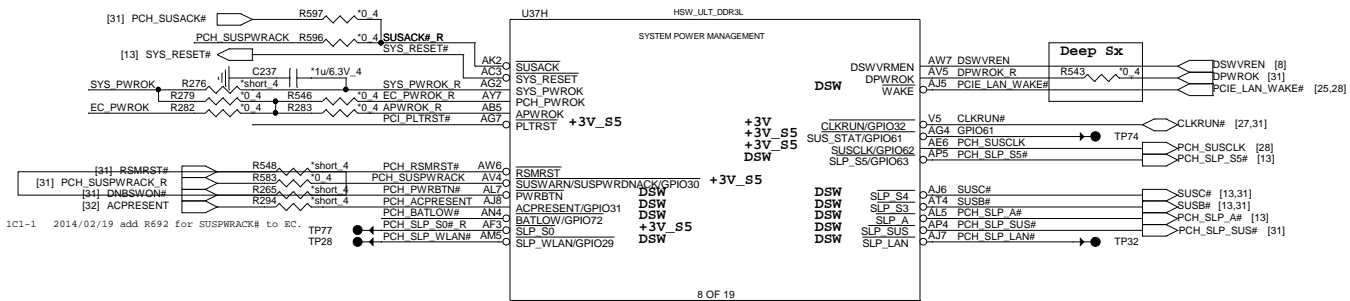
Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R289 ~*1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R606 ~*1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R610 ~*1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED/DEFAULT; IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R614 ~*1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO SVID ACTIVITY	CFG9 R619 ~*1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R295 ~*1K 4

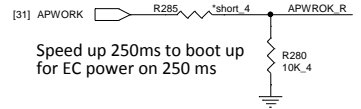
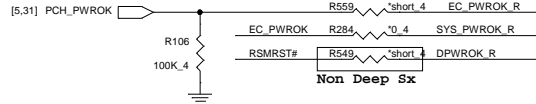
Quanta Computer Inc.
PROJECT : ZRT / ZRTA
Haswell 5/5 (CFG/GND)

Size Document Number
Date: Wednesday, February 11, 2015 Sheet 6 of 44 Rev 3A

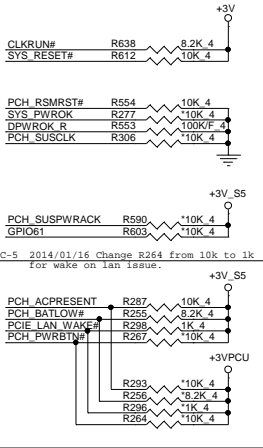
Haswell ULT PM (PM)



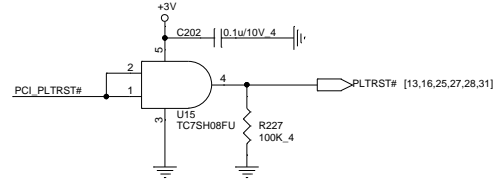
Power Sequence



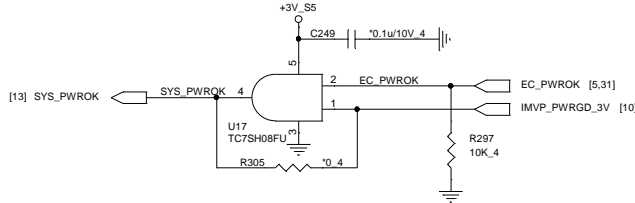
PCH PM PU/PD



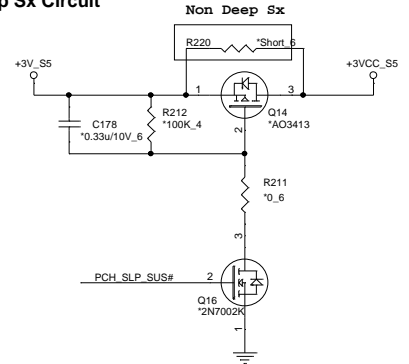
PLTRST# Buffer



SYSPWOK



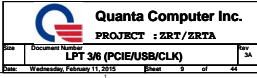
Deep Sx Circuit



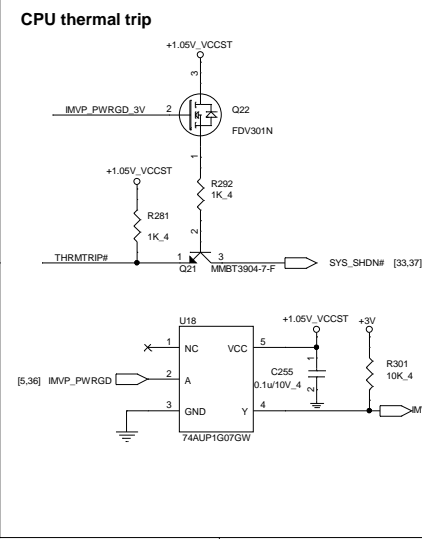
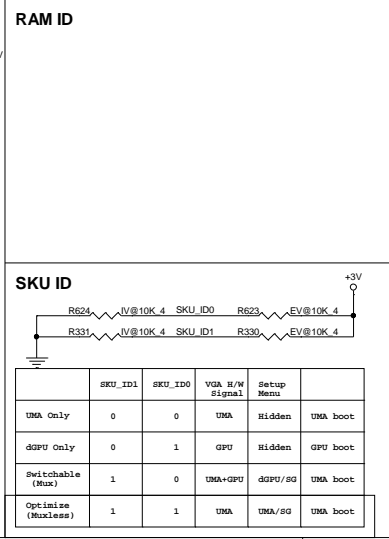
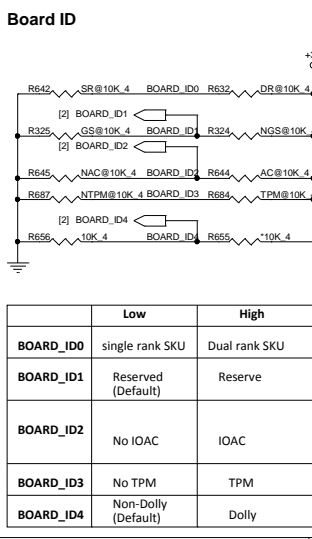
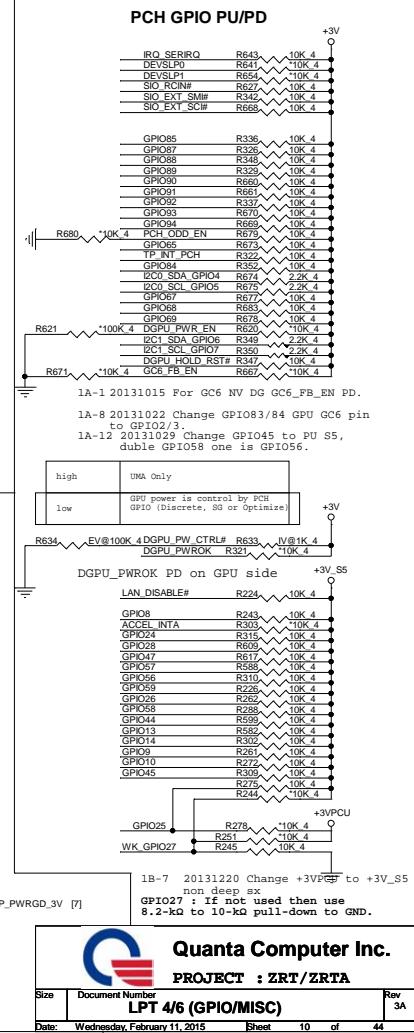
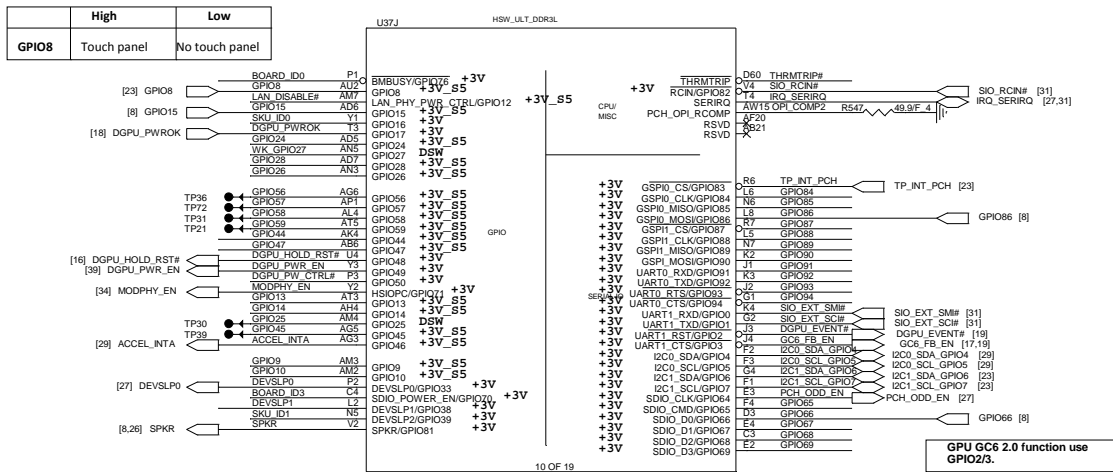
		Quanta Computer Inc. PROJECT : ZRT / ZRTA
Size	Document Number	Rev
	LPT 1/6 (DMI/FDI/VGA)	3A
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Haswell ULT PCH (CLOCK)

1A-1 2013/10/15 following up acer define and swap USB3 and USB2



Haswell ULT PCH (GPIO,CPU/MISC,NCTF)



Quanta Computer Inc.

PROJECT : ZRT/ZRTA

LPT 4/6 (GPIO/MISC)

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Rev 3A

[illegible]

1A-1 2013/10/11 del LDO change to MOS.

PCH VCCHSIO Power

1A-1 2013/10/11 del LDO change to MOS.

Two circuit diagrams for PCH VCCHSIO Power are shown. The left diagram is labeled "41mA" and the right diagram is labeled "42mA". Both diagrams show a power supply circuit with an inductor (L27 and L26 respectively) and capacitors (C543, C542, C524 for the 41mA circuit; C534, C540, C529 for the 42mA circuit). The input voltage is +1.05V_MOOPHY and the output voltage is +V1.05S_AUSB3PLL for the 41mA circuit and +V1.05S_ASATA3PLL for the 42mA circuit. The current is 41mA and 42mA respectively.

2013/10/31 PN change to H=0.85, L17 H=0.9

VCCAPLL power

The schematic shows a power supply for VCCAPLL. It starts with a +1.05V input connected to a network of inductors (L21, L22) and capacitors (C303, C293, C282). The output is labeled +V1.055_APLL0P1 with a current of 57mA. Ground connections are shown for C303, C293, and C282.

PCH HDA Power

The schematic shows a power supply for PCH HDA. It starts with a +3V_SS input connected to a network of inductors (R222, R223) and capacitors (C199). The output is labeled +V3.30X_1.50X_1.80X_AUDIO with a current of 11mA. A note indicates to "Place close to ball" for the capacitor C199. Ground connections are shown for C199 and the output.

PCH HDA Power

11mA

3V_55


+V3.3DX_1.5DX_1.8DX_AUDIO

R222

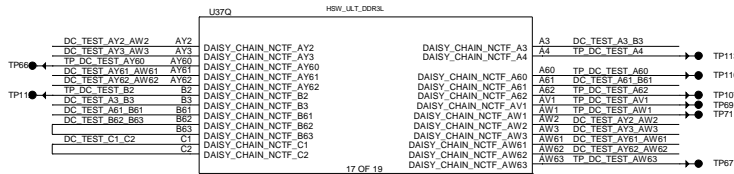
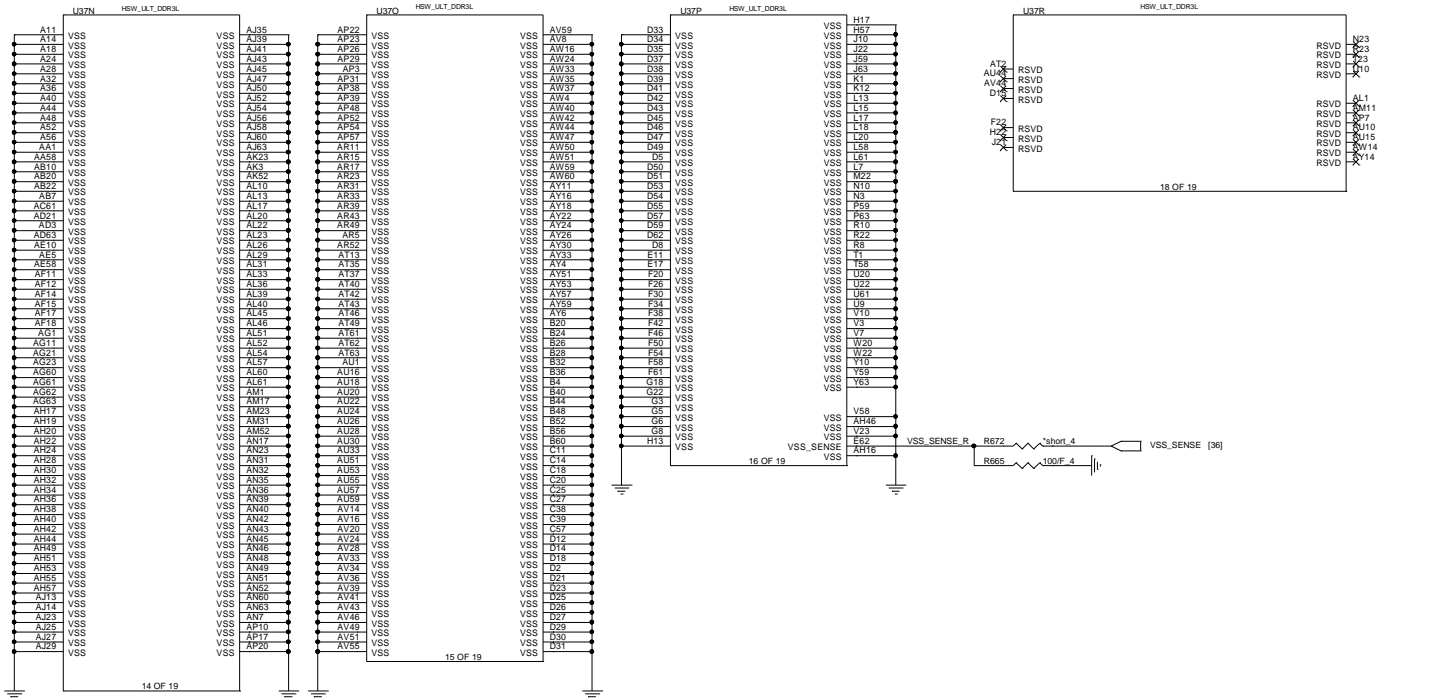
Shost_6

C199
0.1uF/10V_4

Place close to ball

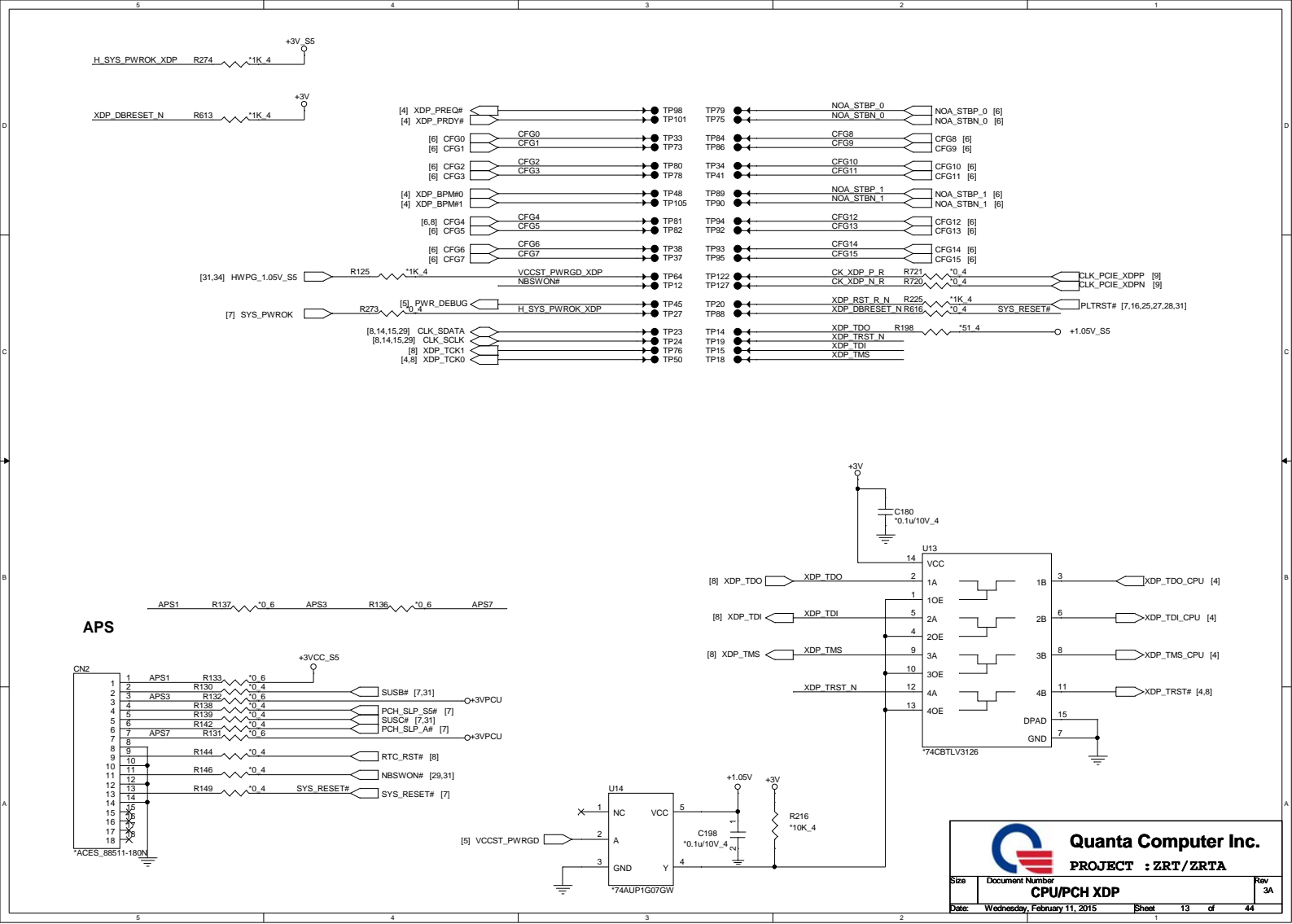
 Quanta Computer Inc. PROJECT : ZRT / ZRTA		
Size	Document Number	Rev
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Date:	Wednesday, February 11, 2015	Sheet 11 of 44

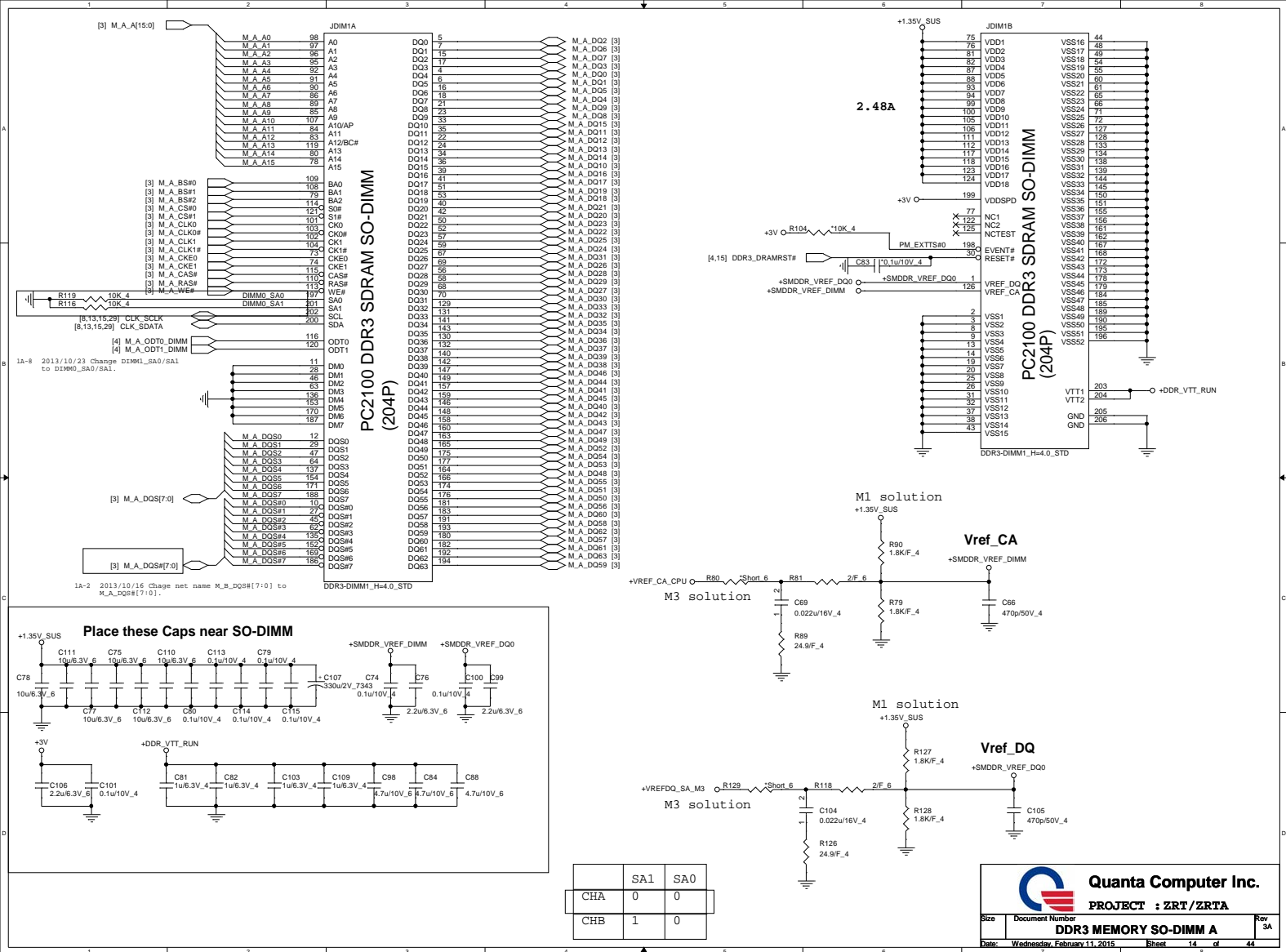
Haswell ULT (GND)

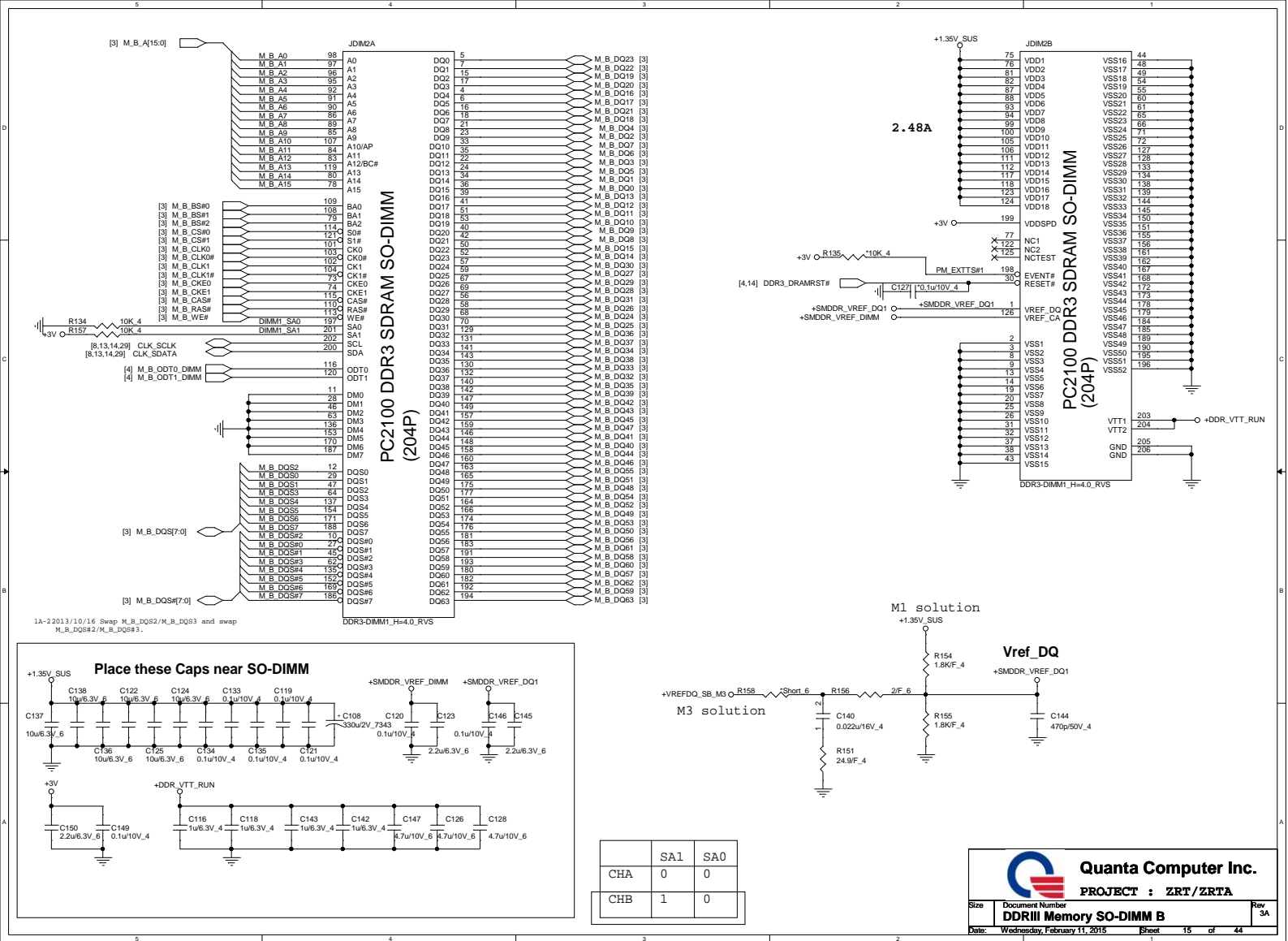


Quanta Computer Inc.
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	LPT 6/6 (GND)	3A
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PEX_I0VDD + PEX_I0VDDQ = 1.042A

PEX_PLL HVDD +
PEX_SVDD_3V3 = 143mA


PEX_PLLVDD = 130mA

NVDD = 32.22 - 26.66 A

VDD33 = 56mA

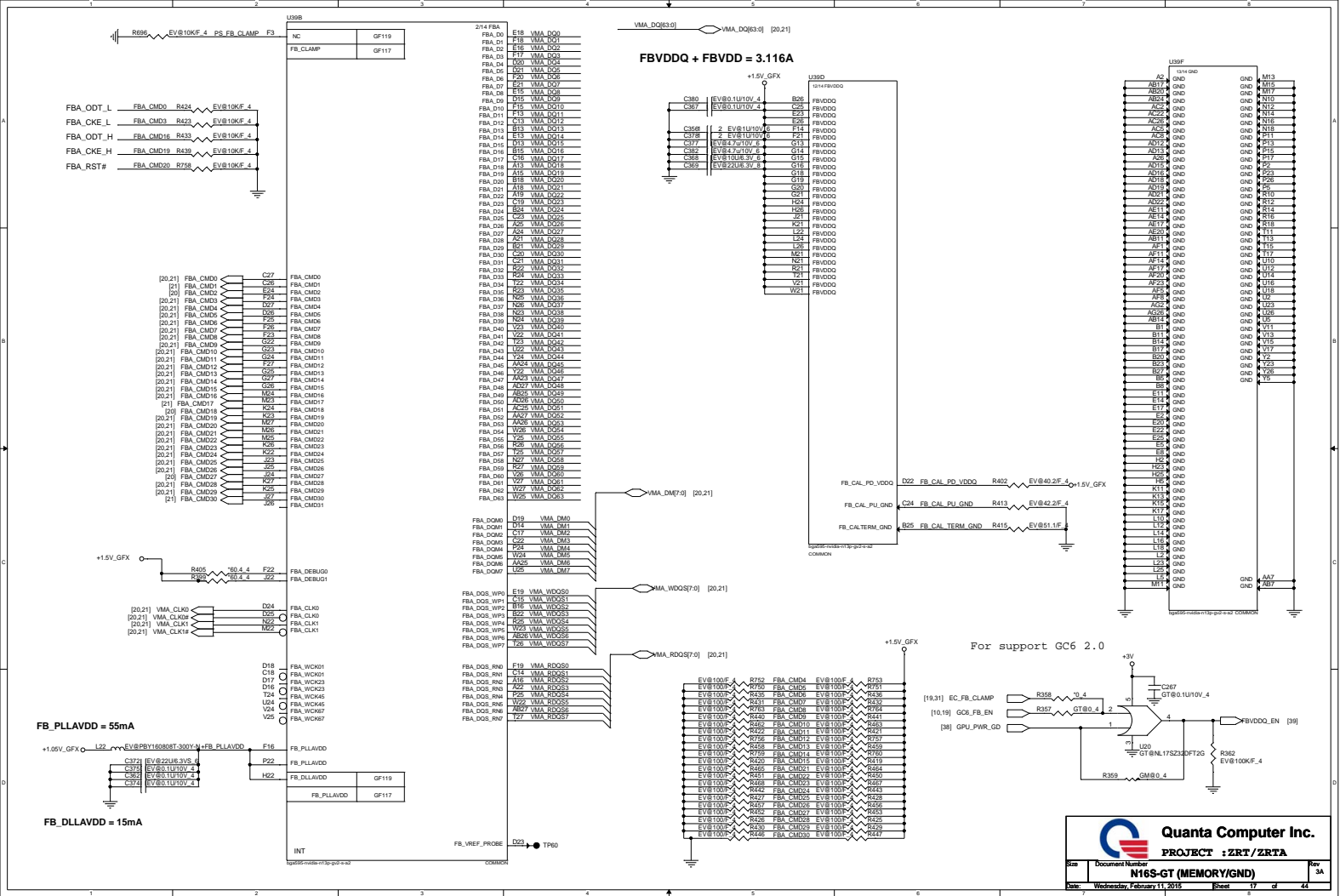
Power up sequence

Power down sequence

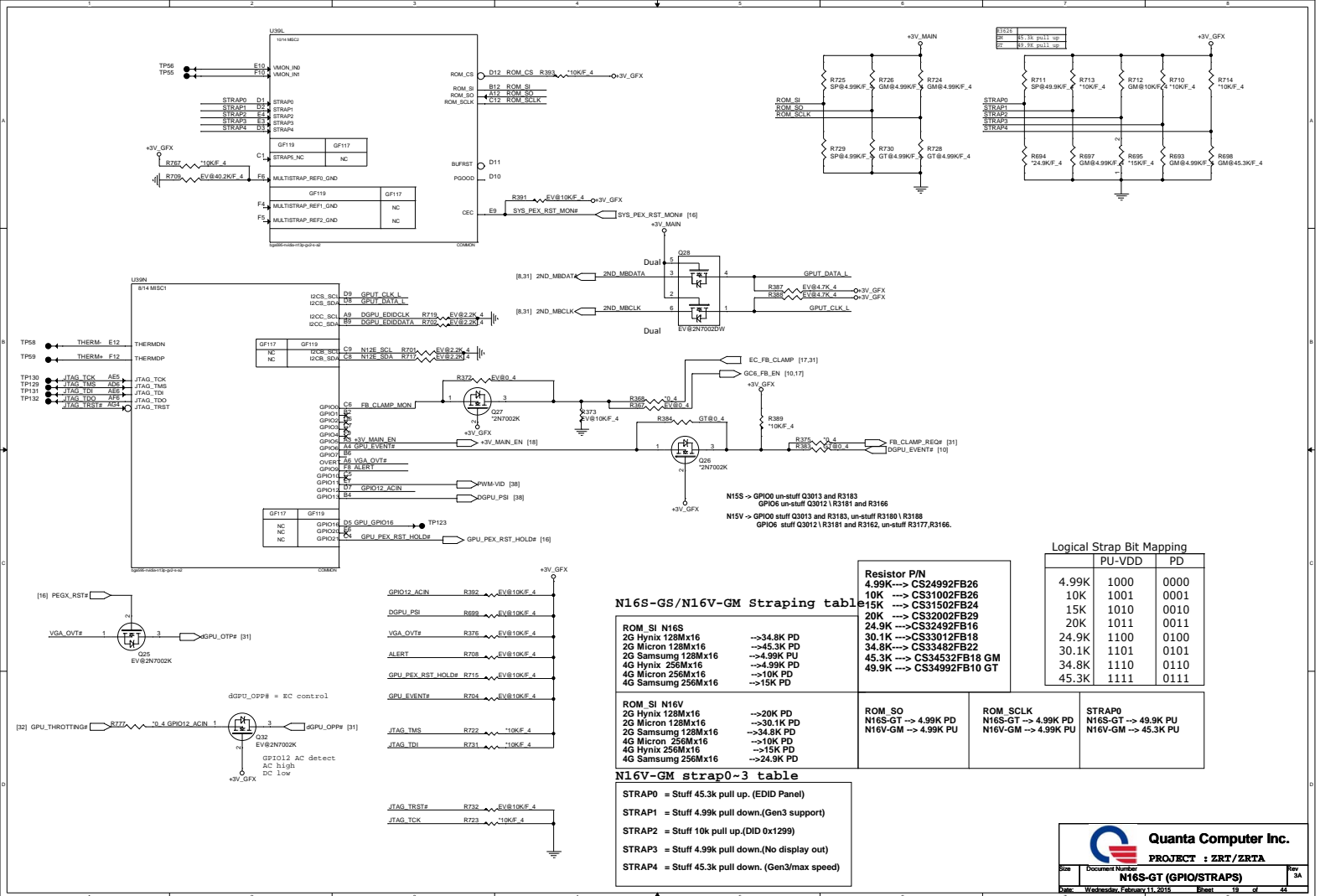


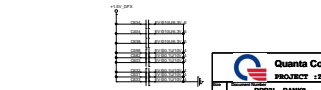
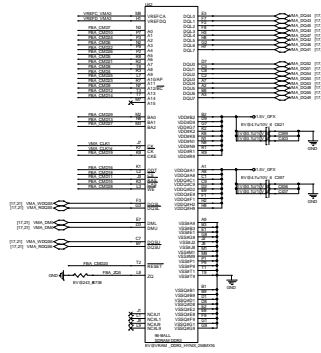
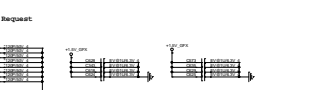
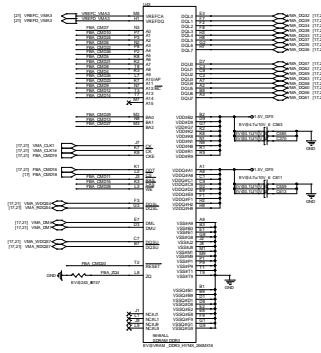
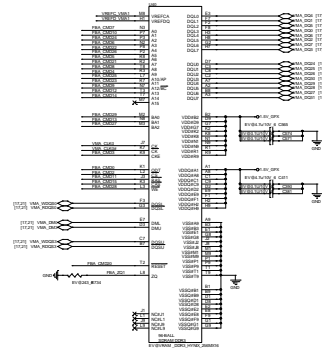
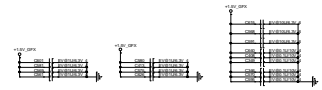
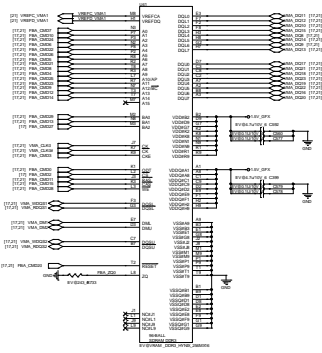
Quanta Computer Inc.
PROJECT : ZRT / ZRTA

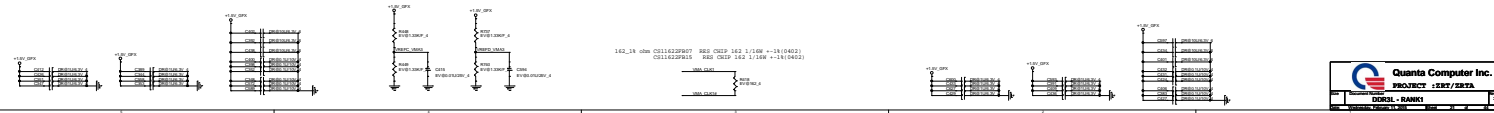
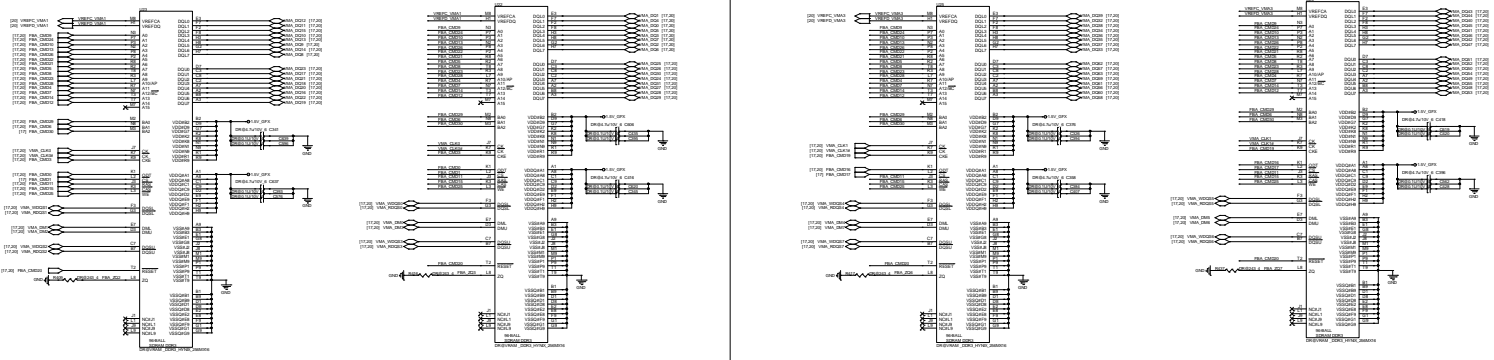
Size	Document Number	N16S-GT (PCIe IF) NVDD	Rev	3A
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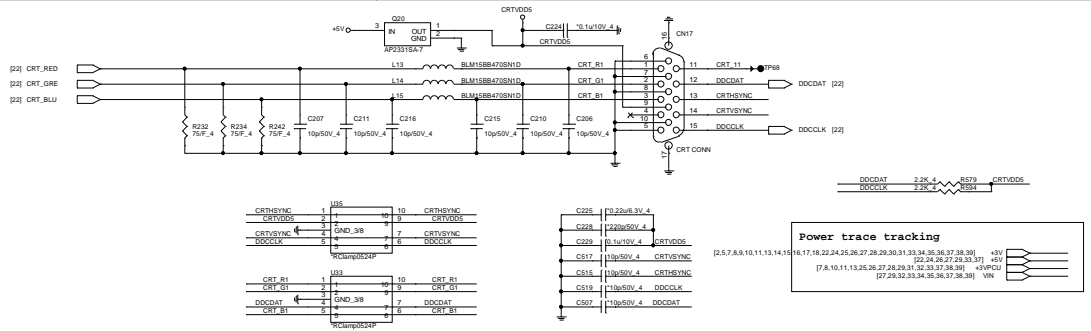




 Quanta Computer Inc. PROJECT : ZRT/ZRTA	
Size	Document Number DP to VGA IT6165
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10-1 2014/01/10 Remove U29 and add U40 and U41.

The diagram shows the removal of U29 and the addition of U40 and U41. U29 is a 74VHC123DFG timer. U40 is a 74VHC123DFG timer. U41 is a 74VHC123DFG timer. The diagram shows the pin connections for U29, U40, and U41, including power supply connections to +5V and GND, and signal connections to HSYNC and VSYNC.



Hall Sensor (HSR)

1st AL009240000 – BCD
2nd AL009132001 – ANC

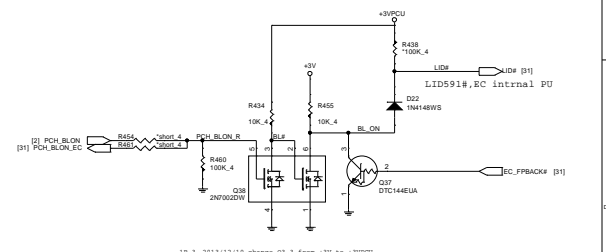
LCD Power

The diagram shows the LCD power circuit. A 3V regulator (U543) provides power to the LCD module. The regulator's input is connected to a 3V supply through a 100K pull-up resistor (R470). The regulator's output is connected to the LCD module's VCC pin. The LCD module's GND pin is connected to ground. The LCD module's EDP pin is connected to the EDP pin of the LCD module through a 100K pull-up resistor (R470). The LCD module's EDP pin is also connected to the EDP pin of the LCD module through a 100K pull-up resistor (R470). The LCD module's EDP pin is also connected to the EDP pin of the LCD module through a 100K pull-up resistor (R470).

[2] EDP_VDD_EN \rightarrow R465 \rightarrow 100k \rightarrow EDP_VDD_EN_3

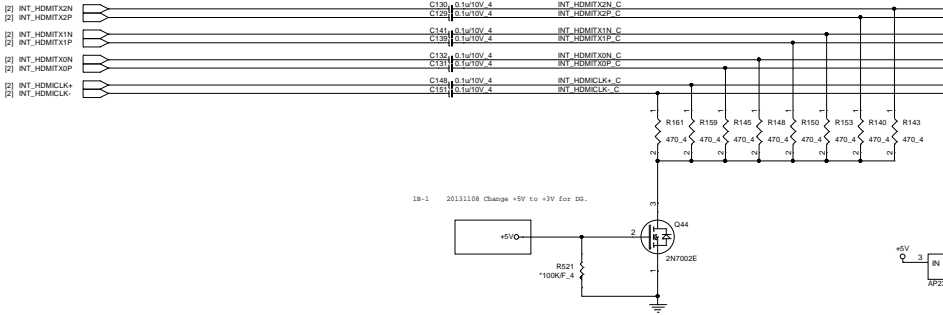
Touch screen level shift I2C(reserve)

TYPD->100KHz, TS=400KHz
Intel design guide suggestion
MCP PIN ID:
For touch V_D TS<35inch
400kHzID-10Hz <+2.4-0.4k.
100KHz 10-10Hz<9K-1K.

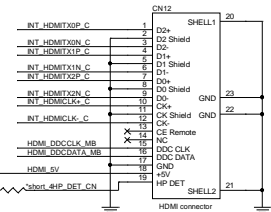


HDMI

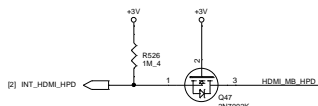
From PCH



HDMI connector

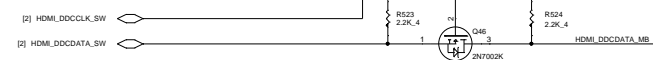


HDMI-detect

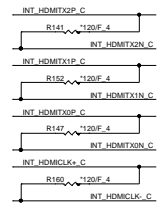


I2C

From PCH



EMI



Power trace tracking

[2,5,7,8,9,10,11,12,14,15,16,17,18,22,23,25,26,27,28,29,30,31,33,34,35,36,37,38,39]

+3V
+5V



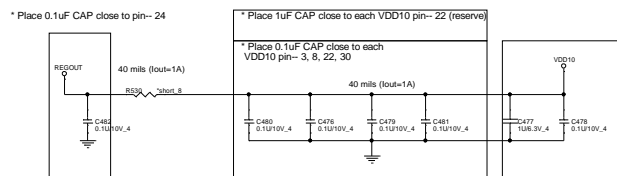
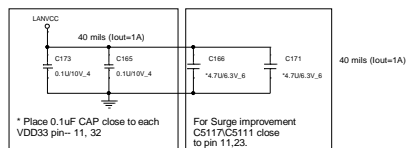
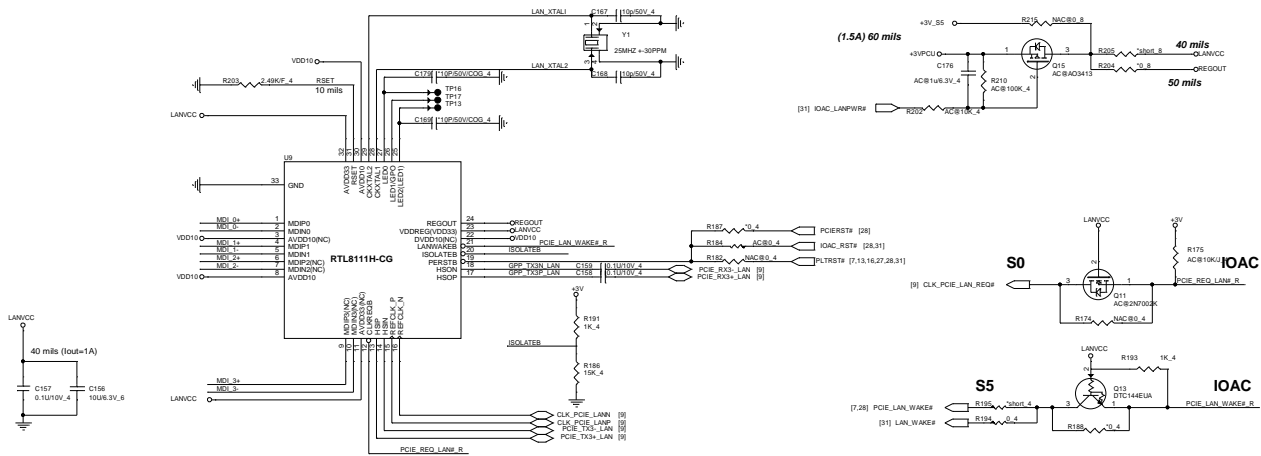
Quanta Computer Inc.

PROJECT : ZRT/ZRTA

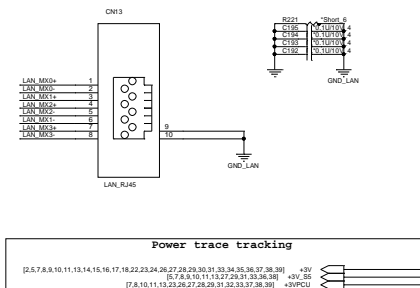
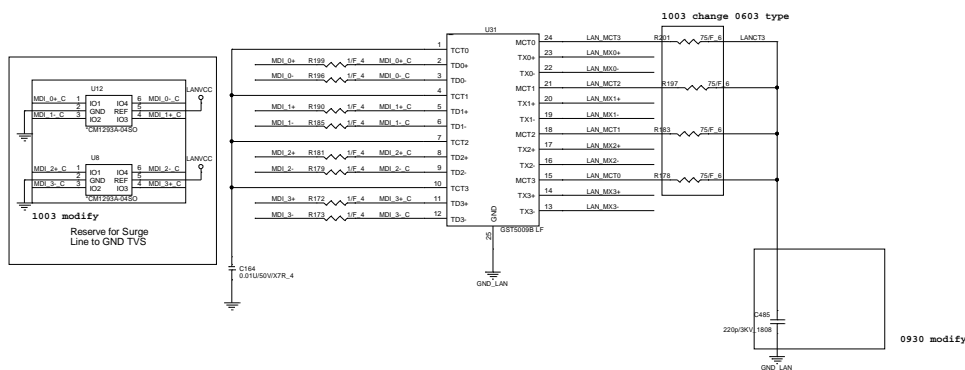
HDMI (PS8101)

Size	Document Number	Rev
1A		1A

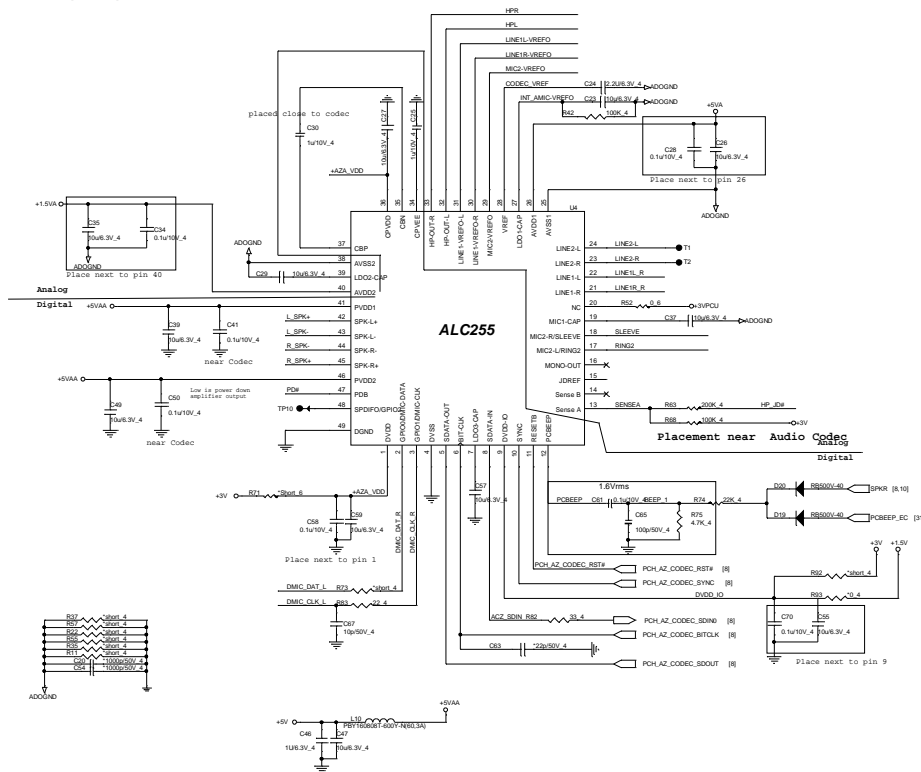
LAN



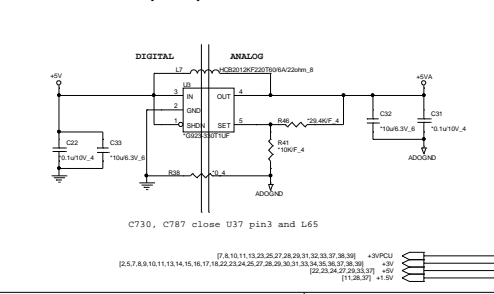
Transformer



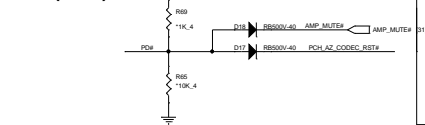
Codec(ADO)



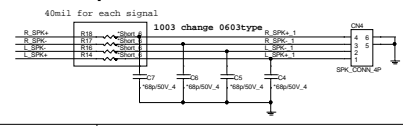
Codec PWR 5V(ADO)



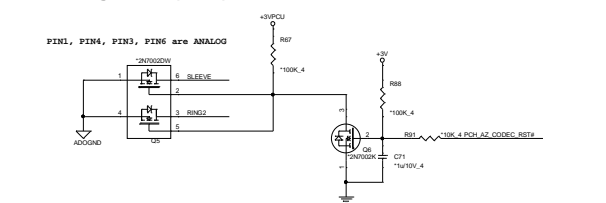
Mute(ADO)



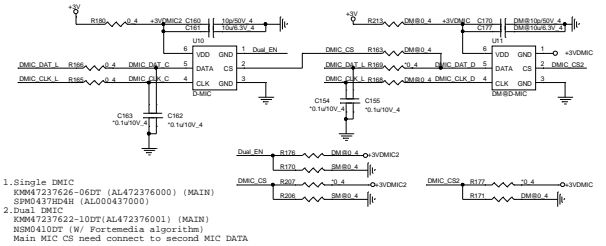
Internal Speaker



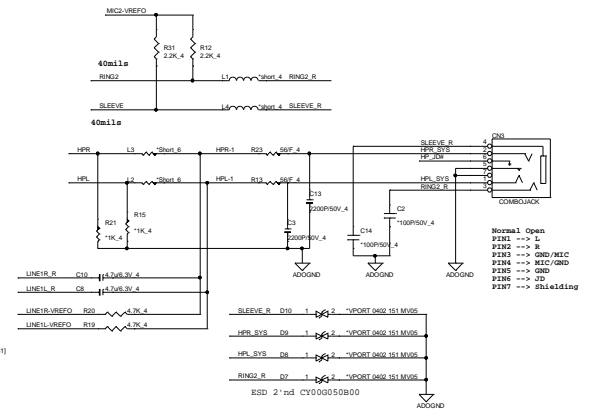
Grounding circuit(ADO)



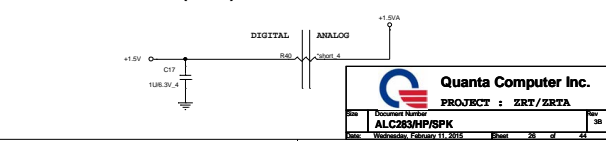
D-Mic



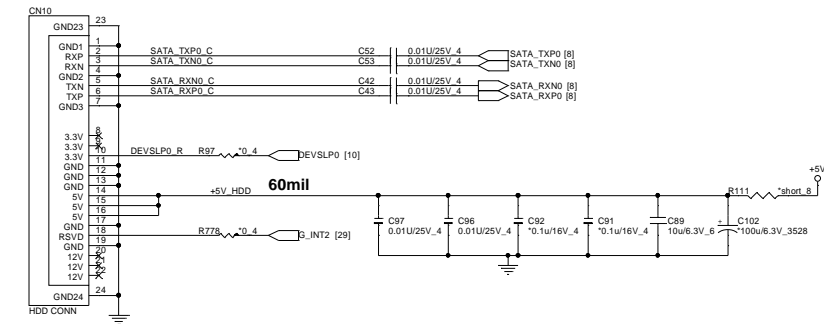
Universal Audio Jack



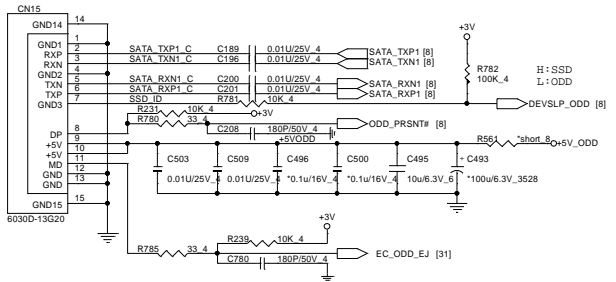
Codec PWR 3V/1.5V(ADO)



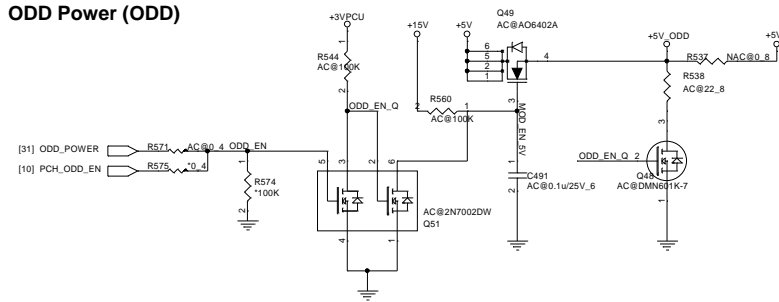
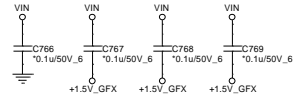
2.5" SATA HDD (HDD)



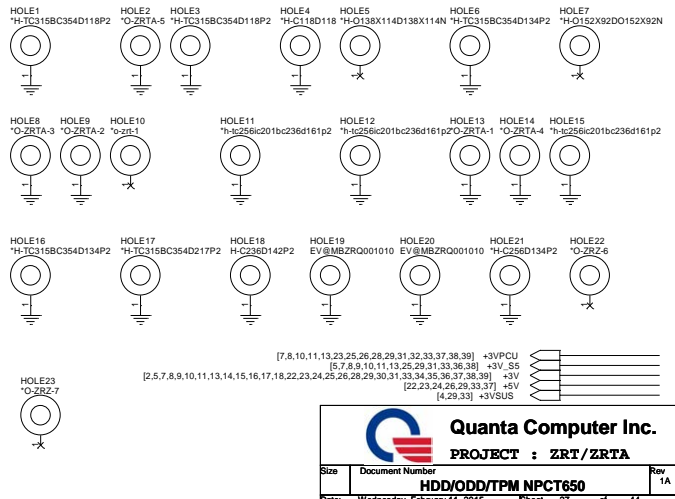
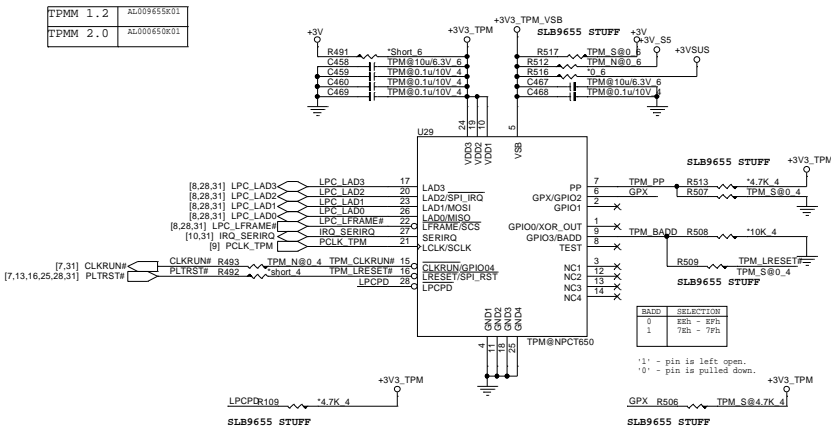
SATA ODD Connector(ODD)



ODD Power (ODD)

**EMI**

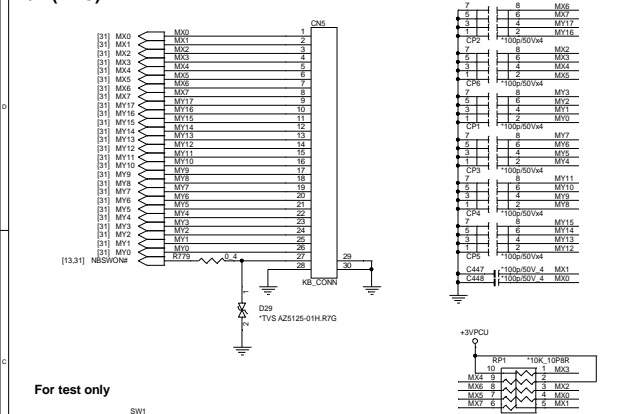
TPM NPCT650 (TPM)



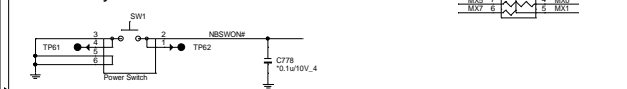
[7,8,10,11,13,23,25,26,27,29,31,32,33,37,38,39] +3VPCU
[11,26,37] +1.5V
[2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,25,26,27,29,30,31,33,34,35,36,37,38,39] +3V



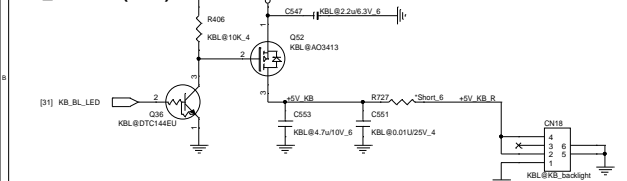
K/B (KBC)



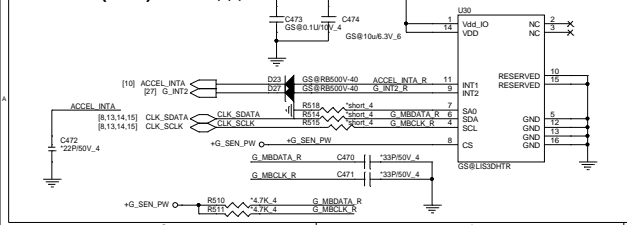
For test only



KB_BL LED (KBL)

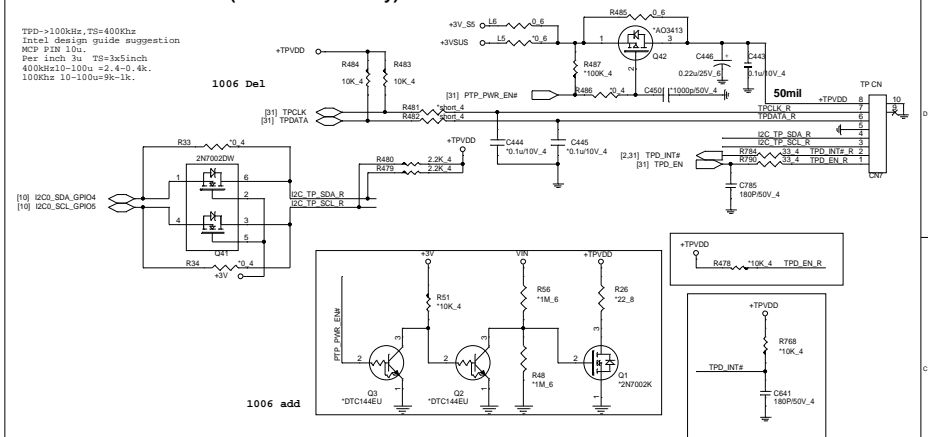


G-sensor(ACS)

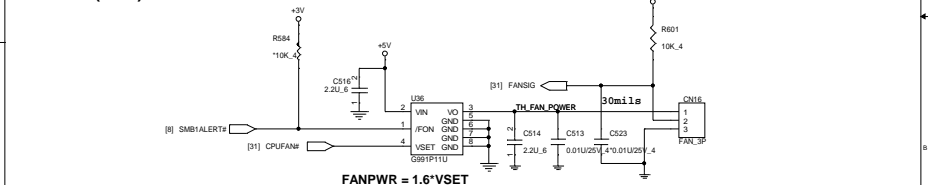


3	
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)	

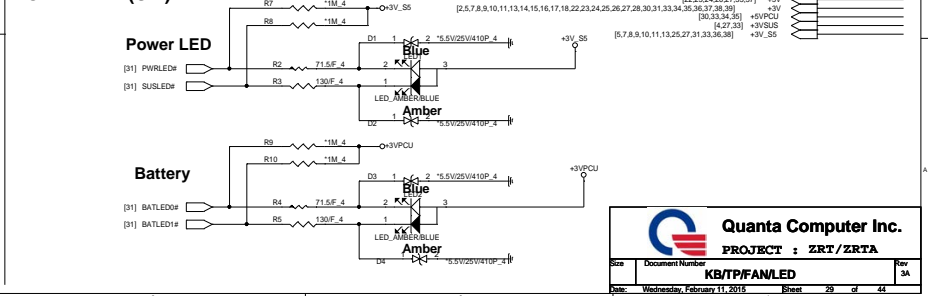
TPD->100kHz, TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10-100u = 2.4-0.4k.
100Khz 10-100u=9k-1k.



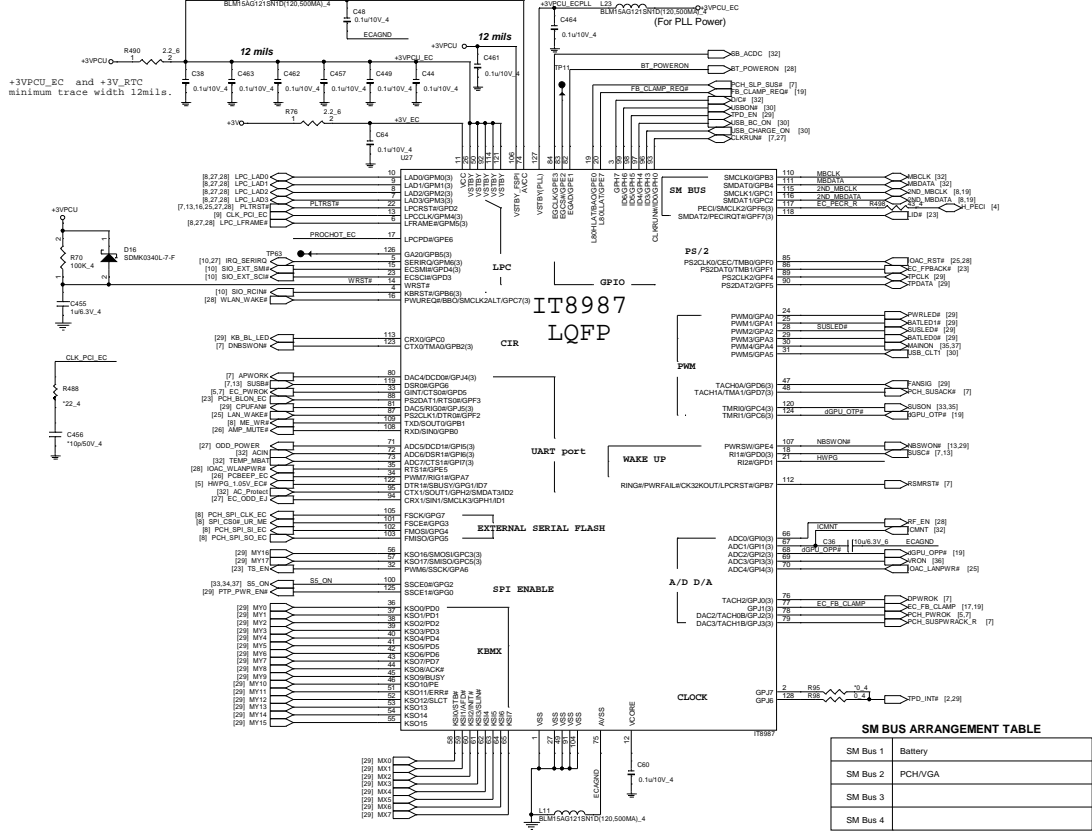
CPU FAN (THM)



POWER LED(UIF)



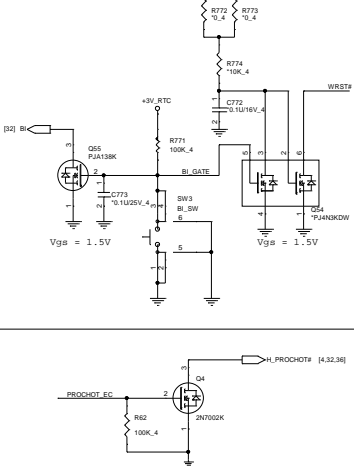
EC(KBC)



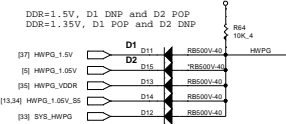
SM BUS PU(KBC)

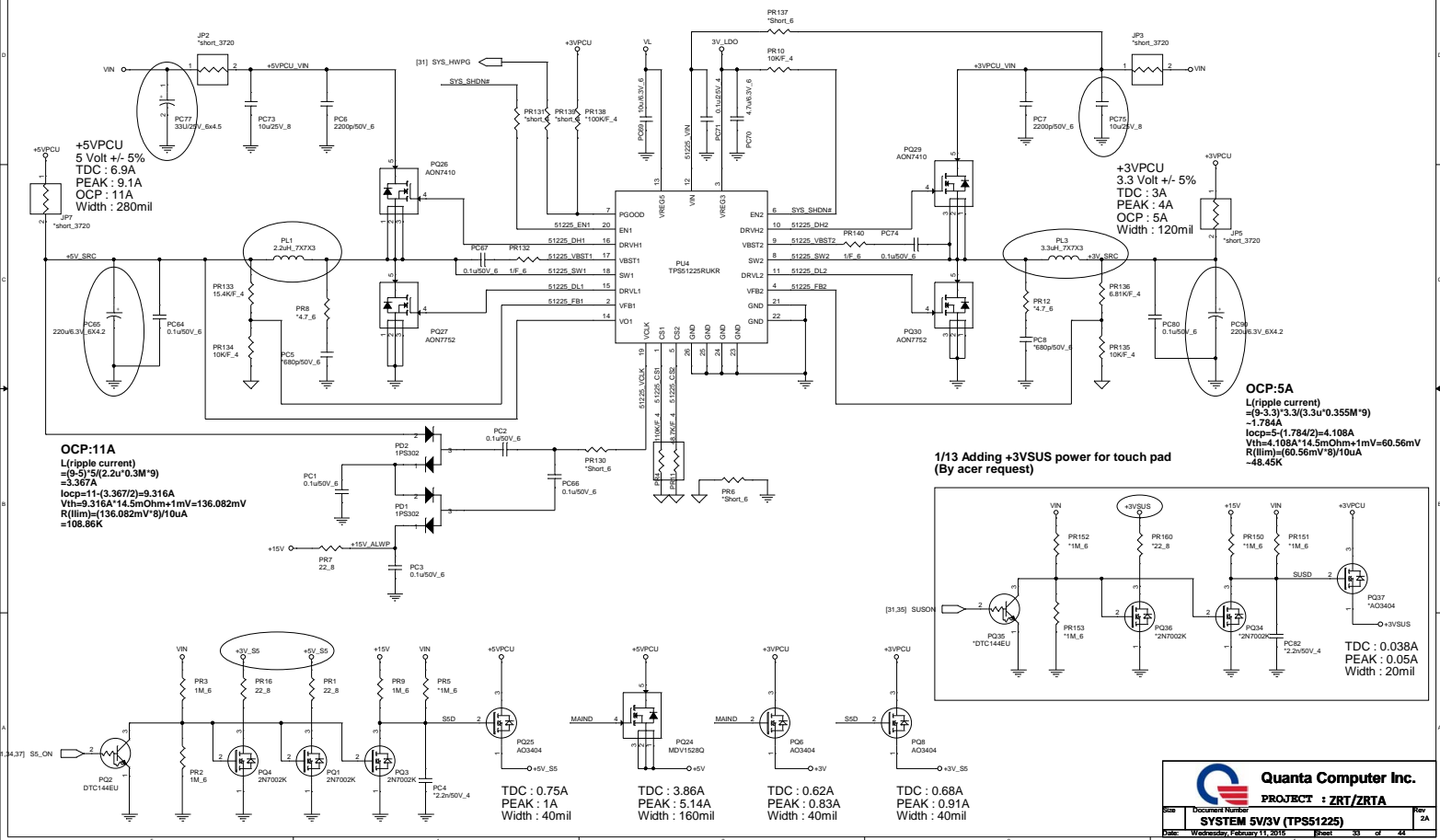


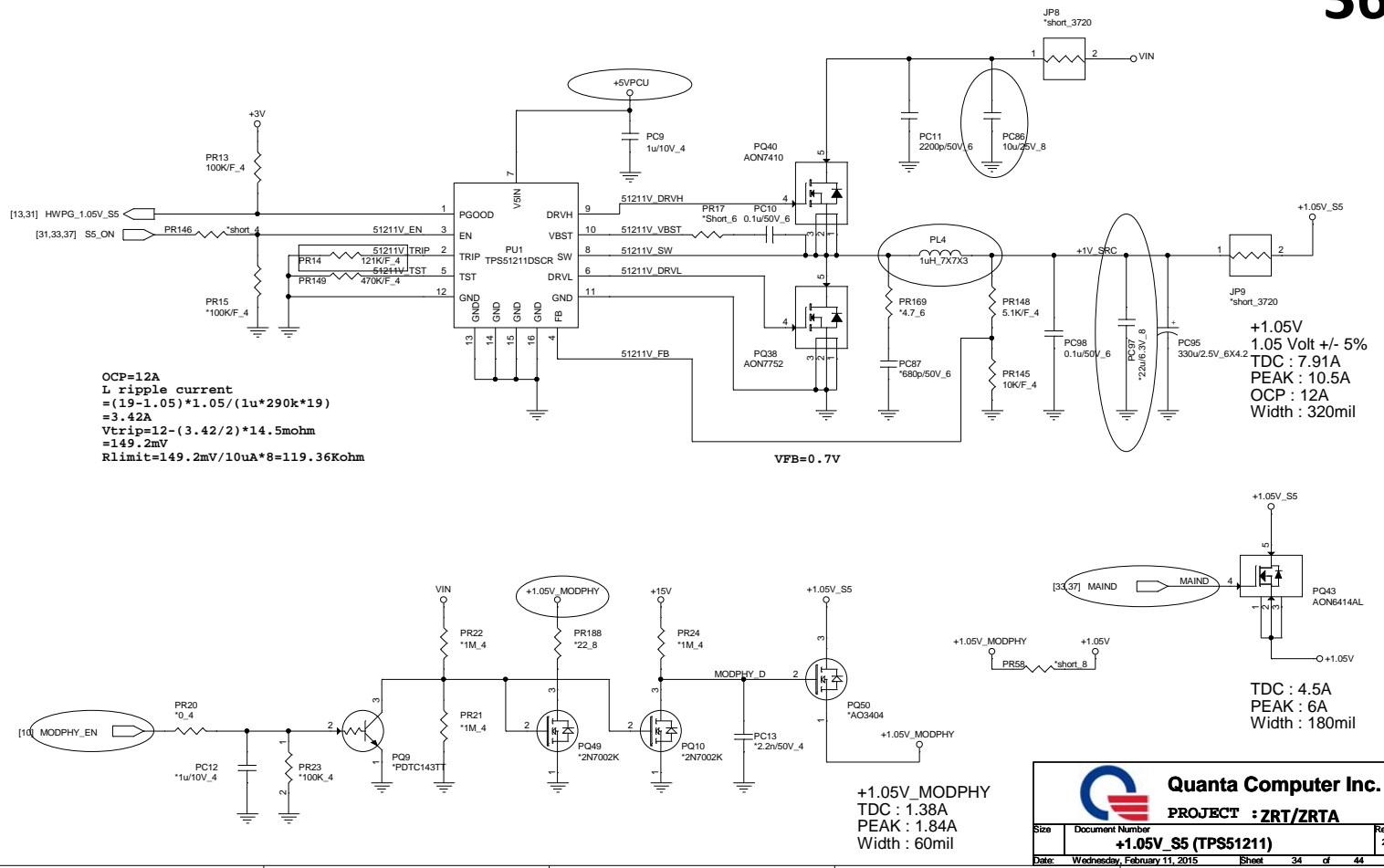
Battery B/I SW

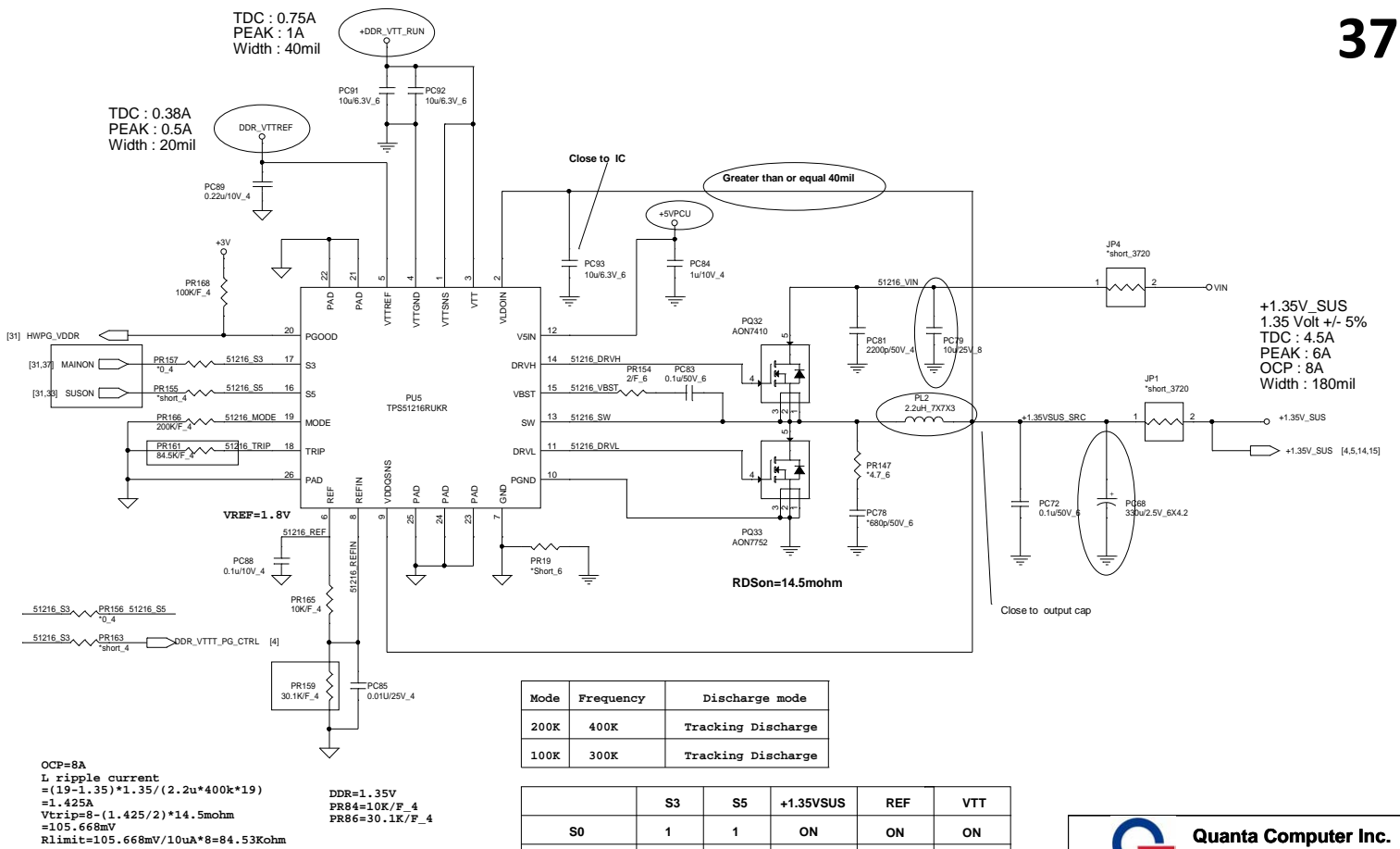


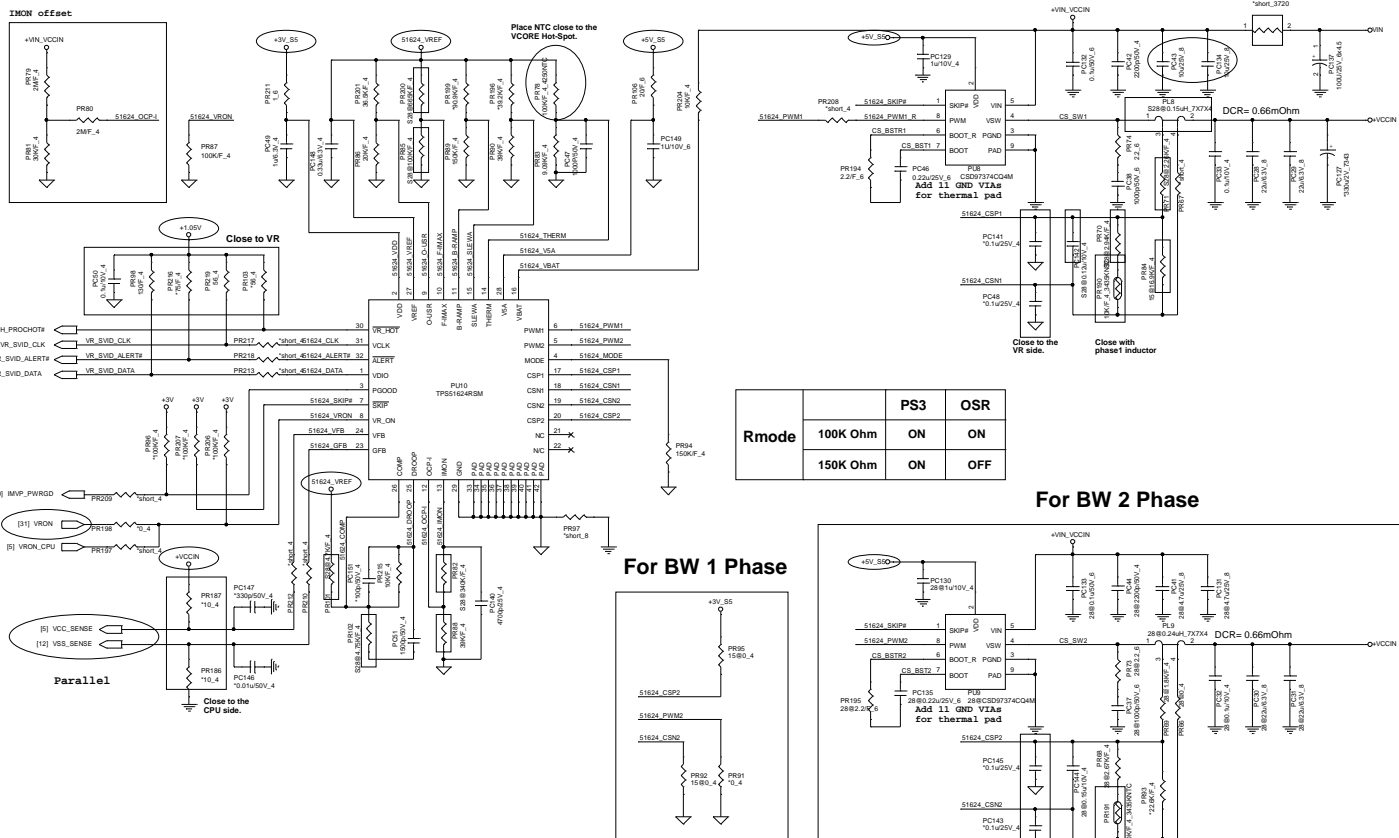
HWP(G(KBC)

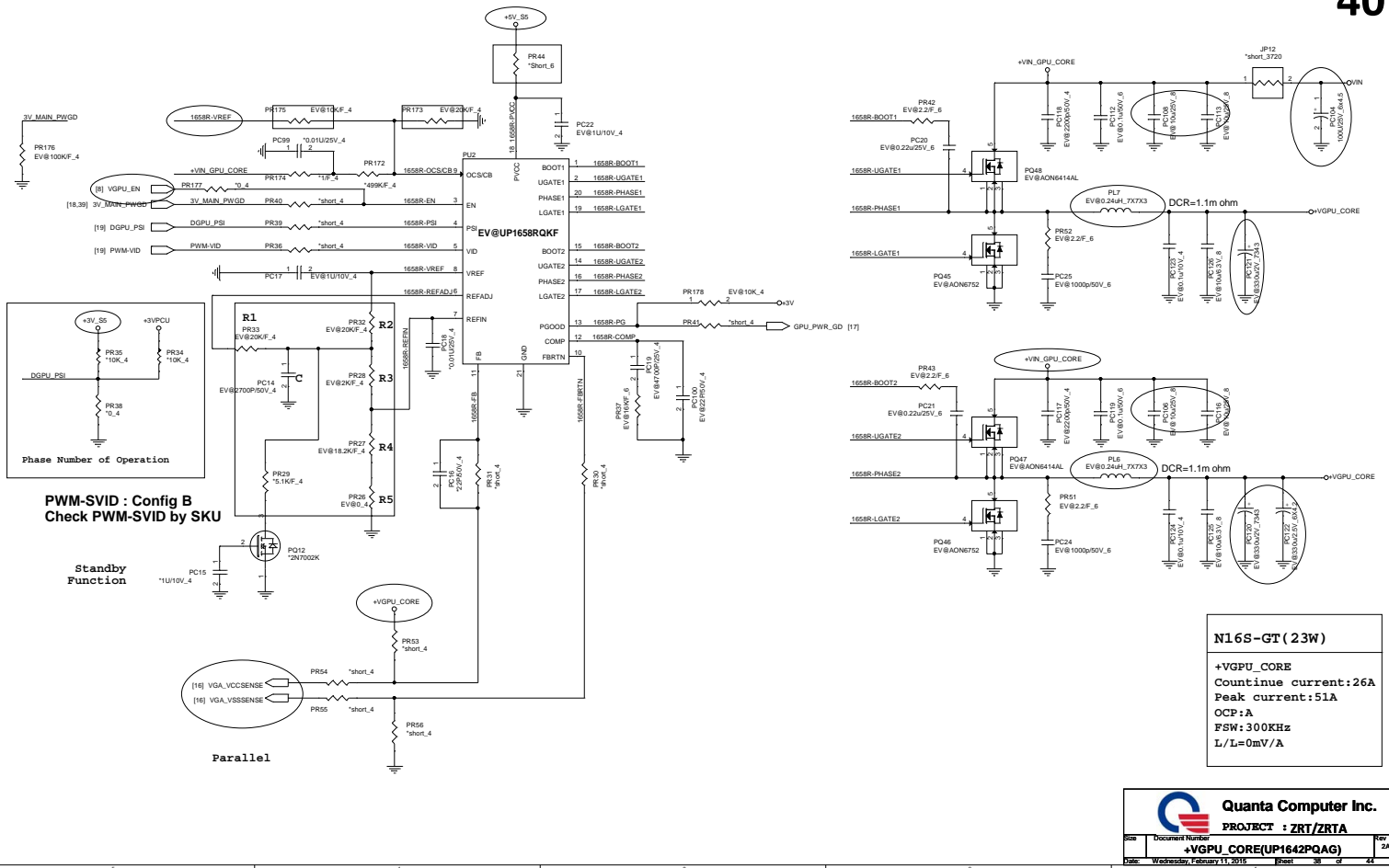




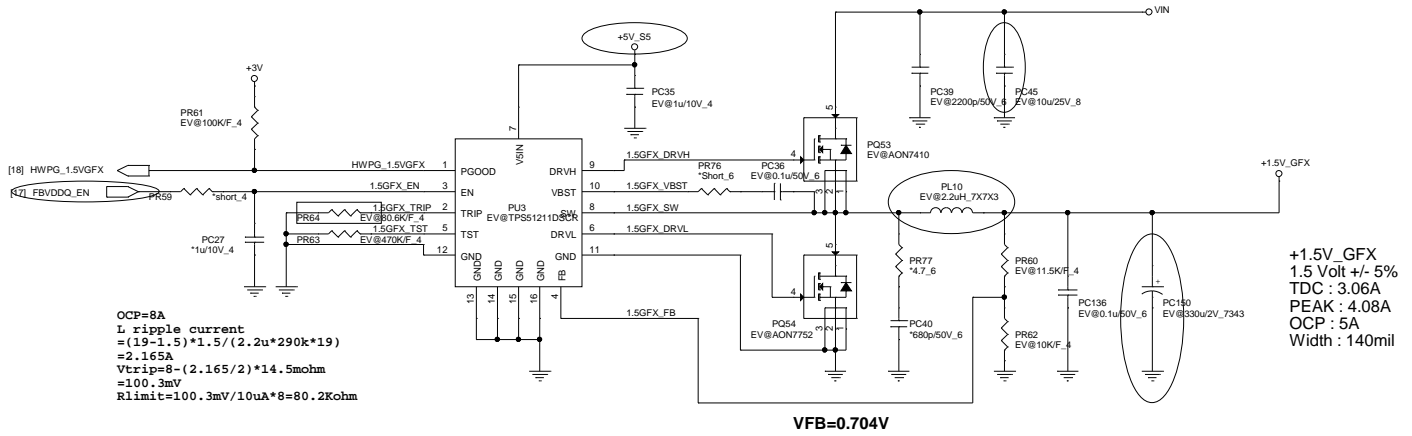
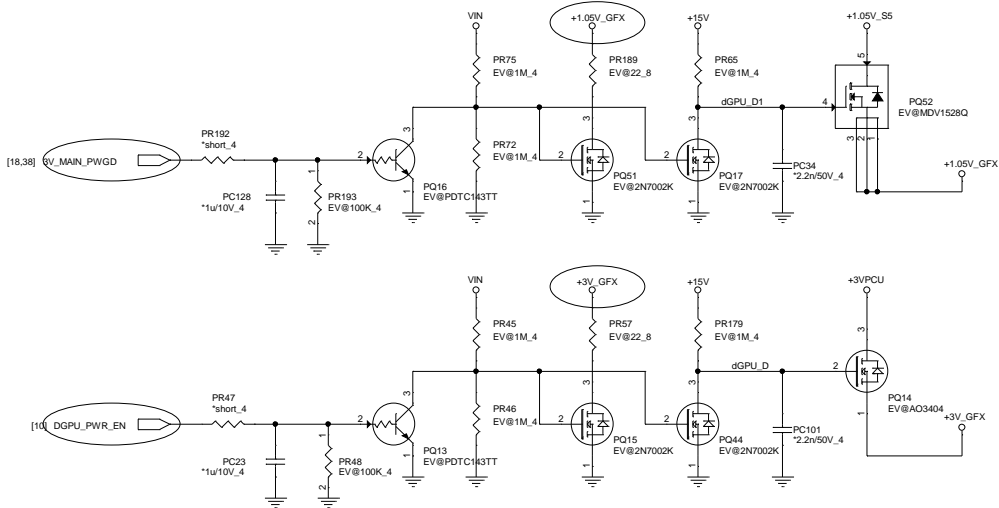




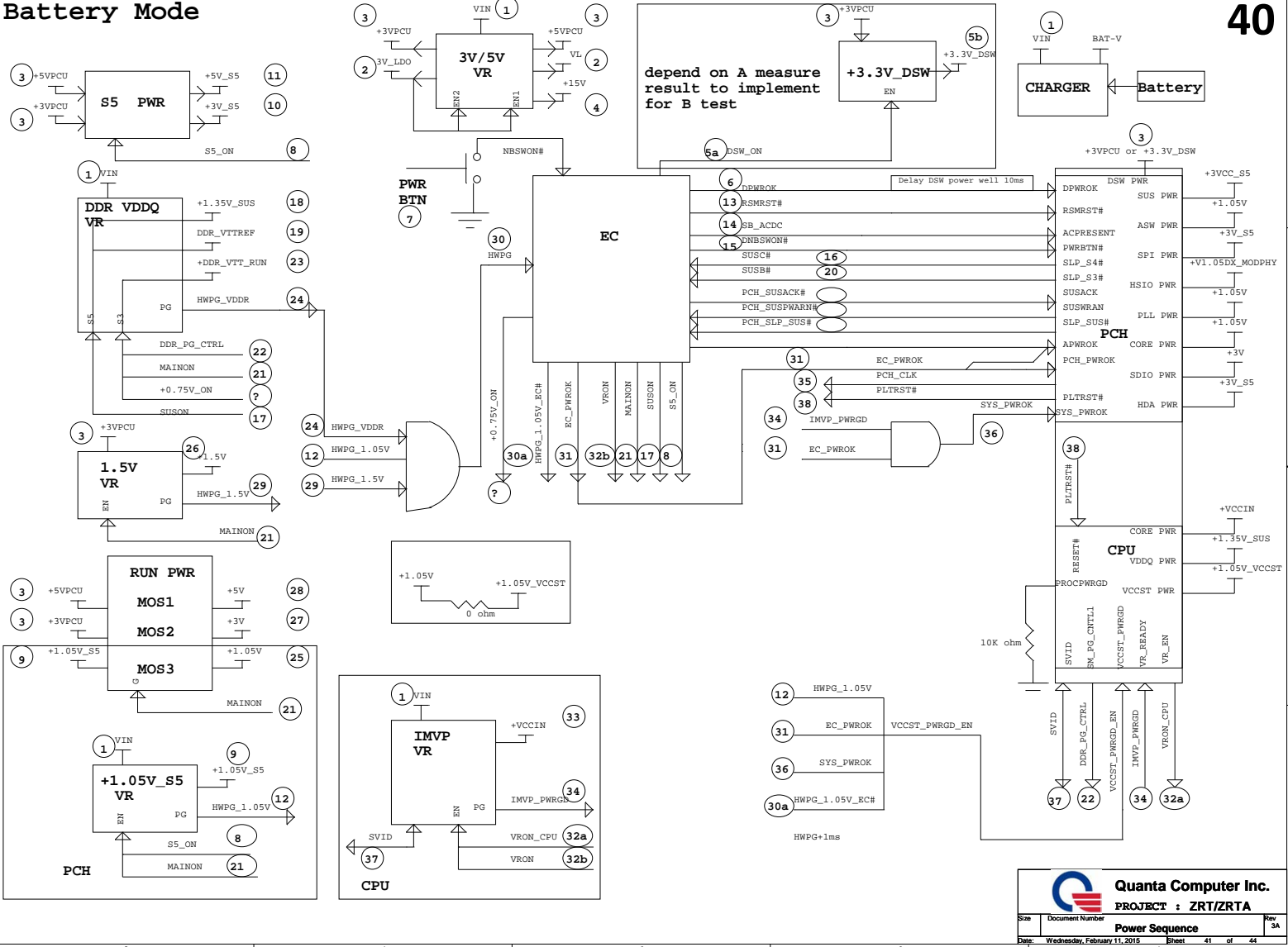


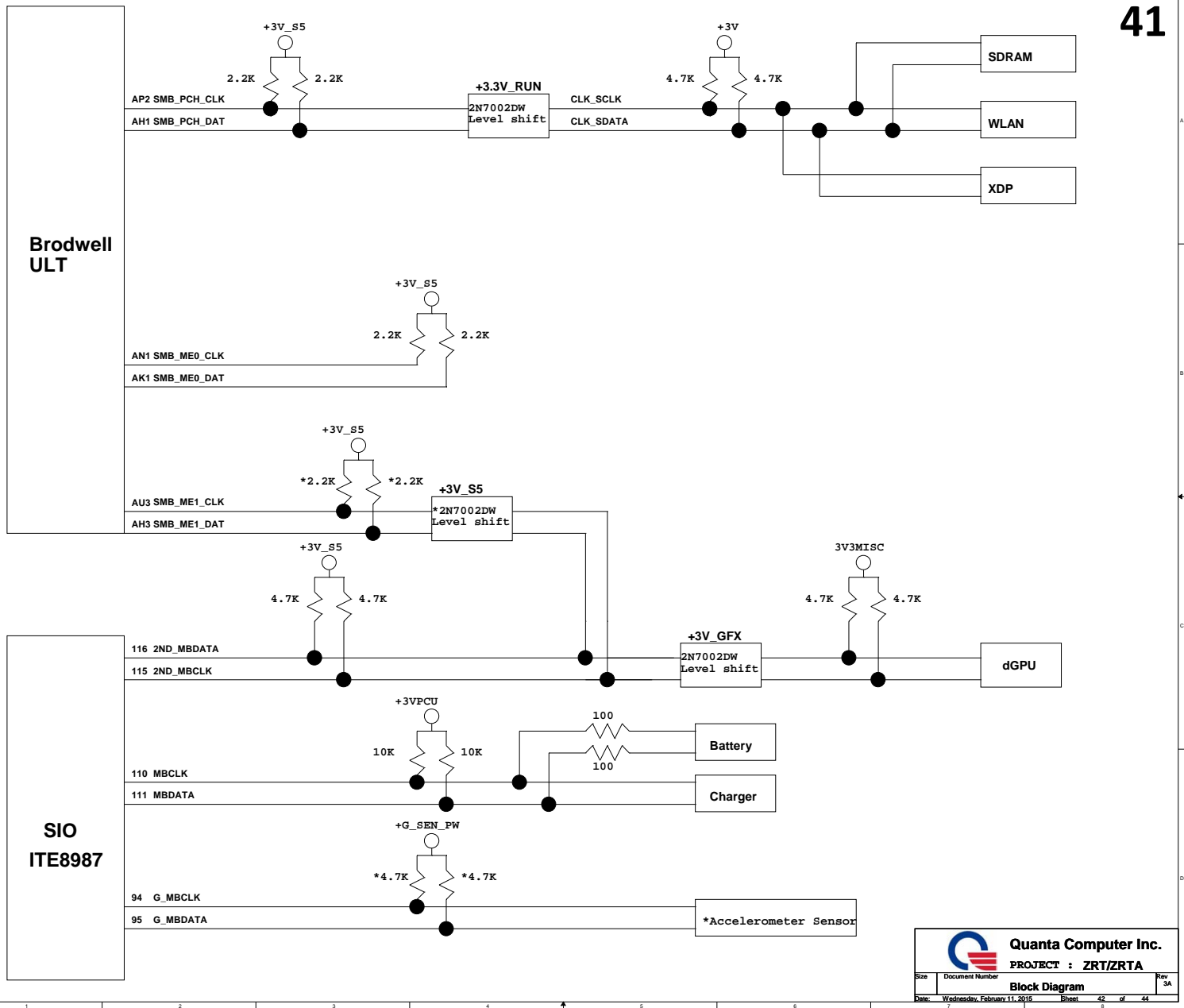


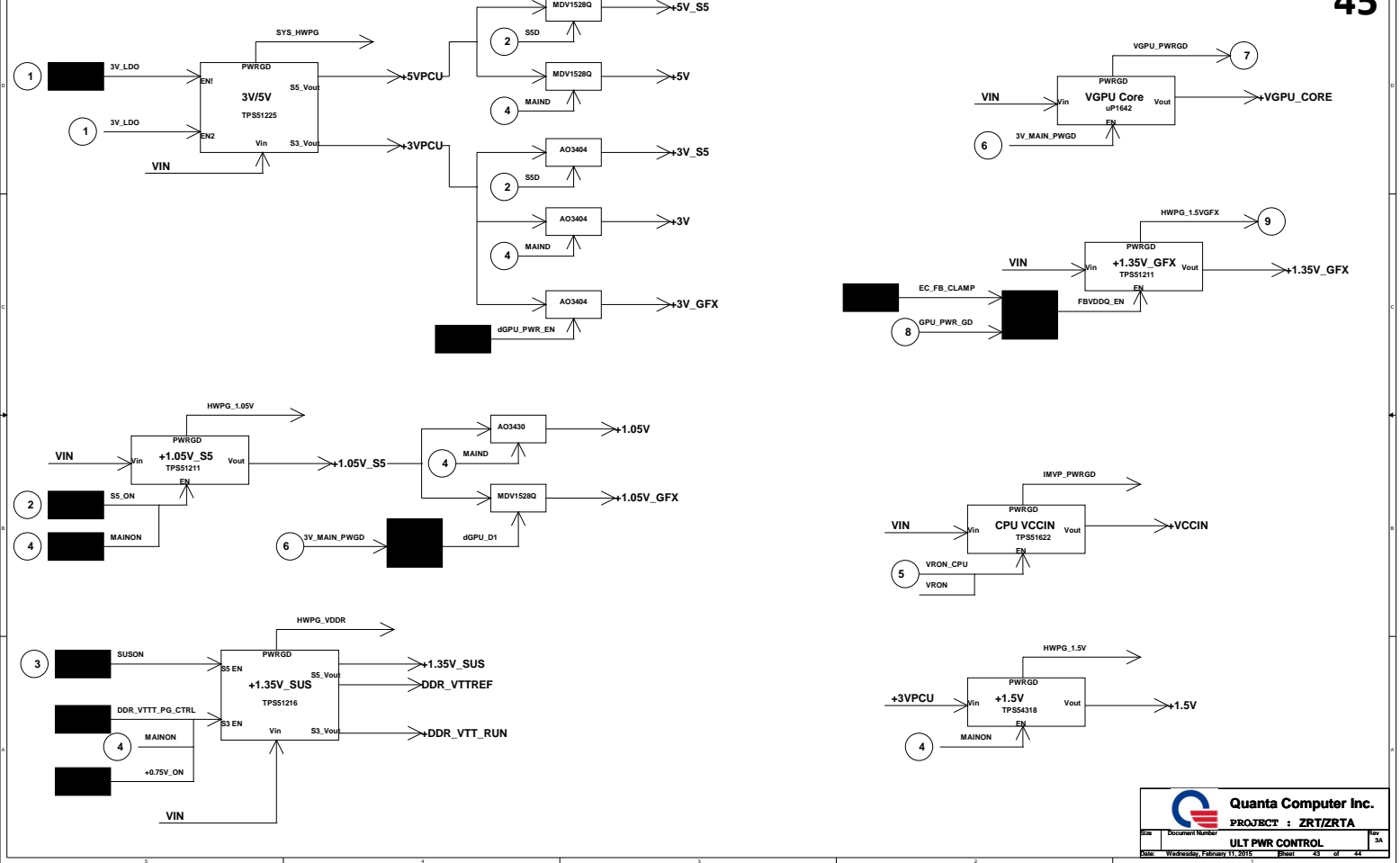
[16,17,18] +1.05V_GFX
[17,20,21,27] +1.5V_GFX
[16,18,19,31] +3V_GFX



Battery Mode







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