

Compal Confidential

Z5WAE Schematics Document

AMD "Beema" Platform

AMD 25W APU With Puma+ Core

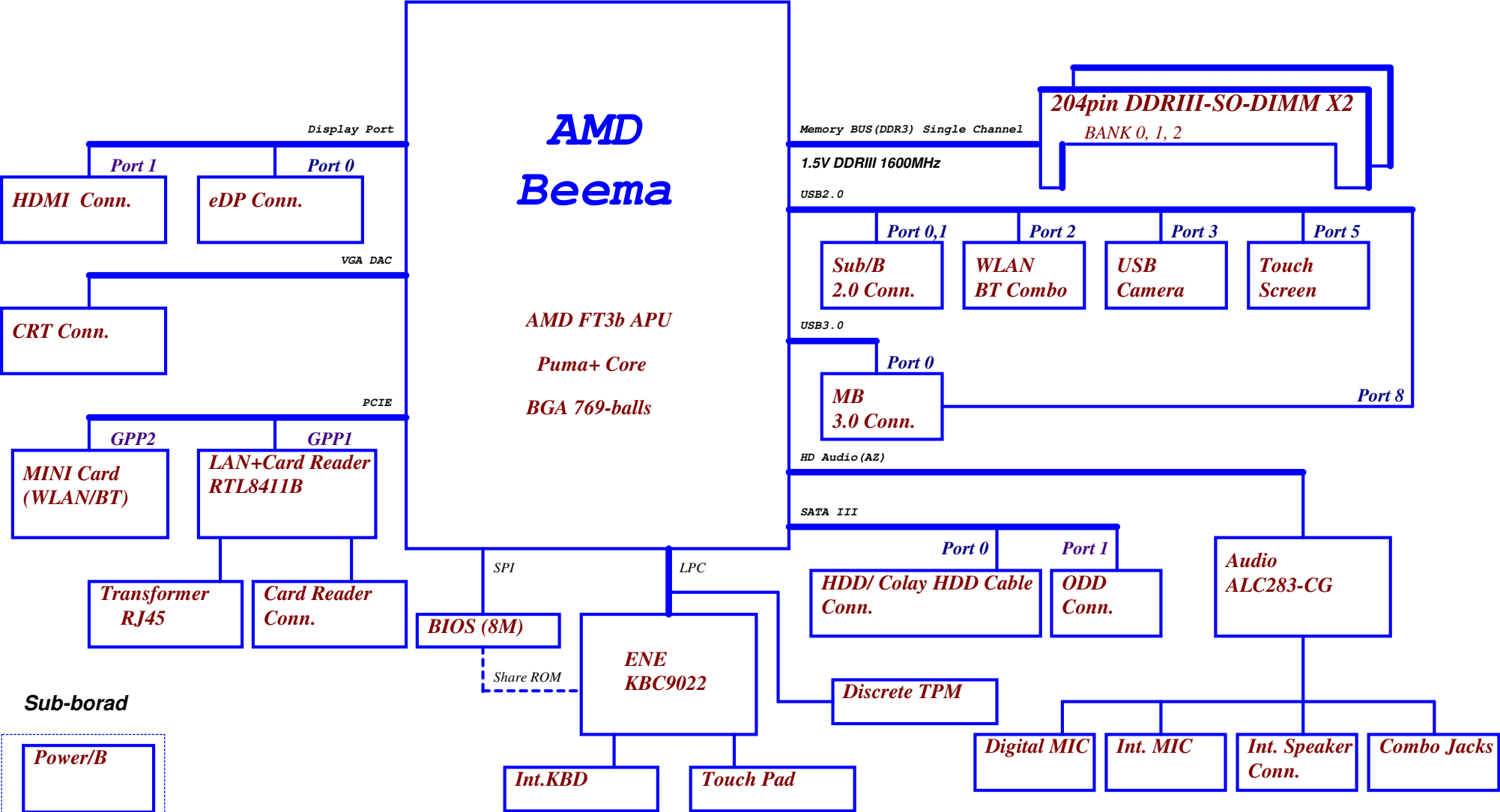
LA-B232P REV: 1.0

2014-03-27

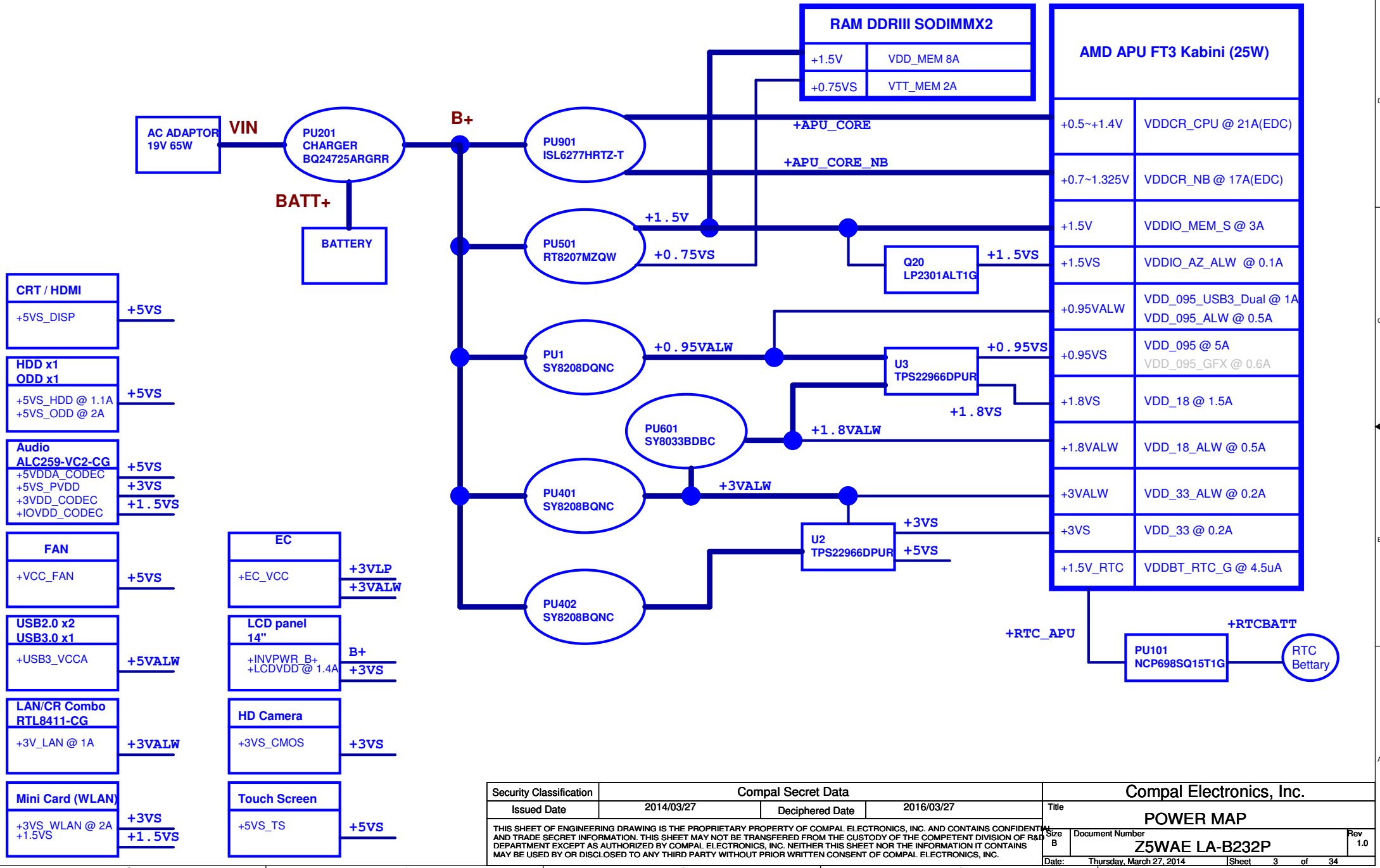
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Model Name : Z5WAE



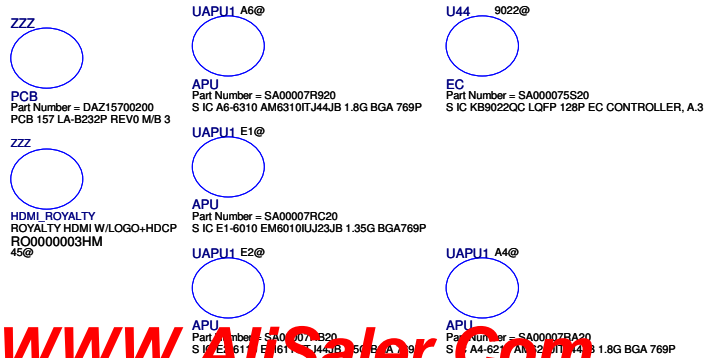
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[illegible]

EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H

APU SMBus Port0 (+3VS)			APU SMBus Port1(+3VALW)		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H			
DDR DIMM2	1010 001Xb	A2H			



Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF

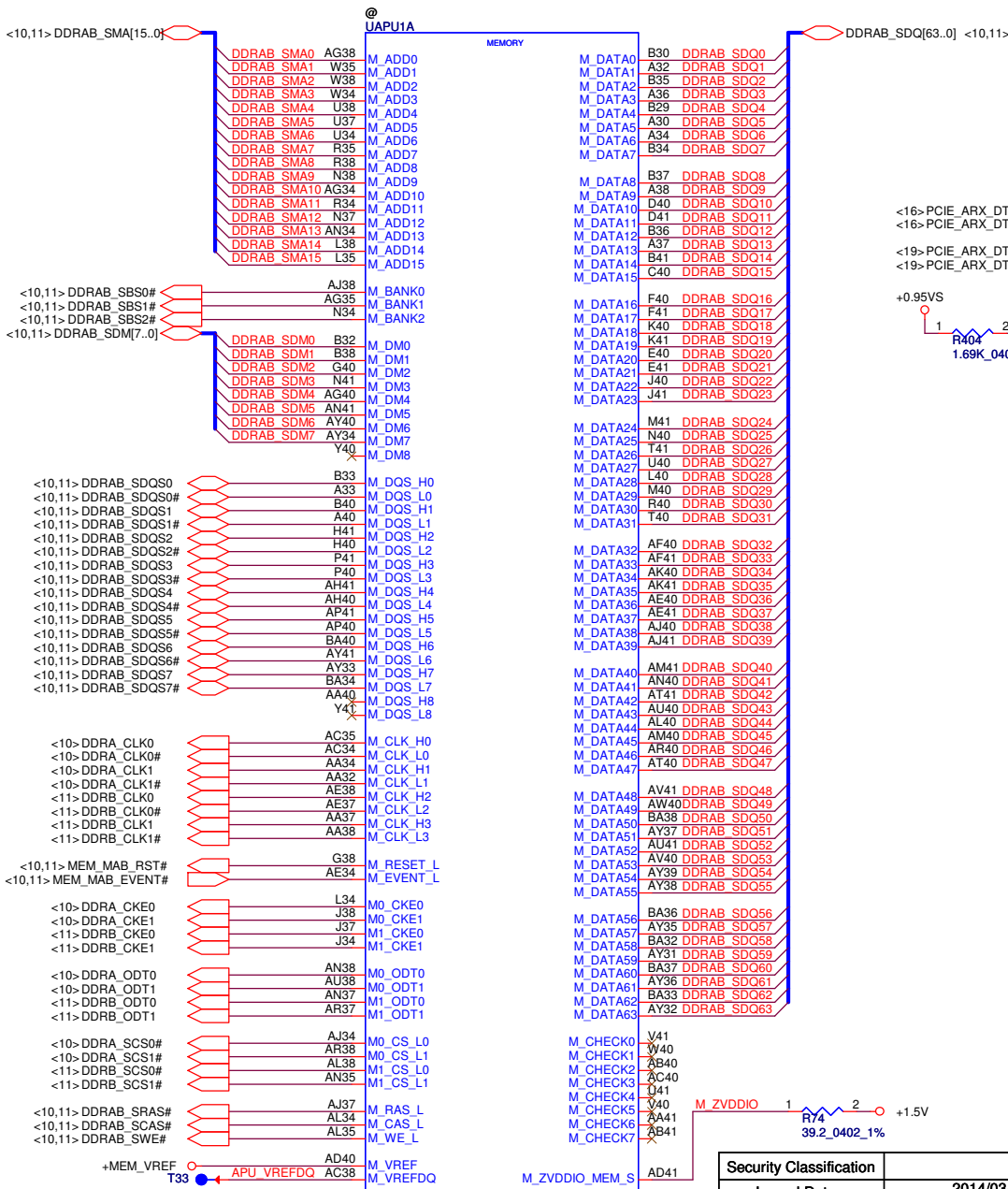
Board ID	PCB Revision
0	EVT
1	DVT
2	PVT
3	Pre-MP
4	
5	
6	
7	

[illegible]

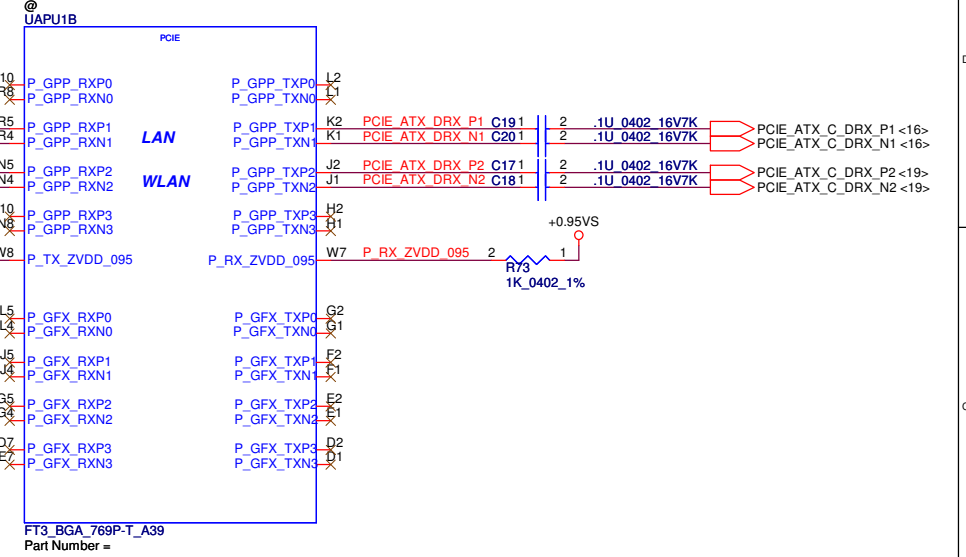
<i>STATE</i> \ <i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>Full ON</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S1 (Power On Suspend)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>LOW</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

The diagram illustrates the power-up sequence for the ADXL345. The signals are: **G-A** (+RTC), **EC_ON**, **G-B** (+3VALW/+5VALW), +1.8VALW, +0.95VALW, **SYSON**, **G-C** (+1.5V), **SUSP#**, **G-D** (+3VS), +1.8VS, +1.5VS, +0.95VS, **VR_ON**, **G-E** (+APU_CORE), and +APU_CORE_NB. The timing sequence is as follows: 1. +RTC is high. 2. EC_ON is high. 3. +3VALW/+5VALW is high. 4. +1.8VALW is high. 5. +0.95VALW is high. 6. SYSON is high. 7. +1.5V is high. 8. SUSP# is high. 9. +3VS is high. 10. +1.8VS is high. 11. +1.5VS is high. 12. +0.95VS is high. 13. VR_ON is high. 14. +APU_CORE is high. 15. +APU_CORE_NB is high. 16. CS is high.

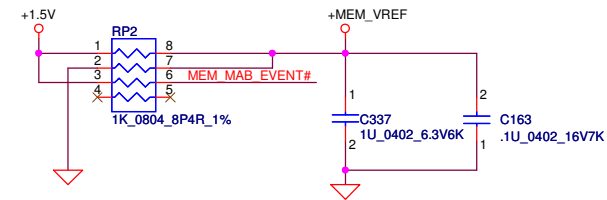
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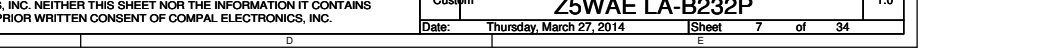
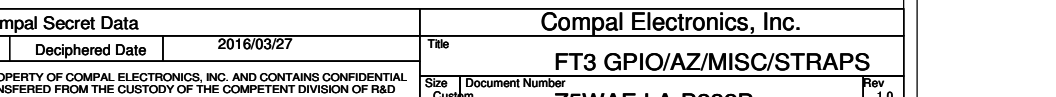
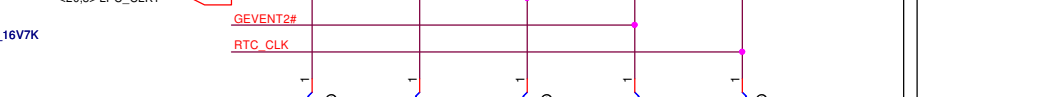
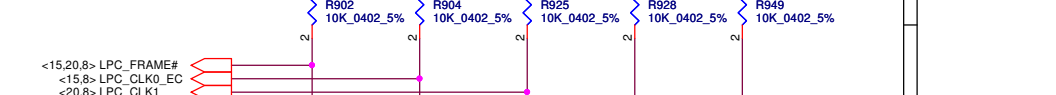
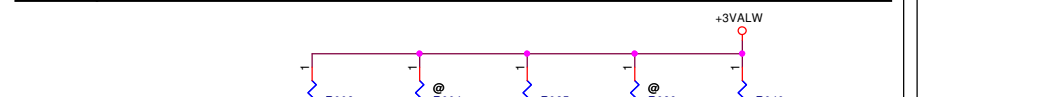
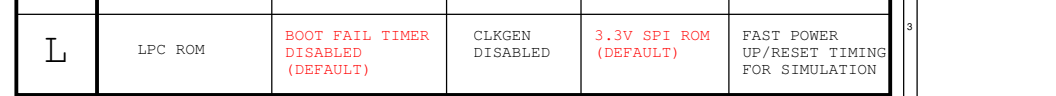
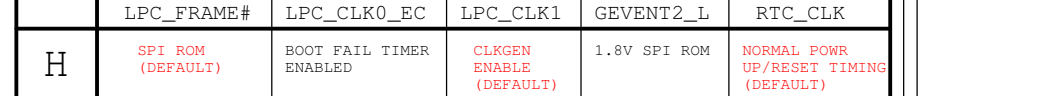
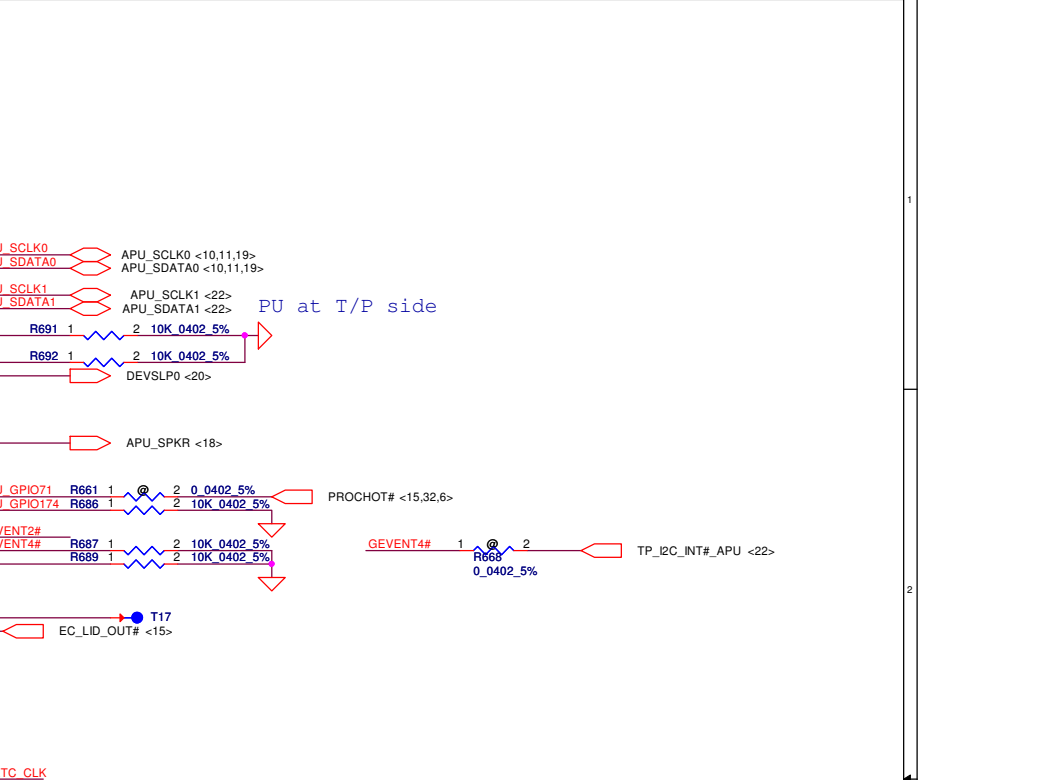
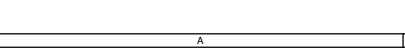
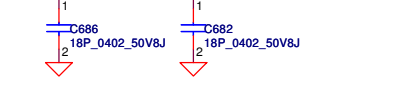
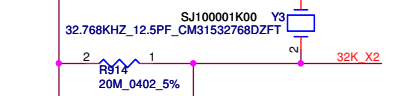
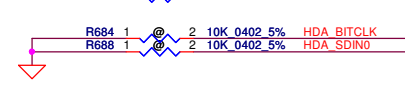
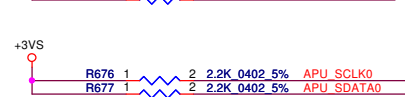
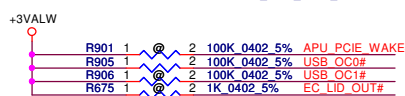
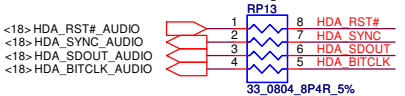
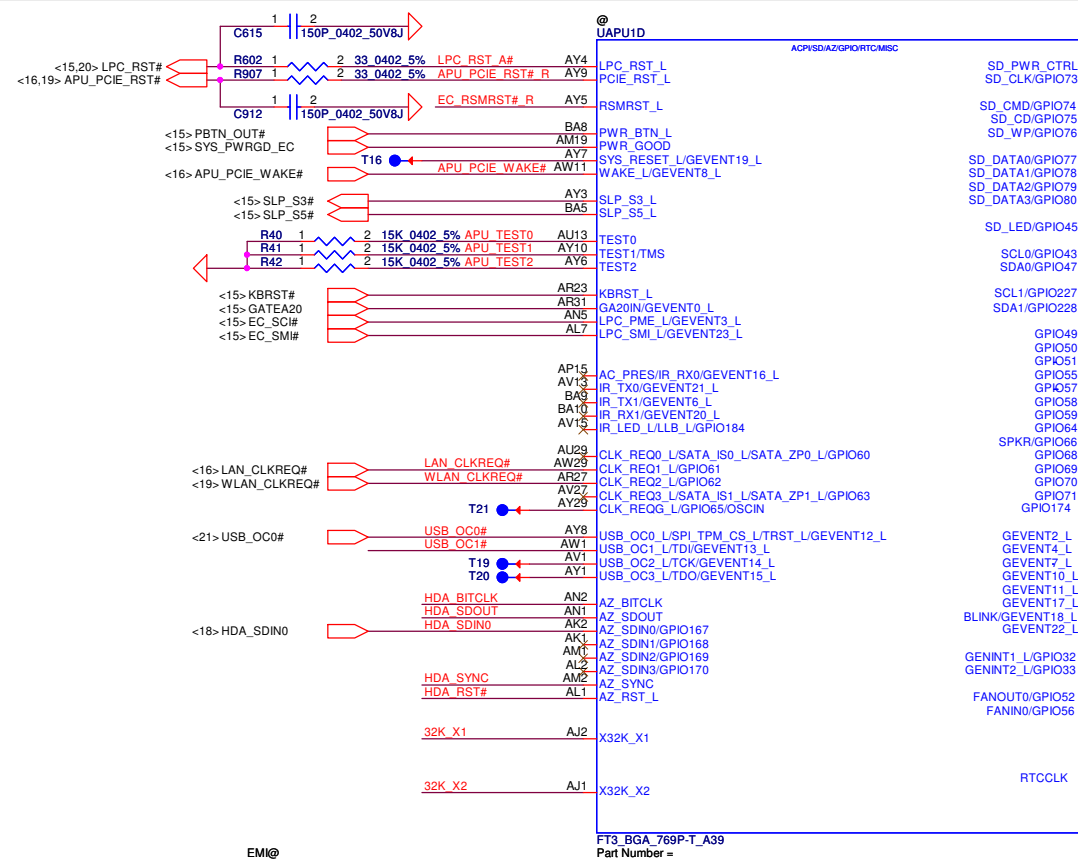
DDRAB_SDQ[63..0] <10,11>



MEMORY VREF



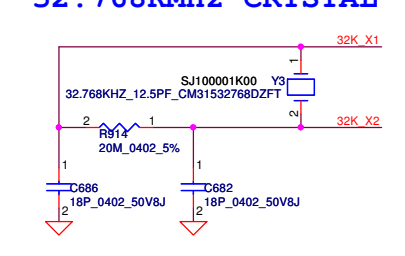
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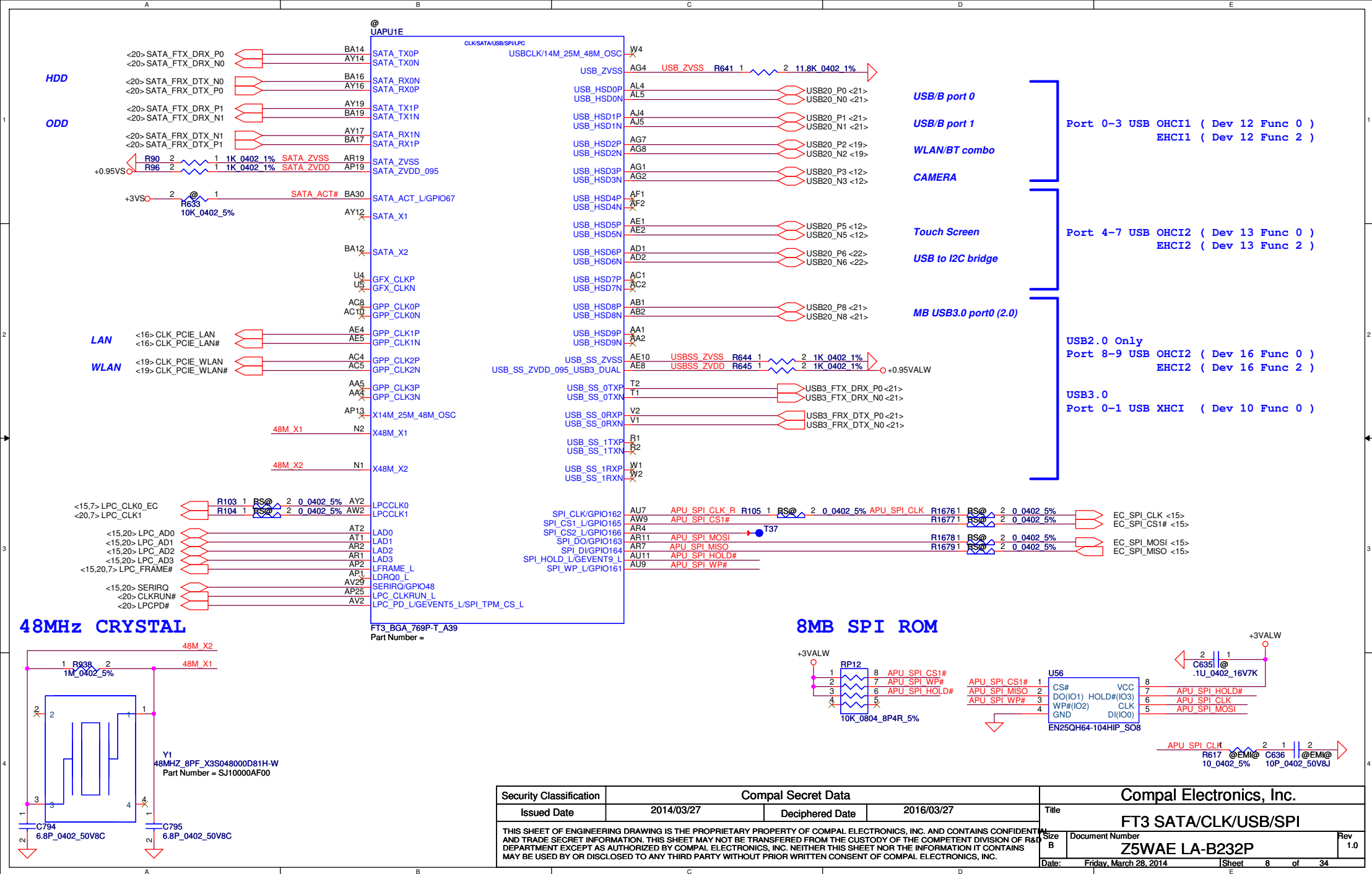
STRAPS OF APU

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	GEVENT2_L	RTC_CLK
H	SPI ROM (DEFAULT)	BOOT FAIL TIMER ENABLED	CLKGEN ENABLE (DEFAULT)	1.8V SPI ROM	NORMAL POWER UP/RESET TIMING (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLKGEN DISABLED	3.3V SPI ROM (DEFAULT)	FAST POWER UP/RESET TIMING FOR SIMULATION

32.768KMHZ CRYSTAL



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+APU CORE



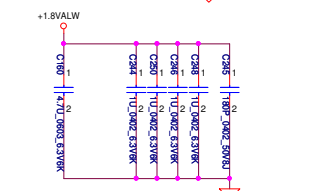
+3VS +3V



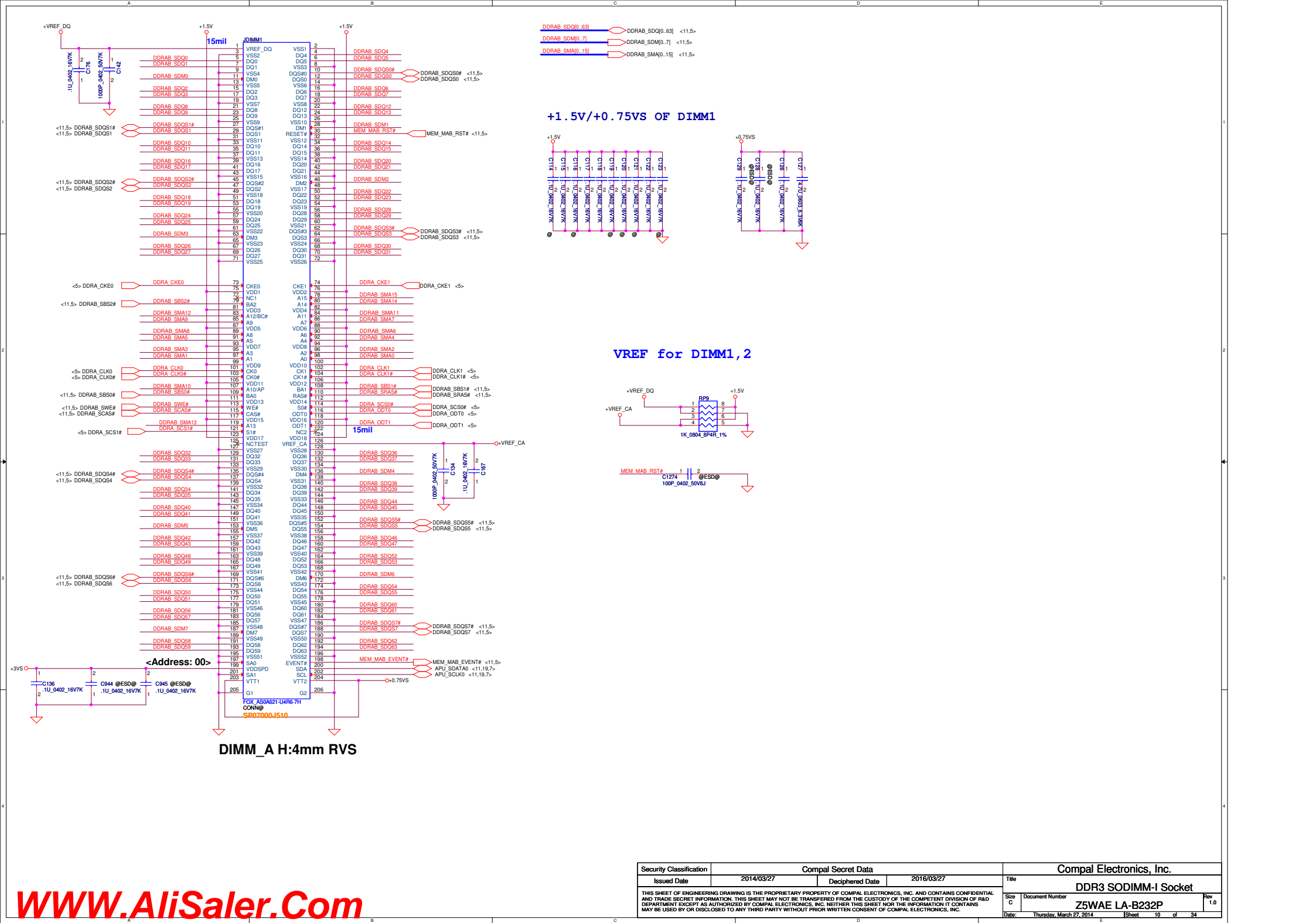
+1.5VS

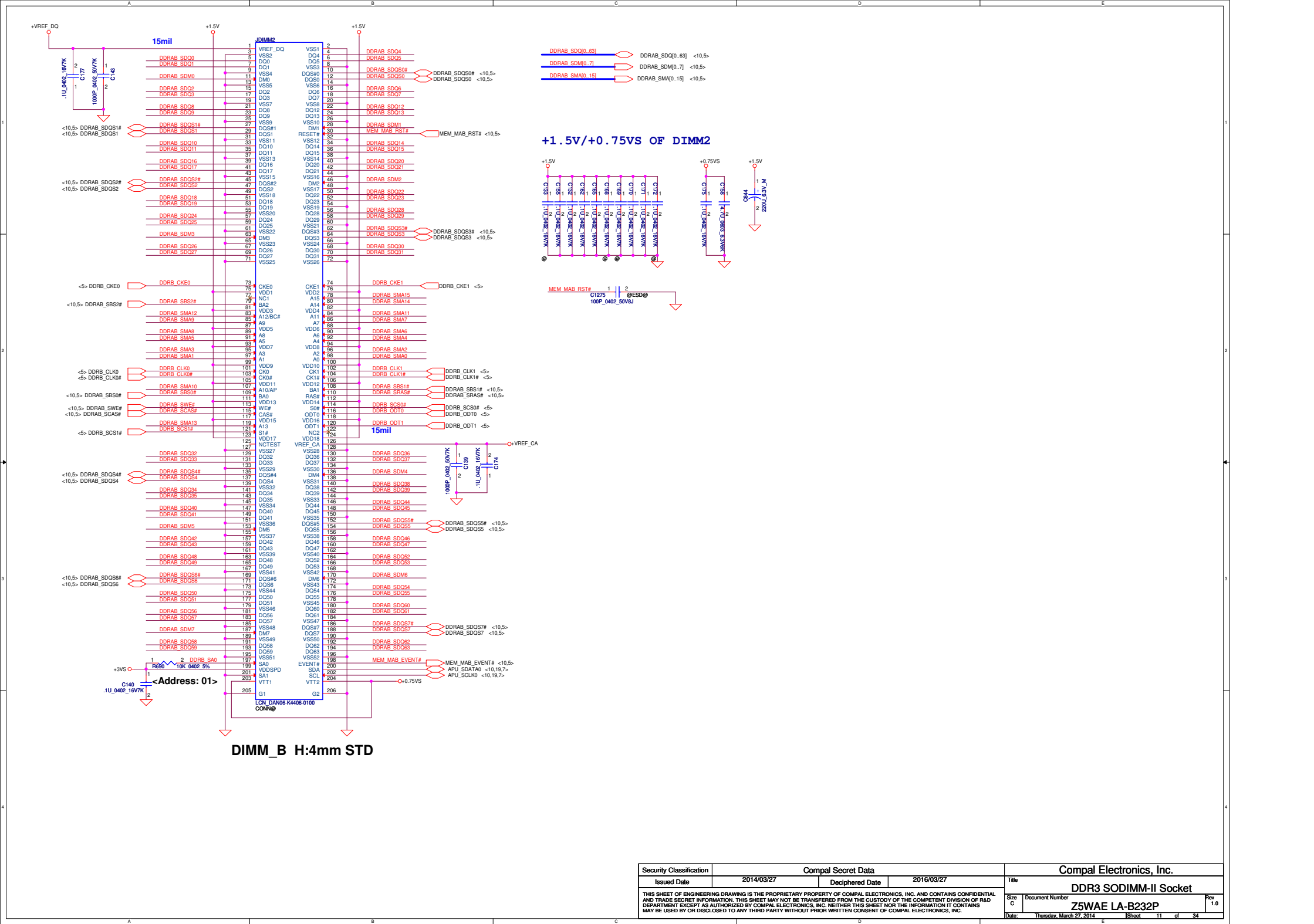


VDD 18

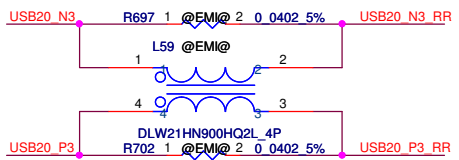
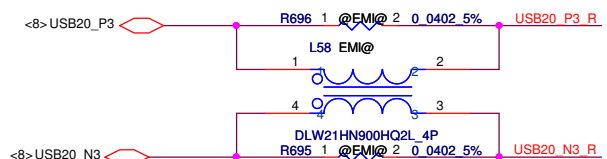
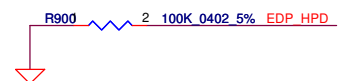
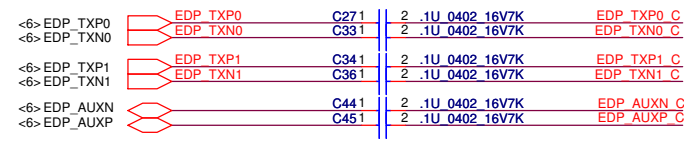
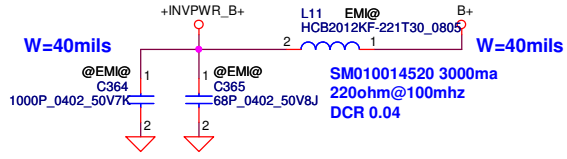
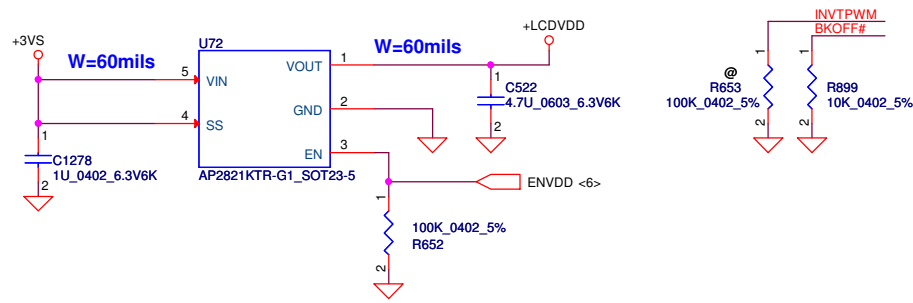


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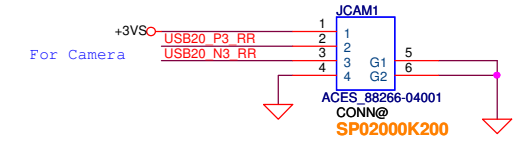
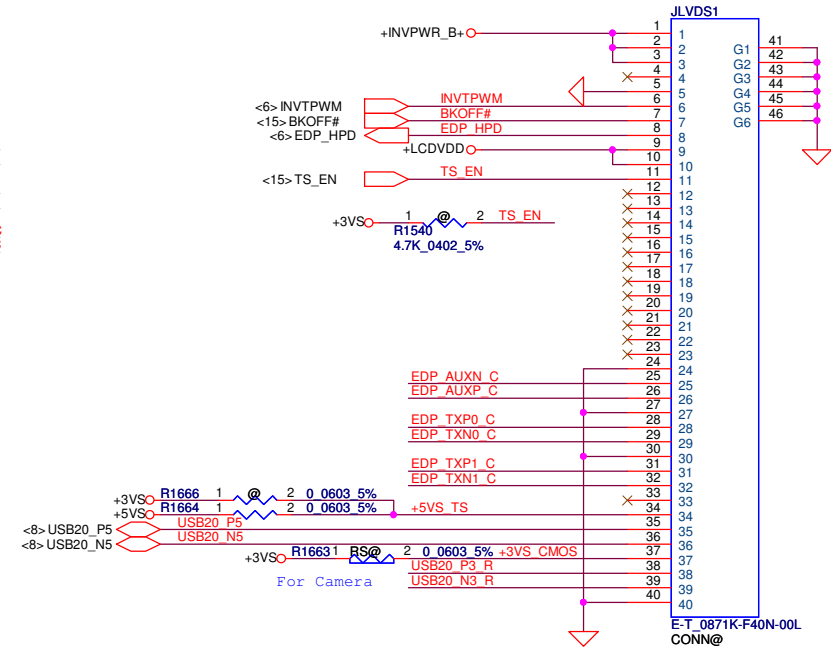




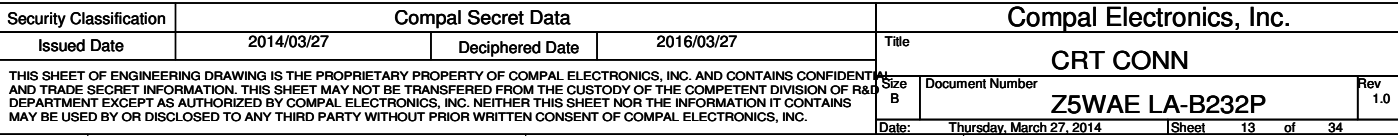
LCD POWER CIRCUIT

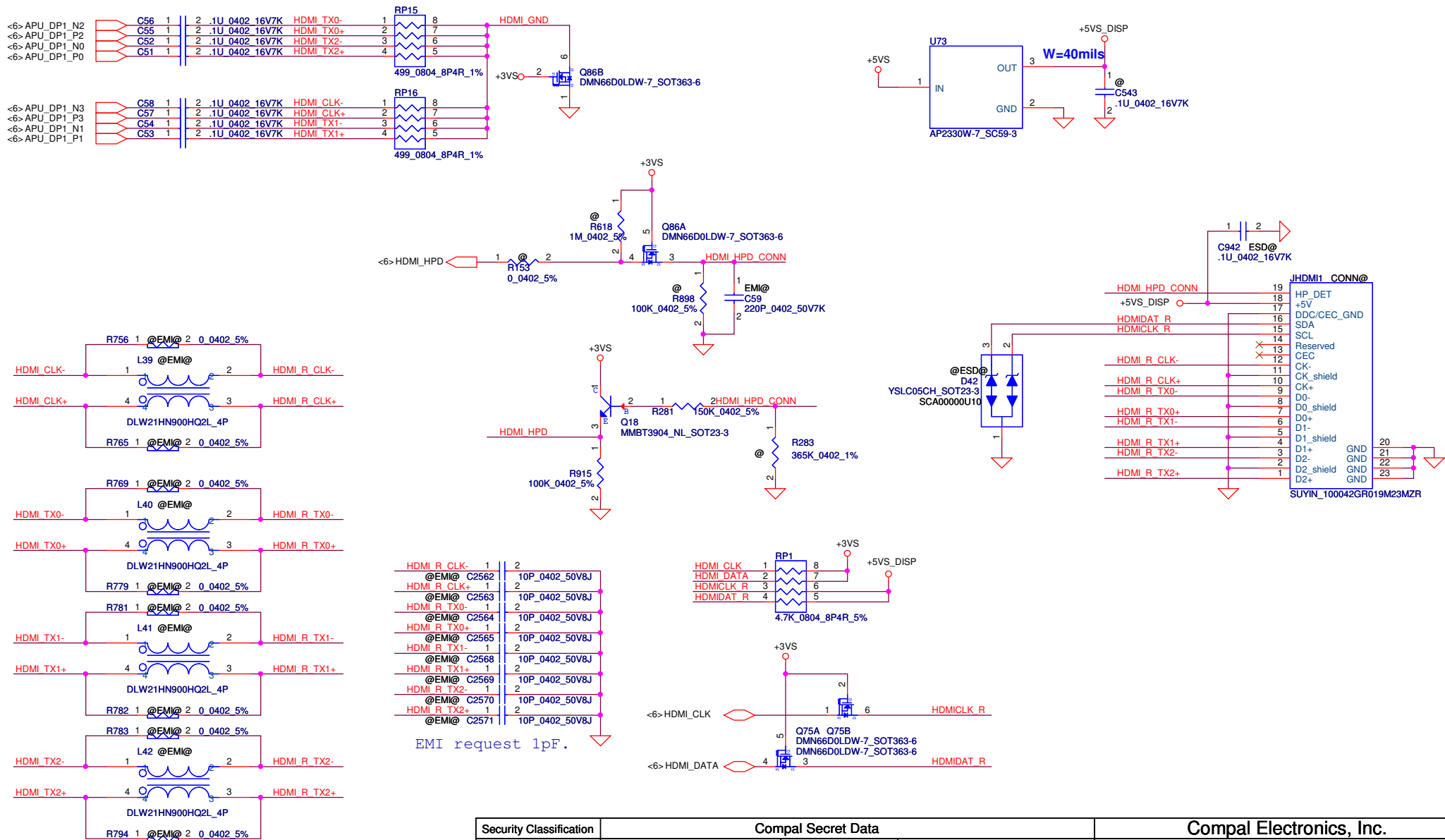


eDP PANEL Conn.

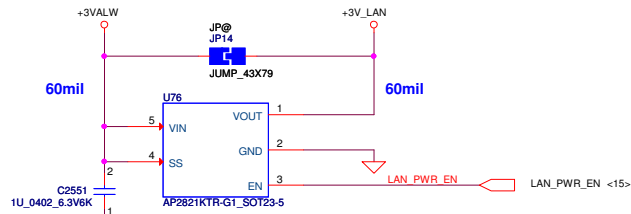


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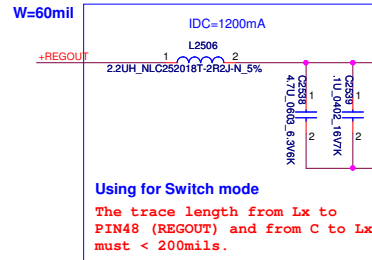
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From EC

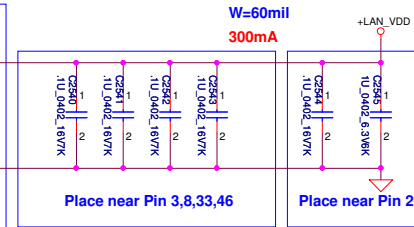
High active.
EN threshold voltage min:1.2V typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

+3V_LAN Rising time must >0.5ms and <100ms



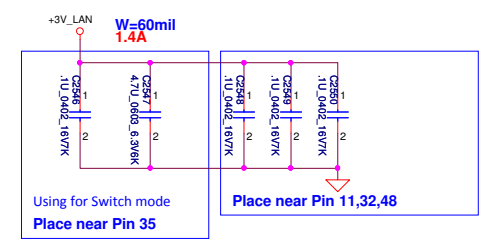
Using for Switch mode

The trace length from Lx to PIN48 (REGOUT) and from C to Lx must < 200mils.



Place near Pin 3,8,33,46

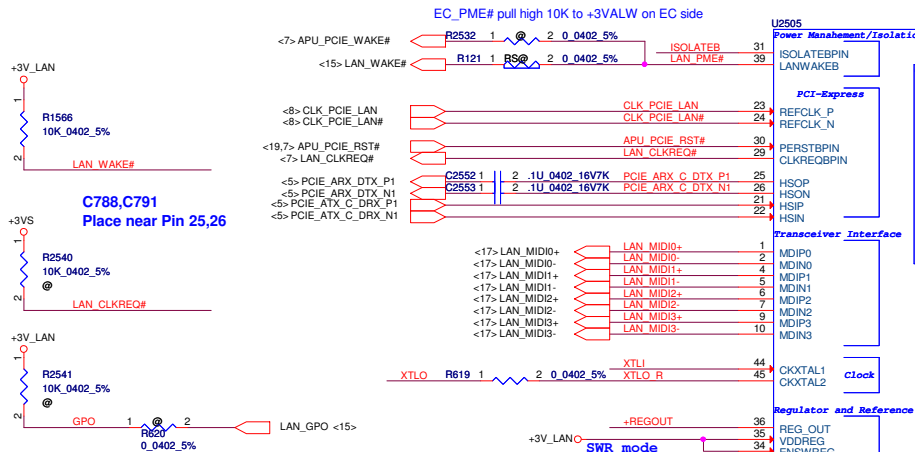
Place near Pin 20



Using for Switch mode

Place near Pin 35

Place near Pin 11,32,48



Power Management/Isolation

ISOLATEBPIN LANWAKEB

ISOLATEBPIN LANWAKEB

ISOLATEBPIN LANWAKEB

ISOLATEBPIN LANWAKEB

ISOLATEBPIN LANWAKEB

ISOLATEBPIN LANWAKEB

ISOLATEBPIN LANWAKEB

ISOLATEBPIN LANWAKEB

ISOLATEBPIN LANWAKEB

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ISOLATEBPIN LANWAKEB

SD_D0MS_D1

SD_D1

SD_CLKMS_D0

SD_CMD/MS_D2

SD_D3MS_D3

SD_D2MS_CLK

MS_BS/SD_WP#

SD_CD#

MS_CD#

SD_CD#

SD_CD#

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SD_CD#

SD_D0MS_D1

SD_D1

SD_CLKMS_D0

SD_CMD/MS_D2

SD_D3MS_D3

SD_D2MS_CLK

MS_BS/SD_WP#

SD_CD#

MS_CD#

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SD_CD#

SD_D0MS_D1

SD_D1

SD_CLKMS_D0

SD_CMD/MS_D2

SD_D3MS_D3

SD_D2MS_CLK

MS_BS/SD_WP#

SD_CD#

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SD_D0MS_D1

SD_D1

SD_CLKMS_D0

SD_CMD/MS_D2

SD_D3MS_D3

SD_D2MS_CLK

MS_BS/SD_WP#

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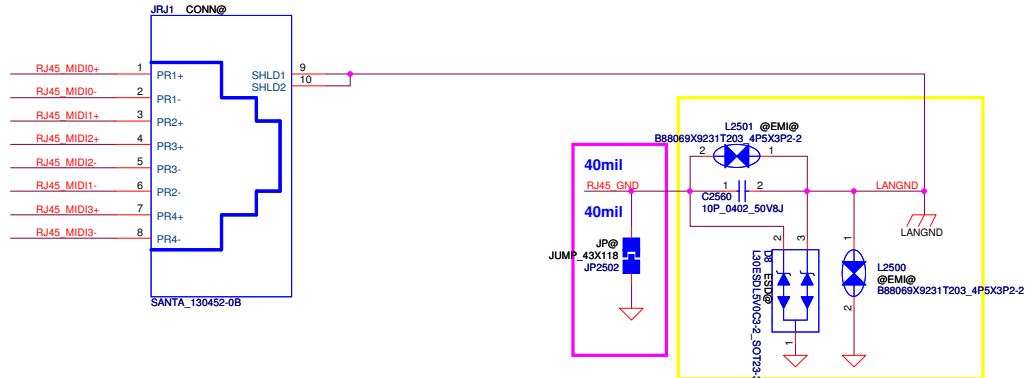
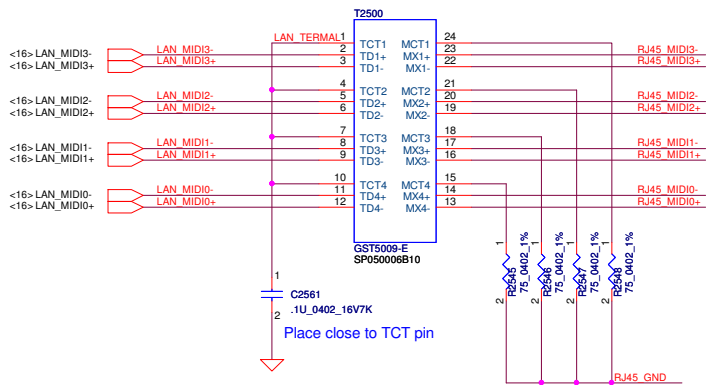
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SD_CD#

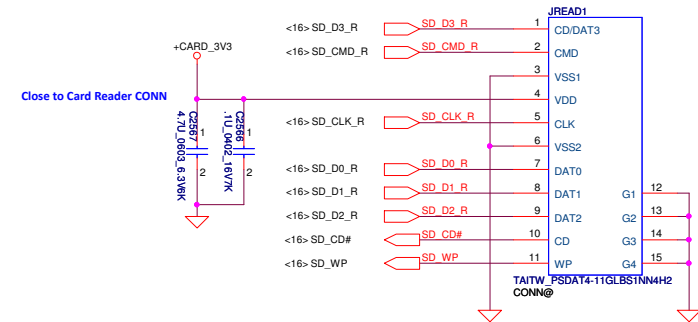
SD_D0MS_D1

SD_D1

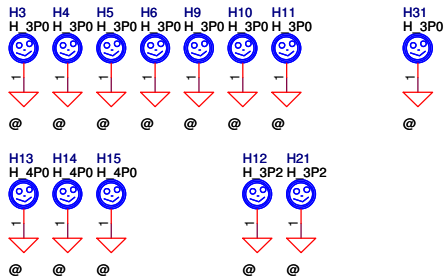
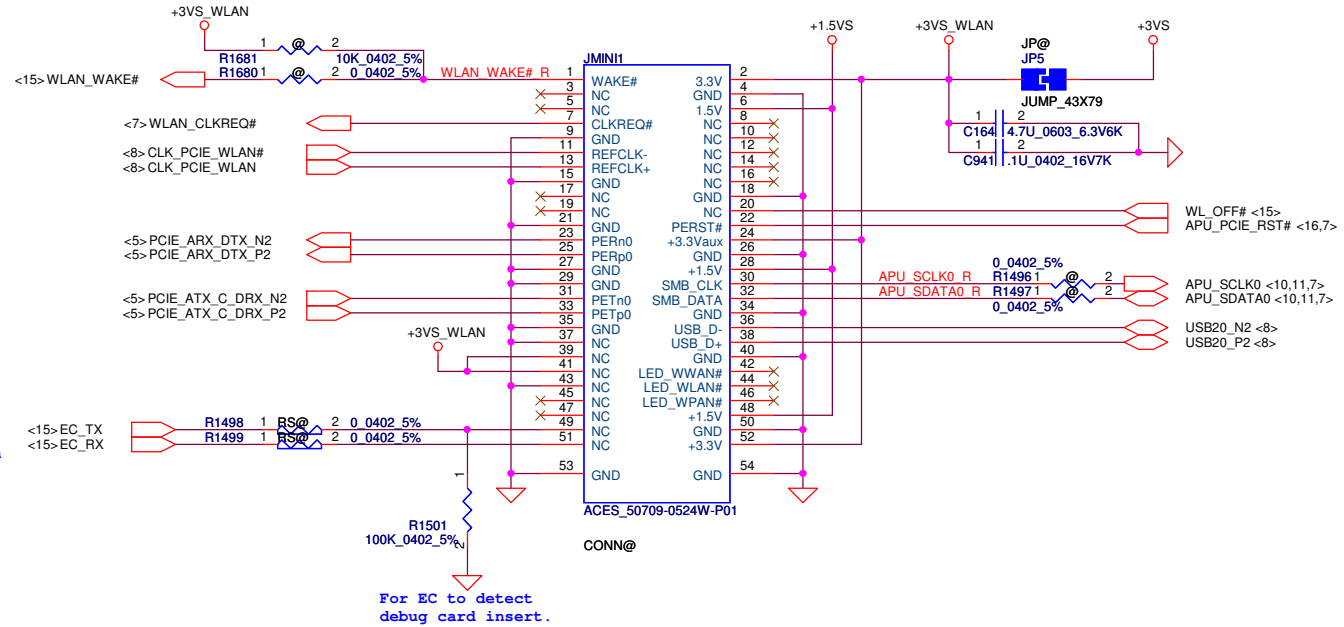
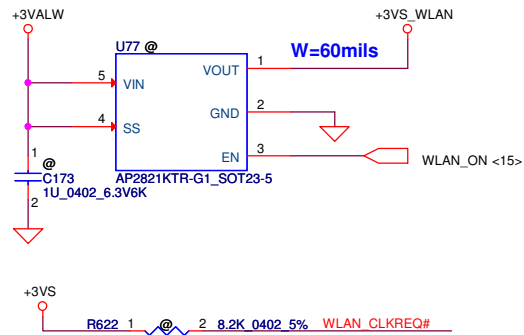
LAN Connector



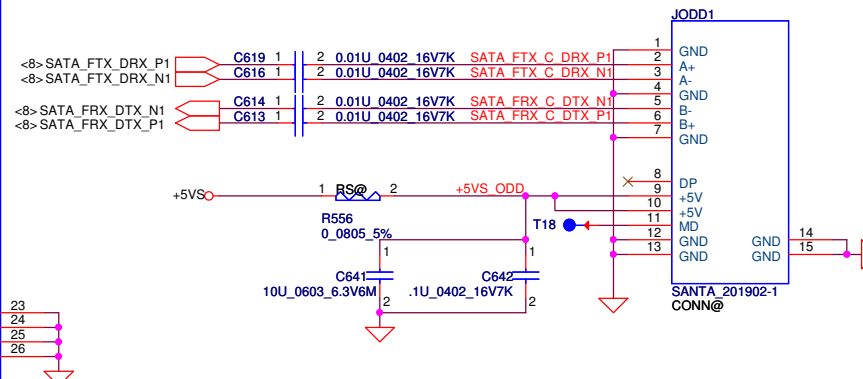
Card Reader Connector



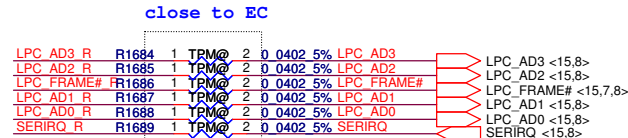
Mini-Express Card(WLAN/WiMAX) H=4mm



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SATA ODD Conn.

TPM



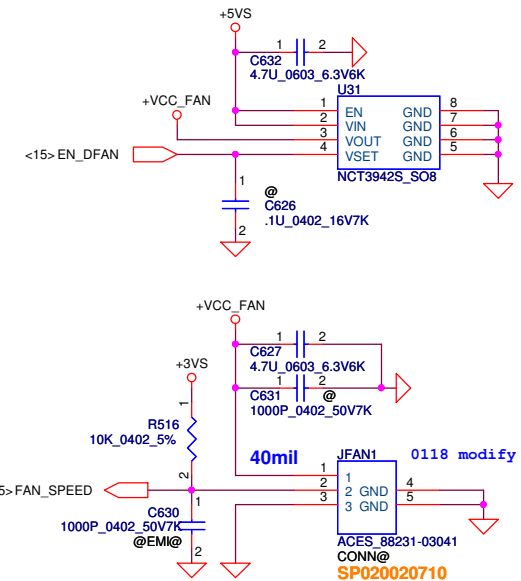
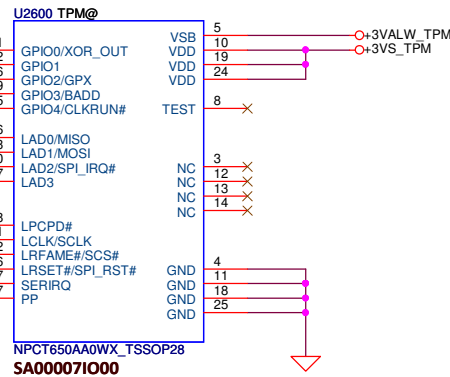
GPIO3/BADD with Internal PH (default)

AMD CLKRUN# no need P

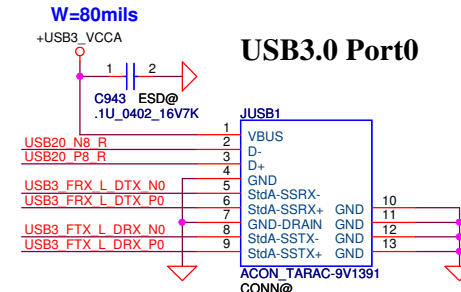
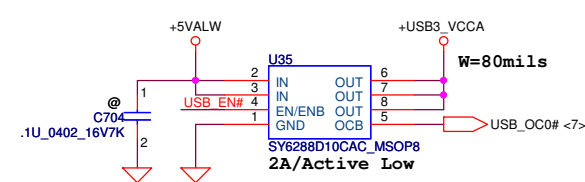
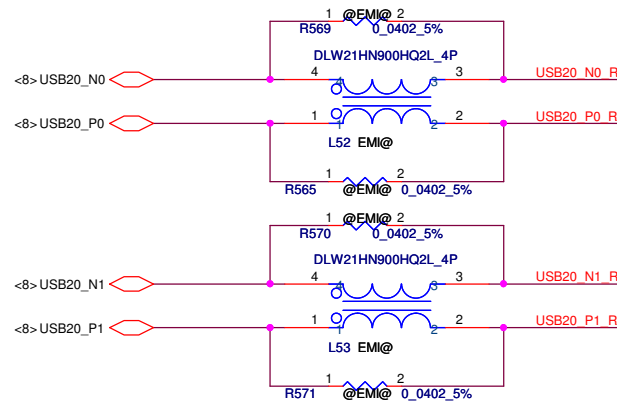
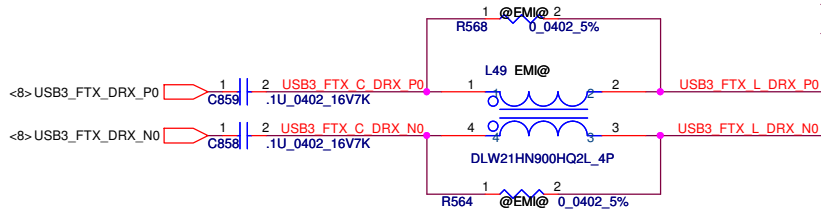
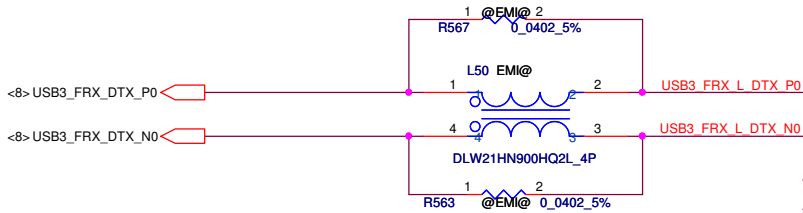
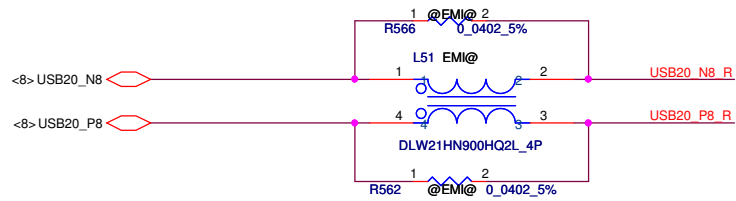
AMD CLKRUN# no need P

LPCPD# had internal PH <8> LPCPD#

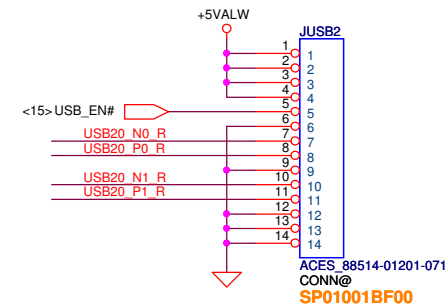
SERIRQ no need PH



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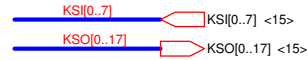


USB/B(USB Port 0, Port1)

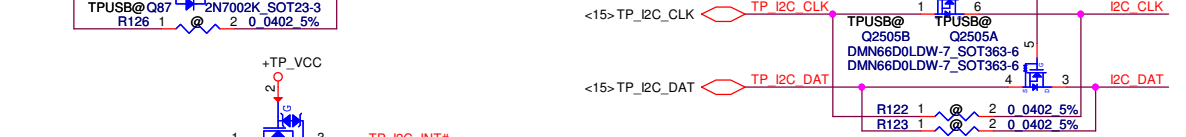


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2014/03/27				2016/03/27				Title			
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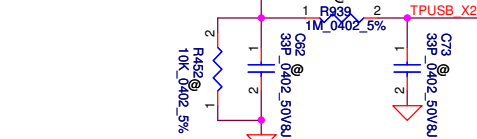
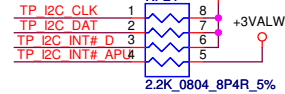
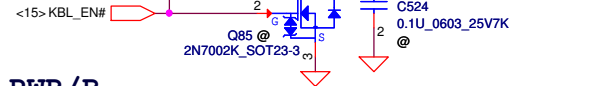
KB Conn.



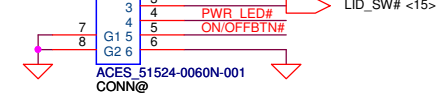
To TP/B Conn.



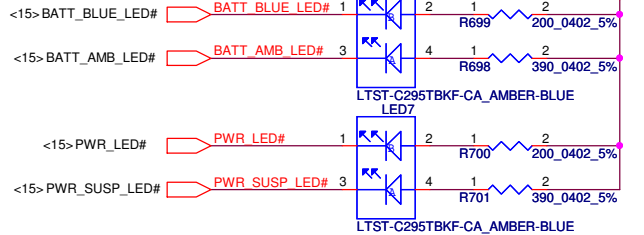
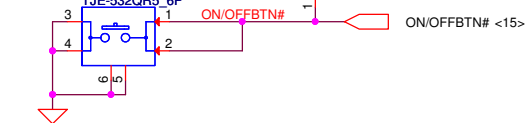
KB BackLight Conn. Reserve



PWR/B

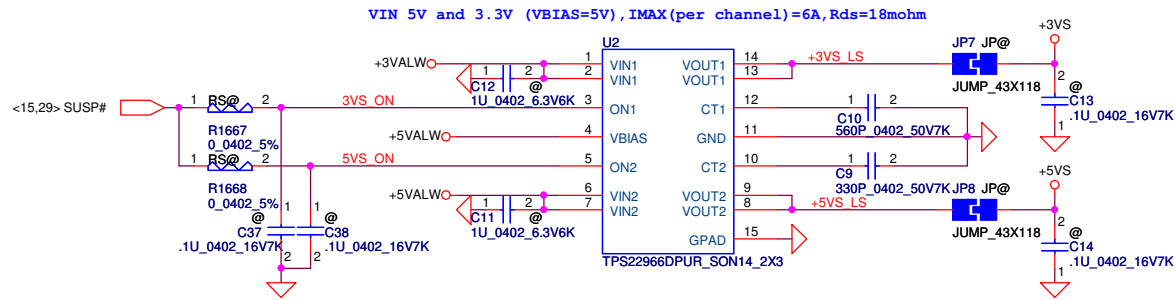


ON/OFF BTN

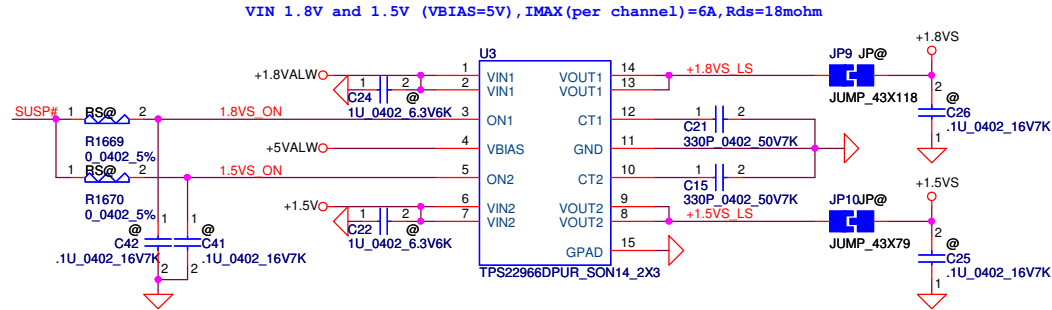


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				Size B	Document Number	Rev 1.0
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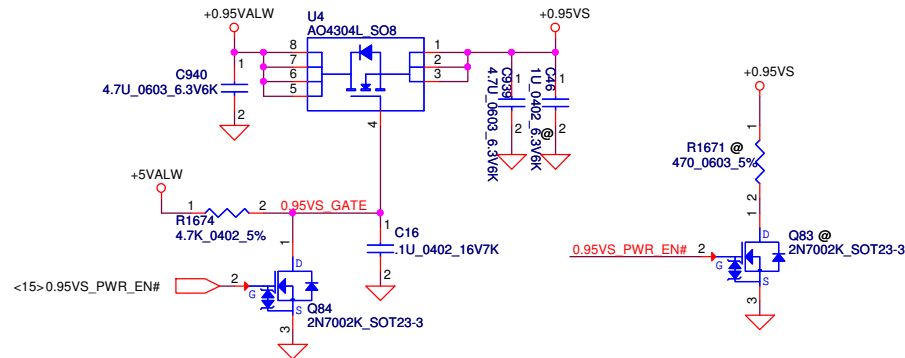
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



+1.8VALW TO +1.8VS
+1.5V TO +1.5VS
Load switch



+0.95VALW to +0.95VS



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0.1

- 1. Add R139 for colay CY7C65211 and MA723C
- 2. Change Y3 to SJ100001K00
- 3. Change Q9 to MESS138
- 4. Reserve C607 pad for ESD request
- 5. Swap D10.2, D10.3 and change D10.3 to RING2
- 6. Delete L22, C950, C203
- 7. Change R404, R73 connect to +0.95VS
- 8. Connect R139 to U69.2
- 9. Change R452 to 10K
- 10. Change C43 to 4.7U
- 11. Change C43 to 1U
- 12. Add T18, T24, T25
- 13. Chagne U2 and U3 P/N to SA00006FD00
- 14. Change U2 and U3 P/N to SA00004MM00
- 15. Unpop Q2505,Q87, RP24; Pop R122,R123,R134,R1683

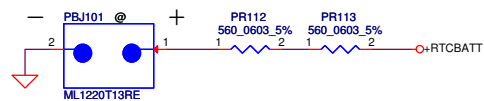
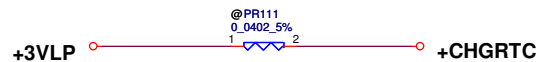
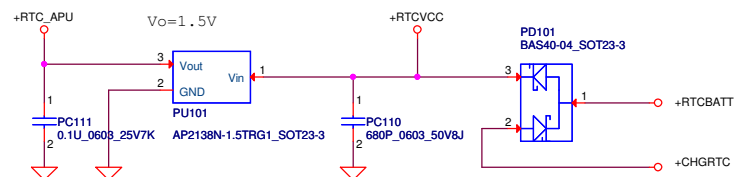
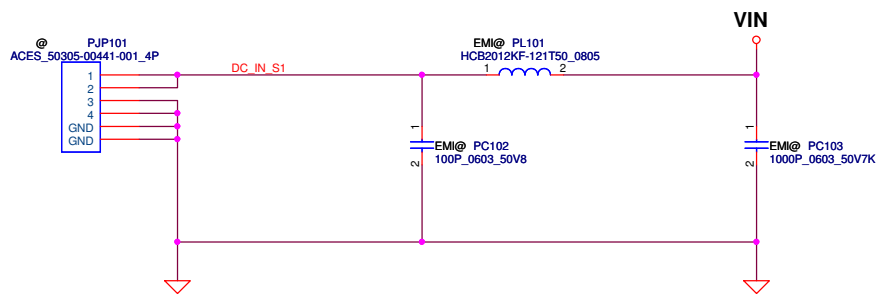
0.2

- 1. Change R119 to Rshort
- 2. Add U23,U24,Q2506,D20 and D21 for D-sub
- 3. Change U69 power to +3VALW and +5VALW; modify Q2505 body diode issue.
- 4. Add L52,L53,R565,R569,R570 and R571 for EMI request.
- 5. Add R127,R128,R140,R141,R142,R143 for reserve USB TP
- 6. Add R209 to prevent EC out of control
- 7. Change LAN_WAKE# PU to +3V_LAN
- 8. Change BID to 1 for DVT
- 9. Change C99,C100 to 10p for crystal test
- 10. Change R238 and R237 to 59ohm
- 11. Add L76,L77,C2142 and C2140 for ESD request
- 12. Change R756,R765,R769,R779,R781,R782,R783 and R794 to Rshort for EMI request
- 13. Pop Q89, unpop R1690
- 14. Change D10 to SCA00001B00
- 15. Add C609 for ESD request
- 16. Change L11 to SM01000EJ00
- 17. Add C668 and C832 for vendor request
- 18. Remove APU_ALERT#_R
- 19. Add H12,remove H30,swap H21 and H31

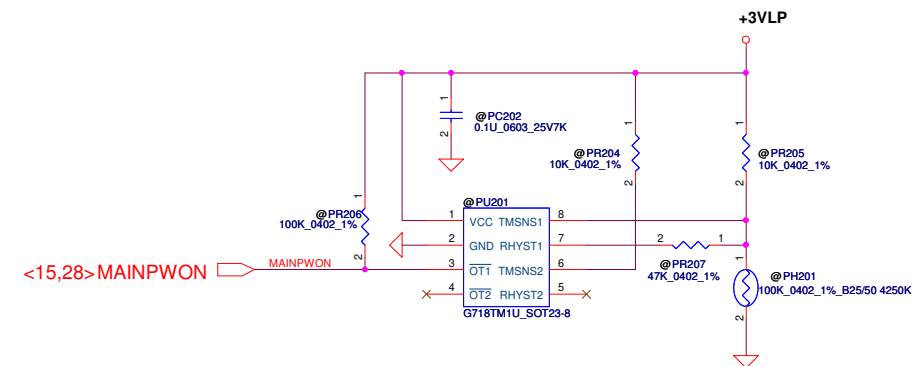
0.3

- 1. Change JTP1
- 2. Add U78 for TP +3V power plane
- 3. Change C736 to 150u D2 type.
- 4. Change R699, R700 to 330ohm; R698, R701 to 560ohm
- 5. Change U69 +3VALW to +3VS
- 6. Add C366, C367, C368, C369 for EMI request
- 7. Add on board TPM
- 8. Add R619

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					Size	Document Number	Rev
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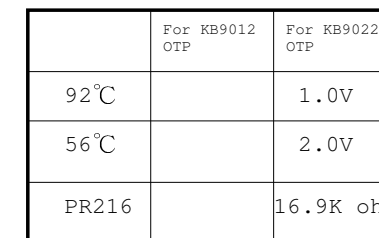
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title	DCIN	
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PIN1	GND	PIN8	GND
PIN2	GND	PIN7	GND
PIN3	SMD	PIN6	SMD
PIN4	SMC	PIN5	SMC
PIN5	TS	PIN4	TS
PIN6	B/I	PIN3	B/I
PIN7	Batt+	PIN2	Batt+
PIN8	Batt+	PIN1	Batt+

PIN8	GND
PIN7	GND
PIN6	SMD
PIN5	SMC
PIN4	TS
PIN3	B/I
PIN2	Batt+
PIN1	Batt+

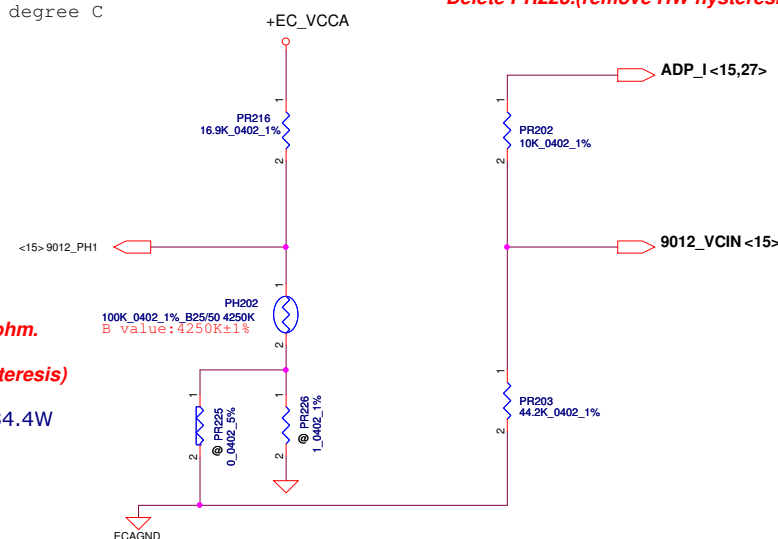
Battery is 3-cell design.
B+=9V



For KB9022 sense 20mΩ	Active	Recovery
40W	43W, 0.73V	34.4W, 0.59V

2013/12/16 Modify
Delete PR223.(remove HW hysteresis)

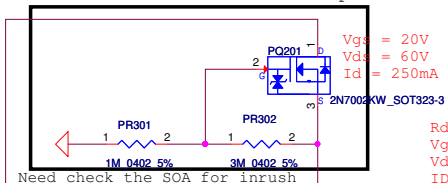
For 40W adapter==>action 43W , Recovery 34.4W



2013/10/25 Modify
PR227(9012@) change to 26.1K ohm.
2014/02/07 Modify
Delete @PR227.(remove HW hysteresis)

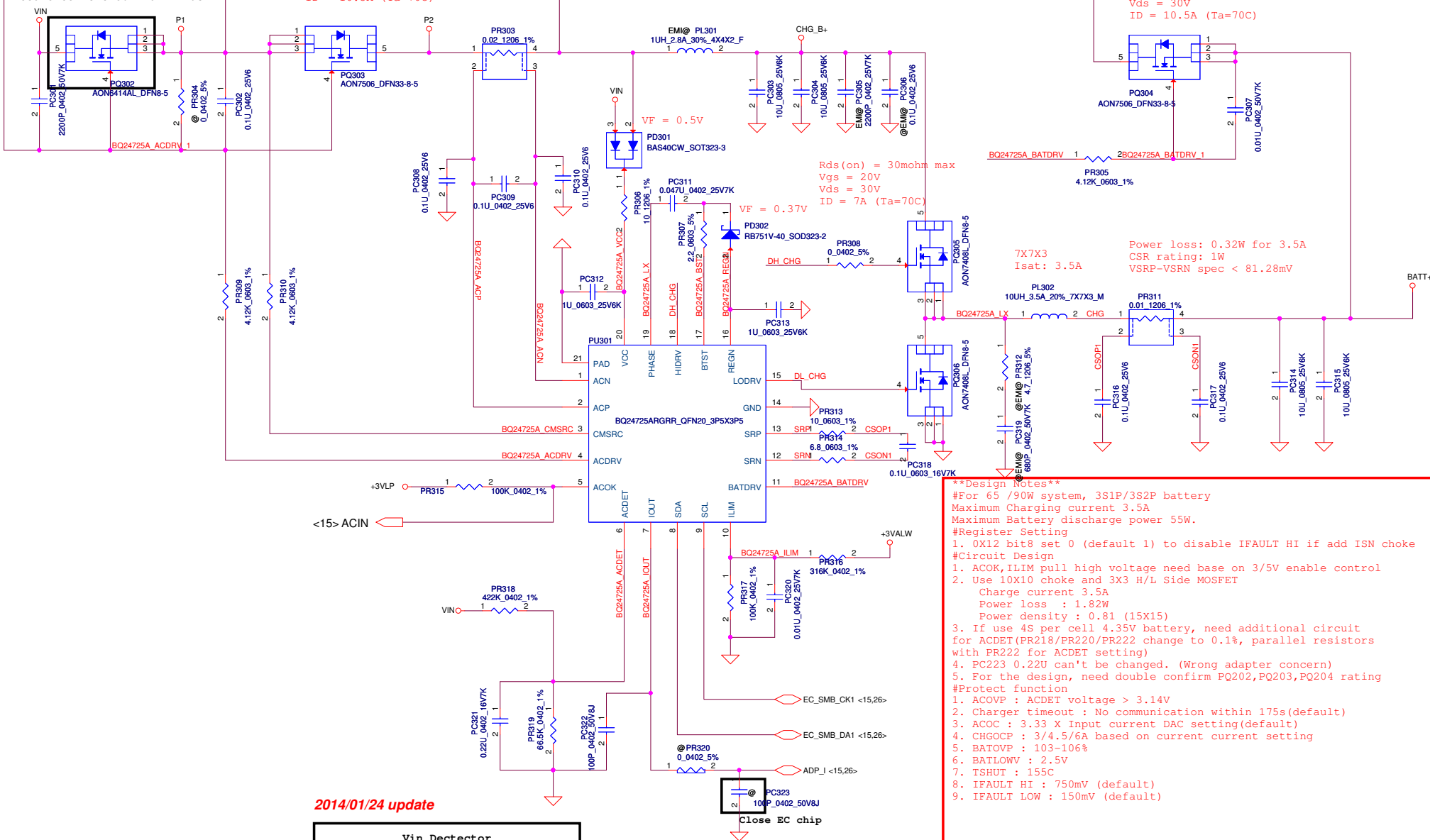
ECAGND					
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Protection for reverse input



2013/10/14
PR303 10m ohm chang -->20m ohm
SD00000S120

Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)



2014/01/24 update

Vin Detector			
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
 ILIM = 3.3*100/(100+316)/20/0.01
 = 3.966 A

2013/10/16 Modify
PQ305,PQ306 change to AON7408L.
2013/10/22 Modify
PL302 change to common part.
2013/11/29 Modify
PL301 change to common part.

Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)

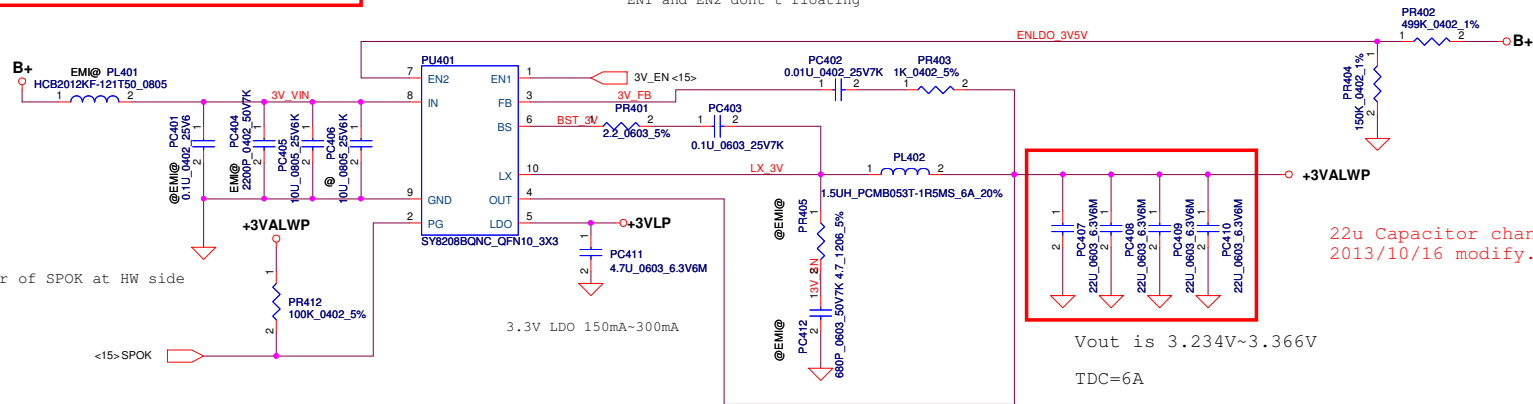
****Design Notes****
 #For 65 /90W system, 3S1P/3S2P battery
 Maximum Charging current 3.5A
 Maximum Battery discharge power 55W.
 #Register Setting
 1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
 #Circuit Design
 1. ACOK,ILIM pull high voltage need base on 3/5V enable control
 2. Use 10X10 choke and 3X3 H/L Side MOSFET
 Charge current 3.5A
 Power loss : 1.82W
 Power density : 0.81 (15X15)
 3. If use 4S per cell 4.35V battery, need additional circuit for ACDET (PR218/PR220/PR222 change to 0.1%, parallel resistors with PR222 for ACDET setting)
 4. PC223 0.22u can't be changed. (Wrong adapter concern)
 5. For the design, need double confirm PQ202,PQ203,PQ204 rating
 #Protect function
 1. ACOVP : ACDET voltage > 3.14V
 2. Charger timeout : No communication within 175s(default)
 3. ACOC : 3.33 X Input current DAC setting(default)
 4. CHGOC : 3/4.5/6A based on current current setting
 5. BATOV : 103-106%
 6. BATLOW : 2.5V
 7. TSHUT : 155C
 8. IFAULT HI : 750mV (default)
 9. IFAULT LOW : 150mV (default)

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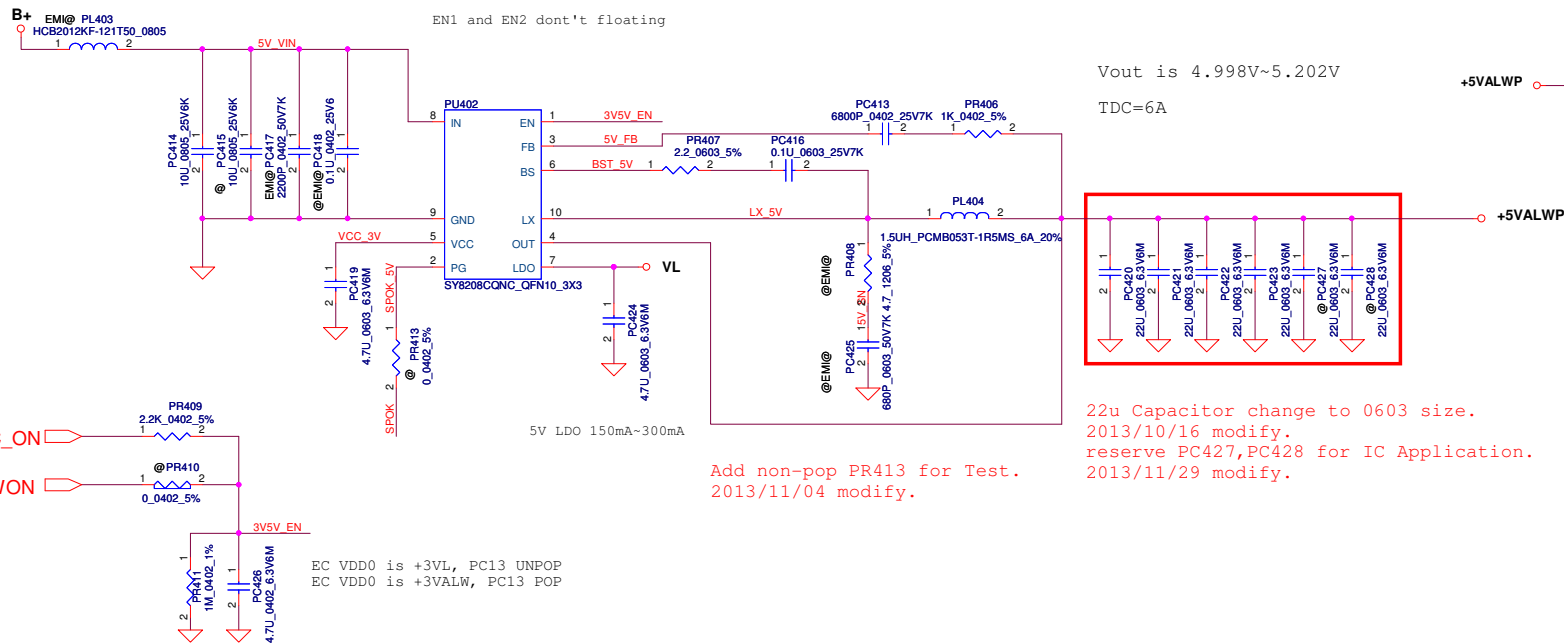
Module model information

SY8208B_V2.mdd
SY8208C_V2.mdd

EN1 and EN2 don't floating



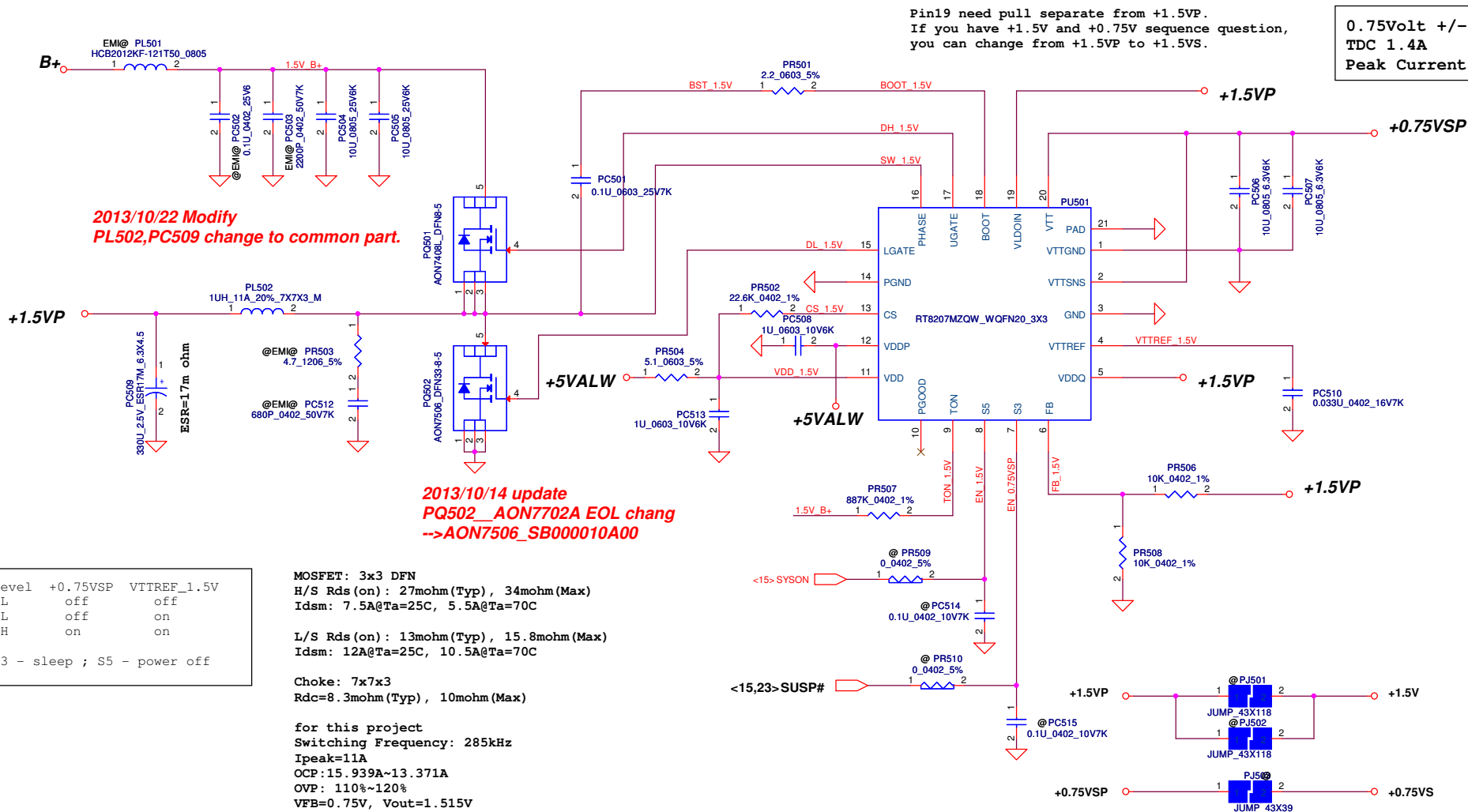
EN1 and EN2 don't floating



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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer



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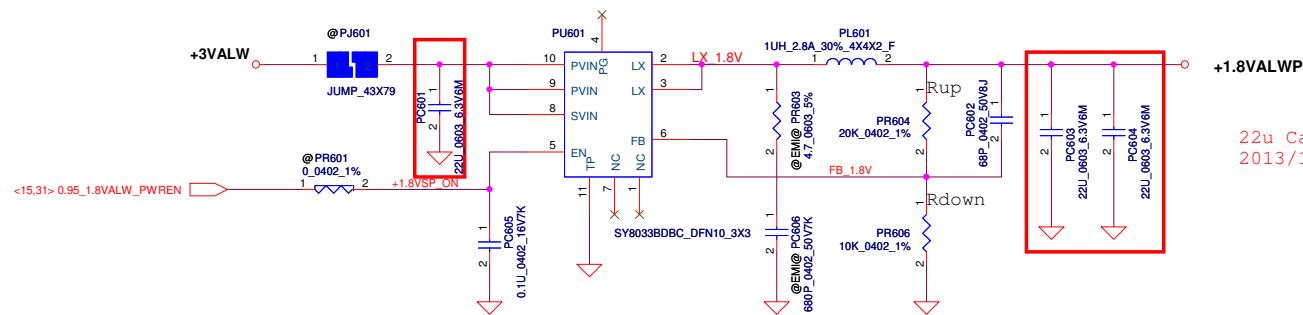
Module model information

SY8033_V1.mdd

22u Capacitor change to 0603 size.
2013/10/16 modify.

2013/10/22 Modify
PL601 change to common part.

FB=0.6V
Note: Iload (max)=3.5A



22u Capacitor change to 0603 size.
2013/10/16 modify.

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

Delete PR605, because same net name have two PD resister in circuit.
2013/11/29 modify.



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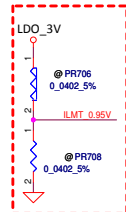
+1.8VALWP

Module model information

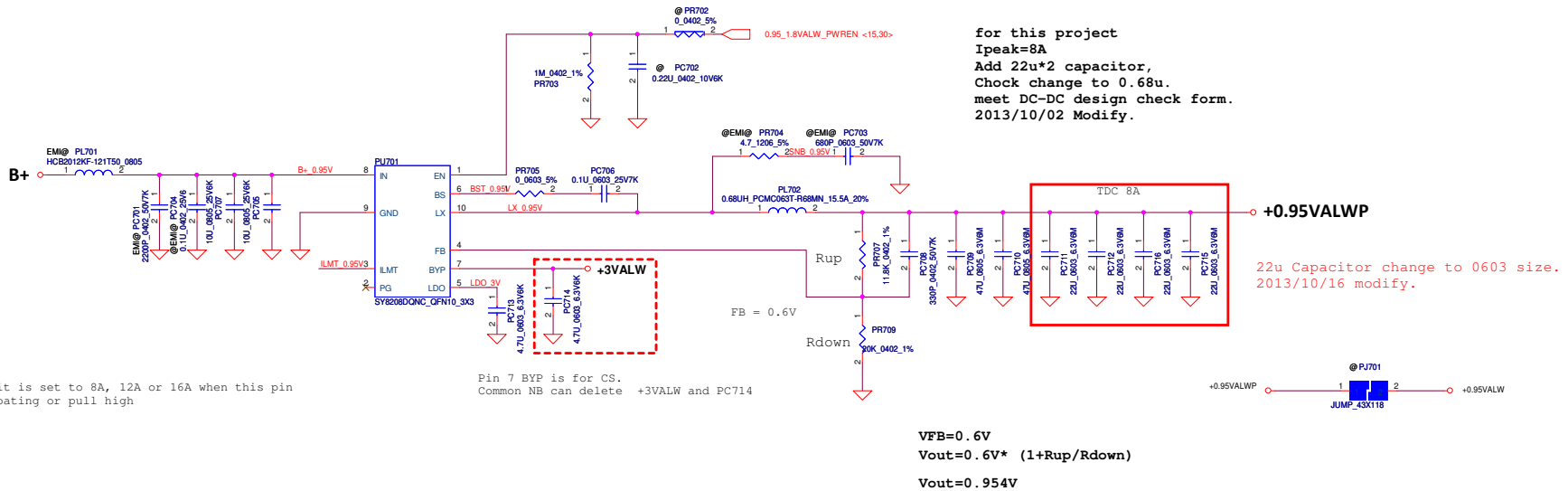
SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

for this project
Ipeak=8A
Add 22u*2 capacitor,
Chock change to 0.68u.
meet DC-DC design check form.
2013/10/02 Modify.



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

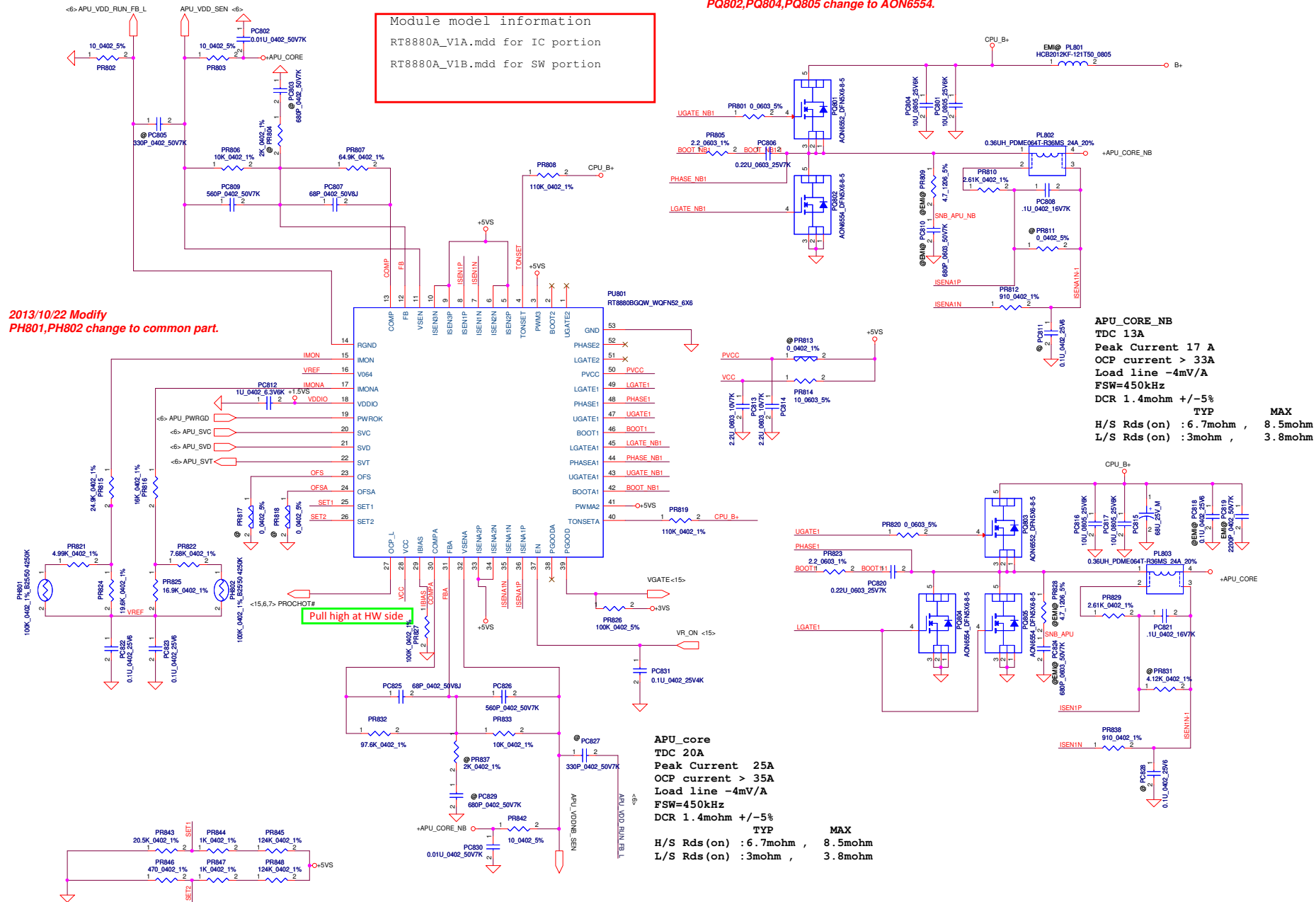


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2013/10/16 Modify
 PQ801,PQ803 change to AON6552.
 PQ802,PQ804,PQ805 change to AON6554.

Module model information
 RT8880A_V1A.mdd for IC portion
 RT8880A_V1B.mdd for SW portion

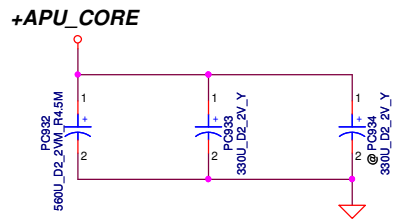
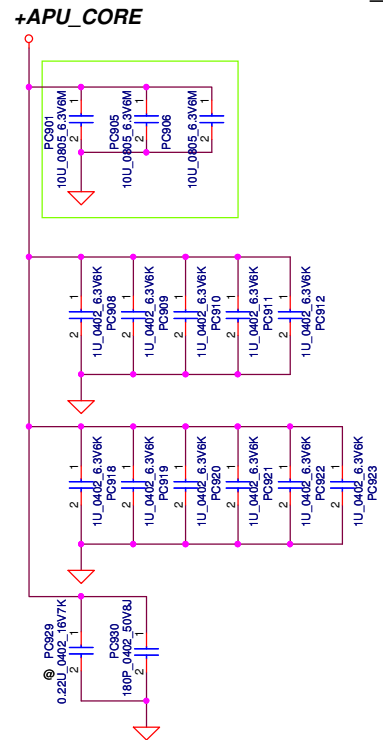
2013/10/22 Modify
 PH801,PH802 change to common part.



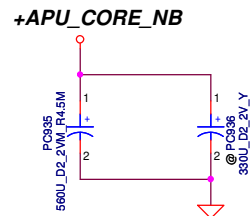
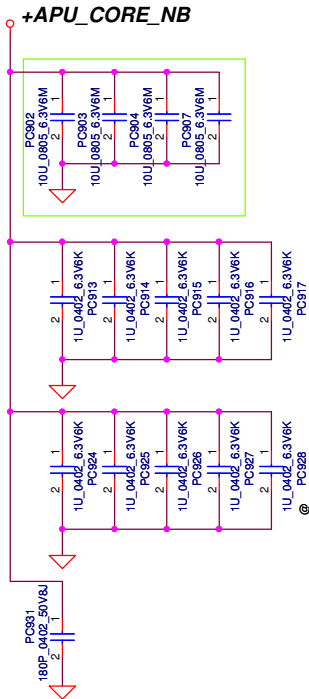
Delete PR834.PR835.PR836.PR839.PR840.PR841,
 follow vender FAE suggest.
 2013/11/29 modify.

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+APU_CORE (36.4)



+APU_CORE_NB (36.5)



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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Design Change.	Design Change of Diode Application.	0.2	25	Change PD101 to SCSS4004010(S SCH DIO BAS40-04 SOT23).	2013/11/29	DVT
2	Design Change.	Design Change of IC Application.	0.2	28	Add non-pop component PC427,PC428.	2013/11/29	DVT
3	Design Change.	reduce part count.	0.2	30	Delete PR605 PD resister.	2013/11/29	DVT
4	Design Change.	reduce part count.	0.2	32	Delete @PR834.@PR835.@PR836.@PR839.@PR840.@PR841.	2013/11/29	DVT
5	Design Change.	Design Change of common part.	0.2	27	Change PL301 to SH00000YG00 (S COIL 1UH +-30% 2.8A 4X4X2 FERRITE).	2013/11/29	DVT
6	Design Change.	Design Change of EC Type Application.	0.2	28	Add PD401 SCS00000Z00(S SCH DIO RB751V-40 SOD-323)	2013/11/29	DVT
7	Design Change.	Design Change of Circuit Application.	0.2	26	Delete PR223.(remove HW hysteresis)	2013/12/16	DVT
8	Design Change.	Design Change of Circuit Application.	0.2	27	Change PQ303,PQ304 to SB000010A00(S TR AON7506 1N DFN).	2013/12/19	DVT
9	Design Change.	Design Change of Circuit Application.	0.2	26	Add PL202 SM01000C000 (S SUPPRE_ TAI-TECH HCB2012KF-121T50 0805)	2013/12/19	DVT
10	Design Change.	Design Change of Circuit Application.	0.2	26	Change PR211 to SD028000080(S RES 1/16W 0 +-5% 0402).	2013/12/25	DVT
11	Design Change.	Design Change of Circuit Application.	0.2	28	Change PC426 to pop.	2013/12/25	DVT
12	Design Change.	Design Change of Circuit Application.	0.2	26	Change PR216 to SD034162280(S RES 1/16W 16.2K +1% 0402).	2013/12/25	DVT
13	Design Change.	Design Change of Circuit Application.	0.2	26	Change PR216 to SD034169280(S RES 1/16W 16.9K +-1% 0402).	2014/01/02	DVT
14	Design Change.	Design Change of Circuit Application.	0.2	26	Change PR202 to SD034100280(S RES 1/16W 10K +-1% 0402).	2014/01/02	DVT
15	Design Change.	Design Change of Circuit Application.	0.2	26	Change PR203 to SD034442280(S RES 1/16W 44.2K +-1% 0402).	2014/01/02	DVT
16	Design Change.	Design Change of Circuit Application.	0.3	30.31.32	Change PR813,PR601,PR706,PR702, to SD028000080(S RES 1/16W 0 +-5% 0402).	2014/02/07	PVT

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