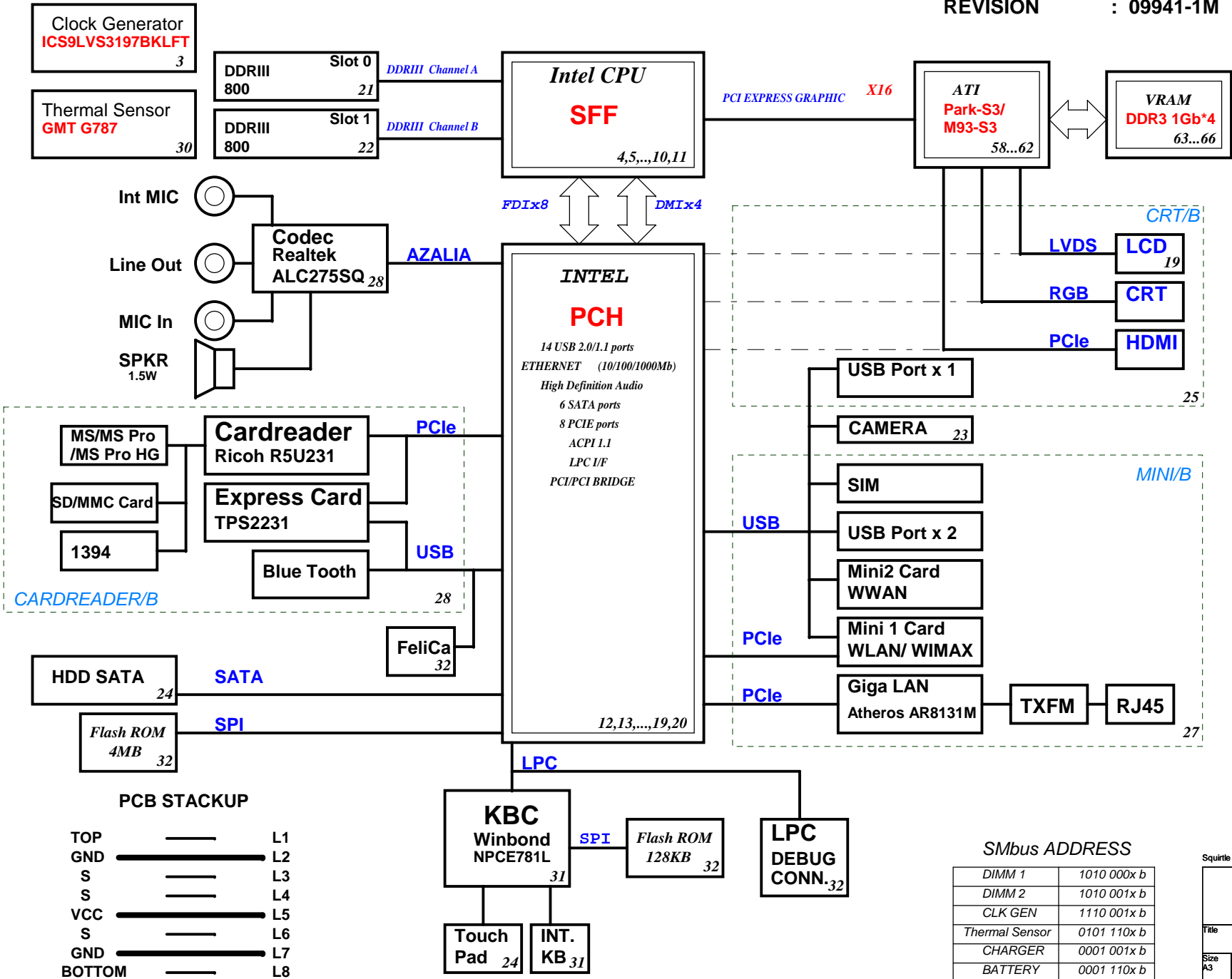


CADIZ-CP Block Diagram

PROJECT CODE : 91.4JH01.001
PCB P/N : 48.4JH01.01M
REVISION : 09941-1M



SYSTEM DC/DC RT8223 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(9A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5
RT8209 39	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(20A)
RT8209 38	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(13.5A)
RT9026 36	
INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 1.2A
CHARGER BQ24751 32	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC ADP3211 36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 27A
VGA/ GFX Core ADP3211 40	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE/ VCC_GFXCORE 11A

Squirrel CP DIS SAMSUNG

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

BLOCK DIAGRAM		
Size A3	Document Number	Rev -1M
Date: Saturday, April 24, 2010	Sheet 1 of 57	

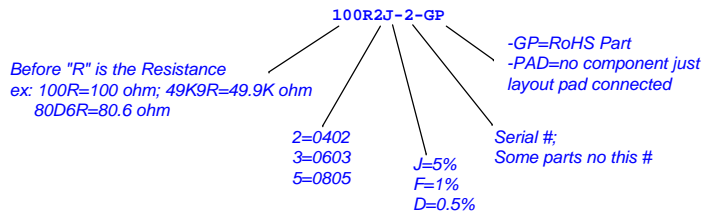
PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

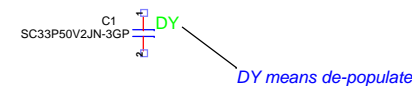
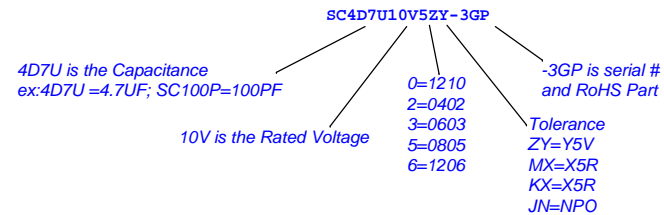
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ESI) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (xPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

Resistor

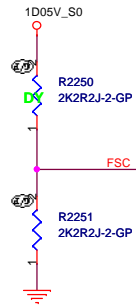
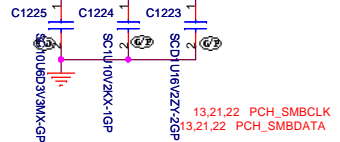
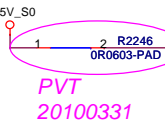
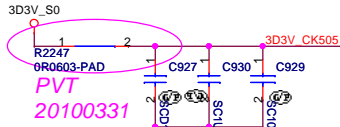
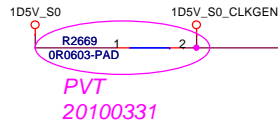
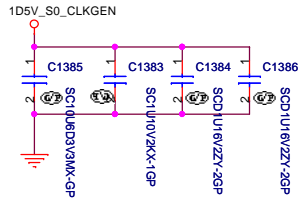


Capacitor



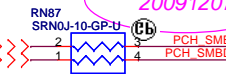
Squintle CP DIS SAMSUNG

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reference			
Size A3	Document Number	CADIZ-CP	Rev -1M
Date: Saturday, April 24, 2010		Sheet 2	of 57

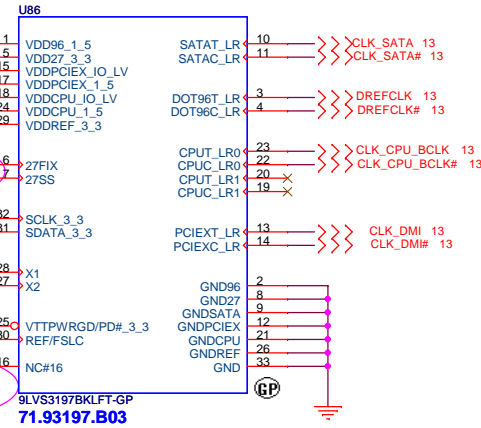


14.318 MHz

FSC	0	1
SPEED	133MHz (Default)	100MHz

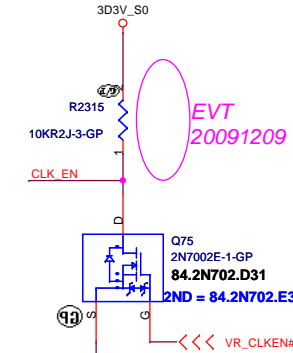
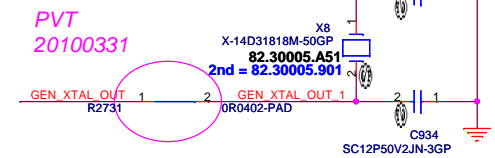


PIN#	1	5	15	17	18	24	29	16
9LRS3197	3.3V	3.3V	1.05V~3.3V	3.3V	1.05V~3.3V	3.3V	3.3V	CPU_STOP#
9LVS3197	1.5V	3.3V	1.05V~1.5V	1.5V	1.05V~1.5V	1.5V	3.3V	NC



100 MHz SATA
96 MHz PCH
133-MHz CPU
100 MHz DMI

14.31818M HZ
CL=10pF±0.2pF



Squirtle CP DIS SAMSUNG

緯創資通

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Title

Clock Generator

Size

Document Number

CADIZ-CP

Date

Saturday, April 24, 2010

Sheet

3

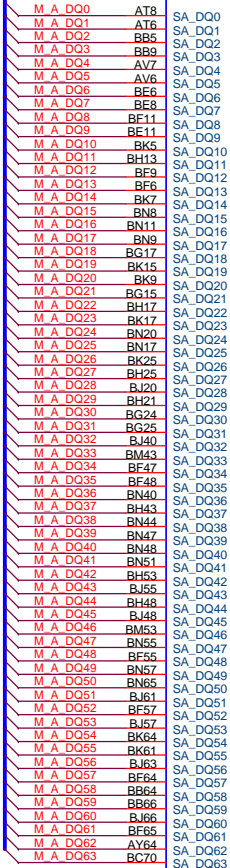
of

57

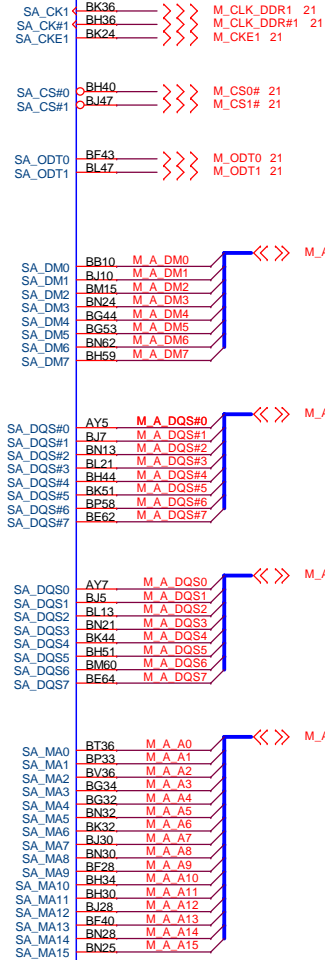
Rev

-1M

21 M_A_DQ[63..0] <<>>



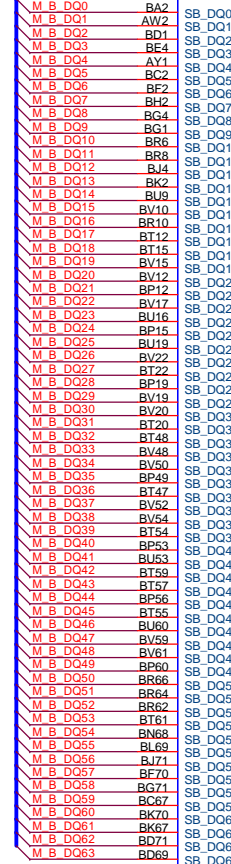
DDR SYSTEM MEMORY A



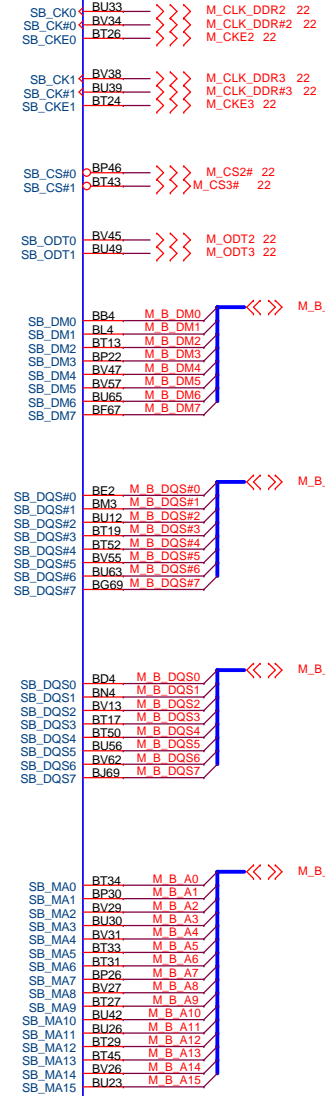
AUBURDALE-1-GP-U3-NF



22 M_B_DQ[63..0] <<>>



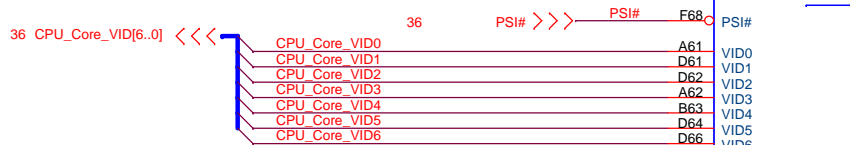
DDR SYSTEM MEMORY - B



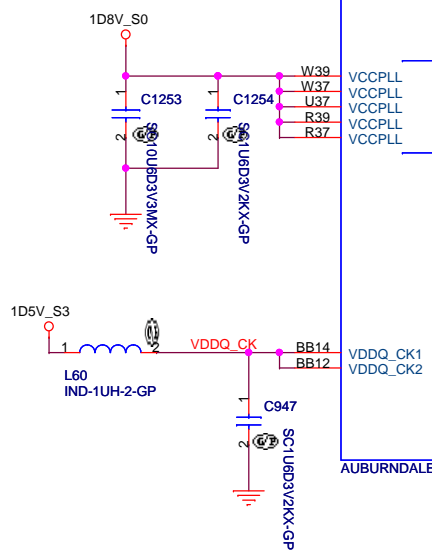
Squirtle CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title CPU SFF 3 of 8(DDR)			
Size A3	Document Number CADIZ-CP	Rev -1M	
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EVT
20091201



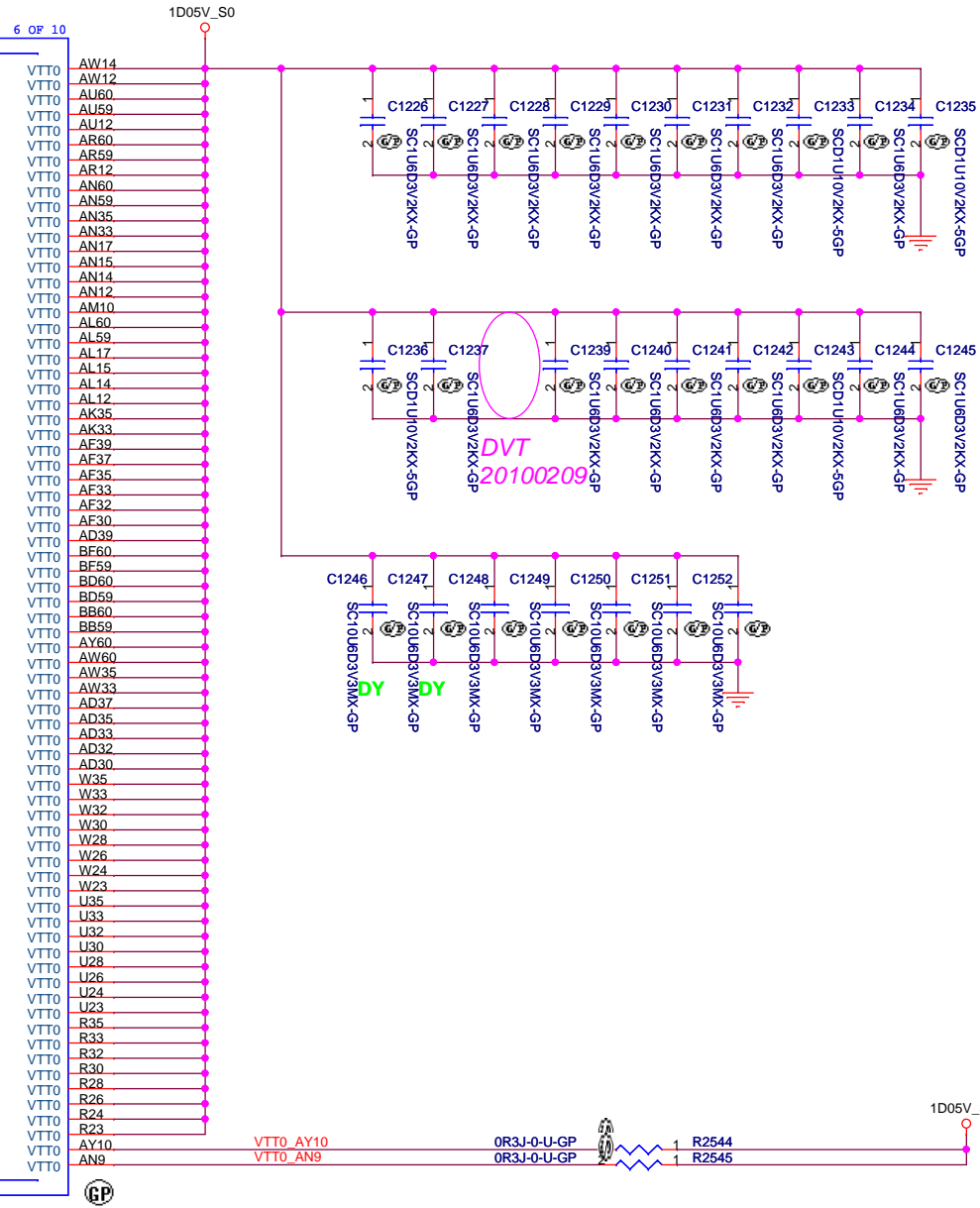
Please note that the VTT Rail
Values are Auburndale
VTT=1.05V; Clarksfield
VTT=1.1V

POWER

CPU VIDS

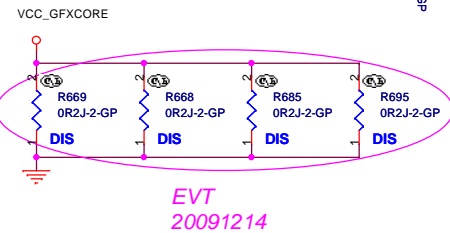
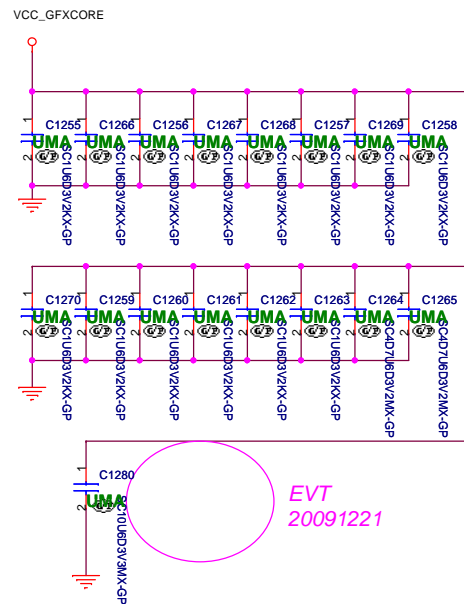
SENSE LINES

1.1V RAIL POWER

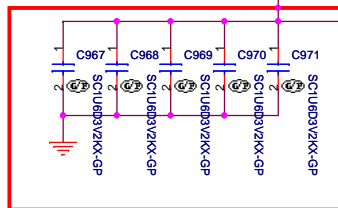
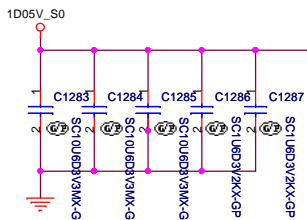


Squirrelle CP DIS SAMSUNG

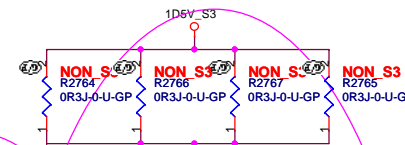
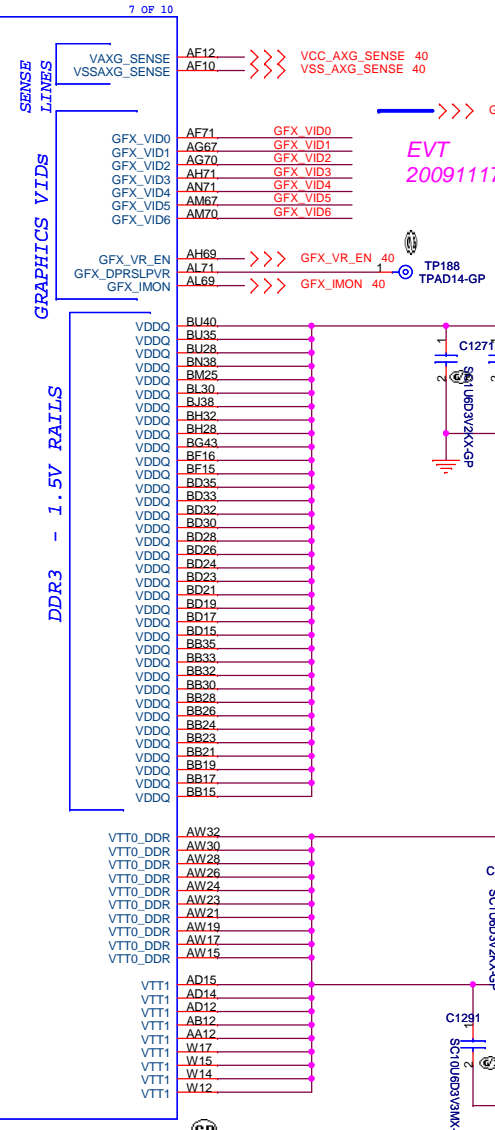
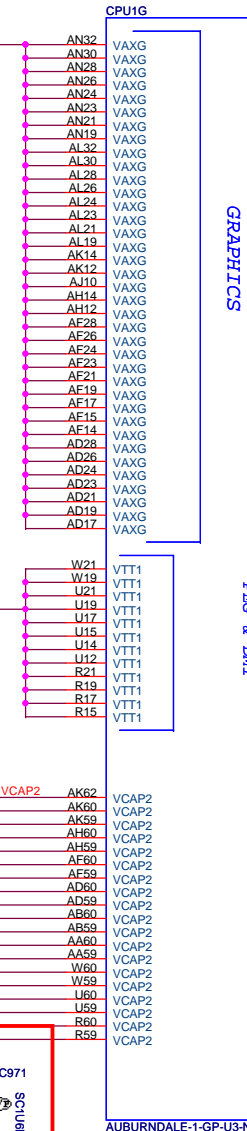
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU SFF 4 of 8(POWER/VTT)	
Size Custom	Document Number CADIZ-CP
Date: Saturday, April 24, 2010	Sheet 7 of 57
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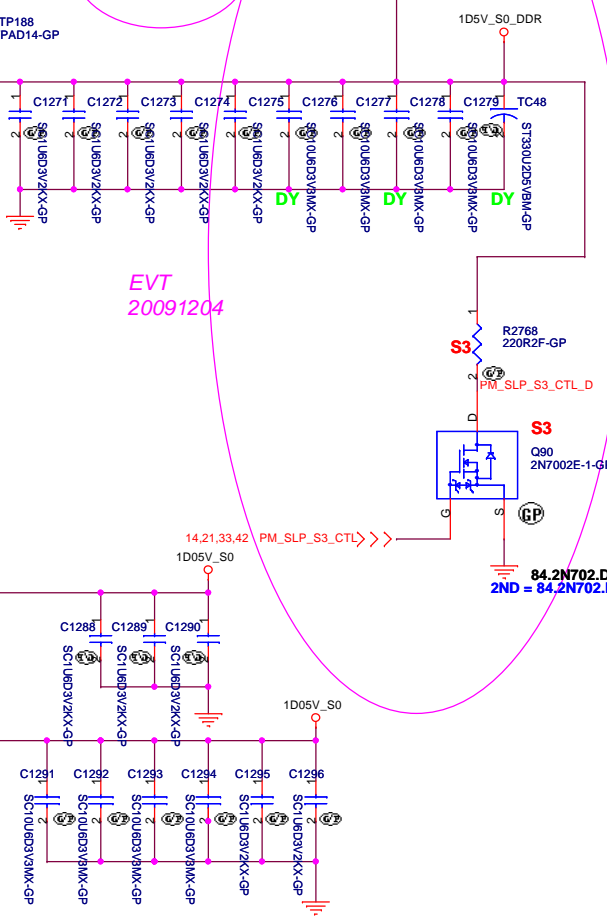
EVT
20091214



Do not dummy these CAPS



EVT
20091204



Squirrelle CP DIS SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU SFF 5 of 8(PWR/DDR/GFX/)	
Size A3	Document Number CADIZ-CP
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Rev -1M	

CPU1E

5 OF 10

RSVD#W66
RSVD#W64W66
W64RSVD#AC69
RSVD#AC71AC69
AC71RSVD#AA71
RSVD#AA69AA71
AA69RSVD#R66
RSVD#R64R66
R64RSVD_NCTF#BT5
RSDV_NCTF#BR5BT5
BR5RSDV_NCTF#BV6
RSDV_NCTF#BV8BV6
BV8RSVD#AV69
RSVD#AK71AV69
AK71RSVD#AN69
RSVD#AP66AN69
AP66RSVD#AH66
RSVD#AK66AH66
AK66RSVD#AR71
RSVD#AM66AR71
AM66RSVD#AK69
RSVD#AU71AK69
AU71RSVD#AT70
RSVD#AR69AT70
AR69RSVD#AU69
RSVD#AT67AU69
AT67RSVD_TP2
RSVD_TP1AP2
AN7RSVD#AV4
RSVD#AU2AV4
AU2RSVD#BE69
RSVD#BE71BE69
BE71

RESERVED

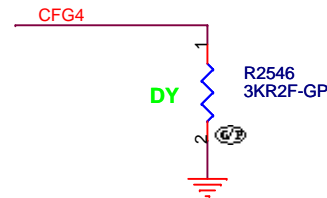
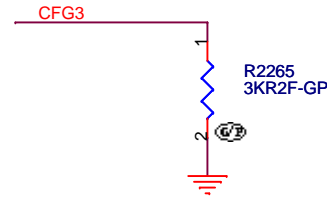
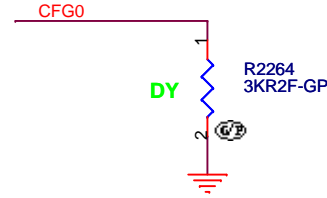
RSVD_TP0

RSVD#T4
RSVD#T2RSVD#U1
RSVD#V2RSVD#AV71
RSVD#AW70RSVD#AY69
RSVD#BB69RSVD#D8
RSVD#B7RSVD#A10
RSVD#B9RSVD_NCTF#C5
RSVD_NCTF#A6RSVD_NCTF#E3
RSVD_NCTF#F1

NCTF TEST PIN:

A5, A68, A69, A71, C3, C71, E1, E71, BR1, BR71,
BT1, BT71, BV1, BV3, BV5, BV68, BV69, BV71NCTF_DC_TEST#BV71
NCTF_DC_TEST#BV69
NCTF_DC_TEST#BV68
NCTF_DC_TEST#BV5
NCTF_DC_TEST#BV3
NCTF_DC_TEST#BV1
NCTF_DC_TEST#BT71
DC_TEST_BT69
DC_TEST_BT3
NCTF_DC_TEST#BT1
NCTF_DC_TEST#BR71
NCTF_DC_TEST#BR1
NCTF_DC_TEST#E71
NCTF_DC_TEST#E1
NCTF_DC_TEST#C71
DC_TEST_C69
NCTF_DC_TEST#C3
NCTF_DC_TEST#A71
NCTF_DC_TEST#A69
NCTF_DC_TEST#A68
NCTF_DC_TEST#A5BV71
BV69
BV68
BV5
BV3
BV1BT71
BT69
BT3
BT1BR71
BR1
E71C71
C69
C3A71
A69
A68
A5TP149
TPAD14-GPTP150
TPAD14-GPTP151
TPAD14-GPTP152
TPAD14-GP

GP



PCI-Express Configuration Select

CFG0	1:Single PEG 0:Bifurcation enabled
------	---------------------------------------

CFG3 - PCI-Express Static Lane Reversal

CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...
------	--

CFG4 - Display Port Presence

CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port
------	---

Squirrel CP DIS SAMSUNG

緯創資通

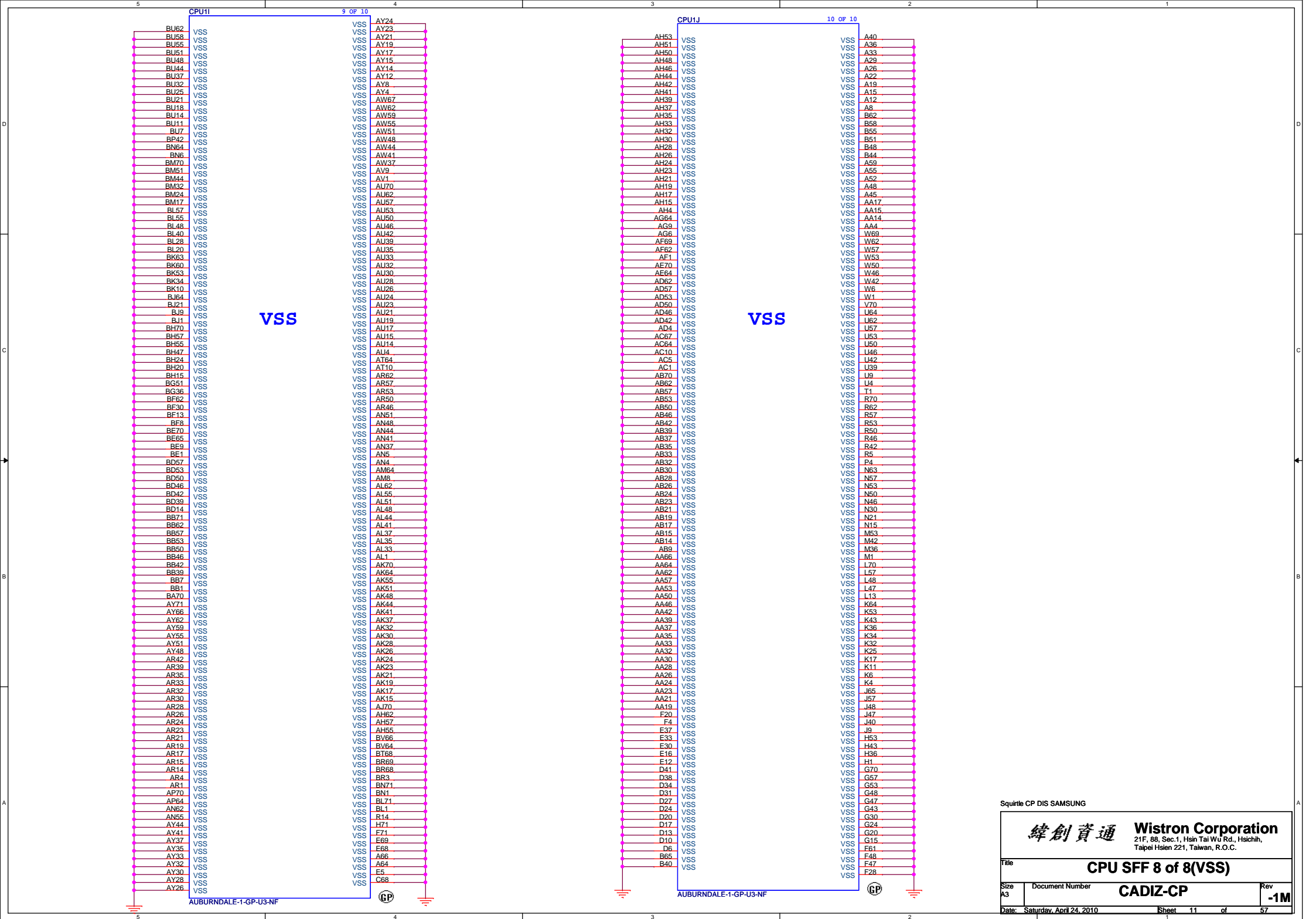
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title CPU SFF 7 of 8(REERVED)

Size A4 Document Number CADIZ-CP Rev -1M

Date: Saturday, April 24, 2010 Sheet 10 of 57



MINICARD1-WLAN

CARDREADER

LAN

ExpressCard

EVT
20091120EVT
20091201

MINICARD1-WLAN

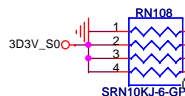
CARDREADER

LAN

ExpressCard

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).



CLK_PCIE_LAN#

CLK_PCIE_LAN#

DVT
20100210

PCH1B

2 OF 10

PCI-E*

Controller

Link

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M-GP-NF

BG30

BJ30

PERP1

PETN1

PETP1

AW30

BA30

PERP2

PETN2

PETP2

AU30

AT30

PERP3

PETN3

PETP3

BA32

BB32

PERP4

PETN4

PETP4

BF33

BH33

BG32

BJ32

BA34

BC34

BD34

AT34

AU34

AV36

BG34

BJ34

BG36

BJ36

AK48

AK47

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

P9

B9

H14

C8

J14

C6

G8

M14

E10

G12

T13

T11

T9

H1

AD43

AD45

AN4

AN2

AT1

AT3

AW24

BA24

AP3

AP1

F18

E18

AH13

AH12

P41

J42

AH51

AH53

AF38

T45

P43

T42

N50

T45

P43

T42

N50

T45

P43

T42

N50

T45

P43

T42

N50

T45

P43

T42

N50

T45

P43

T42

N50

T45

P43

T42

N50

T45

P43

T42

N50

T45

P43

T42

N50

EC_SW# 14,31

SMB_CLK

SMB_DATA

PCH_GPIO60 17

SMB_CLK

SMB_DATA

PCH_GPIO74 16

KBC_SCL1 31

KBC_SDA1 31

CL_CLK1

CL_DATA1

CL_RST1#

PEG_A_CLKRQ# 1

CLK_PCH_PEGA_N

CLK_PCH_PEGA_P

CLK_EXP_N

CLK_EXP_P

CLKOUT_DP_N/CLKOUT_BCLK1_N

CLKOUT_DP/CLKOUT_BCLK1_P

CLKIN_DMI_N

CLKIN_DMI_P

CLKIN_BCLK_N

CLKIN_BCLK_P

CLKIN_DOT_96N

CLKIN_DOT_96P

CLKIN_SATA_N/CKSSCD_N

CLKIN_SATA_P/CKSSCD_P

REFCLK14IN

CLK_PCH_FB 16

XTAL25_IN

XTAL25_OUT

XCLK_RCOMP

CLKOUTFLEX0/GPIO64

CLKOUTFLEX1/GPIO65

CLKOUTFLEX2/GPIO66

CLKOUTFLEX3/GPIO67

33MHZ

33MHZ

33MHZ

48MHZ

33MHZ

33MHZ

33MHZ

33MHZ

33MHZ

33MHZ

33MHZ

33MHZ

33MHZ

33MHZ

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33MHZ

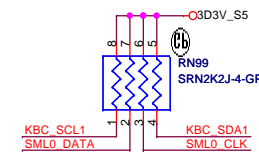
33MHZ

33MHZ

33MHZ

33MHZ

33MHZ



3D3V_S5

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

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3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

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3D3V_S0

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3D3V_S0

3D3V_S0

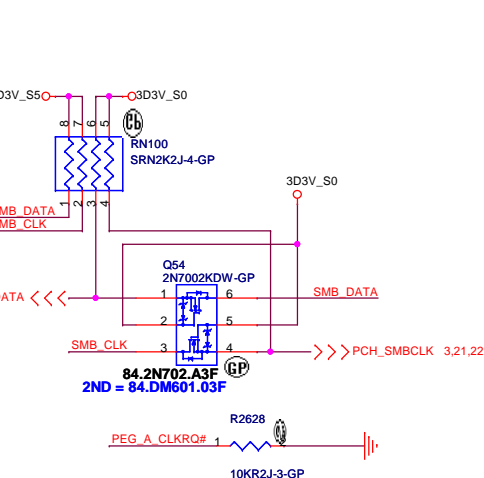
3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0



3D3V_S5

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

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3D3V_S0

3D3V_S0

3D3V_S0

3D3V_S0

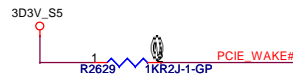
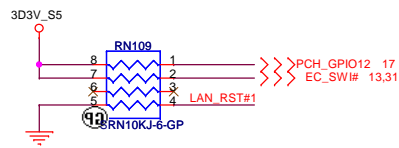
3D3V_S0

3D3V_S0

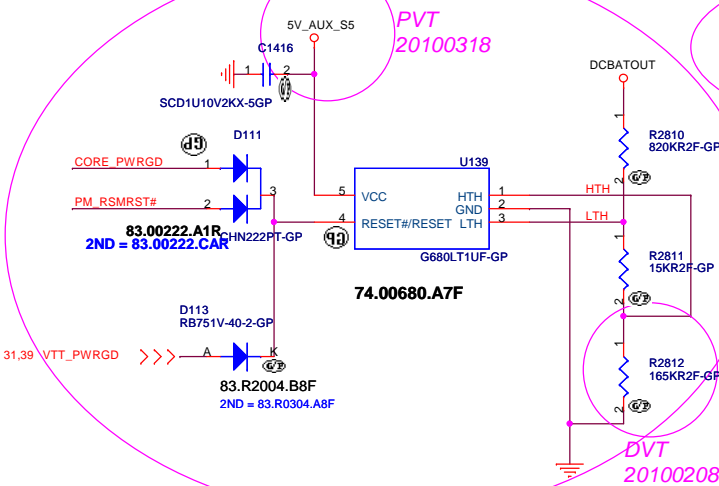
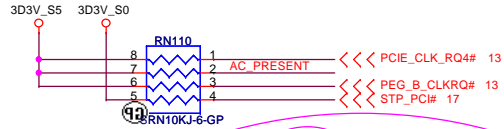
3D3V_S0

3D3V_S0

3D3V_S0

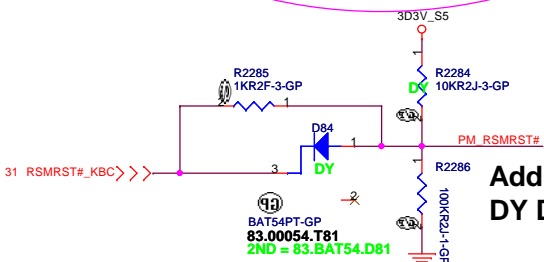


Delete PM_PWRBTN# pull high

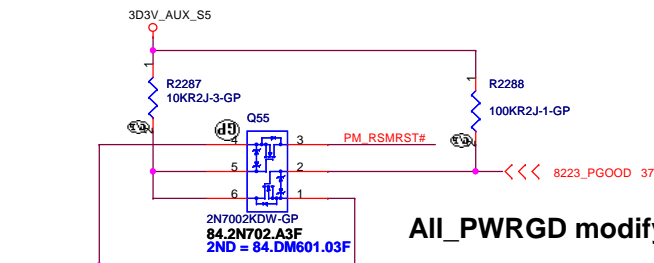


$$V_L = 1.245 \left(\frac{R1+R2+R3}{R2+R3} \right)$$

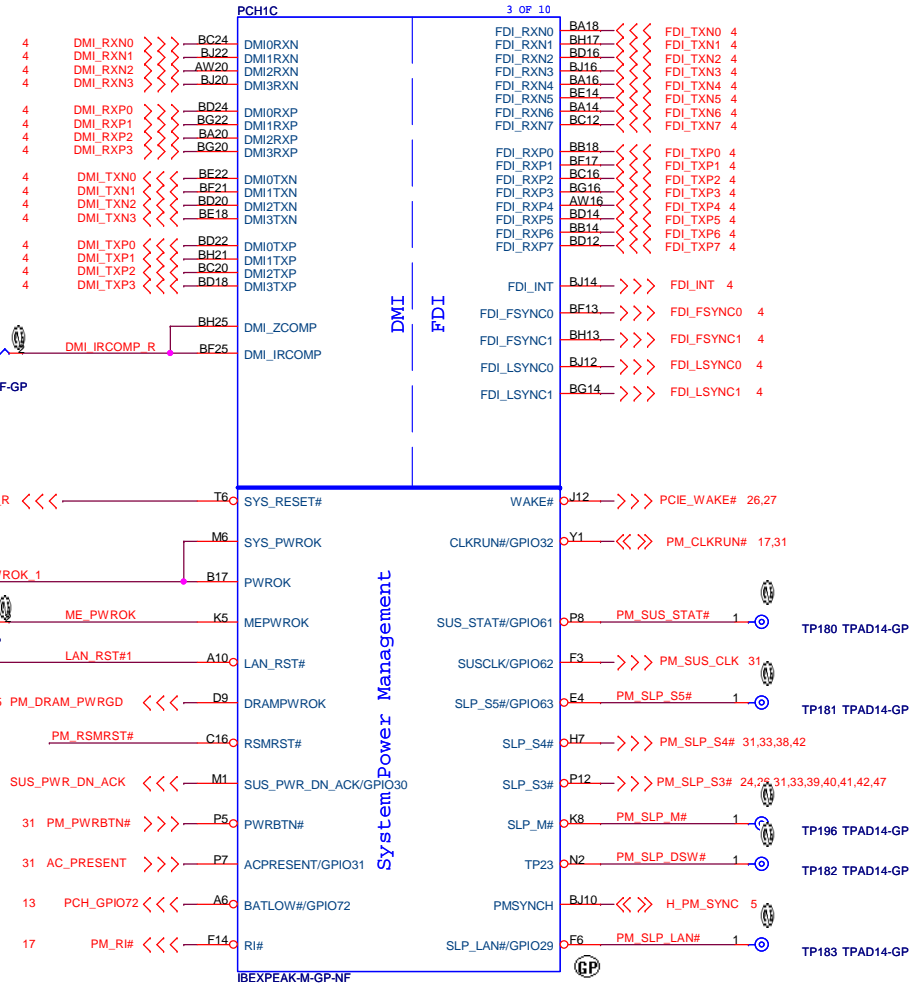
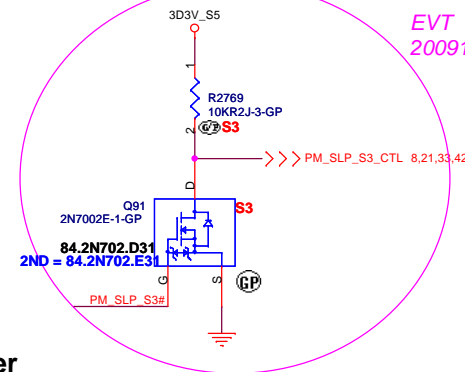
$$V_h = 1.245 \left(\frac{R1+R2+R3}{R3} \right)$$



Add RTC Data lose function
DY D2



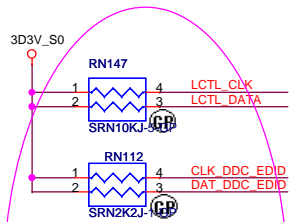
All_PWRGD modify 51123_PGOOD from 3V/5V power



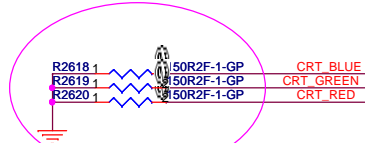
Squirrel CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

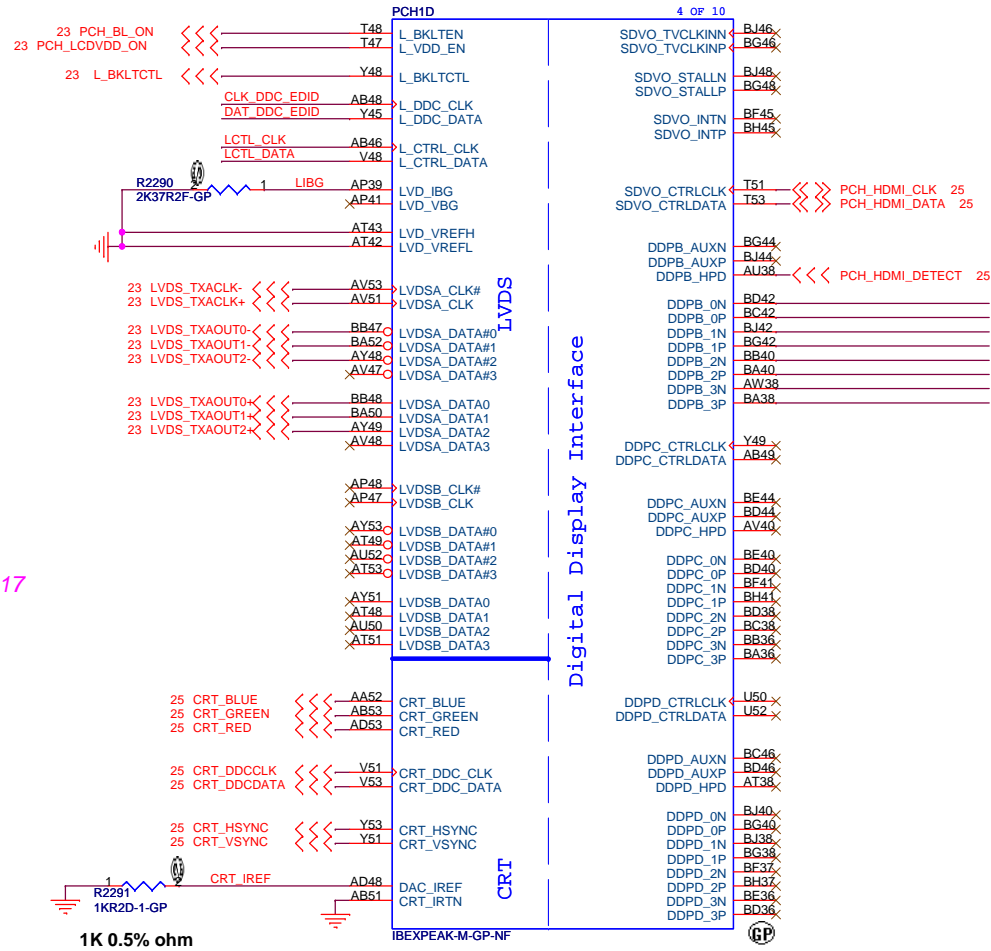
Panel backlight enable control for LVDS -
used to gate power into the backlight circuit



EVT
20091117



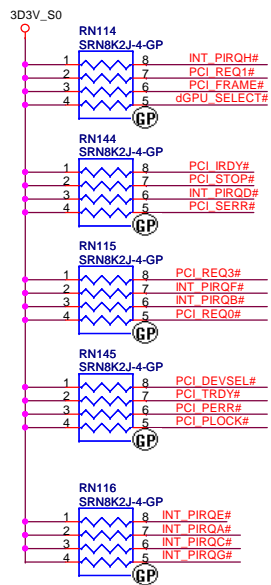
EVT
20091117



Squirrel CP DIS SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

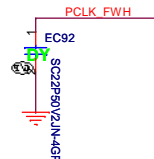
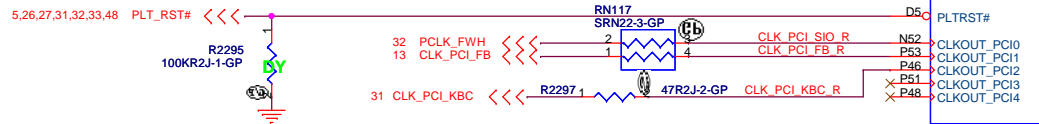
Title			PCH 4 of 9(LVDS/CRT/DP)	
Size	Document Number	CADIZ-CP		Rev
Custom				-1M
Date:	Saturday, April 24, 2010	Sheet	15	of 57



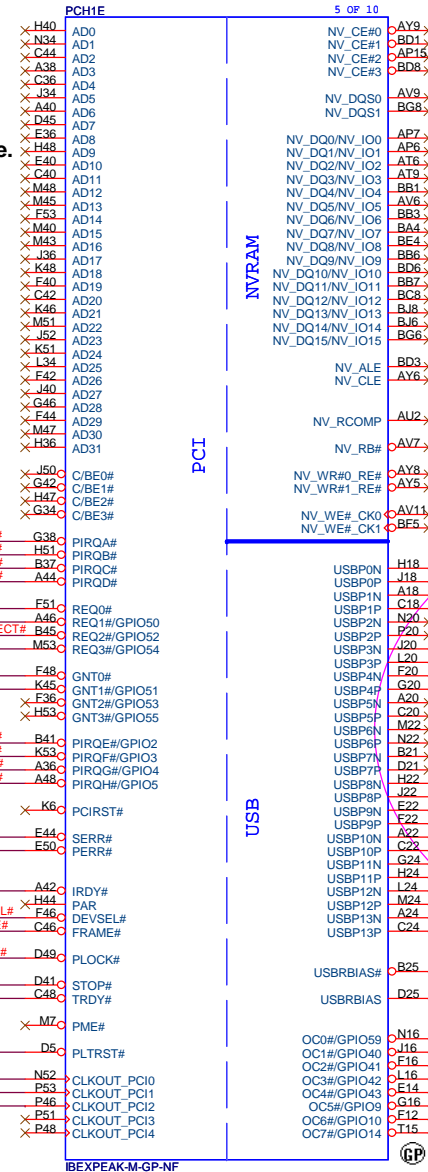
These pins are left as NC,
because the function is disable.



BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI



DVT
20100210

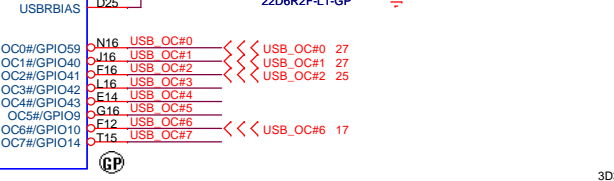


These pins are left as NC,
because the function is disable.

USB Table

Pair	Device
0	External #0
1	External #1
2	NC
3	EXPRESS CARD
4	External #2
5	NC
6	NC
7	NC
8	WIMAX(HS)
9	CAMERA(HS)
10	WWAN(HS)
11	FELICA(FS)
12	BLUETOOTH(FS)
13	MULTIMEDIA SIM(FS)

EVT
20091120



Squire CP DIS SAMSUNG

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title PCH 5 of 9(PCI/USB)

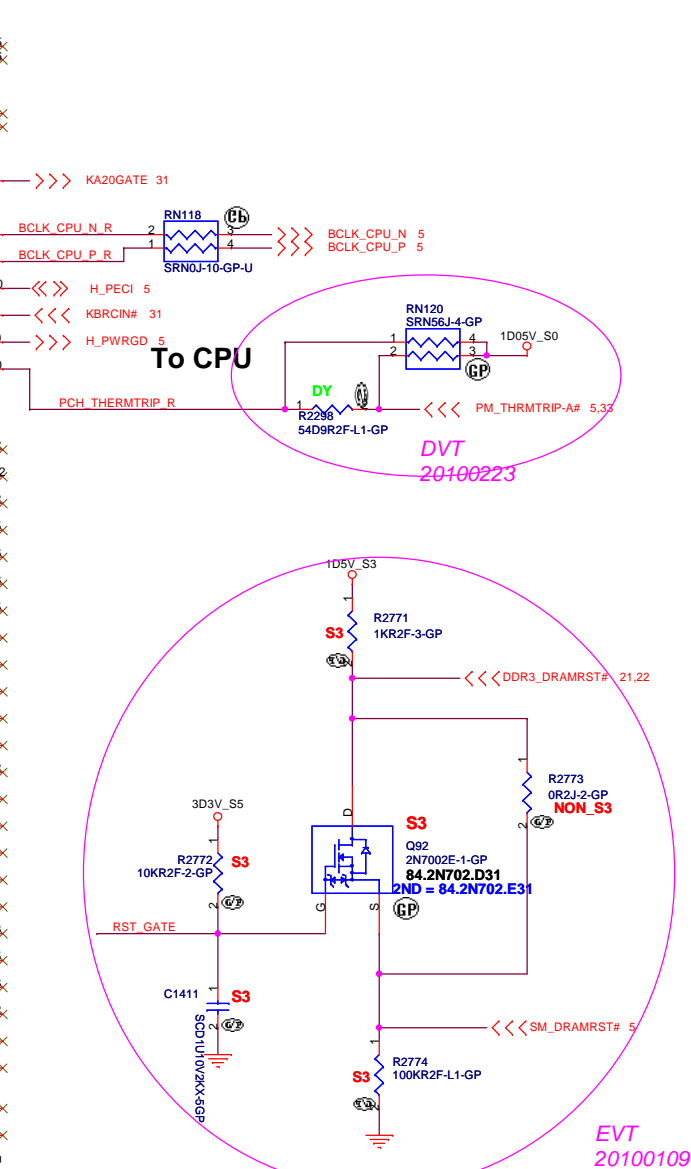
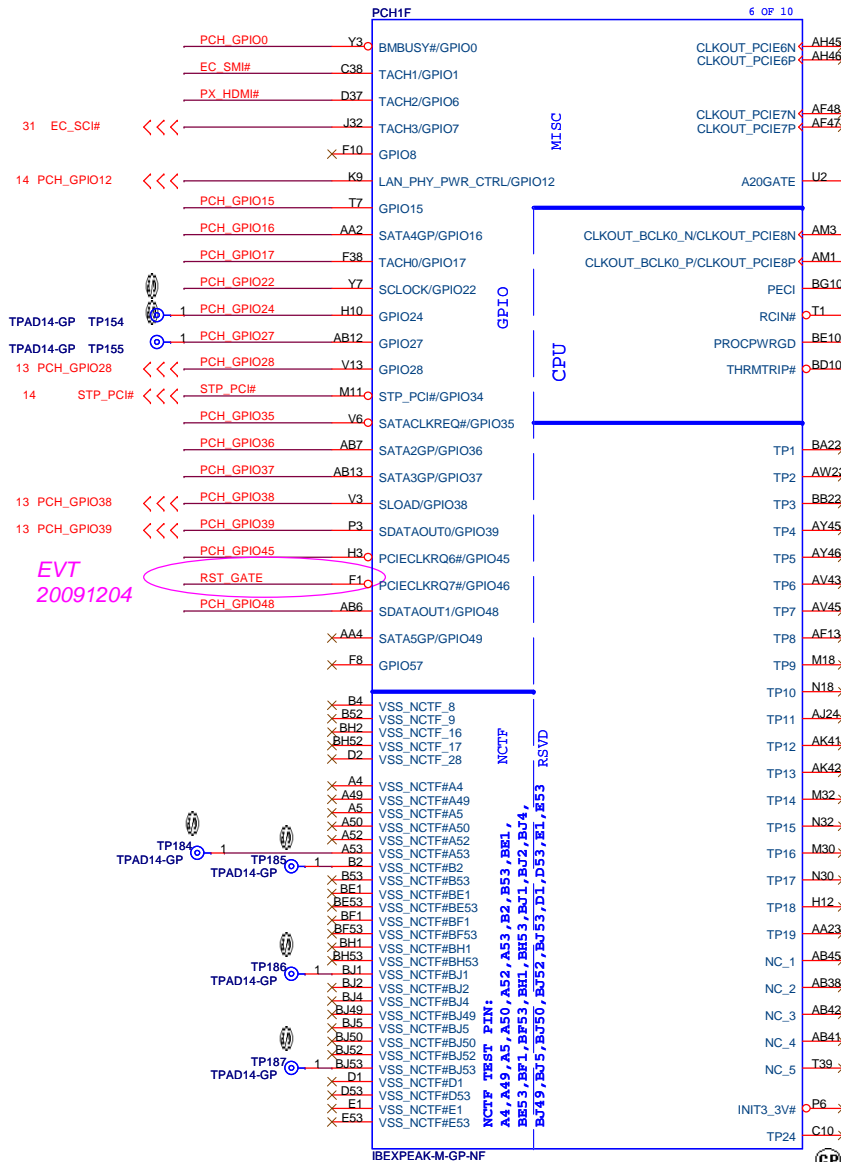
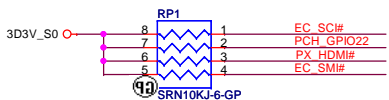
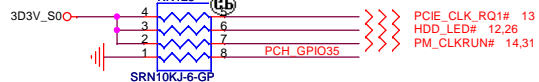
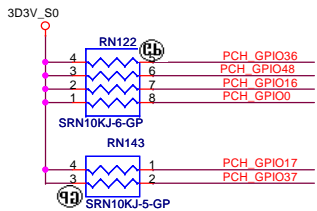
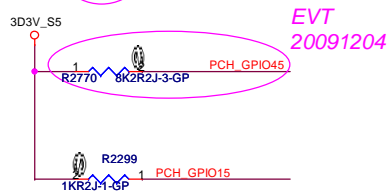
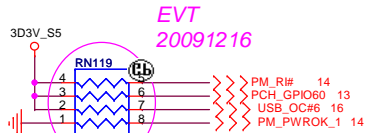
Size A3 Document Number CADIZ-CP Rev -1M

Date: Saturday, April 24, 2010 Sheet 16 of 57

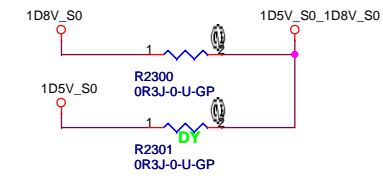
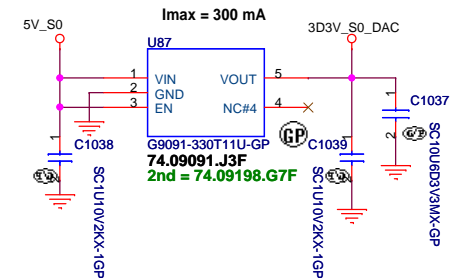
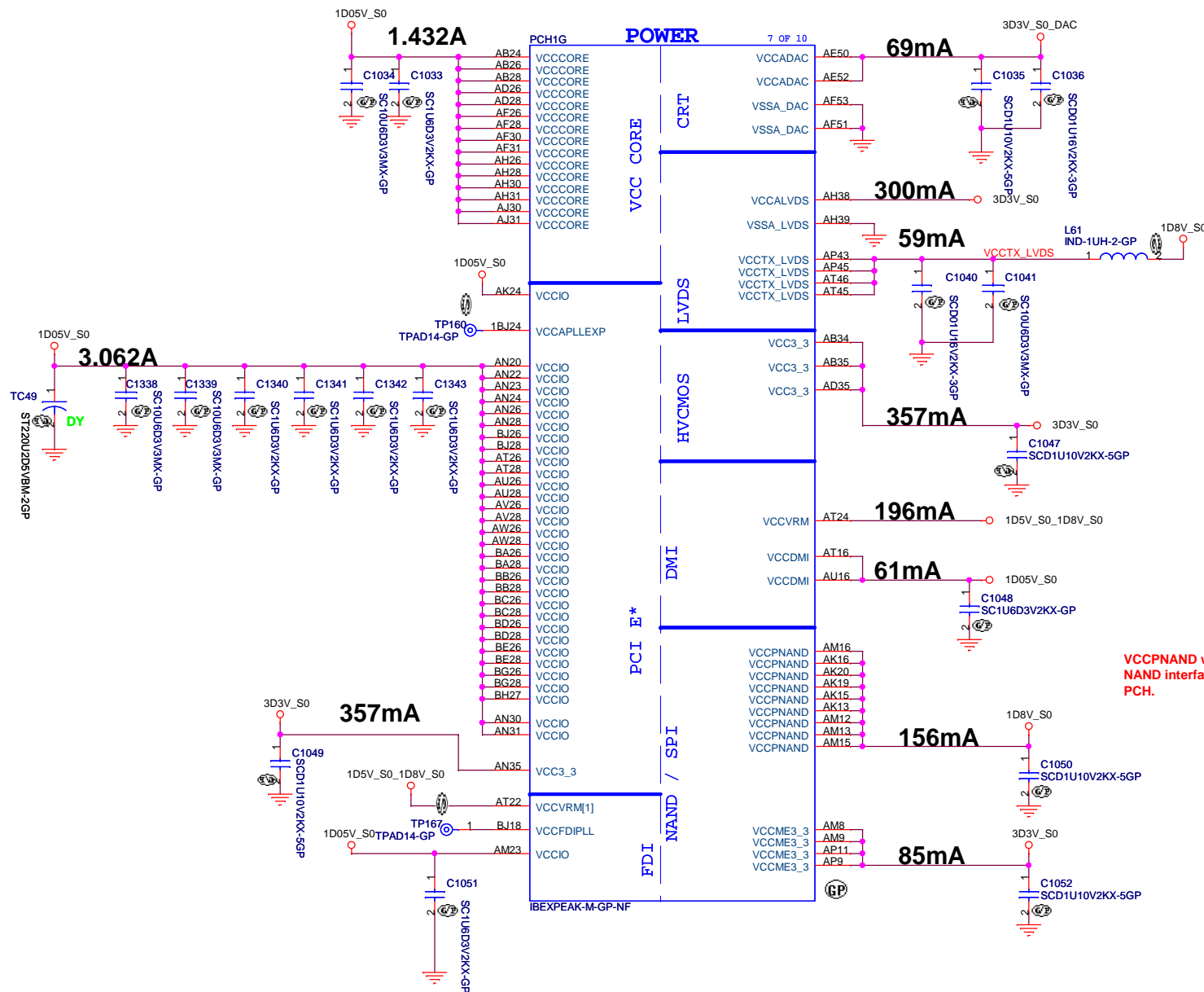
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



Squirrel CP DIS SAMSUNG

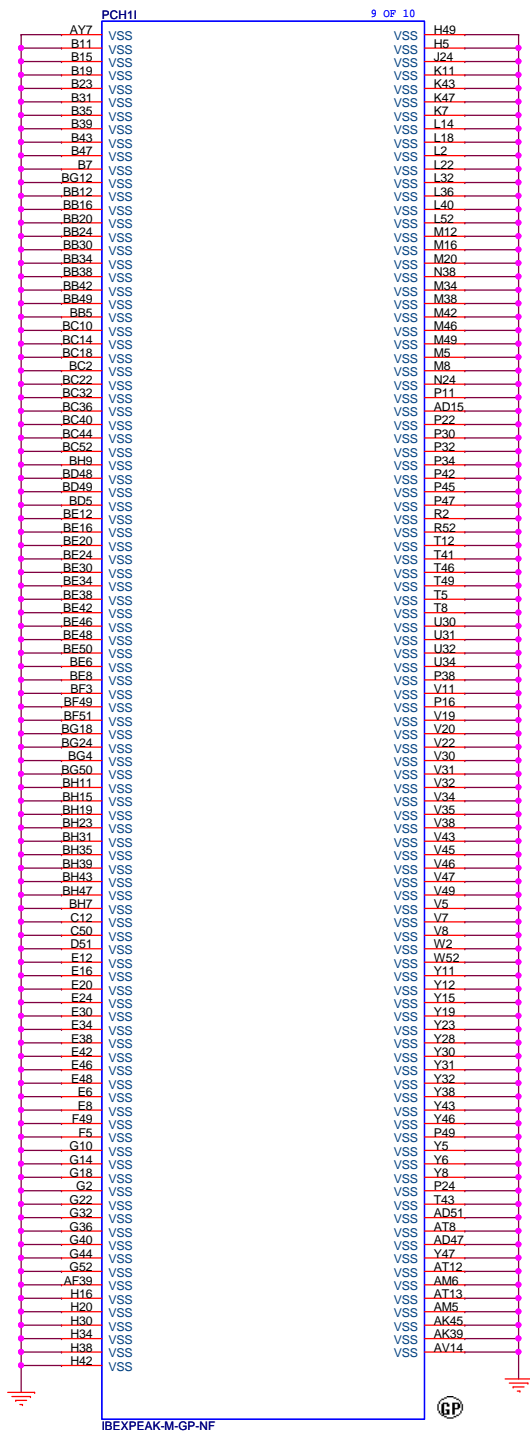


VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

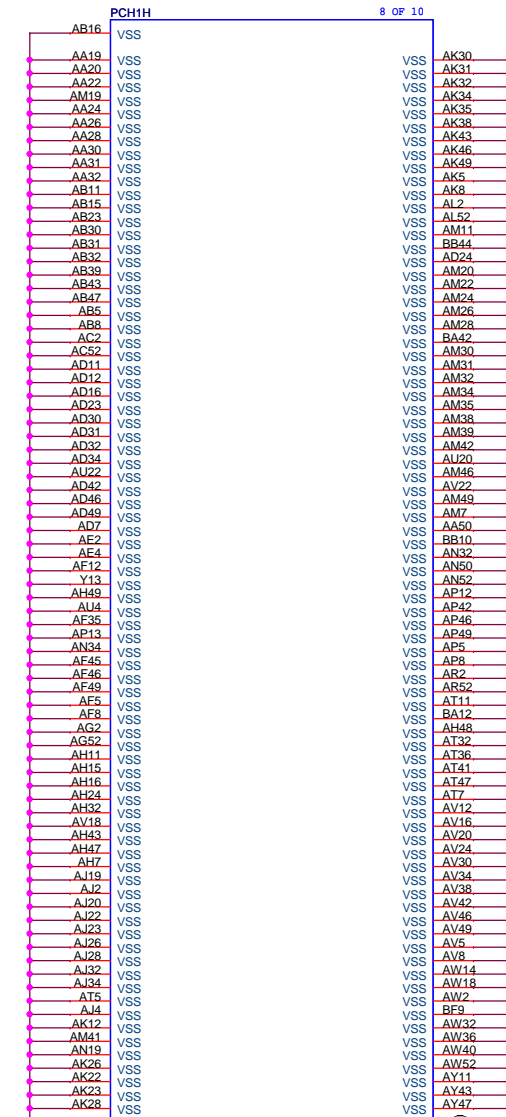
Squirtle CP DIS SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

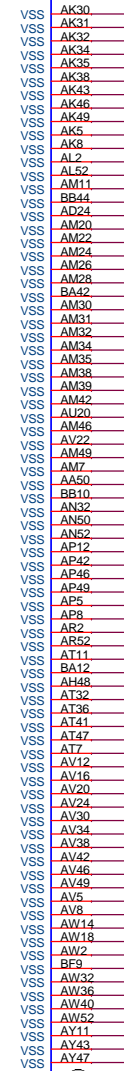
Title			PCH 7 of 9(PWR/VCORE/LVDS)
Size	Document Number	Rev	
Custom	CADIZ-CP	-1M	
Date:	Saturday, April 24, 2010	Sheet	18 of 57



IBEXPEAK-M-GP-NF

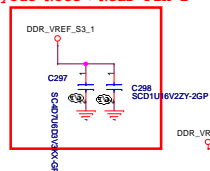


IBEXPEAK-M-GP-NF

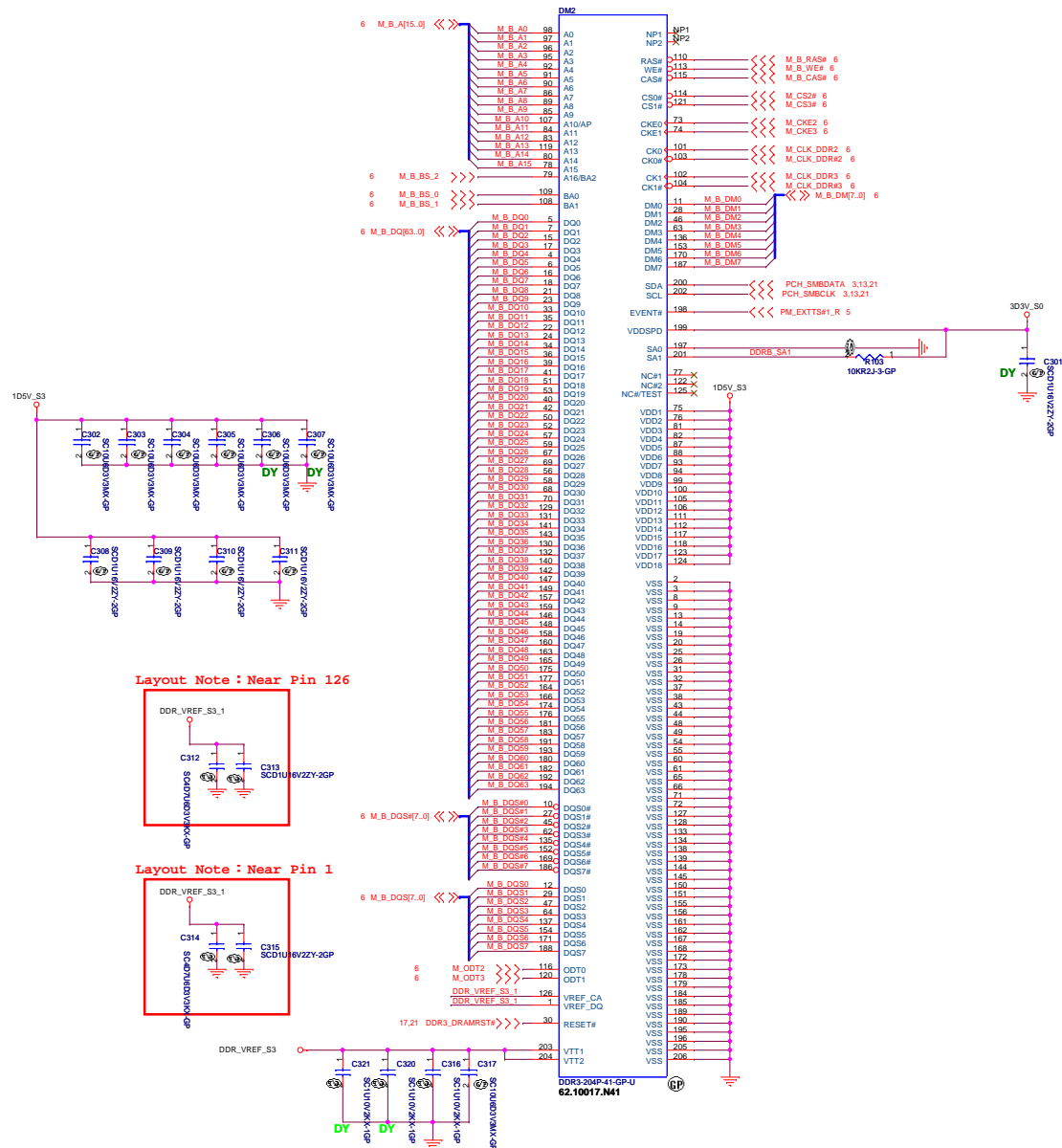


Squire CP DIS SAMSUNG

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title PCH 9 of 9(VSS)			
Size A3	Document Number CADIZ-CP	Rev -1M	
Date: Saturday, April 24, 2010	Sheet 20 of 57		



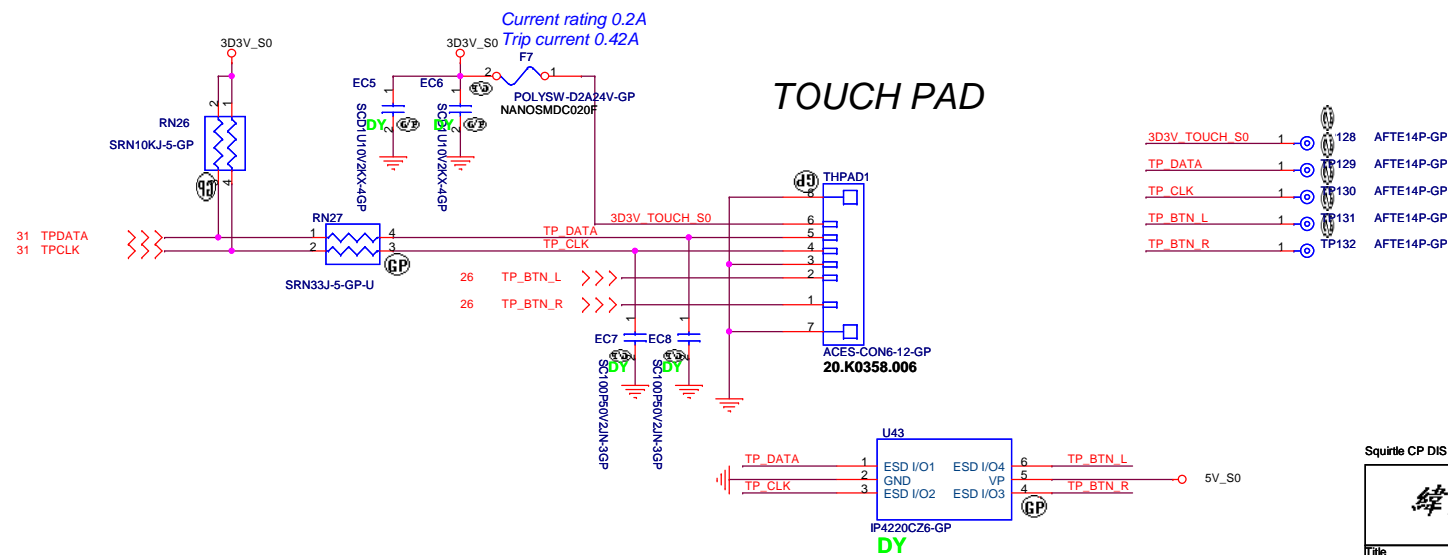
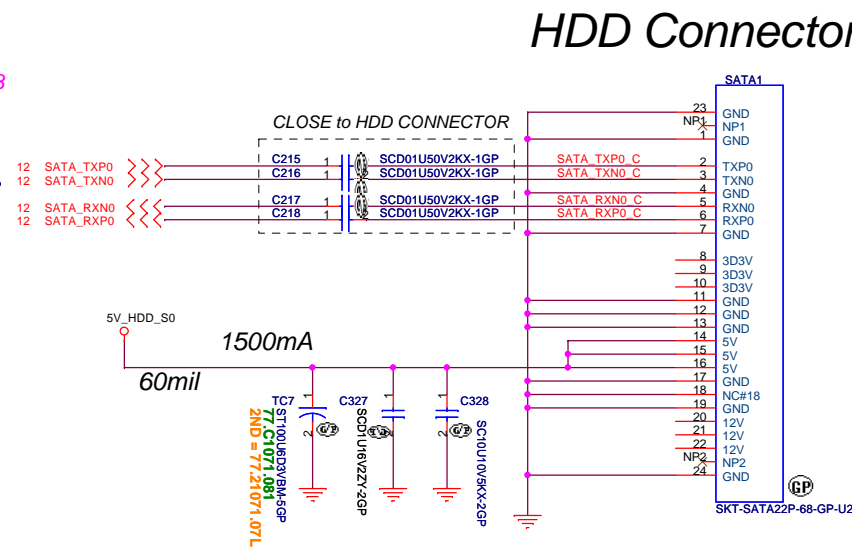
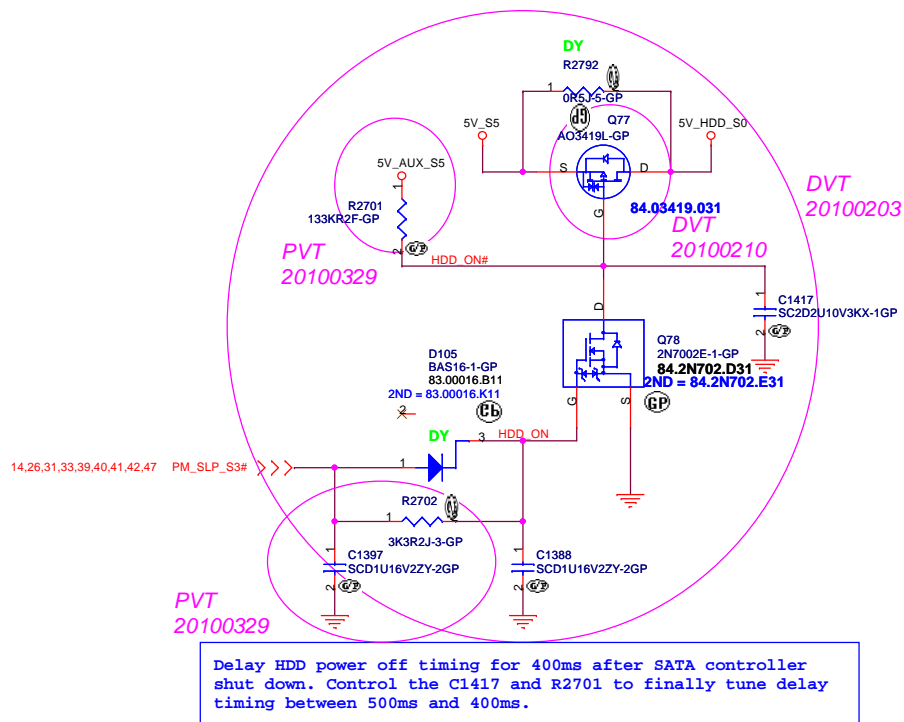
DDR3 SOCKET_2



1



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USB4: EXTERNAL #2

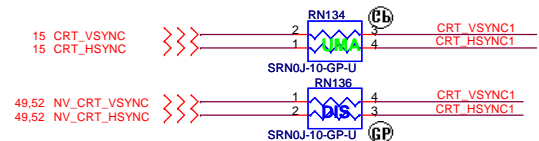
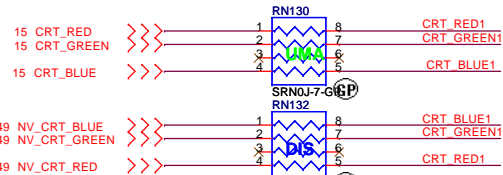
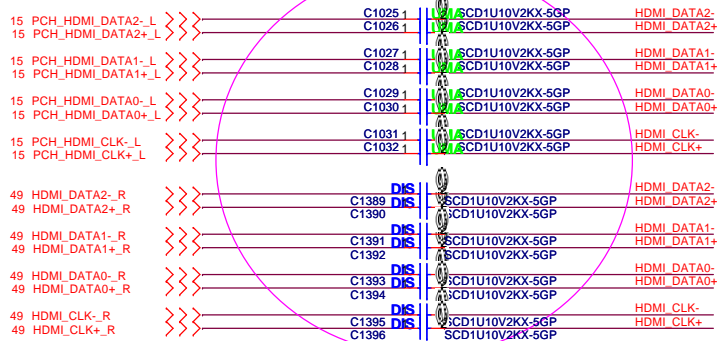
16 USBPP4
16 USBPN4

HDMI CLK-
HDMI CLK+
HDMI DATA0-
HDMI DATA0+
HDMI DATA1-
HDMI DATA1+
HDMI DATA2-
HDMI DATA2+

CRT_VSYNC1
CRT_HSYNC1
CRT_BLUE1
CRT_GREEN1
CRT_RED1

EVT
20091125

HDMI Caps near BTBCRT1



BTBCRT1

NP1

NP2

FOX CONN60A-6-GP-U

20.F0940.060

3D3V_S0

CORE_PWRGD 14,36

5V CRT_SS

5V_S0

EC11

SC33P50V2JN-3GP

USB_PWR_EN# 27,31

USB_OC#2 16

HDMI_DETECT

HDMI_CLK

HDMI_DATA

CRT_DDCCLK1

CRT_DDCDATA1

PolySwitch
mihiSMD260F

F4

FUSE-ZD6A6V-3GP

69.50007.881

2ND = 69.42601.001

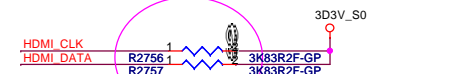
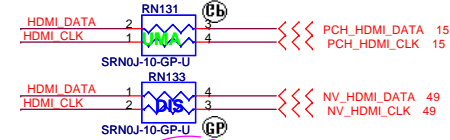
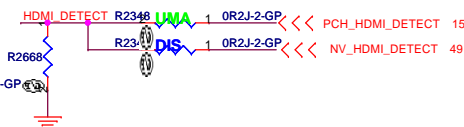
5V_S5

C495

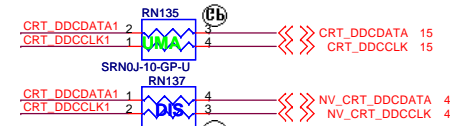
SC4D7U10V3KX-GP

C494

SC31U16V2ZV-2GP



EVT
20091202



EVT
20091202

Squirrel CP DIS SAMSUNG

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT BD CONN

Size

Document Number

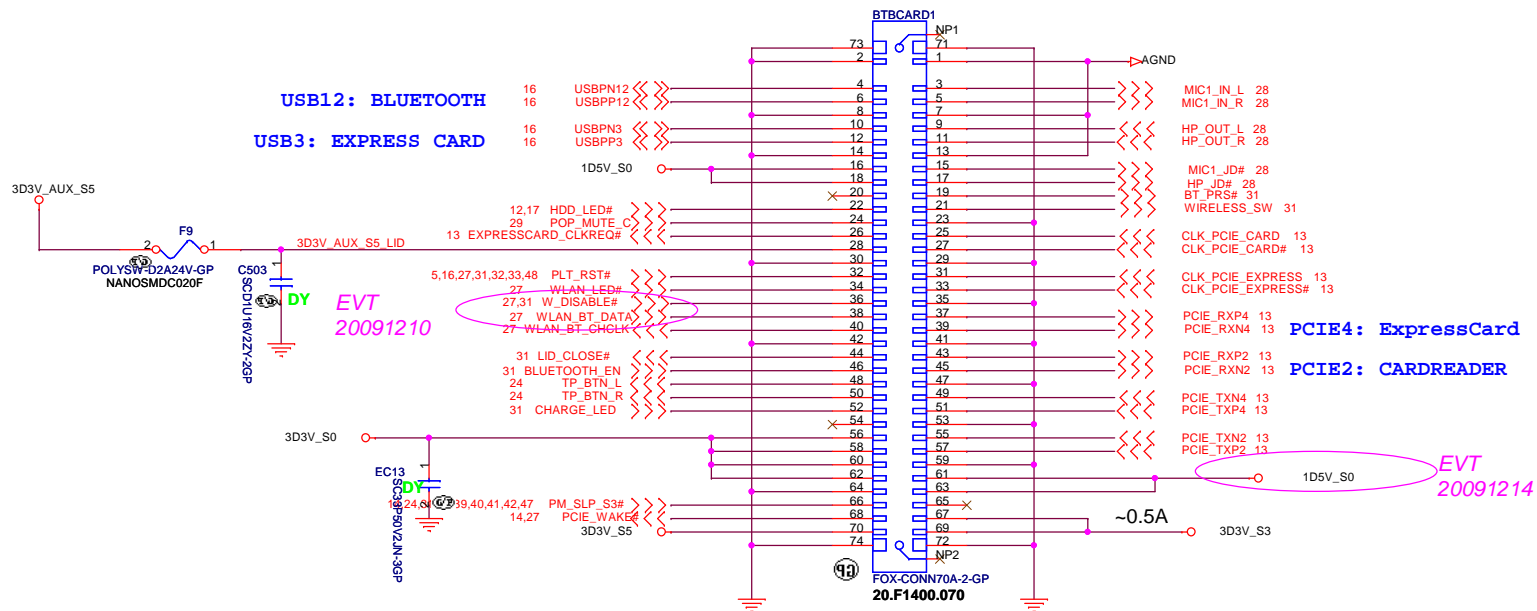
CADIZ-CP

Rev

-1M

Date: Saturday, April 24, 2010

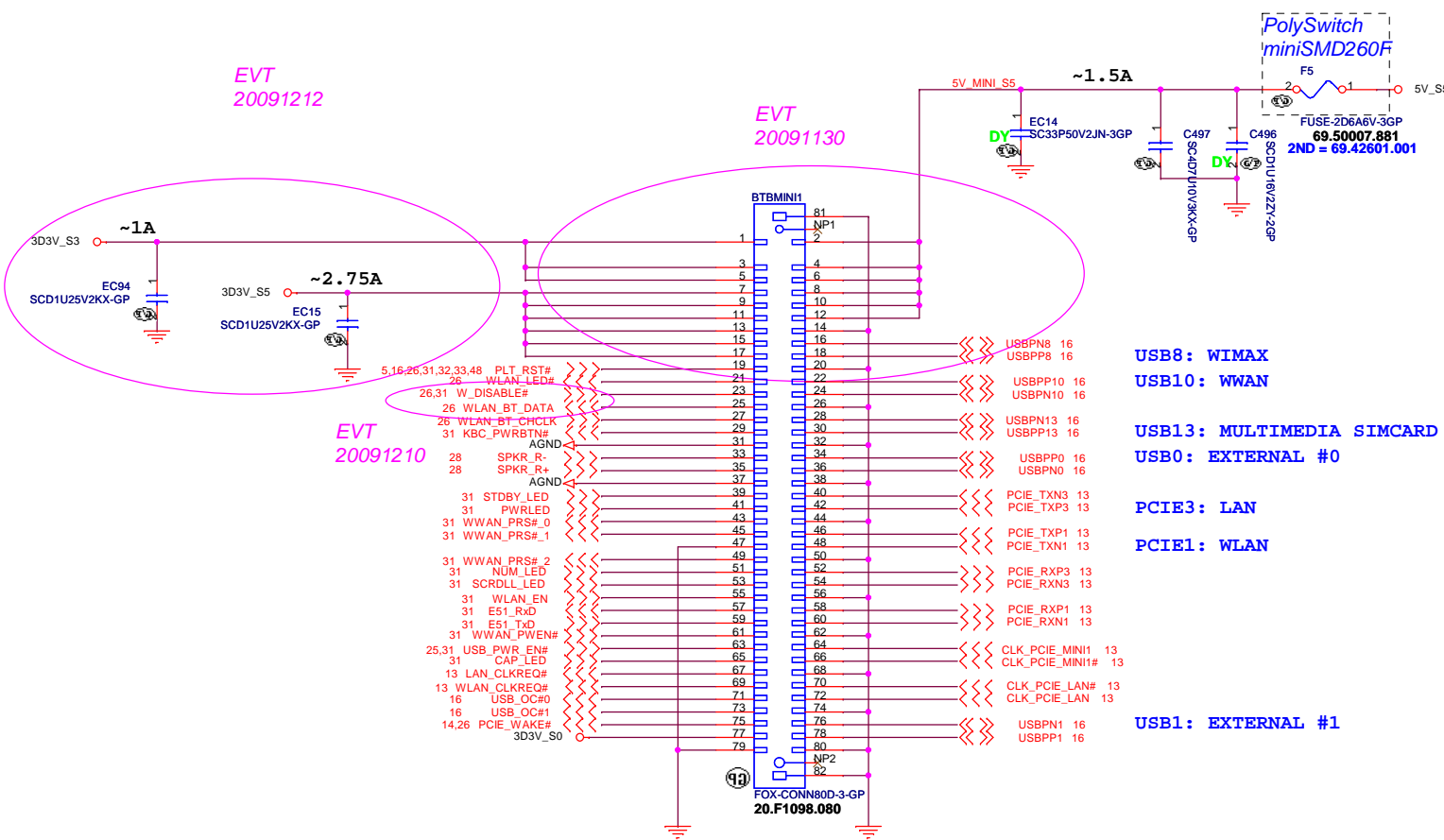
Sheet 25 of 57



Squirrel CP DIS SAMSUNG

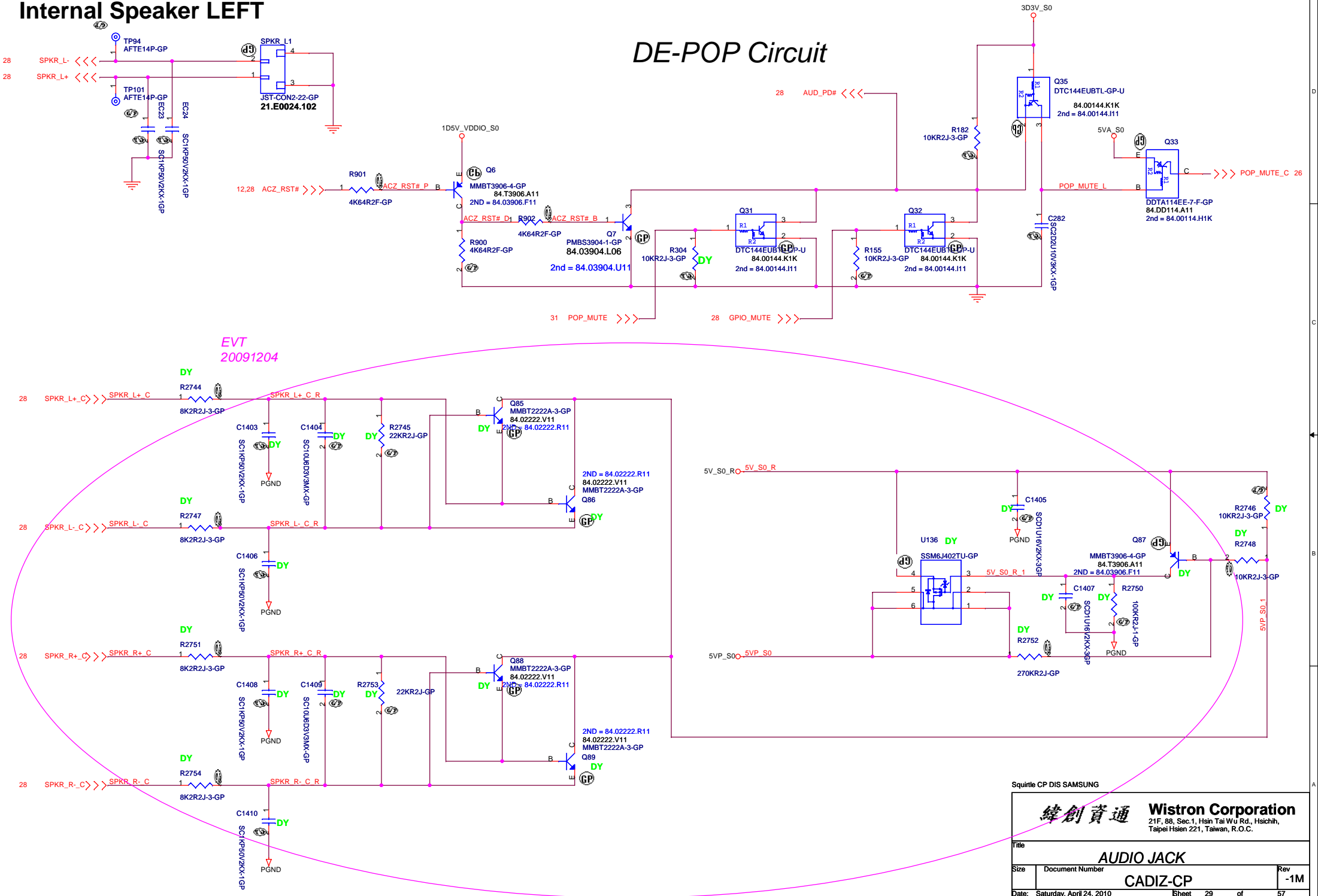
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CARDREADER BD CONN
Size	Document Number	Rev	
		CADIZ-CP	
Date: Saturday, April 24, 2010	Sheet	26	of 57

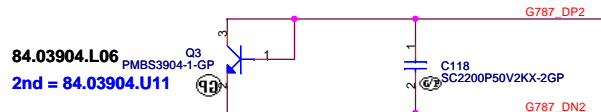


Internal Speaker LEFT

DE-POP Circuit

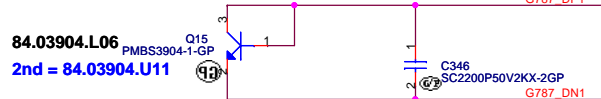


for T8 thermal diode

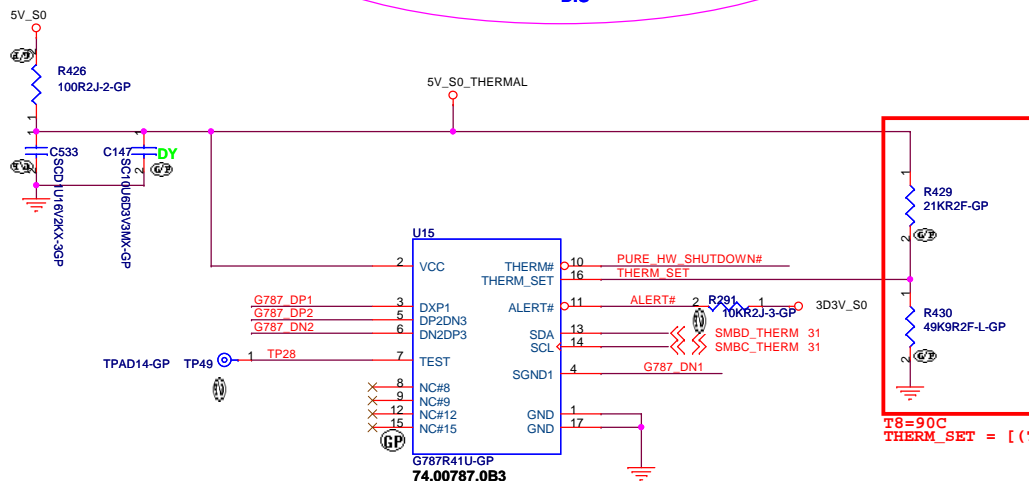
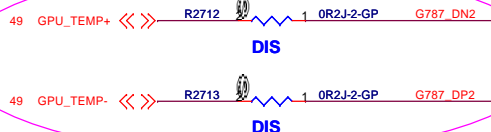


C1252 & C1254 CLOSE TO G787

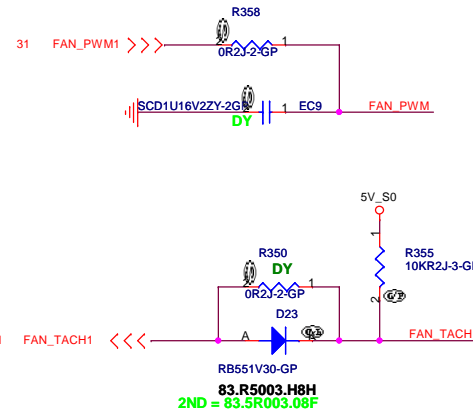
for system thermal diode



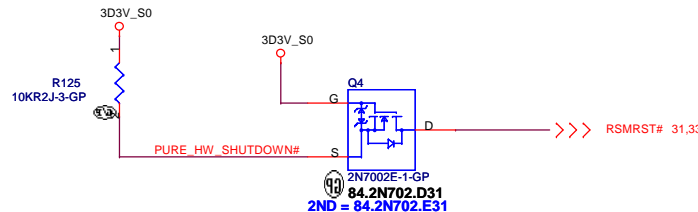
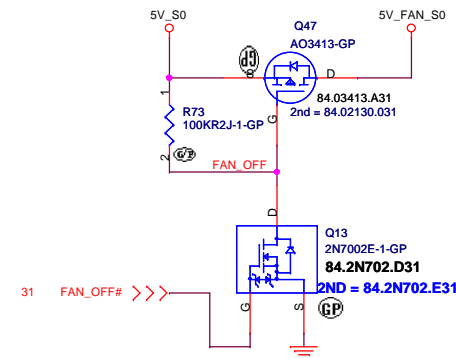
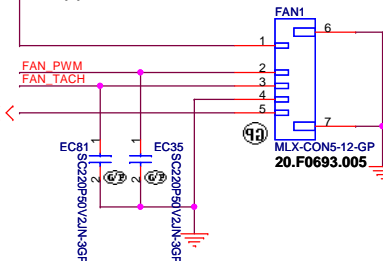
EVT
20091201



T8=90C
THERM_SET = [(Tset-72) x 0.02+0.34] x VCC



ps. FAN1 POWER TRACE WIDTH ~15 MIL
Max current is 235mA;
Stopped is ~10mA

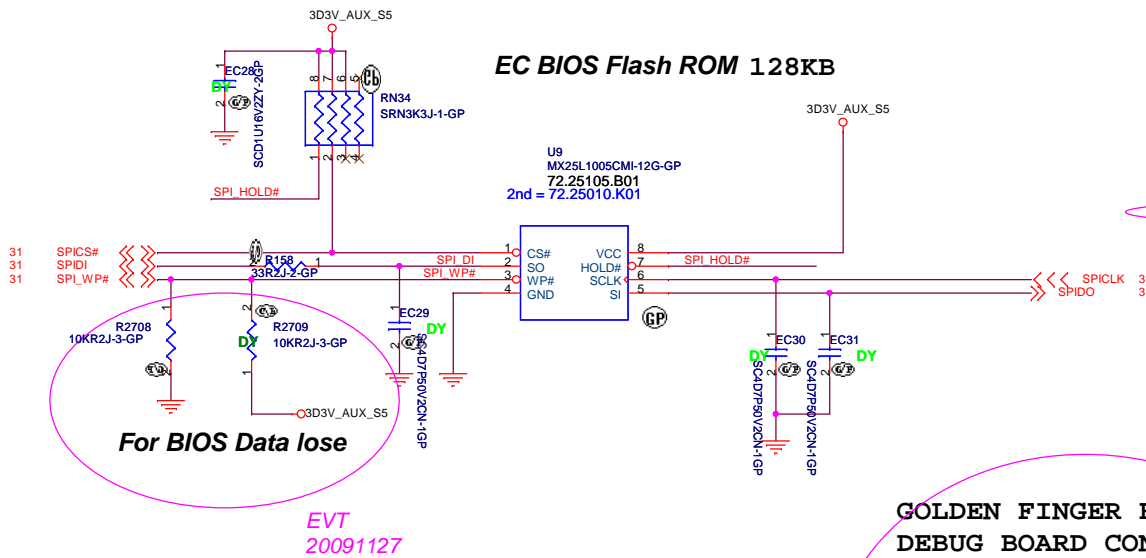


Squirrel CP DIS SAMSUNG

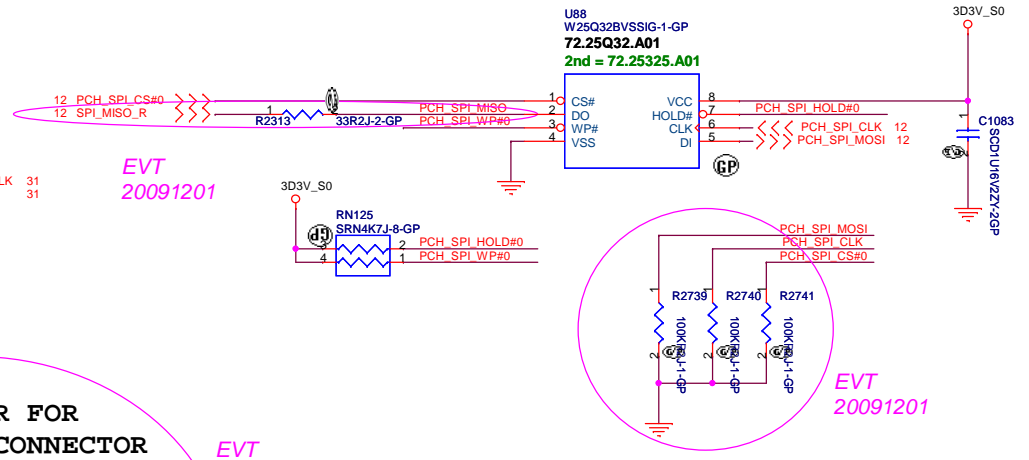
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
Thermal/Fan Controllor			
Size	Document Number		Rev
CADIZ-CP		-1M	
Date:	Saturday, April 24, 2010	Sheet 30 of 57	

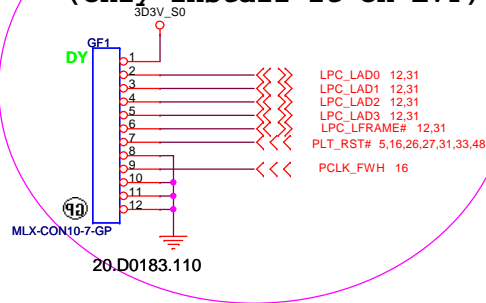
EC BIOS Flash ROM 128KB



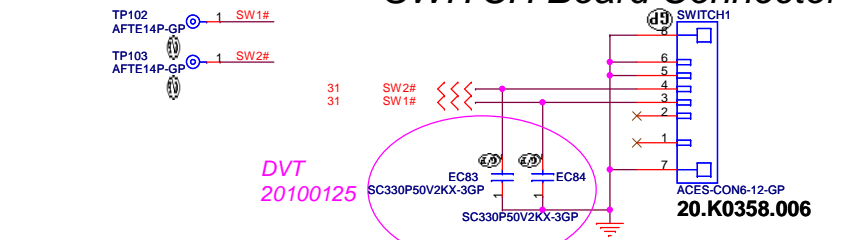
System BIOS Flash ROM (4MB)



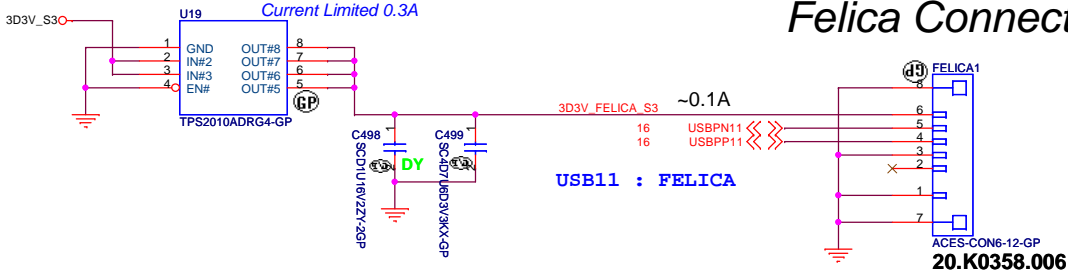
GOLDEN FINGER FOR DEBUG BOARD CONNECTOR (only install it on EVT)



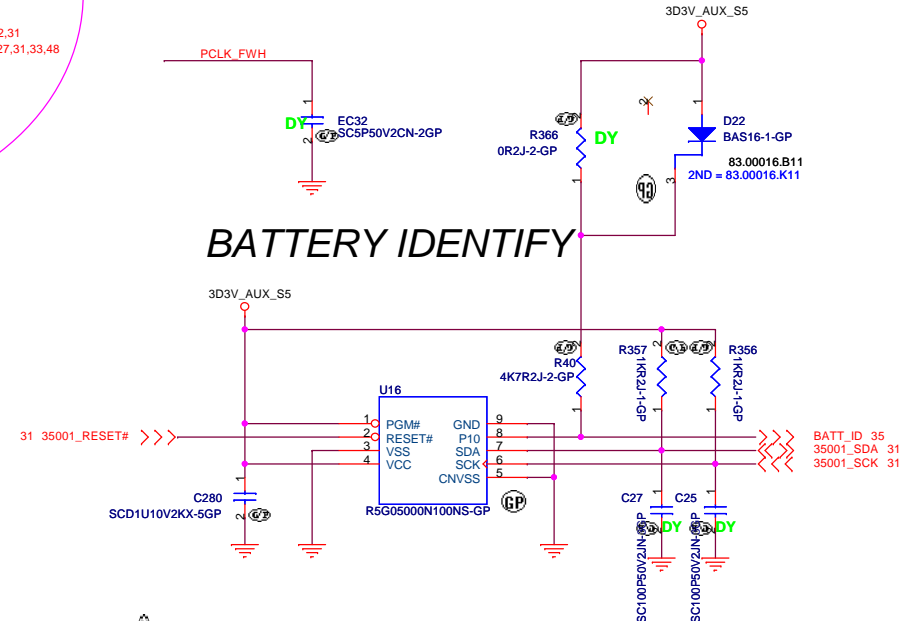
SWITCH Board Connector



Felica Connector



BATTERY IDENTIFY



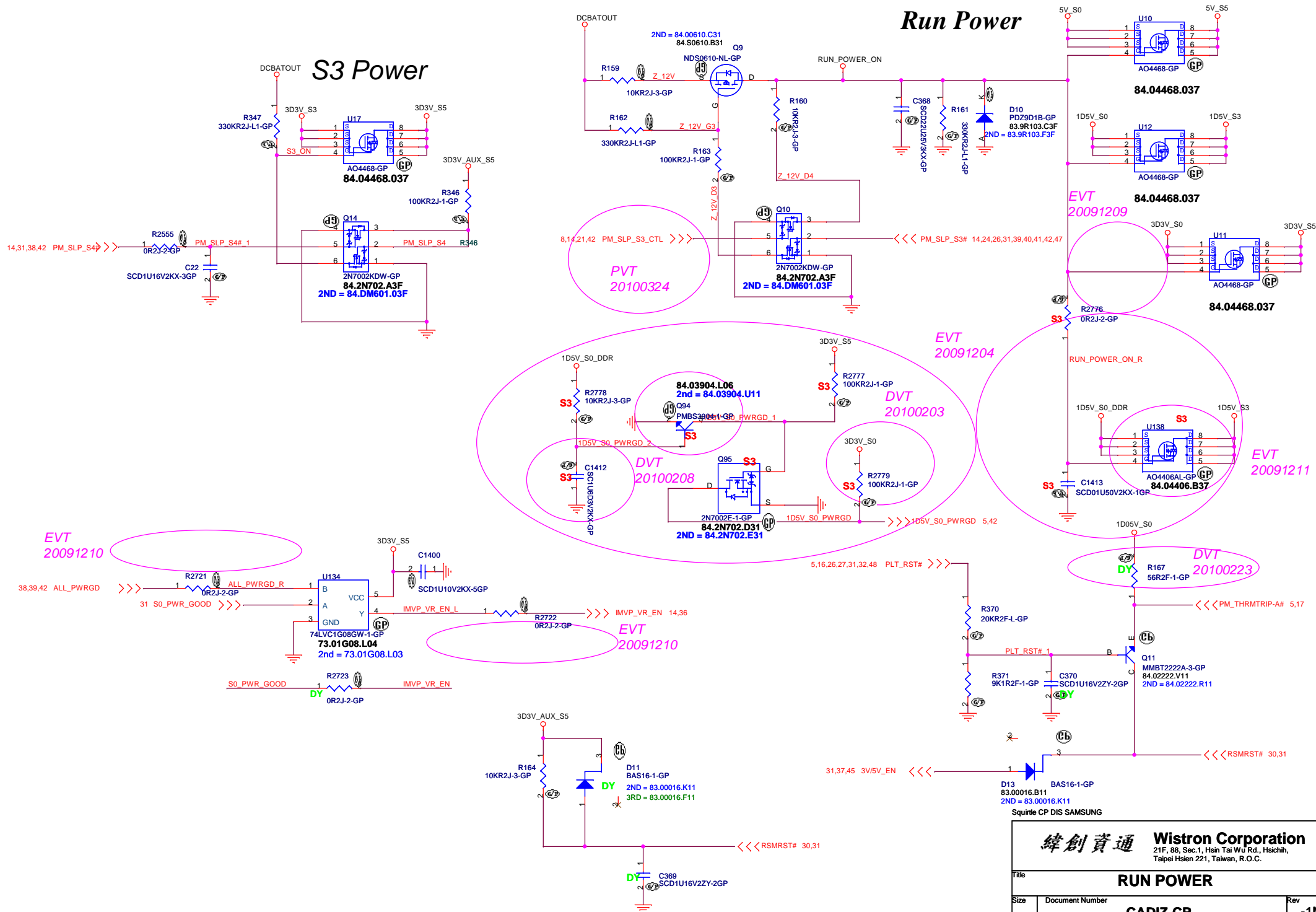
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

BIOS & SW/C & BAT ID & Felica

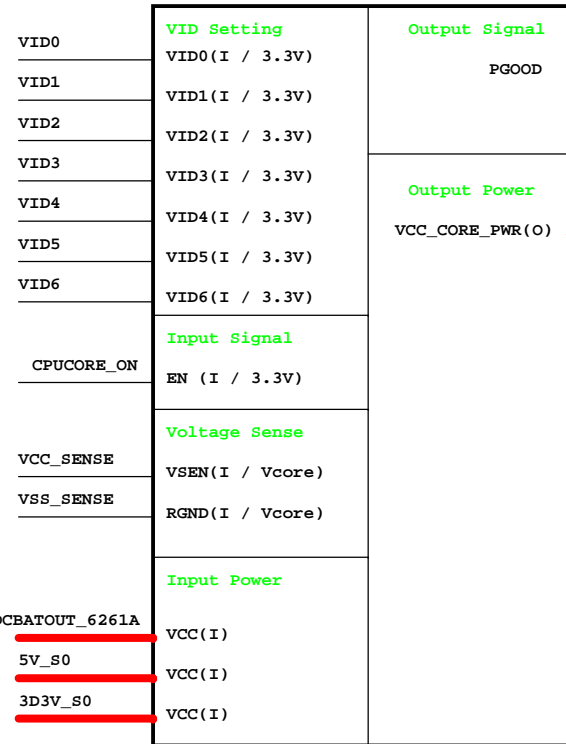
CADIZ-CP

Rev -1M

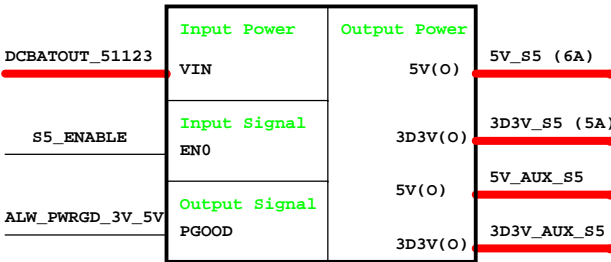
Date: Saturday, April 24, 2010 Sheet 32 of 57



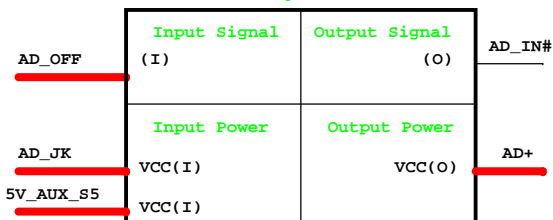
CPU_CORE ADP3211



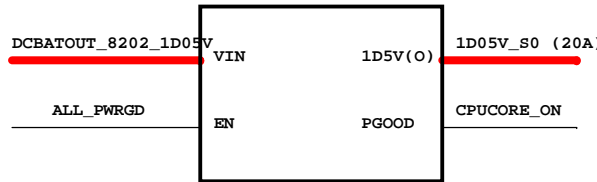
5V/3D3V RT8223



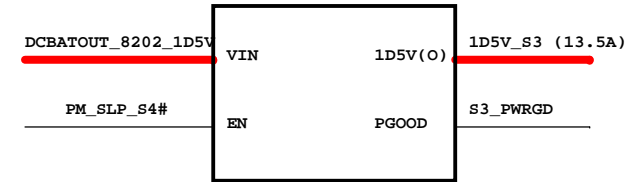
Adapter



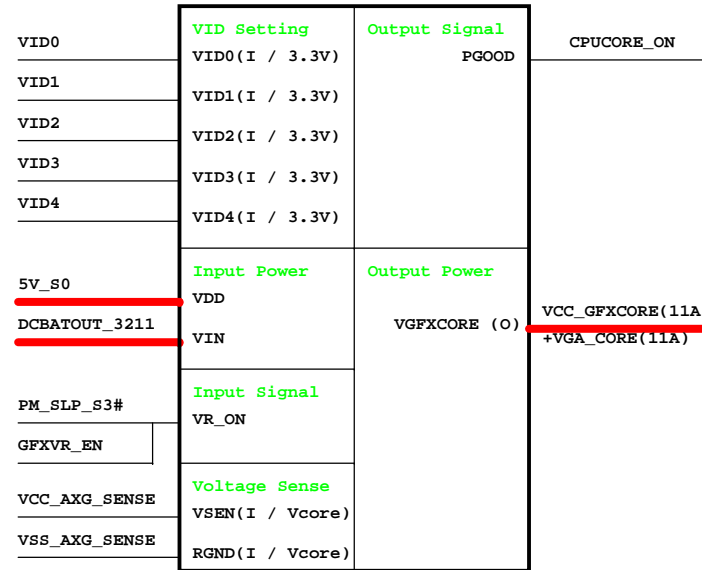
RT8209 1D05V_S0



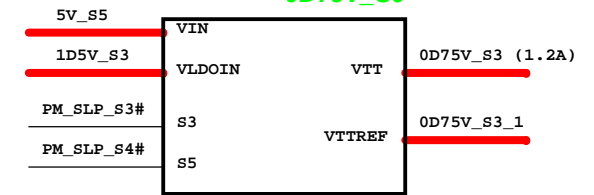
RT8209 1D5V_S3



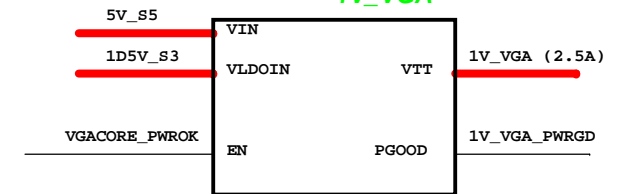
GFX_CORE/ VGA_CORE ADP3211



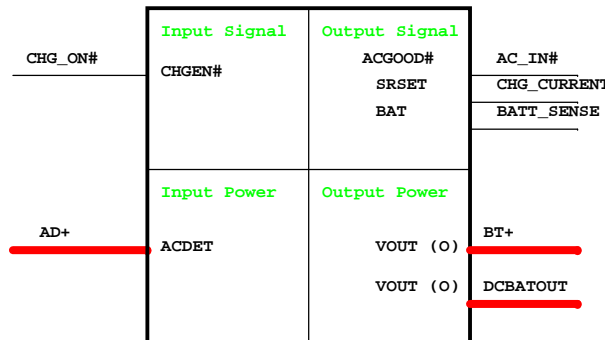
RT9026 0D75V_S0



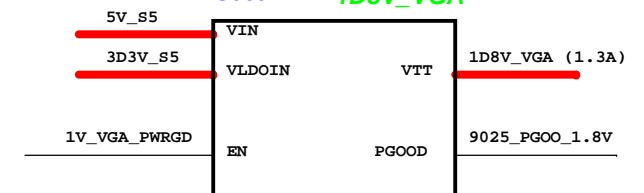
APL5930 1V_VGA



Charger BQ24751



G9661 1D8V_VGA



Squirtle CP DIS SAMSUNG

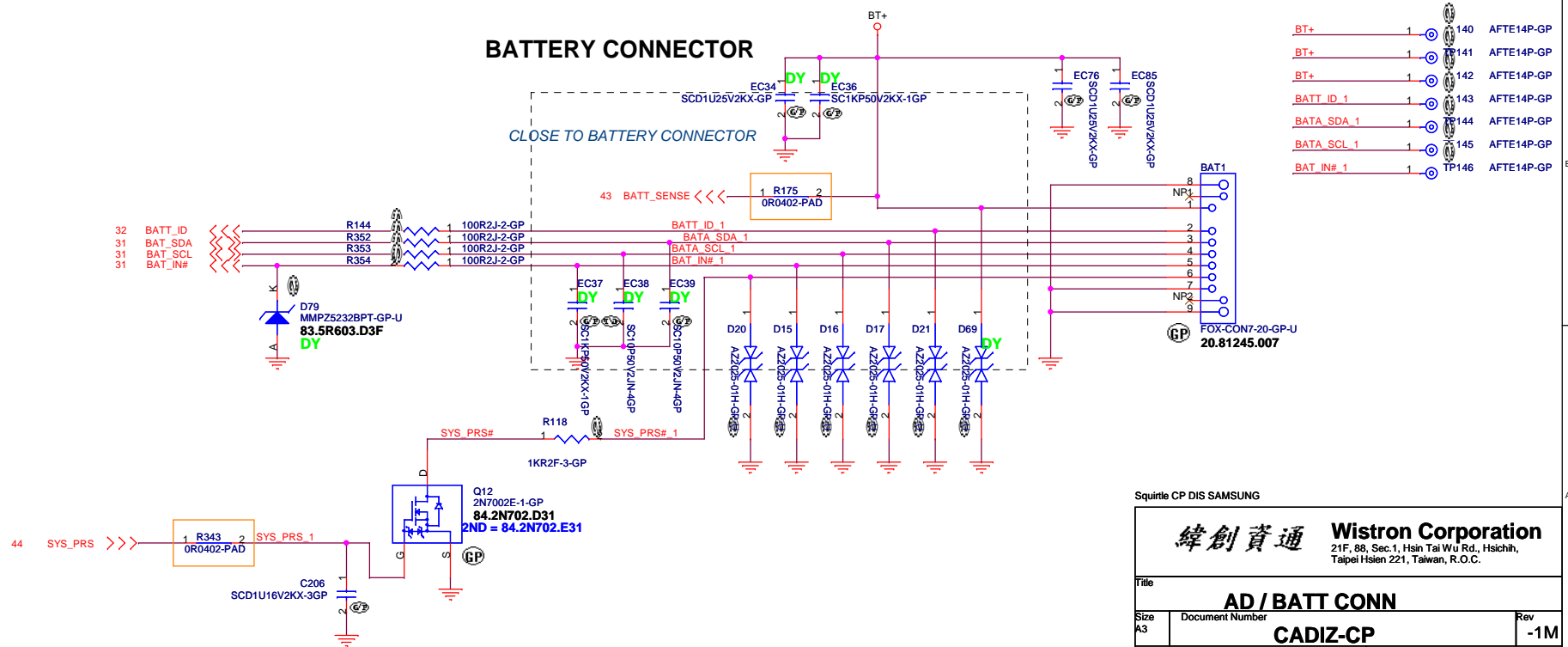
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

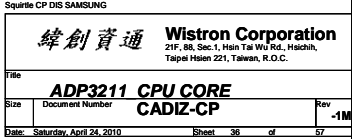
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Size	Document Number	CADIZ-CP		Rev
A3				-1M
Date:	Saturday, April 24, 2010	Sheet	34	of 57

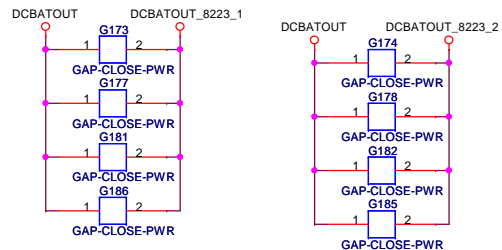
The schematic shows the AD+ input signal path. It includes three test points (TP77, TP69, TP70) connected to the AFTE14P-GP module. The signal passes through a series of components: a capacitor C33 (SCD1U25V2KX-GP), a capacitor C371 (SCD1U25V2KX-GP), and a diode D14 (PS8BMJ2APT-GP). The final output is labeled AD+. Ground symbols are shown at various points along the signal path.

SCD1U25V2KX

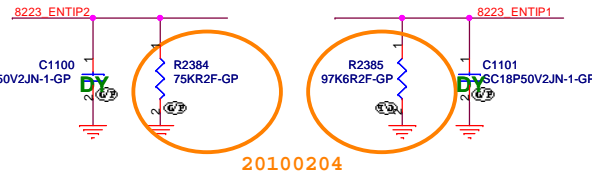
CLOSE TO BATTERY CONNECTOR



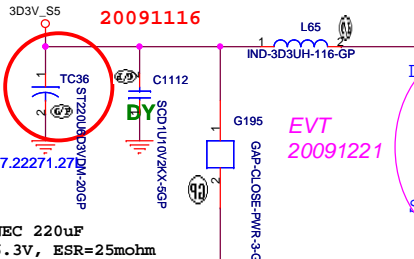
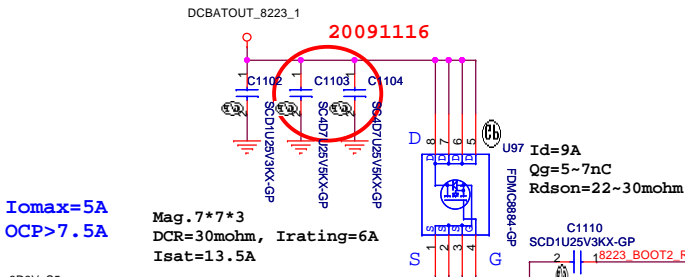
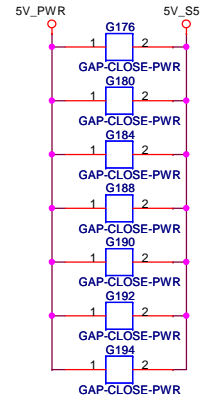




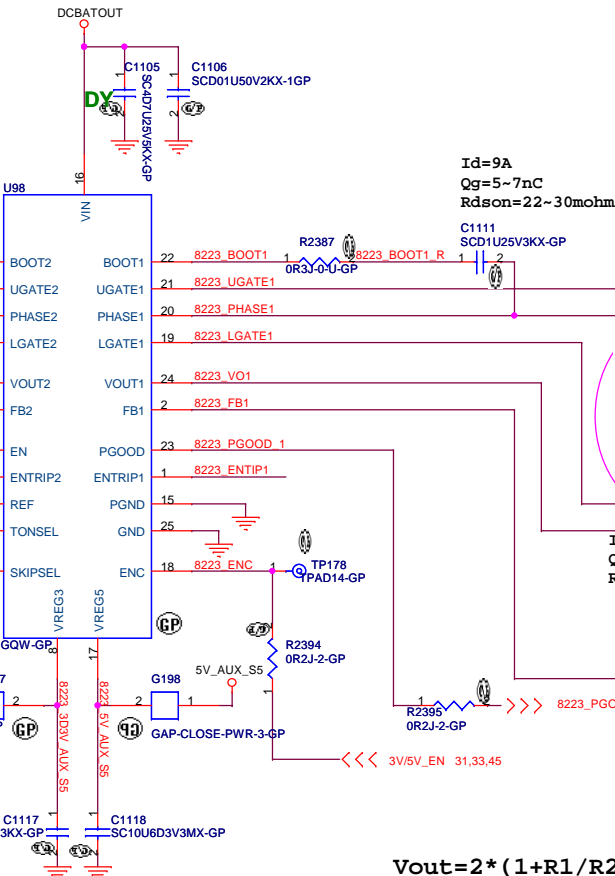
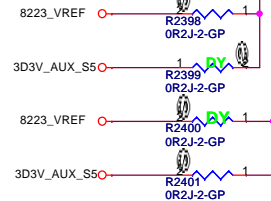
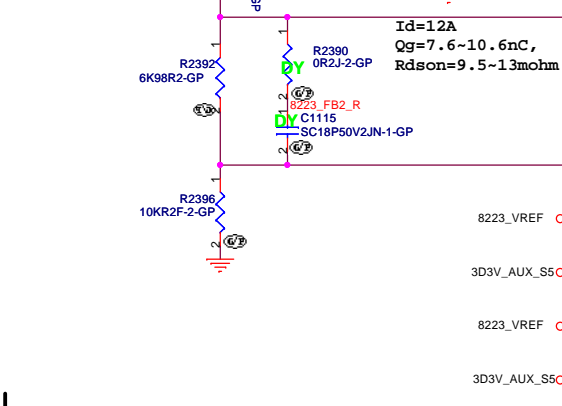
EVT
20091202



20100204



EVT
20091221



$$V_{out} = 2 * (1 + R1/R2)$$

	8223_REF	3D3V_AUX_S5
SKIPSEL	PWM	00A AUTOSKIP
TONSEL	245k/CH1 305k/CH2	300k/CH1 375k/CH2

Squirrel CP DIS SAMSUNG

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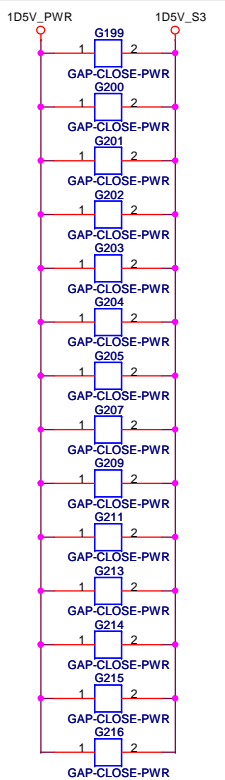
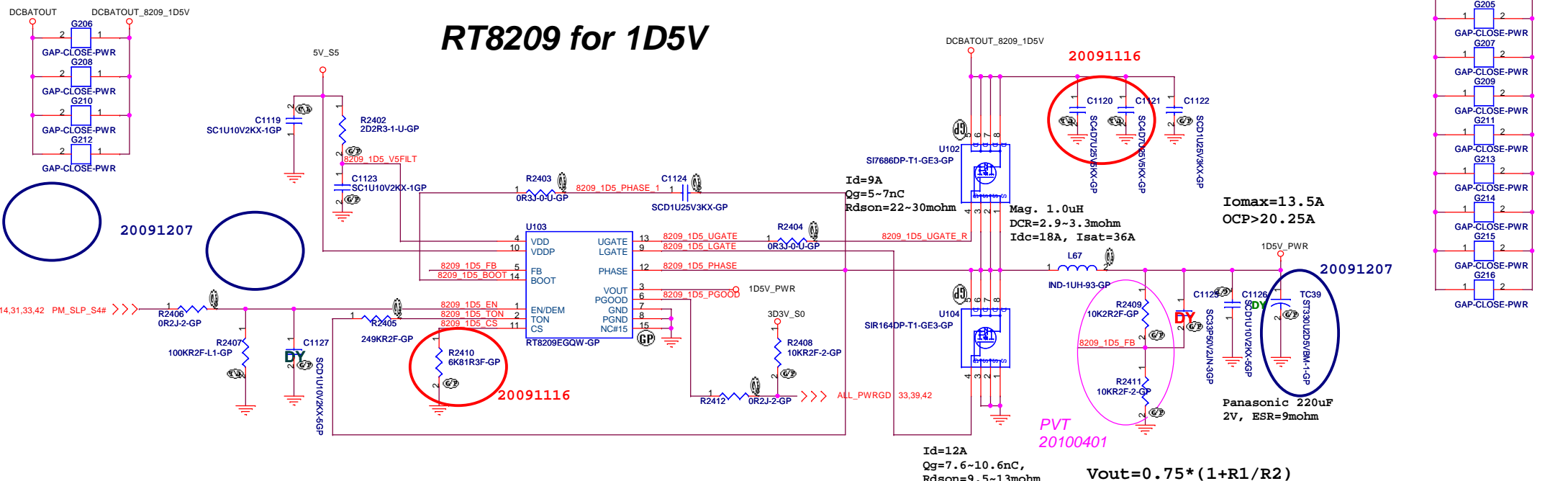
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Size: Document Number

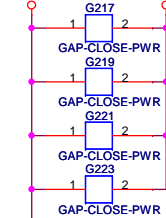
Date: Saturday, April 24, 2010

Sheet 37 of 57

Rev -1M

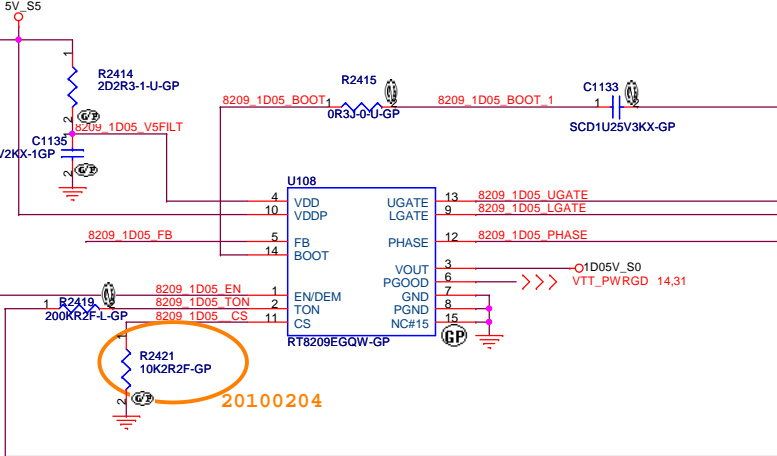


DCBATOUT DCBATOUT_RT8209_1D05V



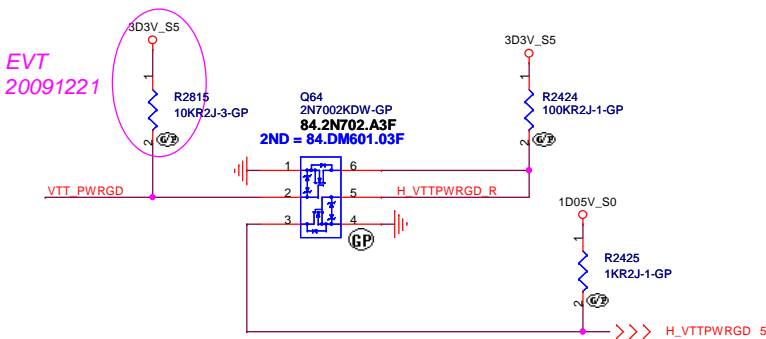
EVT
20091214

RT8209 1D05V



20100204

EVT
20091221



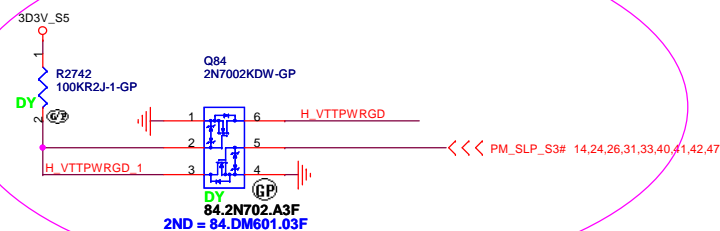
20091207

Id=9A
Qg=5~7nC
Rdson=22~30mohm

Id=12A
Qg=7.6~10.6nC,
Rdson=9.5~13mohm

EVT
20091201

The processor needs to be warned about the VTT rails shutdown at least 100 ns before the VTT rail falls to -5% of nominal value.



20091116

Mag. 1.0uH
DCR=2.9~3.3mohm
Idc=18A, Isat=36A

Vout=0.75*(1+R1/R2)

Iomax=20A
OCP>30A

EVT
20091204

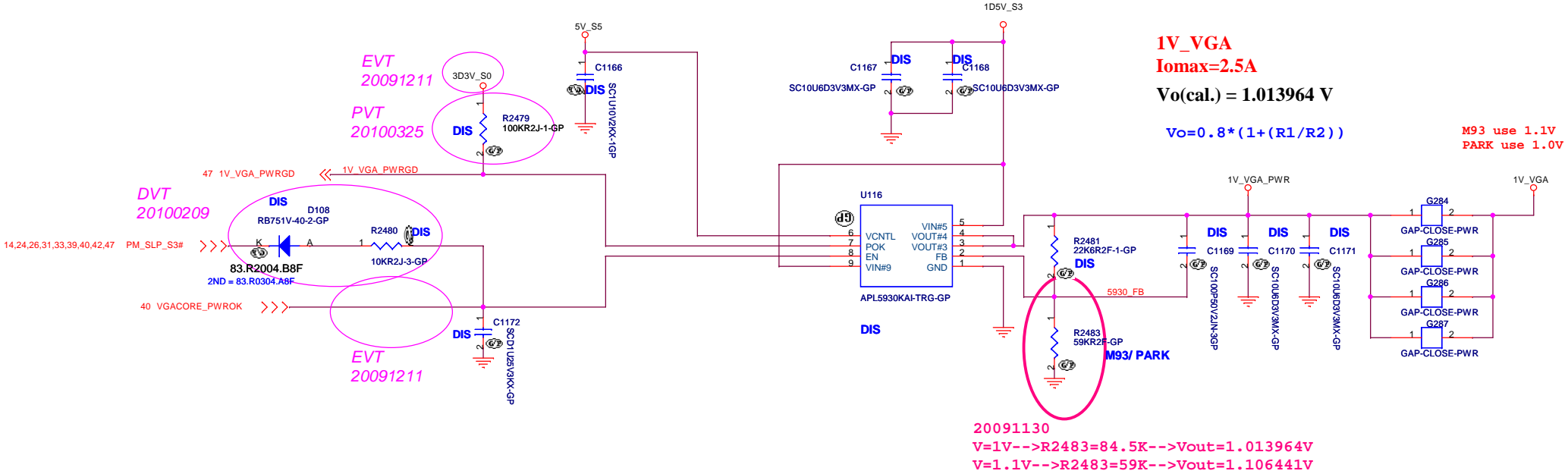
Squirrel CP DIS SAMSUNG

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Title			RT8209_1D05V
Size	Document Number	CADIZ-CP	
Date: Saturday, April 24, 2010	Sheet	39	of 57

Rev
-1M

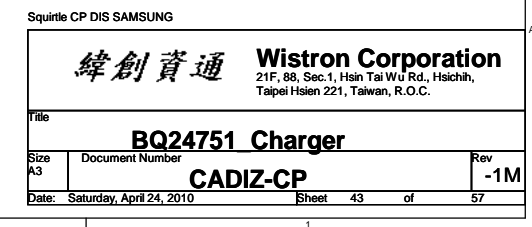
APL5930 for 1V_VGA

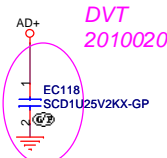
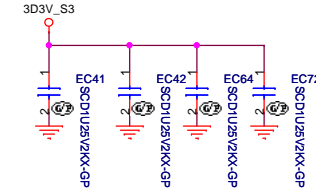
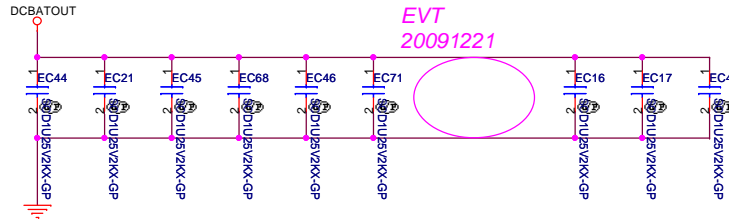
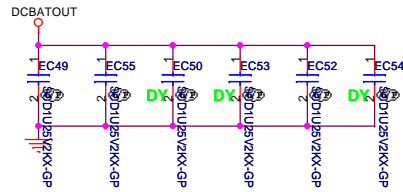


Squirrel CP DIS SAMSUNG

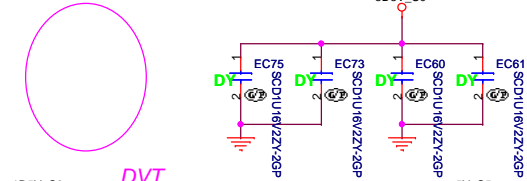
緯創資通 Wistron Corporation
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Title		
ISL62881 +VCC GFXCORE		
Size	Document Number	Rev
A3	CADIZ-CP	-1M
Date: Saturday, April 24, 2010		
Sheet 41 of 57		

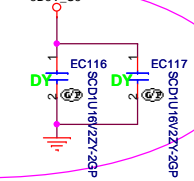
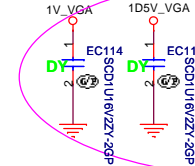
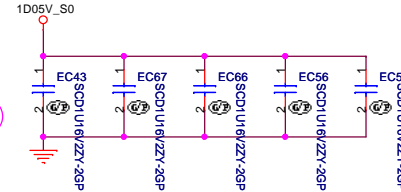
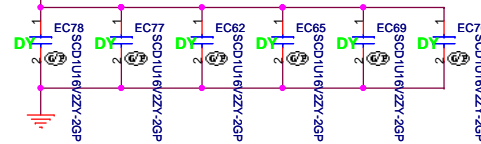




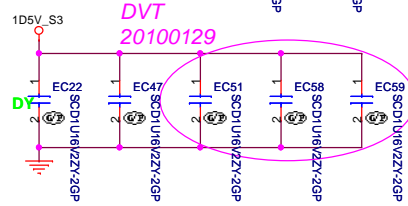
EVT
20091221



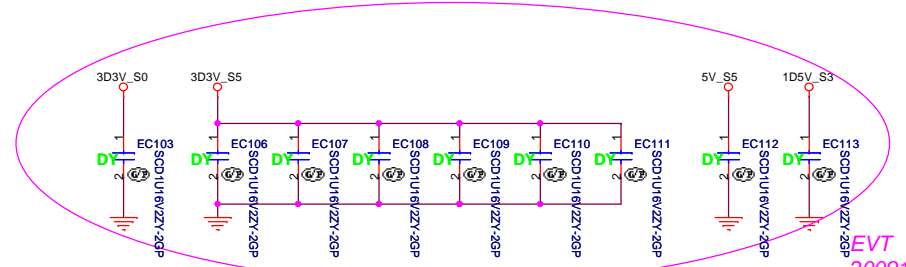
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20091221



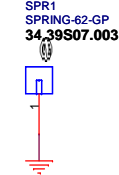
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20091221



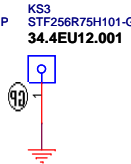
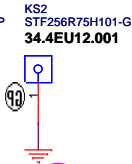
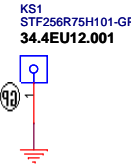
DVT
20100129



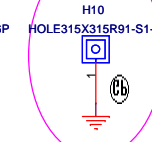
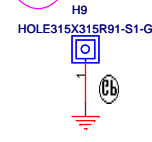
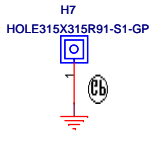
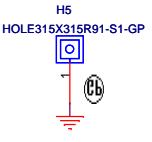
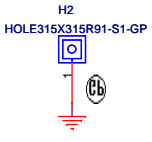
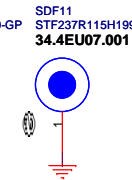
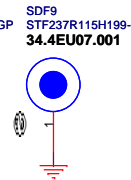
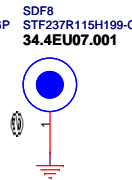
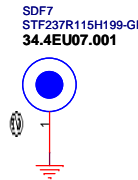
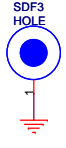
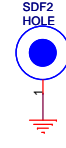
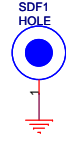
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20091221



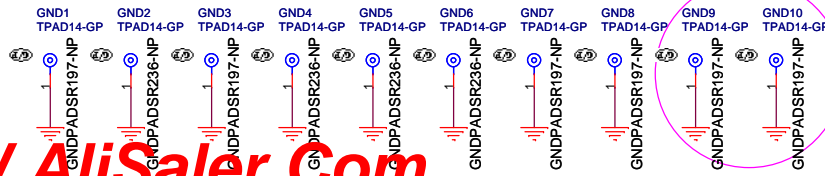
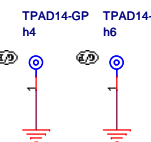
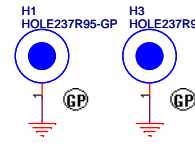
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20091221



EVT
20091208



EVT
20091117

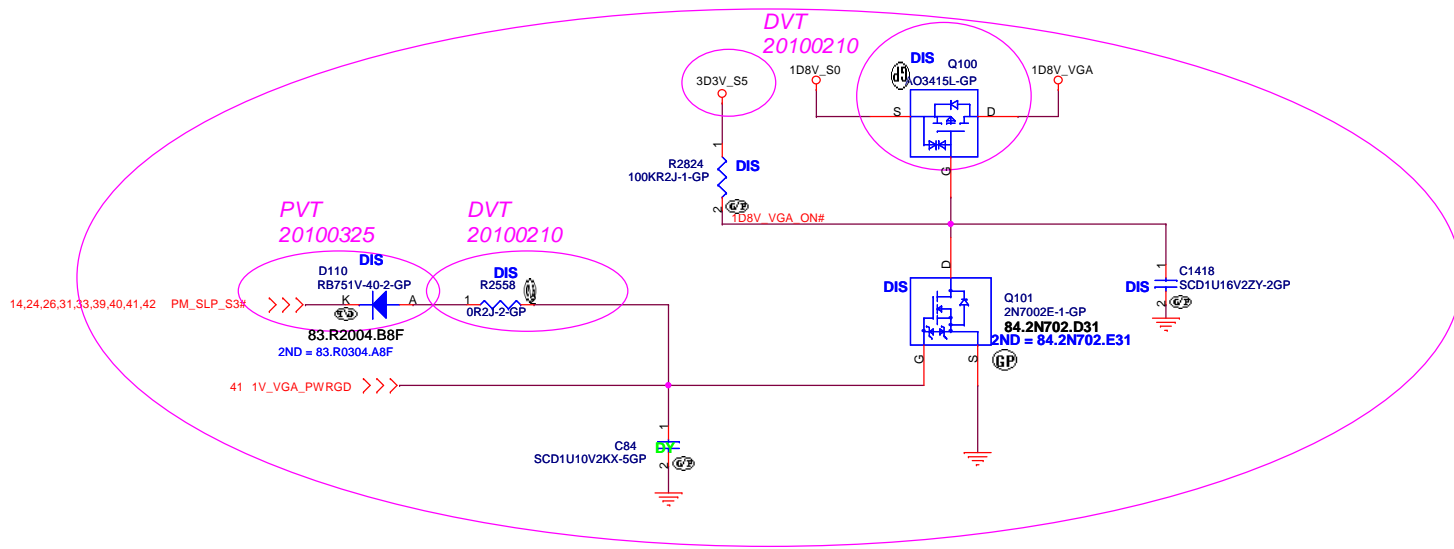
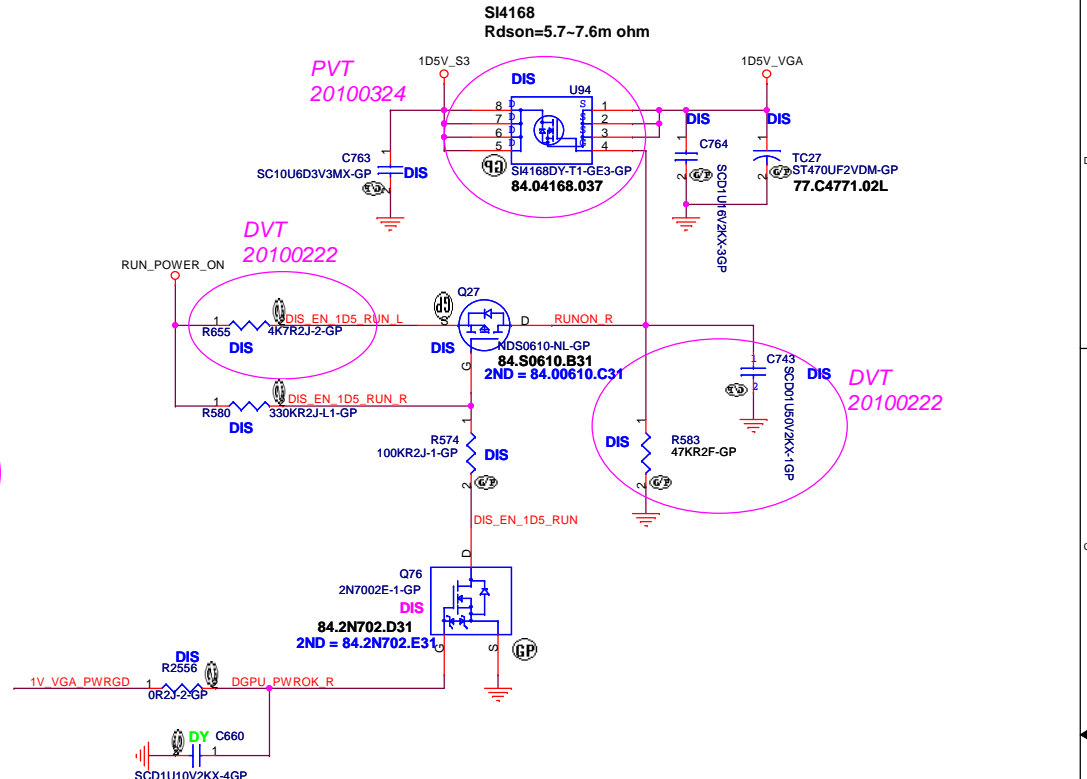
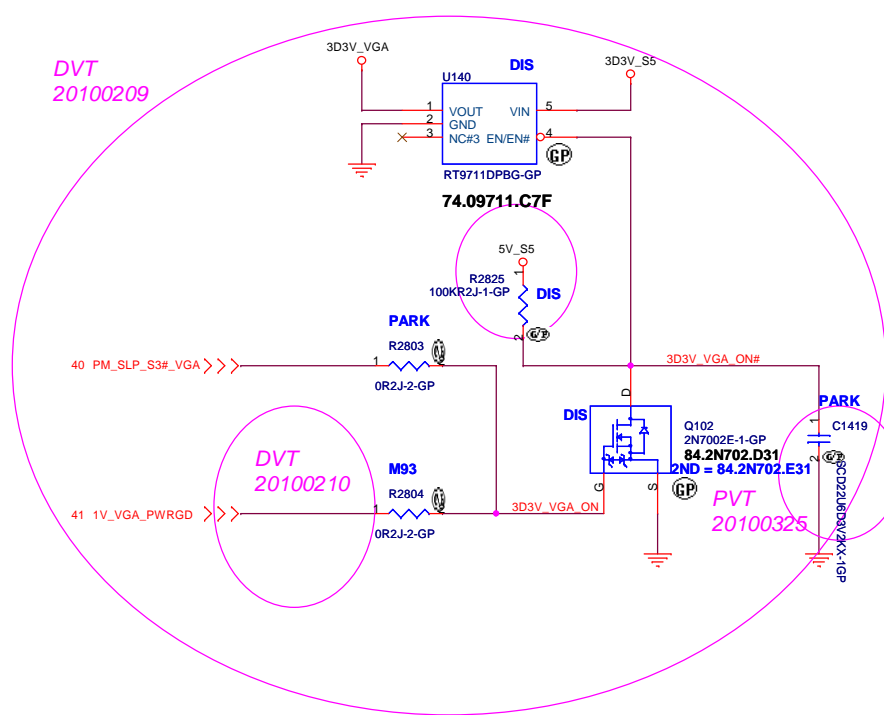


EVT
20091208

Squire CP DIS SAMSUNG

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Taipei Hsien 221, Taiwan, R.O.C.

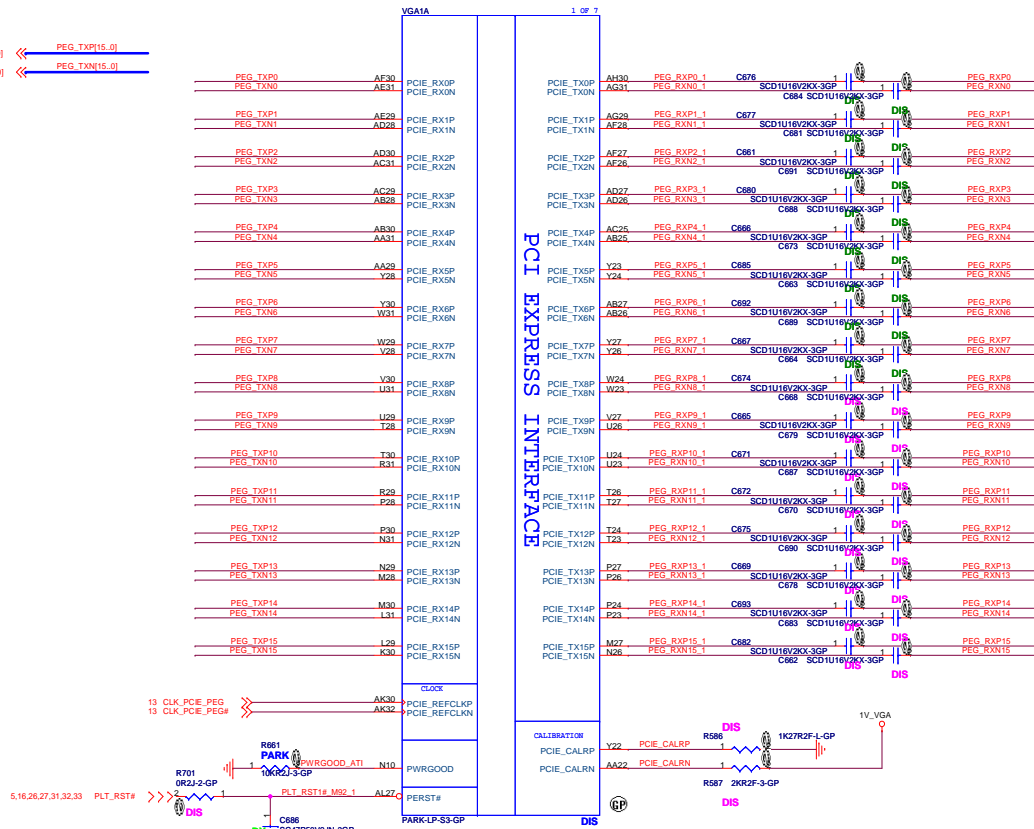
Title			EMI/Spring/Boss
Size	Document Number	Rev	-1M
Date: Saturday, April 24, 2010			CADIZ-CP
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Squirtle CP DIS SAMSUNG

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4 PEG_TXN[15..0] << PEG_TXN[15..0]

4 PEG_RXP[15..0] << PEG_RXP[15..0]
4 PEG_RXN[15..0] << PEG_RXN[15..0]

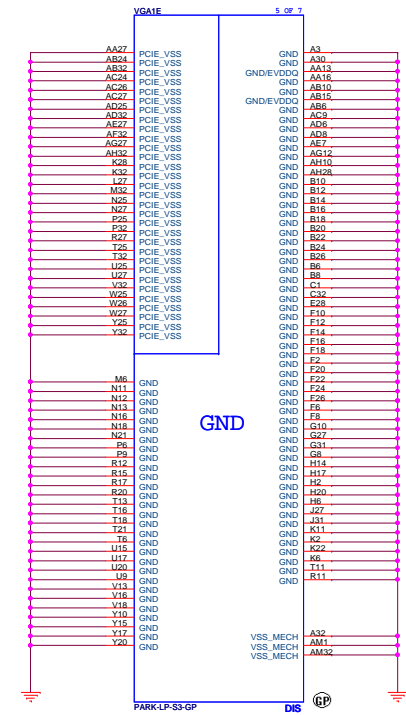
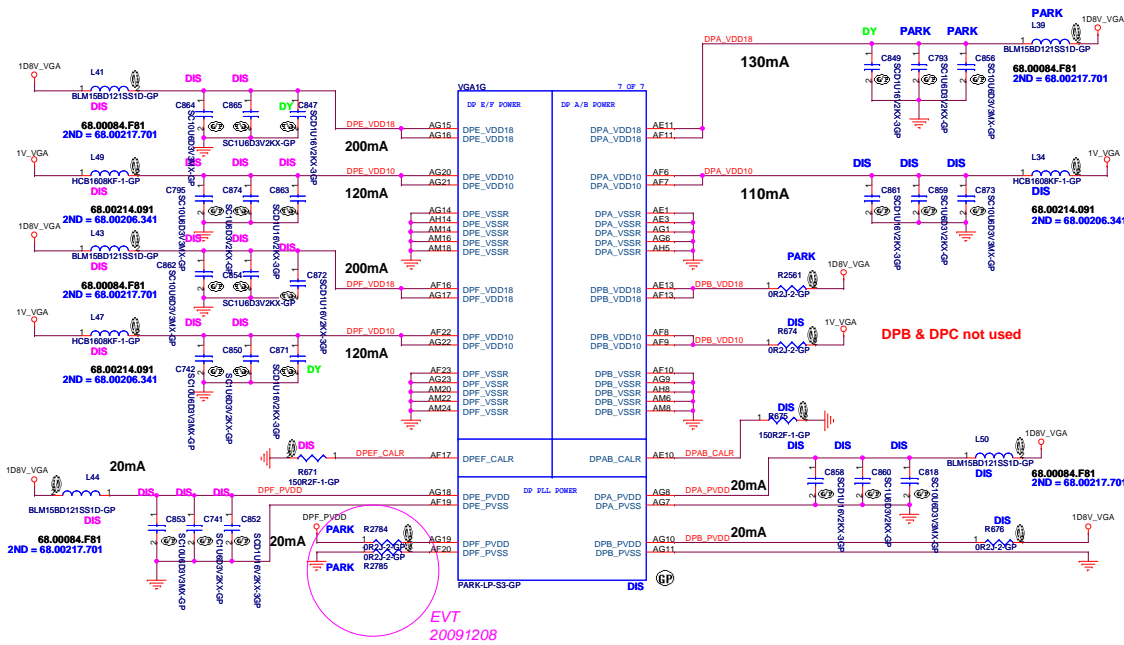


EVT
20091210

BB_ENA = 0V FOR BACK BIASING DISABLED
N FET Q5 = OFF, P FET Q4 = OFF, N FET Q3 = ON
+BBP = VDD_CORE
BB_ENA = +3.3V FOR BACK BIASING ENABLED
N FET Q5 = ON, P FET Q4 = ON, N FET Q3 = OFF
+BBP = +1.8V

Square CP DIS SAMSUNG

緯創資通 Wistron Corporation		21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.	
Title Madison PCIE			
Size A2	Document Number CADIZ-CP	Rev -1M	
Date: Saturday, April 24, 2010	Sheet 46	of 57	

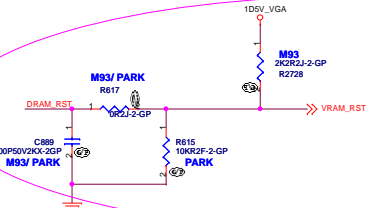
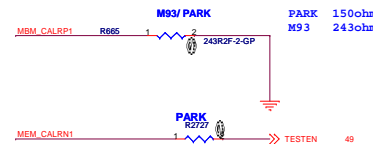
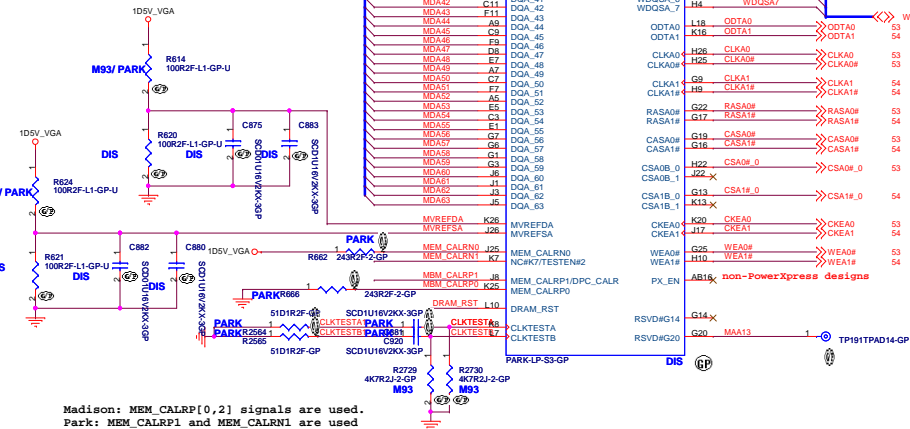


For M9X-S2/S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

For Park-S3

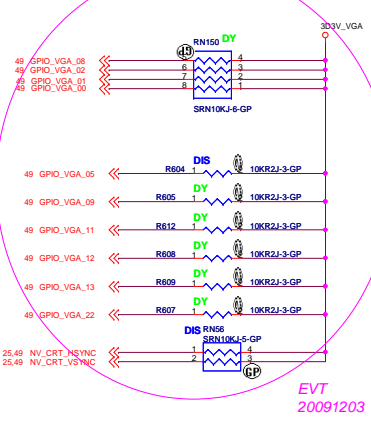
DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R



Designator	For M93-S2 and M93-S3	For Park-S3
R_MEM_1	001	100
R_MEM_2	00/Short	51R
R_MEM_3	2.2K	001
C_MEM	2.2uF	68uF

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS
TX_PWRS_ENB (Internal PD)	GPIO0	PCIe FULL TX OUTPUT SWING Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
BIF_GEN2_EN_A	GPIO2	PCIe GEN2 ENABLED	0
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_ROM=0, then Config[3:0] defines the primary memory aperture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
H2SYNC, GENERICCC, GPIO2, GPIO21				
If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST	M25P05A	0100
256MB	x001	ST	M25P10A	0101
512MB	x010	ST	M25P20	0101
1GB	x	ST	M25P40	0101
2GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
4GB	x	Chingis (formerly PMC)	Pm25LV010A	0101



Squire CP DIS SAMSUNG

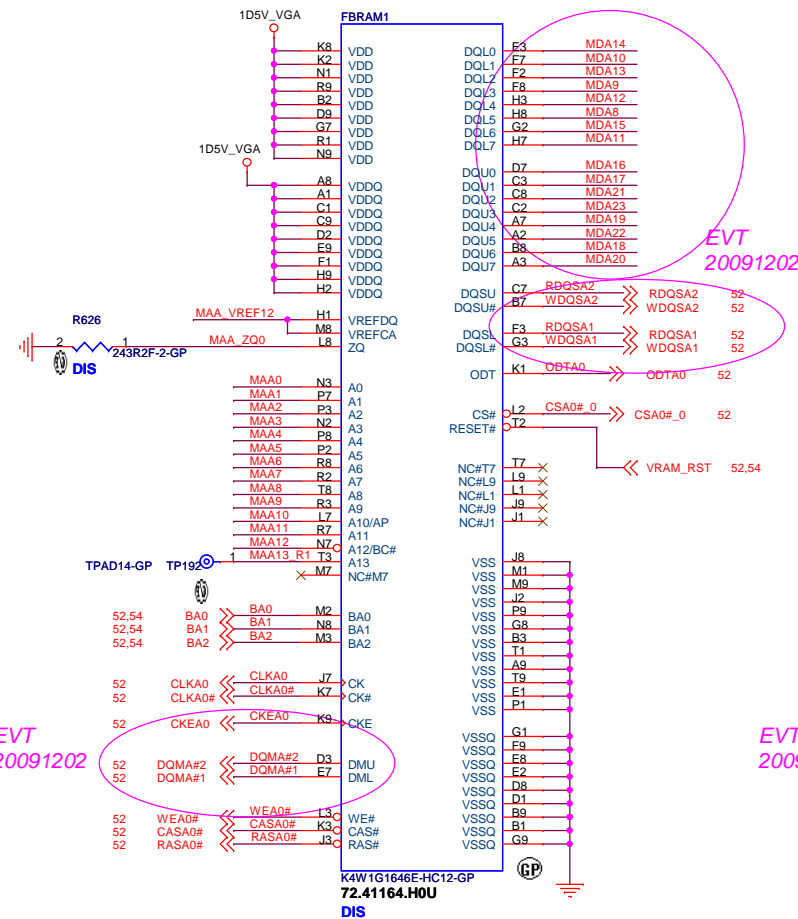
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

File: **Madison Memory / Straps**

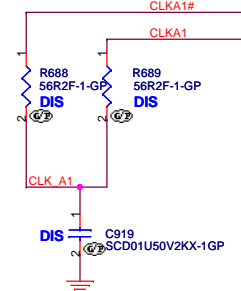
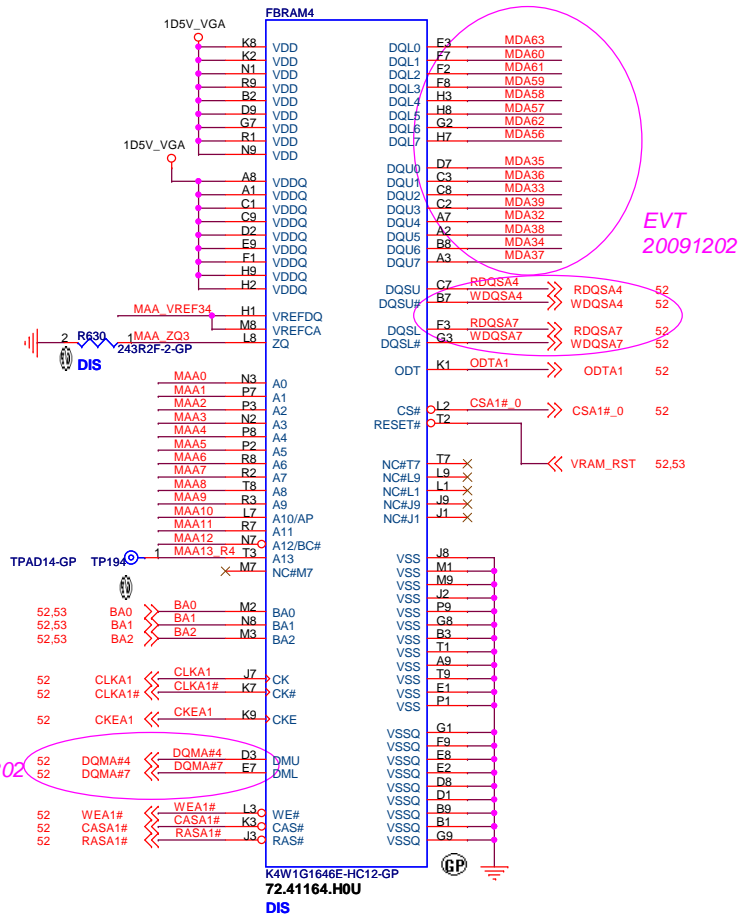
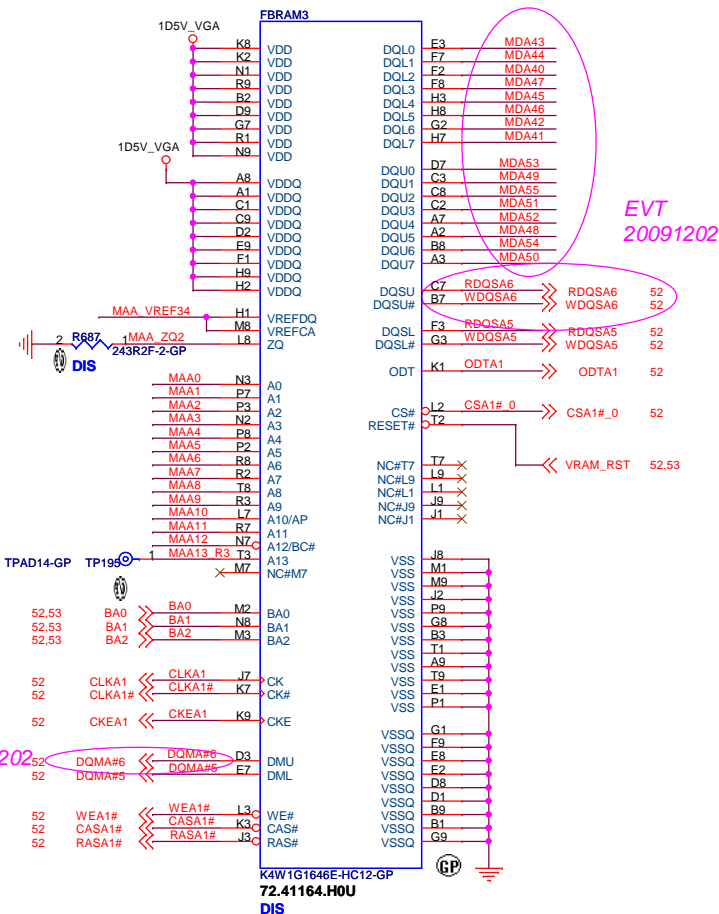
Size: A2 Document Number: **CADIZ-CP** Rev: **1M**

Date: Saturday, April 24, 2010 Sheet: 52 of 57

DDR3

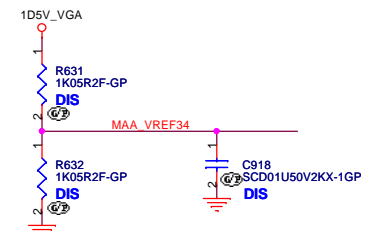


DDR3



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

52,53 DQMA#[0..7] <<>>
52,53 RDQSA#[0..7] <<>>
52,53 WDQSA#[0..7] <<>>
52,53 MAA#[0..12] <<>>
52,53 MDA#[0..63] <<>>



EVT

(2009/11/17)	
P.8 CPU SFF(5 of 8)-PWR/DDR/GFX]	Delete R2263 (GFX_VR_EN double pull-low)
P.15 [PCH 4 of 9(LVDS/CRT/DP]	Delete RN22 (CLK_DDC_EDID, DAT_DDC_EDID double pull-high)
P.15 [PCH 4 of 9(LVDS/CRT/DP]	Modify RN112 and add RN147
P.15 [PCH 4 of 9(LVDS/CRT/DP]	Change RN113 to three single resistors for PCH RGB signal.
P.23 [LCD CONN]	Add R2621, R2625 100Kohm pull-low for BLON_IN and BLON_OUT_R
P.25 [CRT BD CONN]	Add RN146 pull-high to 3D3V_S0 for CRT_DDCCLK1 and CRT_DDCDATA1
P.47 [EMI/Spring/Boss]	ME add stand off KS1--KS4 and H10
P.50 [PARK-S3 IO]	Change RN86 to three single resistors for VGA RGB signal.
(2009/11/20)	
P.13 PCH (2 of 9)-PCIE/CLK/SMB	Modify PCI express ports connection assigned table
P.16 PCH (5 of 9)-PCI/USB	Modify USB ports connection assigned table
P.27 MINI BD CONN	Add USB port for MINI1 WIMAX function
(2009/11/23)	
P.25 [CRT BD CONN]	Delete RN126--RN129
(2009/11/25)	
P.24 [HDD CONN & TOUCHPAD]	Add HDD protection circuit
P.27 MINI BD CONN	Modify WIMAX USB pair connection
P.25 [CRT BD CONN]	Change HDMI 0.1UF caps to BTBCRT1 side..
(2009/11/27)	
P.32 [BIOS & SW/C & BAT ID & Felic]	Add 10Kohm pull low for SPI_WP#
(2009/11/30)	
P.27 MINI BD CONN	Modify 5V_MINI_S5, 3d3v_s3 and USB8 net arrangement
P.3 Clock Generator	Add damping resistor for the 14MHz crystal
P.12 PCH (1 of 9)-SATA/RTC/HDA	Add damping resistor for the 32KHz crystal
(2009/12/01)	
P.13 PCH (2 of 9)-PCIE/CLK/SMB	Modify PCI express clock connection assigned table
P.40 ADP3211_GFX_CORE/ VGA_CORE	Modify VGA/ GFX co-lay power circuit
P.30 Thermal/Fan Controllor	Modify thermal contral circuit.
P.32 [BIOS & SW/C & BAT ID & Felic]	Modify net name SPI_MOSO_R to SPI_MISO_R
P.32 [BIOS & SW/C & BAT ID & Felic]	Add 100K ohms pull-down resistors on each SPI0_CLK, SPI0_MOSI and SPI0_CS# net.
P.12 PCH (1 of 9)-SATA/RTC/HDA	Add damping resistor for LPC_LAD0--LPC_LAD3 and LPC_LFRAME#
P.7 CPU SFF(4 of 8)-POWER/VTT	Delete VCORE SENSE pin double pull high/low resistors.
P.39 RT8209_1D05V	Add sequence circuit for VTTTPWRGOOD and VTT.
(2009/12/02)	
P.29 AUDIO JACK	Add speaker protection circuit.
P.32 [BIOS & SW/C & BAT ID & Felic]	Add golden finger debug connector GF1 and only install it on EVT
P.37 [RT8223_5V/3D3V]	Delete 3D3V_PWR 7pcs gaps for more place.
P.12 PCH (1 of 9)-SATA/RTC/HDA	Add test point for JTAG.
P.25 [CRT BD CONN]	Change HDMI_CLK, HDMI_DATA, CRT_DDCCLK1, CRT_DDCDATA1 pull high resistors to 3.83Kohm.
P.53 [VRAM(1/2)]	Swap VRAM DQ, DQS, DIM net.
P.54 [VRAM(3/4)]	Swap VRAM DQ, DQS, DIM net.
(2009/12/03)	
P.13 PCH (2 of 9)-PCIE/CLK/SMB	Change PCIE_CLK_RQ2# to pull low for cardreader.
P.23 [LCD CONN]	Change descrete brightness source from EC to VGA.
P.52 [M93/ PARK-S3 Memory / Straps]	Modify GPIO setting
(2009/12/04)	
P.40 ADP3211_GFX_CORE/ VGA_CORE	Modify sense pin circuit.
P.28 Audio Codec ALC275	Modify speaker protection circuit.
P.29 AUDIO JACK	Modify speaker protection circuit.
P.39 RT8209_1D05V	Delete 1D05V output gaps.
P.42 G9661_1D8V/ RT9026_0D75	Add S3 Power Reduction schematics.
P.5 CPU SFF(2 of 8)-CLK/Thermal	Add S3 Power Reduction schematics.
P.17 PCH (6 of 9)-GPIO/RSVD	Add S3 Power Reduction schematics.
P.33 RUN POWER	Add S3 Power Reduction schematics.
P.8 CPU SFF(5 of 8)-PWR/DDR/GFX	Add S3 Power Reduction schematics.
P.21 DDR3-SOCKET_1	Add S3 Power Reduction schematics.
P.14 PCH (3 of 9)-DMI/FDI	Add S3 Power Reduction schematics.
(2009/12/07)	
P.31 KBC_NPCE781L / KB	Modify W_Disable# direction to output from EC
P.27 MINI BD CONN	Modify W_Disable# direction to output from EC
P.13 PCH (2 of 9)-PCIE/CLK/SMB	Delete RN102 and omit the routing prom PCH to CPU
P.5 CPU SFF(2 of 8)-CLK/Thermal	always install RN89 for UMA and DIS.
P.27 MINI BD CONN	Modify power source 6 pins of 3D3V_S3 to 3D3V_S5 for WWAN power off sequence by software request.
(2009/12/08)	
P.46 EMI/Spring/Boss	Delete SDF4, KS4 and add GND9, GND10 for ME request.
P.50 M93/ PARK-S3 POWER	Pins A11, Y11, V11, U11 can left unconnected at M93-S3 and PARK-S3.
P.51 M93/ PARK-S3 DP POWER_GND	DPF_PVDD, DPF_PVSS add damping resistor for PARK-S3.
P.49 M93/ PARK-S3 IO	Change A2VSSQ connection to clean ground.
P.52 M93/ PARK-S3 Memory / Straps	Modify "DRAM_RST" output circuit.
P.39 RT8209_1D05V	Power team modify circuit (delete U107)
P.40 ADP3211_GFX_CORE/ VGA_CORE	Modify VGA power sequence
P.41 APL5930_1V	Modify VGA power sequence
P.48 M93/ PARK-S3 PCIE	Modify VGA power sequence
(2009/12/09)	
P.33 RUN POWER	Delete R344 and C28.
P.3 Clock Generator	Modify symbol to 9LVS3197BKLFT that only one CLKGEN source we will use. Delete pin16 CPU_STOP# to NC for 9LVS3197BKLFT.
P.31 KBC_NPCE781L / KB	Add 100Kohm pull up resistor for ME_UNLOCK# and combine 3pcs 100Kohm pull up to one 8P4R resistor.
P.36 ADP3211_CPU CORE	Change TC60 power plane from DCBATOUT to DCBATOUT_3211_CPU and add TC61 for DCBATOUT
P.9 CPU SFF(6 of 8)-CPUCORE	Delete C978, C979, C982, C983 for placement.
P.17 PCH (6 of 9)-GPIO/RSVD	Change PCH_GPIO57 DIS/UMA selection to KBC.
(2009/12/10)	
P.36 ADP3211_CPU CORE	Change net 3211_PWRGD pull high 1Kohm to 3D3V_S0
P.12 PCH (1 of 9)-SATA/RTC/HDA	Change 4pcs TP to two dummy 0402 resistor for layout space.
P.33 RUN POWER	Delete R2720 and R513.
P.14 PCH (3 of 9)-DMI/FDI	Delete R464 and PM_PWROK connection to PCH.B17(PWROK).
P.48 M93/ PARK-S3 PCIE	Delete M93 +BBP circuit.
P.27 MINI BD CONN	Add one more power pin on BTBMINI1 for 3D3V_S3.
P.36 ADP3211_CPU CORE	Modify VID[5:3] setting for 27A CPU core power rating.
P.26 CARDREADER BD CONN	Modify WLAN_BT_DATA direction
P.27 MINI BD CONN	Modify WLAN_BT_DATA direction
P.40 ADP3211_GFX_CORE/ VGA_CORE	Add R2791 0ohm resistor installed on UMA SKU to separate the connection between VGA power circuit and CPU
P.12 PCH (1 of 9)-SATA/RTC/HDA	Add R2793 pull low resistor on la
P.39 RT8209_1D05V	Add sequence circuit for VTTTPWRGOOD and VTT when system suddenly moves to G3 by removing both AC and battery at the same time.
P.14 PCH (3 of 9)-DMI/FDI	Add sequence circuit for SYS_PWROK , PWROK, MEPWROK when system suddenly moves to G3 by removing both AC and battery at the same time.
(2009/12/11)	
P.5 CPU SFF(2 of 8)-CLK/Thermal	Modify RN93 resistor to two single resistors.
P.40 ADP3211_GFX_CORE/ VGA_CORE	Delete R2644 and change R2642 to 10Kohm.
P.41 APL5930_1V	Delete R2482.
P.47 ATI POWER	Modify R2330 pull-up from 3D3V_S3 to 3D3V_S0.
P.41 APL5930_1V	Modify R2479 pull-up from 3D3V_S3 to 3D3V_S0.
P.47 ATI POWER	Modify 3D3V_VGA sequence circuit.
P.27 MINI BD CONN	Modify to 8pin 3D3V_S3.
P.33 RUN POWER	Change U138 to AO4406AL.
(2009/12/12)	
P.27 MINI BD CONN	Modify BTBMINI1 to 3pins of 3D3V_S3 and 6pins of 3D3V_S5.
(2009/12/14)	
P.36 ADP3211_CPU CORE	Change R2573 from 1.91Kohm to 10Kohm.
P.26 CARDREADER BD CONN	Modify 5V_S0 power to 1D5V_S0 because 5V_S0 has not used on cardreader board.
P.16 PCH (5 of 9)-PCI/USB	Modify USB_OC#3--USB_OC#7 to single pull-up.
P.39 RT8209_1D05V	Delete G227, G225.
P.8 CPU SFF(5 of 8)-PWR/DDR/GFX	Change R669,R668,R685,R695 to 0402 resistors.
P.9 CPU SFF(6 of 8)-CPUCORE	Delete C1313, C1314.
P.14 PCH (3 of 9)-DMI/FDI	Add D112 to match the sequence IMVP_VR_EN and SYS_PWROK/PCH_PWROK.
(2009/12/14)	
P.50 M93/ PARK-S3 POWER	Add 0ohm 0805 resistor for VDDCI.
(2009/12/15)	
P.14 PCH (3 of 9)-DMI/FDI	Modify reset circuit for POWEROK and VTTTPWRGOOD sequence when system suddenly moves to G3.
P.13 PCH (2 of 9)-PCIE/CLK/SMB	Add 0ohm resistor for XTAL25_OUT.
(2009/12/16)	
P.14 PCH (3 of 9)-DMI/FDI	Modify reset circuit for POWEROK,PM_RSMRST# and VTTTPWRGOOD sequence when system suddenly moves to G3.
P.40 ADP3211_GFX_CORE/ VGA_CORE	Modify VCC_AXG_SENSE,VSS_AXG_SENSE connection.
P.17 PCH (6 of 9)-GPIO/RSVD	[Bom change] change RN119 from 10Kohm to 33Kohm.
P.36 ADP3211_CPU CORE	[Bom change] change R2580 from 1Kohm to 3.3Kohm.
P.39 RT8209_1D05V	[Bom change] delete Q84, R2742.
(2009/12/17)	
P.14 PCH (3 of 9)-DMI/FDI	Change D112 direction.
P.50 M93/ PARK-S3 POWER	Change one 0805 resistor to two 0402 resistors for layout placement space.
P.40 ADP3211_GFX_CORE/ VGA_CORE	Change R2660 size from 0402 to 0805 for VCC_AXG_SENSE/ VSS_AXG_SENSE routing.
(2009/12/21)	
P.46 EMI/Spring/Boss	EMC add EC103, EC106--EC117 for 3D3V_S0, 3D3V_S5, 5V_S5, 1D5V_S3, 1V_VGA, 1D5V_VGA.
P.8 CPU SFF(5 of 8)-PWR/DDR/GFX	Delete C1282, C1281 and change C1264, C1265 to 4.7uF for layout placement space.
P.50 M93/ PARK-S3 POWER	Delete C834, C807, C800, C811, C816, C815, C737, C799 and change C789 to 4.7uF for layout placement space.
P.46 EMI/Spring/Boss	Delete EC80, EC79, EC82, EC59, EC58, EC51, EC12, SPR2 for layout placement space.
P.31 KBC_NPCE781L / KB	Change PCB version setting for power saving in S5.
P.39 RT8209_1D05V	Add VTT_PWRGD pull-up resistor.
P.37 [RT8223_5V/3D3V]	Because the shortage of FDMC8296, change U100, U101 to FDMC7692.
(2010/01/09)	
P.17 PCH (6 of 9)-GPIO/RSVD	[BOM Change] change Q92 from transistor to MOS 2N7002 and change C1411 from 0.047uF to 0.1uF.
P.33 RUN POWER	[BOM.Change] change Q94, Q95,from transistor to MOS 2N7002.

Squirrel CP DIS SAMSUNG

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DVT

(2010/01/21)	
P.38 [RT8209_1D5V]	[BOM change] R2409 change from 30Kohm to 31.6Kohm.
P.37 [RT8223_5V/3D3V]	[BOM change] R2393 change from 30Kohm to 31.6Kohm.
(2010/01/25)	
P.13 [PCH (2 of 9)-PCIE/CLK/SMB]	[BOM change] C1023, C1024 change from 18pF to 15pF.
P.49 [M93/ PARK-S3 IO]	[BOM change] C719, C721 change from 10pF to 12pF.
P.32 [BIOS & SW/C & BAT ID & Felic]	[BOM change] Add EC83, EC84 to 330pF for EMC request.
(2010/01/29)	
P.23 [LCD CONN]	[BOM change] Change DIS brightness source to EC control.
P.46 [EMI/Spring/Boss]	Add EC51, 58,59 to 0.1uF for EMC request.
(2010/02/03)	
P.24 [HDD CONN & TOUCHPAD]	Change R2701 to 91Kohm and add C1417 to 2,2uF for HDD protection.
P.33 [RUN POWER]	[BOM change] change R2779 to 100Kohm for 1D5V_S0_PWRGD.
P.42 [G9661_1D8V/ RT9026_0D75]	[BOM change] change R2780 to 0ohm for 1D5V_S0_PWRGD.
(2010/02/04)	
P.36 [ADP3211_CPU CORE]	Change TC60 from EL CAP to POSCAP and change R2593 to 91Kohm.
P.37 [RT8223_5V/3D3V]	Change R2384 to 75Kohm and change R2385 to 97.6Kohm.
P.39 [RT8209_1D05V]	Change R2421 to 10.2Kohm.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Modify +VGA_CORE feedback trace connection and change C1373 to 820pF
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change R2645 to 8.66Kohm for GFX.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change R2657 to 63.4Kohm and cahnge R2647 to 6.65Kohm for VGA.
P.45 [UVP Protect]	Change Q72 to P-MOSFET and add R2816, R2817 to 200Kohm.
P.36 [ADP3211_CPU CORE]	Dummy R2613.
(2010/02/05)	
P.31 [KBC_NPCE781L / KB]	Change R2714 to 20Kohm for PCB version.
P.33 [RUN POWER]	Add a dummy resistor R2818 to 100Kohm.
(2010/02/08)	
P.14 [PCH (3 of 9)-DMI/FDI]	Change R2812 to 165Kohm.
P.49 [M93/ PARK-S3 IO]	Change R2562, R2563 options to PARK.
P.50 [M93/ PARK-S3 POWER]	Change L75, R2426, C783, C867 options to M93.
P.50 [M93/ PARK-S3 POWER]	Change L58, C841, C877, C842, C843 options to PARK.
P.52 [M93/ PARK-S3 Memory / Straps]	Change R665 to 243ohm, R617 to 0ohm, C889 to 2.2nF for M93.
P.41 [APL5930_1V]	Change R2483 to 59Kohm for M93.
P.50 [M93/ PARK-S3 POWER]	Delete C810 for placement space.
P.33 [RUN POWER]	Cahnge Q94 to transistor, C1412 to 1uF, R2818 to 330Kohm and stuff it.
P.31 [KBC_NPCE781L / KB]	Add R2819 pull-up to 3D3V_AUX_S5 and change C364 to 1uF for vender request.
P.24 [HDD CONN & TOUCHPAD]	Modify R2701pull-up to 5V_AUX_S5 and dummy D105.
P.47 [ATI POWER]	Change 3D3V_VGA solution from MOS to switch.
(2010/02/09)	
P.42 [RT8015_1D8V/ RT9026_0D75]	Change 1D8V_S0 power solution to RT8015.
P.46 [EMI/Spring/Boss]	Add EC118 to 0.1uF at AD+ for EMC request.
P.47 [ATI POWER]	Change 1D8V_VGA power solution and R2558 to 1Kohm.
P.7 [CPU SFF(4 of 8)-POWER/VTI]	Delete C1238 for placement space.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Add R2823 to 267Kohm and dummy R2689.
P.14 [PCH (3 of 9)-DMI/FDI]	Change U139 VCC to 3D3V_AUX_S5.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change D107 to 83.R2004.B8F and R2786 to 47Kohm.
P.41 [APL5930_1V]	Change D108 to 83.R2004.B8F and R2480 to 10Kohm.
P.12 [PCH (1 of 9)-SATA/RTC/HDA]	Change R2733~R2737 to 56ohm.
P.47 [ATI POWER]	Modify 3D3V_VGA solution.
(2010/02/10)	
P.47 [ATI POWER]	Change R2824 pull up to 3D3V_S5.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change R2642 pull up to 3D3V_S5.
P.47 [ATI POWER]	Change R2558 to 0ohm, delete D109, R2788, C1415.
P.12 [PCH (1 of 9)-SATA/RTC/HDA]	Change C1008, C1009 to 5pF.
P.13 [PCH (2 of 9)-PCIE/CLK/SMB]	Delete EC91 for placement space.
P.16 [PCH (5 of 9)-PCI/USB]	Delete EC93 for placement space.
P.31 [KBC_NPCE781L / KB]	Delete C363 for placement space.
P.50 [M93/ PARK-S3 POWER]	Stuff C821 to 1uF.
P.47 [ATI POWER]	Change Q100 to AO3415.
P.24 [HDD CONN & TOUCHPAD]	Change Q77 to AO3419.
P.17 [PCH (6 of 9)-GPIO/RSVD]	Stuff R2298 to 54.9ohm and dummy RN120 for THERMTRIP#.
P.33 [RUN POWER]	Stuff R167 to 56ohm for THERMTRIP#.
P.5 [CPU SFF(2 of 8)-CLK/Thermal]	Stuff R2305 to 0ohm for PROCHOT#.
(2010/02/11)	
P.42 [RT8015_1D8V/ RT9026_0D75]	Add more one gap G330 for 1D8V_S0.
P.42 [RT8015_1D8V/ RT9026_0D75]	Add EC119 to 0.1uF for EMC request.
(2010/02/22)	
P.41 [APL5930_1V]	Change R2479 to 10Kohm for vga sequence.
P.47 [ATI POWER]	Change C743 to 0.01uF, R583 to 47Kohm and R655 to 4.7Kohm for vga sequence.
P.33 [RUN POWER]	Dummy R2818.
(2010/02/23)	
P.17 [PCH (6 of 9)-GPIO/RSVD]	Dummy R2298 and stuff RN120 for THERMTRIP#.
P.33 [RUN POWER]	Dummy R167 for THERMTRIP#.
P.47 [ATI POWER]	Change U94 to AO4430 Rds=5.5~7.5mohm
P.31 [KBC_NPCE781L / KB]	Change U135 to G691L293T73UF.

(2010/02/24)	
P.38 [RT8209_1D5V]	[BOM change] R2409 change from 31.6Kohm to 30Kohm.
P.43 [BQ24751_Charger]	[BOM change] R2512 change from 120Kohm to 63.4Kohm for DIS.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] R2823 change from 267Kohm to 160Kohm for DIS.

PVT

(2010/03/18)	
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Modify +VGA_CORE feedback trace connection.
P.14 [PCH (3 of 9)-DMI/FDI]	Change U139 VCC from 3D3V_AUX_S5 to 5V_AUX_S5.
(2010/03/22)	
P.31 [KBC_NPCE781L / KB]	[BOM change] Dummy R142 double pull low.
(2010/03/24)	
P.47 [ATI POWER]	[BOM change] Change U94 toSI4168 Rds=5.7~7.6mohm.
P.33 [RUN POWER]	Delete R2818 and change Q10 pin5 connection to PM_SLP_S3_CTL.
(2010/03/25)	
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Change R2642 to 100Kohm for VGA sequence.
P.41 [APL5930_1V]	[BOM change] Change R2479 to 100Kohm for VGA sequence.
P.47 [ATI POWER]	[BOM change] Change D110 to RB751V for VGA sequence.
P.47 [ATI POWER]	[BOM change] C1419 to 0.22uF for VGA sequence PARK only.
(2010/03/29)	
P.24 [HDD CONN & TOUCHPAD]	[BOM change] Change R2701 to 133Kohm and change R2702 to 3.3Kohm for HDD protection sequence.
P.24 [HDD CONN & TOUCHPAD]	Add C1379 to 0.1uF for HDD protection sequence.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	Change R2660 0ohm resistor to 0805 size.
(2010/03/30)	
P.36 [ADP3211_CPU CORE]	Change U127 to TPCA8030 and change U128, U129 to TPCA8028 for VCC_CORE quality.
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Dummy R2823 and add R2689 to 100Kohm for VGACORE level.
(2010/03/31)	
P.31 [KBC_NPCE781L / KB]	Add CP and CP2 option circuit.
Change 0ohm resistors to 0ohm pads	0402-pad: R2547, R2732, R2566, R2553, R2568, R2567, R2574, R2552, R2554, R2572, R2550, R2570, R2549, R2731, R2569, R2551, R2578, R2548 0603-pad: R2669, R2246, R2247
(2010/04/01)	
P.38 [RT8209_1D5V]	[BOM change] Change R2411 to 10Kohm and change R2409 to 10.2Kohm to rise 1% of 1D5V_S3 level.
P.49 [M93/ PARK-S3 IO]	[BOM change] C719, C721 change to 6.8pF.
P.13 [PCH (2 of 9)-PCIE/CLK/SMB]	[BOM change] C1023, C1024 change to 12pF.
(2010/04/02)	
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Change R2659, R2698 to 0ohm resistor for VGA_CORE transition overshoot.
(2010/04/07)	
P.40 [ADP3211_GFX_CORE/ VGA_CORE]	[BOM change] Change C1414 0.1UF capacitor from Y5V to X7R.
(2010/04/12)	
P.49 [M93/ PARK-S3 IO]	[BOM change] Add 2nd source for X7.

MP

(2010/04/21)	
P.19 [PCH (8 of 9)-PWRISATAIUSB]	Change VCCSUSHDA power plane to 1.5V_S5.
(2010/04/24)	
P.19 [PCH (8 of 9)-PWRISATAIUSB]	Add R2826 dummy pull low resistor for enable pin.