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11	PCH (PCI-E,SMBUS,CLK)	1.0		53	VRAM Power(+1_8V)
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Project Code & Schematics Subject:	M931 Main Board	PCB P/N:	(IRIS) (Hannstar)
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M931 BOM Control Table								
VALUE Head	CFD+PM55 N11P 1GVRAM-H	CFD+PM55 N11P 1GVRAM-S	CFD+PM55 N11M 512MVRAM-H	CFD+PM55 N11M 512MVRAM-S	ARD+PM55 N11P 1GVRAM-H	ARD+PM55 N11P 1GVRAM-S	ARD+PM55 N11M 512MVRAM-H	ARD+PM55 N11M 512MVRAM-S
NV_	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff	Stuff
NP_	Stuff	Stuff	Dummy	Dummy	Stuff	Stuff	Dummy	Dummy
NM_	Dummy	Dummy	Stuff	Stuff	Dummy	Dummy	Stuff	Stuff
NVH_	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy
NVS_	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff	Dummy	Stuff
NC_	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy	Dummy

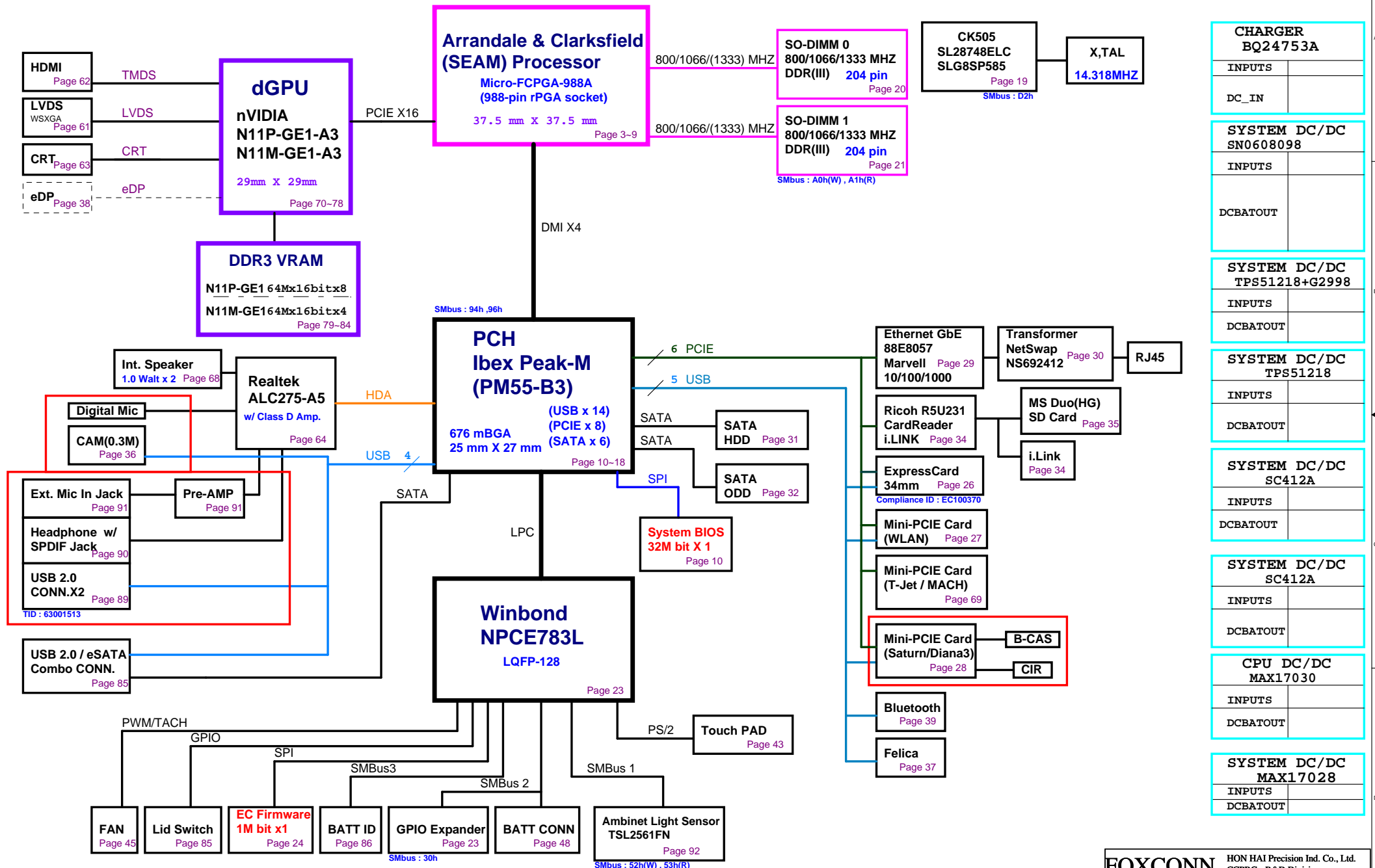
TJ_ for T-JET SKU (CTO)

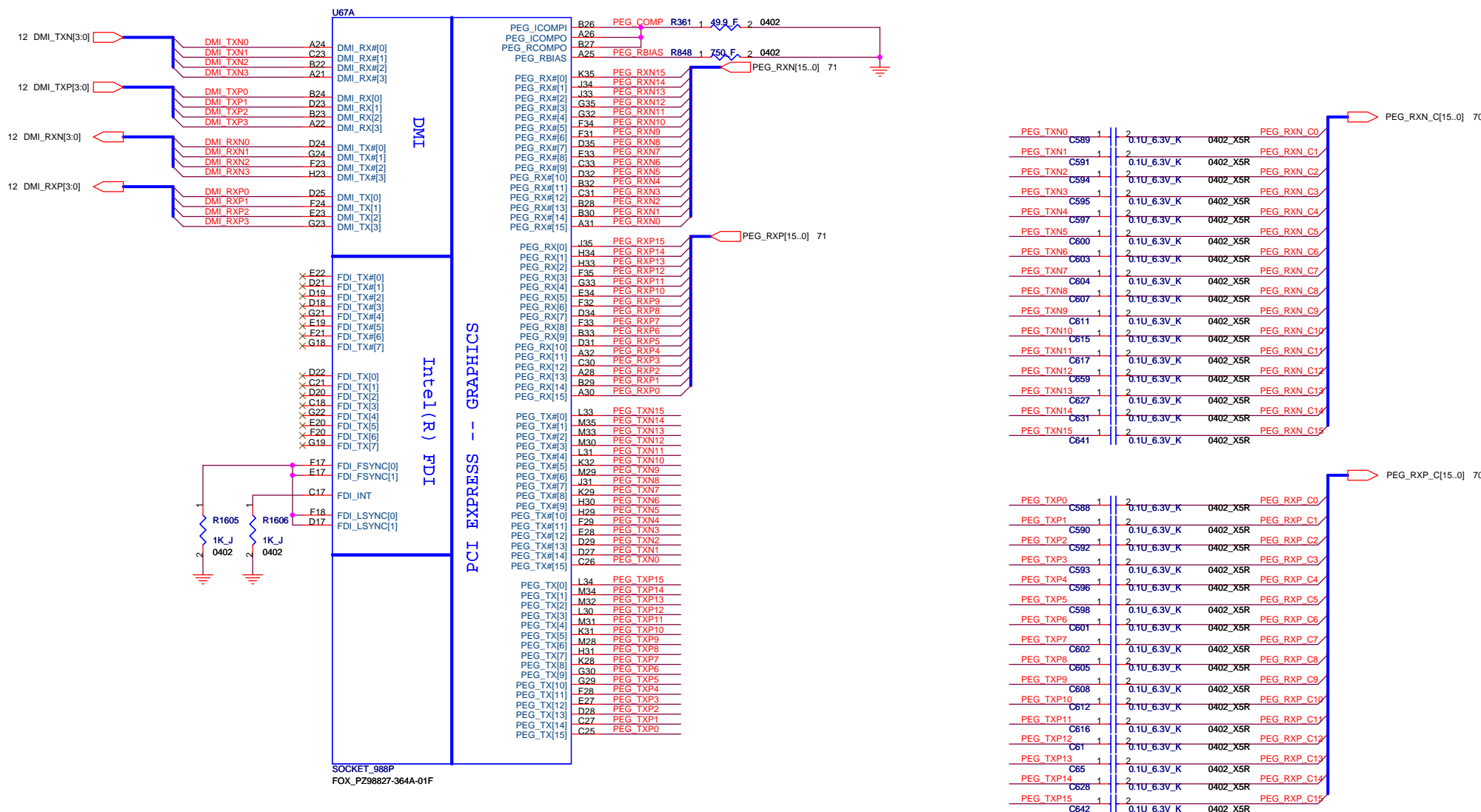
85	LID Switch/eSATA COMBO	1.0
86	Identify IC	1.0
87	HOLE & AMI LABEL	1.0
88	USB & AUDIO Conn.	1.0
89	USB Port	1.0
90	HP Jack (S/PDIF)	1.0
91	Ext MIC Jack	1.0
92	Function SW & ALS	1.0

P. Leader	Check by	Design by

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Size	Document Number	Rev	
Custom	M931 (MBX-215)	SA	
Date:	Wednesday, January 06, 2010	Sheet	1 of 93

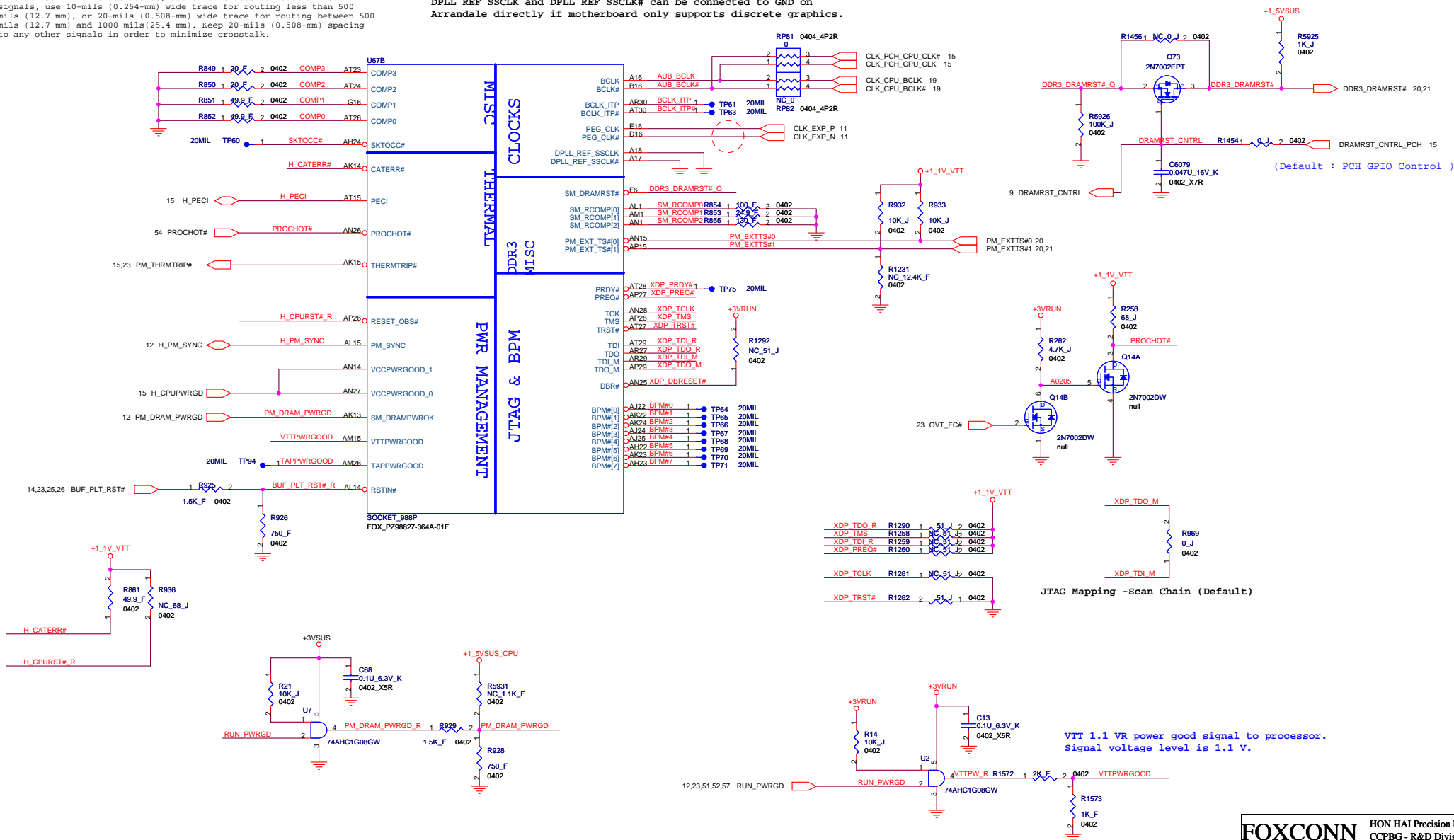
M931 (IRX-5300) Calpella Platform+ nVIDIA N11P/M Discrete Graphic



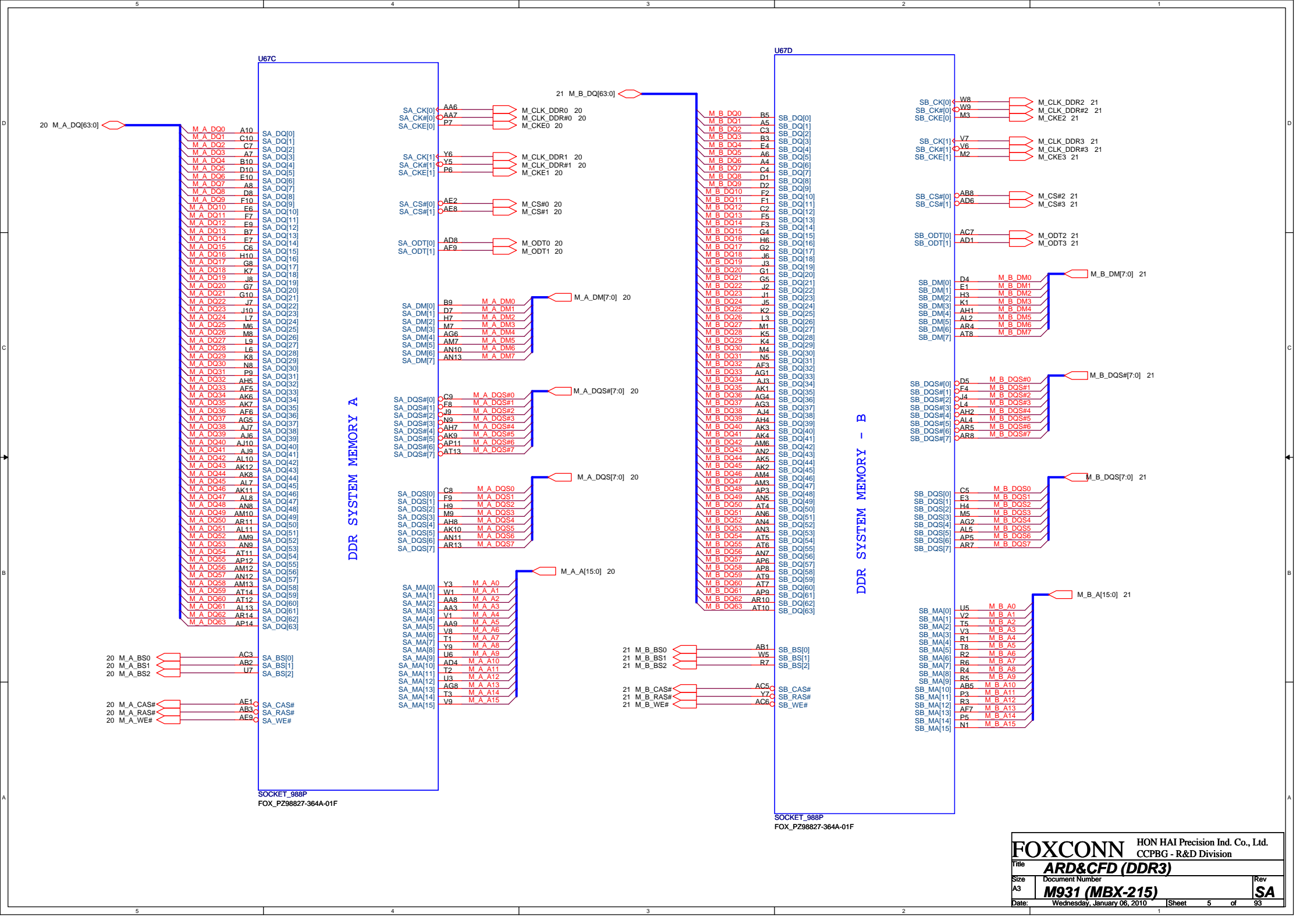


Layout Note:
In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils (0.254-mm) wide trace for routing less than 500 mils (12.7 mm), or 20-mils (0.508-mm) wide trace for routing between 500 mils (12.7 mm) and 1000 mils(25.4 mm). Keep 20-mils (0.508-mm) spacing to any other signals in order to minimize crosstalk.

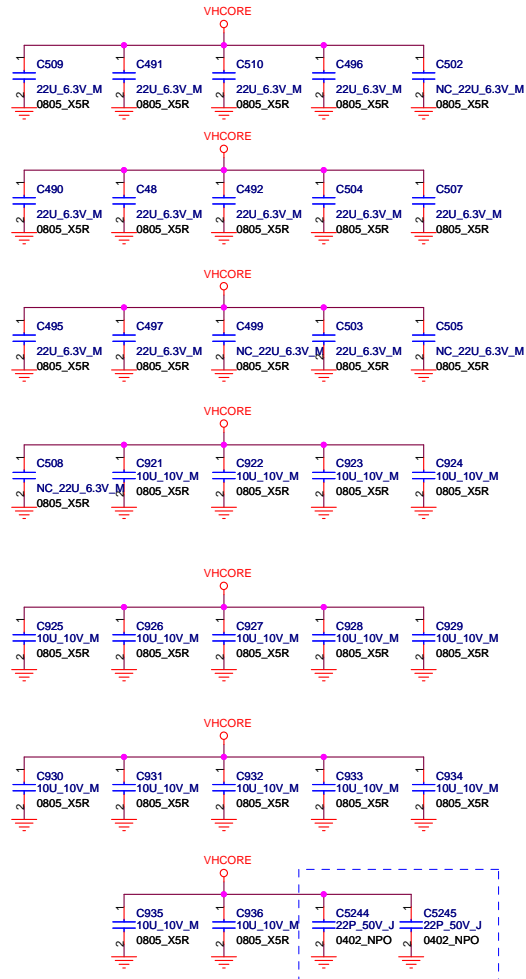
For Disable Auburndale Graphic
DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on Arrandale directly if motherboard only supports discrete graphics.



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	ARD&CFD (CLK,MISC,JTAG)		
Size	Document Number		Rev
Custom	M931 (MBX-215)		SA
Date:	Wednesday, January 06, 2010	Sheet	4 of 93

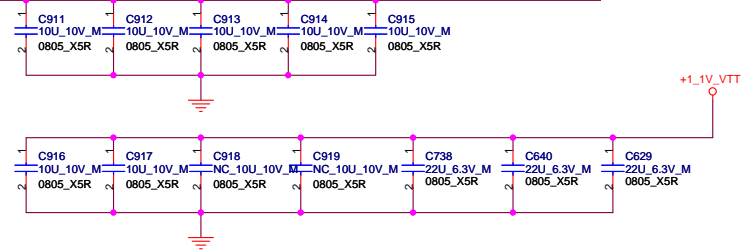


52A (CFD SV)

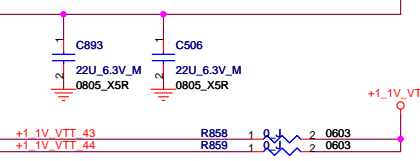


For RF Noise

18A(CFD SV) (VTT)



18A(CFD SV) (VTT)



VHOCORE

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AC25 VCC41
AC24 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

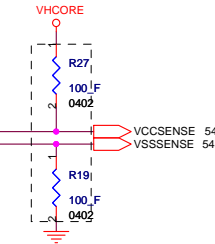
SOCKET_988P
FOX_P298827-364A-01F

1.1V RAIL POWER

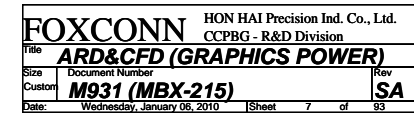
CPU CORE SUPPLY

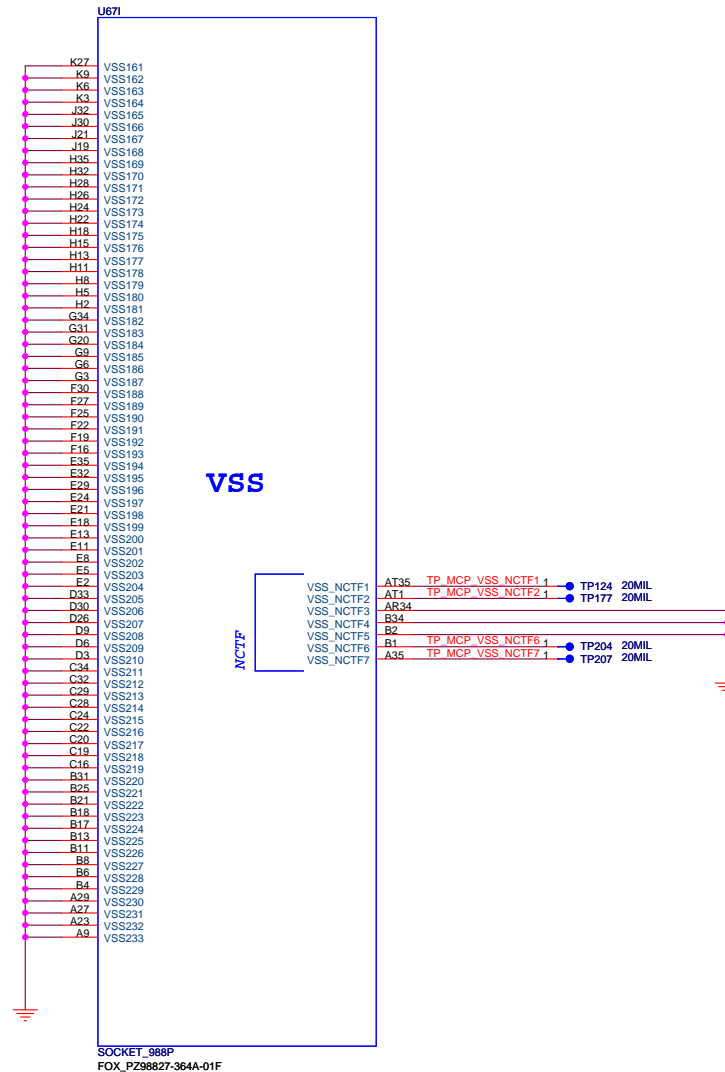
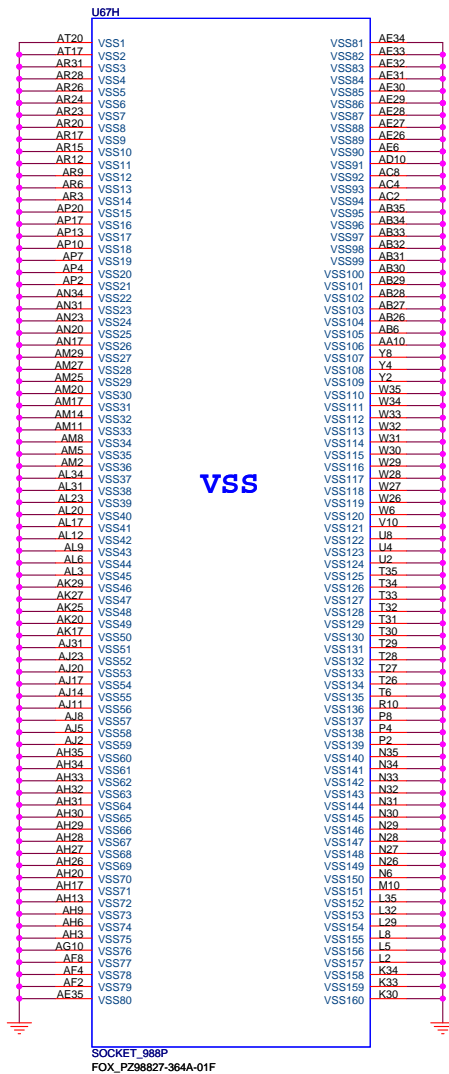
POWER
CPU VIDS

SENSE LINES

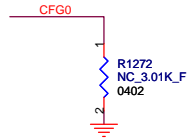


For Disable Auburndale Graphic
VAXG should be connected to GND when disable iGPU.

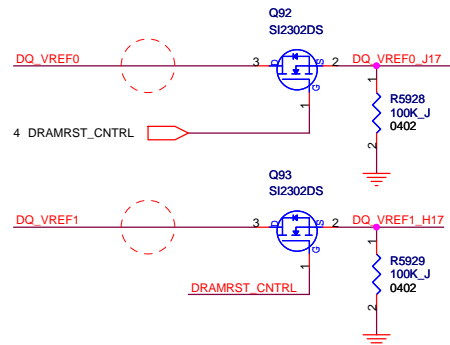
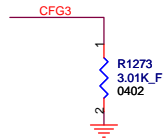




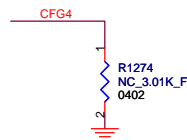
PCI Express Configuration Select
CFG0 1 : Single PEG
0 : Bifurcation enable



CFG3 PCI Express Static Lane Reversal
CFG3 1 : Normal Operation
0 : Lane Numbers Reversed
15 -> 0 , 14 -> 1 , ...

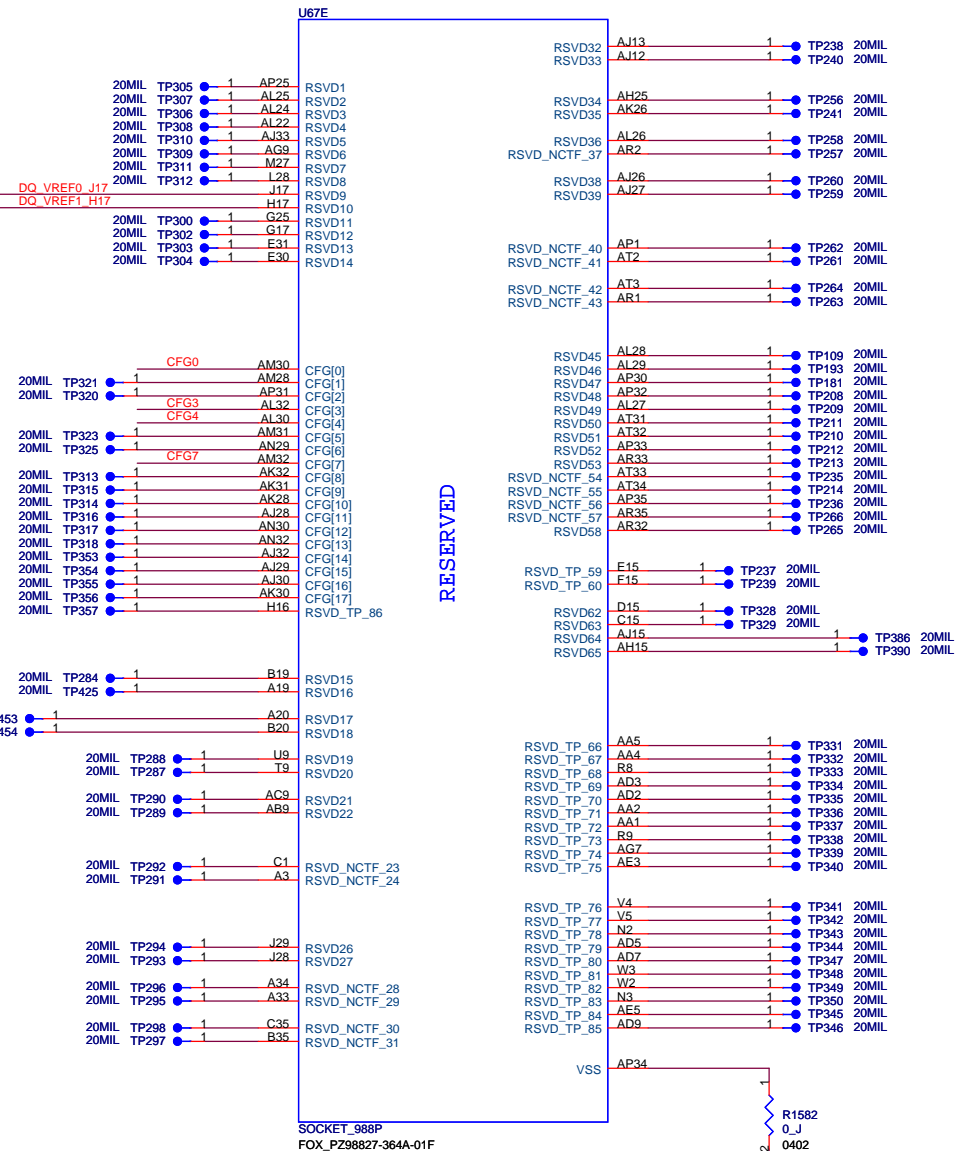
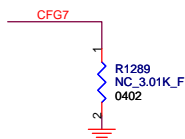


CFG4 Display Port Presence
CFG4 1 : Disabled ; No Physical Display Port
attached to Embedded Display Port
0 : Enable ; An external Display Port device
is connected to the Embedded Display Port



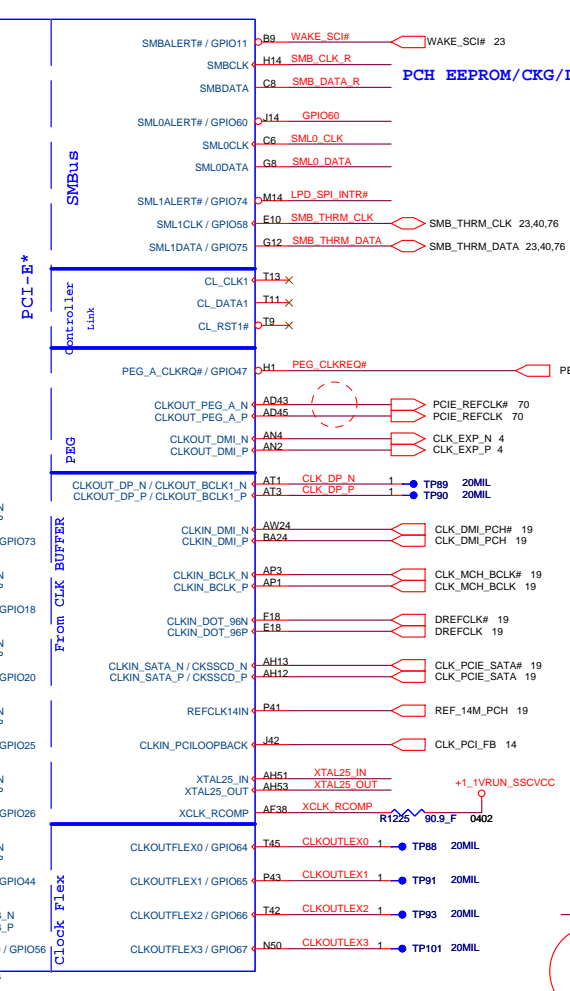
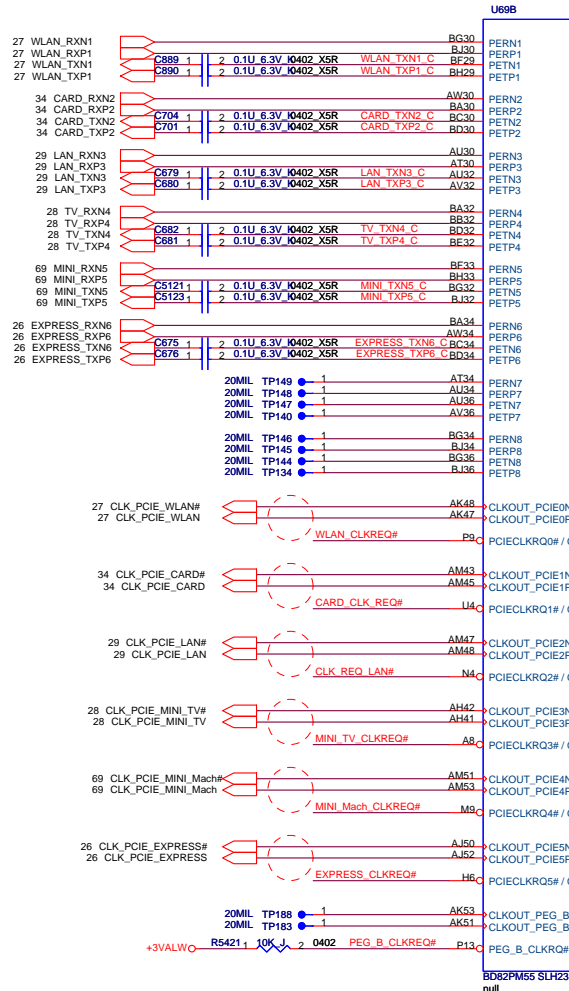
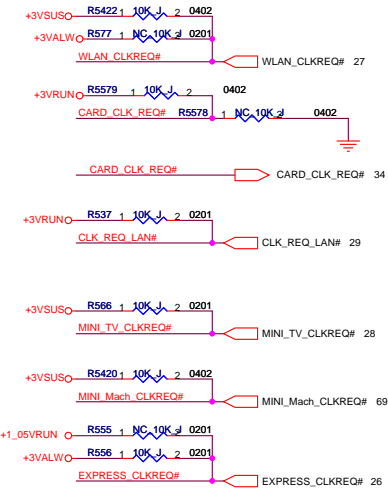
2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down). Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.

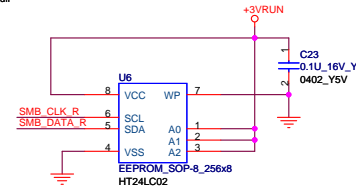
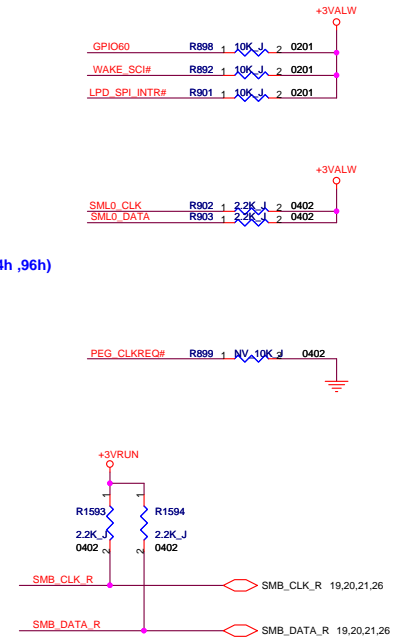


PCI-E Port Table

Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	ISDB-T Tuner (JP)
Port5	Mach
Port6	ExpressCard/34 (PCIE)
Port7	NC
Port8	NC

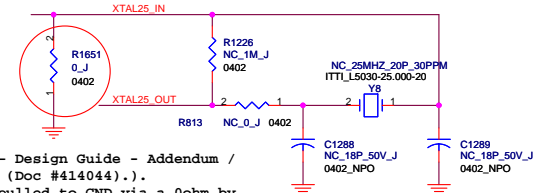


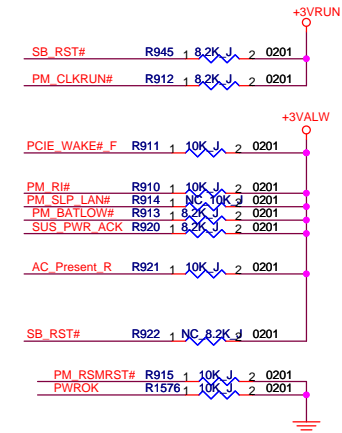
EC / ALS / dGPU
(SMBus Address: 94h, 96h)



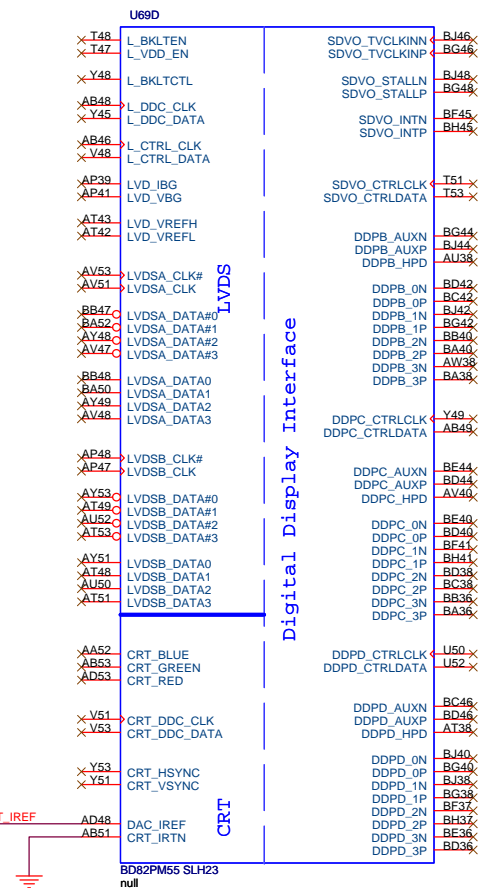
SMBus Address: AEH

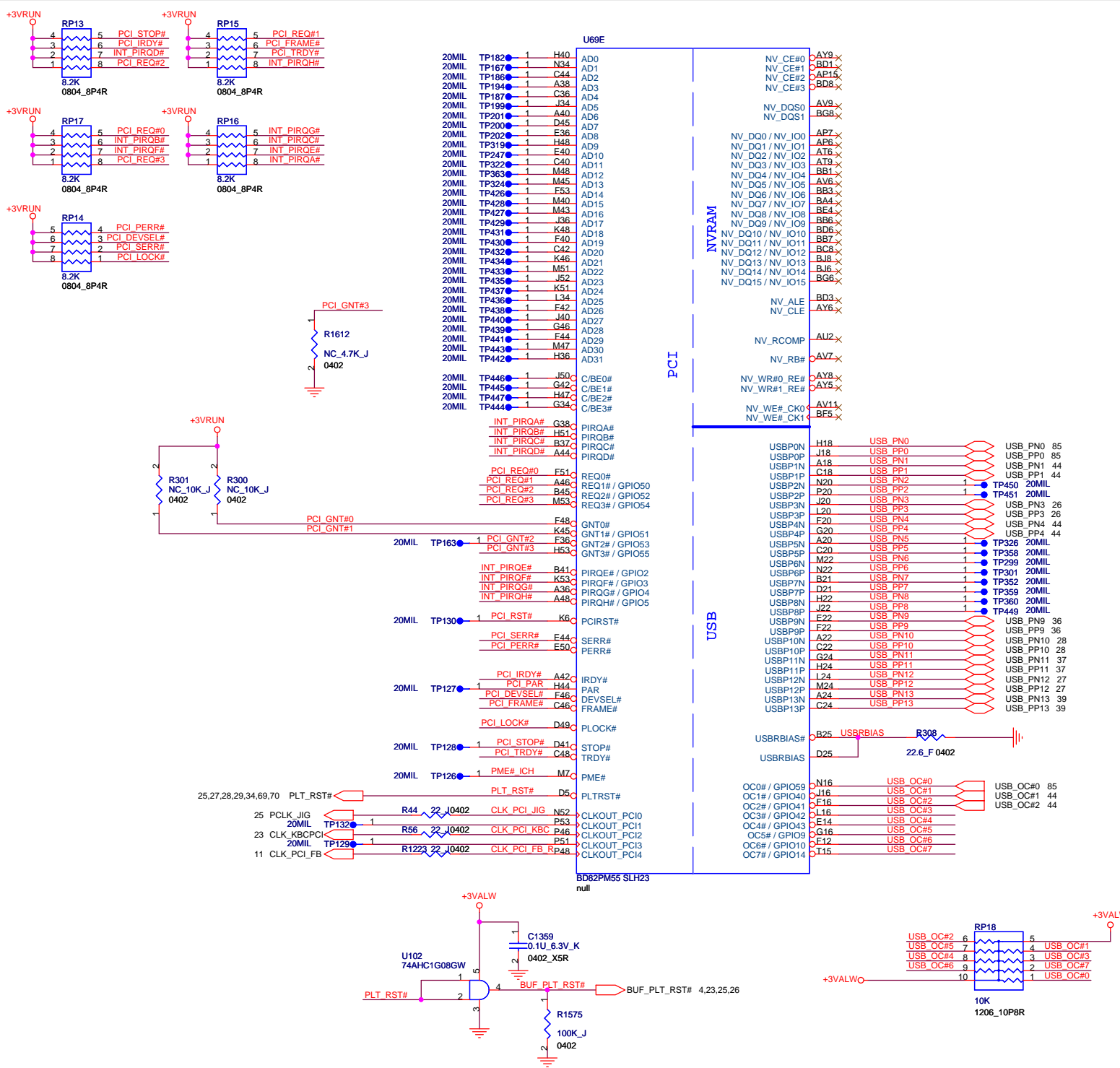
Calpella Platform - Design Guide - Addendum /
Update - Rev. 1.52 (Doc #414044).
XTAL_IN should be pulled to GND via a 0ohm by
default.
This pull-down resistor on XTAL_IN should only
be un-stuffed when 25MHz crystal is used.





Calpella Platform - Design Guide - Addendum
/ Update - Rev. 1.52 (Doc #414044).).



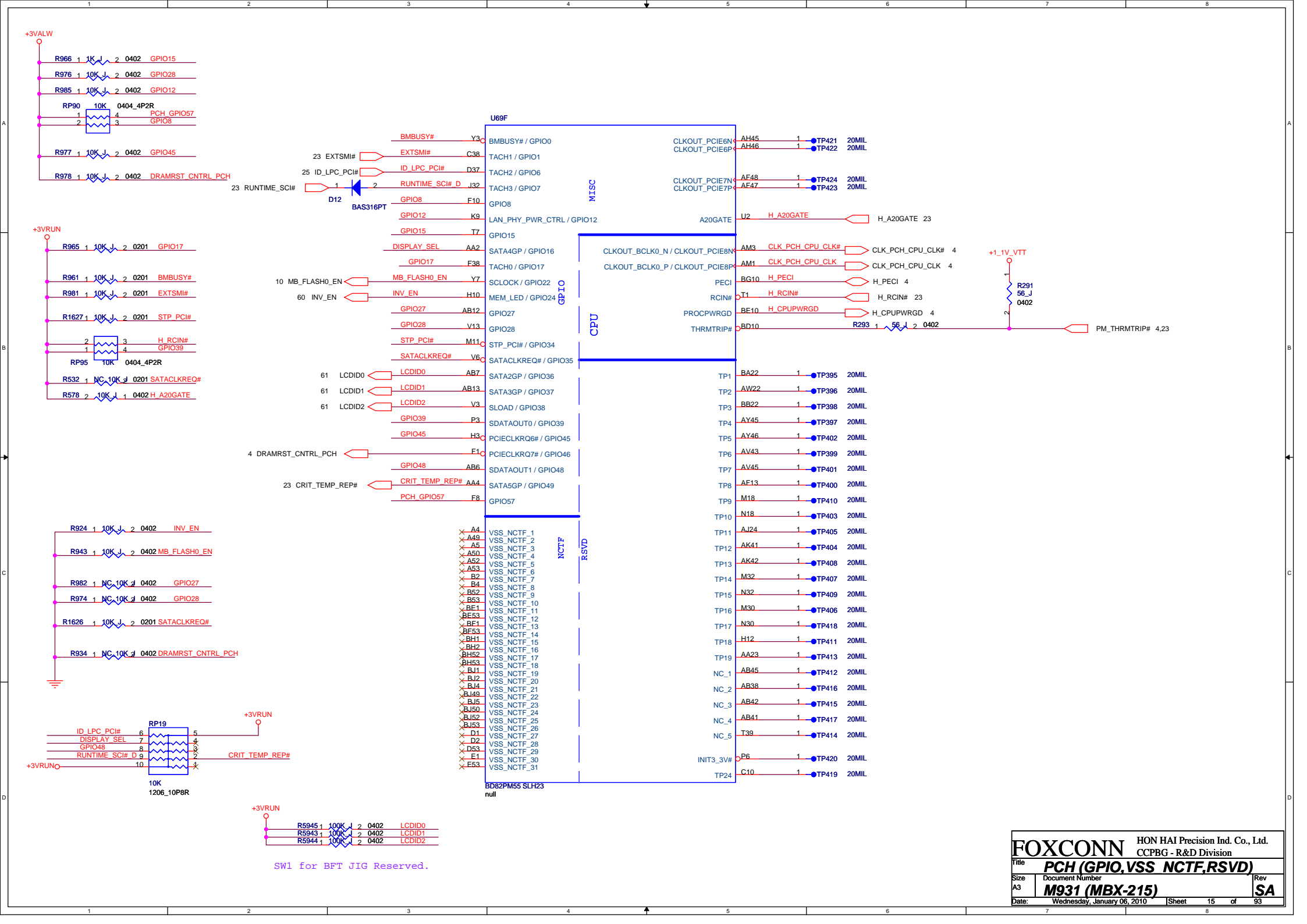


DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

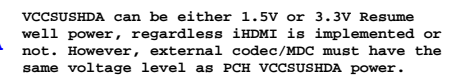
Intel Anti-Theft Technology
Disabled when Low , NC R1616
Enabled when High , Stuff R1616

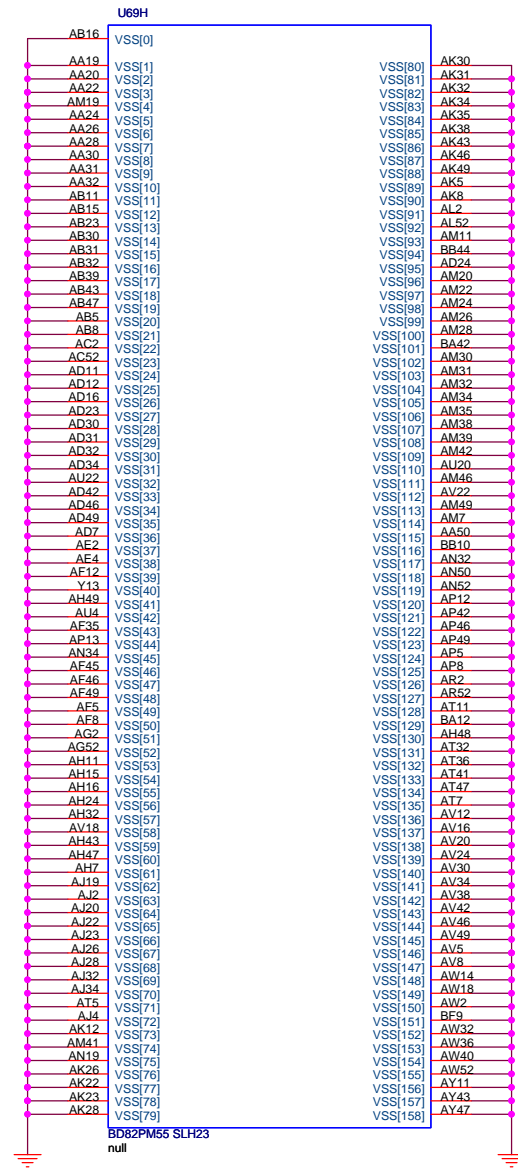
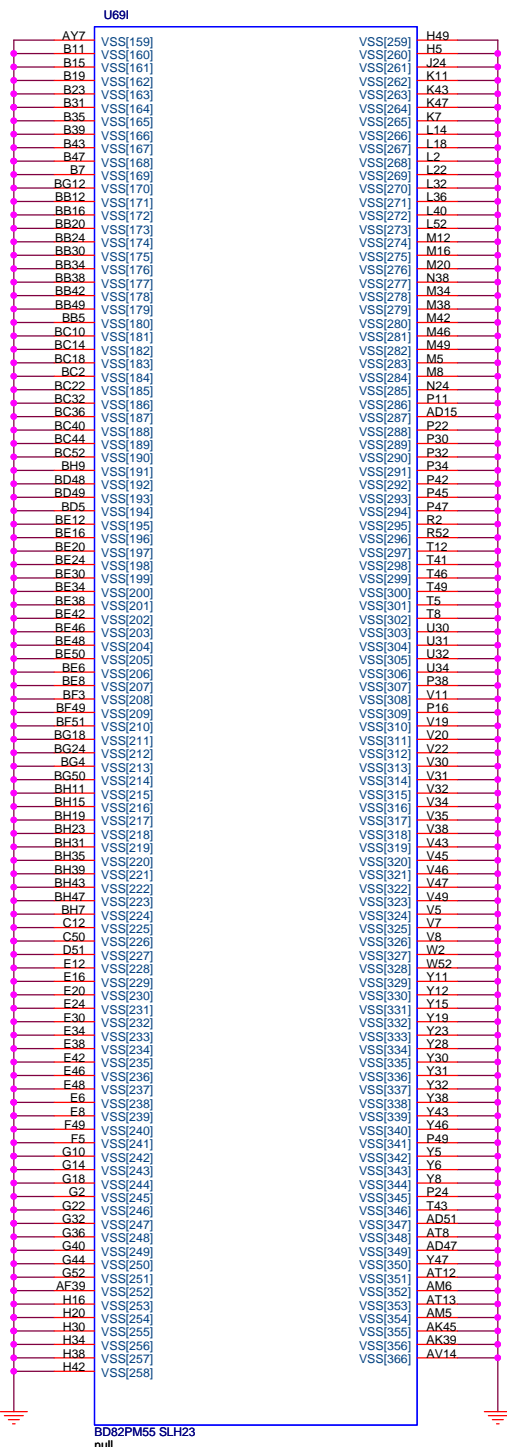
USB PORT	Function
PORT-0	On Board Port
PORT-1	External Port
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port
PORT-5	
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	IR Receiver (JP)
PORT-11	Felica
PORT-12	Wireless LAN (WiMAX)
PORT-13	Bluetooth

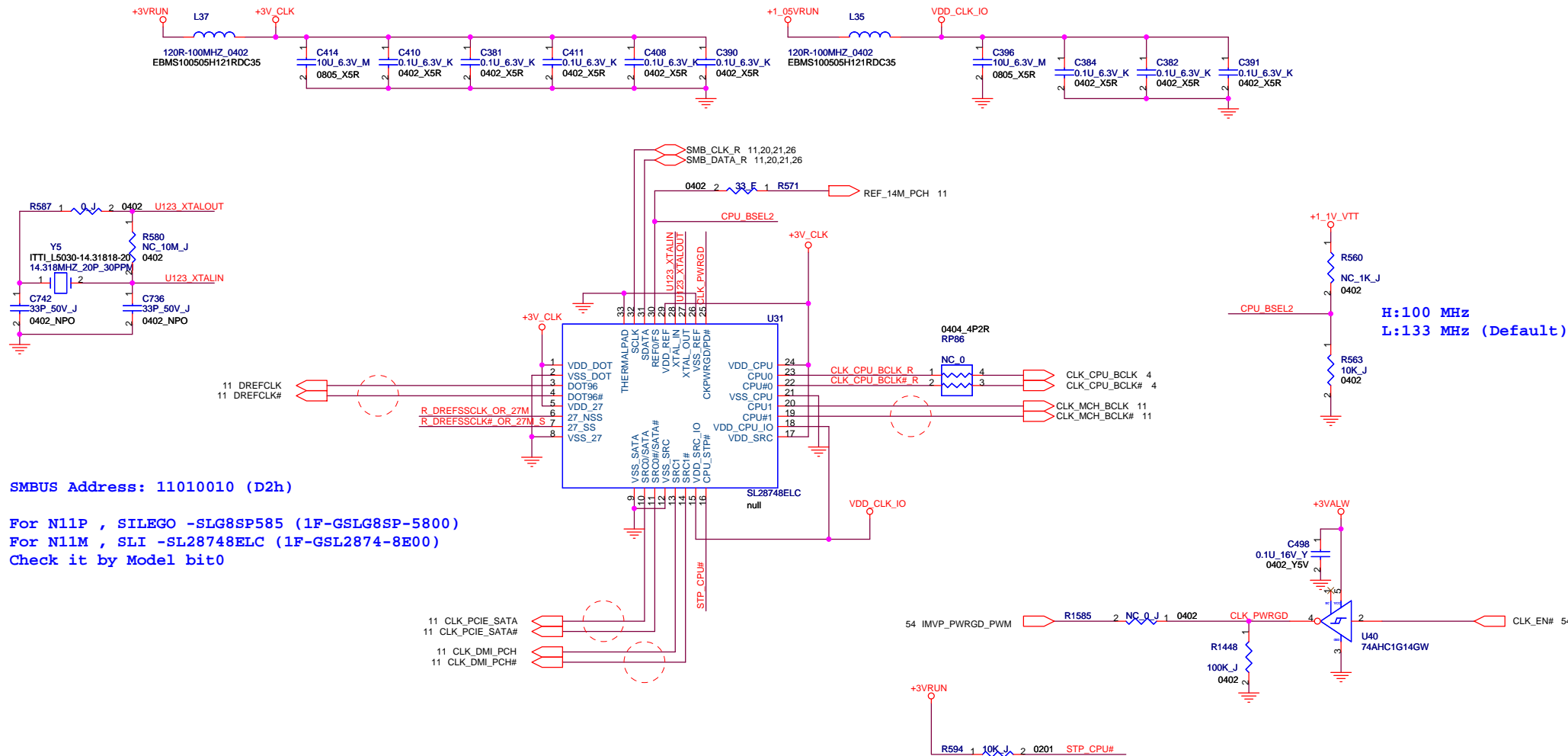
Buffer to reduce loading on PLT_RST#.

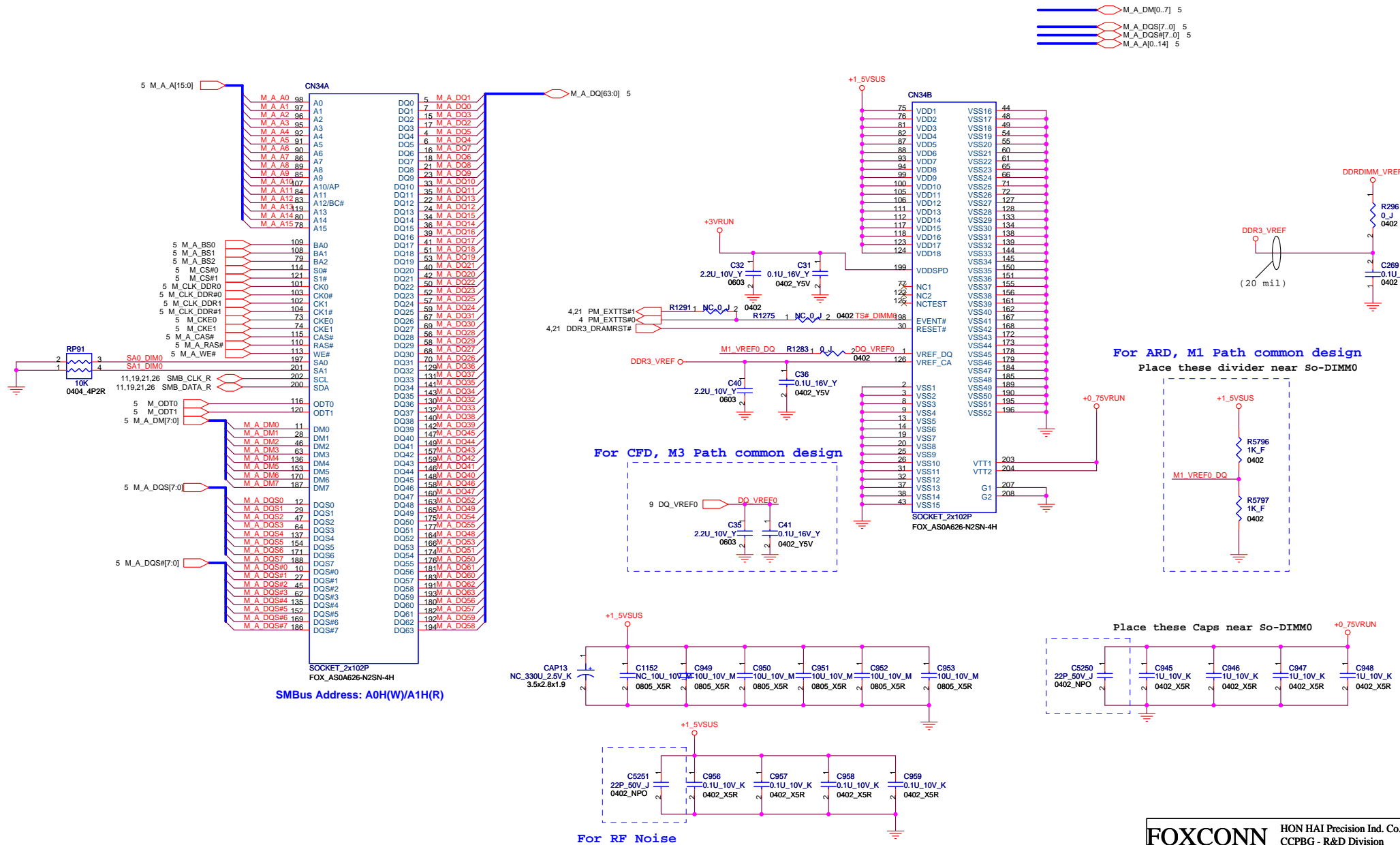


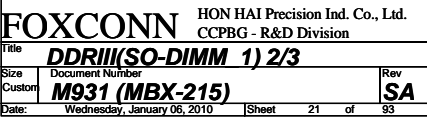
For Disable Auburndale Graphic
GPIO27 floating as Internal VRM and there is no need external supply



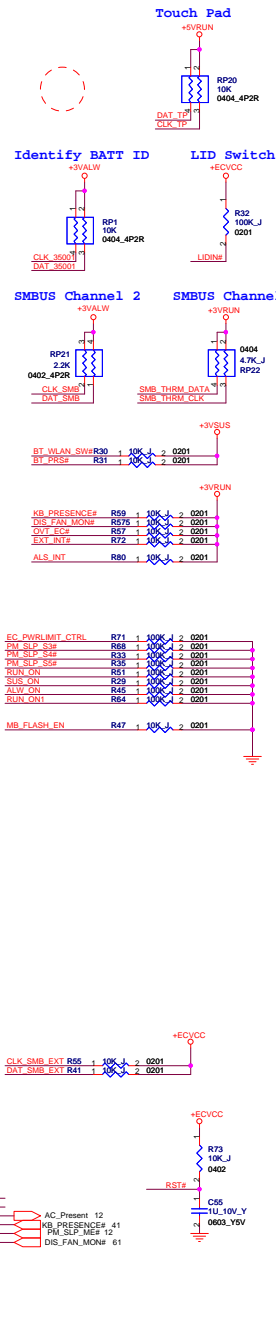






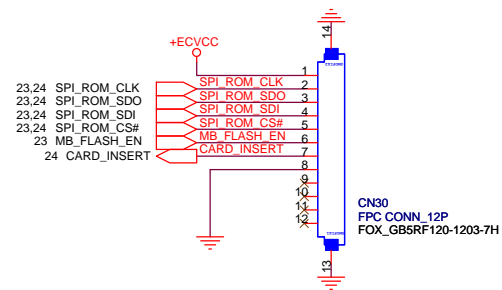


Delete M2 Path (Intel Revised)



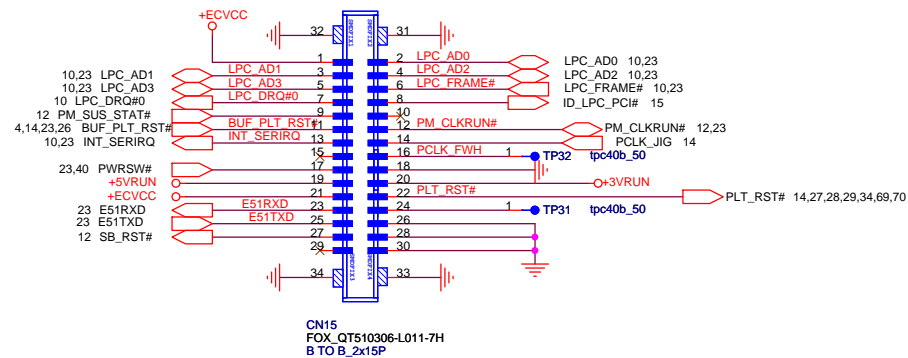
ID1	ID0	Model Name
0	0	M930
0	1	M931
1	0	Reserve
1	1	Reserve



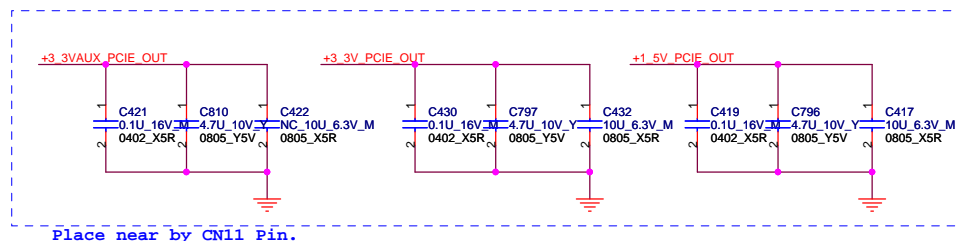
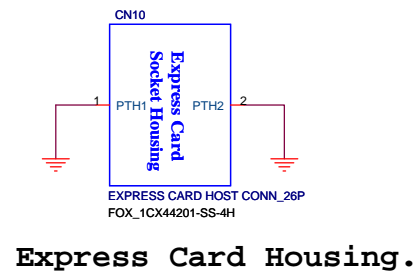
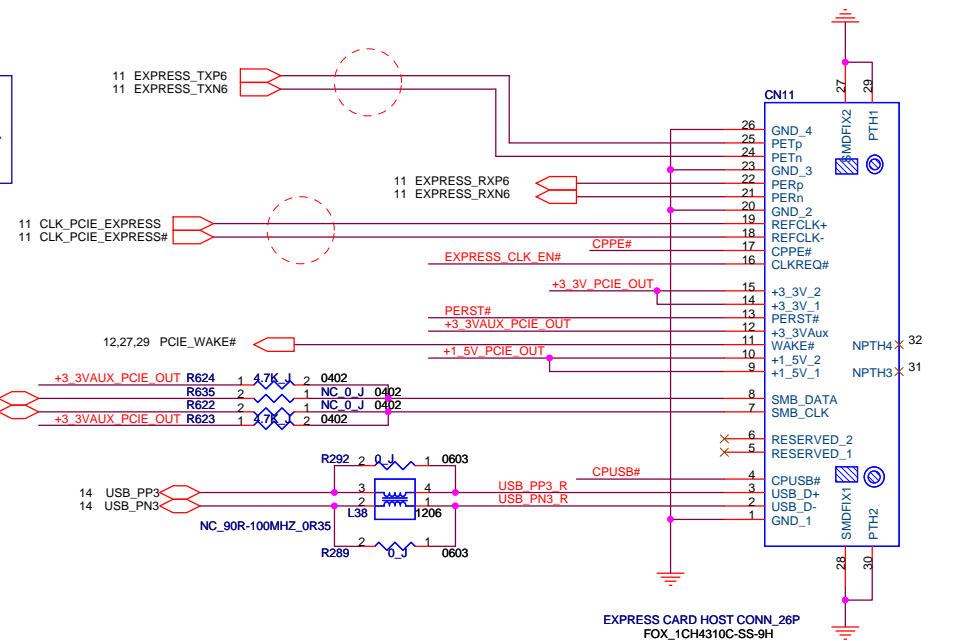
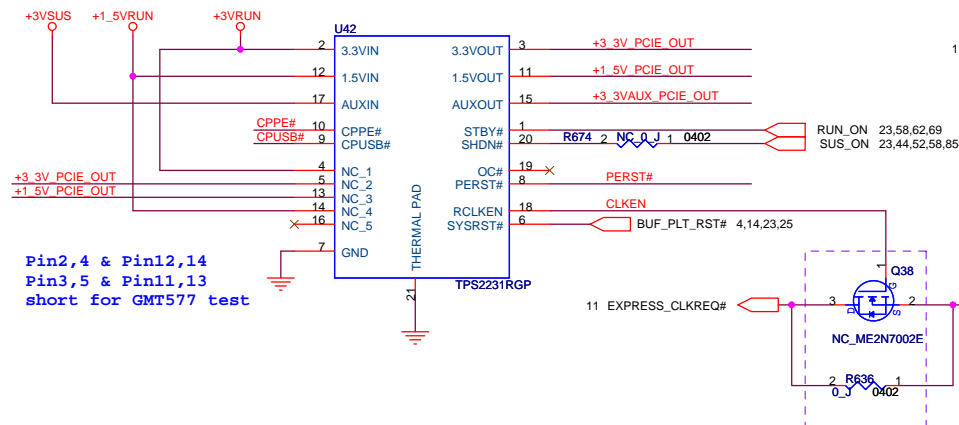


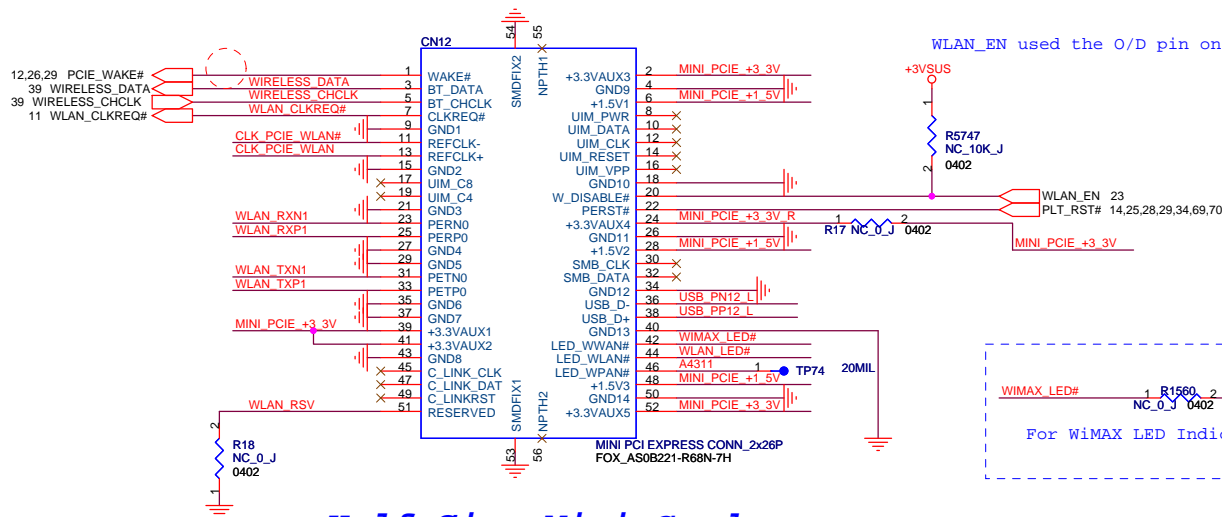
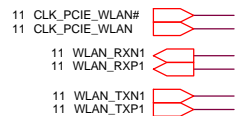
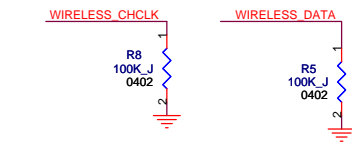
EXTERNAL SPI ROM INTERFACE (EC)

For MP, Dummy R43, C20 ,U3 ,CN30 and Stuff R775



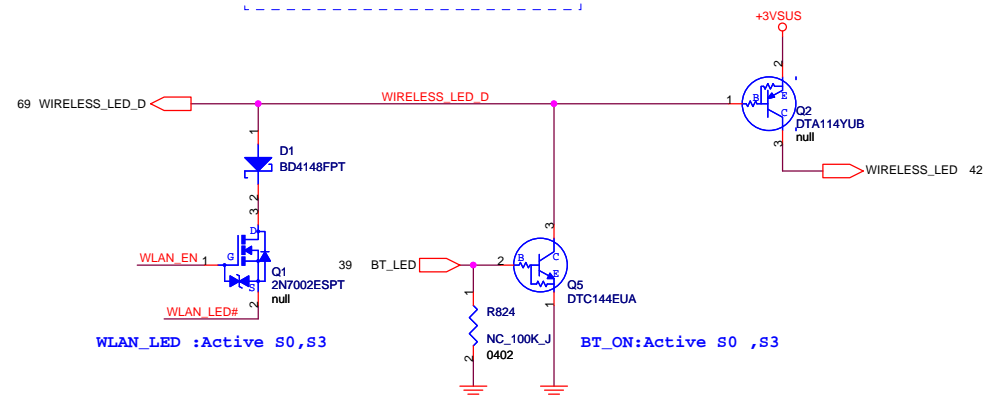
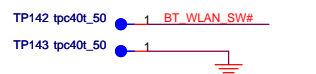
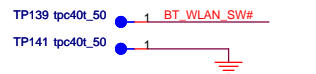
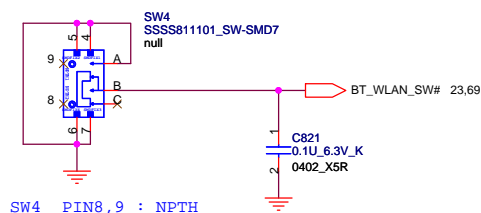
JIG-120



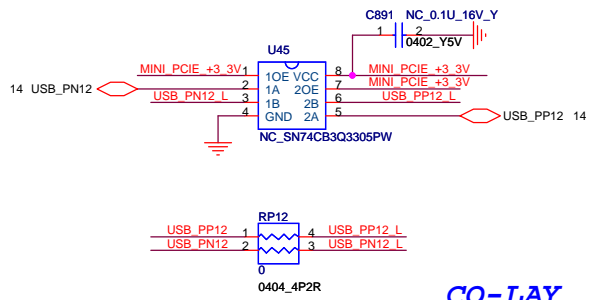


Half Size Mini Card

WLAN Switch



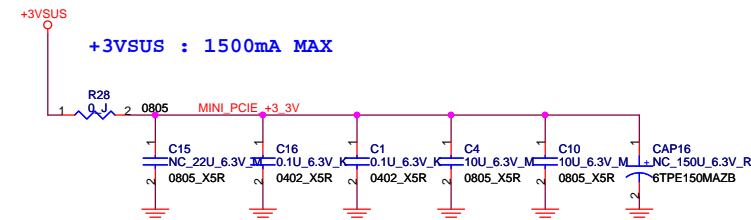
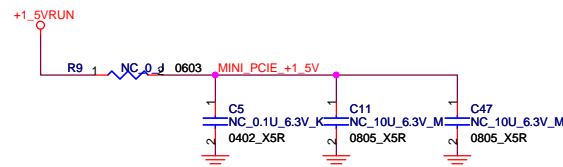
USB I/F for Wi-MAX(Kilmer Peak)

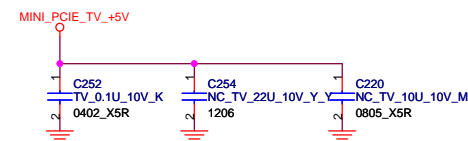
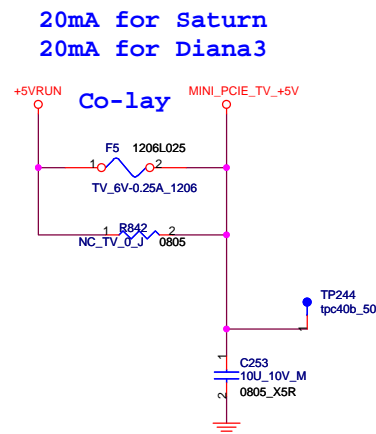
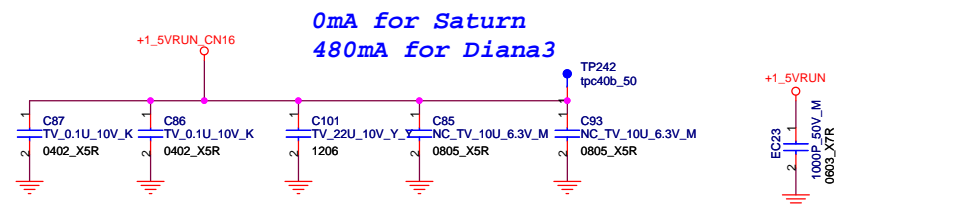
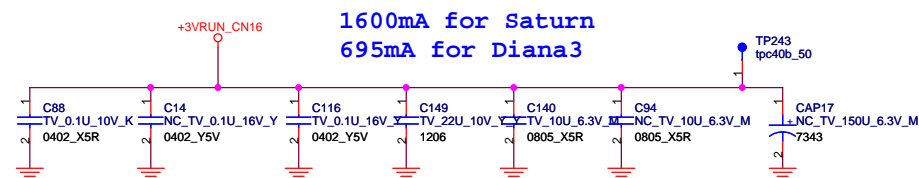
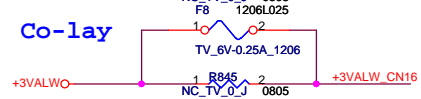
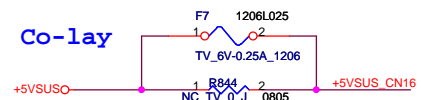
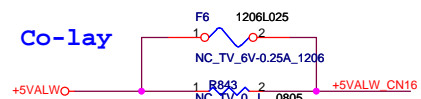
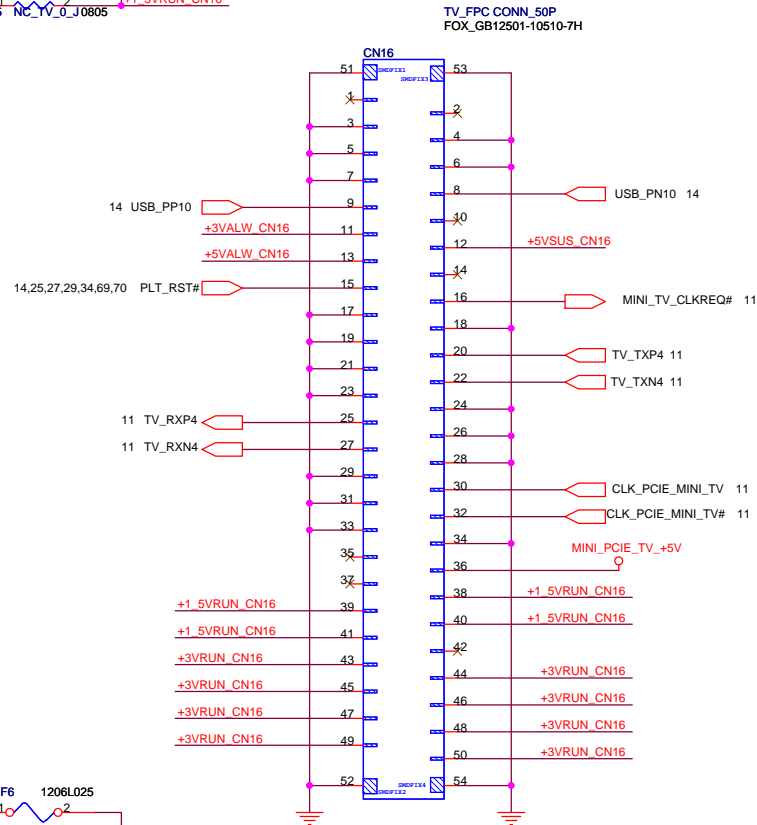
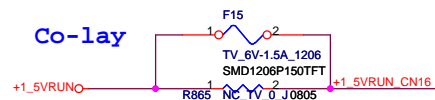
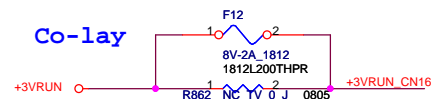


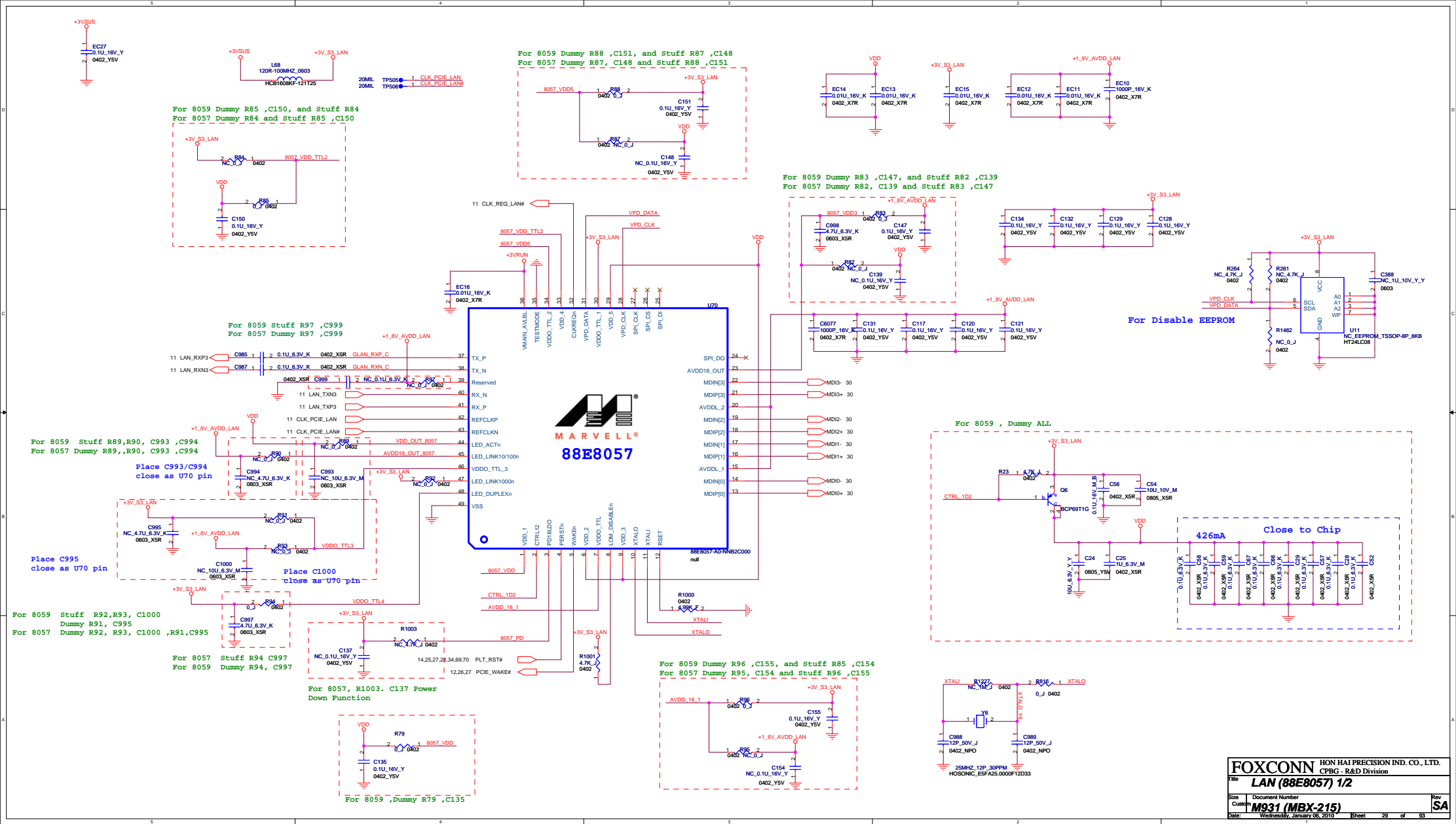
CO-LAY

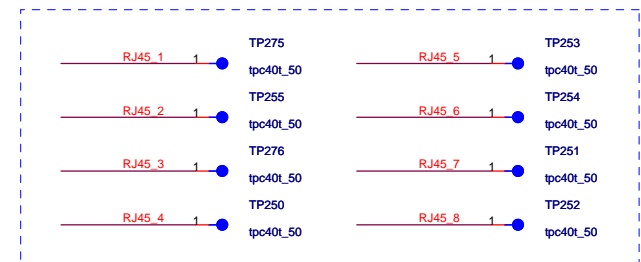
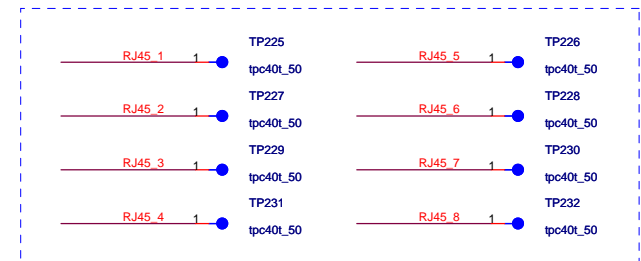
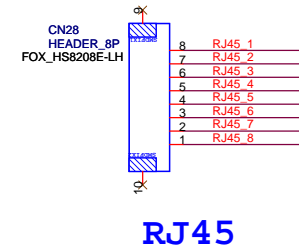
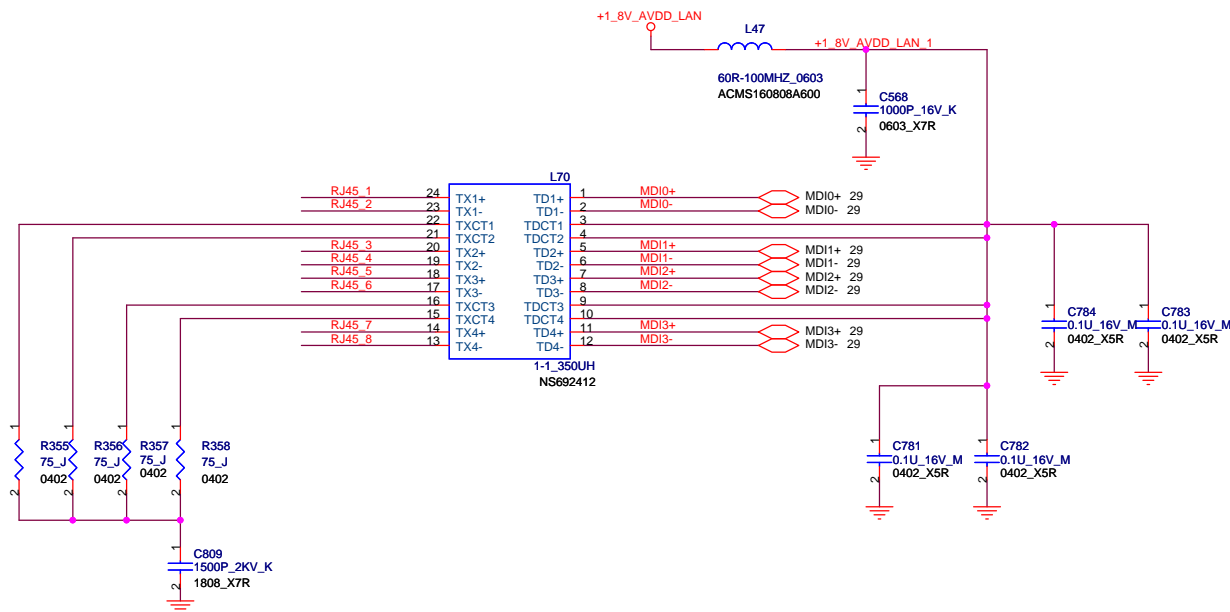
+1_5VRUN : 330mA MAX

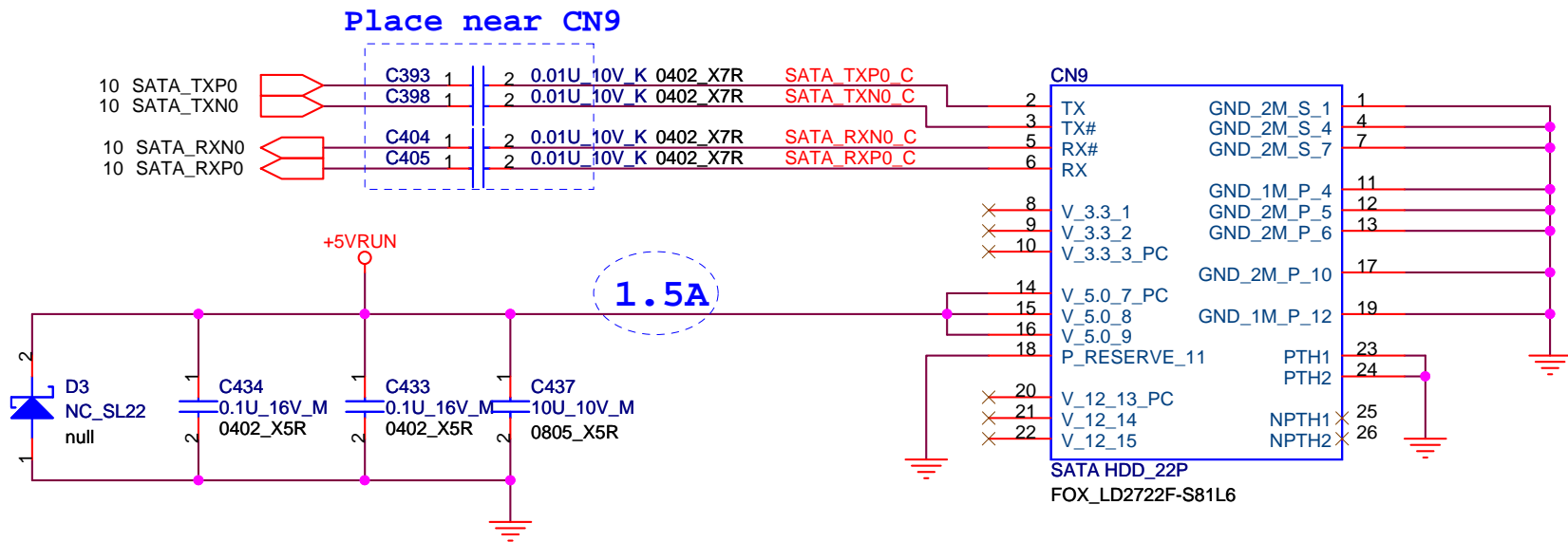
Intel Puma Peak & Kilmer Peak nonsupport +1_5VRUN





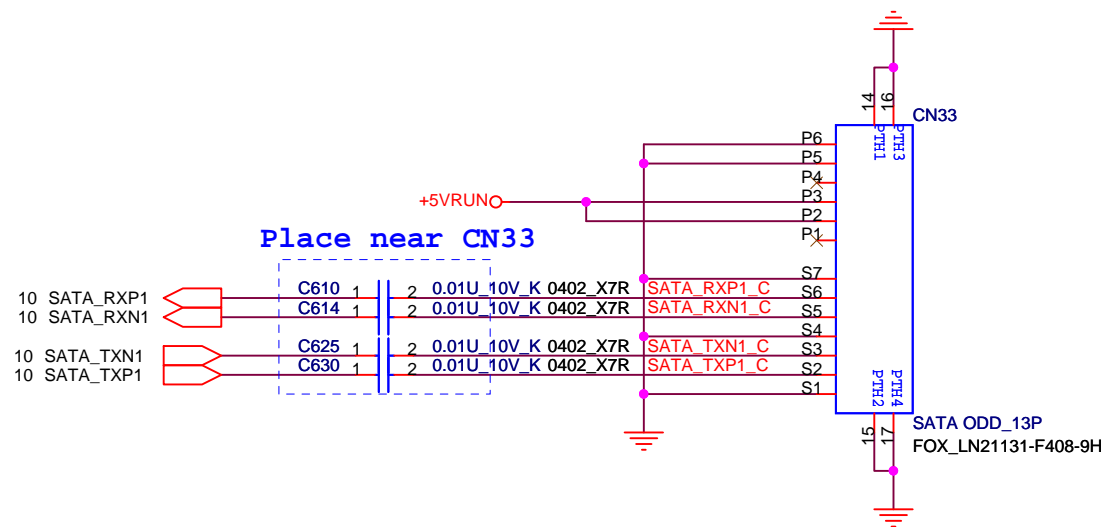




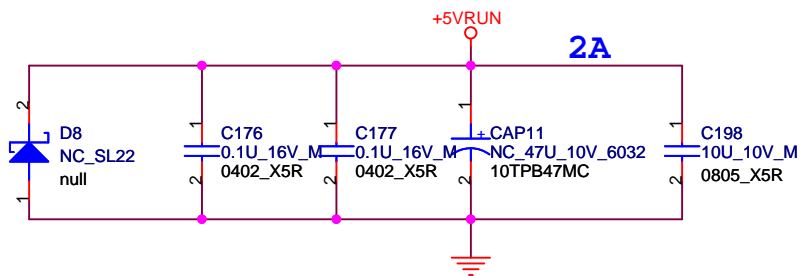


SATA HDD CONN

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title SATA HDD			
Size A	Document Number M931 (MBX-215)		Rev SA
Date:	Wednesday, January 06, 2010	Sheet	31 of 93



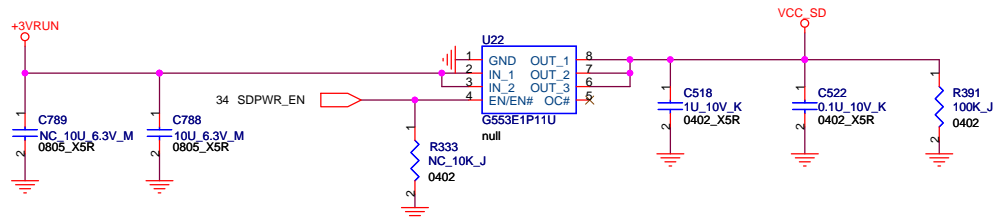
SATA ODD CONN



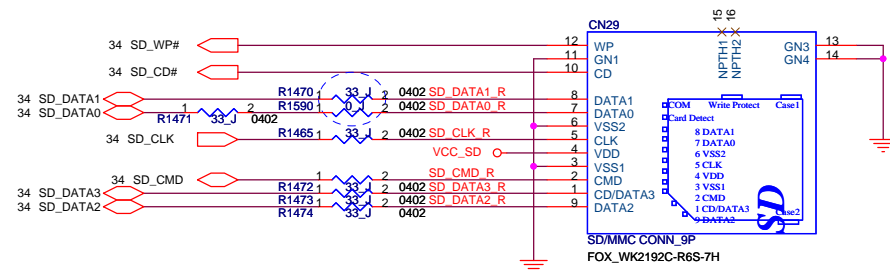
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title SATA ODD			
Size	Document Number		Rev
A4	M931 (MBX-215)		SA
Date:	Wednesday, January 06, 2010	Sheet	32 of 93

Remove Braidwood (Intel Updated and MOR confirmed)

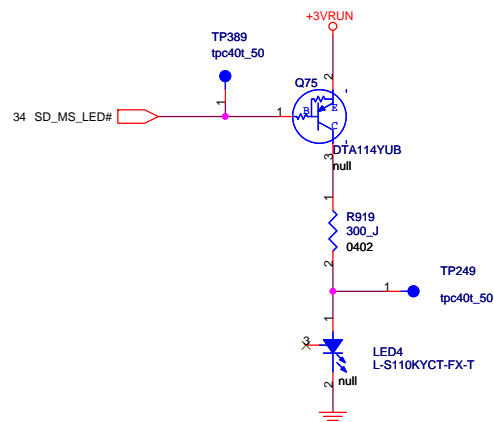
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title Braidwood Connector			
Size	Document Number		Rev
Custom	M931 (MBX-215)		SA
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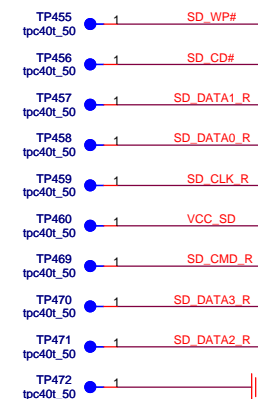
SD POWER



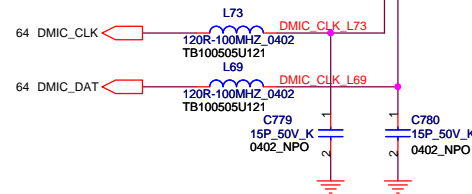
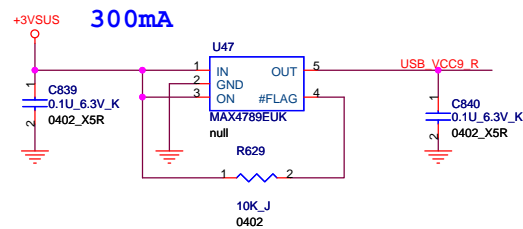
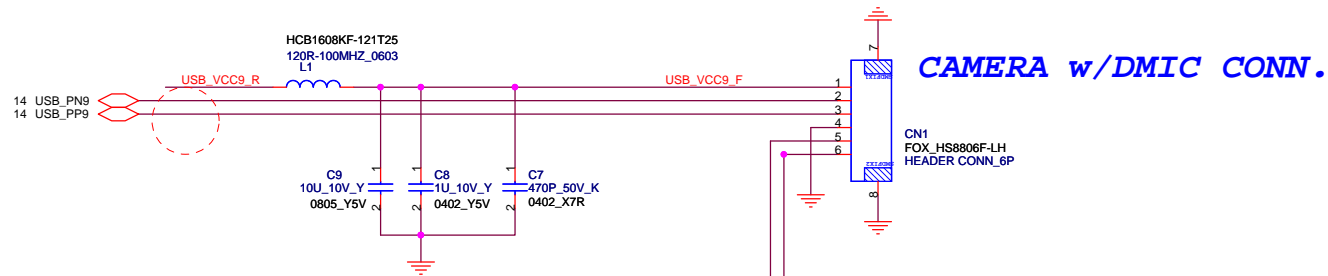
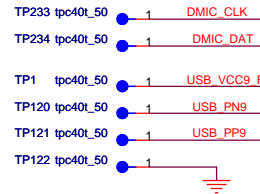
SD CONN.

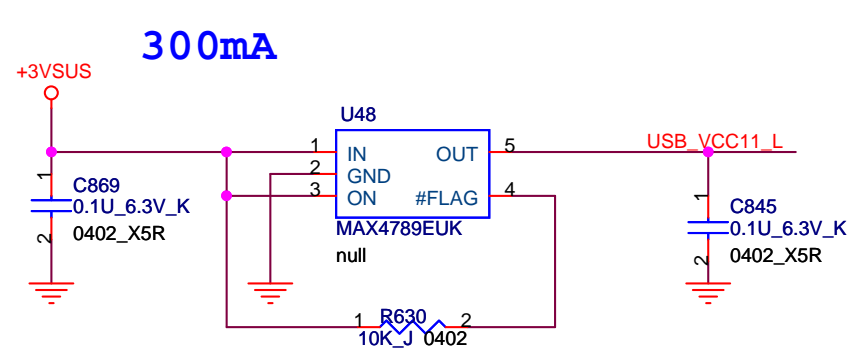
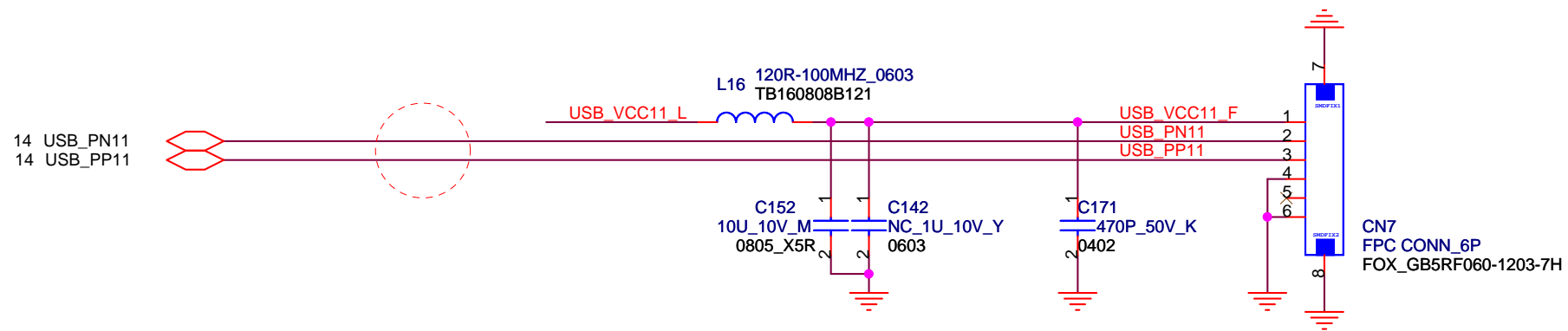


SD/MS LED

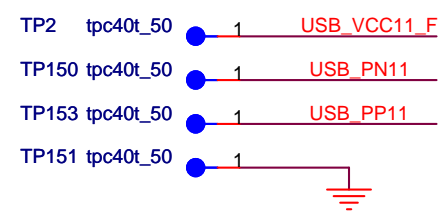


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title PCIE (SD) 2/2		CCPBG - R&D Division	
Size	Document Number	Rev	
Custom	M931 (MBX-215)	SA	
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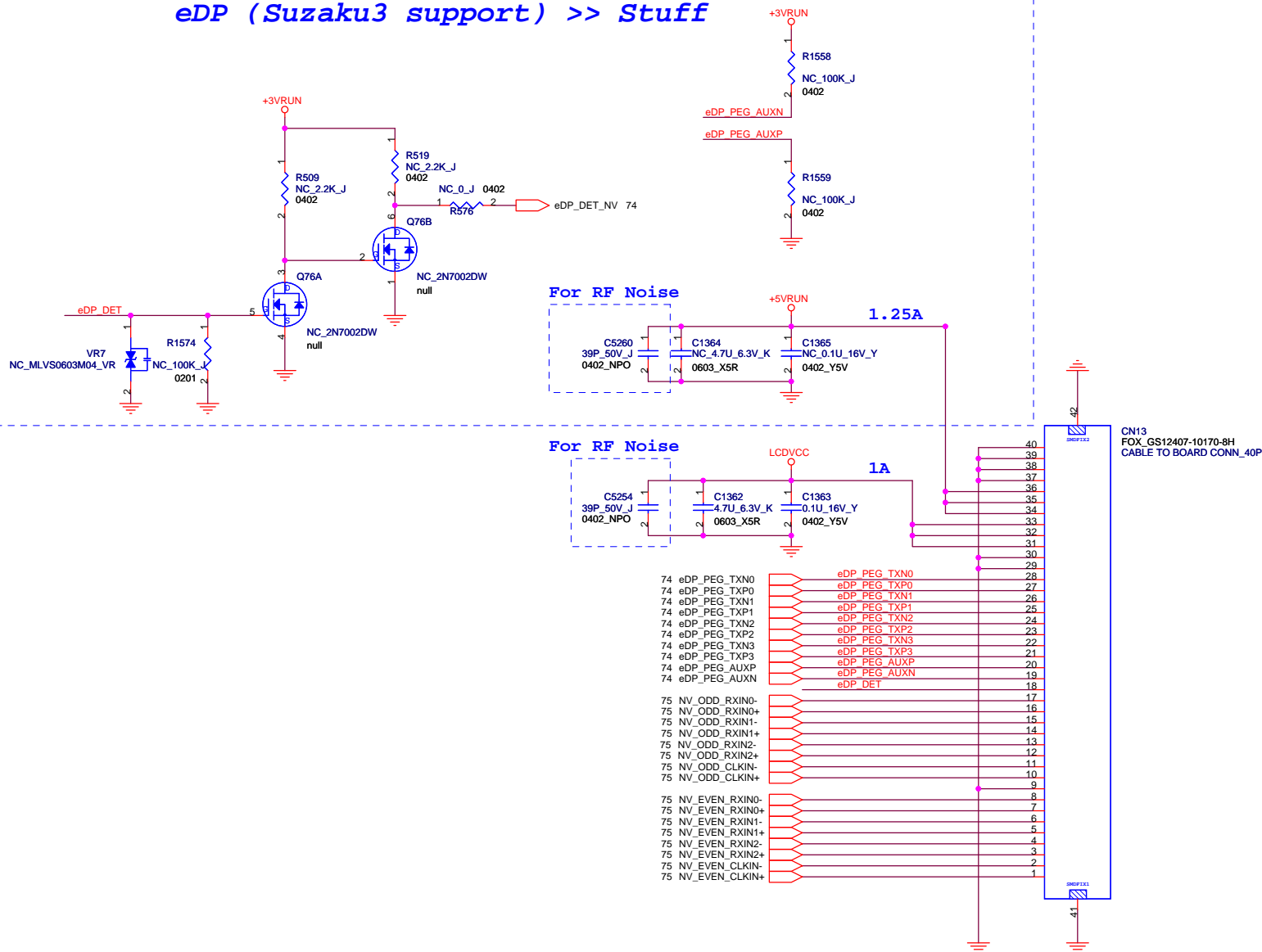
Felica Conn.
Felica Vdd Spec. (3.15V to 3.45V)



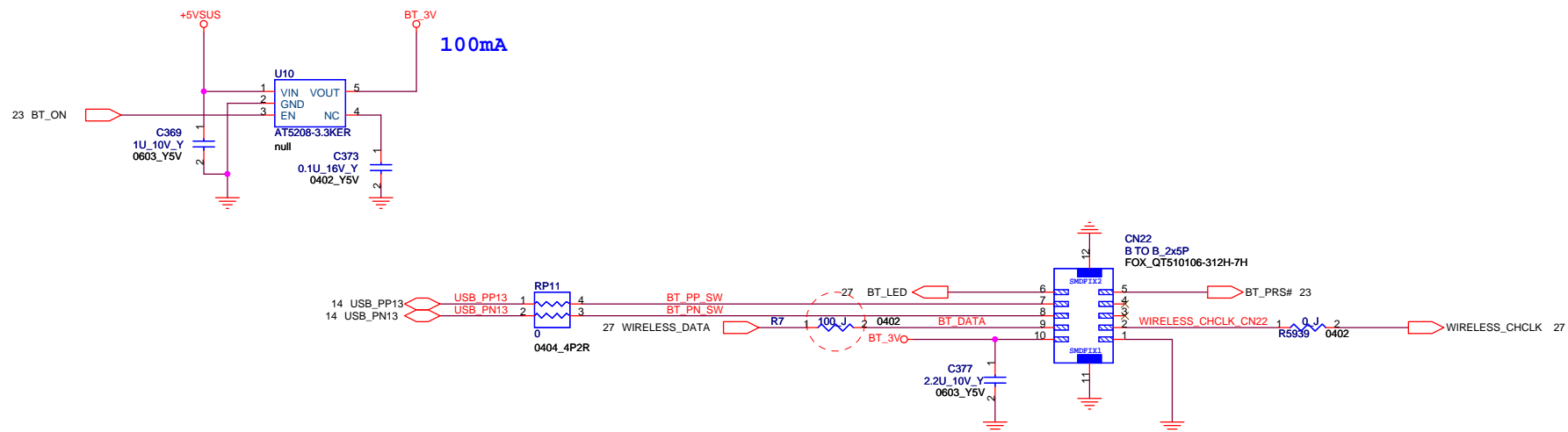
Current Limit Switch

FOXCONN		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title Felica Connector			
Size A	Document Number M931 (MBX-215)		Rev SA
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eDP (Suzaku3 support) >> Stuff



eDP & LVDS CONNECTOR

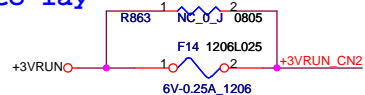


Place C377 close to CN22, Pin10

Bluetooth CONN.

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Size		Document Number	
Custom		M931 (MBX-215)	
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Co-lay



Light Sensor (EC)

Switch Keyboard Matrix

Keyboard LED

Power Button

11,23,76 SMB_THRM_DATA
11,23,76 SMB_THRM_CLK
23 ALS_INT

23 KSO18
23,41 KSI0
23,41 KSI1
23,41 KSI2
23,41 KSI3
23,41 KSI4
23,41 KSI5
23,41 KSI6
23,41 KSI7

NUMLOCK_LED#_DB
SCRLOCK_LED#_DB
CAPLOCK_LED#_DB
POWER_LED_DB
SUSPEND_LED_DB

23,25 PWRSW#

CN2
FPC CONN_24P
FOX_GB5RF240-1203-7H

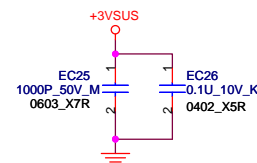
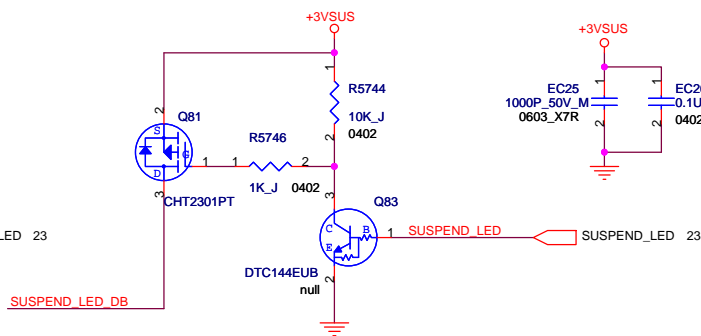
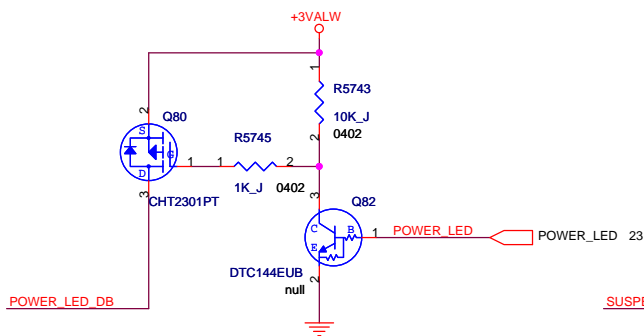
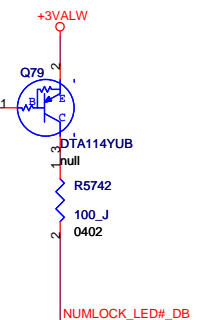
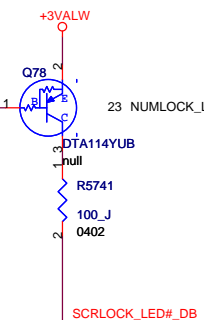
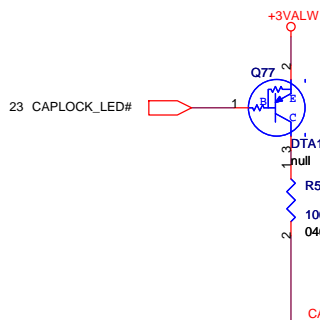
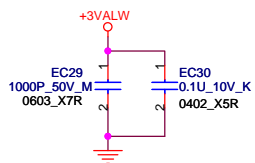
Switch DB Conn.

TP385 tpc40b_50 1 PWRSW#
TP376 tpc40b_50 1

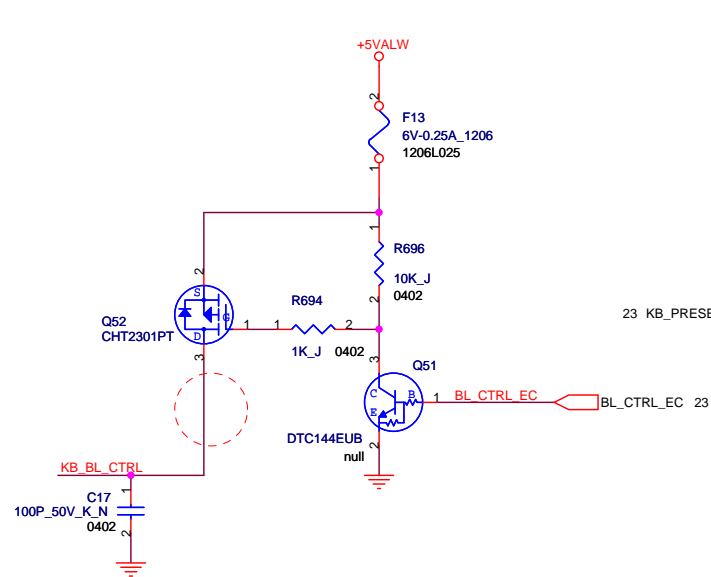
Top side ,Closer together

TP462 tpc40b_50 1 PWRSW#
TP384 tpc40b_50 1

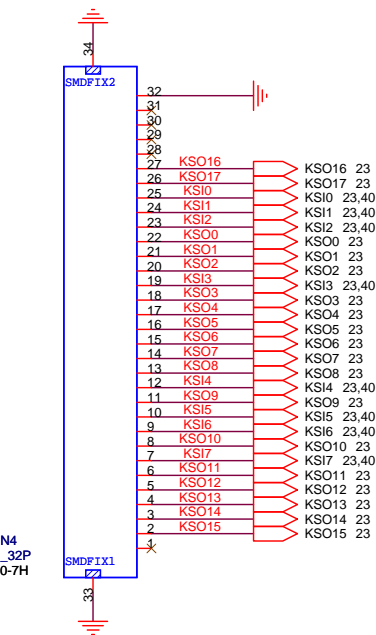
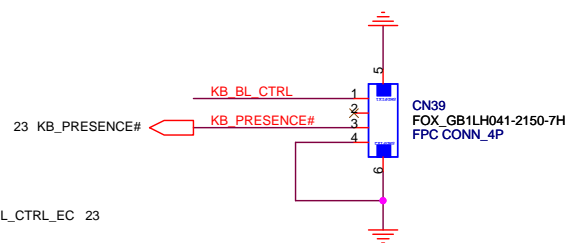
Bot side ,Closer together



FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	Switch DB Connector		
Size	Document Number		Rev
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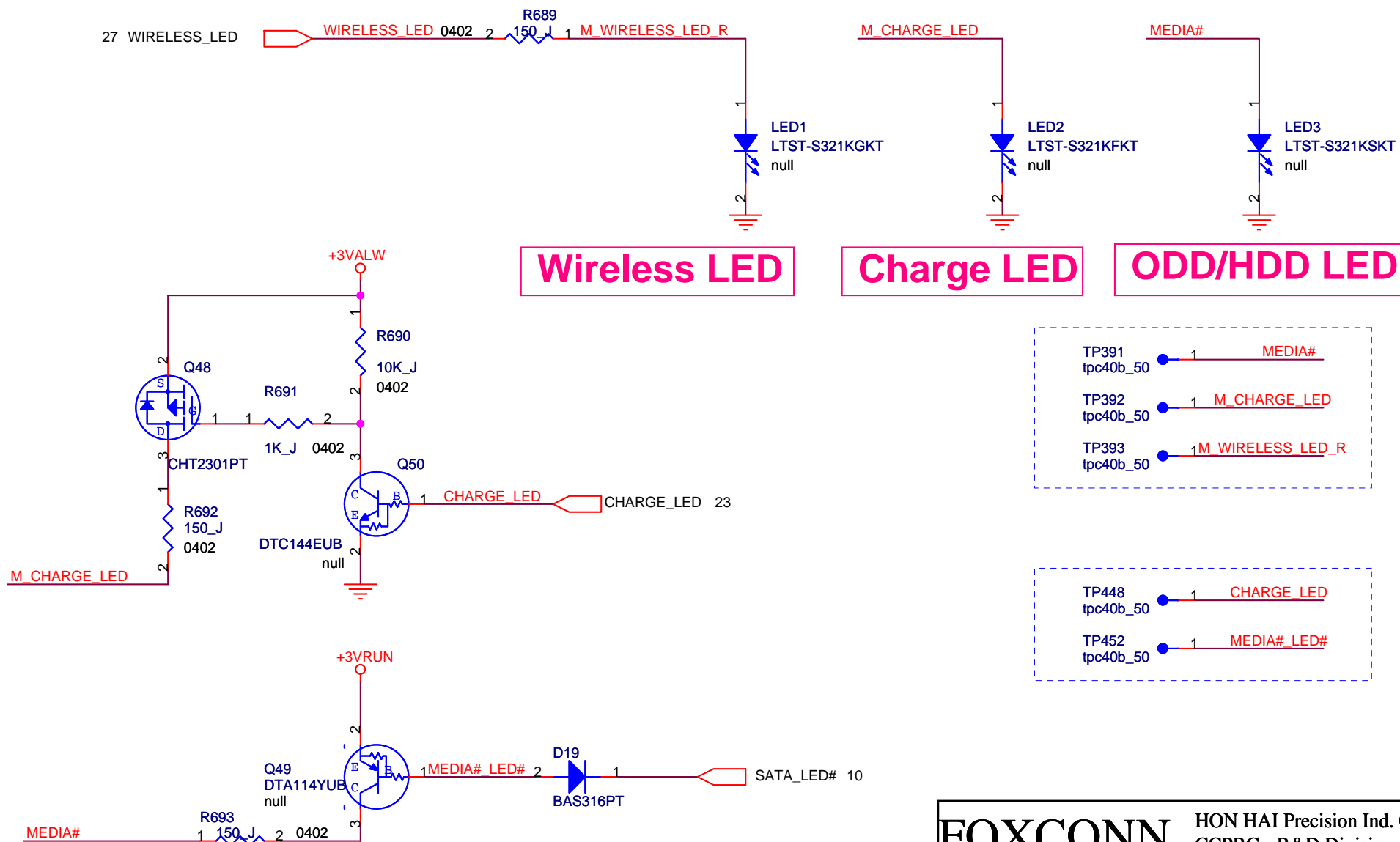
Backlit Power Conn



KBC Conn

KSI0	1	TP382	tpc40t_50
KSO10	1	TP381	tpc40t_50
KSI7	1	TP383	tpc40t_50
KSI2	1	TP394	tpc40t_50
KSO6	1	TP461	tpc40t_50

KSI0	1	TP280	tpc40t_50
KSO10	1	TP281	tpc40t_50
KSI7	1	TP282	tpc40t_50
KSI2	1	TP387	tpc40t_50
KSO6	1	TP388	tpc40t_50



FOXCONN

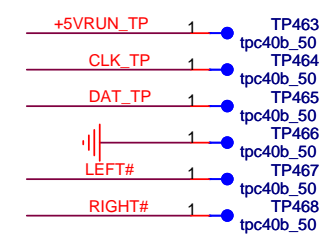
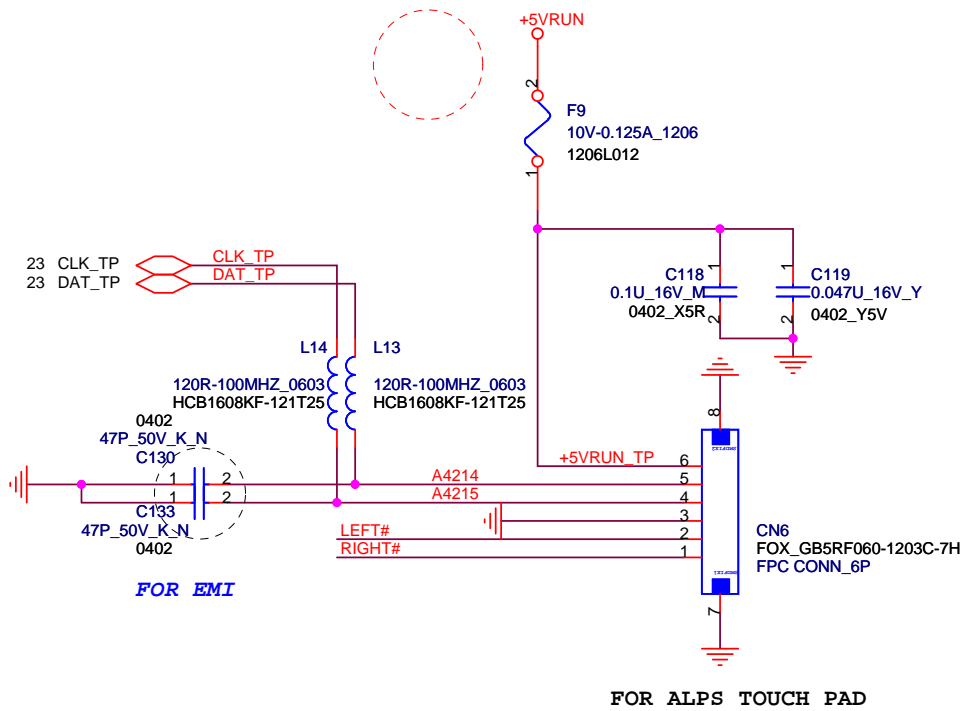
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title **Status LED**

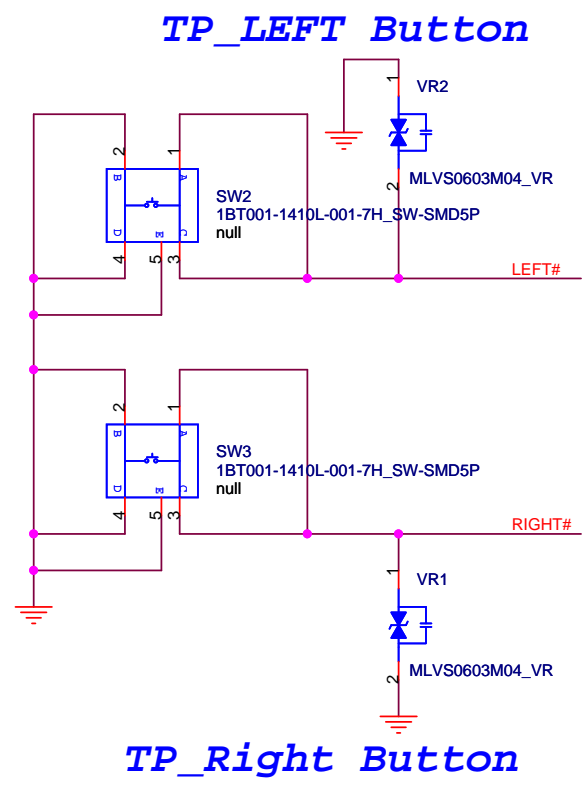
Size A Document Number **M931 (MBX-215)**

Rev **SA**

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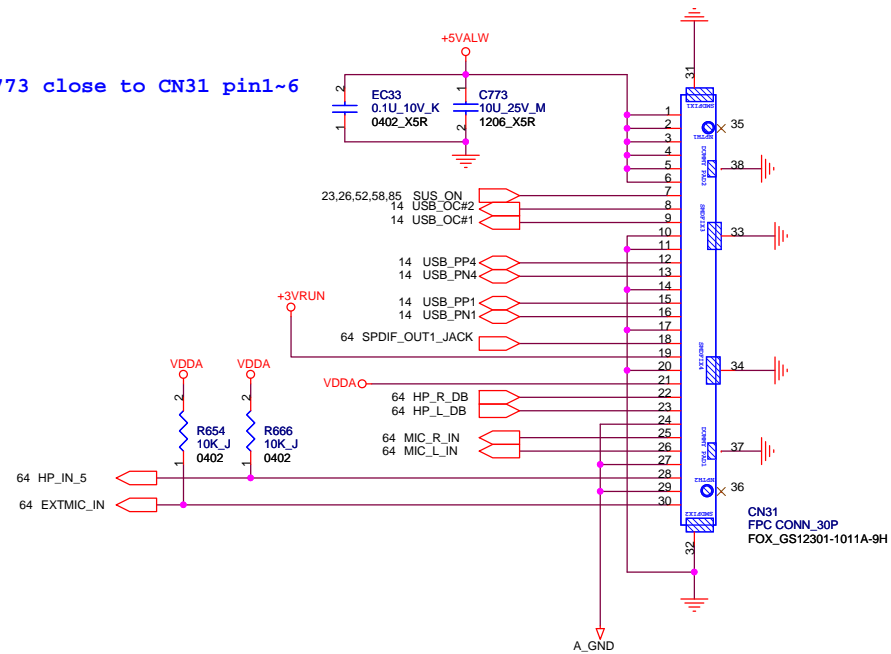


Touch Pad Conn **(Support Multi Touch)**



FOXCONN		HON HAI Precision Ind. Co., Ltd.
		CCPBG - R&D Division
Title Touch Pad		
Size	Document Number	Rev
Custom	M931 (MBX-215)	SA
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Place C773 close to CN31 pin1~6



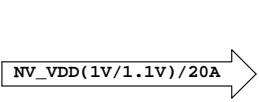
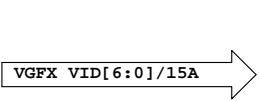
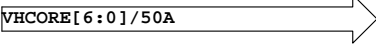
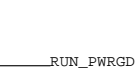
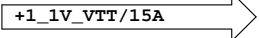
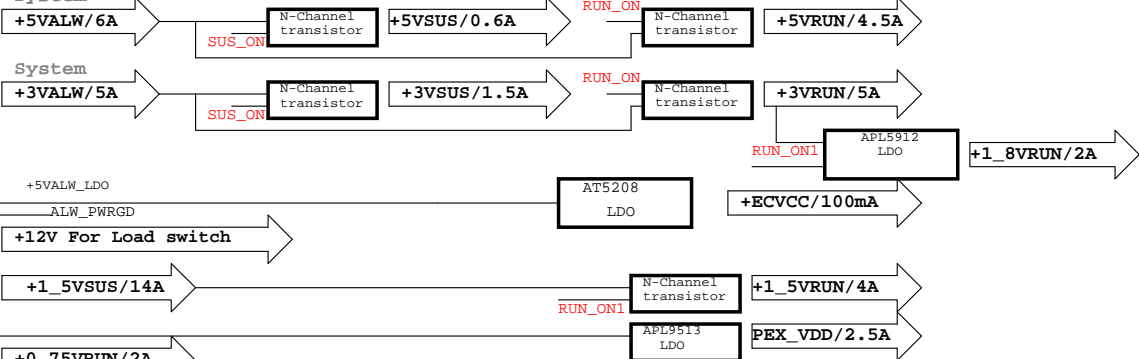
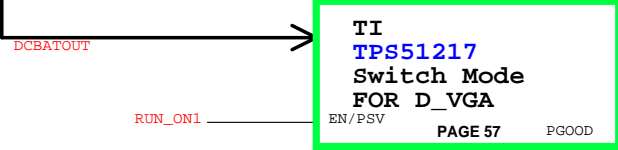
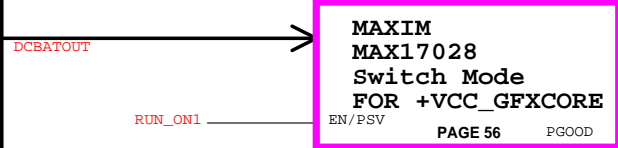
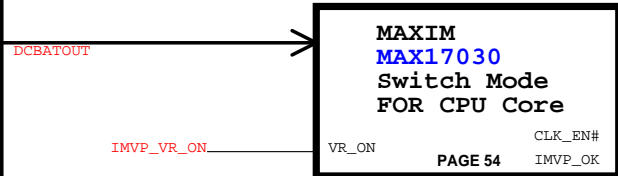
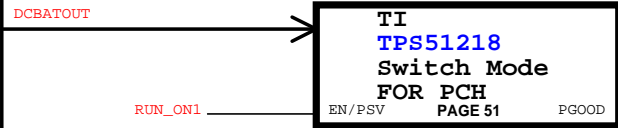
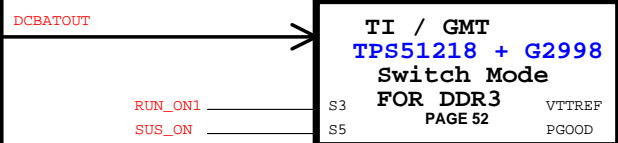
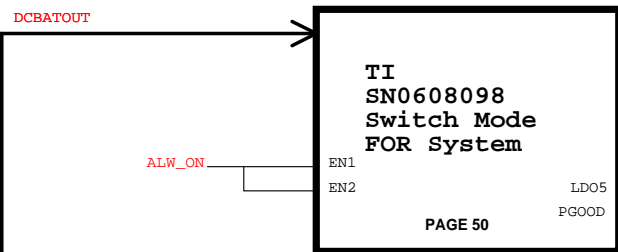
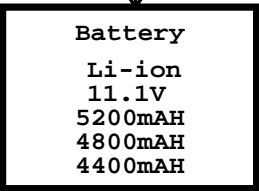
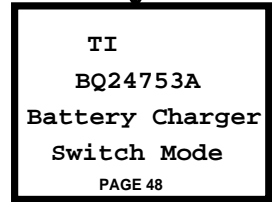
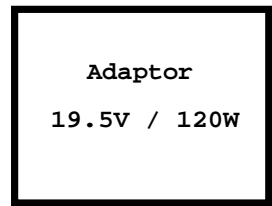
The schematic diagram illustrates the fan control circuit for the TP40B50 module. It features a 5V regulator (F11) powered by +5VRUN, which provides VCCFAN1 to the fan (CN14). A tachometer signal (FAN1_TACH) is connected to the fan's tachometer pin and a pull-up resistor (R383) to +3VRUN. The fan's PWM pin is connected to the FAN1_PWM signal and a pull-down capacitor (C514). The fan's ground pins are connected to the module ground.

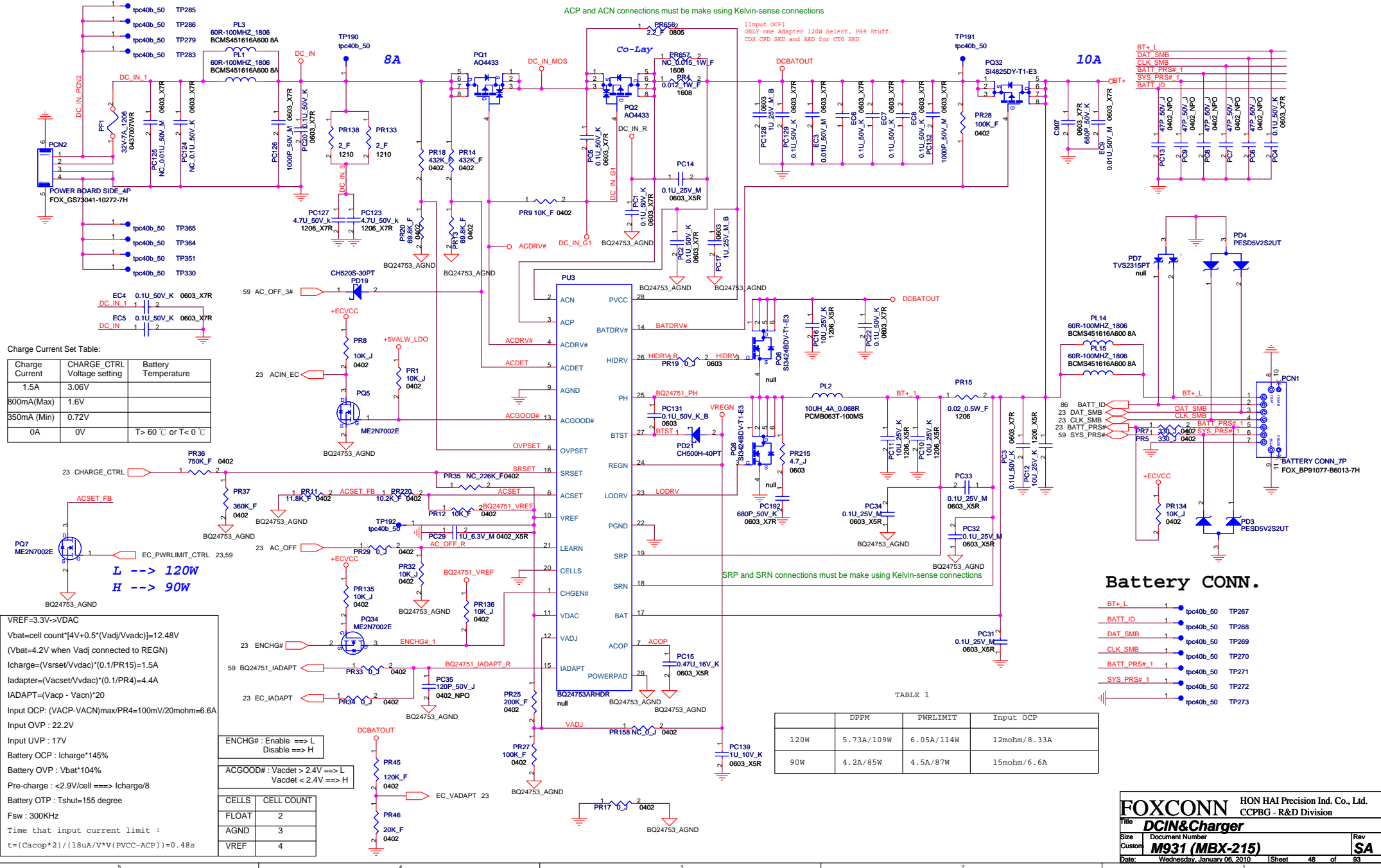
Key components and connections include:

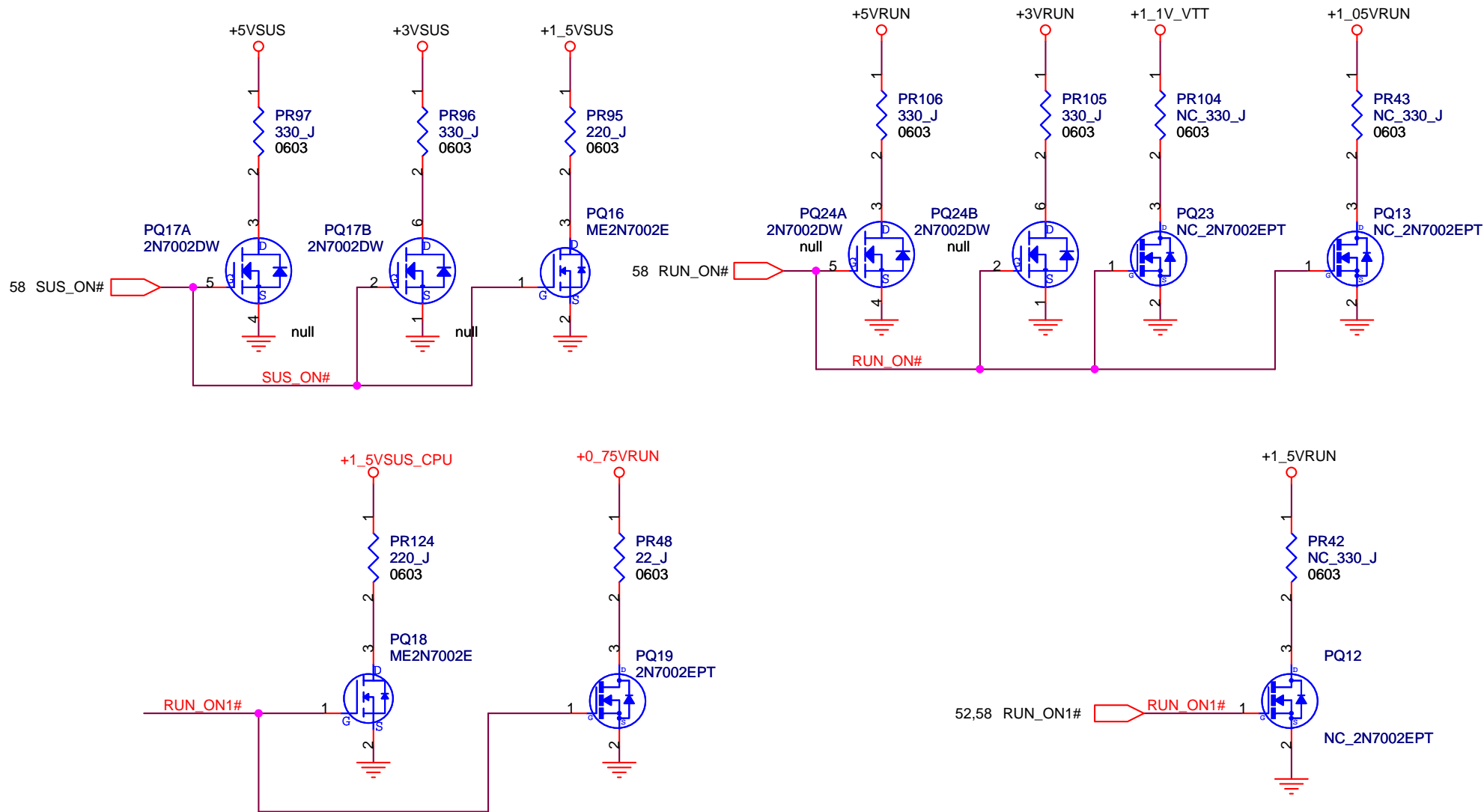
- Power Regulation:** +5VRUN is regulated by F11 (6V-1.5A_1206 1206L150) to provide VCCFAN1.
- Capacitors:** C481 (1u_16V_K 0603_X5R) and C579 (0.1u_16V_Y 0402_Y5V) are used for decoupling. C514 (1000P_50V_K 0402_X7R) is a pull-down capacitor for the PWM signal.
- Resistors:** R404 (NC_4.7K_J 0402) and R383 (4.7K_J 0402) are used for signal conditioning.
- Fan Control:** The fan (CN14, FOX_HS8104E-LH HEADER CONN_4P) is controlled by FAN1_PWM and FAN1_TACH signals.
- Signal Connections:** FAN1_PWM is connected to the fan's PWM pin and a pull-down capacitor. FAN1_TACH is connected to the fan's tachometer pin and a pull-up resistor to +3VRUN.
- Grounding:** The fan's ground pins are connected to the module ground.

Legend for signal connections:

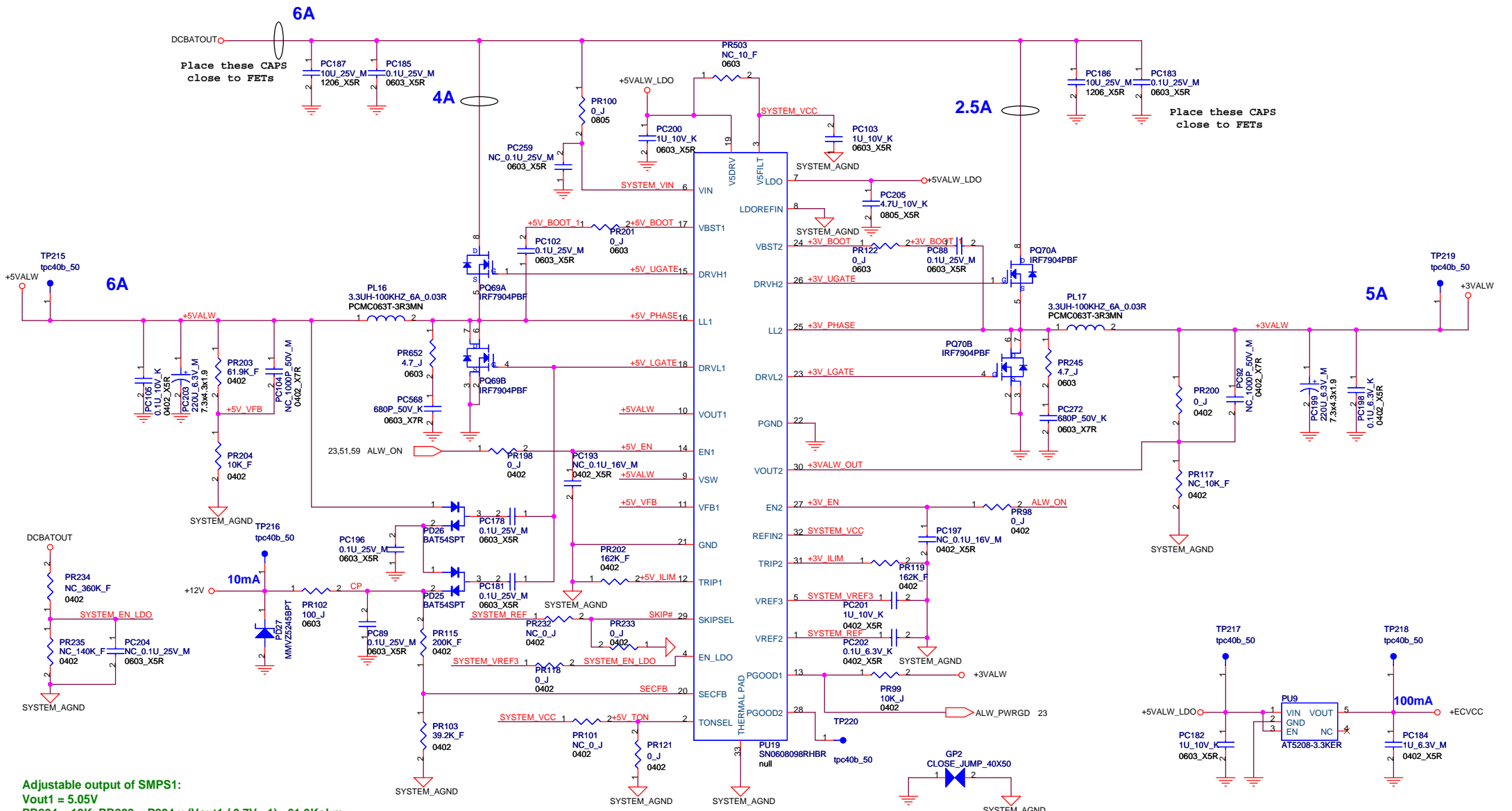
- VCCFAN1: TP24 tpc40b_50
- FAN1_PWM: TP26 tpc40b_50
- FAN1_TACH: TP27 tpc40b_50
- TP28 tpc40b_50







FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <i>DISCHARGE CIRCUIT</i>			
Size A	Document Number <i>M931 (MBX-215)</i>		Rev <i>SA</i>
Date:	Wednesday, January 06, 2010	Sheet 49	of 93



Adjustable output of SMPS1:
 Vout1 = 5.05V
 PR204 = 10K, PR203 = P204 x (Vout1 / 0.7V - 1) = 61.9Kohm

Second Feedback :
 Vout_sec = 12V, PR103 = 20Kohm
 PR115 = PR103 x (Vout_sec / 2V - 1) = 100Kohm

TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

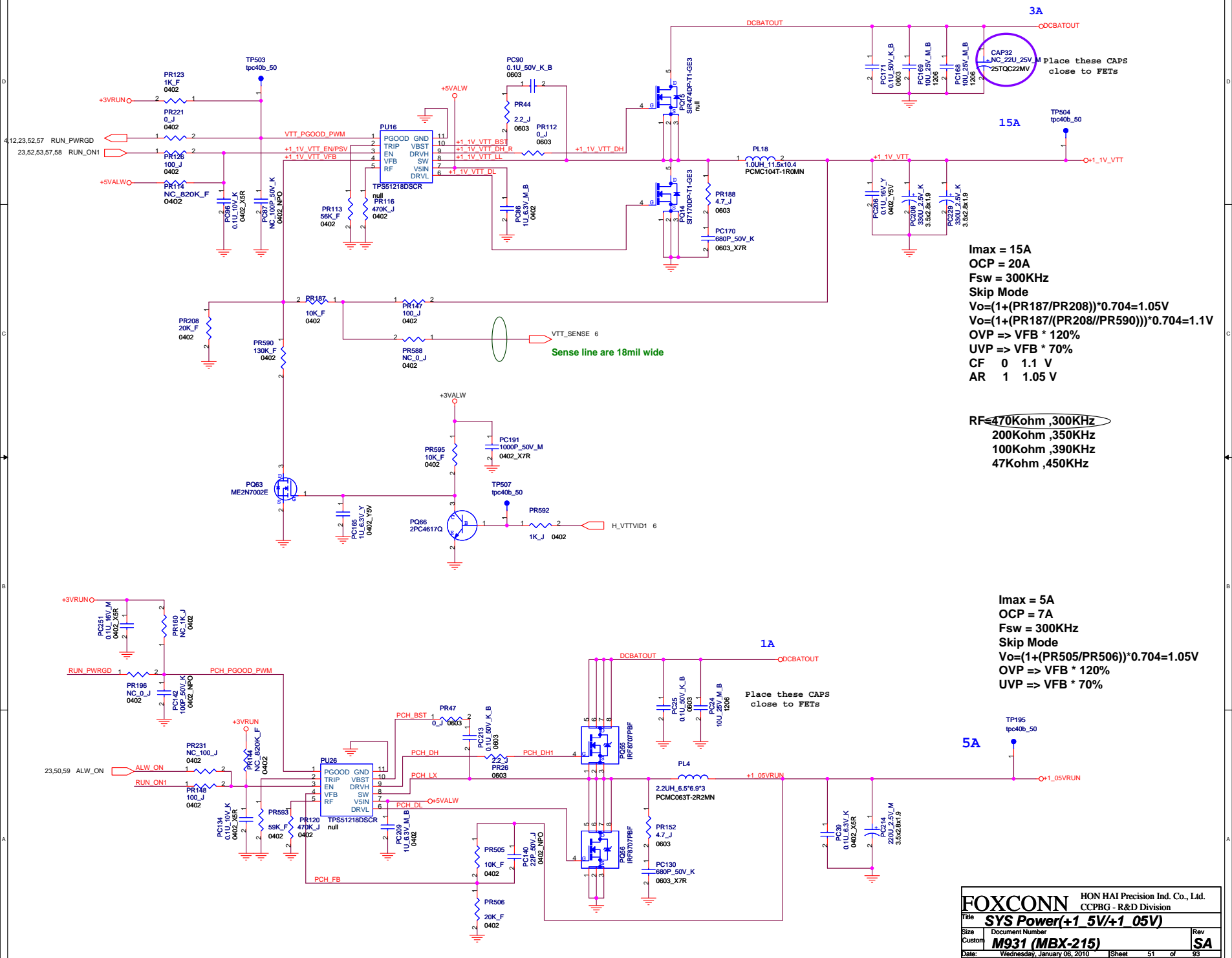
$$L = VOUT (VIN - VOUT) / (VIN * F * LIR * ILOAD (MAX))$$

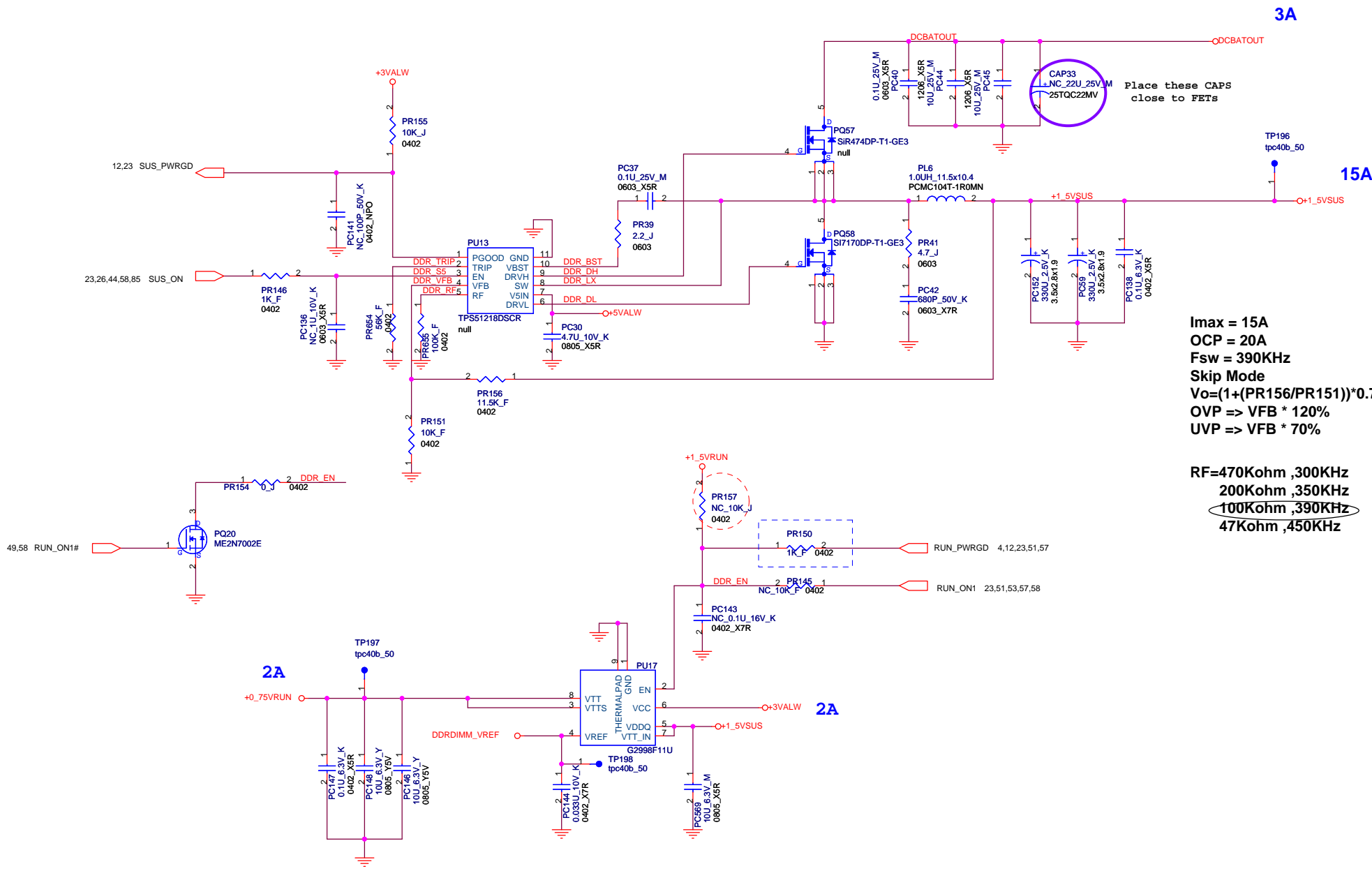
$$Rocp = (Iocp - Irripple / 2) * (10 * Rds (on)) / 5u$$

$$+5VALW = ((PR186 / PR188) + 1) * VFB1$$

Current limit resistor for SMPS1 :
 Ivalley_5 = 5.775A, Rcs_5 = Rds1 = 10.8mohm
 PR202 = (10 x Ivalley_5 x Rcs_5) / 5uA = 162K

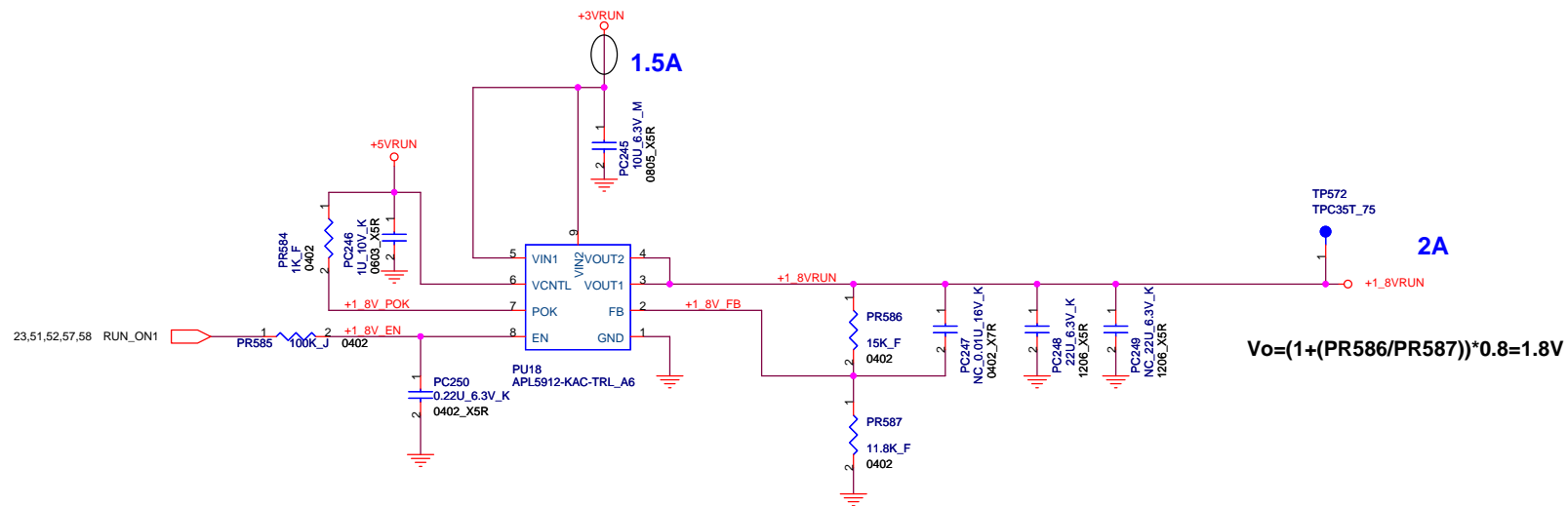
Current limit resistor for SMPS2 :
 Ivalley_3 = 5.525A, Rcs_3 = Rds2 = 10.8mohm
 PR119 = (10 x Ivalley_3 x Rcs_3) / 5uA = 162K

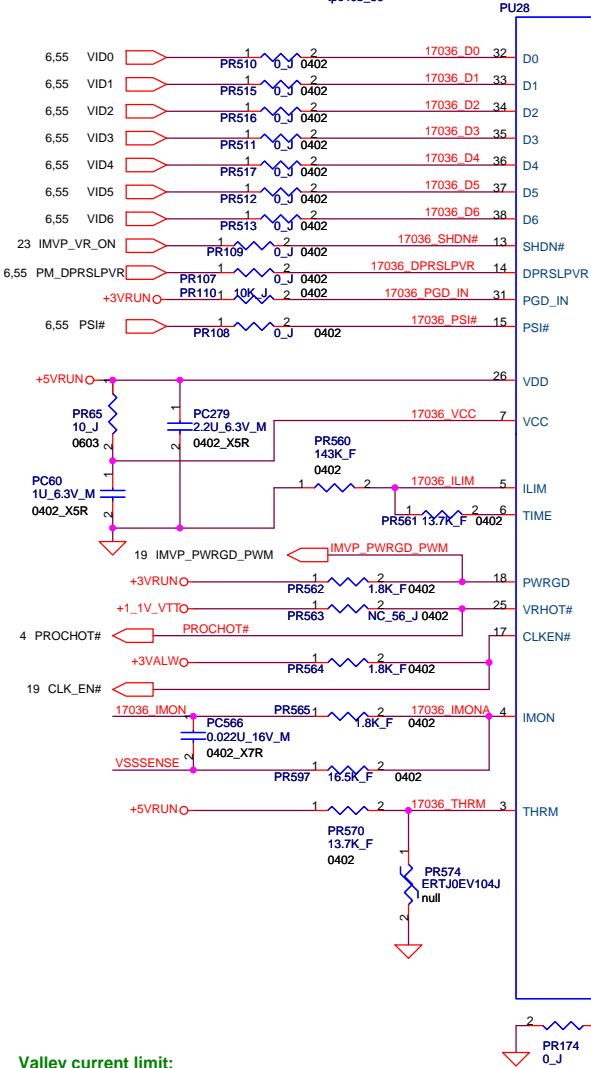
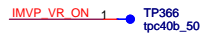
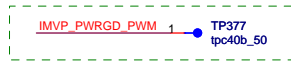




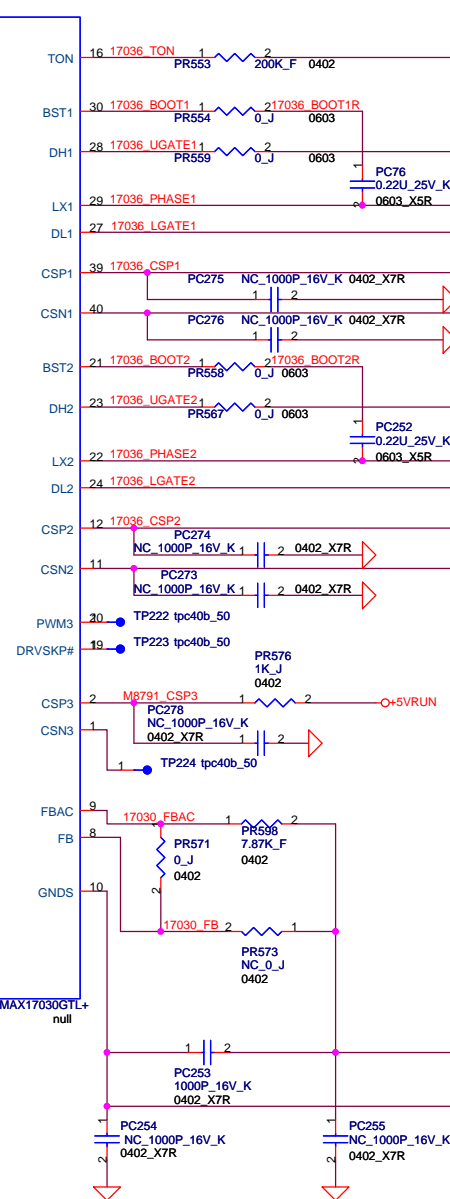
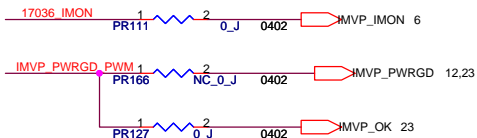
Imax = 15A
OCP = 20A
Fsw = 390KHz
Skip Mode
 $V_o = (1 + (PR156/PR151)) * 0.704 = 1.514V$
OVP => VFB * 120%
UVP => VFB * 70%

RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz



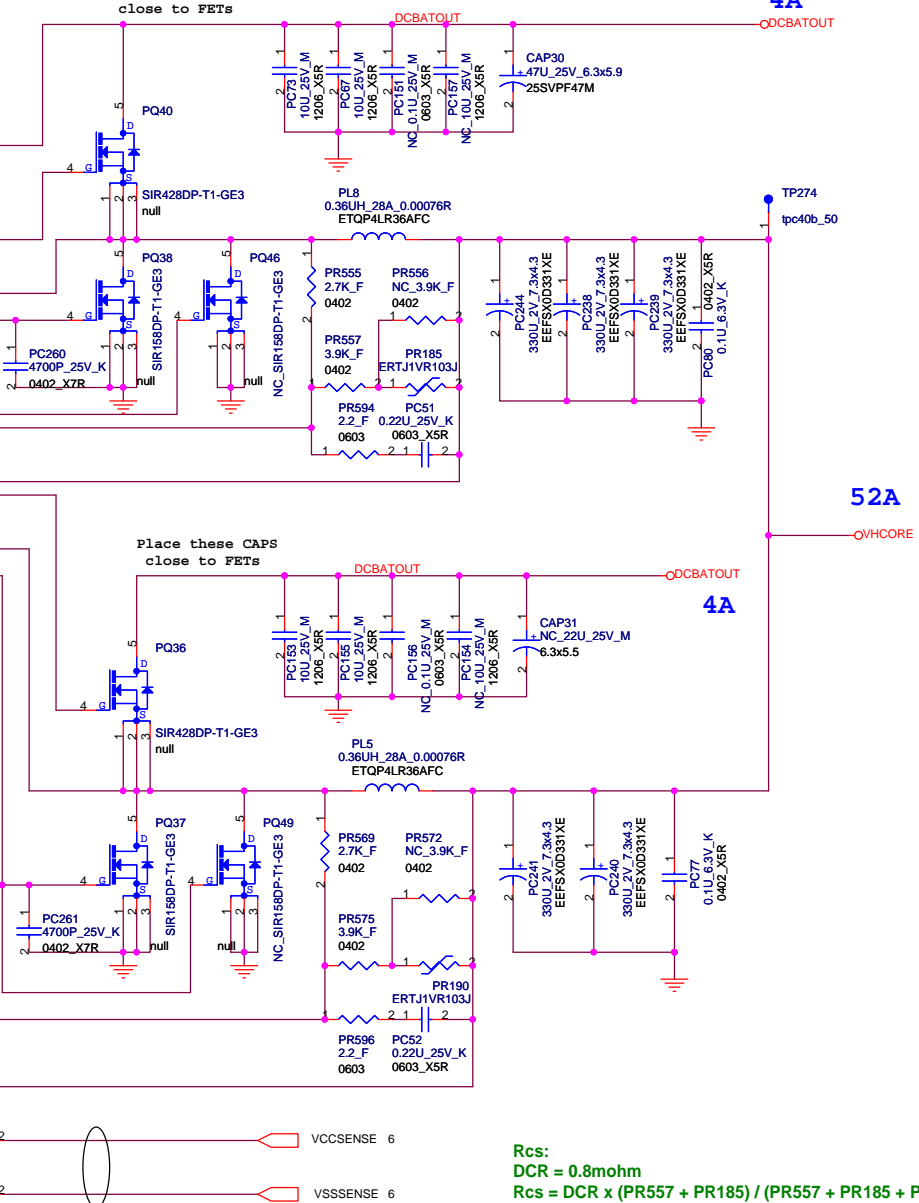


Valley current limit:
 $V_TIME_LIM = 0.2 \times PR561 / (PR560 + PR561) = 20.2mV$
 $I_LIM = V_TIME_LIM / R_{cs} = 19A$



Sense line are 18mil wide

Place these CAPS close to FETs

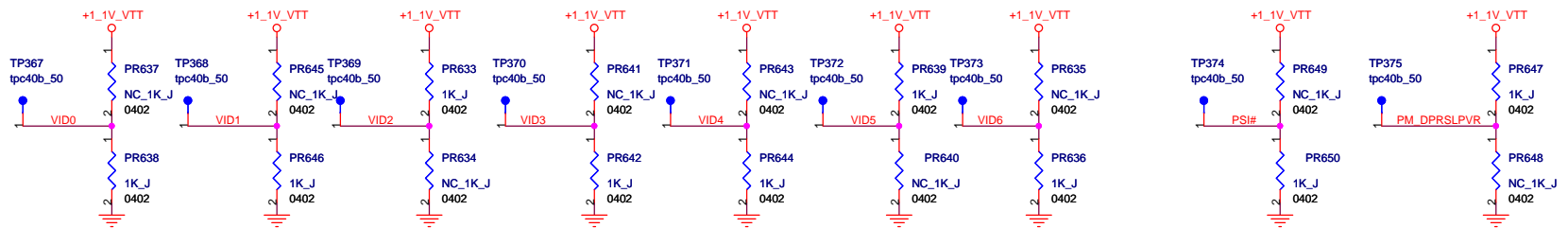
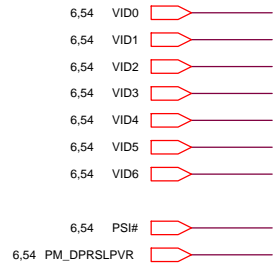


Rcs:
 $DCR = 0.8mohm$
 $R_{cs} = DCR \times (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.709mohm$
 Load-Line R_{FBAC} : Load-Line=-1.9mV/A
 $R_{cs} = 0.709mohm$
 $PR598 = (1.9mV/A) / (R_{cs} \times 400us) = 6.34K$

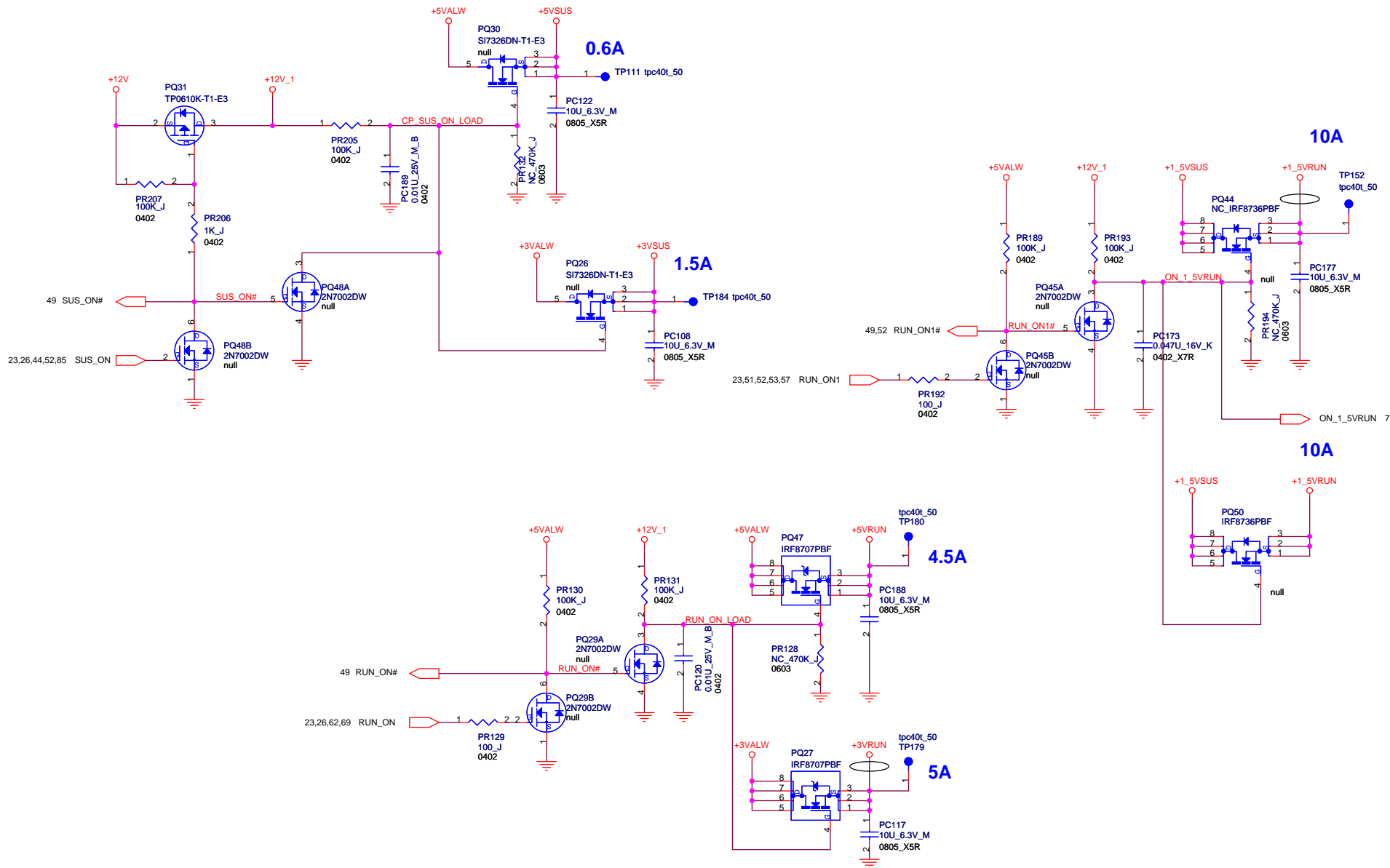
Default value of VID [6:0] = [0100100] , PSI# = 0 , PROC_DPRSPLVR = 1

Market Segment Selection MSID[2:0] = [100] (SV)

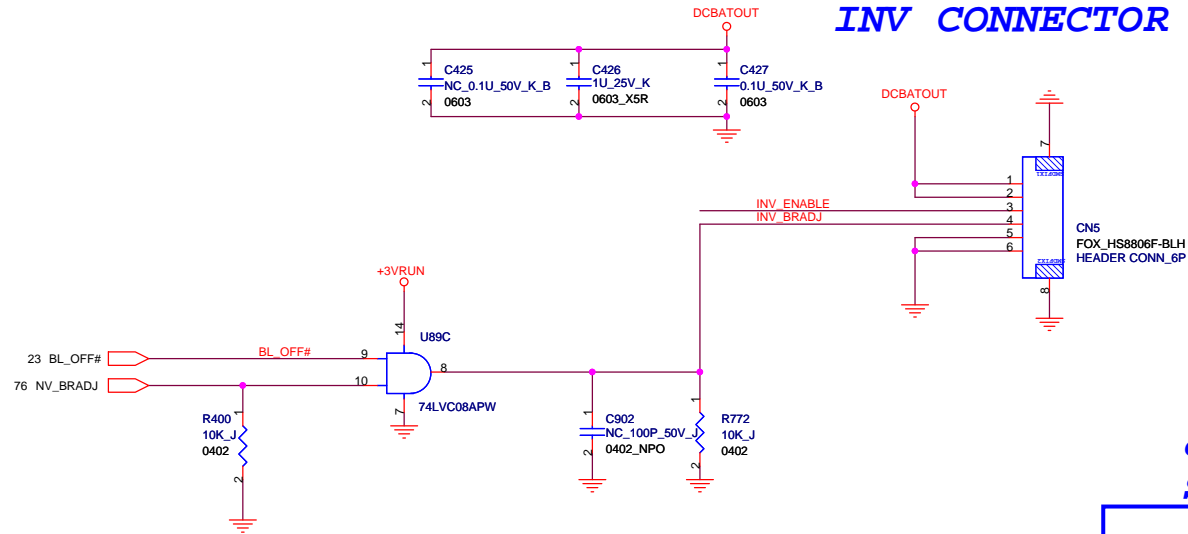
- 416056_416056_Ard_EDS_Rev.1.1
- 403779_Clarksfield_MPG_Rev1.5



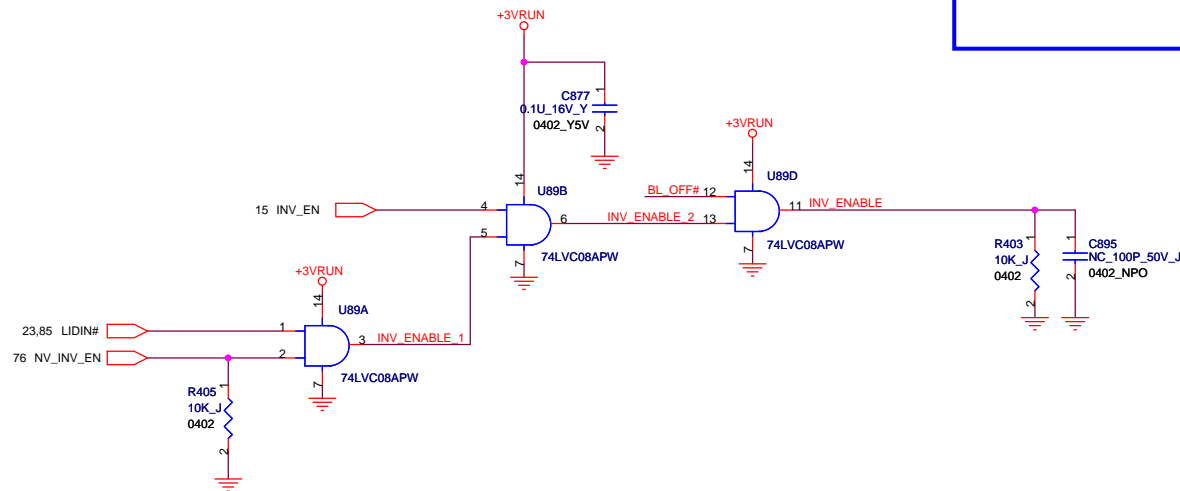
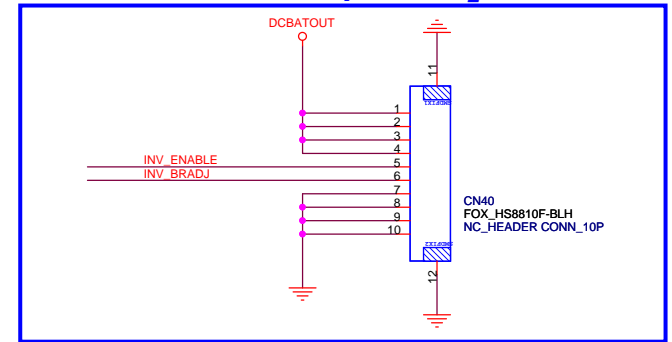
Delete iGPU Path on DVT for Cost Down



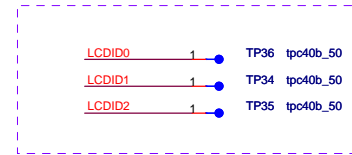
INV CONNECTOR



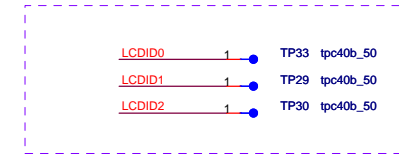
eDP (Suzaku3 support) >>
Stuff CN40 , Dummy CN5



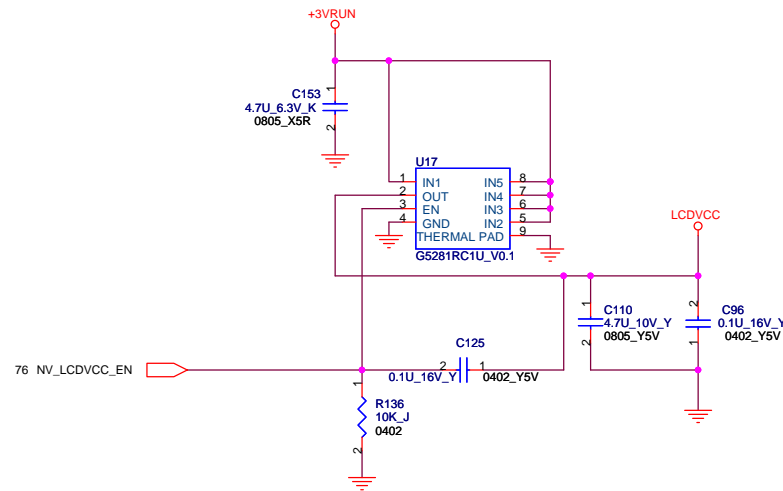
Bot-Side



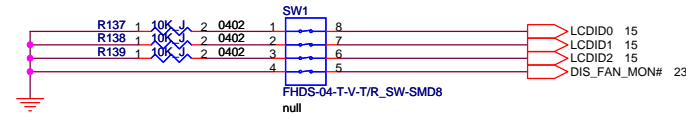
Top-Side



LCDVCC Power

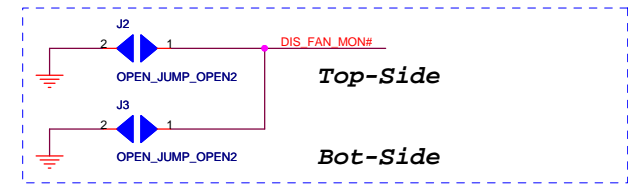


PANEL ID

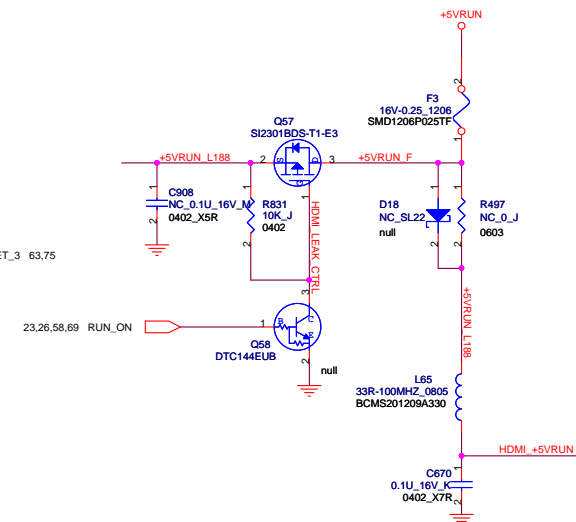
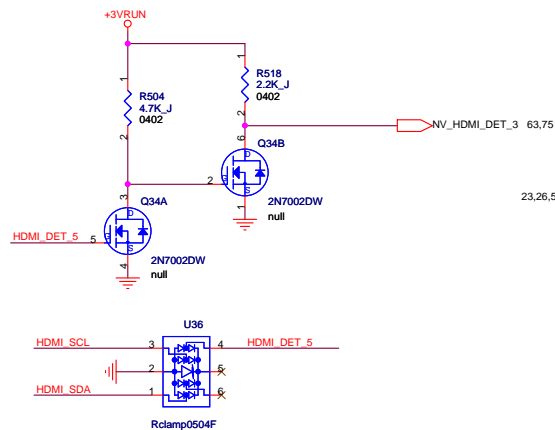
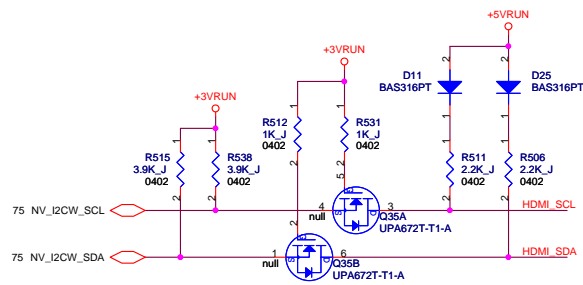


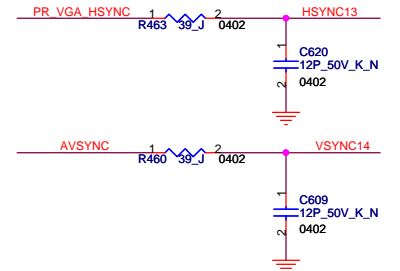
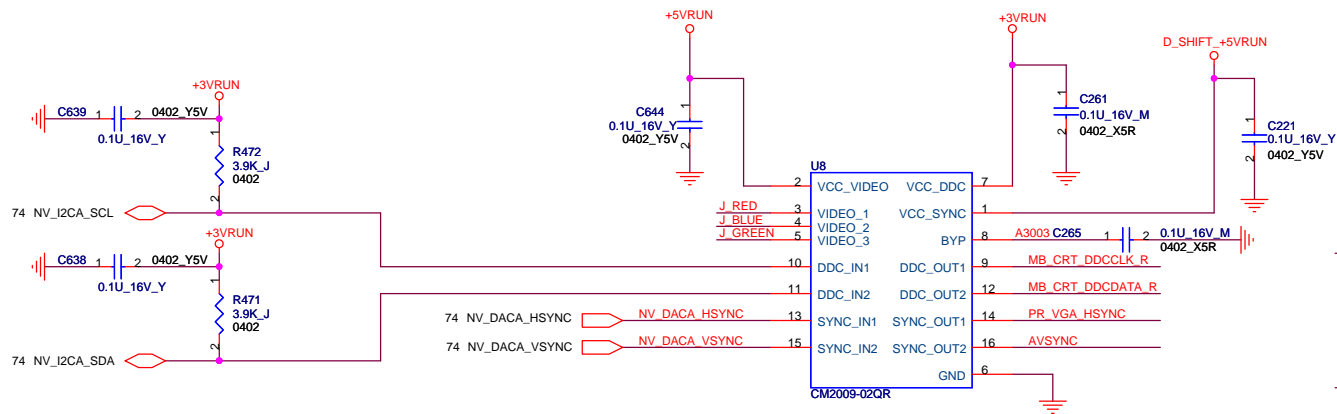
SW1 (Panel ID)	LCDID2	LCDID1	LCDID0	FAN Lock
CRT (No LCD)	0	0	0	ON: Disable OFF: Enable
EW1 (Sharp)	0	0	1	
RESERVED	0	1	0	
EW1 (LGD)	0	1	1	
EW3 (Sharp)	1	0	0	
EWX (Sharp)	1	0	1	
RESERVED	1	1	0	
RESERVED	1	1	1	

ON:0 , OFF:1

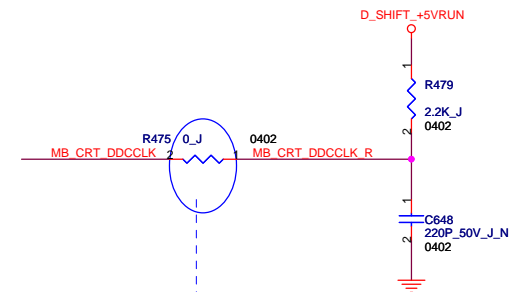
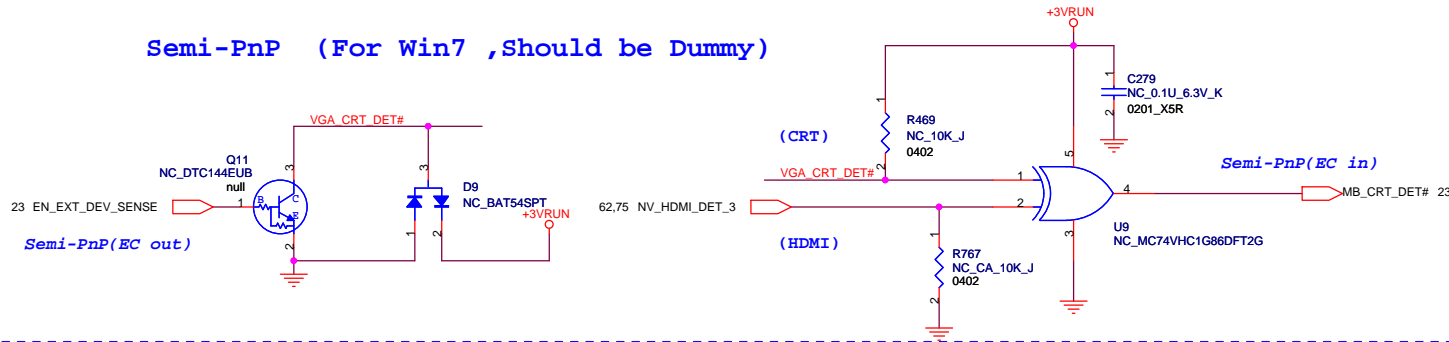


DIS_FAN_MON# for L6 BFT Test

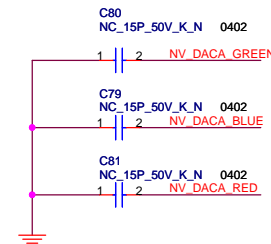
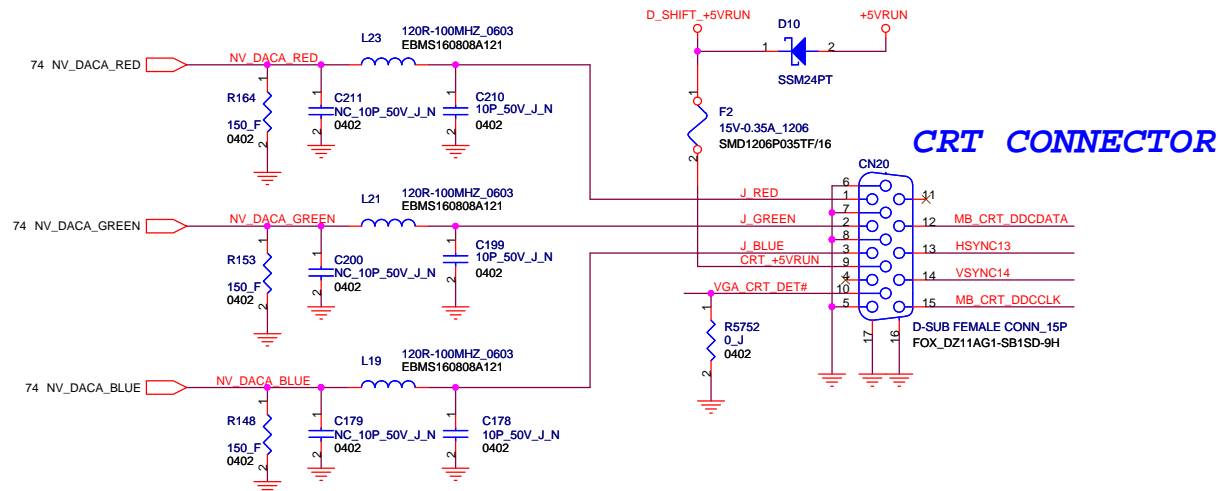
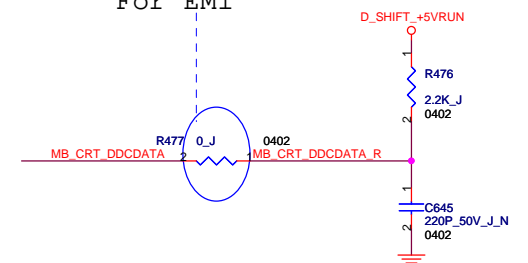




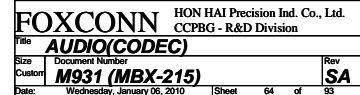
Semi-PnP (For Win7 ,Should be Dummy)

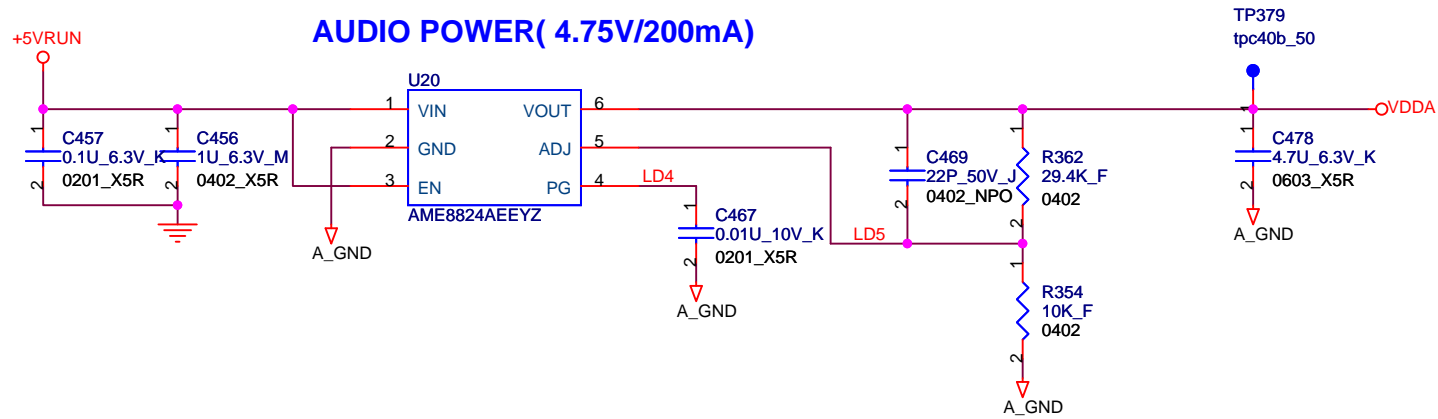


For EMI



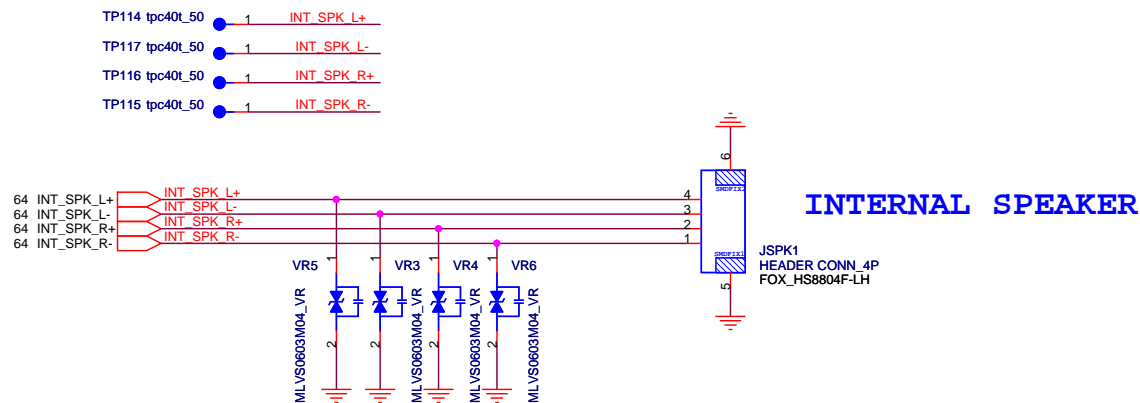
BOM Option for ALC275 and ALC269
(Default is ALC275.)



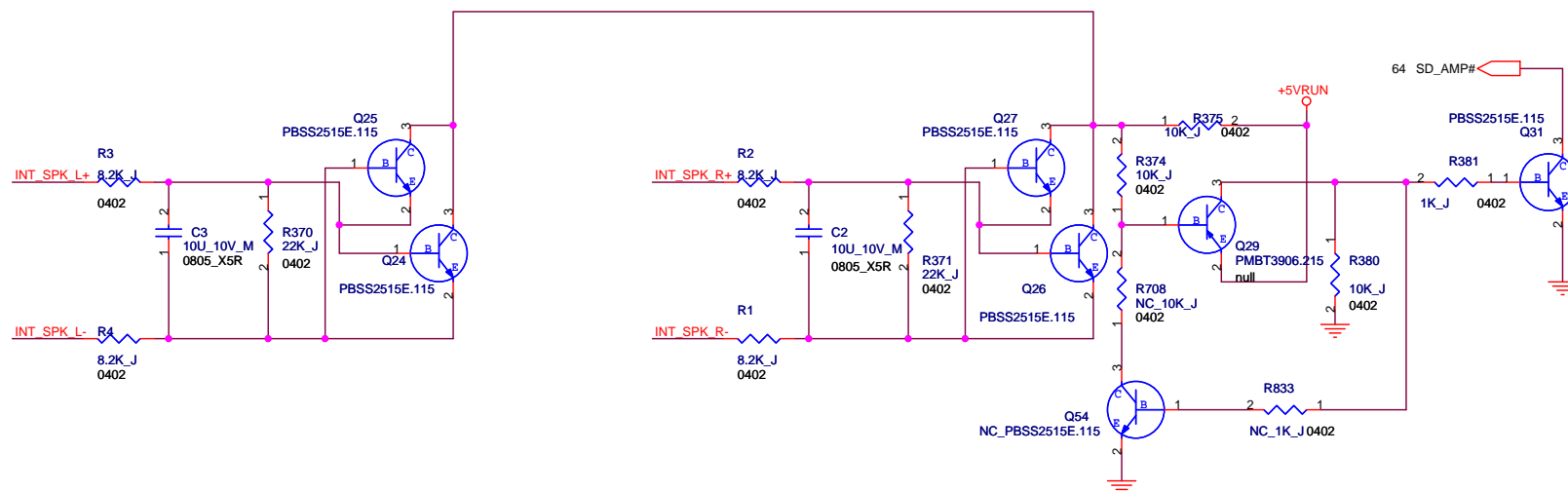


FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title		AUDIO POWER	
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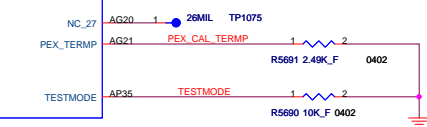
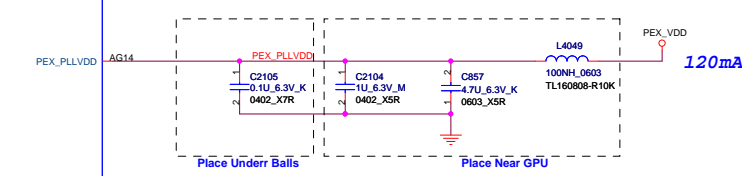
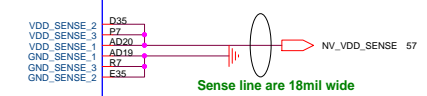
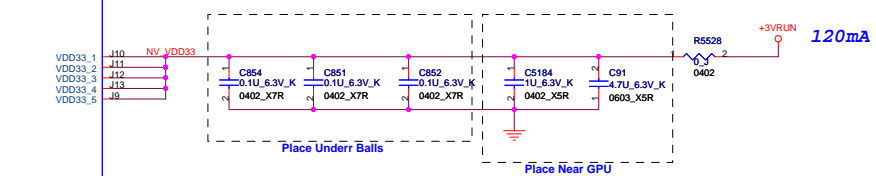
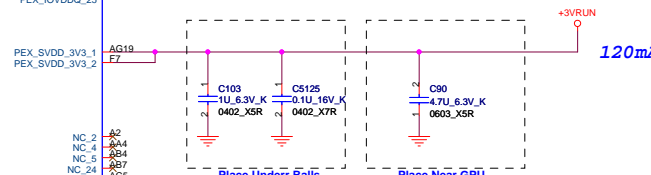
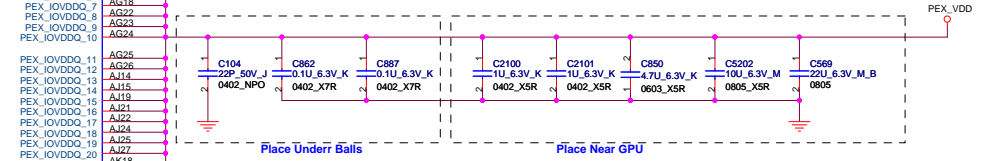
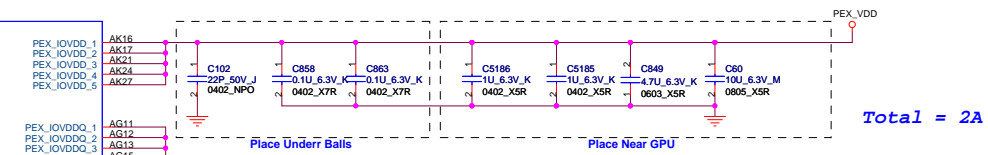
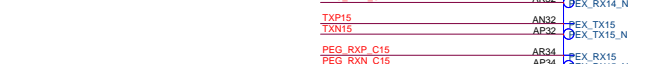
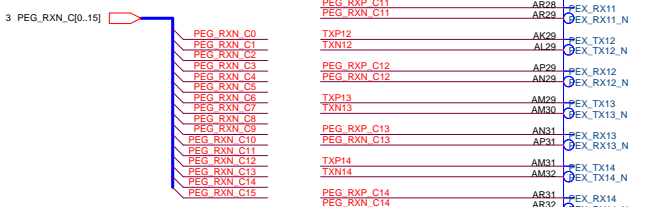
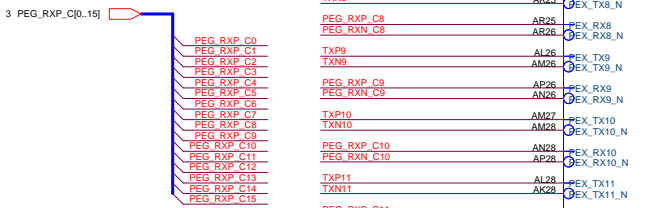
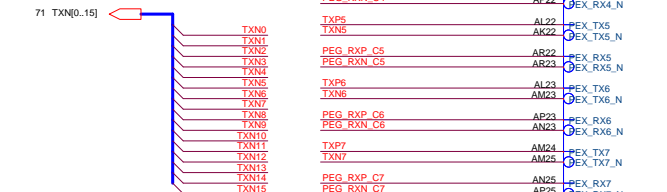
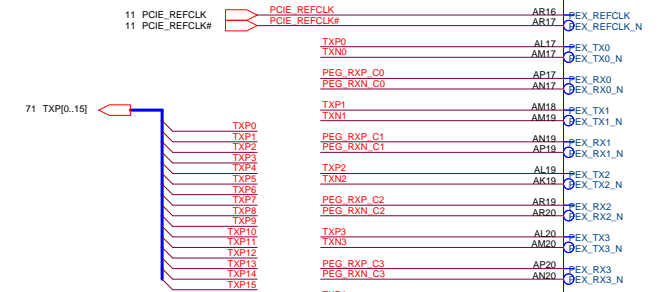
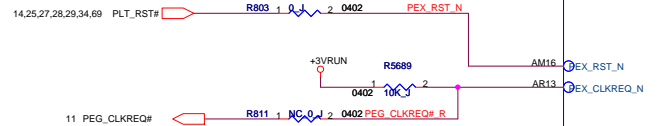
Delete Class D Amp. when implemented ALC275.



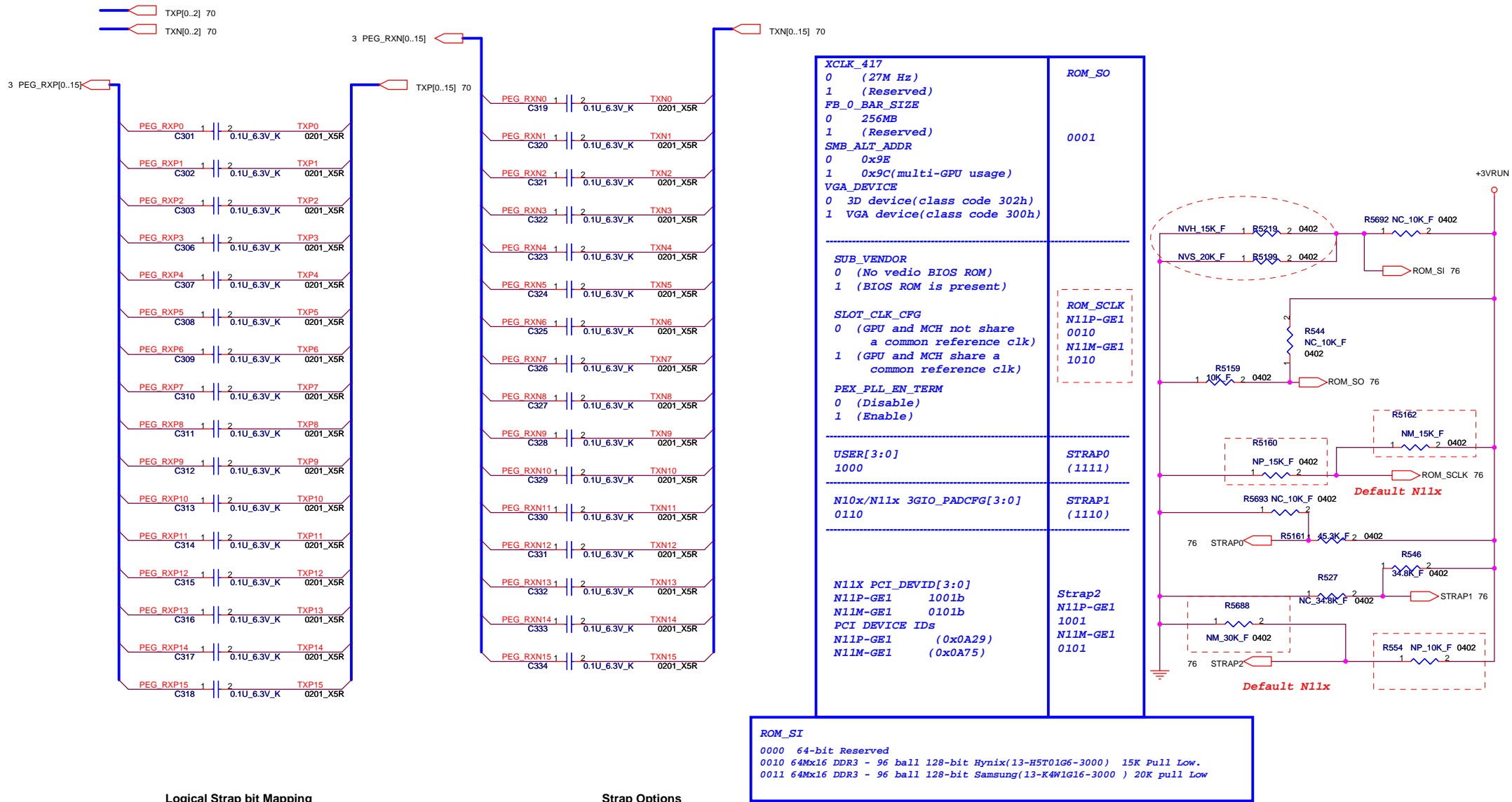
For Shut-down Codec Amp. power (PVDD1 and PVDD2)

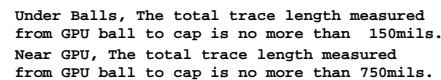


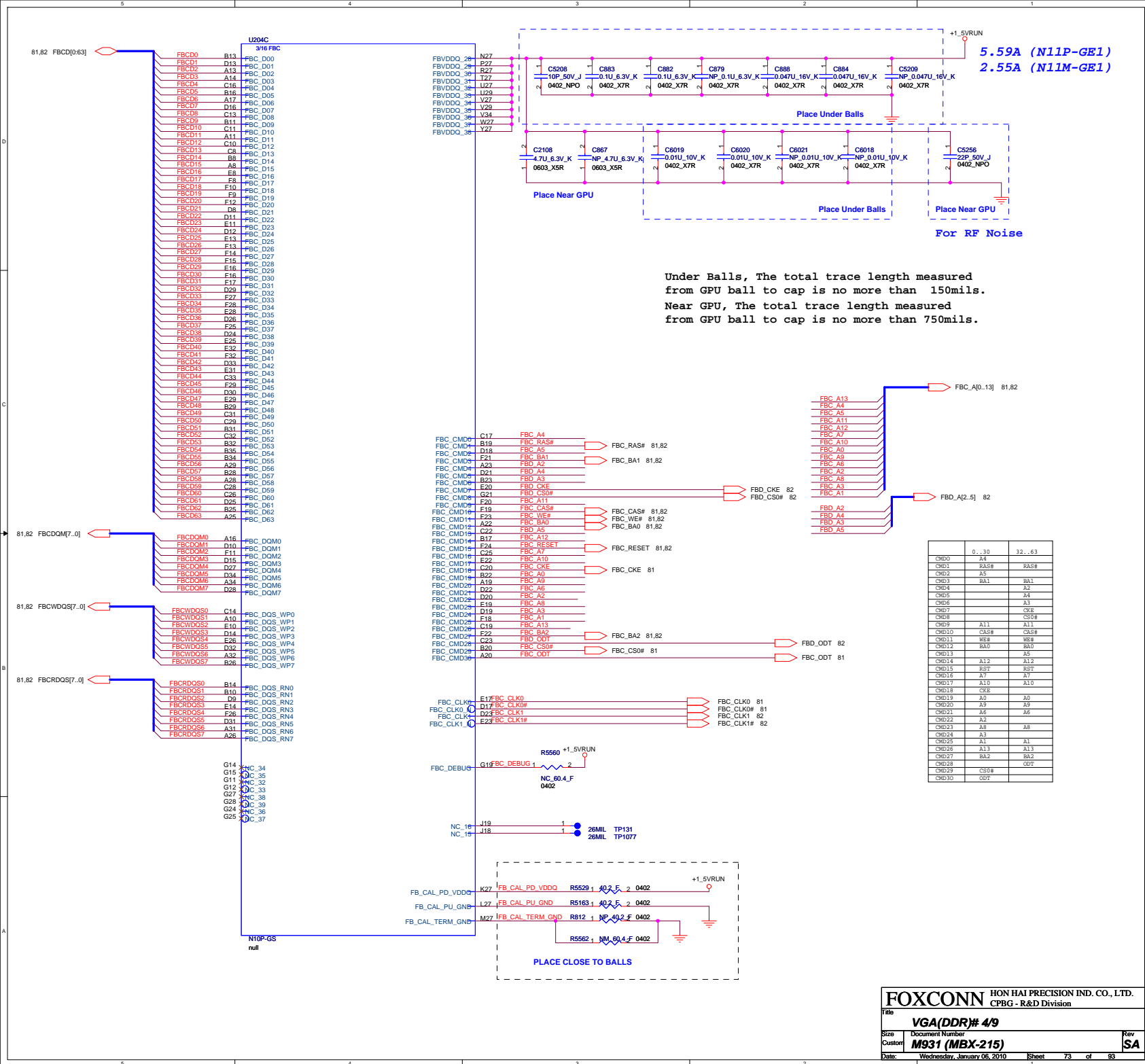
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Size		Document Number	
B		M931 (MBX-215)	
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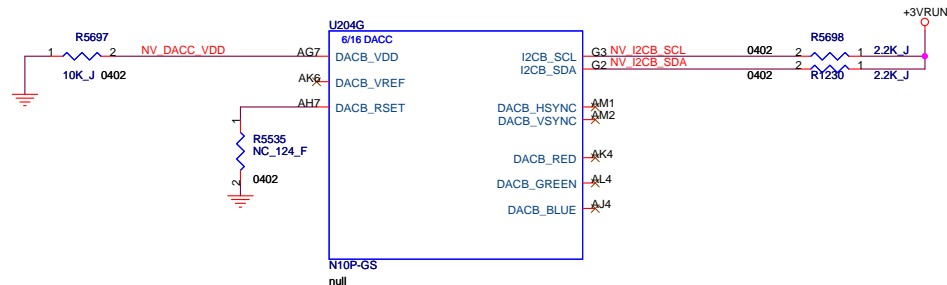
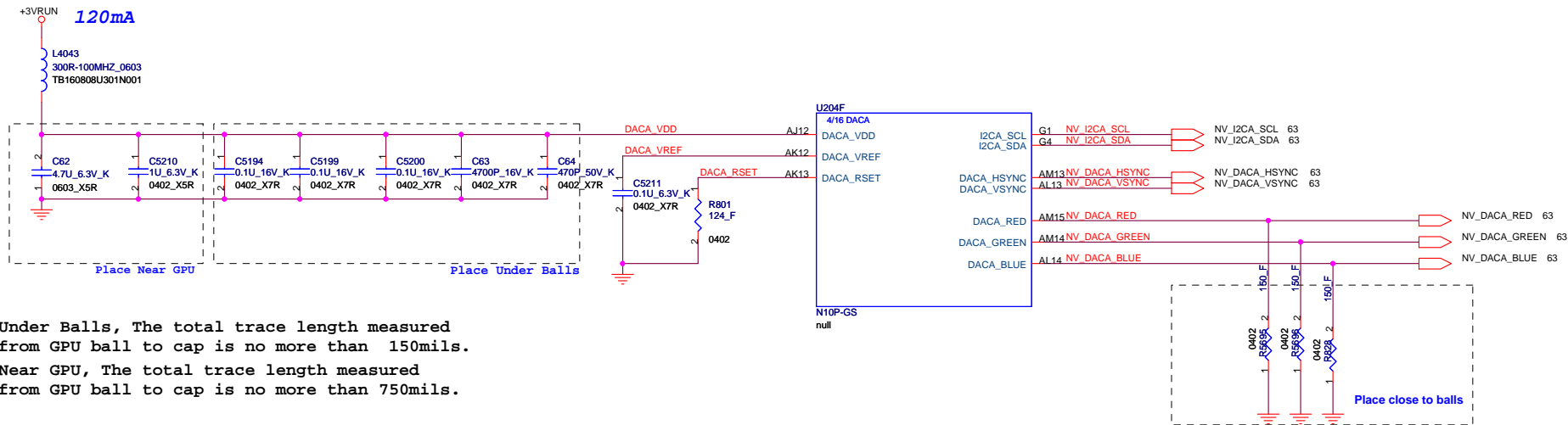


Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

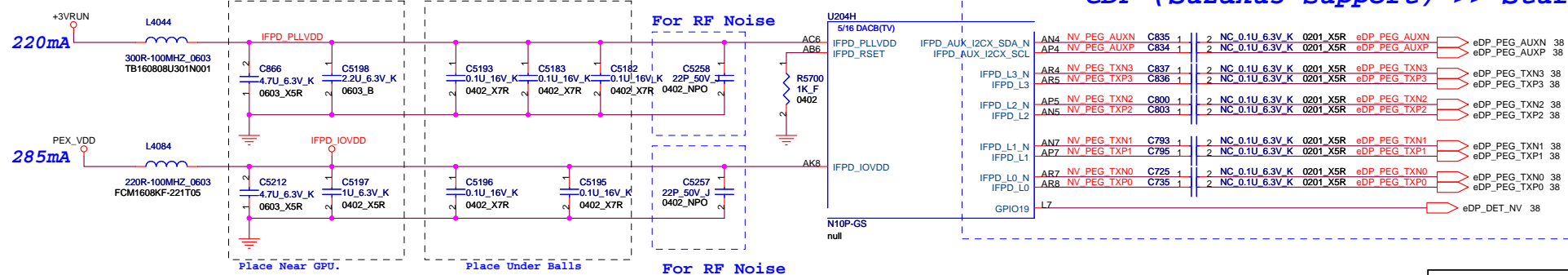


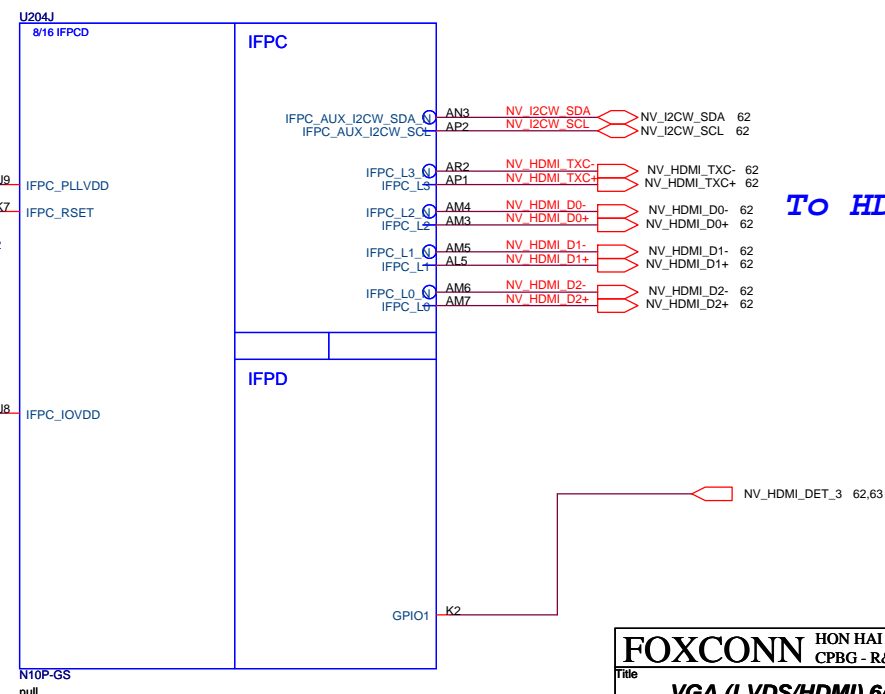
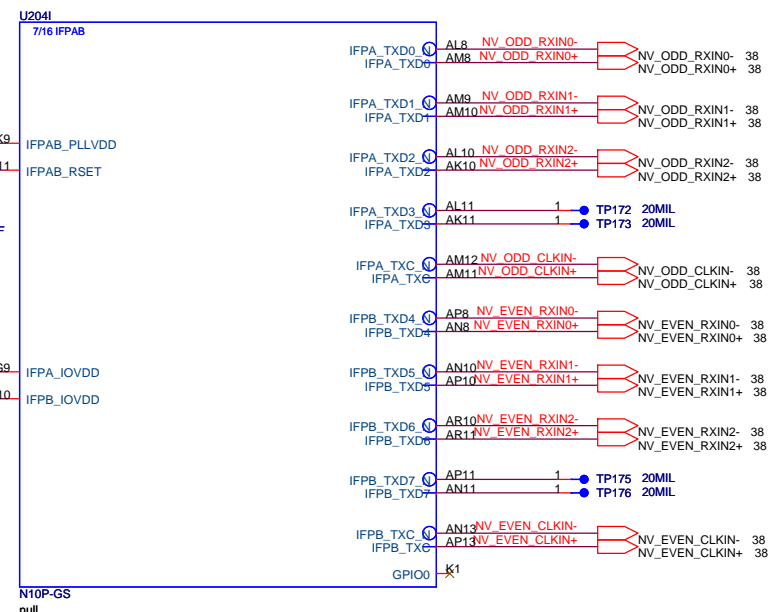




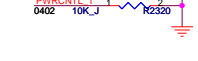
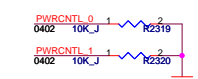
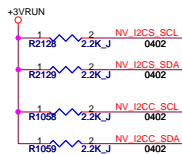
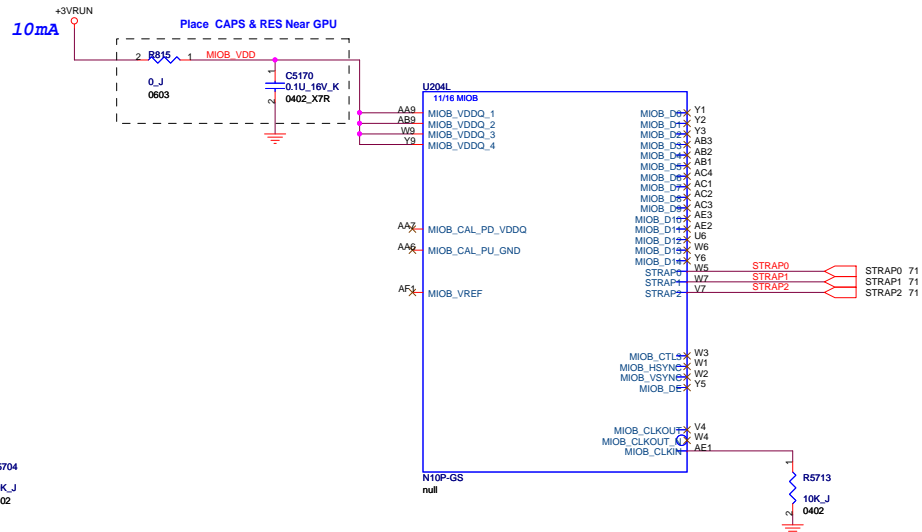
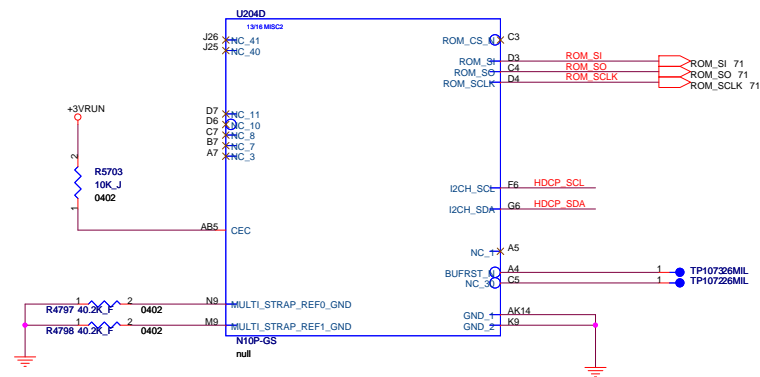


DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDA	SDA



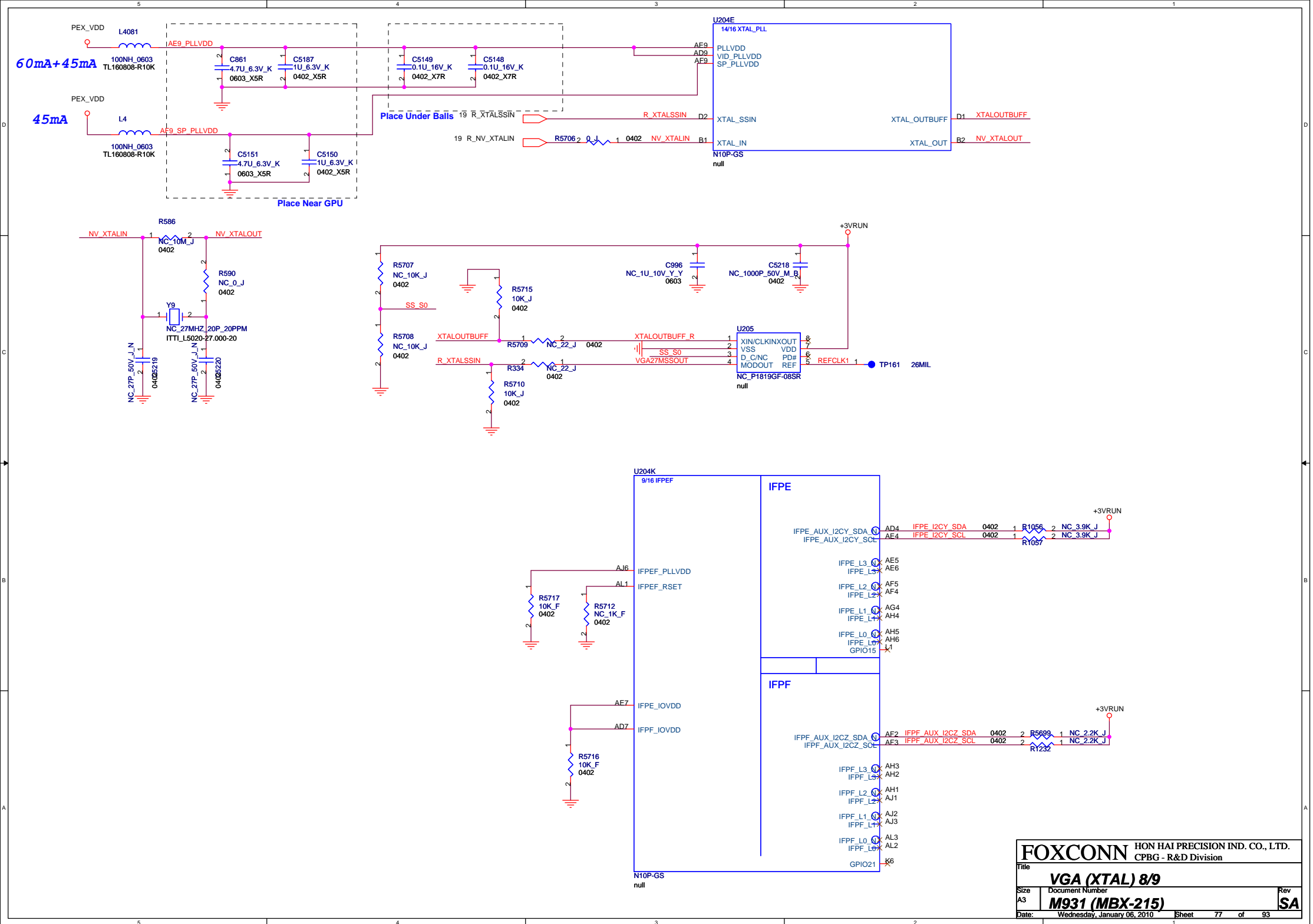


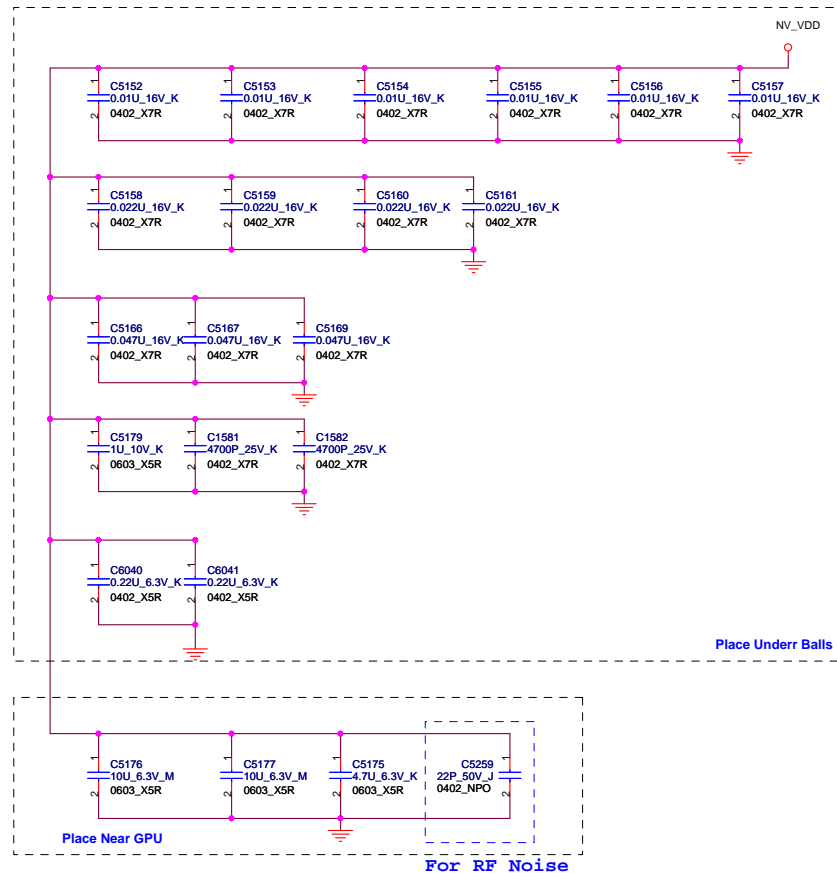
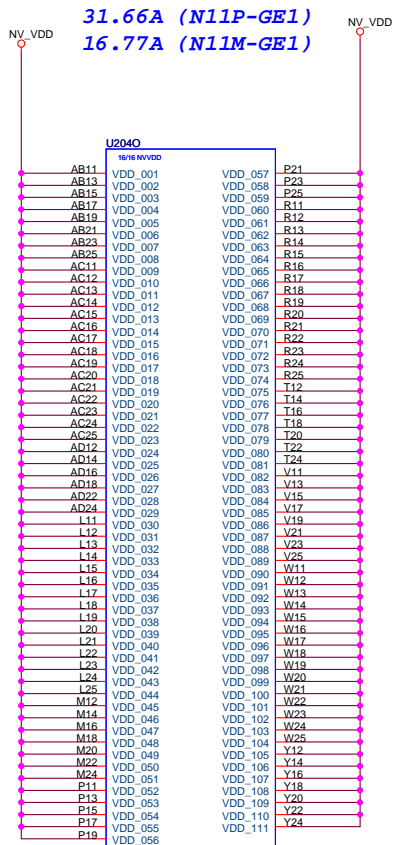
Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.



GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	Yes		
GPIO1	I	Yes	HDMI Hot Plug Detect 0 (HPD0)	Active High
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	Active High
GPIO3	O	No	Panel Power(LCD0_VDD)	Active High
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	Active High
GPIO5	O	No	FOR Power Control NVDD	Active High or Low
GPIO6	O	Yes	FOR Power Control NVDD	Active High or Low
GPIO8	O	No	reserve for reset EC	
GPIO9	I	No	System Power Limit Alert Input	Active Low

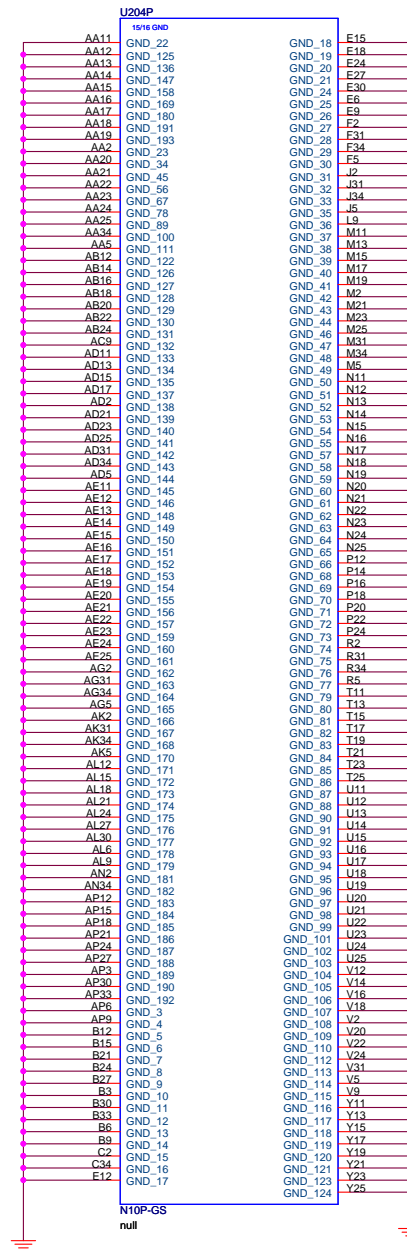
SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CS_SCL I2CS_SDA	I/O	For VGA thermal I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor

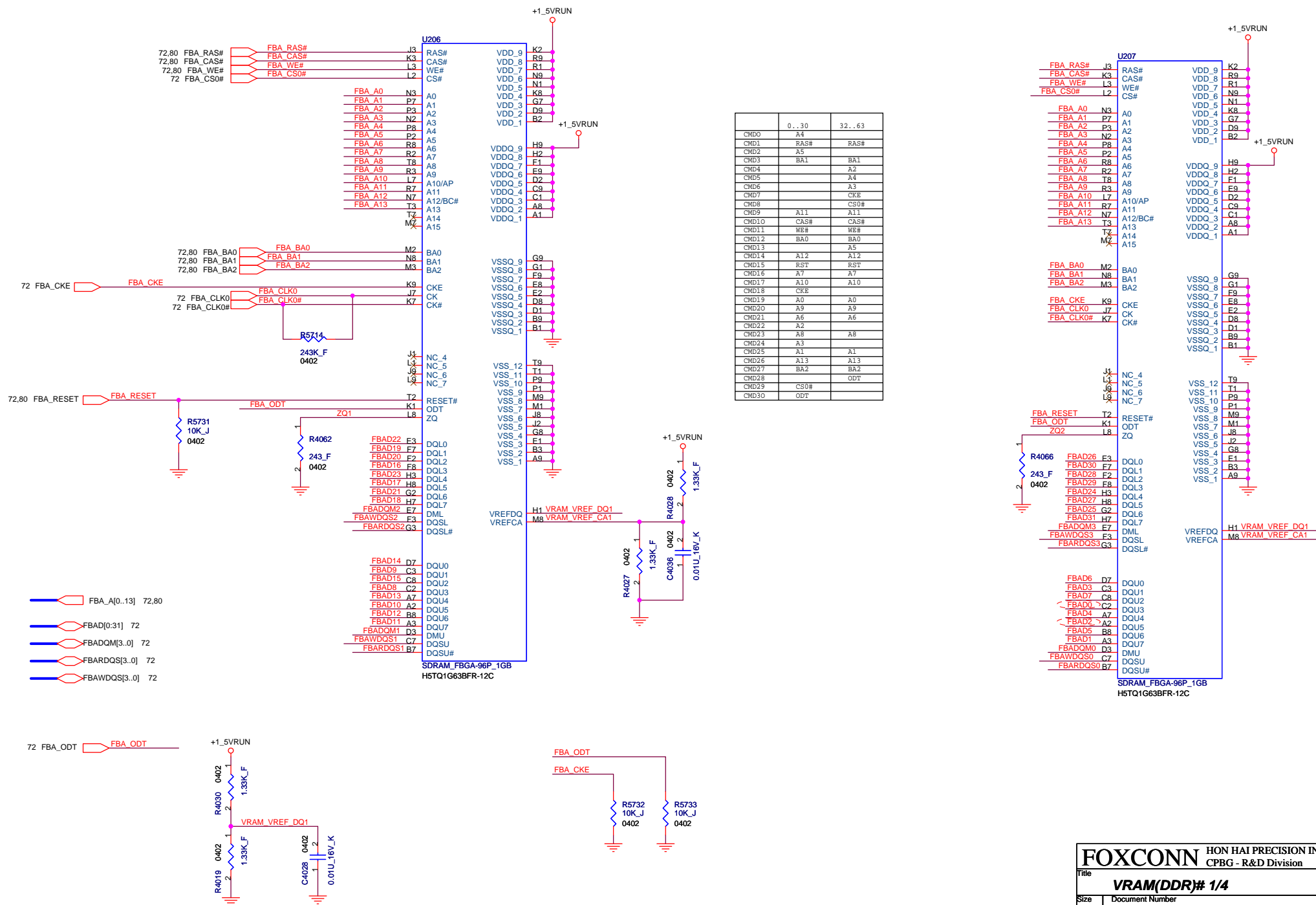


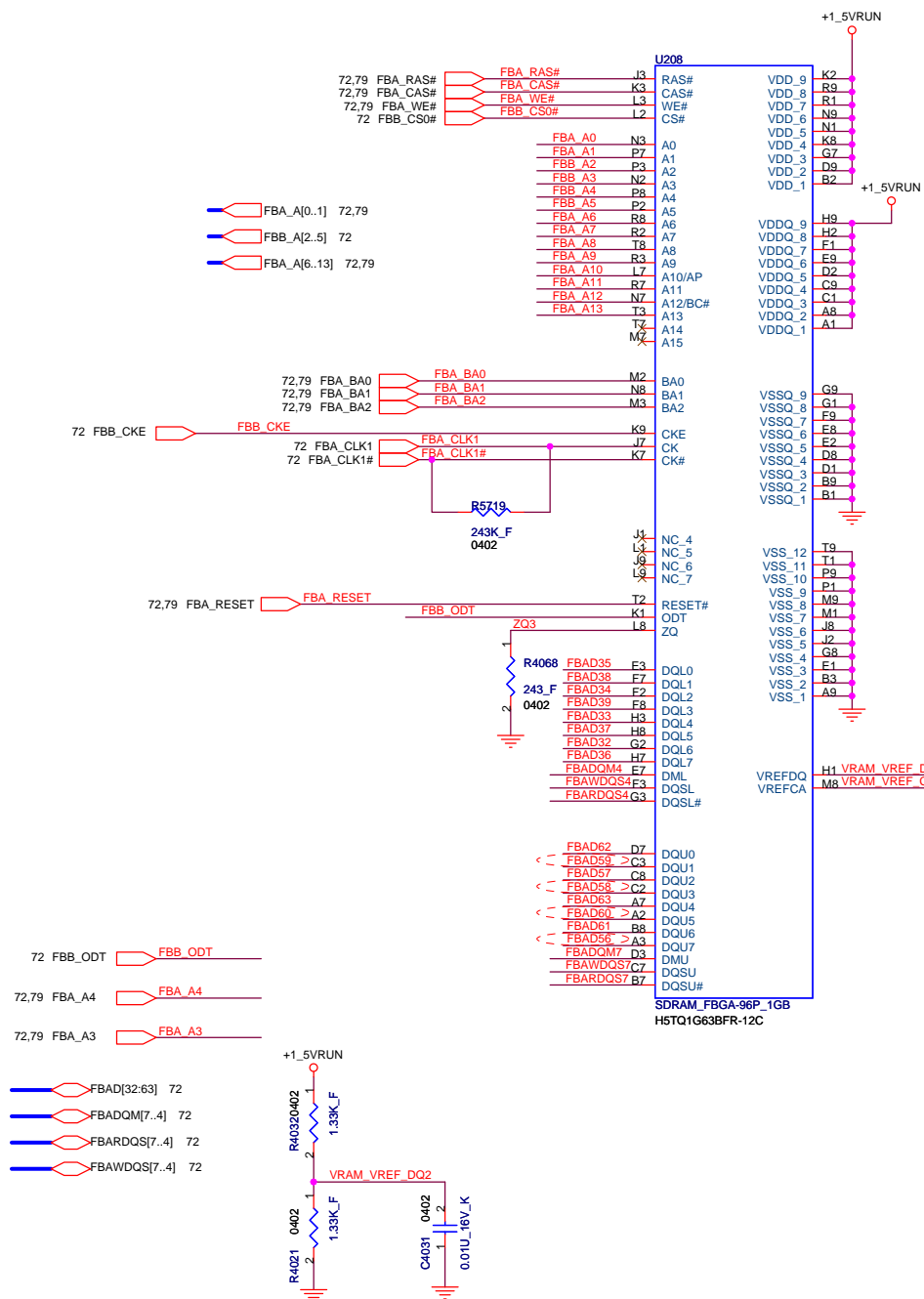


Under Balls, The total trace length measured from GPU ball to cap is no more than 150mils.

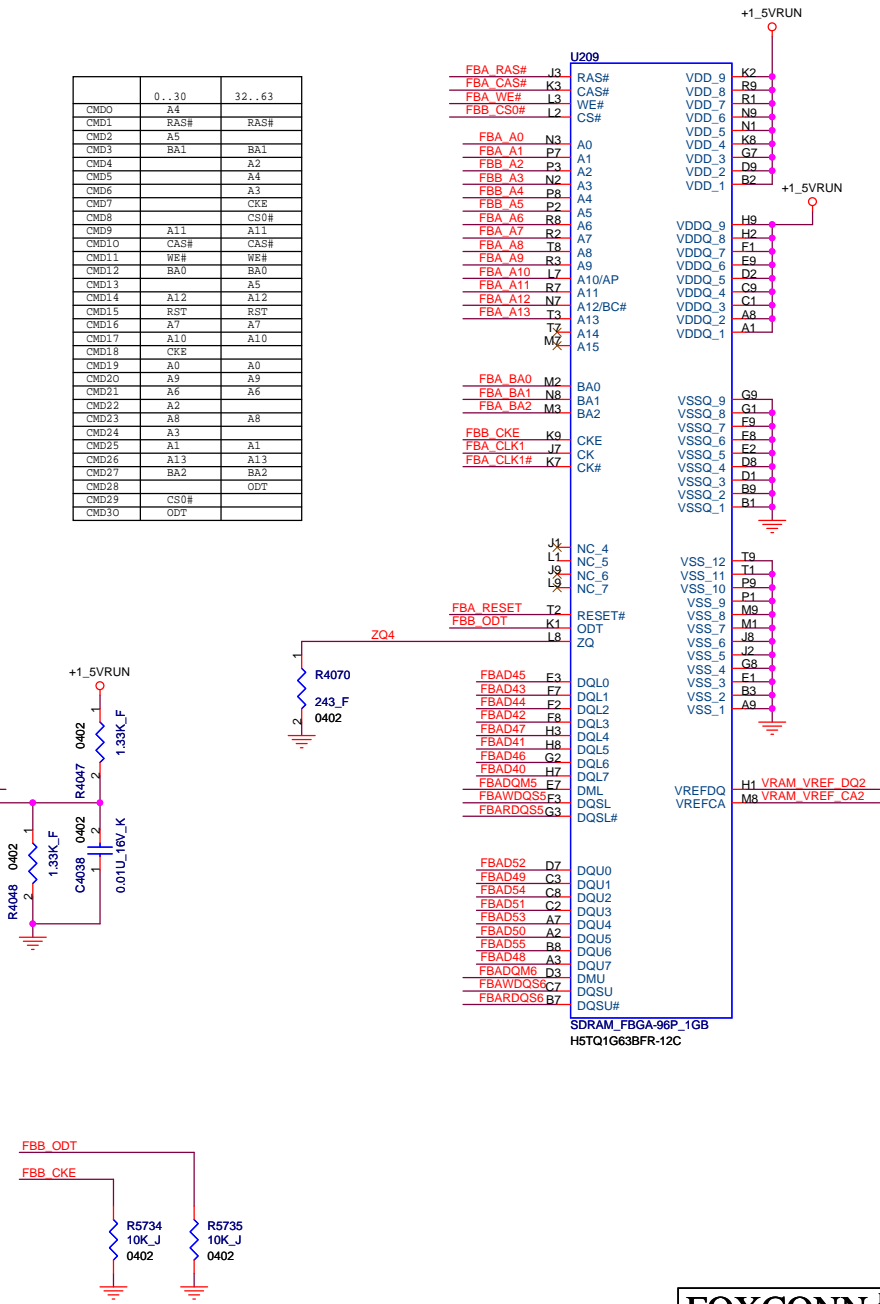
Near GPU, The total trace length measured from GPU ball to cap is no more than 750mils.

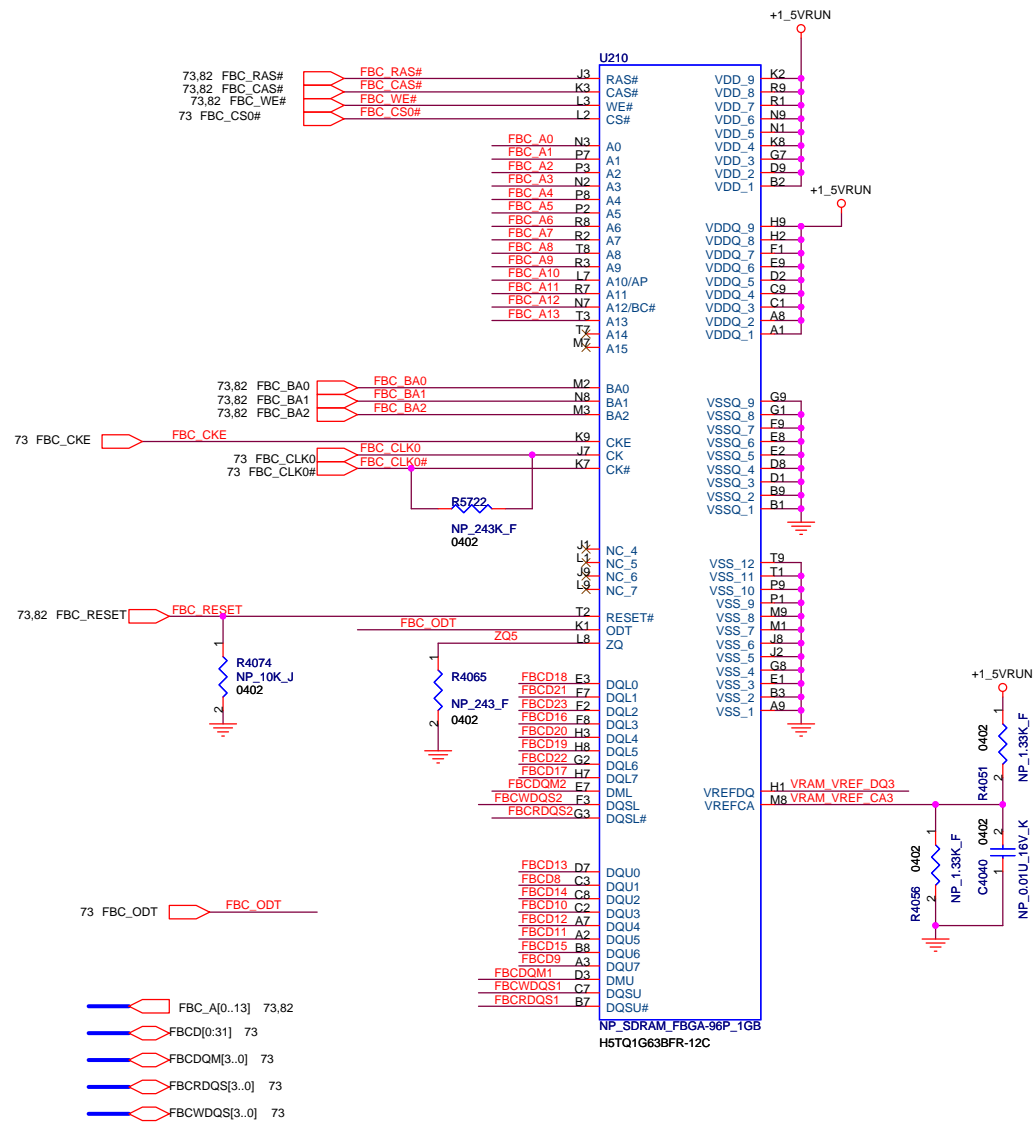




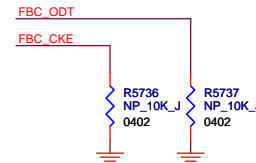
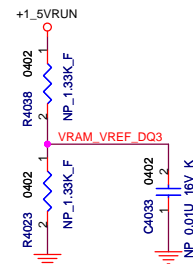
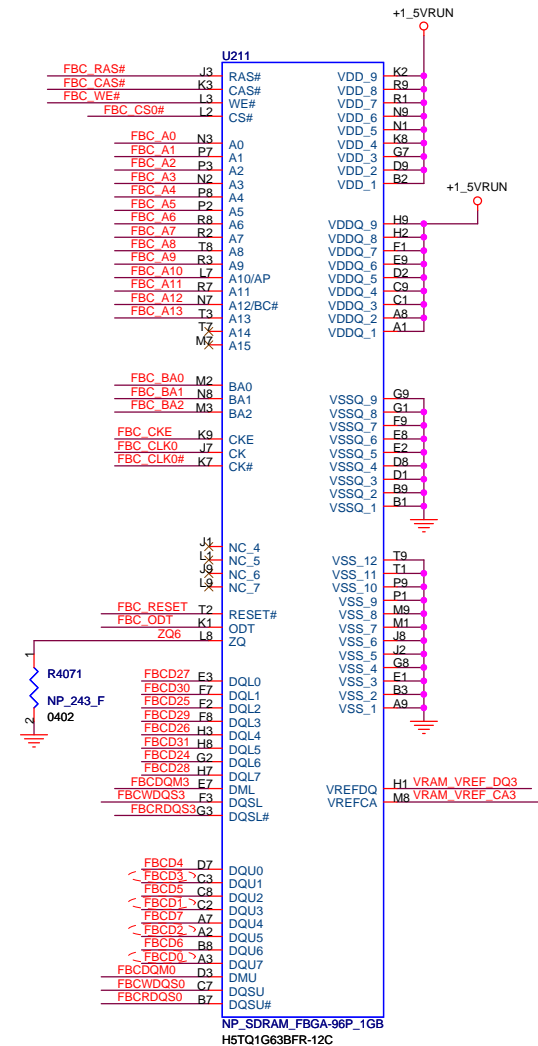


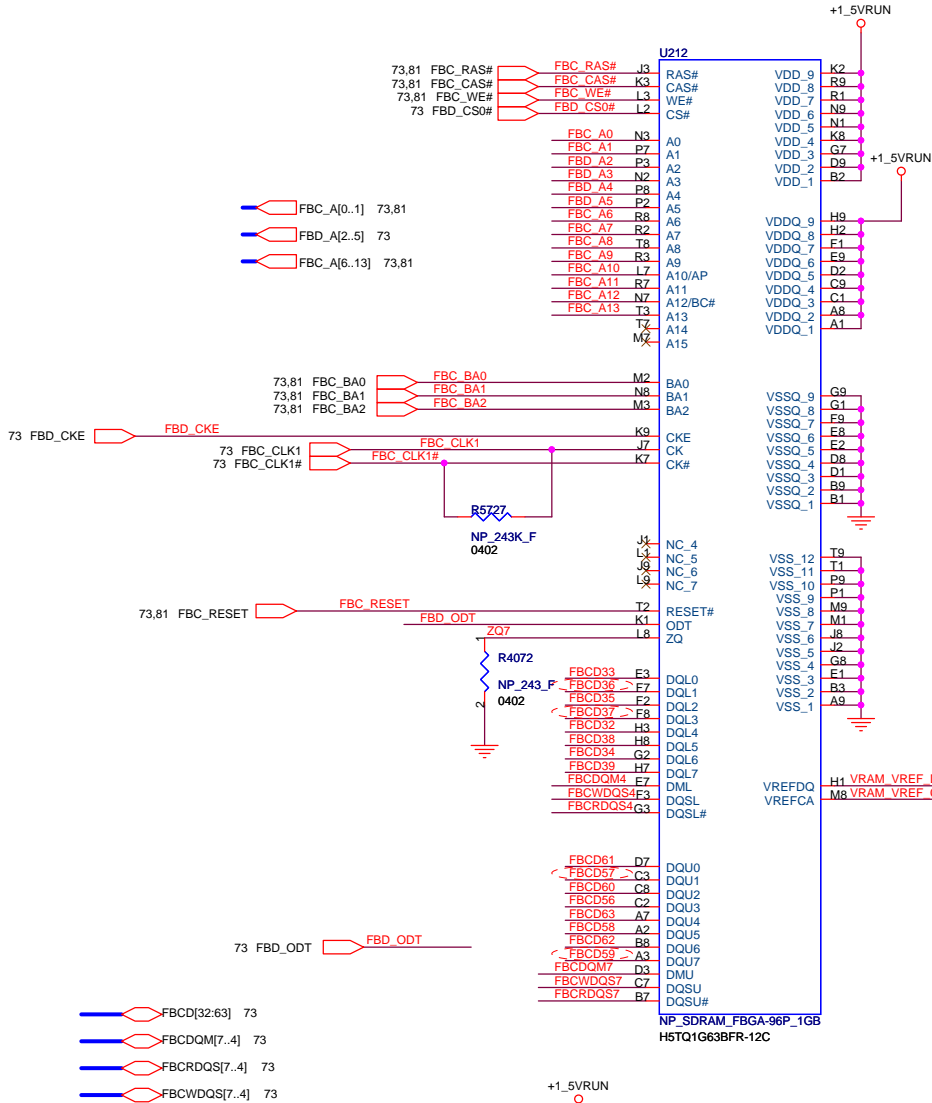
	0...30	32...63
CMDO	A4	
CMO1	RAS#	RAS#
CMO2	A5	
CMO3	BA1	BA1
CMO4	A2	
CMO5	A4	
CMO6	A3	
CMO7		CKE
CMO8		CSO#
CMO9	A11	A11
CMO10	CAS#	CAS#
CMO11	WE#	WE#
CMO12	BA0	BA0
CMO13		A5
CMO14	A12	A12
CMO15	RST	RST
CMO16	A7	A7
CMO17	A10	A10
CMO18	CKE	
CMO19	A0	A0
CMO20	A9	A9
CMO21	A6	A6
CMO22	A2	
CMO23	A8	A8
CMO24	A3	
CMO25	A1	A1
CMO26	A13	A13
CMO27	BA2	BA2
CMO28		ODT
CMO29	CSO#	
CMO30	ODT	



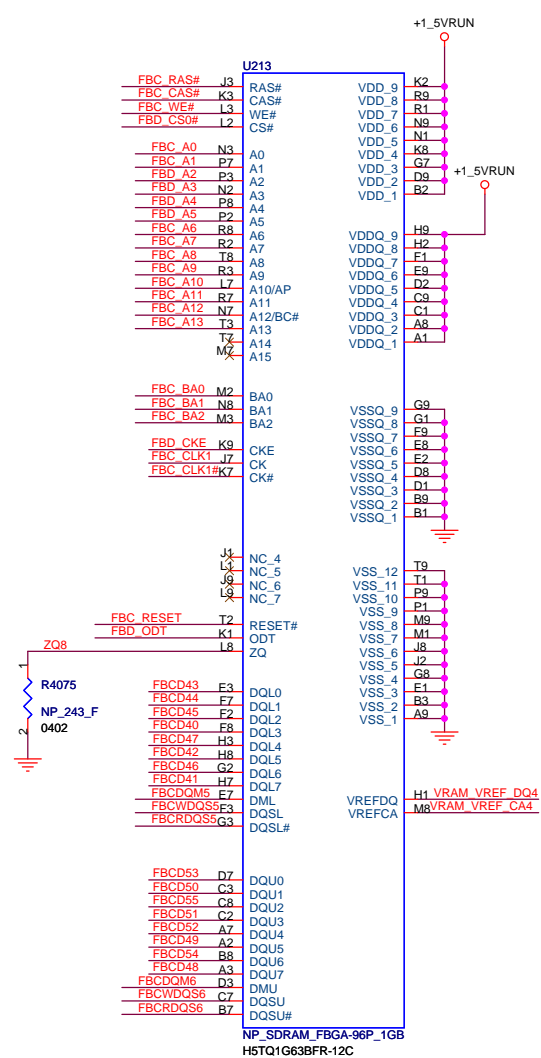
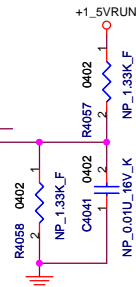


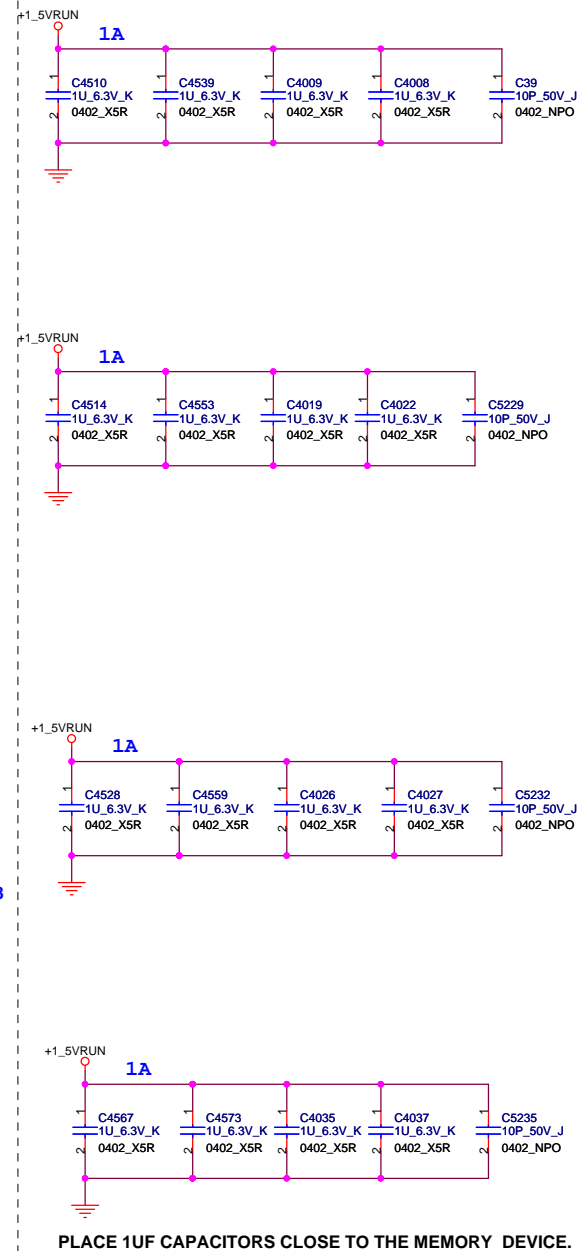
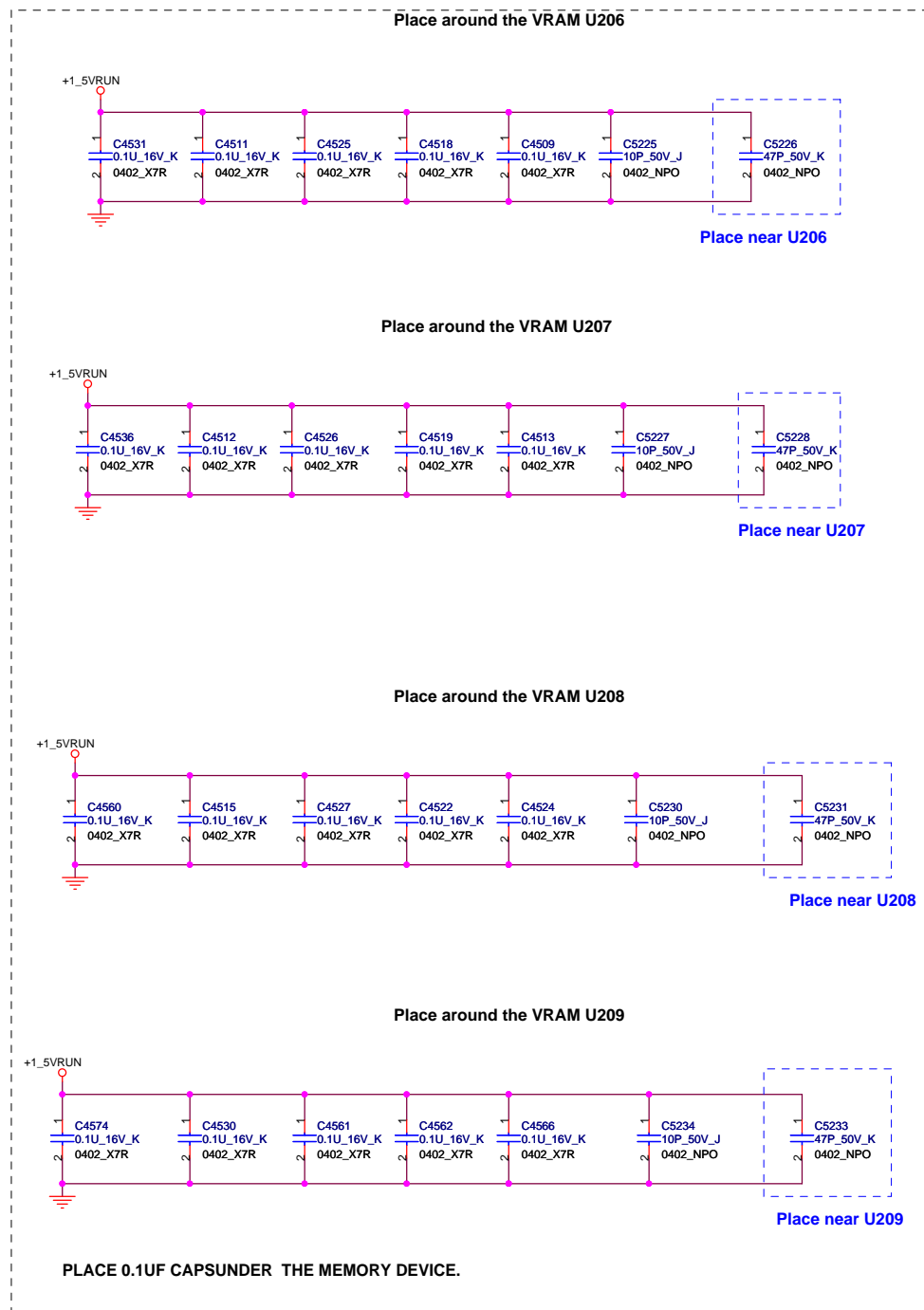
	0...30	32...63
CMD0	A4	RAS#
CMD1	RAS#	RAS#
CMD2	A5	BA1
CMD3	BA1	A2
CMD4	A4	A3
CMD5	A3	CKE
CMD6	CKE	CS0#
CMD7	A11	A11
CMD8	CAS#	CAS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	A5	A5
CMD12	A12	A12
CMD13	RST	RST
CMD14	A7	A7
CMD15	A10	A10
CMD16	A0	A0
CMD17	A9	A9
CMD18	A6	A6
CMD19	A2	A2
CMD20	A8	A8
CMD21	A3	A3
CMD22	A1	A1
CMD23	A13	A13
CMD24	BA2	BA2
CMD25	CS0#	ODT
CMD26	ODT	
CMD27		
CMD28		
CMD29		
CMD30		



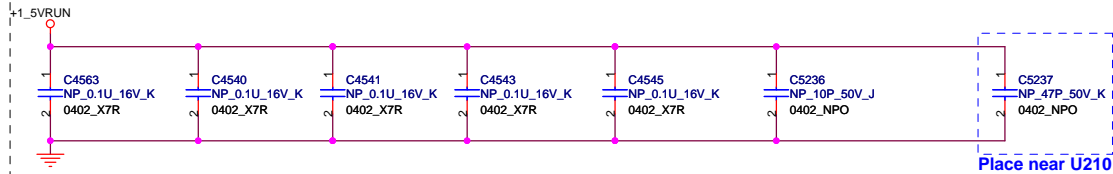


	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	A7	CSE
CMD8		CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A5	A5
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS0#	
CMD30	ODT	



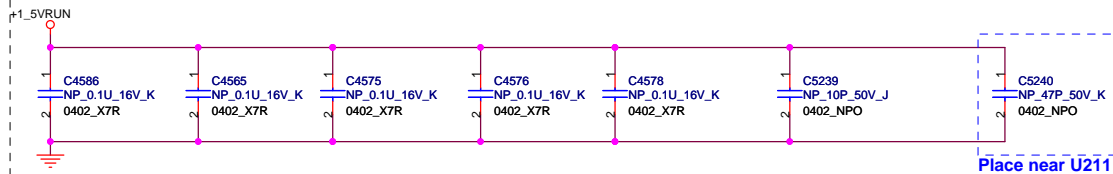


Place around the VRAM U210



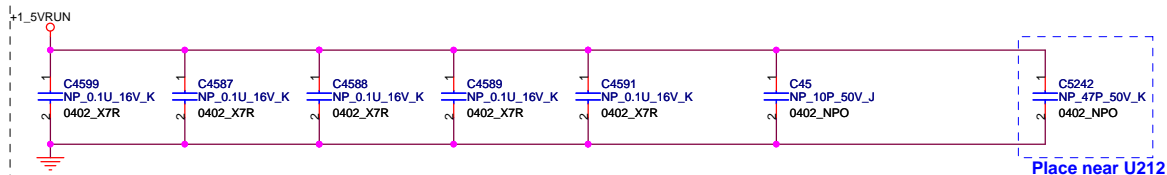
Place near U210

Place around the VRAM U211



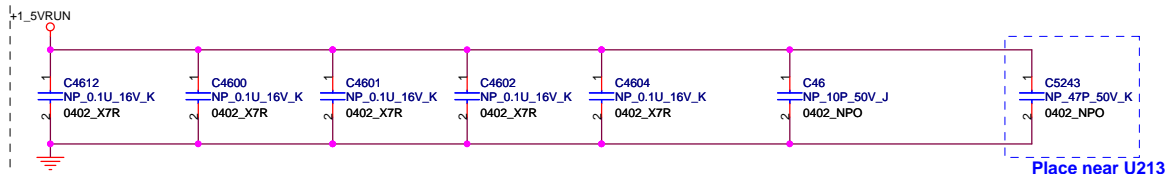
Place near U211

Place around the VRAM U212



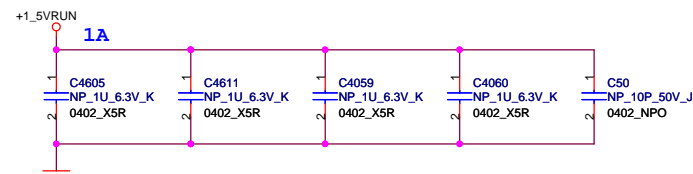
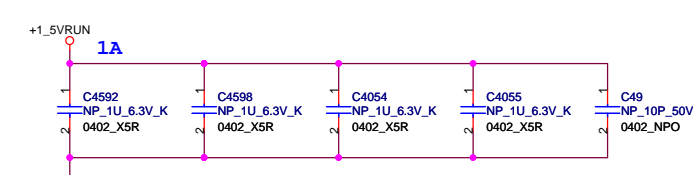
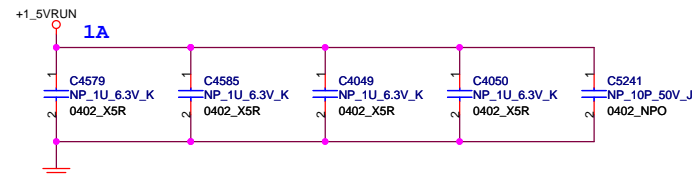
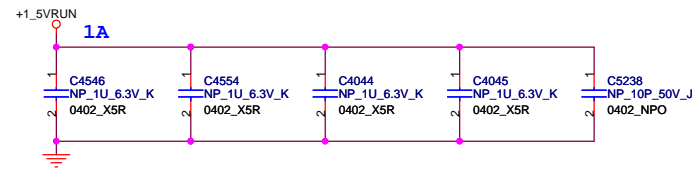
Place near U212

Place around the VRAM U213

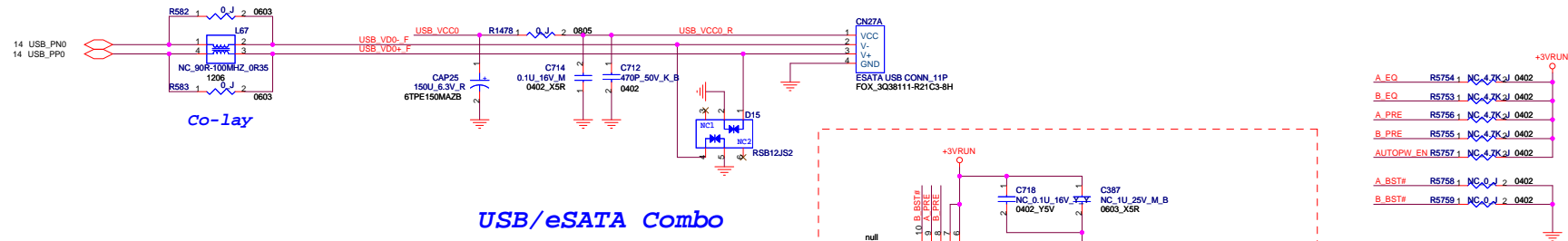
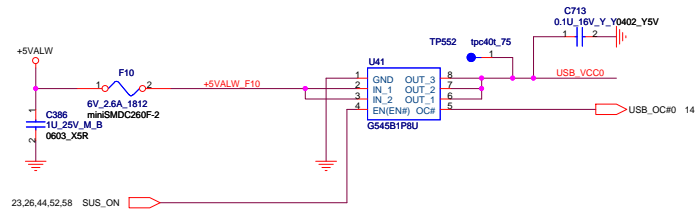


Place near U213

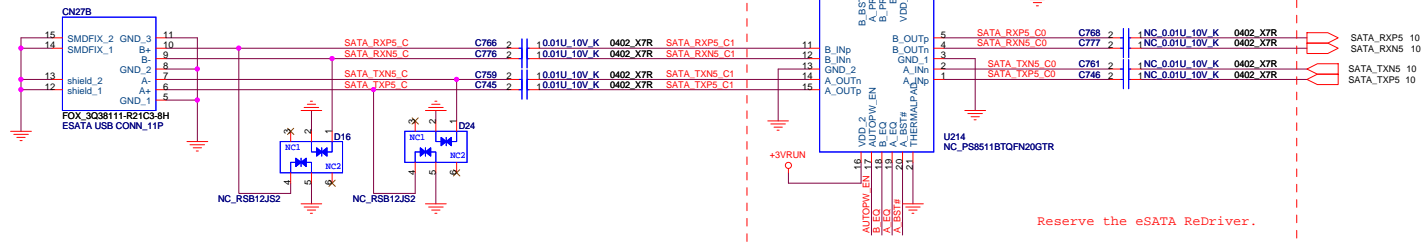
PLACE 0.1UF CAPSUNDER THE MEMORY DEVICE.



PLACE 1UF CAPACITORS CLOSE TO THE MEMORY DEVICE.

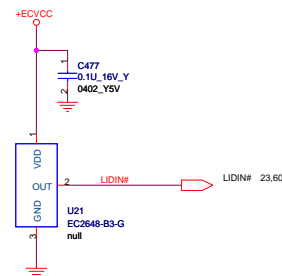


USB/eSATA Combo

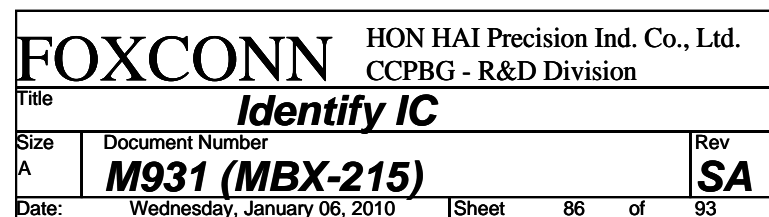


Close to U124 ,Pin11 ,12 ,14 ,15

Close to U124 and C768 ,C777 ,C761 ,C746 Pin2



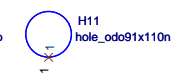
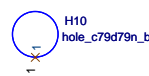
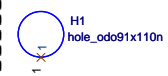
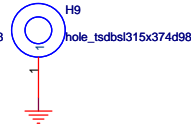
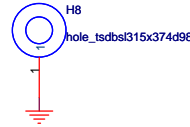
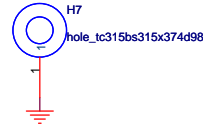
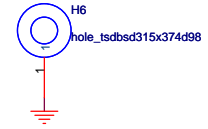
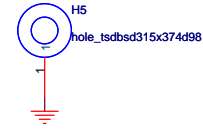
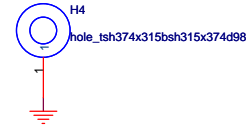
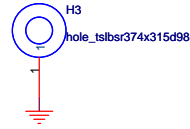
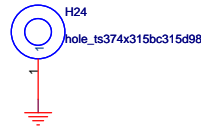
LID Switch



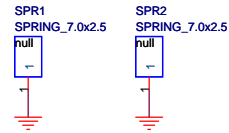
AMI Label (For MP Only)

TABLE1
NC_AMI-APTIO

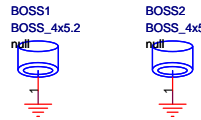
MB PAD & Screw Hole



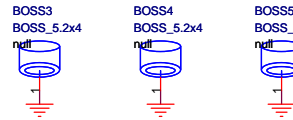
NPTH



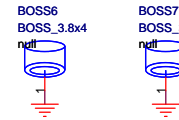
EMI SPRING



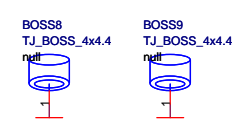
WLAN Module



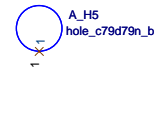
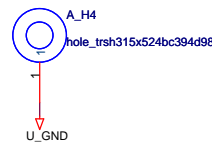
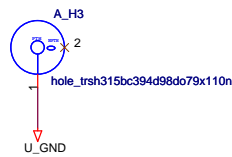
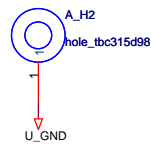
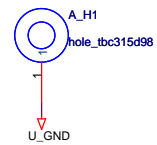
Thermal Modul



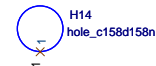
Bluetooth Bracket



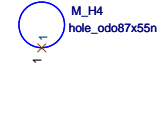
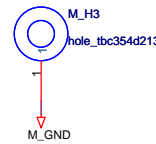
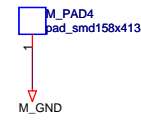
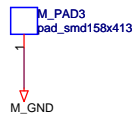
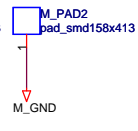
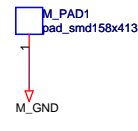
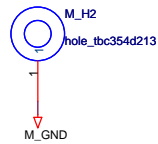
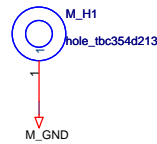
T-jet (MACH)



Audio & USB DB

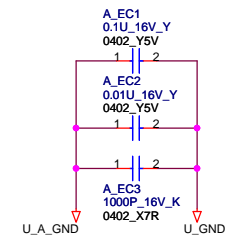
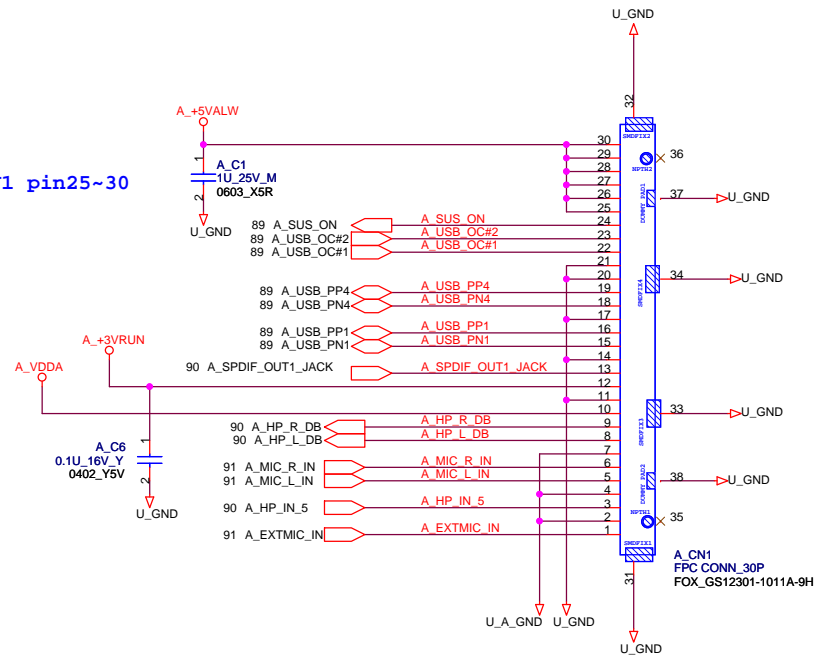


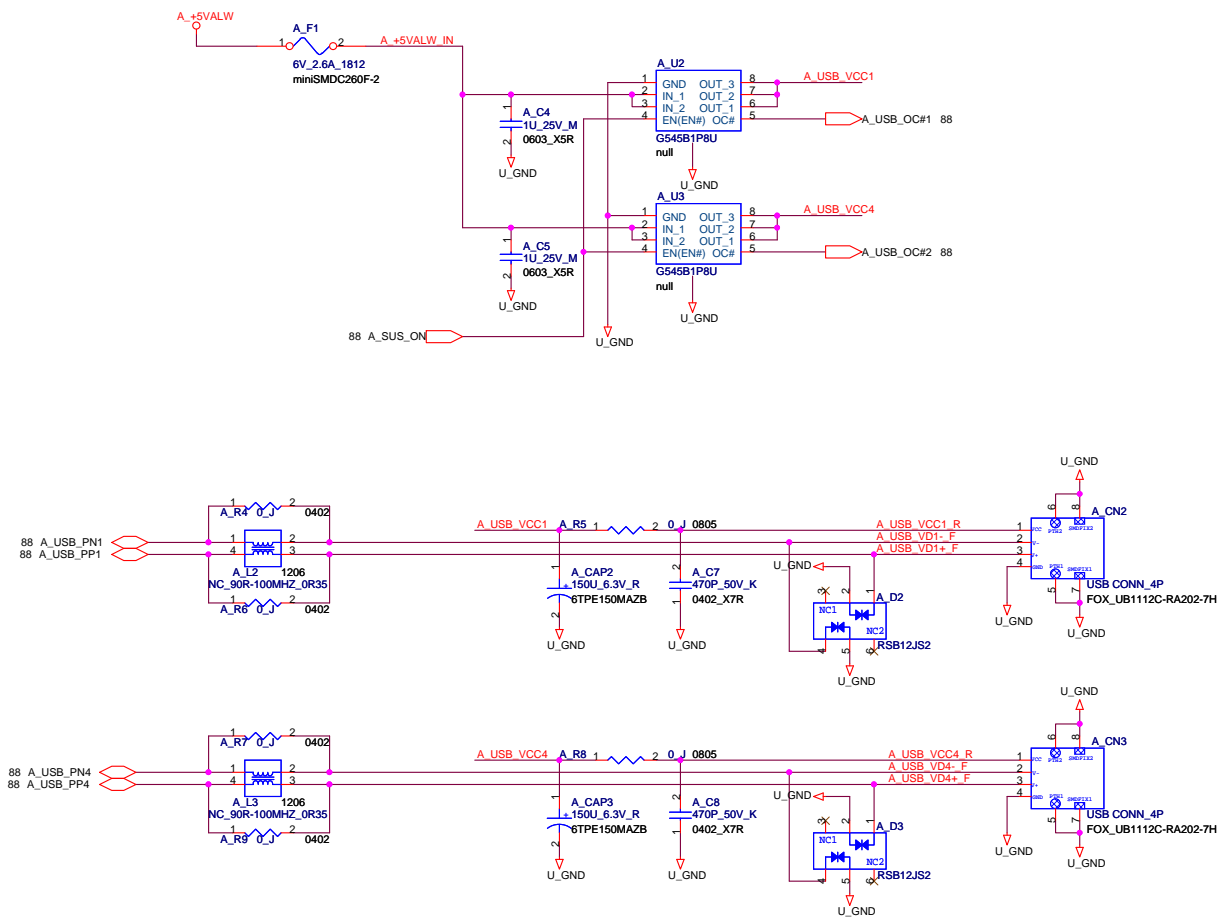
CPU Plate

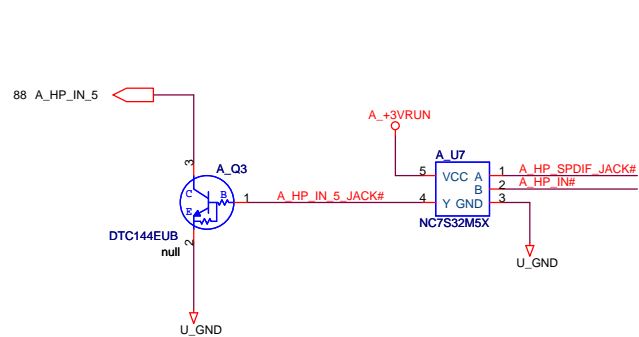
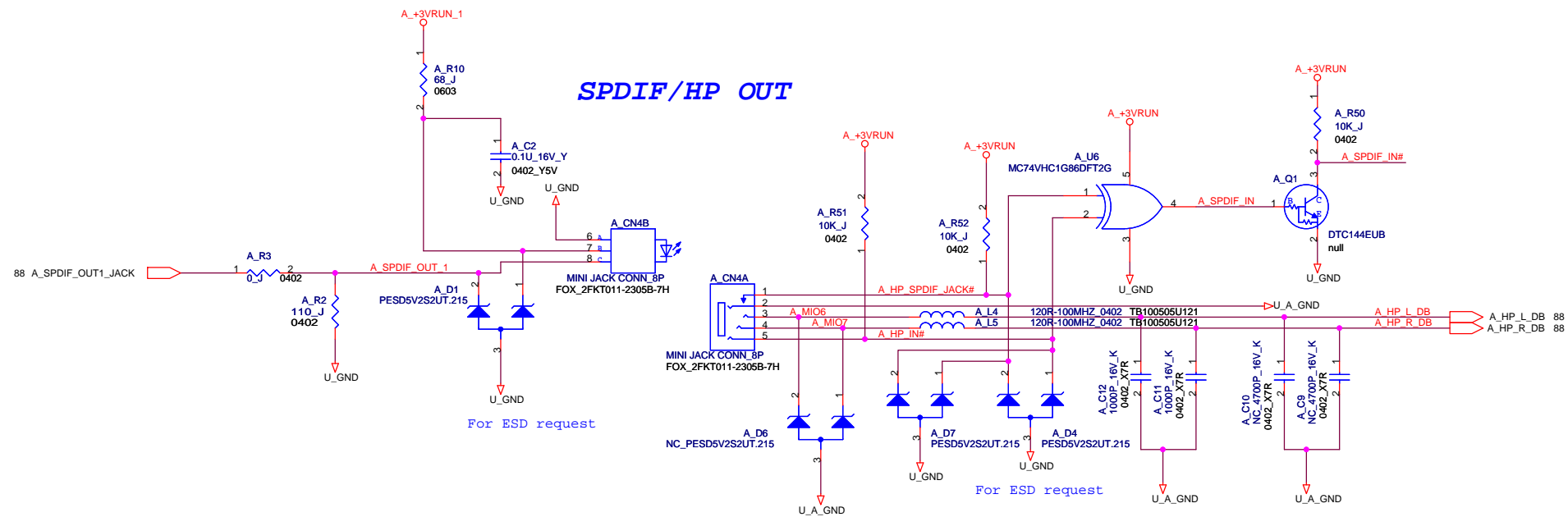


Switch DB

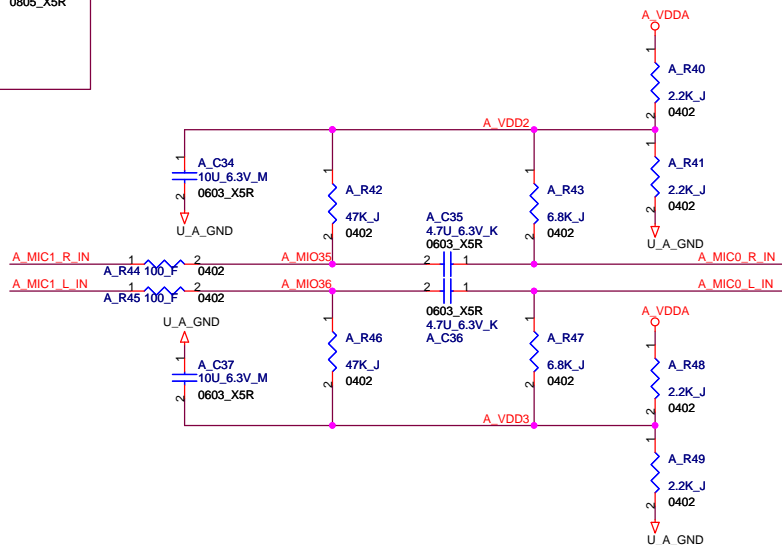
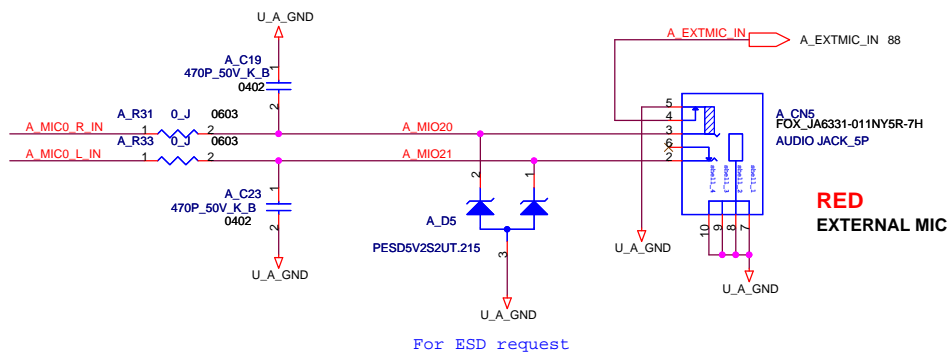
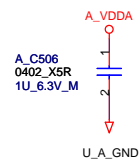
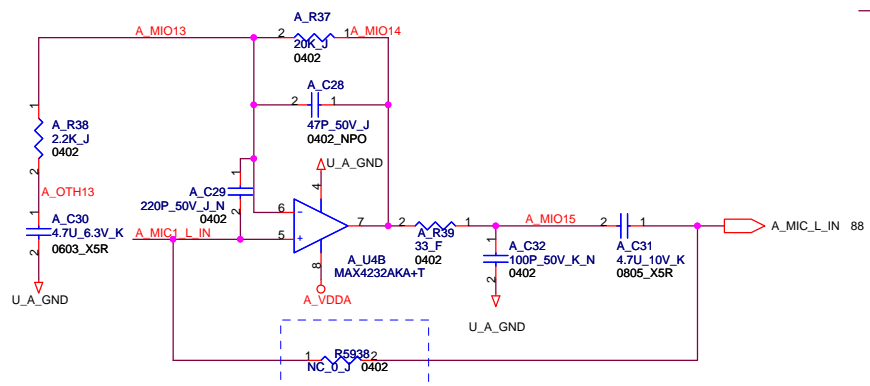
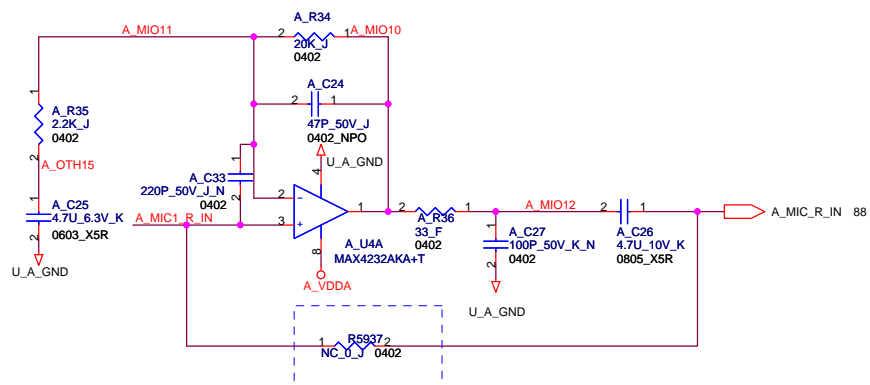
Place A_C1 close to A_CN1 pin25~30

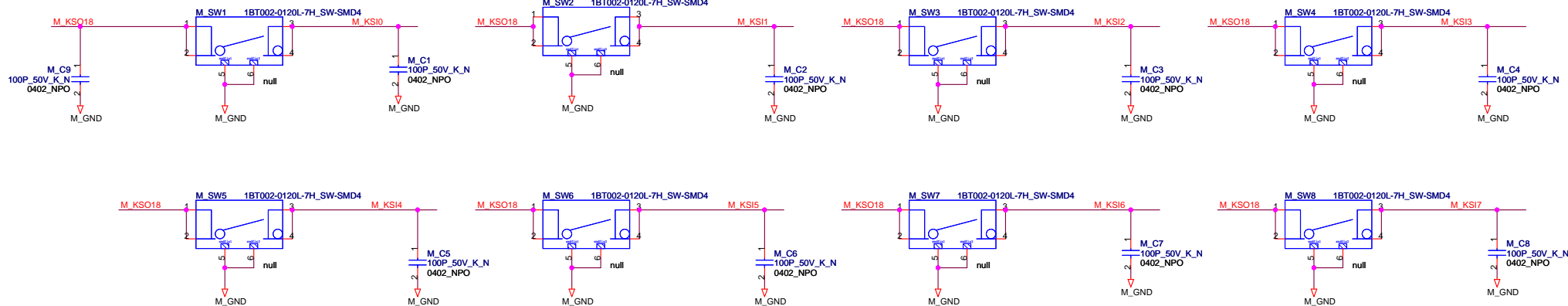
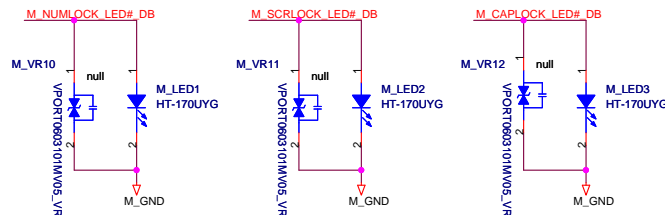
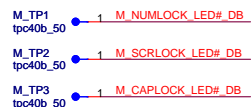
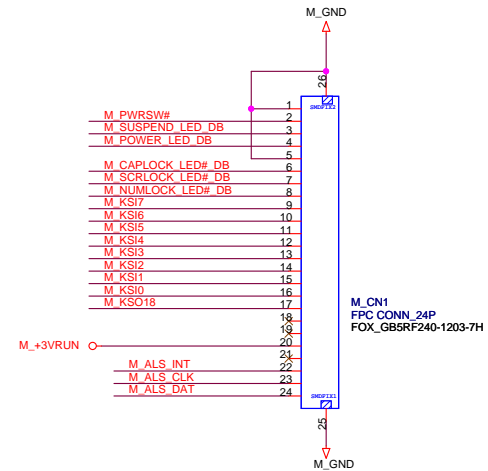
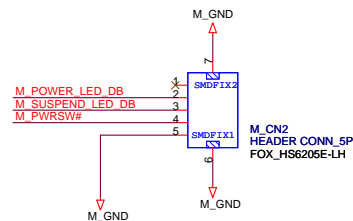
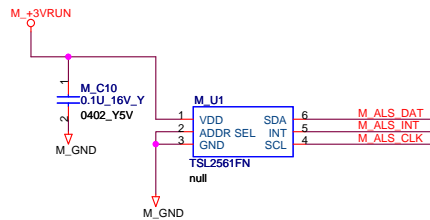






	Pin 1	Pin 5	LED A_SPDIF_IN#	A_HP_IN_5
HP	0	0	1 off	1
SPDIF	0	1	0 on	0
No plug	1	1	1 off	0





(2009/11/27) M930-MP ECN Changed
P.48 {DCIN} PR11 Change to SMD,RES,11.8K,1/16W,1%,0402
P.48 {DCIN} PR12 Change to SMD,RES,10K,1/16W,1%,0402
P.48 {DCIN} PR220 Change to SMD,RES,10.2K,1/16W,1%,0402
P.57 {VGA Power} PR566 Change to SMD,RES,88.7K,1/16W,1%,0402
P.51 {VTT Power} PR26 Change to SMD,RES,2.2ohm,1/10W,5%,0603
P.51 {VTT Power} PR152 Change to SMD,RES,4.7ohm,1/10W,5%,0603
P.51 {VTT Power} PC130 Change to SMD,MLCC,X7R,680pF,50V,10%,0603(0.8mm)
P.12 {PCH} Delete D28, D29
P.92 {DB} Delete M_VR1,M_VR2,M_VR3,M_VR4,M_VR5,M_VR6,M_VR7,M_VR8,M_VR9
P.92 {DB} Add M_VR10,M_VR11, M_VR12
P.23 {EC} Add C487 ,SMD,MLCC,X7R,1000pF,16V,10%,0402
P.27 {WLAN} SW4 Change to ALPS,SSSS811101,Switch,SMD-7,Slide SW
P.64 {CODEC} Change U215 vendor number from ALC275SQ-GR-A5 to ALC275SQ-GR

(2009/12/02)
P.2 {Block Digram} Revised Model Name and Feature
P.4 {CPU} Short RP80
P.7 {CPU} Short R1561
P.9 {CPU} Short R1586, R1587
P.11 {PCH} Short RP69 ,RP71 ,RP67 ,RP70 ,RP78 ,RP68 ,RP89
P.12 {PCH} Short R927
P.19 {CLK} Short RP9 ,RP84 ,RP85 ,RP79
P.23 {EC} Delete RP23
P.26 {ExpressCard} Short R343, R337 ,Delete L40
P.27 {WLAN} Short R22
P.36 {Camera} Short R376 ,R377 ,Delete L46
P.37 {Felica} Short R192 ,R193 ,Delete L25
P.39 {BT} Change R7 to 100ohm as RF team Request.
P.39 {BT} Delete U1 ,R6 ,C6 ,U12
P.41 {KB} Short R695
P.43 {TP} Short R533 ,Delete R530
P.46 {Thermal} Delete D20 ,C547 ,C534 ,U26 ,R946 ,R61
P.46 {Thermal} Delete U5 ,R65 ,C42 ,R54 ,R53 ,R60
P.62 {HDMI} Delete L57 ,L60 ,L74 ,L76 ,Short R495 ,R483 ,R487 ,R492 ,R489 ,R498 ,R499 ,R494
P.64 {Audio} Short R5767.
P.85 {eSATA} Reserved C768 ,C777 ,C761 ,C746 ,U214
P.85 {eSATA} Delete L62 ,L66 ,Short R589 ,R588 ,R592 ,R591
P.86 {BAT ID} Short PR125

(2009/12/18)
P.57 {VGA Power} Change PR182 to PWRCNTL_0 Net.
P.57 {VGA Power} Change PR180 to PWRCNTL_1 Net.
P.11 {PCH} U69 P/N :12-1BEXPEA-0004 (INTEL,BD82PM55 SLH23,BGA-1071,Intel Platform Controller Hub)
P.35 {SD} Reserve the R1590 for SD Slot (CN29) Damppling.
P.52 {0.75VPower} Change PC143 to 1C-2B20104-K300 (0.1uF/X7R/10%)

(2009/12/23)
P.76 {VGA} Reserve the TP245 and TP246
P.52 {DDR3 Power} Reserve the PR150 /PR157 Path

(2009/12/29)
P.51 {VTTV Power} Reserve the CAP32 for Power Noise Reduce
P.52 {1.5V Power} Reserve the CAP33 for Power Noise Reduce
P.57 {VGA Power} Reserve the CAP34 for Power Noise Reduce

(2010/01/06)
P.34 {SD} Revise R817 pull-up connection from +3VRUN to VCC_SD