

Compal Confidential

Model Name :Q5WV1/Q5WS1

Compal Project Name :

File Name : LA-7912P

Compal Confidential

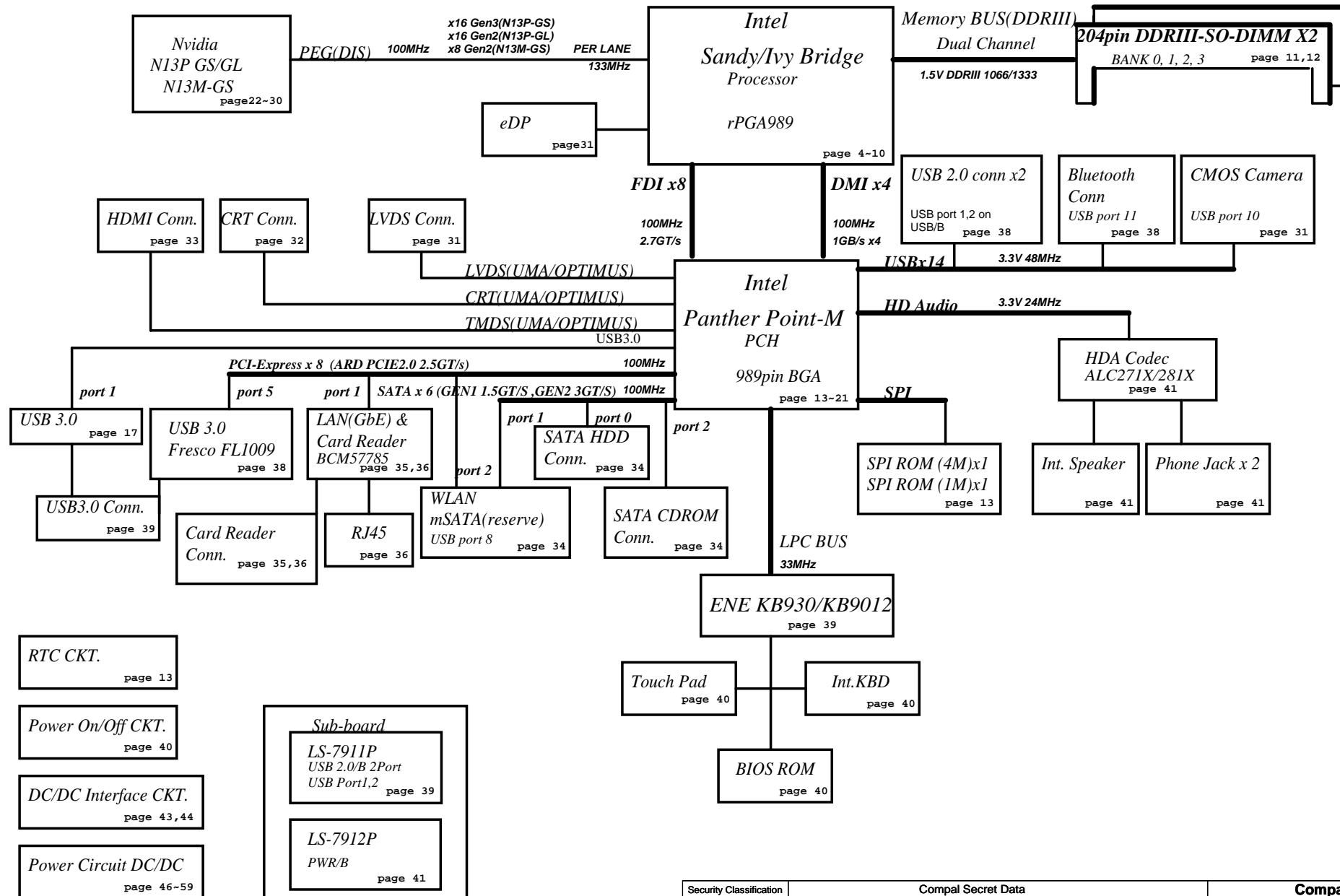
Q5WV1 M/B Schematics Document  
Intel Sandy/Ivy Bridge Processor with DDRIII + Panther Point PCH  
Nvidia N13P GS/GL

2012-02-03b  
REV : 0 . 3

MB PCB	
Part Number	Description
DA60000SV00	PCB 0N4 LA-7912P REV0 M/B



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

## EC SM Bus2 address

## PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

4319IDBOL01SMT MB A7912 Q5WV1 HM77 QC UMA 3
4319IDBOL02SMT MB A7912 Q5WV1 HM77 QC 13PGL1G 3
4319IDBOL03SMT MB A7912 Q5WV1 HM77 QC 13PGL2G 3
4319IDBOL04SMT MB A7912 Q5WV1 HM77 QC 13PGS1G 3
4319IDBOL05SMT MB A7912 Q5WV1 HM77 QC 13PGS2G 3
4319IDBOL06SMT MB A7912 Q5WV1 HM77 DC UMA 2
4319IDBOL07SMT MB A7912 Q5WV1 HM77 DC UMA 3
4319IDBOL08SMT MB A7912 Q5WV1 HM77 DC 13PGL1G 2
4319IDBOL09SMT MB A7912 Q5WV1 HM77 DC 13PGL1G 3
4319IDBOL10SMT MB A7912 Q5WV1 HM77 DC 13PGL2G 2
4319IDBOL11SMT MB A7912 Q5WV1 HM77 DC 13PGL2G 3
4319IDBOL12SMT MB A7912 Q5WV1 HM77 DC 13MGS1G 2
4319IDBOL13SMT MB A7912 Q5WV1 HM77 DC 13MGS1G 3
4319IDBOL14SMT MB A7912 Q5WV1 HM77 DC 13PGS2G 3

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	0.1
4	0.2
5	0.3
6	0.4
7	

## BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAC@
Dis with OPTIMUS	DIS@
Blue Tooth	BT@
Internal USB 3.0	PUSB3@
Internal USB 2.0	PUSB@
USB 2.0 flag	PUSB2@
eDP	eDP@
VRAM	X76@
Connector	CONN@
Unpop	@
N13P-GS	GS@
N13P-GL	GL@
Win8	Win8@
Audio ALC271X	271X@
Audio ALC281X	281X@
PCH HM65	HM65@
PCH HM76	HM76@
N13P-GS & GL	GSGL@
N13M-GS	GM@
support AC function	AC@
no AC function	NOAC@

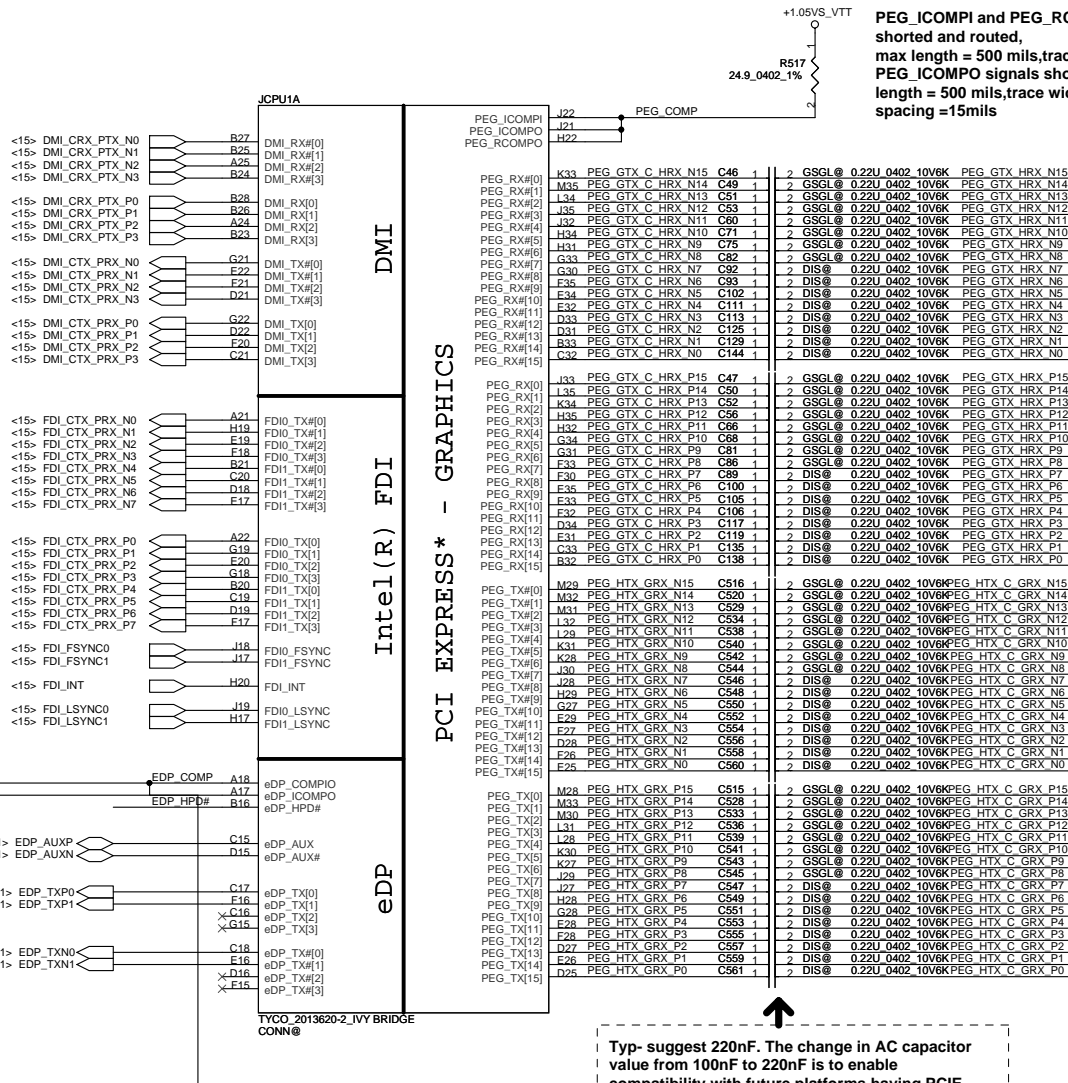
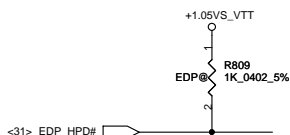
## USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB3.0 colay USB2.0 Conn
		1	USB/B (Right Side)
		2	USB/B (Right Side)
	UHCI1	3	
		4	
		5	
	UHCI2	6	
EHCI2	UHCI3	7	
		8	Mini Card 1(WLAN)
	UHCI4	9	
		10	Camera
		11	BlueTooth
	UHCI5	12	
		13	

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eDP\_COMPIO and ICOMPO signals should be shorted near balls,  
Trace Width for EDP\_COMPIO=4mils,  
EDP\_ICOMPO=12mils,  
and both length less than 500 mils...  
should not be left floating  
,even if disable eDP function...

Add eDP circuit

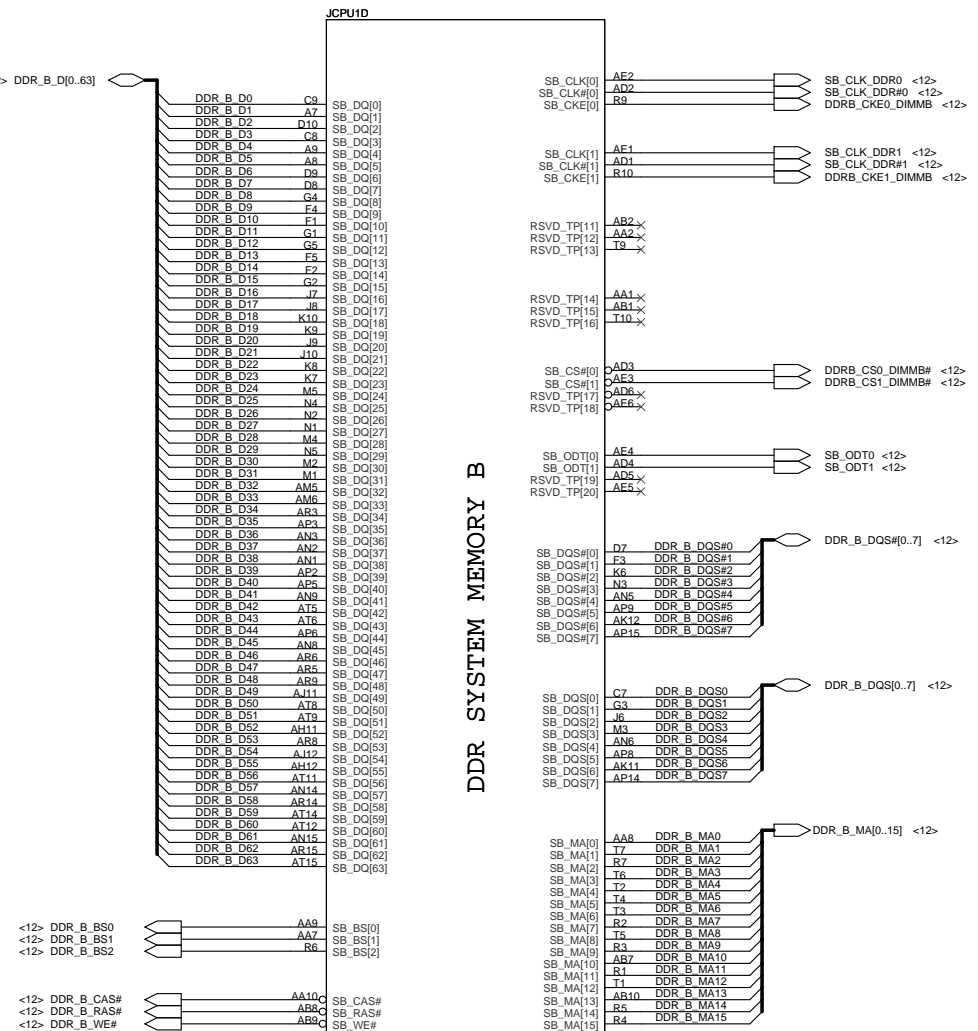
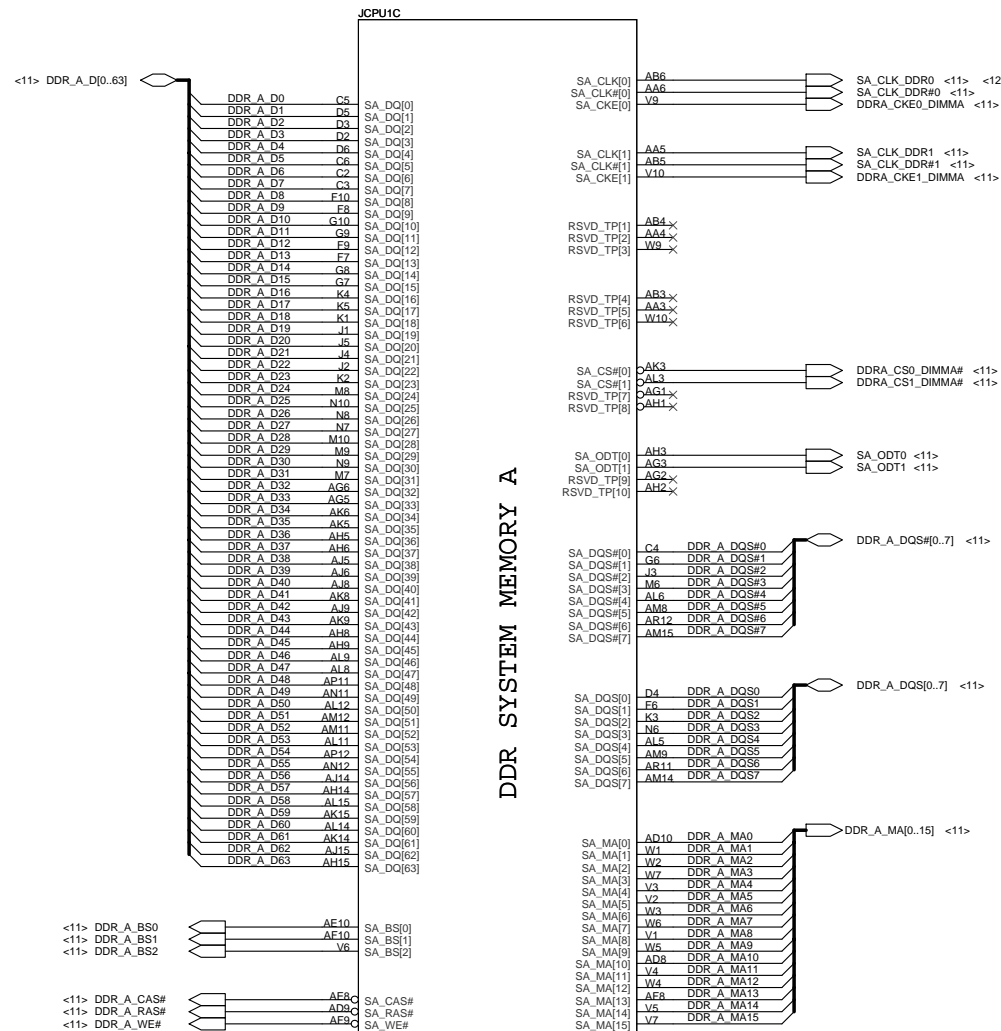


PEG\_ICOMPI and PEG\_RCOMPO signals should be shorted and routed,  
max length = 500 mils,trace width=4mils  
PEG\_ICOMPO signals should be routed with - max  
length = 500 mils,trace width=12mils  
spacing =15mils

PEG\_TX[0] GRX\_N[0..15] <22>  
PEG\_TX[0] GRX\_P[0..15] <22>  
PEG\_TX[0] GRX\_N[0..15] <22>  
PEG\_TX[0] GRX\_P[0..15] <22>

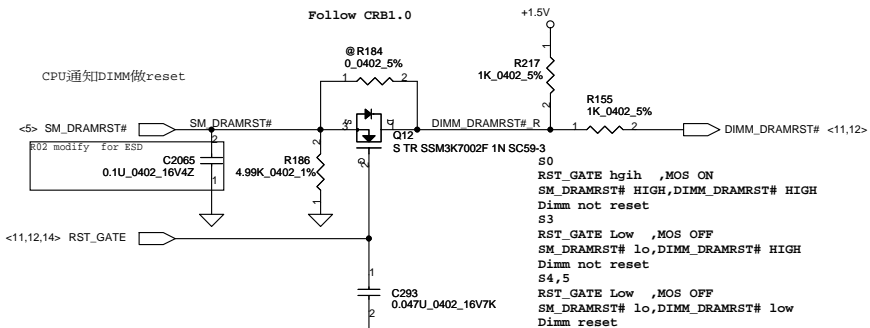
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DDR SYSTEM MEMORY A

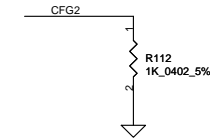
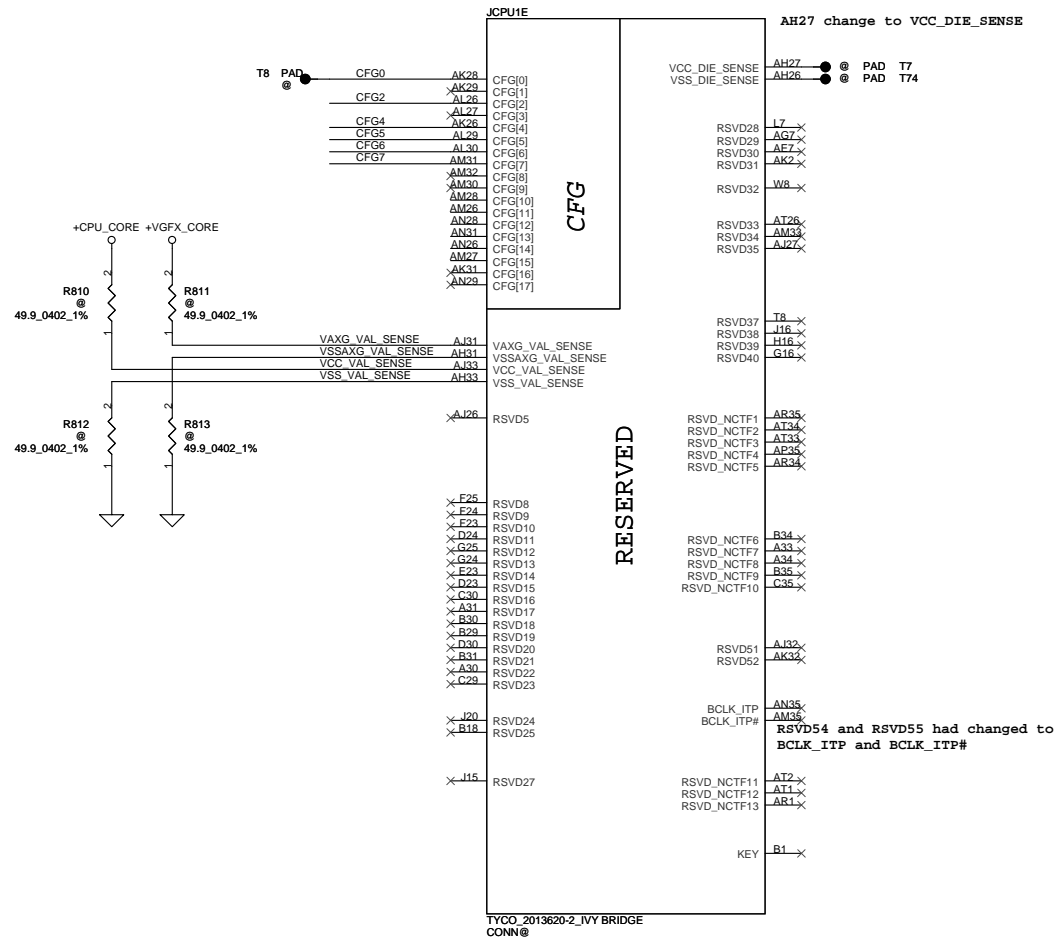
DDR SYSTEM MEMORY B



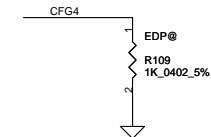
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## CFG Straps for Processor

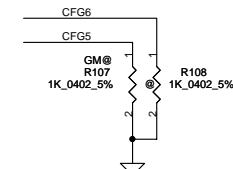
AH26	Sandy	Ivy
	GND	VSS_DIE_SENS



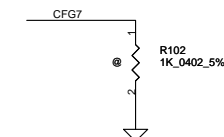
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<p>1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>★ 0: Lane Reversed</p>



Display Port Presence Strap	
CFG4	<p>★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

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SV type CPU JCPU1F

+CPU\_CORE  
QC 53A  
DC 53A

AG35 VCC1  
AG34 VCC2  
AG33 VCC3  
AG32 VCC4  
AG31 VCC5  
AG30 VCC6  
AG29 VCC7  
AG28 VCC8  
AG27 VCC9  
AG26 VCC10  
AF35 VCC11  
AF34 VCC12  
AF33 VCC13  
AF32 VCC14  
AF31 VCC15  
AF30 VCC16  
AF29 VCC17  
AF28 VCC18  
AF27 VCC19  
AD26 VCC20  
AD35 VCC21  
AD34 VCC22  
AD33 VCC23  
AD32 VCC24  
AD31 VCC25  
AD30 VCC26  
AD29 VCC27  
AD28 VCC28  
AD27 VCC29  
AD26 VCC30  
AC35 VCC31  
AC34 VCC32  
AC33 VCC33  
AC31 VCC34  
AC30 VCC35  
AC29 VCC36  
AC28 VCC37  
AC27 VCC38  
AC26 VCC39  
AA35 VCC40  
AA34 VCC41  
AA33 VCC42  
AA32 VCC43  
AA31 VCC44  
AA30 VCC45  
AA29 VCC46  
AA28 VCC47  
AA27 VCC48  
AA26 VCC49  
Y35 VCC50  
Y34 VCC51  
Y33 VCC52  
Y32 VCC53  
Y31 VCC54  
Y30 VCC55  
Y29 VCC56  
Y28 VCC57  
Y27 VCC58  
Y26 VCC59  
V35 VCC60  
V34 VCC61  
V33 VCC62  
V32 VCC63  
V31 VCC64  
V30 VCC65  
V29 VCC66  
V28 VCC67  
V27 VCC68  
V26 VCC69  
U35 VCC70  
U34 VCC71  
U33 VCC72  
U32 VCC73  
U31 VCC74  
U30 VCC75  
U29 VCC76  
U28 VCC77  
U27 VCC78  
U26 VCC79  
R35 VCC80  
R34 VCC81  
R33 VCC82  
R32 VCC83  
R31 VCC84  
R30 VCC85  
R29 VCC86  
R28 VCC87  
R27 VCC88  
R26 VCC89  
P35 VCC90  
P34 VCC91  
P33 VCC92  
P32 VCC93  
P31 VCC94  
P30 VCC95  
P29 VCC96  
P28 VCC97  
P27 VCC98  
P26 VCC99  
P25 VCC100

## POWER

8.5A

+1.05VS\_VTT

VCCIO1 AH13  
VCCIO2 AH10  
VCCIO3 AC10  
VCCIO4 Y10  
VCCIO5 U10  
VCCIO6 P10  
VCCIO7 L10  
VCCIO8 J14  
VCCIO9 J13  
VCCIO10 J12  
VCCIO11 J11  
VCCIO12 H14  
VCCIO13 H12  
VCCIO14 H11  
VCCIO15 G14  
VCCIO16 G13  
VCCIO17 G12  
VCCIO18 F14  
VCCIO19 F13  
VCCIO20 F12  
VCCIO21 F11  
VCCIO22 E14  
VCCIO23 E12  
VCCIO24 J23  
VCCIO25 F11  
VCCIO26 D14  
VCCIO27 D13  
VCCIO28 D12  
VCCIO29 D11  
VCCIO30 C14  
VCCIO31 C13  
VCCIO32 C12  
VCCIO33 C11  
VCCIO34 B14  
VCCIO35 B12  
VCCIO36 A14  
VCCIO37 A13  
VCCIO38 A12  
VCCIO39 A11  
VCCIO40 J23

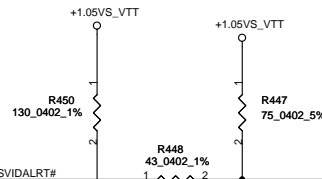
PEG AND DDR

CORE SUPPLY

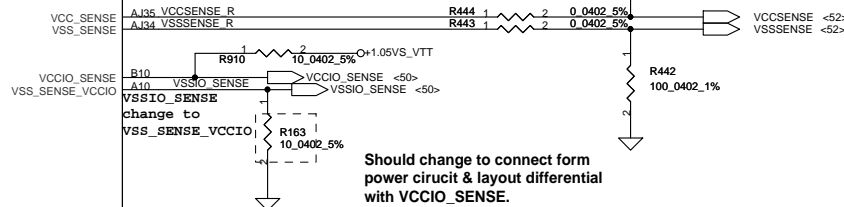
SVID

SENSE LINES

VIDALERT# H CPU SVIDALRT#  
VIDSCLK H CPU SVIDCLK  
VIDSOUT H CPU SVIDDAT



Place the PU resistors close to CPU



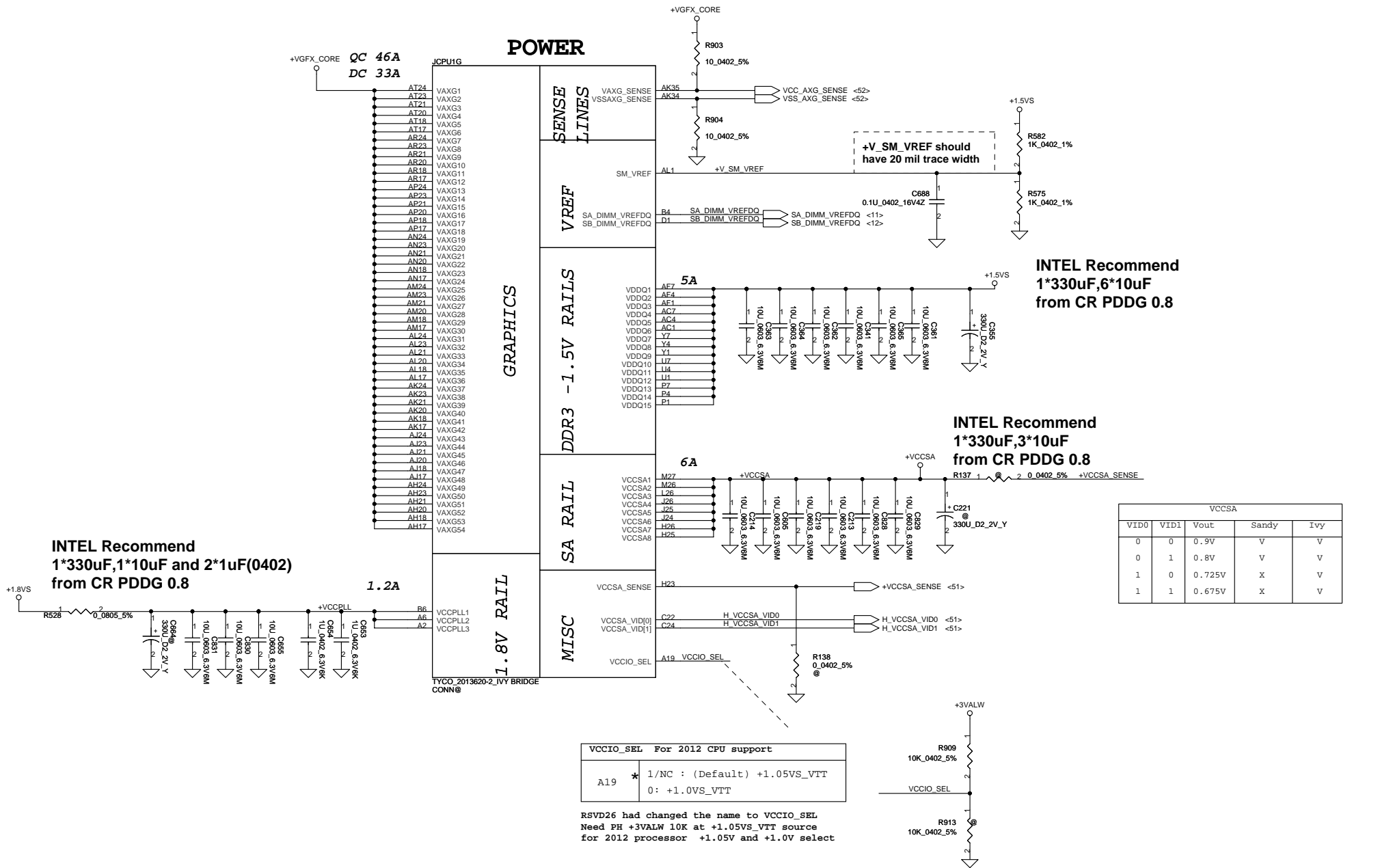
Should change to connect form power circuit & layout differential with VCCIO\_SENSE.

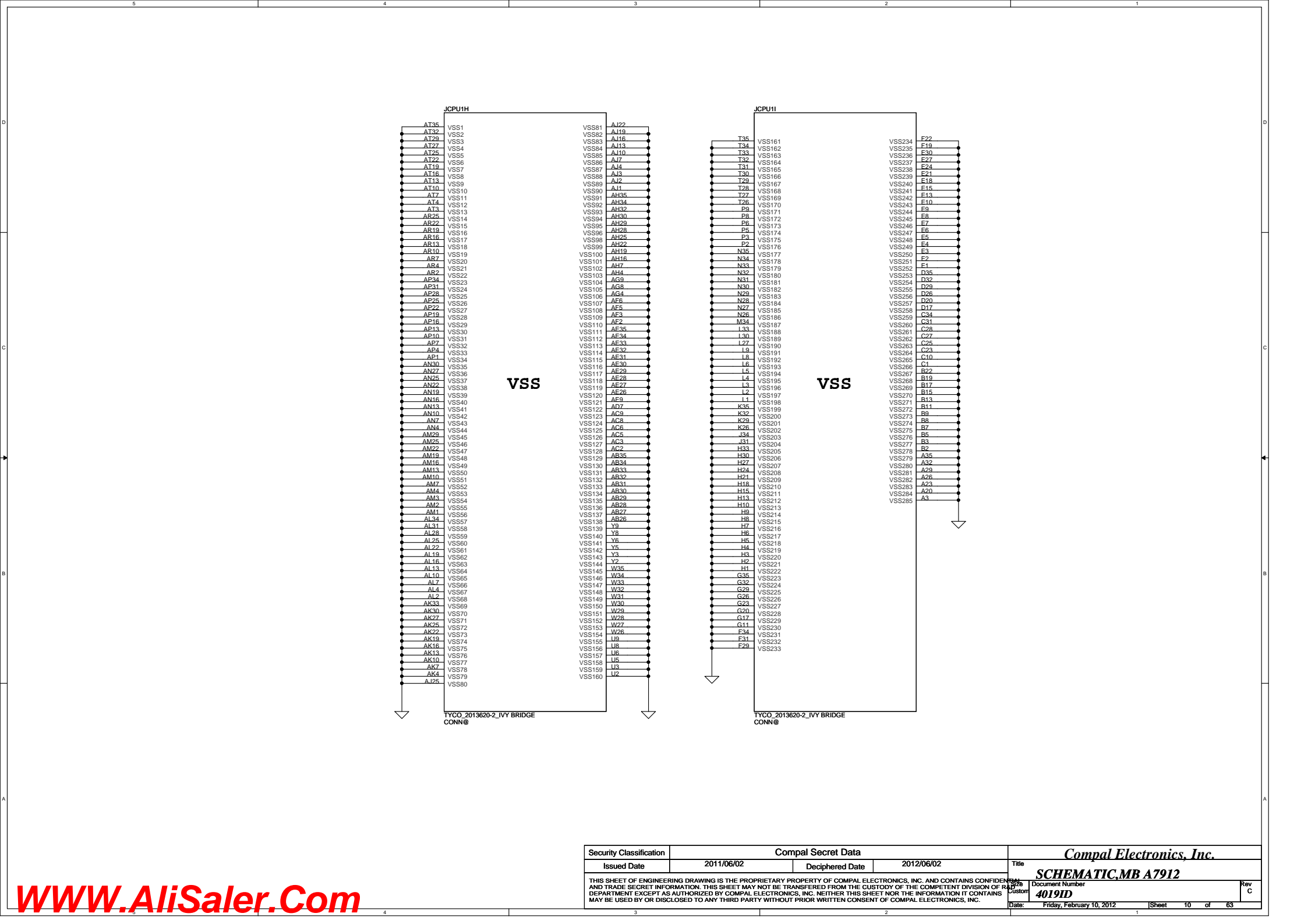
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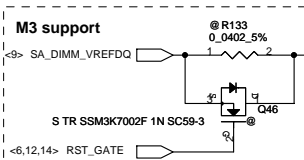
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All VREF traces should have 10 mil trace width

<6> DDRA\_CKE0\_DIMMA

<6> DDR\_A\_BS2

<6> SA\_CLK\_DDR0

<6> SA\_CLK\_DDR#0

<6> DDR\_A\_BS0

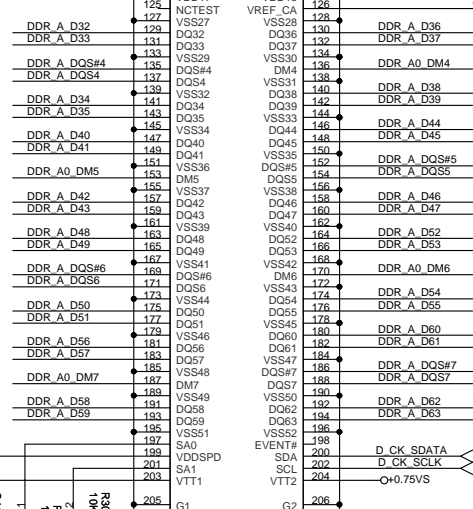
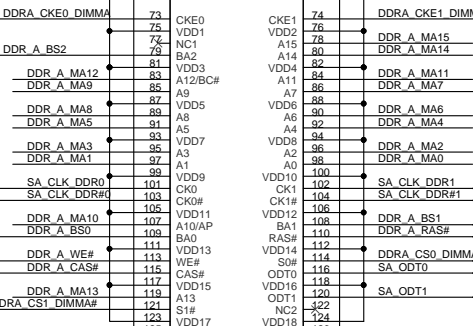
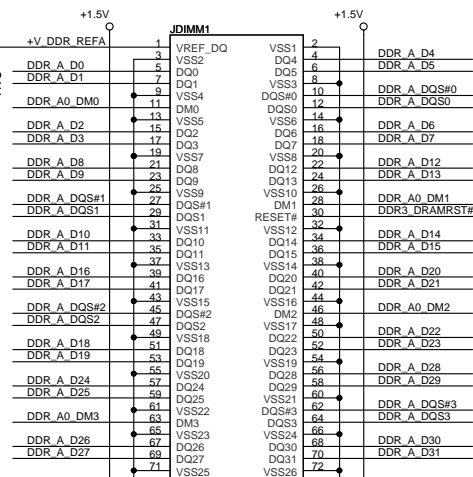
<6> DDR\_A\_WE#

<6> DDR\_A\_CAS#

<6> DDRA\_CS1\_DIMMA#

<Address(SA1,SA0): 00>

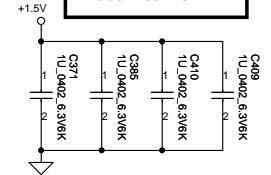
DIMM\_1 Reserve H:8mm



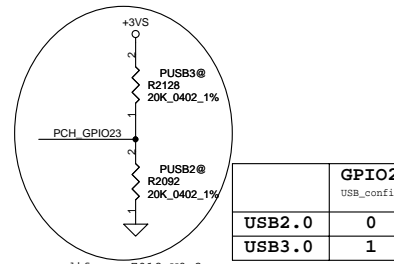
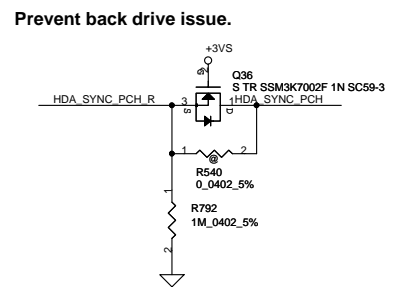
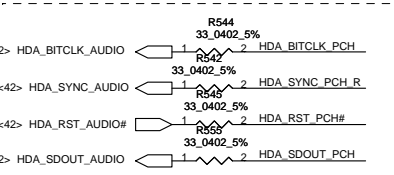
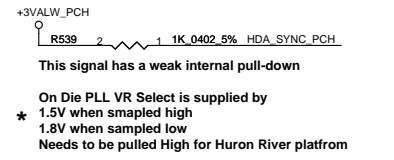
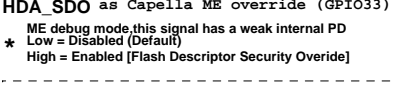
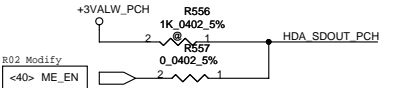
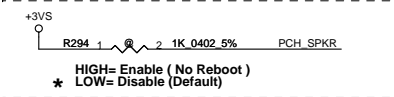
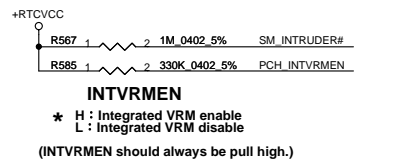
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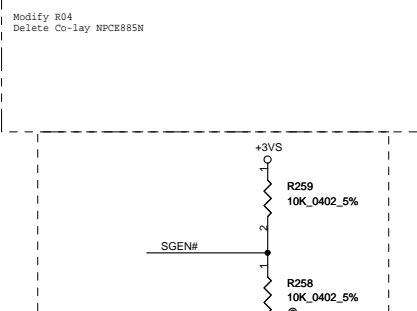
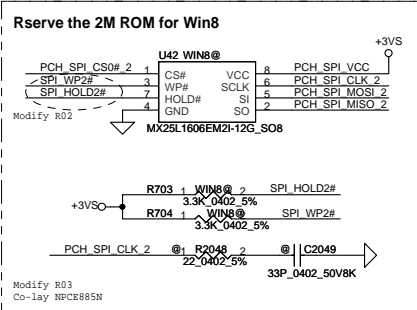
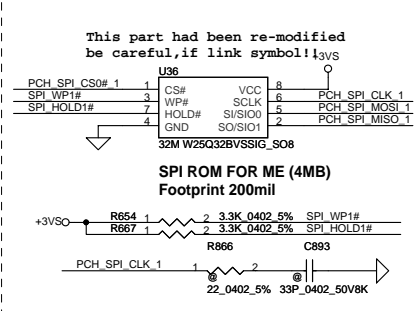
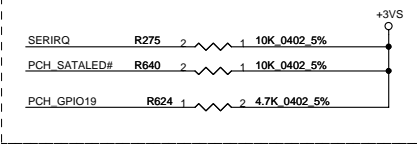
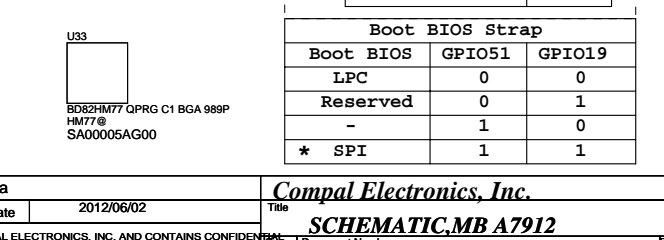
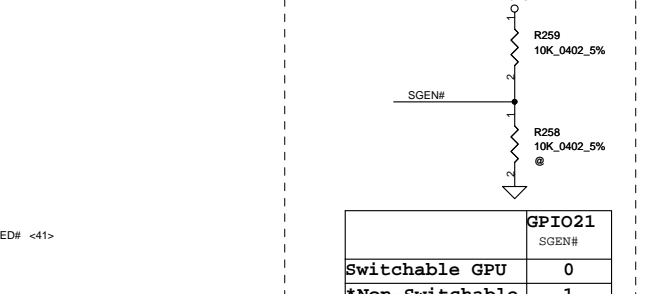
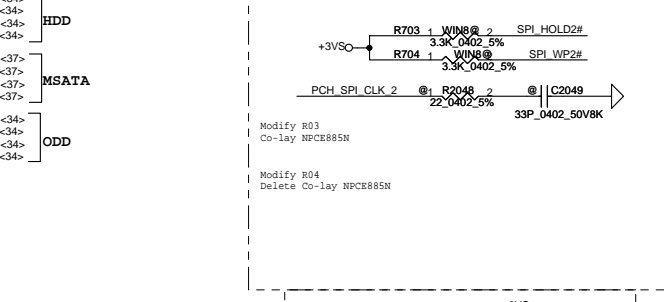
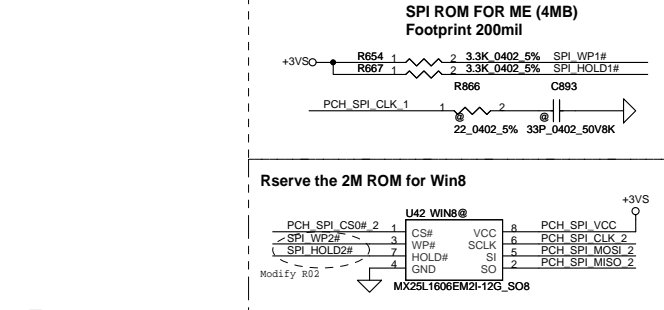
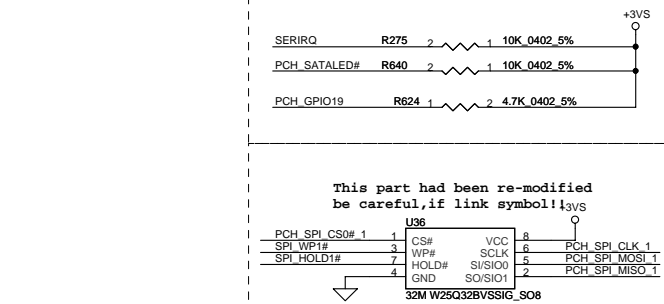
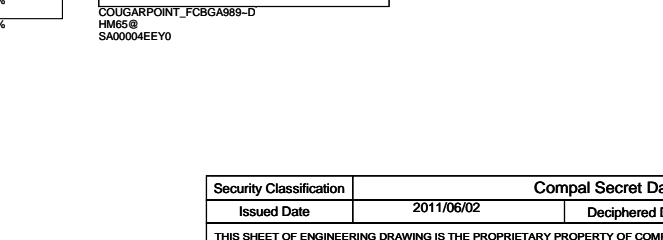
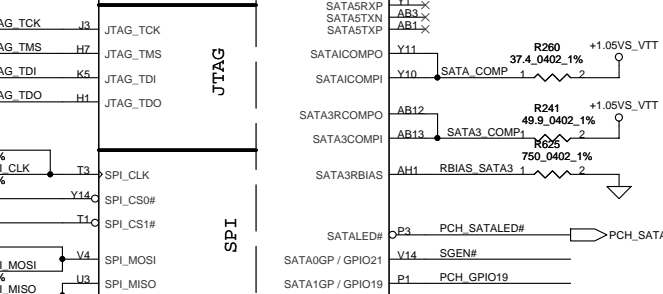
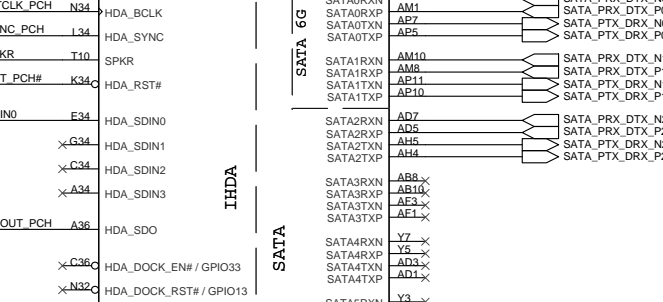
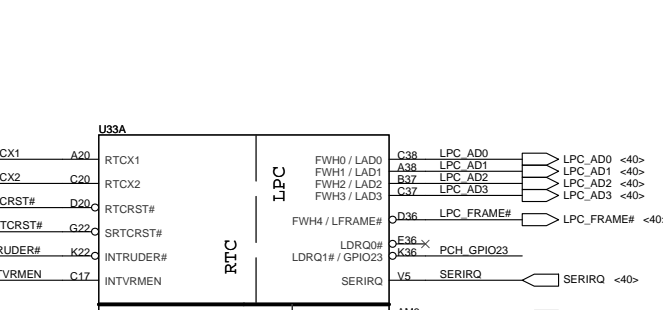
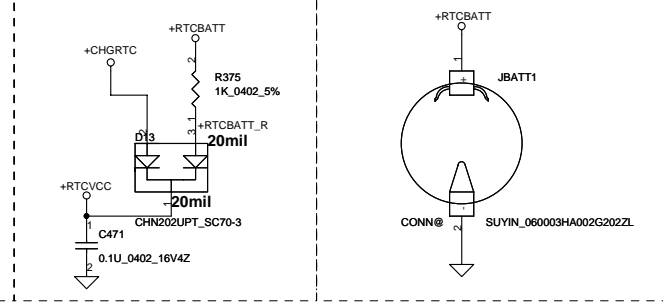
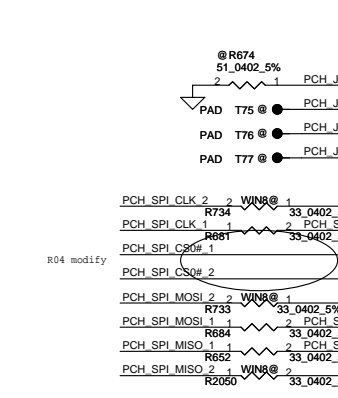
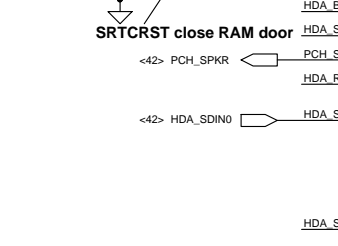
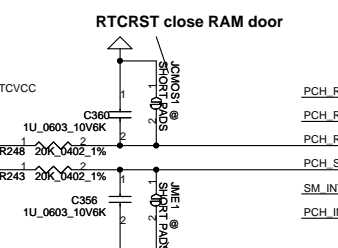
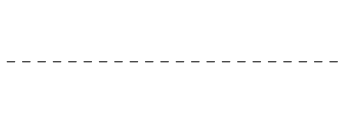
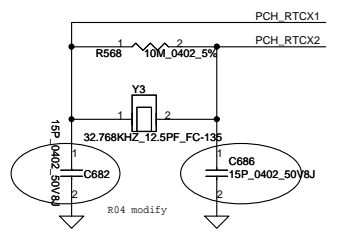
Layout Note:  
Place near JDIMM1





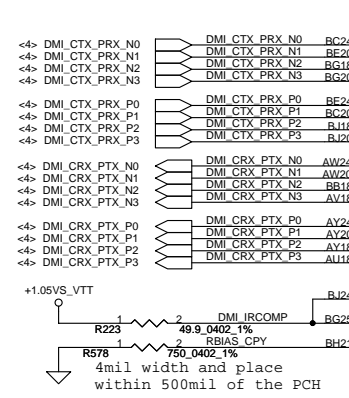
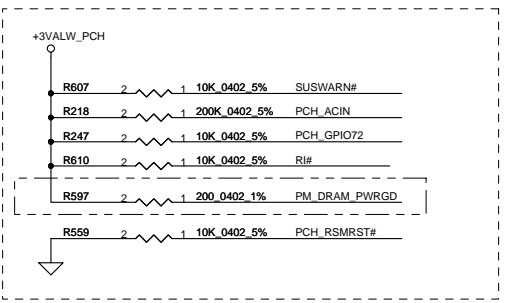


	GPIO23
USB2.0	0
USB3.0	1

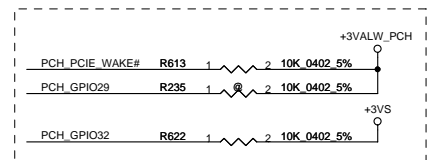
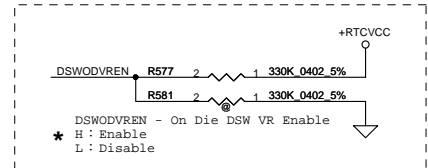
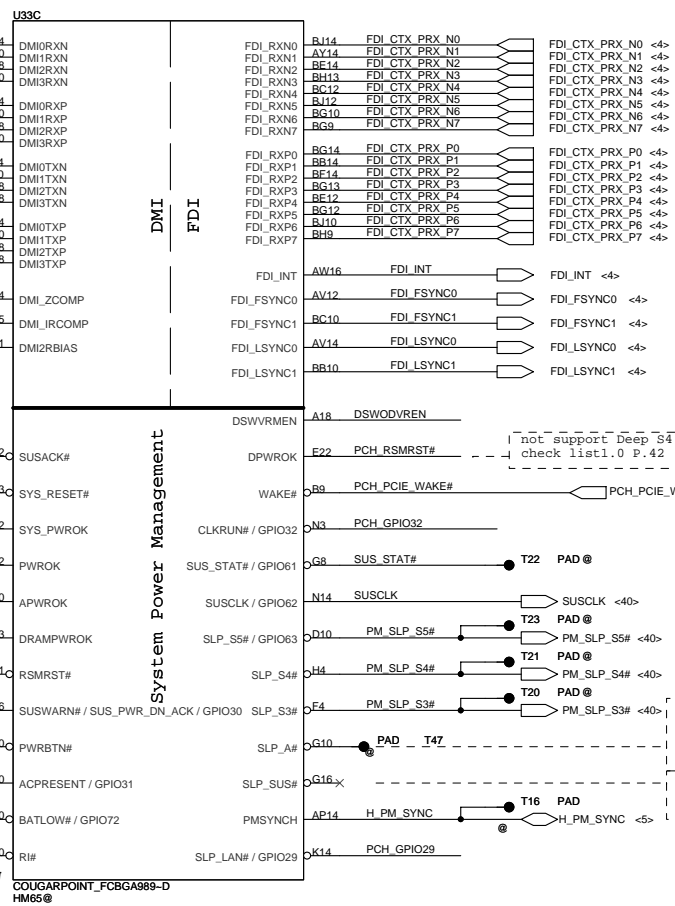
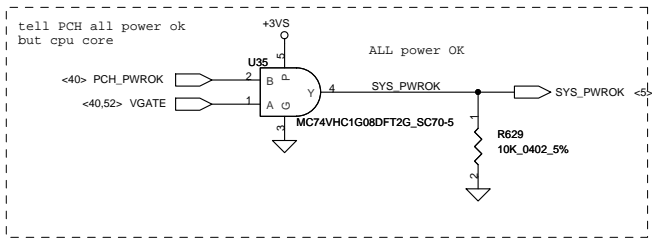
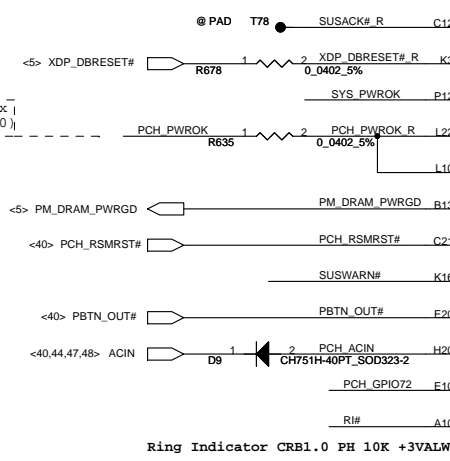


Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

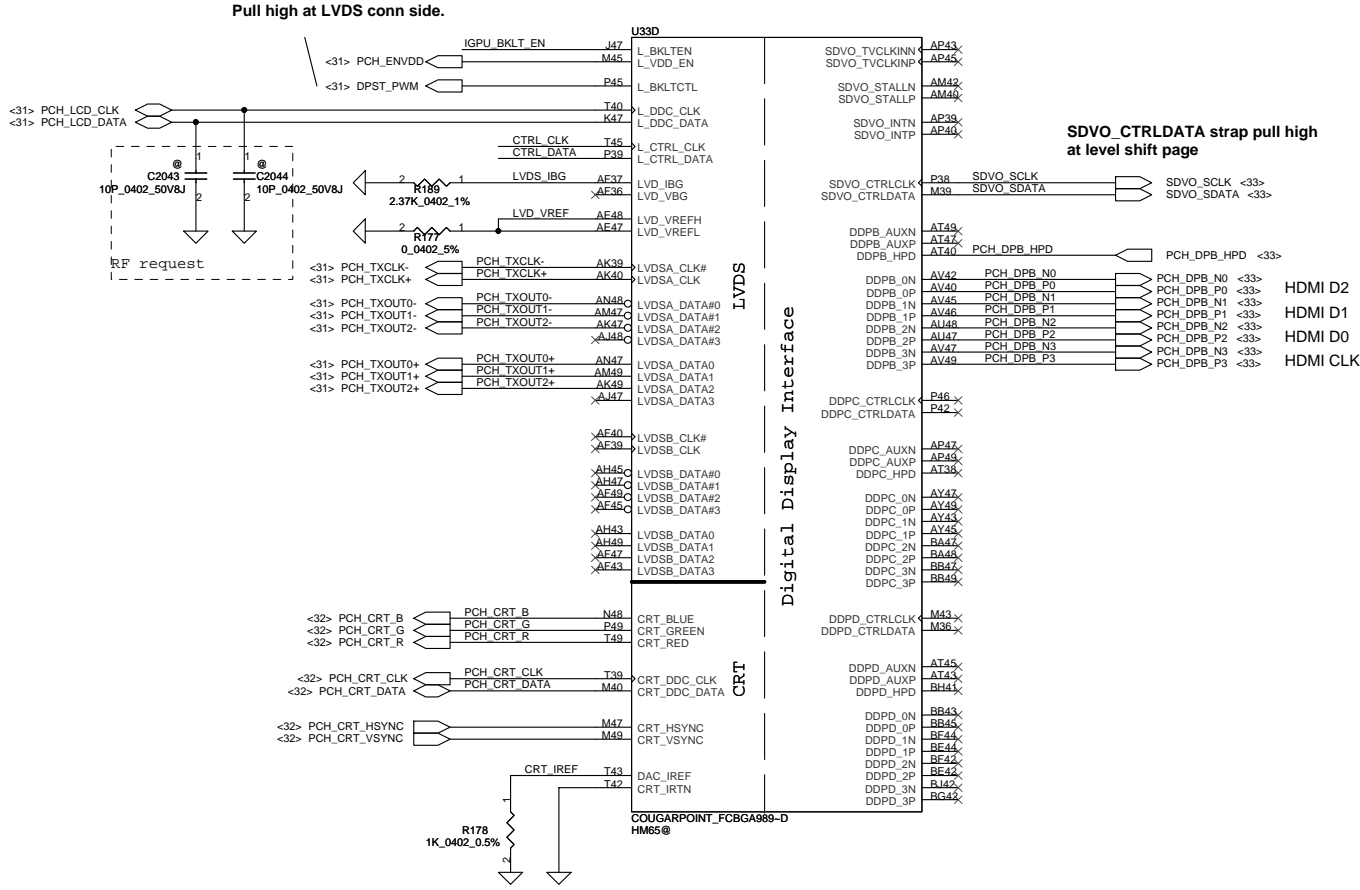
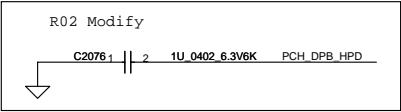
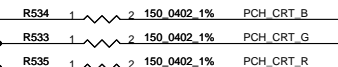
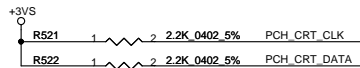
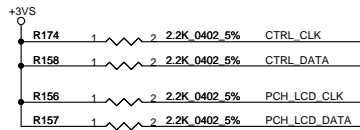
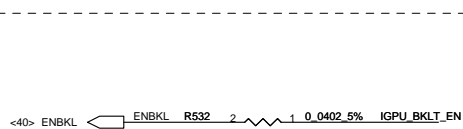




not support AMT APWROK can mux with PWROK (check list1.0 P.40)

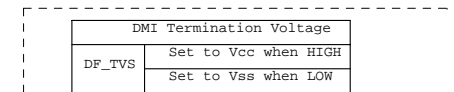
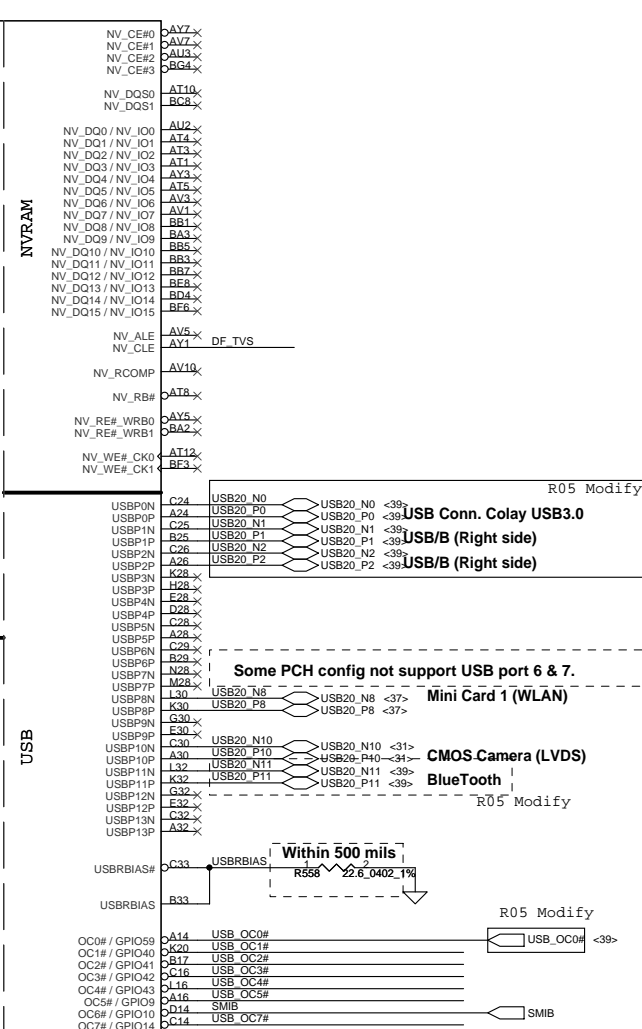
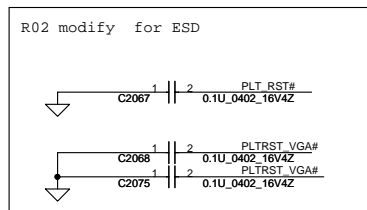
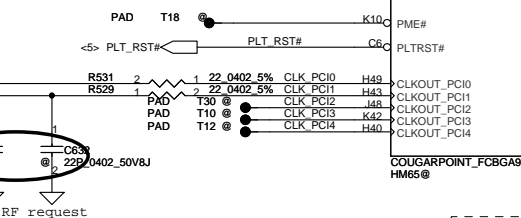
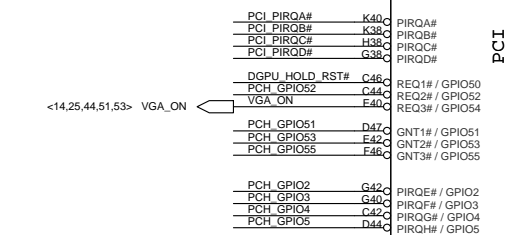
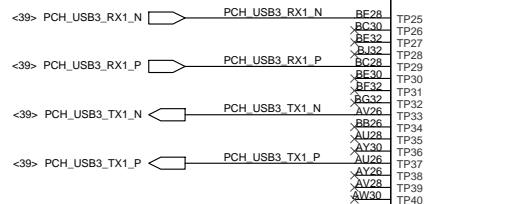
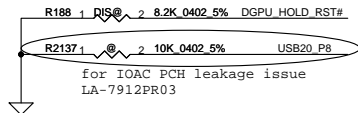


Can be left NC when IAMT is not support on the platform  
not support Deep S4,S5 can NC PCH EDS1.2 P.74

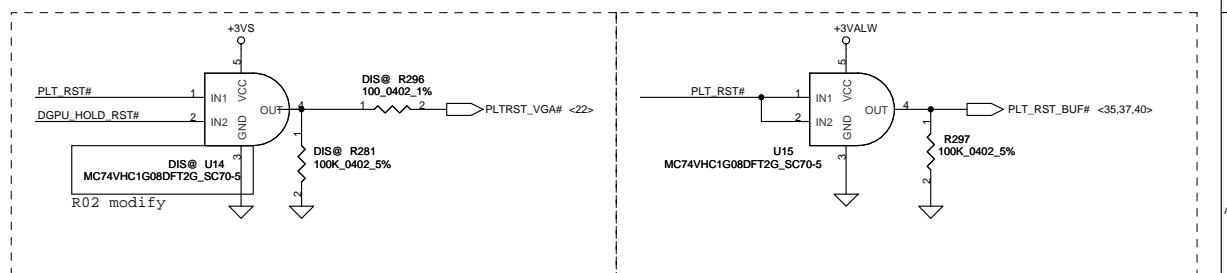
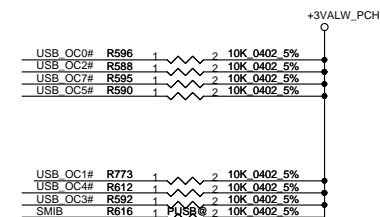
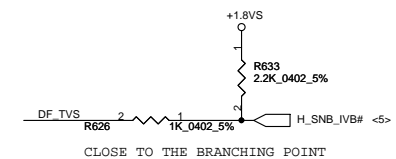


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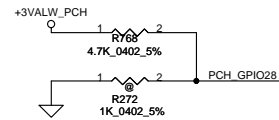


DG 1.2 CRB1.0 PH 2.2K series 1K

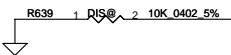
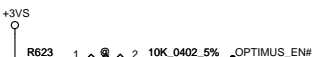
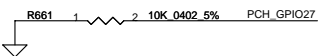


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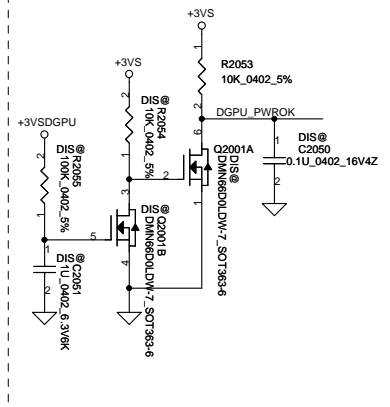
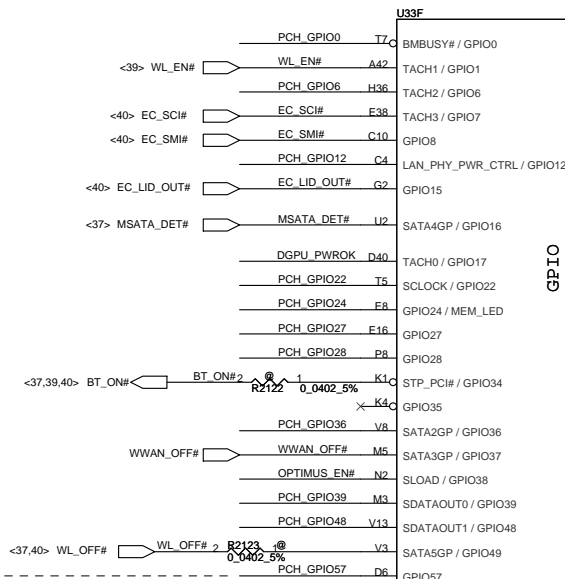
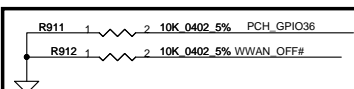
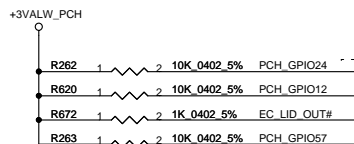
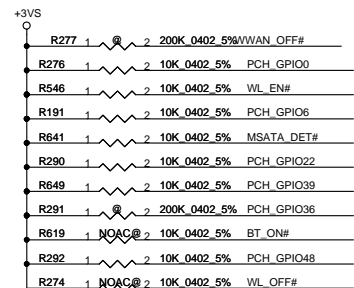
```
* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable
```



```
Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70
```



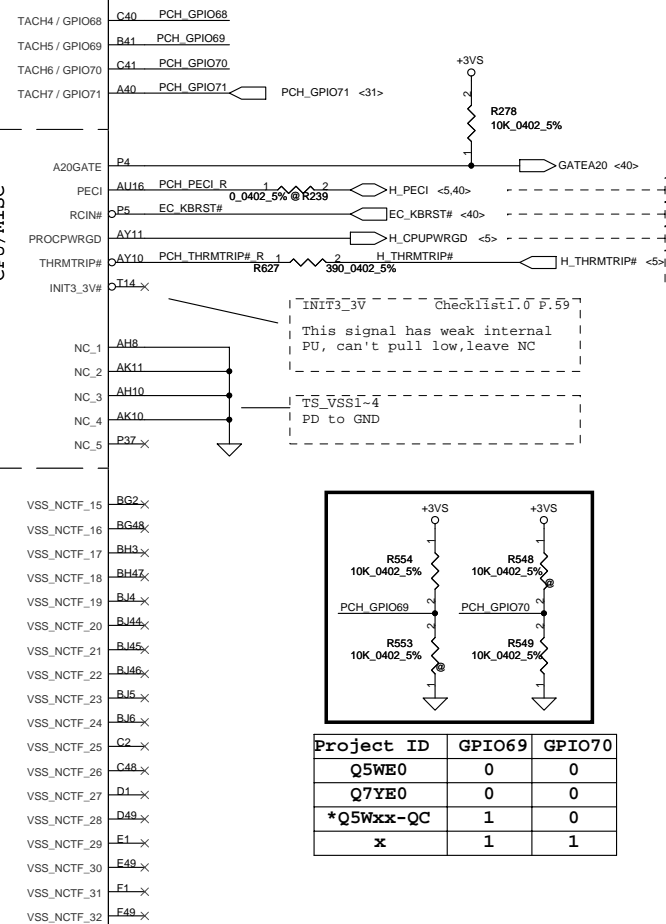
	<b>GPIO38</b> OPTIMUS_EN#
<b>OPTIMUS</b>	<b>0</b>
<b>DIS Only</b>	<b>1</b>



```
GPIO24 Unmultiplexed
NOTE: GPIO24 configuration
register bits are not cleared by
CF9h reset event.
```

CRB1.0 PH10K to +3VALW

```
GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When used as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check 11 page 47
```



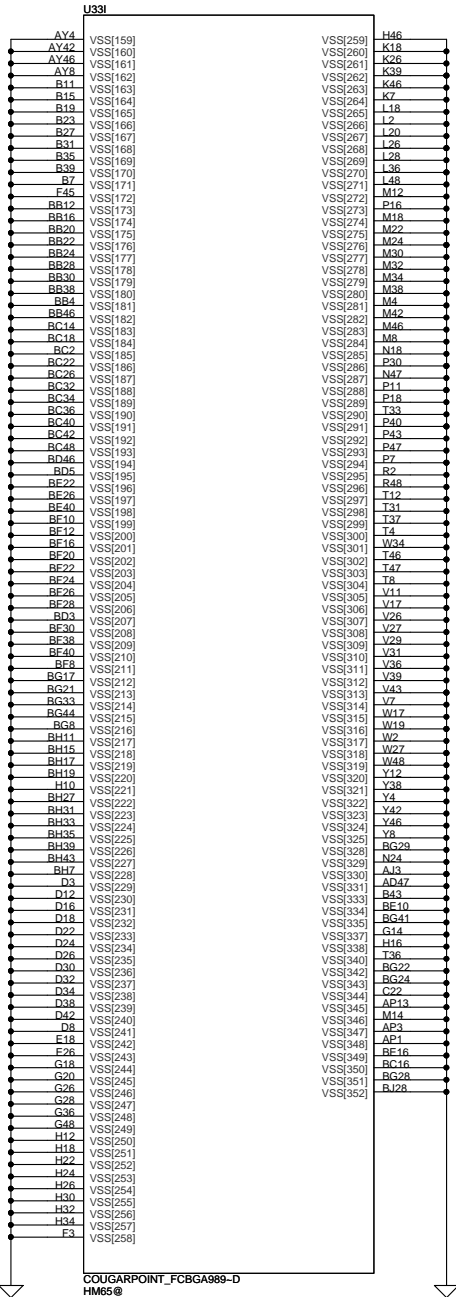
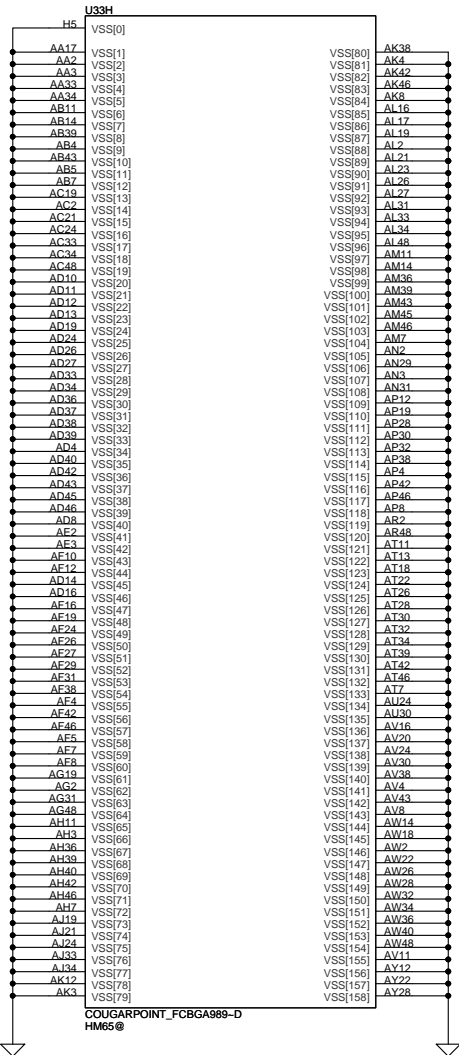
Project ID	GPIO69	GPIO7
Q5WE0	0	0
Q7YE0	0	0
*Q5Wxx-QC	1	0
x	1	1

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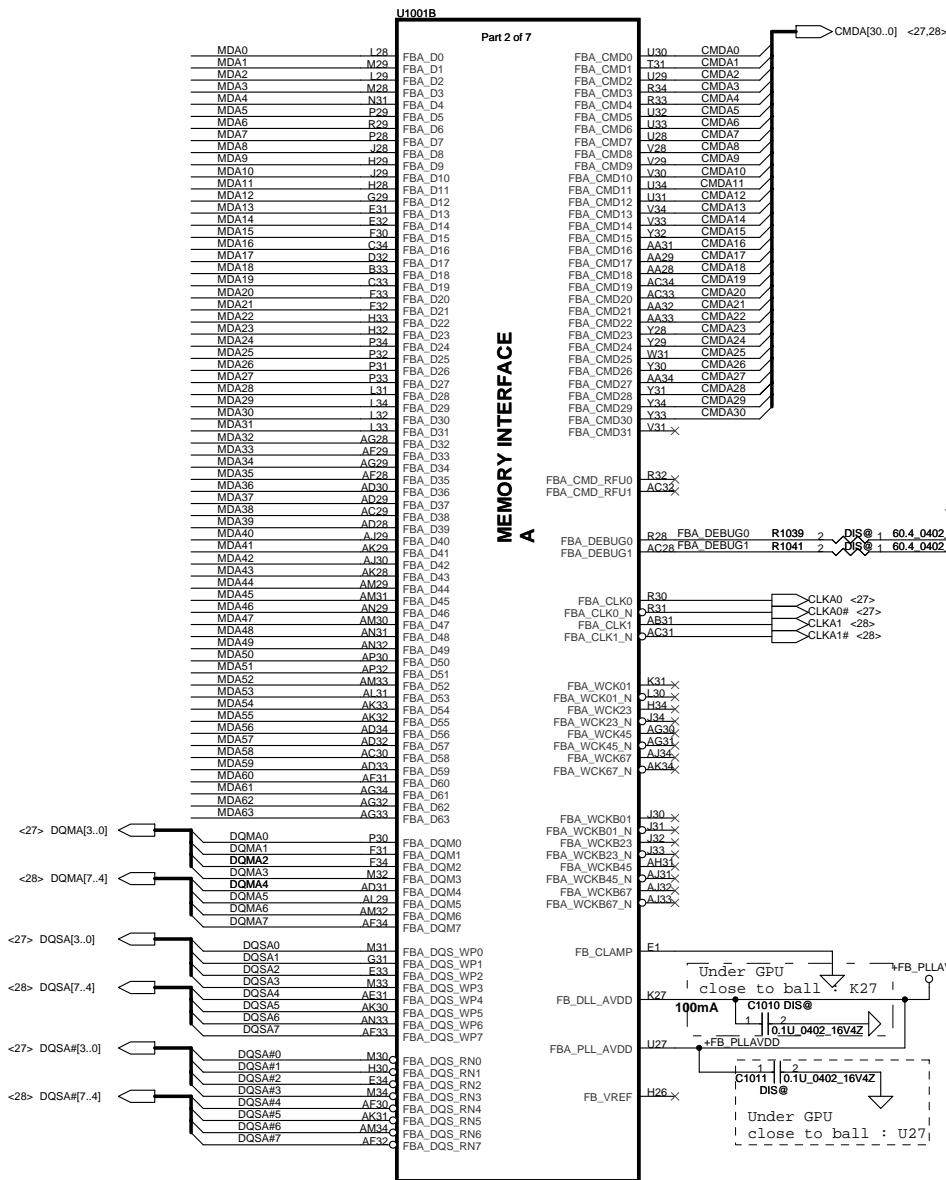
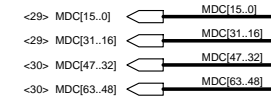
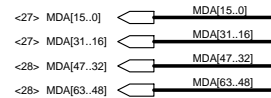


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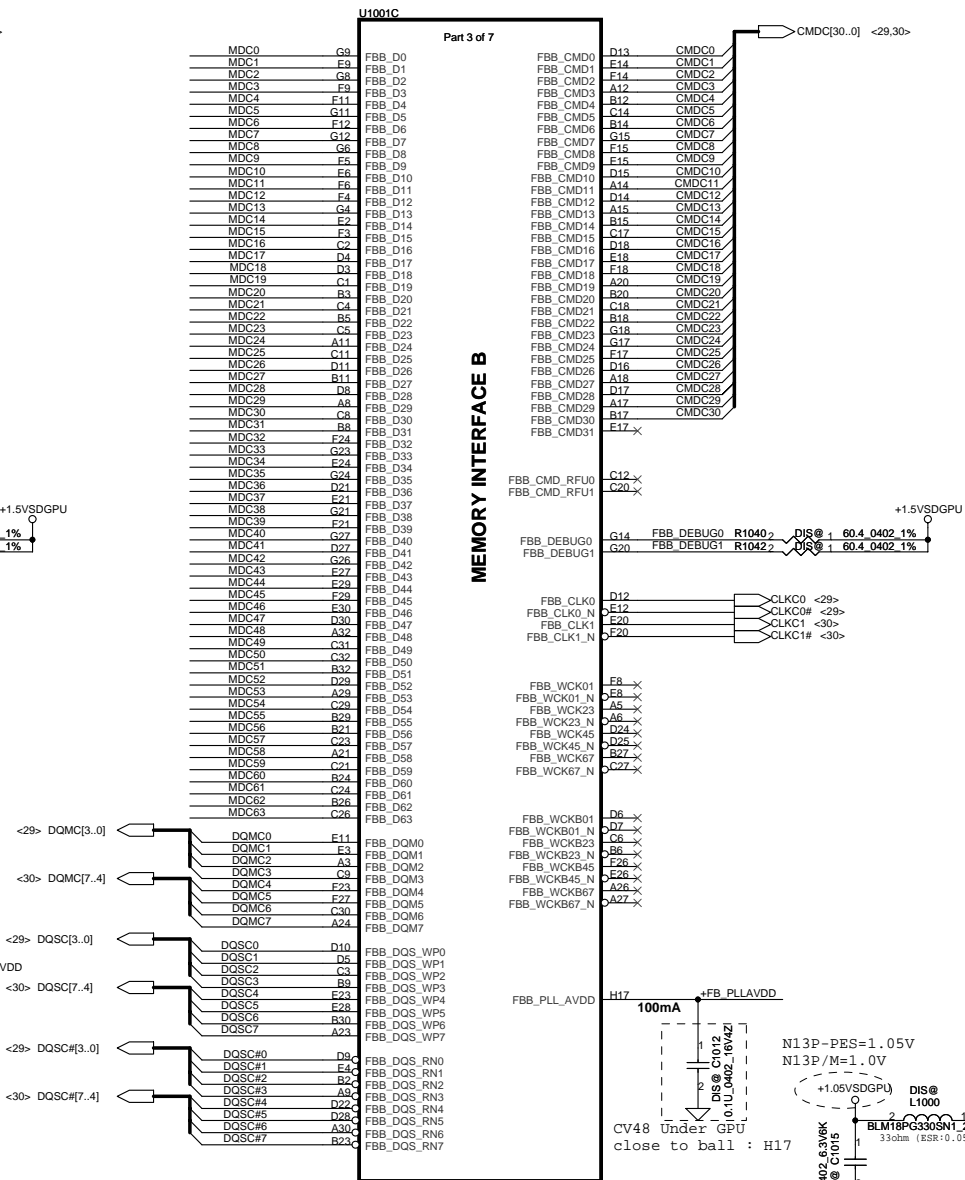




# VRAM Interface



N13P-PES-A1\_FCBGA908  
GF108@



N13P-PES-A1\_FCBGA908  
GF108@

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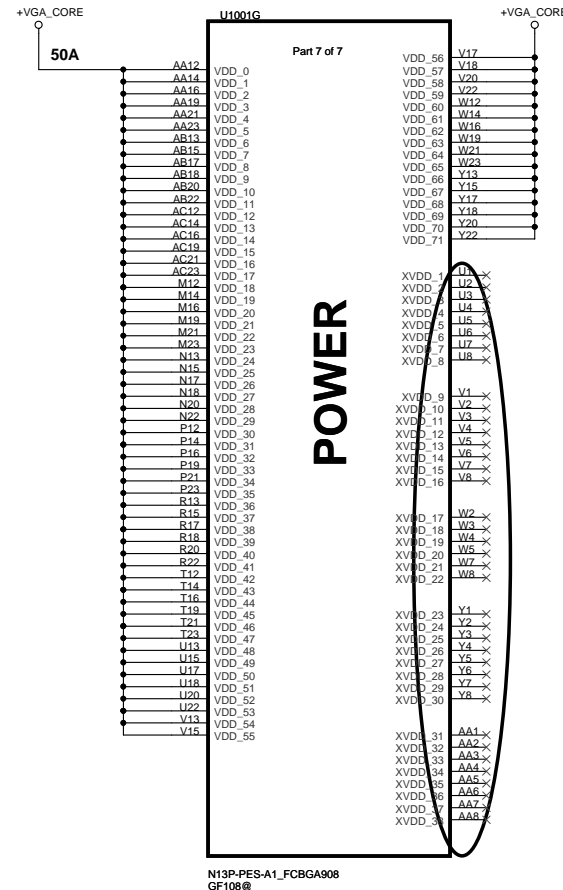
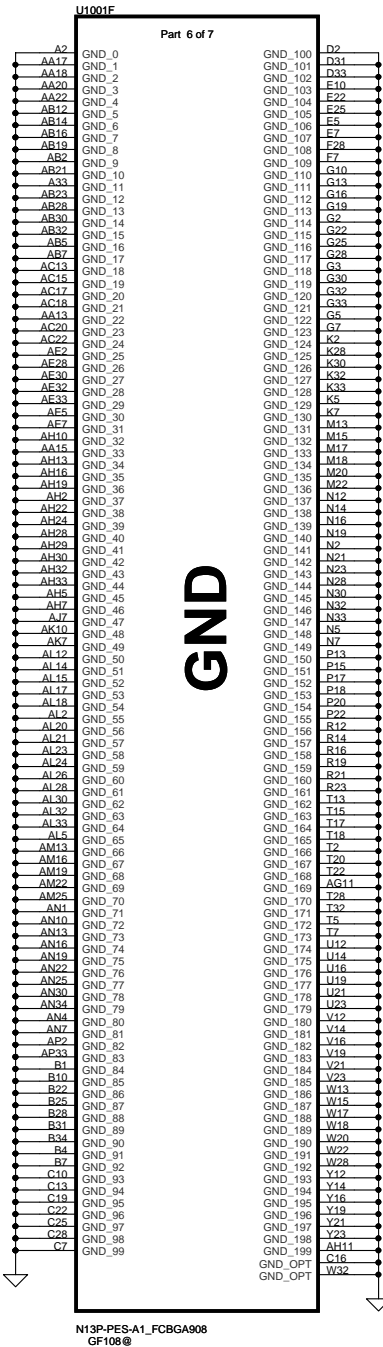


[illegible][illegible]

Figure 10: Power supply connections for the PEX. The diagram illustrates the power distribution network, showing connections for various power planes and signal traces. A dashed circle highlights a 2700 mA current requirement, with the text "total 2700mA Design guide p. 10". A 150 mA current requirement is also indicated. The layout includes connections for PEX\_I/OVDD\_0 through PEX\_I/OVDD\_13, PEX\_I/OVDD\_Q\_0 through PEX\_I/OVDD\_Q\_13, PEX\_PLL\_HVDD, PEX\_SVDD\_3V3, PEX\_PLLVDD, VDD33\_0 through VDD33\_3, IFPAB\_PLLVDD, IFPAB\_RST, IFPA\_I/OVDD, IFPA\_I/OVDD, IFPC\_PLLVDD, IFPC\_RST, IFPC\_I/OVDD, IFPD\_PLLVDD, IFPD\_RST, IFPD\_I/OVDD, IFPEF\_PLLVDD, IFPEF\_RST, IFPEF\_I/OVDD, and IFPEF\_I/OVDD. Various components like resistors (R1130, R1069, R1131, R1071, R1073, R1074, R1076, R1078, R1079, R1081, R1082, R1083) and capacitors (C1049, C1050) are shown with their values and tolerances. The diagram is labeled "Design guide p. 10".

Figure 10: Reference Schematic for the 300R@100MHz Design Guide. The schematic shows a multi-stage power supply regulation circuit. It starts with a 3VSDGPU input, followed by a series of capacitors (C1028, C1029, C1030, C1031, C1036) and diodes (D1002, D1003, D1004, D1005, D1006, D1007, D1008, D1009, D1010, D1011, D1012). The output is regulated to +1.05VSDGPU. The schematic is divided into sections: 'Near GPU', 'Under GPU', and 'Under GPU (one per pin)'. A callout shows the L1002 component, which is a 0.0603 5% GM@SD013000080 resistor.

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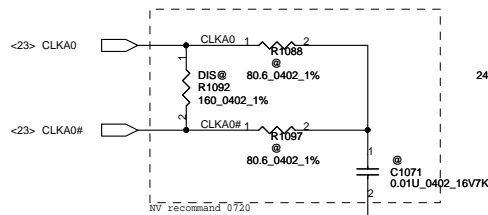
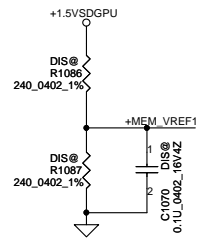
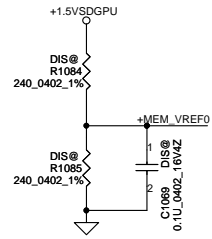


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# VRAM DDR3 chips (1GB)

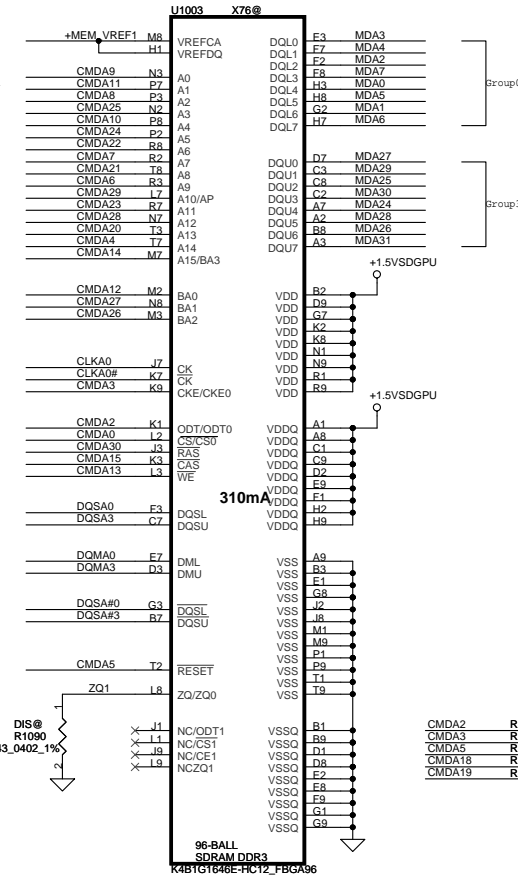
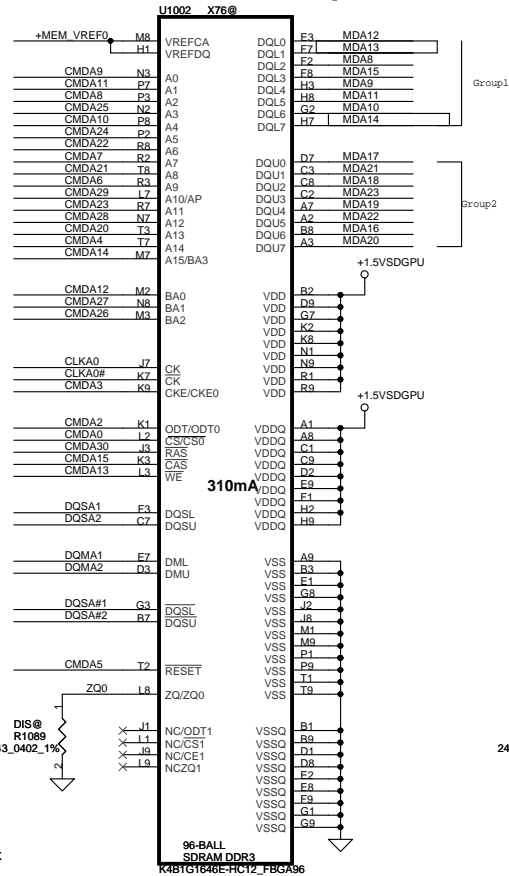
64Mx16 DDR3 \*8==>1GB  
128Mx16 DDR3 \*8==>2GB

<23,28> DQSA[7..0] DQSA[7..0]  
<23,28> DQSA# [7..0] DQSA# [7..0]  
<23,28> DQMA[7..0] DQMA[7..0]  
<23,28> MDA[63..0] MDA[63..0]  
<23,28> CMDA[30..0] CMDA[30..0]



R04 modify for EMI

R02 modify  
Swap MDA13 and MDA14



CMDA2 R1091 DIS@ 2 10K 0402 5%  
CMDA3 R1092 DIS@ 2 10K 0402 5%  
CMDA5 R1094 DIS@ 2 10K 0402 5%  
CMDA18 R1095 DIS@ 2 10K 0402 5%  
CMDA19 R1096 DIS@ 2 10K 0402 5%

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CAS*	No Termination

Hynix : SA00003YO20 (S IC D3 128M16 H5TQ2G63BFR-11C FBGA)  
Hynix : SA000041S40 (S IC D3 64Mx16 H5TQ1G63DFR-11C FBGA )

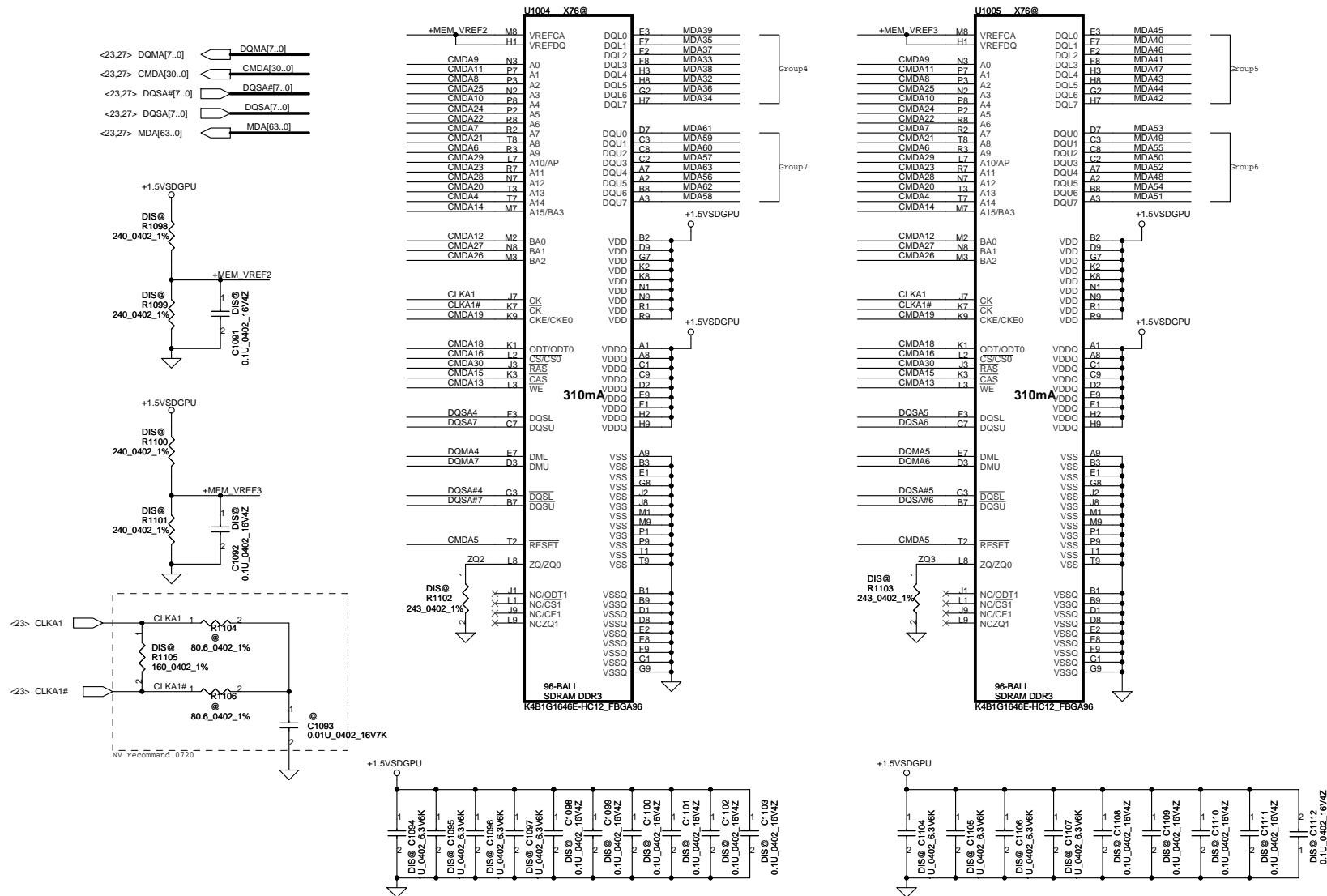
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		ODT_H
CMD18		CKE_H
CMD19		
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available	LOW	HIGH

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Hynix : SA00003YO20 (S IC D3 128M16 H5TQ2G63BFR-11C FBGA) Hynix : SA000041S40 (S IC D3 64Mx16 H5TQ1G63DFR-11C FBGA )				C
Date: Friday, February 10, 2012				Sheet 27 of 63

# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

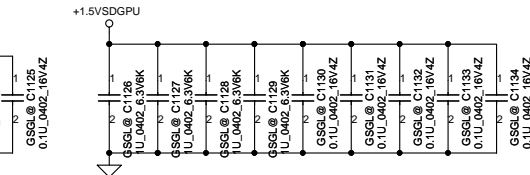
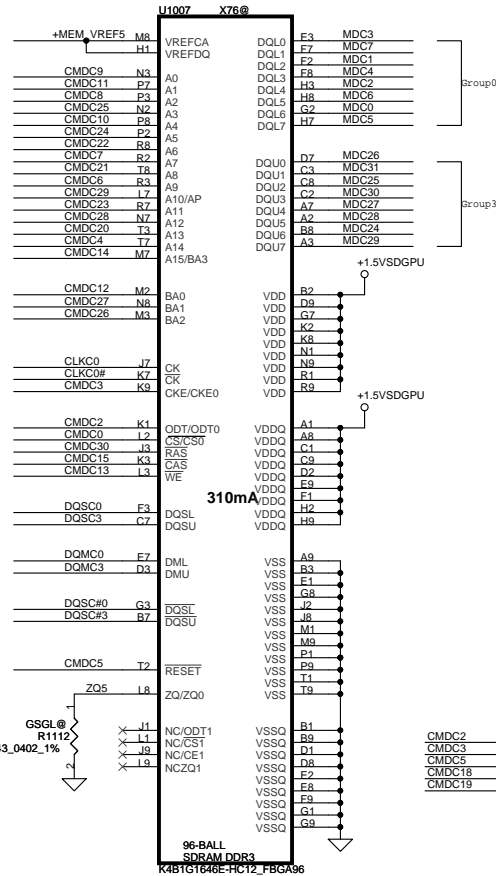
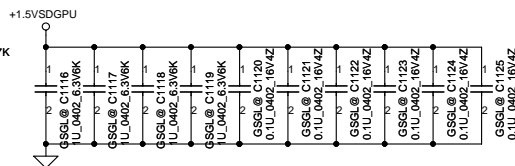
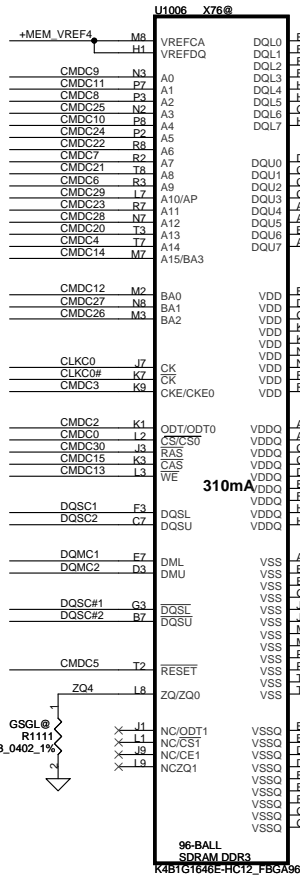
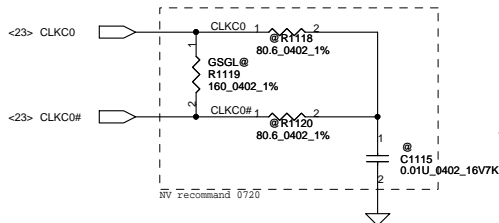
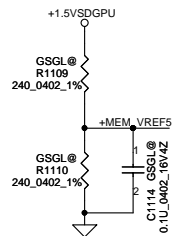
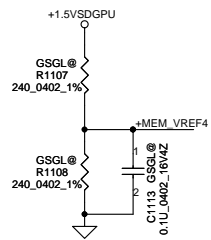
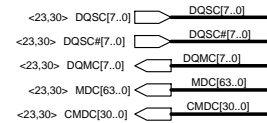
128Mx16 DDR3 \*8==>2GB



# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

128Mx16 DDR3 \*8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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				Date	Friday, February 10, 2012
				Sheet	29 of 63

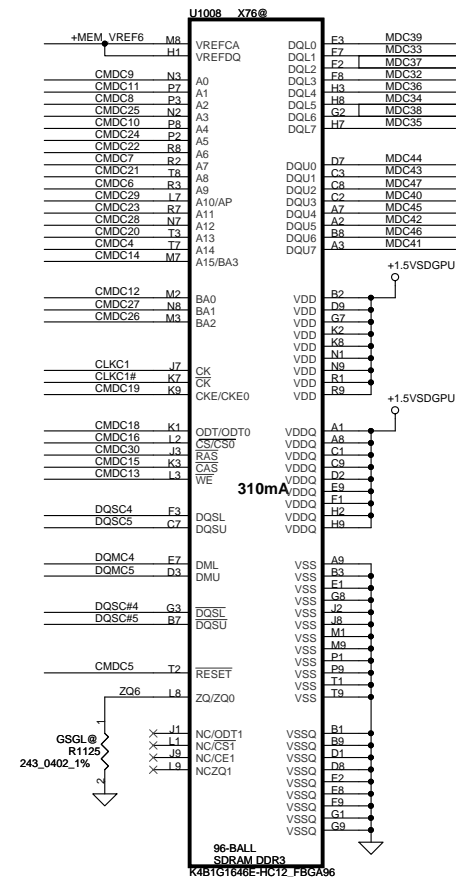
# VRAM DDR3 chips (1GB)

64Mx16 DDR3 \*8==>1GB

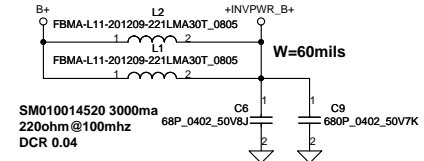
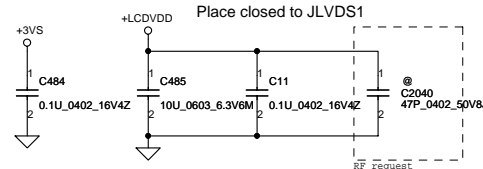
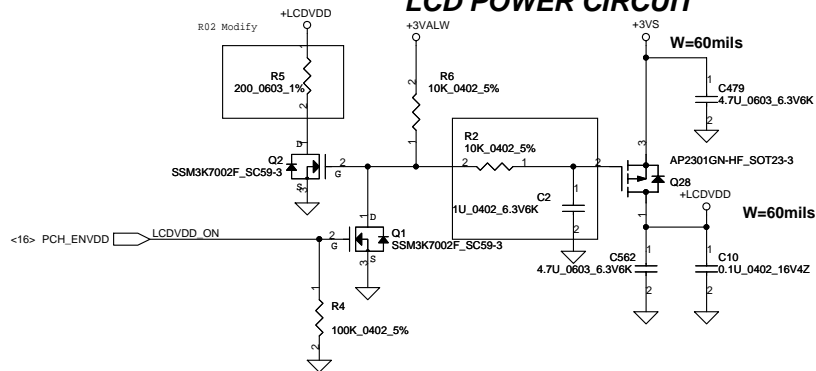
128Mx16 DDR3 \*8==>2GB

<23,29> DQMC[7..0] ← DQMC[7..0]  
<23,29> CMD[30..0] ← CMD[30..0]  
<23,29> DQSC[7..0] ← DQSC[7..0]  
<23,29> DQSC[7..0] ← DQSC[7..0]  
<23,29> MDC[63..0] ← MDC[63..0]

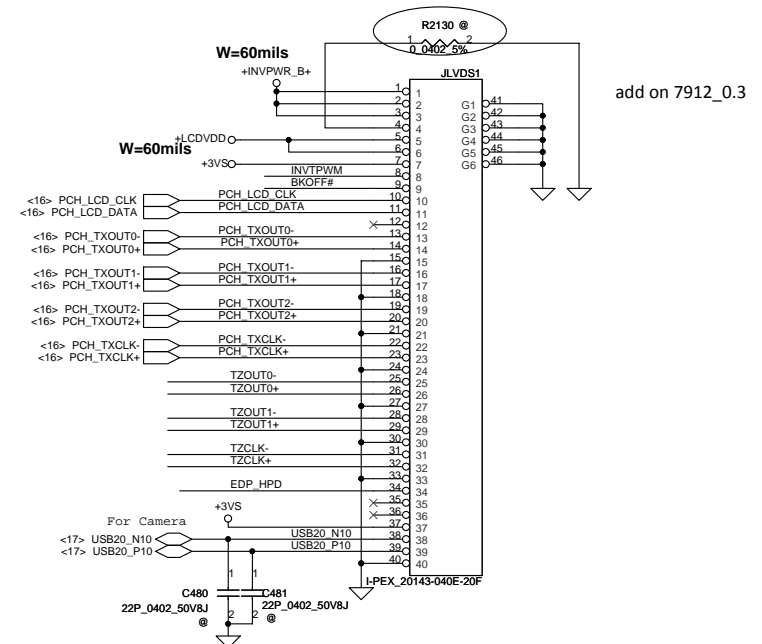
R02 modify  
Swap MDC37 and MDC38



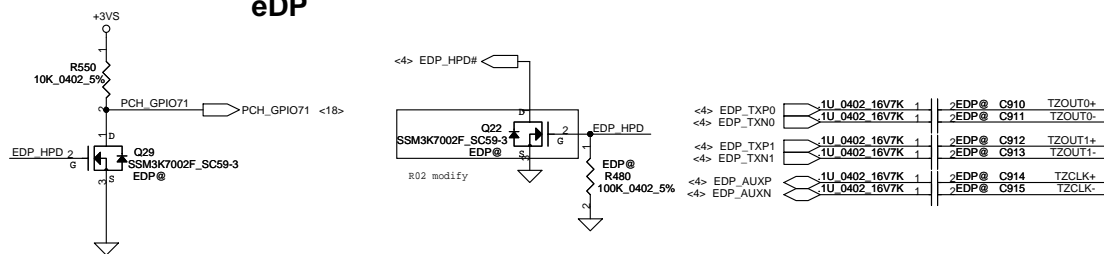
## LCD POWER CIRCUIT



## LCD/LED PANEL Conn.



## eDP

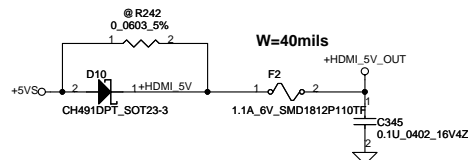


	<b>GPIO71</b>
	PCH_GPIO71
<b>eDP</b>	0
<b>LVDS</b>	1

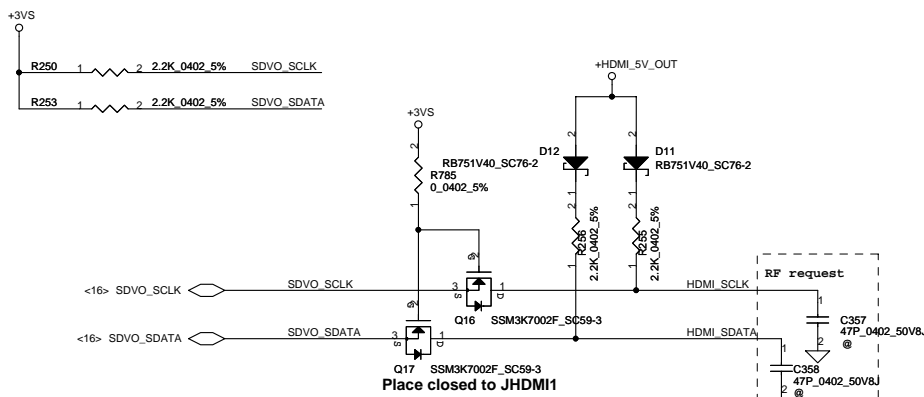
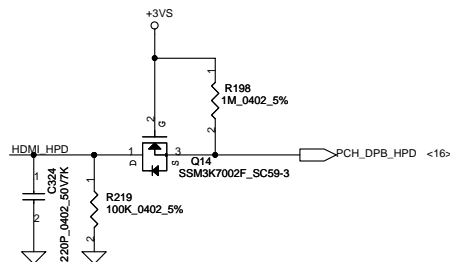
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Date:		Friday, February 10, 2012		Sheet		31	of	63



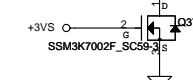
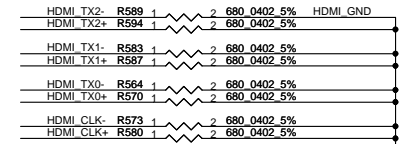
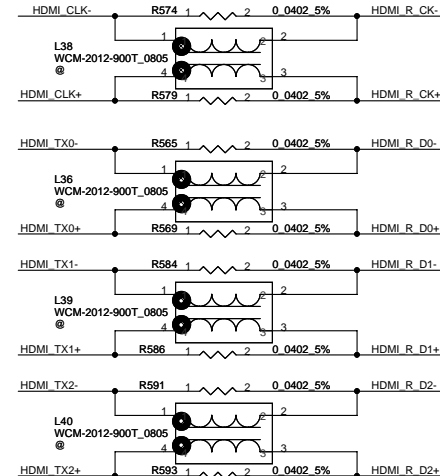




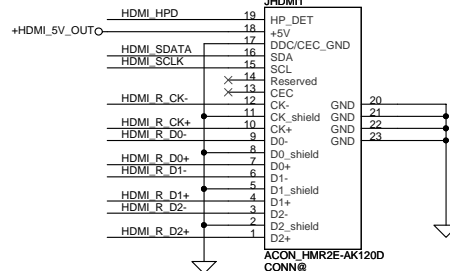
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<16> PCH_DPB_P0	C281	2	1	.1U_0402_16V7K	HDMI TX2+
<16> PCH_DPB_N1	C283	2	1	.1U_0402_16V7K	HDMI TX1-
<16> PCH_DPB_P1	C282	2	1	.1U_0402_16V7K	HDMI TX1+
<16> PCH_DPB_N2	C287	2	1	.1U_0402_16V7K	HDMI TX0-
<16> PCH_DPB_P2	C286	2	1	.1U_0402_16V7K	HDMI TX0+
<16> PCH_DPB_N3	C285	2	1	.1U_0402_16V7K	HDMI CLK-
<16> PCH_DPB_P3	C284	2	1	.1U_0402_16V7K	HDMI CLK+



SM070001310 400ma 90ohm@100mhz DCR 0.3

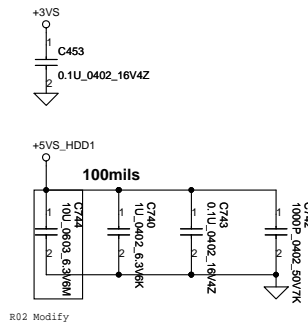
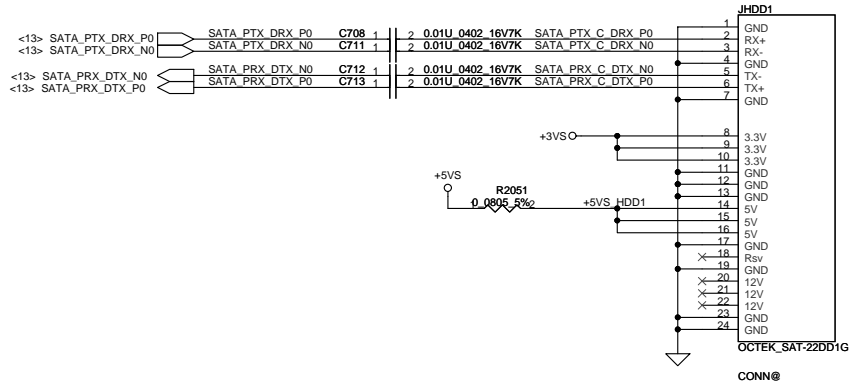


# HDMI connector

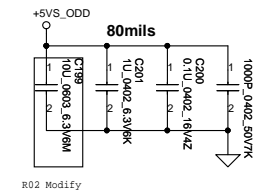
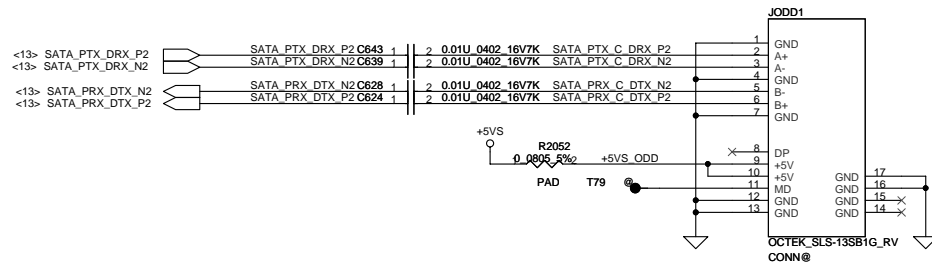


## SATA HDD1 Conn.

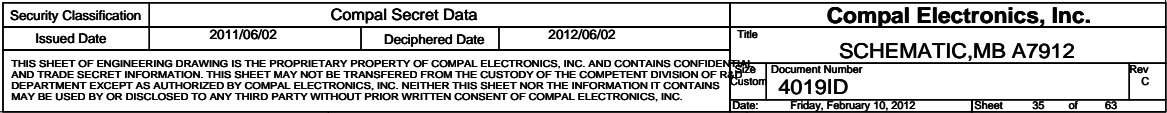
CL 4.0 mm

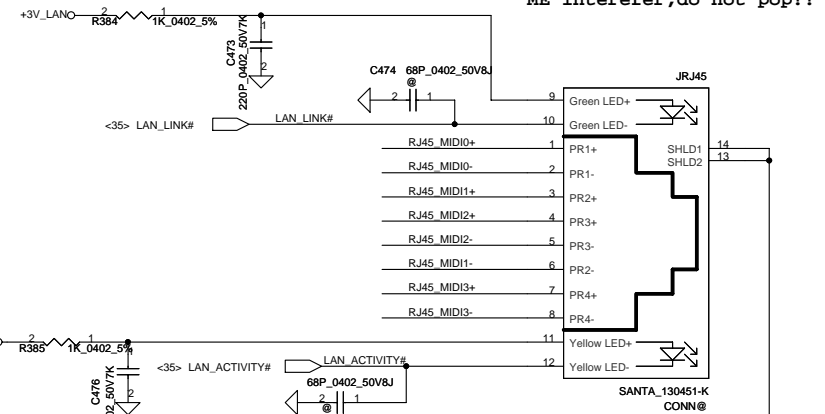


## SATA ODD Conn.

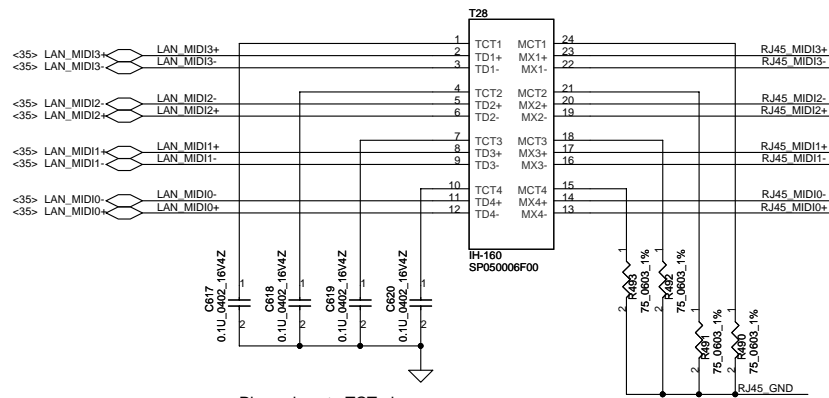


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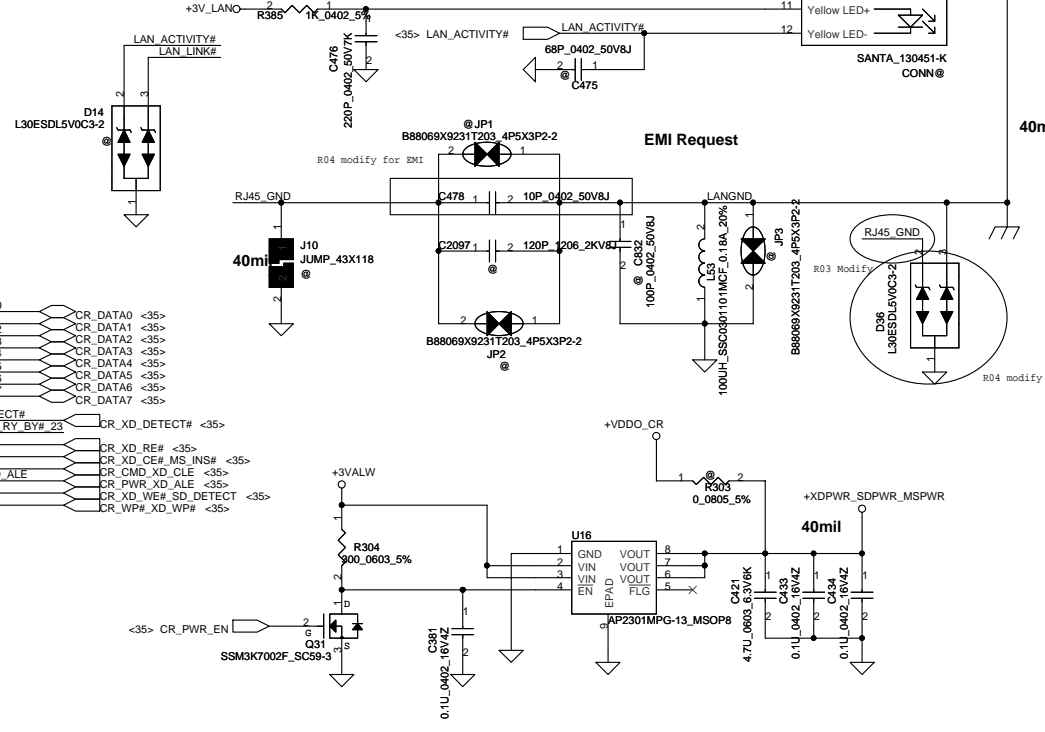




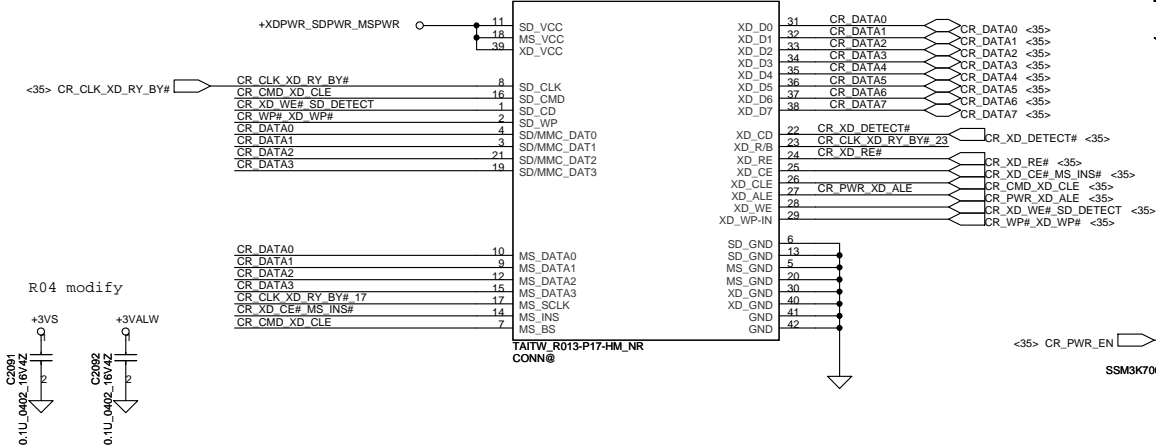
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TIMAG:S X'FORM\_ IH-160 LAN , SP050006F00



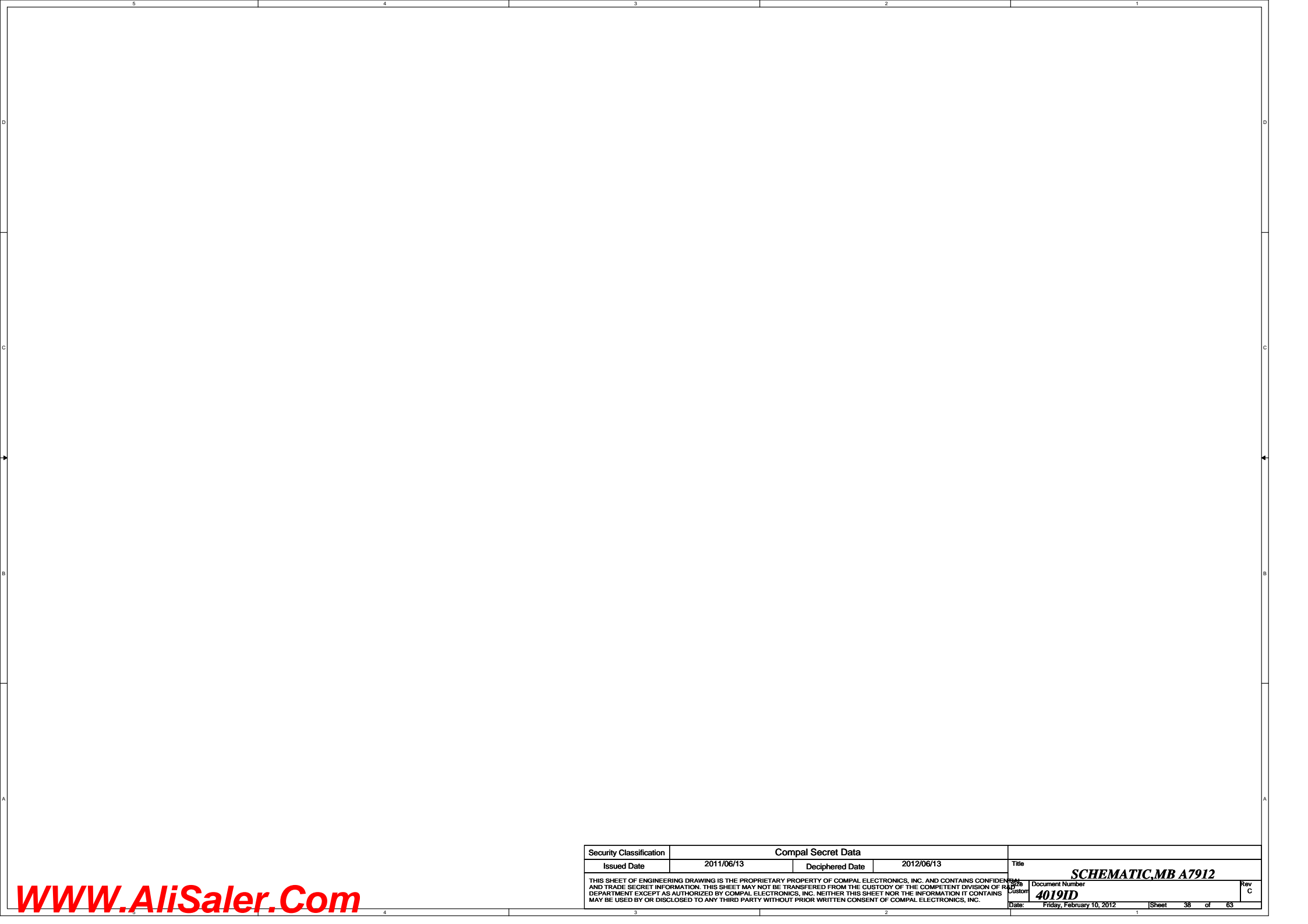
TAITW\_R013-P17-HM\_NR  
CONN@



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				Custom	4019ID	
				Date:	Friday, February 10, 2012	Sheet 36 of 63

A	B	C	D	E
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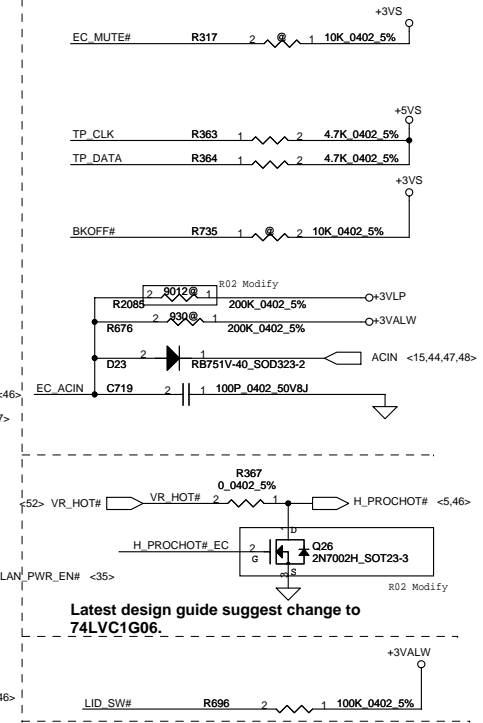
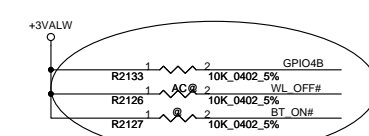
2



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Date: Friday, February 10, 2012				Sheet 38 of 63	Document Number 40191D





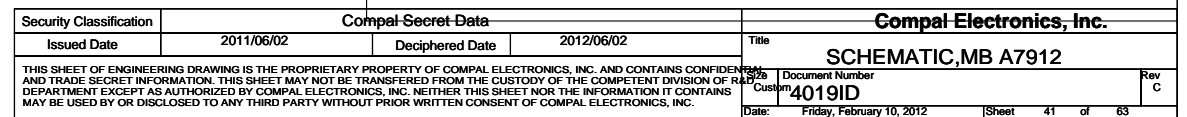
LID SW# R696 2 1 100K 0402 5% +3VALW

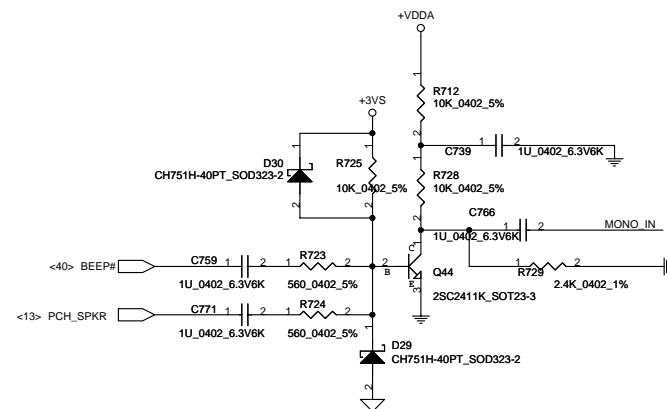
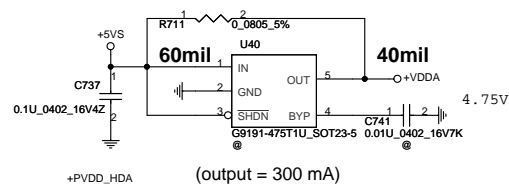
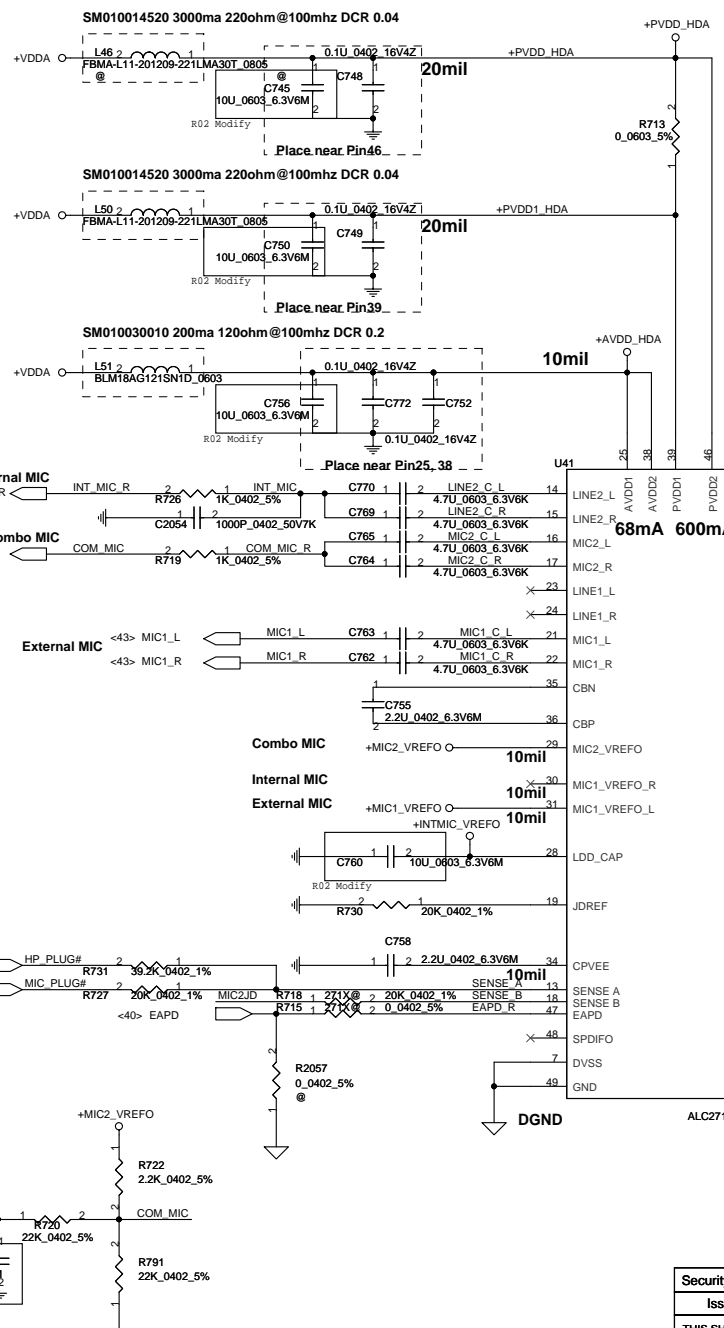
R03 Modify            R04 Modify  
Co\_lay NPCE885N Delete Co\_lay NPCE885

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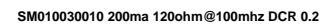
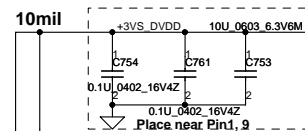


Test Only  
Bottom Side

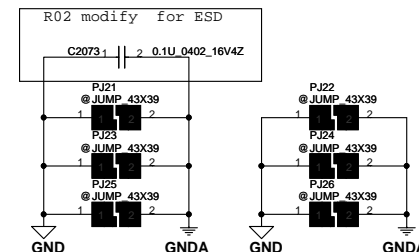
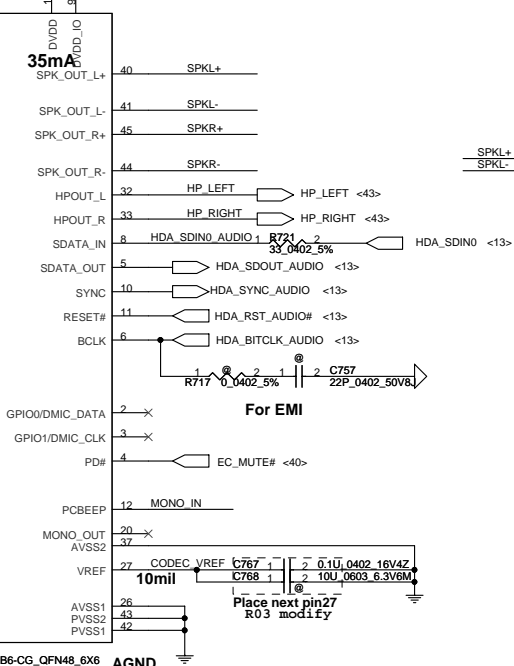
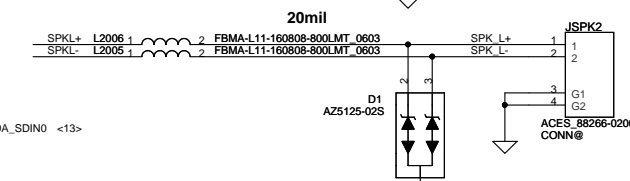
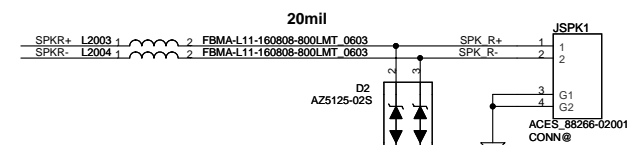




### HD Audio Codec



**Int. Speaker Conn.**



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				Date:	Friday, February 10, 2012
				Sheet	42 of 63

Singatron 2SJ2326  
DC021007151

Headphone Out

SINGA\_2SJ2326-001111  
CONN@

MIC JACK

SINGA\_2SJ-A960-C01  
CONN@

Int. MIC

ACES\_85266-02001  
CONN@

D16  
AZ5125-02S

FAN1 Conn

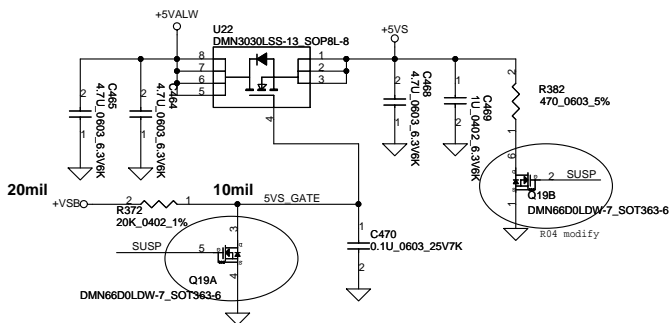
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FAN Stand-Off

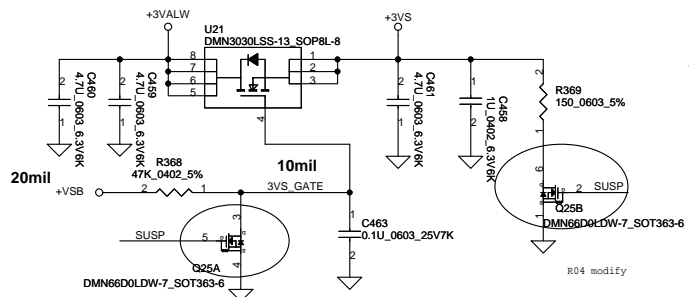
JUSB3 Stand-Off

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Customer				Document Number	4019ID
Date: Friday, February 10, 2012				Sheet	43 of 63

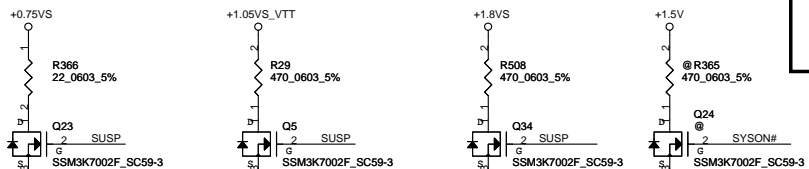
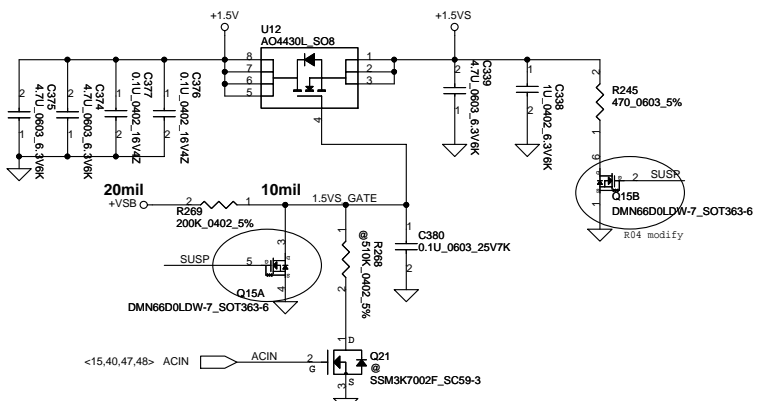
**+5VALW TO +5VS**



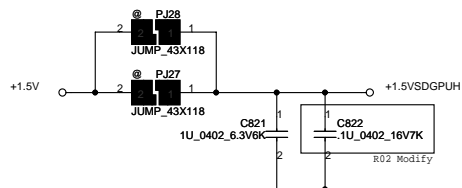
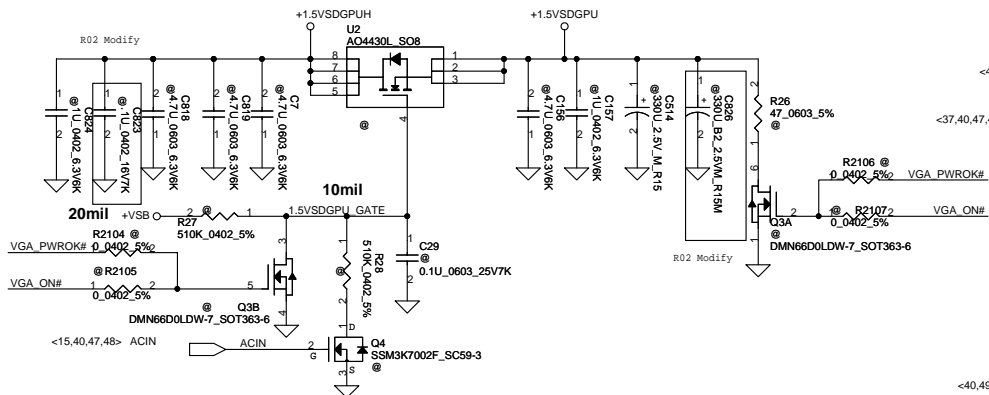
**+3VALW TO +3VS**



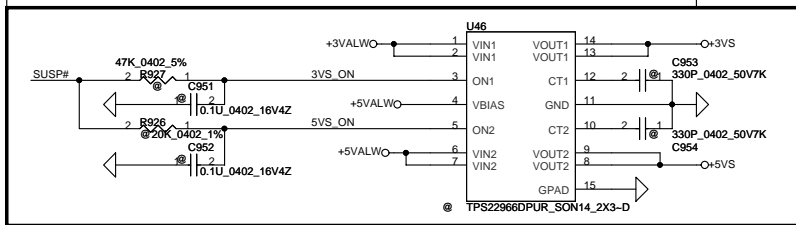
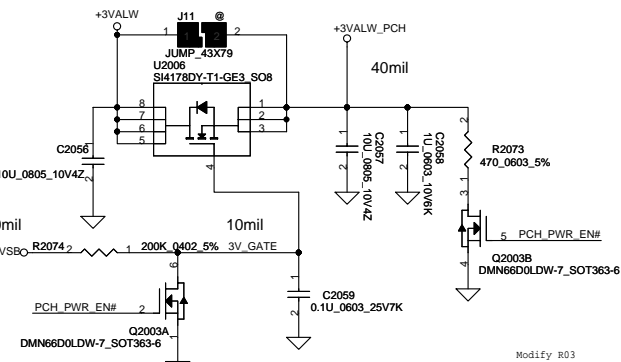
**+1.5V to +1.5VS**



**+1.5VSDGPUH to +1.5VSDGPU for GPU**



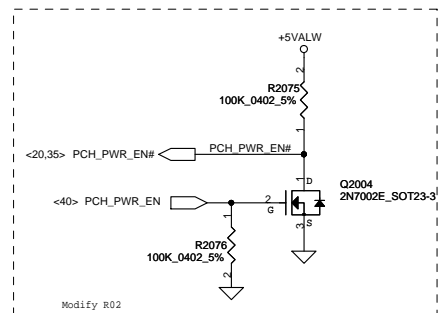
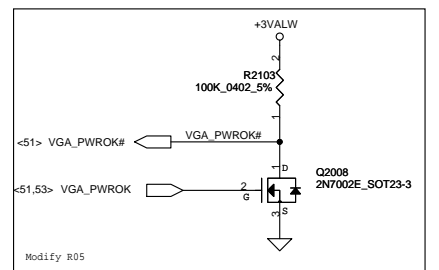
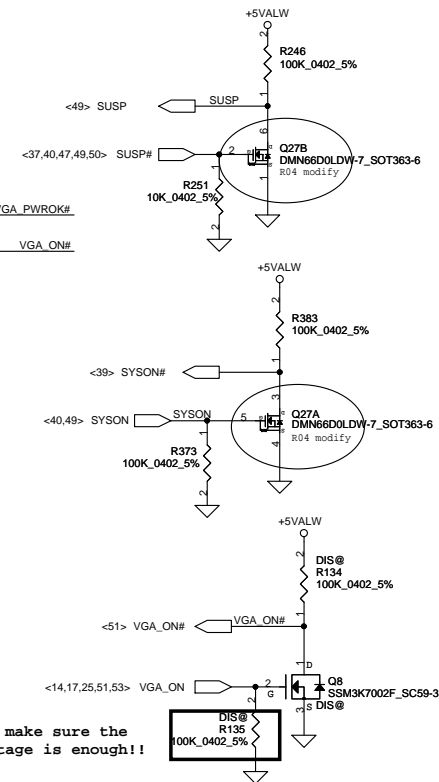
+3VALW TO +3VALW(PCH AUX Power)



Reserved

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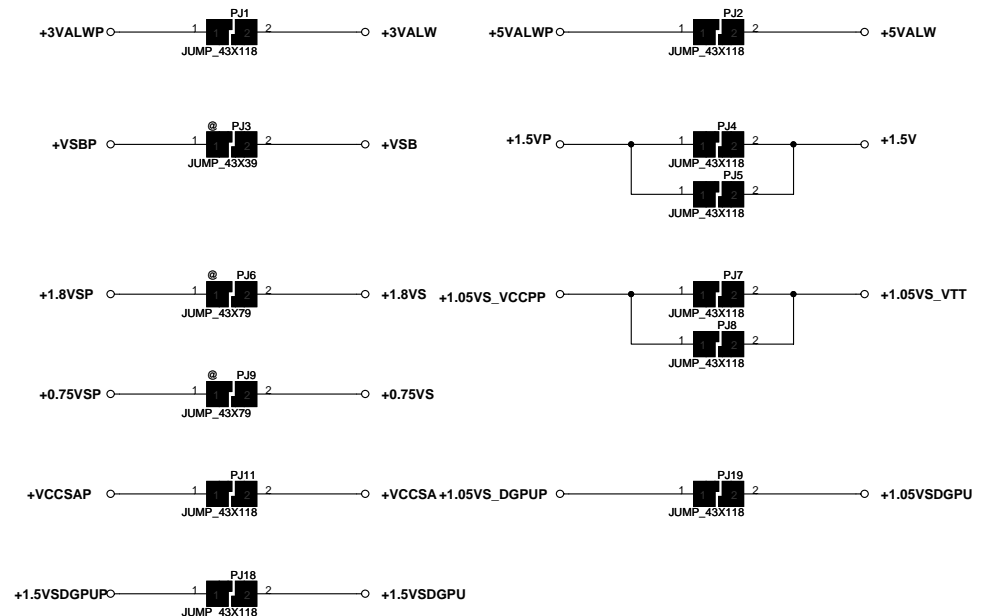
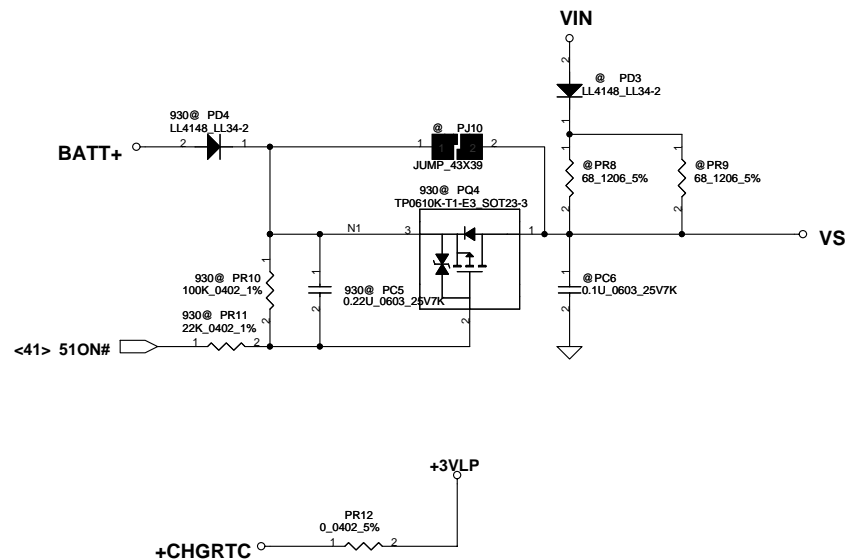
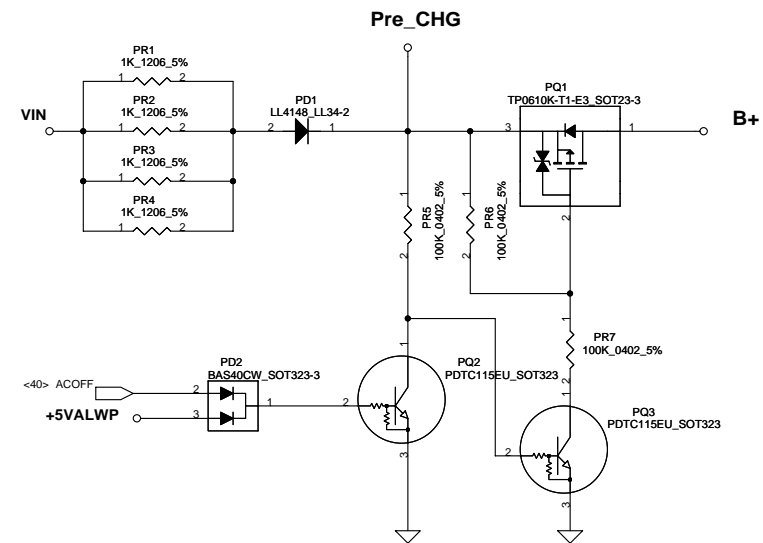
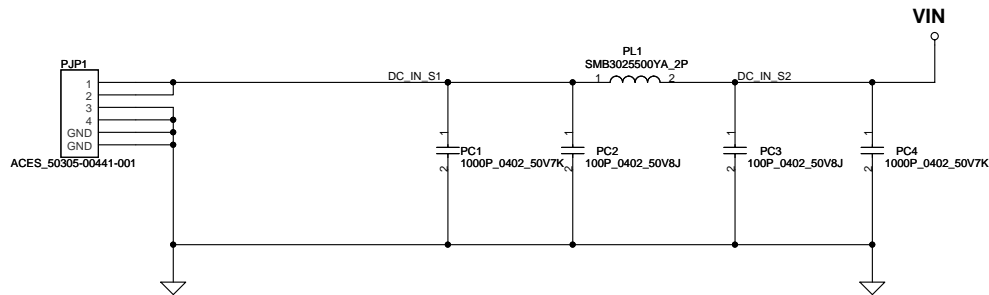
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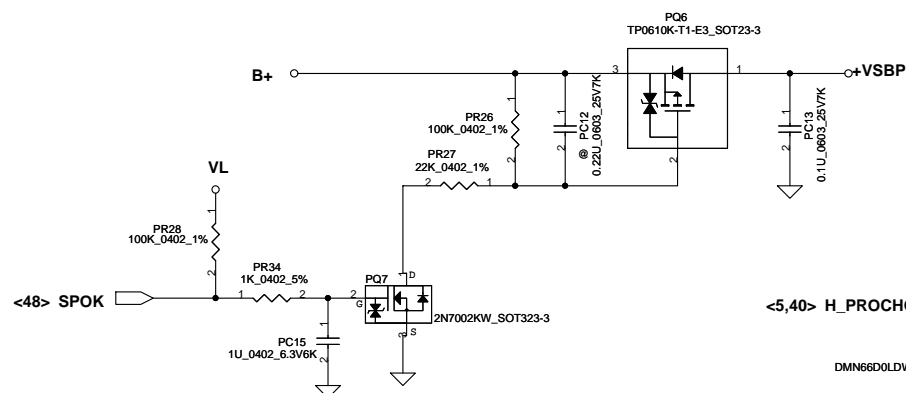
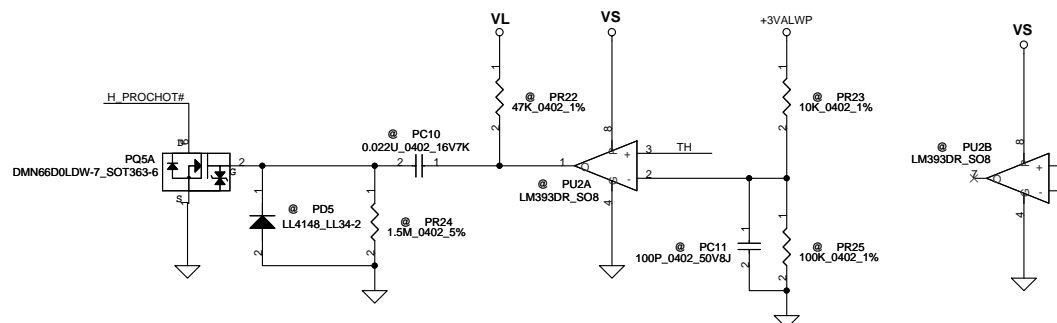
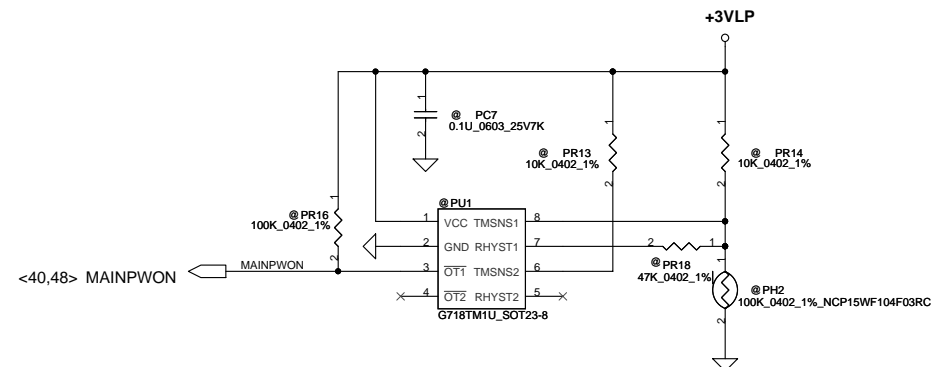
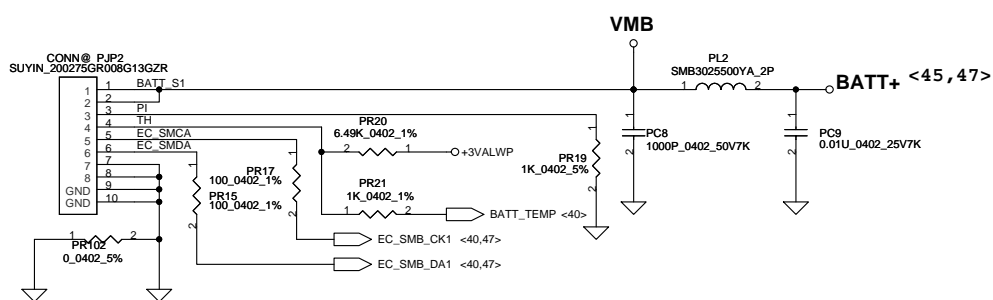
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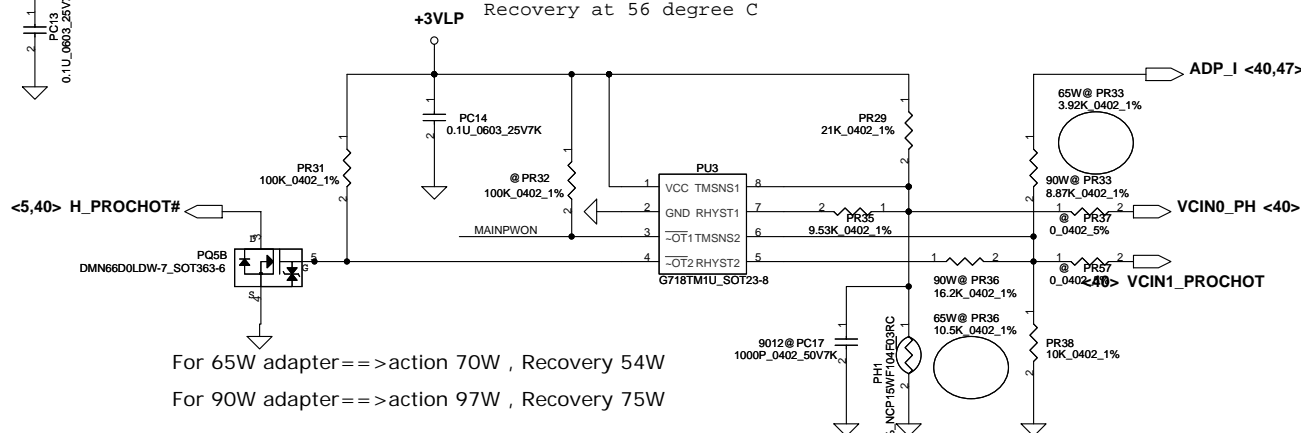
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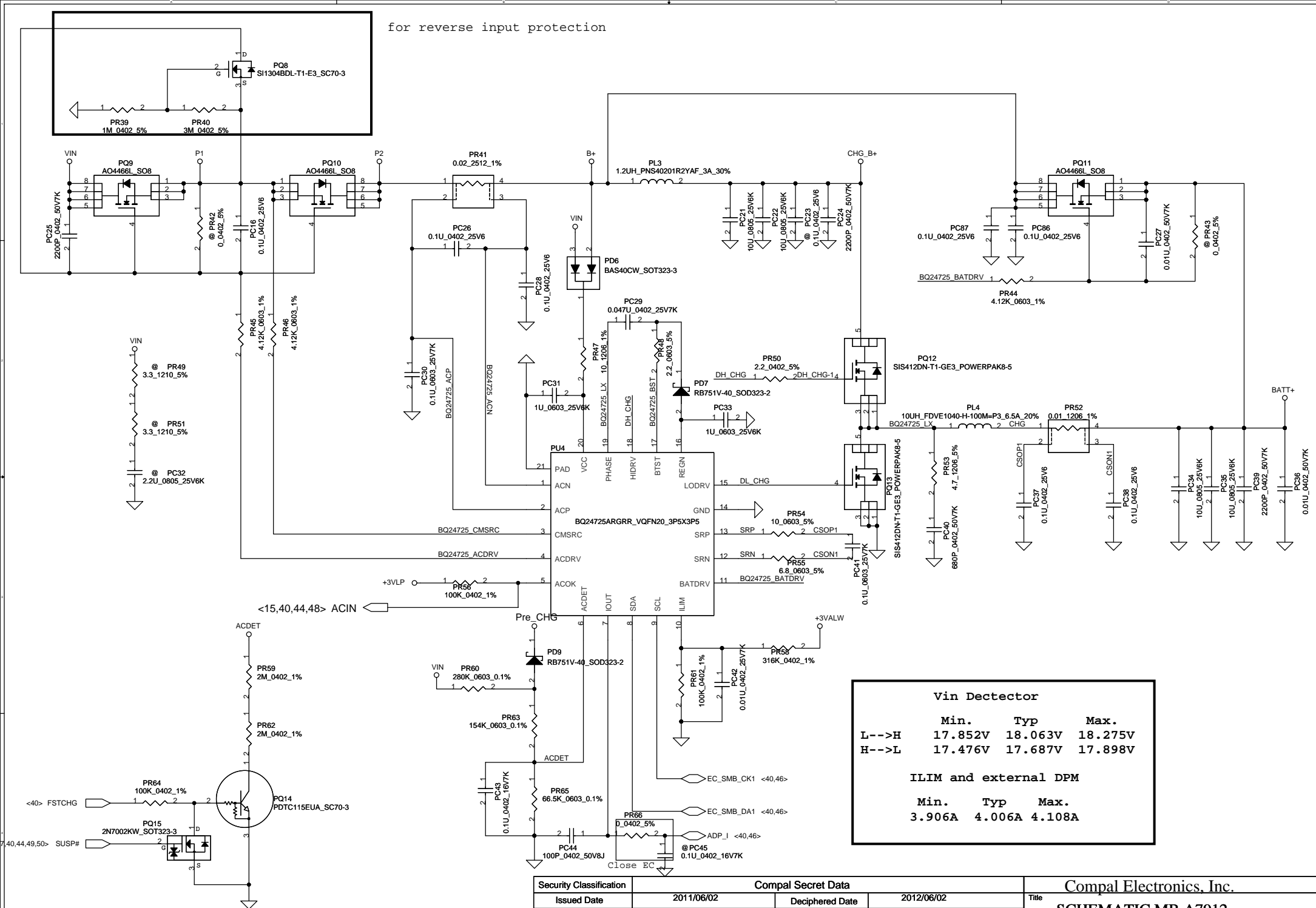
PH1 under CPU bottom side :  
CPU thermal protection at 92 degree C  
Recovery at 56 degree C



For 65W adapter==>action 70W , Recovery 54W  
For 90W adapter==>action 97W , Recovery 75W

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for reverse input protection



### Vin Detector

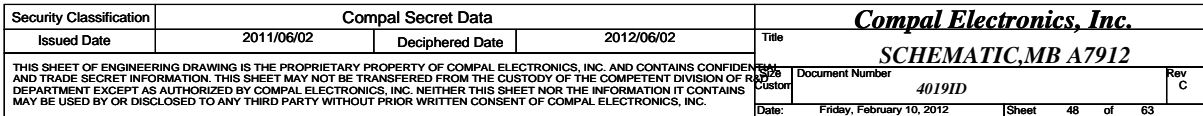
	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

### ILIM and external DPM

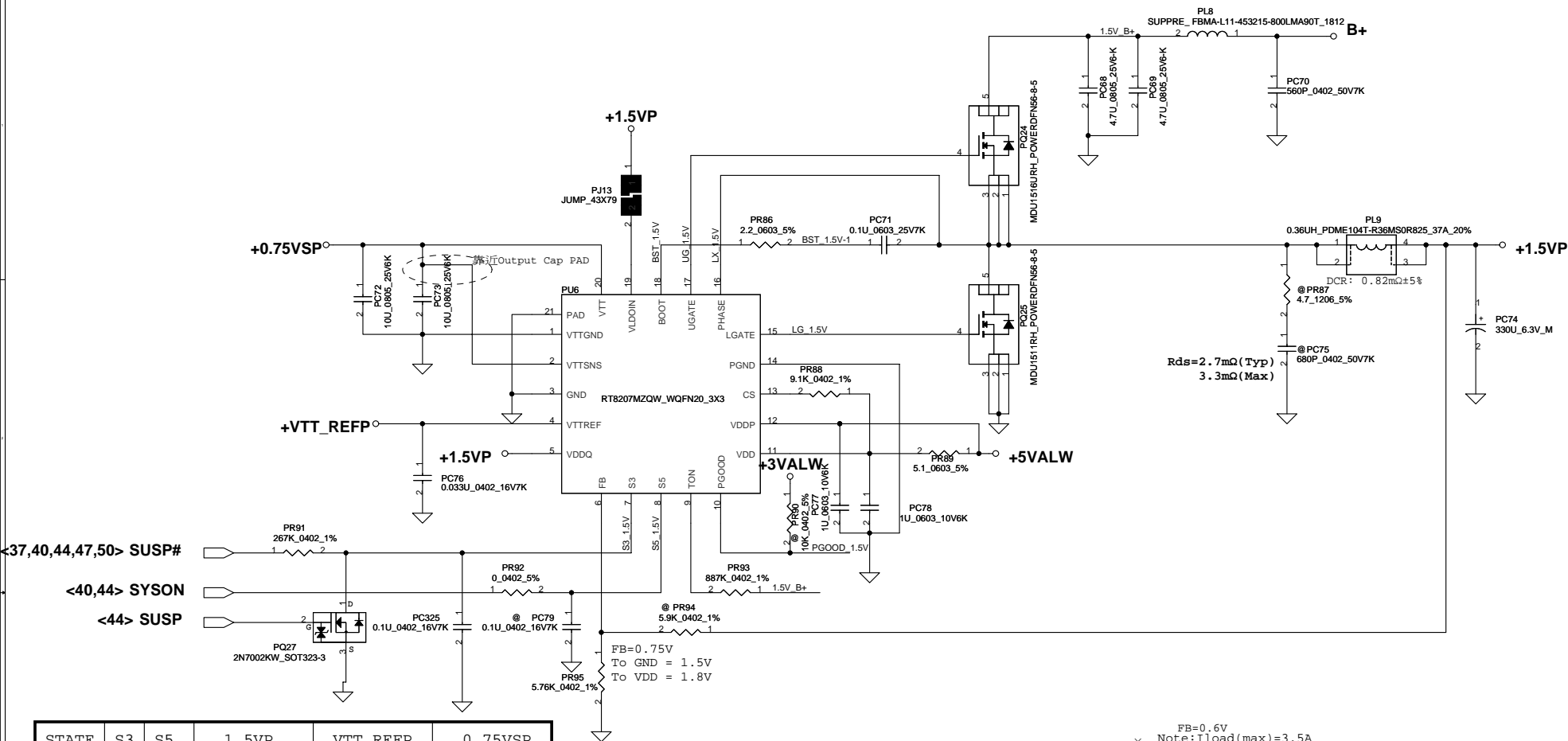
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

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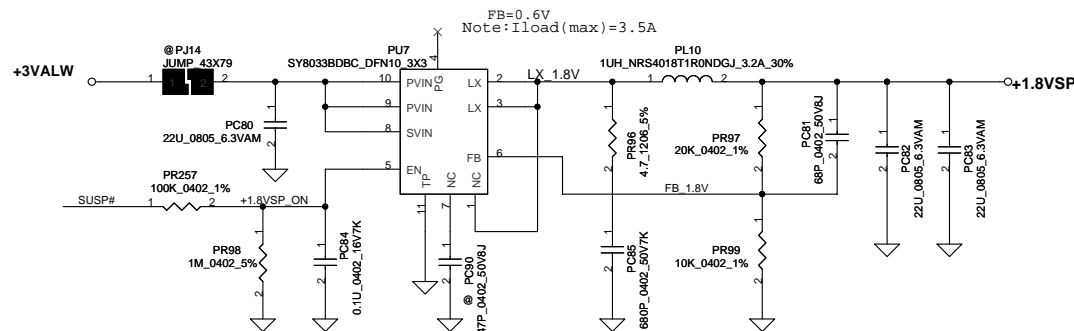
**WWW.AliSaler.Com**



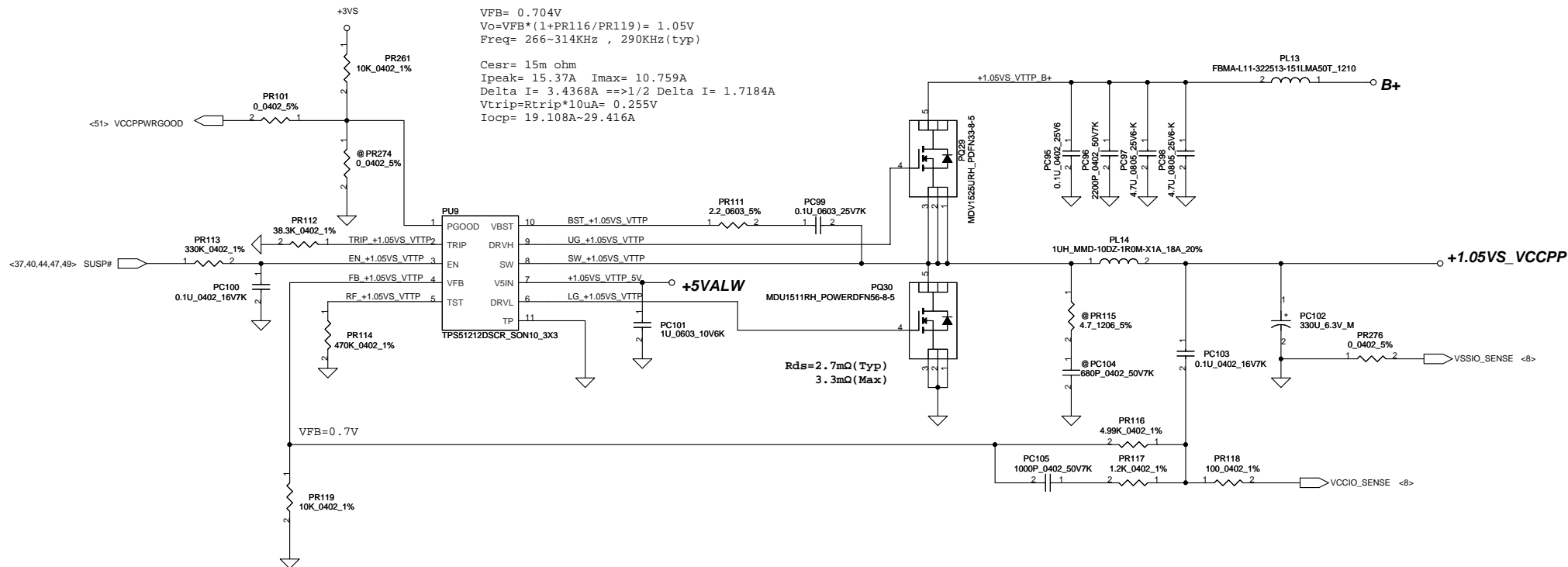




STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

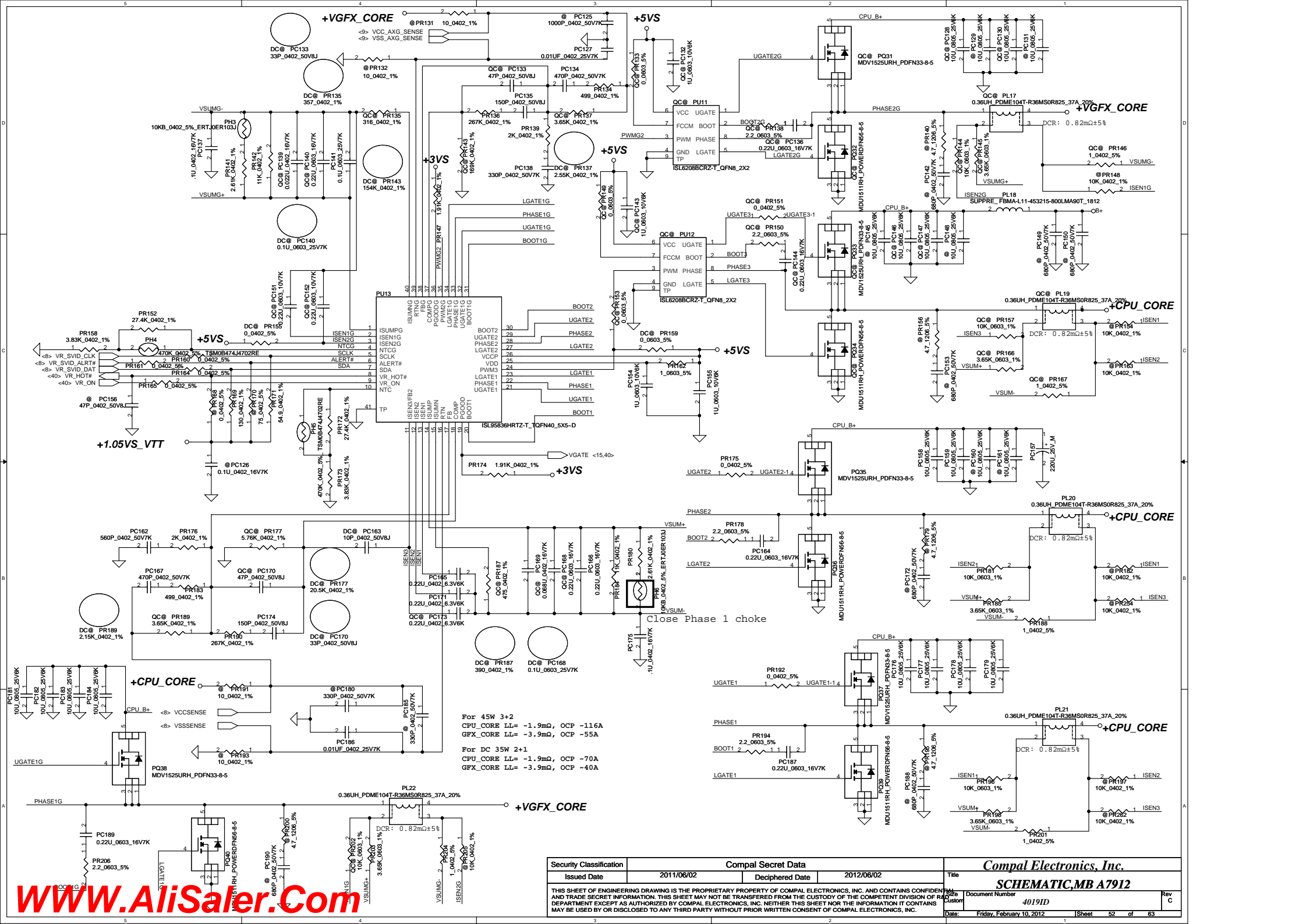


Notice: Internal resistance about 500K on 2nd EN pin

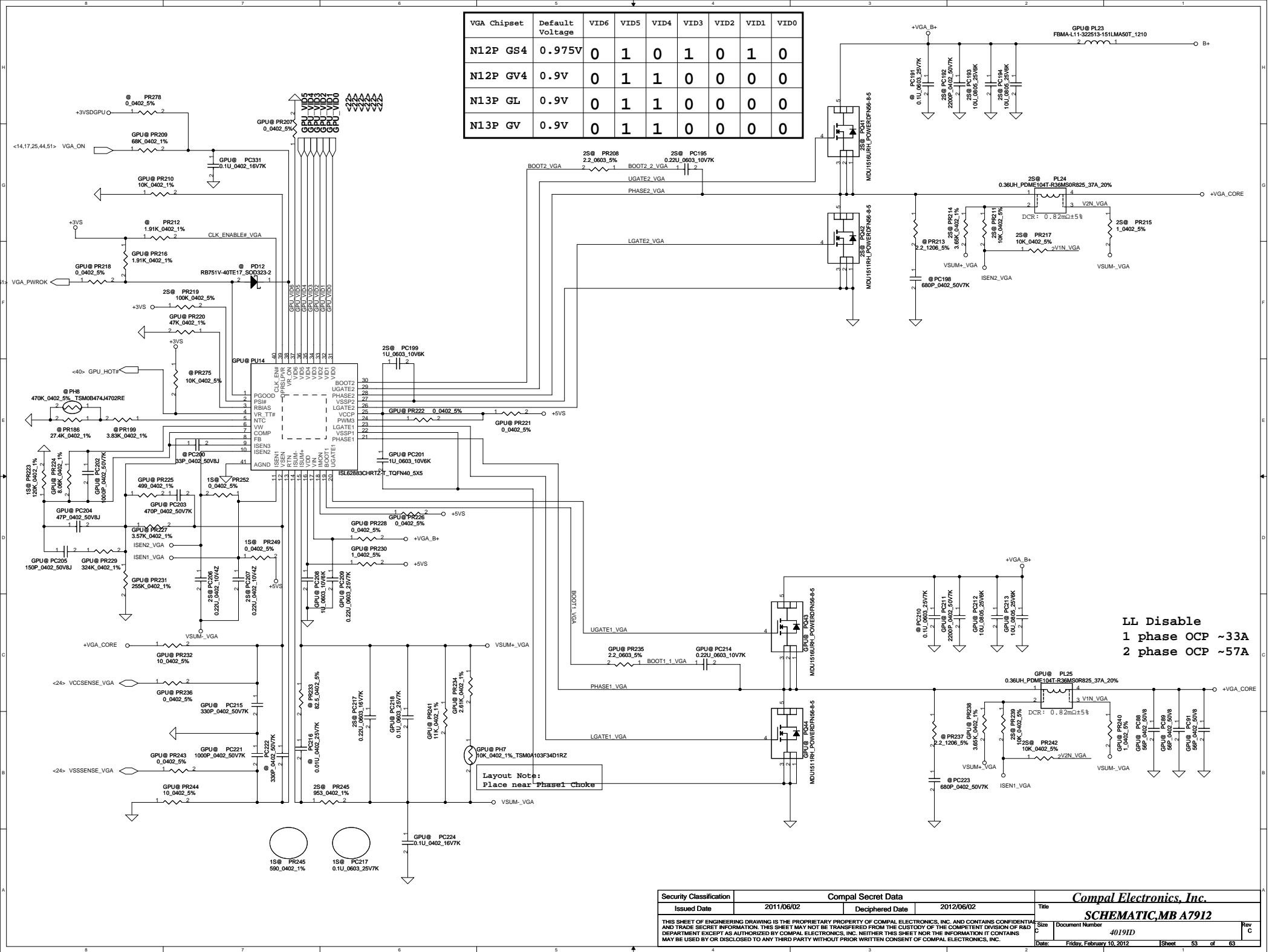


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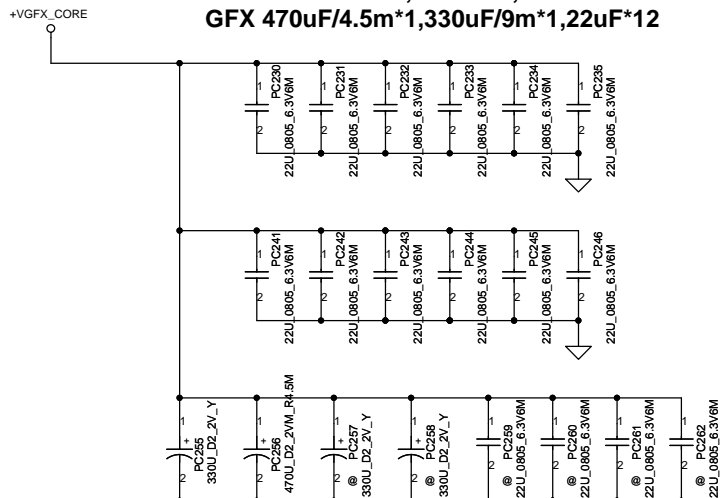




VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
N12P GS4	0.975V	0	1	0	1	0	1	0
N12P GV4	0.9V	0	1	1	0	0	0	0
N13P GL	0.9V	0	1	1	0	0	0	0
N13P GV	0.9V	0	1	1	0	0	0	0

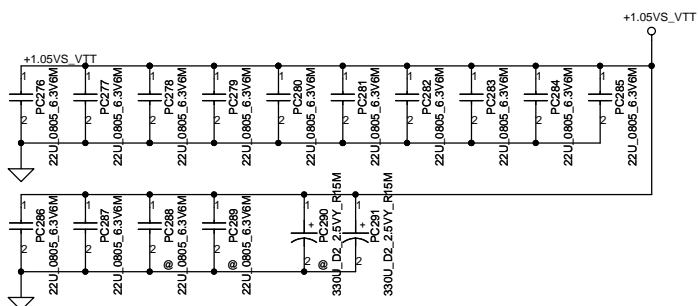


**PWR Rule**  
**CPU 330uF/9m \*5,22uF \*16,10uF\*10**  
**GFX 470uF/4.5m\*1,330uF/9m\*1,22uF\*12**

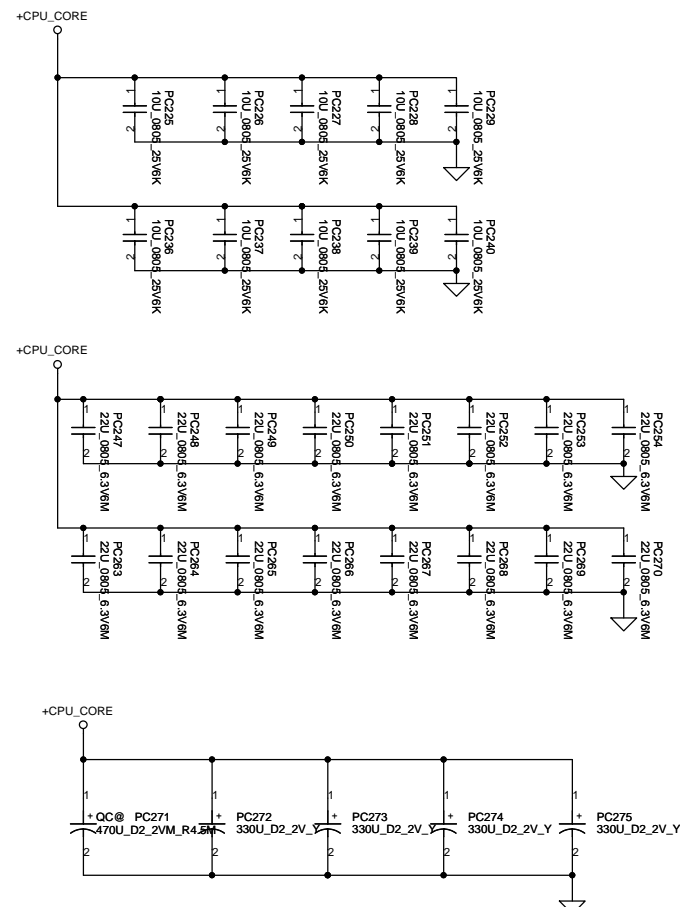


**Vaxg**

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

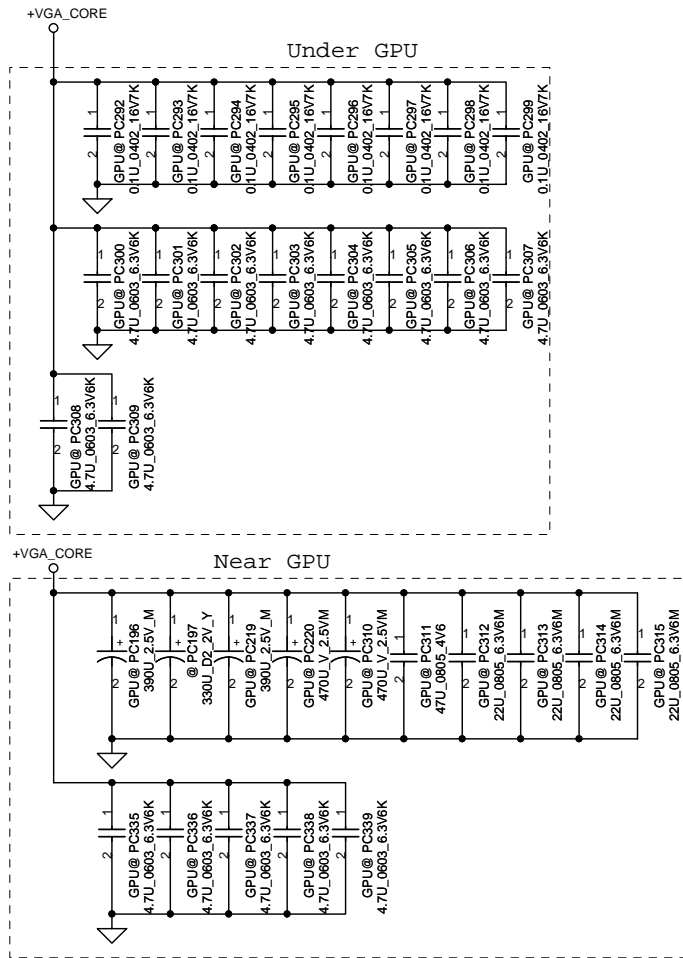


**INTEL Recommend**  
**3\*330uF(1 in other page),12\*22uF, 5 no stuff**  
**from PDDG 1.0**



DC@ PC271  
 330U\_D2\_2V\_Y

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	S3 sequence @ DC	Meet Intel sequence SPEC		49	Change RP91 to 267K	2011 1208	DVT
2	1.5VSDGPU lose	Improve FB pin anit-noise		51	Change RP248 to 2K, PR255 to 1.74K, PR253 to 137K	2011 1208	DVT
3	Cut-in SMT memo			52	Add PC182, PC184	2011 1208	DVT
4		Standard design			Change PR138, PR150, PR178, PR194, RP205 , PR235 to 2.2	2011 1208	DVT
5	Vth has risk			51	Change PU16 from G971 to APL5930	2011 1212	DVT
6		Enable select		51	Add PR266	2011 1217	PVT
7	Cut-in EMI solution			53	Add PC88, PC89, PC91	2011 1221	PVT
8		Consider part rating		51	Change PR277 from 0402 to 0603	2011 1222	PVT
9		Tune transient character		52	Add PC139, PC169 Swap PC271 & PC275	2011 1222	PVT
10		PH1 OTP and ADP_I throttling by H/W control		46	Delete PR37, PR57	2011 1222	PVT
11		Follow Power design		55	Add PC313, PC314, PC315	2011 1222	PVT
12	VGA sequence meet nVidia SPEC			51	Swap PR258 & PR263, PR266 & PR264, PR246 & PR265	2011 1223	PVT
13	Cut-in EMI solution			47	Add PR53, PC40	2012 0104	PVT2
10							
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
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17							

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.40.13		9/7	EC	Change th HDA_SDO to ME_EN		0.2
2	P.40		9/7	HW	Add R2085 ,change the EC_ACIN pull high to +3VLP		0.2
3	P.37		9/7	HW	Add f11009 USB3.0 TX coupling capacitor (c2060,c2061)		0.2
4	P.38.39.40		9/7	HW	Add USB chargeaer schematic(C2060.C2061.R2077~R2084,R2065~R2072)		0.2
5	P.22.40		9/7	HW	Follow ABO request,add ADPS function(Q2005),R2086.R2087)		0.2
6	P.20		9/7	HW	<del>Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2088)</del>		0.2
7	P.44		9/7	HW	<del>Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)</del>		0.2
8	P.43		9/7	HW	For FSOV spec,Chang R714,R716 from 75ohm to 47ohm.		0.2
9	P.13		9/7	HW	For WIN8,Change R681.R651.R684.R652 to 33ohm		0.2
10	P.44		9/7	HW	Delete C817,Change C826 from D2 size to B2 size		0.2
11	P.17.37		9/7	HW	Follow chief river common design, please chang Mini-Card 2(port 11) to port 9		0.2
12	P.38		9/7	HW	Delete +1.5V to +1.05V_V128 Transfer(U2002.R2002.R2003.R2005.C2002.C2003.C2005.R2008)		0.2
13	P.38		9/7	HW	Delete USB3.0 EEPROM(U2004.R2035.R2034.C2039)		0.2
14	P.37		9/7	HW	Reserve Mini-Card 2		0.2
15	P.19		9/7	HW	F2 flick issue on projector P5202 D-sub Add C2063.C2064		0.2
16	P.22.40		9/8	HW	Change VGA GPIO12 of dGPU connection to EC controlled for the power limited usage Add EC pin 107-->GPU ACIN		0.2
17	P41		9/14	HW	Add SW5.SW6 for EG project.		0.2
18	P27.30		9/14	HW	Swap MDC37 and MDC38 Swap MDA13 and MDA14		0.2
19	P06.11.17.35. P39.40.42		9/14	HW	For ESD request Add C2065~C2075		0.2
20	P16		9/16	HW	For HDMI PCH_DPB_HPD noise Add C2076		0.2
21	P31		9/16	HW	For LVDS power sequence Change R5 from 300 to 200 ohm Change R2 from 1k to 10k ohm change C2 from 0.047uF to 1uF		0.2
22	P18		9/16	HW	Delete PCH test ponit(T31~T46,T49~T61,T63~T65)		0.2
23	P21,40		9/19	HW	Change Q22,Q26 from SB000008J10 to SB000009080		0.2
24	P14,22,35,38		9/19	HW	For Crystal Change Y2 ,Y4 from SJ10000DJ00 to SJ10000E800 Change Y1000 from SJ10000DK00 to SJ100009700 Change C630,C631,C2019,C2028,C1008,C1009 to 10pF Change C681,C679 to 15pF		0.2

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25	P.44		9/20	EMI	For EMI request (Add C2079~C2084)		0.2
26	P.36		9/20	HW	For SD3.0 issue (Add R2088,R2089)		0.2
27	P.20		10/17	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2090)		0.3
28	P.44		10/17	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.3
29	P.40		10/17	HW	Board ID error. Add R353.		0.3
30	P.40		10/17	HW	Board ID 0.3. Change R353 to 18K		0.3
31	P.17,39		10/17	HW	Follow Intel's suggestion; Change USB3.0 from port 2 to port 1 Change USB2.0 from port 0,1 to port 2,9		0.3
32	P.18		10/18	HW	Support eDP GPIO71-->0 (eDP) GPIO71-->1 (LVDS)		0.3
33	P.13.40		10/25	HW	Co_lay NPCE885N Delete U38,C722,R690,R695,C727 Add C2085,R2091~R2096		0.3

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43	P.41		11/16	ME		Delete SW5,SW6, Pop SW2,SW3	0.4
44	P.05		11/16	HW	BUF_CPU_RST# noise	Add C2090	0.4
45	P.35		11/17	HW	LAN SPROM on Chip	De-pop U31,R537 Pop R538	0.4
46	P.36		11/17	EMI		Change C478 to 10P_50V	0.4
47	P.13		11/17	HW	RTC issue	Change C682,C686 to 15P	0.4
48	P.31,32,41		11/17	ESD		De-pop D3,D4,D17,D18,D15 Pop D24,D36	0.4
49	P.40		11/17	HW		De-pop R891,R893	0.4
50	P.24		11/21	HW		N13P_GS Change strap2 to PD 15k Change strap4 to PD 10k	0.4
51	P.13		11/21	HW		Chip Select Change R651,R2049 to 0ohm	0.4
52	P.13,40		11/21	HW		Delete NPCE885N (R2091.R2092.R2094.R2095.R2096,R698, R699,R692,C2085)	0.4
53	P.45		11/22	HW		Change +1.05VSDGPU JUMP size PJ19 change to 43x118	0.4
55	P.35,36		11/23	HW		Card Reader Change R216 to 22 ohm Change R2088 to 47ohm Change R2089 to 22 ohm Add C2091~C2093 Change R525,R536,R537,R538 to 1k	0.4
56	P.13		11/23	HW		Delete R2093,R2049,R651(0ohm)	0.4
57	P.13		11/23	HW		Change N13P-GS to SA000051880 Change U33 to SA00005AG00	0.4
58	P.35, P36		11/23	HW		Del C2093, R222, R2089, net(CR_CLK_XD_RY_BY#_23) Add R2101, C2094	0.4
59	P.36		11/24	HW		ADD R2102, C2096 for EMI ISSUE	0.4

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58	P.24.25		12/02			Change R1057 from 35kohm to 45kohm Change R1077 from 40.2ohm to 42.2ohm Change R1080 from 60.4ohm to 51.1ohm	0.4
59	P.22		12/02			for N13P_GS, the boot voltage is 0.9V pop R1022,R1021,R1036,R1035,R1034,R1033 for N13P_GL, the boot voltage is 0.95V pop R1022,R1037,R1020,R1019,R1034,R1033 for N13M_GS, the boot voltage is 0.925V pop R1022,R1037,R1020,R1019,R1018,R1033	0.4
60	P.44		12/02			Change R369 from 470ohm to 150ohm Change R26 from 470ohm to 47ohm Pop Q3	0.4
61	P.13		12/02			BIOS ROM(4M) Change U36 to SA00003K800	0.4
62	P.35		12/06			EMI suggestion for Card Reader Change R195 from 33ohm to 22ohm Change R216 from 22ohm to 0ohm Change C2094 from 6pF to 6.8pF Change R2101 from 0ohm to 22ohm Change R2088 from 47ohm to 75ohm Change R2102 from 47ohm to 0ohm De-pop C2096	0.4
63	P.36		12/07			EMI request for 家電下鄉 Add C2097	0.5
64	P.39		12/07			For PCH HM70 Change USB port0 to co-lay USB3.0 Change USB port2 to USB2.0 Change USB port 11 to BT	0.5
65	P.44		12/07			Change 1.5VSDGPU EN from VGA_ON# to VGA_PWROK# Add R2103,Q2008	0.5
66	P.18		12/09			For eDP Change Q2007 from SB501380020 to SB501110010	0.5

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67	P.31		12/16	EE		change Q2007 to 2N7002 for eDP_HPD circuit	LA-7912 0.2
68	P.40		12/16	EE		add WLAN_PME# on pin85. add wlan_on signal on EC pin38 add AC circuit	LA-7912 0.2
69	P.35		12/16	EE		reserve Q2007 for open +3V_LAN by PCH_PWREN#	LA-7912 0.2
70	P.40		12/16	EE		add R2063 for pull high VCIN0_PH to +3VL 10k add R2059 for pull low VCIN1 10k	LA-7912 0.2
71	P.41		12/20	EE		resever R2116 ~ R2119 for change LED power to 3VLA-7912 resever C2101~C2107 56pF on T/P for EMI	0.2
72	P.36, 14		12/22	EE		change R384 & R385 power to +3V_LAN unpop R630 & reserve R2120 to pull high +3V_LAN	LA-7912 0.2
73	P.42, 35		12/22	EE		change Q43 from 2n7002 to BSS138 unpop R209	LA-7912 0.2
74	P.40		12/23	PWR		change R353 to 56k for board ID 0.2 power request pop R2063, R2059 un-pop R880, R891, R893	LA-7912 0.2
75	P.39		12/23	EMI		change USB3 signal pass by chock (SM070001600)	LA-7912 0.2
76	P.41		12/23	ME		Change LED(Blue) SC591NB5A30 to SC591TBKA10 Change LED(AMBEL) SC500007700 to SC500005930 change (R2116=130ohm), (R377,2118,378=390ohm) (R2117,2119 = 51 ohm)	LA-7912 0.2
78	P.36		12/23	EMI		R2088 change to 10ohm	LA-7912 0.2
79	P.25		12/23	EMI		L1002 use SM010028800 (for N13P_GL) use 0ohm on N13P_GS,N13M_GS	LA-7912 0.2
80	P.44		12/24	EE		POP R2104, R2106 unpop R2105, R2107 for VGA sequence	LA-7912 0.2
81	P.41,24		12/24	EMI,EE		De-pop C217,C216 EMI request. add R1019, R1020, R1037 for GM@ (VGA_CORE)	LA-7912 0.2
82	P.40,27		12/27	EE		change R2059&R2063 to 10k ohm for EC request C2086~C2089 change bom sturte to DIS@	LA-7912 0.2
83	P.40		12/27	EE		add R2125, R2123 for option WL_OFF# to EC or PCH add R2122, R2124 for option BT_ON# to EC or PCH reserve R2126 to pull high 3VALW reserve R2127 to pull high 3VALW	LA-7912 0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
83	P.41		01/02	EE		reserve R2121 for WLAN_LED connect +3VALW change C2101~2107 bomstucture to GM@	LA-7912 0.3
84	P.13		01/09	EE		add GPIO23 for define USB config. (R2128 & R2092)	LA-7912 0.3
85	P.45~56		01/09	PWR		update power circuit	LA-7912 0.3
86	P.37		01/09	EE		change R2110 to pull high +3VS_FULLL	LA-7912 0.3
87	P.31		01/10	EE		add R2130 reserve for lvds short issue	LA-7912 0.3
88	P.40		01/10	EE		change board ID to 0.3 (R353 100k)	LA-7912 0.3
89	P.37		01/11	EE		change R2110 to pull high +3VALW	LA-7912 0.3
90	P.37		01/11	EE		pop +3VS_FULLL 開電線路	LA-7912 0.3
91	P.13		01/11	EE		add new bom structer usb2@ for usb flag	LA-7912 0.3
92	P.44		01/11	EE		UNPOP +1.5VSDGPUH to +1.5VSDGPU circuit	LA-7912 0.3
93	P.35, 40		01/12	EE		add R2131,R2132 for option turn off 3VLAN power by PCH_PWR_EN# or LAN_PWR_EN# (from EC)	LA-7912 0.3
94	P.37, 40		01/18	EE		add R2134~R2136 reserve for AOIC for ACER request	LA-7912 0.3
95	P.17		01/18	EE		reserve R2137 pull low USB_P8 for PCH leakage	LA-7912 0.3
96	P.32		02/02	EE		change R428 & R426 to 0 ohm for CRT issue	LA-7912 0.3

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