

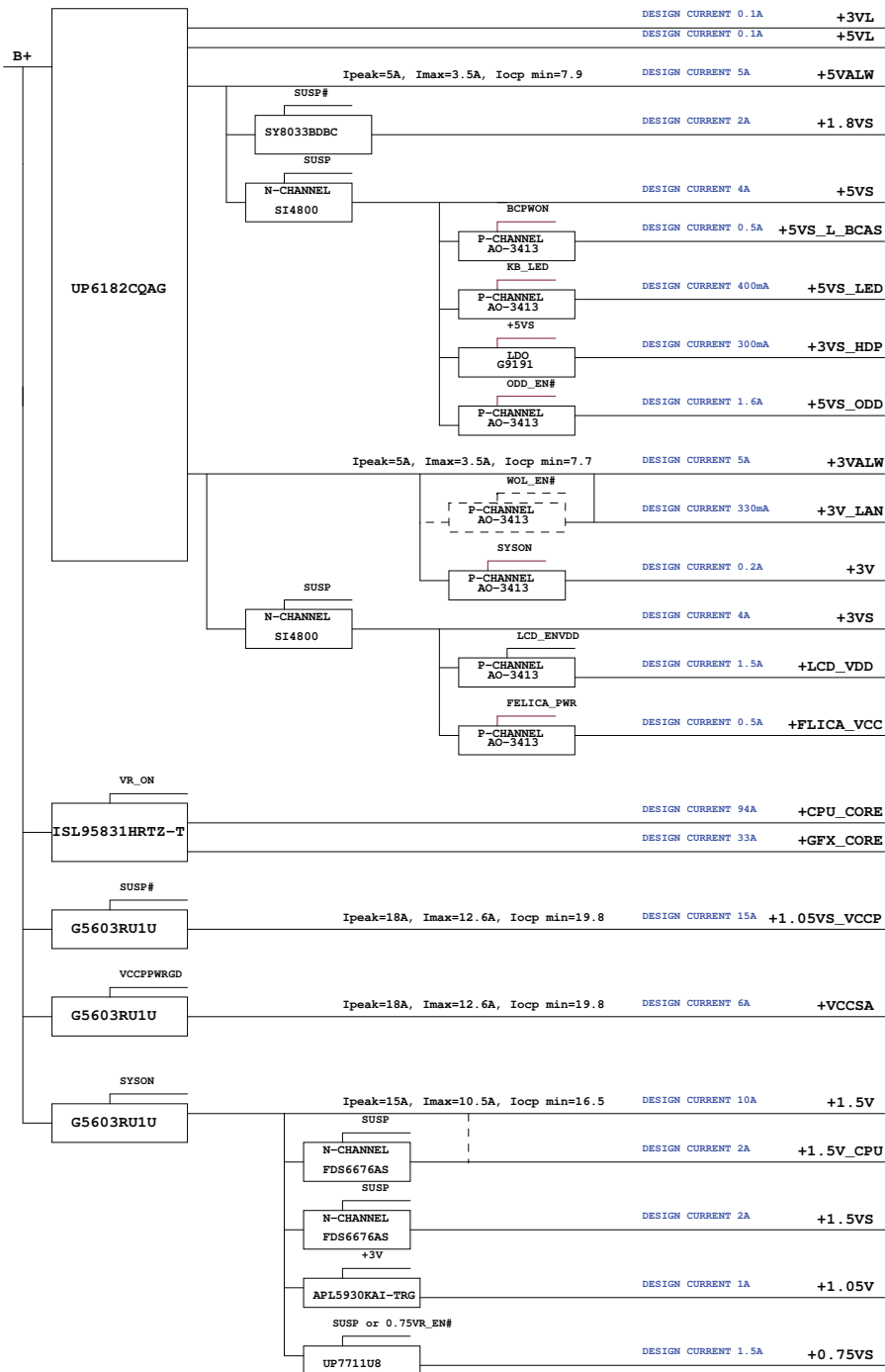
PHQAA

Marseille 10R/10RG

LA-6832P REV 0.2 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2010-09-03 Rev 0.1

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				Date:	Thursday, October 07, 2010
				Sheet	1 of 45
				Rev	0.2
				PHQAA LA-6832P M/B	



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				Date	Thursday, October 07, 2010
				Sheet	3 of 45
				Rev	0.3
				PHQAA LA-6832P M/B	

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b	+3VS	NVIDIA GPU	9A H	1001 1010 b
				+3VS	G-Sensor	40 H	0100 0000 b
				+3VS	Light Sensor	52 H	0101 0010 b
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/ Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

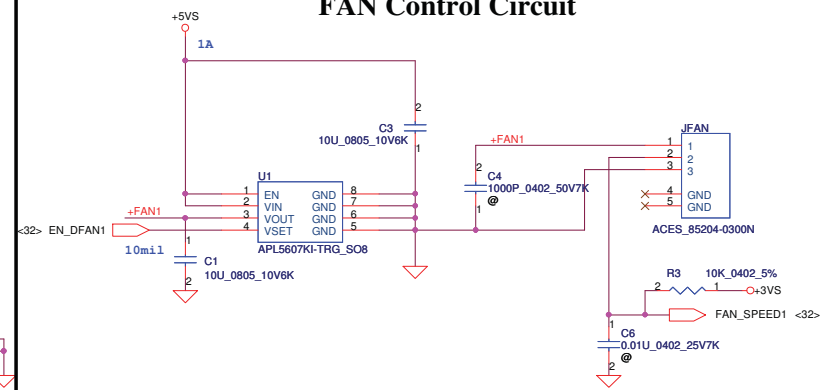
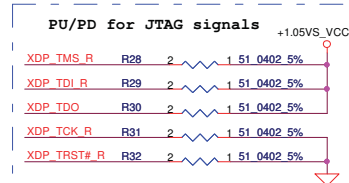
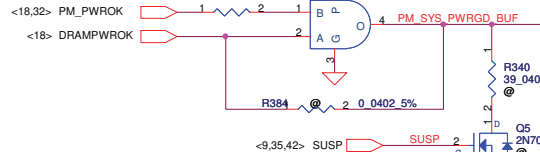
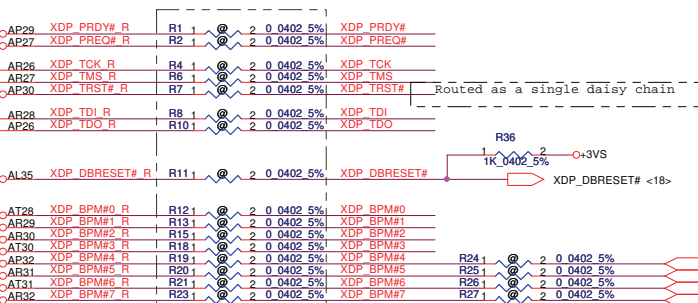
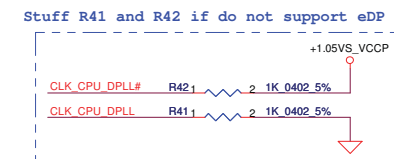
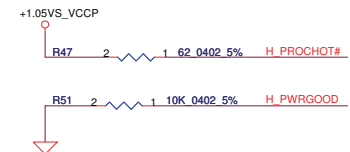
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					
description	S3 Power Saving		N11P & N11E			N11M		
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-GE2	N11M-OP1
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE1@	N11MGE2@	N11MOP@

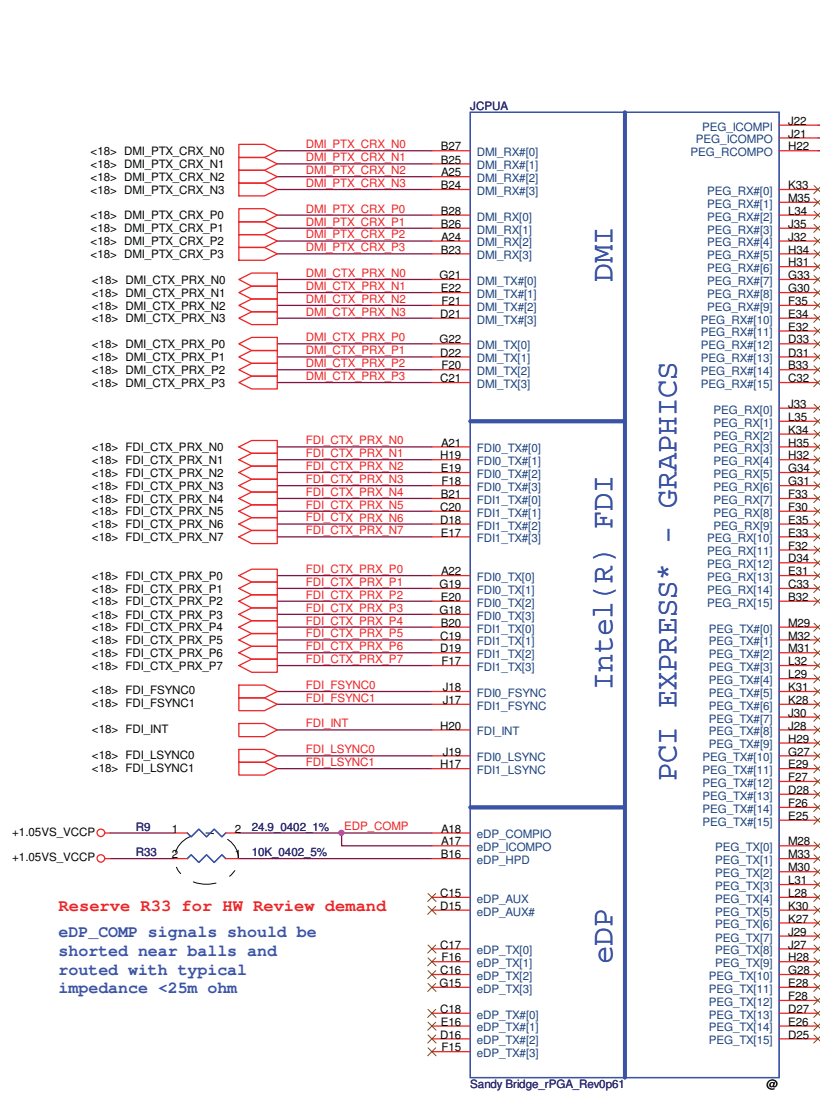
Function	Card reader		New Card
description	JMB385C/389C		New Card
explain	JMB385C	JMB389C	New Card
BTO	JMB385@	JMB389@	NEW@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

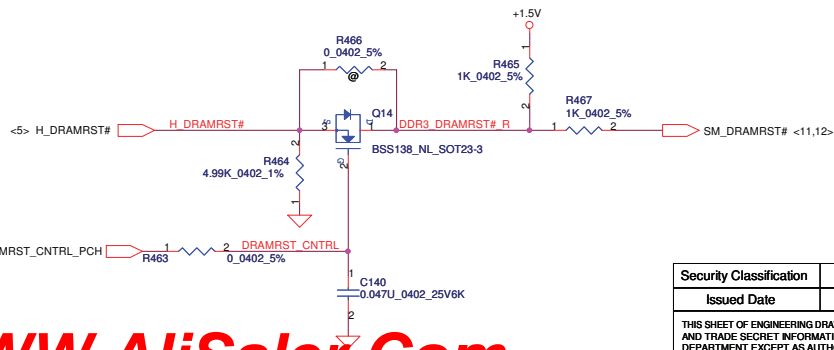
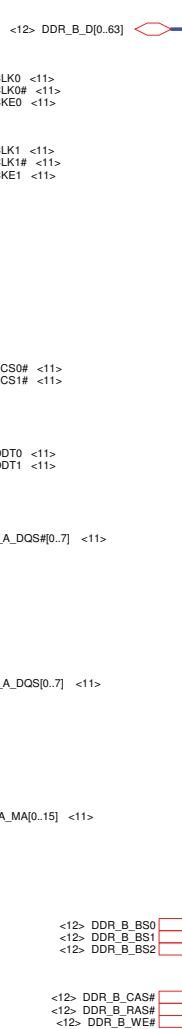
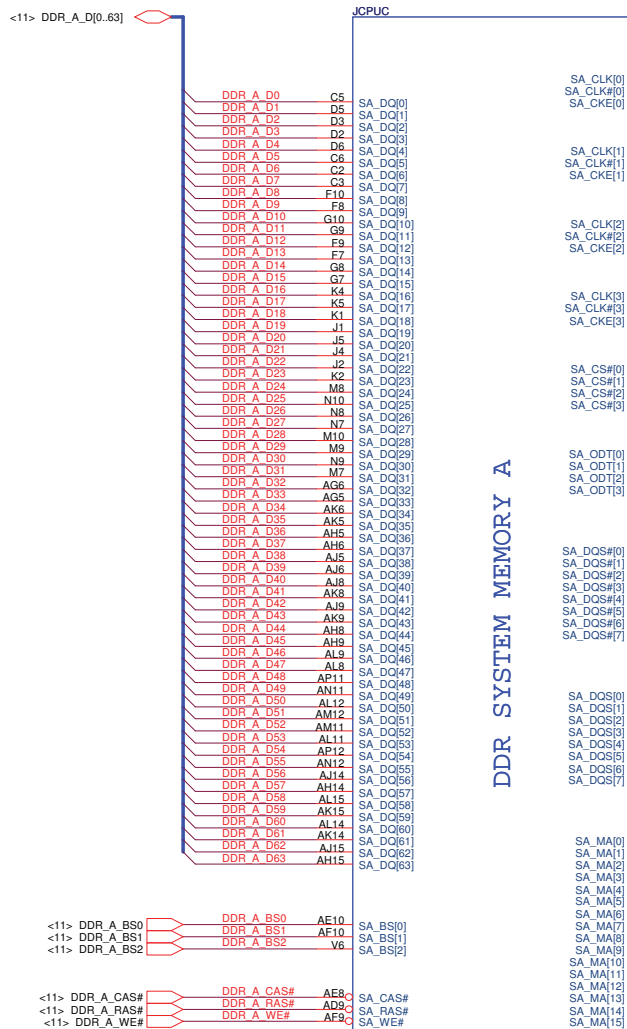
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								Date:		Thursday, October 07, 2010		Sheet



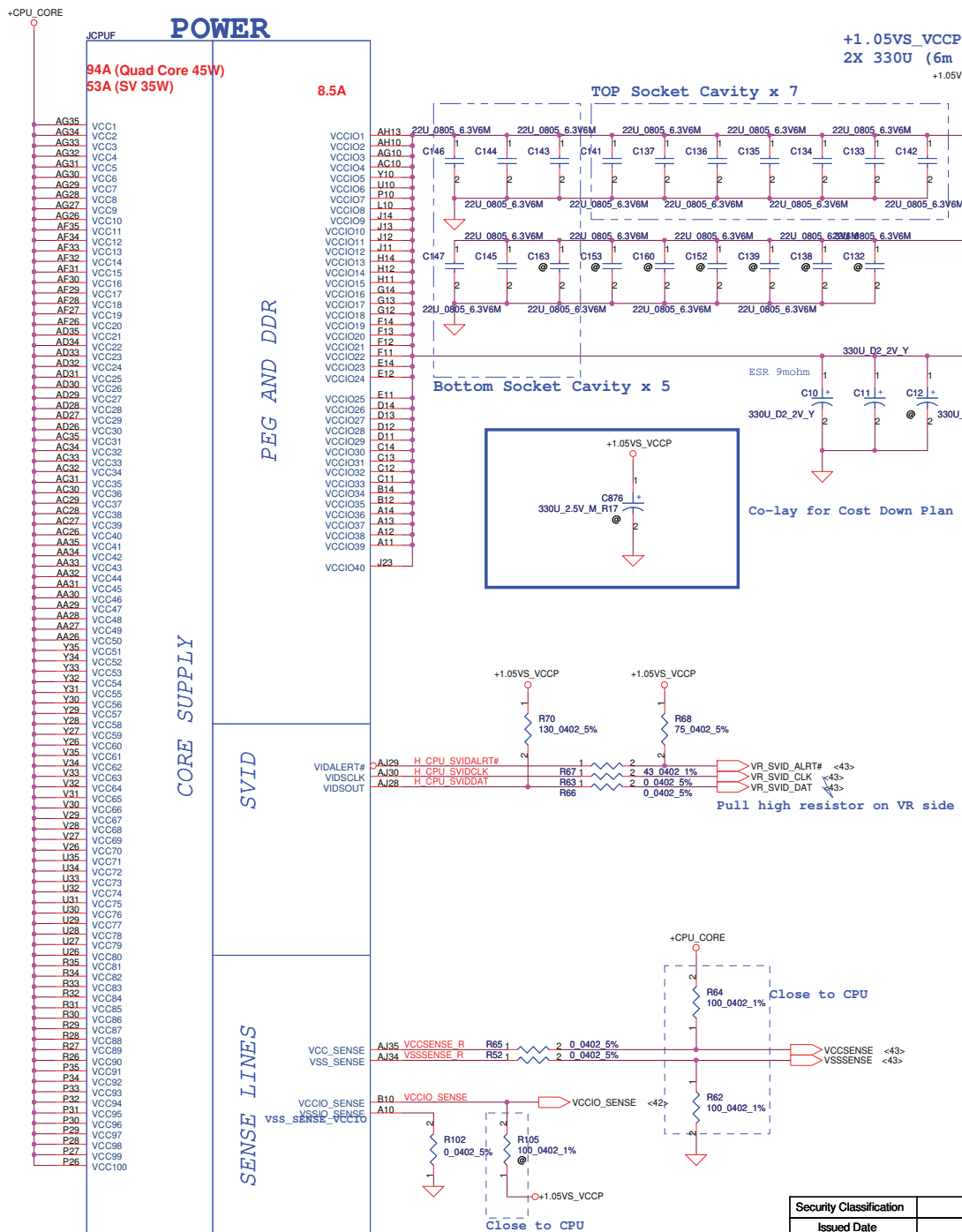
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	Sandy Bridge_JTAG/XDP/FAN	
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				Custom	PHQAA LA-6832P M/B	0.2
				Date:	Thursday, October 07, 2010	Sheet 5 of 45



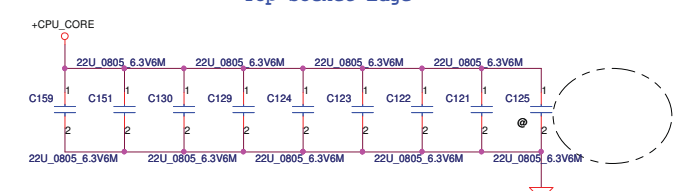
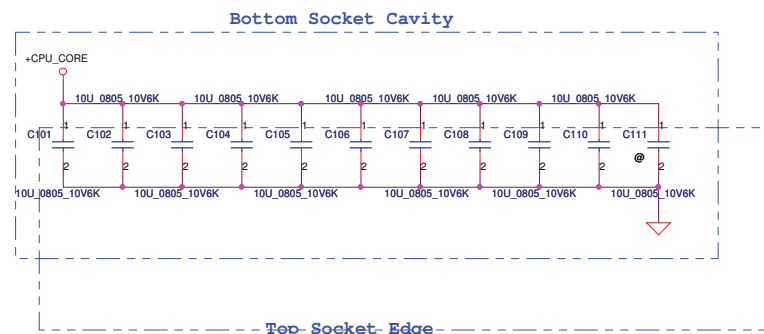
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Date:	Thursday, October 07, 2010	Sheet	6	of	45



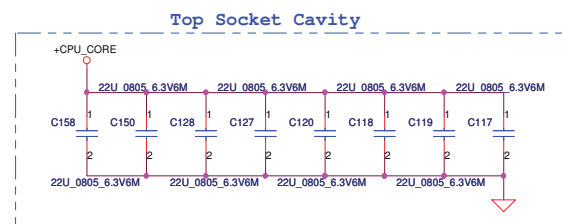
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				Date Thursday, October 07, 2010	Rev 0.2
				Sheet 7	of 45



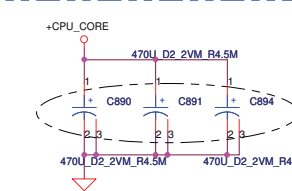
+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U



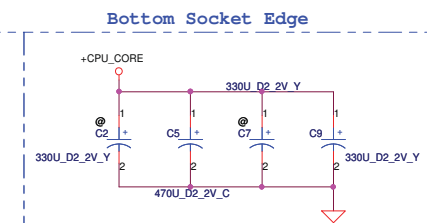
9/02 Remove C126, C131 by Power Demand



Co-Lay with C2, C5, C7, C9

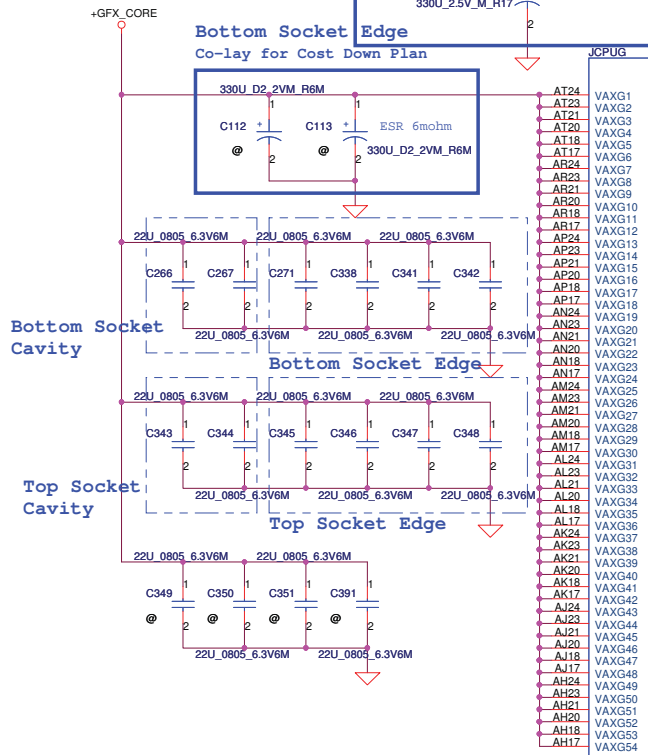


9/02 Add C898 3Pin Bulk Cap by Power Demand
9/02 Change C890, C891, C894 from SGA00005R00 to SGA00004X80 for Power demand

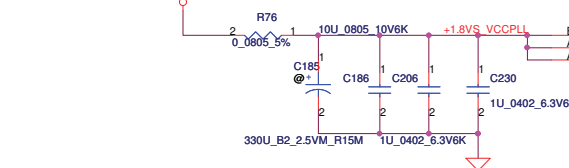


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						Custom	PHQAA LA-6832P M/B	0.2
						Date:	Thursday, October 07, 2010	Sheet 8 of 45

+GFX_CORE Decoupling:
2X 470U (4m ohm), 12X 22U



VCCPLL Decoupling:
1X 330U (6m ohm), 1X 10U, 2x1U



POWER

SENSE LINES
VAXG_SENSE
VSSAXG_SENSE

VREF

DDR3 -1.5V RAILS

SA RAIL

MISC

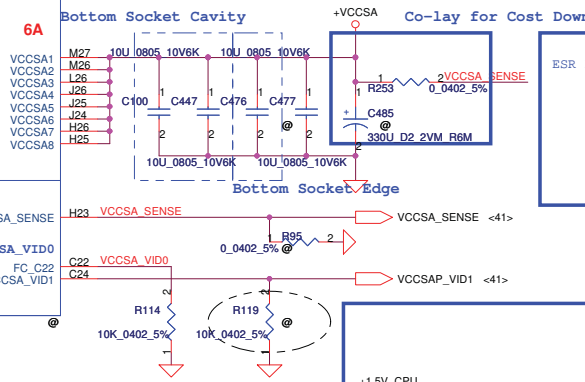
1.8V RAIL

5A

6A

1.2A

+VCCSA Decoupling:
1X 330U (6m ohm), 3X 10U



08/18 Reserve R119 to follow CRB 1.0

+GFX_CORE
Close to CPU

+V_SM_VREF
have 20 mil trace width

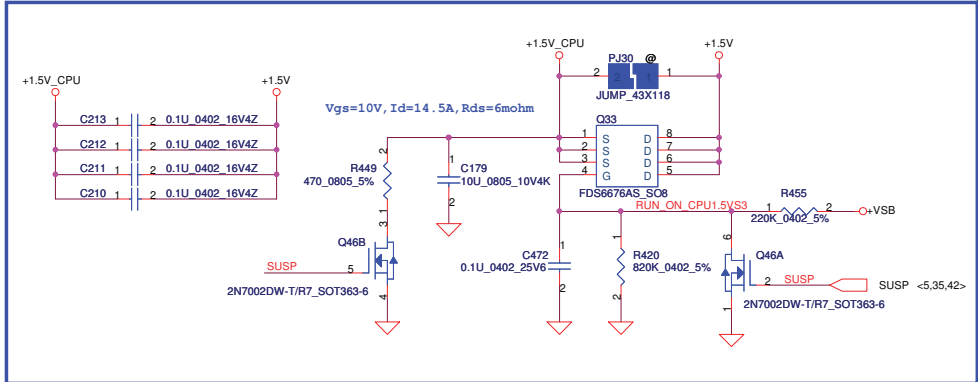
+1.5V_CPU Decoupling:
1X 330U (6m ohm), 6X 10U

+VCCSA
Co-layer for Cost Down Plan

+VCCSA
Co-layer for Cost Down Plan

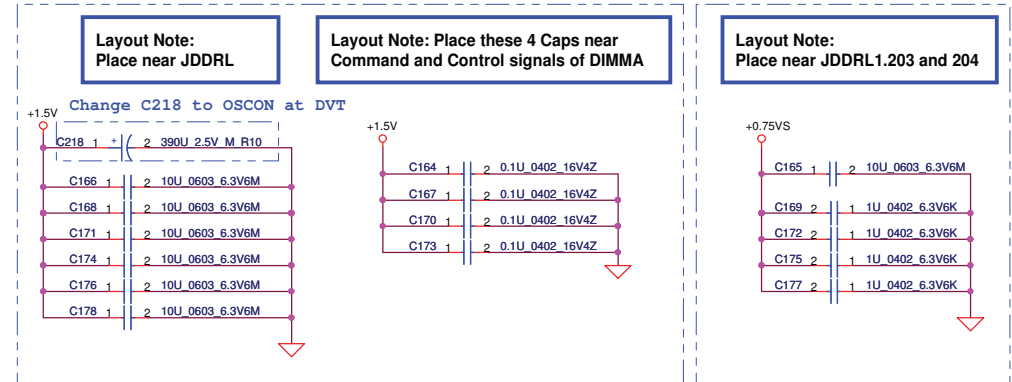
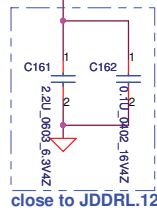
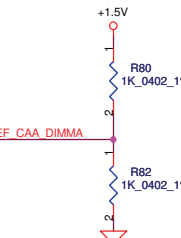
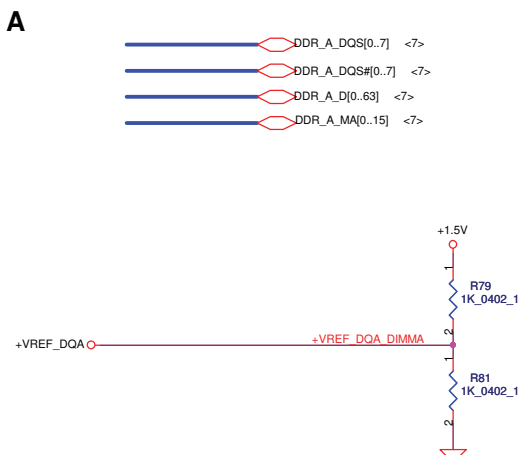
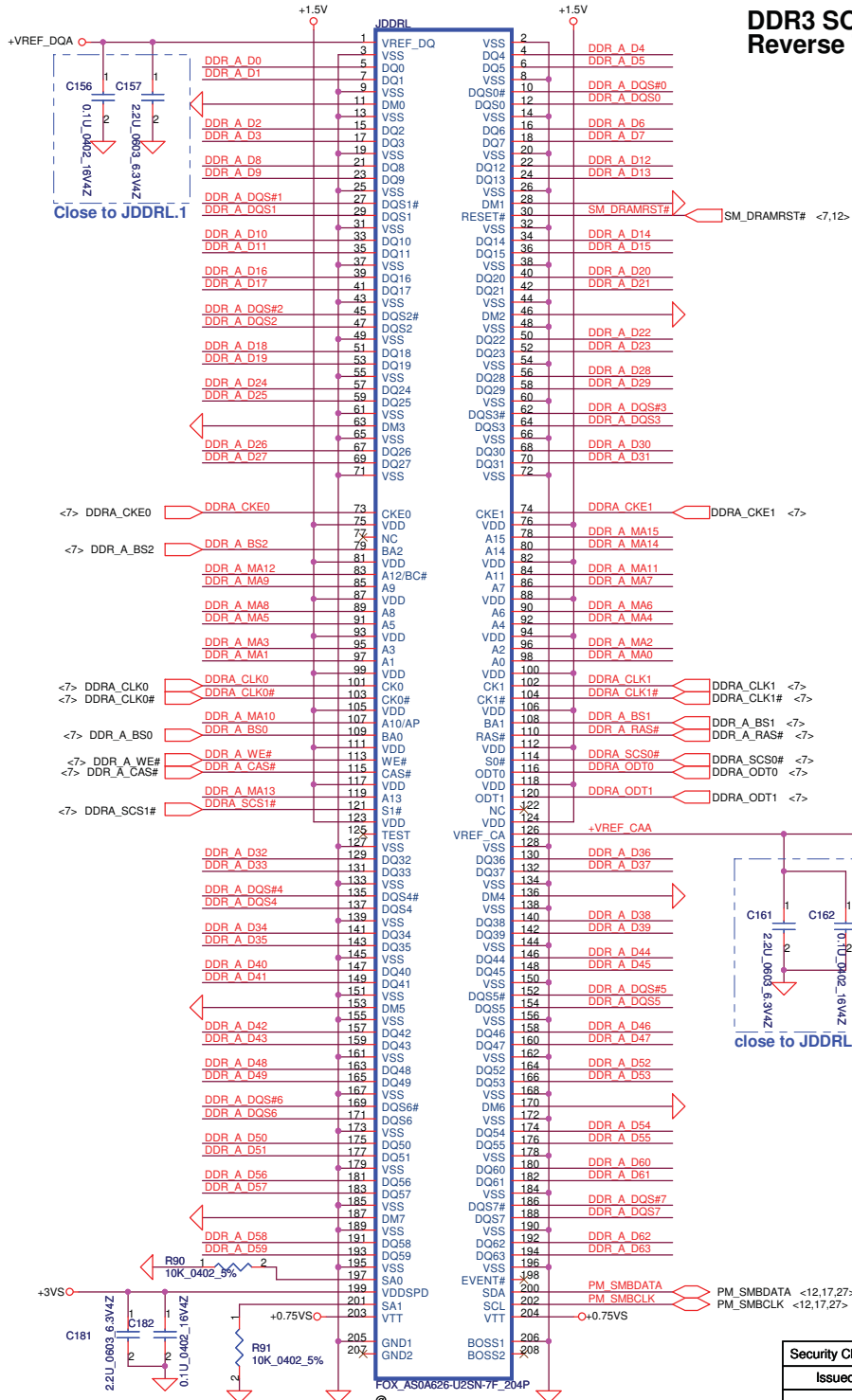
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.75 V
1	1	0.65 V

For Sandy Bridge



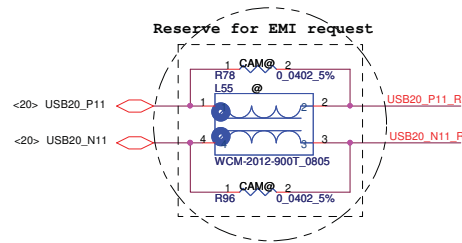
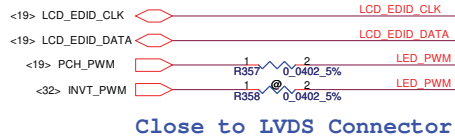


DDR3 SO-DIMM A Reverse Type

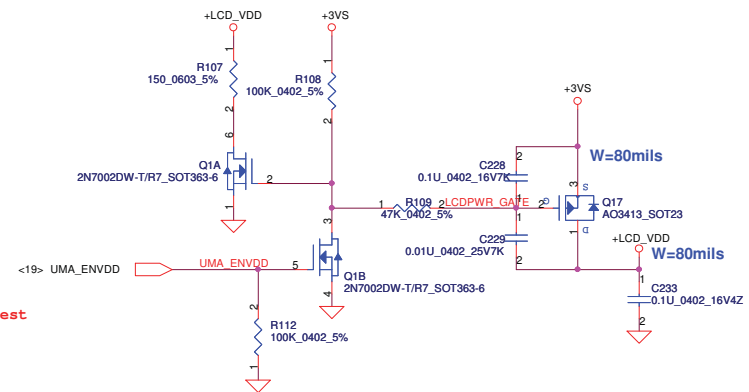


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				DDR3-SODIMMO	
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				PHQAA LA-6832P M/B	
				Date:	Thursday, October 07, 2010
				Sheet	11 of 45

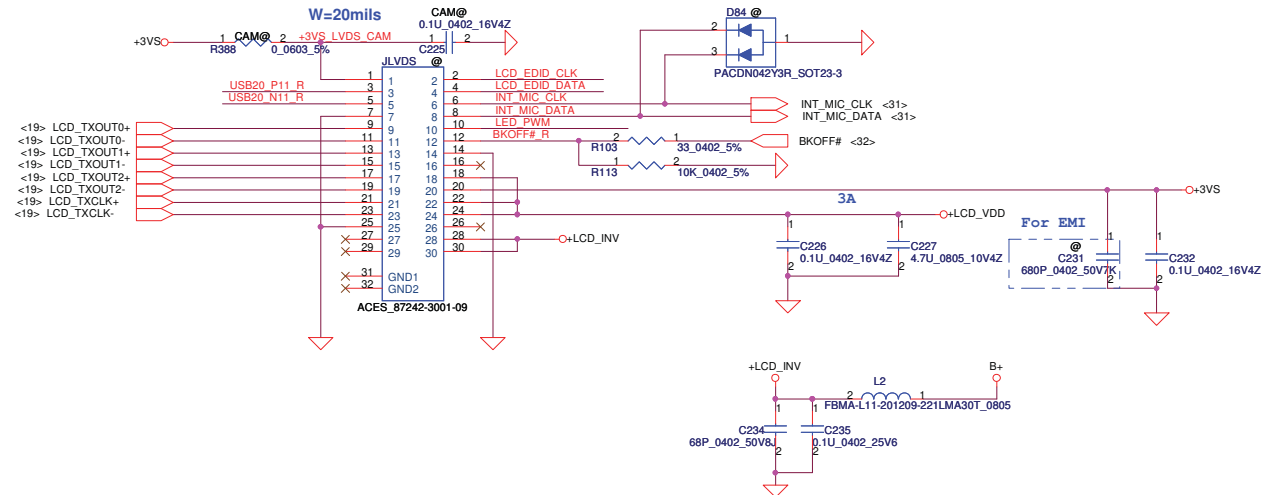




8/20 Swap USB20_P11 and USB20_N11 for layout request

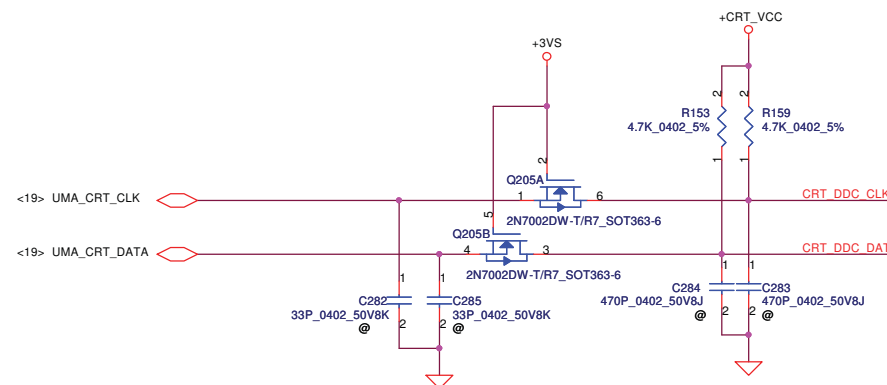
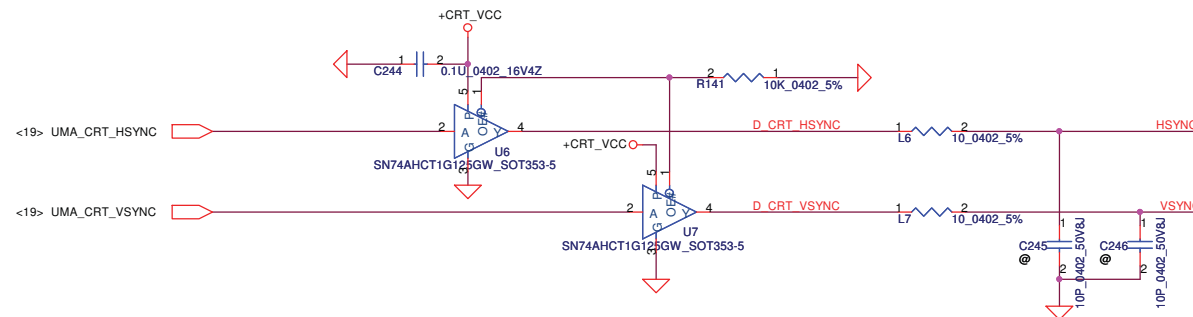
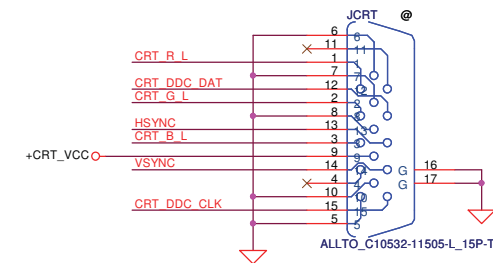
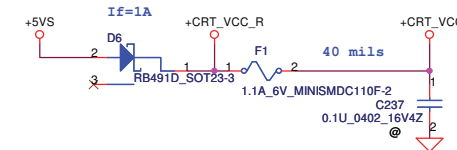
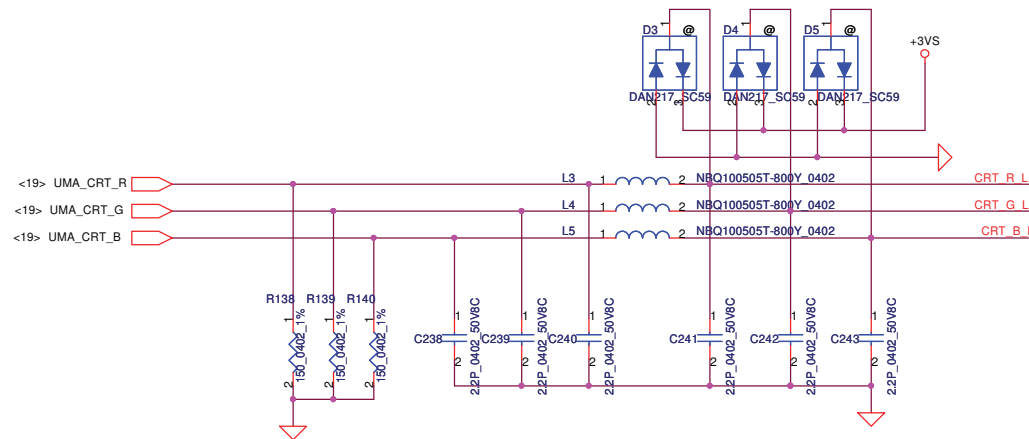


LCD/PANEL BD. Conn.



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				PHQAA LA-6832P M/B	
				Date: Thursday, October 07, 2010	Sheet 13 of 45

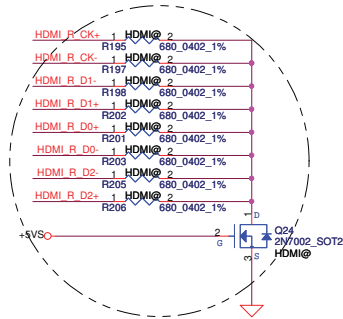
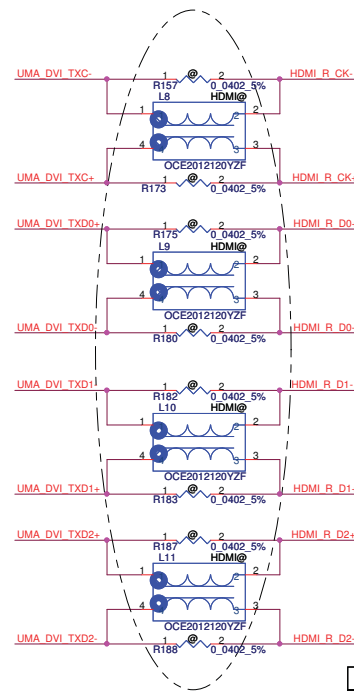
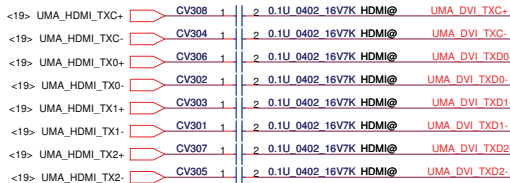
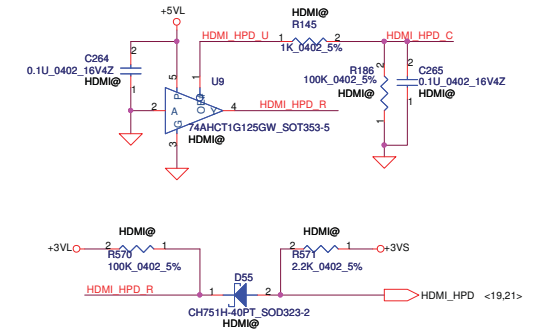
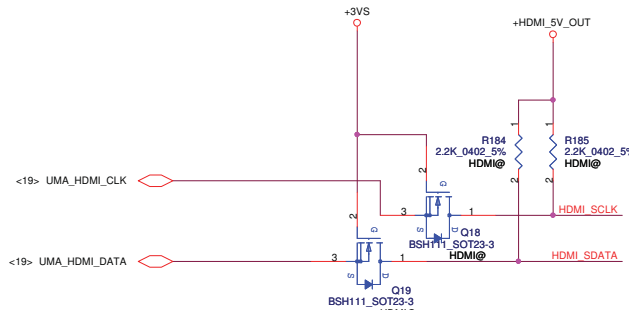
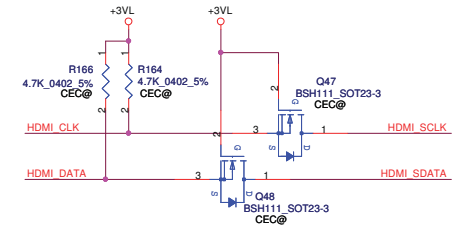
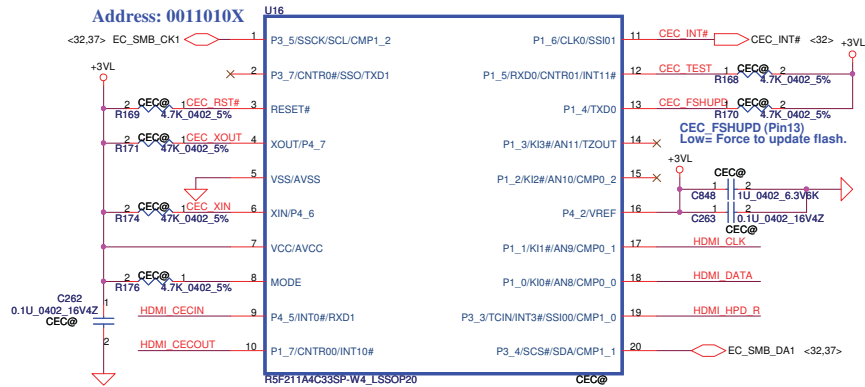
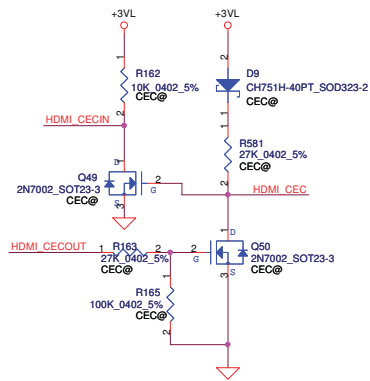
CRT CONNECTOR



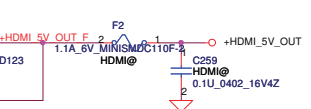
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										Rev 0.2	
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										Sheet 14 of 45	

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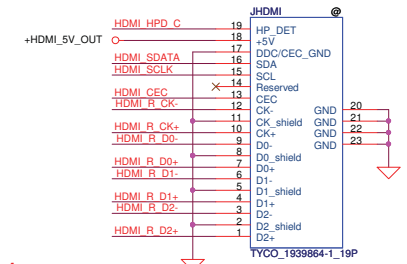
HDMI CEC Controller



08/18 Change R195, R197, R198, R202, R201, R203, R205, R206 to SD028680080 for UMA request

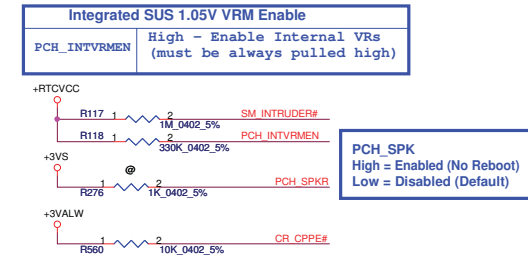
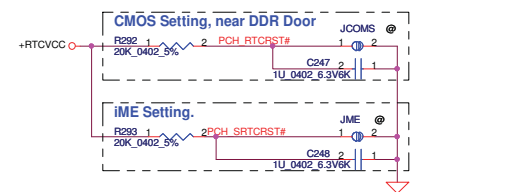


HDMI Connector



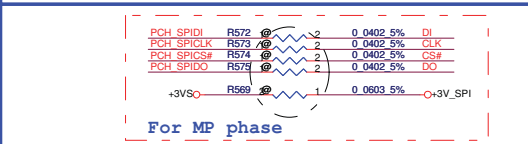
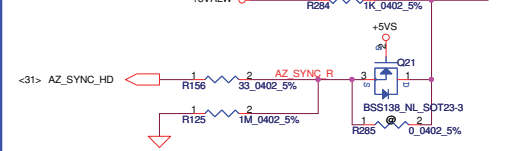
08/13 Change L8, L9 L10, L11 from SM070001600 to SM070001310 by EMI demand

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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	HDMI Conn./CEC
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					PHQAA LA-6832P M/B
				Date	Thursday, October 07, 2010
				Sheet	15 of 45
				Rev	0.2

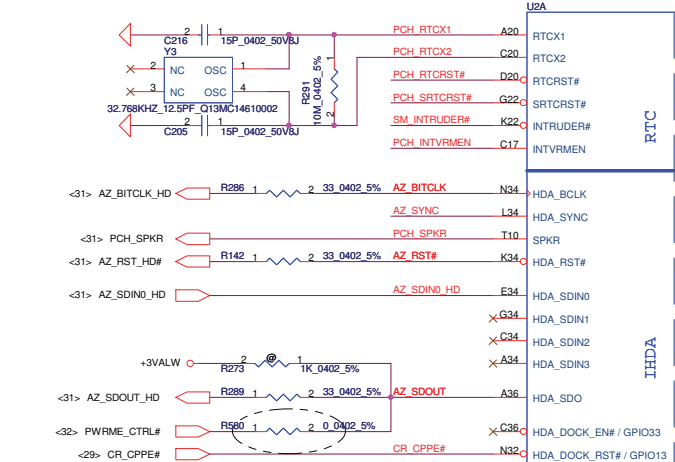
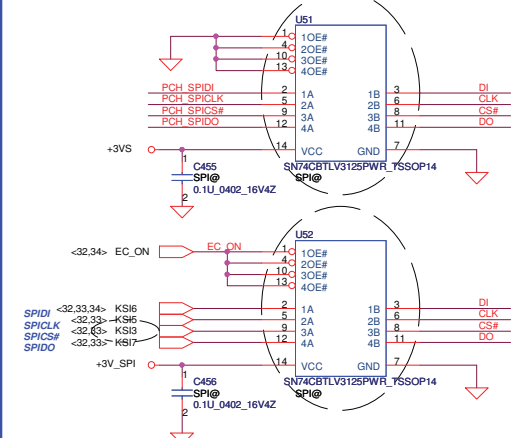


HDA_SDO
ME debug mode, this signal has a weak internal pull down
★Low = Disable (default)
High = Enable (flash descriptor security override)

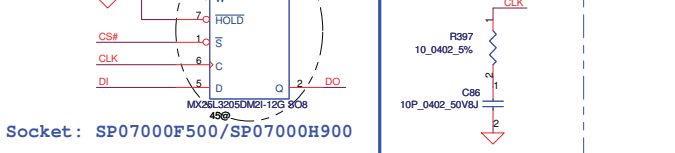
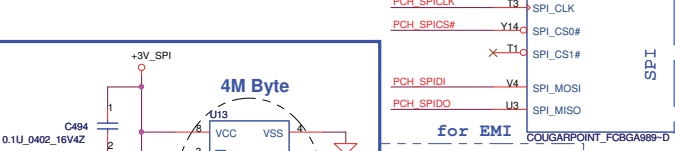
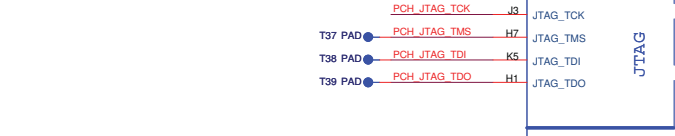
HDA_SYNC
★This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform



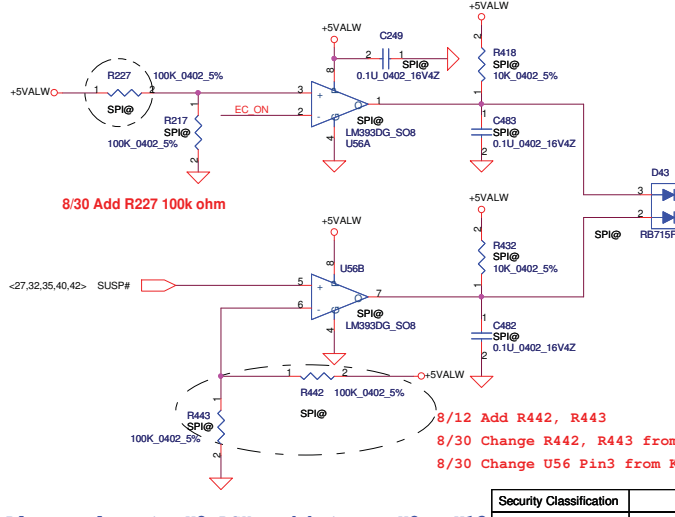
8/ 12 Change R572, R573, R574, R575, R569 from @ to mount



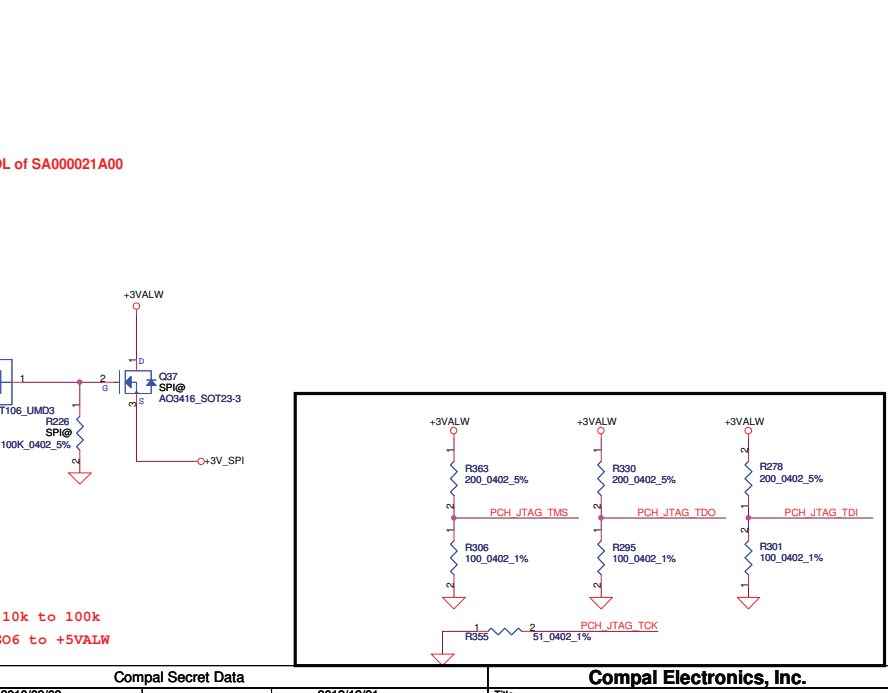
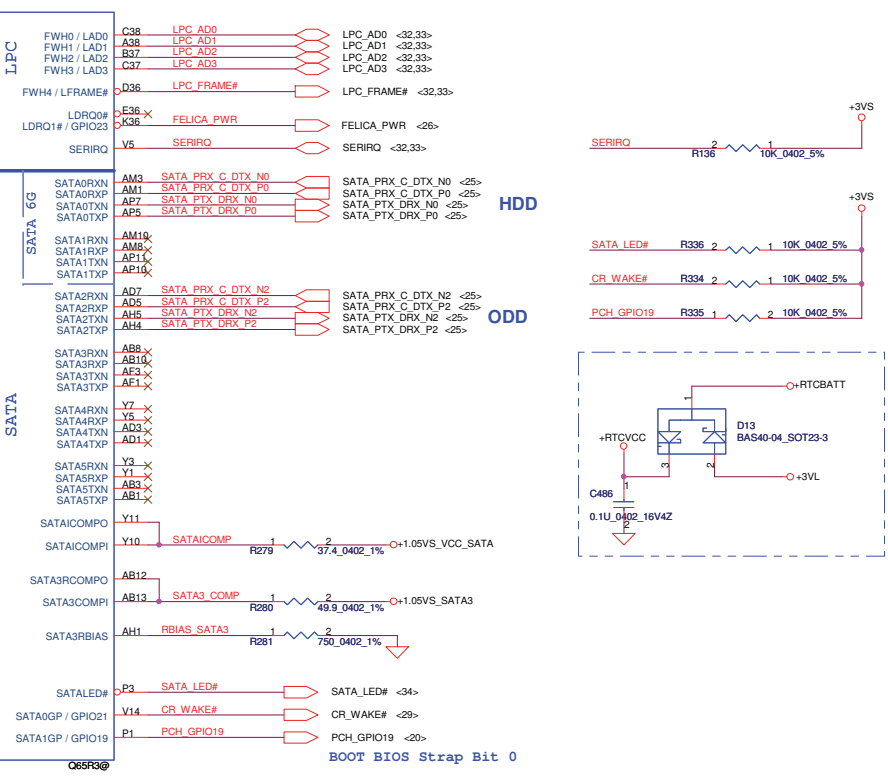
8/30 Change PWRME_CTRL# to HDA_SDO by PCH EDS



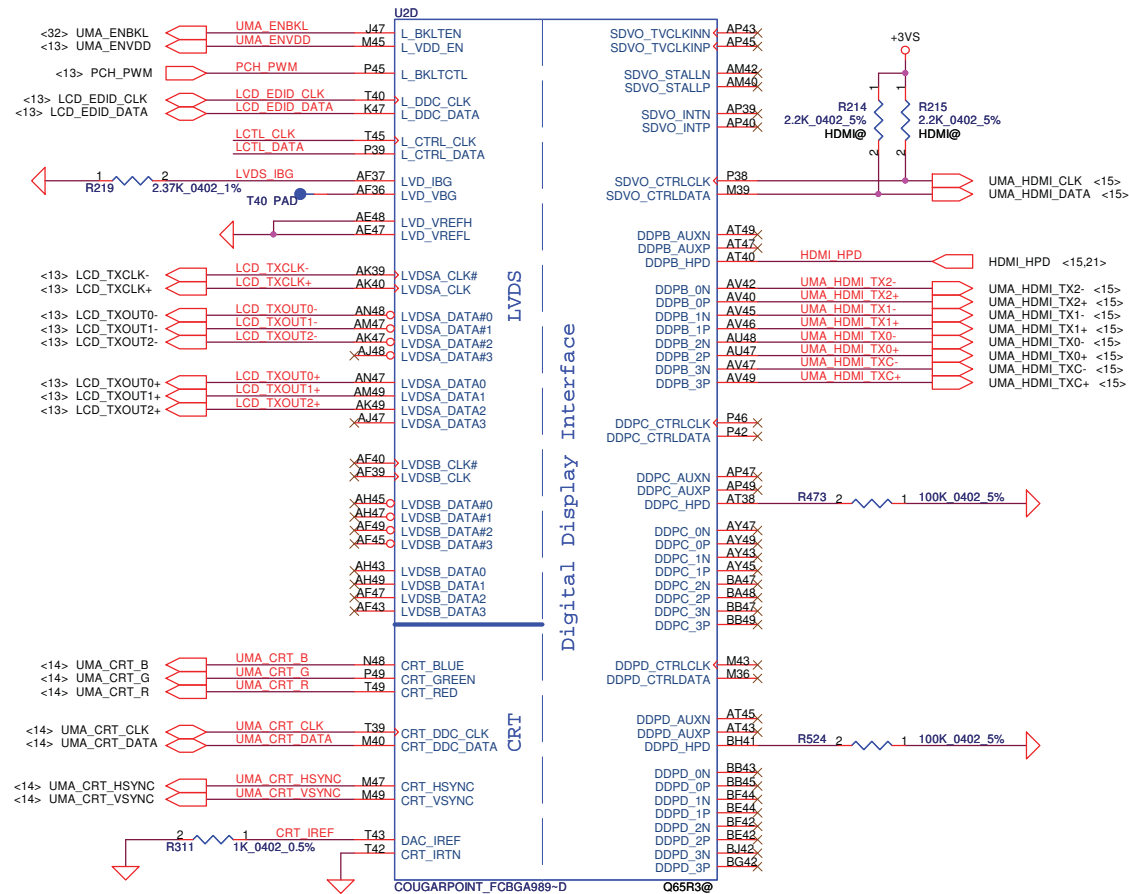
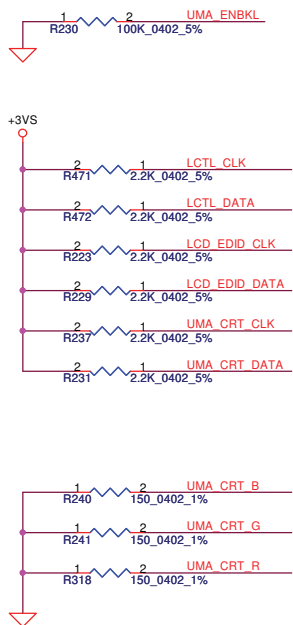
Please close to U2 PCH 8/30 Change U13 from SA000021A00 to SA000031N00 due to EOL of SA000021A00



Please close to U2 PCH, and between U2 & U13

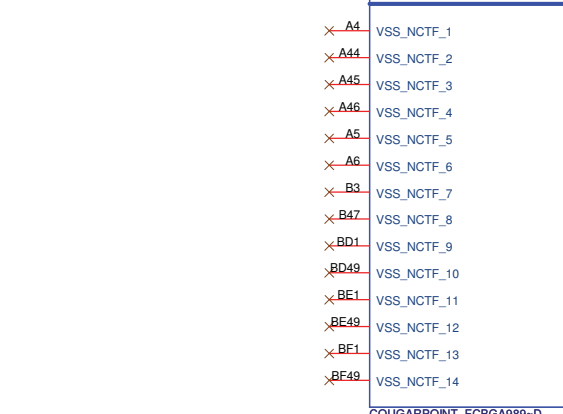
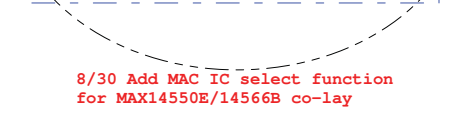
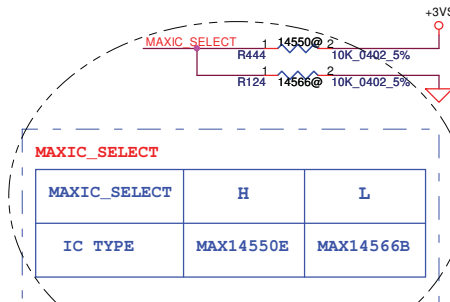
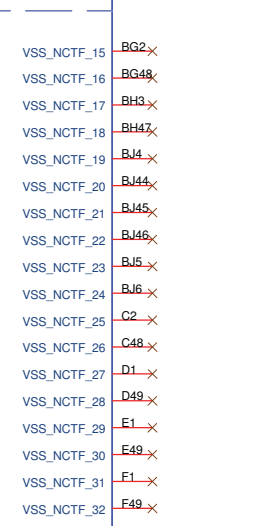
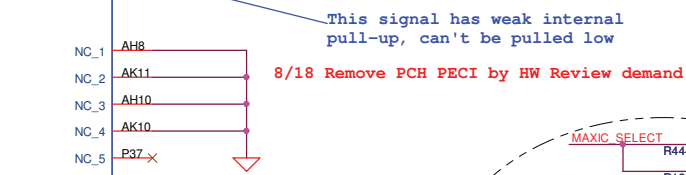
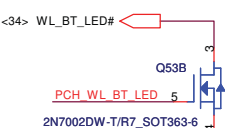
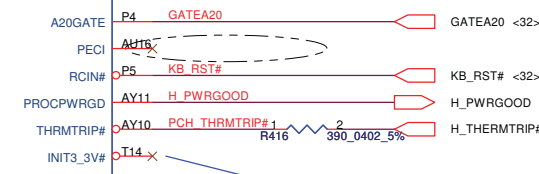
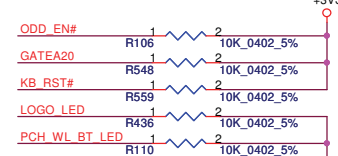
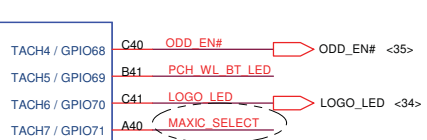
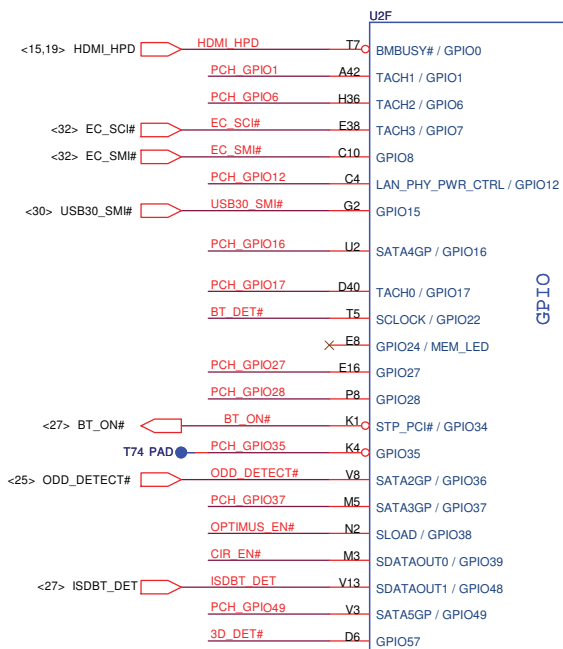
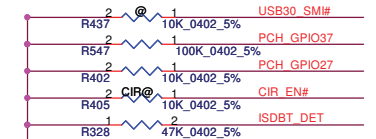
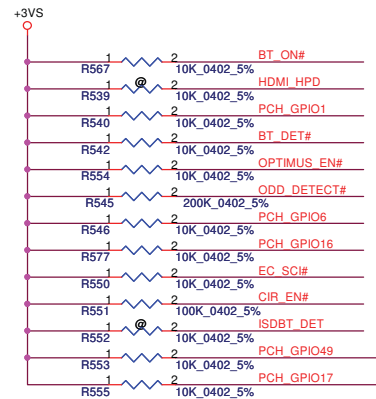
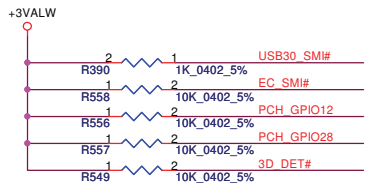


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				Document Number	PHQAA LA-6832P M/B
				Date	Thursday, October 07, 2010
				Sheet	16 of 45

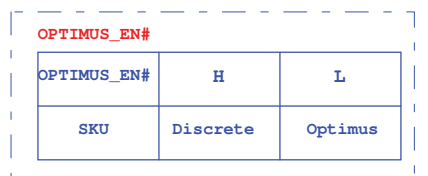
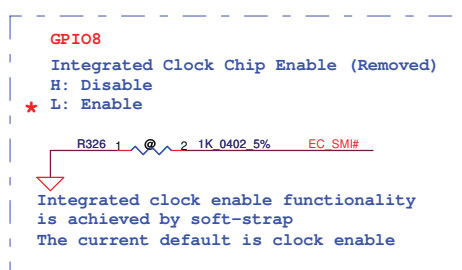
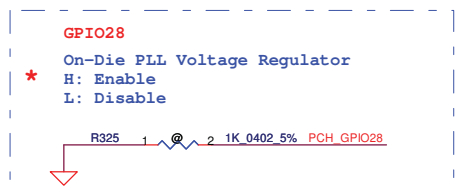


HDMI

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Issued Date				2010/09/03		Deciphered Date		2012/12/31		Title	
										PCH_CRT/LVDS/HDMI	
										PHQAA LA-6832P M/B	
										Date: Thursday, October 07, 2010	
										Sheet 19 of 45	
										Rev 0.2	



COUGARPOINT_FCBGA989-D Q65R3@



OPTIMUS_EN#	H	L
SKU	Discrete	Optimus

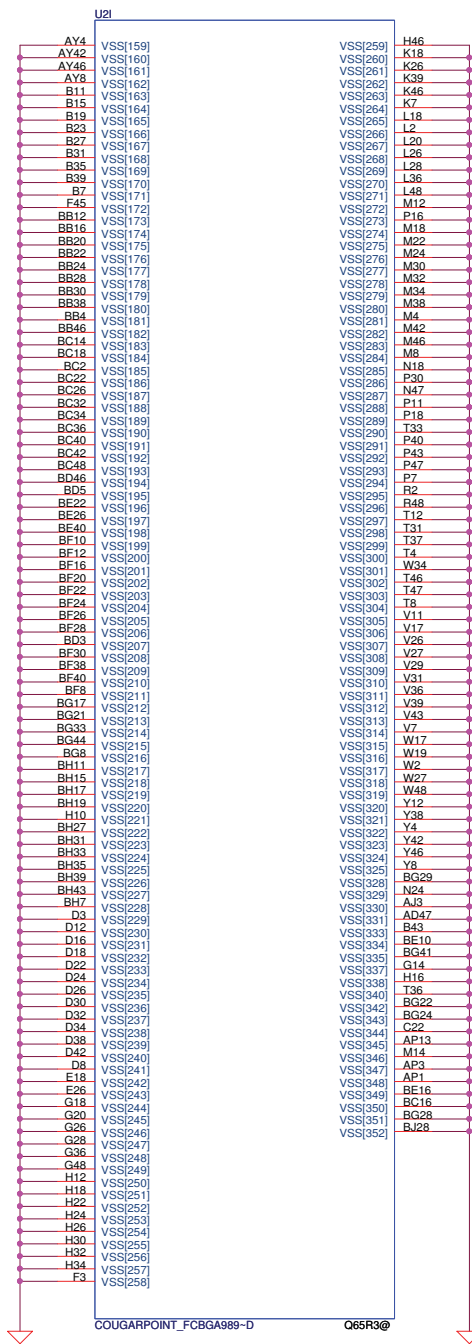
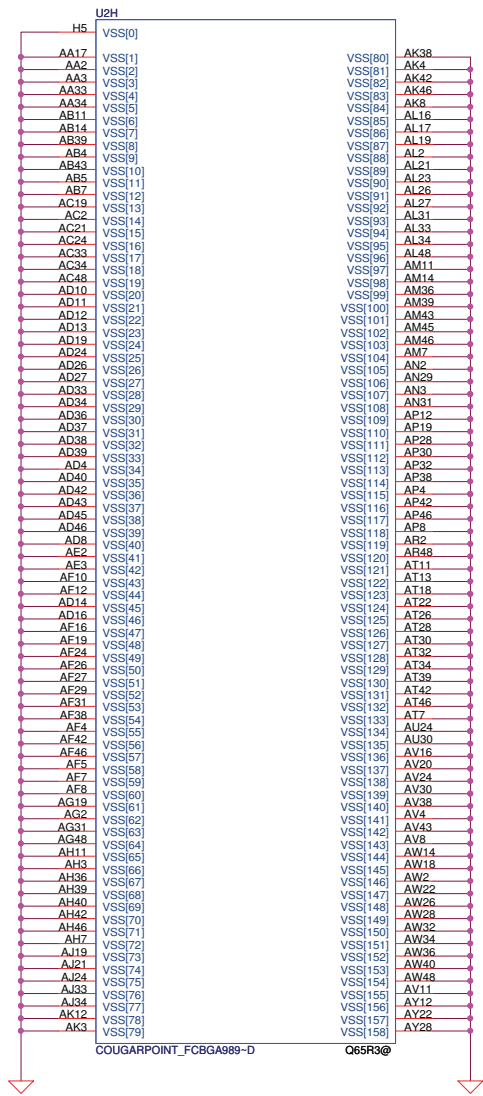
This signal has weak internal pull-up, can't be pulled low
8/18 Remove PCH Peci by HW Review demand

8/30 Add MAC IC select function for MAX14550E/14566B co-lay

9/1 Reserve C896, C897 for ESD request

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				PCH_CPU/GPIO	
				Size B	Document Number
				PHQAA LA-6832P M/B	
				Date	Thursday, October 07, 2010
				Sheet	21 of 45
				Rev	0.2

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Size		Document Number		Rev	
Custom		PHQAA LA-6832P M/B		0.2	
Date:		Thursday, October 07, 2010		Sheet 24 of 45	

Place closely JHDD SATA CONN.

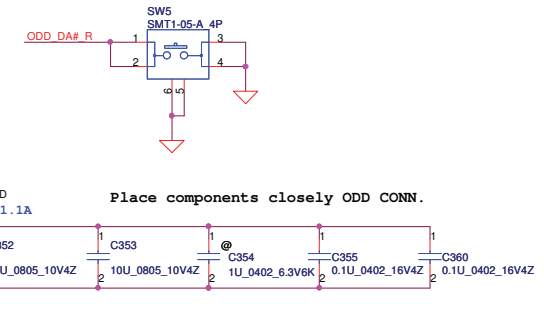
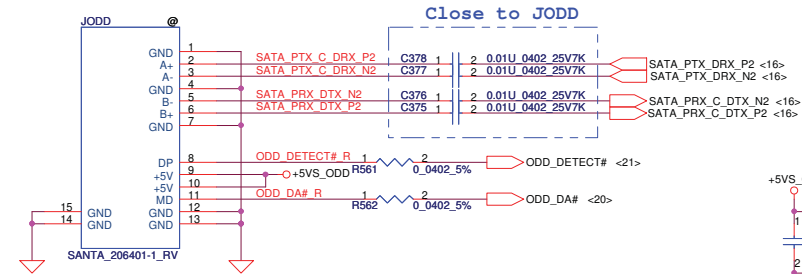
5VS 1.2A

C356 10U_0805_10V4Z

C357 0.1U_0402_16V4Z

C358 0.1U_0402_16V4Z

C359 0.1U_0402_16V4Z



USB Board@ Right Side

Power Section:

- Input: +5VALW, USB_EN#
- IC: U14 RT9715BGS_S08
- Output: +USB_VCCA (2.5A)
- Capacitors: C361 (1000P_0402_50V7K), C362 (4.7U_0805_10V4Z)
- Label: For EMI

Signal Section:

- USB20_P0, USB20_N0, USB20_P1, USB20_N1
- USB_OC#0 <20,32>
- WCM-2012-900T_0805
- Resistors: R75, R87, R77, R53, R88 (0.0402_5%)

Connector Section:

- W=60mils
- Pin 1: +USB_VCCA
- Pin 2: +5VL
- Pin 3: +5VALW
- Pin 4: +5V_IO
- Pin 5: USB20_N1_R
- Pin 6: USB20_P1_R
- Pin 7: USB20_N0_R
- Pin 8: USB20_P0_R
- Pin 9: <31> HP_L
- Pin 10: <31> HP_L
- Pin 11: <31> MIC1_L
- Pin 12: <31> MIC1_R
- Pin 13: <31> NBA_PLUG
- Pin 14: <31> BACK_SENSE
- Pin 15: J10
- Pin 16: ACES_85201-2005N

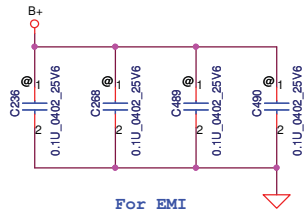
Notes:

- 10/04 Swap USB20_P0, USB20_N0, USB20_P1, USB20_N1 for layout request

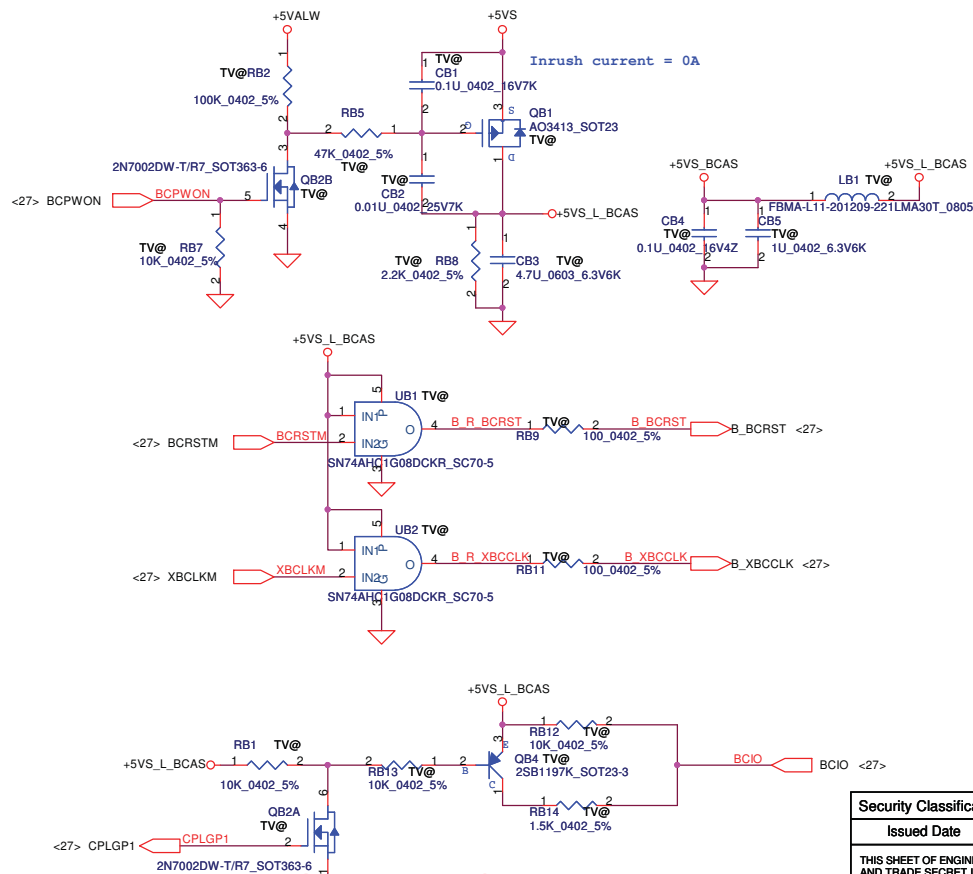
The schematic diagram illustrates a USB-to-serial converter circuit. At the top, a USB connector (USB) is connected to a USB-to-serial converter IC (PJDLC05C_SOT23-3). The IC is connected to a serial-to-USB IC (AC03413_SOT23). The serial-to-USB IC is connected to a USB connector (USB) and a USB-to-serial converter IC (PJDLC05C_SOT23-3). The circuit also includes a USB-to-serial converter IC (PJDLC05C_SOT23-3) and a USB-to-serial converter IC (PJDLC05C_SOT23-3).

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				PHQAA LA-6832P M/B		0.2
Date:				Thursday, October 07, 2010	Sheet	25 of 45

Screw cap for ESD request

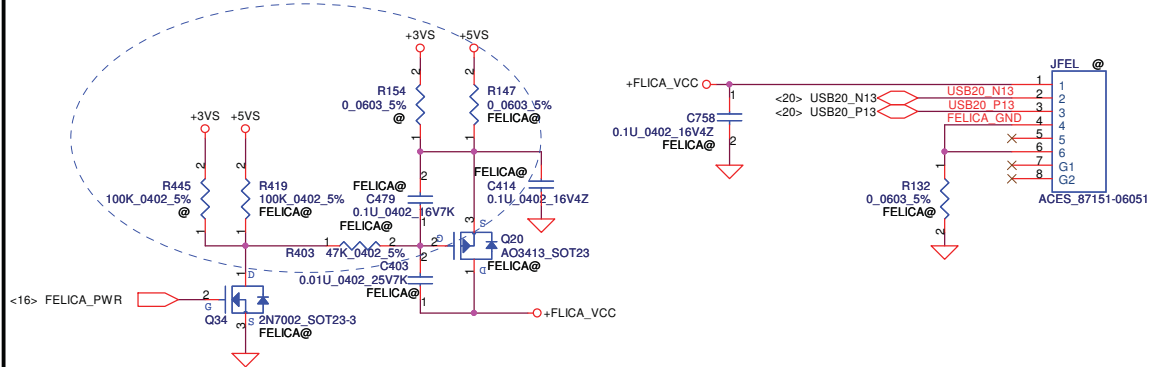


B-CAS Circuit

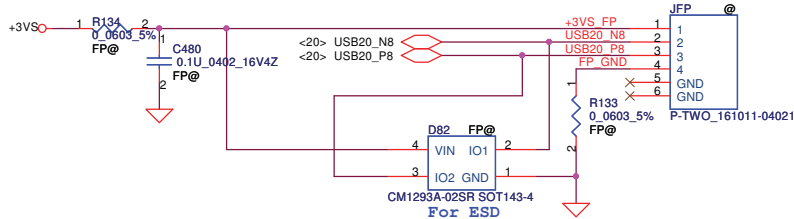


Felica

Reserve +3VS Felica by Customer demand.
2010/09/27



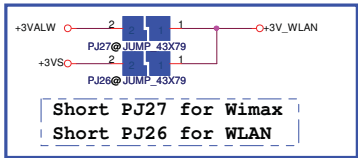
Finger printer



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		Size	Document Number						Rev
			PHQAA LA-6832P M/B						0.2
		Date:	Thursday, October 07, 2010			Sheet	26	of	45

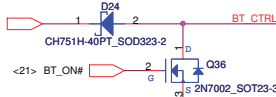
Slot 1 Half PCIe Mini Card-WLAN/ WiMax



WLAN+BT Combo module circuits

	BT on module	BT on module
	Enable	Disable
BT_CTRL	H	L
BT_ON#	L	H

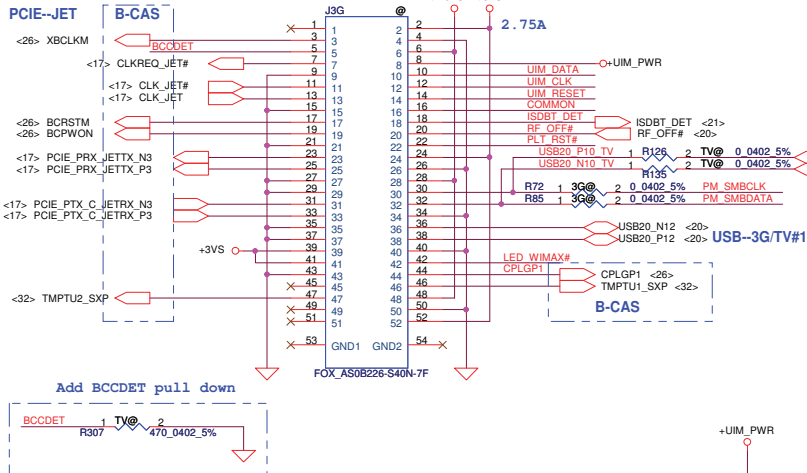
**If +3V_WLAN is +3VS, please remove D24



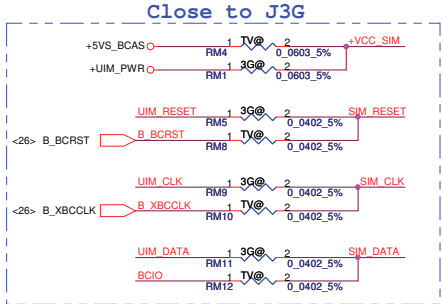
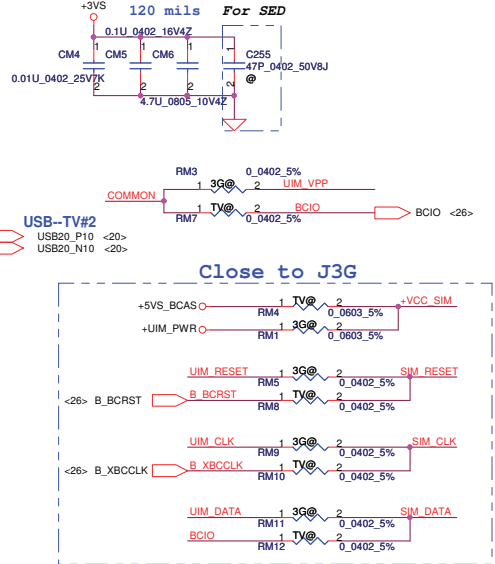
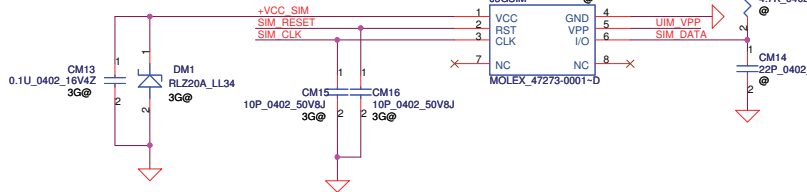
For isolate Intel Rainbow Peak and Compal Debug Card.

8/30 Reserve R1443 for WLAN Mini PCIe Card Pin5

Slot 2 Full PCIe Mini Card- 3G/ TV Tuner
Half PCIe Mini Card- JET



Add BCCDET pull down

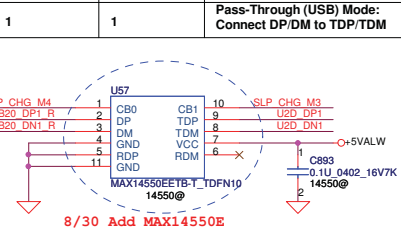
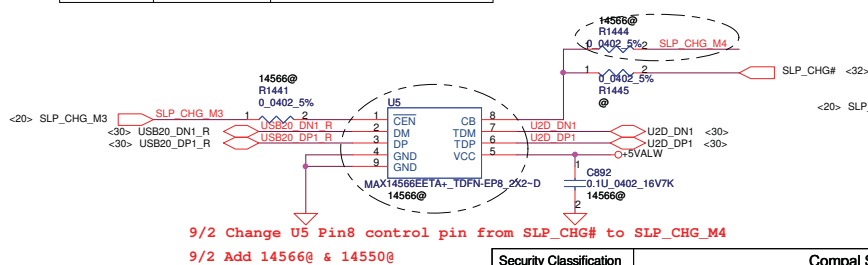
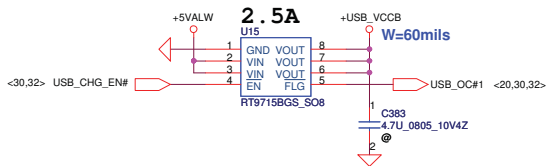


USB Sleep & Charge
Auto-Mode
Mode3/Mode4

MAX14566B		
CB0 SLP_CHG#	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14566E	
CB: SLP_CHG#	STATUS
0	AUTO MODE
1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

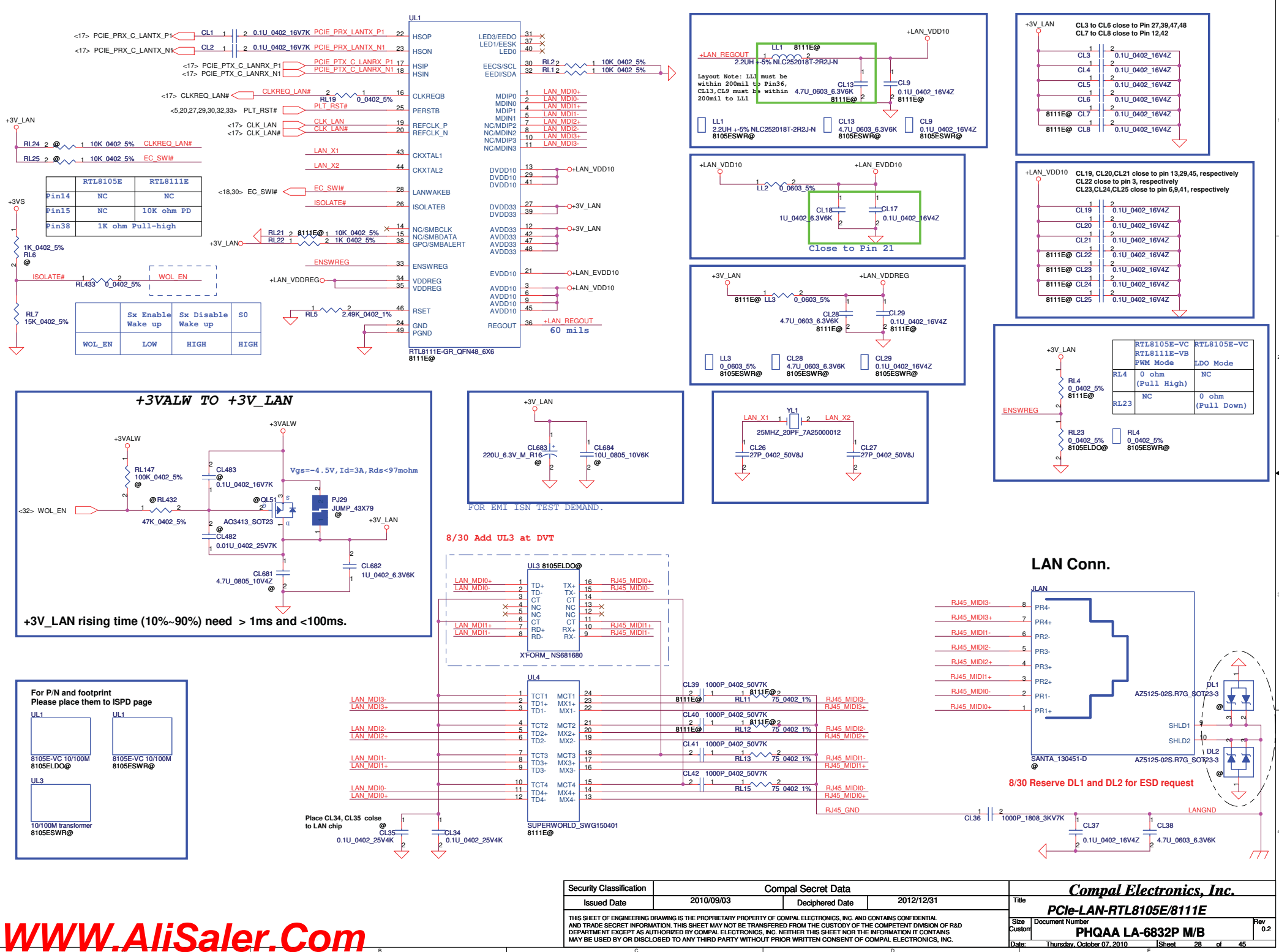
MAX14550E		
CB0 SLP_CHG_M4	CB1 SLP_CHG_M4	STATUS
0	0	AUTO MODE
0	1	MODE3
1	0	MODE4
1	1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM



9/2 Change U5 Pin8 control pin from SLP_CHG# to SLP_CHG_M4
9/2 Add 14566@ & 14550@

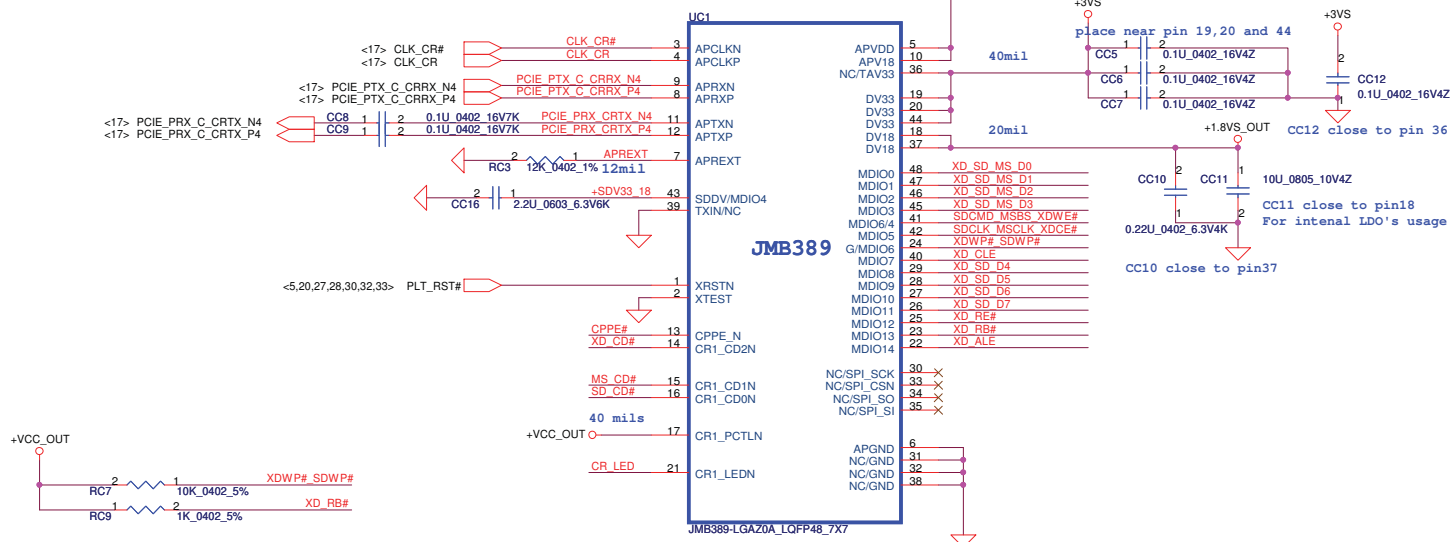
8/30 Add MAX14550E

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				PHQAA LA-6832P M/B	
				Date	Thursday, October 07, 2010
				Sheet	27 of 45



CC16 close to pin43
For internal LDO in SD3.0

JMB389C

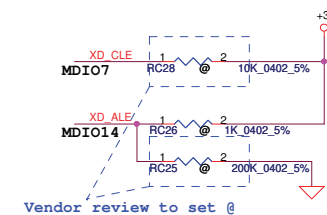


D3E mode



Power On Strapping setting

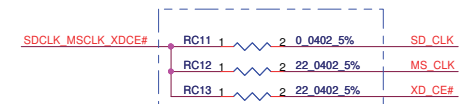
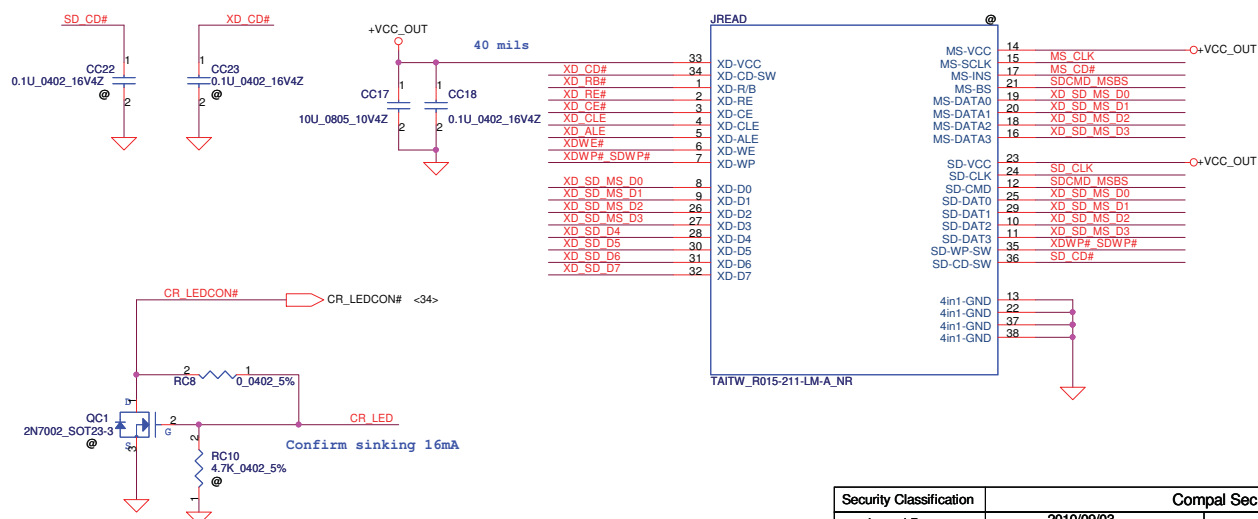
Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO14	CR_LED high active	CR_LED low active★



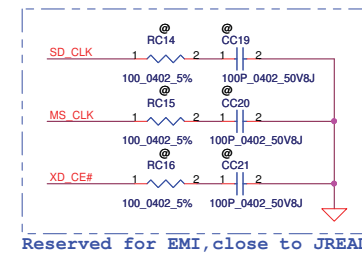
Add RC24 and RC17 close to UC1 for xD issue



5 in 1 Card Reader



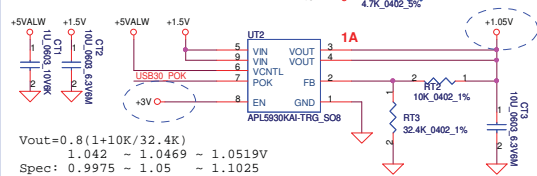
Reserved for EMI,close to UC1.42



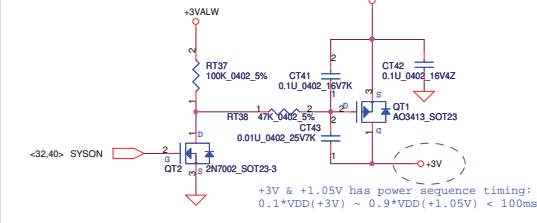
Reserved for EMI,close to JREAD

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Compal Electronics, Inc.				Document Number
PCle-CardReader JMB389				PHQAA LA-6832P M/B
Date: Thursday, October 07, 2010				Rev 0.2
Sheet 29 of 45				

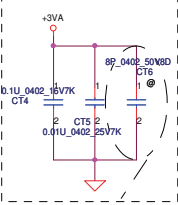
+1.5V to +1.05V Transfer



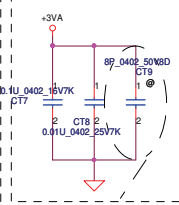
+3VALW to +3V Transfer



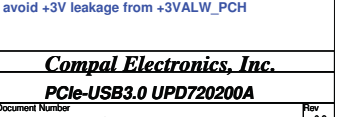
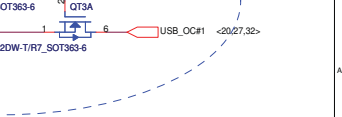
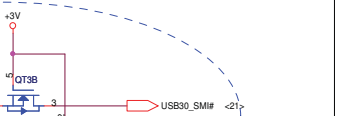
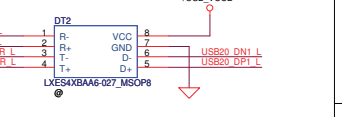
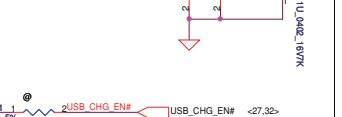
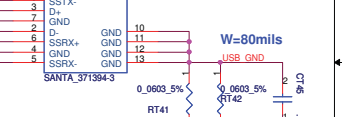
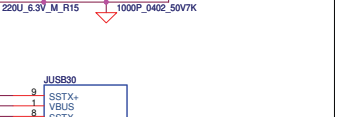
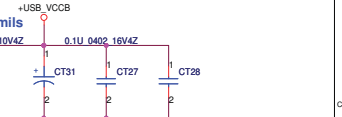
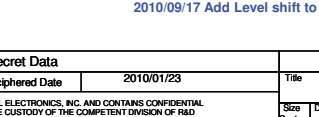
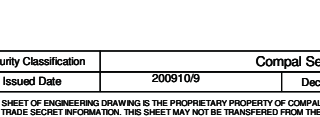
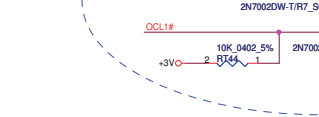
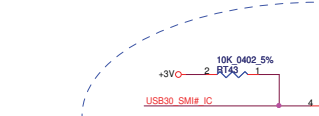
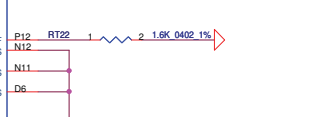
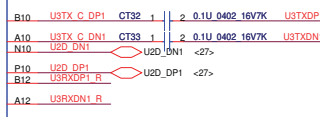
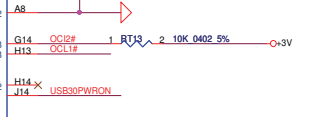
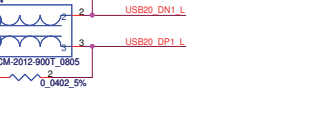
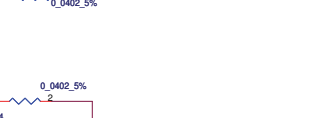
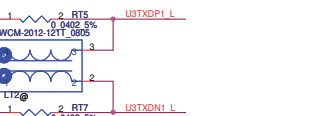
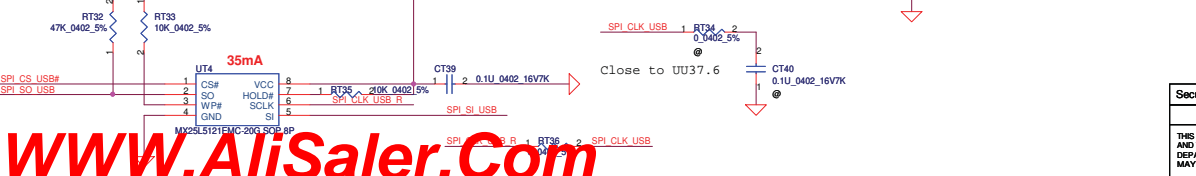
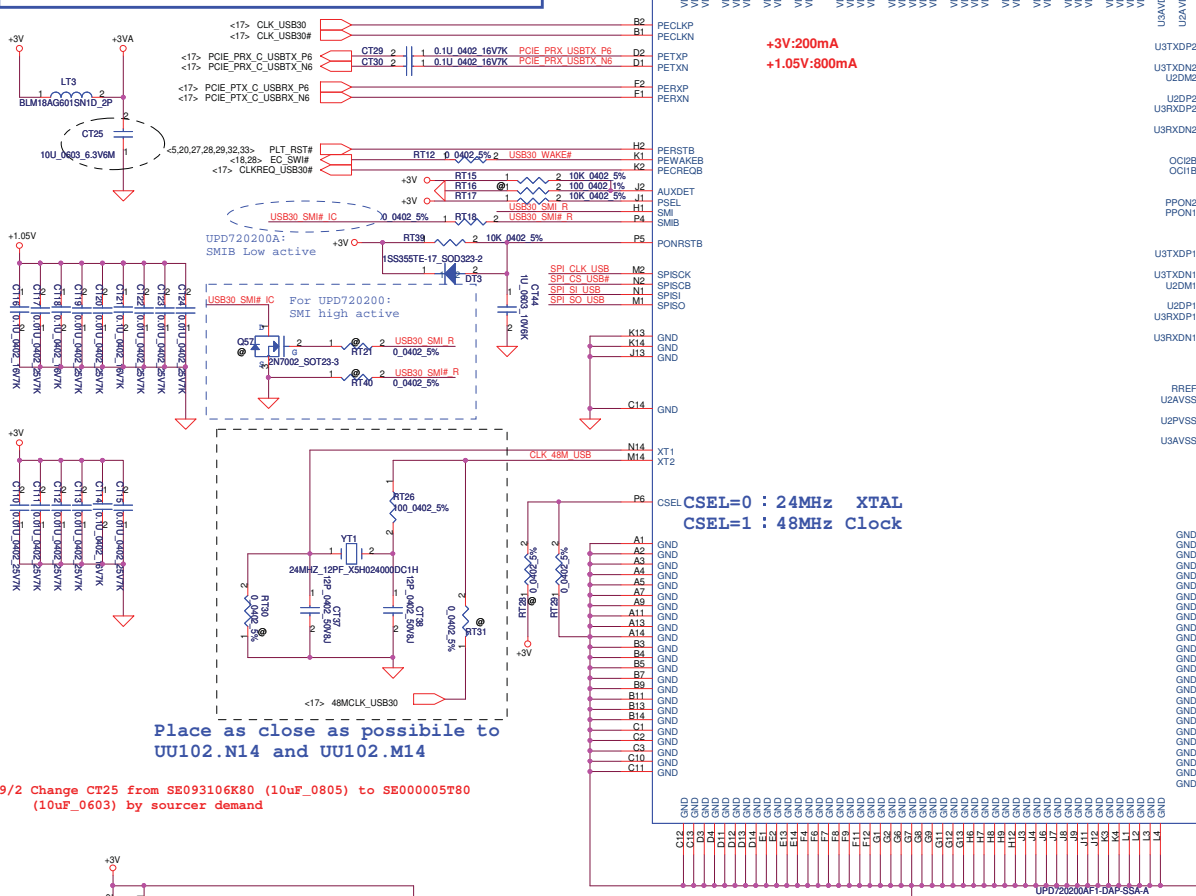
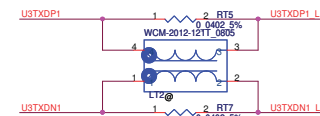
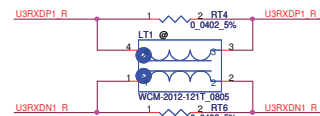
Close to U102.D7



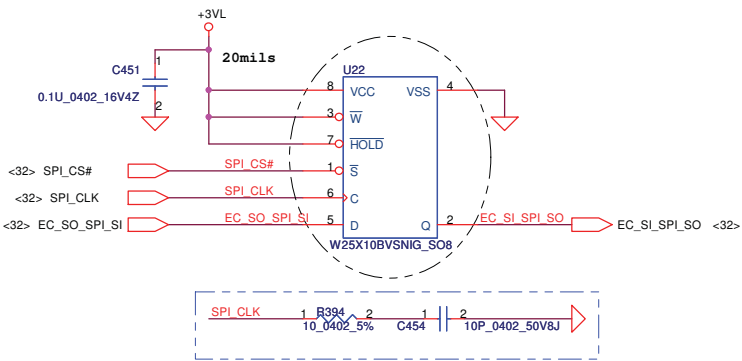
Close to U102.P13



Follow Vendor recommend.



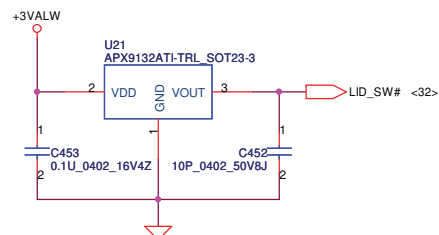
SPI Flash (256KB)



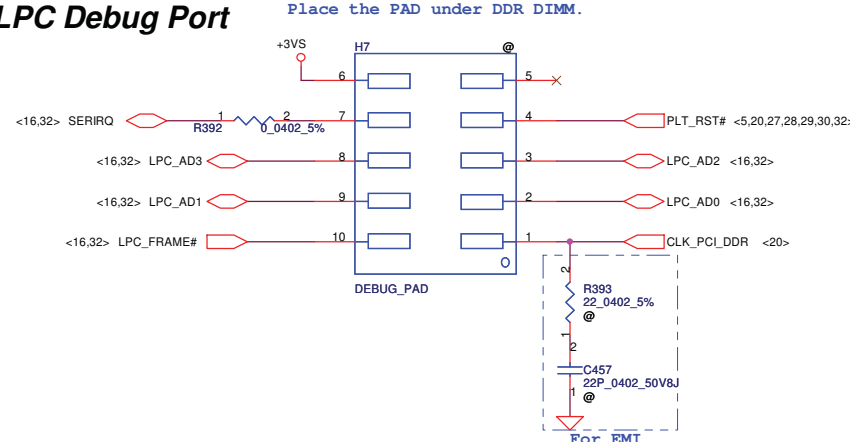
8/30 Change U22 From SA00003GK00 to SA00003GM10 due to EOL of SA00003GK00

9/03 Change U22 change to SA00003FL10

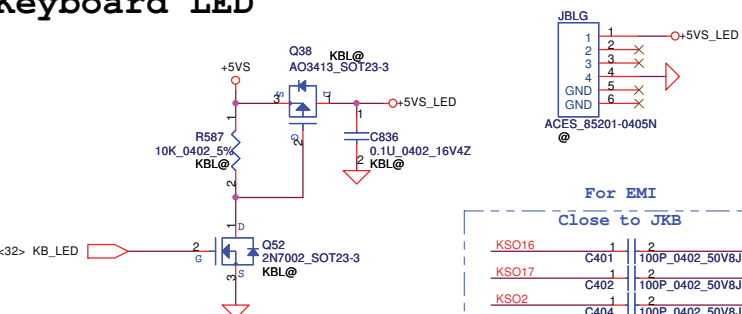
Lid SW



LPC Debug Port



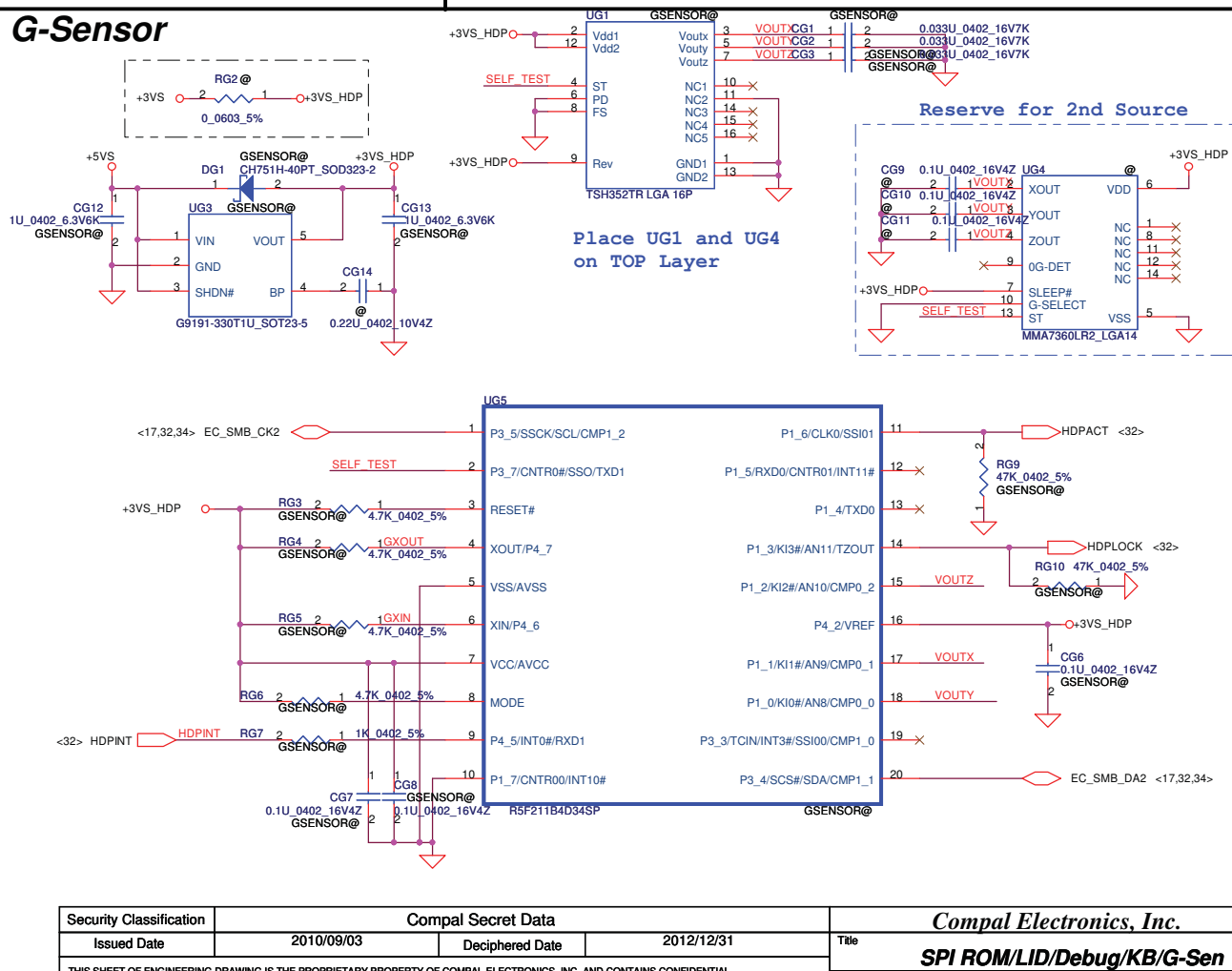
Keyboard LED



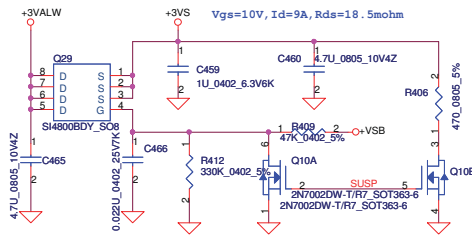
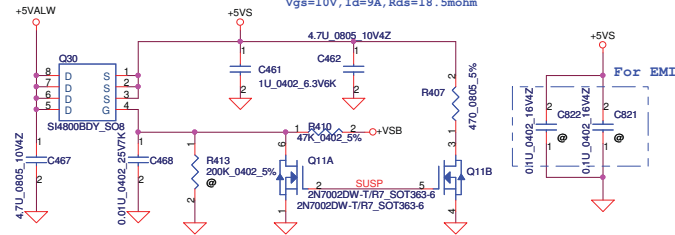
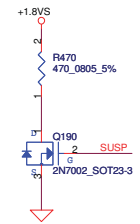
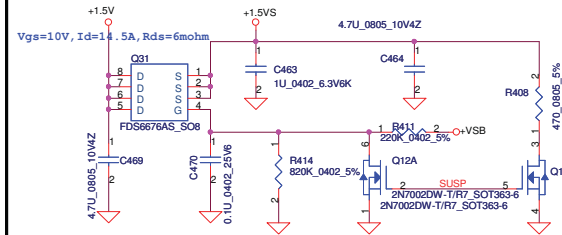
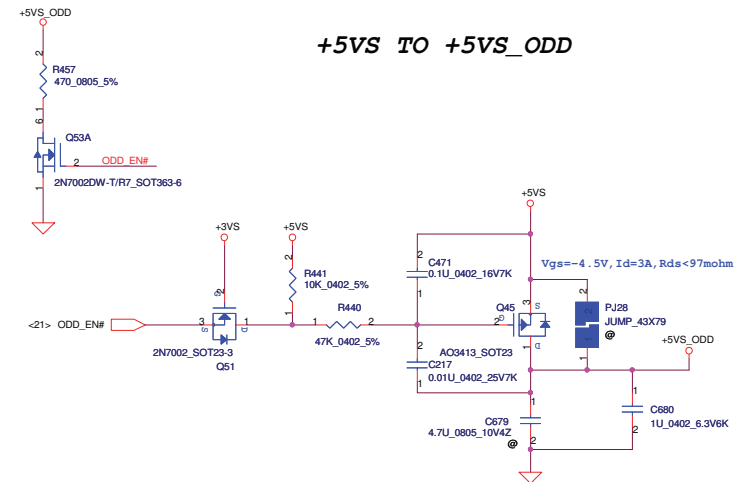
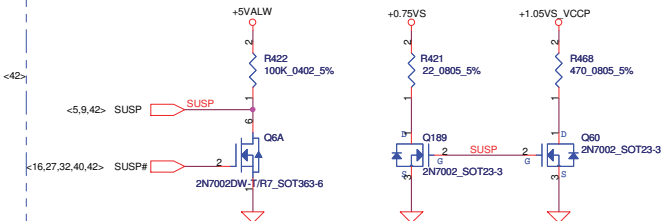
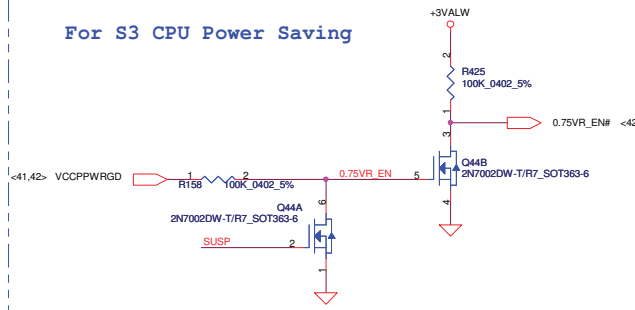
KEYBOARD CONN.



G-Sensor

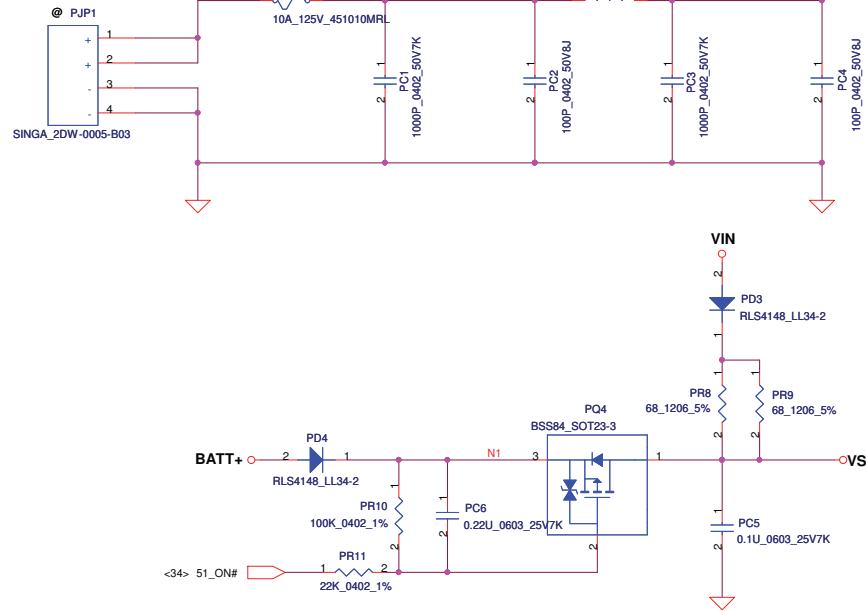


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				Date:	Thursday, October 07, 2010
				Sheet	33 of 45

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				DC-DC INTERFACE	
				Size Document Number	
				PHQAA LA-6832P M/B	
				Rev 0.2	
Date:				Thursday, October 07, 2010	
				Sheet 35 of 45	

DC301001M80



+3VALWP @ PJ332
JUMP_43X118
(5A,200mils ,Via NO.= 10)
OCP=8.6A

+0.75VSP @ PJ76
JUMP_43X79
(1A,40mils ,Via NO.= 2)

+5VALWP @ PJ352
JUMP_43X118
(5A,200mils ,Via NO.= 10)
OCP=7.9A

+VCCSAP @ PJ452
JUMP_43X118
(6A,240mils ,Via NO.= 12)

+1.8VSP @ PJ182
JUMP_43X118
(1.65A,70mils ,Via NO.= 4)
OCP=4.2A

+3VLP @ PJ333
JUMP_43X39
(100mA,40mils ,Via NO.= 2)

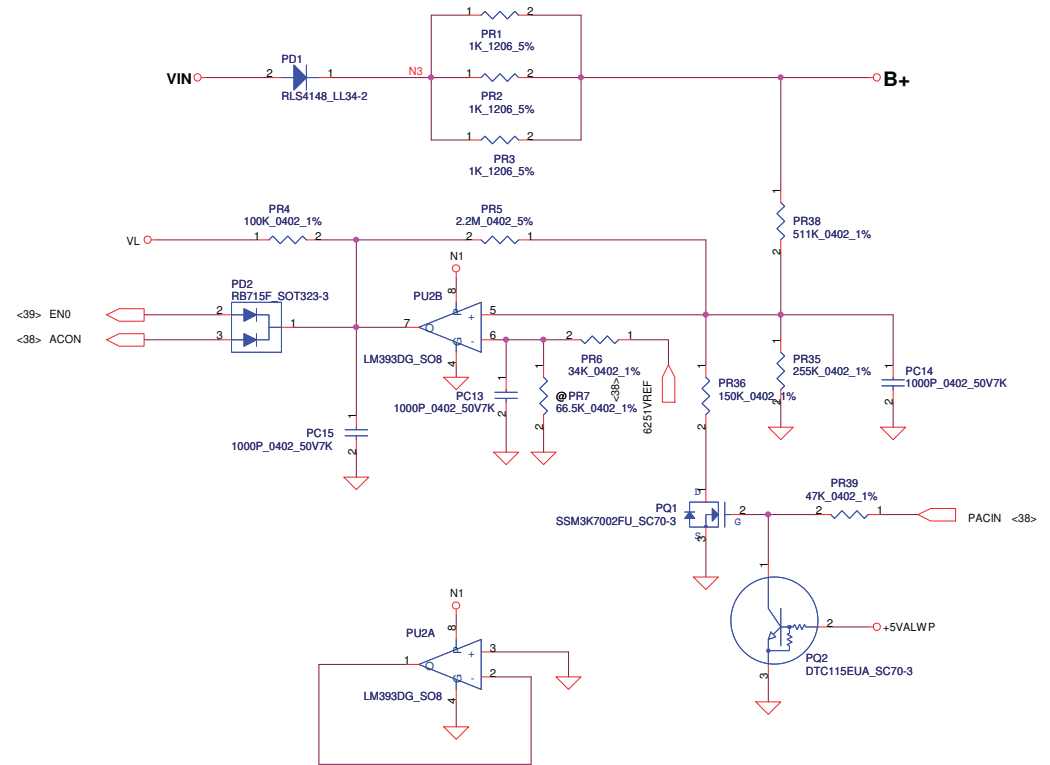
+VSBP @ PJ2
JUMP_43X39
(120mA,40mils ,Via NO.= 1)

VL @ PJ353
JUMP_43X39
(100mA,40mils ,Via NO.= 2)

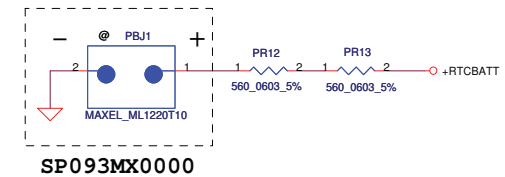
+1.5VP @ PJ152
JUMP_43X118
(16A,640mils ,Via NO.= 32)

+1.05VS_VCCPP @ PJ402
JUMP_43X118
+1.05VS_VCCP @ PJ403
JUMP_43X118
(17A,680mils ,Via NO.=34)

+GFX_COREP @ PJ502
JUMP_43X118
+GFX_CORE @ PJ503
JUMP_43X118
(33A,1320mils ,Via NO.=66)
OCP=40A



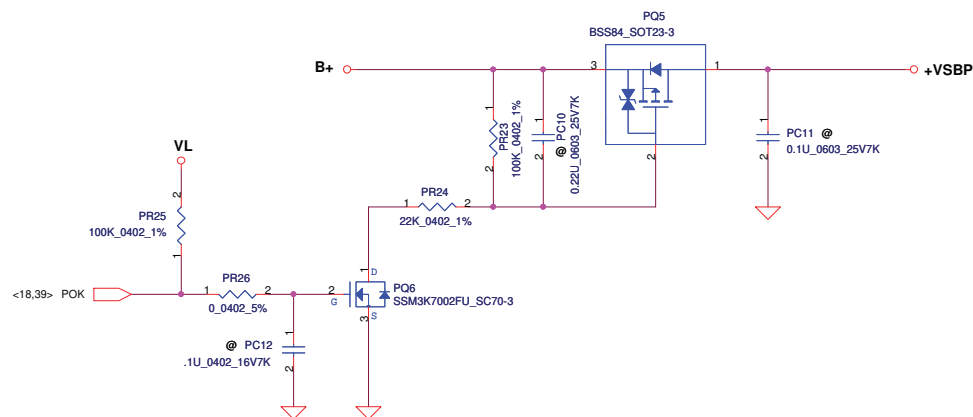
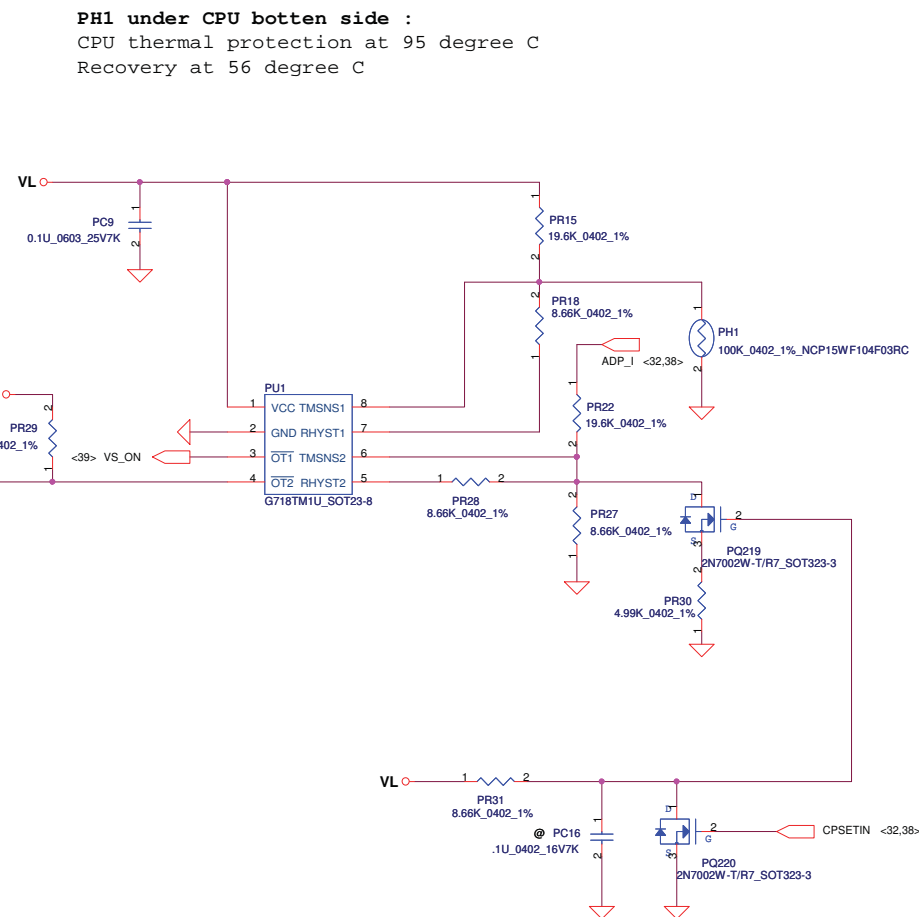
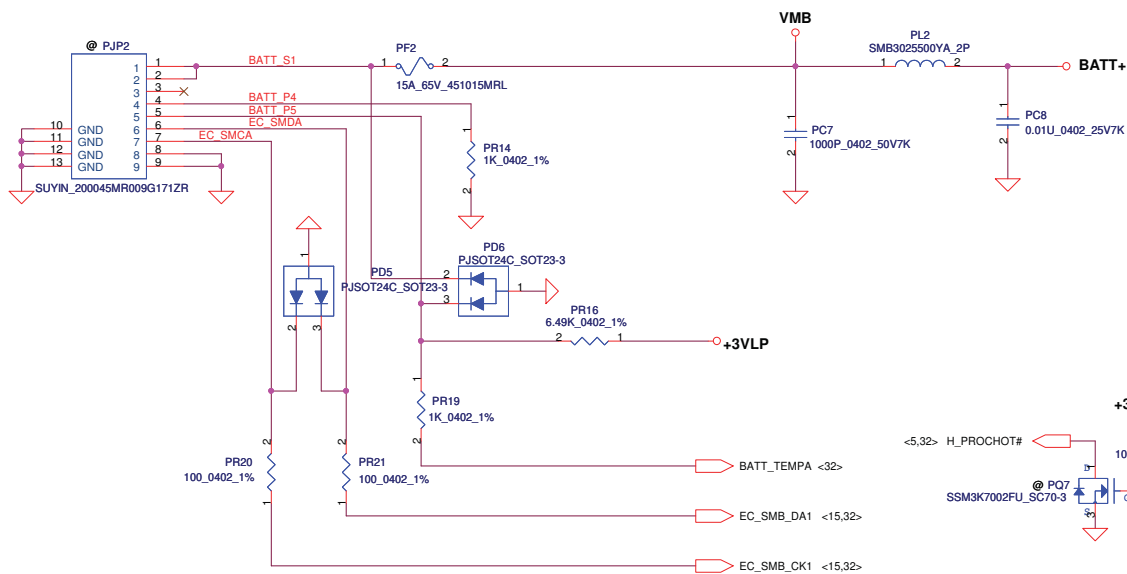
RTC Battery



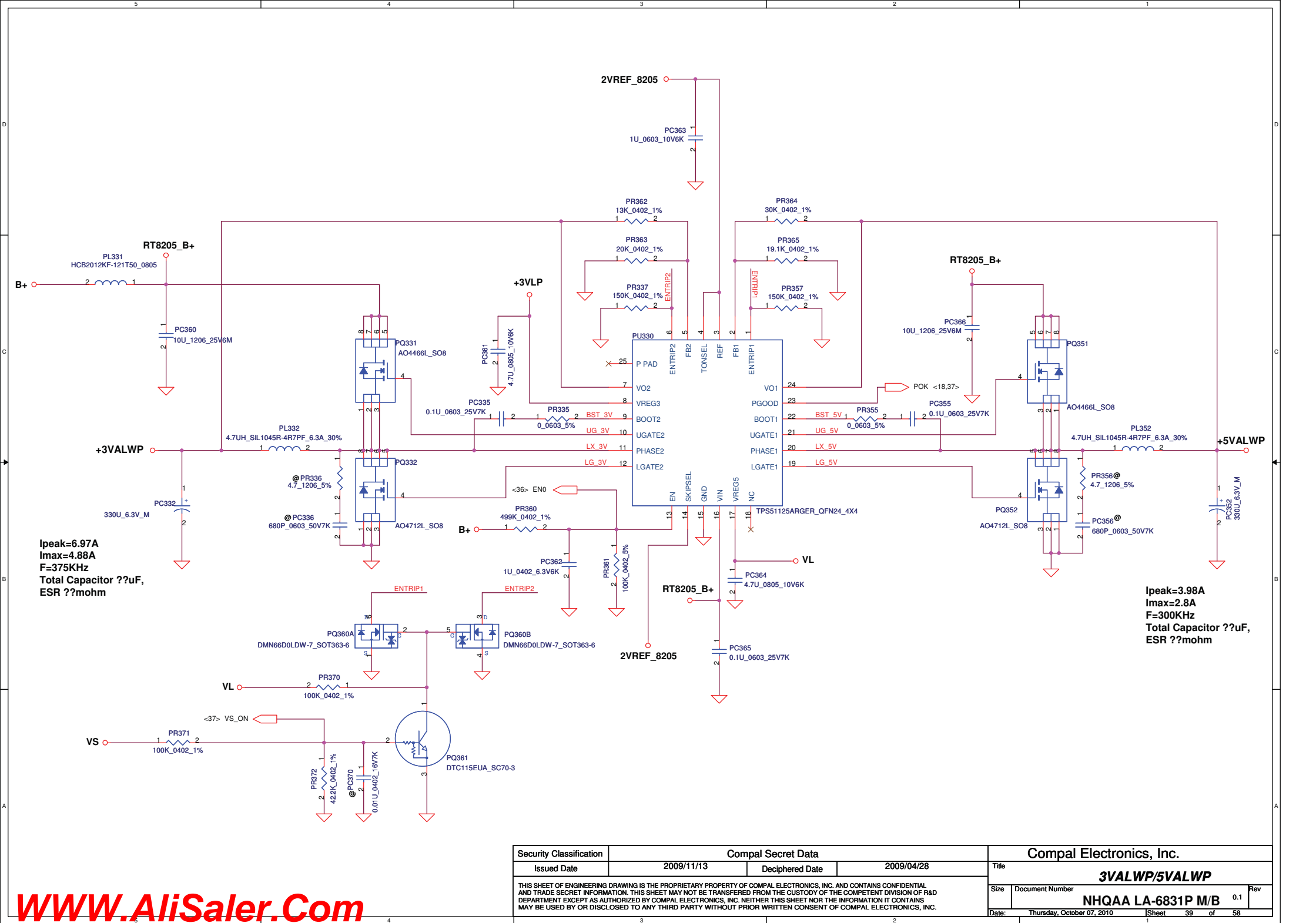
ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

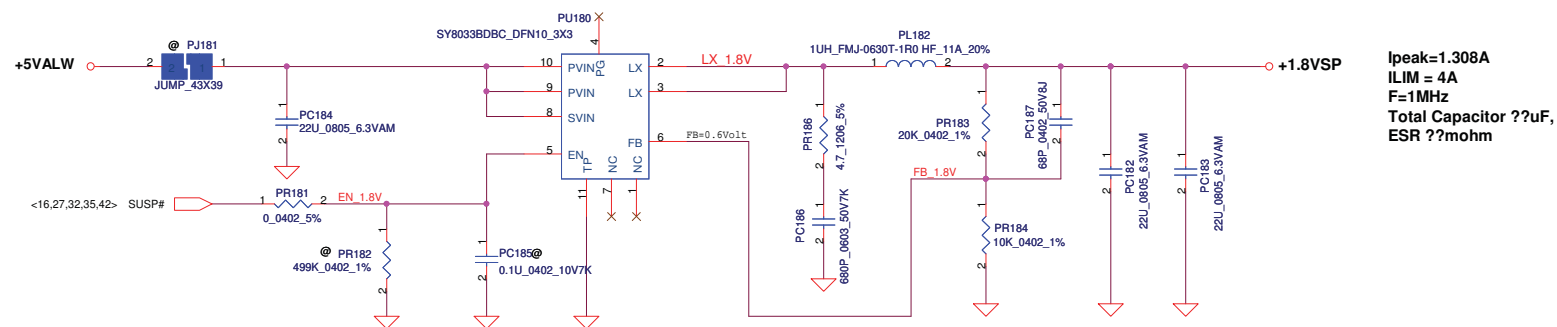
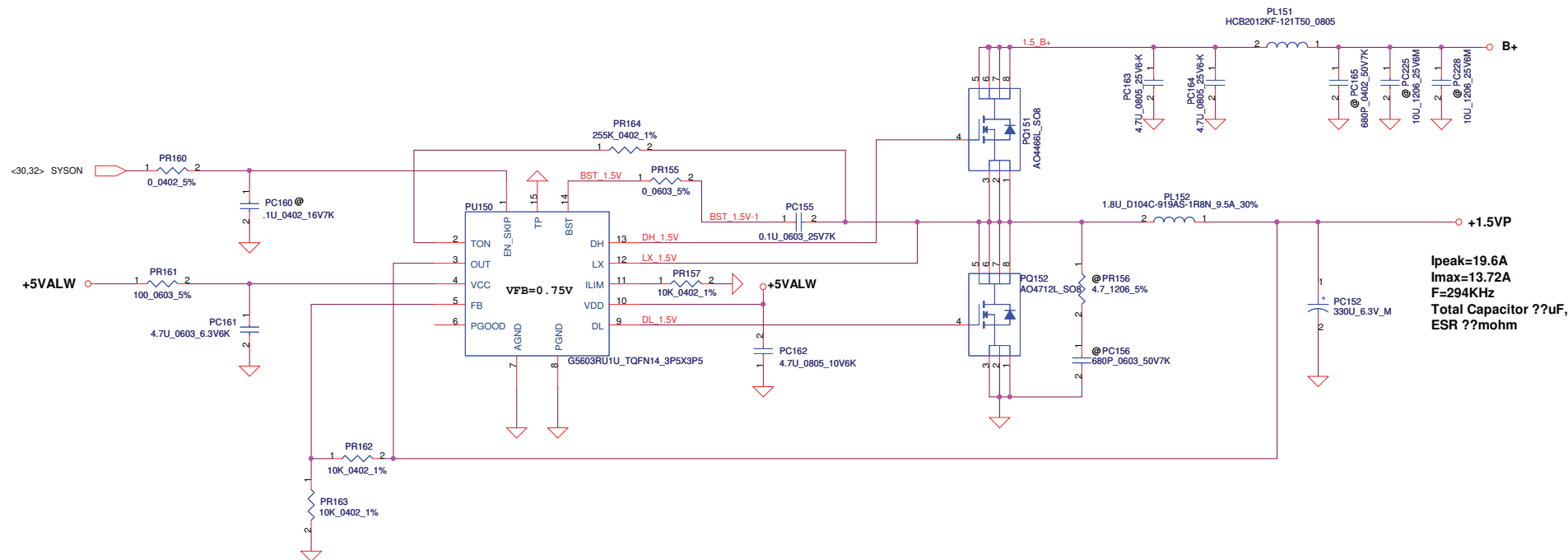
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Issued Date	2009/11/13	Deciphered Date	2009/04/28	Title	
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				Date:	Thursday, October 07, 2010
				Sheet	36 of 58



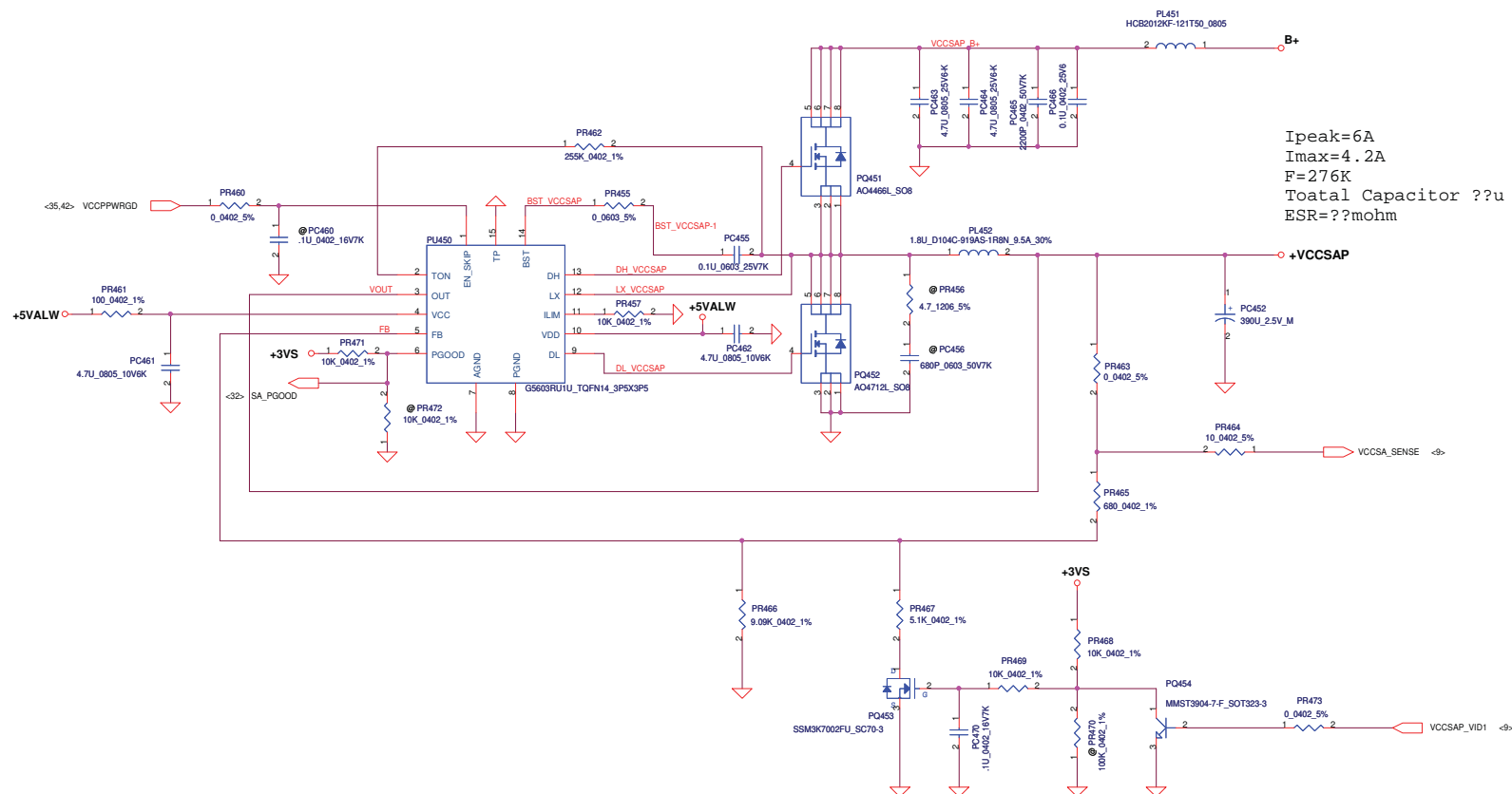
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Issued Date	2009/11/13	Deciphered Date	2009/04/28	Title	
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				Date:	Thursday, October 07, 2010
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Size	Document Number	NHQAA LA-6831P M/B		0.1	Rev
Date:	Thursday, October 07, 2010	Sheet	39	of 58	

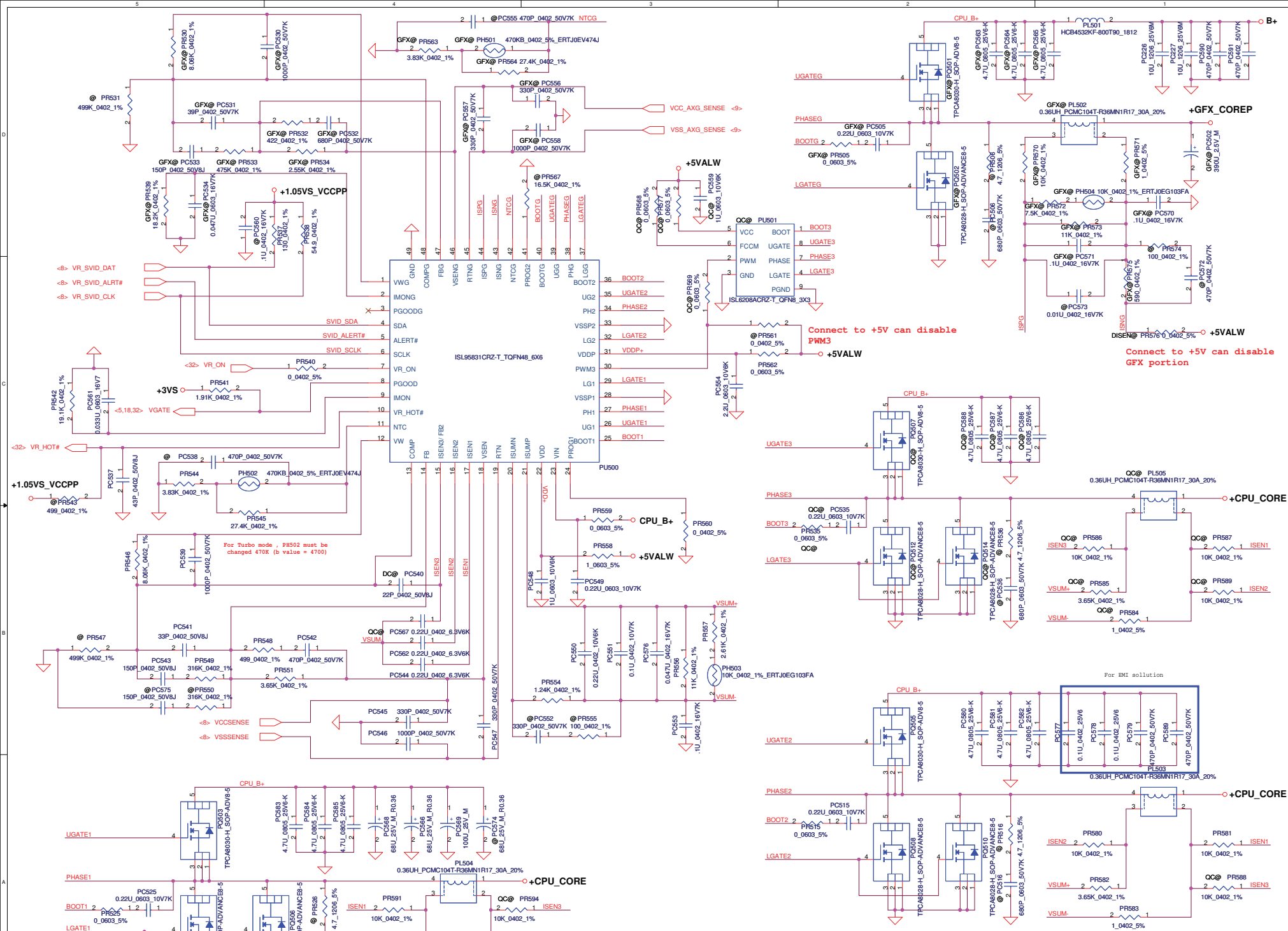


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				Custom	NHQA LA-6831P M/B
				Date:	Thursday, October 07, 2010
				Sheet	40 of 58



Ipeak=6A
Imax=4.2A
F=276K
Toatal Capacitor ??u
ESR=??mohm

VID1	+VCCSAP
1	0.8V
0	0.9V



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Date	Thursday, October 07, 2010	Sheet	43	of	58

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	2010/09/07	P37-PWR_BATTERY CONN / OTP	Remove PQ7 SSM3K7002FU	Adapter protect circuit not ready
2.	2010/09/07	P40-PWR-+1.5VP/+1.8VSP	Change PQ152 to AO4712L	Use same part number
3.	2010/09/07	P41-PWR_+VCCSAP	Change PQ452 to AO4712L	Use same part number
4.	2010/09/07	P40-PWR-+1.5VP/+1.8VSP	Change PQ151 to AO446L	Use same part number
5.	2010/09/07	P53-PWR_+VCCSAP	Change PQ451 to AO446L	Use same part number
6.	2010/09/07	P50-PWR-CHARGER	Change PQ201,PQ202 to AO4466L	Use same part number
7.	2010/09/07	P50-PWR-CHARGER	Change PQ203 to AO4435L and remove PQ207	For UMA SKU
8.	2010/09/07	P50-PWR-CHARGER	Add PR234 12.4k	For DC and QC CP setting
9.	2010/09/07	P55-PWR-CPU_CORE/GFX	Add PR560 0 Ohm	Set CPU VBOOT to 0V
10.	2010/09/07	P50-PWR-CHARGER	Add PR222 24k and PR223 20k	For CP setting
11.	2010/09/07	P55-PWR-CPU_CORE/GFX	Add PR544 3.83k,PR545 27.4k,PH502 470k	Add CPU NTC NET
12.	2010/09/07	P55-PWR-CPU_CORE/GFX	Change PR551 from 3.83k to 3.65k	For CPU_CORE load line
12.	2010/09/07	P55-PWR-CPU_CORE/GFX	Change PC550 0.33u to 0.22u and add PC551 0.1u	For shortage issue

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								Size	Document Number						Rev
									NHQAA LA-6831P M/B						0.1
								Date:	Thursday, October 07, 2010			Sheet	44	of	58

HW PIR (Product Improve Record)

NWQAA LA-6832P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1

GERBER-OUT DATE: 2010/09/03

NO DATE PAGE MODIFICATION LIST

PURPOSE

Item	Date	Page	Component	Solution	Request
1)	07/21		Delete	308,DHDMI8,DI88,EDP8,NO3D8,OPT8,UMA8	For low cost Huron River
2)	08/11		Update	room	
3)	08/11	09	Change	R119 change to 8	
4)	08/12	16	Add	R442, R443	For SPI debug circuit
5)	08/12	16	Change	R572, R573, R574, R575, R569 from 8 to mount	For SPI debug circuit
6)	08/12	20	Remove	USB20_P3/N3 from PCH	Don't need USB20/30 BTO
7)	08/12	30	Remove	DT1, USB20, RT14, RT20, RT23, RT24	Don't need USB20/30 BTO
8)	08/12	32	Change	C449, C450, Y4 from 8 to mount	
9)	08/13	15	Change	L8, L9 L10, L11 from SM070001600 to SM070001310	For EMI demand
10)	08/13	30	Change	RT11 to 8	
11)	08/13	30	Change	RT19 to USB308	
12)	08/13	30	Change	CT3 from SE0000005TN0 to SE0000005T80	
13)	08/13	30	Remove	RT25, RT27	Don't need USB20/30 BTO
14)	08/17	5	Remove	R14	For HW Review demand
15)	08/18	6	Reserve	R33	For HW Review demand
16)	08/18	9	Reserve	R119	To follow CRB 1.0
17)	08/18	11	Remove	R32, R89	For HW Review demand
18)	08/18	12	Remove	R35, R97	For HW Review demand
19)	08/18	26	Reserve	C236, C268, C490	For HW Review demand
20)	08/18	15	Remove	R435, R438, R453(0 ohm)	
21)	08/18	15	Change	R195, R197, R198, R202, R201, R203, R205, R206 to SD028680080	
22)	08/18	15	Remove	R207	For HW Review demand
23)	08/18	18	Change	Net name from PM_CLKRUN# to PCH_GPIO32	For HW Review demand
24)	08/18	20	Change	R324 From 1K to 2.2K	For Intel check list demand
25)	08/18	21	Remove	PCH PECL signal	By HW Review demand
26)	08/18	25	Remove	C363, C364, C365, C366	By HW Review demand
27)	08/18	30	Change	UT4 to SA00004600	For CIC demand
28)	08/18	30	Change	USB308 to always mount	Due to no BTO USB20/30.
29)	08/18	27	Remove	all new card function	
30)	08/20	9	Add	PJ32	For Cost down +1.5V to +1.5V_CPU
31)	08/20	13	Swap	USB20_P11 and USB20_N11	For layout request
32)	08/20	25	Swap	USB20_P0, USB20_N0, USB20_P1, USB20_N1	For layout request
33)	08/23		Update	Power schematic	
34)	08/23	20	Swap	PCI_PIRQC#, PCH_GPIO4, PCH_GPIO2, PCI_PIRQA#	For layout request
35)	08/23	20	Swap	SLP_CHG_M3, SLP_CHG_M4, USB_OC#0	For layout request
36)	08/30	18	Reserve	R259	For cost down plan
37)	08/30		Change	USB3.0 Connector	For ME demand
38)	08/30	21	Add	USB Sleep & Charge MAXIC_Select pin in GPIO71(Remove T73)	For MAX14550E/14566B co-lay
39)	08/30	25	Change	C426 to Aluminum Solid Cap 220u	For cost down
40)	08/30	27	Add	USB Sleep & Charge IC: MAX14550E	
41)	08/30	28	Add	16pin X'form for cost down, and P/N is SP050006E00	For cost down
42)	08/30	28	Change	PWRME_CTRL# from PCH_GPIO33 to HDA_SDO	By Intel spec
43)	08/30	16	Change	U53 PIN 9 from KS14 to KS13	
44)	08/30	16	Change	R442, R443 from 10k to 100k	
45)	08/30	16	Change	U56 Pin3 from K506 to +5VALW	
46)	08/30	16	Add	R227 100k ohm	
47)	08/30	28	Reserve	D85 and D86	For ESD request
48)	08/30	30	Swap	U3RXDN1_R, U3RXDN1_R_L, U3RXDP1_R, U3RXDP1_R_L	For layout request
49)	08/30	16	Change	U13 from SA000021A00 to SA000031N00	Due to EOL of SA000021A00
50)	08/30	27	Reserve	R1443 for WLAN Mini PCIE Card Pin5	
51)	08/30	33	Change	U22 From SA00003GK00 to SA00003GM10	Due to EOL of SA00003GK00
52)	08/30	34	Change	SW1, SW4 to SM100002Y00	
53)	09/01	28	Add	LL5 for ISN Test	For EMI demand
54)	09/01	31	Change	RA12 from 10k to 4.7kohm and CA18 from 0.1uF to 100pF	For Beep by A51 demand.
55)	09/01	32	Add	CPSETIN to power	For 65W/75W select
56)	09/01	18,20,21	Reserve	C894, C895, C896, C897	For ESD request
57)	09/02	08	Remove, add	C126, C131 and add C898 3Pin Bulk Cap	By Power Demand
58)	09/02	27	Add	145668 & 145508	
59)	09/02	27	Change	U5 Pin8 control pin from SLP_CHG# to SLP_CHG_M4	
60)	09/02	33	Change	EC ROM size from 256KB(SA00003GM10) to 128KB(SA00003FL10)	
61)	09/02	11	Change	C165,C166,C168,C171,C174,C176,C178 from SE093106M80 to SE0000005T80	For sourcer demand
62)	09/02	12	Change	C191,C192,C194,C197,C200,C202,C204 from SE093106M80 to SE0000005T80	For sourcer demand
63)	09/02		Change	CT25 from SE093106K80 (10uF_0805) to SE0000005T80 (10uF_0603)	For sourcer demand
64)	09/03	08	Change	C890, C891, C894 from SGA00005R00 to SGA00004X80	For Power demand
65)	09/06	33	Change	U22 change to SA00003FL10	
66)	09/06	28	Delete	U14 8105ELDO8 and 8105ESWR8	

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Date:	Thursday, October 07, 2010	Sheet	87	of	87