

# Compal Confidential

Cougar

## LA-6851P Schematics Document

Intel Pine View Processor/ Tiger point

2010-10-10

REV: 1.0

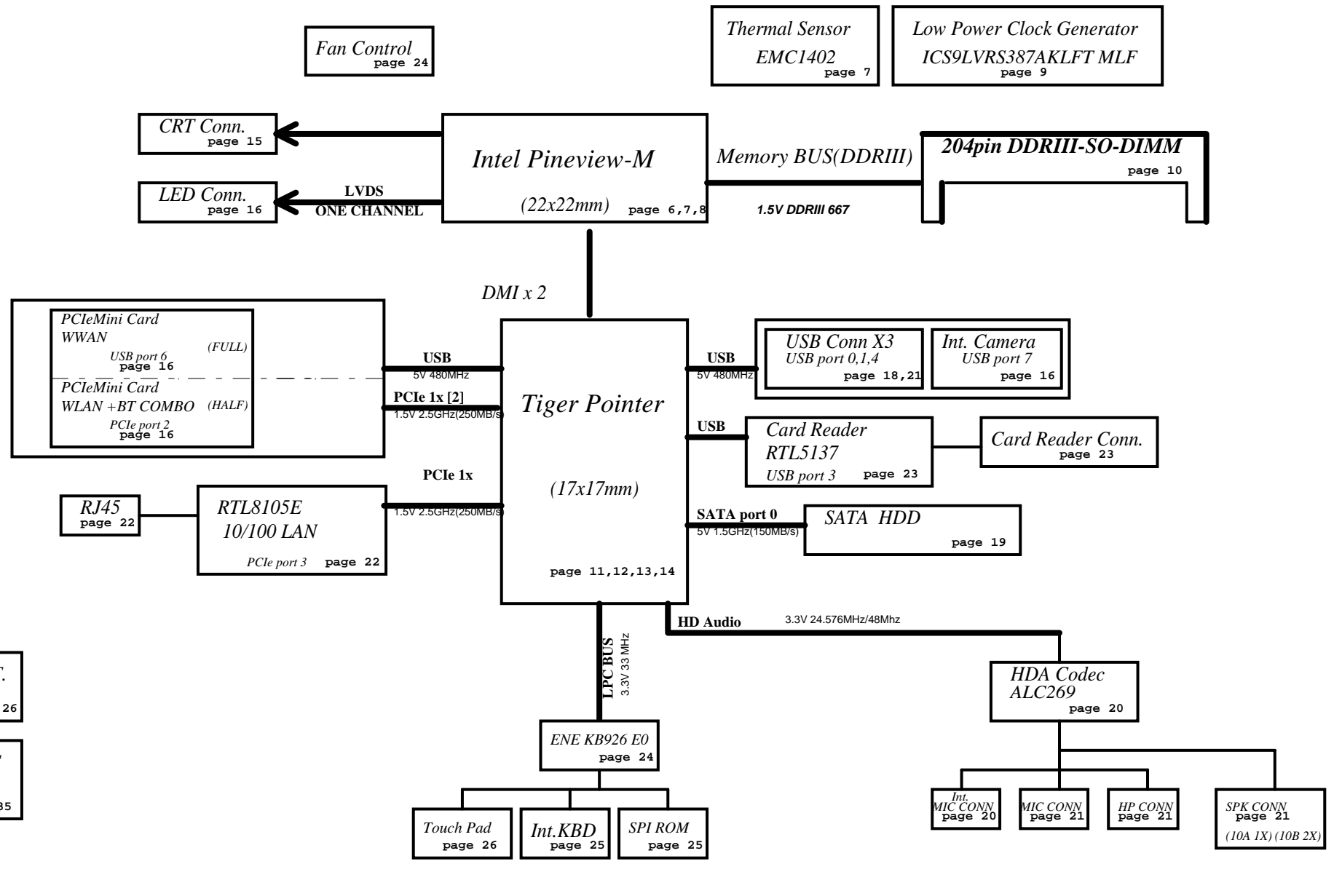
Toshiba Satellite NB500 NB505

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# Compal Confidential

Model Name : PBU00

File Name : LA-6851P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	ON	OFF	OFF
+5VALW	5V always on power rail	ON	OFF	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				CAMERA & MIC		BLUE TOOTH		Clock gen	
description										
explain	Wi-Fi	WiMax	3GGPS	3G	CAMERA	MIC	BLUE TOOTH		Tpye	
BTO	WLAN@	WIMAX@	3GGPS@	3G@	CAM@	MIC@	BT@		low@	normal@

Function			
description			
explain			
BTO			

EC SM Bus1 address

EC SM Bus2 address

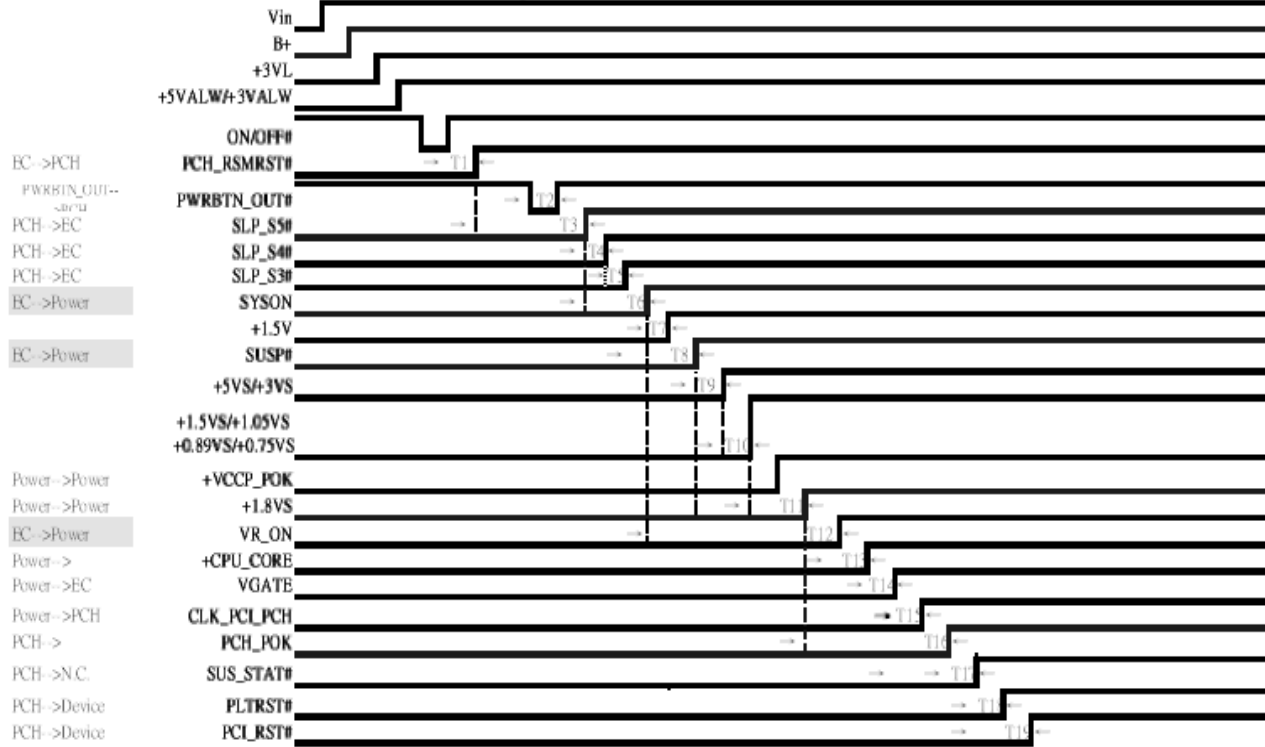
Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb
WWAN/WLAN	

# PBU00 Power ON sequence

2010/7/2



## Power-on Sequence

Time	Description	Expected
T1	Power Button active to PCH_RSMRST# inactive	> 105ms
T2	Power Button active to PBTN_OUT# inactive	< T1
T3	PCH_RSMRST# inactive to PM_SLP_S5# inactive	< 110ms
T4	PM_SLP_S5# inactive to PM_SLP_S4# inactive	28.992us ~ 64.088us
T5	PM_SLP_S4# inactive to PM_SLP_S3# inactive	28.992us ~ 64.088us
T6	PM_SLP_S3# inactive to SYSON active	> 10ms
T7	SYSON active to +1.5V active	> 0
T8	PM_SLP_S3# inactive to SUSP# inactive	> 10ms
T9	SUSP# inactive to +5VS active	> 0
T9	SUSP# inactive to +3VS active	> 0
T10	SUSP# inactive to +1.5VS active	> 0
T10	SUSP# inactive to +0.89VS active	> 0
T10	SUSP# inactive to +0.75VS active	> 0
T11	+1.05VS inactive to +1.8VS active	> 0
T12	SUSP# inactive to VR_ON active	> 10ms
T13	VR_ON active to +CPU_CORE active	> 0
T14	+CPU_CORE active to VGATE	< 10ms
T15	VGATE active to CLK_PCI_ICH stable	< 1.8ms
T16	+1.5VS power active to ICH_PWROK active	> 99ms
T17	ICH_PWROK active to SUS_STAT# inactive	0.928ms ~ 1.218ms
T18	SUS_STAT# inactive to PLT_RST# inactive	57.984us ~ 96.132us
T23	SUS_STAT# inactive to PCI_RST# inactive	57.984us ~ 96.132us

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# Cougar Power Map

B+

DESIGN CURRENT 250mA

Ipeak=6.97A, Imax=4.88A

DESIGN CURRENT 522mA

+3VALWP +-5%

UP6182CQAG

\*\* The SW just is reserved.  
The power passes by jump or  
0-ohm resistor.

WOL\_EN#

\*\* P-CHANNEL  
AO3413

DESIGN CURRENT 300mA

+3V\_LAN

Ipeak=3.98A, Imax=2.8A

DESIGN CURRENT 3010mA

+5VALWP +-5%

SUSP

N-CHANNEL

SI4800BDY

DESIGN CURRENT 2286mA

+5VS

SUSP

N-CHANNEL

SI4800BDY

DESIGN CURRENT 5586mA

+3VS

ENVDD

P-CHANNEL  
AO3413

DESIGN CURRENT 2000mA

+LCD\_VDD

SUSP#

SY8033BDBC

DESIGN CURRENT 2640mA

+0.89VSP

SUSP#

SY8033BDBC

Ipeak=1.308A, Imax=4A

DESIGN CURRENT 3489mA

+1.05VSP +-5%

VR\_ON

ADP3211AMNR2G

Imax=3.5A

DESIGN CURRENT 6000mA

+CPU\_CORE

SYSON

G5603RU1U

Ipeak=19.6A, Imax=13.72A

DESIGN CURRENT 2000mA

+1.5VP +-5%

SUSP#

IRF8113PBF

DESIGN CURRENT 2112mA

+1.5VSP

SUSP

UP7711U8

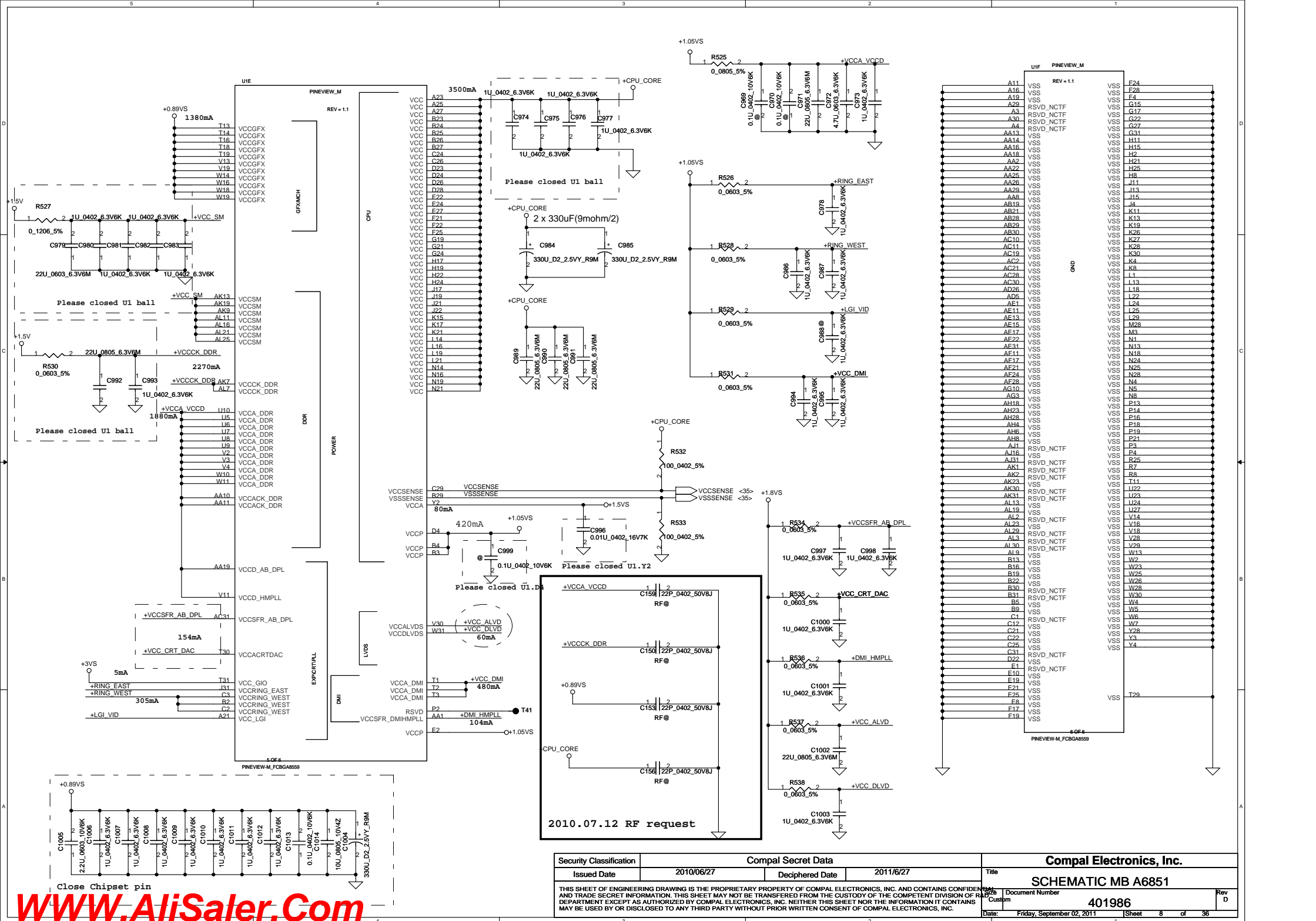
DESIGN CURRENT 500mA

+0.75VSP

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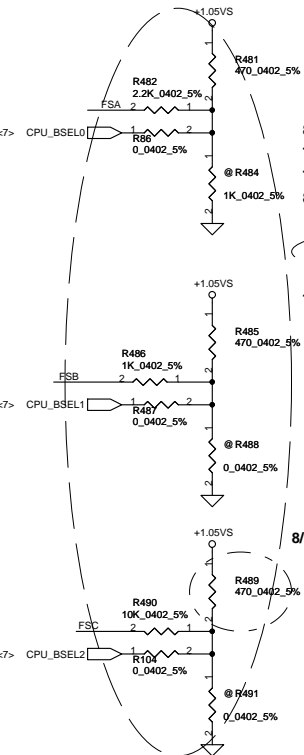






FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

	Normal Power	Low Power
R477	@	Stuff
R478	Stuff	@
R479	Stuff	@
R480	@	Stuff
R483	@	Stuff



8/24 Change net name to FSB for U3.2

7/13 Add 33pF to GND for RF request

7/21 Reserve 33pF to GND for RF request

8/27 C303, C324, C325, C326, C327 to GND for RF request

7/22 Add R241 pull up to +3VS for RF Intel request

8/14 Add R250 pull up for Intel request

7/13 Add 33pF to GND for RF request

For ITP\_EN, 0 = SRC8 / SRC8#; 1 = ITP / ITP#

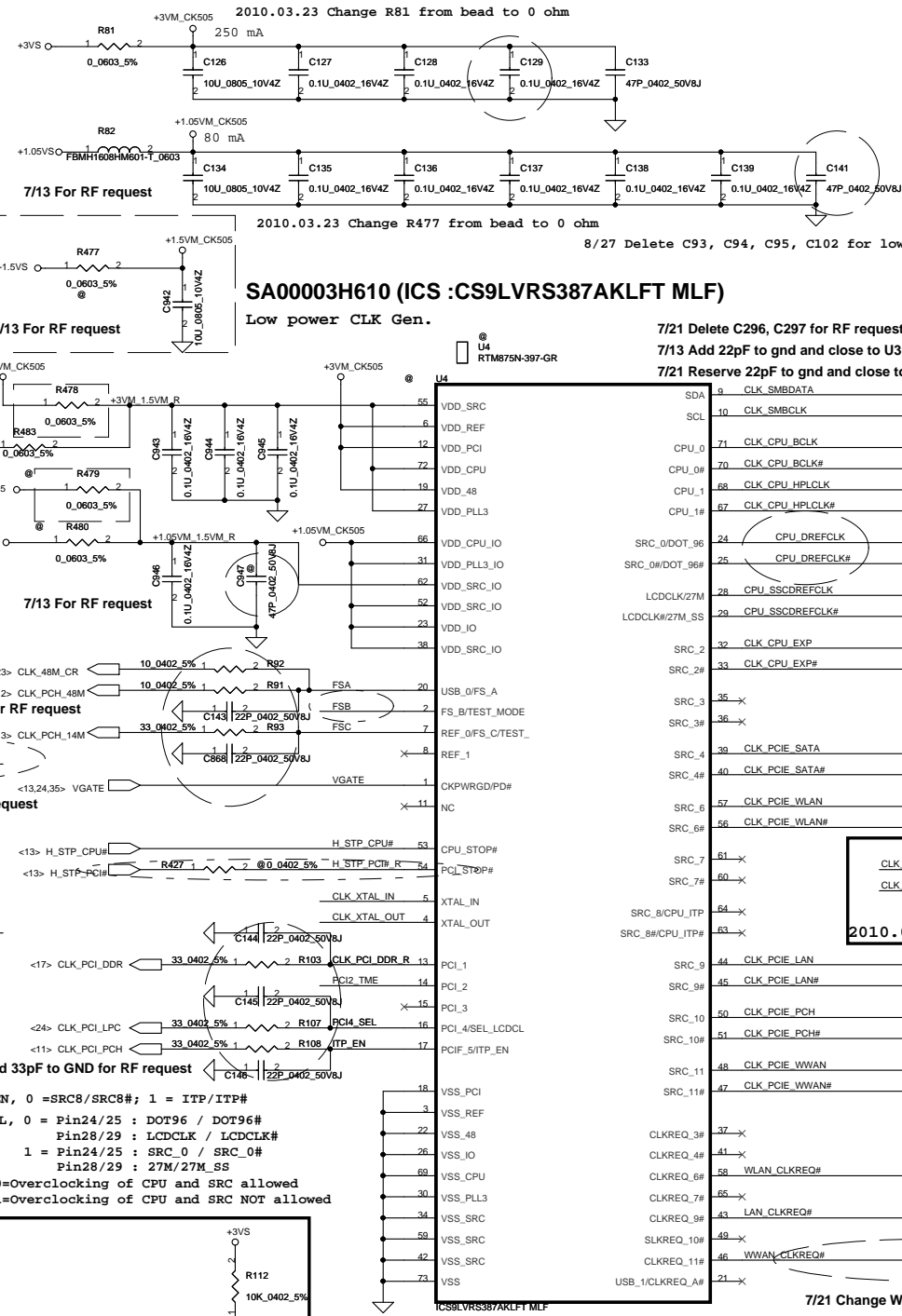
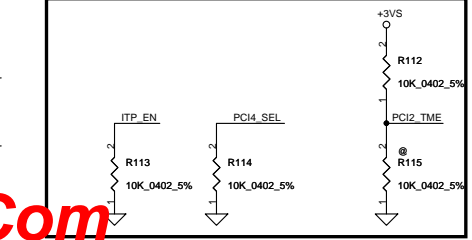
For PCI4\_SEL, 0 = Pin24/25 : DOT96 / DOT96#

Pin28/29 : LCDCLK / LCDCLK#

1 = Pin24/25 : SRC\_0 / SRC\_0#

Pin28/29 : 27M / 27M\_SS

For PCI2\_TME: 0=Overclocking of CPU and SRC allowed (ICS only) 1=Overclocking of CPU and SRC NOT allowed



## SA00003H610 (ICS:CS9LVRS387AKLFT MLF)

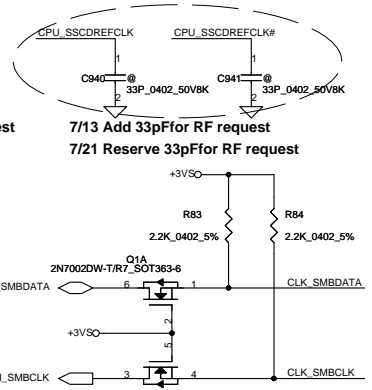
Low power CLK Gen.

- 7/21 Delete C296, C297 for RF request
- 7/13 Add 22pF to gnd and close to U3 for RF request
- 7/21 Reserve 22pF to gnd and close to U3 for RF request

SDA	9	CLK_SMBDATA	CLK_SMBDATA <10,17>
SCL	10	CLK_SMBCLK	CLK_SMBCLK <10,17>
CPU_0	71	CLK_CPU_BCLK	CLK_CPU_BCLK <7>
CPU_0#	70	CLK_CPU_BCLK#	CLK_CPU_BCLK# <7>
CPU_1	68	CLK_CPU_HPLCLK	CLK_CPU_HPLCLK <7>
CPU_1#	67	CLK_CPU_HPLCLK#	CLK_CPU_HPLCLK# <7>
SRC_0DOT_96	24	CPU_DREFCLK	CPU_DREFCLK <7>
SRC_0#DOT_96#	25	CPU_DREFCLK#	CPU_DREFCLK# <7>
LCDCCLK/27M	28	CPU_SSCDREFCLK	CPU_SSCDREFCLK <7>
LCDCCLK/27M_SS	29	CPU_SSCDREFCLK#	CPU_SSCDREFCLK# <7>
SRC_2	32	CLK_CPU_EXP	CLK_CPU_EXP <6>
SRC_2#	33	CLK_CPU_EXP#	CLK_CPU_EXP# <6>
SRC_3	35	×	×
SRC_3#	36	×	×
SRC_4	39	CLK_PCIE_SATA	CLK_PCIE_SATA <11>
SRC_4#	40	CLK_PCIE_SATA#	CLK_PCIE_SATA# <11>
SRC_6	57	CLK_PCIE_WLAN	CLK_PCIE_WLAN <17>
SRC_6#	56	CLK_PCIE_WLAN#	CLK_PCIE_WLAN# <17>
SRC_7	61	×	×
SRC_7#	60	×	×
SRC_8/CPU_ITP	64	×	×
SRC_8#CPU_ITP#	63	×	×
SRC_9	44	CLK_PCIE_LAN	CLK_PCIE_LAN <22>
SRC_9#	45	CLK_PCIE_LAN#	CLK_PCIE_LAN# <22>
SRC_10	50	CLK_PCIE_PCH	CLK_PCIE_PCH <12>
SRC_10#	51	CLK_PCIE_PCH#	CLK_PCIE_PCH# <12>
SRC_11	48	CLK_PCIE_WWAN	CLK_PCIE_WWAN <17>
SRC_11#	47	CLK_PCIE_WWAN#	CLK_PCIE_WWAN# <17>
CLKREQ_3#	37	×	×
CLKREQ_4#	41	×	×
CLKREQ_6#	58	WLAN_CLKREQ#	WLAN_CLKREQ# <17>
CLKREQ_7#	65	×	×
CLKREQ_9#	43	LAN_CLKREQ#	LAN_CLKREQ# <22>
SLKREQ_10#	49	×	×
CLKREQ_11#	46	WWAN_CLKREQ#	WWAN_CLKREQ# <17>
USB_1/CLKREQ_A#	21	×	×

2010.07.12 RF request

7/21 Change WWAN\_CLKREQ# from REQ4 to REQ11



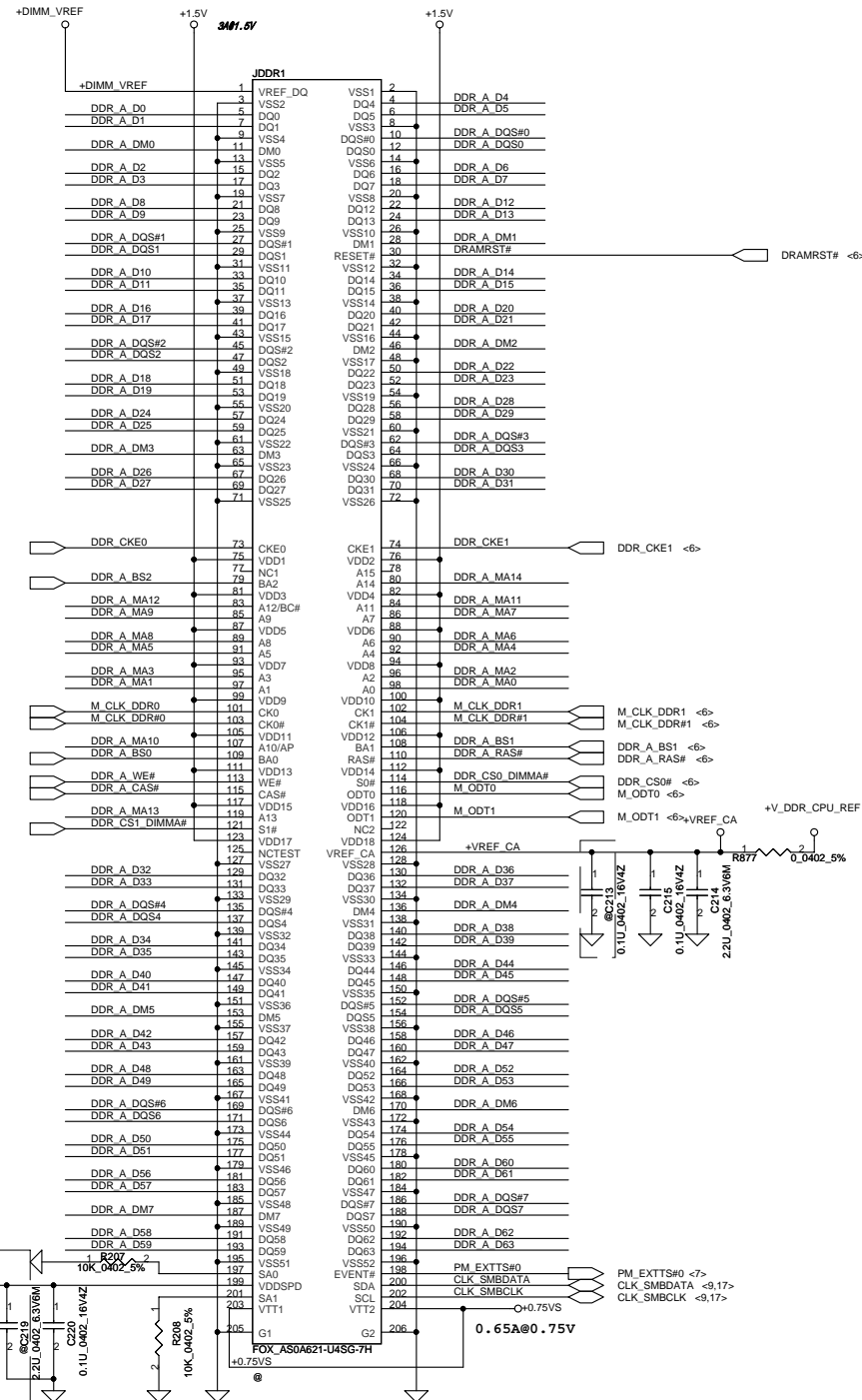
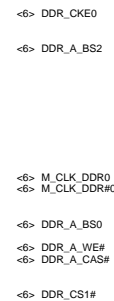
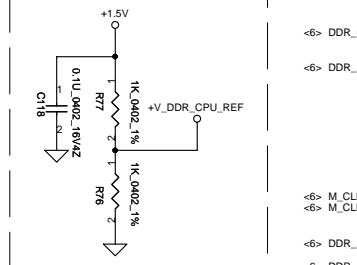
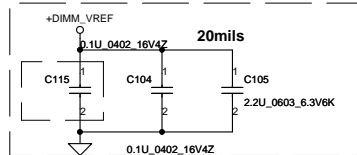
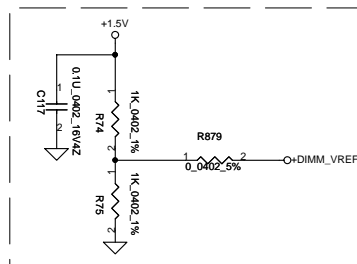
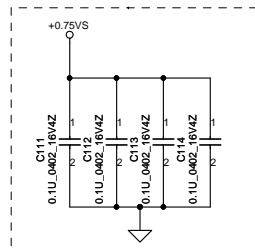
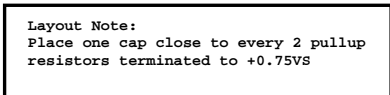
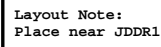
## SRC PORT LIST

PORT	DEVICE
SRC0	CPU_DREFCLK
SRC2	CPU_EXP
SRC3	
SRC4	PCIE_SATA
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_PCH
SRC11	PCIE_WWAN

## REQ PORT LIST

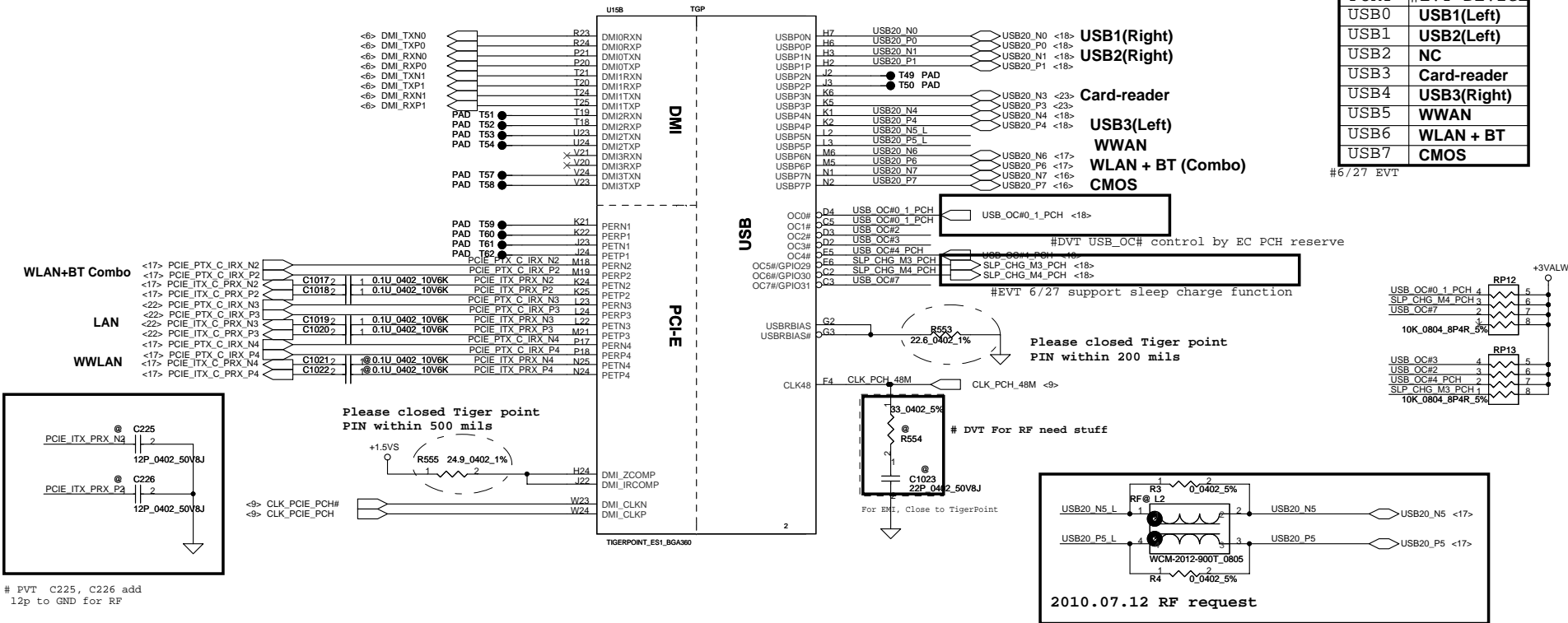
PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	PEIC_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PEIC_WWAN
REQ_A#	

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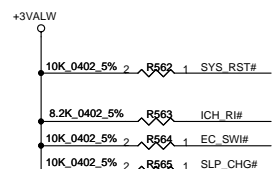
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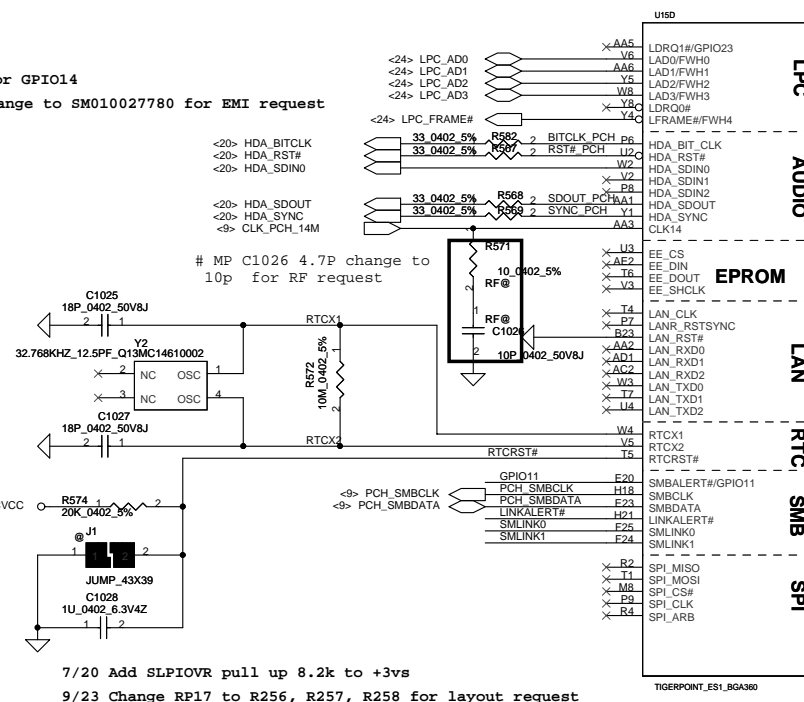
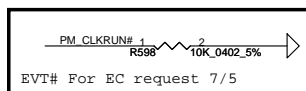
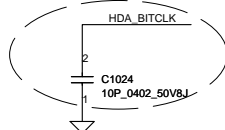
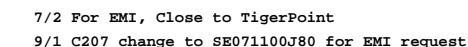
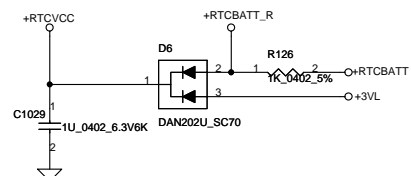
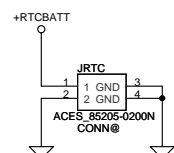
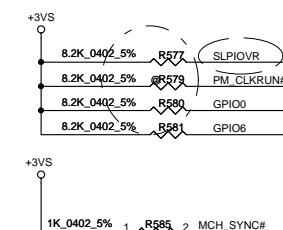
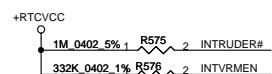
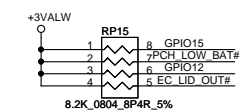
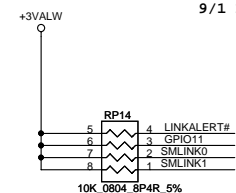


# PVT C225, C226 add  
12p to GND for RF

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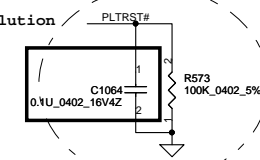
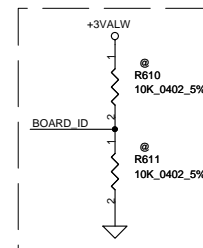
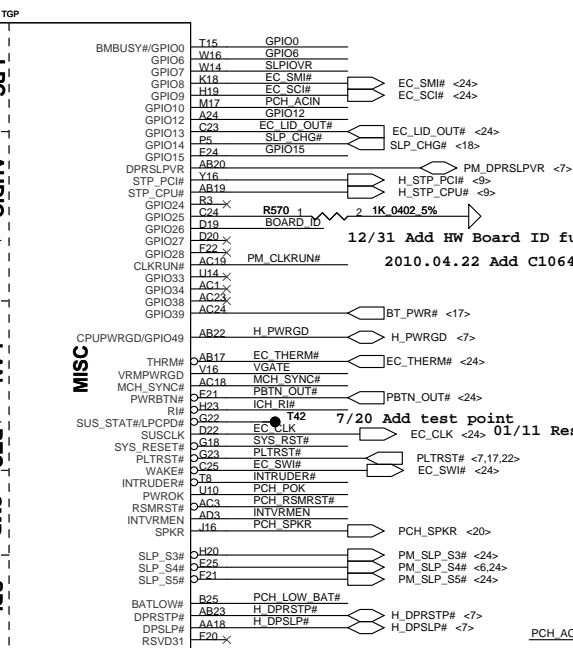
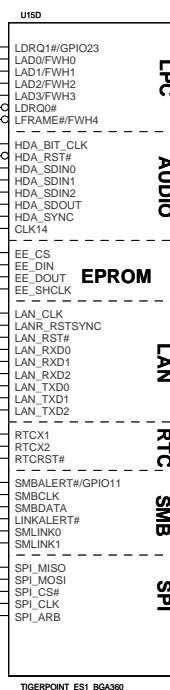


9/1 R125 change to SM010027780 for EMI request



7/20 Add SLPIOVR pull up 8.2k to +3vs

9/23 Change RP17 to R256, R257, R258 for layout request



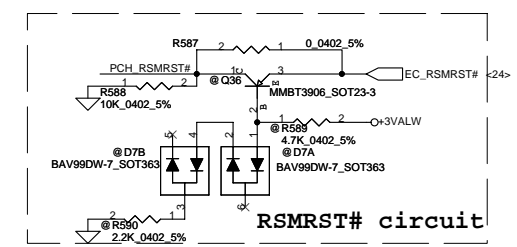
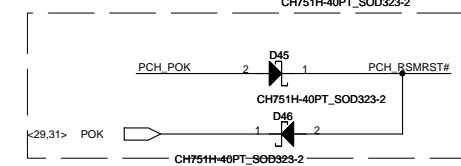
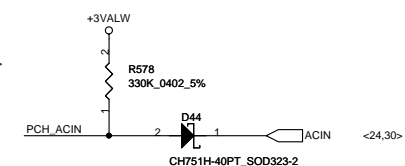
12/31 Add HW Board ID function

2010.04.22 Add C1064 for ESD solution

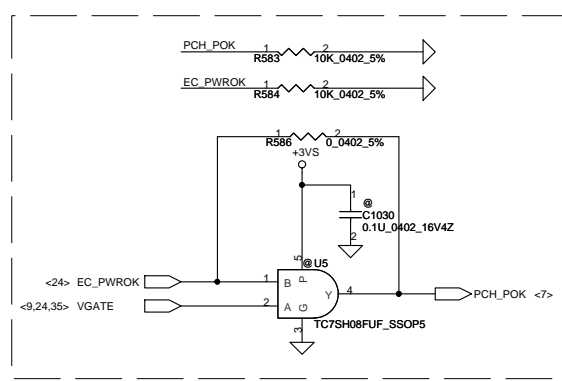
7/20 Add test point

EC\_CLK <24> 01/11 Reserve EC\_CLK for KBC

8/24 Add R254 pull down for EC request

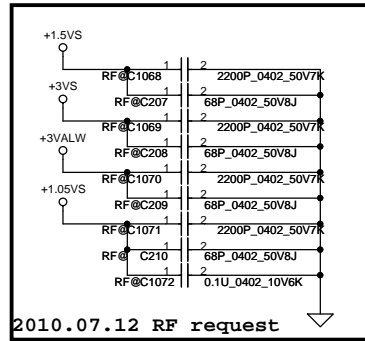
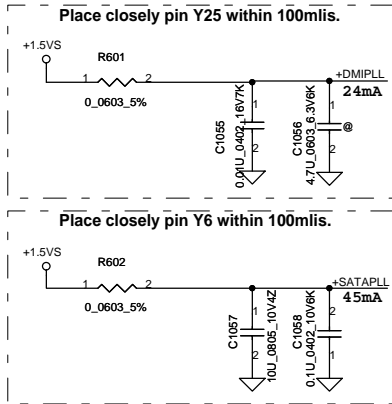
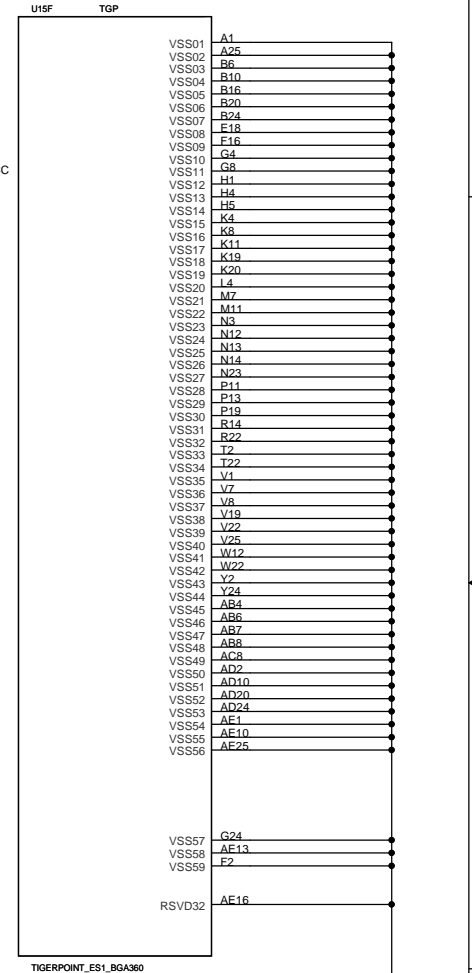
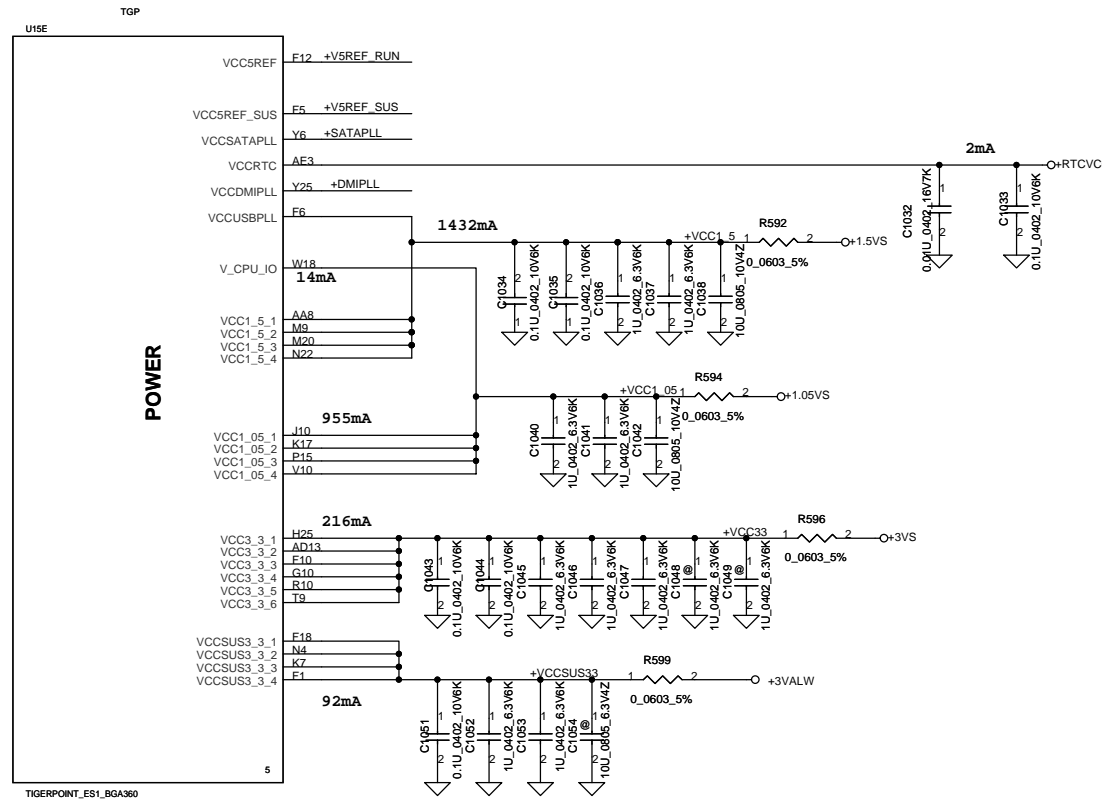
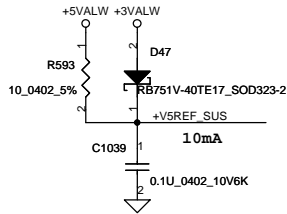
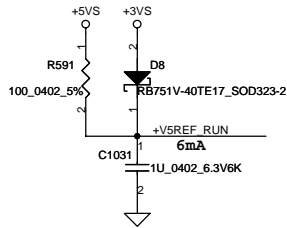


2010.03.22 Un-stuff RSMRST# circuit and use 0 ohm bypass



2010.03.22 Un-stuff U5 and C1030

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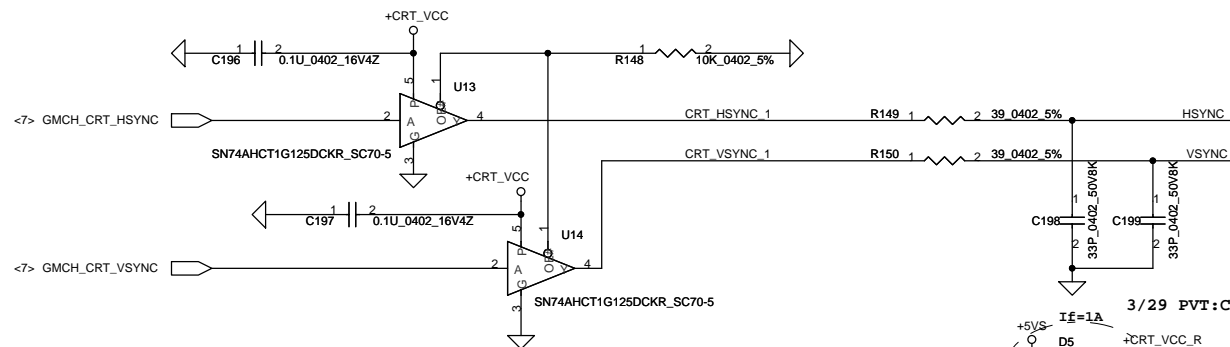
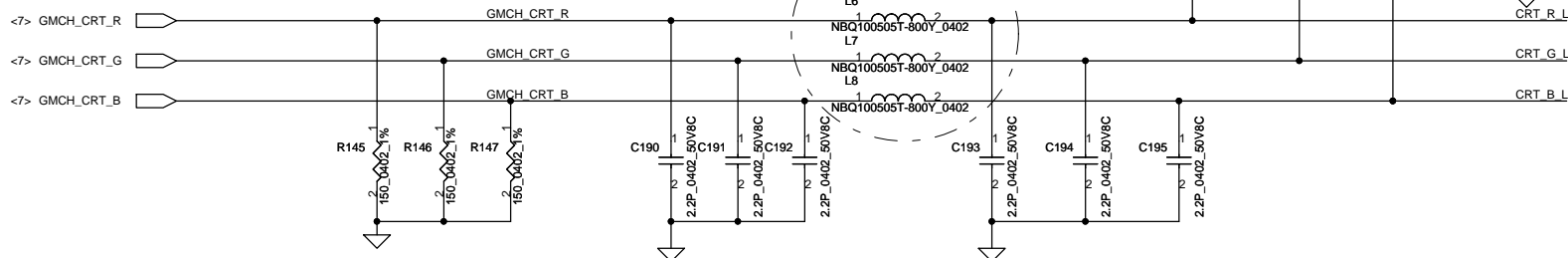
# CRT CONNECTOR

Place closed to conn.

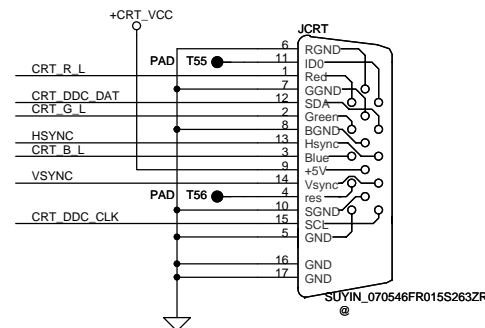
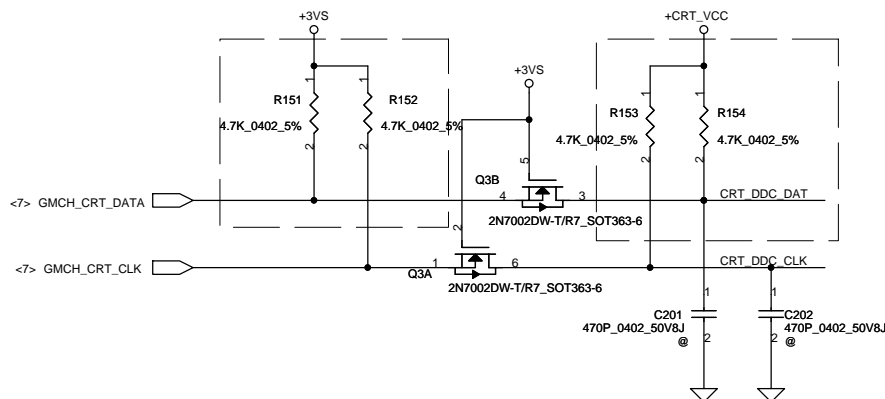
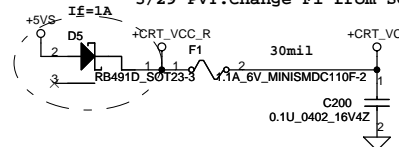
3/16 PVT: Change to high speed bead

2/16 DVT: Mount C504 for EMI request

Place closed to conn.



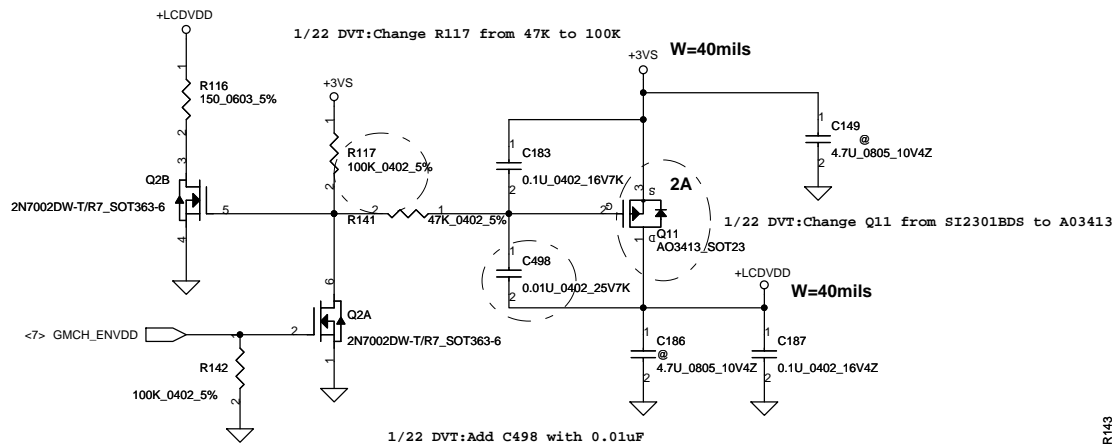
3/29 PVT: Change F1 from SC04301P000 to SP04301P120.



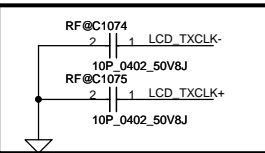
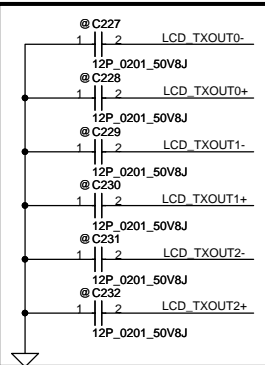
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# LCD POWER CIRCUIT



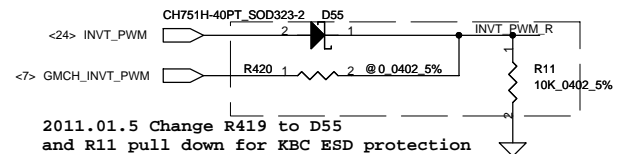
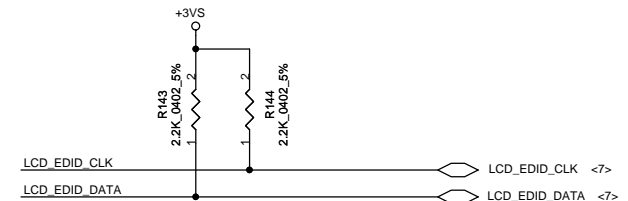
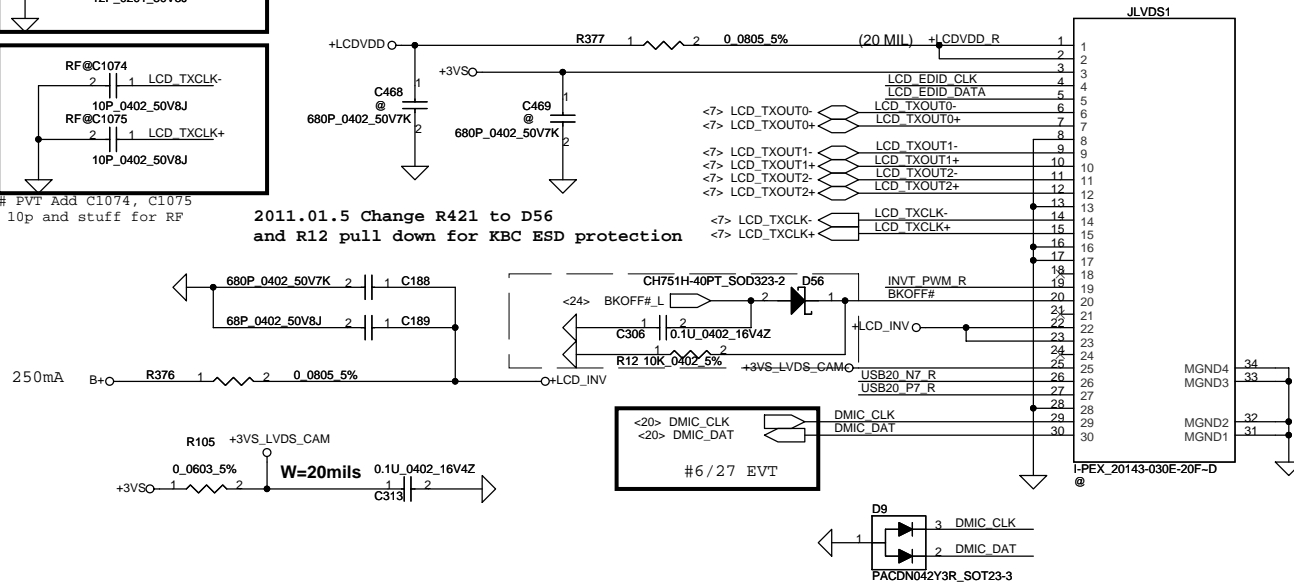
# MP Add C227~C232 for RF request



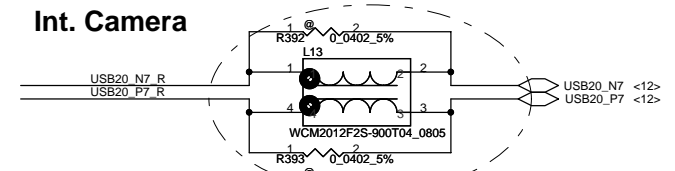
# PVT Add C1074, C1075  
10p and stuff for RF

## LED/PANEL BD. Conn.

2011.01.5 Change R421 to D56  
and R12 pull down for KBC ESD protection



## Int. Camera



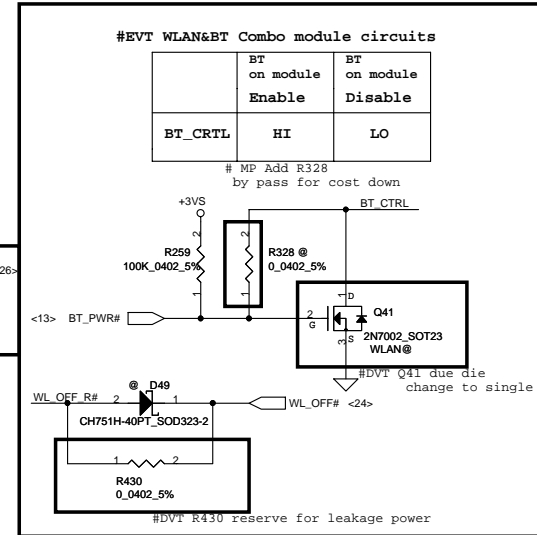
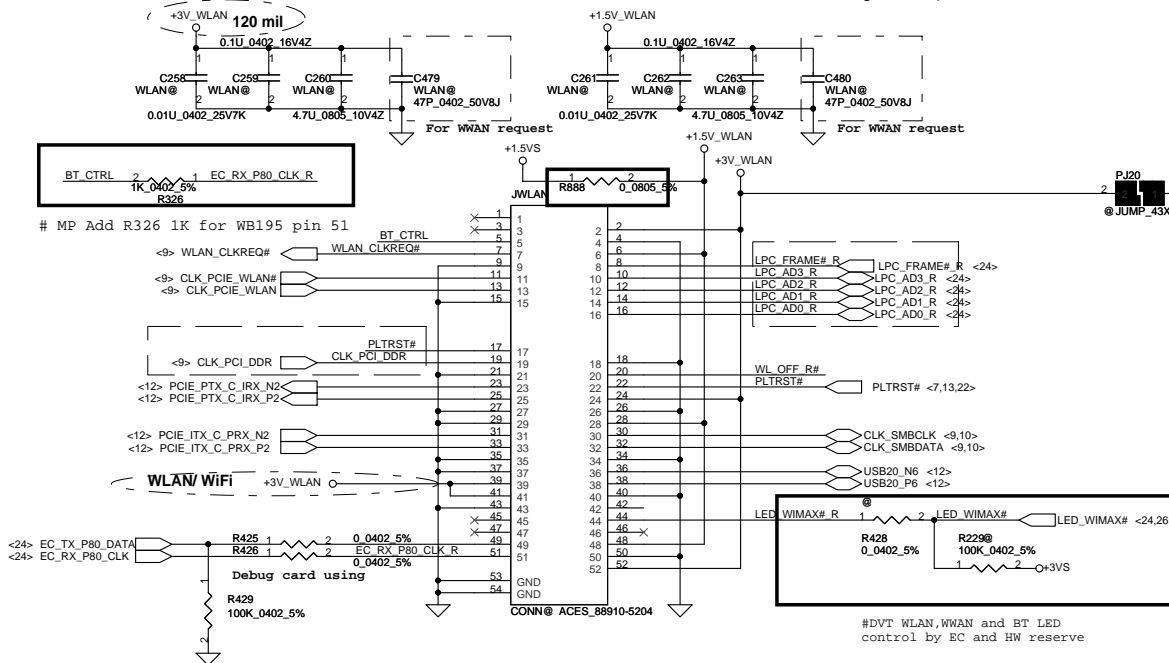
For EMI request

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# Mini-Express Card for WLAN/WiMax

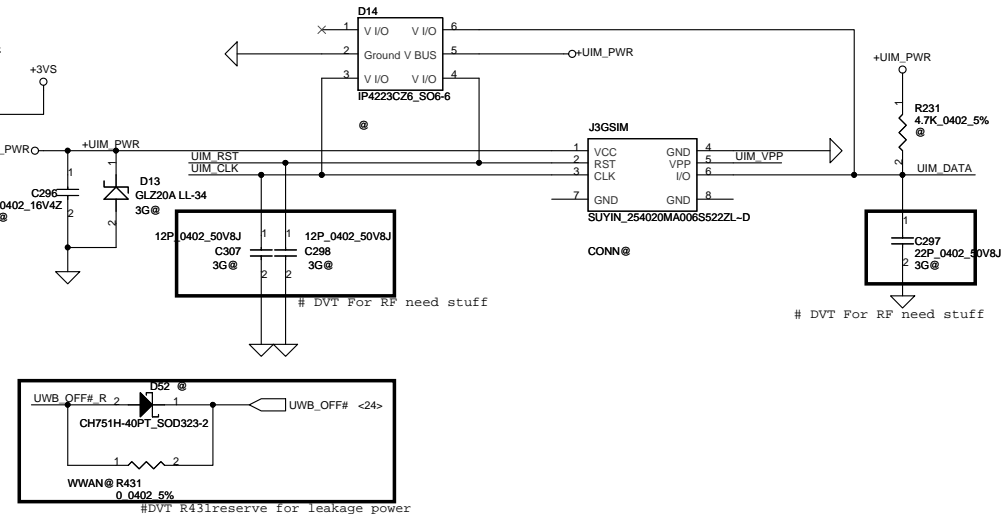
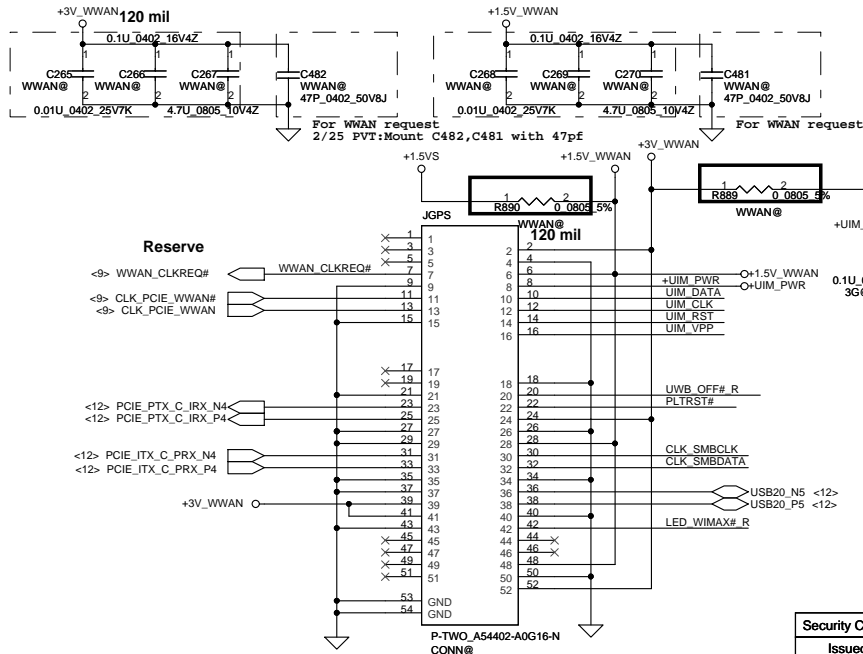
2/25 PVT:Mount C479,C480 with 47pf  
3/16 PVT:Add BOM Config of C481,C482 to WLAN@



# Mini-Express Card for 3G/GPS

3G current need to 2750mA

3/16 PVT:Add BOM Config of C481,C482 to 3GGPS@

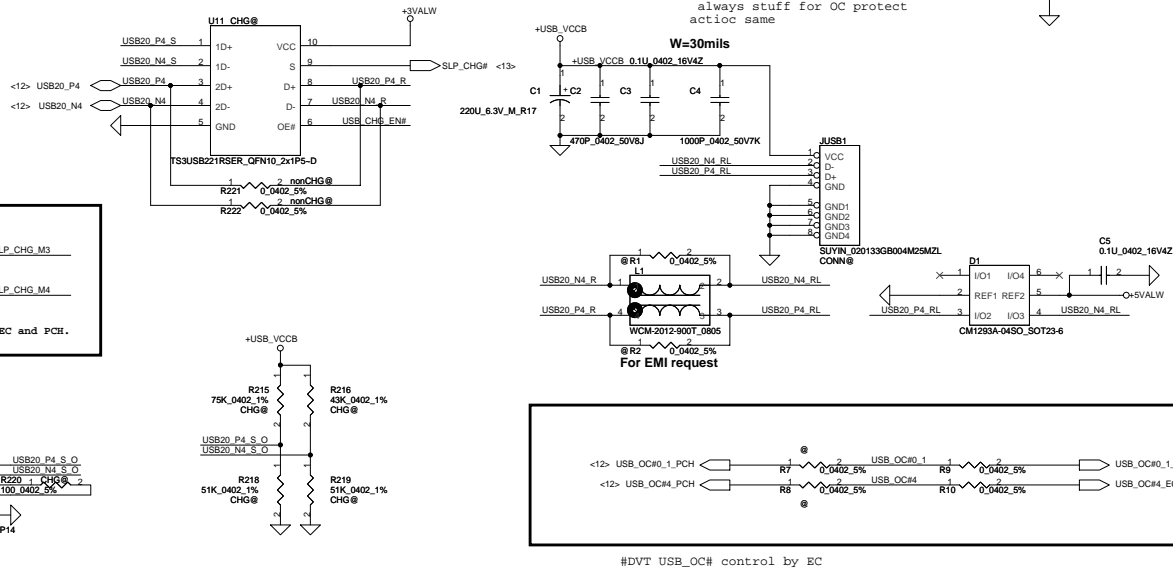


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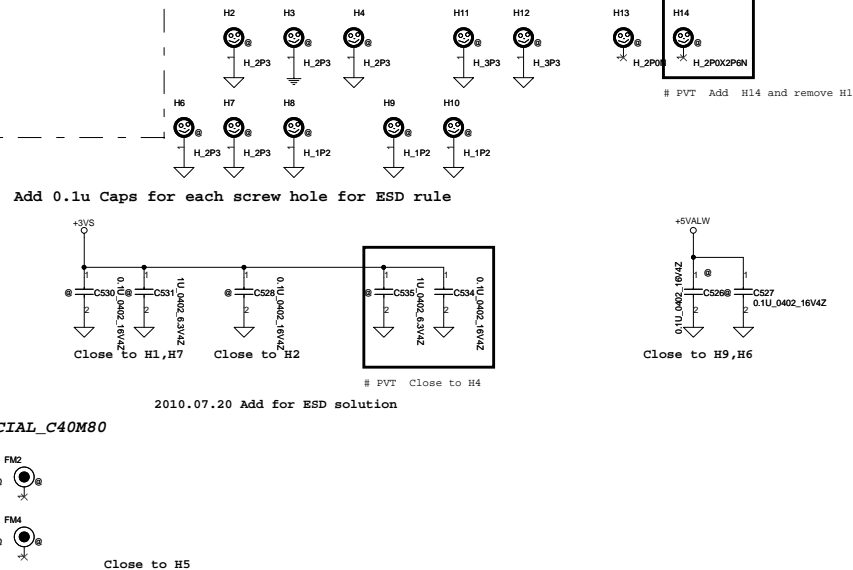
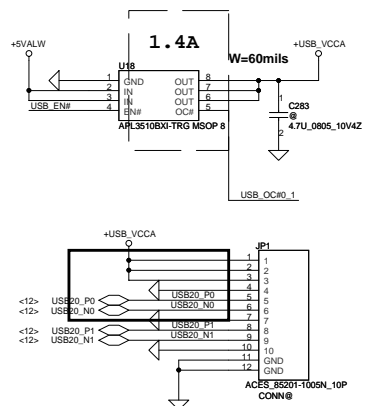
### USB CONN- -Left

	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D

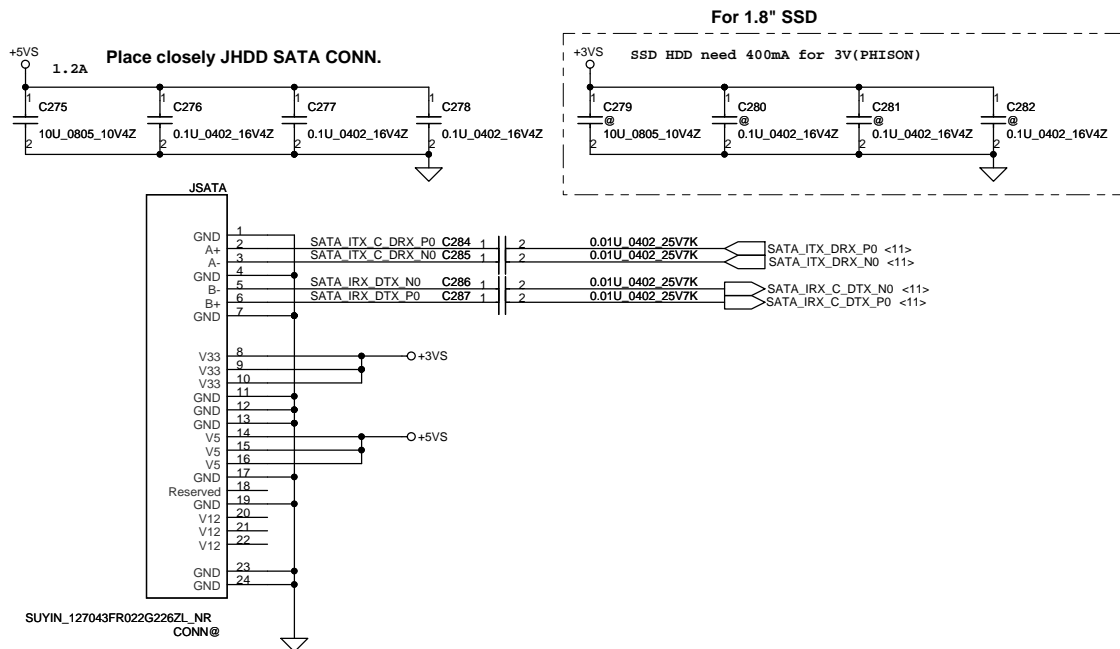


## USB CONN



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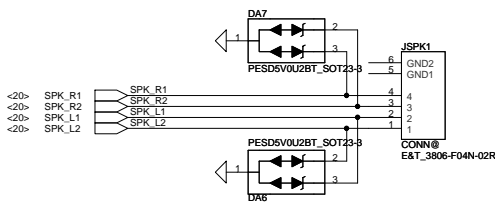
# SATA Conn.



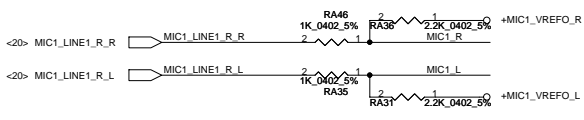
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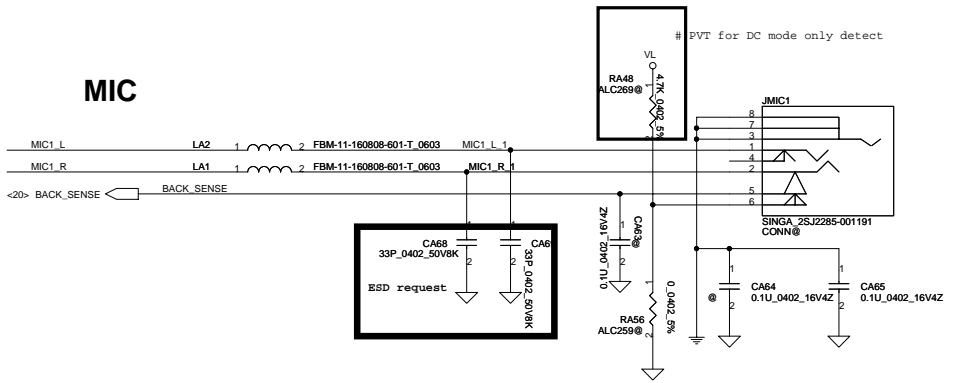
SPEAKER



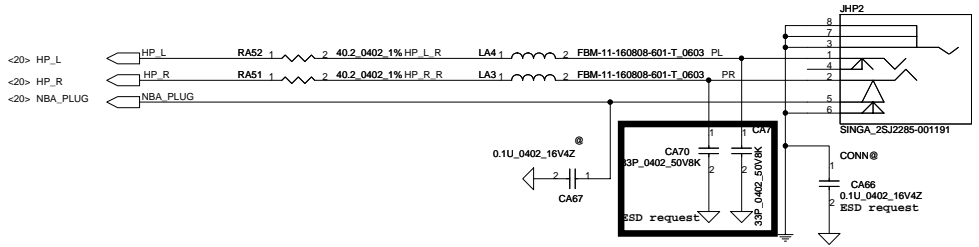
Ext.MIC/LINE IN JACK



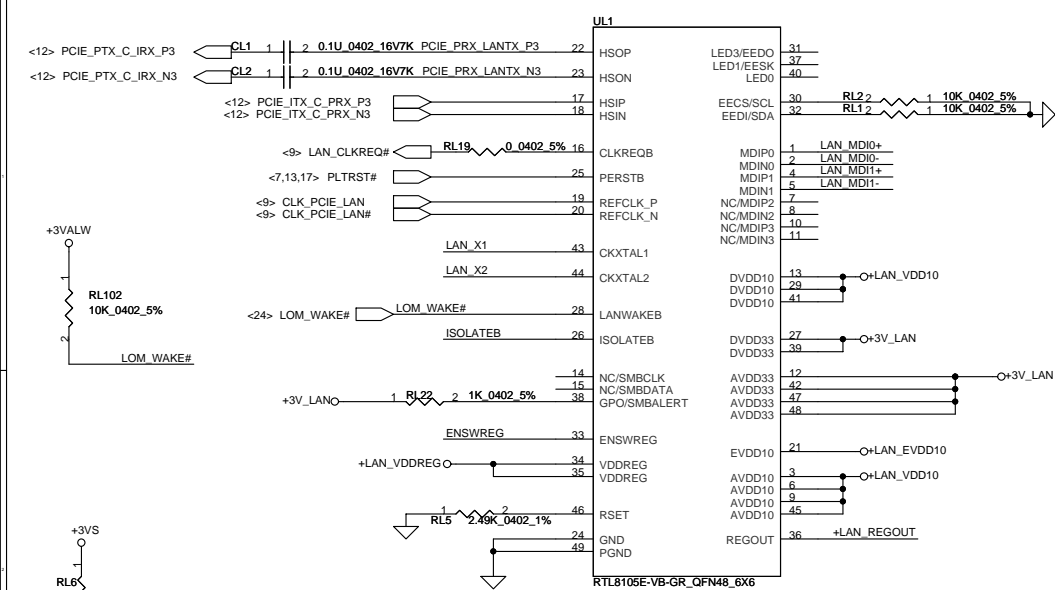
MIC



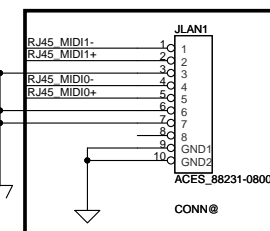
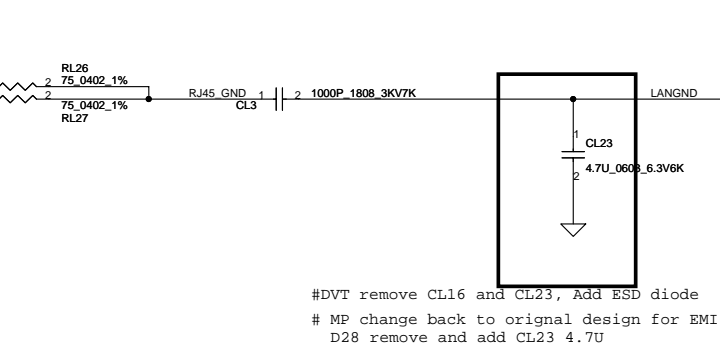
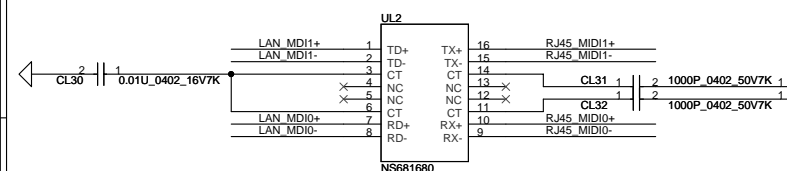
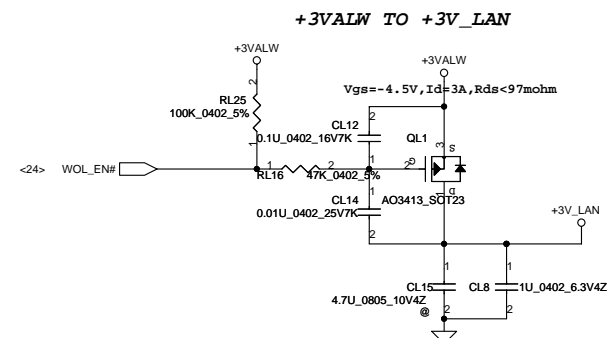
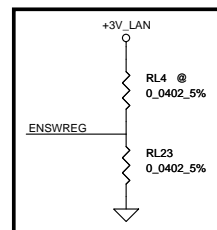
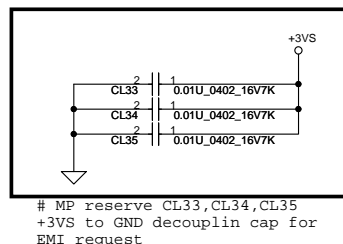
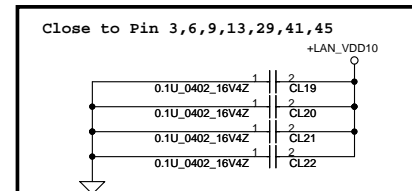
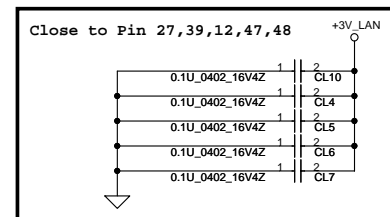
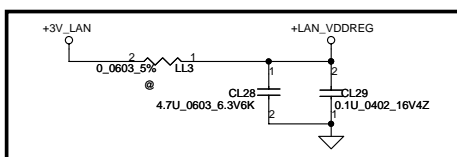
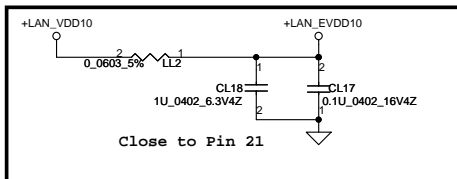
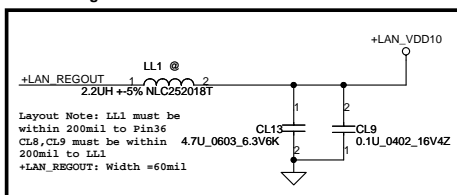
Head phone



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### 3/10 Change CL13 0805-->0603

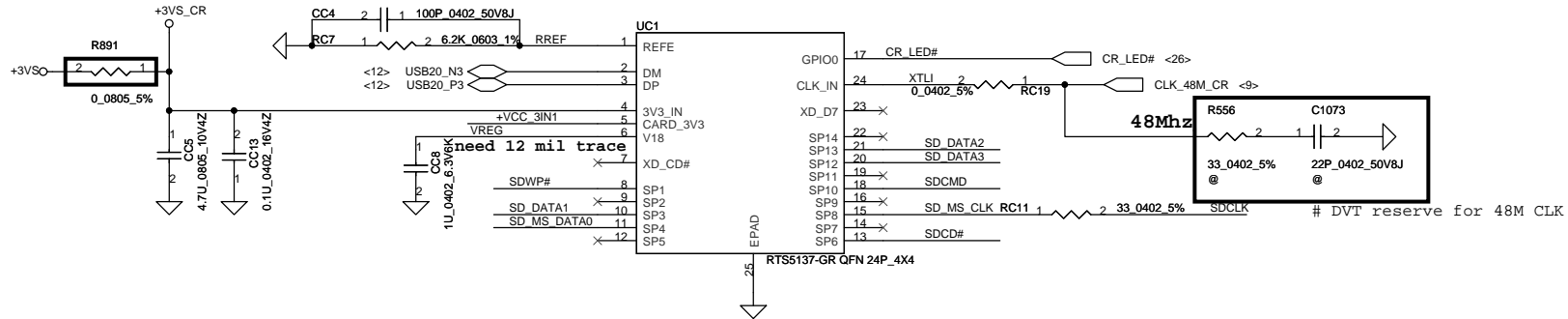


#DVT remove CL16 and CL23, Add ESD diode  
# MP change back to original design for EMI  
D28 remove and add CL23 4.7U

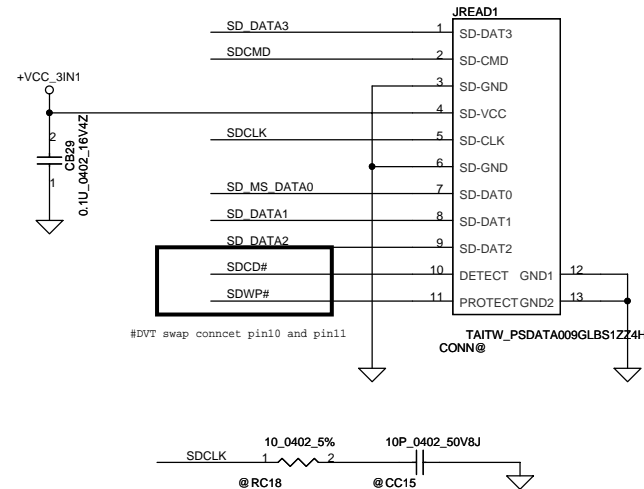
#DVT LAN connect pin definid change  
# PVT Add pin 7 connect to LANGND

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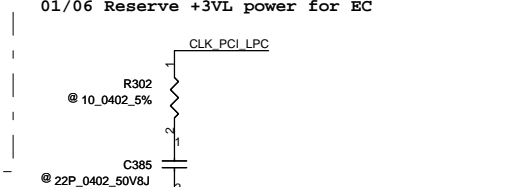
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_C#	SD_D1	
SP4	XD_CLE	SD_D0	MS_D7
SP5	XD_ALE	SD_D7	MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP	SD_D6	MS_D6
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1	SD_D5	MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3	SD_D4	MS_D4
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	MS_D5
SP14	XD_D6		MS_BS
	XD_D7		



## 2 in 1 Card Reader



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Place closely pin 109

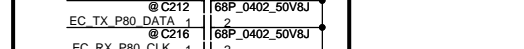
R243 47k\_0402\_5%

R330 0.040\_0402\_5%

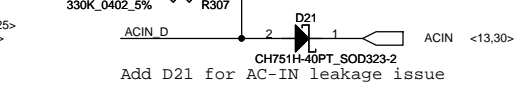
R329 0.040\_0402\_5%

C525 0.1u\_0402\_16V42

# MP change LID# pull up to +3VL



00F\_0402\_00V83



26>

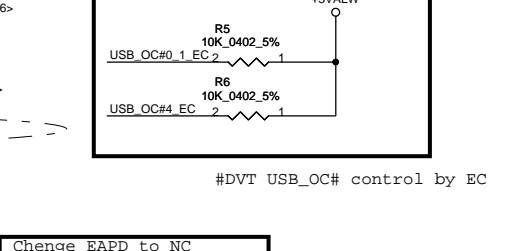


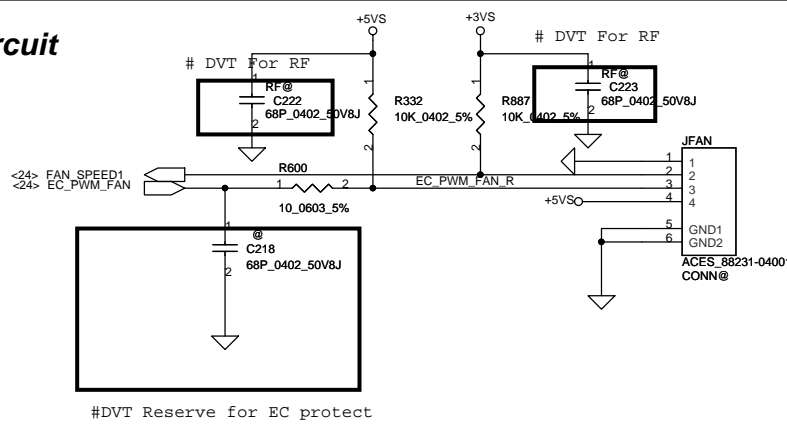
Figure 10-10 shows a circuit diagram for a test setup. A +5V source is connected to two resistors, R595 and R607, both labeled 4.7K 0402 5%. R595 is connected to TP\_CLK and R607 is connected to TP\_DATA.



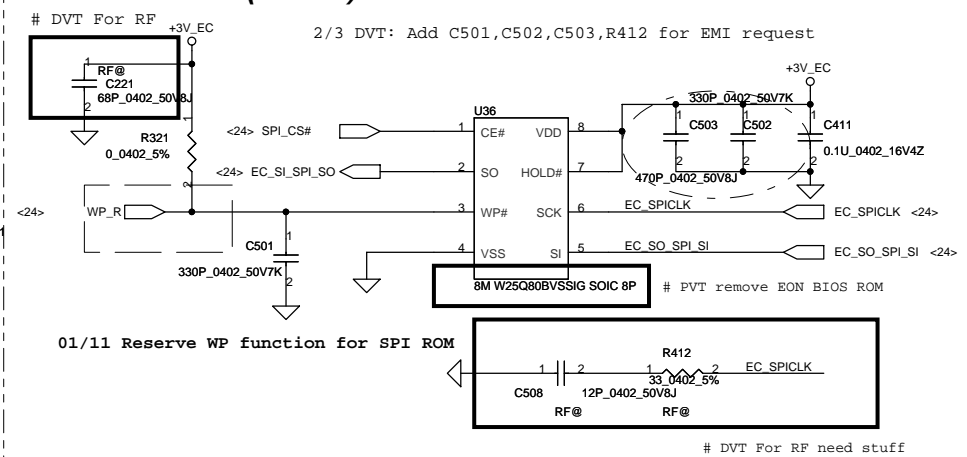
**WWW.AliSaler.Com**



## FAN Control Circuit

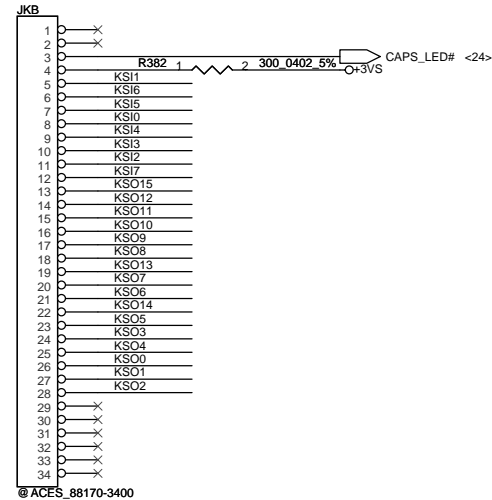


## SPI Flash (8Mb\*1)

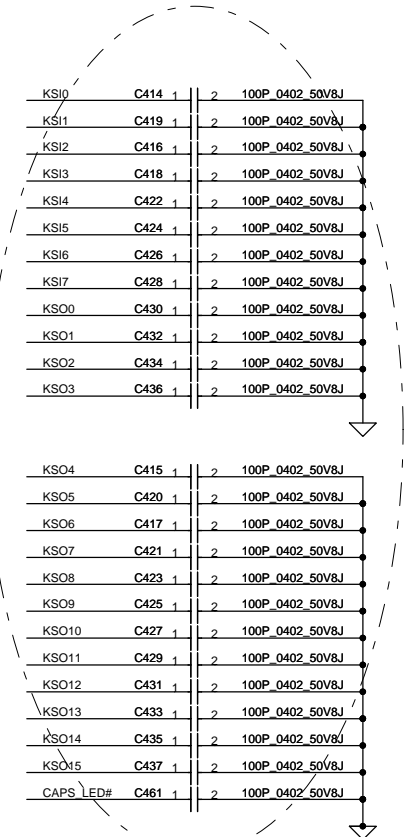


## LPC Debug Port

## KEYBOARD CONN.



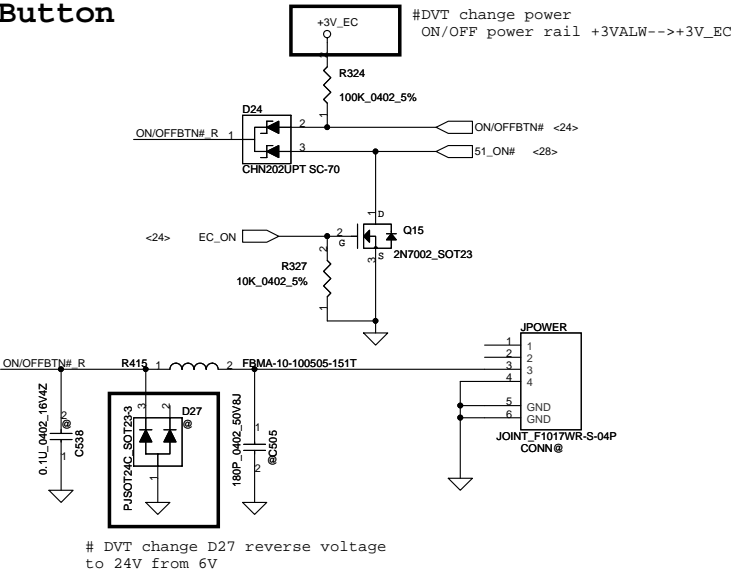
12/18 Follow KB Matrix the same to KSKAA



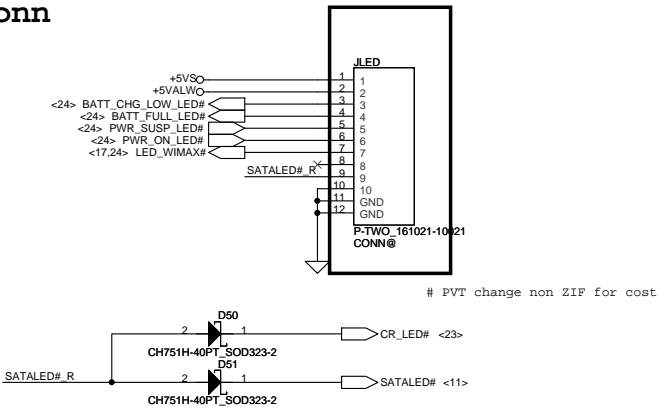
3/4 PVT:Mount C414~C437,C461 for EMI request

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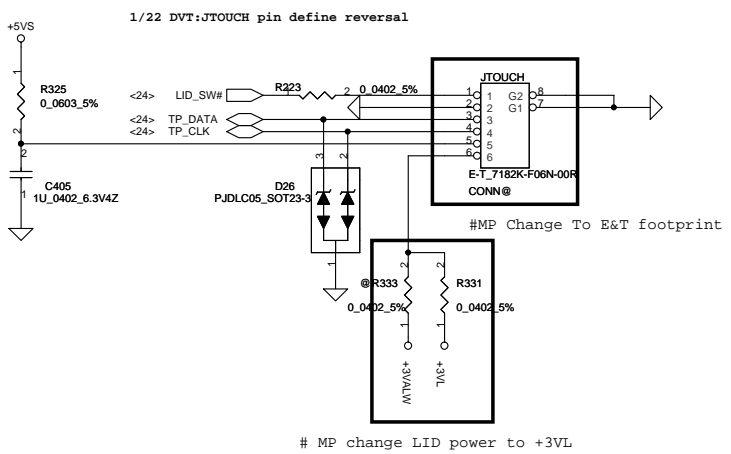
Power Button



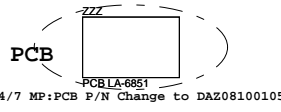
LED Conn



Touch/B Connector



ISPD



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**ESD solution**

2/25 PVT:Change C447 with 0.022uF

The schematic shows the SYSON# pin configuration. The SYSON# pin is connected to a 5V supply through a 100K resistor (R362) and to the gate of the MOSFET. The gate is also connected to a 5V supply through a 10K resistor (R402). The MOSFET is labeled Q28B.

1.8VS

R604@  
470\_0603\_5%

@Q31B

2N7002DW-T/R7\_SOT363-6

SUSP

The diagram illustrates the power supply circuit for the R237 hardware design. A +1.5V input is connected to a network of capacitors (C1059, C1060, C1061, C1062) and a resistor (R606). A MOSFET (Q33, Si7226DN-T1-E3\_PAK12) is used as a switch. The output is labeled "8/31 Change Q20 from SB00".

7/9 Add Q29, Q30, R228 for Intel power sequence.

reserve U08 to control power down sequence between 1.8vs and 1.05vs,01/08,2010

8/31 Change Q20 from SB000002880 to SB00000DW00 for HW design

#DVT change to 470 ohm for +VS power leakage

<32> SUSP

<24,33,34> SUSP#

R401  
10K\_0402\_5%

2N7002DW-T/R7\_SOT363-6

2N7002DW-T/R7\_SOT363-6

2N7002DW-T/R7\_SOT363-6

2/6 DVT: Reserve +1.5VS,+1.05VS,+0.75VS,+1.8VS discharge circuit

+0.75VS

@ R366  
470\_0603\_5%

@Q25A

2N7002DW-T/R7\_SOT363-6

+1.5V

@ R367  
470\_0603\_5%

@ Q26

2SYSON#

2N7002\_SOT23

+1.05VS

C533

1U\_0402\_6.3V4Z

R365@  
470\_0603\_5%

C532

1U\_0402\_6.3V4Z

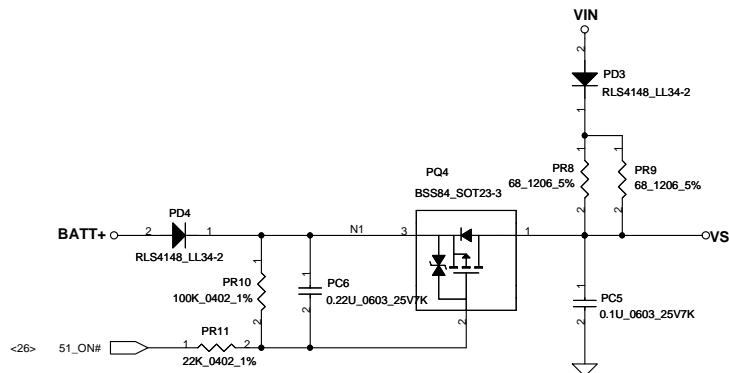
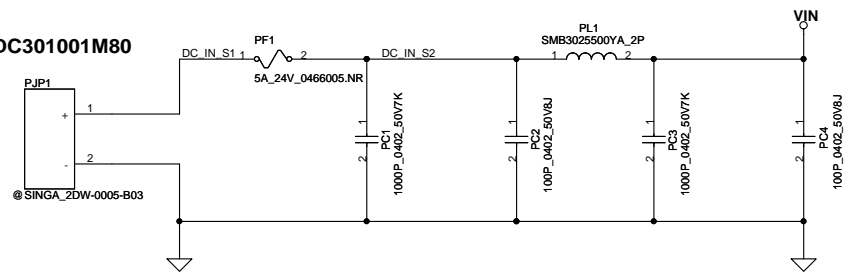
@ Q24

2N7002\_SOT23

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DC301001M80



+3VALWP 2 1 +3VALW  
PJ330  
@JUMP\_43X118  
(6A,240mils ,Via NO.= 10)  
(OCP min=8A)

+1.5VP 2 1 +1.5V  
PJ150  
@JUMP\_43X118  
(4.1A,180mils ,Via NO.= 12)  
(OCP min=6.03A)

+5VALWP 2 1 +5VALW  
PJ350  
@JUMP\_43X118  
(5.5A,220mils ,Via NO.= 10)  
(OCP min=7.8A)

+1.05VSP 2 1 +1.05VS  
PJ105  
@JUMP\_43X118  
(3.5A,140mils ,Via NO.=7)

+VSBP 2 1 +VSB  
PJ5  
@JUMP\_43X39  
(120mA,40mils ,Via NO.= 1)

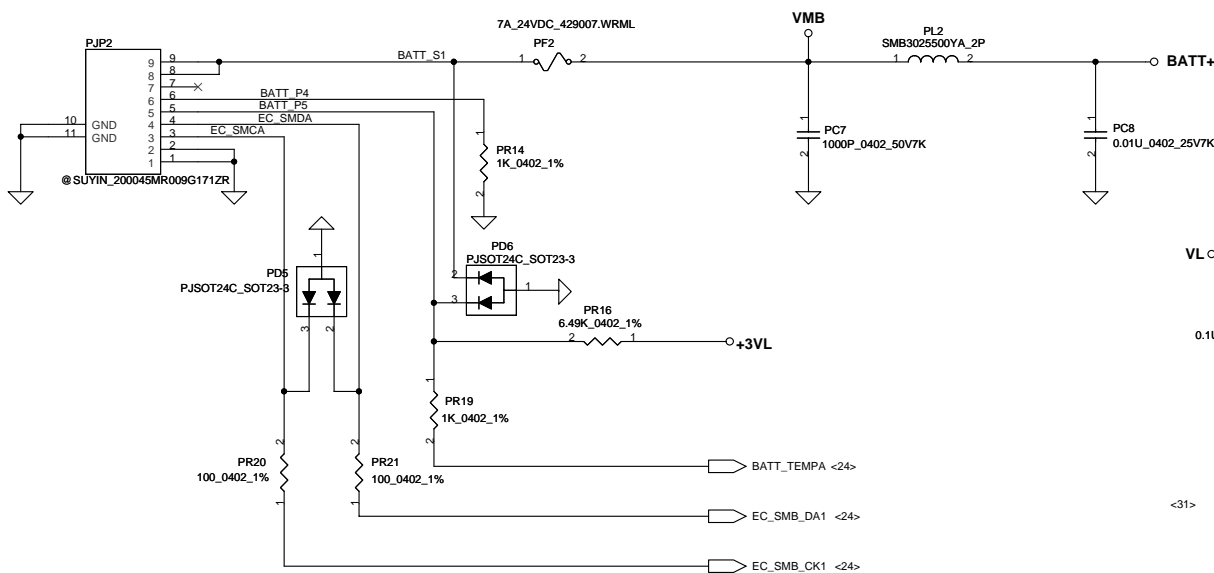
+1.8VSP 2 1 +1.8VS  
PJ180  
@JUMP\_43X118  
(3A,120mils ,Via NO.= 1)

+0.75VSP 2 1 +0.75VS  
PJ75  
@JUMP\_43X79  
(1A,40mils ,Via NO.= 3)

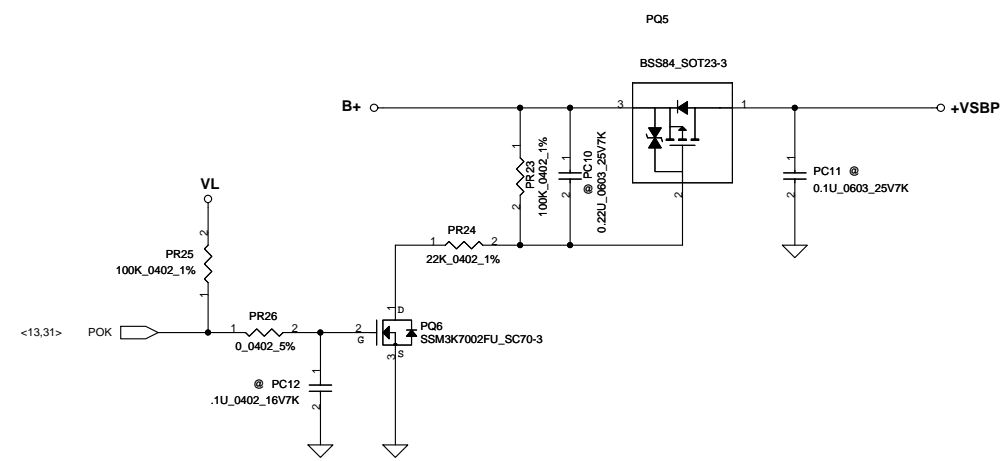
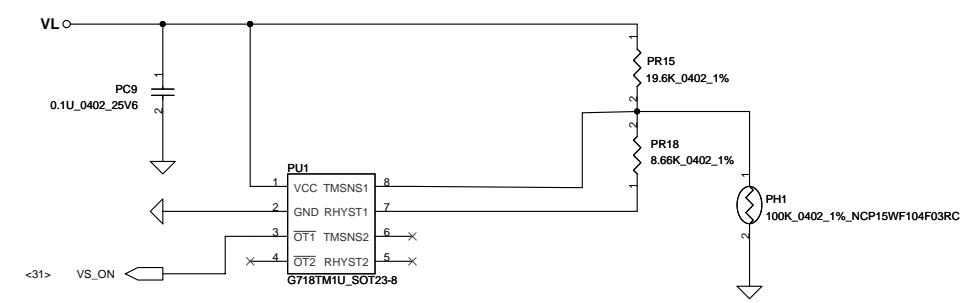
+0.89VSP 2 1 +0.89VS  
PJ89  
@JUMP\_43X118  
(2.6A,120mils ,Via NO.=6)

+3VLP 2 1 +3VL  
PJ331  
@JUMP\_43X39  
(100mA,40mils ,Via NO.= 2)

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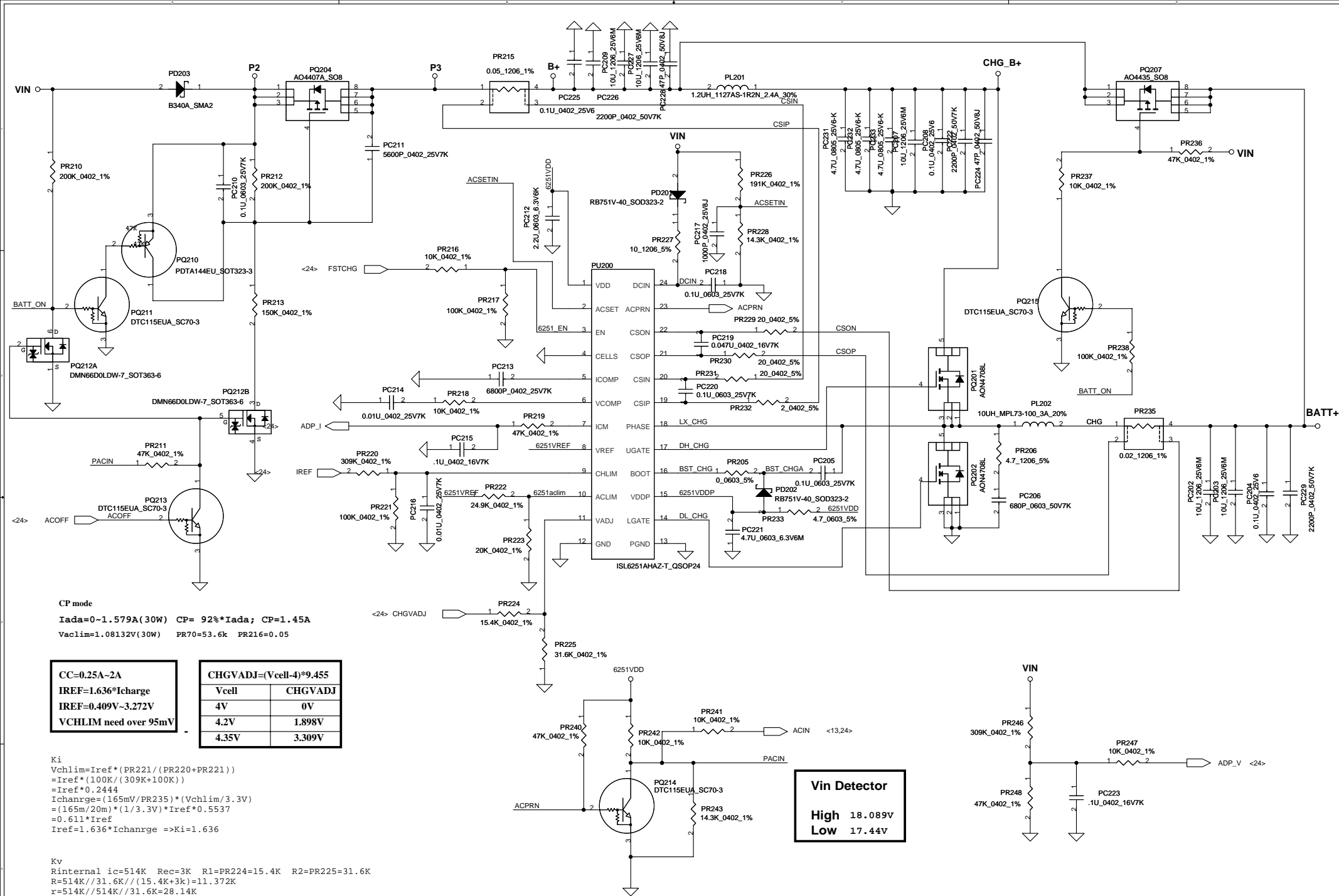


PH1 under CPU botten side :  
 CPU thermal protection at 95 degree C  
 Recovery at 56 degree C



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CP mode  
 $I_{ada}=0-1.579A(30W)$   $CP=92\% \cdot I_{ada}$ ;  $CP=1.45A$   
 $V_{aclim}=1.08132V(30W)$   $PR70=53.6k$   $PR216=0.05$

CC=0.25A~2A	
IREF=1.636*Icharge	
IREF=0.409V~3.272V	
VCHLIM need over 95mV	

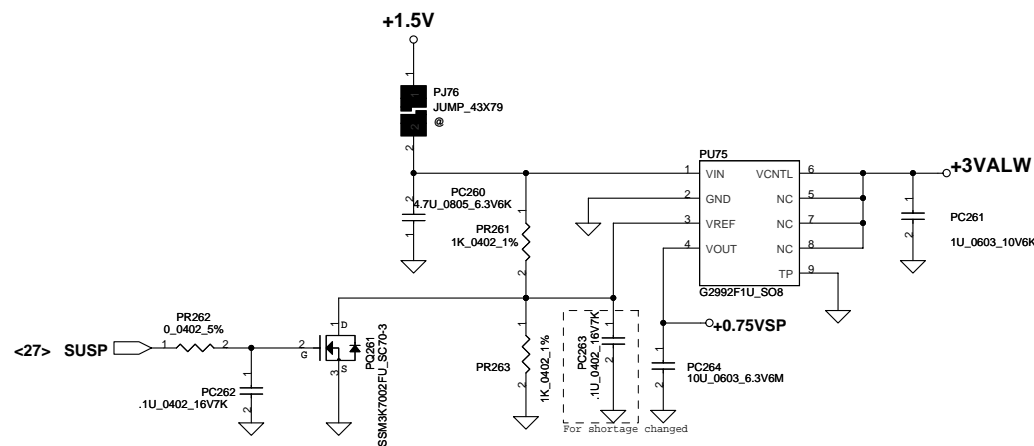
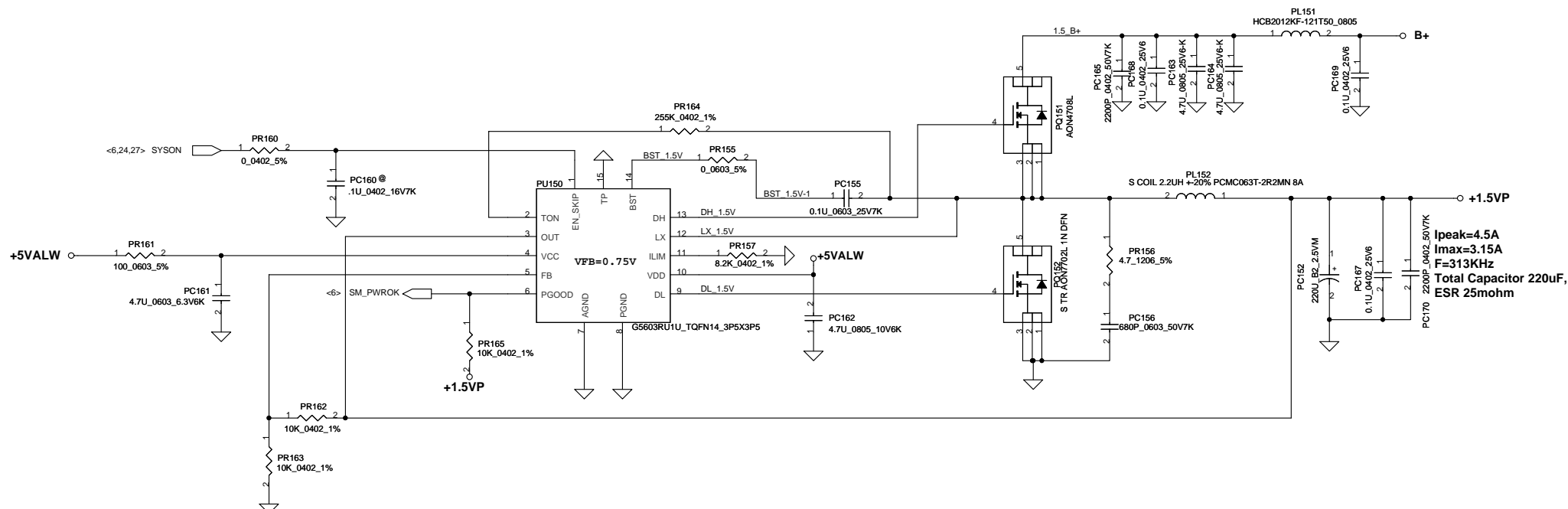
CHGVADJ=(Vcell-4)*9.455	
Vcell	CHGVADJ
4V	0V
4.2V	1.898V
4.35V	3.309V

Ki  
 $V_{chlim}=I_{ref} \cdot (PR221 / (PR220 + PR221))$   
 $= I_{ref} \cdot (100K / (309K + 100K))$   
 $= I_{ref} \cdot 0.2444$   
 $I_{chARGE} = (165mV / PR235) \cdot (V_{chlim} / 3.3V)$   
 $= (165m / 20m) \cdot (1 / 3.3V) \cdot I_{ref} \cdot 0.5537$   
 $= 0.611 \cdot I_{ref}$   
 $I_{ref} = 1.636 \cdot I_{chARGE} \Rightarrow Ki = 1.636$

Kv  
 Internal ic=514K Rec=3K R1=PR224=15.4K R2=PR225=31.6K  
 $R=514K // 31.6K // (15.4K + 3K) = 11.372K$   
 $r=514K // 514K // 31.6K = 28.14K$   
 $V_{cell} = 0.175 \cdot V_{adj} + 3.99V$   
 $4.2V = 0.175 \cdot V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$   
 $V_{adj} = V_{ref} \cdot (R / (R + 514K)) + CALIBRATE \cdot (r / (r + 514K))$   
 $1.1483 = CALIBRATE \cdot 0.6046 \Rightarrow CALIBRATE = 1.899$   
 $1.899 = (4.2 - (V_{cell} + A \cdot 0.175)) \cdot Kv = (4.2 - (4.2 + A \cdot 0.175)) \cdot Kv$   
 $A = V_{ref} \cdot (R / (R + 514K)) = 0.052$   
 $K1 = 4.5$

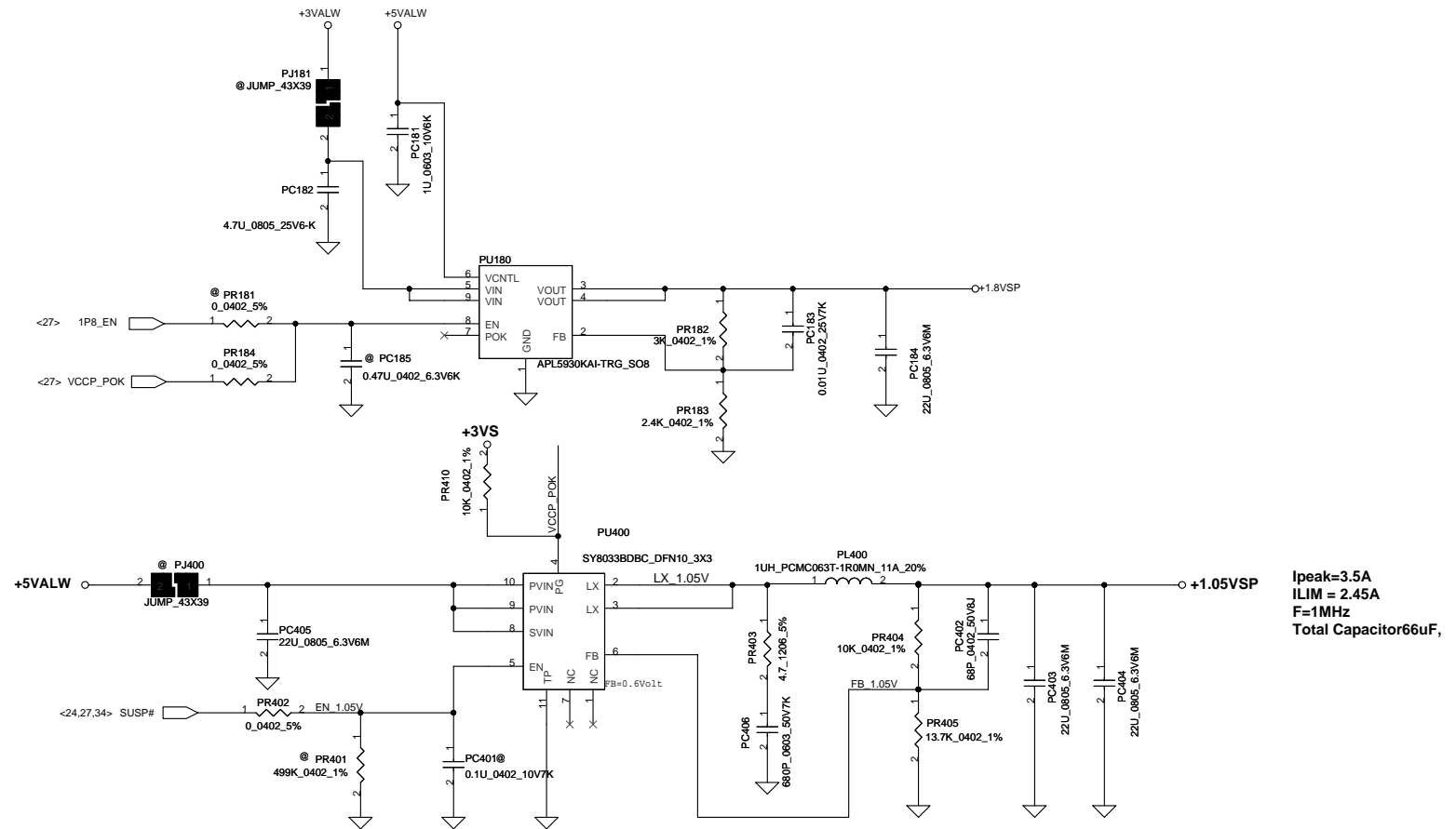
<b>Vin Detector</b>	
High	18.089V
Low	17.44V





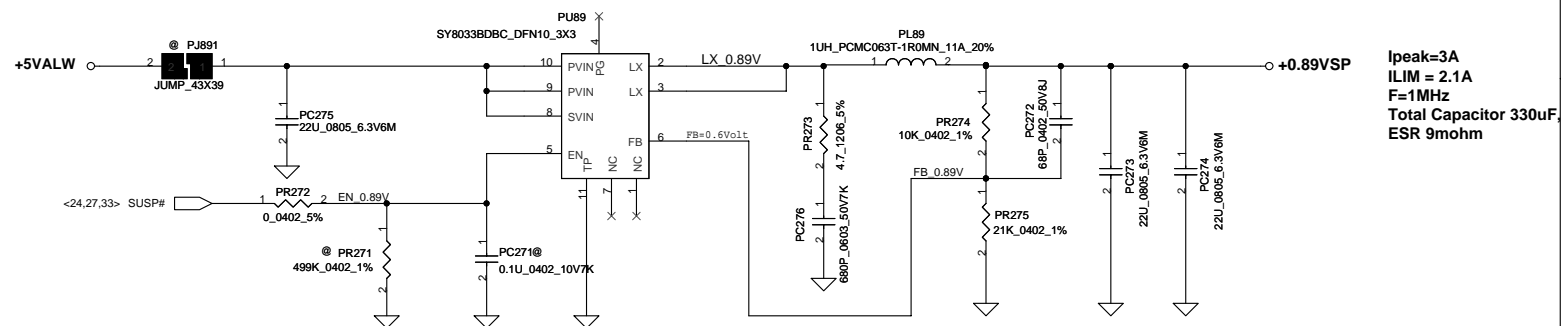
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Pin 1 define same with Pin 2 & Pin 3 that just for SY8035 ,  
SY8035 is for 5A loading , let LX shape can bigger!!

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NO DATE	PAGE	MODIFICATION LIST	PURPOSE
2010/8/23(DVT)	P32 +1.5VP/+0.75VSP	Change PU75 UP7711(SA00003XI00) -->G2992(SA00000VE80)	UPI had patent issue
2010/8/23(DVT)	P30 Charger	Change PU200 G5209(SA00003TK00) -->ISL6251(SA00001EP80)	G5209 had leakage issue
2010/8/23(DVT)	P31 +5VALWP/+3VALWP	Change PU330 UP6182(SA000043H00) -->TI51125A(SA000020C80)	UPI had patent issue
2010/8/23(DVT)	P30 Charger	add PR247(SD034100280) PC223(SE076104K80) PR246(SD034309380) PR248(SD034470280)	Support SA ECO unit
2010/8/23(DVT)	P35 CPU_CORE	Change PR526 174K (SD034174380) -->124K(SD034124380)	debug CPU load issue
2010/8/23(DVT)	All snuber	Change PC273,PC274,PC275,PC403,PC404,PC405 22u(SE000008L80) -->PC273,PC274,PC275,PC403,PC404,PC405 22u(SE000000I10)	Chose the same material s
2010/8/23(DVT)	P30 Charger	Install PC222 PC224 0.1u (SE00000G880)	EMI commond
2010/8/23(DVT)	P30 Charger	Install PC227,PC209,PC207,PC208,PC204 10u (SE142106M80)	EMI commond
2010/8/23(DVT)	P35 CPU_CORE	Change PL500(SM01000BY00)-->(SM01000C000)	Chose the same material s
2010/8/23(DVT)	P31 +5VALWP/+3VALWP	Install PC371,PC369 0.1u (SE00000G880)	RF commond
2010/8/23(DVT)	P31 +5VALWP/+3VALWP	Install PC367 2200P(SE074222K80)	RF commond
2010/8/23(DVT)	P32 +1.5VP	Install PC165 2200P(SE074222K80)	RF commond
2010/8/23(DVT)	P32 +1.5VP	Install PC169,PC168,PC167 0.1u(SE00000G880)	RF commond
2010/8/23(DVT)	P35 CPU_CORE	add PC518 (SE071101J80)	debug CPU VR-ON issue
2010/9/21(PVT)	P30 Charger	Install PC225 PC208PC204 ( 0.1u) , PC226 PC222 PC229(2200P) Add PC208 add PC228 PC224 (47P),install snubber PR206,PC206	RF commond
2010/9/21(PVT)	P31 +5VALWP/+3VALWP	Add PC372 PC374(0.1u) , PC375(47P) PC371 (2200P)	RF commond
2010/9/21(PVT)	P32 +1.5VP	Add PC170(2200P) install snubber PR156 PC156	RF commond
2010/10/8(pre-MP)	P30 Charger	Change PL210 to 1.2u (SH00000B100)	EMI commond
2010/10/08(Pre-MP)	P31 +5VALWP/+3VALWP	Change PC332 & PC352 to ESR 45 m ohm	cost down plane
2010/10/08(Pre-MP)	P32 +1.5VP	Change PC152 to ESR 35 m ohm	cost down plane
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