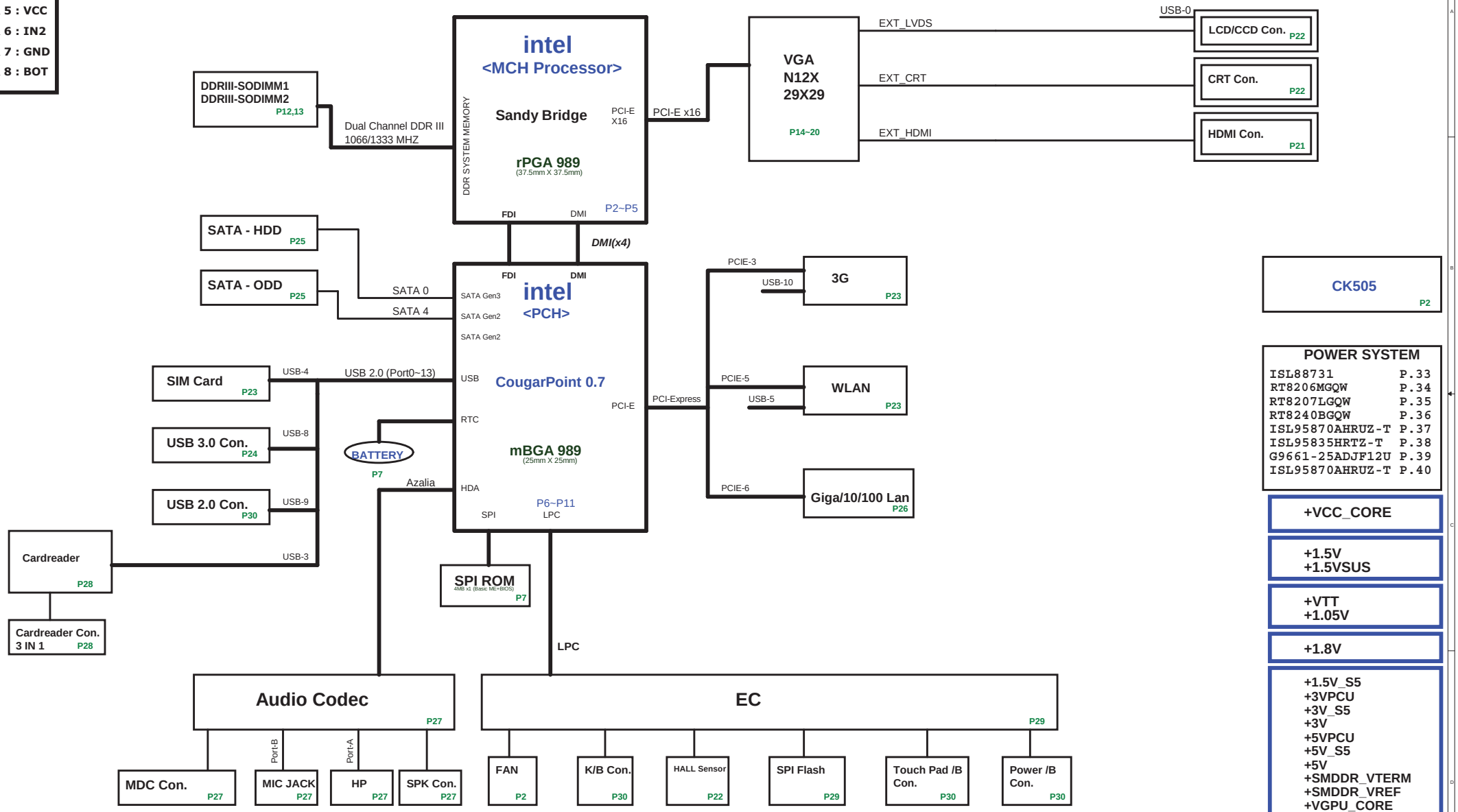
BLBD Block Diagram

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : GND
- LAYER 5 : VCC
- LAYER 6 : IN2
- LAYER 7 : GND
- LAYER 8 : BOT



CK505 P2

POWER SYSTEM

ISL88731	P.33
RT8206MGQW	P.34
RT8207LGQW	P.35
RT8240BGQW	P.36
ISL95870AHRUZ-T	P.37
ISL95835HRTZ-T	P.38
G9661-25ADJF12U	P.39
ISL95870AHRUZ-T	P.40

- +VCC_CORE
- +1.5V
  +1.5VSUS
- +VTT
  +1.05V
- +1.8V
- +1.5V_S5
  +3VPCU
  +3V_S5
  +3V
  +5VPCU
  +5V_S5
  +5V
  +SMDDR_VTERM
  +SMDDR_VREF
  +VGPU_CORE
  +VAXG

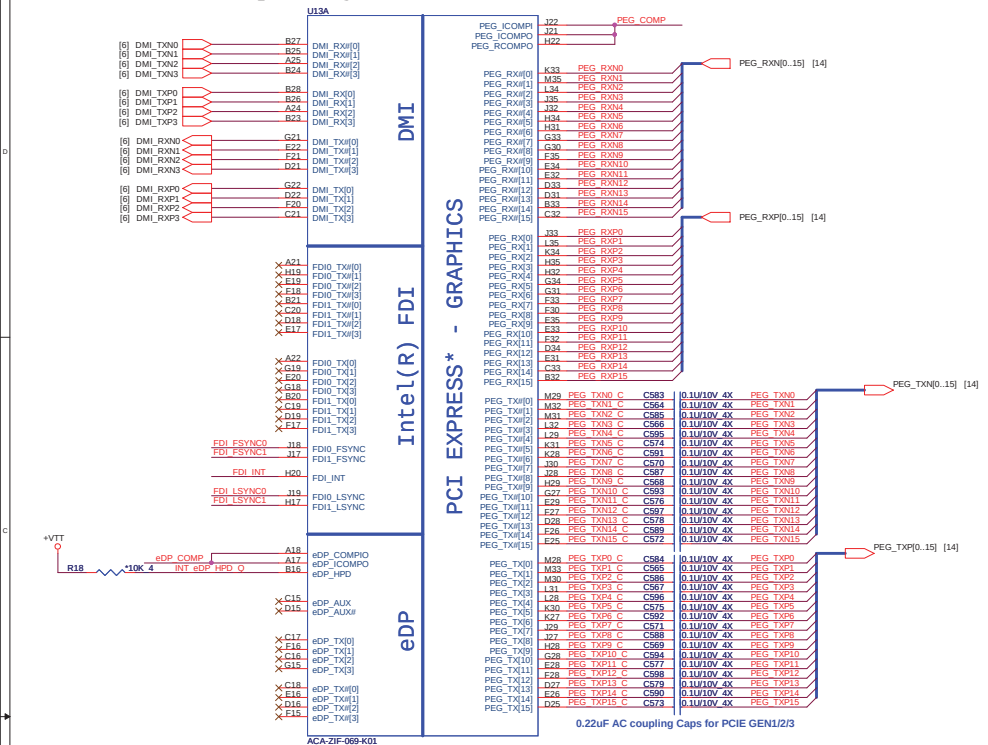
Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	Block Diagram	1A

Date: Monday, November 22, 2010 Sheet 1 of 42

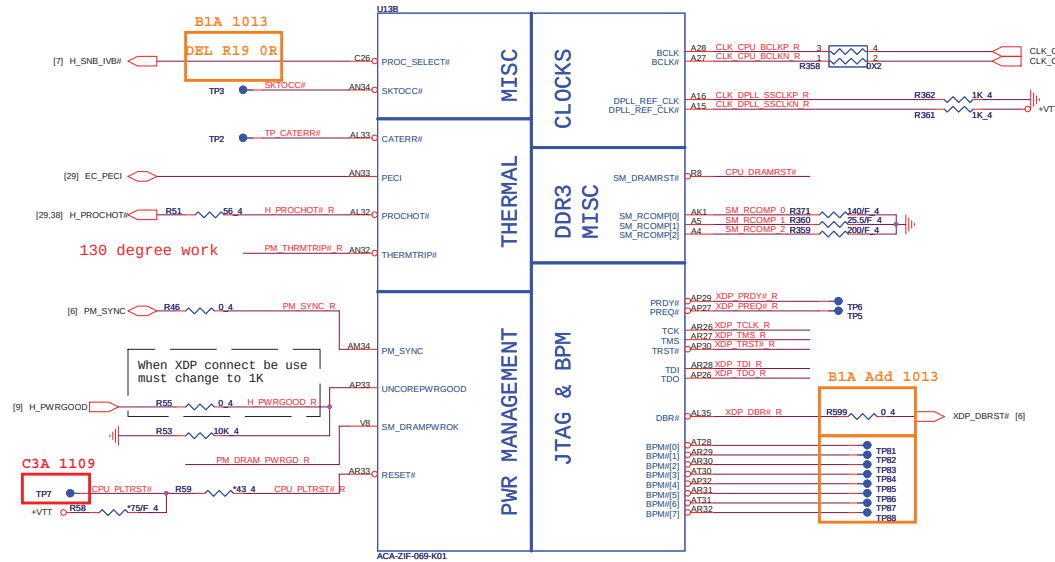
Sandy Bridge Processor (DMI,PEG,FDI)

02

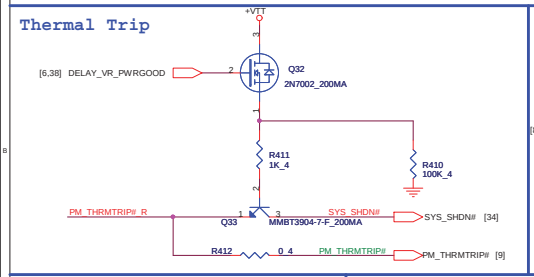


Sandy Bridge Processor (CLK,MISC,JTAG)

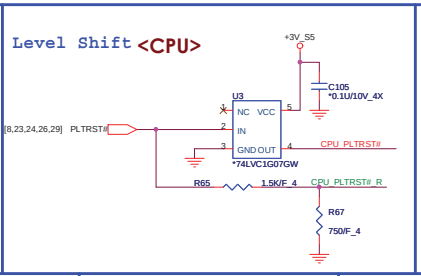
SNB_IVB# N.A at SNB EDS #27637 0.7v1



Thermal Trip

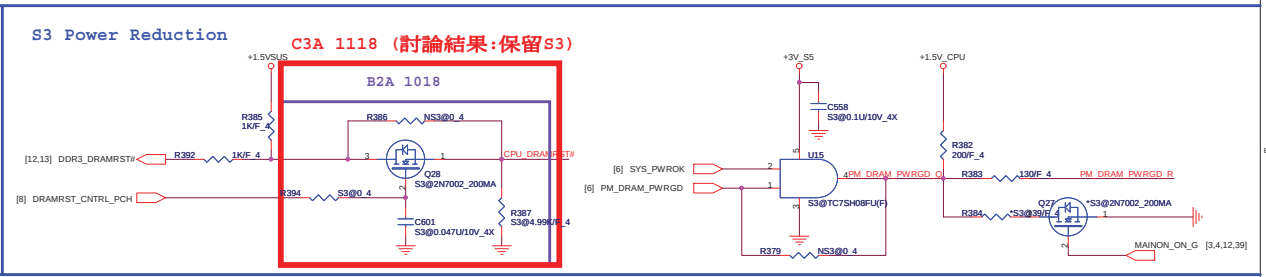


Level Shift <CPU>

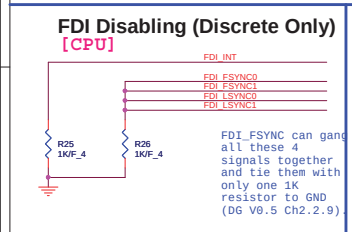


S3 Power Reduction

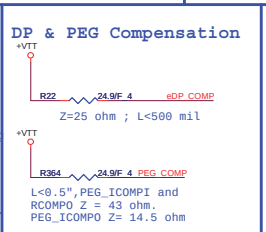
C3A 1118 (討論結果:保留S3)



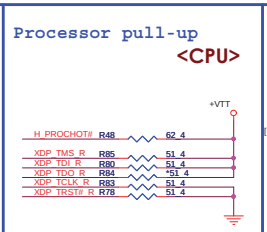
FDI Disabling (Discrete Only) [CPU]



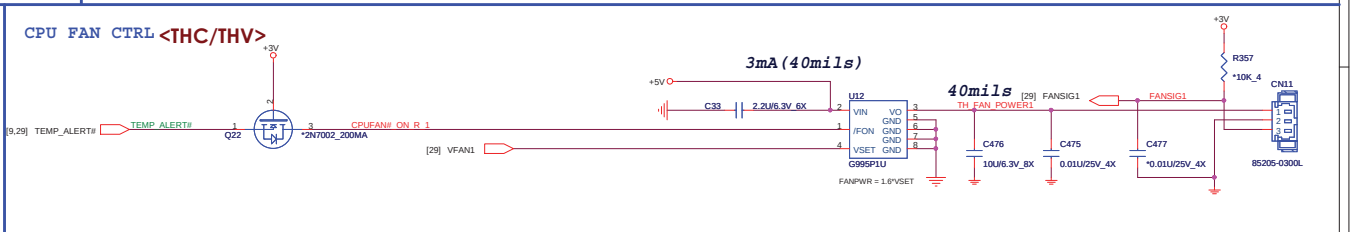
DP & PEG Compensation



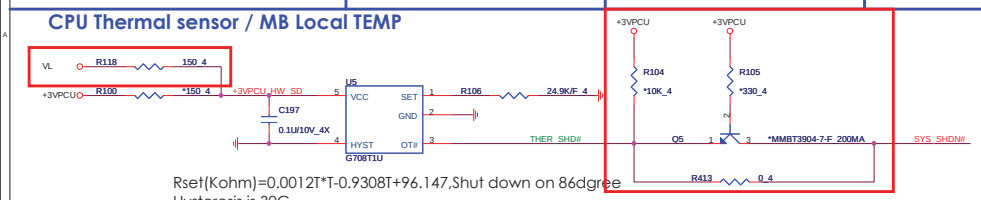
Processor pull-up <CPU>



CPU FAN CTRL <THC/THV>



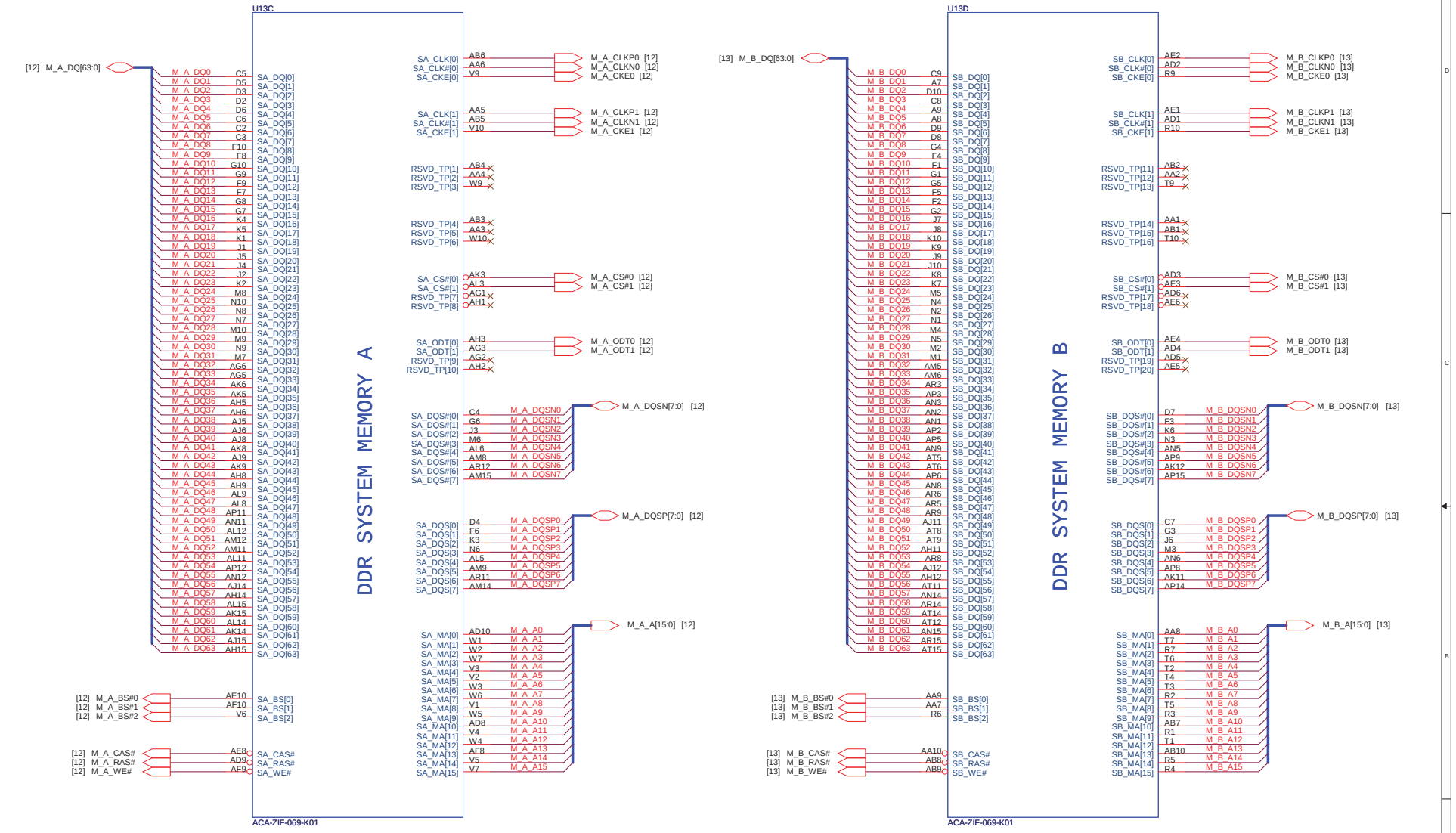
CPU Thermal sensor / MB Local TEMP

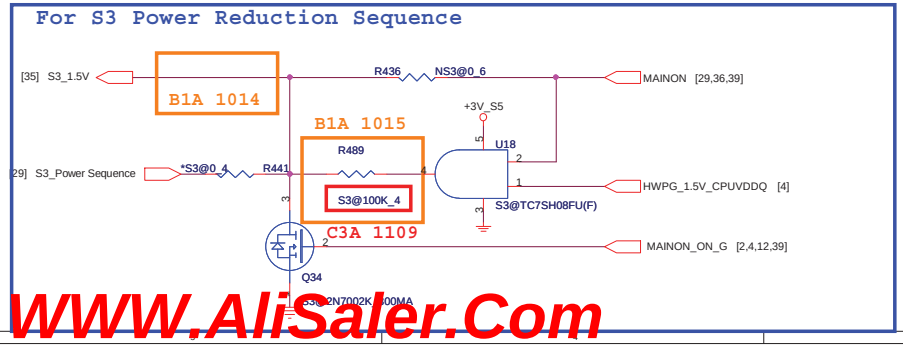


Quanta Computer Inc.
PROJECT : BLBD
Size | Document Number: Sandy Bridge 1/4 | Rev 1A
Date: Monday, November 22, 2010 | Sheet 2 of 42

Sandy Bridge Processor (DDR3)

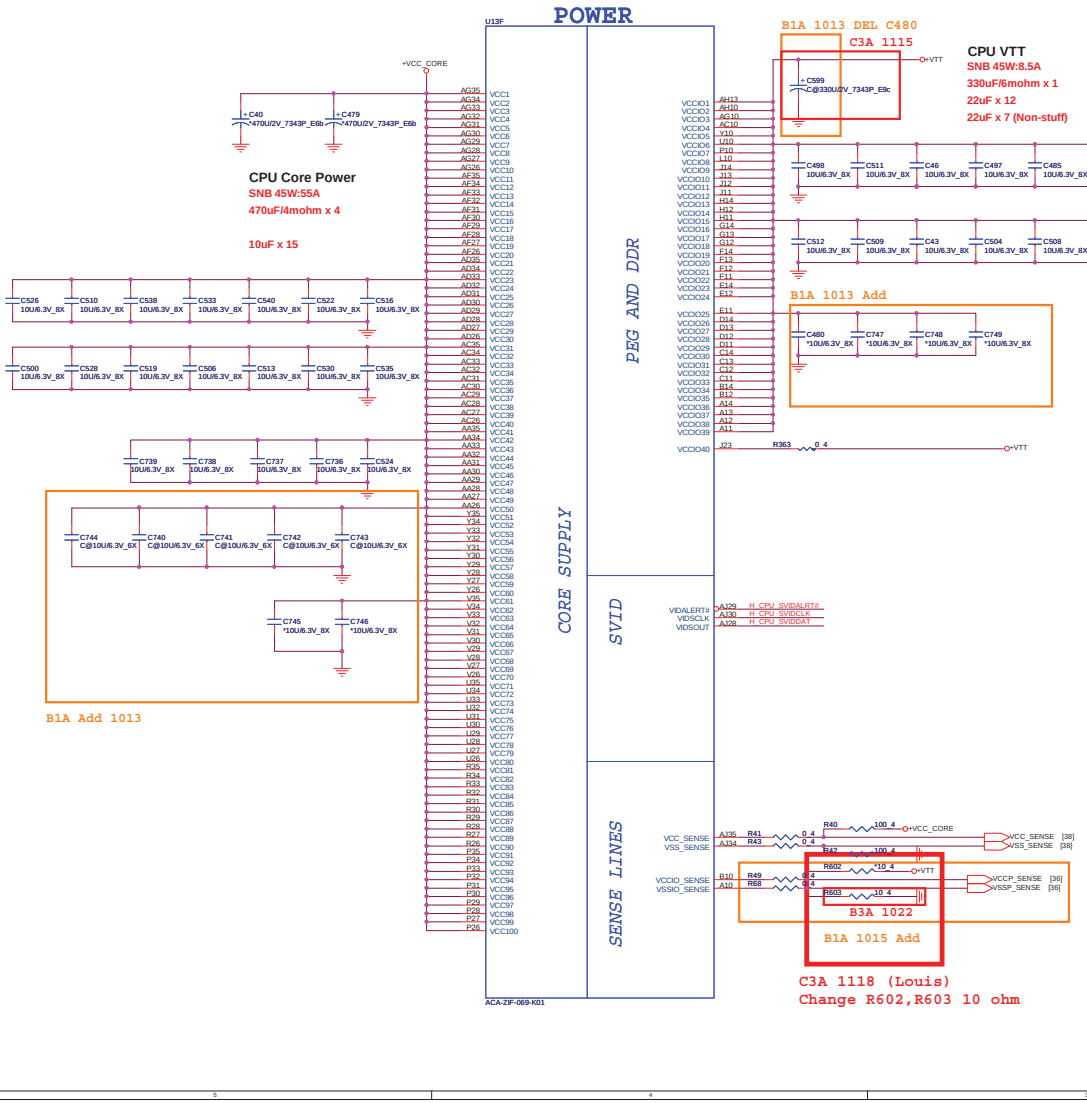
03



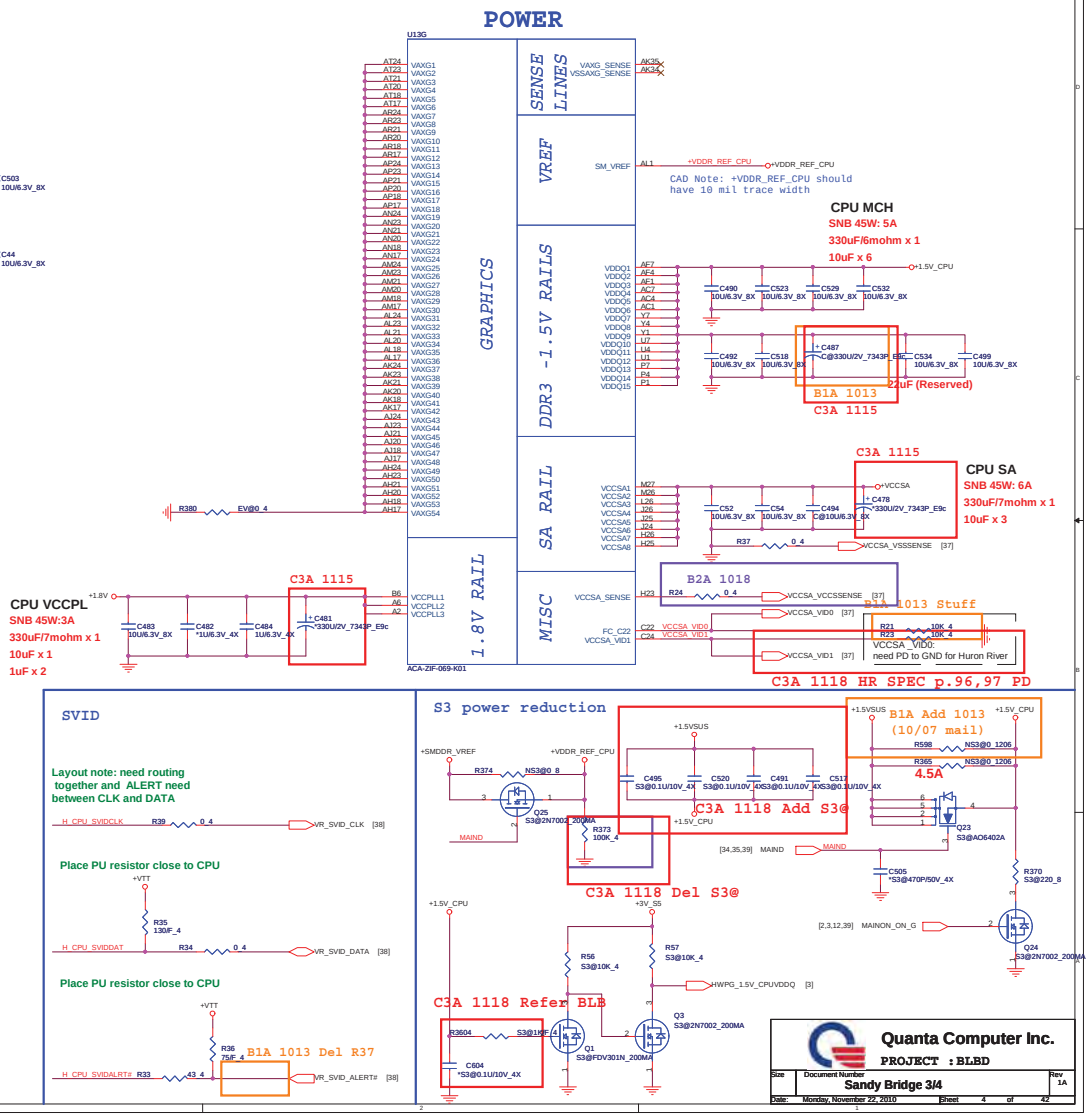


Quanta Computer Inc.			
PROJECT : BLBD			
Size	Document Number		Rev
	Sandy Bridge 2/4		1A
Date: Monday, November 22, 2010	Sheet 3 of 42		

Sandy Bridge Processor (POWER)

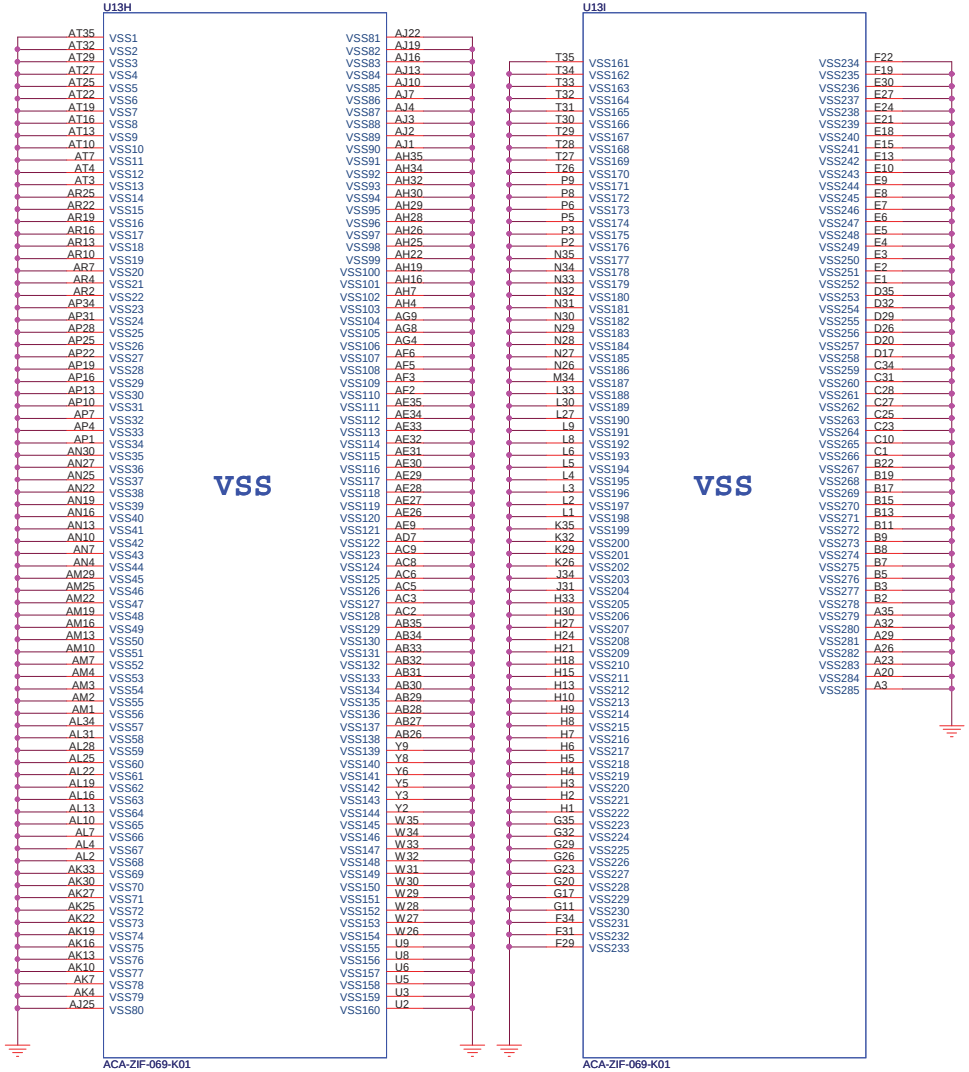


Sandy Bridge Processor (GRAPHIC POWER)

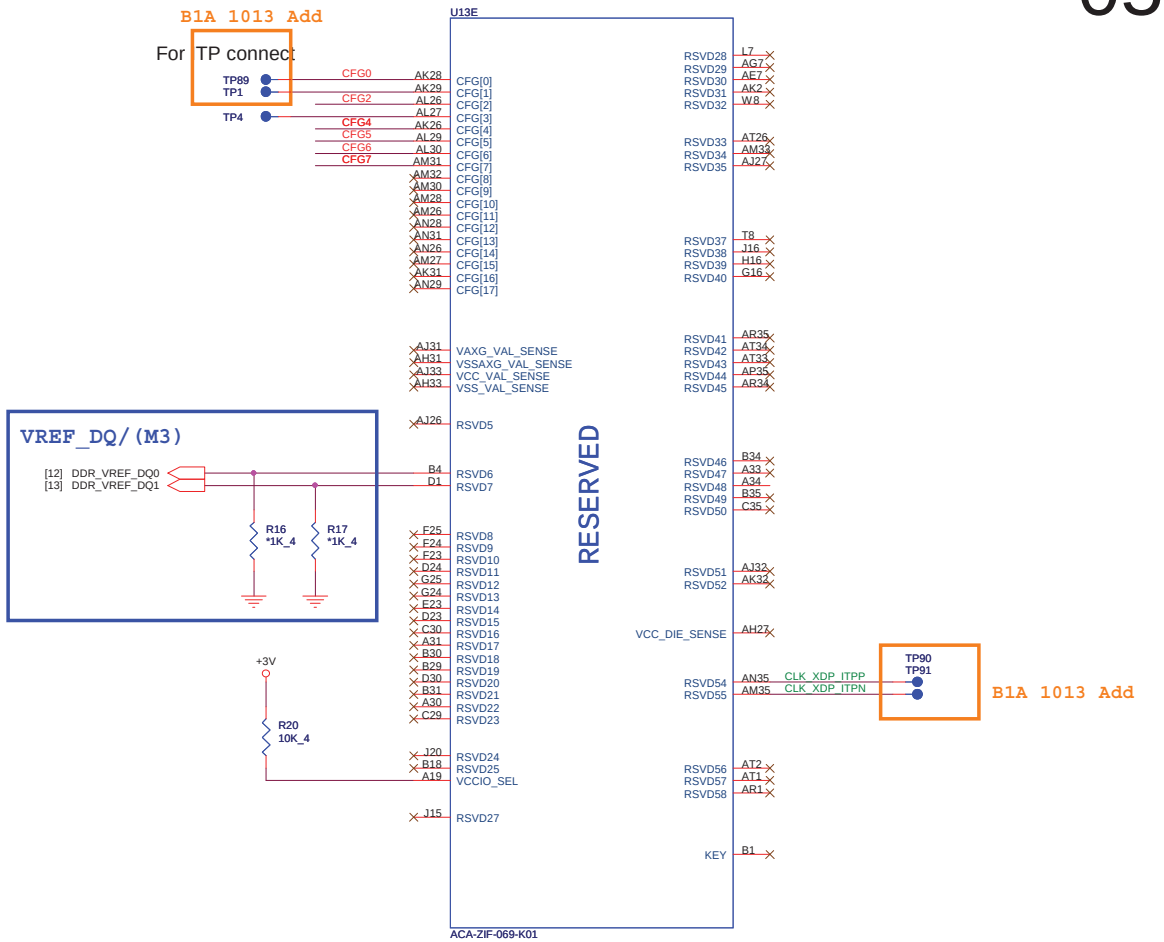


Quanta Computer Inc.
PROJECT : BLBD
Size: Document Number: Sandy Bridge 3/4 Rev: 1A
Date: Monday, November 22, 2010 Sheet 4 of 42

Sandy Bridge Processor (GND)



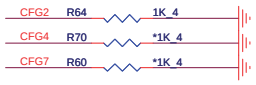
Sandy Bridge Processor (RESERVED, CFG)

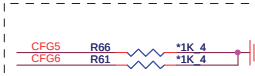


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	**Normal Operation**	Lane Reversed
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





CFG[6:5] (PCIE Port Bifurcation Straps)

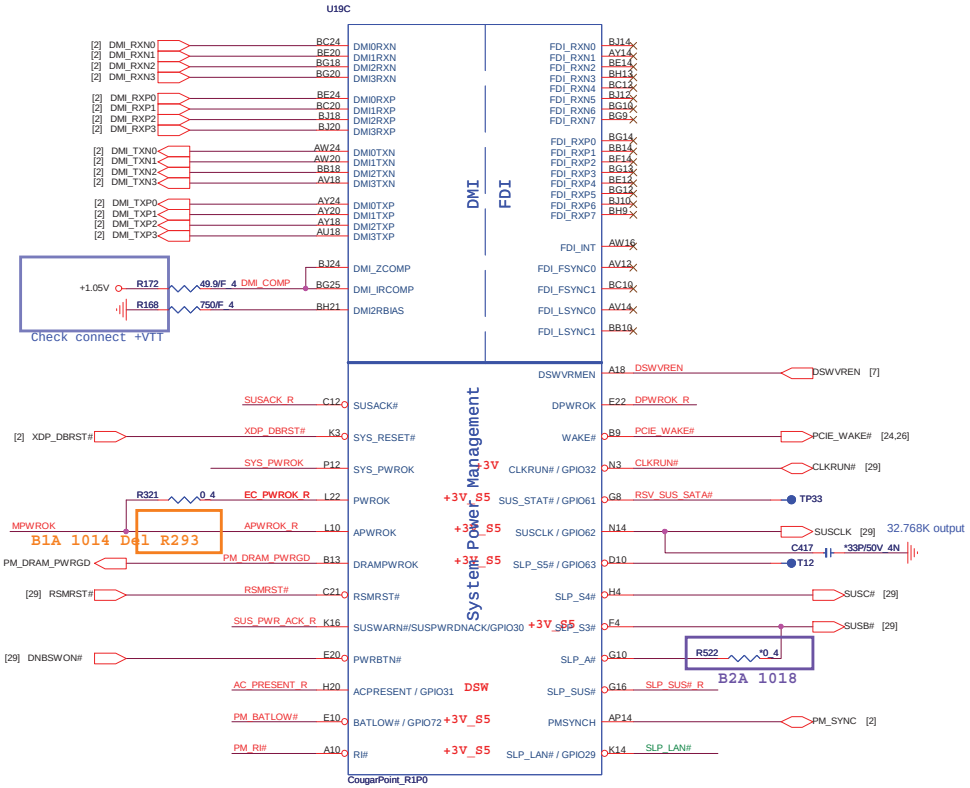
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Quanta Computer Inc.
PROJECT : BLBD

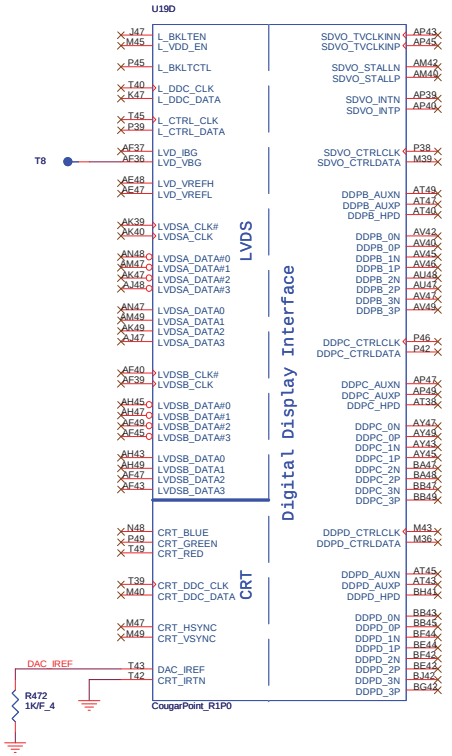
Size	Document Number	Rev
	Sandy Bridge 4/4	1A

Date: Monday, November 22, 2010 Sheet 5 of 42

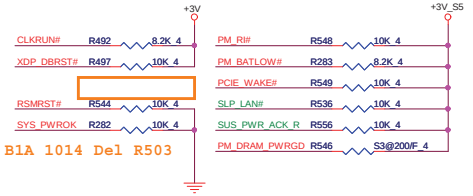
Cougar Point (DMI,FDI,PM)



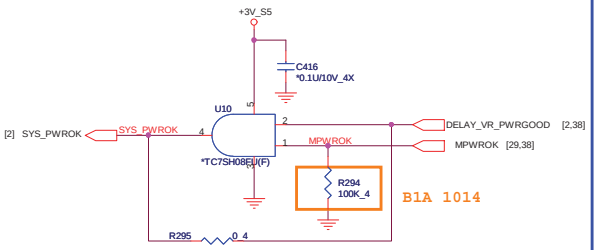
Cougar Point (LVDS,DDI)



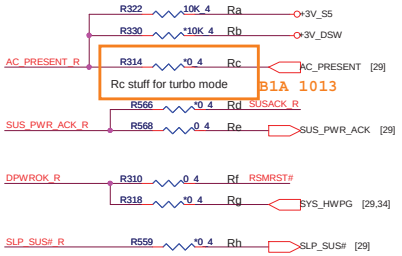
PCH Pull-high/low(CLG)



System PWR_OK(CLG)



Deep Sx



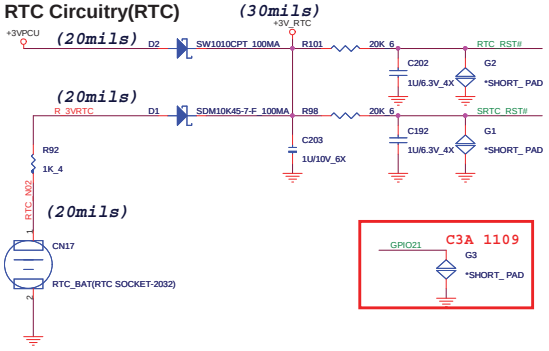
Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

Quanta Computer Inc.
PROJECT : BLBD

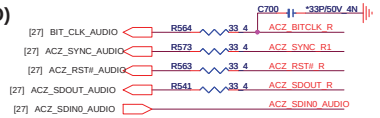
Size	Document Number	Rev
	Cougar Point 1/6	1A

Date: Monday, November 22, 2010 Sheet 6 of 42

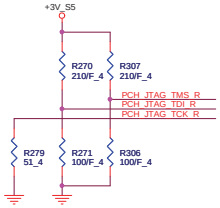
RTC Circuitry(RTC)



HDA Bus(ADO)

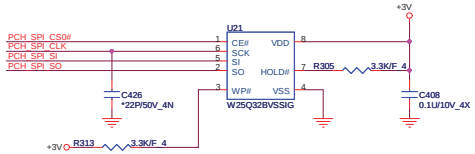


PCH JTAG Debug (CLG)



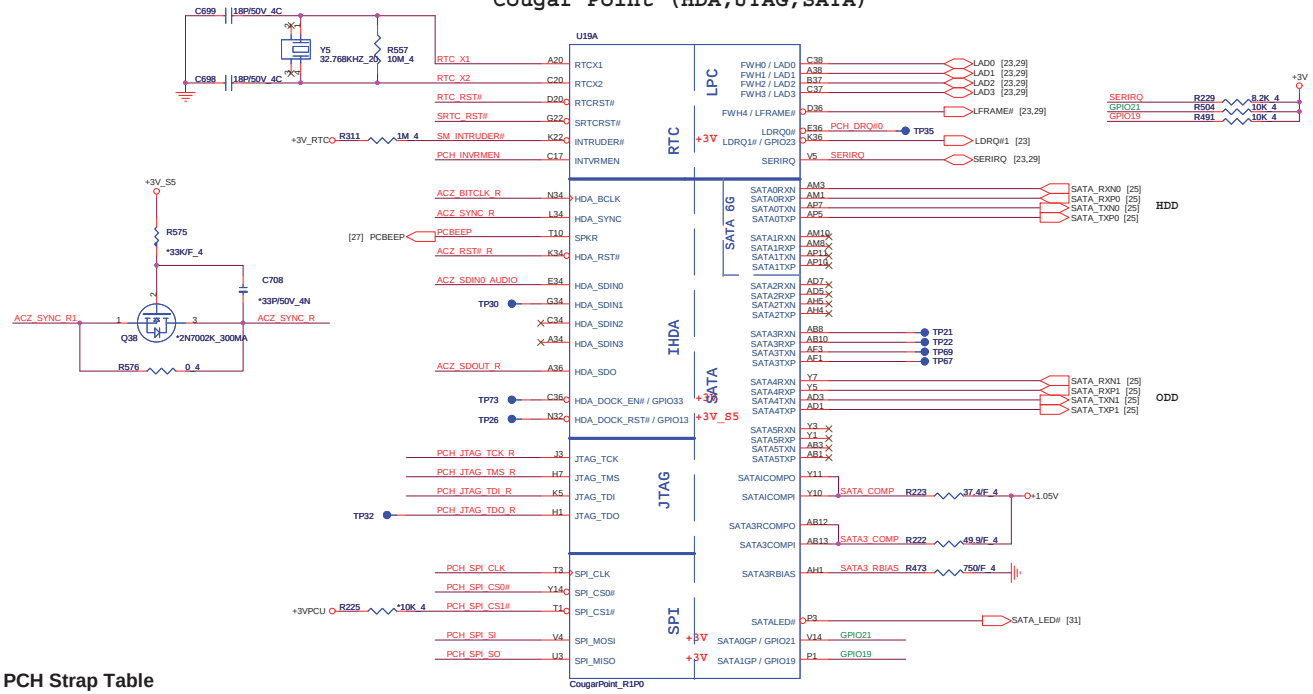
PCH Dual SPI (CLG)

MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031



PCH2 (CLG)

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R245 *1K_4 PCBEEP
INIT3_3V#	**Reserved**	PWROK	1 = Default (weak pull-up 20K)	**Should not pull low. leave as No Connect**
GNT3#/ GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R531 *1K_4 PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R545 330K_4 PCH_INVRMEN
GNT1#/ GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]**
SATA1GP/ GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R527 *1K_4 GNT1 [8] R490 *1K_4 GPIO19
GNT2#/ GPIO53	**ESI Strap (Server Only)**	PWROK	1 = Default. Should not be pulled low for desktop and mobile	**Should not pull low for desktop and mobile**
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Default (weak pull-up 20K) 1 = Override	+3V R542 *1K_4 ACZ_SDOUT_R ACZ_SDOUT_R [29]
DF_TVS	**DMI/FDI Termination voltage**	**PWROK**	**0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**	R448 2.2K_4 R447 4.7K_4 +1.8V DF_TVS [9] H_SNB_IVB# [2]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R248 *1K_4 PLL_ODVR_EN [9]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Default. Support by 1.8V 1 = Support by 1.5V	+3V_S5 R577 1K_4 ACZ_SYNC_R
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS no Confidentiality 1 = TLS Confidentiality	+3V_S5 R518 1K_4 GPIO15 GPIO15 [9]
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	DSWVREN [6] +3V_RTC R537 330K_4 R552 *330K_4
SATA2GP/ GPIO36	**Reserved**	PWROK	0 = Default	**Should not be pulled hight when strap is sampled**
SATA3GP/ GPIO37	**Reserved**	PWROK	0 = Default	**Should not be pulled hight when strap is sampled**

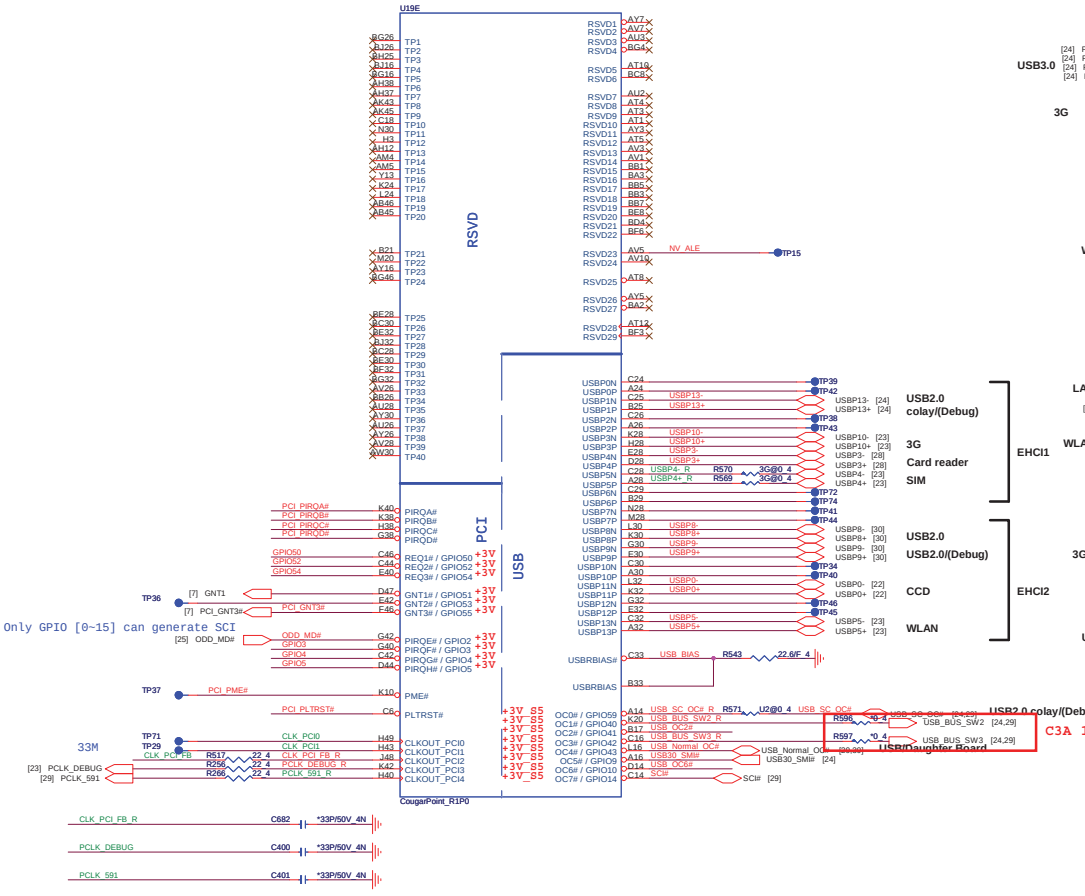
Check List 1.0 :
Needs to be pulled High for Huron River platform.

Quanta Computer Inc.
PROJECT :BLBD

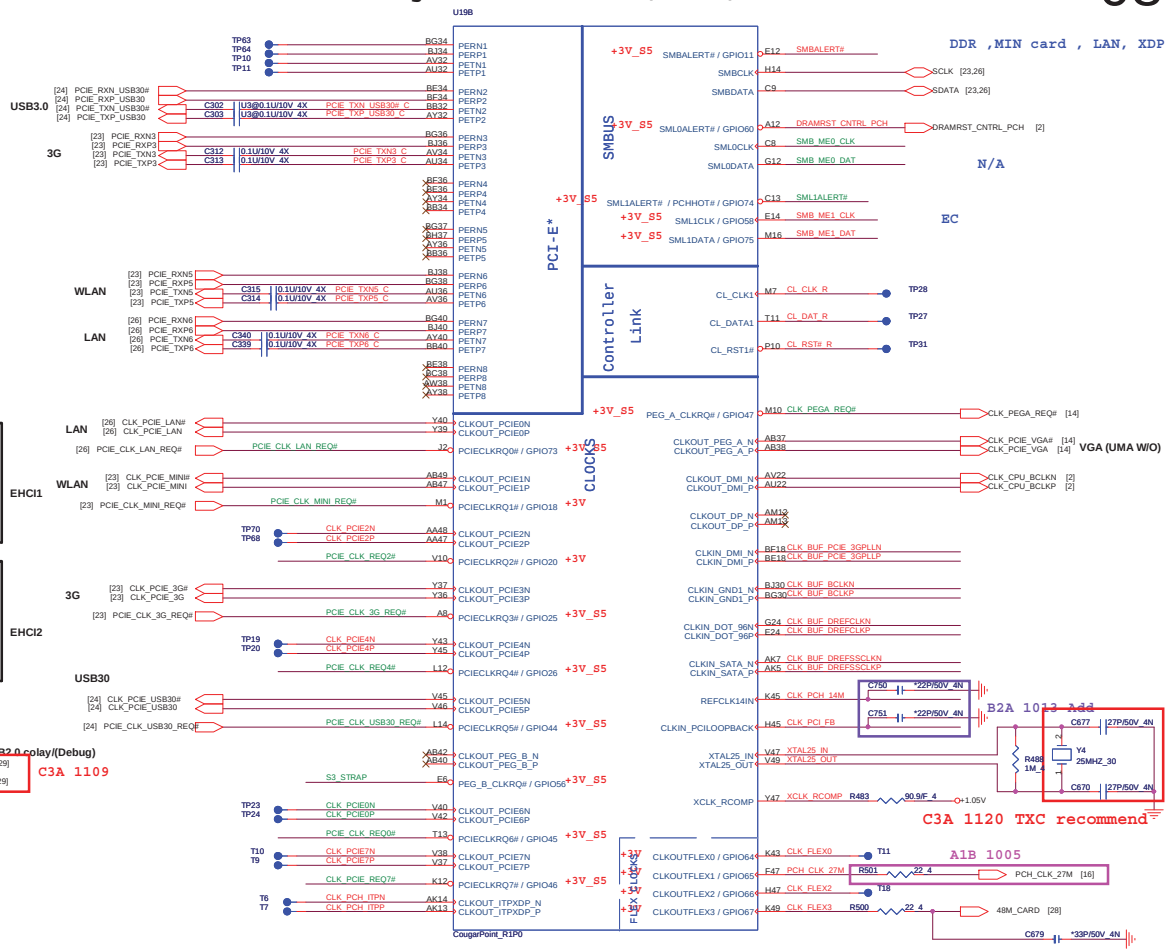
Size	Document Number	Rev
	Cougar Point 2/6	1A

Date: Monday, November 22, 2010 Sheet 7 of 42

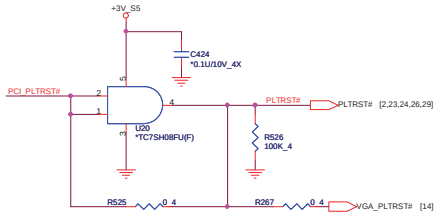
Cougar Point-M (PCI,USB,NVRAM)



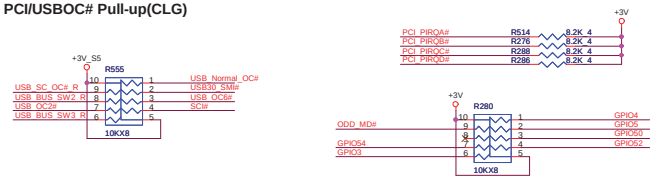
Cougar Point-M (PCI-E,SMBUS,CLK)



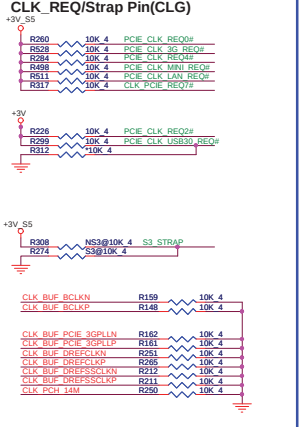
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)

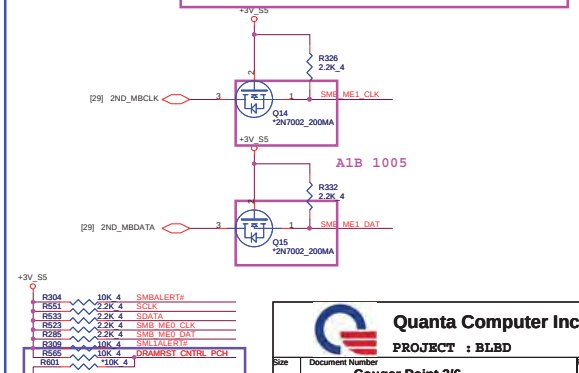


CLK_REQ/Strap Pin(CLG)



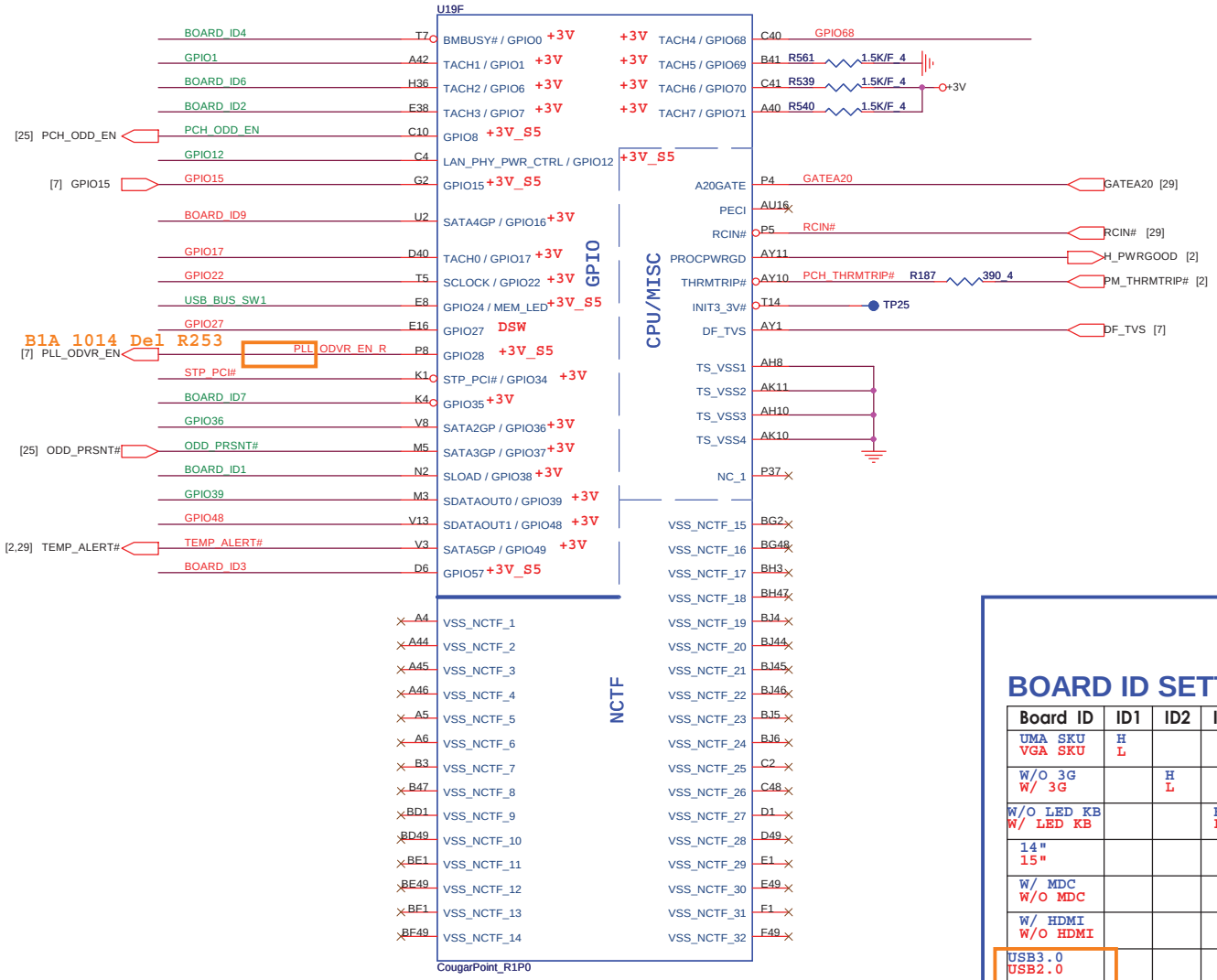
SMBus/Pull-up(CLG)

cost down the isolate parts
EC does not read SMBUS of PCH 0928 mail

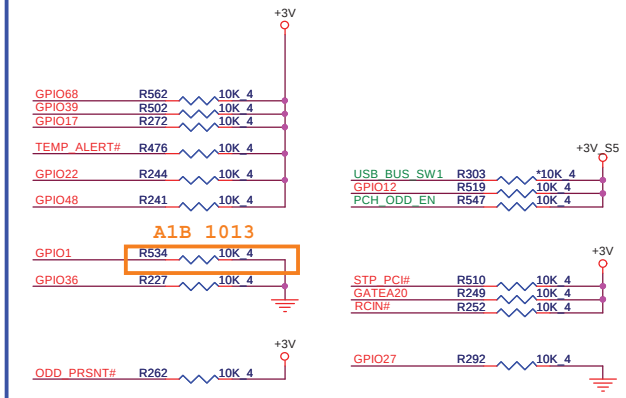


Quanta Computer Inc.	
PROJECT : BLBD	
Size	Document Number: Cougar Point 3/6
Rev	1A
Date: Monday, November 22, 2010	Sheet 8 of 42

Cougar Point (GPIO,VSS_NCTF,RSVD)



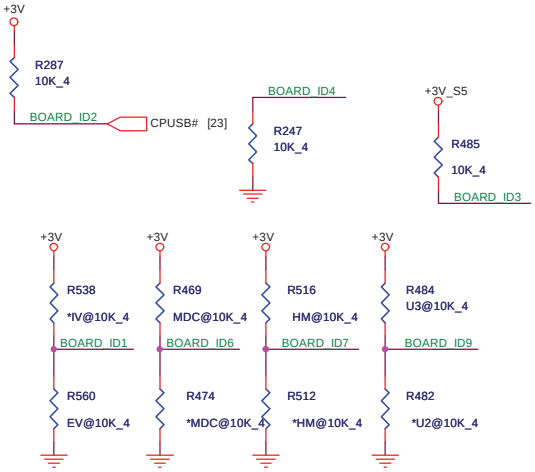
GPIO Pull-up/Pull-down(CLG)



BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID6	ID7	ID9
UMA SKU VGA SKU	H L						
W/O 3G W/ 3G		H L					
W/O LED KB W/ LED KB			H L				
14" 15"				H L			
W/ MDC W/O MDC					H L		
W/ HDMI W/O HDMI						H L	
USB3.0 USB2.0							H L

B1A 1014



Quanta Computer Inc.

PROJECT : BLBD

Size	Document Number	Rev
	Cougar Point 4/6	1A
Date: Monday, November 22, 2010	Sheet 9 of 42	

COUGAR POINT (POWER)

B1A 1018
Add R604

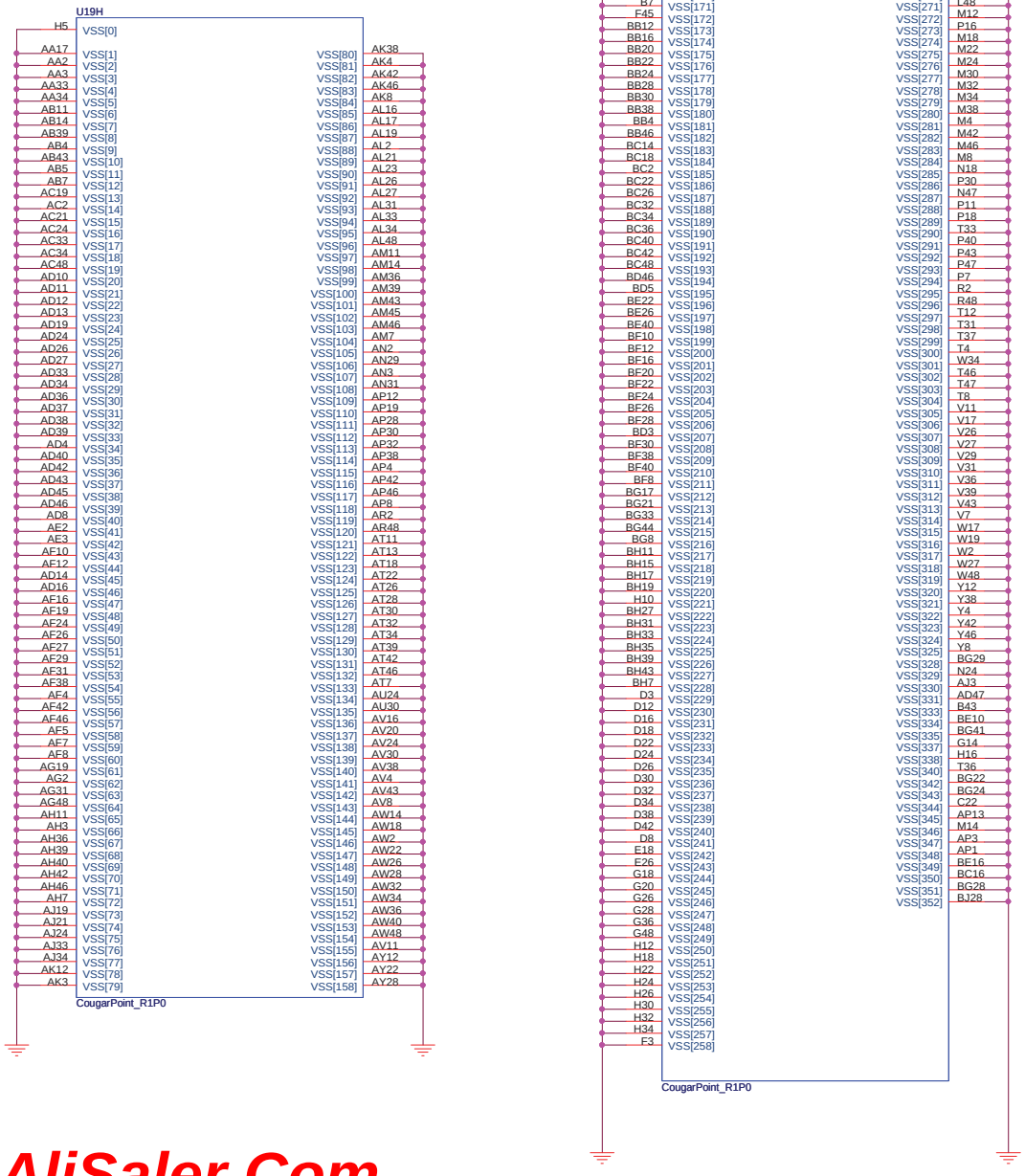
VccADAC =1mA(8mils)
VccALVDS=1mA(8mils)
VccTX_LVDS=60mA(10mils)
VccCORE =1.3 A(60mils)
VccIO =2.925 A(140mils)
VccASW =1.01 A(60mils)
VCCDMI = 42mA(10mils)
VCCCLKDMI = 20mA(8mils)
VCCPNAND = 190 mA(15mils)
VCCSPI = 20mA(8mils)
VCCVRM: 1.8V (Destop) 02/20 del for Pre-ES1
1.5V (Mobile)
Del R455
C3A 1109
B1A 1014 Add
B1A 1014

Cougar Point-M (POWER)

Deep Sx
VCCDSW3_3= 3mA
VCCME(+1.05V) = ??A(??mils)
65mA(10mils)
8mA(8mils)
VCCDIFFCLKN= 55mA(10mils)
VCCSSC= 95mA(10mils)
1mA(8mils)
VCCRTC<1mA(8mils)
VCCVRM= 114mA(15mils)
VCCSUS3_3 = 119mA(15mils)
V5REF= 1mA
VCCPCORE = 28mA(10mils)
VCCME = 1.01A(60mils)
VCCSUSHDA= 10mA(8mils)

Quanta Computer Inc.
PROJECT : BLBD
Size | Document Number: Cougar Point 5/6 | Rev: 1A
Date: Monday, November 22, 2010 | Sheet 10 of 42

IBEX PEAK-M (GND)



Quanta Computer Inc.

PROJECT : BLBD

Size	Document Number	Rev
	Cougar Point 6/6	1A
Date: Monday, November 22, 2010	Sheet 11 of 42	

H=4

JDIM2A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

JDIM2B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

VREF_DQ/(M3)

B1A 1014 Add

Place these Caps near So-Dimm0.

VREF_DQ/(M1)

S3 Power Reduction

Quanta Computer Inc.

PROJECT : BLBD

Size	Document Number	Rev
	DDR3 DIMM-0	1A

Date: Monday, November 22, 2010 Sheet 12 of 42

H=8

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP4B

[3] M_B_A[15:0]

M_B_A0 98
M_B_A1 97
M_B_A2 96
M_B_A3 95
M_B_A4 92
M_B_A5 91
M_B_A6 90
M_B_A7 86
M_B_A8 89
M_B_A9 85
M_B_A10 107
M_B_A11 84
M_B_A12 83
M_B_A13 119
M_B_A14 80
M_B_A15 78

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14 A15

[3] M_B_BS#0 109
[3] M_B_BS#1 108
[3] M_B_BS#2 79
[3] M_B_CS#0 114
[3] M_B_CS#1 121
[3] M_B_CLKP0 101
[3] M_B_CLKN0 103
[3] M_B_CLKP1 102
[3] M_B_CLKN1 104
[3] M_B_CKE0 73
[3] M_B_CKE1 74
[3] M_B_CAS# 115
[3] M_B_RAS# 110
[3] M_B_WE# 113

BA0 BA1 BA2 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE#

+3V
R54 10K/F_4 DIMM1_SA0 197
R52 10K/F_4 DIMM1_SA1 201

SA0 SA1

[12,23] CGCLK_SMB 202
[12,23] CGDAT_SMB 200

SCL SDA

[3] M_B_ODT0 116
[3] M_B_ODT1 120

ODT0 ODT1

11 28 46 63 136 153 170 187

DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

[3] M_B_DQSP[7:0]

M_B_DQSP0 12
M_B_DQSP1 29
M_B_DQSP2 47
M_B_DQSP3 64
M_B_DQSP4 137
M_B_DQSP5 154
M_B_DQSP6 171
M_B_DQSP7 188

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

[3] M_B_DQSN[7:0]

M_B_DQSN0 10
M_B_DQSN1 27
M_B_DQSN2 45
M_B_DQSN3 62
M_B_DQSN4 135
M_B_DQSN5 152
M_B_DQSN6 169
M_B_DQSN7 186

DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

M_B_DQ[63:0] [3]

M_B_DQ0 5
M_B_DQ1 7
M_B_DQ2 15
M_B_DQ3 17
M_B_DQ4 4
M_B_DQ5 6
M_B_DQ6 16
M_B_DQ7 18
M_B_DQ8 21
M_B_DQ9 23
M_B_DQ10 33
M_B_DQ11 35
M_B_DQ12 22
M_B_DQ13 24
M_B_DQ14 34
M_B_DQ15 36
M_B_DQ16 39
M_B_DQ17 41
M_B_DQ18 51
M_B_DQ19 53
M_B_DQ20 40
M_B_DQ21 42
M_B_DQ22 50
M_B_DQ23 52
M_B_DQ24 57
M_B_DQ25 59
M_B_DQ26 67
M_B_DQ27 69
M_B_DQ28 56
M_B_DQ29 58
M_B_DQ30 68
M_B_DQ31 70
M_B_DQ32 129
M_B_DQ33 131
M_B_DQ34 141
M_B_DQ35 143
M_B_DQ36 130
M_B_DQ37 132
M_B_DQ38 140
M_B_DQ39 142
M_B_DQ40 147
M_B_DQ41 149
M_B_DQ42 157
M_B_DQ43 159
M_B_DQ44 146
M_B_DQ45 148
M_B_DQ46 158
M_B_DQ47 160
M_B_DQ48 163
M_B_DQ49 165
M_B_DQ50 175
M_B_DQ51 177
M_B_DQ52 164
M_B_DQ53 166
M_B_DQ54 174
M_B_DQ55 176
M_B_DQ56 181
M_B_DQ57 183
M_B_DQ58 191
M_B_DQ59 193
M_B_DQ60 180
M_B_DQ61 182
M_B_DQ62 192
M_B_DQ63 194

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

VREF_DQ/(M3)

[5] DDR_VREF_DQ1
R14 *0_6
SMDDR_VREF_DQ1

H=8

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP4B

+1.5VSUS

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

+3V
VDDSPD 199

NC1 77
NC2 122
NCTEST 125

+3V
R81 *10K_4 PM_EXTTS#1 198
[2,12] DDR3_DRAMRST# EVENT# 30
RESET#

[12] SMDDR_VREF_DIMM
SMDDR_VREF_DQ1
VREF_DQ 1
VREF_CA 126

VSS1 2
VSS2 3
VSS3 8
VSS4 9
VSS5 13
VSS6 14
VSS7 19
VSS8 20
VSS9 25
VSS10 26
VSS11 31
VSS12 32
VSS13 37
VSS14 38
VSS15 43

VSS16 44
VSS17 48
VSS18 49
VSS19 54
VSS20 55
VSS21 60
VSS22 61
VSS23 65
VSS24 66
VSS25 71
VSS26 72
VSS27 127
VSS28 128
VSS29 133
VSS30 134
VSS31 138
VSS32 139
VSS33 144
VSS34 145
VSS35 150
VSS36 151
VSS37 155
VSS38 156
VSS39 161
VSS40 162
VSS41 167
VSS42 168
VSS43 172
VSS44 173
VSS45 178
VSS46 179
VSS47 184
VSS48 185
VSS49 189
VSS50 190
VSS51 195
VSS52 196

VTT1 203
VTT2 204
+SMDDR_VTERM

GND 205
GND 206

Place these Caps near So-Dimm1.

+1.5VSUS
C514 4.7U/6.3V_6X
C71 4.7U/6.3V_6X
C488 4.7U/6.3V_6X
C493 4.7U/6.3V_6X
C75 4.7U/6.3V_6X
C507 4.7U/6.3V_6X
C47 0.1U/10V_4X
C49 0.1U/10V_4X
C45 0.1U/10V_4X
C87 0.1U/10V_4X
C489 0.1U/10V_4X
C515 *0.047U/10V_4X
C501 *0.047U/10V_4X

SMDDR_VREF_DIMM
C525 0.1U/10V_4X
C527 2.2U/6.3V_6X
C521 *0.047U/10V_4X

SMDDR_VREF_DQ1
C35 0.1U/10V_4X
C42 2.2U/6.3V_6X

+3V
C115 2.2U/6.3V_6X
C121 *0.1U/10V_4X
C116 *0.047U/10V_4X

+SMDDR_VTERM
C563 1U/6.3V_4X
C149 1U/6.3V_4X
C580 1U/6.3V_4X
C150 1U/6.3V_4X
C151 *10U/6.3V_8X
C148 4.7U/6.3V_6X
C600 4.7U/6.3V_6X
C561 *0.047U/10V_4X
C582 *0.047U/10V_4X

VREF_DQ/(M1)

+1.5VSUS
R15 1K/F_4
SMDDR_VREF_DQ1
R13 1K/F_4
C38 0.1U/10V_4X
C36 *0.047U/10V_4X

+1.5VSUS
C486 *330U/2.5V_7343P_E9a

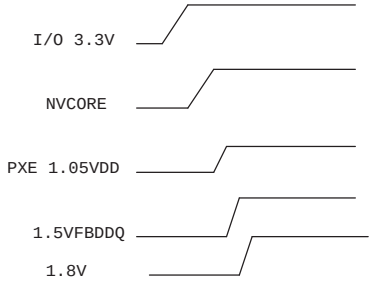
Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	DDR3 DIMM-1	1A

Date: Monday, November 22, 2010 Sheet 13 of 42

15-V

power up sequence



PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

~ 500mA

1600mA

12~16 mils width
110mA

12~16 mils width

GPU3500A
fcbga973-nvidia-n11p-es-a1
COMMON

PCI EXPRESS

Q3503
EV@2N7002_200MA

Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	N12x-Fermi PCIE	1A
Date: Monday, November 22, 2010	Sheet 14 of 42	

GPU3500B
fcbga973-nvidia-n11p-es-a1
COMMON

GPU3500C
fcbga973-nvidia-n11p-es-a1
COMMON

MEMORY I/F A

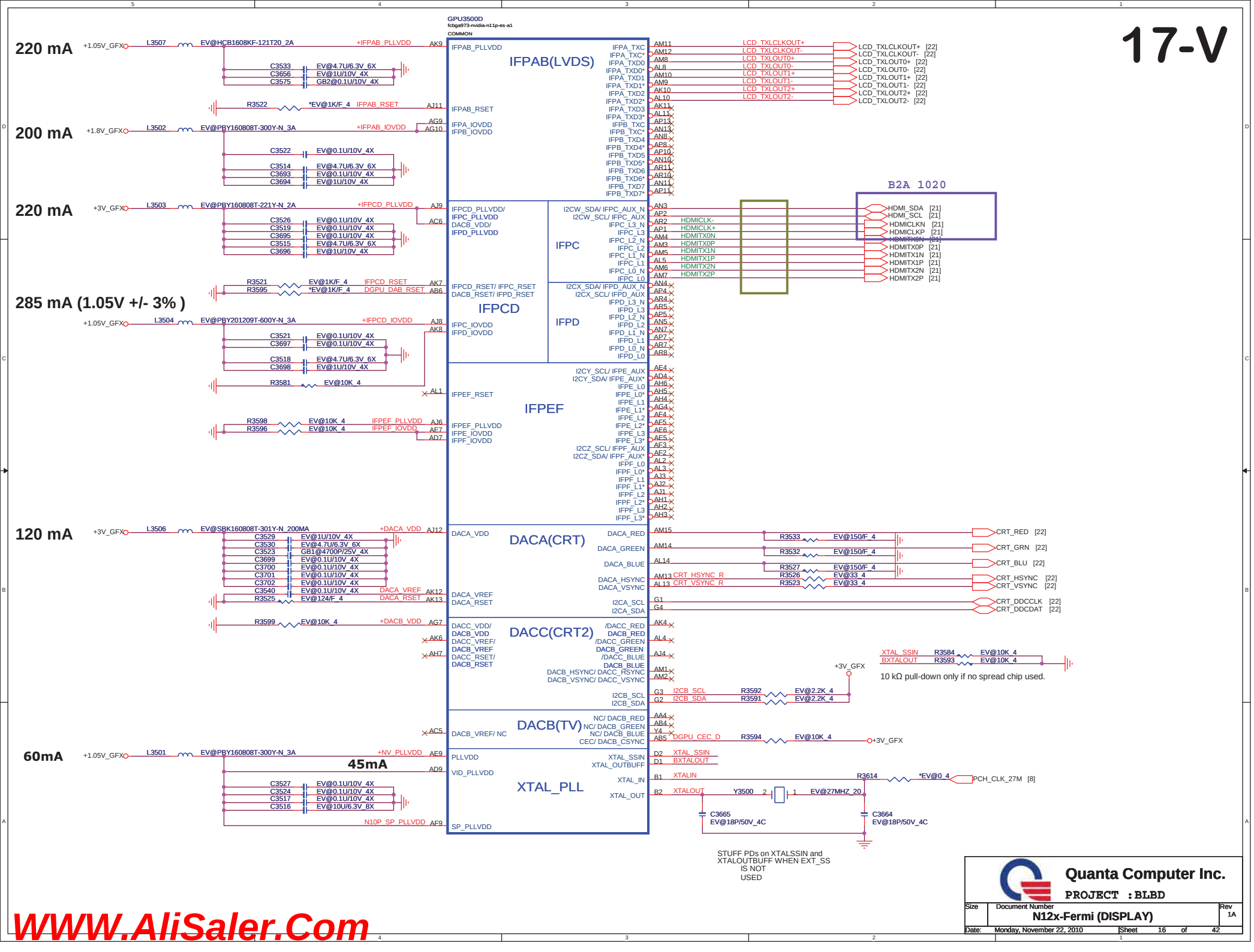
MEMORY I/F C

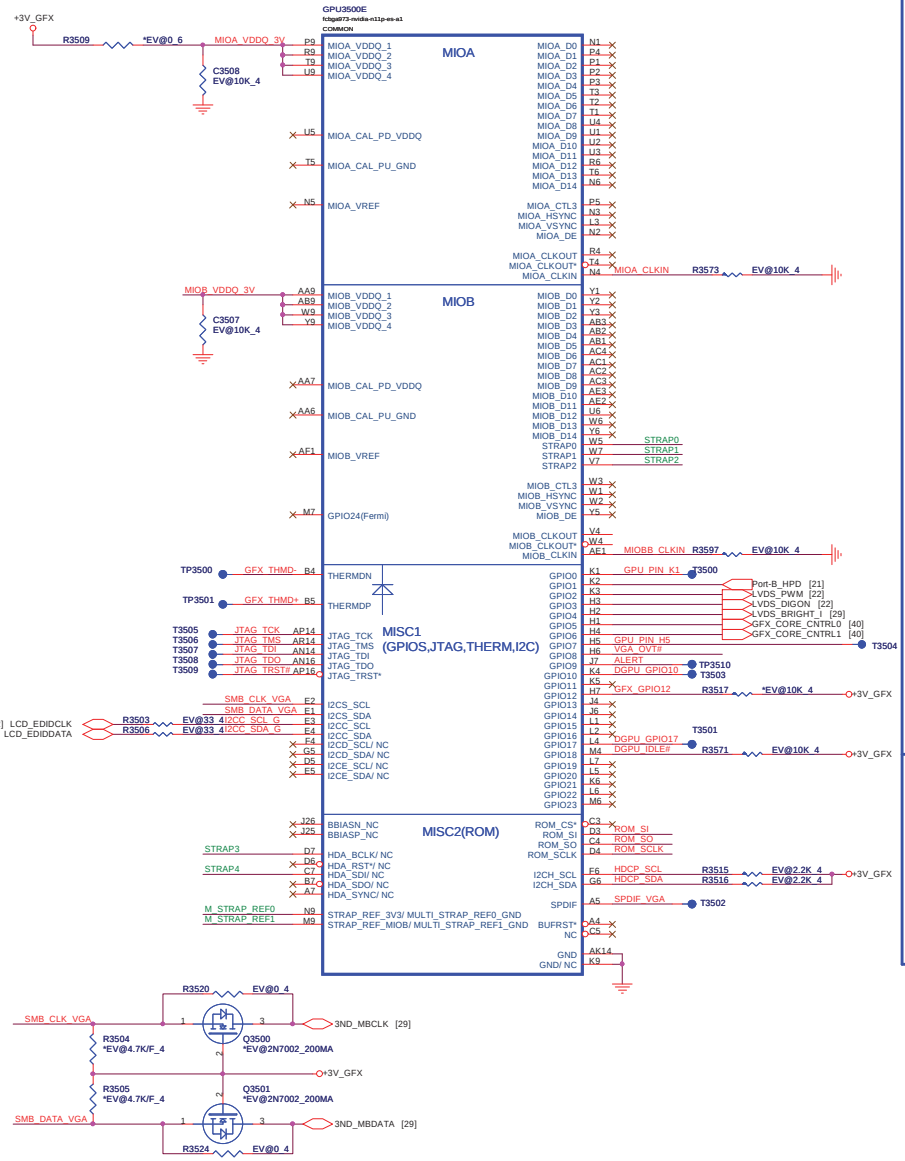
15mils width

15mils width

Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	N12x-Fermi (MEM I/F)	1A
Date: Monday, November 22, 2010	Sheet 15 of 42	


17-V
GPU3500D
fcbga973-nvidia-n11p-es-a1
COMMON
220 mA
200 mA
220 mA
285 mA (1.05V +/- 3%)
120 mA
60mA
45mA
IFPAB(LVDS)
IFPCD
IFPEF
DACA(CRT)
DACC(CRT2)
DACB(TV)
XTAL_PLL
IFPC
IFPD
B2A 1020
10 kΩ pull-down only if no spread chip used.
STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED
Quanta Computer Inc.
PROJECT : BLBD
N12x-Fermi (DISPLAY)
Monday, November 22, 2010
Sheet 16 of 42
WWW.AliSaler.Com

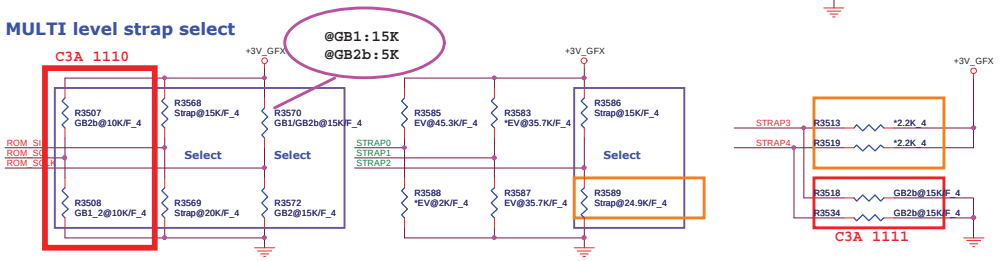


Strappin Model select

MODE	M_STRAP_REF0	M_STRAP_REF1	M_STRAP_REF2
Multi-level	40.2K/F_4 PD	40.2K/F_4 PD	40.2K/F_4 PD

18-V

MULTI level strap select



		Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12M-GE @GB1	N12P-GV @GB2b	N12P-LP @GB2
ROM_SCLK		PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010(15KPU)	1000(5KPU)	0010(15KPD)
ROM_SI		RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	RAMCFG T	RAMCFG T	RAMCFG T
ROM_SO	GB1/2	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE			
	GB2b	FB1	FB0			0001(10KPD)	1001(10KPU)	0001(10KPD)
STRAP0		USER[3]	USER[2]	USER[1]	USER[0]	1111(45KPU)	1111(45KPU)	1111(45KPU)
STRAP1		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110(35KPD)	0110(35KPD)	0110(35KPD)
STRAP2		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1010(15KPU)	0000(5KPD)	1100(25KPU)
STRAP3(Only GB2B)		SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		0010(15KPD)	
STRAP4(Only GB2B)		Reserve	Reserve	PCIE_MAX_SPEED	DP_PLL_VDD33V		0010(15KPD)	

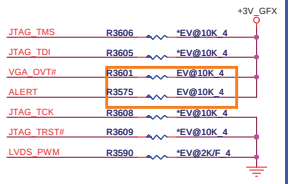
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI	
0x0 0000					
0x1 0001				AKD5LZWTW02	
0x2 0010	DDR3 64Mx16x8, 128bit, 1GB	Hynix	H5TQ1G63DFR-12C(800MHz) / H5TQ1G63DFR-11C(900MHz)		PD 15K
0x3 0011	DDR3 64Mx16x8, 128bit, 1GB	Samsung	K4W1G1646E-HC12(800MHz) / K4W1G1646E-HC11(900MHz)		PD 20K
0x4 0101				AKD5LGHT500	
0x5 0110					
0x6 0110	DDR3 128Mx16x8, 128bit, 2GB	Hynix	H5TQ2G63BFR-12C(800MHz) / H5TQ2G63BFR-11C(900MHz)		PD 35K
0x7 0111	DDR3 128Mx16x8, 128bit, 2GB	Samsung	K4W2G1646C-HC1(800MHz)2 / K4W2G1646C-HC11(900MHz)		PD 45K

N12M-GE(QS)
Device Id=0x0A7A
STRAP2 =15K PU
ROM_SCLK=15K PU

N12P-GV(QS)
Device Id=-x1050
STRAP2 =5K PD
ROM_SCLK=5K PU

N12P-LP(QS)
Device Id=0x0DEC
STRAP2=25K PU
ROM_SCLK=15K PD



GPIO ASSIGNMENTS

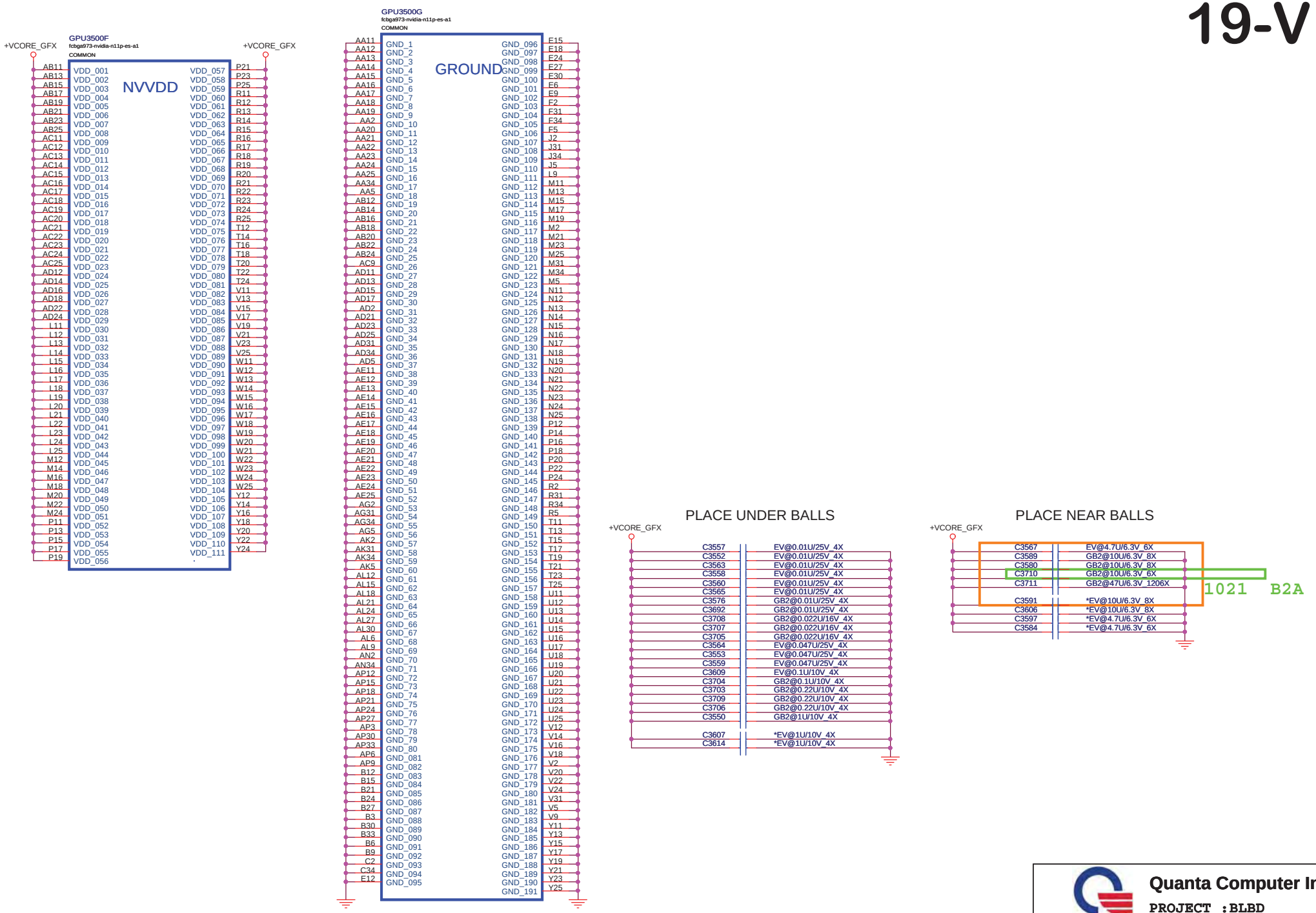
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Quanta Computer Inc.
PROJECT : BLBD
Size | Document Number: N12x-Fermi (GND&Str&Ther) | Rev 1A
Date: Monday, November 22, 2010 | Sheet 17 of 42

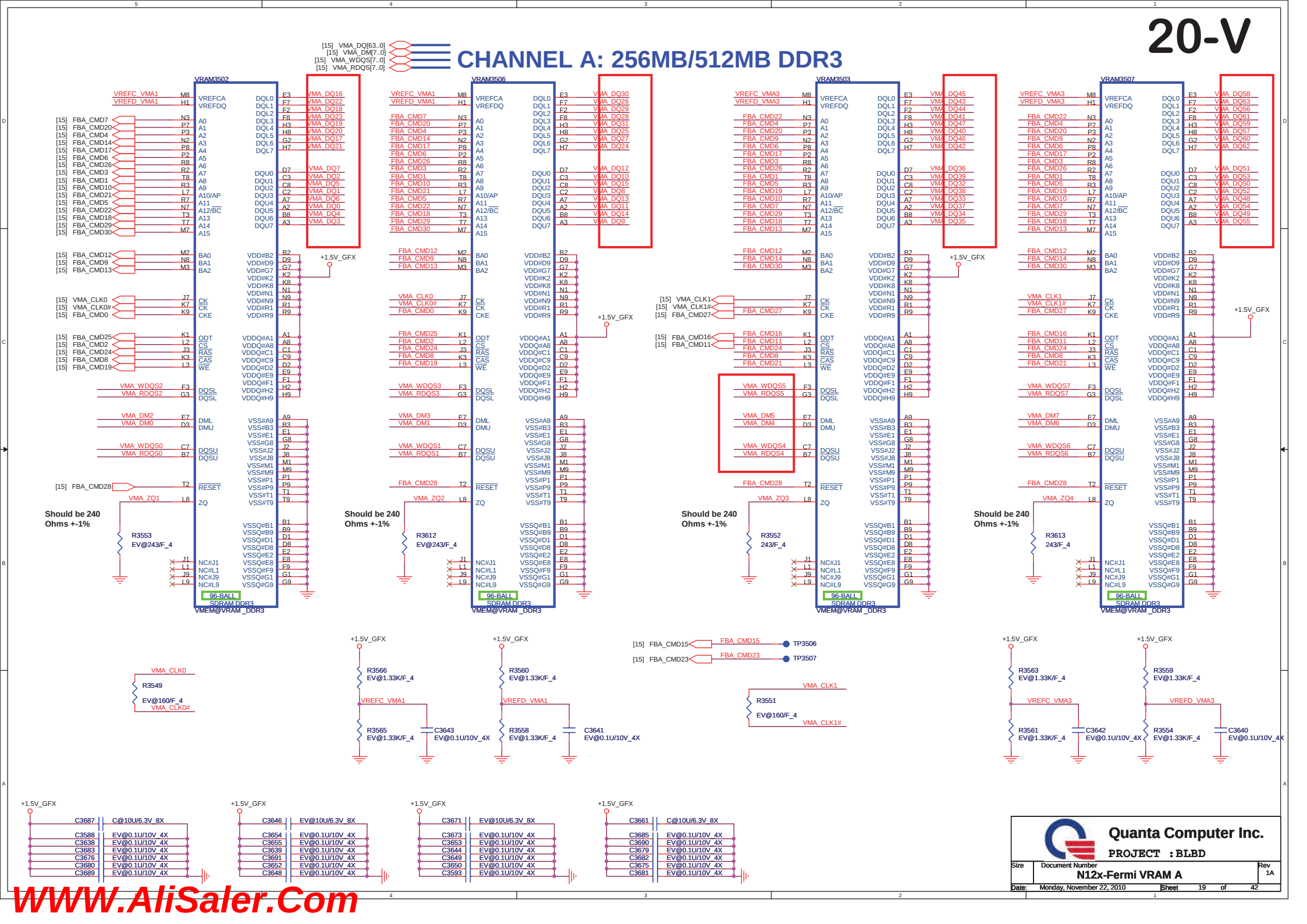
19-V



Quanta Computer Inc.		
PROJECT : BLBD		
Size	Document Number: N12x-Fermi (GND/Power)	Rev: 1A
Date: Monday, November 22, 2010	Sheet 18 of 42	

20-V

CHANNEL A: 256MB/512MB DDR3



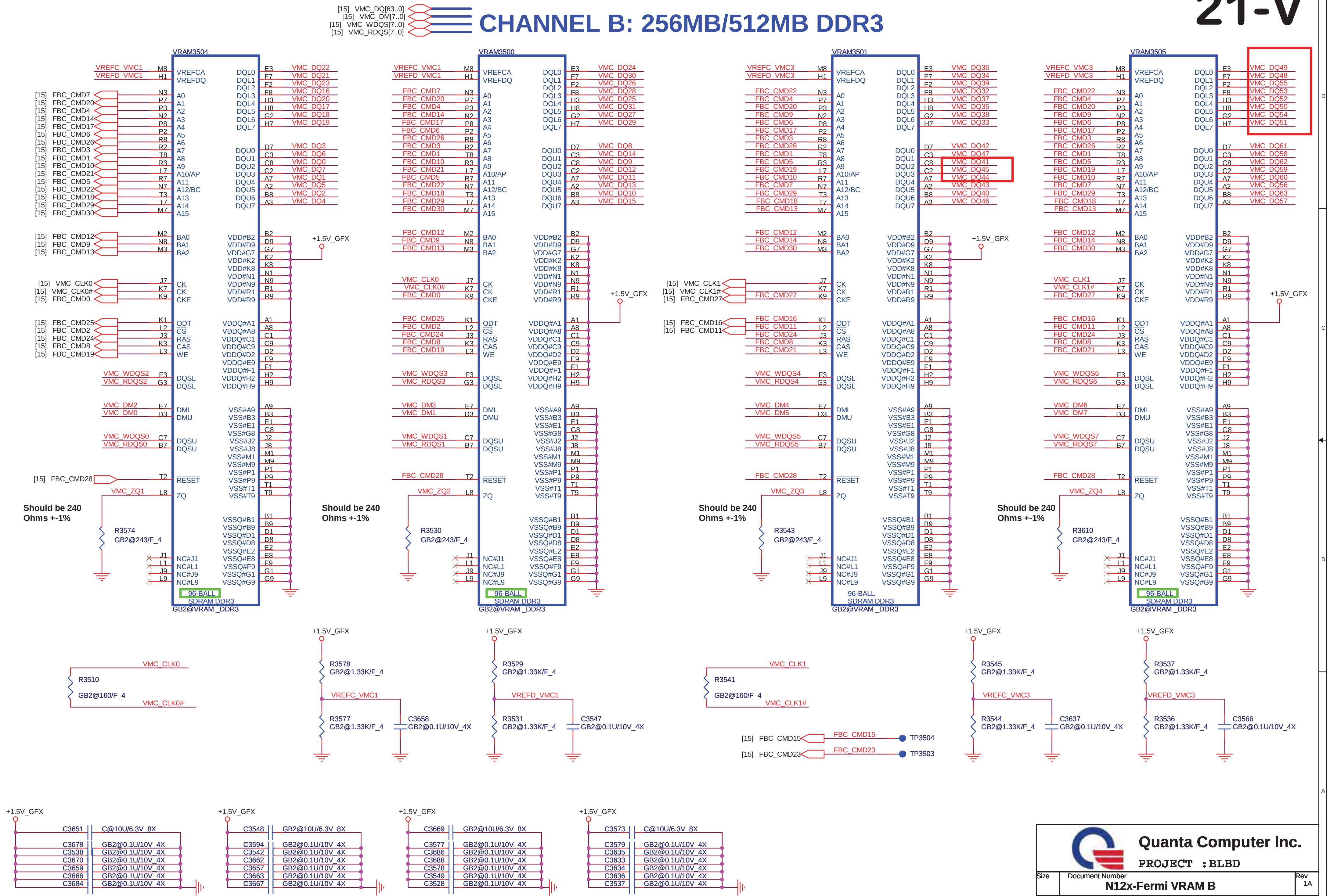
Quanta Computer Inc.

PROJECT : BLBD

Size	Document Number	Rev
	N12x-Fermi VRAM A	1A
Date: Monday, November 22, 2010	Sheet 19 of 42	

21-V

CHANNEL B: 256MB/512MB DDR3



Quanta Computer Inc.

PROJECT :BLBD

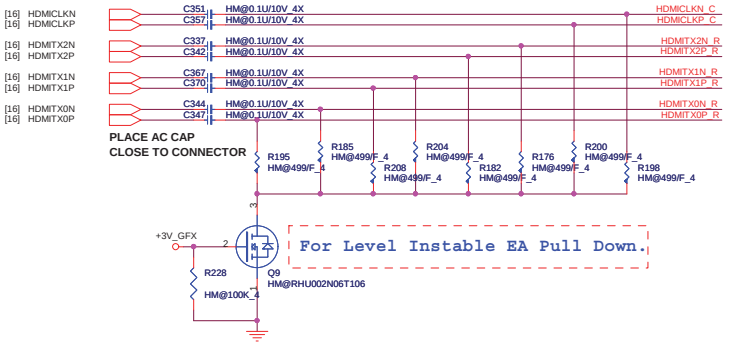
Size	Document Number	Rev
	N12x-Fermi VRAM B	1A

Date: Monday, November 22, 2010 | Sheet 20 of 42

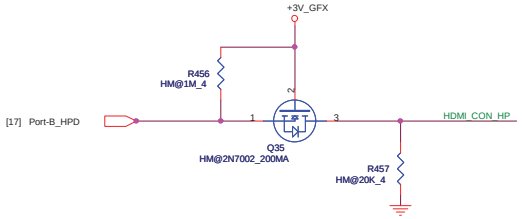
VGA HDMI
HDMI-passive level shift <HMP/HMG>

HDMI Interface

Angelo 0921

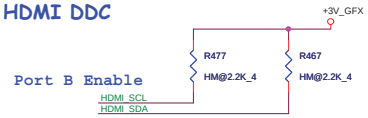


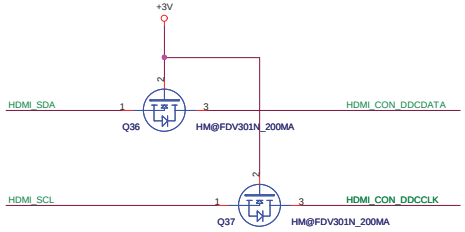
HDMI HPD



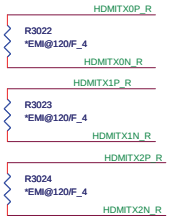
HDMI DDC

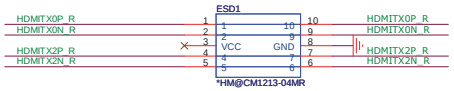
Port B Enable

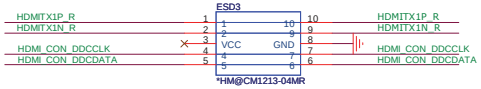


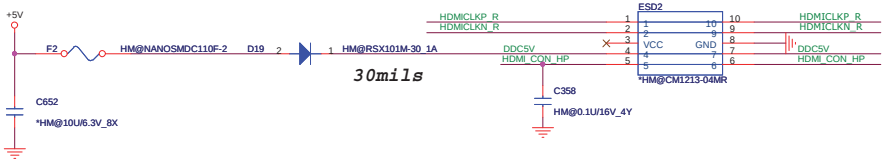


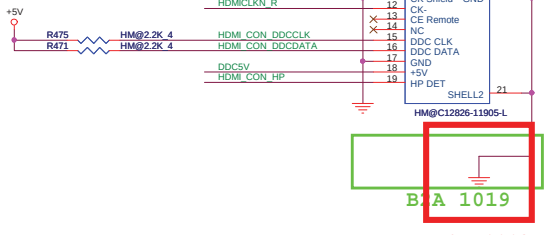
Close to HDMI CONN





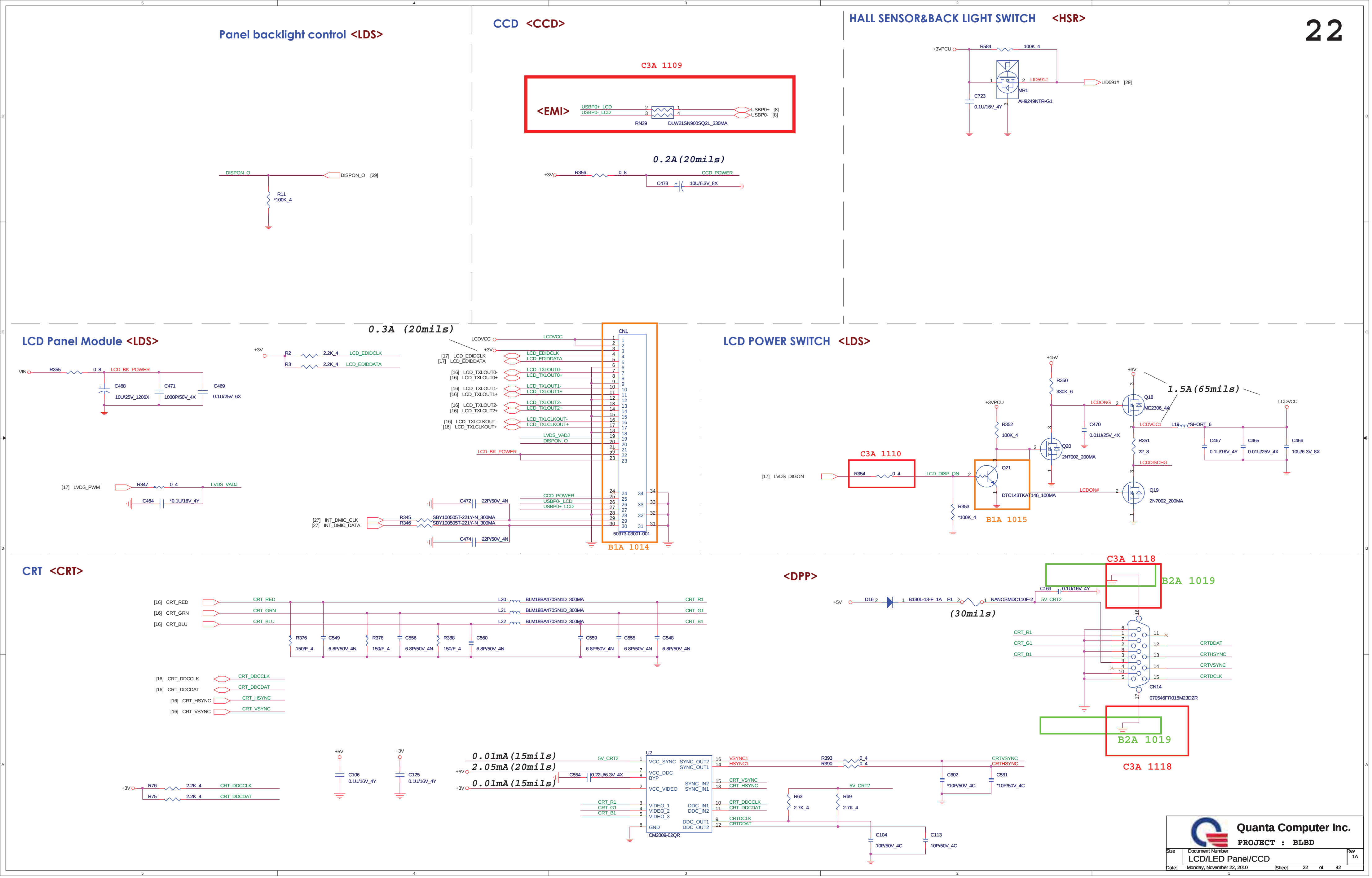






Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	HDMI CONN	1A
Date: Monday, November 22, 2010	Sheet 21 of 42	



WWW.AliSaler.Com

MINI Card Slot#1 (WiFi) <MNW>

+3V → L10 PBY201209T-330Y-N_4A → WIMAX_P

C625 0.1U/16V_4Y, C212 C@0.1U/16V_4Y, C215 C@0.1U/16V_4Y, C196 C@10U/6.3V_8X

0.5A(30mils) +1.5V

2.75A(120mils) WIMAX_P

B2A 1019

[7,29] SERIRQ
[7] LDRQ#1
[8] PCLK_DEBUG
PLTRST#R93 MNW@0_4
R99 *MNW@0_4 SERIRQ_debug
R102 MNW@0_4 LDRQ#1_debug
R107 MNW@0_4 PLTRST#_debug
PCLK_DEBUG_R

CN16 80003-5121

[8] PCIE_TXP5
[8] PCIE_TXN5
[8] PCIE_RXP5
[8] PCIE_RXN5
[8] CLK_PCIE_MINI
[8] CLK_PCIE_MINI#
[8] PCIE_CLK_MINI_REQ#

B1A 1014 Del R184

WIMAX_P R126 *10K_4 BT_RFCTRL_BT R175 *0_4 R181 0_4 SERIRQ_debug

Q8 DTC144EUBTL_30MA

[29] BT_RFCTRL

H=4mm

USBP5+ [8]
USBP5- [8]

WL_SMDATA
WL_SMCLK

0.33A(30mils)

PLTRST#
RF_EN
RF_EN [29]

LFRAME#_PCIE R147 MNW@0_4 LFRAME# [7,29]
LAD3_PCIE R158 MNW@0_4 LAD3 [7,29]
LAD2_PCIE R164 MNW@0_4 LAD2 [7,29]
LAD1_PCIE R167 MNW@0_4 LAD1 [7,29]
LAD0_PCIE R170 MNW@0_4 LAD0 [7,29]

+1.5V C338 *0.01U/25V_4X C241 *0.1U/16V_4Y C199 *10U/6.3V_8X

WL_SMDATA R112 *SHORT_4 CGDAT_SMB [12,13]
WL_SMCLK R121 *SHORT_4 CGCLK_SMB [12,13]

WIMAX_P RP1 4.7KX2
[8,26] SDATA Q4 2N7002_200MA WL_SMDATA

WIMAX_P
[8,26] SCLK Q6 2N7002_200MA WL_SMCLK

MINI Card Slot#2 3G <MNT>

B1A 1015

0.5A(30mils) +1.5V

C308 *3G@0.01U/25V_4X, C348 3G@0.1U/16V_4Y, C229 *3G@0.1U/16V_4Y, C674 *3G@10U/6.3V_8X
C333 *3G@0.01U/25V_4X, C334 *3G@0.1U/16V_4Y, C352 *3G@10U/6.3V_8X

B1A 1015 Add

+3V +3V_3G 2.75A(120mils) R487 3G@0_8

+3V_3G R920 *3G@10K/F_4 PCIE_CLK_3G_REQ#_C Q94 *3G@2N7002_200MA R921 3G@0_4 PCIE_CLK_3G_REQ# [8]

+1.5V +3V_3G

B1A 1015

2.75A(120mils)

CN18 3G@80003-7021

[8] PCIE_TXP3
[8] PCIE_TXN3
[8] PCIE_RXP3
[8] PCIE_RXN3
[8] CLK_PCIE_3G
[8] CLK_PCIE_3G#
PCIE_CLK_3G_REQ#_C

B1A 1015

H=9mm

CPUSB# [9]
USBP10+ [8]
USBP10- [8]
WL_SMDATA
WL_SMCLK
PLTRST# 3G_EN
PLTRST# [2,8,24,26,29]
3G_EN [29]
UIM_VPP_R
UIM_RST_R
UIM_CLK_R
UIM_DATA_R
UIM_PWR_R
C259 *3G@100P/50V_4N

SIM CARD board to board <MNT>

CN10 3G@88020-12101

UIM_CLK
UIM_DATA
USBP4+
USBP4-
[8] USBP4+
[8] USBP4-
UIM_VPP
UIM_PWR
UIM_RST

3G CONN <MNT>

CN5 *3G@88511-120N

UIM_CLK_R
UIM_DATA_R
UIM_RST_R
UIM_VPP_R
UIM_PWR_R
C678 *3G@0.1U/16V_4Y

Close to 3G MINI Card

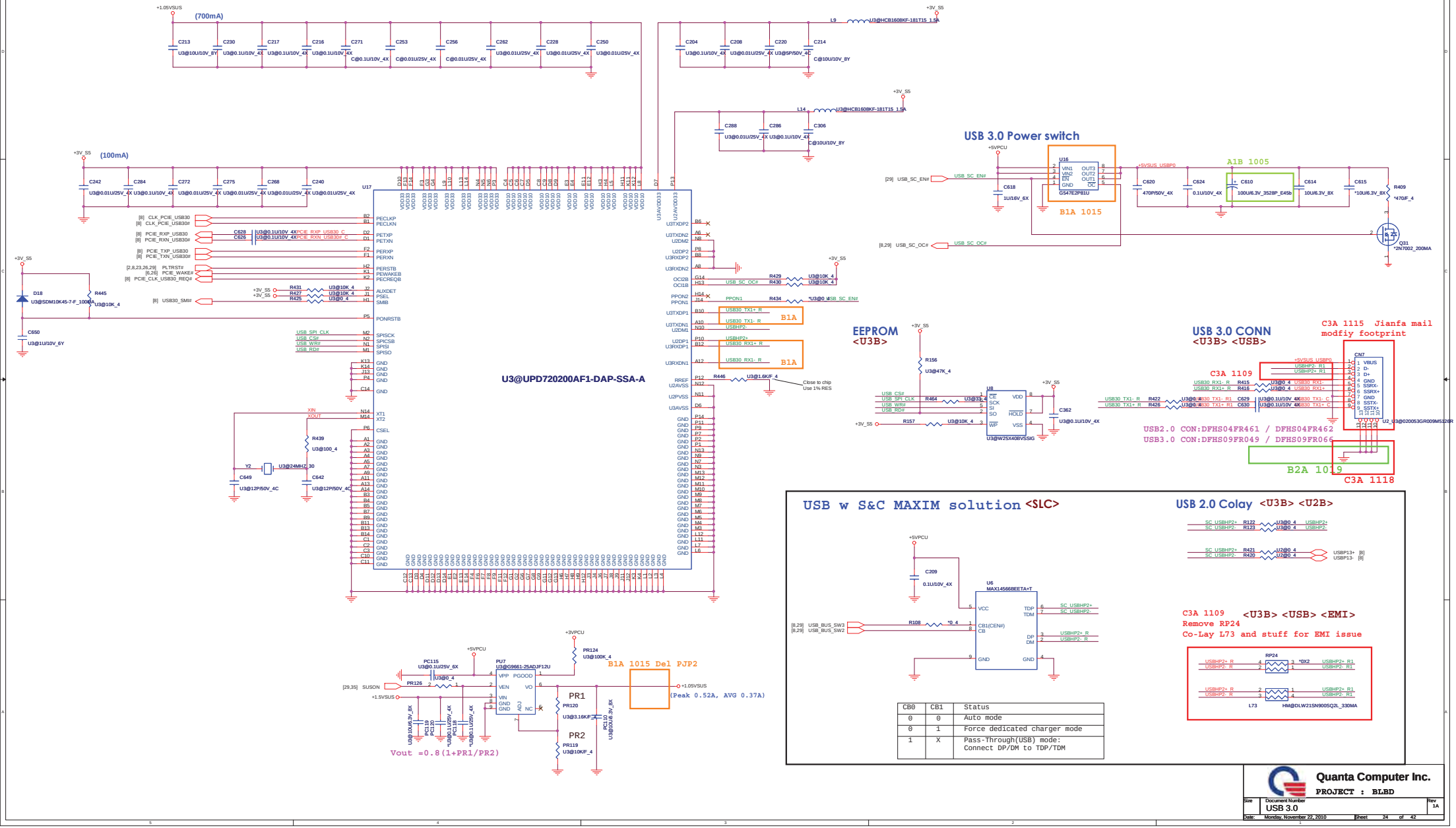
UIM_VPP_R	R493	*3G@0_4	UIM_VPP_RR	R505	*3G@0_4	UIM_VPP
UIM_RST_R	R494	*3G@0_4	UIM_RST_RR	R506	*3G@0_4	UIM_RST
UIM_CLK_R	R495	*3G@0_4	UIM_CLK_RR	R507	*3G@0_4	UIM_CLK
UIM_DATA_R	R496	*3G@0_4	UIM_DATA_RR	R508	*3G@0_4	UIM_DATA
UIM_PWR_R	R499	*3G@0_4	UIM_PWR_RR	R509	*3G@0_4	UIM_PWR

CN8 *3G@88511-120N

UIM_PWR
UIM_VPP
UIM_RST
UIM_DATA
UIM_CLK

Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	MINI CARD(WLAN/3G/SIM Card)	1A
Date: Monday, November 22, 2010	Sheet 23 of 42	



CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

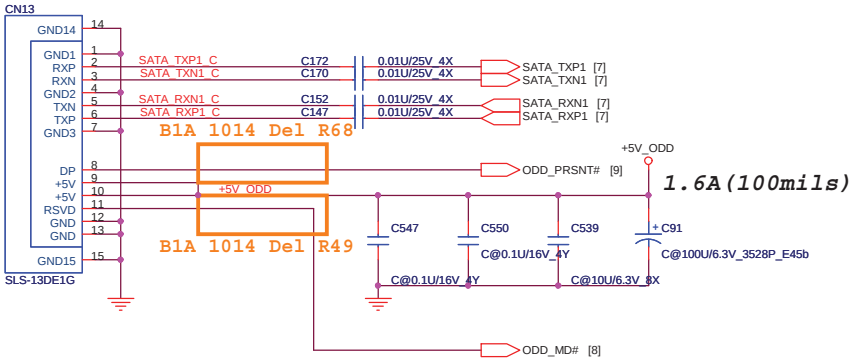
Quanta Computer Inc.

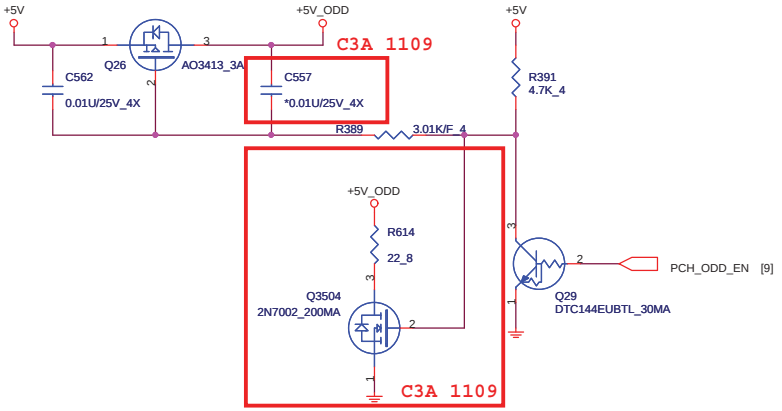
PROJECT : BLBD

Size	Document Number	Rev
	USB 3.0	1A
Date: Monday, November 22, 2010	Sheet 24 of 42	

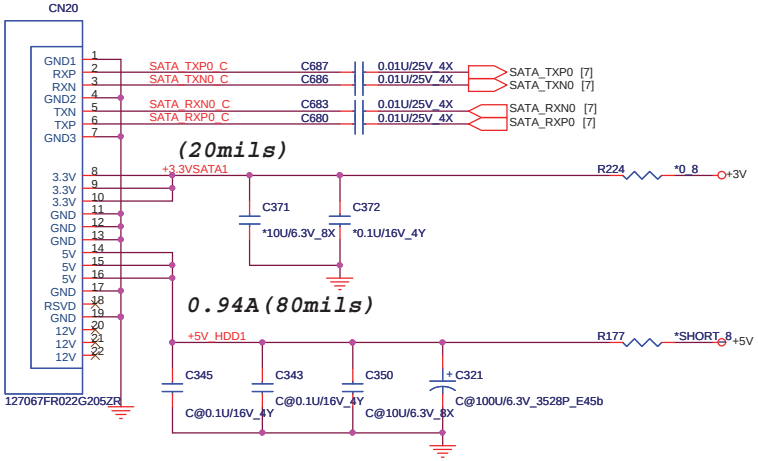
SATA ODD

ODD Zero power . (Only for Intel)<OZP>

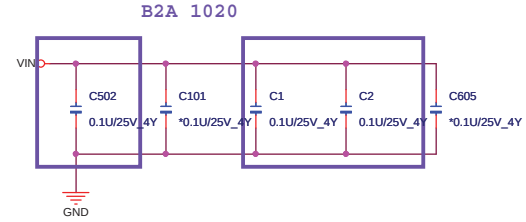


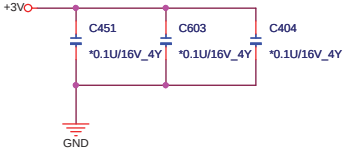


SATA HDD



EMI





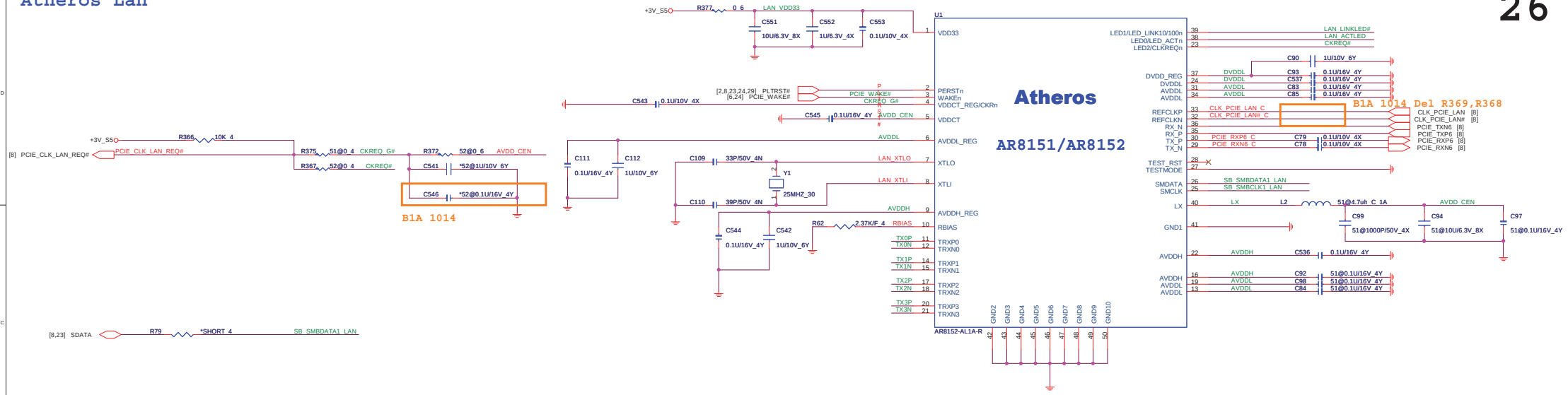
Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	HDD/ODD/EMI	1A

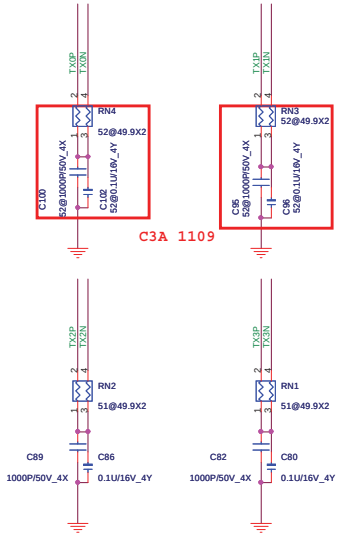
Date: Monday, November 22, 2010 Sheet 25 of 42

Atheros Lan

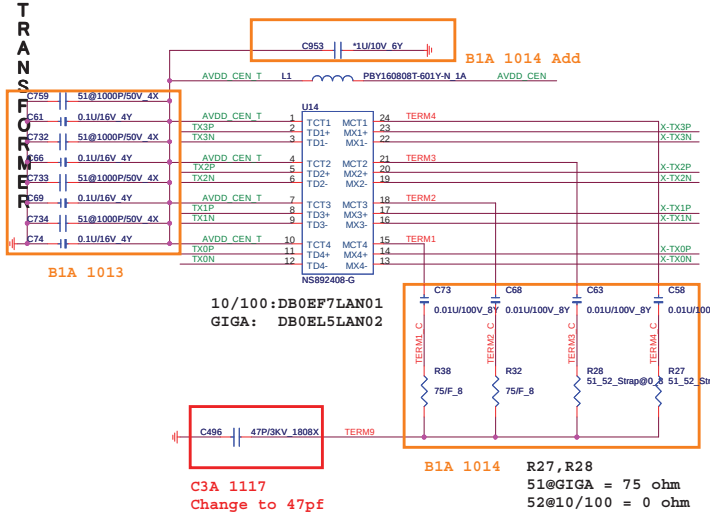
0.163A(20mils)



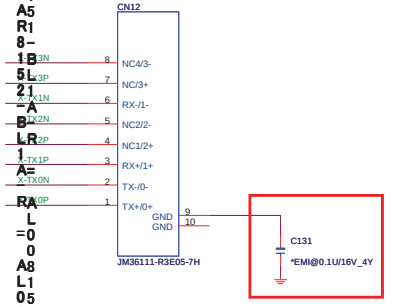
PLACE NEAR LAN IC SIDE



TRANSFORMER

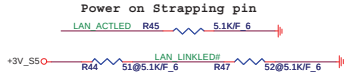


RJ45

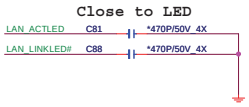


LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

Power on Strapping pin



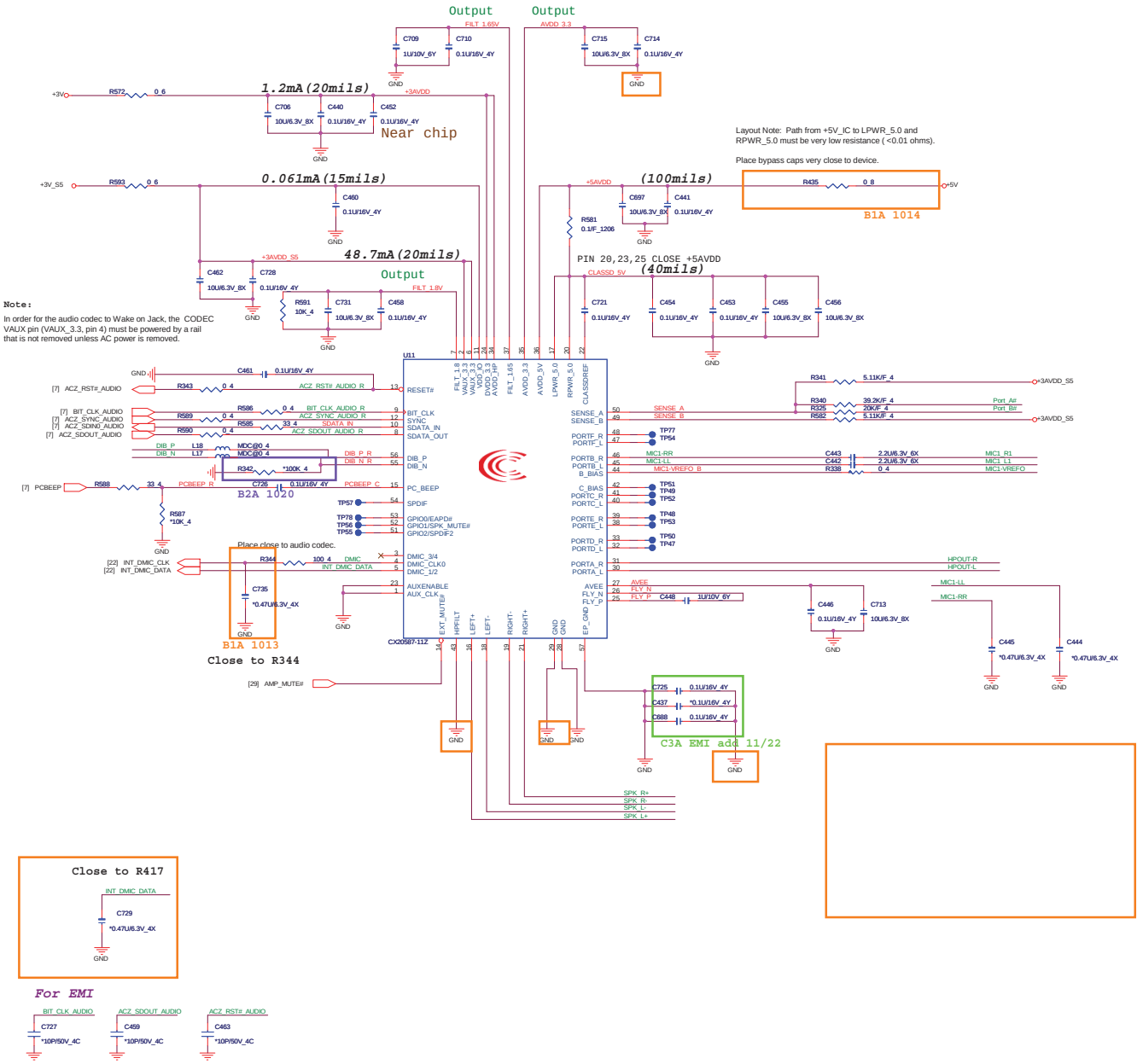
Close to LED



Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	Atheros Lan	1A
Date: Monday, November 22, 2010	Sheet 26 of 42	

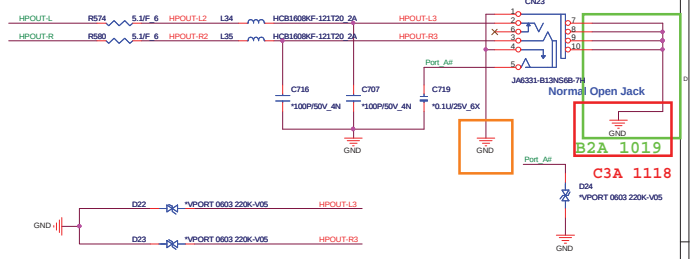
Codec (CX20587) <ADO/MDC/SLM>



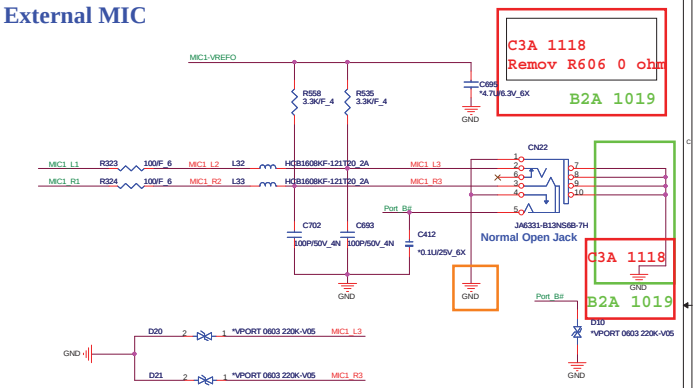
AUDIO JACKS

27

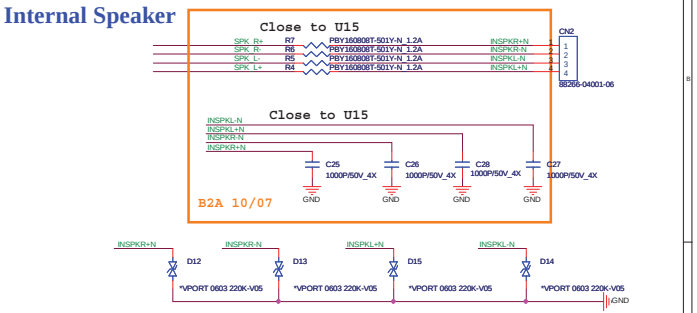
Earphone



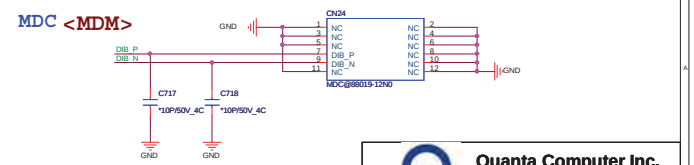
External MIC



Internal Speaker



MDC <MDM>



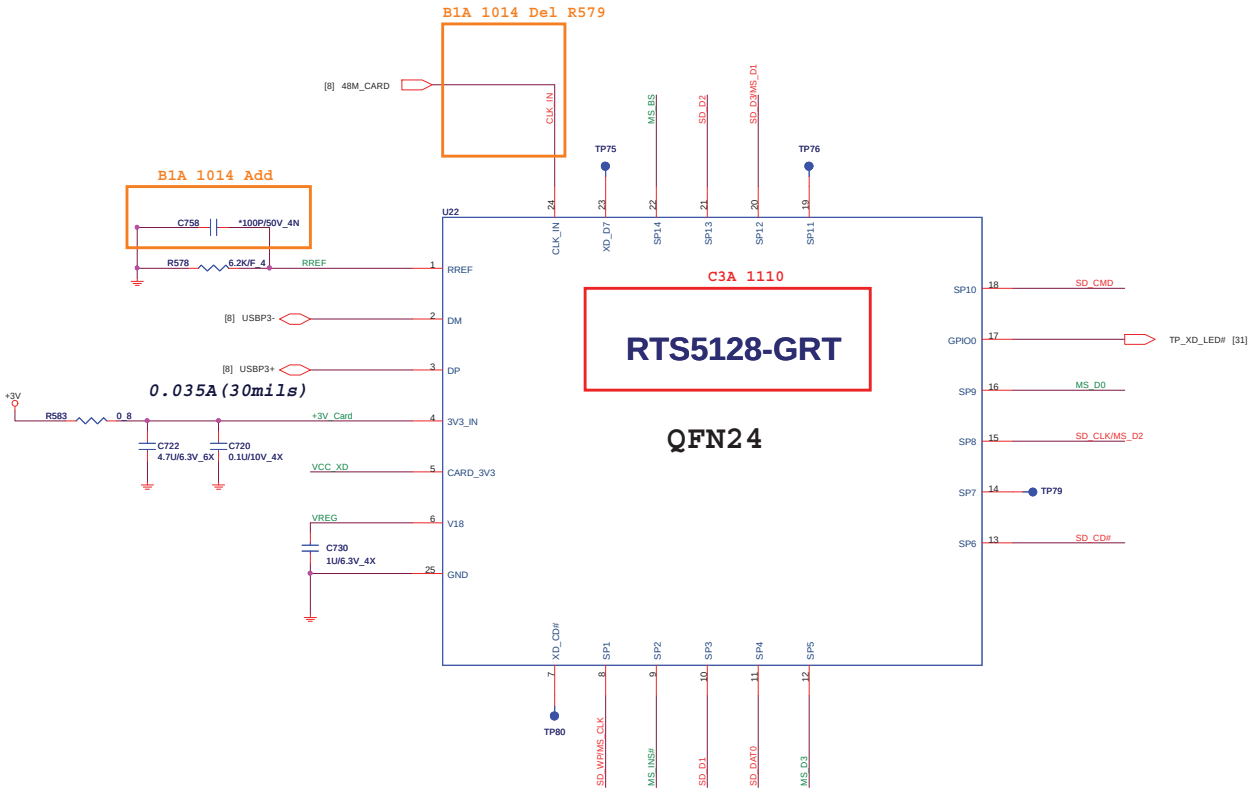
Quanta Computer Inc.

PROJECT : BLBD

Size	Document Number	Rev
	Audio Codec (CX20587)	1A

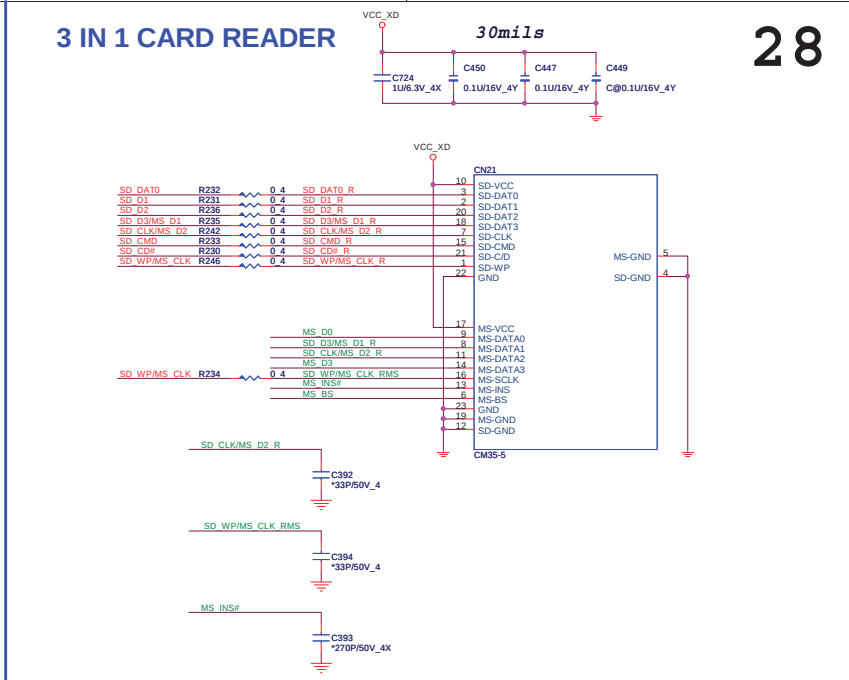
Date: Monday, November 22, 2010 Sheet 27 of 42

3 IN 1 CARD READER



AL005128001 IC CTRL(24P) RTS5128-GRT(QFN)

3 IN 1 CARD READER



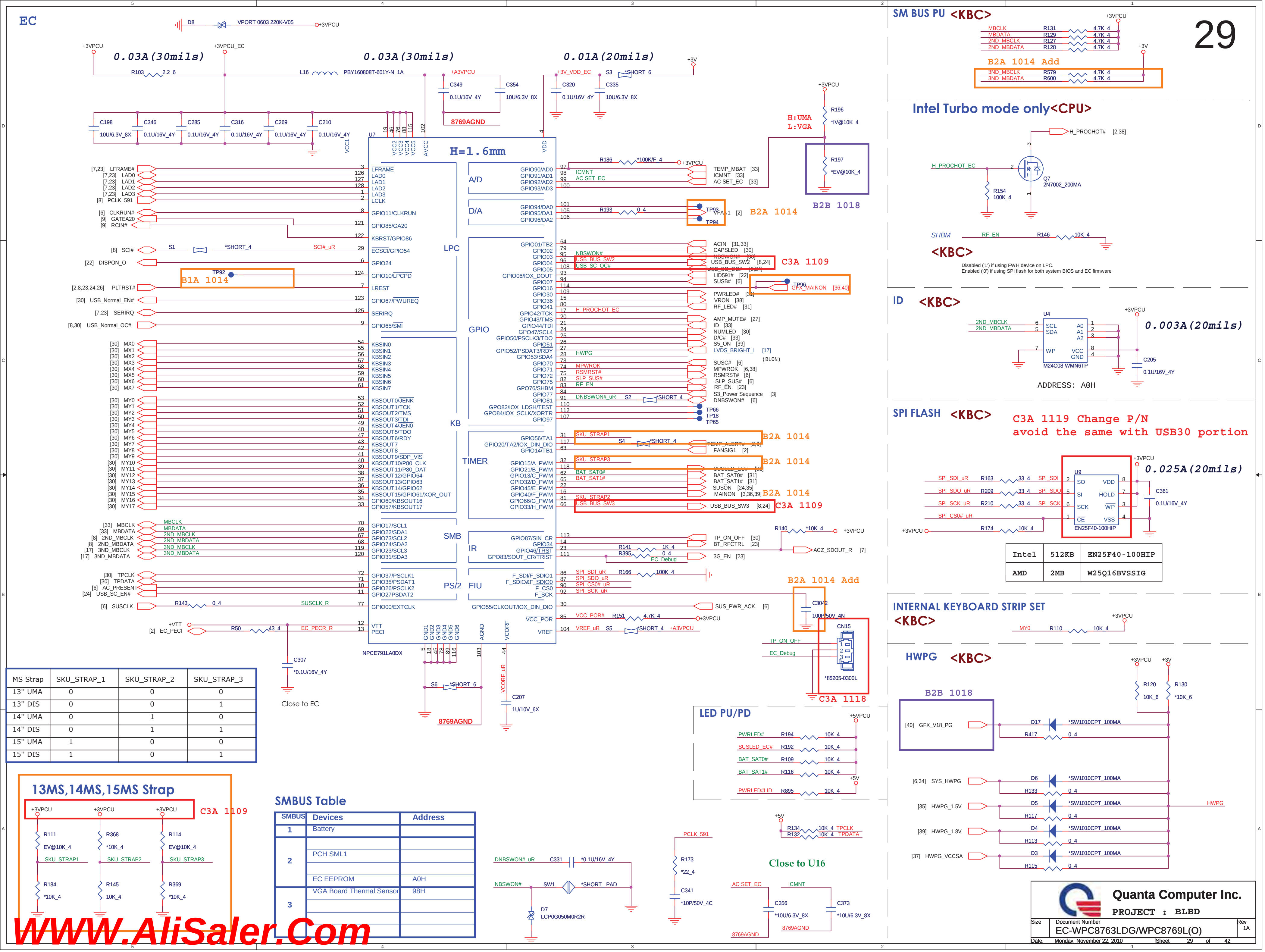
Quanta Computer Inc.

PROJECT : BLBD

Size	Document Number	Rev
	RTS5159 (Card Reader)	1A

Date: Monday, November 22, 2010 Sheet 28 of 42

EC



MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3
13" UMA	0	0	0
13" DIS	0	0	1
14" UMA	0	1	0
14" DIS	0	1	1
15" UMA	1	0	0
15" DIS	1	0	1

SMBUS Table

SMBUS	Devices	Address
1	Battery	
2	PCH SML1	
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

Intel	512KB	EN25F40-100HIP
AMD	2MB	W25Q16BVSSIG

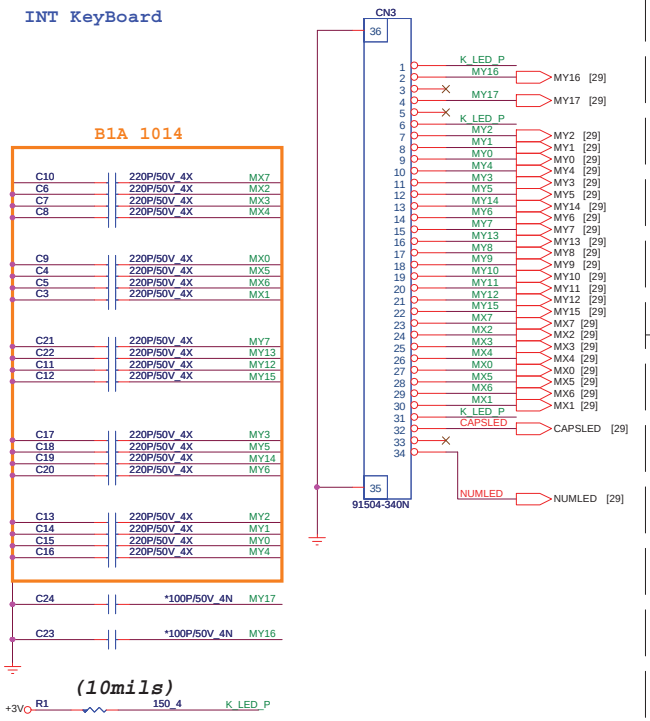
Quanta Computer Inc.

PROJECT : BLBD

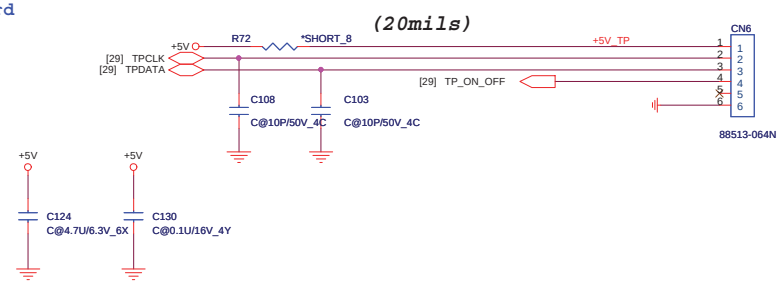
Size	Document Number	Rev
	EC-WPC8763LDG/WPC8769L(O)	1A

Date: Monday, November 22, 2010 Sheet 29 of 42

INT KeyBoard

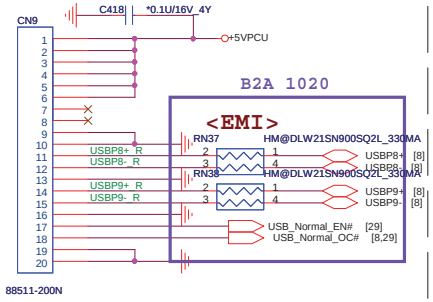


TP board

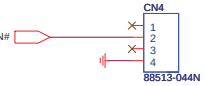


Bluetooth

USB board



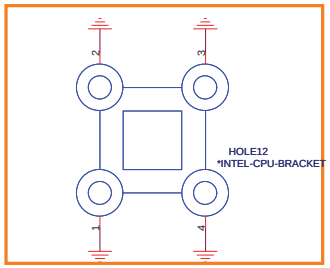
Power board



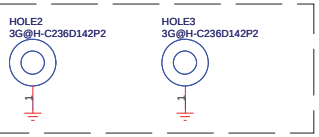
NUT

B1A 1014

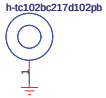
CPU



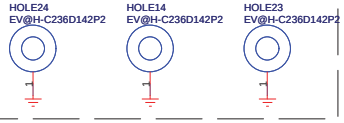
SIM



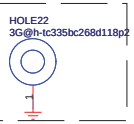
WLAN/Mini Card



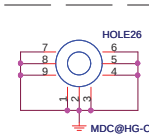
VGA



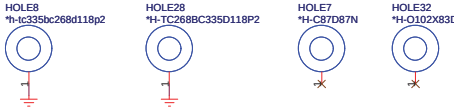
3G Mini Card

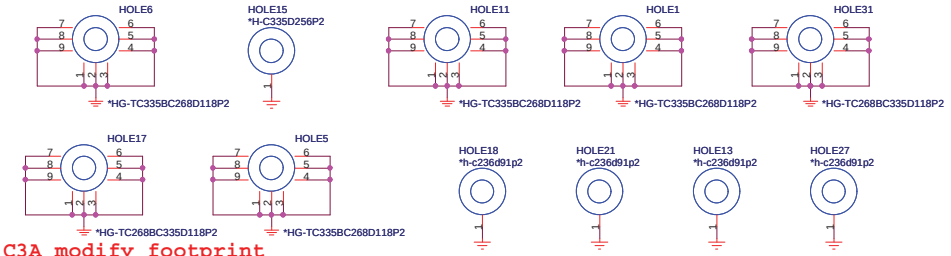


MDC



HOLE



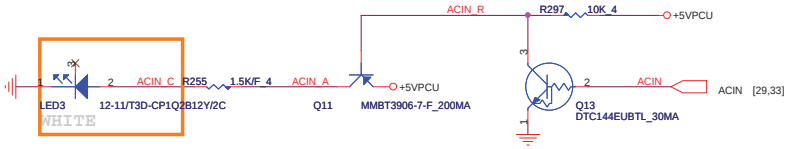


Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	KB/TP/PB/USB/HOLE	1A
Date: Monday, November 22, 2010	Sheet 30 of 42	

LED

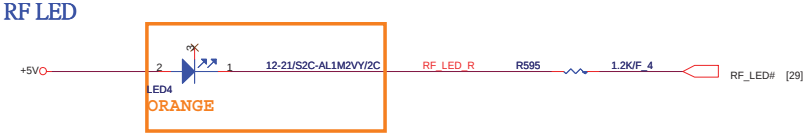
AC-IN



B1A 1015

POWER

RF LED

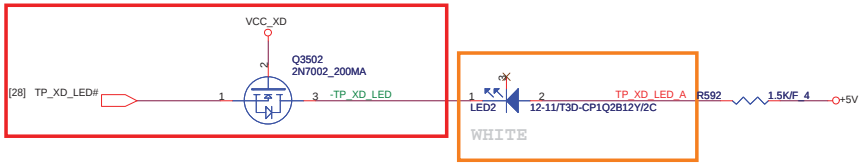


B1A 1015

BATERRY

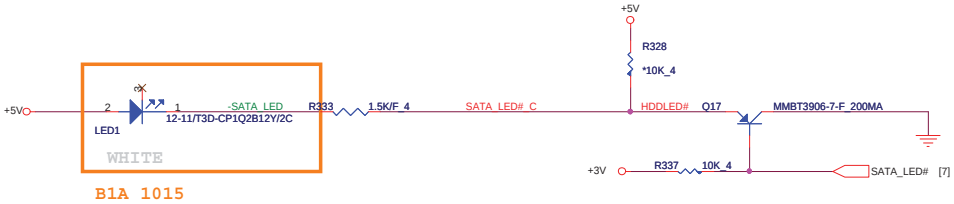
CARDREADER

C3A 1109
DEL Q16, Add Q3502



B1A 1015

HDD/ODD



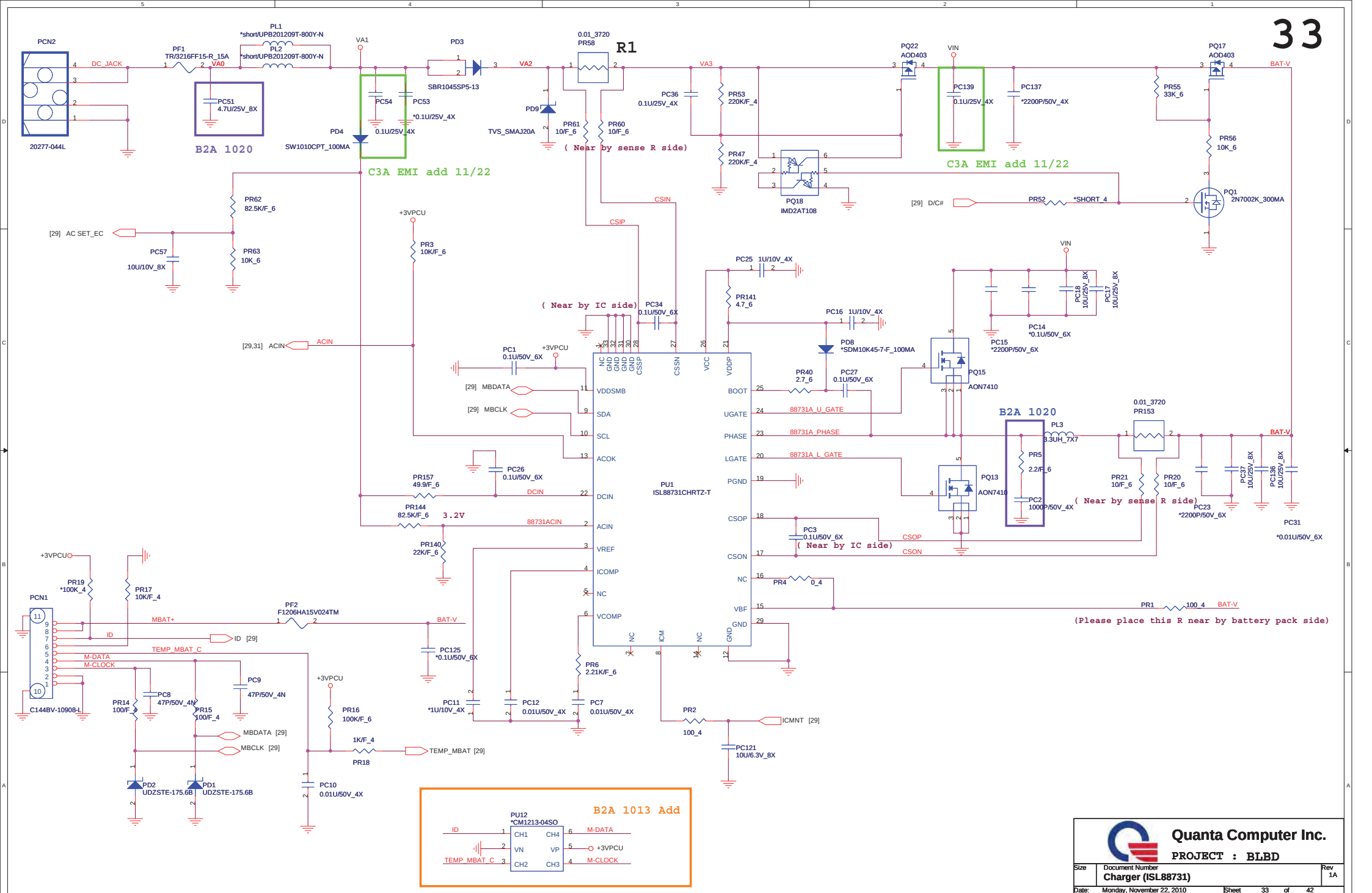
B1A 1015

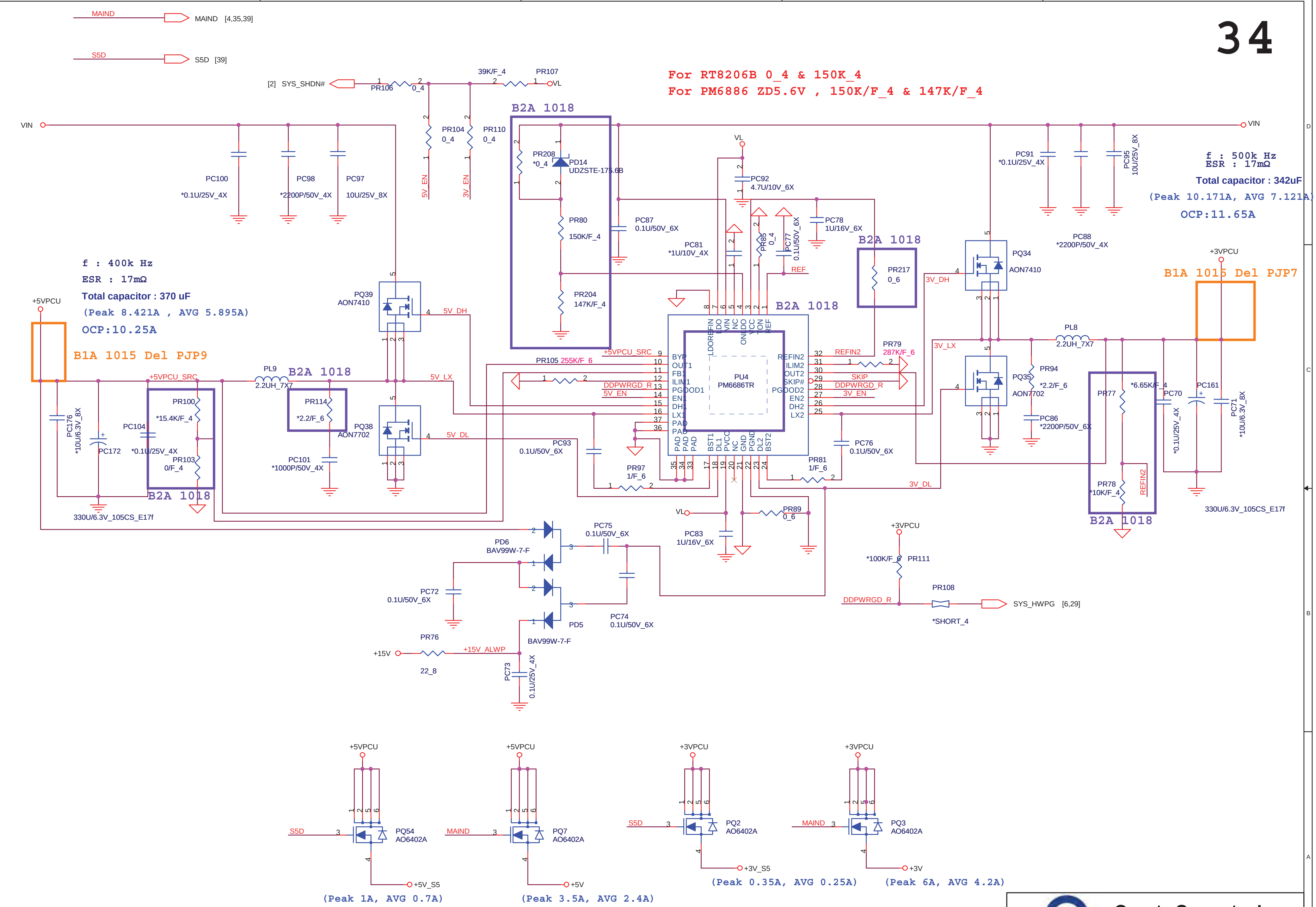
ESD Protect

Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	LED	1A
Date: Monday, November 22, 2010	Sheet 31 of 42	

BLANK



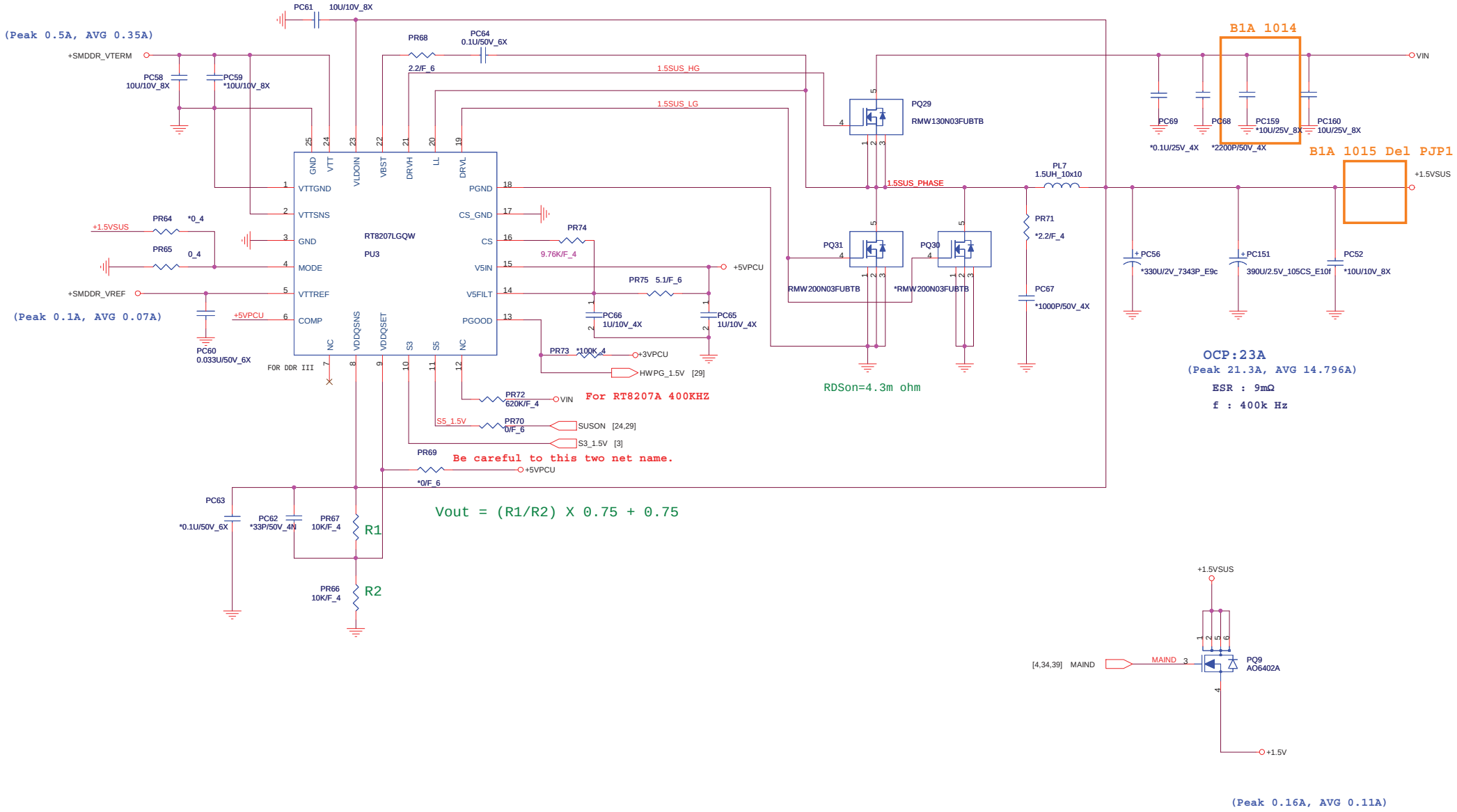


Quanta Computer Inc.

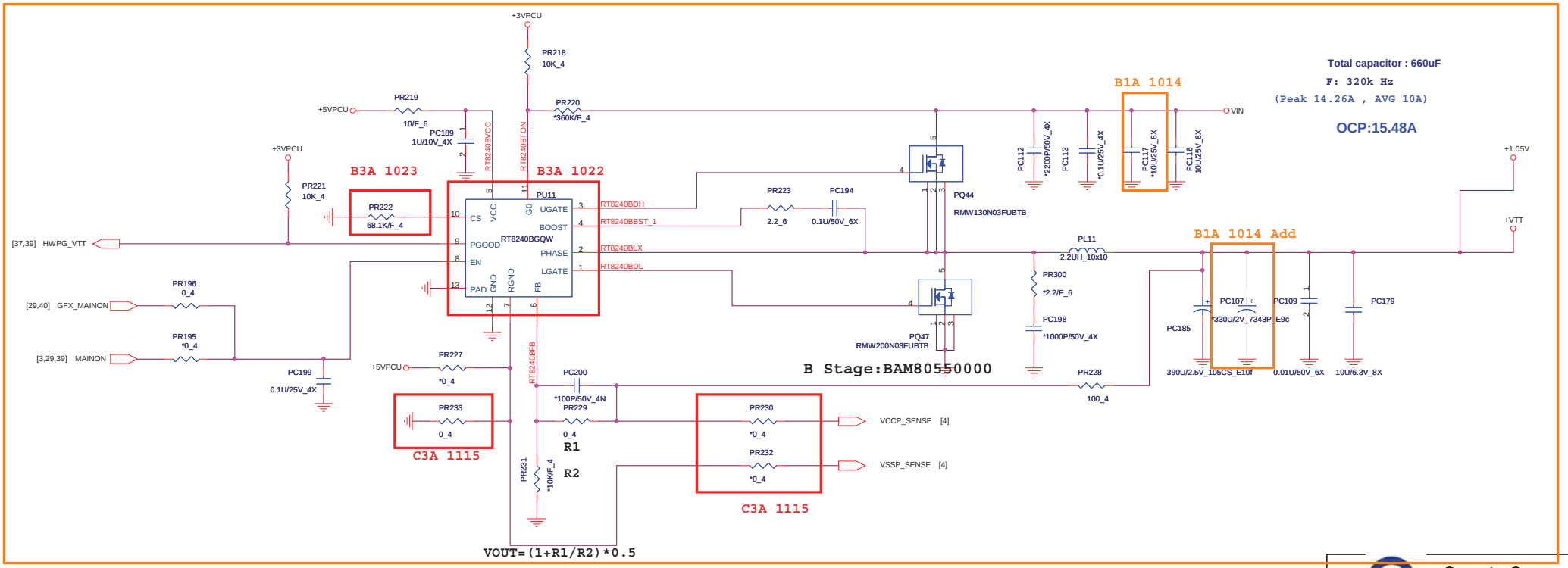
PROJECT : BLBD

Size	Document Number	Rev
	System 5V/3V (RT8210BGQW)	1A

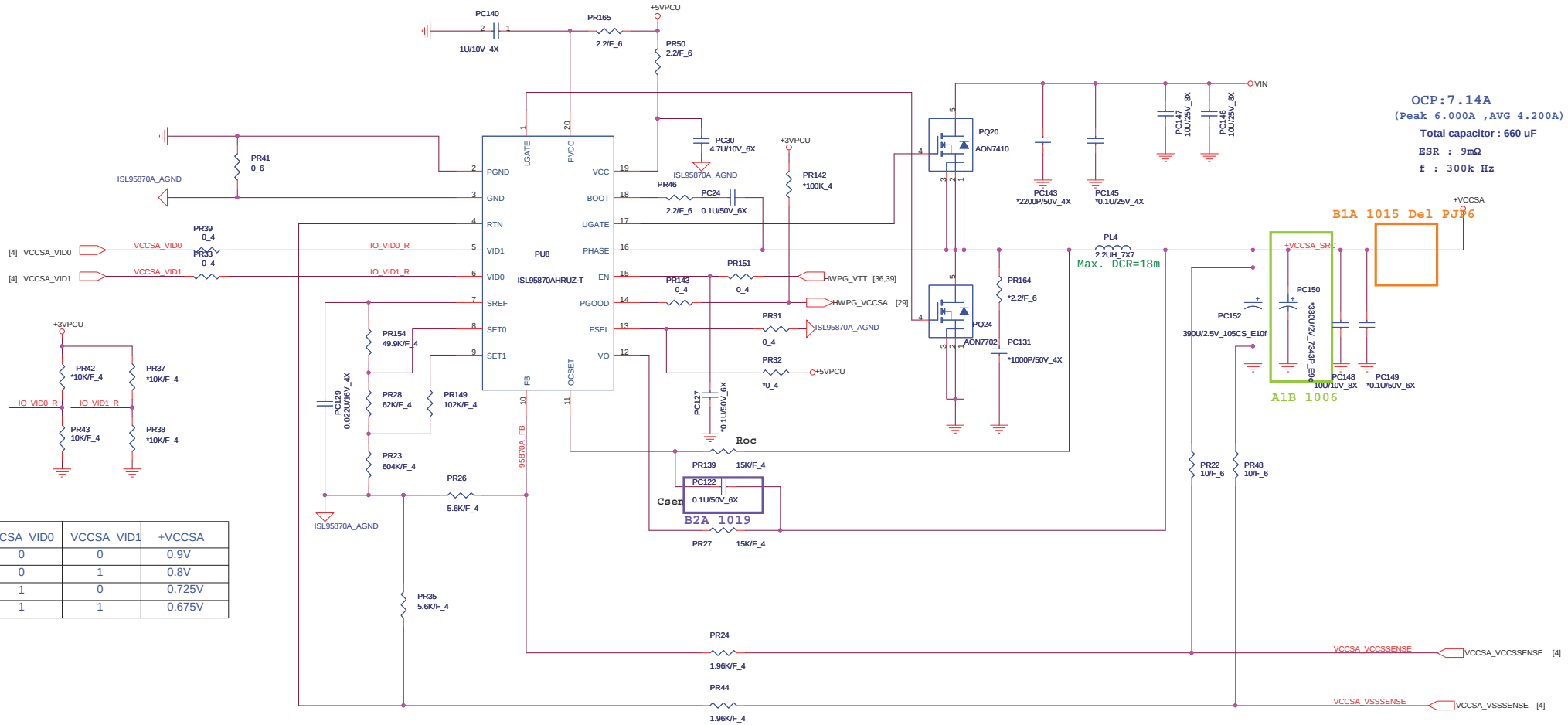
Date: Monday, November 22, 2010 Sheet 34 of 42



Quanta Computer Inc.		
PROJECT : BLBD		
Size	Document Number: DDR 1.5V(RT8207LGQW)	Rev: 1A
Date: Monday, November 22, 2010	Sheet 35 of 42	



Quanta Computer Inc.		
PROJECT : BLBD		
Size	Document Number: +VTT /+1.05V(UP1522RQDD)	Rev: 1A
Date: Monday, November 22, 2010	Sheet 36 of 42	

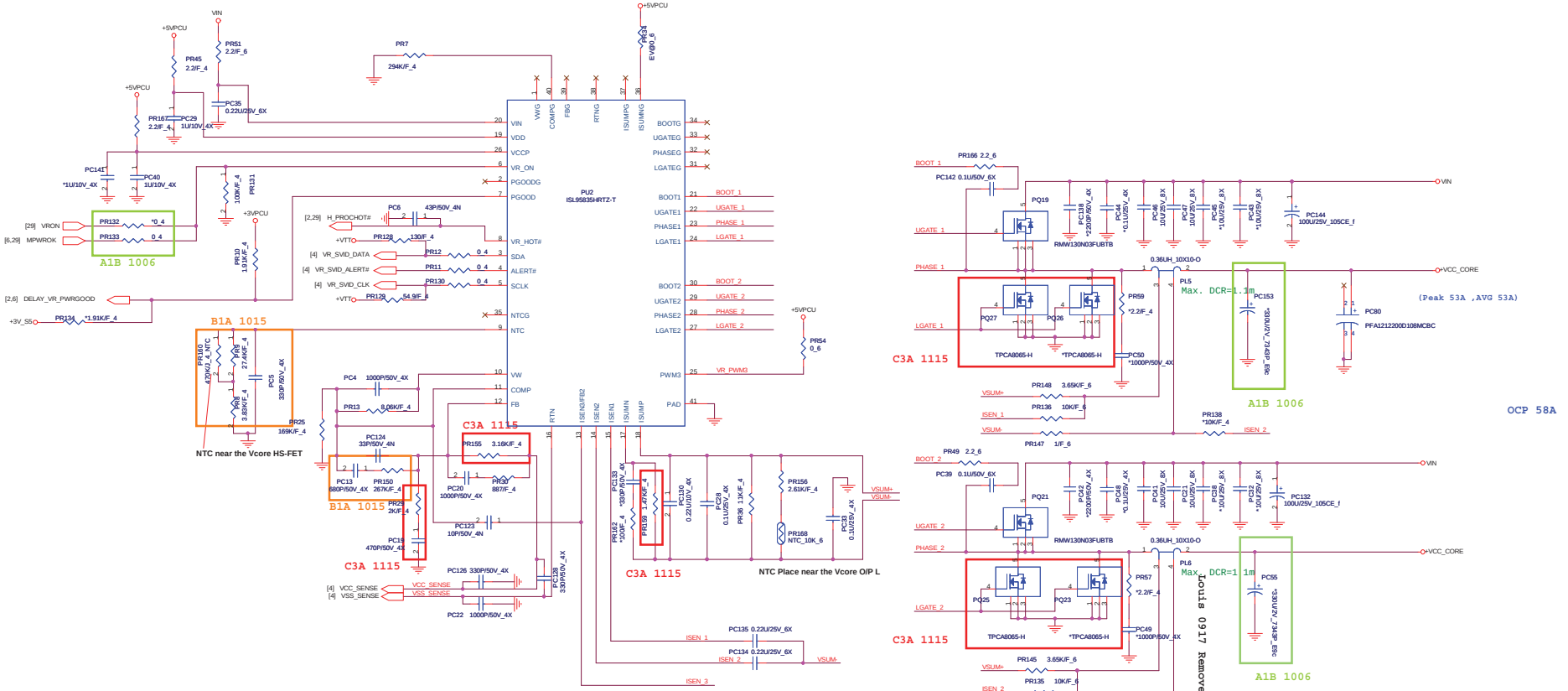


OCP:7.14A
(Peak 6.000A ,AVG 4.200A)
Total capacitor : 660 uF
ESR : 9mΩ
f : 300k Hz

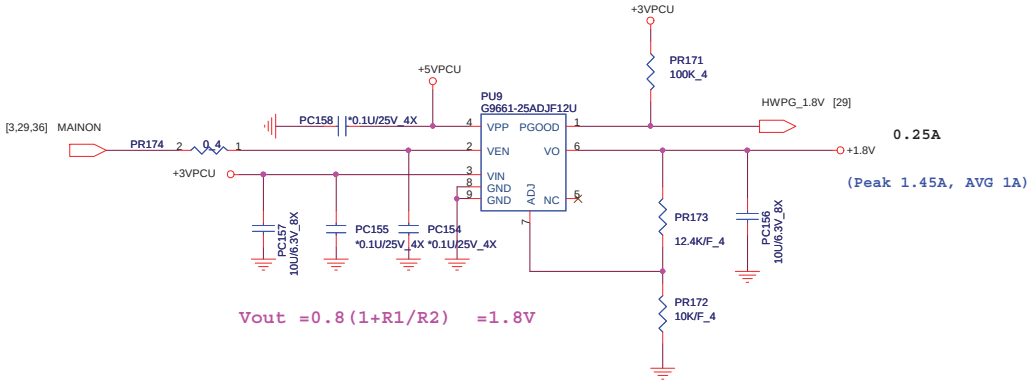
VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

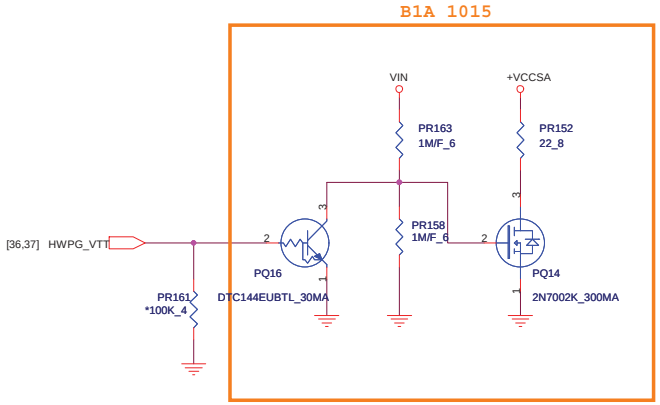
Quanta Computer Inc.
PROJECT : BLBD

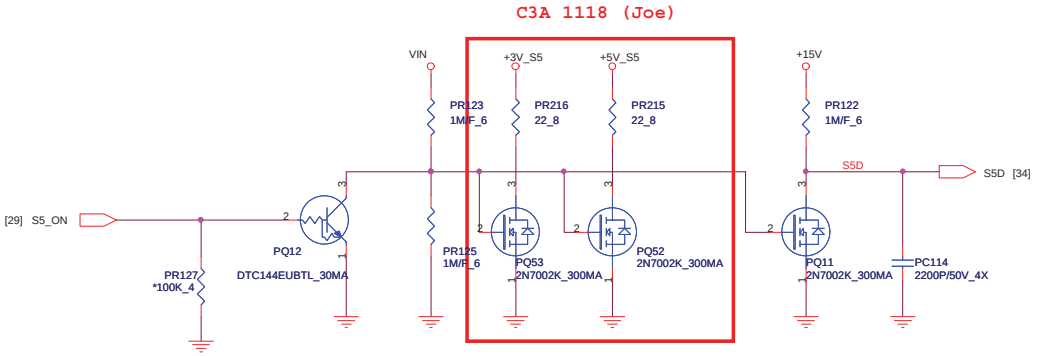
Size	Document Number	Rev
	+VCCSA ISL95870A)	1A
Date: Monday, November 22, 2010	Sheet 37 of 42	

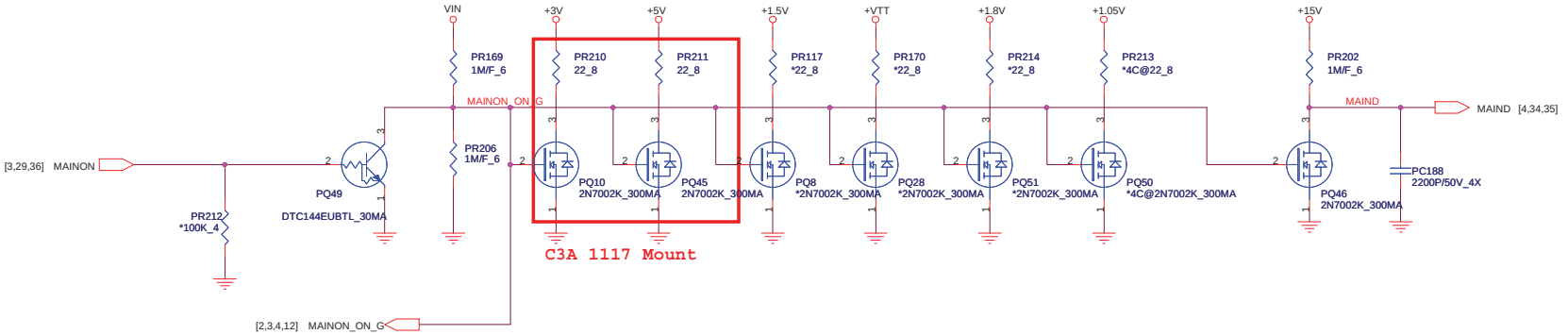


Quanta Computer Inc.		
PROJECT : BLBD		
Size	Document Number	Rev
	+VCC_CORE (ISL95835HRTZ-T)	1A
Date: Monday, November 22, 2010	Sheet 38 of 42	







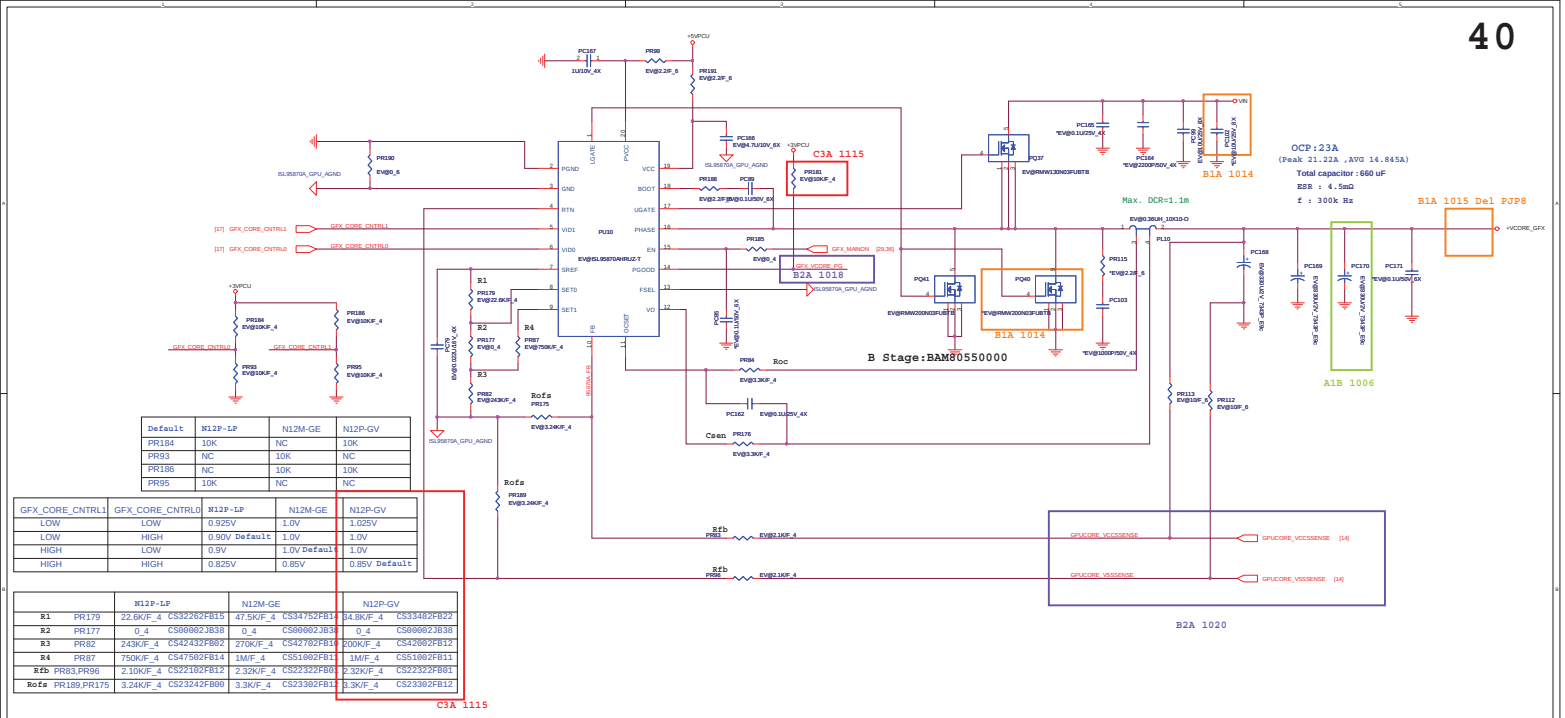


Quanta Computer Inc.

PROJECT : BLBD

Size	Document Number	Rev
	Discharge (1.5V_S5/1.8V)	1A

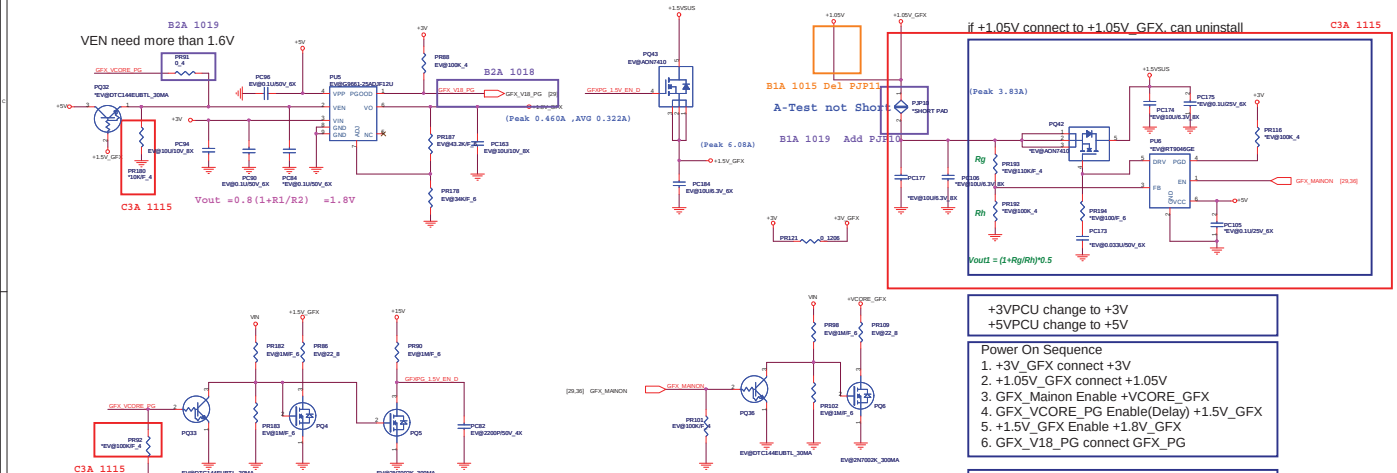
Date: Monday, November 22, 2010 Sheet 39 of 42



Default	N12P-LP	N12M-GE	N12P-GV
PR184	10K	NC	10K
PR93	NC	10K	NC
PR186	NC	10K	10K
PR95	10K	NC	NC

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12P-LP	N12M-GE	N12P-GV
LOW	LOW	0.925V	1.0V	1.025V
LOW	HIGH	0.90V Default	1.0V	1.0V
HIGH	LOW	0.9V	1.0V Default	1.0V
HIGH	HIGH	0.825V	0.85V	0.85V Default

		N12P-LP	N12M-GE	N12P-GV
R1	PR179	22.6K/F_4 CS32262FB15	47.5K/F_4 CS34752FB1	34.8K/F_4 CS33482FB22
R2	PR177	0_4 CS00002JB38	0_4 CS00002JB38	0_4 CS00002JB38
R3	PR82	243K/F_4 CS42432FB02	270K/F_4 CS42702FB12	200K/F_4 CS42002FB12
R4	PR87	750K/F_4 CS47502FB14	1M/F_4 CS51002FB11	1M/F_4 CS51002FB11
Rfb	PR83,PR86	2.10K/F_4 CS22102FB12	2.32K/F_4 CS23222FB01	2.32K/F_4 CS23222FB01
Rofs	PR189,PR175	3.24K/F_4 CS23242FB00	3.3K/F_4 CS23302FB12	3.3K/F_4 CS23302FB12

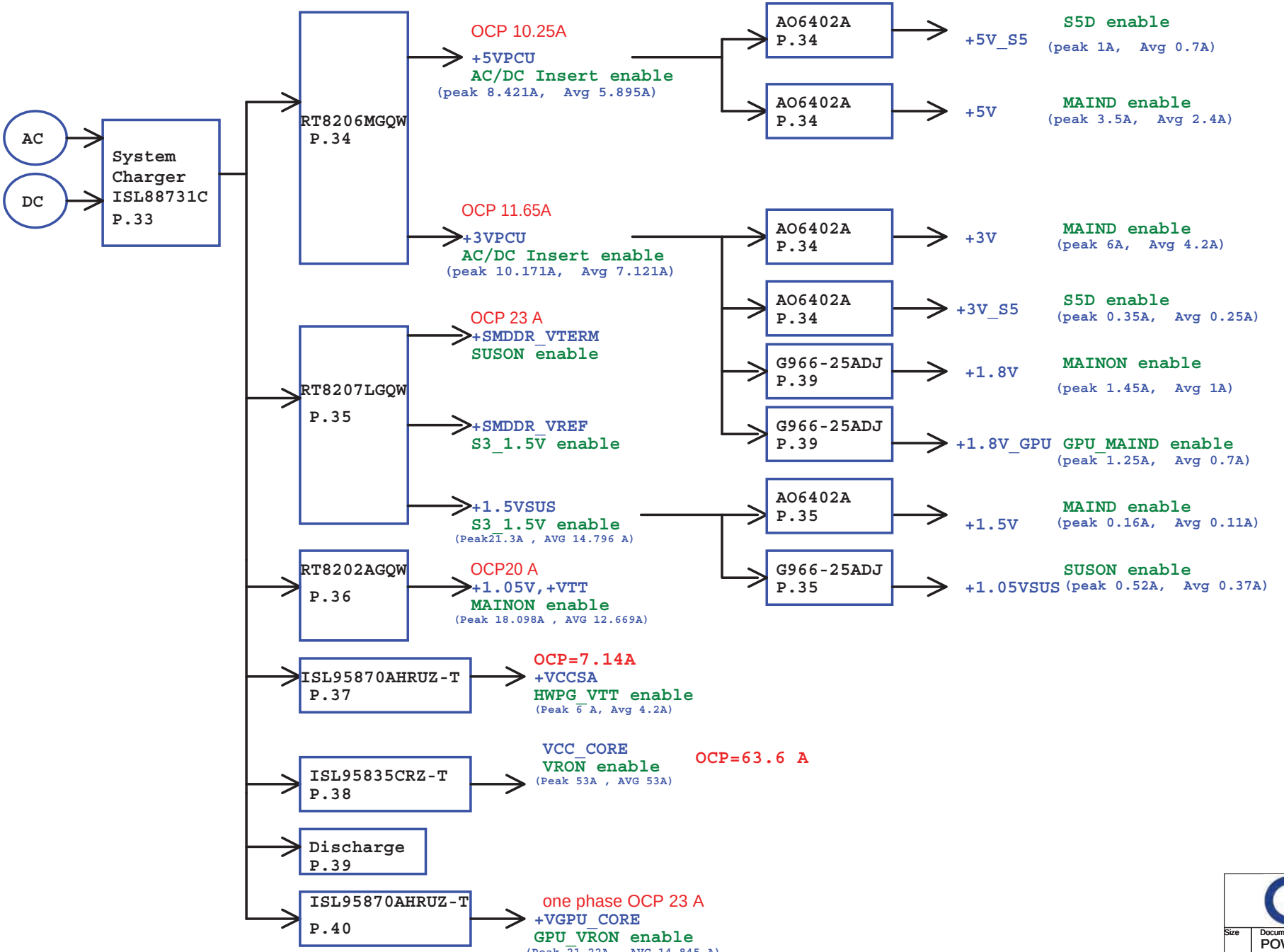


+3VPCU change to +3V
+5VPCU change to +5V

Power On Sequence
1. +3V_GFX connect +3V
2. +1.05V_GFX connect +1.05V
3. GFX_Mainon Enable +VCORE_GFX
4. GFX_VCORE_PG Enable(Delay) +1.5V_GFX
5. +1.5V_GFX Enable +1.8V_GFX
6. GFX_V18_PG connect GFX_PG

Power Off Sequence
compare +VCC3_GFX with +V1.8_GFX

Quanta Computer Inc.
PROJECT : BLBD
Size | Document Number: +VGACORE(ISL95870AHRUZ-T) | Rev: 1A
Date: Monday, November 23, 2009 | Sheet 40 of 42



Quanta Computer Inc.
PROJECT : BLBD

Size	Document Number	Rev
	POWER TREE TABLE	1A

Date: Monday, November 22, 2010 Sheet 41 of 42

Model	REV	CHANGE LIST
BLBD MB	1A	PAGE 2: Del R19 0 ohm PAGE 2: ADD R599 0 ohm, TP81,TP82,TP83,TP84,TP85,Tp86,TP87 PAGE 2: STUFF R385,R394,Q28,C601,R387. NC R386 PAGE 4: DEL C430, R37, R23, Add C477,C478,C479,C480,C740,C741,C742,C743,C744,C745,C746,R602,R603,R598, Stuff R21 PAGE 5: ADD TP89, TP1 PAGE 6: DEL R293, R503, NC R52, ADDR294 PAGE 8: ADD C750, C751, R601, STUFF R501, NC Q14, Q15 PAGE 9: DEL R253; R534 CHANGE TO PD PAGE 9: CHANGE Board ID9 strap Function name PAGE 10: ADD R604 PAGE 17: CHANGE GPU MULTI level strap select PAGE 17: MODIFY GPU STRAP 1 SETTING PAGE 22: CHANGE LVDS CN1 FOOTPRINT PAGE 23: MINI CARD NC R99, DEL R184 PAGE 23: ADD Q94,R920 BUT NC, ADD R921 AND MOUNT PAGE 25: DEL R68, R49 PAGE 25: MOUNT C502, C1, C2 PAGE 26: DEL R368, R369 PAGE 26: ADD C953 BUT NC PAGE 26: ADD C759,C732,C733,C734 PAGE 27: CHANGE ADOGND TO GND PAGE 27: ADD R342 BUT NC PAGE 27: NC C735 PAGE 28: DEL R579, ADD C758 PAGE 28: ADD R579, R600 PULL 3ND_MBCLK,3ND_MBDATA, NC R197 PAGE 28: ADD SKU_STRAP1,SKU_STRAP2,SKU_STRAP3 PAGE 28: CHANGE NET NAME FOR GFX_VCORE_PG TO GFX_V18_PG PAGE 31: LED1,LED4,LED5,LED6 change symbol and Foot-print PAGE 33: MOUNT PR5,PC2,PC51, ADD PU12 BUT NC PAGE 34: CHANGE PU4 TO PM6886 PAGE 34: NC PR100,PR114,PR208,PR77,PR78, DEL PJP7 PAGE 35: NC PR159, DEL PJP1,PJP2 PAGE 36: CHANGE +VTT/+1.05V SCHEMATIC, CHANGE PU11 TO RT8240 PAGE 37: DEL PJP6 PAGE 40: DEL PJP8,PJP11, ADD PR91, NC PQ40 PAGE 28: ADD Q3502 PAGE 3: Add S3 Power reduction componet R489 PAGE 31: Delete Card Reader LED componet Q16 PAGE 31: Add Card Reader LED componet Q3052 PAGE 8: Add USB_BUS_SW2/3 0 ohm R596,R597 PAGE 10: Add +VCCAFDI_VRM PD Cap C381 PAGE 17: Add 15K strap3/4 for GPU R3518,R3534 PAGE 24: Add common choke for USB EMI solution L73 PAGE 24: Reserve resistor for USB EMI solution RP24 PAGE 25: Add ODD Zero power diischarge R614 PAGE 25: Reserve ODD Zero power diischarge C577 PAGE 26: Change Value for LAN 51@ to 52@, C95,C96,C100,C102,RN3,RN4 PAGE 27: Change Card Reader controller U22 source PAGE 29: Change MS Strap Power name +3V_PCU to +3VPCU PAGE 36: 1.Add PR233 0 ohm PD form Pin7, NC PR230,PR232 PAGE 38: Change PR155 3.09K to 3.16K, PR159 1.37K to 1.47K, mount PR29,PC19 PAGE 38: Change PQ26,PQ27,PQ23,PQ25 RMW200N03FUBTB to TPCA8065-H PAGE 40: Change PR181 to 10K PAGE 40: Change PR181 to 10K,Reserve PR92 100K ,Reserve +1.05 part all material, Reserve PR180 10K PAGE 40: Voltage Setting for N12P-GV PAGE 2: Add R118 R413, reserve R104,R105,Q5 for cost down Q5	

MODEL	BLBD	
PAGE	FROM	To
1	1A	
2	1A	
3	1A	
4	1A	
5	1A	
6	1A	
7	1A	
8	1A	
9	1A	
10	1A	
11	1A	
12	1A	
13	1A	
14	1A	
15	1A	
16	1A	
17	1A	
18	1A	
19	1A	
20	1A	
21	1A	
22	1A	
23	1A	
24	1A	
25	1A	
26	1A	
27	1A	
28	1A	
29	1A	
30	1A	
31	1A	
32	1A	
33	1A	
34	1A	
35	1A	
36	1A	
37	2A	
38	2A	
39	2A	
40	2A	
41	2A	
42	2A	
43	2A	
44	2A	
45	2A	
46	2A	
47	2A	
48	2A	
49	2A	
50	2A	

DOC NO. 204	PROJECT MODEL :	BLBD	APPROVED BY:	Angelo Su	DATE:	2010/10/01
	PART NUMBER:		DRAWING BY:	Angelo Su	REVISON:	1A

Quanta Computer Inc.
PROJECT : BLBD
Size | Document Number: Change list | Rev: 1A
Date: Monday, November 22, 2010 | Sheet 42 of 42