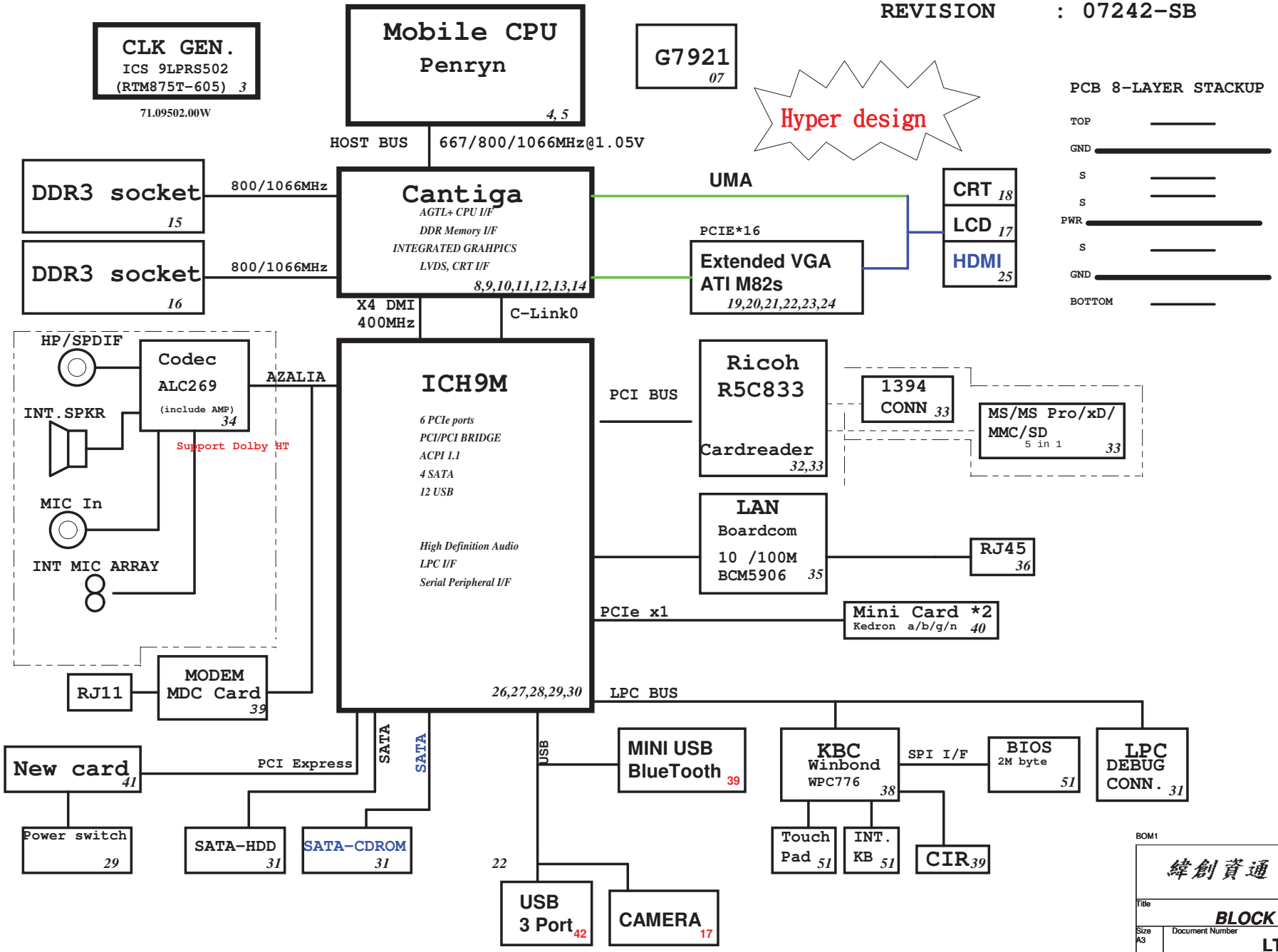
Olympus Block Diagram

Project code: 91.4Y701.001
PCB P/N :
REVISION : 07242-SB



PCB 8-LAYER STACKUP

TOP
GND
S
S
PWR
S
GND
BOTTOM

SYSTEM DC/DC ISL6236 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC TPS51124 40	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(11A) 1D5V_S3(10A)

TPS51117 39	
DCBATOUT	1D8V_S3 (2.5A)

TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5308 39	
3D3V_S0	2D5V_S0 (300mA)

CHARGER BQ24750 42	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6266A 37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

NB DC/DC ISL6263A 41	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE

SC411 48	
DCBATOUT	1D5V_S3

BOM1

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Title: BLOCK DIAGRAM

Size: A3 | Document Number: LT32P | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 1 of 53

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

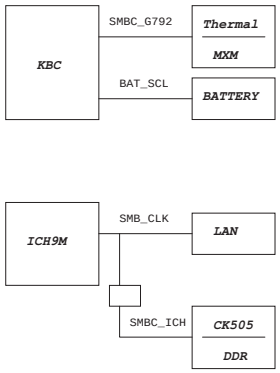
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIE is operational (Default) 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



PCI Routing

page 17

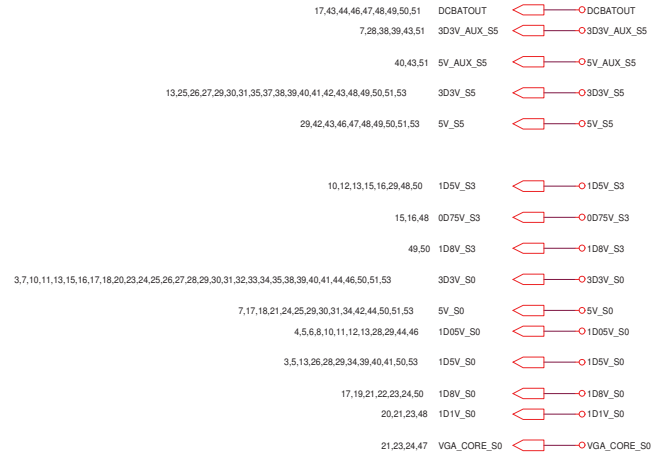
	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	Combo(ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1



BOM1

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Title: Reference

Size: C | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 2 of 53

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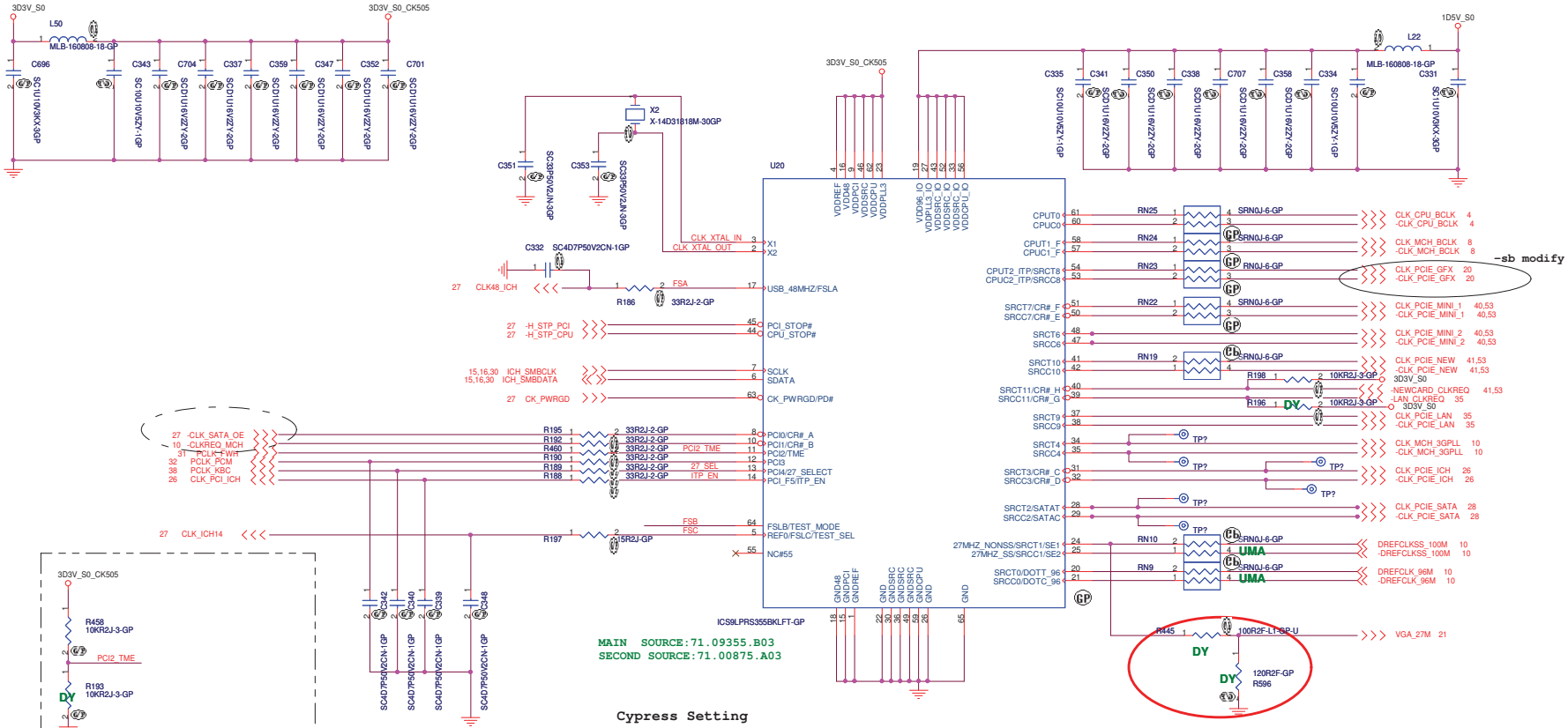

Cypress Setting

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M
0	0	0	266M

default

ITP_EN	Output
0	SRC8
1	CPU_ITP

UMA =0
DIS =1

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1	SRCT0	SRCC0	27M_NSS	27M_SS

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

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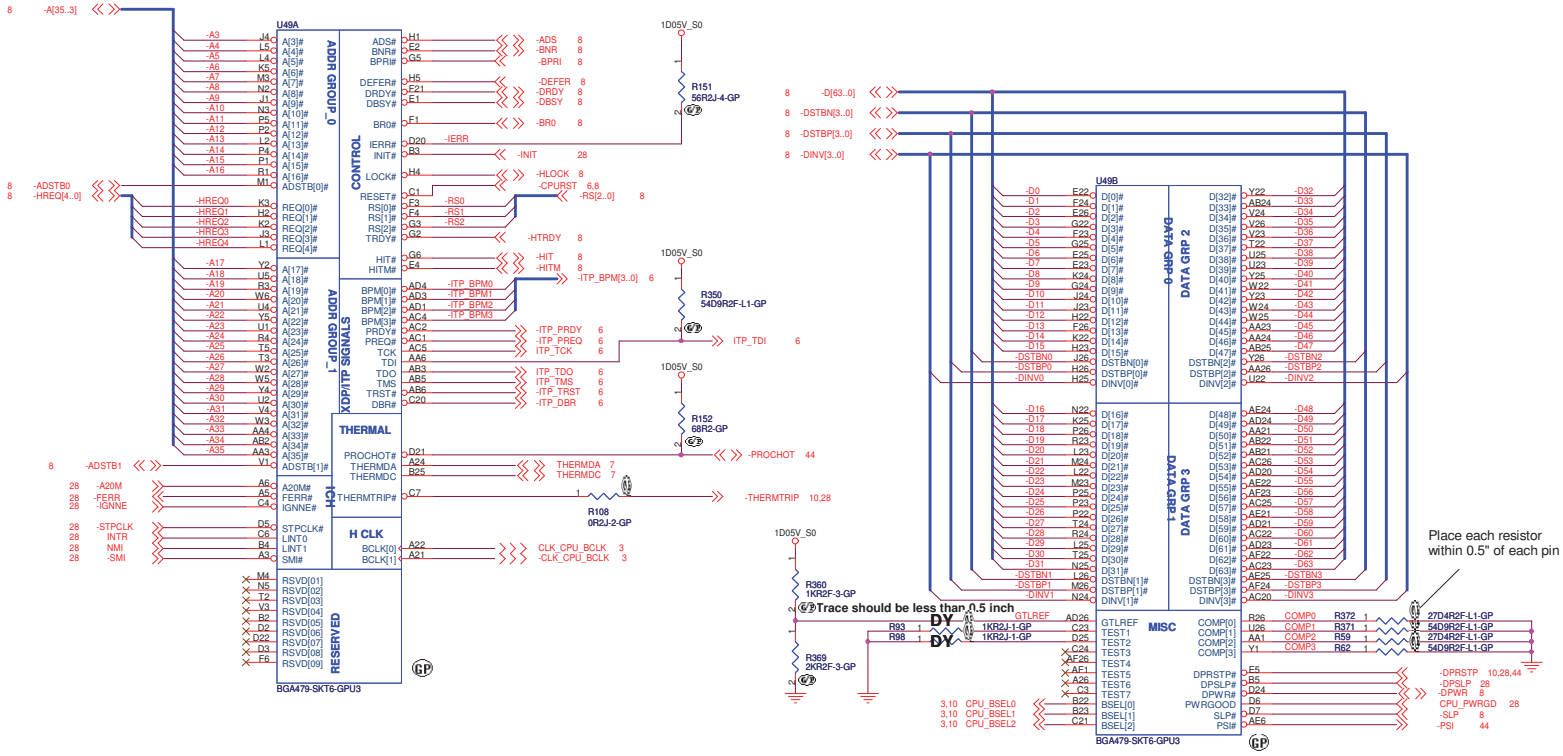
Title: Clock Generator

Size | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 3 of 53



BOM1

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Title: **Penryn CPU(1/2)**

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 4 of 53

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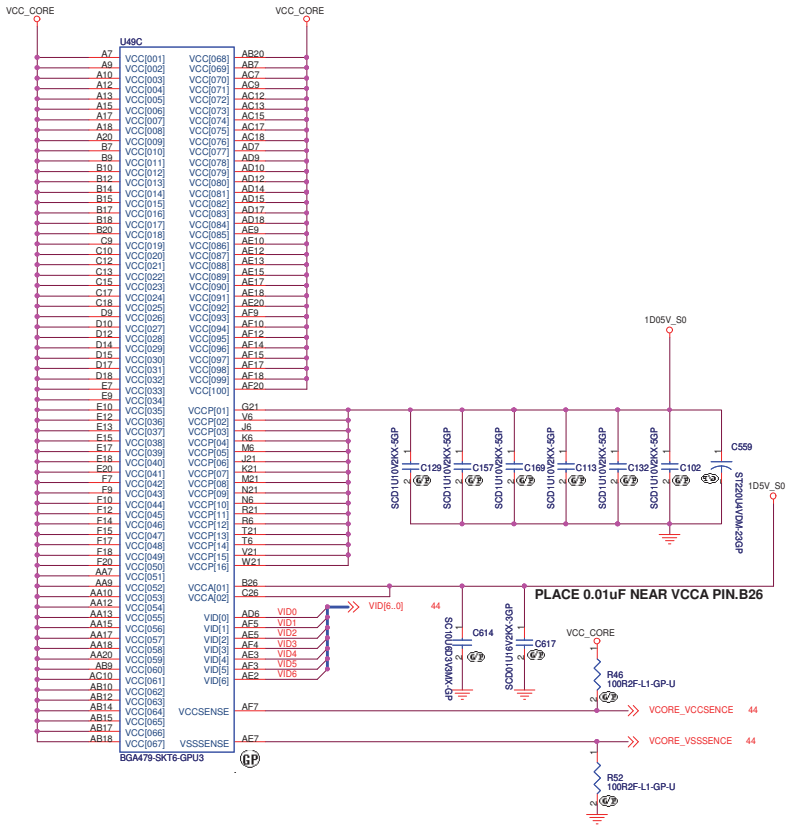

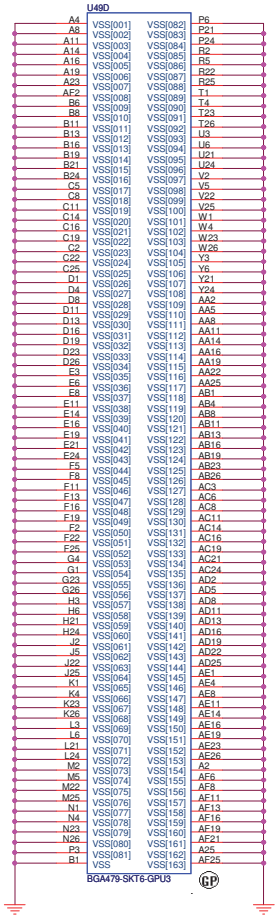

BOM1

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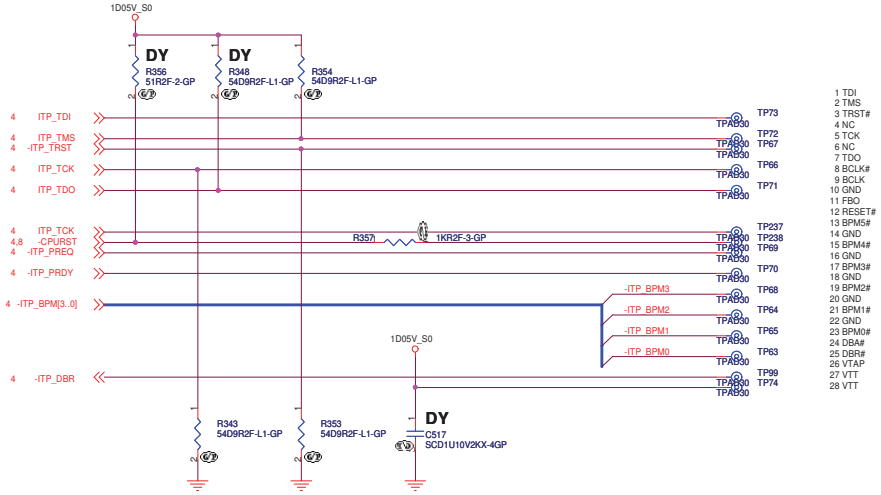
Title	***Penryn CPU(2/2)***	
Size C	Document Number **Olympus**	Rev **SA**
Date: Wednesday, December 26, 2007	Sheet 5 of 53	



(*1) TCK SIGNAL IS BRANCHED AT CPU's PIN

(*2) CPURST# SIGNAL IS BRANCHED AT GMCH's PIN

Ref Des	For ITP-XDP
J1	NO_ASM-->ASM
C157	NO_ASM-->ASM
R140	NO_ASM-->1K 5% ASM
R144	ASM (No Change)
R136	ASM-->NO_ASM
R145	ASM (No Change)
R141	ASM-->54.9 1% ASM
R143	ASM-->54.9 1% ASM

BOM1

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Title: ***ITP CONN***

Size: C | Document Number: **Olympus** | Rev: **SB**

Date: Wednesday, December 26, 2007 | Sheet 6 of 53

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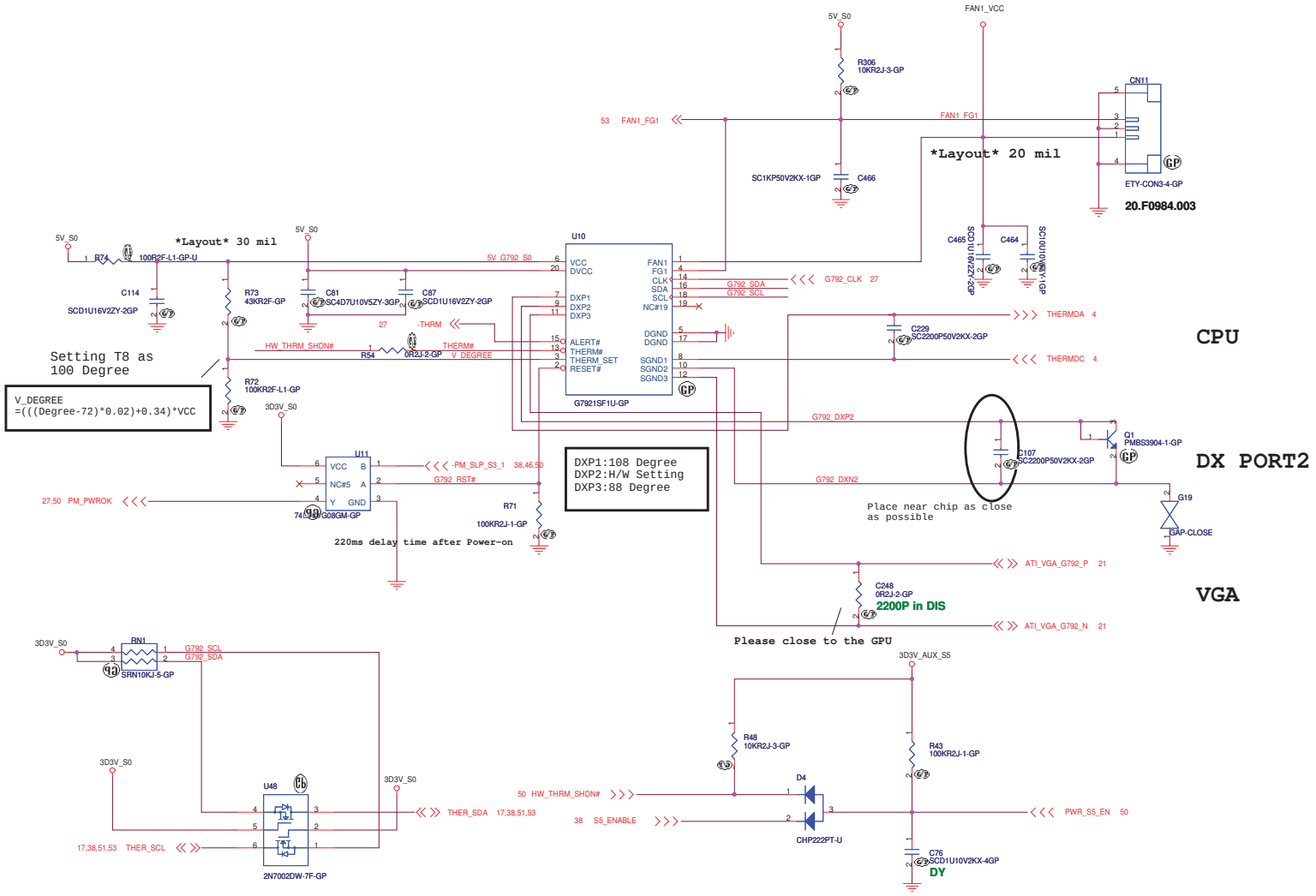

BOM1

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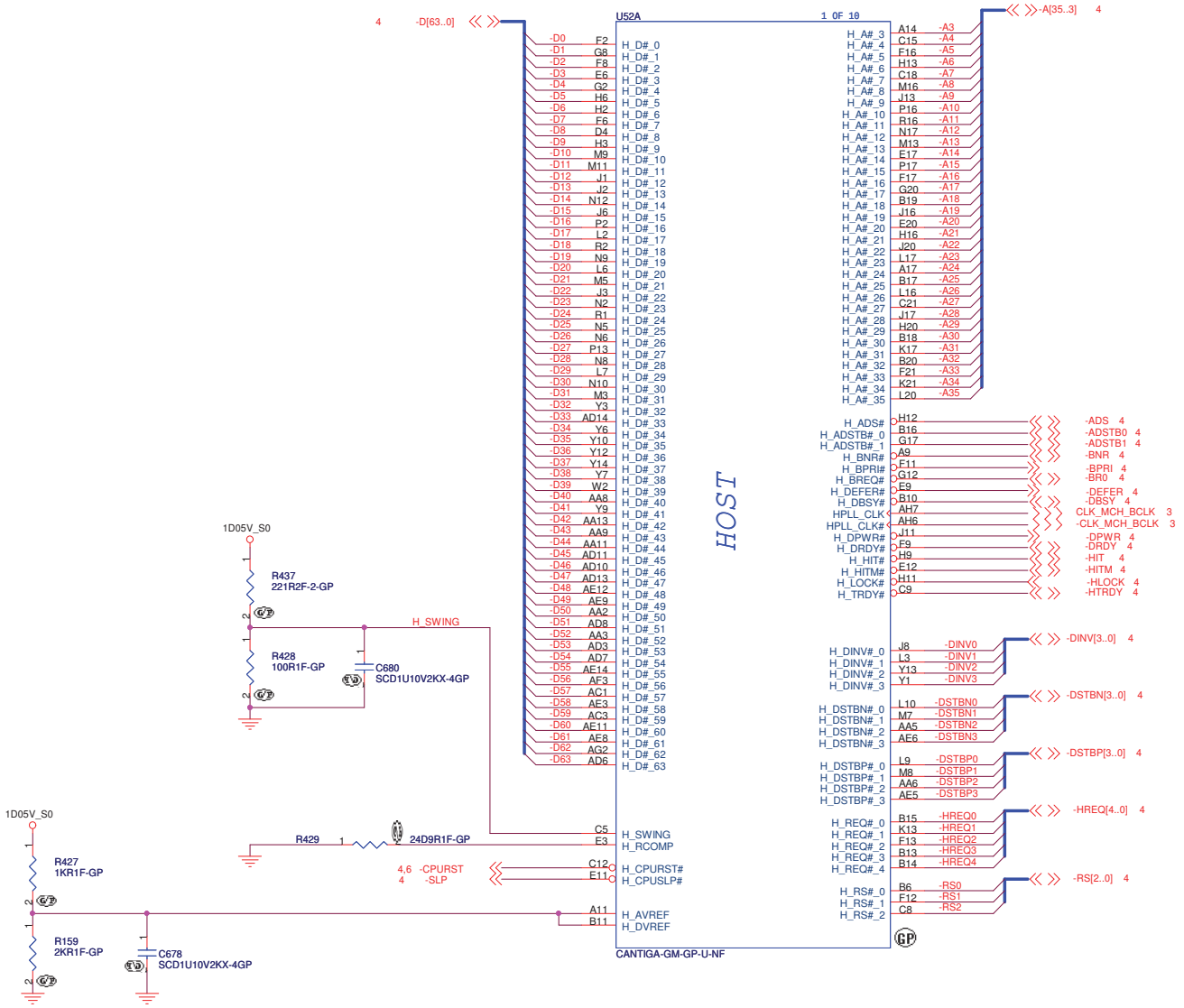
Title	***Thermal/Fan Controllor G792***	
Size C	Document Number **Olympus**	Rev **SB**
Date: Wednesday, December 26, 2007	Sheet 7 of 53	



Route H_XSWING & H_YSWING 10 mil wide / 20 mil spacing

Route H_XRCOMP & H_YRCOMP 10 mil wide / 20 mil spacing

BOM1

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Title: **Cantiga(1/7):HOST I/F**

Size	Document Number	Rev
A3	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 8 of 53

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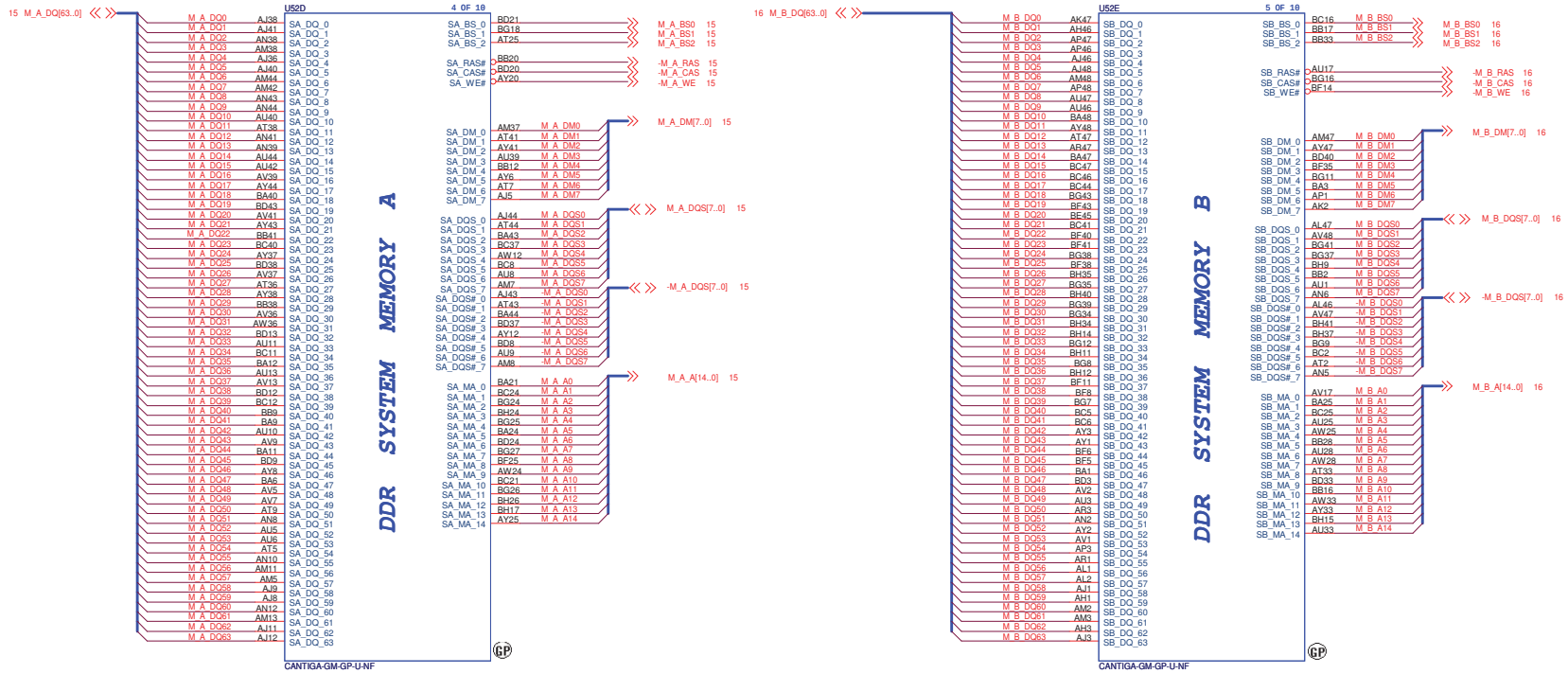

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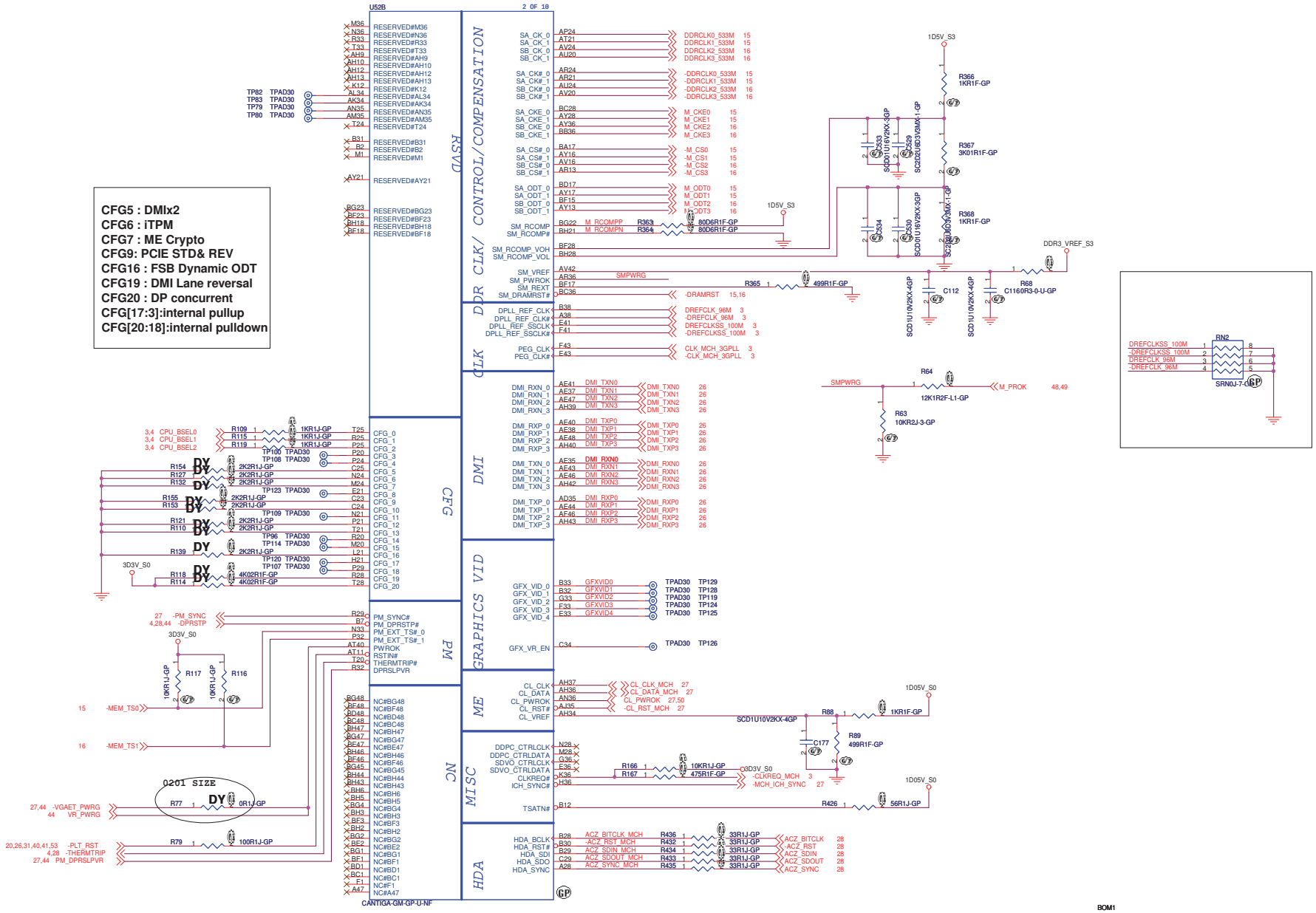
Title: ***Cantiga(2/7):DDR3***

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 9 of 53

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS



BOM1

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Title: Cantiga(3/7):DMI/PM/CFG/GF

Size: C | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 10 of 53

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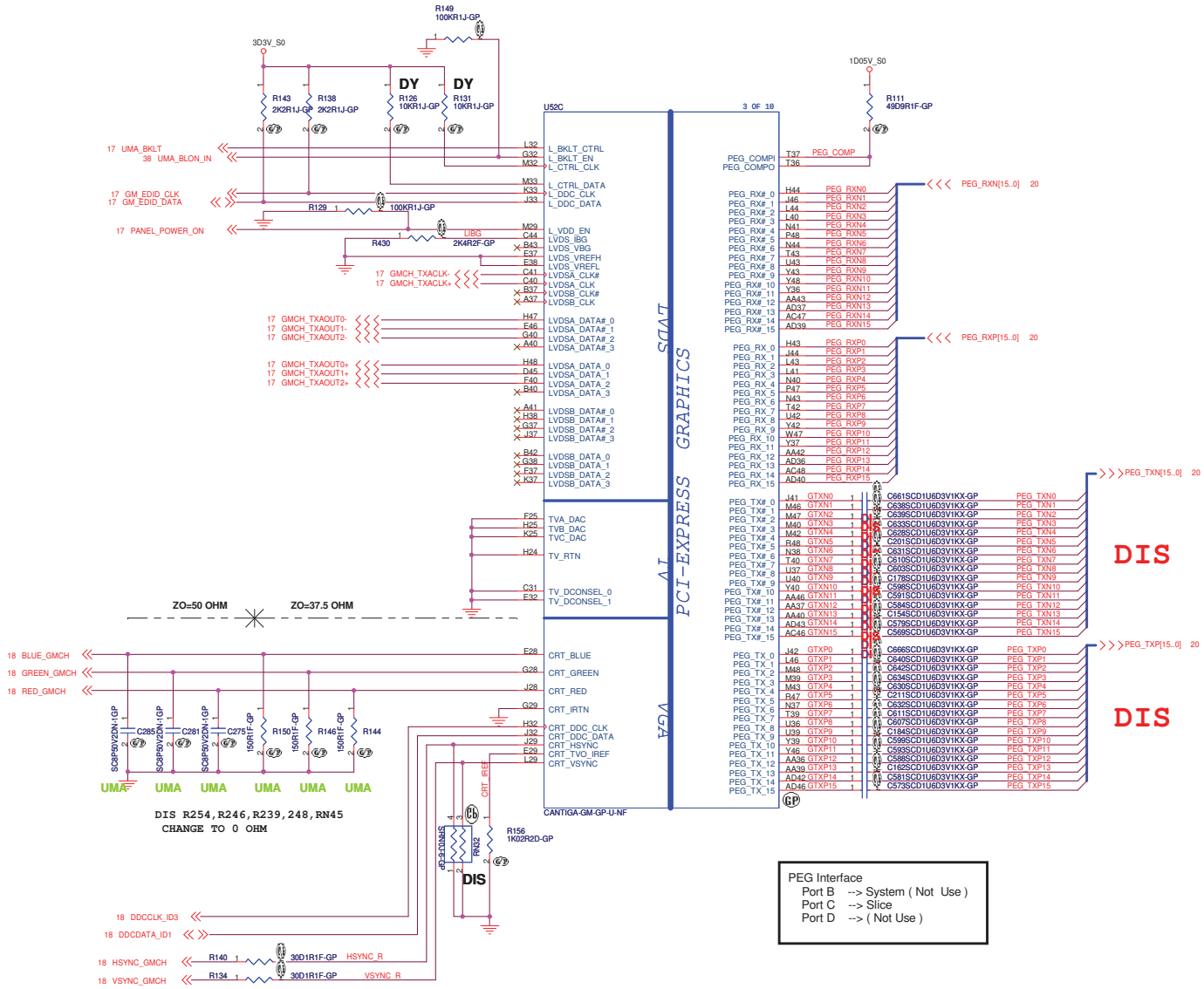

PEG Interface
Port B --> System (Not Use)
Port C --> Slice
Port D --> (Not Use)

BOM1

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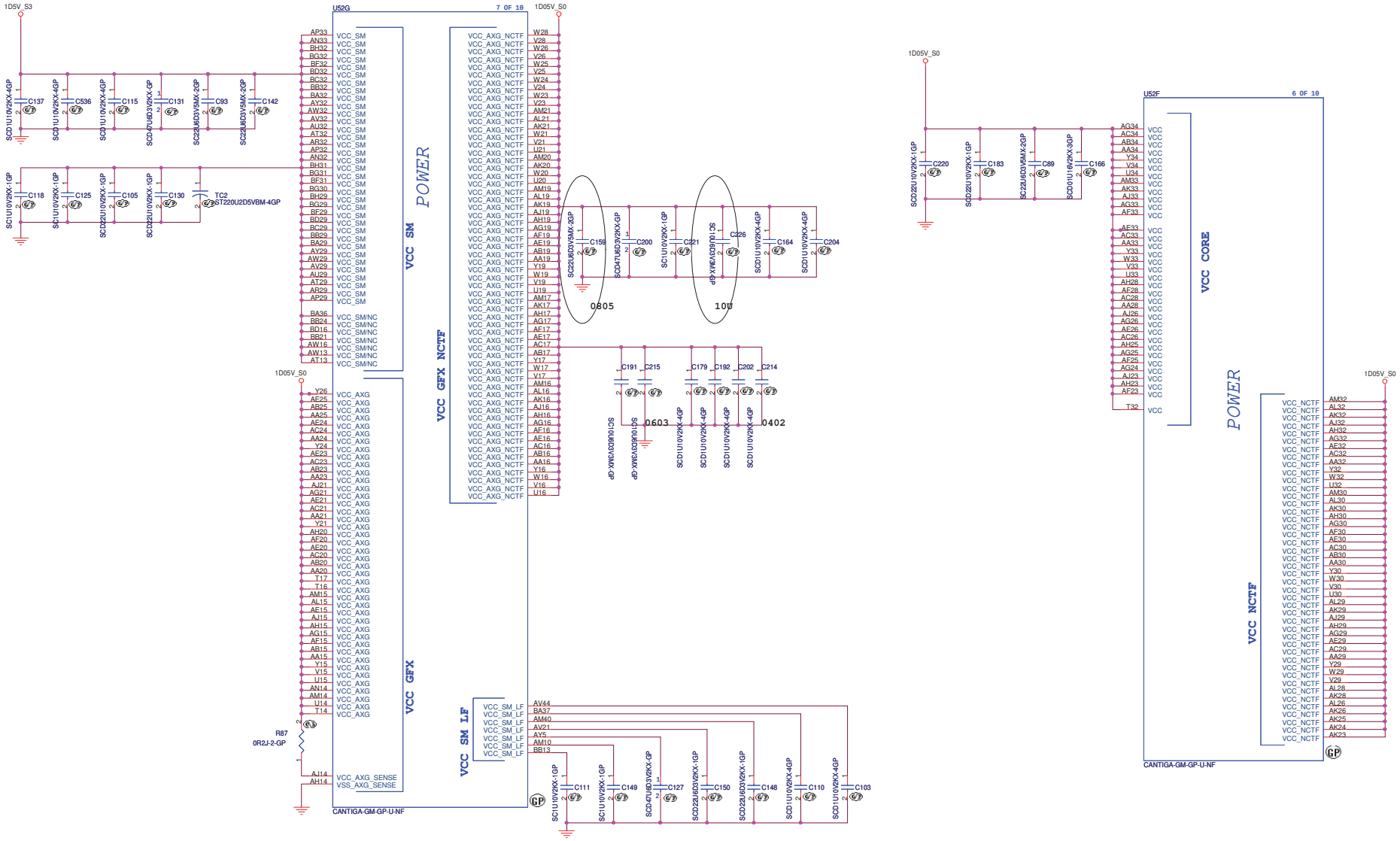
Title: CANTIGA(5/7)-VGA/LVDS

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 11 of 53



BOM1

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Title: Cantiga(5/7):VCC

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 12 of 53

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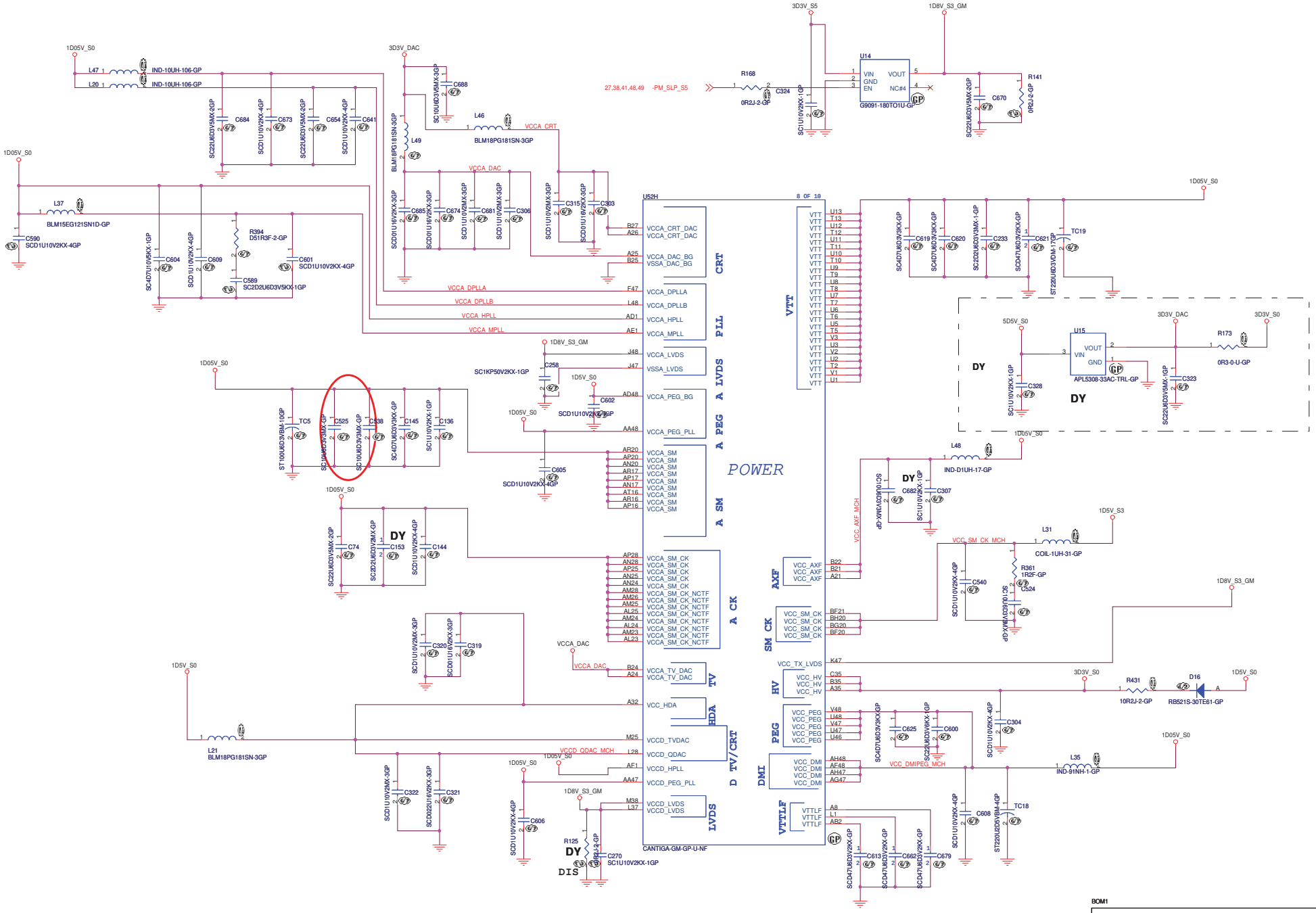

BOM1

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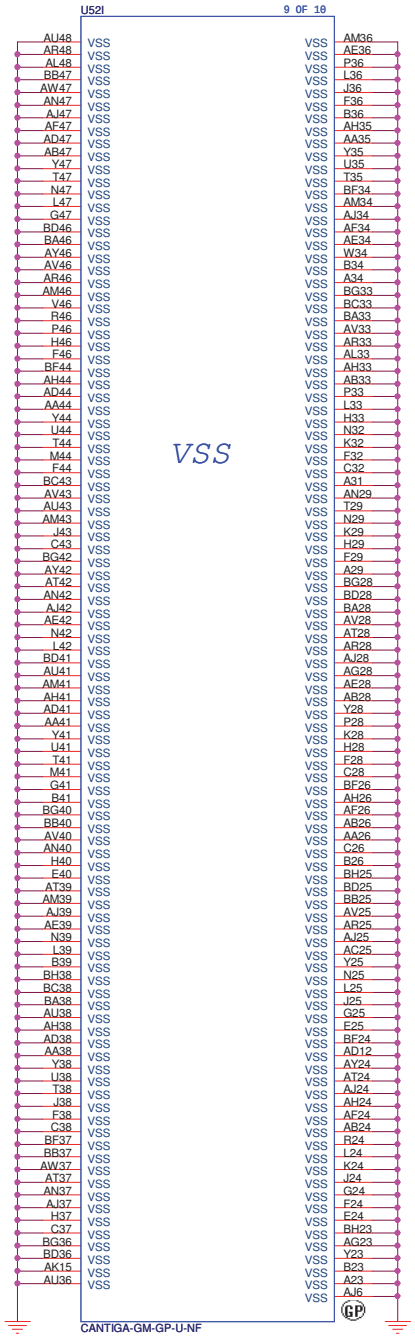
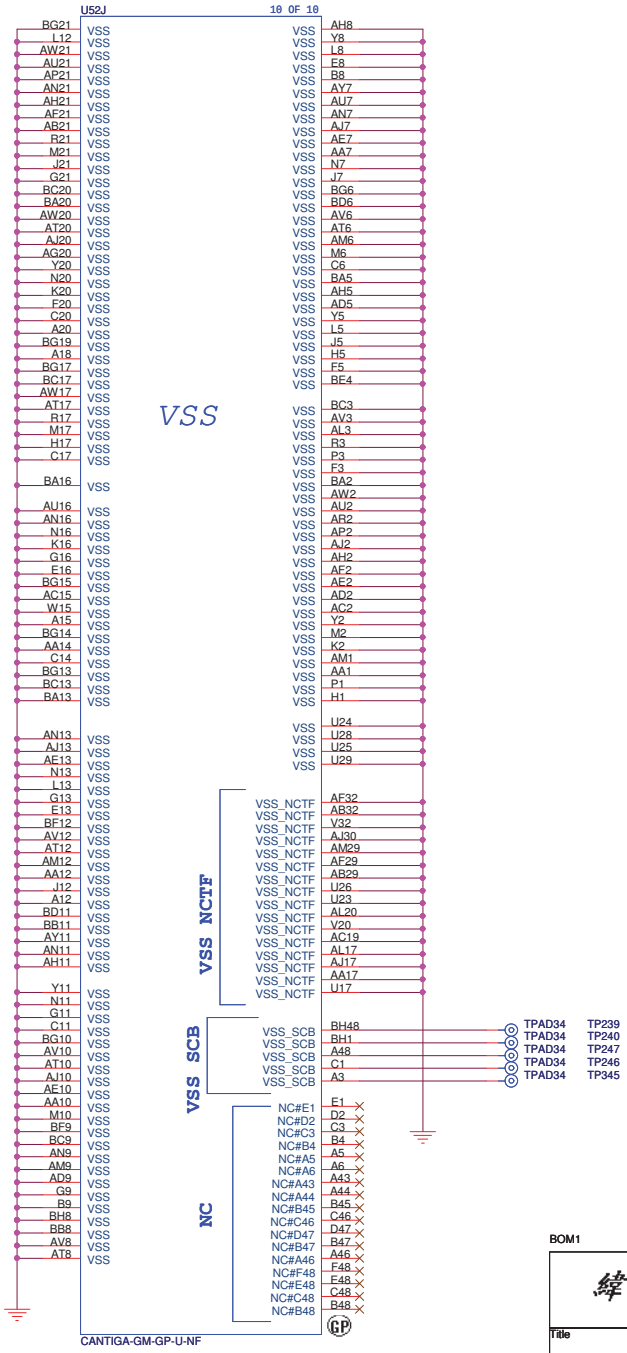
Title: Cantiga(6/7):VCC

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 13 of 53





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Title: ***Cantiga(8/7):GND***

Size	Document Number	Rev
A3	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 14 of 53

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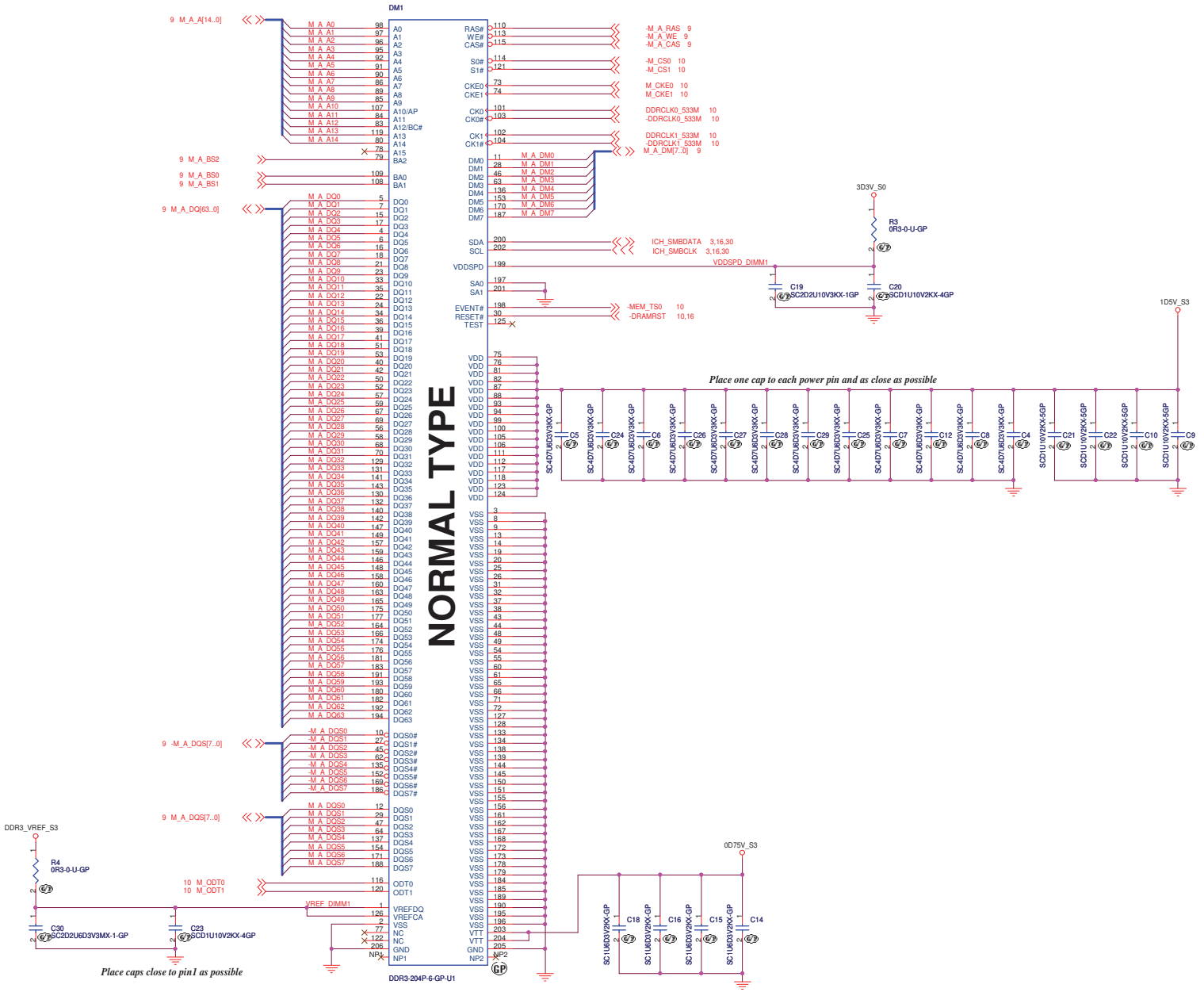

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BOM1

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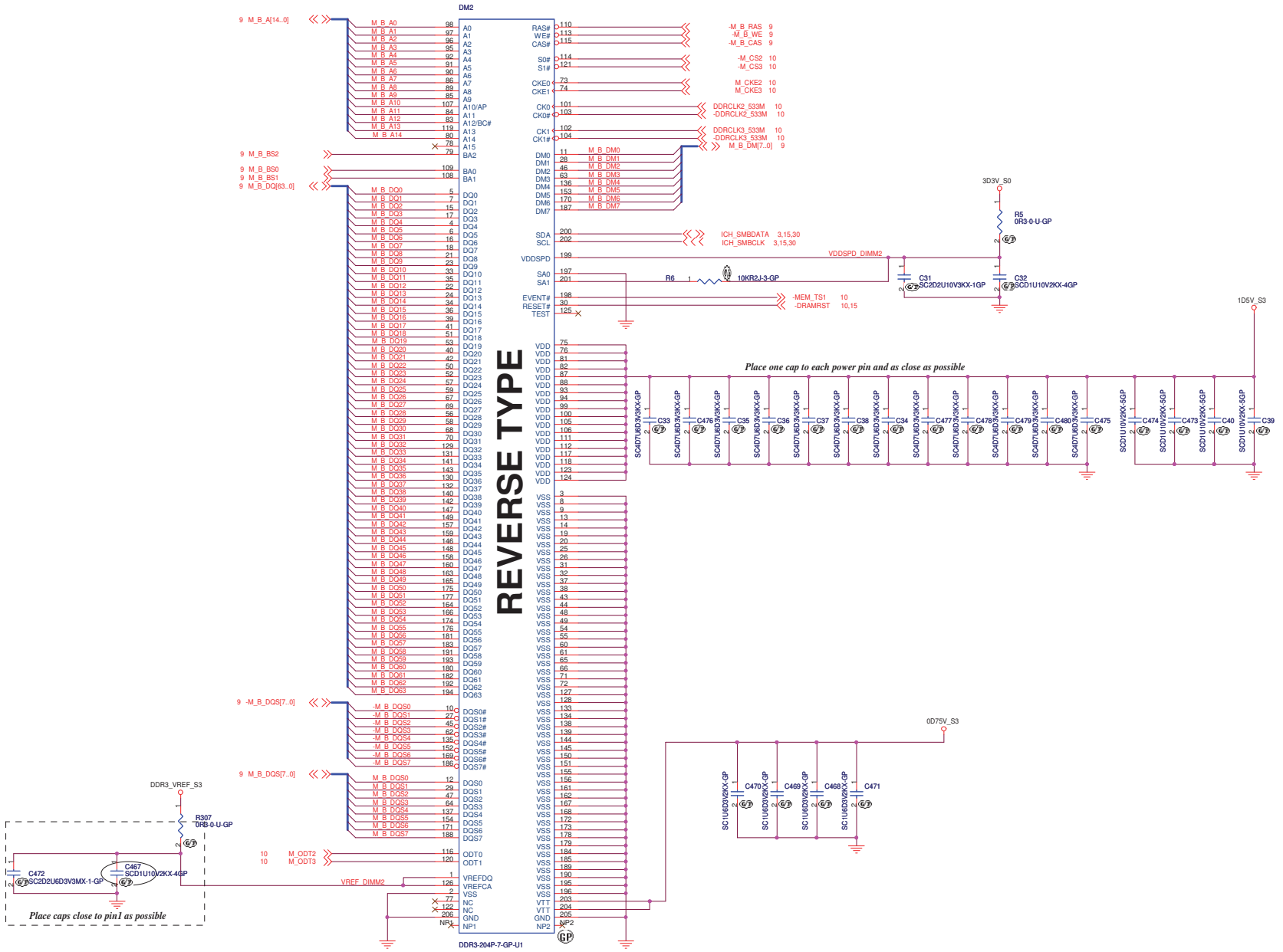
Title: DDR3 SODIMM-A (NORMAL TYPE)

Size	Document Number	Rev
C	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 15 of 53



BOM1

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Title	***DDR3 SODIMM-B (REVERSE TYPE)***
Size C	Document Number: **Olympus** — Rev: **SB**
Date: Wednesday, December 26, 2007	Sheet 16 of 53

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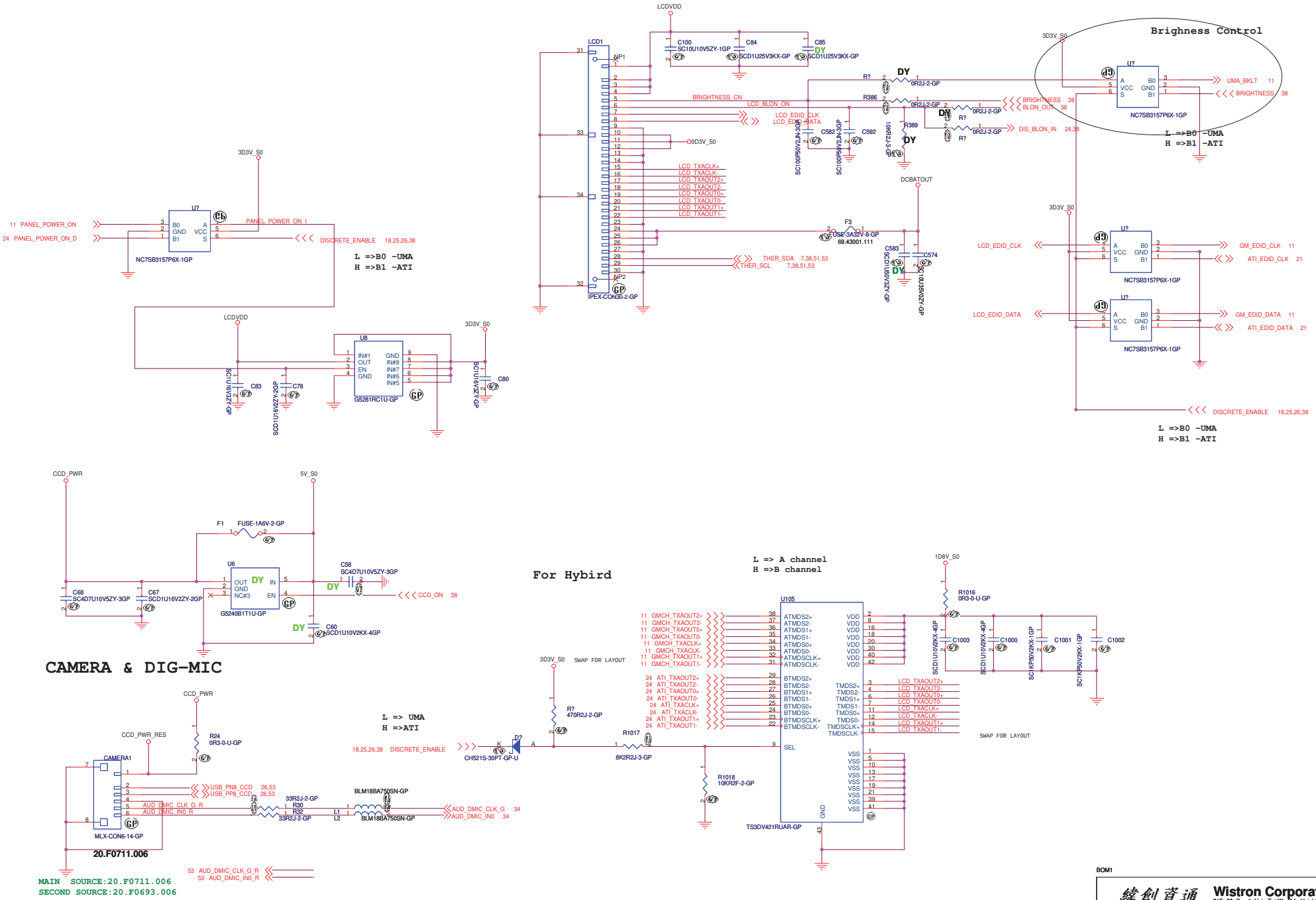
LCD/INVERTER CONN



BOM1

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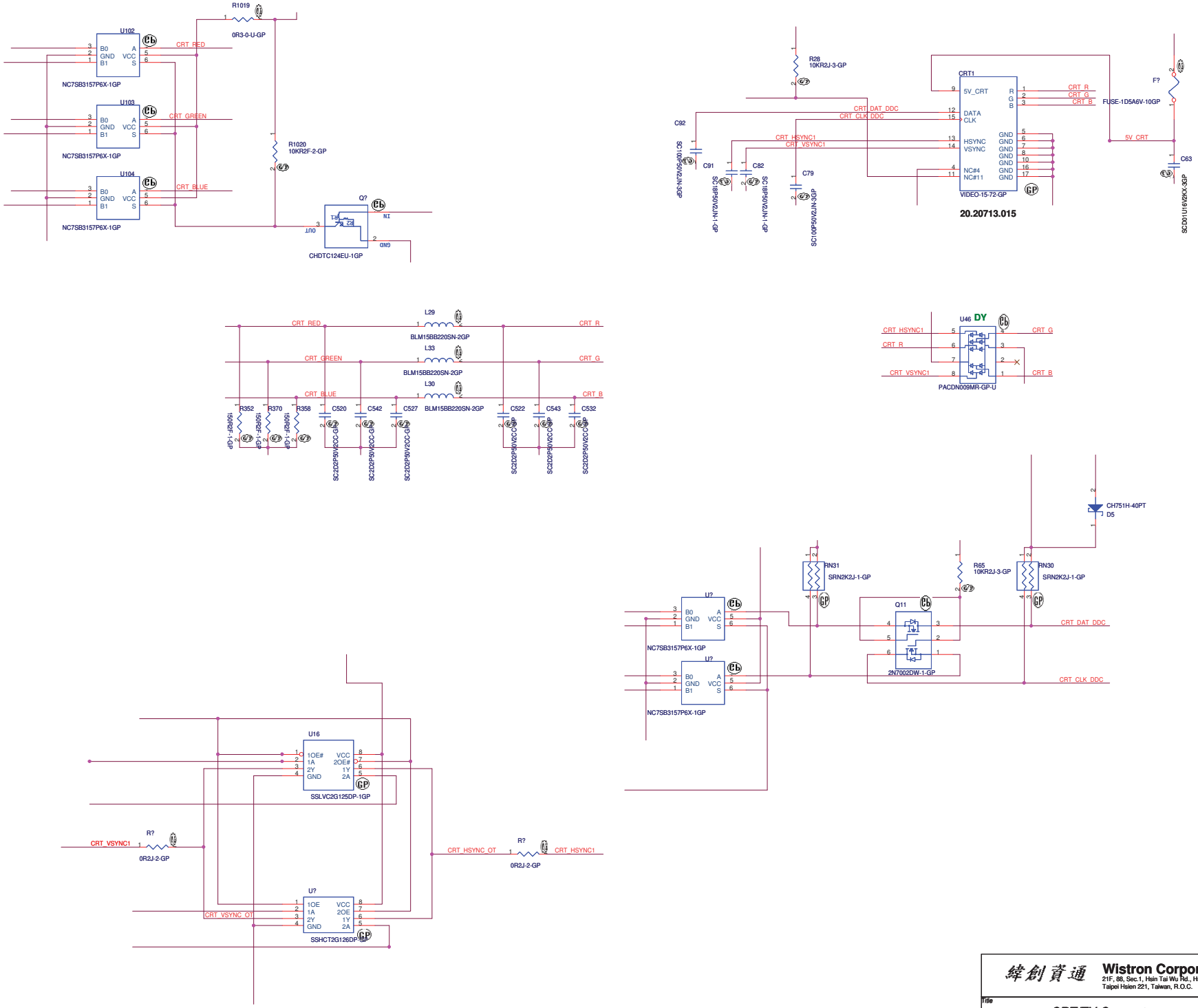
Title: LCD CONN & CAMERA & DIG-MIC

Size | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 17 of 53



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CRT/TV Connector*	
Size	Document Number: Olympus	Rev: SB
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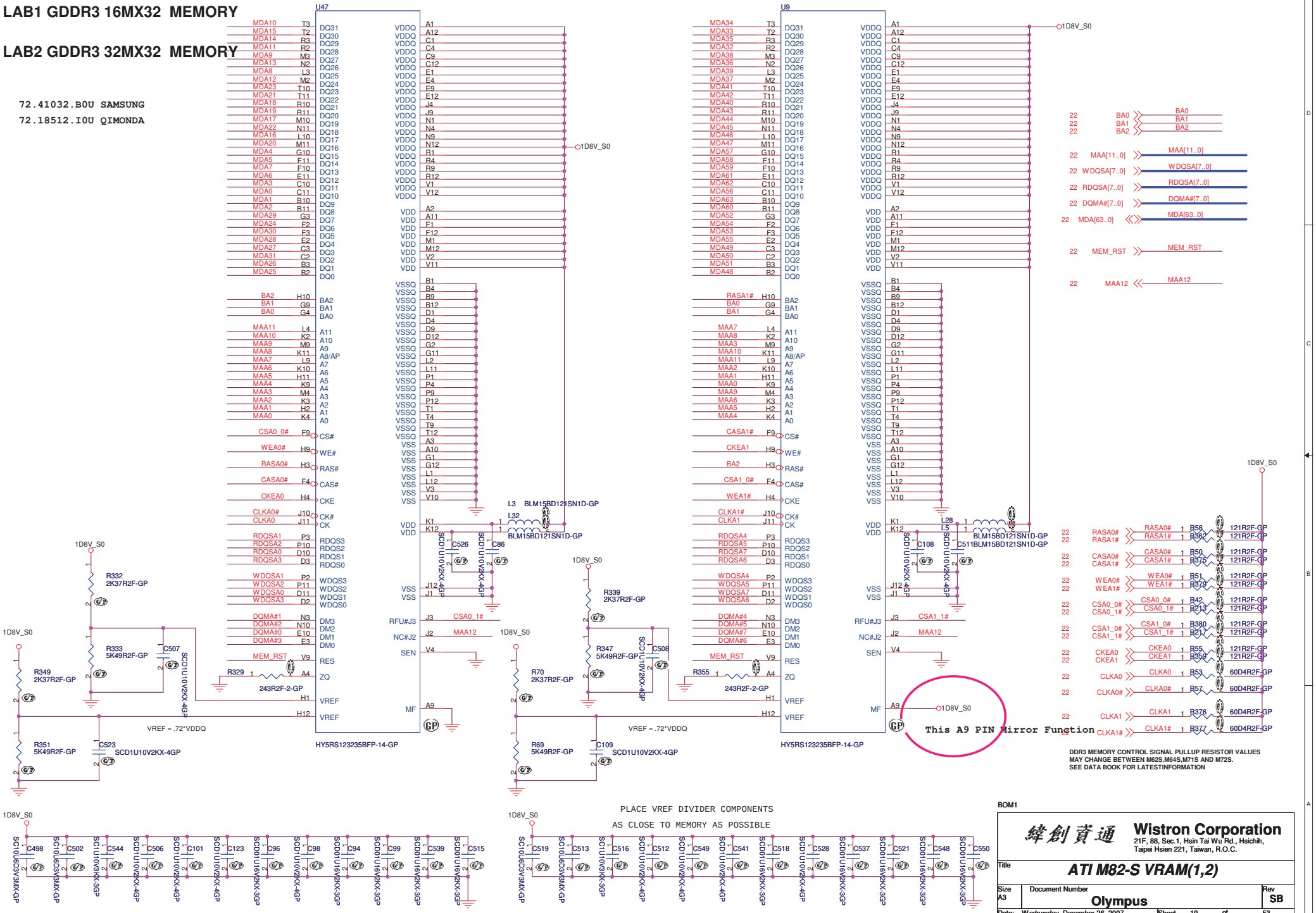
LAB1 GDDR3 16MX32 MEMORY

LAB2 GDDR3 32MX32 MEMORY

72.41032.B0U SAMSUNG
72.18512.I0U QIMONDA



BOM1

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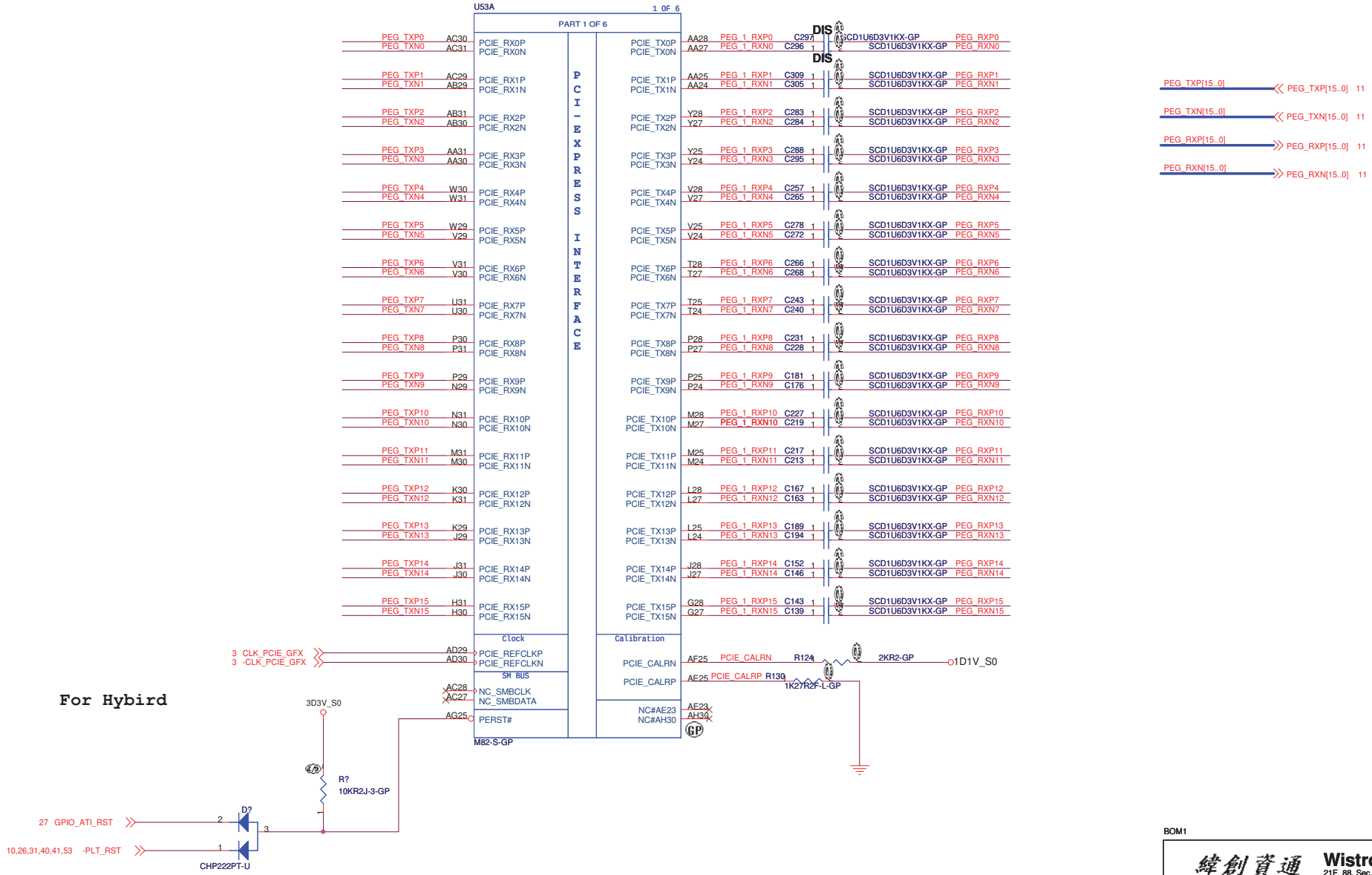
Title: **ATI M82-S VRAM(1,2)**

Size	Document Number	Rev
A3	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 19 of 53



BOM1

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Title	ATI M82-S(1/6):PCIE Interface	
Size A3	Document Number Olympus	Rev SB
Date: Wednesday, December 26, 2007	Sheet 20 of 53	

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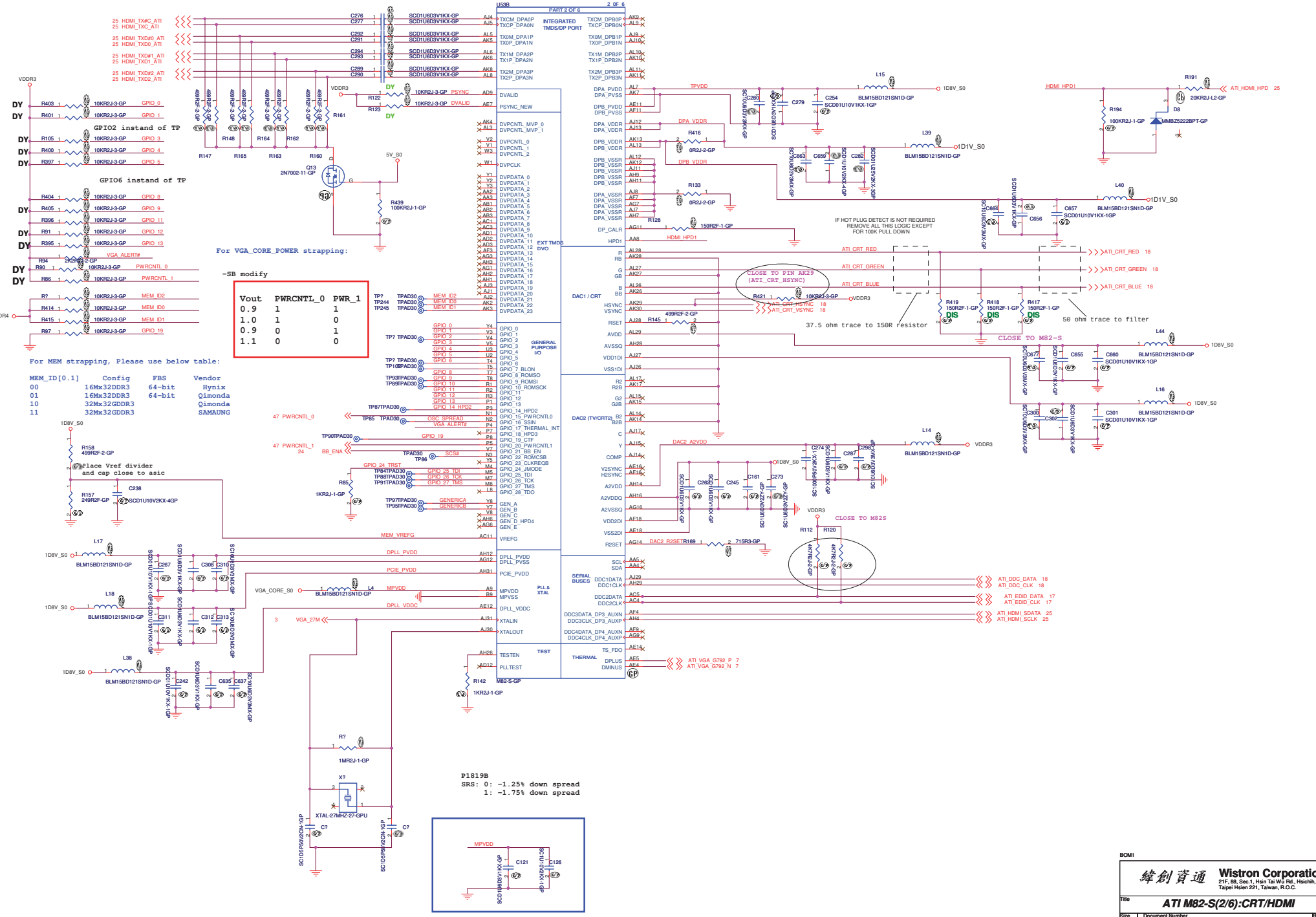


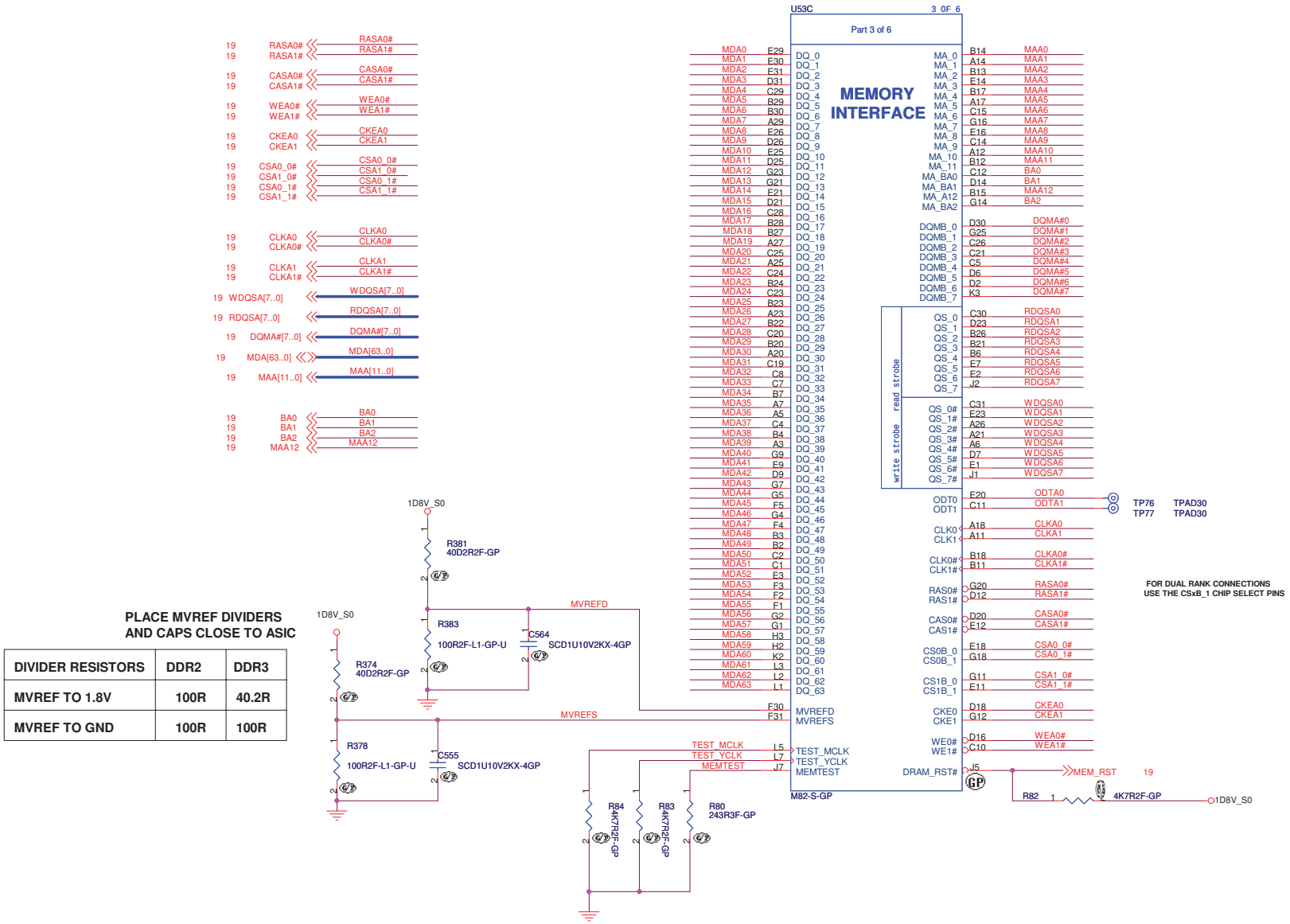
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M82-S(2/6):CRT/HDMI

Size: A2 | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 21 of 53



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

BOM1

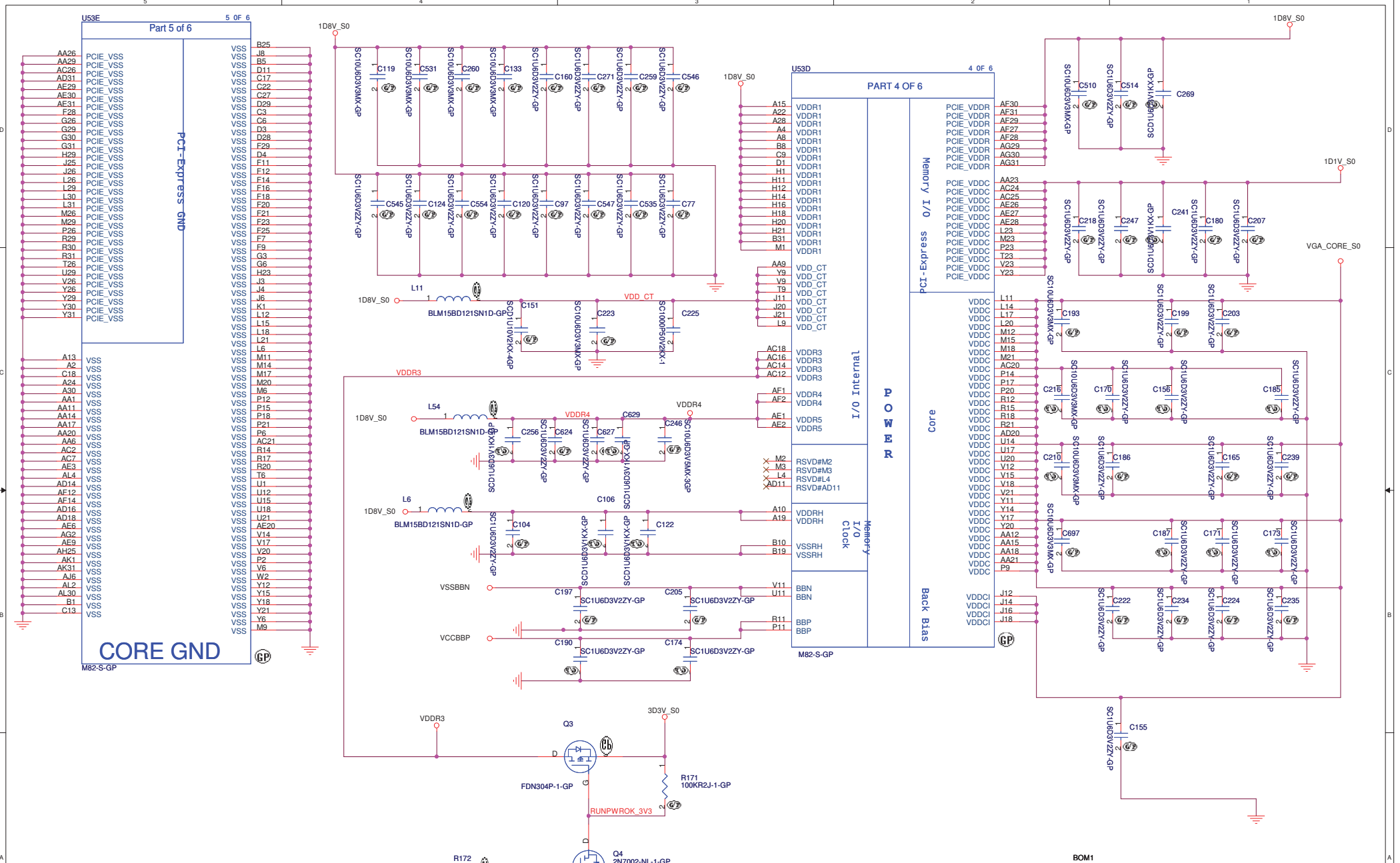
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

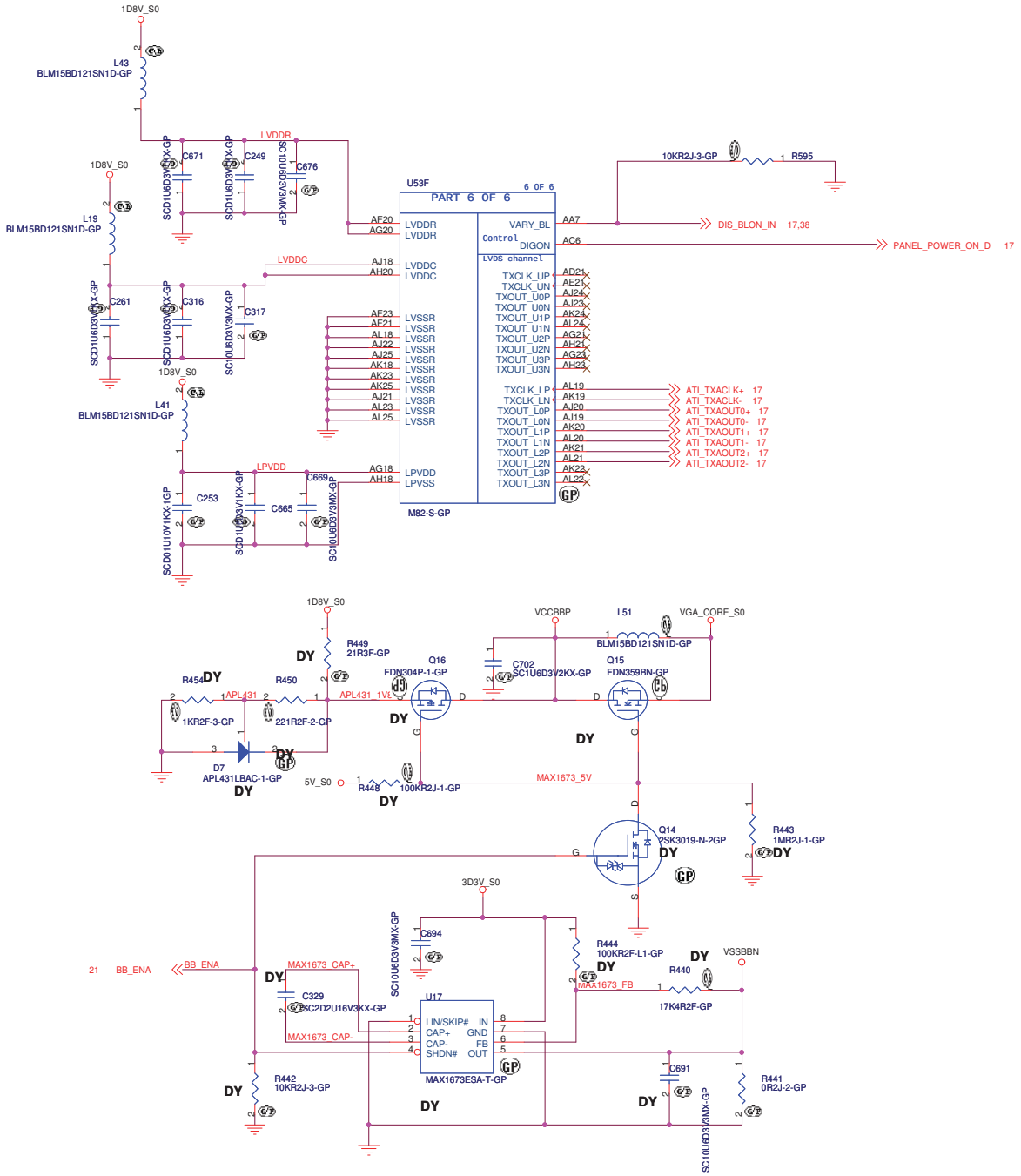
Title: ATI M82-S(3/6):Memory Interface

Size: A3 | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 22 of 53

WWW.AliSaler.Com


U53E
5 OF 6
Part 5 of 6
PCI-Express GND
CORE GND
M82-S-GP
U53D
4 OF 6
PART 4 OF 6
PCI-Express
Memory I/O
I/O Internal
POWER
Core
Back Bias
Memory I/O Clock
M82-S-GP
1D8V_S0
1D1V_S0
VGA_CORE_S0
3D3V_S0
VDD_CT
VDDR3
VDDR4
VSSBBN
VCCBBP
L11
BLM15BD121SN1D-GP
L54
L6
Q3
FDN304P-1-GP
R171
100KR2J-1-GP
RUNPWROK_3V3
Q4
2N7002-NL-1-GP
R172
51KR2-GP
RUNPWROK_1
50 ATI_PROK
C326
SCD1U10V2KX-4GP
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI M82-S(4-5/6):VCC/GND
Size
A3
Document Number
Olympus
Rev
SB
Date: Wednesday, December 26, 2007
Sheet 23 of 53



BOM1

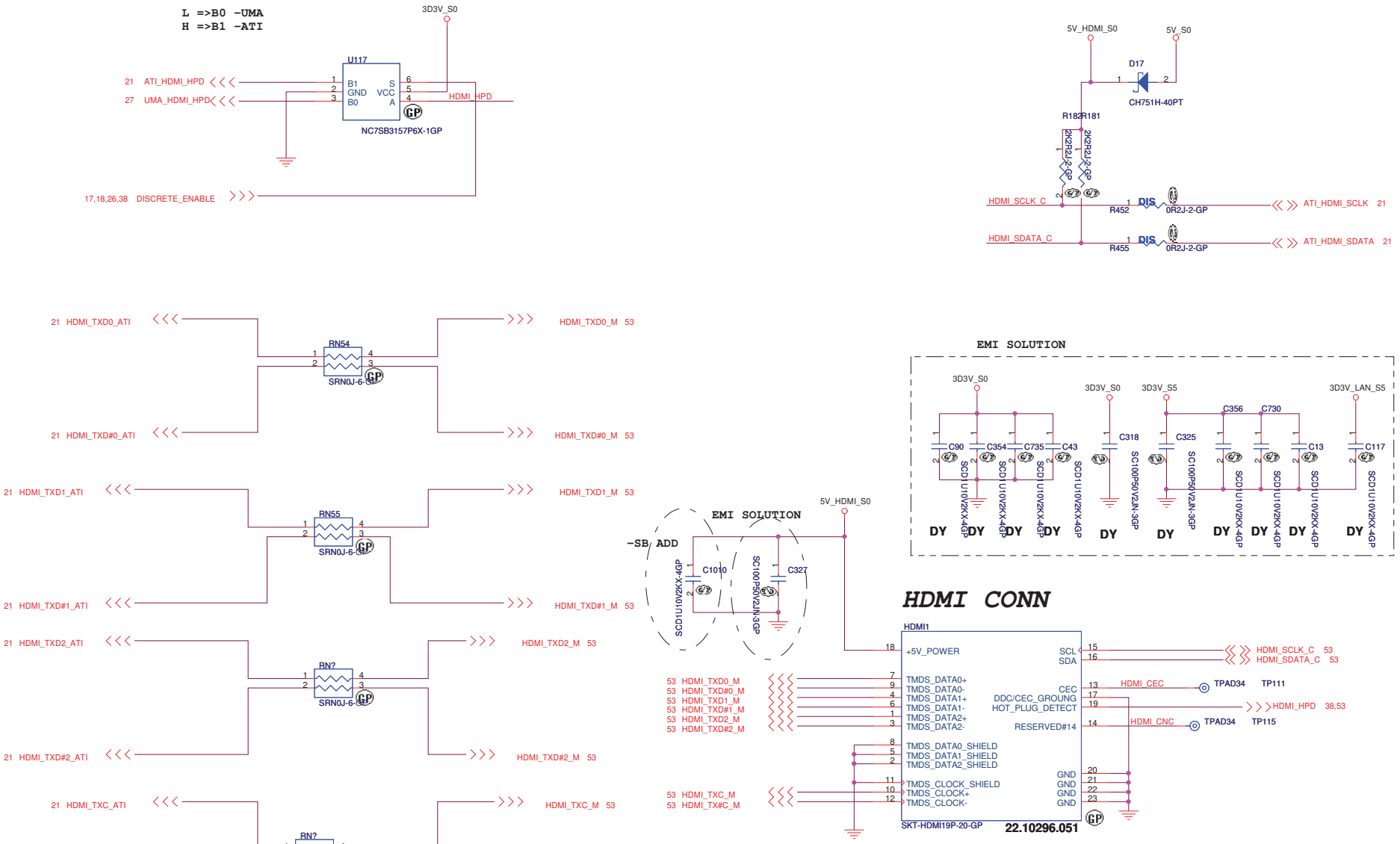
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M82-S(6/6):LVDS**

Size	Document Number	Rev
Custom	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 24 of 53

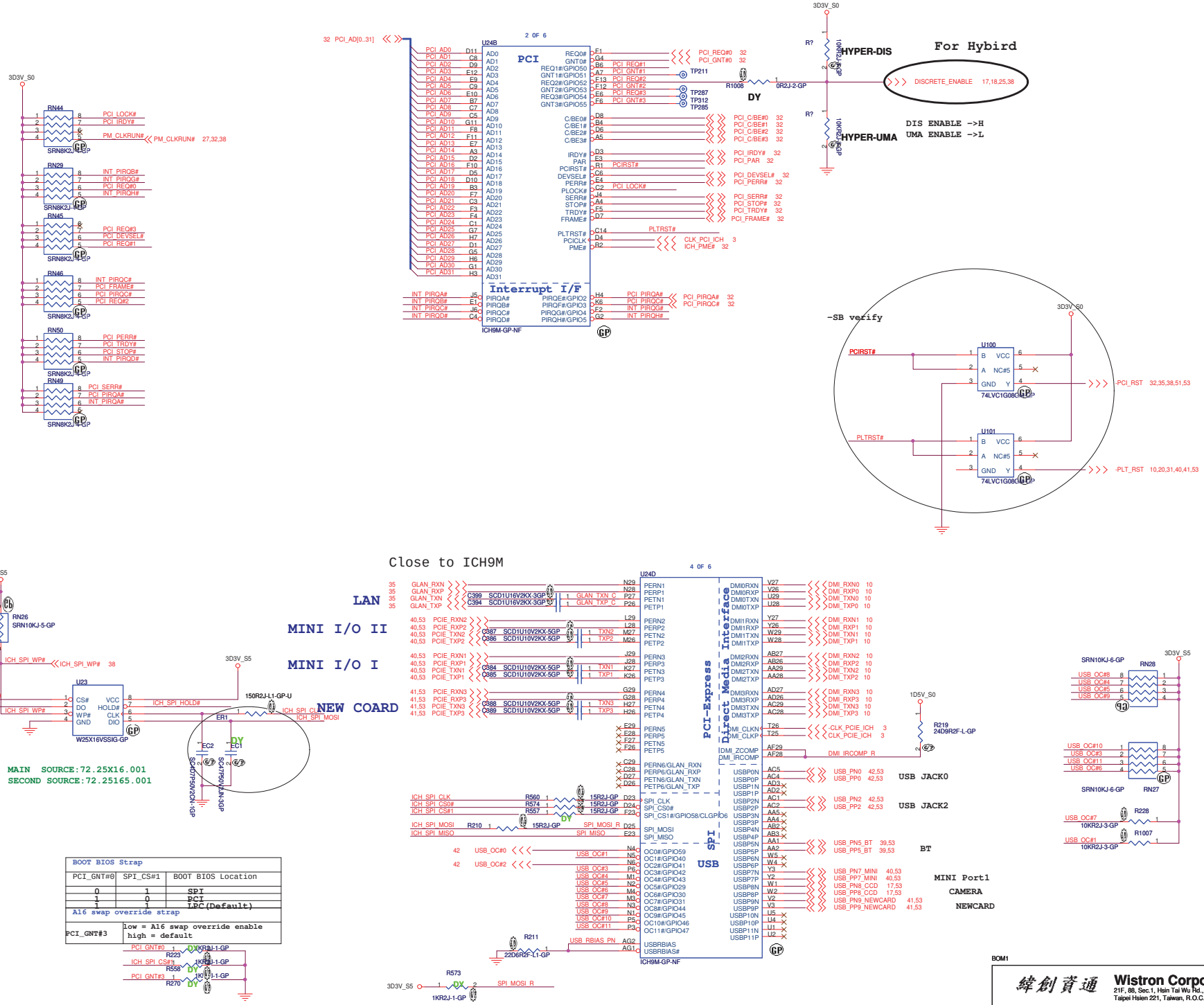
WWW.AliSaler.Com



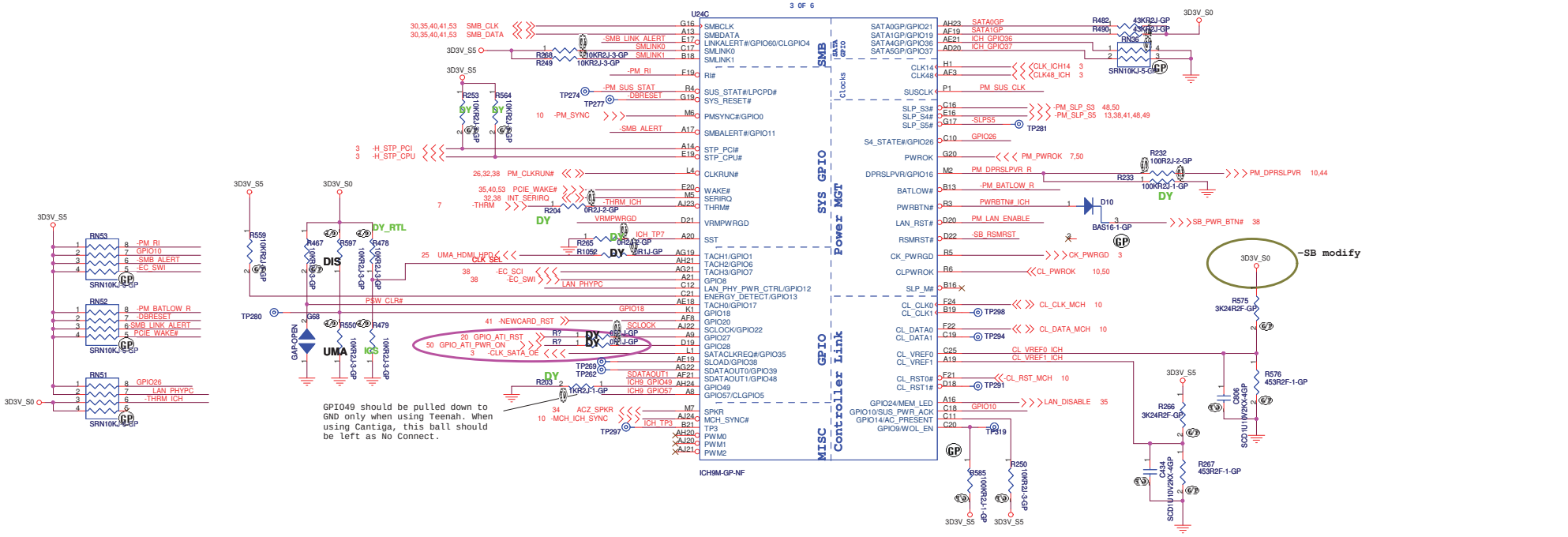
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDMI CONN		
Size A3	Document Number Olympus		Rev SB
Date: Wednesday, December 26, 2007		Sheet 25 of 53	



WWW.AliSaler.Com



No Reboot Strap	
SPKR	LOW = Defaule High=No Reboot

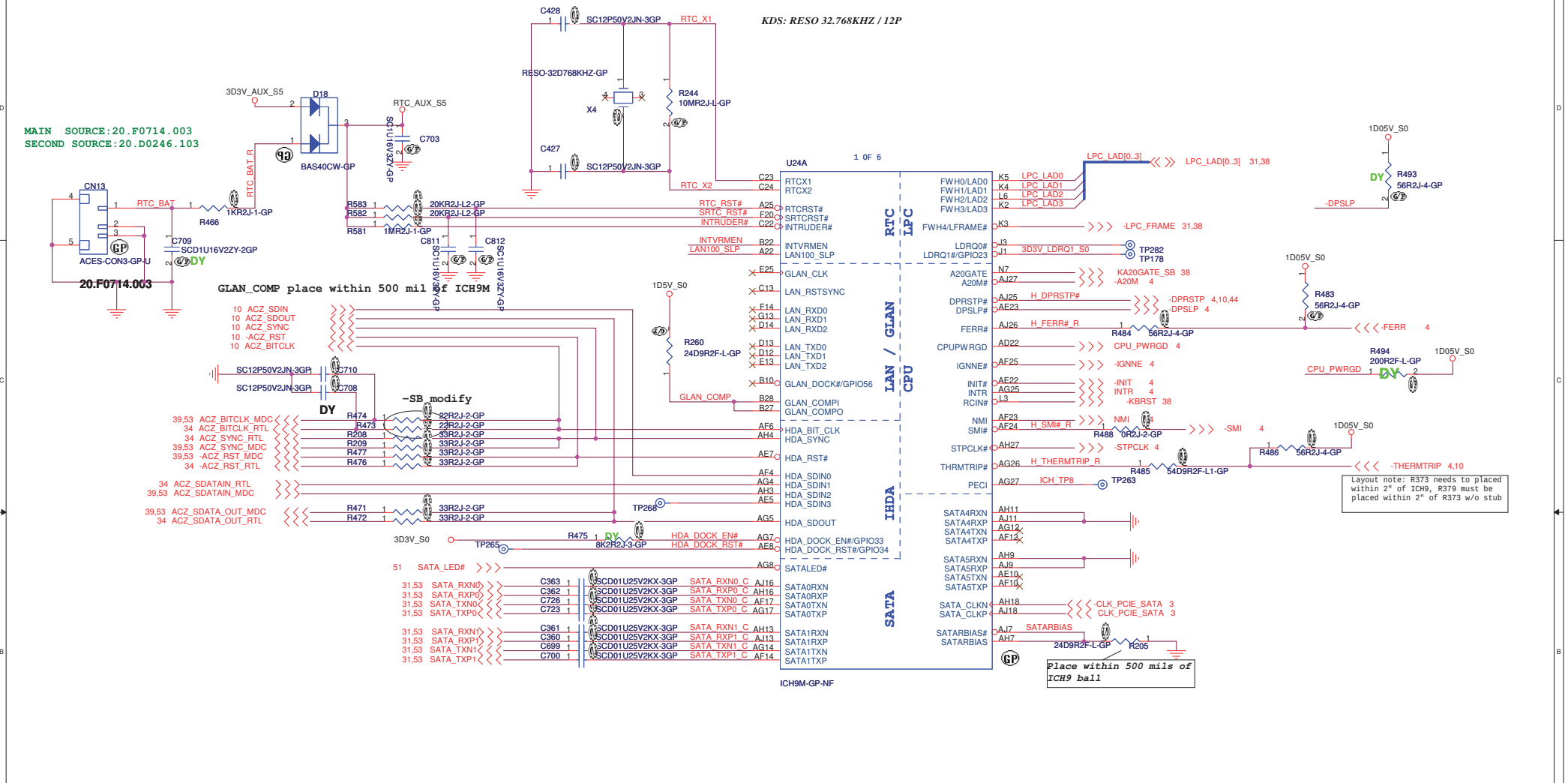
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH9-M (2 of 4)*

Size | Document Number: **Olympus** | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 27 of 53



integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

BOM1

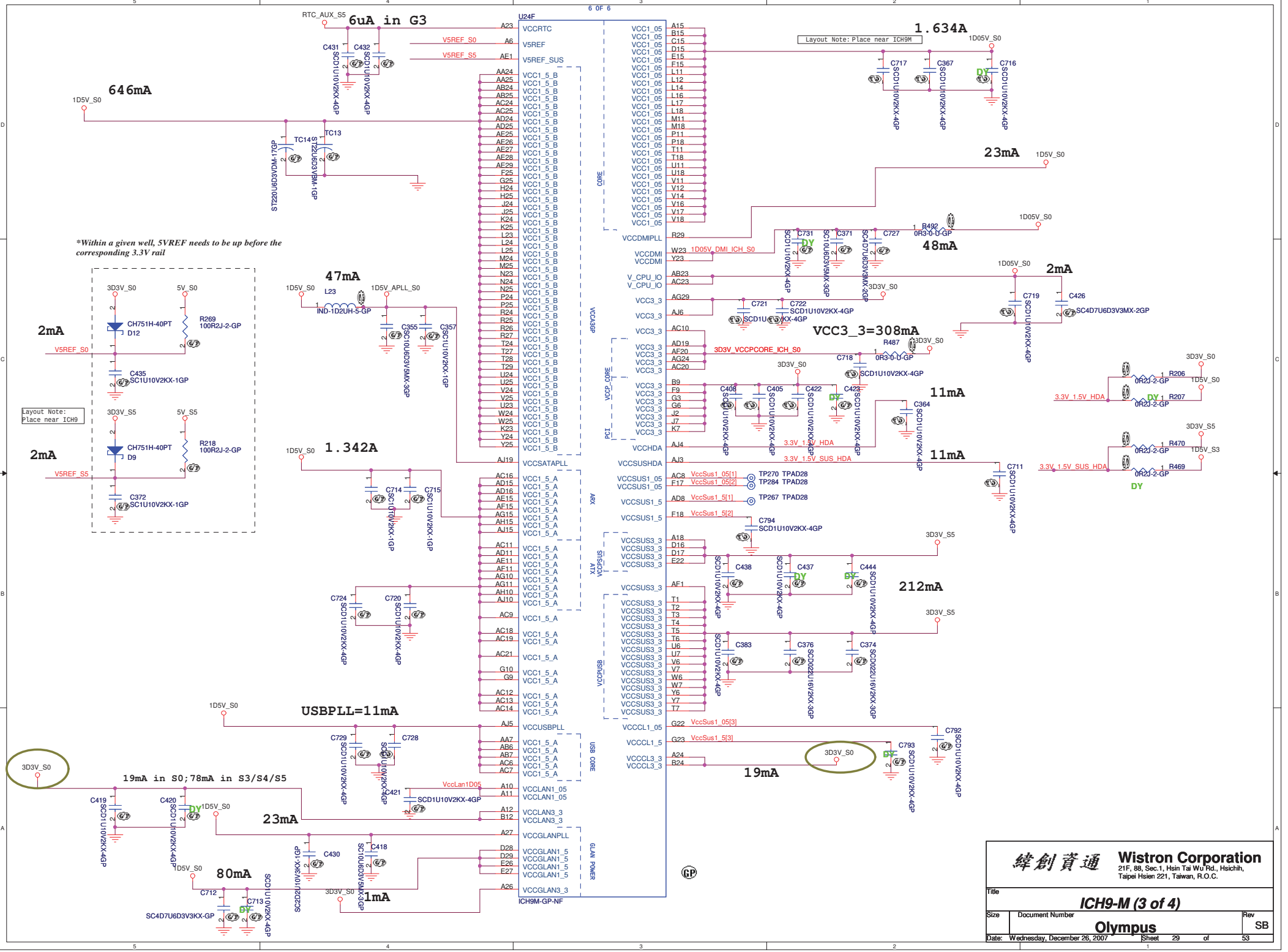
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

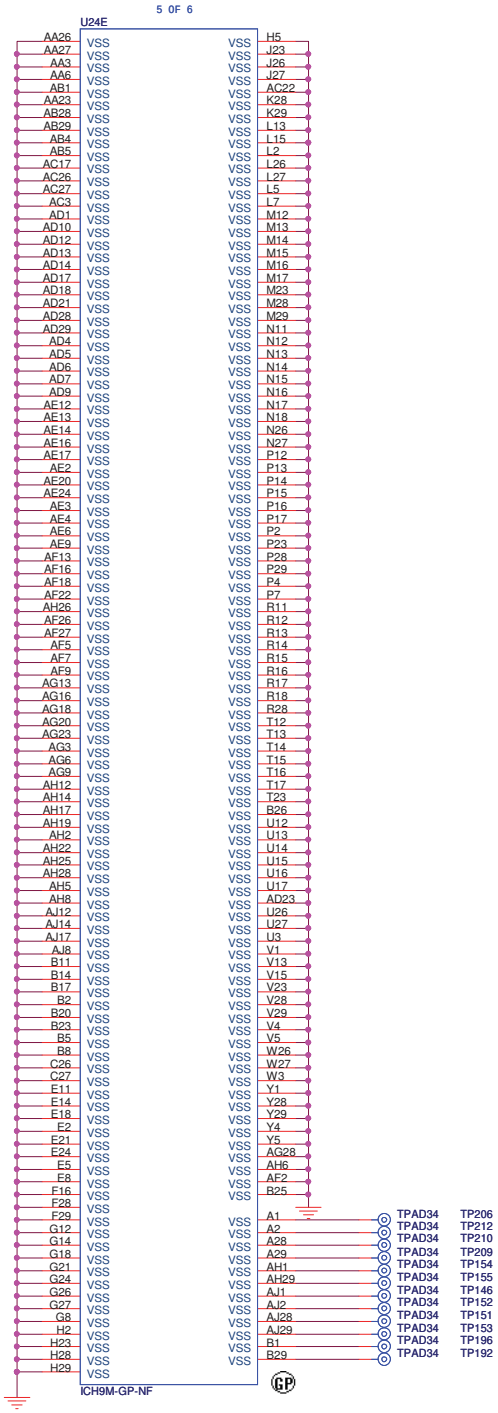
Title: **ICH9-M (1 of 4)**

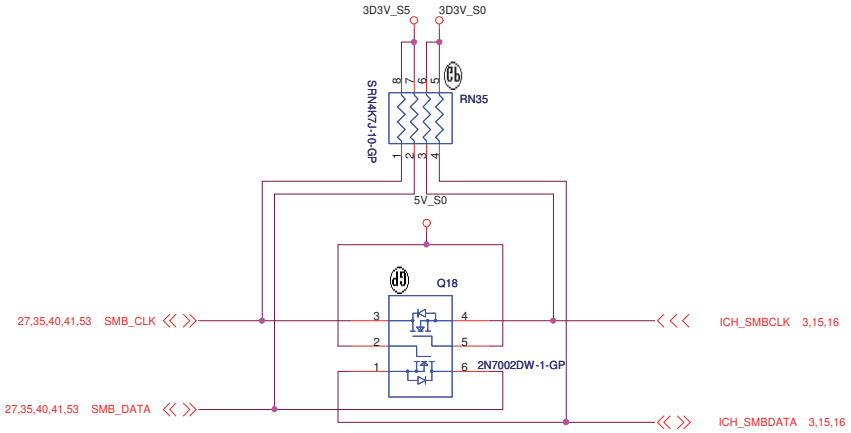
Size | Document Number: **Olympus** | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 28 of 53

WWW.AliSaler.Com


6 OF 6
U24F
ICH9M-GP-NF
6uA in G3
646mA
1.634A
23mA
48mA
2mA
47mA
VCC3_3=308mA
11mA
1.342A
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH9M
Layout Note: Place near ICH9
VCCRTC
V5REF
V5REF_SUS
VCCDMIPLL
VCCDMI
V_CPU_IO
VCC3_3
VCCHDA
VCCSATAPLL
VCCSUSHDA
VCCSUS1_05
VCCSUS1_5
VCCSUS3_3
VCCCL1_05
VCCCL1_5
VCCCL3_3
VCCUSBPLL
VCCLAN1_05
VCCLAN3_3
VCCGLANPLL
VCCGLAN1_5
VCCGLAN3_3
VCC1_5_B
VCC1_5_A
VCC1_5_A
VCC1_5_A





Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***ICH9-M (4 of 4)***	
Size	Document Number **Olympus**	Rev SB
Date: Wednesday, December 26, 2007	Sheet 30 of 53	

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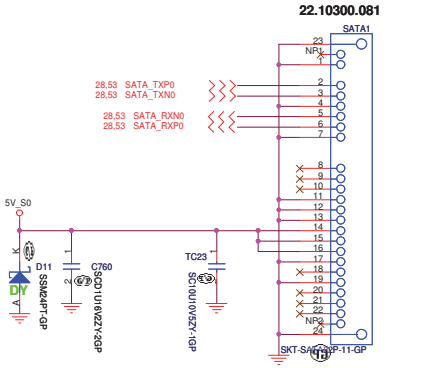
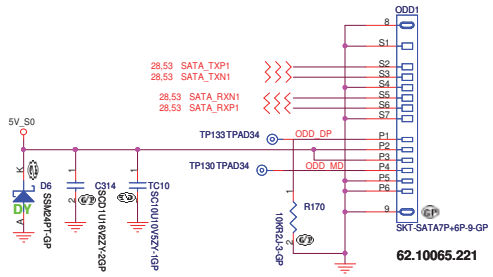
SATA HD Connector



MAIN SOURCE:22.10300.081
SECOND SOURCE:20.80919.022

ODD Connector



Olympus LED's Location and Sequence

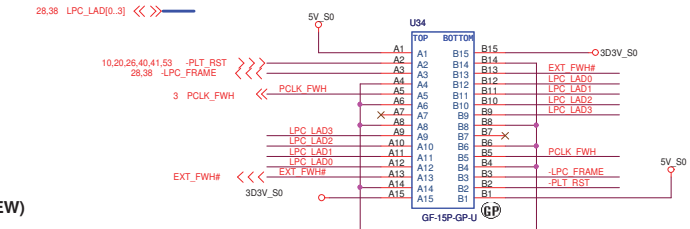
Left side				Right side
TouchPad-MUTE	POWER	Battery	WLAN	
LED1	LED3 LED8	LED4 LED5	LED6 LED7	

TOP VIEW

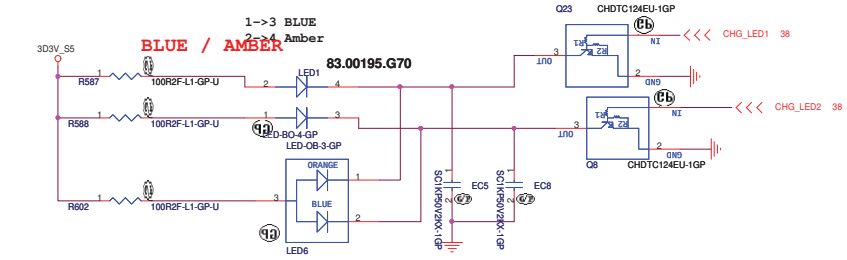
A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

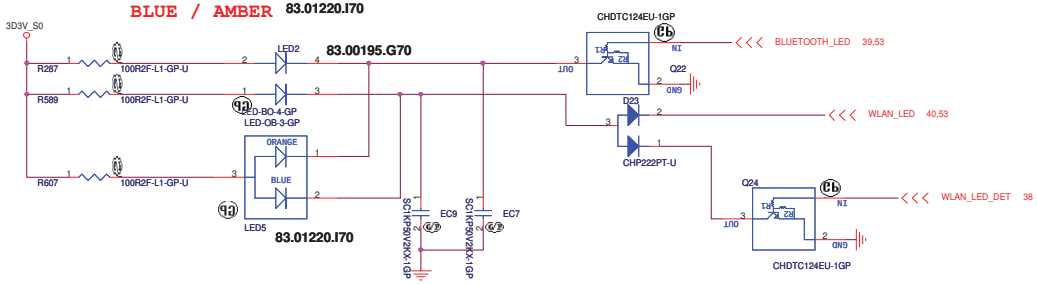
(BOTTOM VIEW)

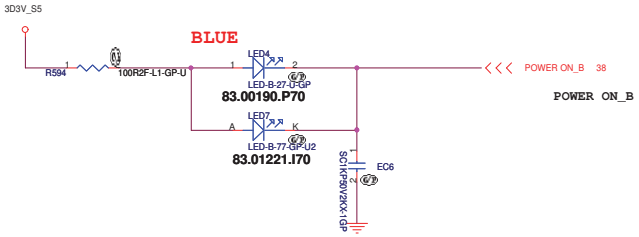
GOLDEN FINGER FOR DEBUG BOARD

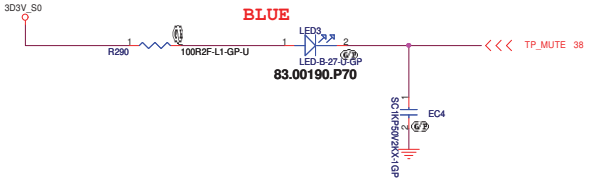


Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



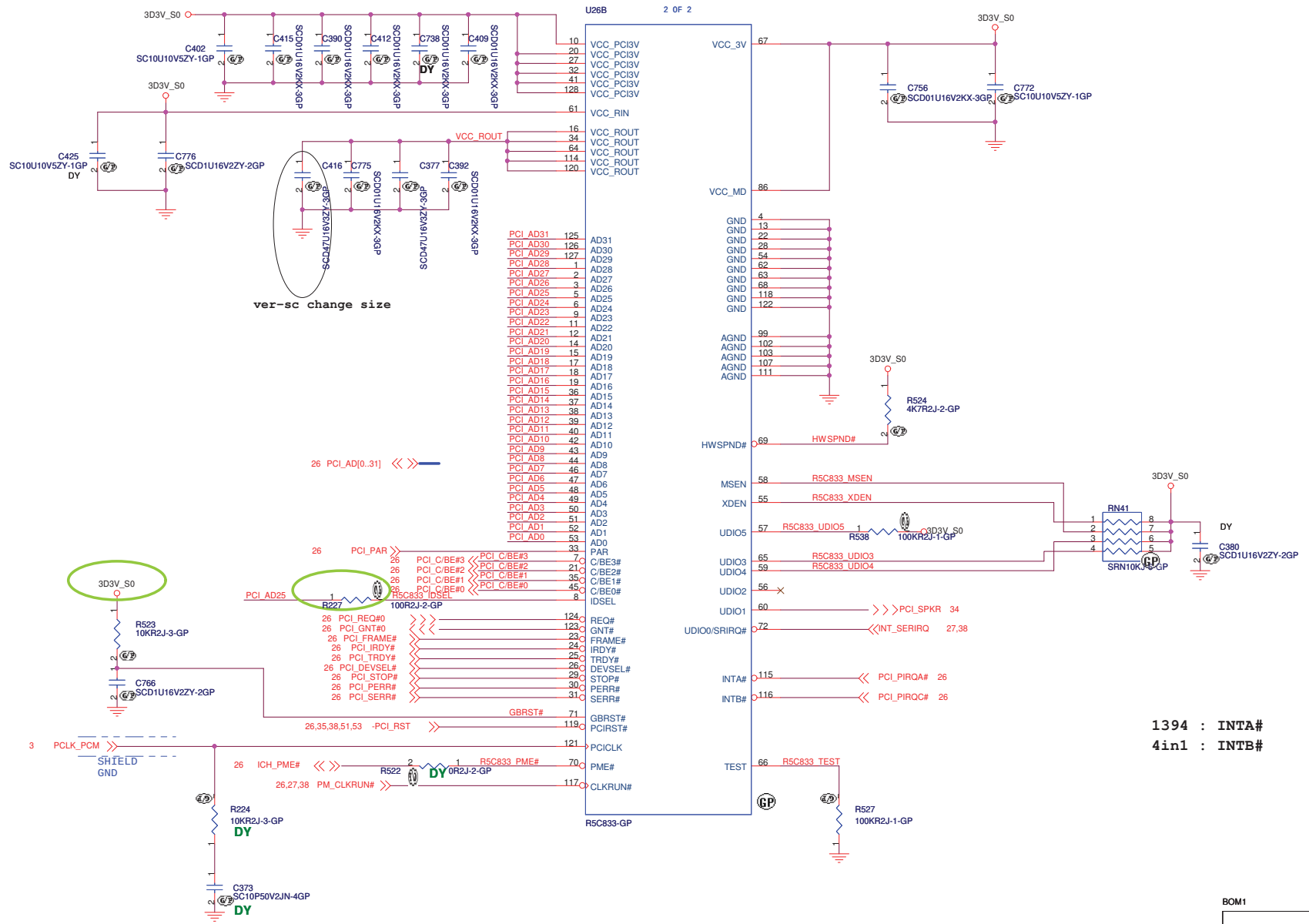






BOM1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD/CDROM/DEBUG / LEDS	
Size	Document Number: Olympus	Rev: SB
Date: Wednesday, December 26, 2007	Sheet 31 of 53	



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: R5C832/PCI		
Size: A3	Document Number: Olympus	Rev: SB
Date: Wednesday, December 26, 2007	Sheet 32 of 53	

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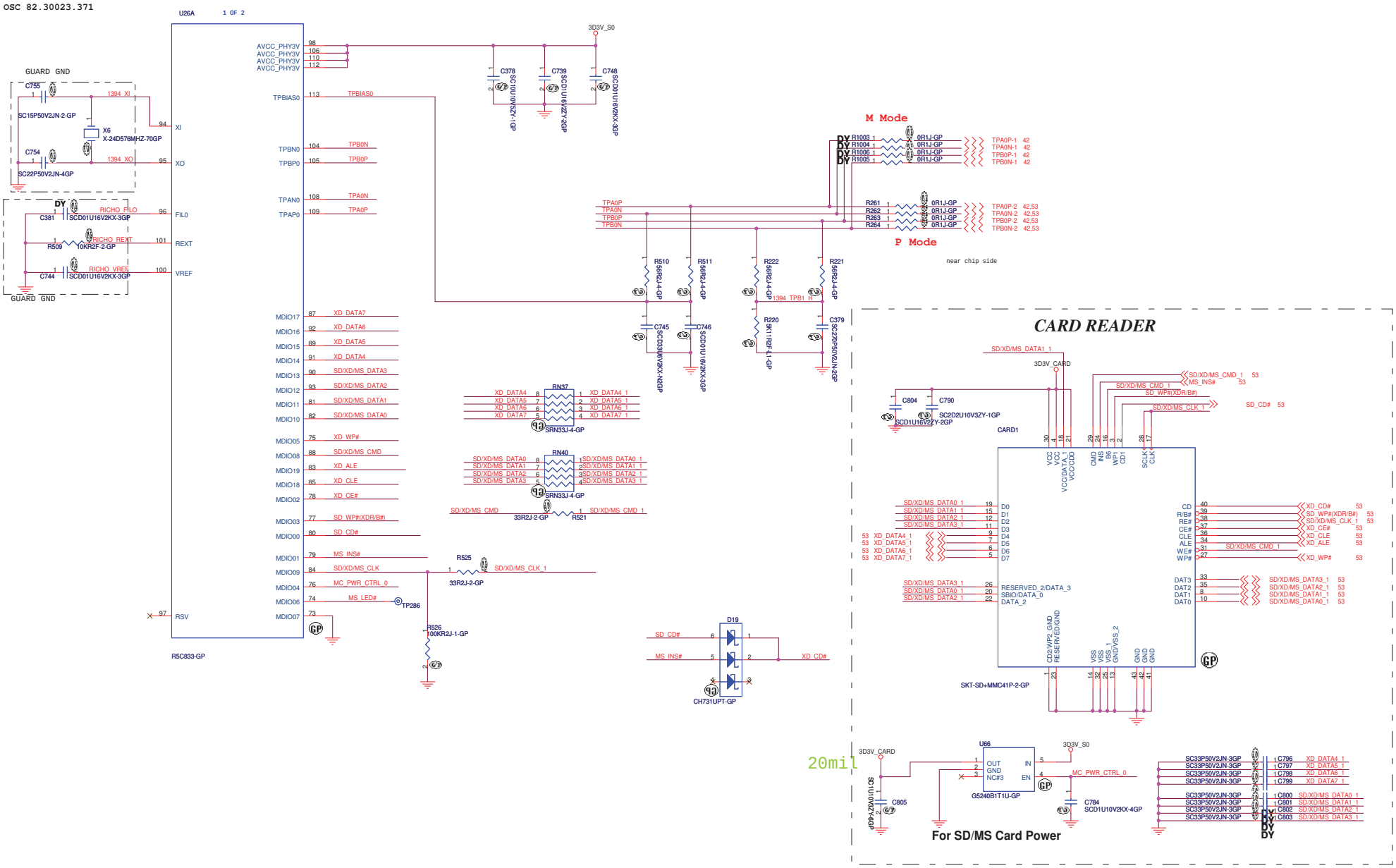


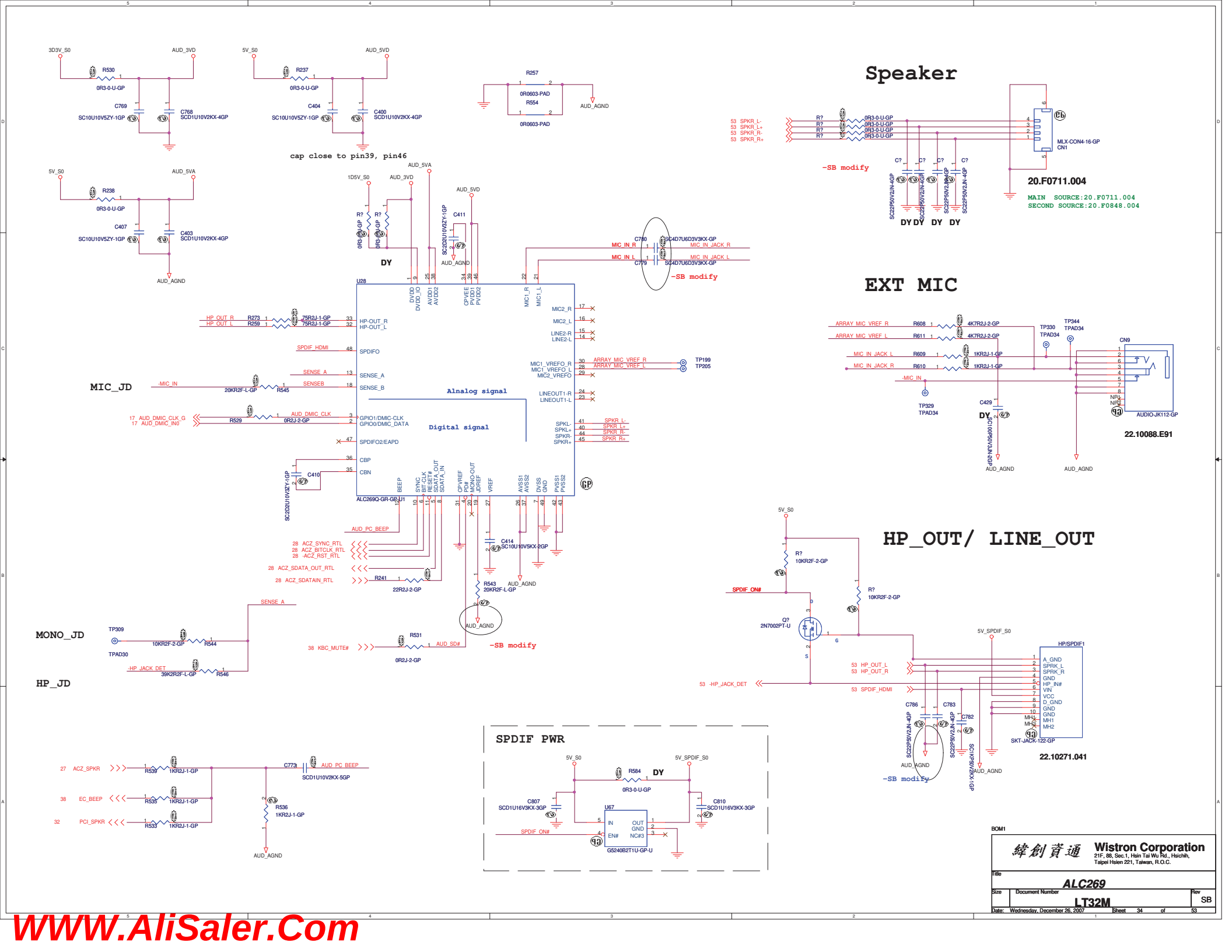
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

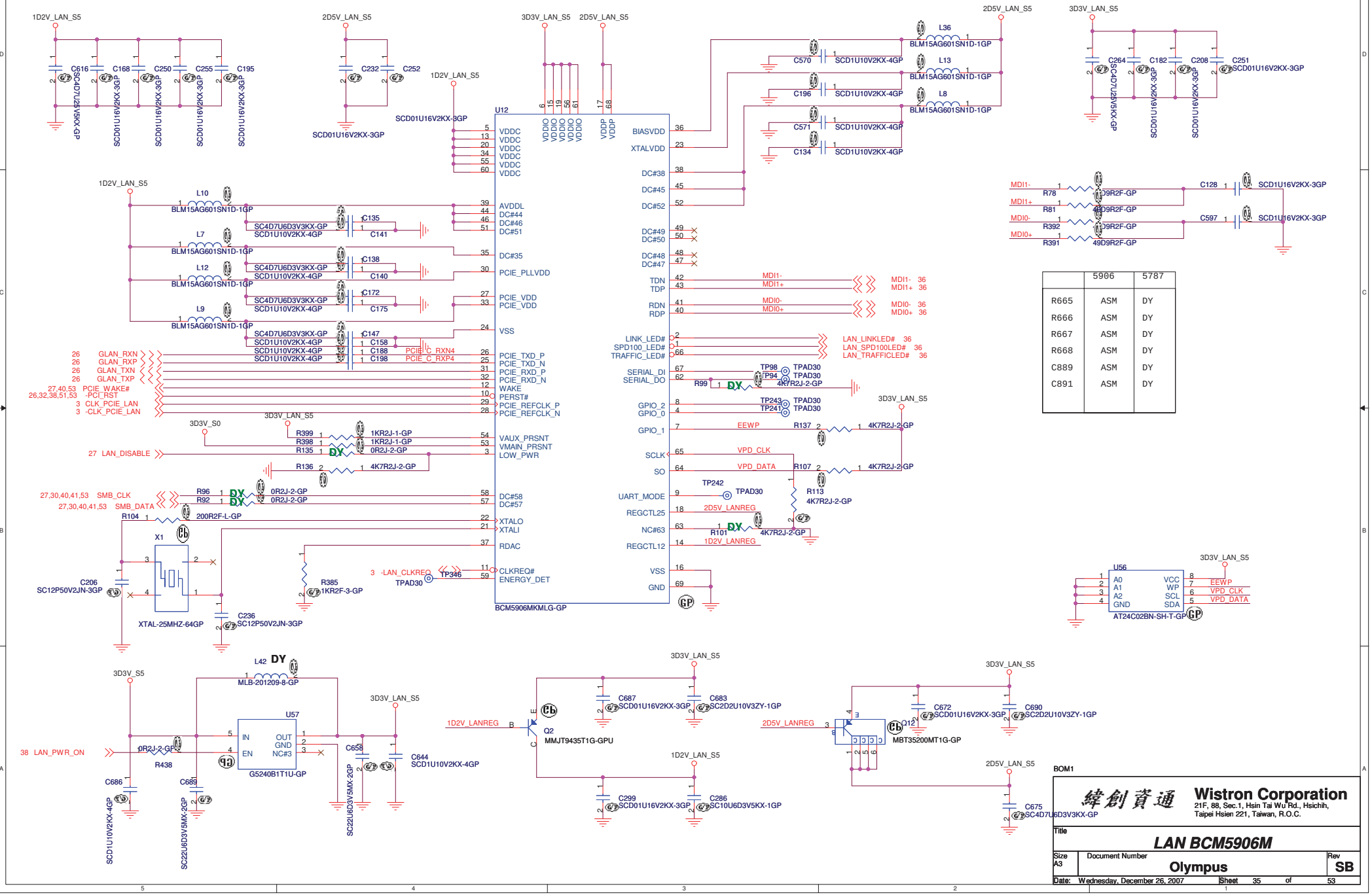
Title: R5C832/IEEE1394/SD/BT

Size: C | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 33 of 53



WWW.AliSaler.Com



	5906	5787
R665	ASM	DY
R666	ASM	DY
R667	ASM	DY
R668	ASM	DY
C889	ASM	DY
C891	ASM	DY

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

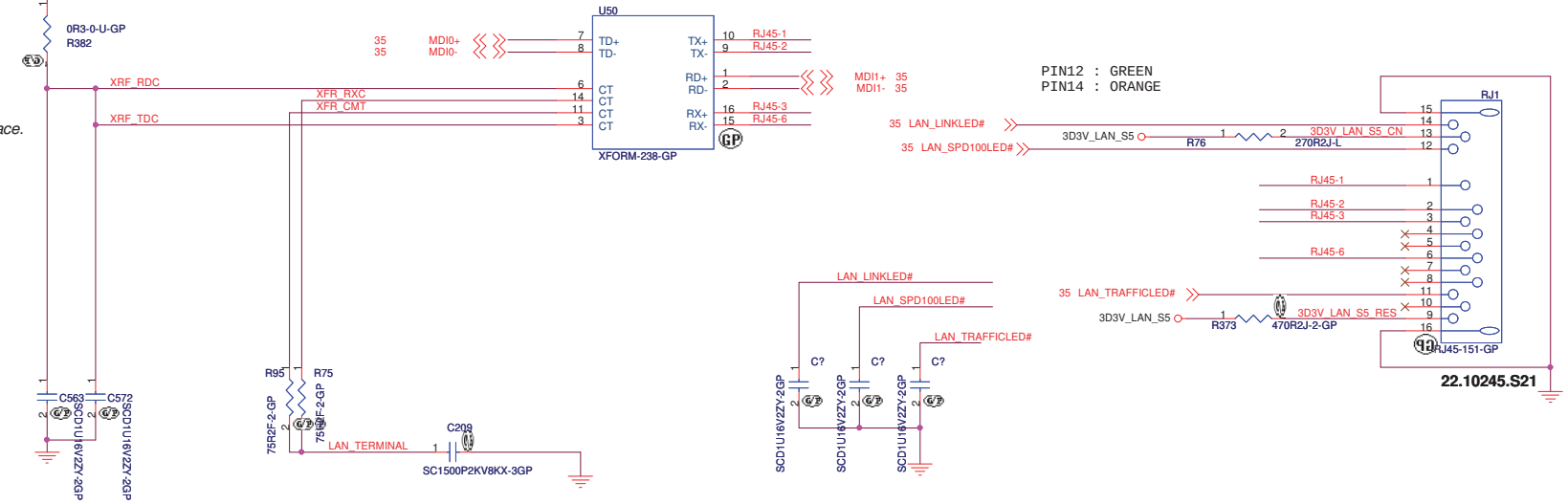
Title: **LAN BCM5906M**

Size: A3 | Document Number: **Olympus** | Rev: **SB**

Date: Wednesday, December 26, 2007 | Sheet 35 of 53

10/100M Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LAN connector/NEW CARD/SIM**	
Size A3	Document Number **Olympus**	Rev **SB**
Date: Wednesday, December 26, 2007	Sheet 36 of 53	

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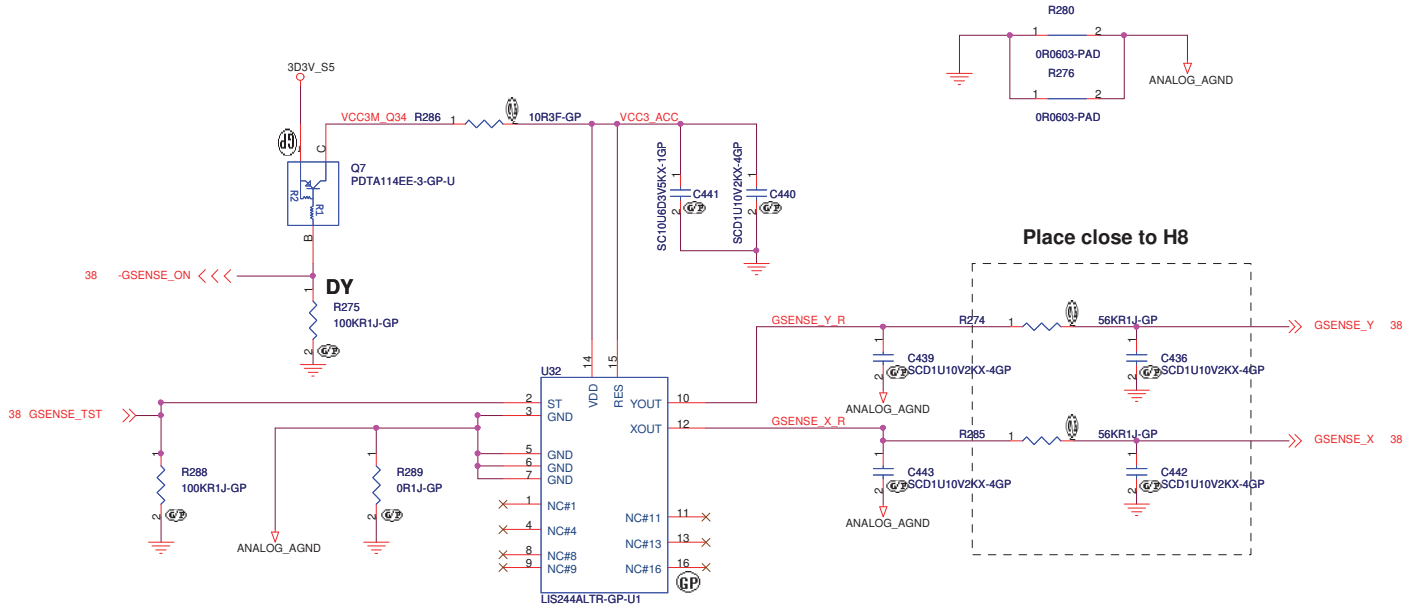


Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil for three Output traces

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C148, C149, Q18, R116, R121, C126, C130, R107, R106 close to U18.

(2) Avoid routing under DCDC switching area.

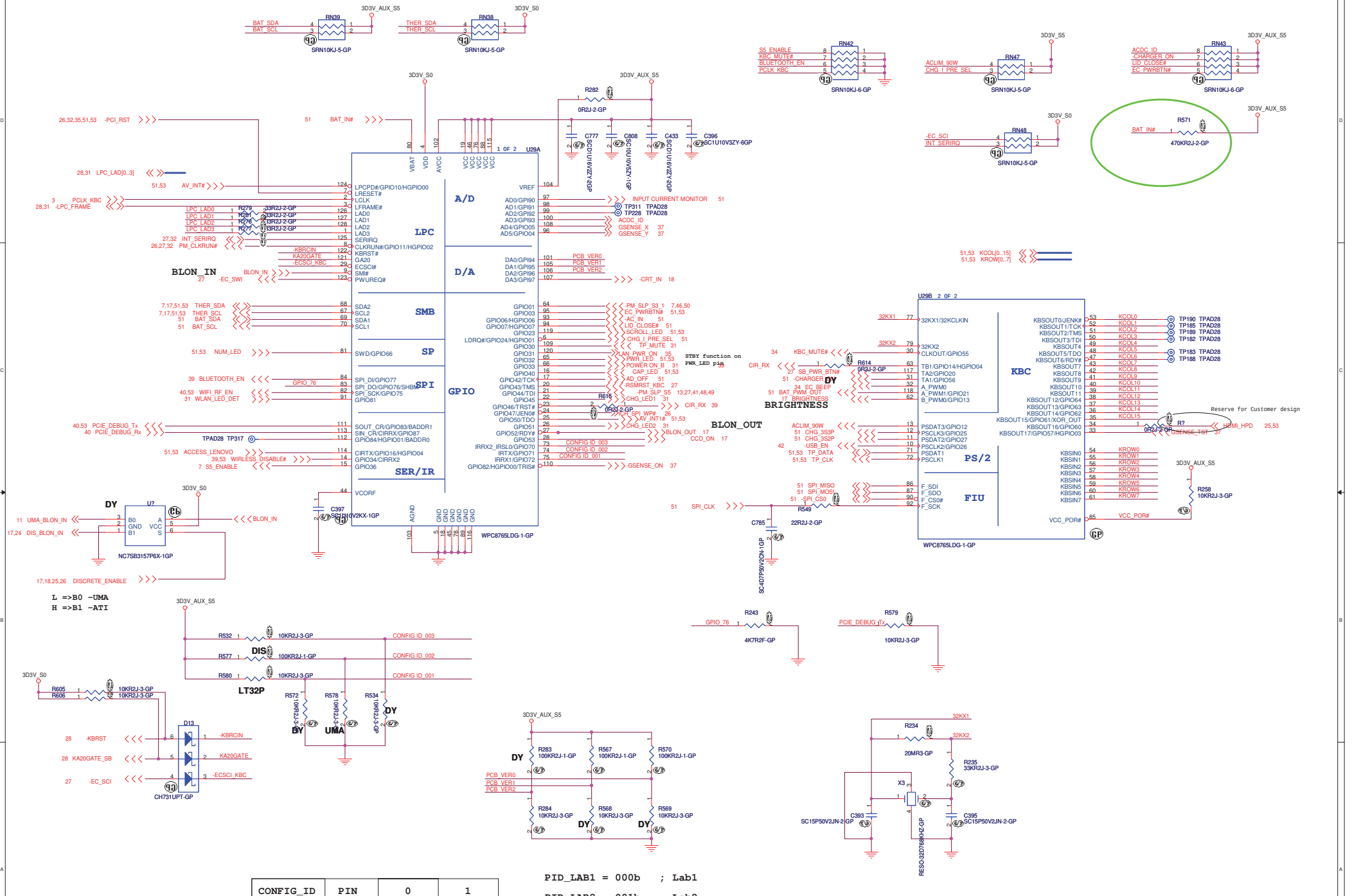
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G-SENSOR

Size: A3 | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 37 of 53



CONFIG_ID	PIN	0	1
001	GPIO34	LT32M(DDR2)	LT32P(DDR3)
002	GPIO55	UMA	DIS
003	GPIO70		OLympus

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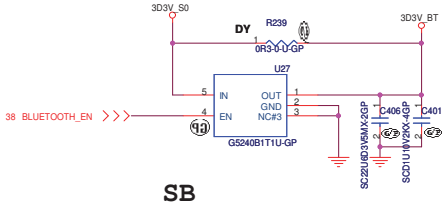
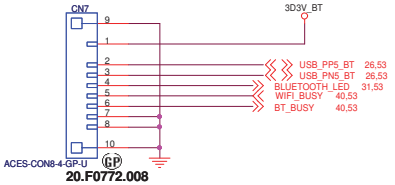


SB

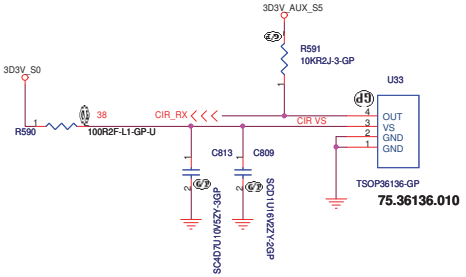
BT CONNECTOR



20.F0772.008

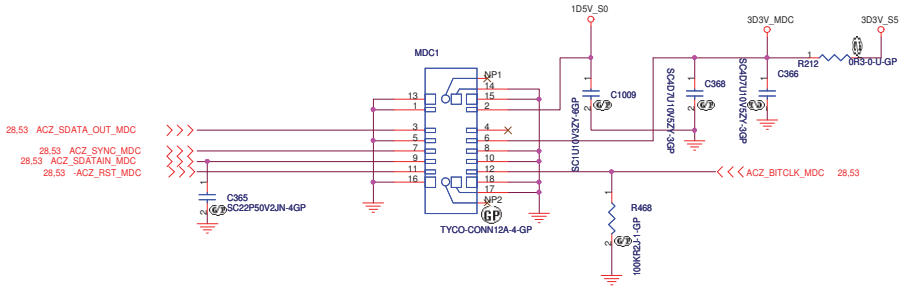
MAIN SOURCE:20.F0772.008
SECOND SOURCE:20.F0983.008

CIR



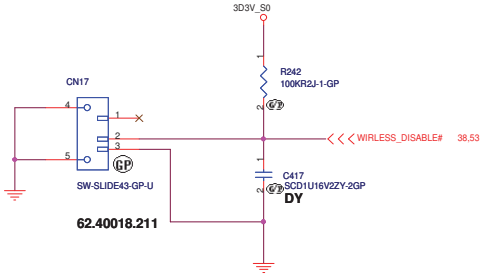
75.36136.010

MDC 1.5 CONN



MAIN SOURCE:20.F0677.012
SECOND SOURCE:20.F0676.012

WIRELESS SWITCH



62.40018.211

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Module_Blue Tooth/Modem/CIR*

Size	Document Number	Rev
	Olympus	SB

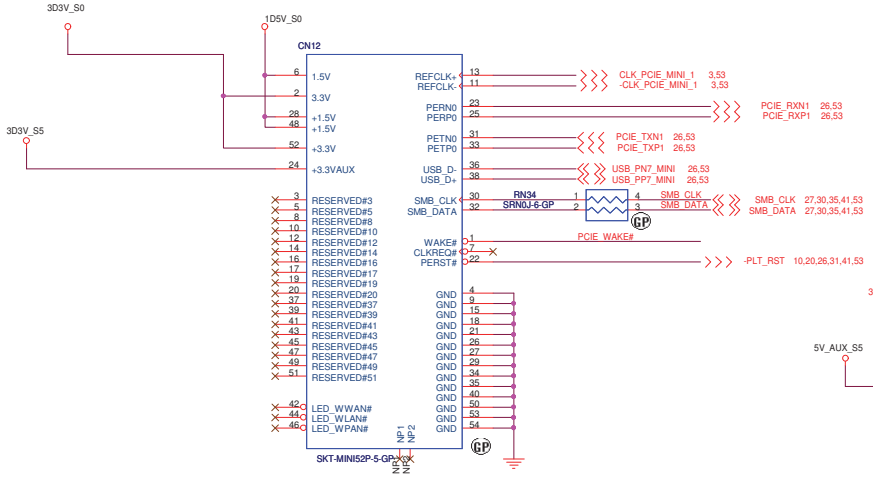
Date: Wednesday, December 26, 2007 Sheet 39 of 53

Mini PCI-E Connector

Only port-1 support USB

For Robson

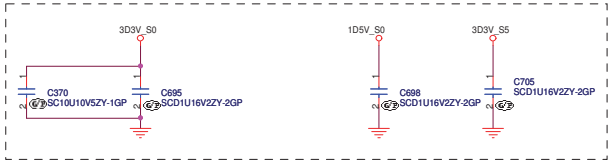
Port-1 High



20.F0832.052

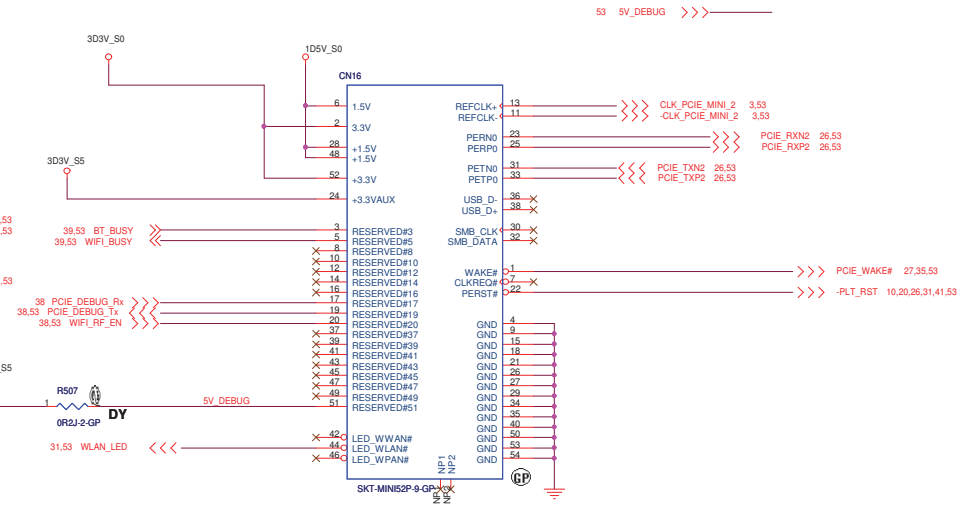
MAIN SOURCE:20.F0832.052

SECOND SOURCE:20.F1107.052



Mini PCI-E Connector

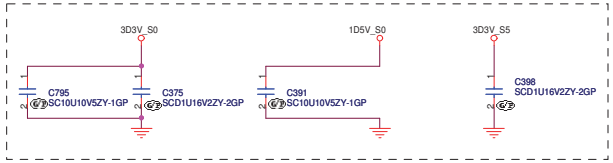
Port-2 low



62.10043.411

MAIN SOURCE:62.10043.411

SECOND SOURCE:20.F1084.052



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD CONN .**

Size: C | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 40 of 53

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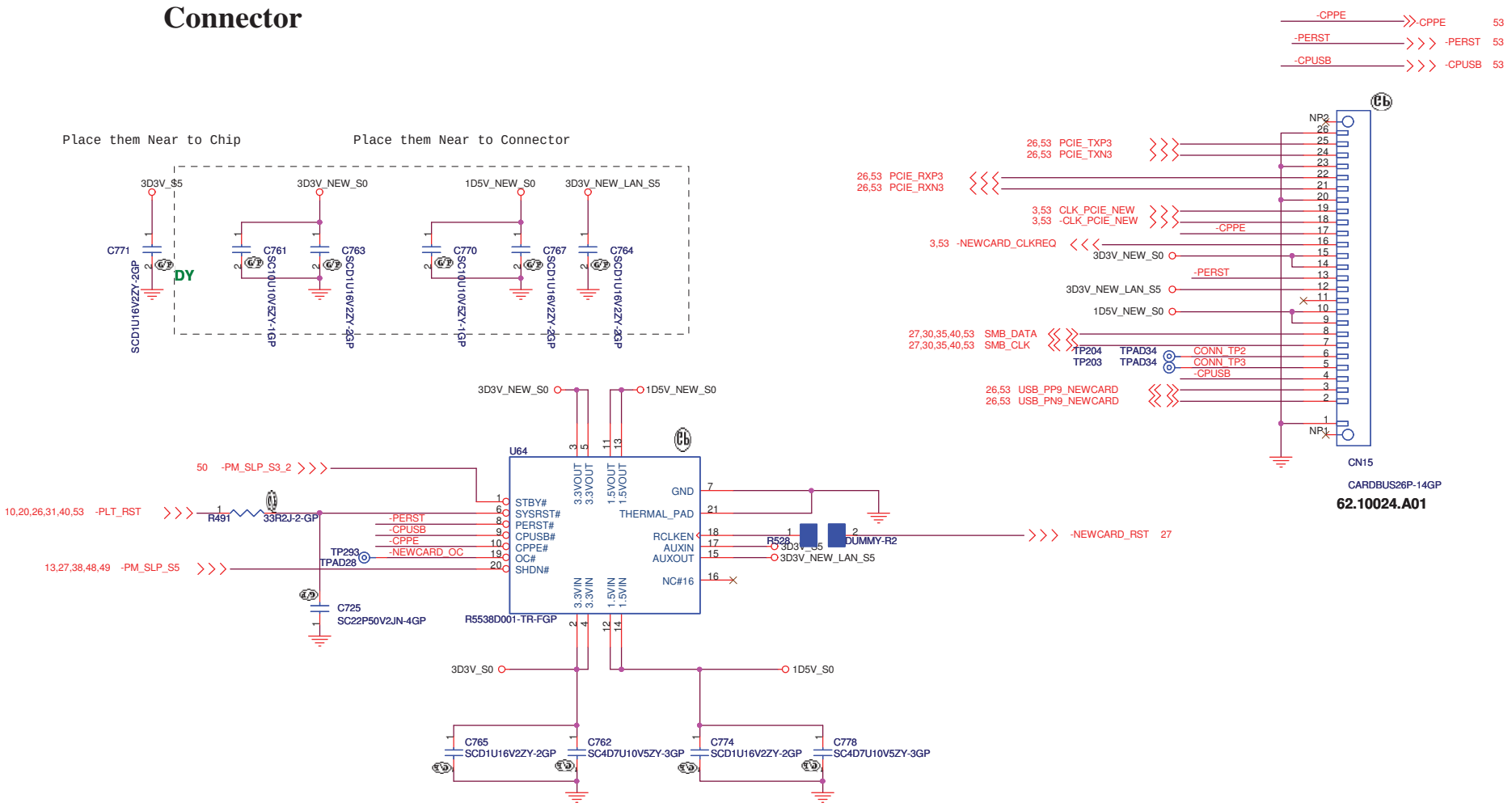
NEWCARD
Connector



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

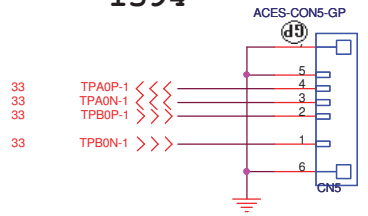
Title		
	Module NewCard	
Size	Document Number	Rev
	Olympus	SB

Date: Wednesday, December 26, 2007 Sheet 41 of 53

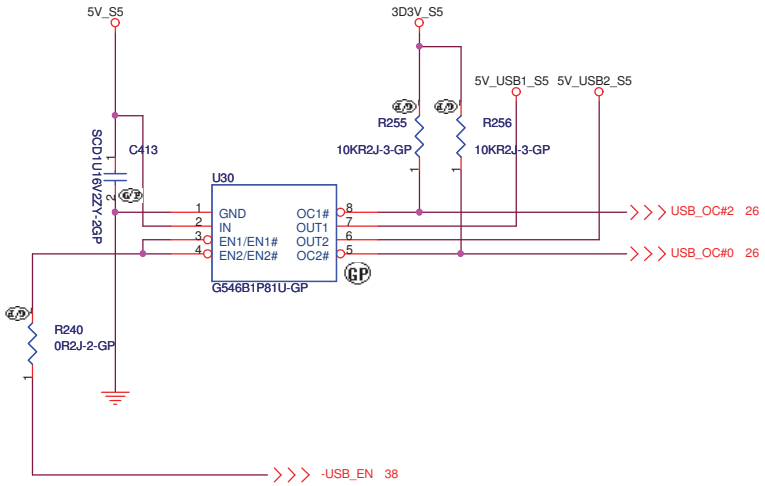
USB * 2 PORT

Low -End USB BOARD

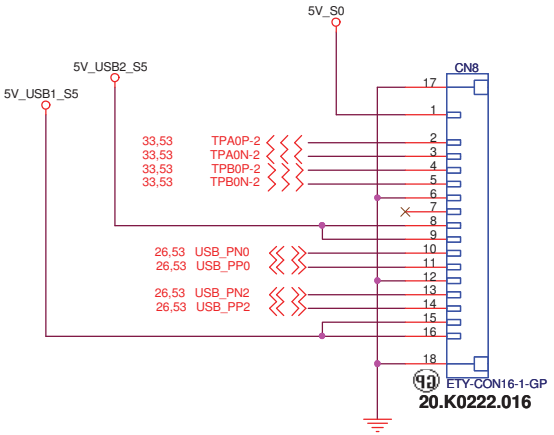
1394



MAIN SOURCE:20.k0196.005
SECOND SOURCE:20.K0212.008



USB*2 + 1394



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB I/O & 1394 CNN	
Size B	Document Number Olympus	Rev SB
Date: Wednesday, December 26, 2007	Sheet 42 of 53	

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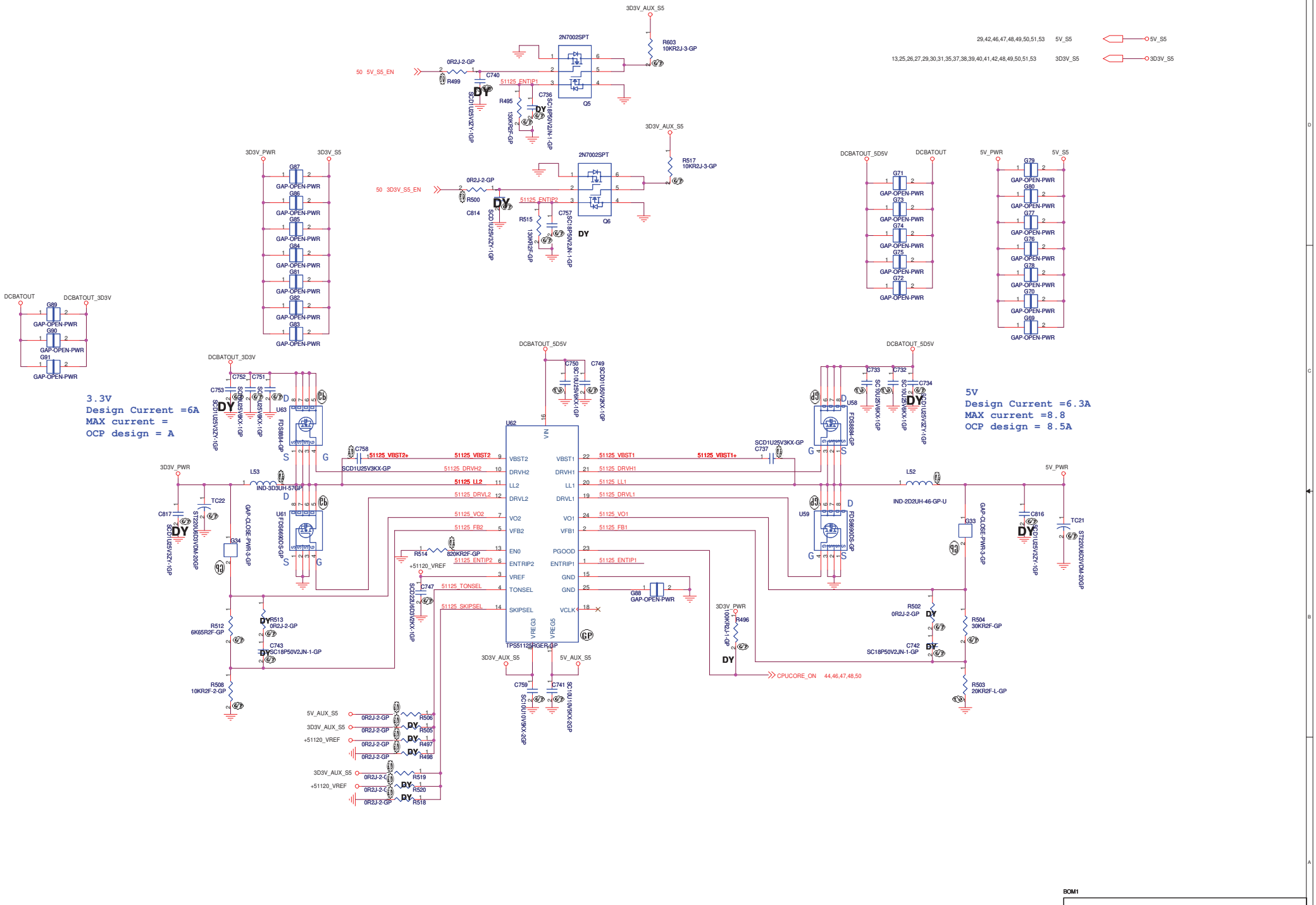
3.3V
Design Current =6A
MAX current =
OCP design = A
5V
Design Current =6.3A
MAX current =8.8
OCP design = 8.5A
TPS51125RGER-GP
U62
Q5
Q6
U61
U58
U59
U63
3D3V_AUX_S5
3D3V_PWR
5V_PWR
5V_S5
DCBATOUT_5D5V
DCBATOUT_3D3V
DCBATOUT
51125_VBST2
51125_VBST1
51125_DRVH2
51125_DRVH1
51125_LL2
51125_LL1
51125_DRVL2
51125_DRVL1
51125_VO2
51125_VO1
51125_FB2
51125_FB1
51125_ENTIP2
51125_ENTIP1
51125_TONSEL
51125_SKIPSEL
CPUCORE_ON
+51120_VREF
5V_AUX_S5
3D3V_AUX_S5
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Olympus
Date: Wednesday, December 26, 2007
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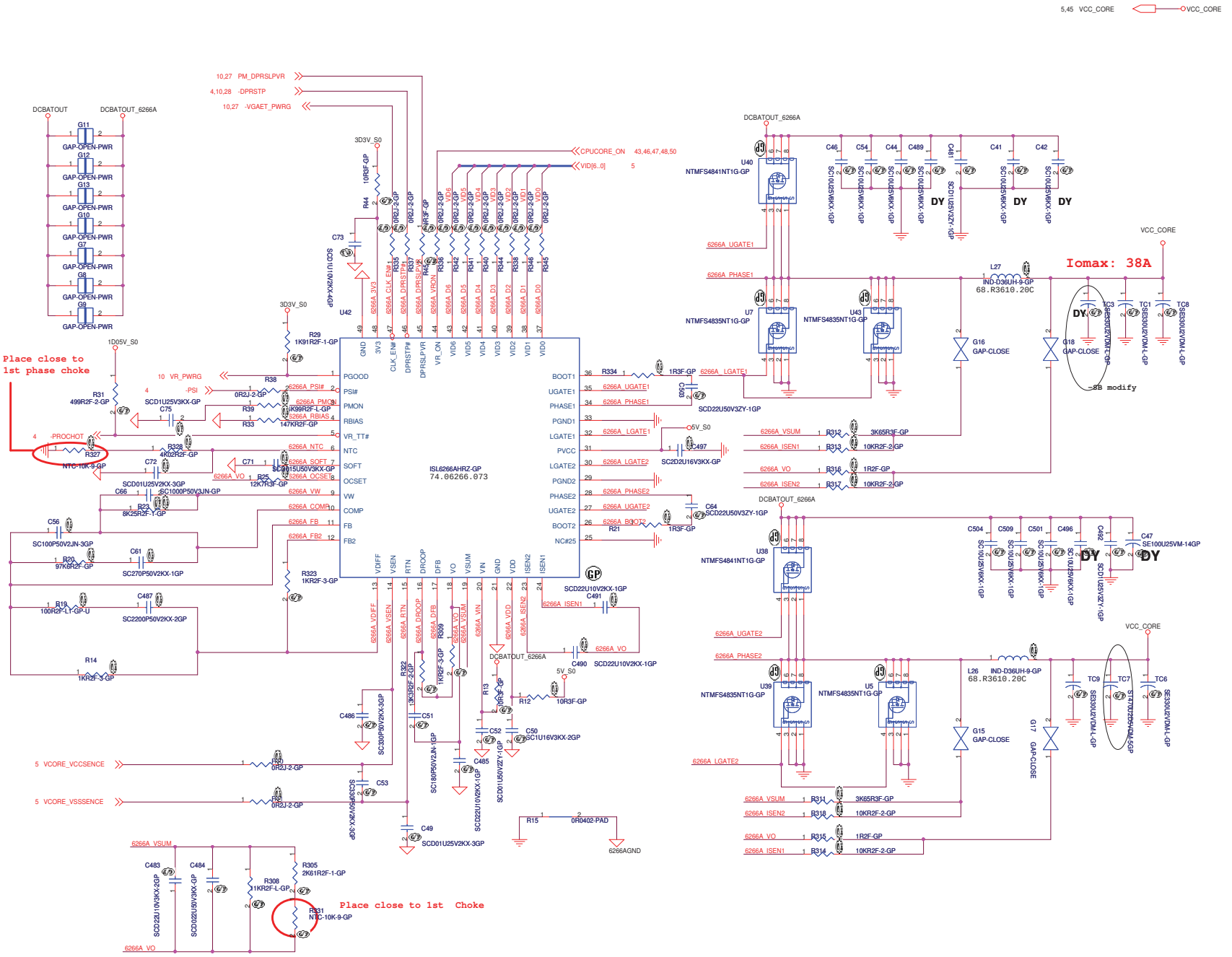
SA



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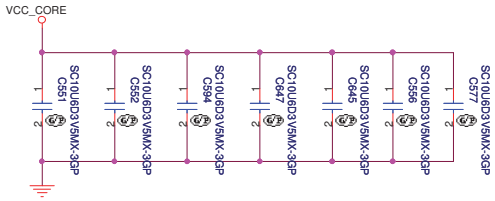
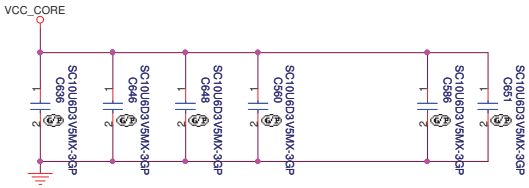
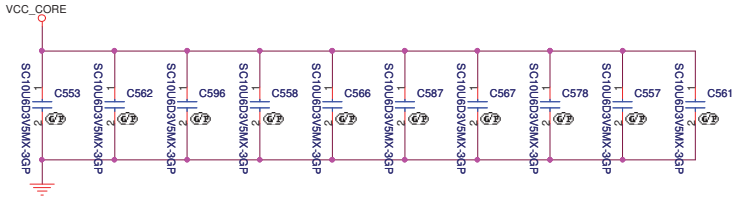
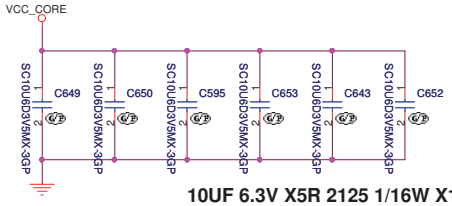




10UF 6.3V X5R 2125 1/16W X16 PCS

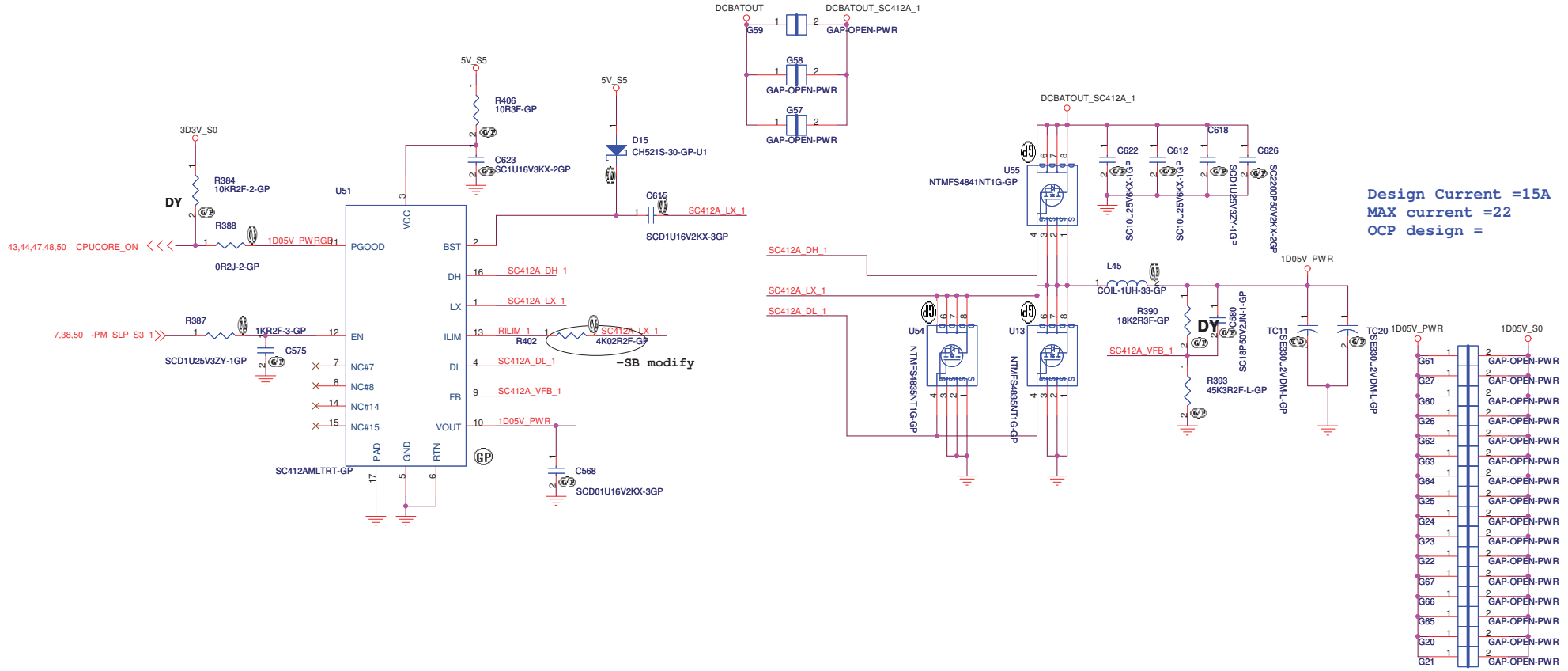




10UF 6.3V X5R 2125 1/16W X16 PCS

BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VCCCPUCORE DECOUPLING***	
Size: Custom	Document Number: **LT32M**	Rev: **SA**
Date: Wednesday, December 26, 2007	Sheet 45 of 53	



BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SC412A +1.05VM***	
Size A3	Document Number **LT32M**	Rev **SA**
Date: Wednesday, December 26, 2007	Sheet 46 of 53	

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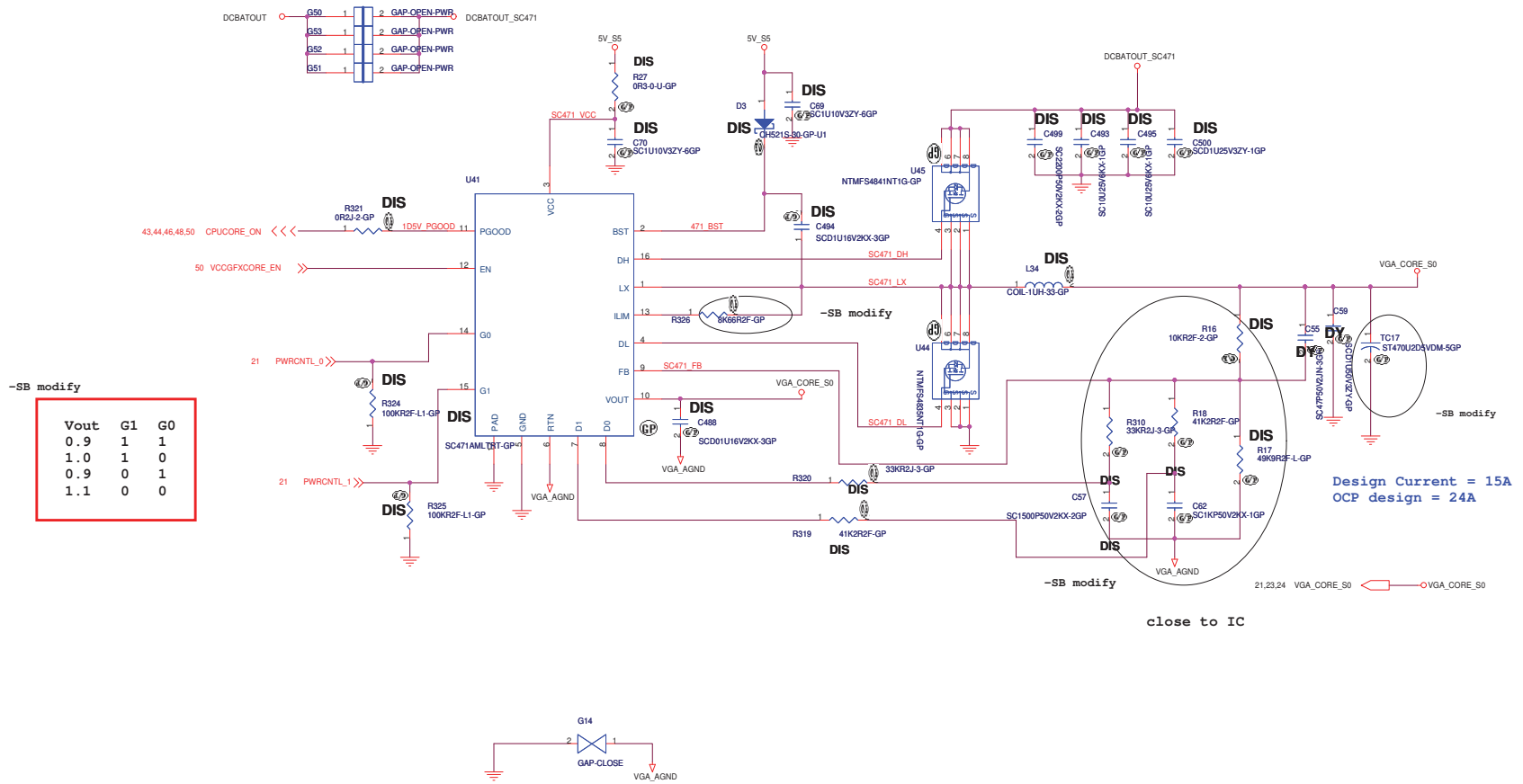


-SB modify

Vout	G1	G0
0.9	1	1
1.0	1	0
0.9	0	1
1.1	0	0

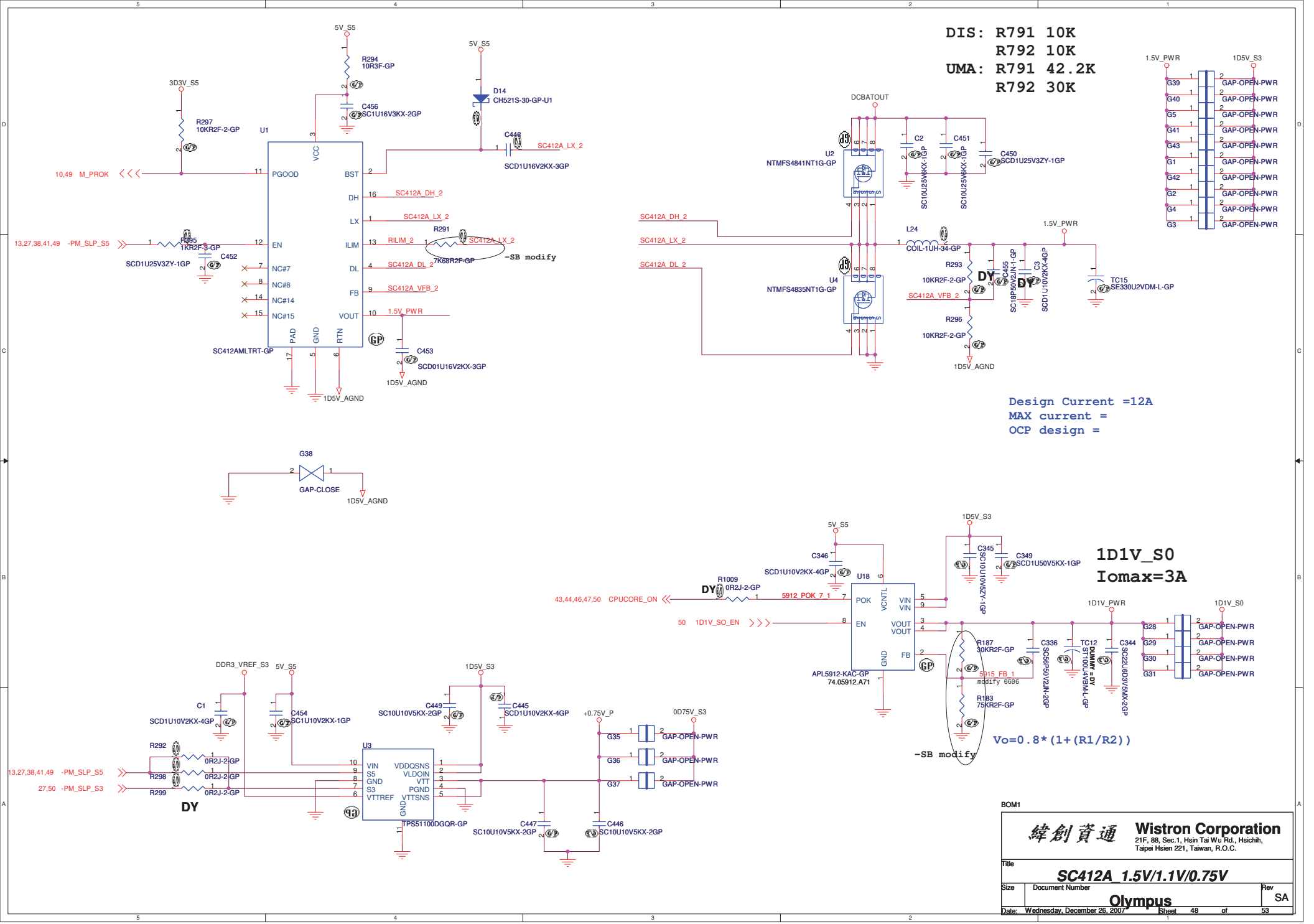
BOM1

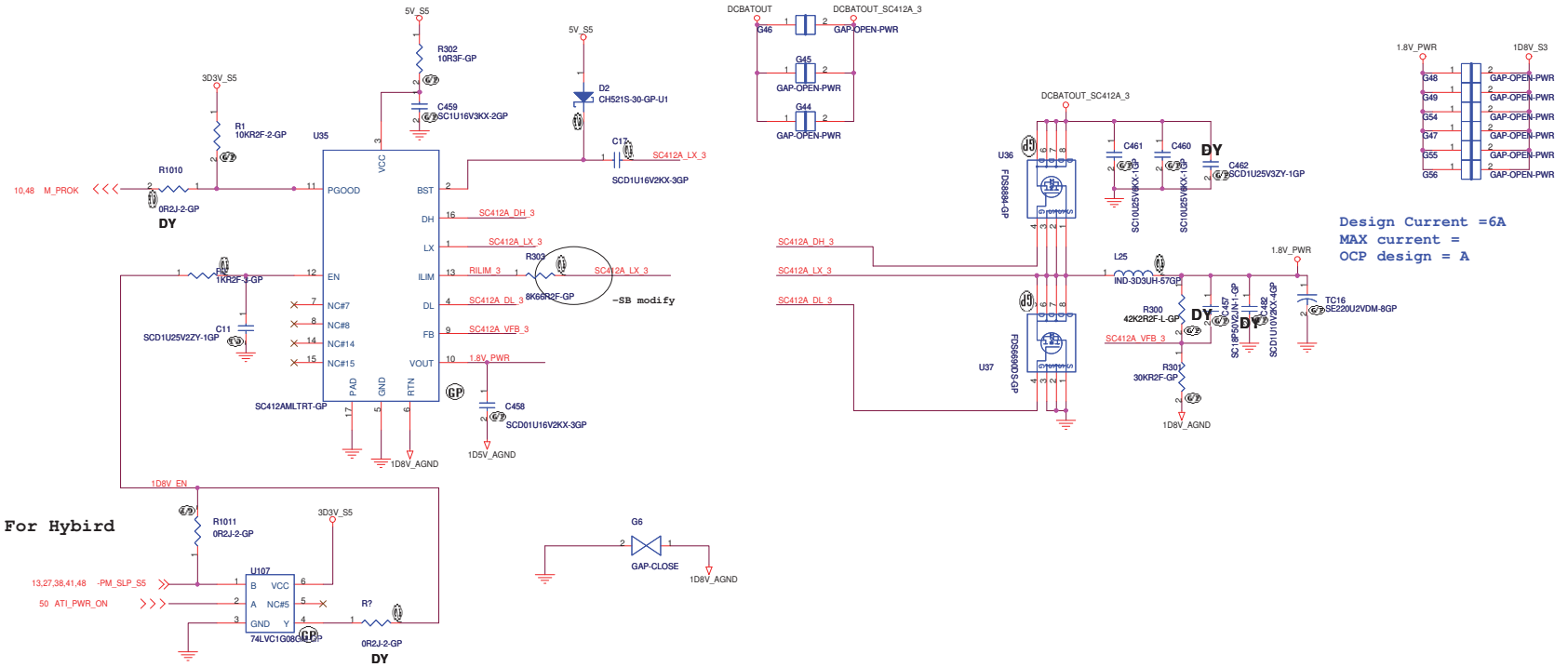
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SC471A VGA CORE**

Size	Document Number	Rev
C	LT32M	SA

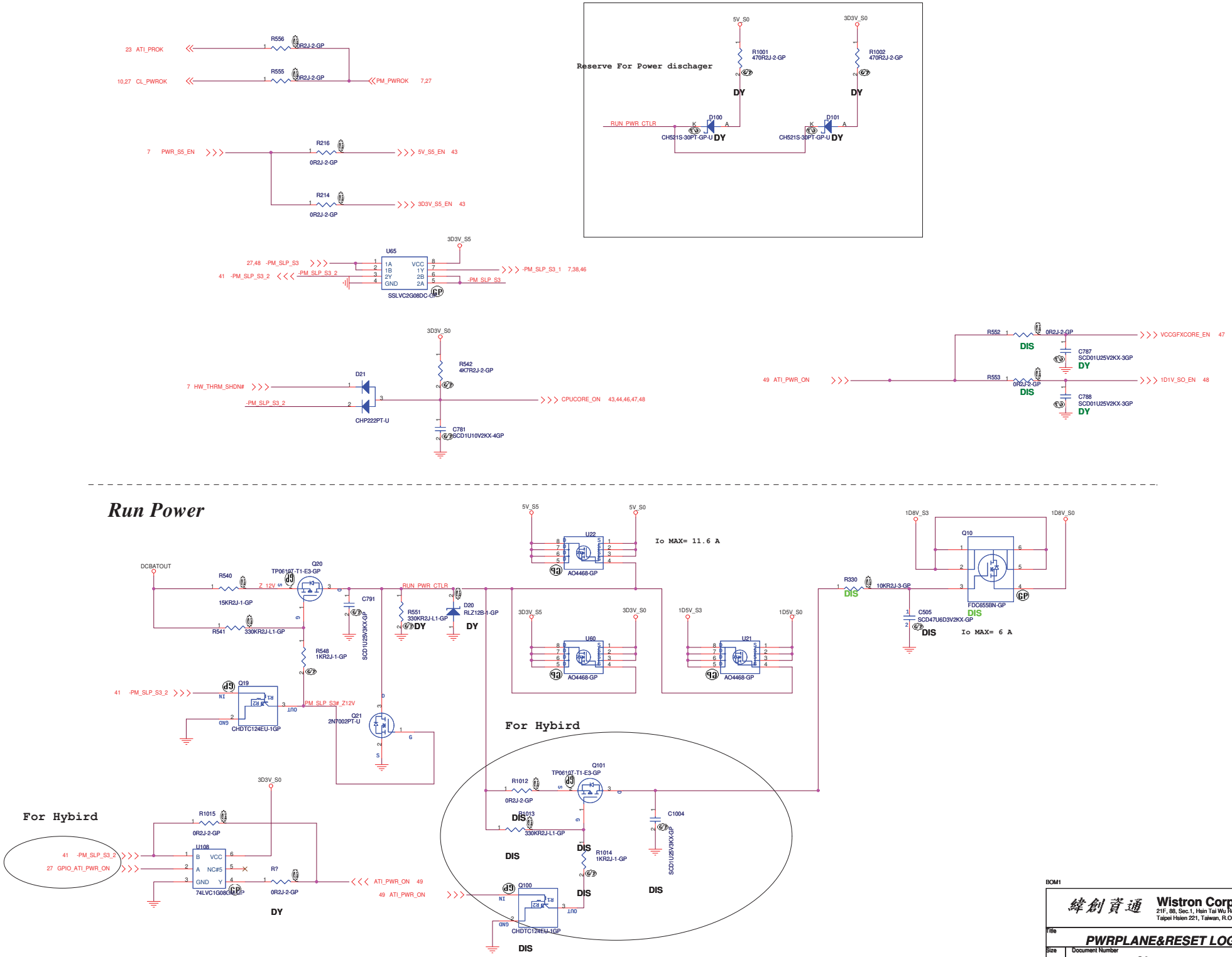
Date: Wednesday, December 26, 2007 Sheet 47 of 53


DIS: R791 10K
R792 10K
UMA: R791 42.2K
R792 30K
U1
SC412AMLTRT-GP
PGOOD
EN
NC#7
NC#8
NC#14
NC#15
VCC
BST
DH
LX
ILIM
DL
FB
VOUT
PAD
GND
RTN
R294 10R3F-GP
R297 10KR2F-2-GP
C456 SC1U16V3KX-2GP
D14 CH521S-30-GP-U1
C448 SCD1U16V2KX-3GP
SC412A_LX_2
SC412A_DH_2
SC412A_DL_2
SC412A_VFB_2
RILIM_2
R291 7K68R2F-GP
-SB modify
R295 1KR2F-3-GP
C452 SCD1U25V3ZY-1GP
C453 SCD01U16V2KX-3GP
1.5V_PWR
1D5V_AGND
M_PROK
-PM_SLP_S5
DCBATOUT
U2 NTMFS4841NT1G-GP
U4 NTMFS4835NT1G-GP
C2 SC10U25V6KX-1GP
C451 SC10U25V6KX-1GP
C450 SCD1U25V3ZY-1GP
L24 COIL-1UH-34-GP
R293 10KR2F-2-GP
R296 10KR2F-2-GP
C455 SC18P50V2JN-1-GP
C3 SCD1U10V2KX-4GP
TC15 SE330U2VDM-L-GP
DY
1.5V_PWR
1D5V_S3
G39
G40
G5
G41
G43
G1
G42
G2
G4
G3
GAP-OPEN-PWR
Design Current =12A
MAX current =
OCP design =
G38
GAP-CLOSE
1D1V_S0
Iomax=3A
U18
APL5912-KAC-GP
74.05912.A71
POK
EN
VCNTL
VIN
VOUT
FB
GND
5912_POK_7_1
CPUCORE_ON
1D1V_SO_EN
R1009 0R2J-2-GP
C346 SCD1U10V2KX-4GP
C345 SC10U10V5ZY-1GP
C349 SCD1U50V5KX-1GP
R187 30KR2F-GP
R183 75KR2F-GP
5915_FB_1
modify 0606
-SB modify
Vo=0.8*(1+(R1/R2))
C336 SC56P50V2JN-2GP
TC12 ST100U4VBM-L-GP
DUMMY = DY
C344 SC22UUD3V5MX-2GP
1D1V_PWR
1D1V_S0
G28
G29
G30
G31
DDR3_VREF_S3
C1 SCD1U10V2KX-4GP
C454 SC1U10V2KX-1GP
C449 SC10U10V5KX-2GP
C445 SCD1U10V2KX-4GP
U3
TPS51100DGQR-GP
VIN
S5
GND
S3
VTTREF
VDDQSNS
VLDOIN
VTT
PGND
VTTSNS
R292 0R2J-2-GP
R298 0R2J-2-GP
R299 0R2J-2-GP
DY
+0.75V_P
0D75V_S3
G35
G36
G37
C447 SC10U10V5KX-2GP
C446 SC10U10V5KX-2GP
BOM1
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SC412A_1.5V/1.1V/0.75V
Size
Document Number
Olympus
Rev
SA
Date: Wednesday, December 26, 2007
Sheet 48 of 53



BOM1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SC412A_1.8V	
Size	Document Number: LT32M	Rev: SA
Date: Wednesday, December 26, 2007	Sheet 49 of 53	



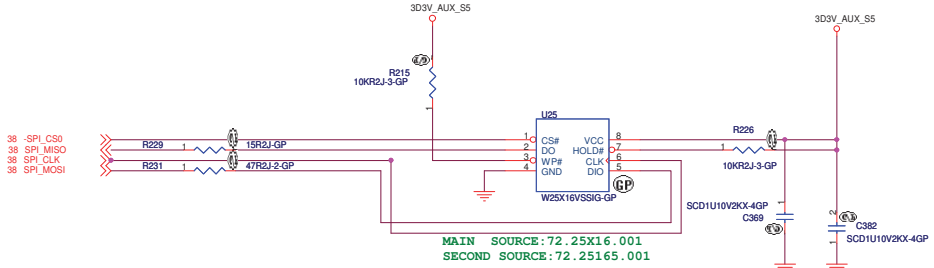
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

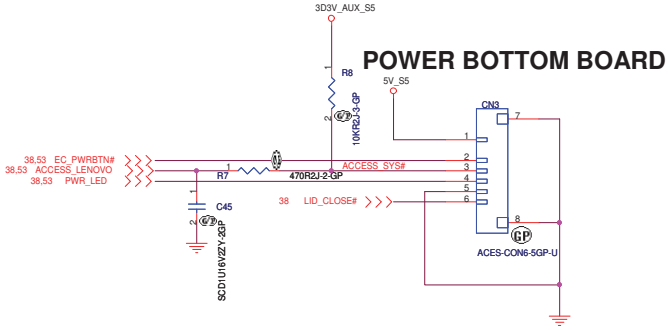
Title: PWRPLANE&RESET LOGIC

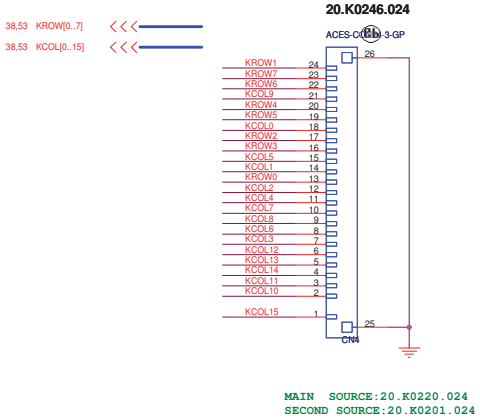
Size | Document Number: Olympus | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 50 of 53

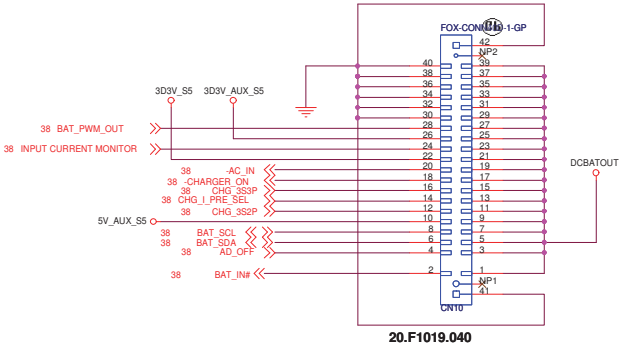


SPI FLASH



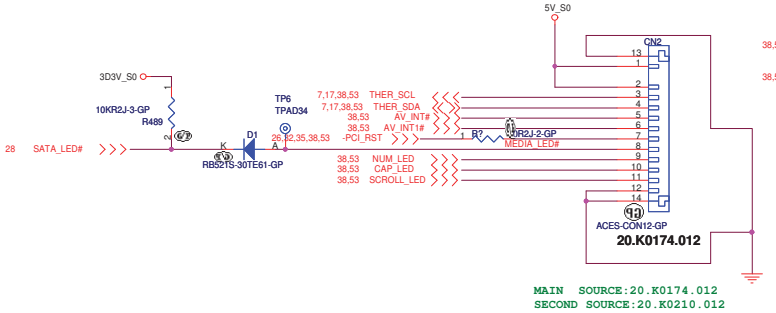


KEYBORD CONNECTOR

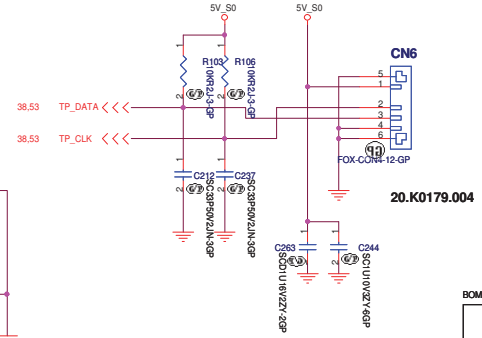


CHARGER CONNECTOR

AV Panel



TouchPad Connector



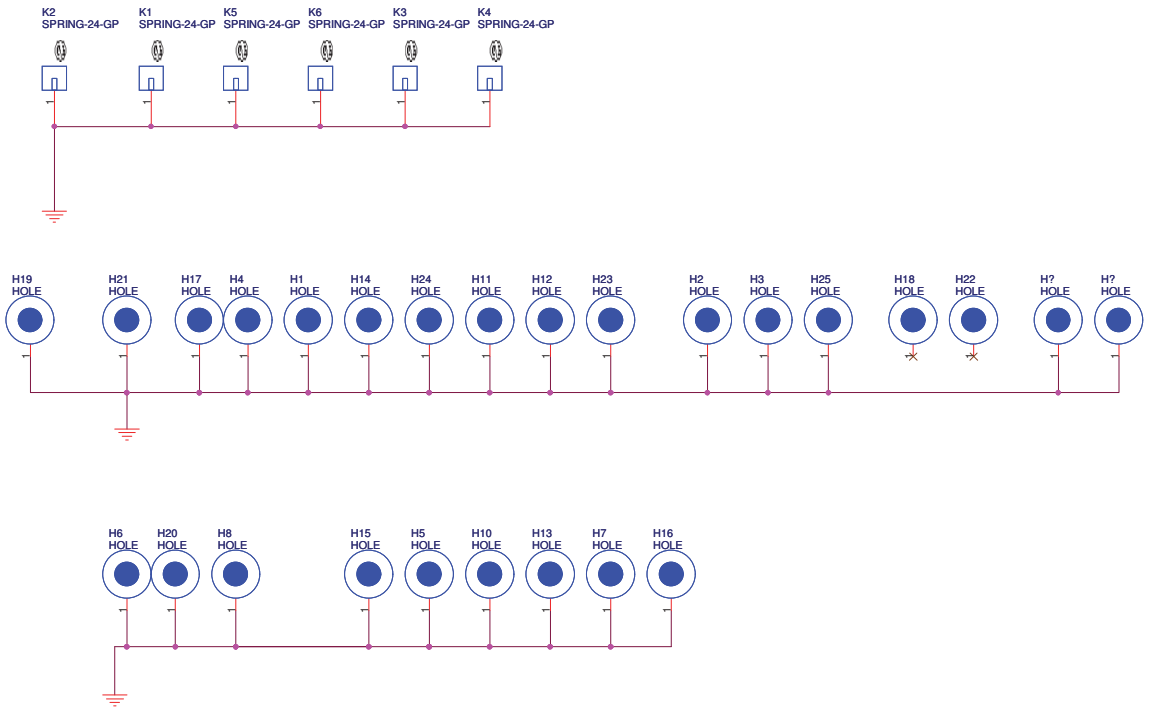
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **KB/TP/SPI/AV/Charger**

Size | Document Number: **Olympus** | Rev: SB

Date: Wednesday, December 26, 2007 | Sheet 51 of 53



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PTH FOR SCREW HOLES***

Size	Document Number	Rev
Custom	**Olympus**	**SB**

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Near CN13 KB

38,51 KROW[0..7]
38,51 KCOL[0..15]

KROW0	TPAD34	TP46
KROW1	TPAD34	TP45
KROW2	TPAD34	TP19
KROW3	TPAD34	TP24
KROW4	TPAD34	TP43
KROW5	TPAD34	TP25
KROW6	TPAD34	TP47
KROW7	TPAD34	TP33
KCOL0	TPAD34	TP42
KCOL1	TPAD34	TP22
KCOL2	TPAD34	TP27
KCOL3	TPAD34	TP37
KCOL4	TPAD34	TP44
KCOL5	TPAD34	TP35
KCOL6	TPAD34	TP29
KCOL7	TPAD34	TP26
KCOL8	TPAD34	TP40
KCOL9	TPAD34	TP28
KCOL10	TPAD34	TP30
KCOL11	TPAD34	TP38
KCOL12	TPAD34	TP31
KCOL13	TPAD34	TP41
KCOL14	TPAD34	TP32
KCOL15	TPAD34	TP39

Near CN24 POWER BOOTOM BOARD

5V_S5	TPAD34	TP36
38,51 EC_PWRBTN#	TPAD34	TP34
38,51 ACCESS_LENOVO	TPAD34	TP20
38,51 PWR_LED	TPAD34	TP21
	TPAD34	TP49

Near CN18 AV PANEL

5V_S0

	TPAD34	TP14
7,17,38,51 THER_SCL	TPAD34	TP17
7,17,38,51 THER_SDA	TPAD34	TP13
38,51 AV_INT#	TPAD34	TP11
38,51 AV_INT1#	TPAD34	TP12
26,32,35,38,51 -PCI_RST	TPAD34	TP10
38,51 NUM_LED	TPAD34	TP7
38,51 CAP_LED	TPAD34	TP50
38,51 SCROLL_LED	TPAD34	TP51
	TPAD34	TP5

Near CN20 TP

5V_S0	TPAD34	TP118
38,51 TP_DATA	TPAD34	TP127
38,51 TP_CLK	TPAD34	TP131
	TPAD34	TP92

Near CN17 USB&1394

33,42 TPA0P-2	TPAD34	TP52
33,42 TPA0N-2	TPAD34	TP53
33,42 TPB0P-2	TPAD34	TP56
33,42 TPB0N-2	TPAD34	TP101
5V_USB2_S5	TPAD34	TP104
	TPAD34	TP105
26,42 USB_PN0	TPAD34	TP106
26,42 USB_PP0	TPAD34	TP103
26,42 USB_PN2	TPAD34	TP227
26,42 USB_PP2	TPAD34	TP223
	TPAD34	TP217
5V_USB1_S5		

Near CAMERA1

CCD_PWR_RES	TPAD34	TP48
17,26 USB_PN8_CCD	TPAD34	TP57
17,26 USB_PP8_CCD	TPAD34	TP59
17 AUD_DMIC_CLK_G_R	TPAD34	TP58
17 AUD_DMIC_IN0_R	TPAD34	TP61
	TPAD34	TP62

Near CN6 MINI PORT-1

1D5V_S0	TPAD34	TP254
3D3V_S0	TPAD34	TP248
3D3V_S5	TPAD34	TP257
3,40 CLK_PCIE_MINI_1	TPAD34	TP150
3,40 -CLK_PCIE_MINI_1	TPAD34	TP144
26,40 PCIE_RXN1	TPAD34	TP113
26,40 PCIE_RXP1	TPAD34	TP116
26,40 PCIE_TXN1	TPAD34	TP110
26,40 PCIE_TXP1	TPAD34	TP112
26,40 USB_PN7_MINI	TPAD34	TP255
26,40 USB_PP7_MINI	TPAD34	TP256
27,30,35,40,41 SMB_CLK	TPAD34	TP252
27,30,35,40,41 SMB_DATA	TPAD34	TP253
27,35,40 PCIE_WAKE#	TPAD34	TP271
10,20,26,31,40,41 -PLT_RST	TPAD34	TP141
	TPAD34	TP250

Near CN7 MINI PORT-2

1D5V_S0	TPAD34	TP306
3D3V_S0	TPAD34	TP295
3D3V_S5	TPAD34	TP342
39,40 WIFI_BUSY	TPAD34	TP303
38,40 PCIE_DEBUG_Tx	TPAD34	TP289
38,40 WIFI_RF_EN	TPAD34	TP323
40 5V_DEBUG	TPAD34	TP273
31,40 WLAN_LED	TPAD34	TP324
3,40 CLK_PCIE_MINI_2	TPAD34	TP325
3,40 -CLK_PCIE_MINI_2	TPAD34	TP194
26,40 PCIE_RXN2	TPAD34	TP326
26,40 PCIE_RXP2	TPAD34	TP327
26,40 PCIE_TXN2	TPAD34	TP176
26,40 PCIE_TXP2	TPAD34	TP173
27,35,40 PCIE_WAKE#		
10,20,26,31,40,41 -PLT_RST	TPAD34	TP283

Near CN12 BT

3D3V_BT	TPAD34	TP177
26,39 USB_PP5_BT	TPAD34	TP180
26,39 USB_PN5_BT	TPAD34	TP171
31,39 BLUETOOTH_LED	TPAD34	TP184
39,40 WIFI_BUSY	TPAD34	TP175
39,40 BT_BUSY	TPAD34	TP181
	TPAD34	TP179

Near MDC1 MDC

3D3V_S5	TPAD34	TP264
28,39 ACZ_SDATA_OUT_MDC	TPAD34	TP259
28,39 ACZ_SYNC_MDC	TPAD34	TP258
28,39 ACZ_SDATAIN_MDC	TPAD34	TP145
28,39 -ACZ_RST_MDC	TPAD34	TP142
28,39 ACZ_BITCLK_MDC	TPAD34	TP149
	TPAD34	TP143

Near CN26 WLAN SW

38,39 WIRLESS_DISABLE#	TPAD34	TP328
	TPAD34	TP233

Near CN25 SPEAKER

34 SPKR_L-	SPKR_L-	TPAD34	TP1
34 SPKR_L+	SPKR_L+	TPAD34	TP2
34 SPKR_R-	SPKR_R-	TPAD34	TP3
34 SPKR_R+	SPKR_R+	TPAD34	TP4

Near HP/SPDIF1

5V_SPDIF_S0	TPAD34	TP218
34 SPDIF_HDMI	TPAD34	TP215
34 HP_OUT_L	TPAD34	TP216
34 HP_OUT_R	TPAD34	TP331
AUD_AGND	TPAD34	TP220
34 -HP_JACK_DET	TPAD34	TP219
	TPAD34	TP234

Near CARD1

3D3V_CARD	TPAD34	TP313
33 SD/XD/MS_DATA1_1	TPAD34	TP302
33 SD/XD/MS_DATA0_1	TPAD34	TP305
33 SD/XD/MS_DATA2_1	TPAD34	TP316
33 SD/XD/MS_DATA3_1	TPAD34	TP307
33 XD_DATA4_1	TPAD34	TP315
33 XD_DATA5_1	TPAD34	TP296
33 XD_DATA6_1	TPAD34	TP314
33 XD_DATA7_1	TPAD34	TP310
33 XD_CD#	TPAD34	TP157
33 SD_WP#(XDR/B#)	TPAD34	TP162
33 SD/XD/MS_CLK_1	TPAD34	TP158
33 XD_CE#	TPAD34	TP292
33 XD_CLE	TPAD34	TP156
33 XD_ALE	TPAD34	TP161
33 SD/XD/MS_CMD_1	TPAD34	TP163
33 MS_INS#	TPAD34	TP159
33 SD_CD#	TPAD34	TP167
33 XD_WP#	TPAD34	TP160
	TPAD34	TP318

Near SATA1

5V_S0	TPAD34	TP275
28,31 SATA_TXP0	TPAD34	TP260
28,31 SATA_TXN0	TPAD34	TP266
28,31 SATA_RXN0	TPAD34	TP332
28,31 SATA_RXP0	TPAD34	TP333
	TPAD34	TP272

Near ODD1

5V_S0	TPAD34	TP132
28,31 SATA_TXP1	TPAD34	TP251
28,31 SATA_TXN1	TPAD34	TP249
28,31 SATA_RXN1	TPAD34	TP136
28,31 SATA_RXP1	TPAD34	TP135
	TPAD34	TP134

Near HDMI1

5V_HDMI_S0	TPAD34	TP208
25 HDMI_TXD0_M	TPAD34	TP213
25 HDMI_TXD#0_M	TPAD34	TP221
25 HDMI_TXD1_M	TPAD34	TP334
25 HDMI_TXD#1_M	TPAD34	TP335
25 HDMI_TXD2_M	TPAD34	TP336
25 HDMI_TXD#2_M	TPAD34	TP337
25 HDMI_TXC_M	TPAD34	TP338
25 HDMI_TXC#_M	TPAD34	TP117
25 HDMI_SCLK_C	TPAD34	TP201
25 HDMI_SDATA_C	TPAD34	TP207
25,38 HDMI_HPD	TPAD34	TP200
	TPAD34	TP202

Near CN1

FAN1_VCC	TPAD34	TP16
5V_S0	TPAD34	TP23
7 FAN1_FG1	TPAD34	TP18
	TPAD34	TP15

Near CN9 NewCard

26,41 PCIE_TXP3	TPAD34	TP166
26,41 PCIE_TXN3	TPAD34	TP168
26,41 PCIE_RXP3	TPAD34	TP339
26,41 PCIE_RXN3	TPAD34	TP340
3,41 CLK_PCIE_NEW	TPAD34	TP170
3,41 -CLK_PCIE_NEW	TPAD34	TP172
41 -CPPE	TPAD34	TP276
3,41 -NEWCARD_CLKREQ	TPAD34	TP174
3D3V_NEW_S0	TPAD34	TP186
41 -PERST	TPAD34	TP187
3D3V_NEW_LAN_S5	TPAD34	TP341
1D5V_NEW_S0	TPAD34	TP301
27,30,35,40,41 SMB_DATA	TPAD34	TP191
27,30,35,40,41 SMB_CLK	TPAD34	TP300
41 -CPUSB	TPAD34	TP214
26,41 USB_PP9_NEWCARD	TPAD34	TP304
26,41 USB_PN9_NEWCARD	TPAD34	TP308
	TPAD34	TP169

BOM1

緯創資通 **Wistron Corporation**
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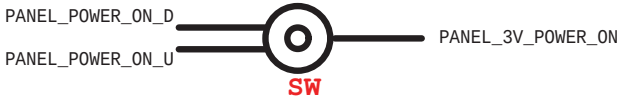
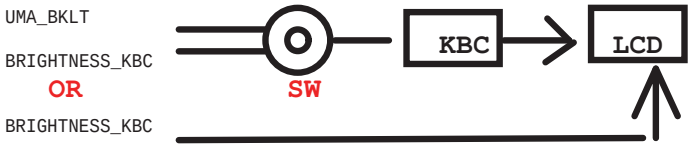
LCD

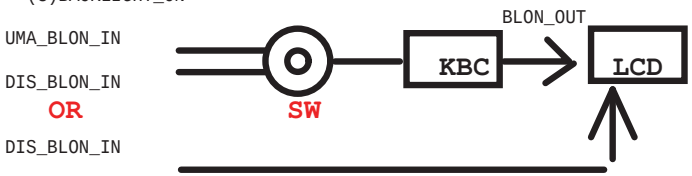
(1)PANEL_3V_ON



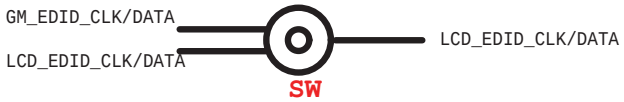
(2)BRIGHTNESS PWM



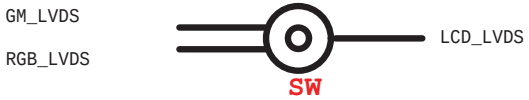
(3)BACKLIGHT_ON



(4)EDID DATA/CLK



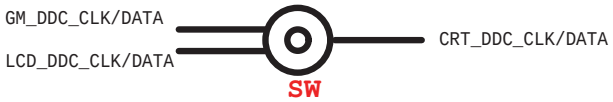
(5) LVDS signal



All the switch control by SB_GPIO52 and define
L => -UMA channel
H => -ATI channel

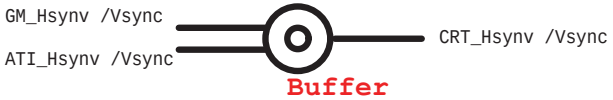
CRT

(1)DDC DATA/CLK



(2) RGB signal

(2) Hsynv & Vsync



BOM1

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