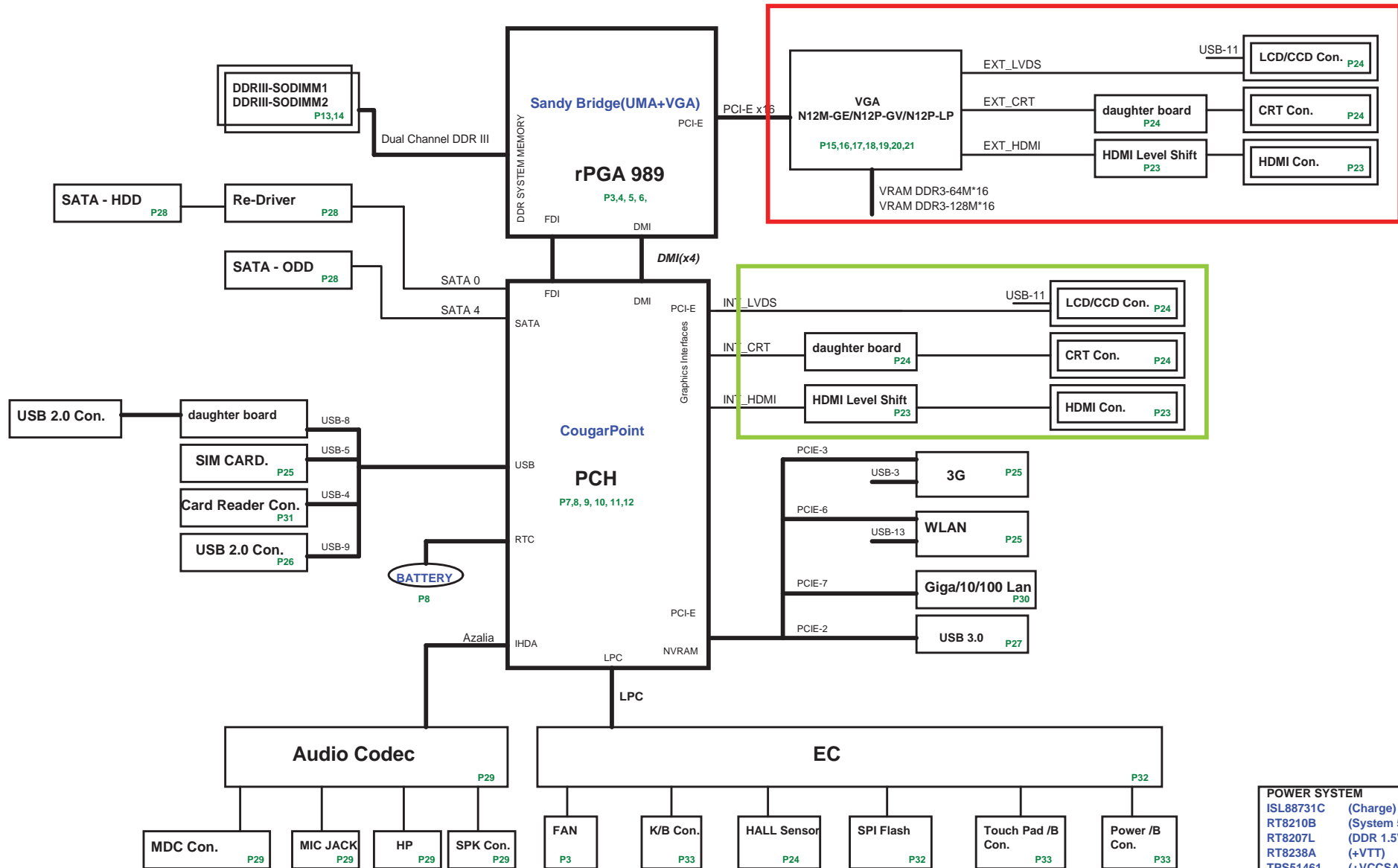


TE5 Block Diagram






01



POWER SYSTEM		
ISL88731C	(Charge)	P35
RT8210B	(System 5V/3V)	P36
RT8207L	(DDR 1.5V)	P37
RT8238A	(+VTT)	P38
TPS51461	(+VCCSA)	P39
ISL95835	(+VCC_CORE)	P40
G966A	(+1.8V)	P41
ISL95870A	(+GPU_CORE)	P42

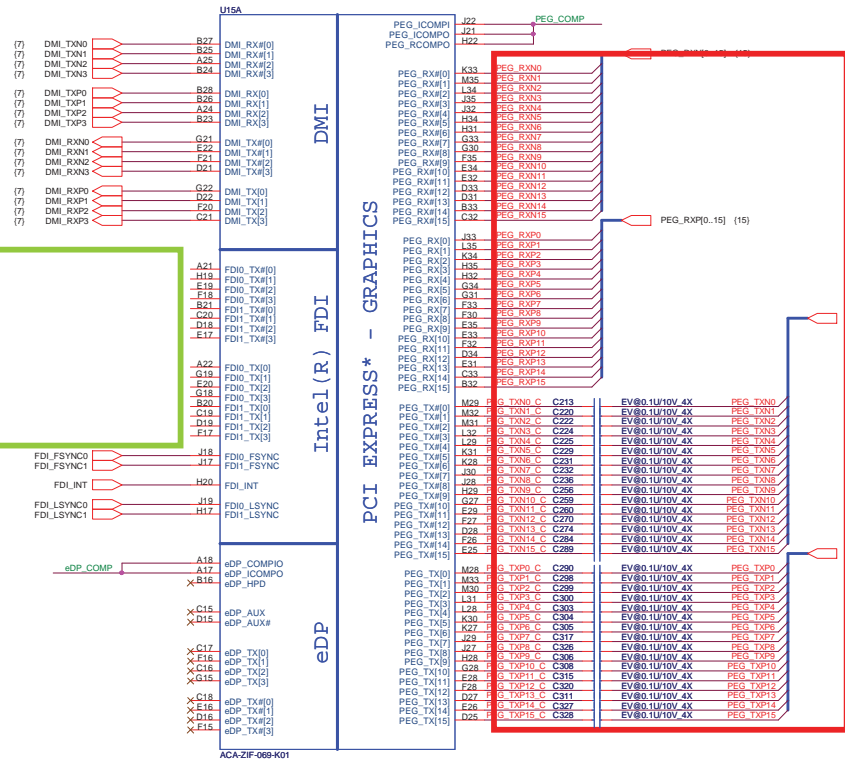
[illegible]

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
+VCCRTC	+3.0V~+3.3V		S0-S5
+3V	+3.3V	MAIN_ON	S0
+3V_S5	+3.3V	S5_ON	S0-S5
+3V_HDP	+3.3V	MAIN_ON	S0
+3VPCU	+3.3V	AC/DC Insert enable	S0
+5V	+5V	MAIN_ON	S0
+5V_S5	+5V	S5_ON	S0-S5
+5VPCU	+5V	AC/DC Insert enable	S0-S5
WIMAX_P	+3.3V	WMAX_P for WLAN	
+1.8V	+1.8V	MAIN_ON	S0
+1.5V	+1.5V	MAIN_ON	S0
+1.5V_SUS	+1.5V	SUSON	S0-S3
+VCC_CORE		VRON	S0
+VTT	+1.05V	MAIN_ON	S0
+1.05V	+1.05V	MAIN_ON	S0
+VAXG		MPWROK	S0

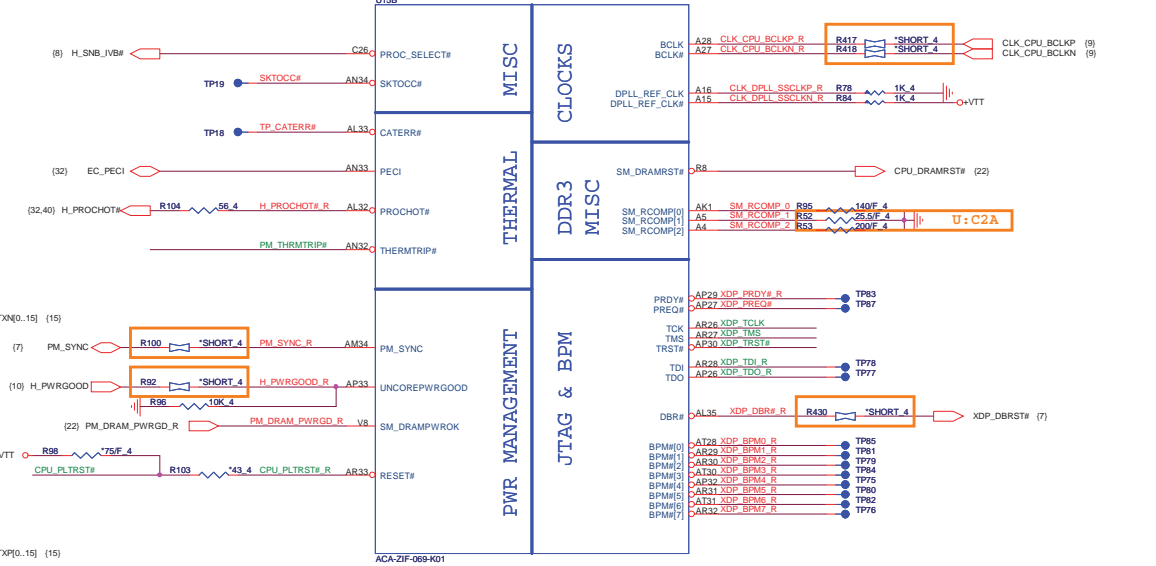
GND PLANE	PAGE
 8769AGND	32
 Audio_GND	29
 Shield_GND	29
 GND	ALL
 ISL95870A_AGND	29

02

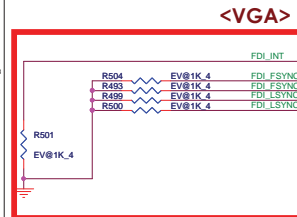
Sandy Bridge Processor (DMI,PEG,FDI) <CPU,VGA>



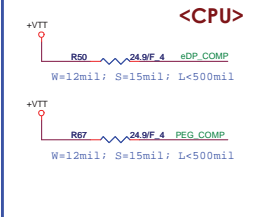
Sandy Bridge Processor (CLK,MISC,JTAG)<CPU>



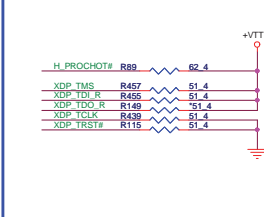
FDI Disabling (Discrete Only)



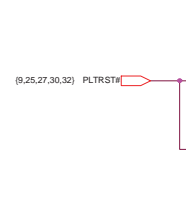
DP & PEG Compensation



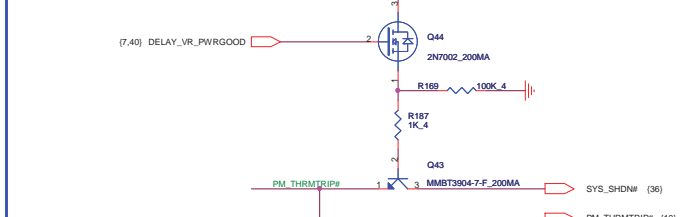
Processor pull-up <CPU>



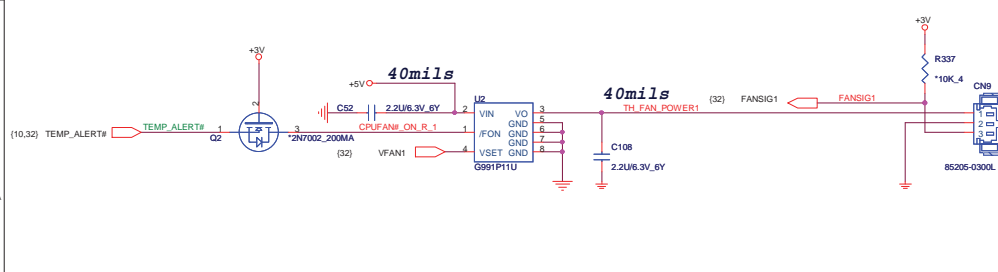
Level Shift <CPU>



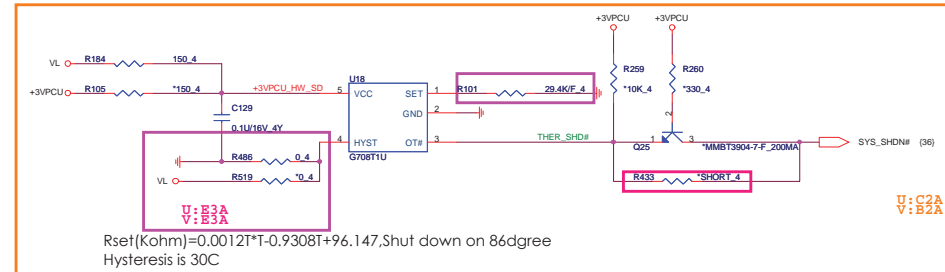
Thermal Trip<CPU>

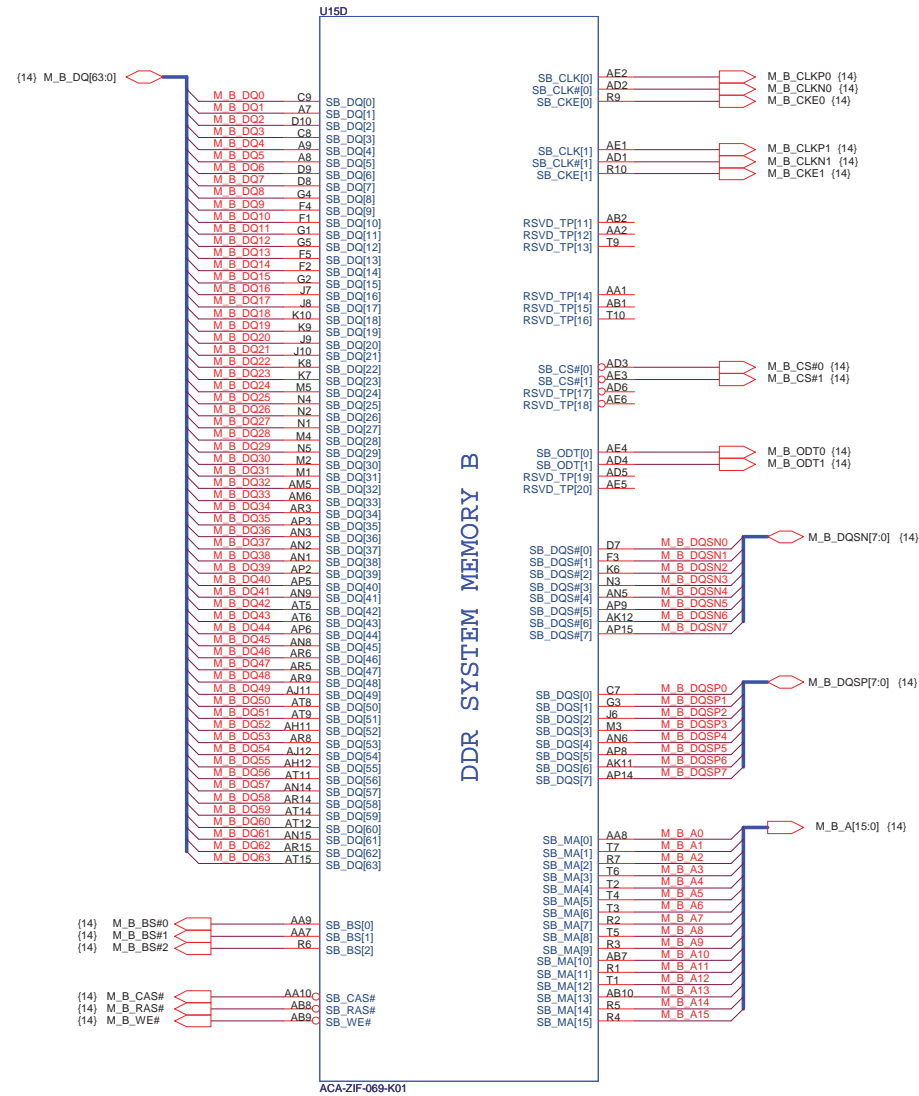


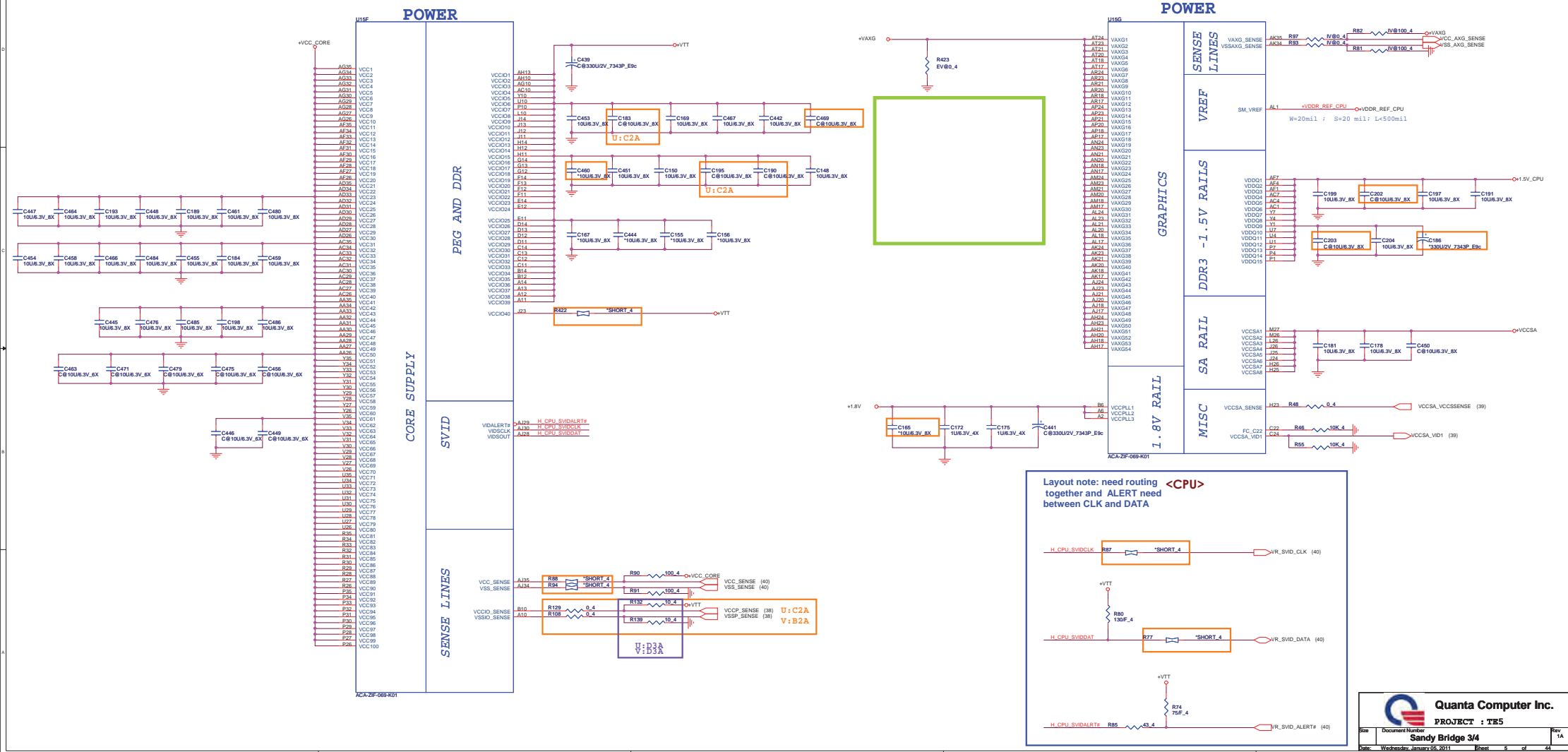
FAN Control-->For one FAN solution <THC/THV>



CPU Thermal sensor / MB Local TEMP <THC>



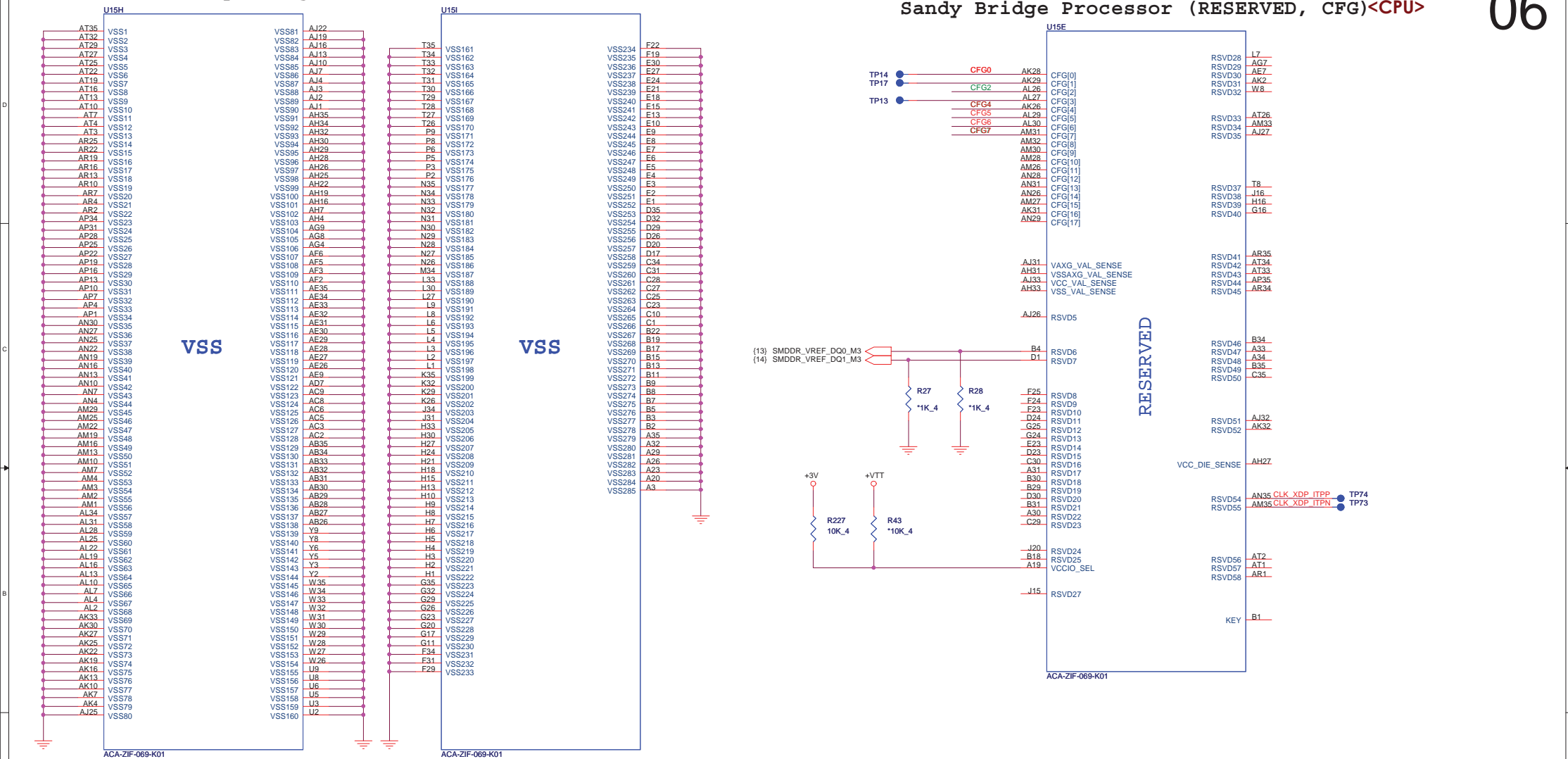




Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)<CPU>

06



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

<CPU>



CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



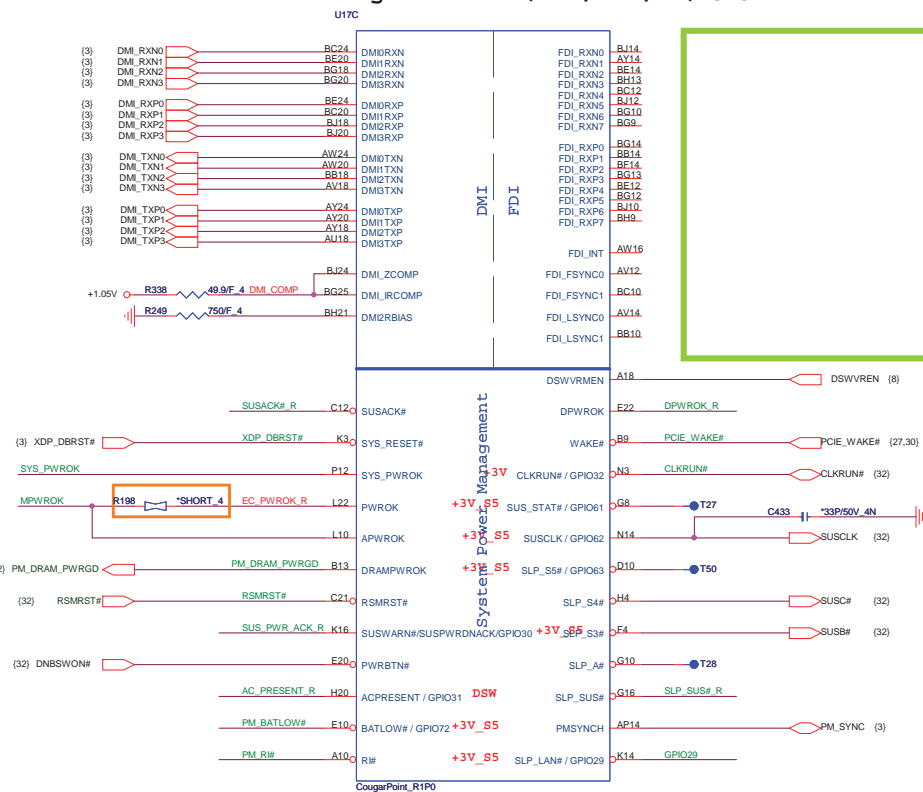
Quanta Computer Inc.

PROJECT : TE5

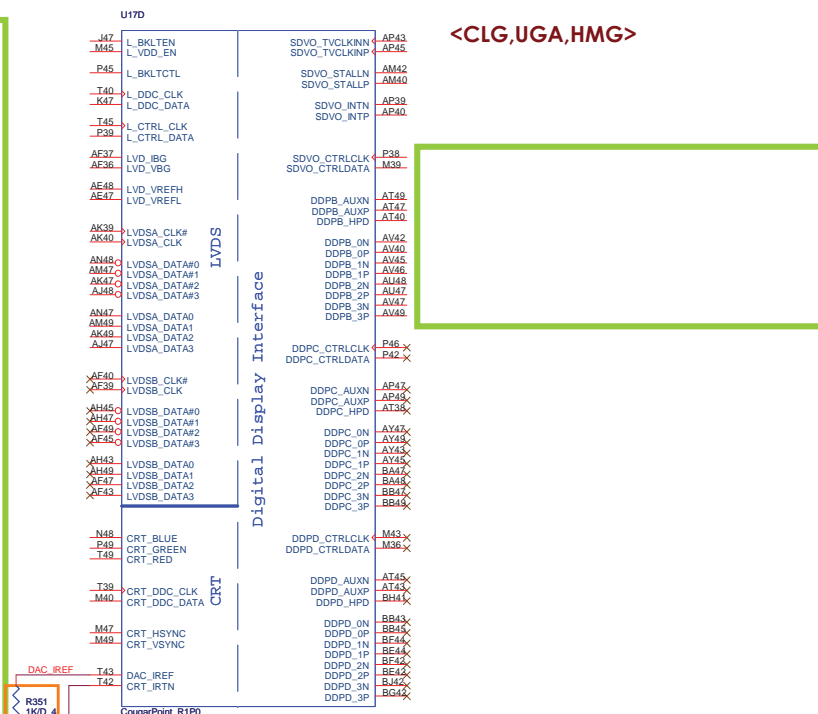
Size	Document Number	Rev
	Sandy Bridge 4/4	1A

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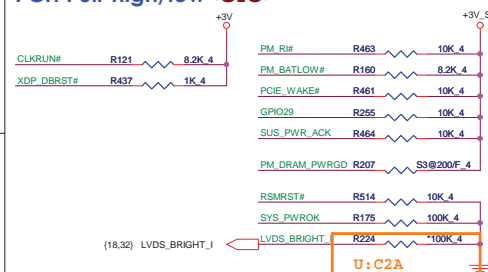
Cougar Point (DMI,FDI,PM)<CLG>



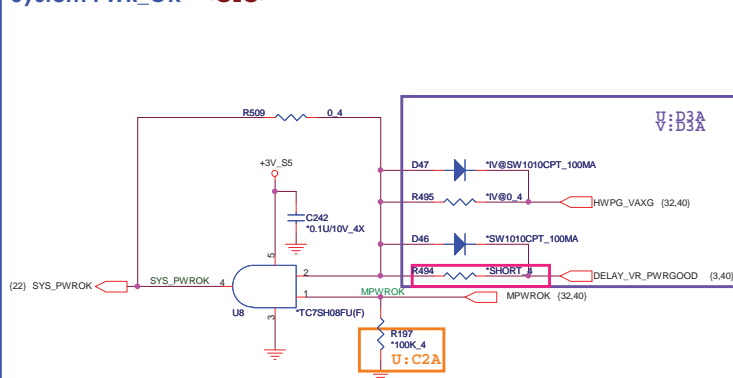
Cougar Point (LVDS,DDI) <CLG/UGA/HMG>



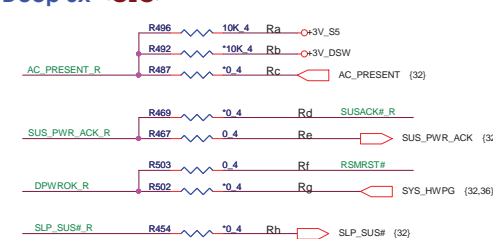
PCH Pull-high/low<CLG>



System PWR OK <CLG>

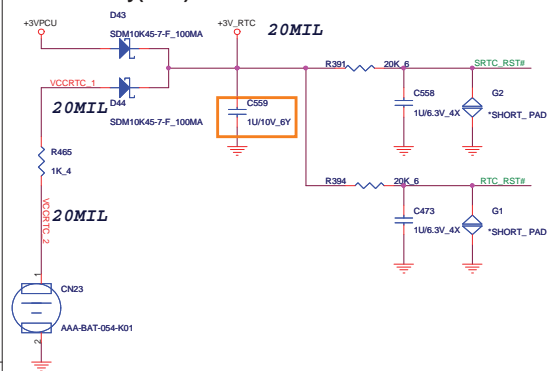


Deep Sx <CLG>

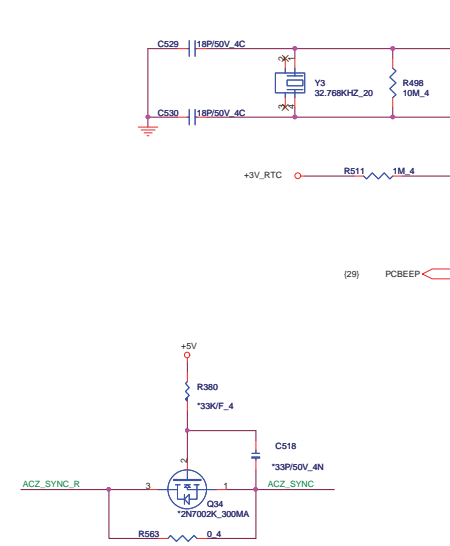


Net Name	Deep Sx Support	Deep Sx No Support
AC_PRESENT	Rb,Rc stuff	Ra stuff
SUS_PWR_ACK	Rd stuff	Re stuff
DPWROK	Rg stuff	Rf stuff
SLP_SUS	Rh stuff	Rh No stuff

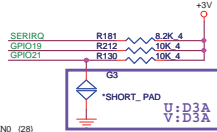
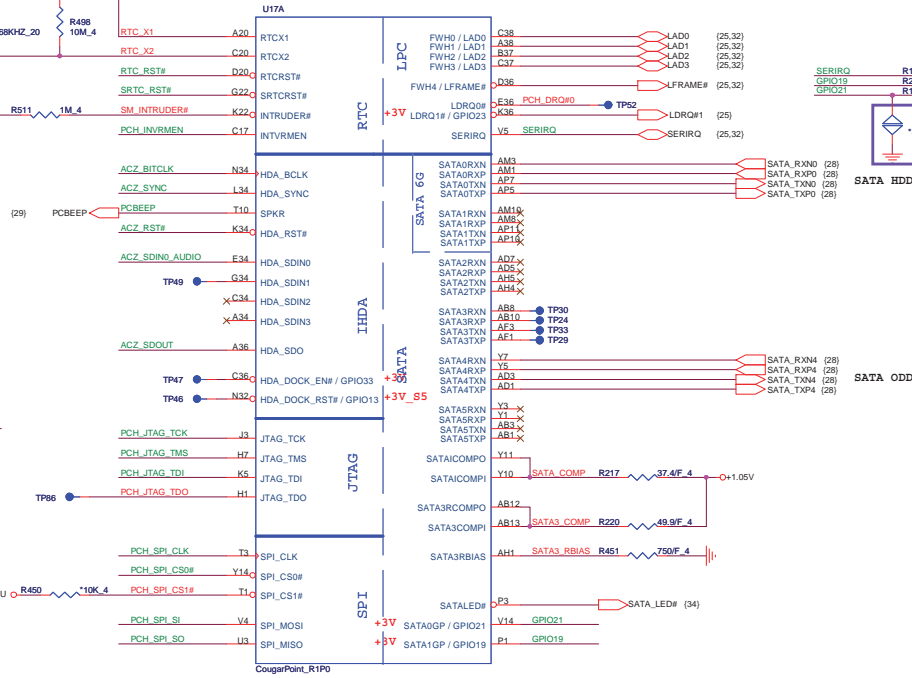
RTC Circuitry(RTC)



PCH2 (CLG)



Cougar Point (HDA, JTAG, SATA)



SATA HDD/SSD

SATA ODD

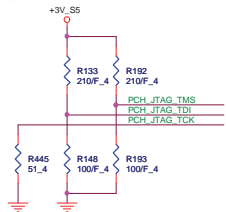
HDA Bus(CLG)



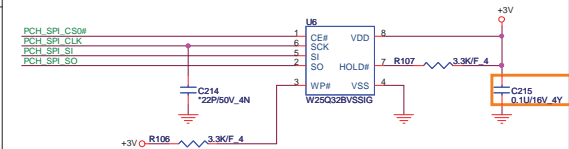
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V ₀ R116 1K 4 PCBEEP
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R530 1K 4 PCL_GNT3# (9)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC ₀ R497 330K 4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		R539 1K 4 GNT1# (9)
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R449 1K 4 GPIO19
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V ₀ R521 1K 4 ACZ_SDOUT ACZ_SDOUT (3)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R453 2.2K 4 DF_TVS (10) R452 1K 4 H_SNB_VB# (3)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3V_S5 R208 10K 4 PLL_ODVR_EN (10) R195 1K 4
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 ₀ R525 1K 4 ACZ_SYNC
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect
GNT2# / GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile
GPIO15	TLS Confidentiality	RSMRST	0 = Default. TLS No Confidentiality 1 = TLS Confidentiality	+3V_S5 ₀ R313 1K 4 GPIO15 (10)
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC
SATA3GP/ GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled
SATA2GP/ GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	+3V_RTC ₀ R489 330K 4 DSWVREN (7) R490 330K 4

PCH JTAG Debug (CLG)

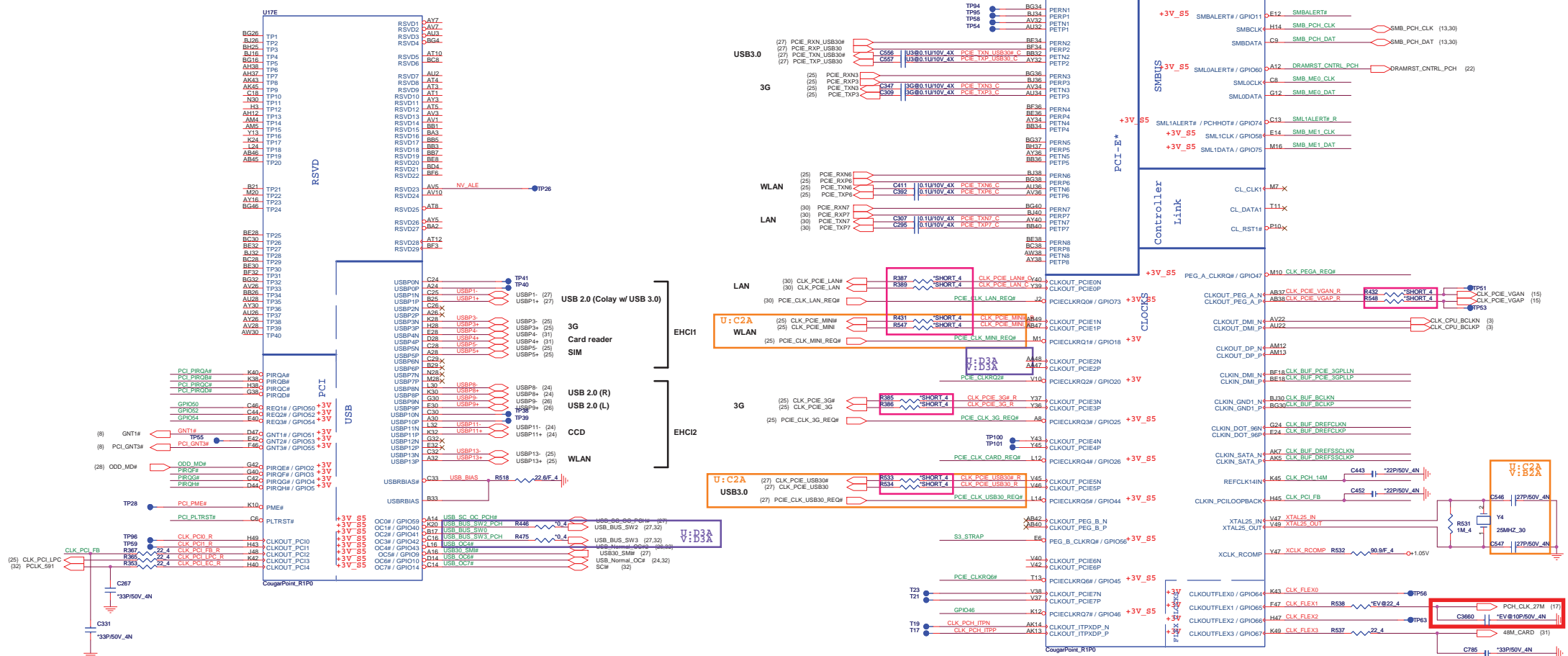


PCH Dual SPI (CLG)

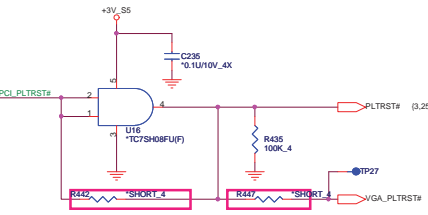


Cougar Point-M (PCI,USB,NVRAM) <CLG>

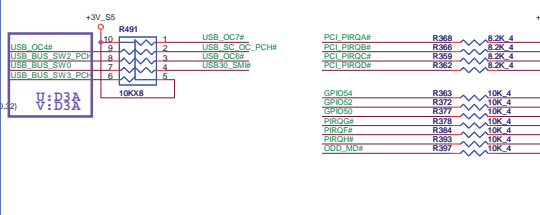
Cougar Point-M (PCI-E,SMBUS,CLK) <CLG,U3B,VGA,MNG>



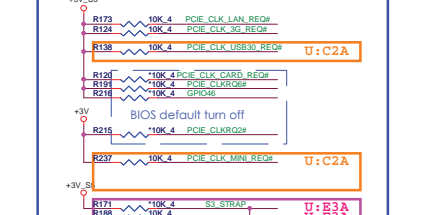
PLTRST# <CLG,VGA>



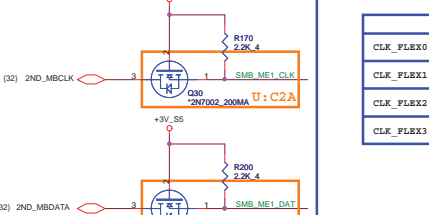
PCI/USBOC# Pull-up <CLG>



CLK_REQ/Strap Pin <CLG>



SMBus/Pull-up <CLG>

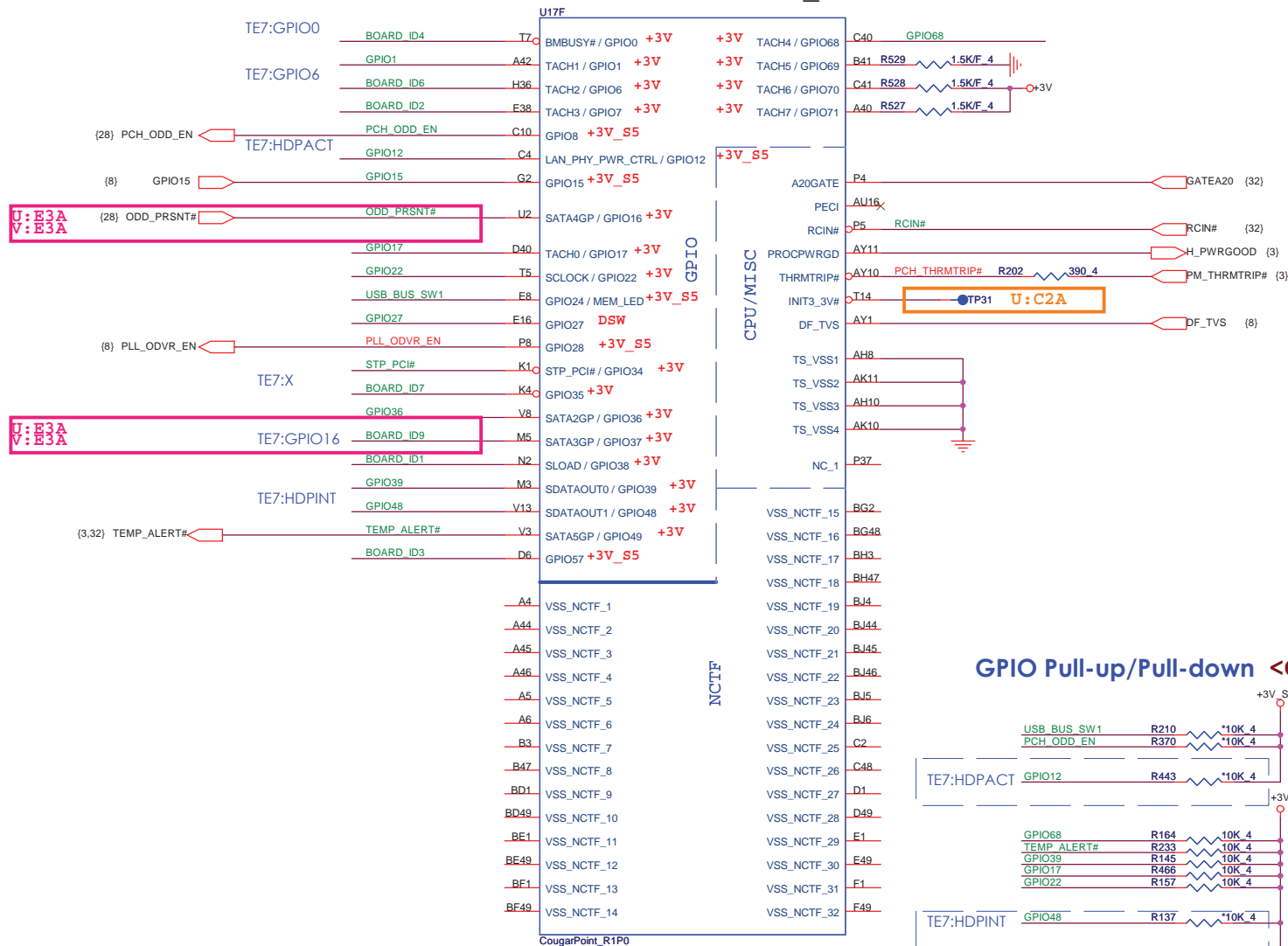


CLK_FLEX0, CLK_FLEX1, CLK_FLEX2, CLK_FLEX3

	33MHz	27MHz	48/24MHz	14.318MHz	25MHz
CLK_FLEX0					
CLK_FLEX1					
CLK_FLEX2					
CLK_FLEX3					

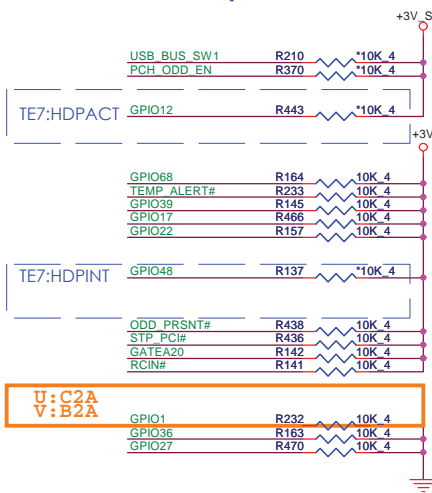
Cougar Point (GPIO,VSS_NCTF,RSVD) <CLG>

BOARD ID SETTING <CLG> 10

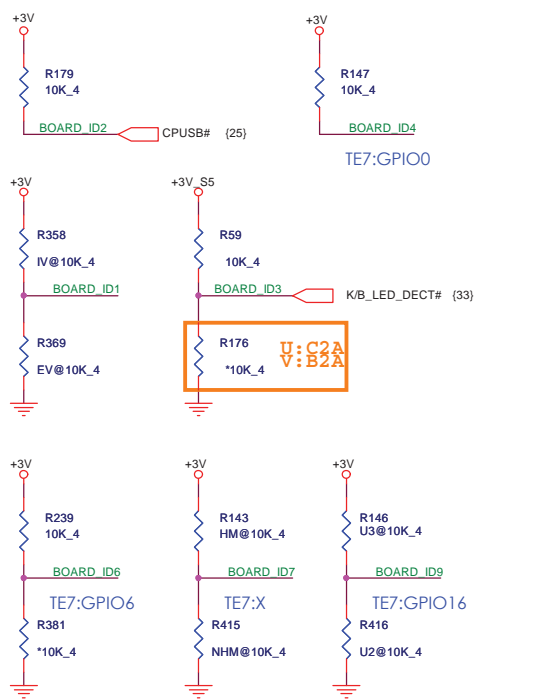


U:C2A

GPIO Pull-up/Pull-down <CLG>



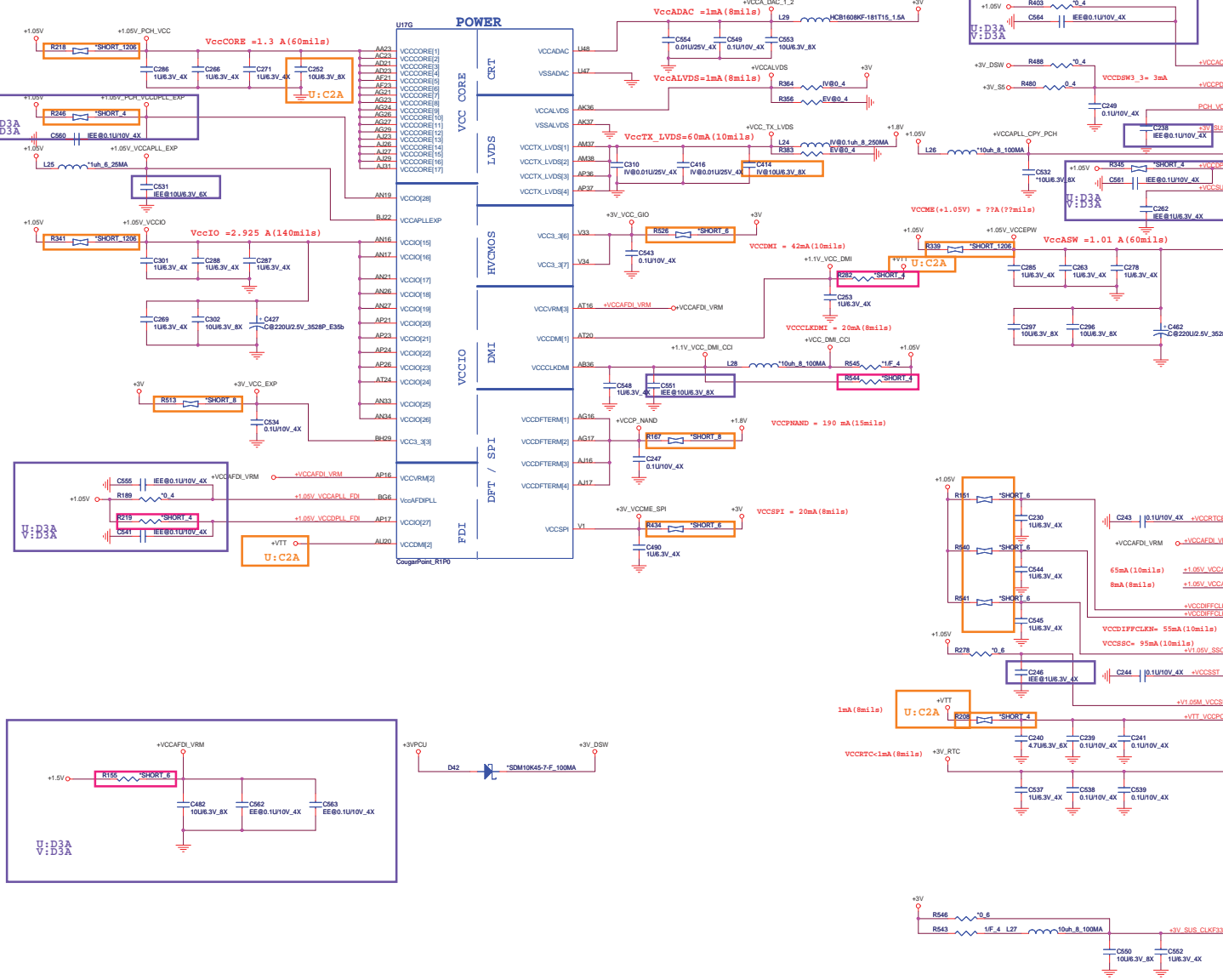
Board ID	ID1	ID2	ID3	ID4	ID6	ID7	ID9	GPIO1
UMA SKU	H							
VGA SKU	L							
W/O 3G		H						
W/ 3G		L						
W/O LED KB			H					
W/ LED KB			L					
14"				H				
15"				L				
W/ MDC					H			
W/O MDC					L			
W/ HDMI						H		
W/O HDMI						L		
USB3.0							H	
USB2.0							L	
W/ G-sensor								H
W/O G-sensor								L



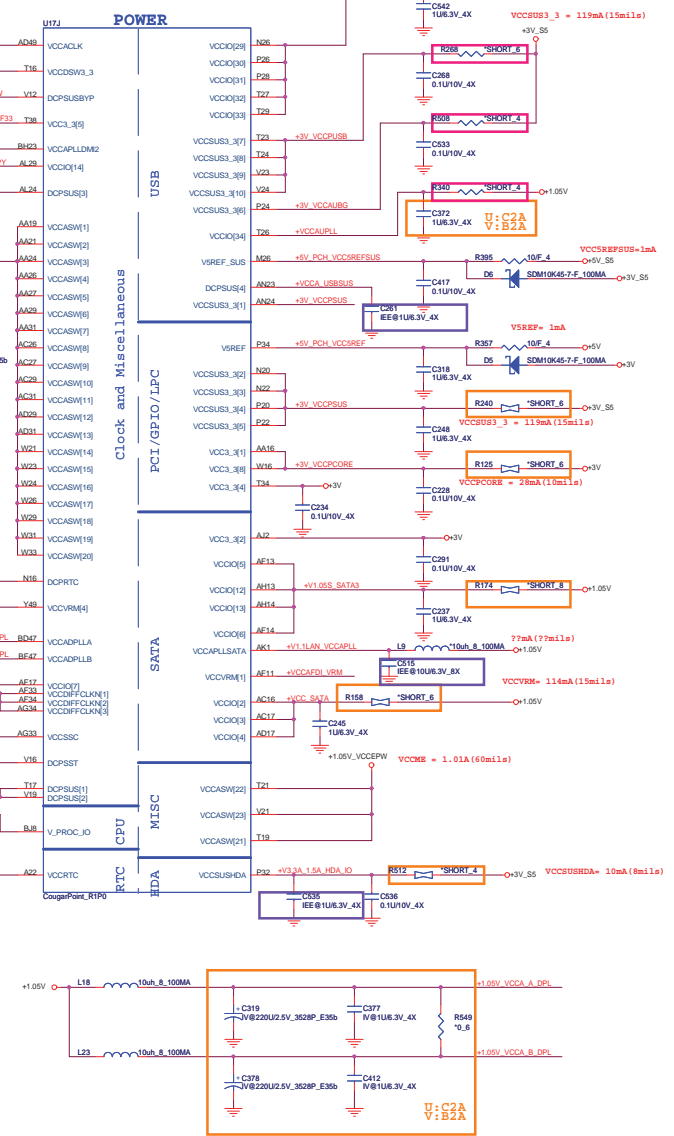
Quanta Computer Inc.
PROJECT : TE5

Size	Document Number	Rev 1A
Cougar Point 4/6		
Date:	Wednesday, January 05, 2011	Sheet 10 of 44

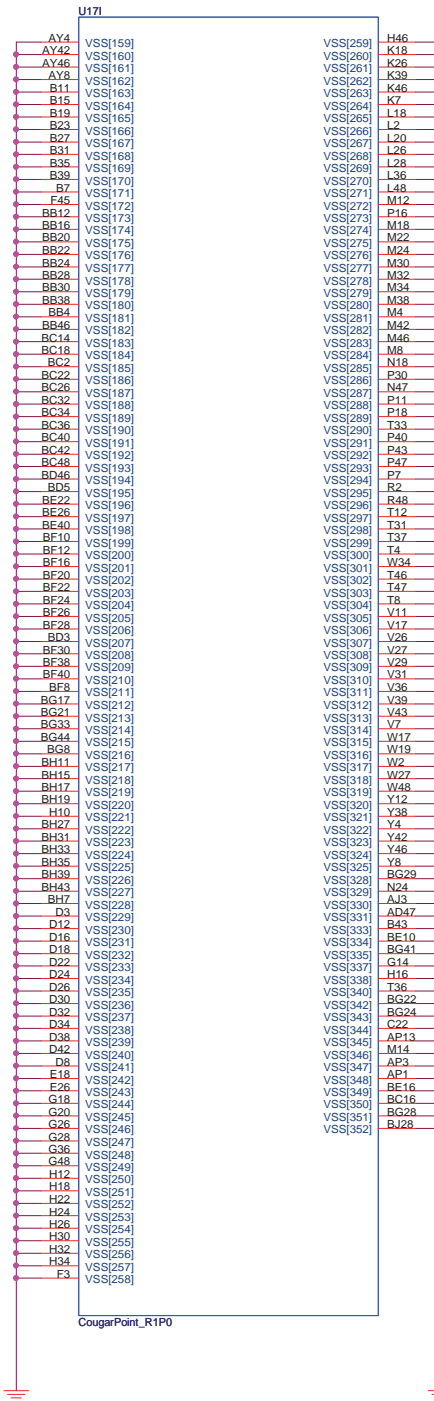
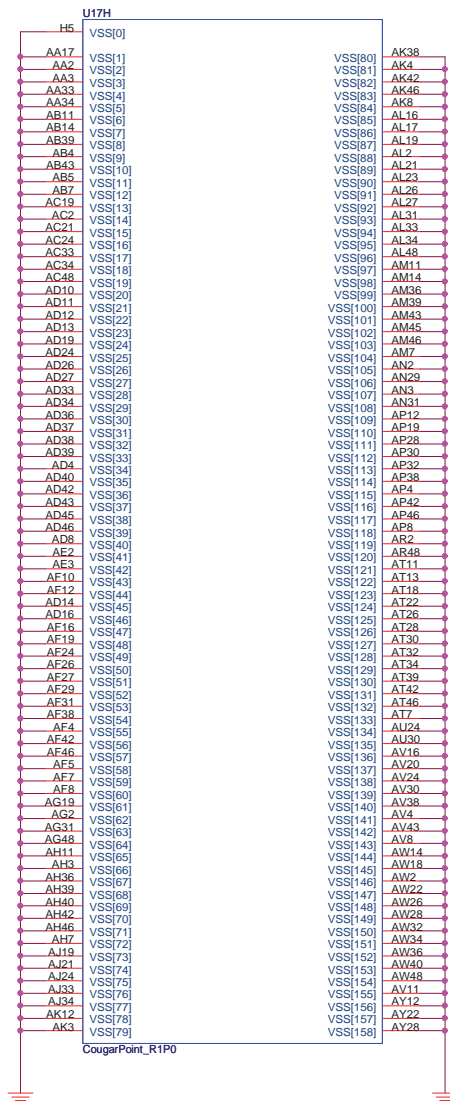
COUGAR POINT (POWER)



Cougar Point-M (POWER)



IBEX PEAK-M (GND)

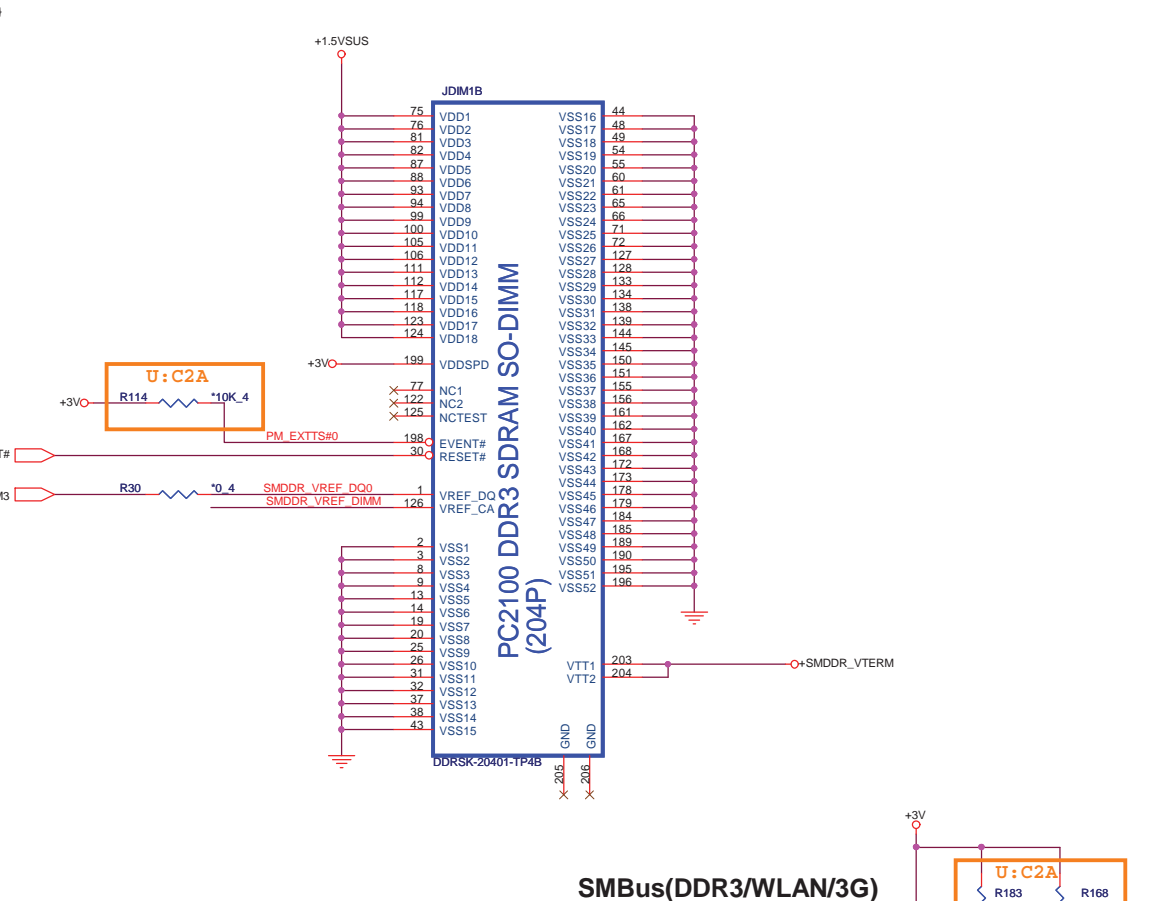
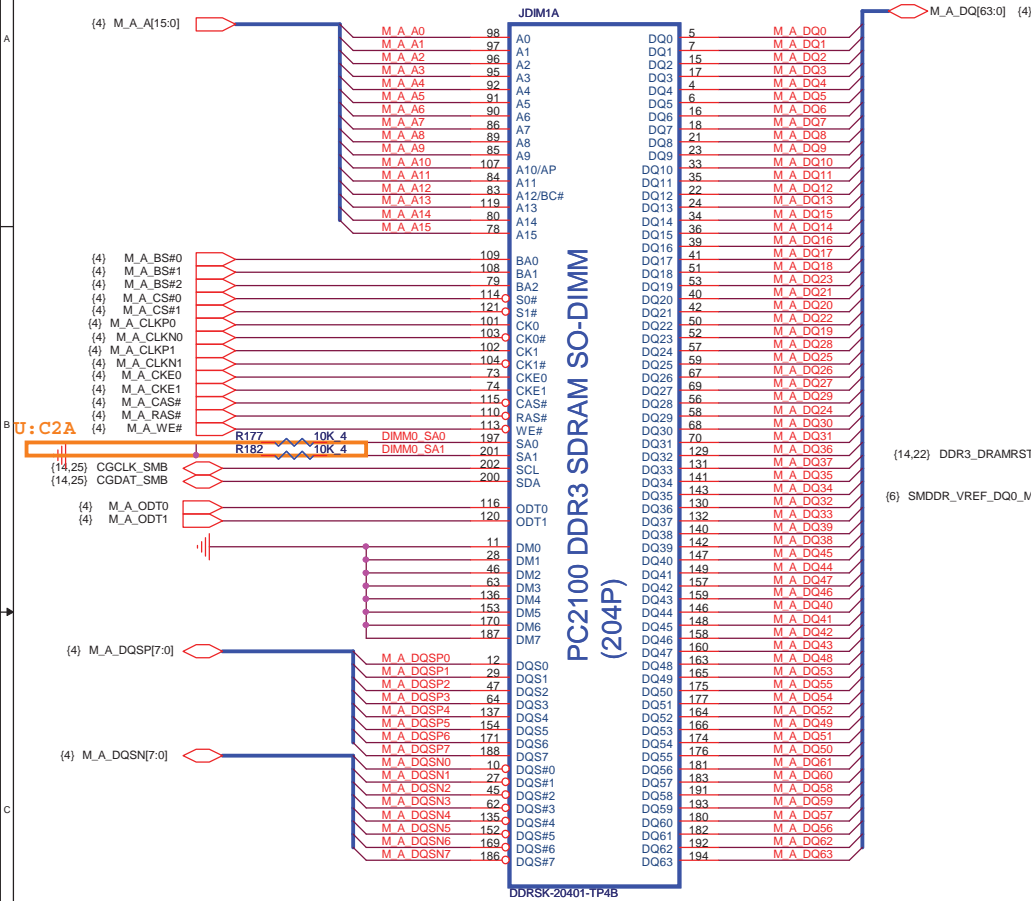


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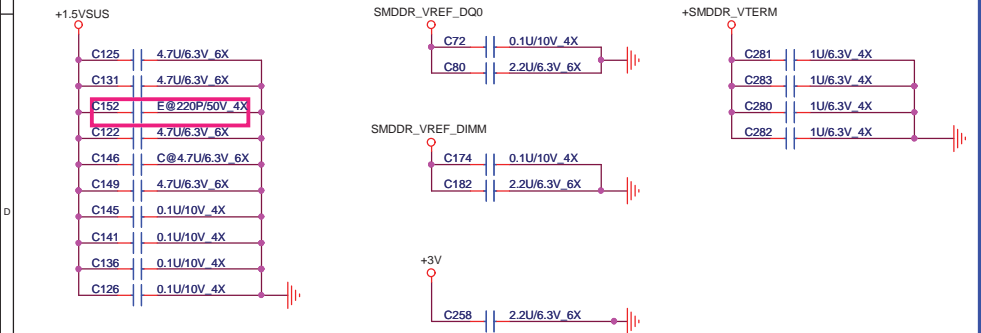
PROJECT : TE5

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	Cougar Point 6/6	1A
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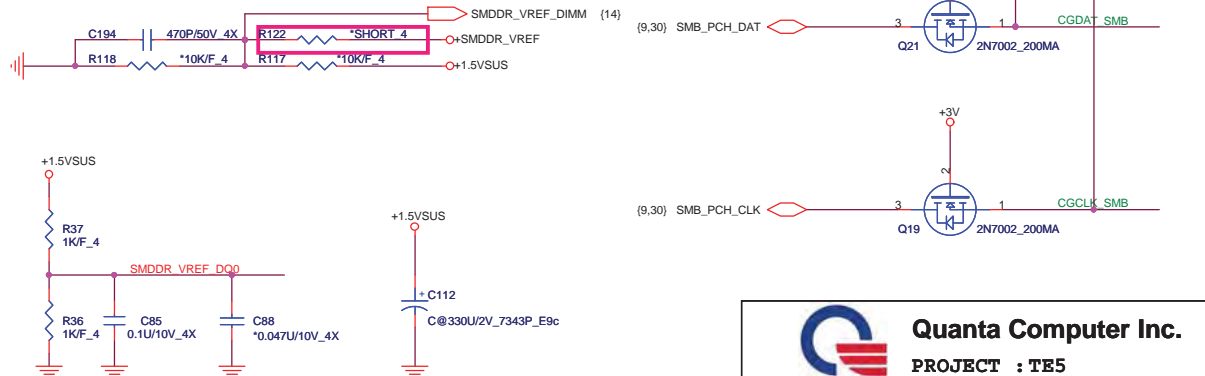
<DDR>

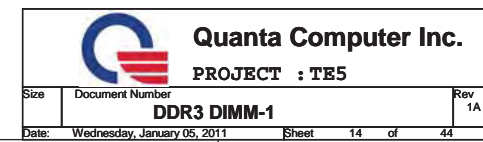


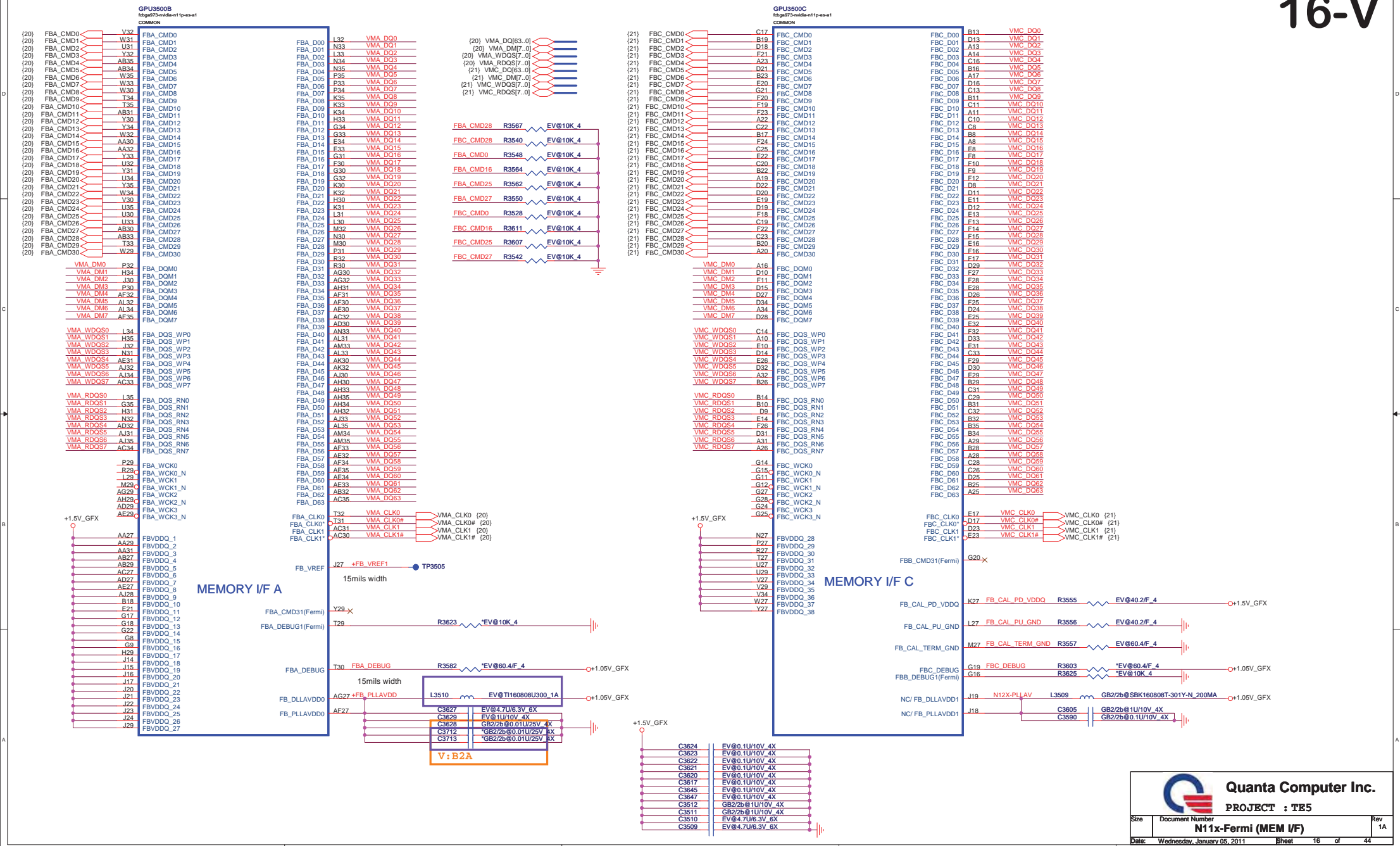
<DDR>



<DDR>

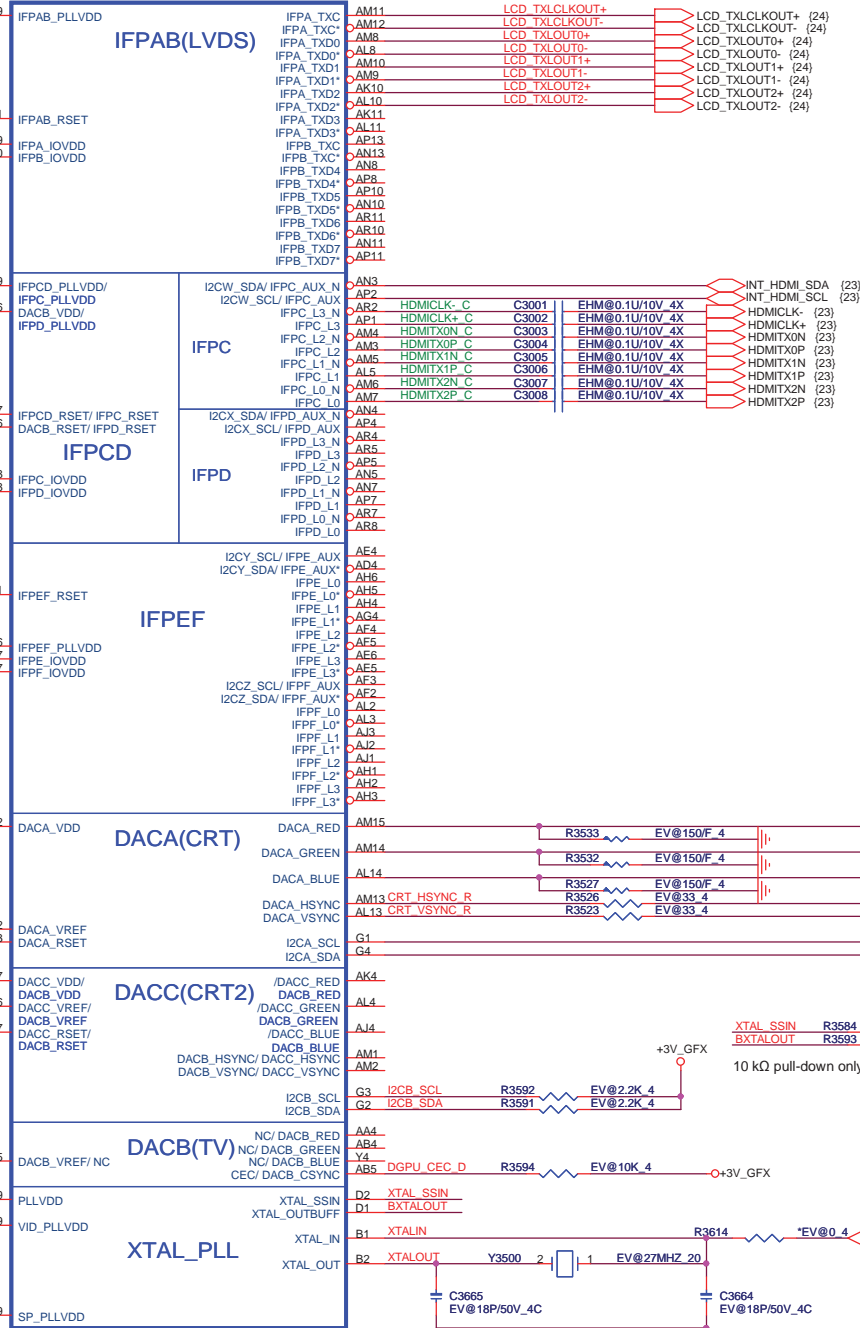
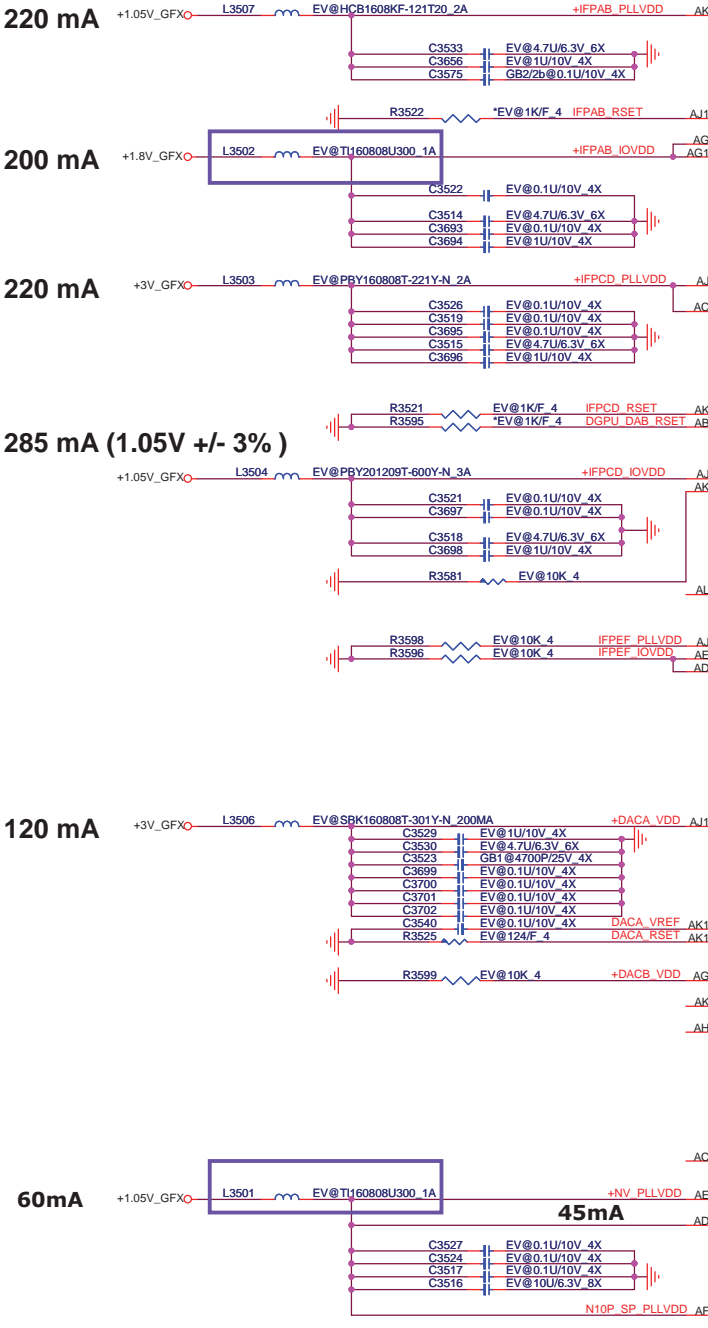






17-V

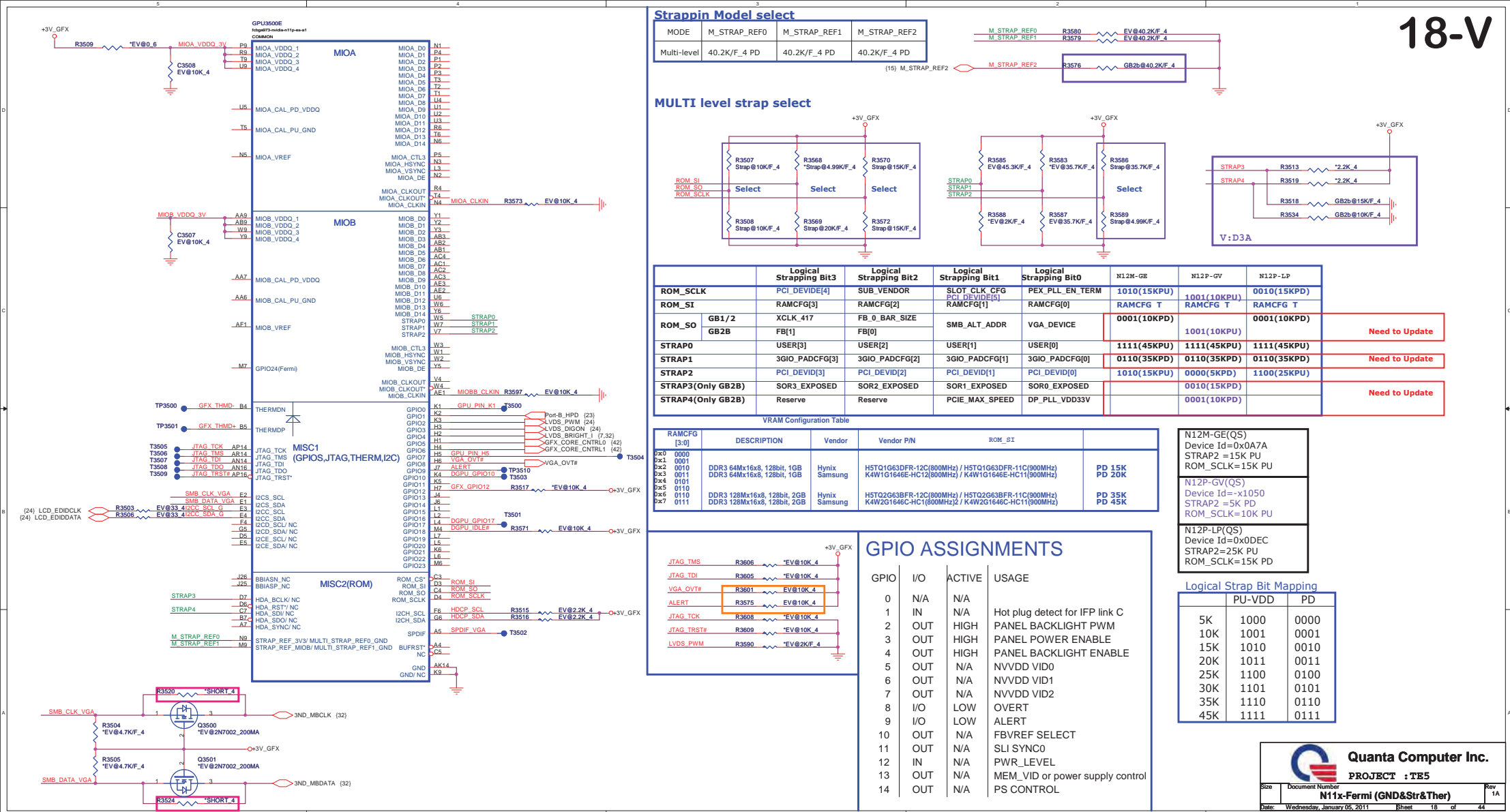
GPU3500D
fcbg973-nvidia-n1 1p-es-a1
COMMON



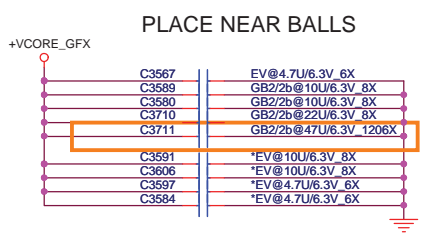
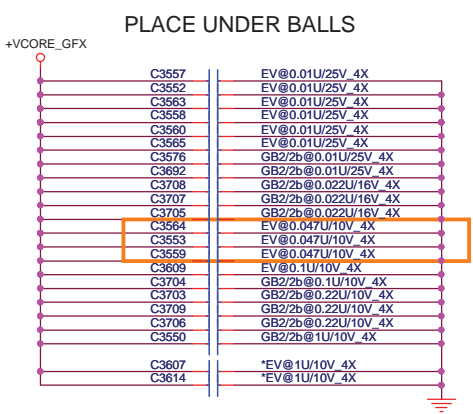
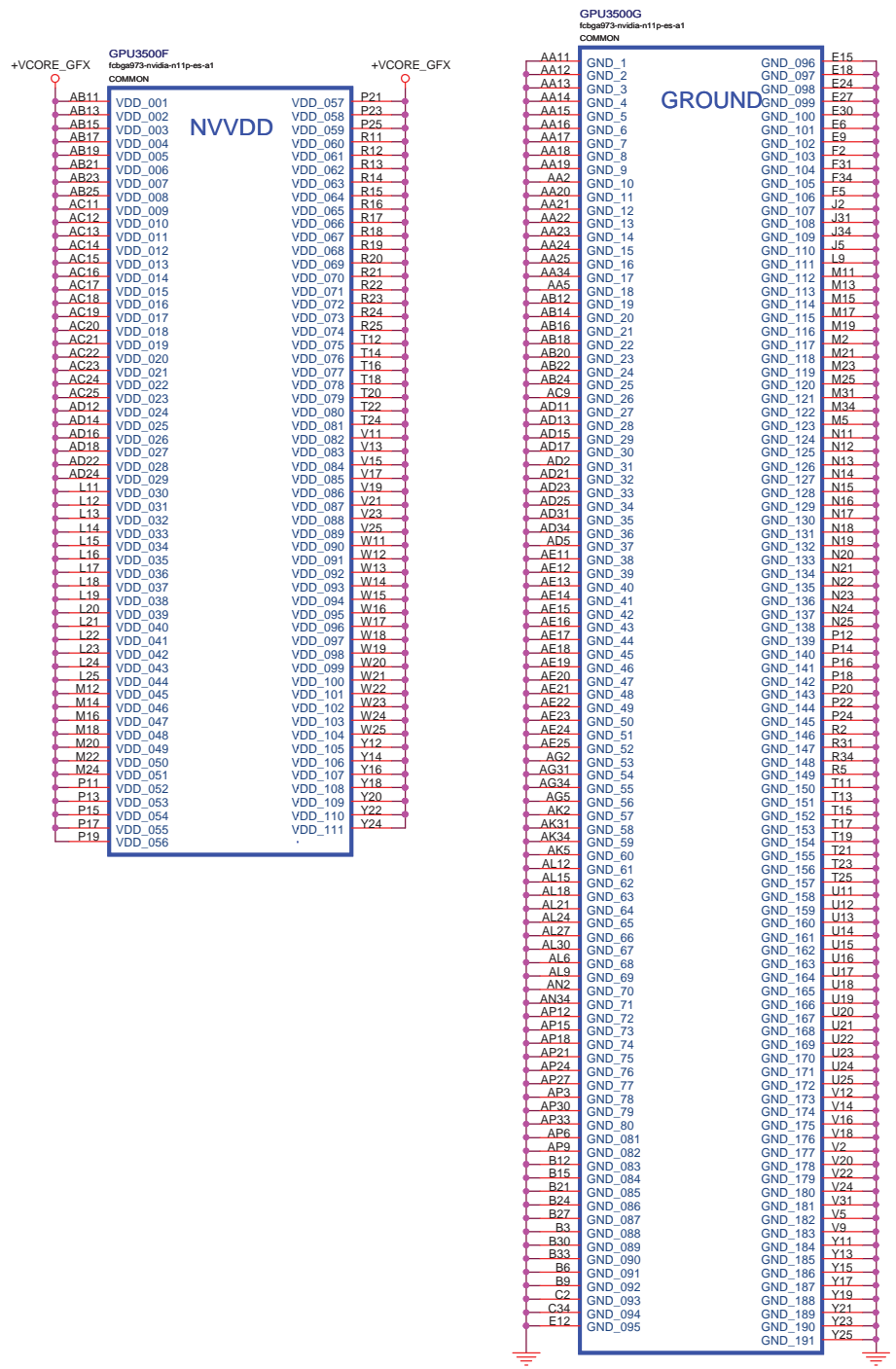
STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED


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	N11x-Fermi (DISPLAY)	1A
Date:	Wednesday, January 05, 2011	Sheet 17 of 44



19-V

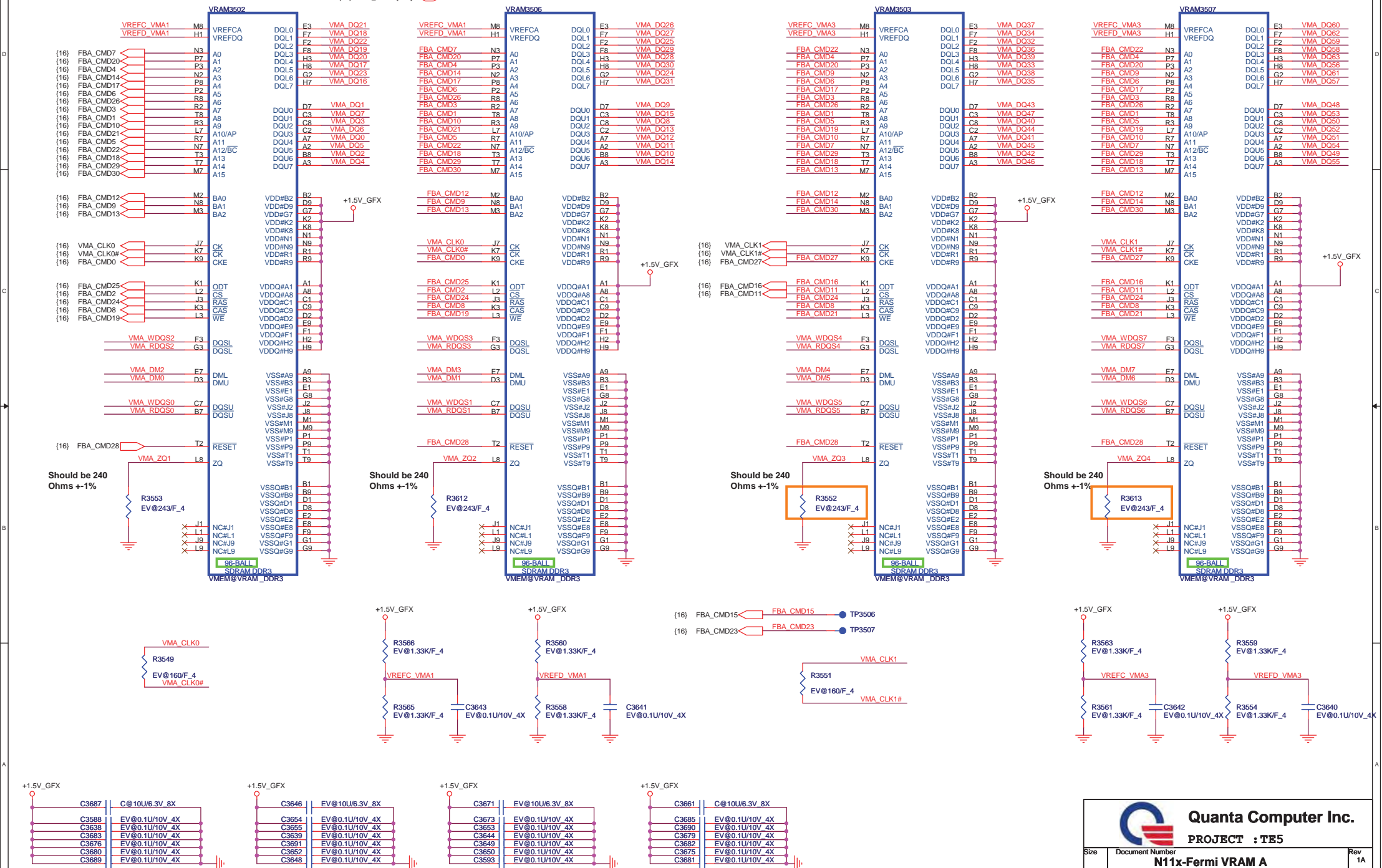




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PROJECT : TE5

Size	Document Number	Rev
	N11x-Fermi (GND/Power)	1A
Date:	Wednesday, January 05, 2011	Sheet 19 of 44

CHANNEL A: 256MB/512MB DDR3

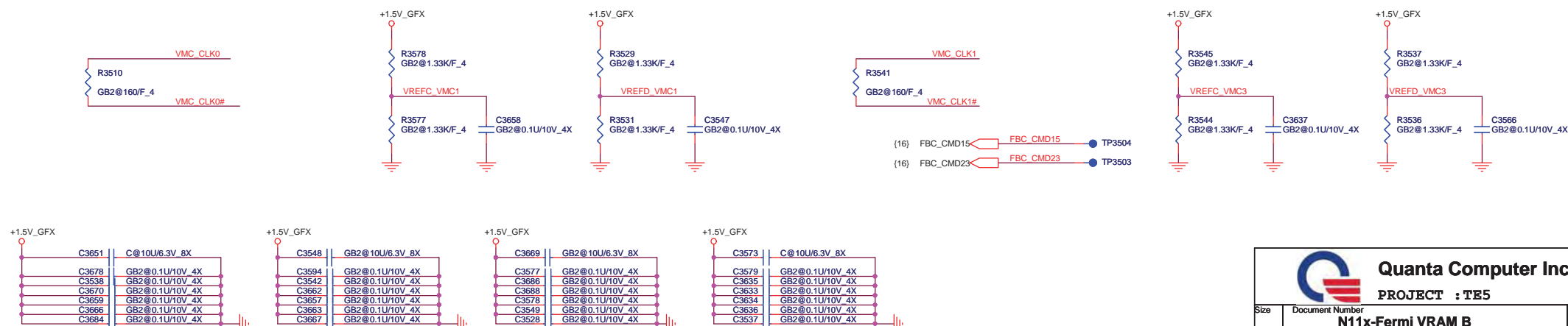
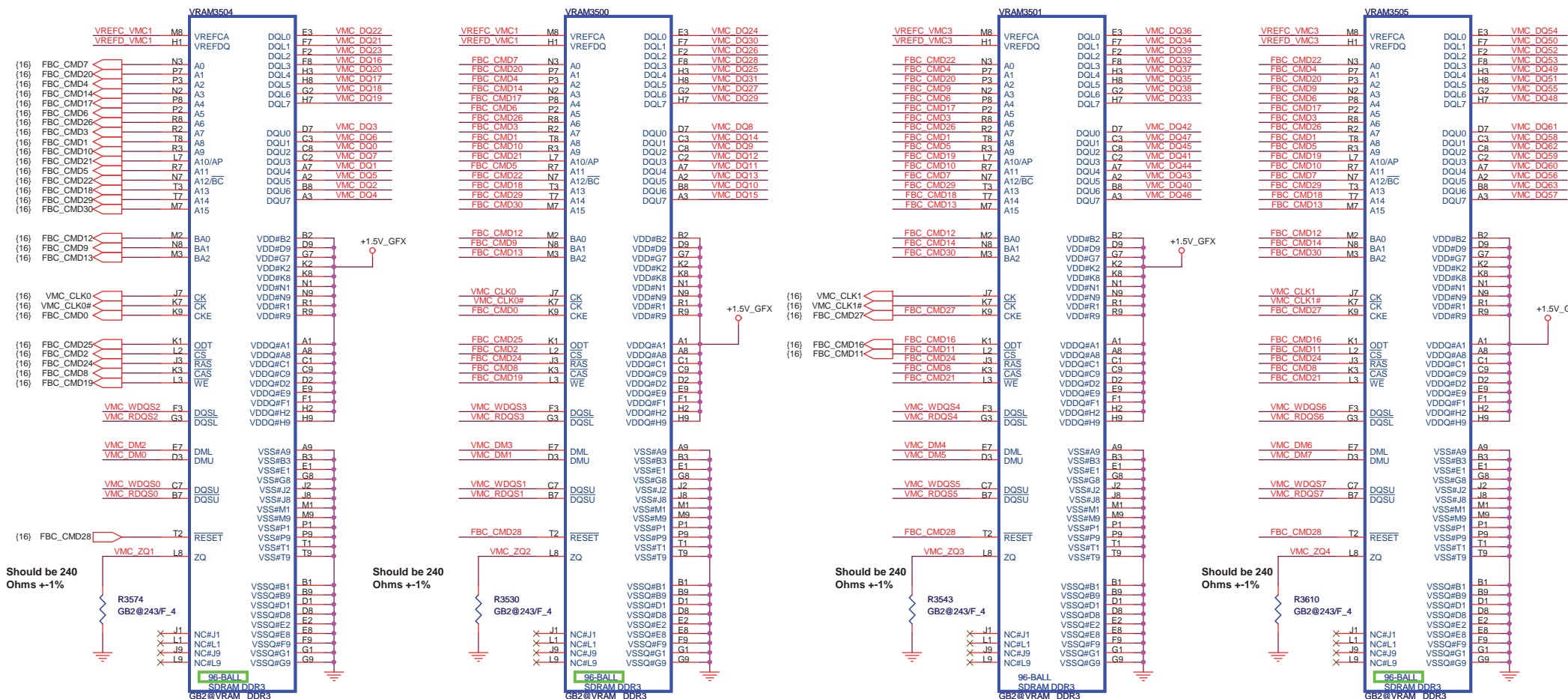


CHANNEL B: 256MB/512MB DDR3

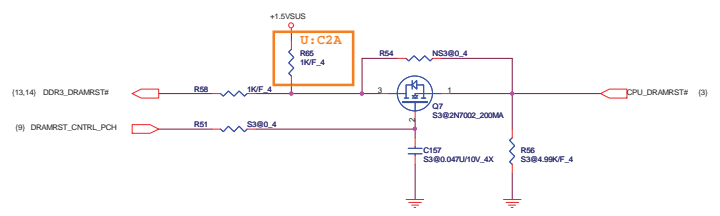
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{16} VMC_DQ[63..0]
{16} VMC_DM[7..0]
{16} VMC_WDQS[7..0]
{16} VMC_RDQS[7..0]

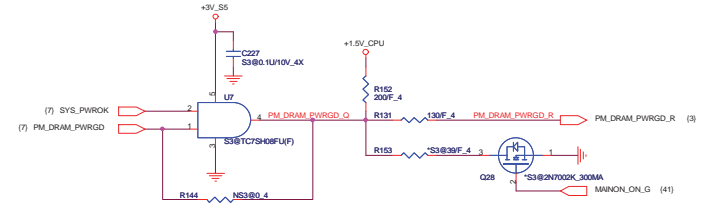
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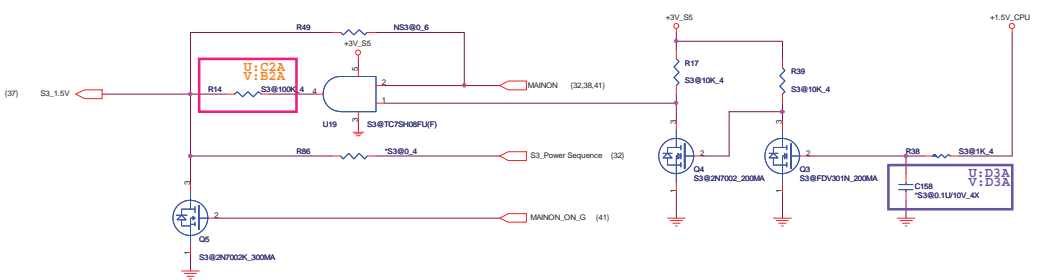
S3 power Reduction (SM_DRAMRST#) <S3P> <4>



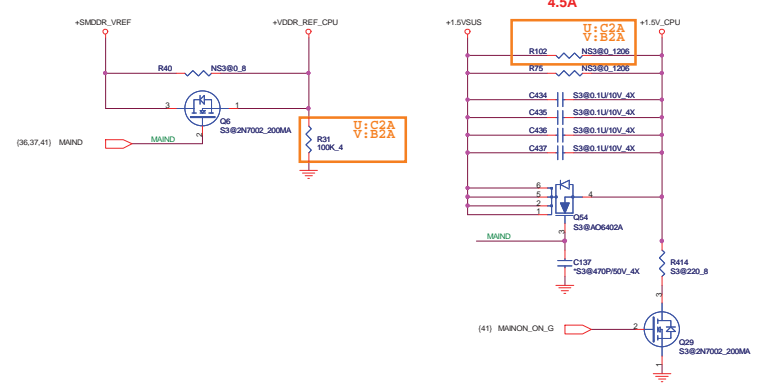
S3 power Reduction (SM_DRAMPWRK) <S3P> <3>



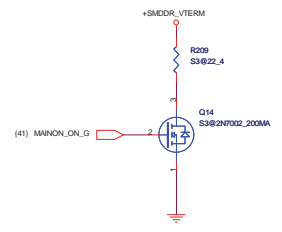
For S3 power Reduction Sequence <S3P> <3>



S3 power Reduction (CPU Power) <S3P> <5>

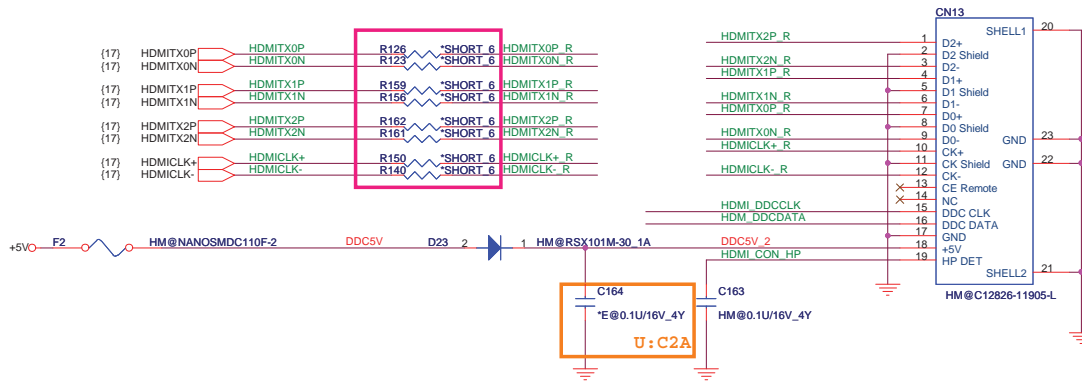


For S3 power Reduction VTT discharge <S3P> <13>

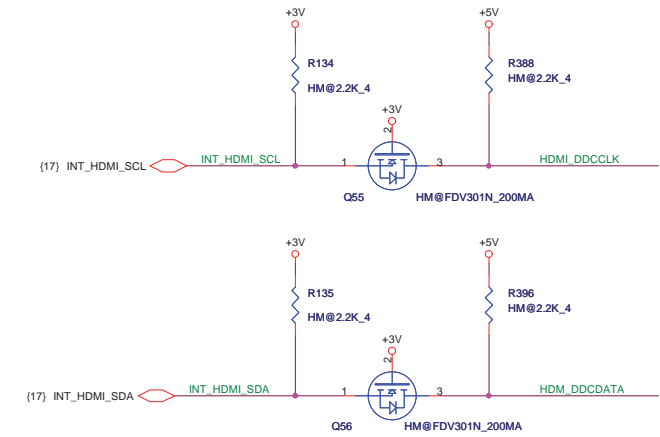


HDMI Conn [HDM]

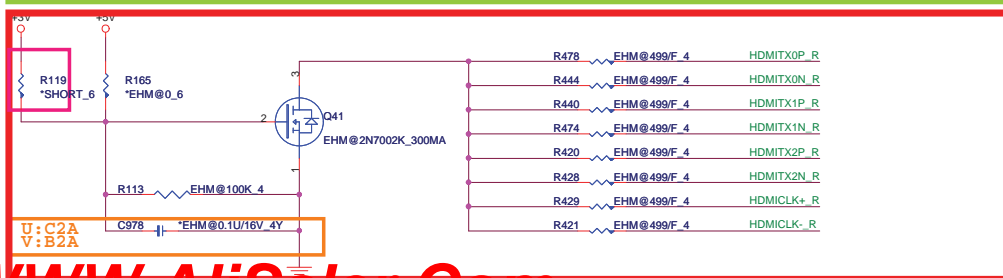
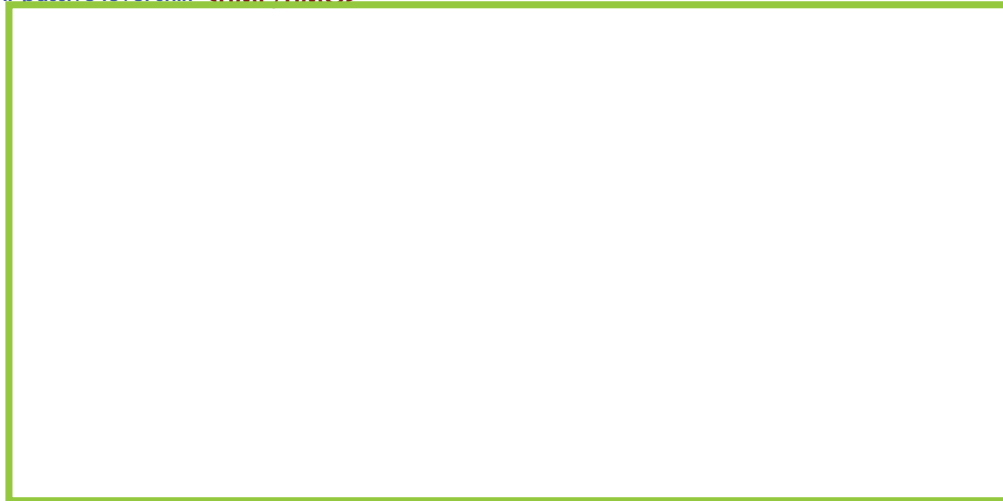
HDMI-CONN <HDM>



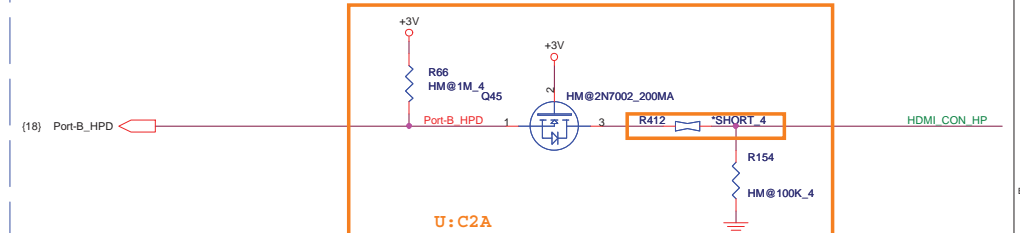
HDMI-SMBus <HDM>

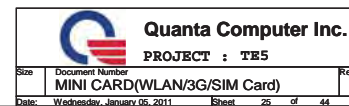


HDMI-passive level shift <HMP/HMG>

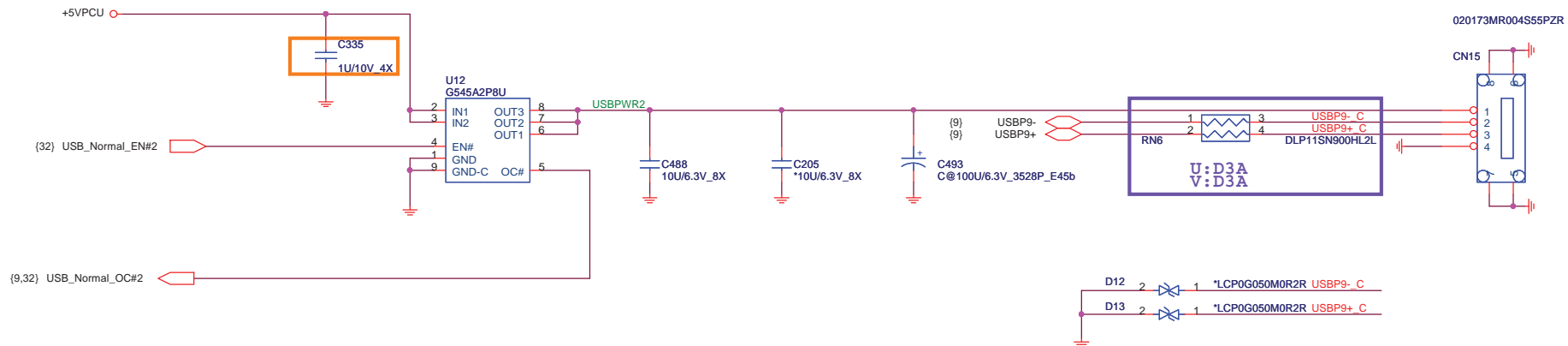


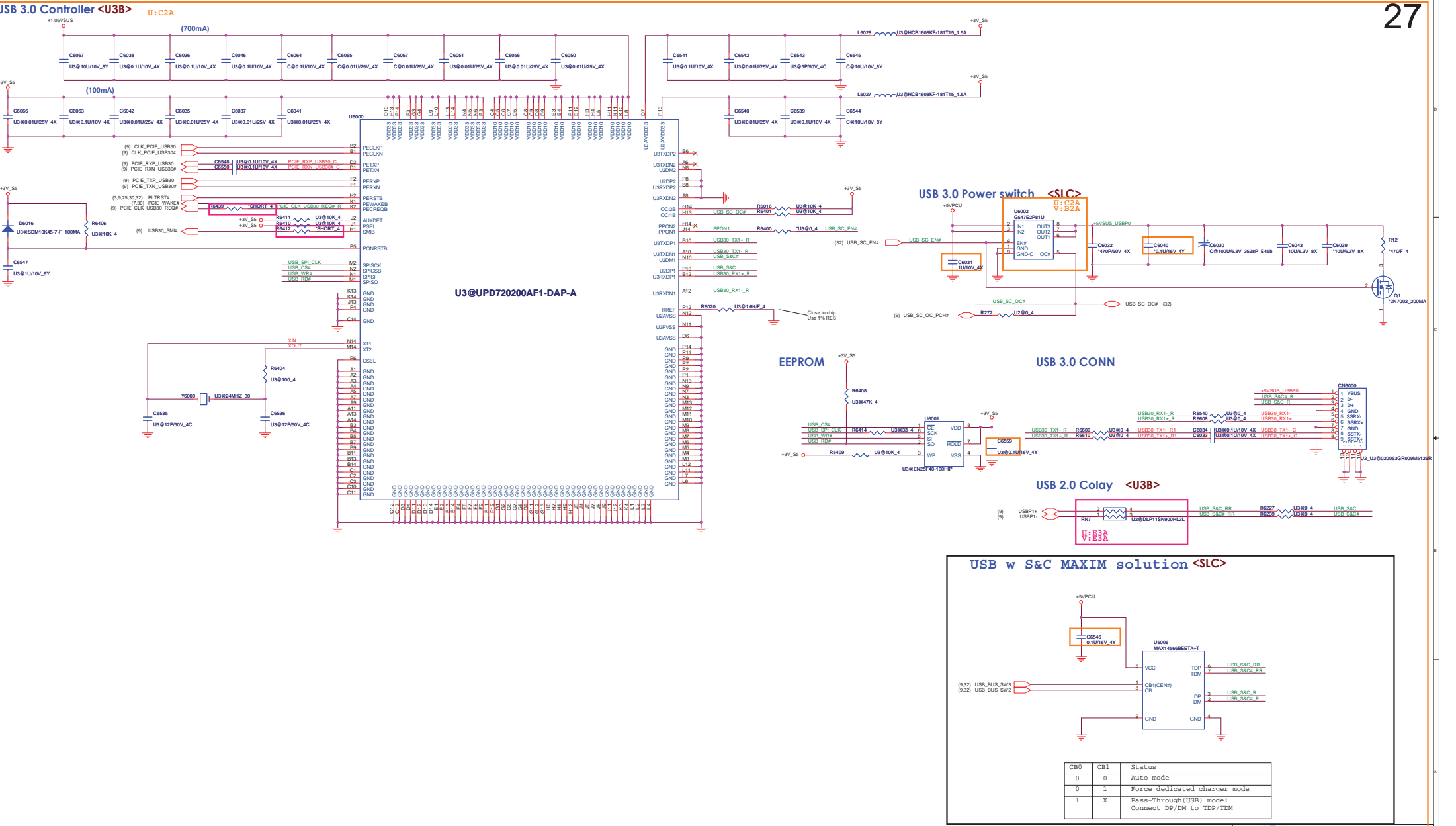
HDMI-HPD <HMP/HMG>





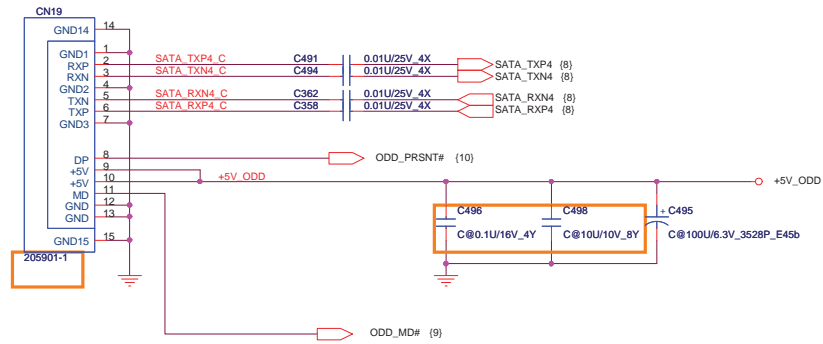
USB2.0 MB SIDE (Left) <USB>



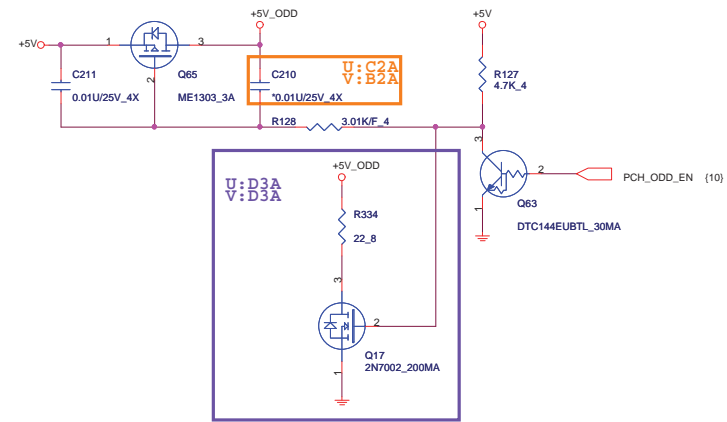


SATA ODD

[ODD]



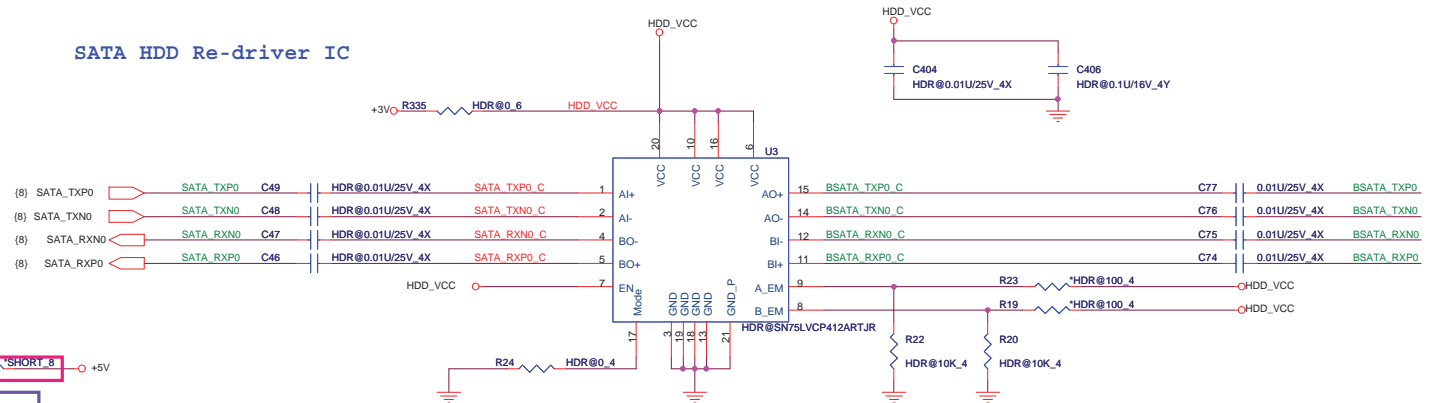
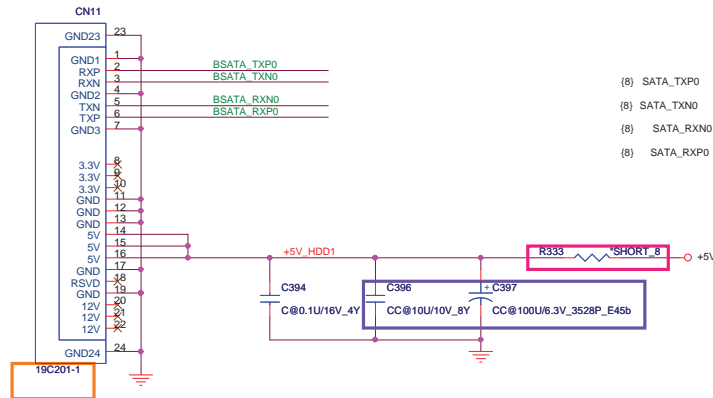
ODD Zero power . (Only for Intel) <OZP>



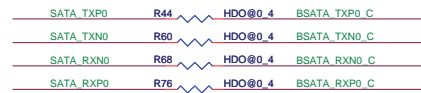
SATA HDD

[HDD]

SATA HDD Re-driver IC



Colay with Redriver IC



SATA Re-driver Bypass

Quanta Computer Inc.
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HDD/ODD/MDC

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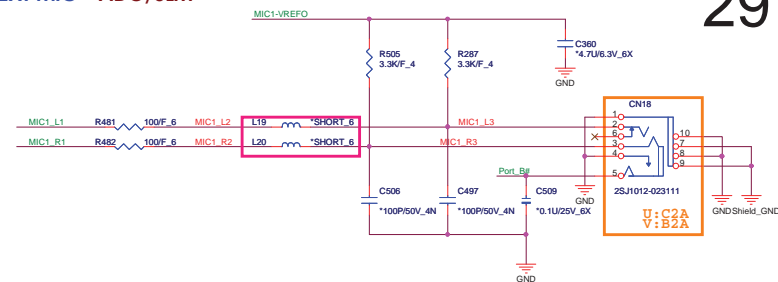
[illegible]

Figure 10 shows the pin connections for the 8206-04001-06 component. The connections are as follows:

- SPK+R is connected to R61.
- SPK-R is connected to R62.
- SPK+L is connected to R63.
- SPK-L is connected to R64.
- R61, R62, R63, and R64 are connected to 0.1F 8 capacitors.
- The capacitors are connected to INSPKR+N, INSPKR-N, INSPKL+N, and INSPKL-N.
- INSPKL+N is connected to C119.
- INSPKL-N is connected to C120.
- INSPKR-N is connected to C118.
- INSPKR-N is connected to C117.
- All capacitors are connected to E@1000P/50V_4X and GND.
- The 8206-04001-06 component is shown on the right.

The schematic diagram illustrates the connection between a Raspberry Pi 3B+ and the MDC88023-12101 module. The Raspberry Pi 3B+ is shown on the left with its pins labeled: 1 (5V), 2 (5V), 3 (GND), 4 (5V), 5 (GND), 6 (5V), 7 (GND), 8 (5V), 9 (GND), 10 (5V), 11 (GND), 12 (5V), 13 (GND), 14 (5V), 15 (GND), 16 (5V), 17 (GND), 18 (5V), 19 (GND), 20 (5V), 21 (GND), 22 (5V), 23 (GND), 24 (5V), 25 (GND), 26 (5V), 27 (GND), 28 (5V), 29 (GND), 30 (5V), 31 (GND), 32 (5V), 33 (GND), 34 (5V), 35 (GND), 36 (5V), 37 (GND), 38 (5V), 39 (GND), 40 (5V), 41 (GND), 42 (5V), 43 (GND), 44 (5V), 45 (GND), 46 (5V), 47 (GND), 48 (5V), 49 (GND), 50 (5V), 51 (GND), 52 (5V), 53 (GND), 54 (5V), 55 (GND), 56 (5V), 57 (GND), 58 (5V), 59 (GND), 60 (5V), 61 (GND), 62 (5V), 63 (GND), 64 (5V), 65 (GND), 66 (5V), 67 (GND), 68 (5V), 69 (GND), 70 (5V), 71 (GND), 72 (5V), 73 (GND), 74 (5V), 75 (GND), 76 (5V), 77 (GND), 78 (5V), 79 (GND), 80 (5V), 81 (GND), 82 (5V), 83 (GND), 84 (5V), 85 (GND), 86 (5V), 87 (GND), 88 (5V), 89 (GND), 90 (5V), 91 (GND), 92 (5V), 93 (GND), 94 (5V), 95 (GND), 96 (5V), 97 (GND), 98 (5V), 99 (GND), 100 (5V).

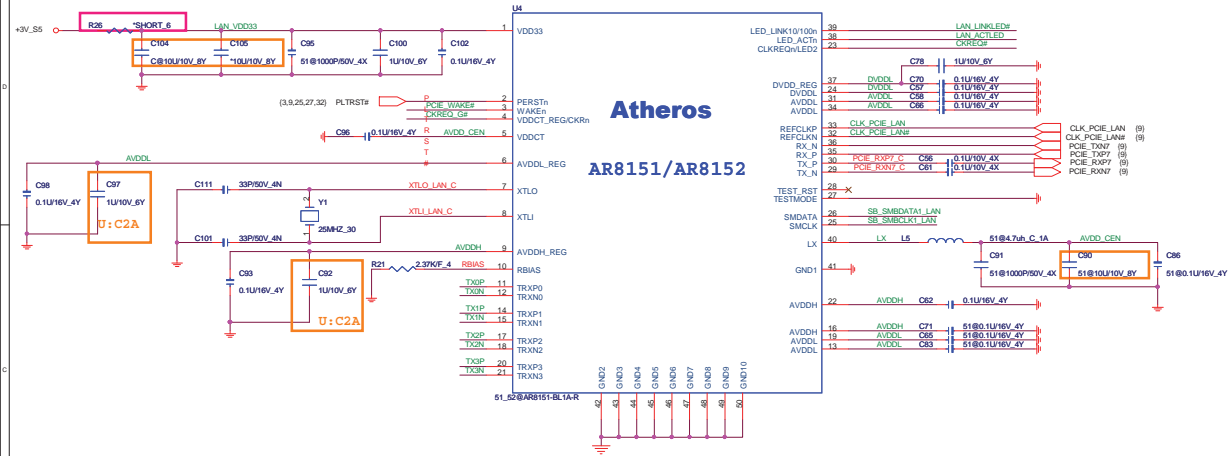
The MDC88023-12101 module is shown on the right with its pins labeled: 1 (SB, GPIO7), 2 (+3V), 3 (SB, GPIO27), 4 (GND), 5 (FM, INT), 6 (AGND), 7 (DIB_P), 8 (FM_L), 9 (DIB_N), 10 (FM_R), 11 (FM_DET#), 12 (AGND).

The connections are as follows:

- Raspberry Pi 3B+ Pin 1 (5V) to MDC88023-12101 Pin 2 (+3V)
- Raspberry Pi 3B+ Pin 3 (GND) to MDC88023-12101 Pin 4 (GND)
- Raspberry Pi 3B+ Pin 5 (GND) to MDC88023-12101 Pin 6 (AGND)
- Raspberry Pi 3B+ Pin 7 (GND) to MDC88023-12101 Pin 8 (FM_L)
- Raspberry Pi 3B+ Pin 9 (GND) to MDC88023-12101 Pin 10 (FM_R)
- Raspberry Pi 3B+ Pin 11 (GND) to MDC88023-12101 Pin 12 (AGND)
- Raspberry Pi 3B+ Pin 13 (GND) to MDC88023-12101 Pin 1 (SB, GPIO7)
- Raspberry Pi 3B+ Pin 15 (GND) to MDC88023-12101 Pin 3 (SB, GPIO27)
- Raspberry Pi 3B+ Pin 17 (GND) to MDC88023-12101 Pin 5 (FM, INT)
- Raspberry Pi 3B+ Pin 19 (GND) to MDC88023-12101 Pin 7 (DIB_P)
- Raspberry Pi 3B+ Pin 21 (GND) to MDC88023-12101 Pin 9 (DIB_N)
- Raspberry Pi 3B+ Pin 23 (GND) to MDC88023-12101 Pin 11 (FM_DET#)

The MDC88023-12101 module is also connected to a 5V supply and ground through capacitors C32 and C30, both labeled E@150P/50V_4N.

Atheros Lan <LAN/LN1/LNG>



LAN-Wake up function <LAN>

PCIE_WAKE# → PCIE_WAKE# (7,27)

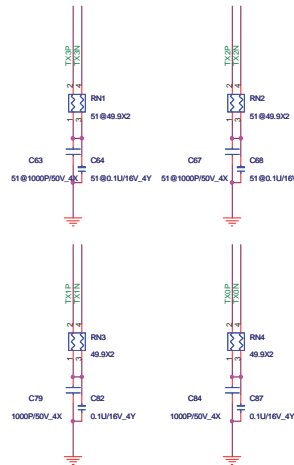
LAN-SM-Bus <LAN>

SB_SMBDATA1_LAN R16 0.4 SMB_PCH_DAT (8,13)

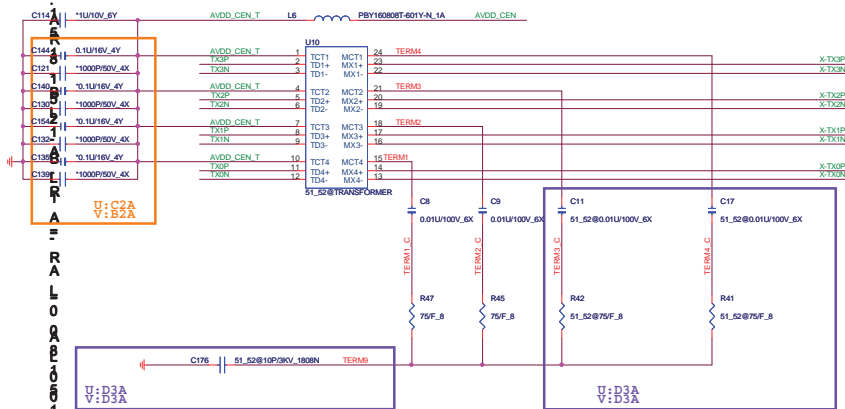
SB_SMBCLK1_LAN R18 0.4 SMB_PCH_CLK (8,13)

LAN-terminator <LAN/LN1/LNG>

PLACE NEAR LAN IC SIDE



LAN-Transformer <LAN/LN1/LNG>

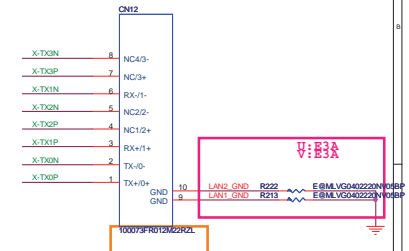


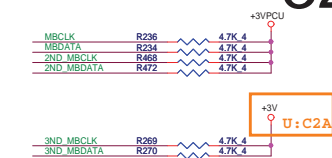
LAN-Strap function <LAN/LN1/LNG>



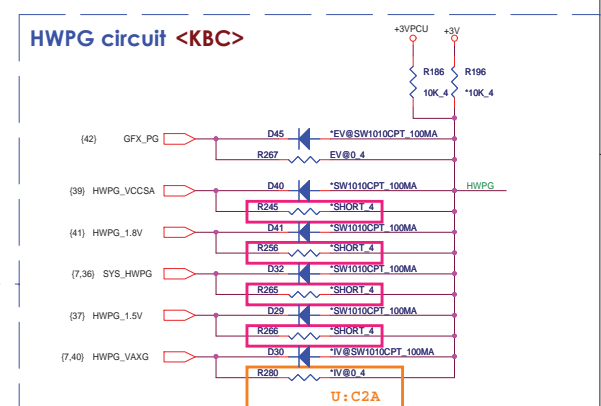
LSD0 = LAN_ACTLED#	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LSD1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

LAN (RJ45) -CONN Interface <LAN>



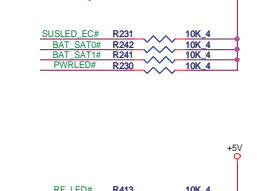


HWPG circuit <KBC>

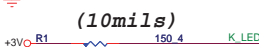
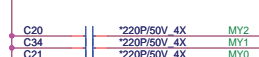
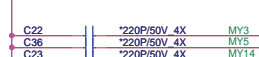
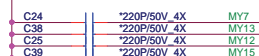
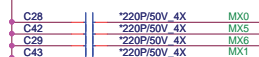
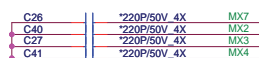


MS Strap	SKU_STRAP_1	SKU_STRAP_2	SKU_STRAP_3
13" UMA	0	0	0
13" DIS	0	0	1
14" UMA	0	1	0
14" DIS	0	1	1
15" UMA	1	0	0
15" DIS	1	0	1

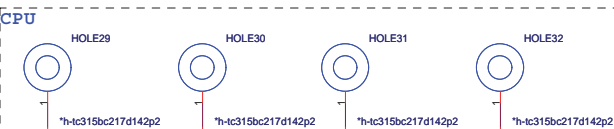
LED PU/PD <LED>



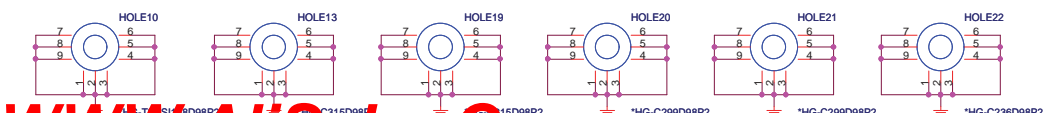
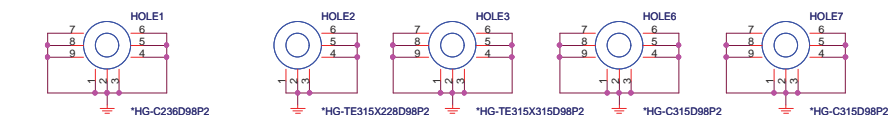
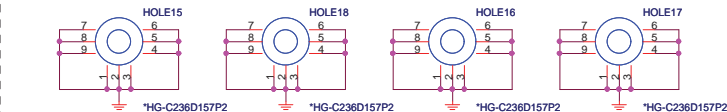
INT KeyBoard <KBC>



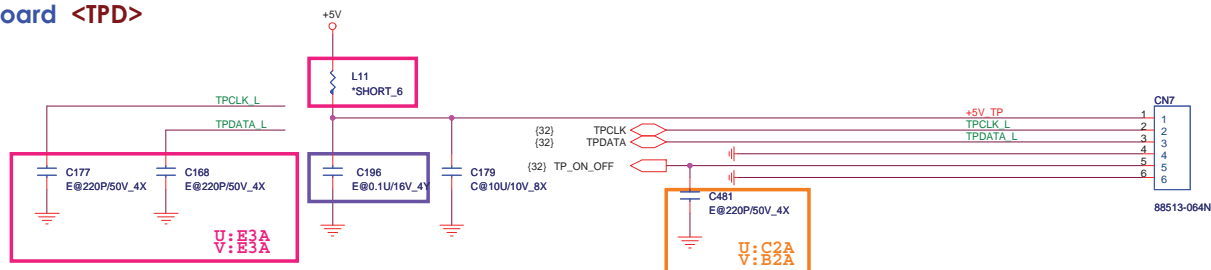
HOLE



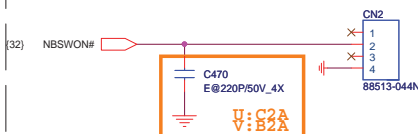
MINI CARD



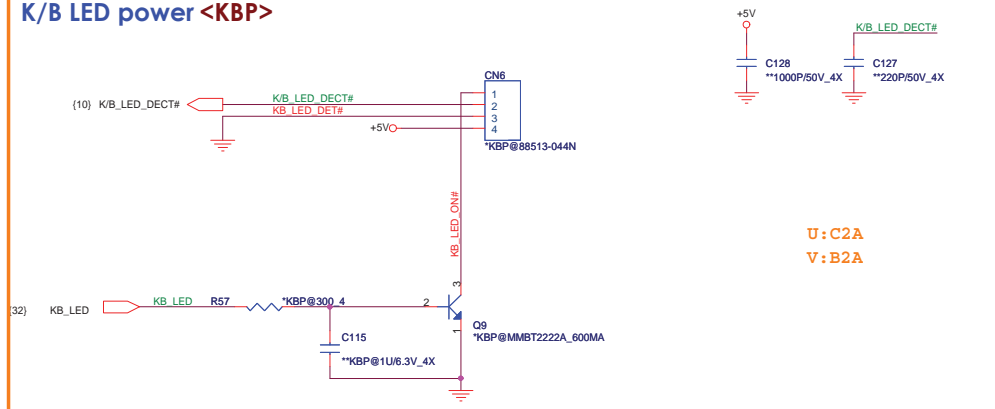
TP board <TPD>



Power board <PSW>



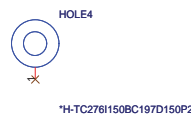
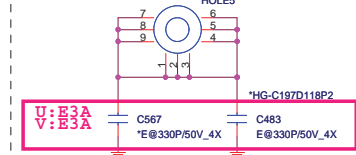
K/B LED power <KBP>



HDD&ODD



MDC



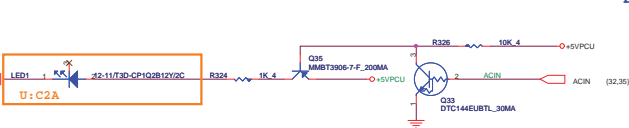
Quanta Computer Inc.

PROJECT : TE5

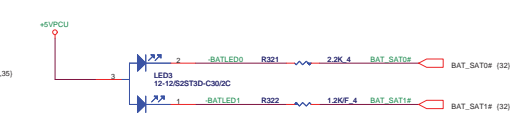
Size	Document Number	Rev
	KB/TP&TP/PB/FL/LEB/MMB/B-CAS	1A
Date:	Wednesday, January 05, 2011	Sheet 33 of 44

LED <LED>

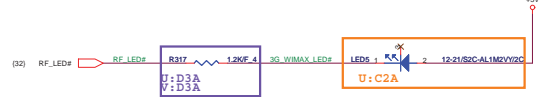
AC-IN



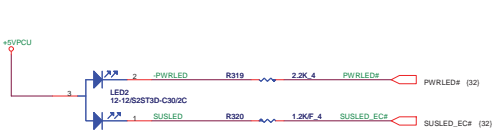
BATTERY



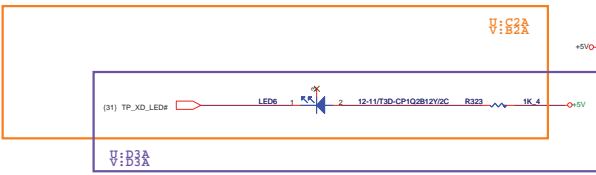
RF LED



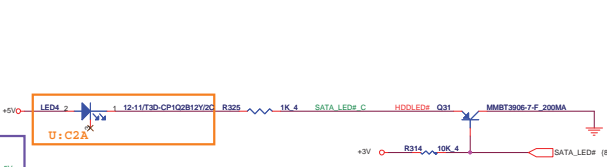
POWER



CARDREADER



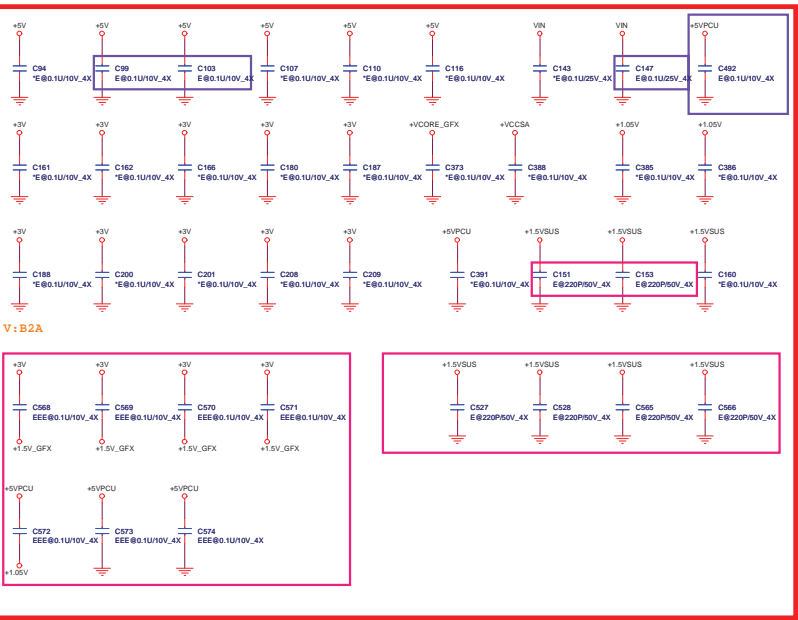
HDD/ODD



ESD Protect



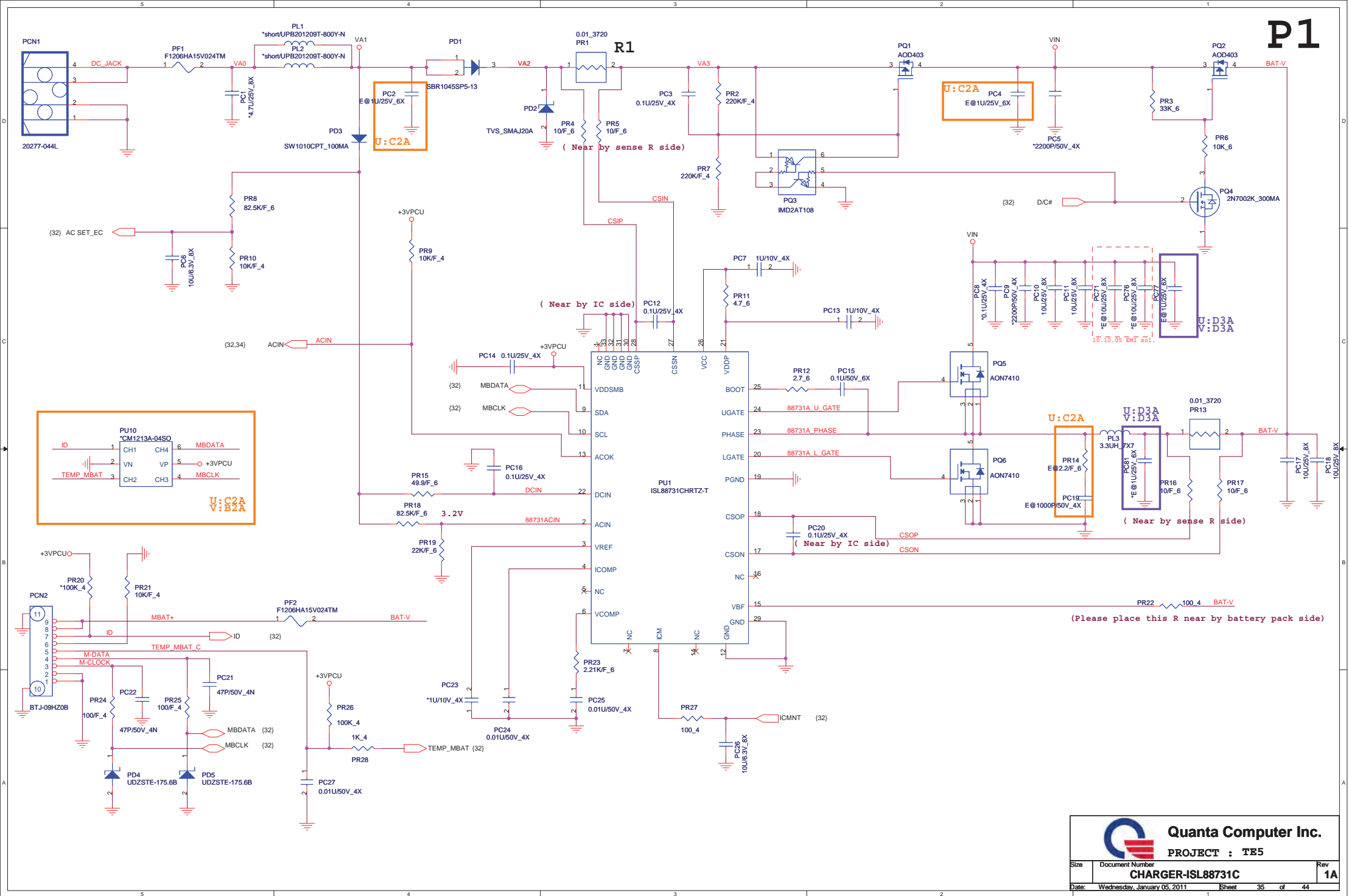
EMI



EMI PAD



WWW.AliSaler.Com

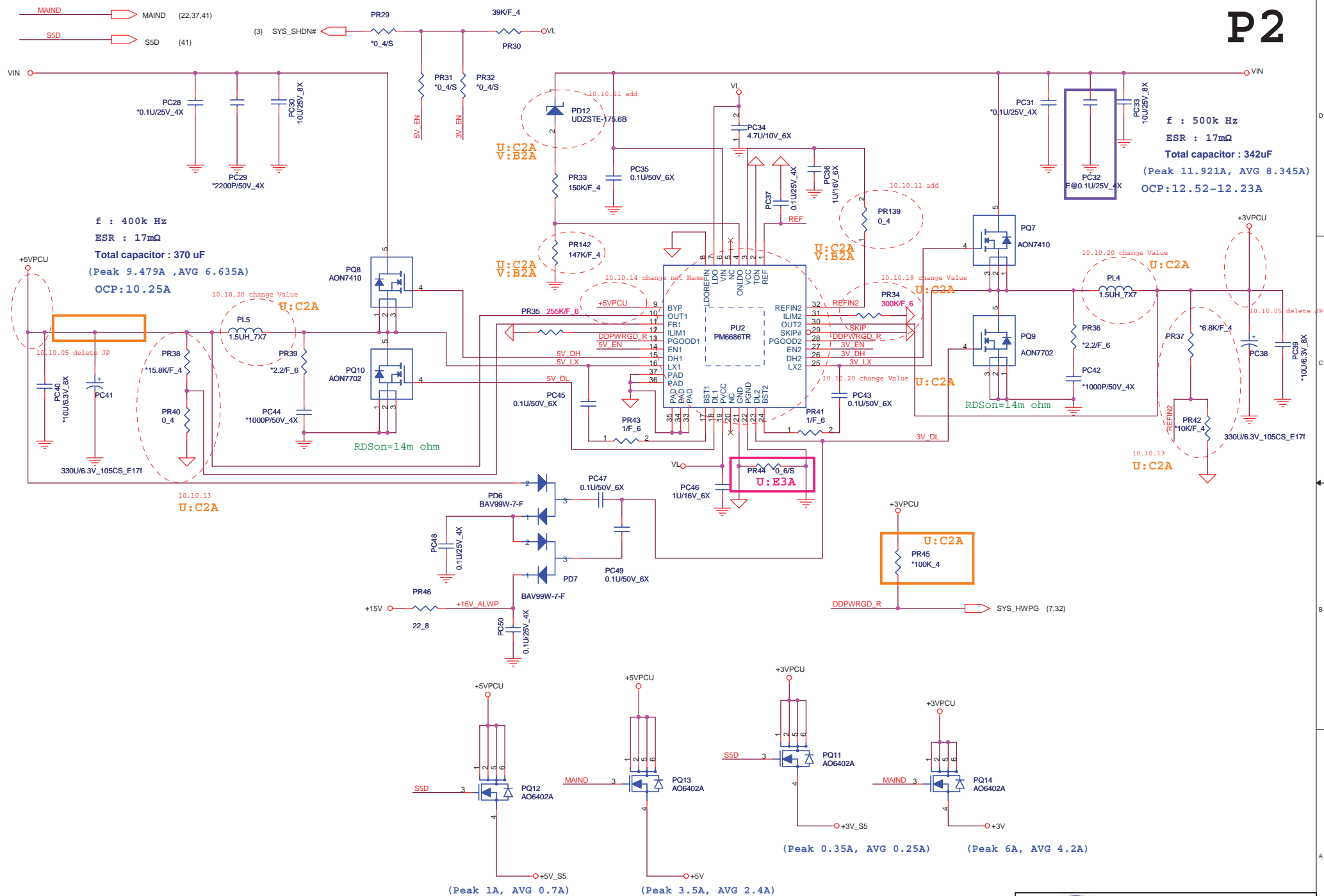


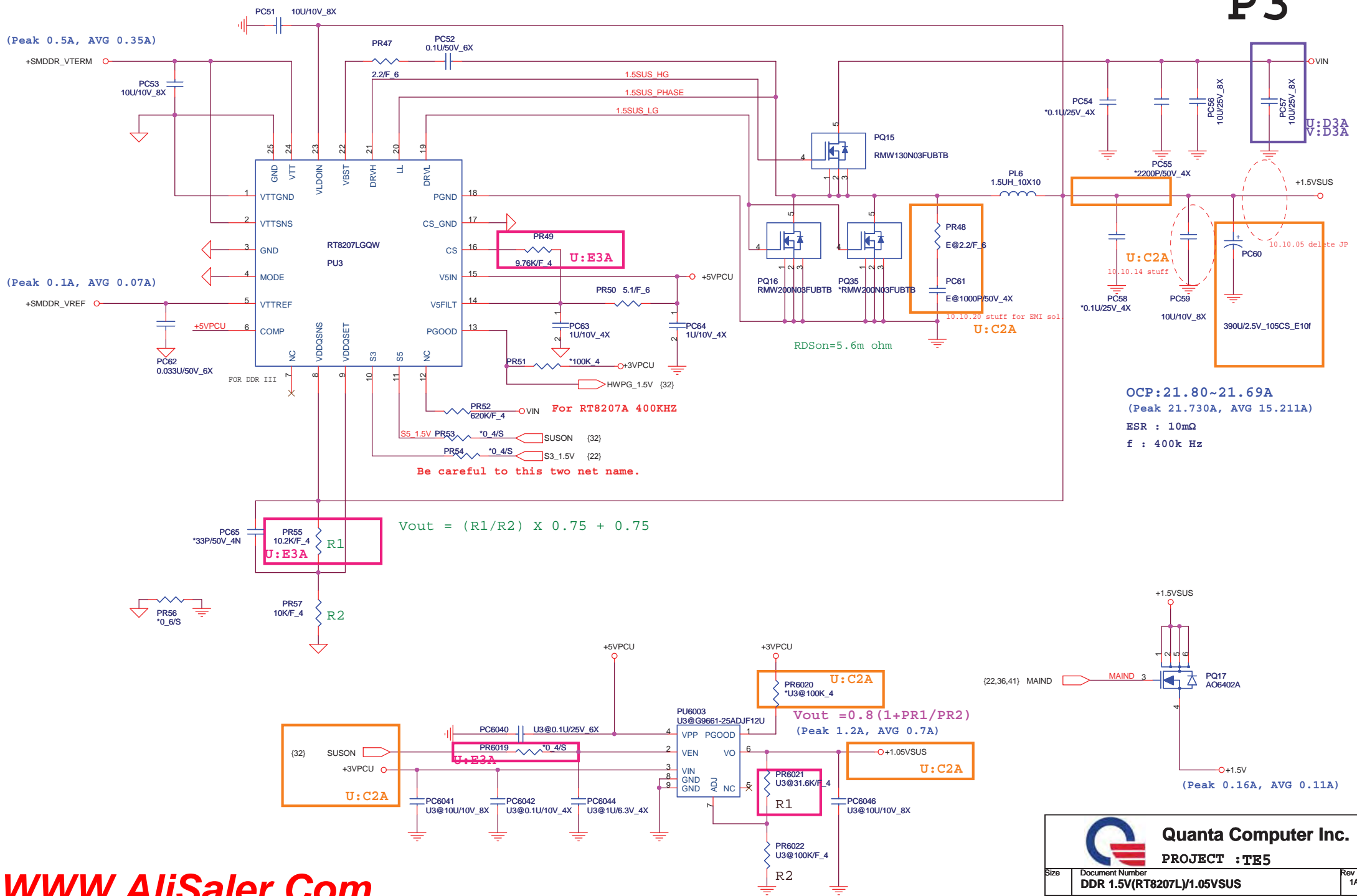
Quanta Computer Inc.

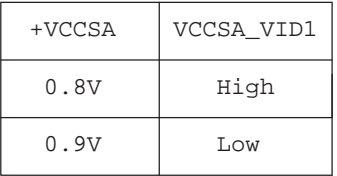
PROJECT : TE5

Size	Document Number	Rev
	CHARGER-ISL88731C	1A
Date:	Wednesday, January 05, 2011	Sheet 35 of 44

P2

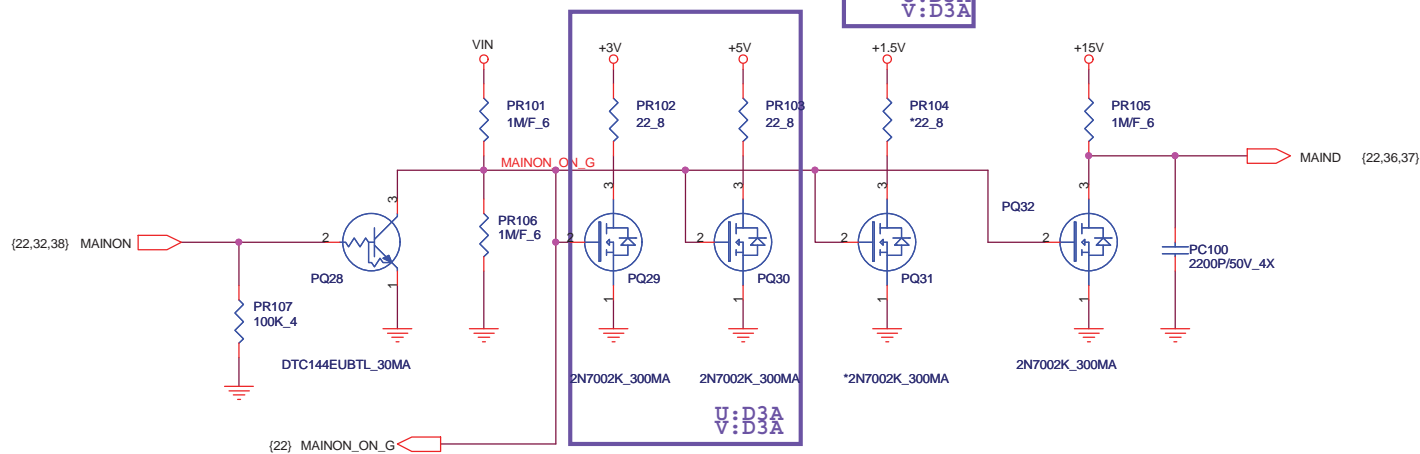
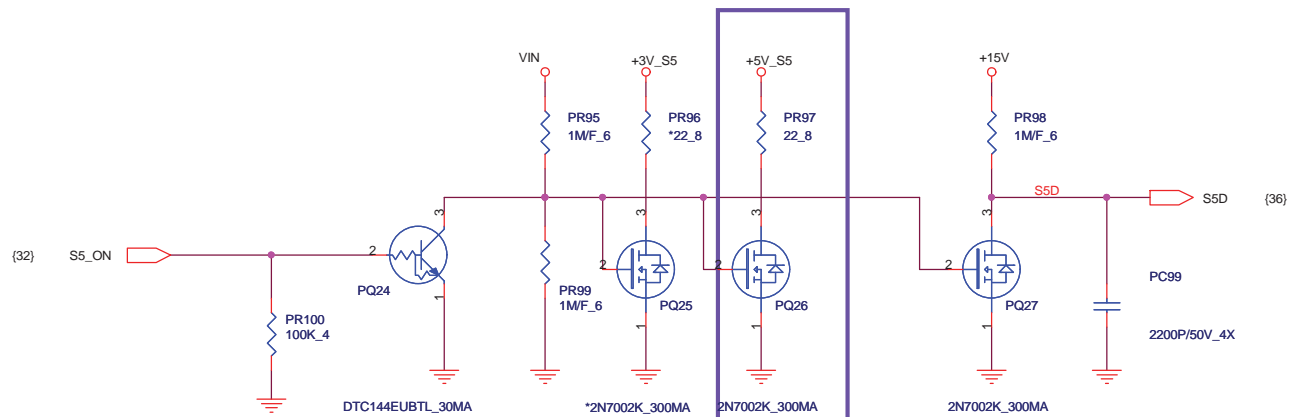
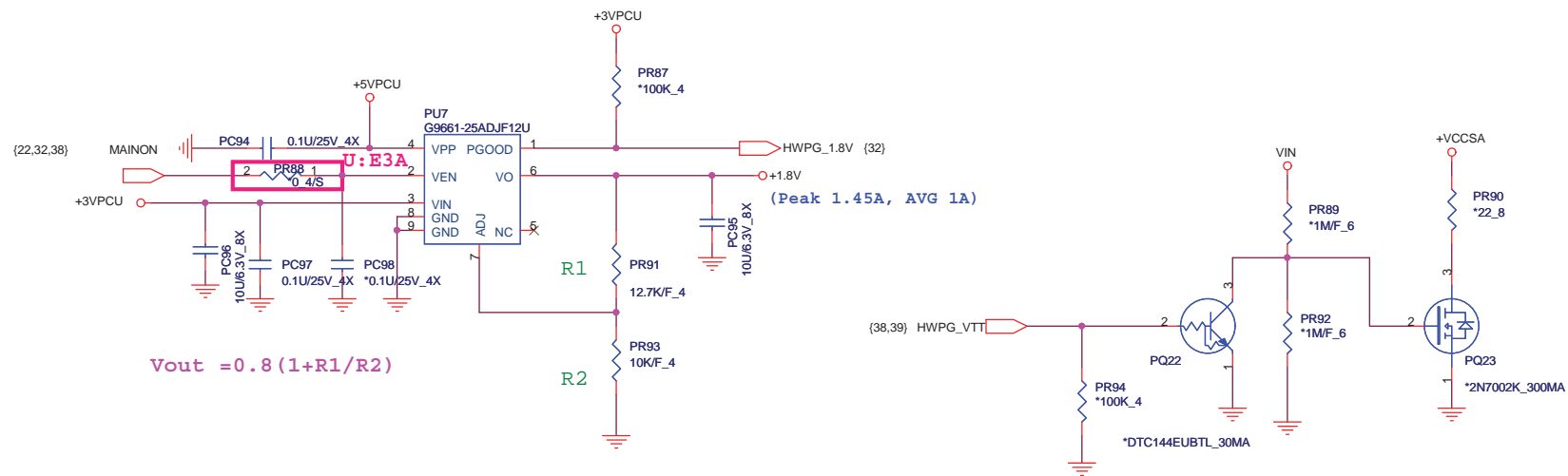


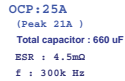




U: C2A



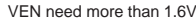




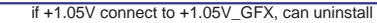
Default	N12M-GE		N12P-LP		N12P-GV	
PR131	R5	NC	10K	CS31002JB28	10K	CS31002JB28
PR113	R6	10K CS31002JB28	NC		NC	
PR121	R7	10K CS31002JB28	NC		10K	CS31002JB28
PR134	R8	NC	10K	CS31002JB28	NC	

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	N12M-GE	N12P-LP	N12P-GV
LOW	LOW	1.0V	0.925V	1.025V
LOW	HIGH	1.0V	0.90V Default	1.0V
HIGH	LOW	1.0V Default	0.9V	1.0V
HIGH	HIGH	0.85V	0.825V	0.85V Default

		N12M-GE		N12P-LP		N12P-GV	
R1	PR117	47.5K/4	CS34752PB14	22.6K/4	CS32262PB15	34.8K/4	CS33482PB22
R2	PR124	0.4	CS00002JB38	0.4	CS00002JB38	0.4	CS00002JB38
R3	PR119	270K/4	CS42702PB10	243K/4	CS42432PB02	200K/4	CS42002PB12
R4	PR114	1.1MF	CS41002PB17	750K/4	CS47502PB14	1.1MF	CS41002PB17
R4PR118,PR123		2.32K/4	CS23232PB01	2.10K/4	CS22102PB12	2.32K/4	CS23232PB01
R4PR118,PR123		3.3K/4	CS23322PB12	3.24K/4	CS23242PB17	3.3K/4	CS23322PB12

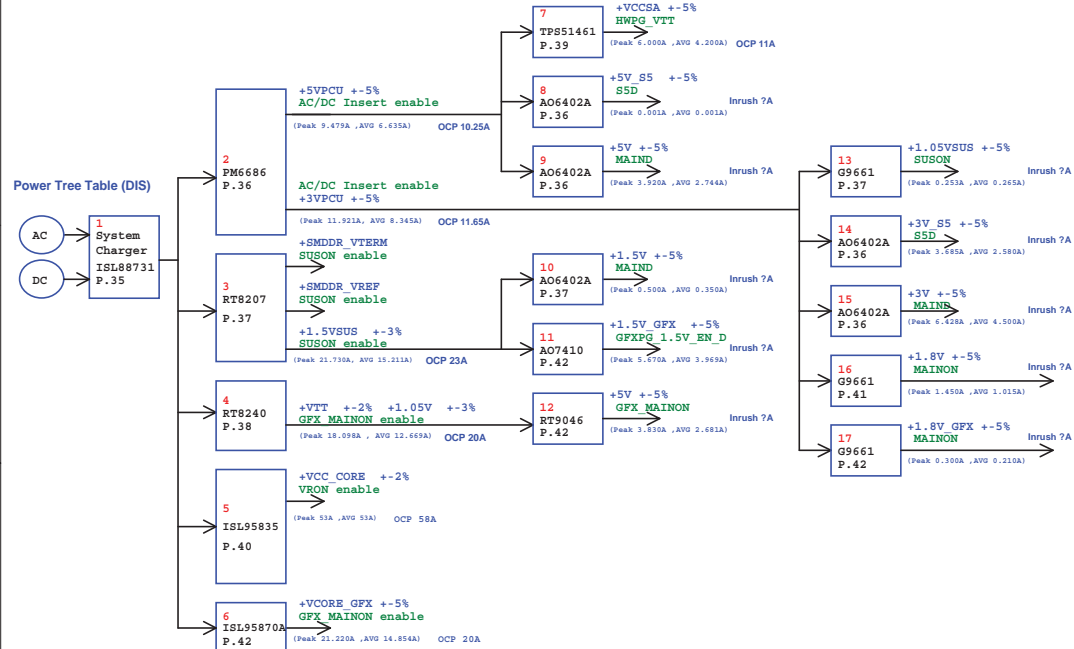


Power Off Sequence
compare +VCC3_GFX with +V1.8_GFX

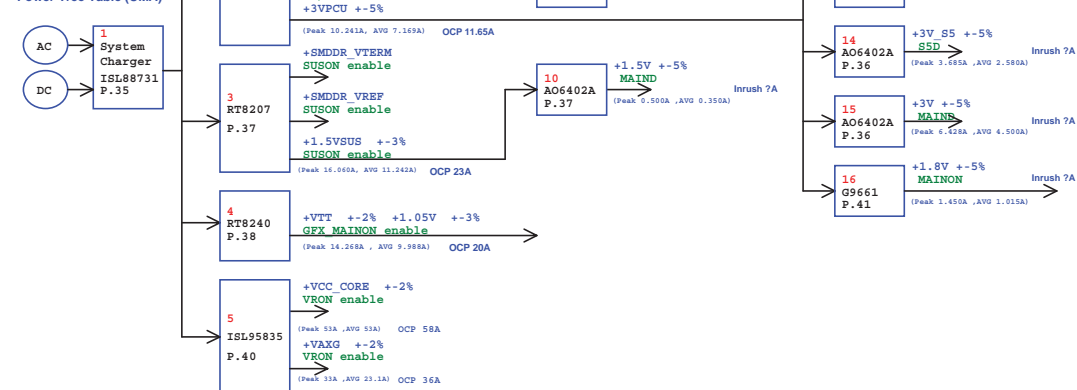


~~$V_{out1} = (1 + R_g/R_h)^{0.5}$~~

Power Tree Table (DIS)




Power Tree Table (UMA)



Power Distribution List

Power	Distribution

Model		REV	CHANGE LIST				MODEL			TE5		
							PAGE	FROM	To			
TE5 MB	1A	PAGE 3: (UMA)--R52 change to 25.5/F_4					1	1A				
		PAGE 5: (UMA)--C183,C190,C195 change to 10U/6.3V_8X					2	1A				
		PAGE 7: (UMA)--R224,R197 change to NC					3	1A				
		PAGE 9: (UMA)--PCIE_CLK_USB30_REQ#, R138 pull up to +3V_S5					4	1A				
		PAGE 9: (UMA)--PCIE_CLK_MINI_REQ#, R237 pull up to +3V					5	1A				
		PAGE 9: (UMA)--R199 NC					6	1A				
		PAGE 9: (UMA)--Q30, Q62 NC					7	1A				
		PAGE 10: (UMA)--add TP31					8	1A				
		PAGE 10: (UMA)--change Board ID9 strap Function name					9	1A				
		PAGE 11: (UMA)--C252 change to 10U/6.3V_8X					10	1A				
		PAGE 11: (UMA)--Net +1.05V change to +VTT					11	1A				
		PAGE 11: (UMA)--R117,R182,R114 change to 10K_4					12	1A				
		PAGE 12: (UMA)--R190,R194,R110 change to 10K_4					13	1A				
		PAGE 23: (UMA)--C978 NC					14	1A				
		PAGE 23: (UMA)--R66,R412,R154,Q45 change Function code to HM@ and delete discrete HDMI-HPD reference					15	1A				
		PAGE 24: (UMA)--add D7					16	1A				
		PAGE 25: (UMA)--add R201,R7,Q10					17	1A				
		PAGE 27: (UMA)--USB3.0 change to NEC solution					18	1A				
		PAGE 30: (UMA)--C97,C92,C106 change to 1U/10V_6Y					19	1A				
		PAGE 31: (UMA)--CN21 Foot-print change to 3in1-cm35-5-21p					20	1A				
		PAGE 32: (UMA)--3ND_MBCLK,3ND_MBDATA R269,R270 pull up to +3V					21	1A				
		PAGE 32: (UMA)--add 13MS,14MS,15MS Strap pin SKU_STRAP_1,SKU_STRAP_2,SKU_STRAP_3					22	1A				
		PAGE 33: (UMA)--add PR1					23	1A				
		PAGE 34: (UMA)--LED1,LED4,LED5,LED6 change symbol and Foot-print					24	1A				
		PAGE 16: (VGA)--add R3712					25	1A				
		PAGE 19: (VGA)--R3711 change to 47U/6.3V_1206X					26	1A				
		PAGE 25: (ALL)--Net name PCIE_CLK_3G_REQ# change to PCIE_CLK_3G_REQ#_C					27	1A				
		PAGE 22: (ALL)--add R65					28	1A				
		PAGE 37: (ALL)--PC60 change to CC7390JM202					29	1A				
		PAGE 18: (VGA)--add R3601, R3575					30	1A				
PAGE 24: (UMA)--CN4 Value change to 87213-2000G												
PAGE 22: (ALL)--add R102												
PAGE 33: (ALL)--Remove K/B LED power circuit												
2A	PAGE 15: (VGA)--delete R3535,R3547											
	PAGE 22: (ALL)--add R31											
	PAGE 22: (ALL)--add R102											
	PAGE 40: (ALL)--add PC168											
	PAGE 32: (ALL)--13MS,14MS,15MS Strap pull up voltage change to +3VPCU											
	PAGE 34: (ALL)--add R213											
	PAGE 42: (VGA)--add PQ49											
DOC NO. 204		PROJECT MODEL :	TE5	APPROVED BY:	Andy Wang	DATE:	2010/10/01	<div> Quanta Computer Inc. PROJECT : TE5</div> <div>Change list</div> <div>Date: Wednesday, January 05, 2011 Sheet 31 of 35</div>				
		PART NUMBER:		DRAWING BY:	Andy Wang	REVISION:	1A					

