

NALAA

Hamburg 10

LA-6041P REV 1.0 Schematic

Intel Arrandale /IBEX PEAK

2009-10-01 Rev 1.0

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Compal Confidential

Model Name : NALAA

File Name : LA-6041P

Intel Arrandale

rPGA-989

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Fan Control

APL5607KI-TRG
page 6

Clock Generator

RTM890N-631-GRT
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Memory BUS(DDRIII)
Dual Channel

200pin DDRIII-SO-DIMM X2

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1.5V DDRIII 800/1066 MT/s

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2.7GHz

DMI X4
2.5GHz

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USB port 5
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USB port 10
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HDMI Conn.
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HDMI Level Shifter
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5V 480MHz

USB
5V 480MHz

PCIe 1x
1.5V 2.5GHz(250MB/s)

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WiMax
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PCieMini Card
WLAN
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5V 3GHz(300MB/s)

SATA HDD
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SATA port 4
5V 3GHz(300MB/s)

SATA ODD
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5V 3GHz(300MB/s)

eSATA
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USB port 3
5V 480MHz

USB
USB port 3
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RJ45
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RTL8105E-GR 10/100M
PCIe port 1
page 28

PCIe 1x
1.5V 2.5GHz(250MB/s)

Intel Ibex Peak

BGA-951

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LPC BUS
3.3V 33 MHz

HD Audio
3.3V/1.5V 24MHz

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DC/DC Interface CKT.
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ALC259-GR
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Touch Pad
page 26

Int.KBD
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EC ROM
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Int.
MIC CONN.
(LYDS CONN)
page 13

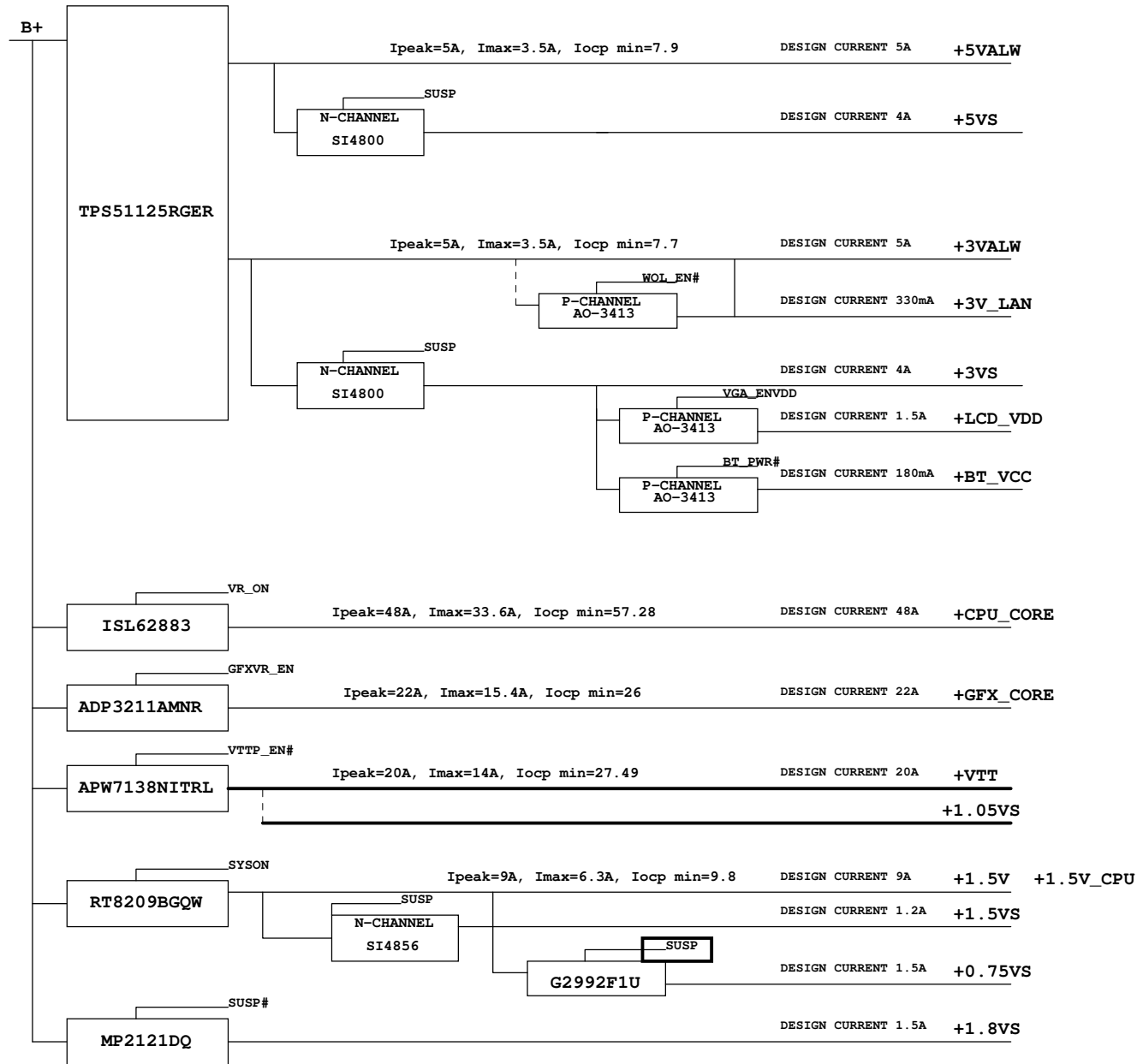
MIC CONN
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HP CONN
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SPK CONN
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NALAA Hamburg Intel Arrandale (UMA)



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Voltage Rails

(O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	RJ11	LAN	HDMI	Card Reader	Express Card		Mini Card
description	(B)	(R)	(E)	(Y)	(W)			
explain	Bluetooth	MDC	LAN	HDMI	Card Reader	New Card	PCMCIA	WIRELESS
BTO	BT@	MDC@		IHDMI@	CARD@			WLAN@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

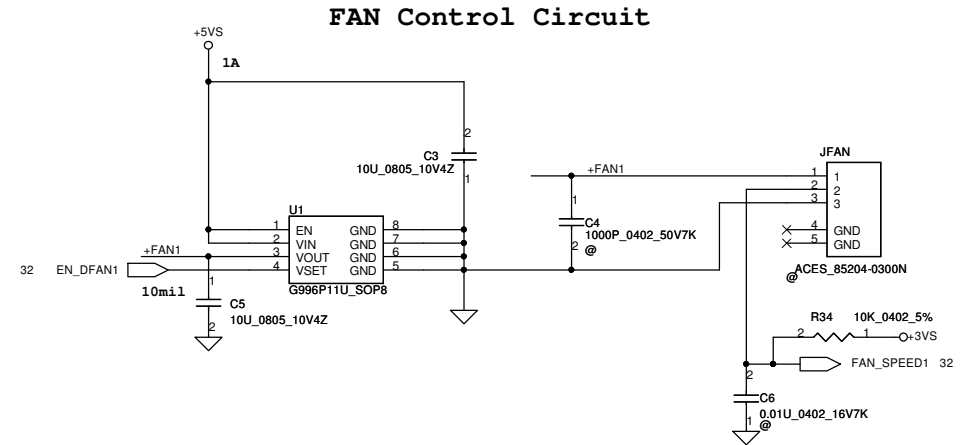
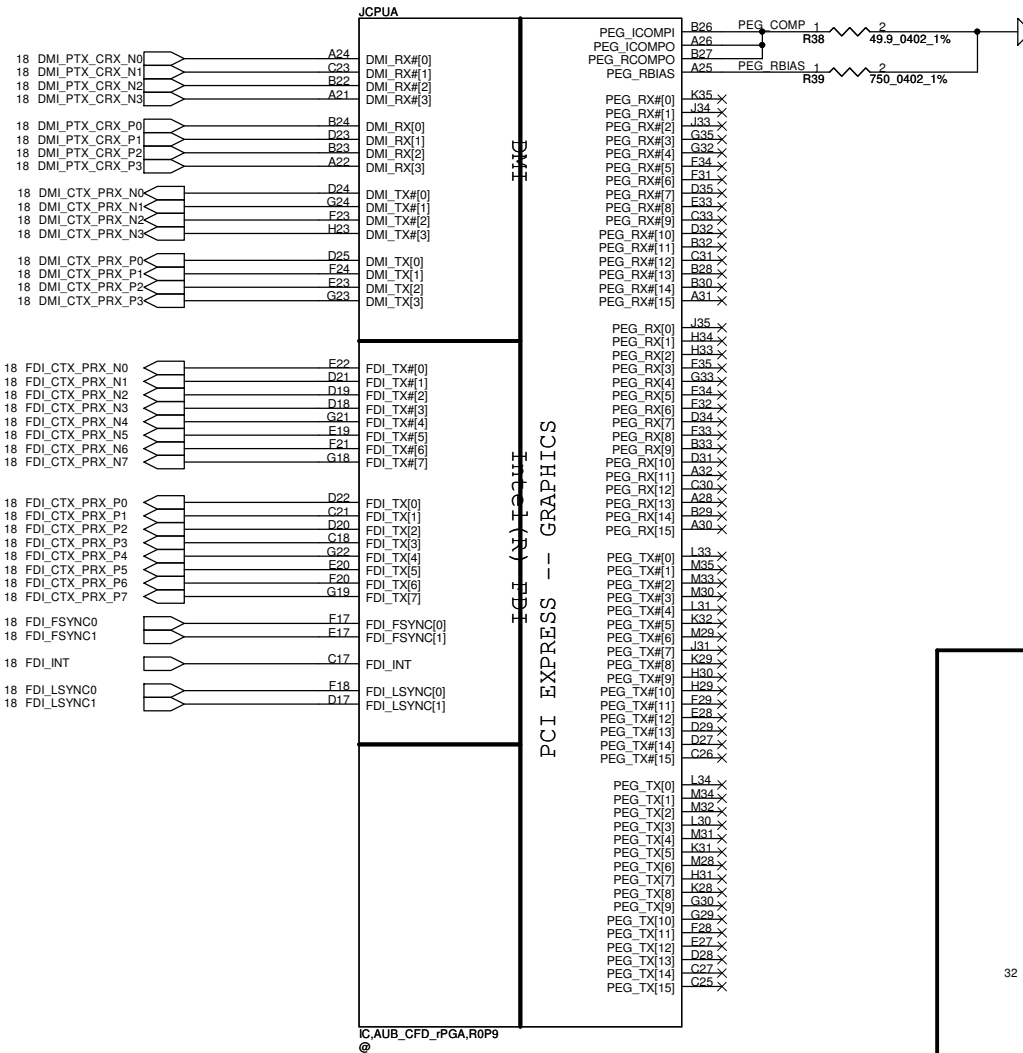
EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VALW	EC KB926 D3		+3VS	EC KB926 D3	
+3VALW	Smart Battery	0001 011x b	+3VS	VGA THM Sensor ADM1032ARMZ	1001 110x b
			+3VS	PCH	0100 110x b

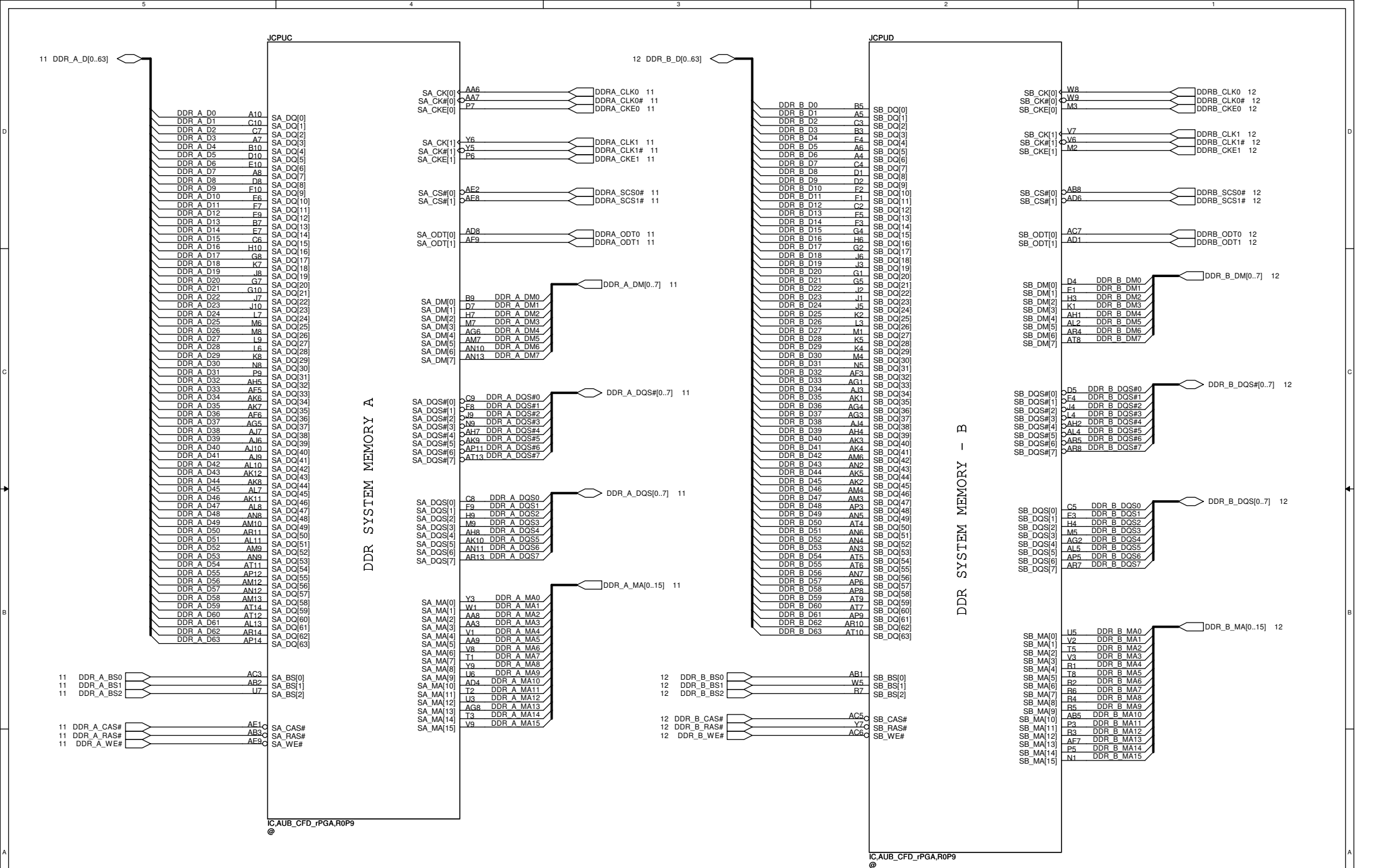
PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	Express	
+3VS	WLAN/Wimax/3G	

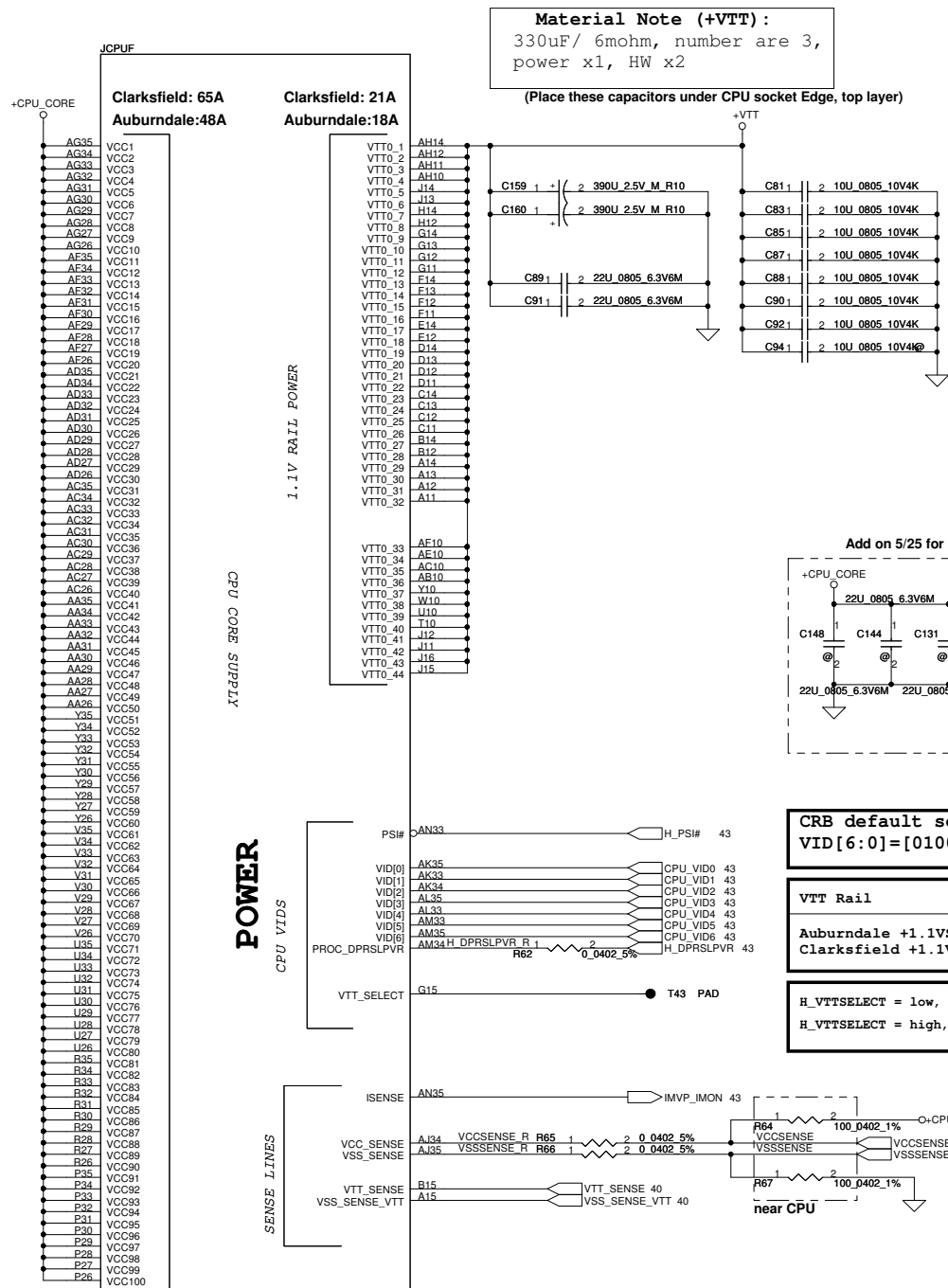
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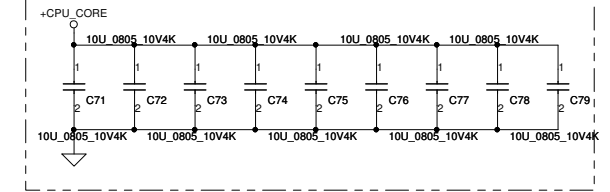
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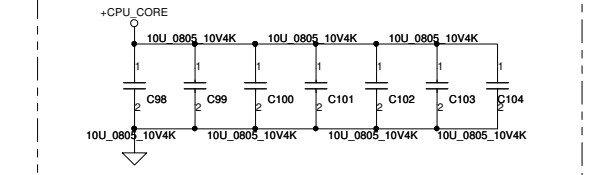
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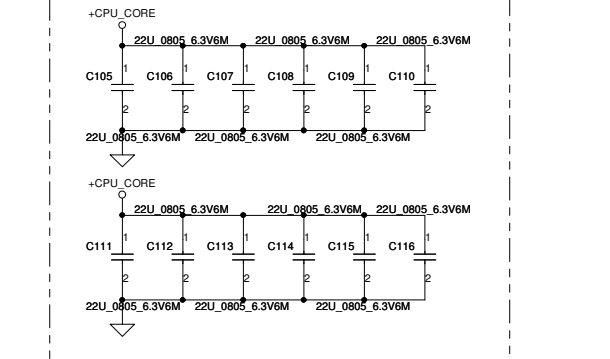
(Place these capacitors between inductor and socket on Bottom)



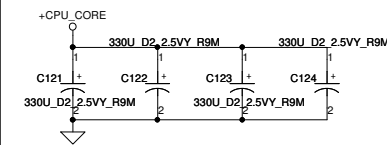
(Place these capacitors under CPU socket, top layer)



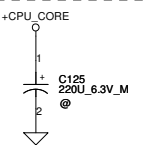
(Place these capacitors on CPU cavity, Bottom Layer)



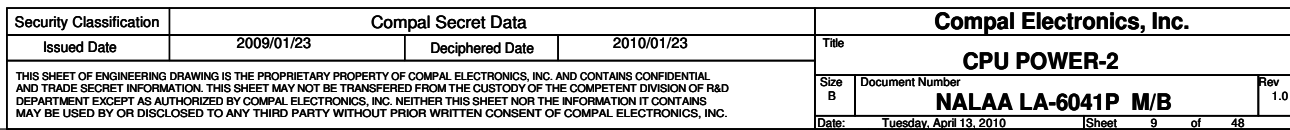
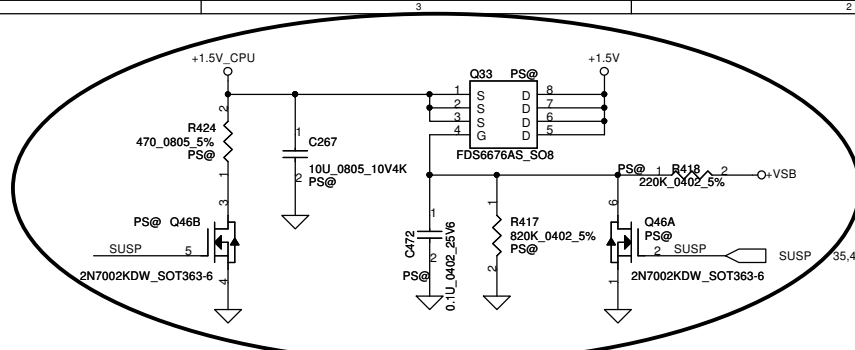
TOP side (under inductor)

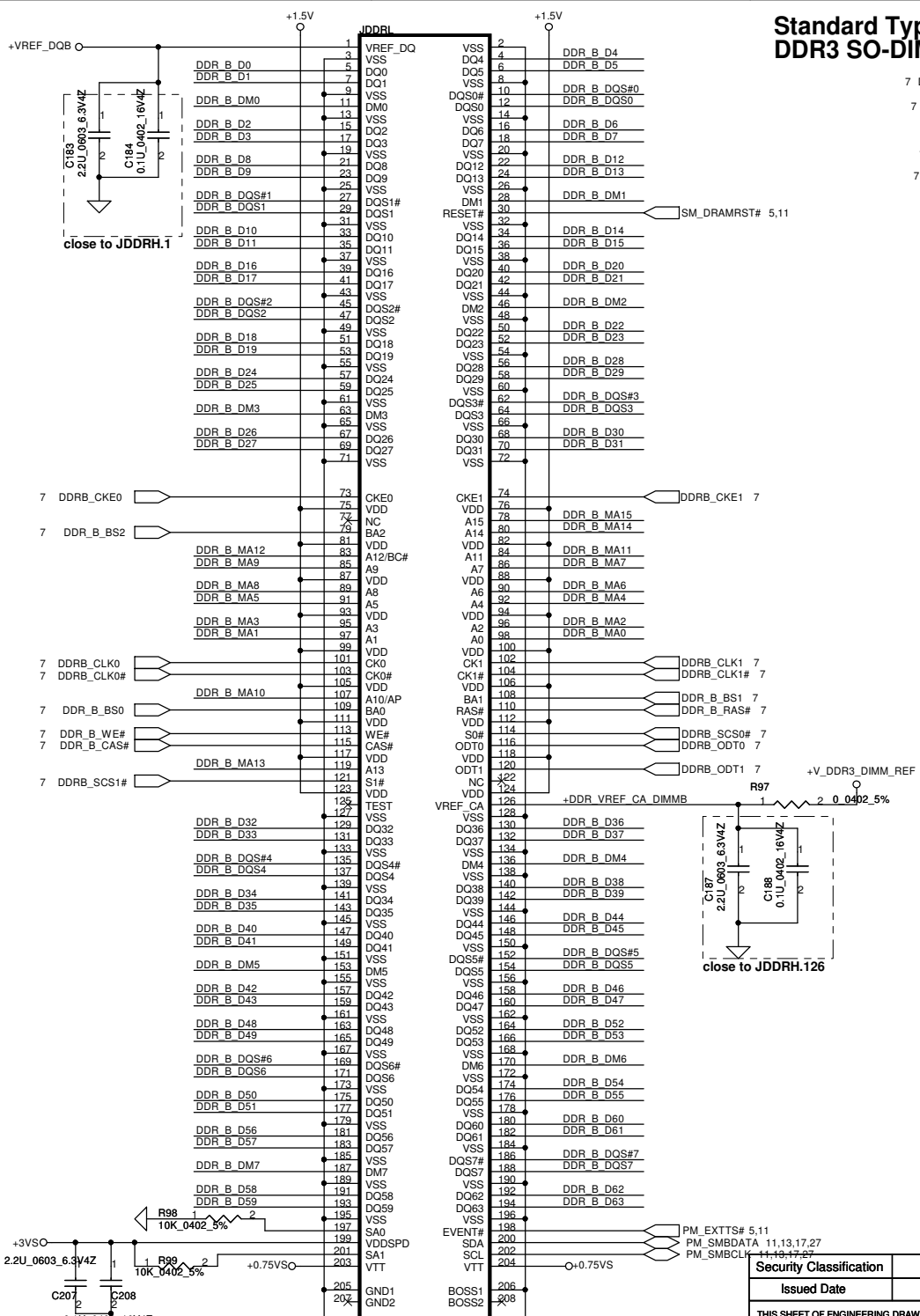


Co-layout with C123

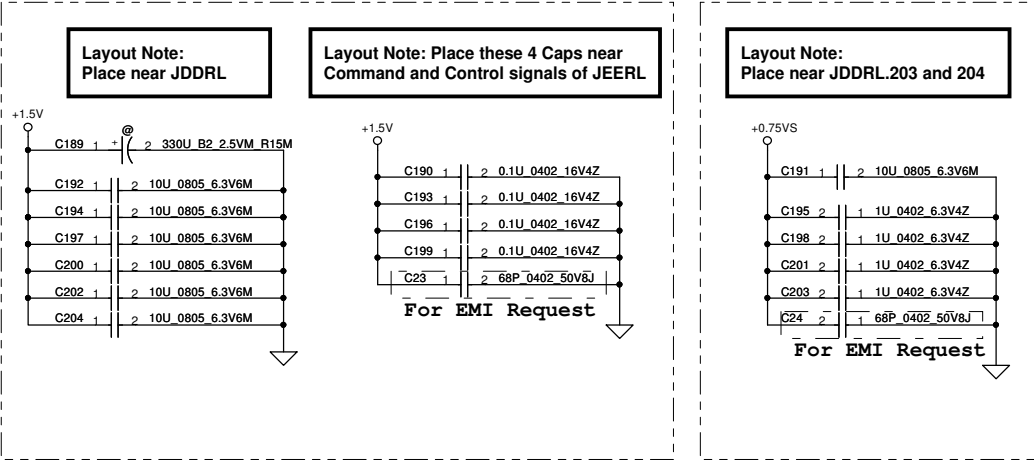
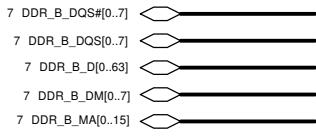


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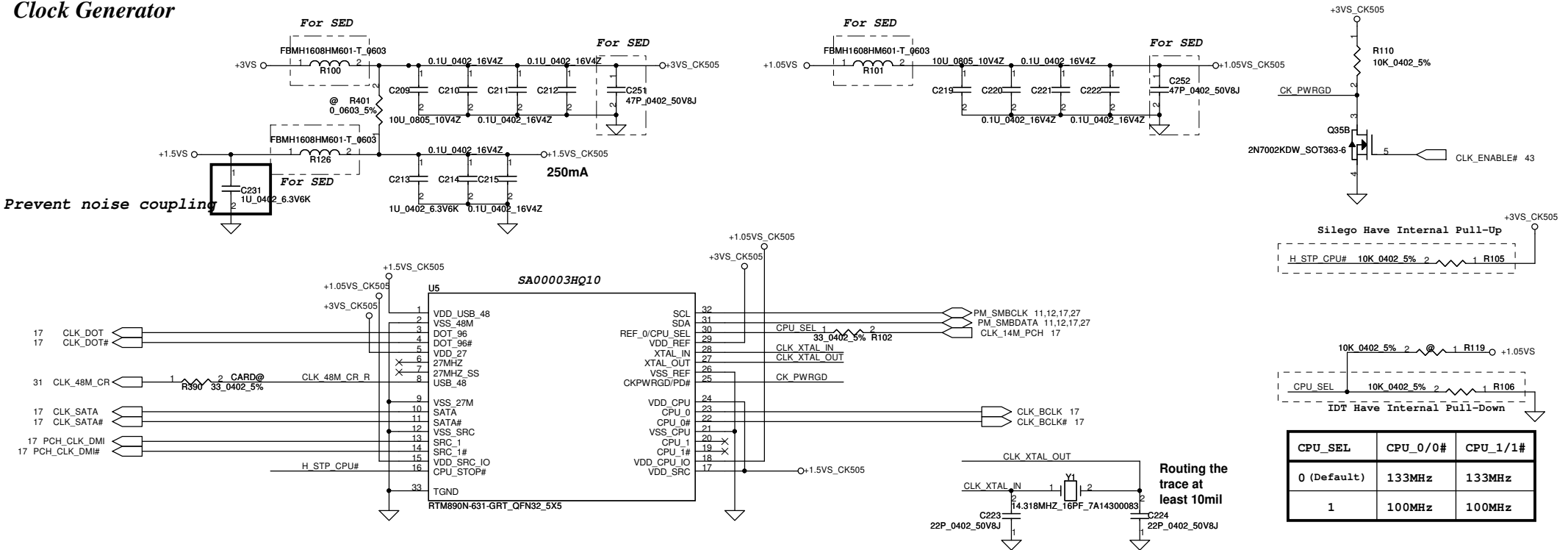
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DDR3 SO-DIMM B



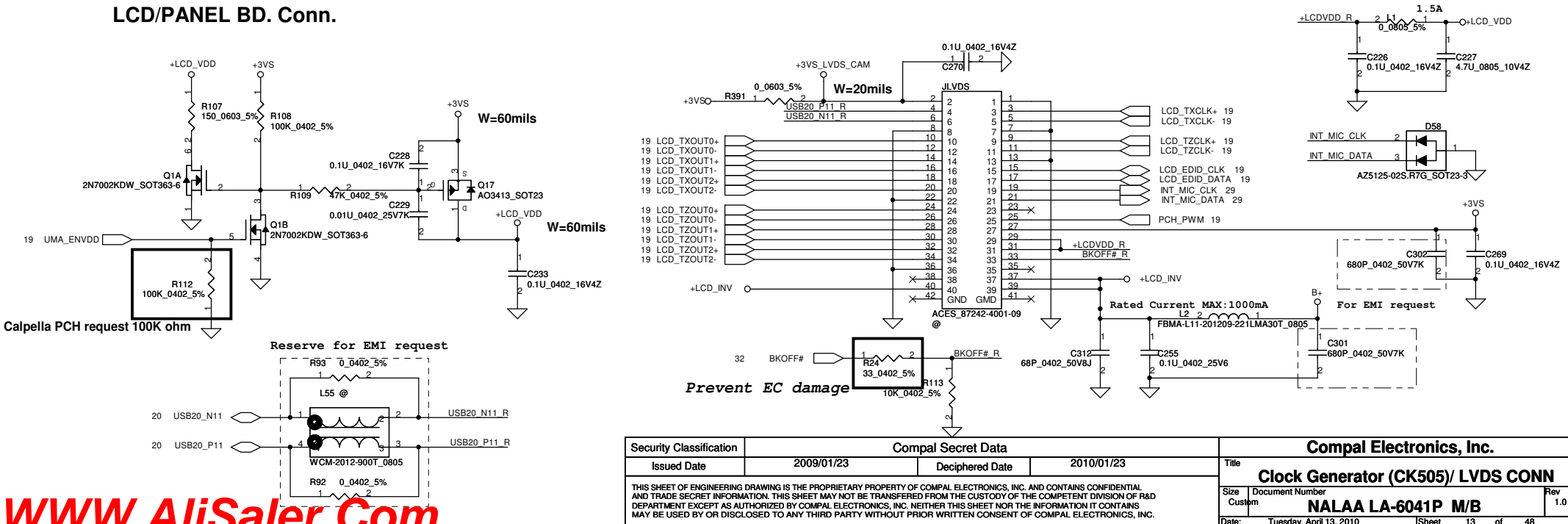
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Clock Generator

Prevent noise coupling

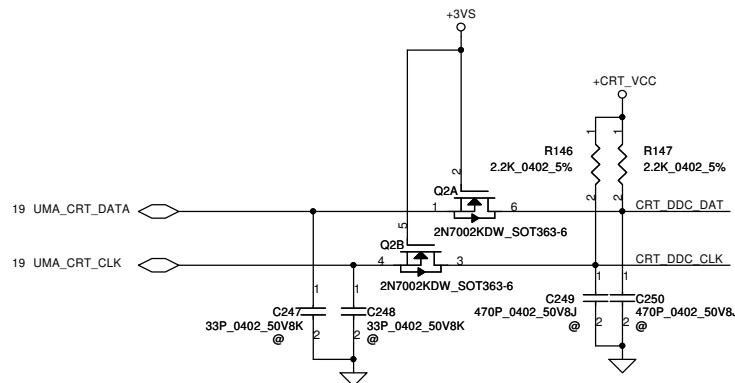
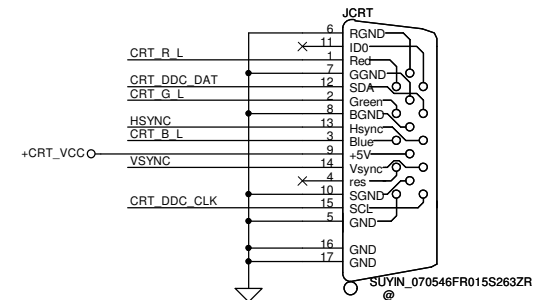
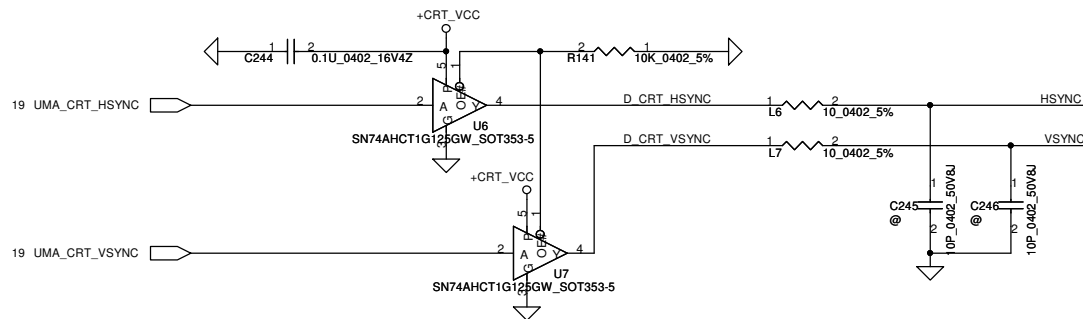
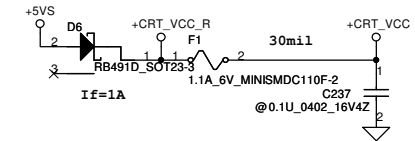
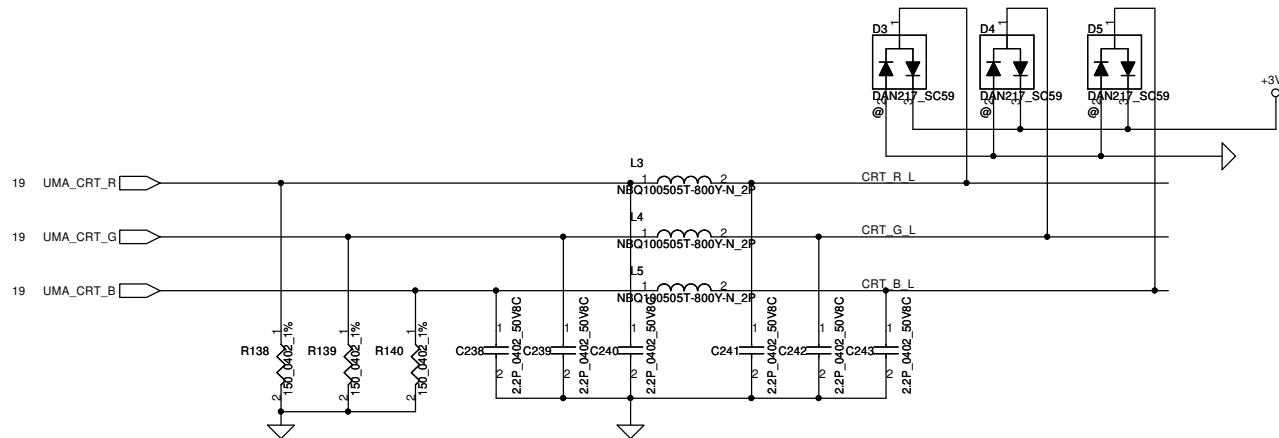


LCD/PANEL BD. Conn.



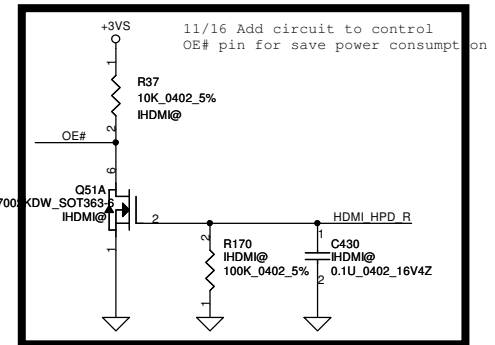
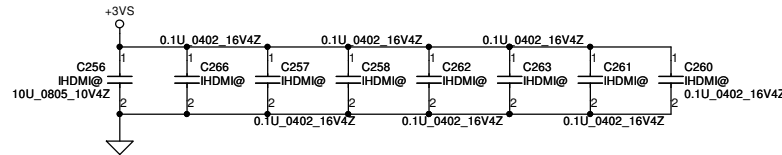
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CRT CONNECTOR

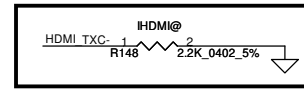
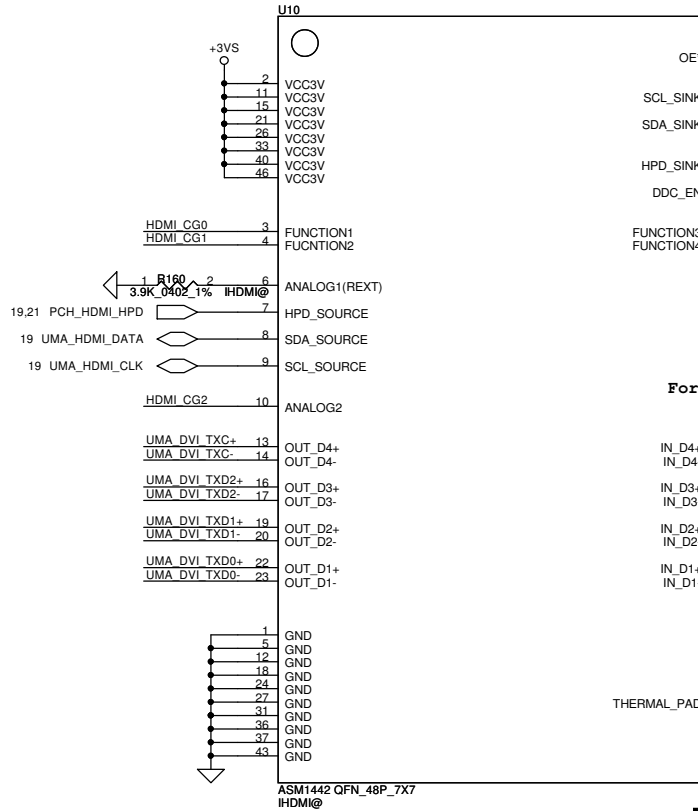
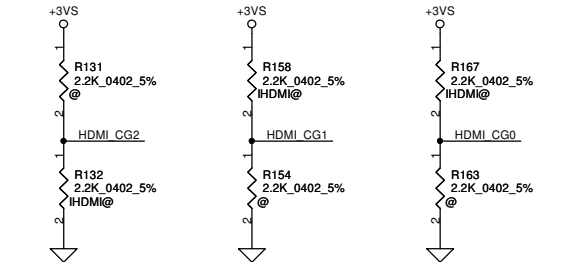


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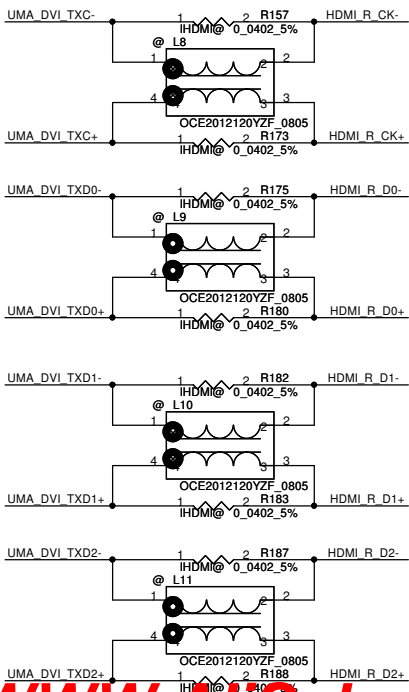
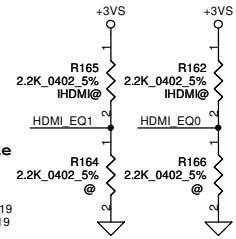
CG2	CG1	CG0	Swing	Pre-amp	Slew-rate	
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0	0	1	420	0	-3dB	Shortest trace
0	1	0	450	0	-3dB	Shortest trace
0	1	1	460	0	-4dB	
1	0	0	340	0	0	
1	0	1	400	2dB	0	Longest trace
1	1	0	400	2dB	0	Longest trace
1	1	1	420	0	0	



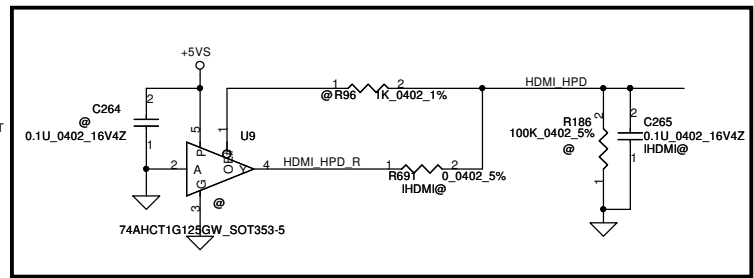
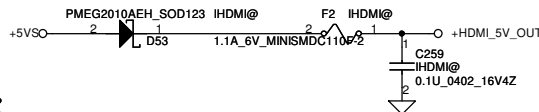
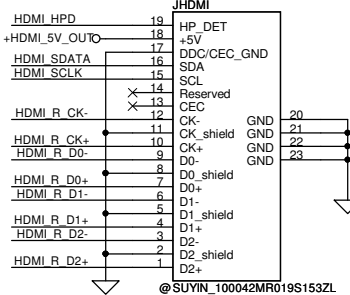
EQ1	EQ0	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB



For UMA HDMI level shift display compatibility issue

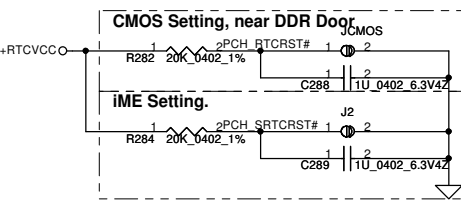


HDMI Connector



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/01/23				Deciphered Date			
2009/01/23				2010/01/23				Title			
								HDMI Connector			
Size				Document Number				NALAA LA-6041P M/B			
								Rev 1.0			
Date				Tuesday, April 13, 2010				Sheet 15 of 48			

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Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)
--------------	---

HDA_SYNC

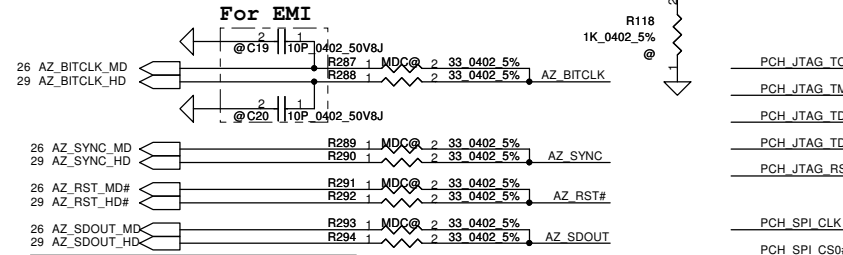
This signal has a weak internal pull down.
 H=>On Die PLL is supplied by 1.5V
 L=>On Die PLL is supplied by 1.8V

HDA_SDO

This signal has a weak internal pull down.
 This signal can't PU

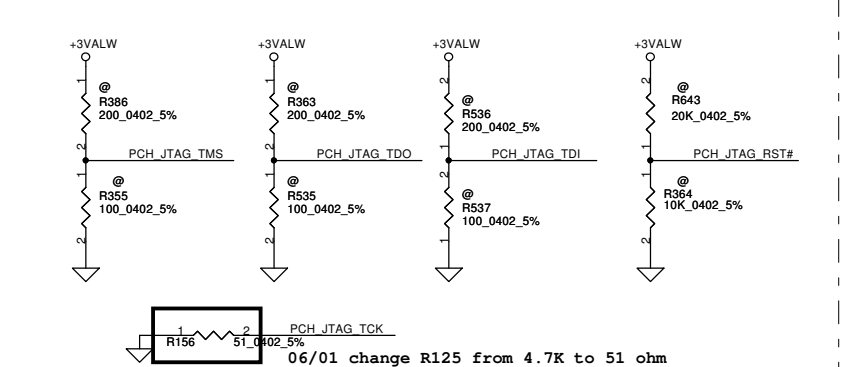
Flash Descriptor Security Override

HDA_DOCK_EN#	Low = Enabled High = Disabled *
--------------	------------------------------------

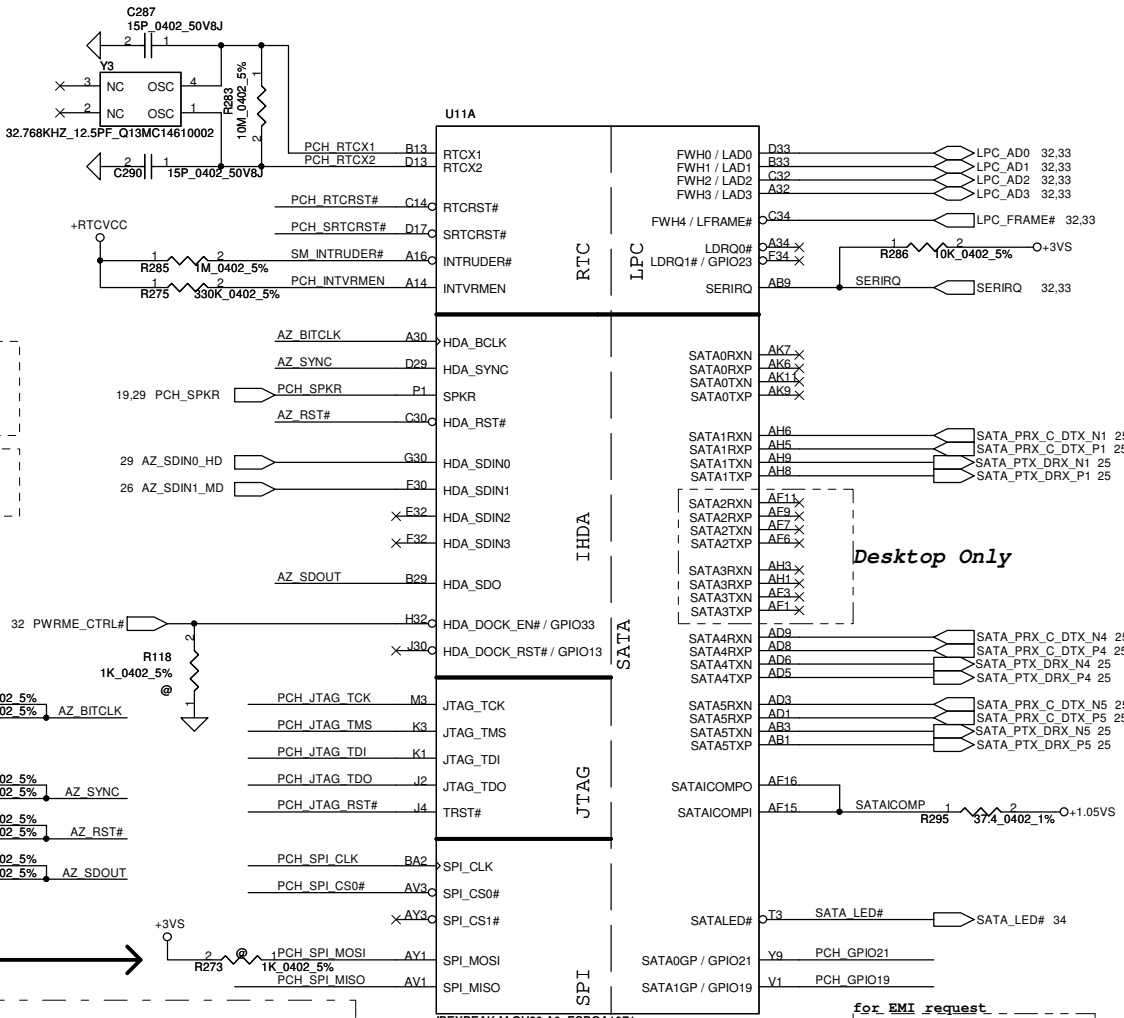


ITPM Enabled Internal: Pull down 20k

SPI_MOSI	High = Enabled Low = Disabled (Default)
----------	--



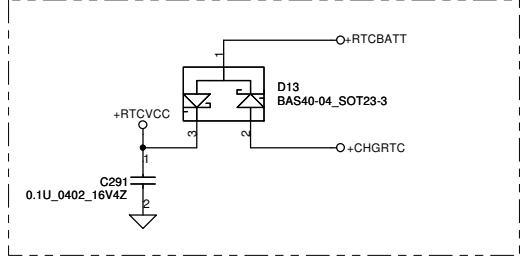
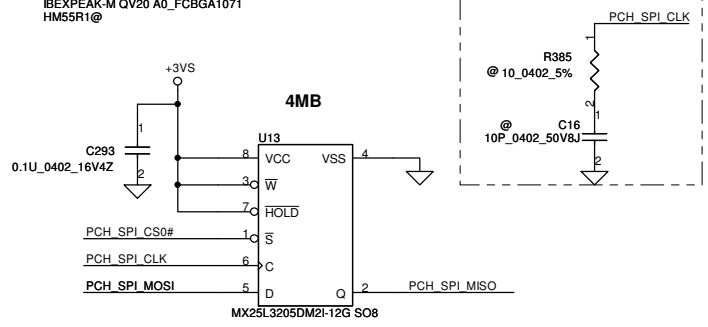
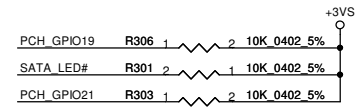
PCH Pin	RefDes	PCH JTAG Enable	PCH JTAG Disable (Default)
PCH_JTAG_TDO	R358	No install	No install
PCH_JTAG_TMS	R355	200ohm	No install
PCH_JTAG_TDI	R536	200ohm	No install
PCH_JTAG_TCK	R156	51ohm	No install



1ST HDD

SATA ODD

eSATA

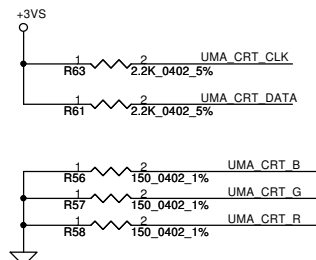
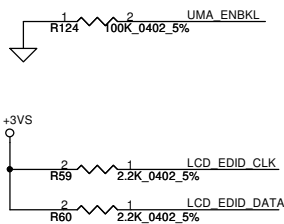


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				NALAA LA-6041P M/B	
Date: Tuesday, April 13, 2010				Sheet	16 of 48

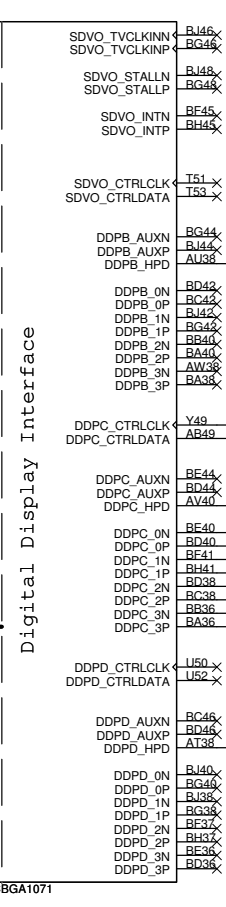
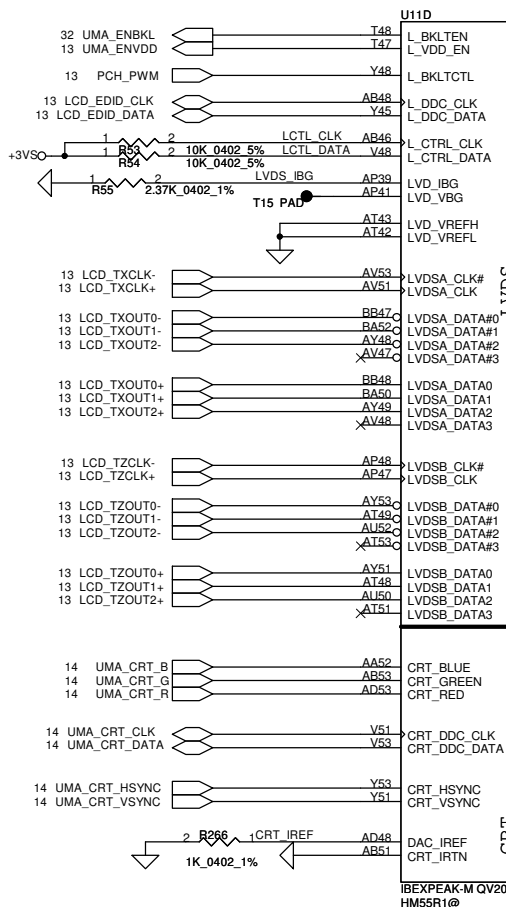
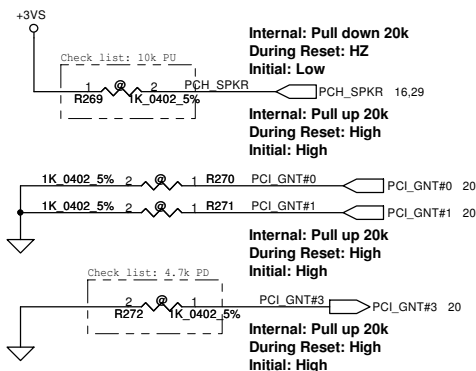




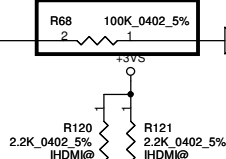
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	PCH-DMI/FDI/PWM
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				Document Number	1.0
				NALAA LA-6041P M/B	
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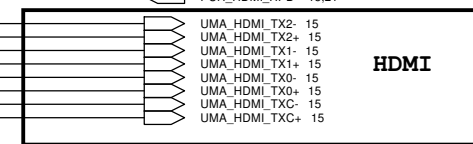
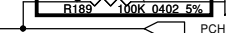
PCH Strap Pin



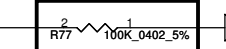
For INTEL issue (pending interrupts from the PCH for unused HDMI ports)



For INTEL issue (pending interrupts from the PCH for unused HDMI ports)



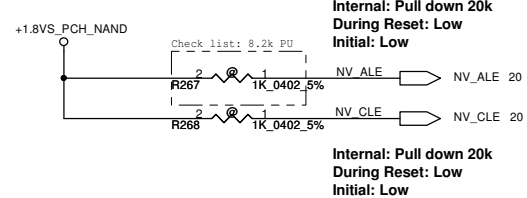
For INTEL issue (pending interrupts from the PCH for unused HDMI ports)



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

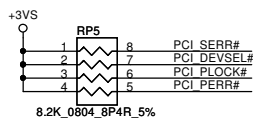
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable
	High= A16 swap override Disable



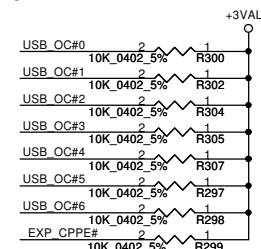
Danbury Technology Enabled	
NV_ALE	High = Enabled
	Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default)
	High= Set to Vcc

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Size	Custom	Document Number	NALAA LA-6041P M/B	Rev	1.0
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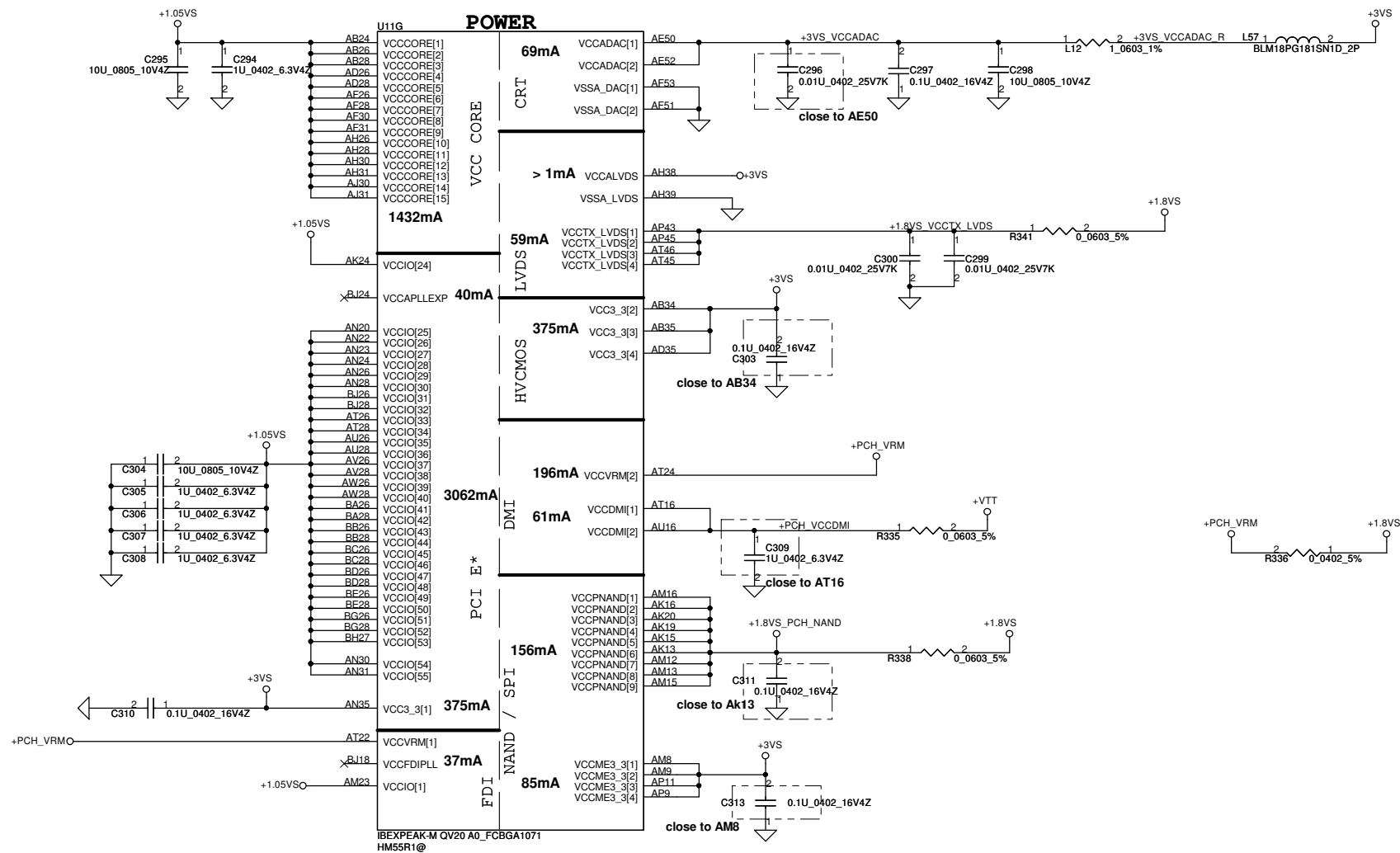
Change to 47 ohm?



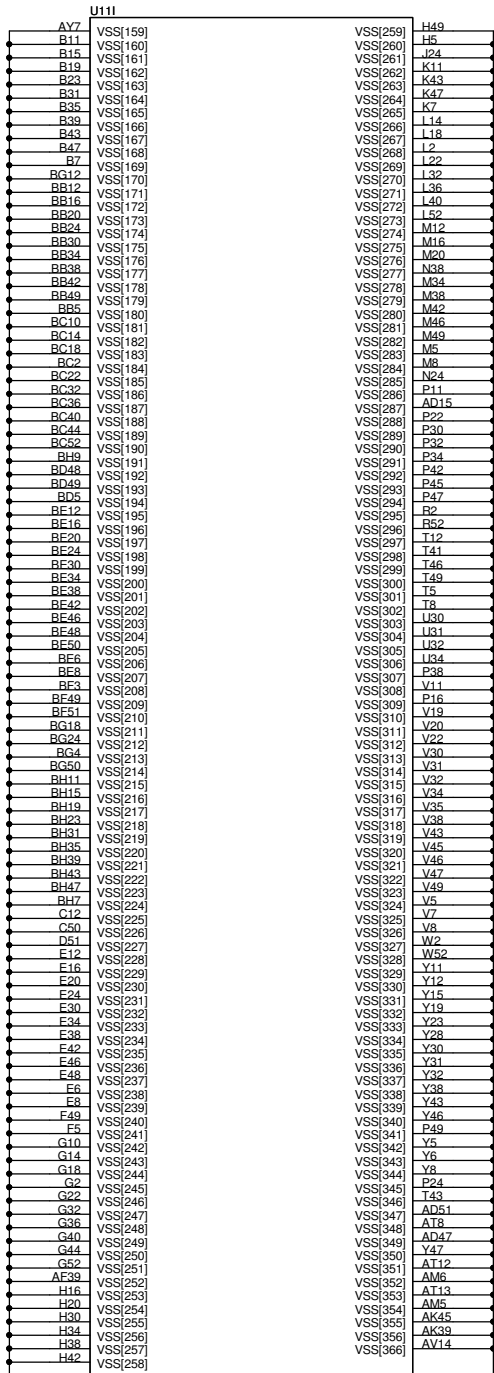
WWW.AliSaler.Com



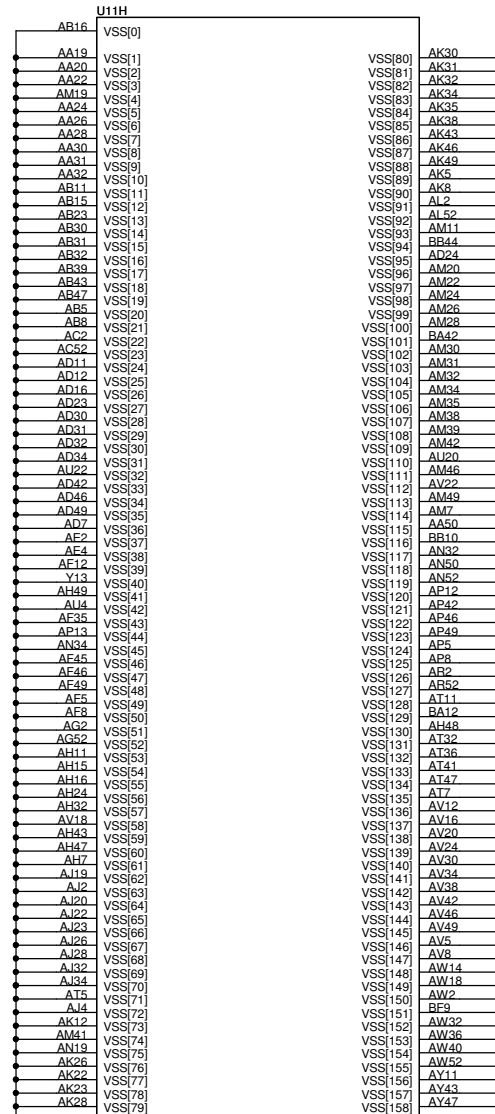
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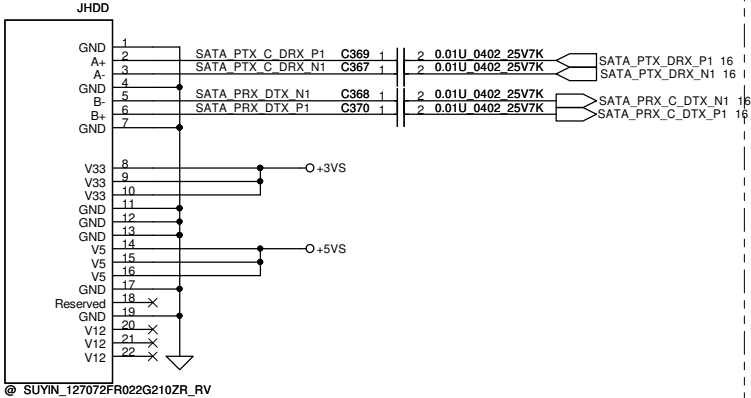
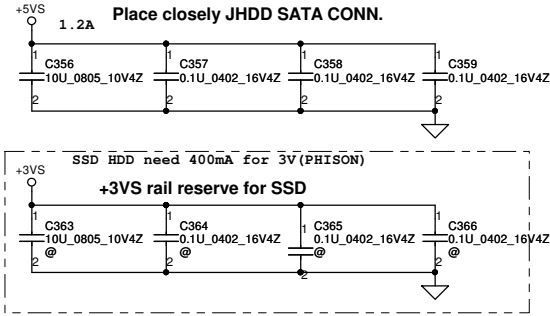
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HM55R1@



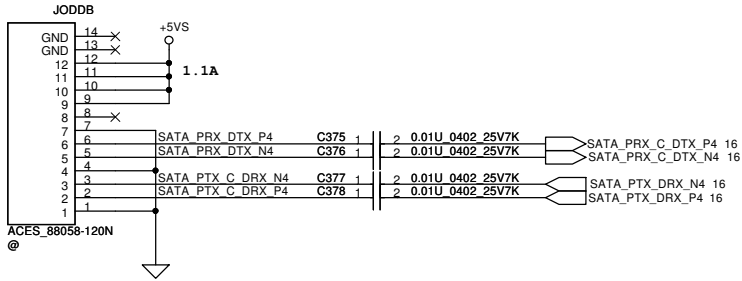
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								Size	Document Number	Rev
								Custom	NALAA LA-6041P M/B	1.0
								Date:	Tuesday, April 13, 2010	Sheet

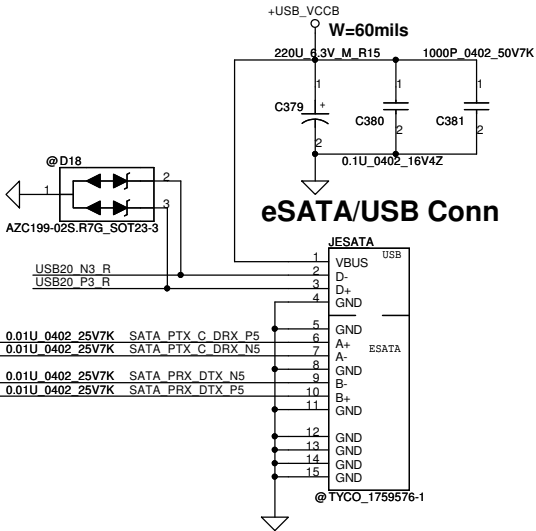
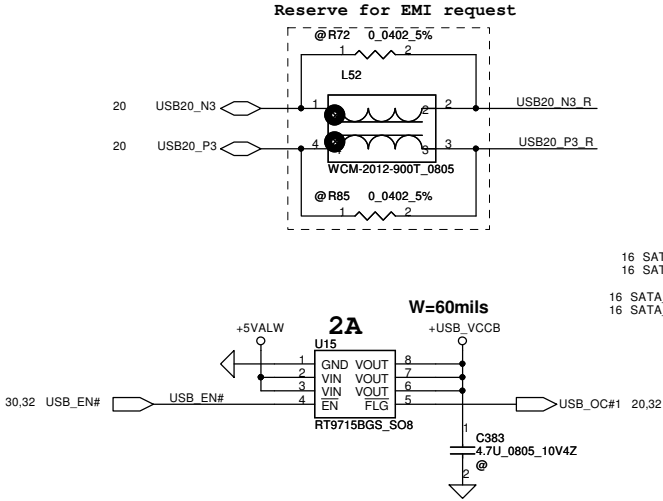
SATA HDD Conn.



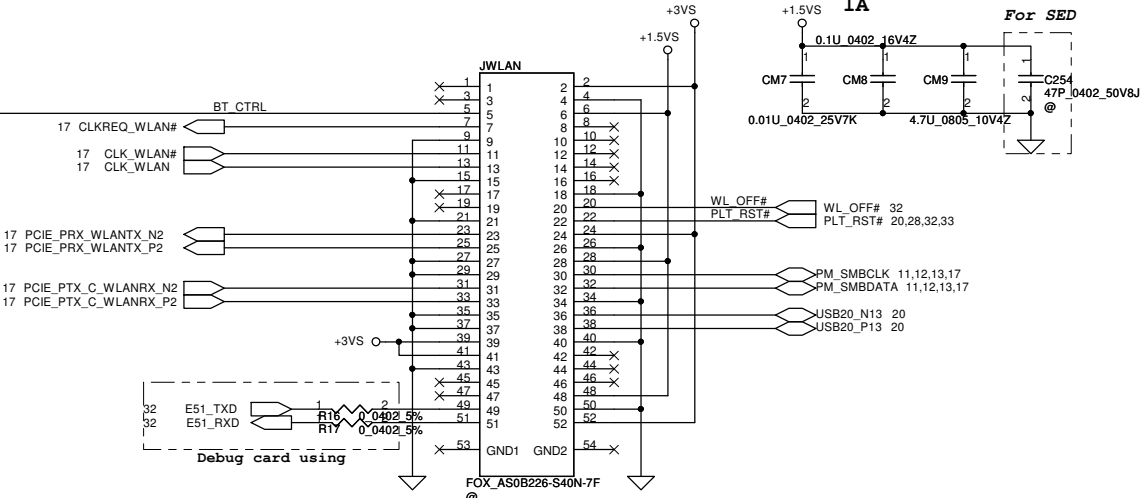
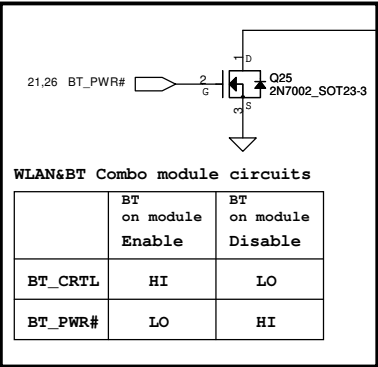
SATA ODD Conn



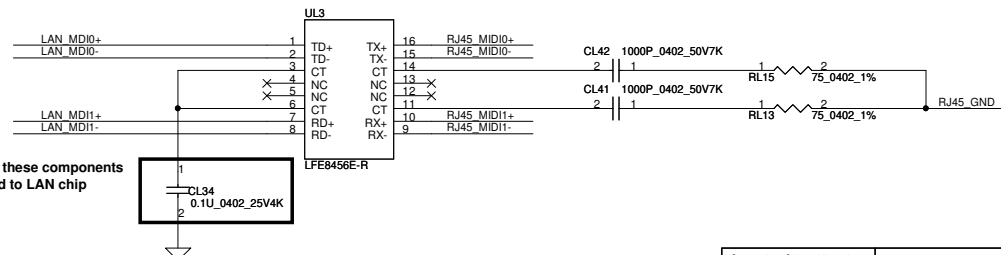
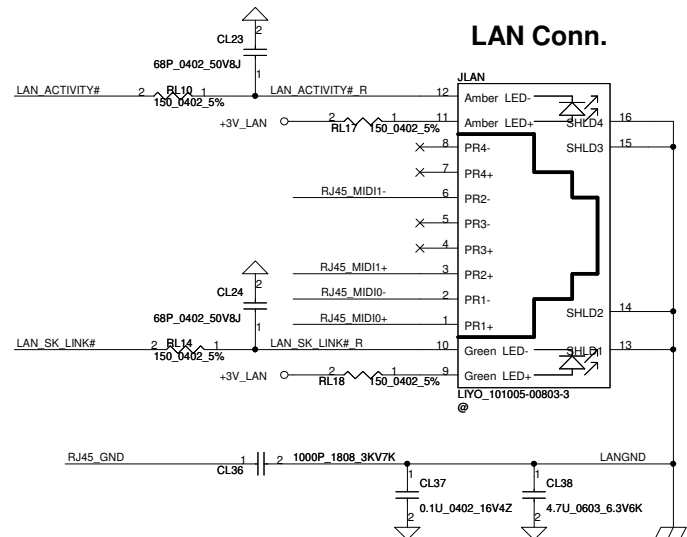
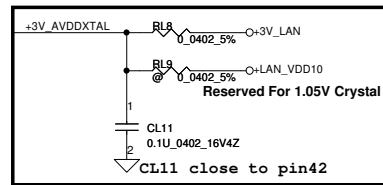
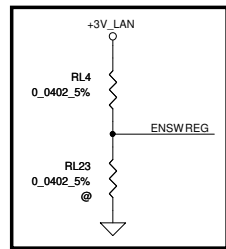
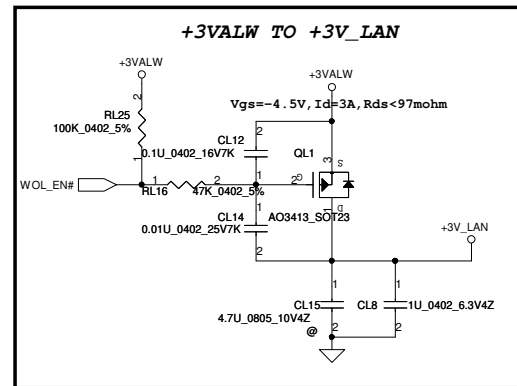
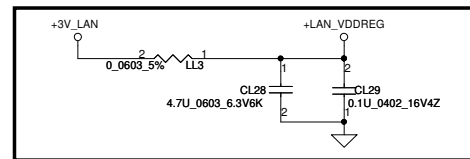
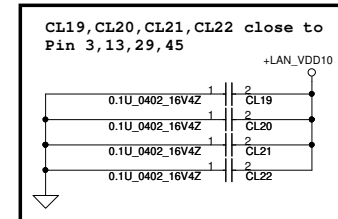
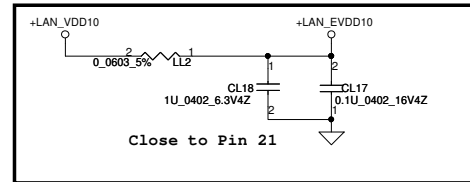
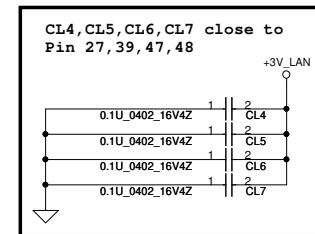
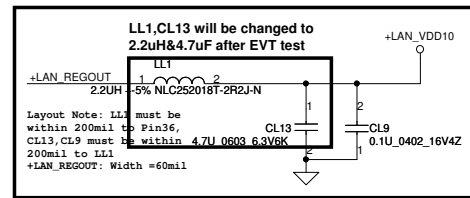
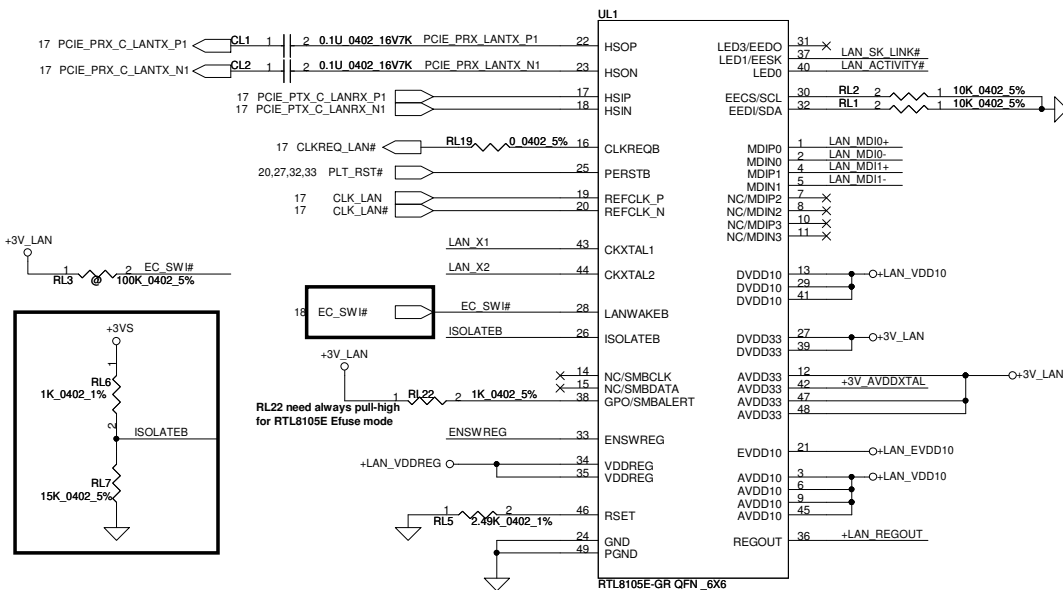
eSATA/USB



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Size	Document Number	NALAA LA-6041P M/B		Rev	1.0
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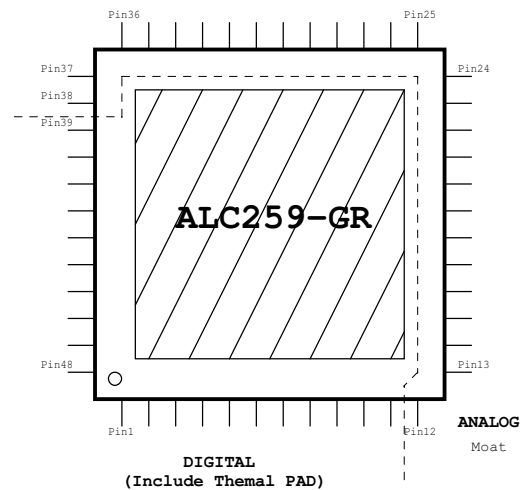
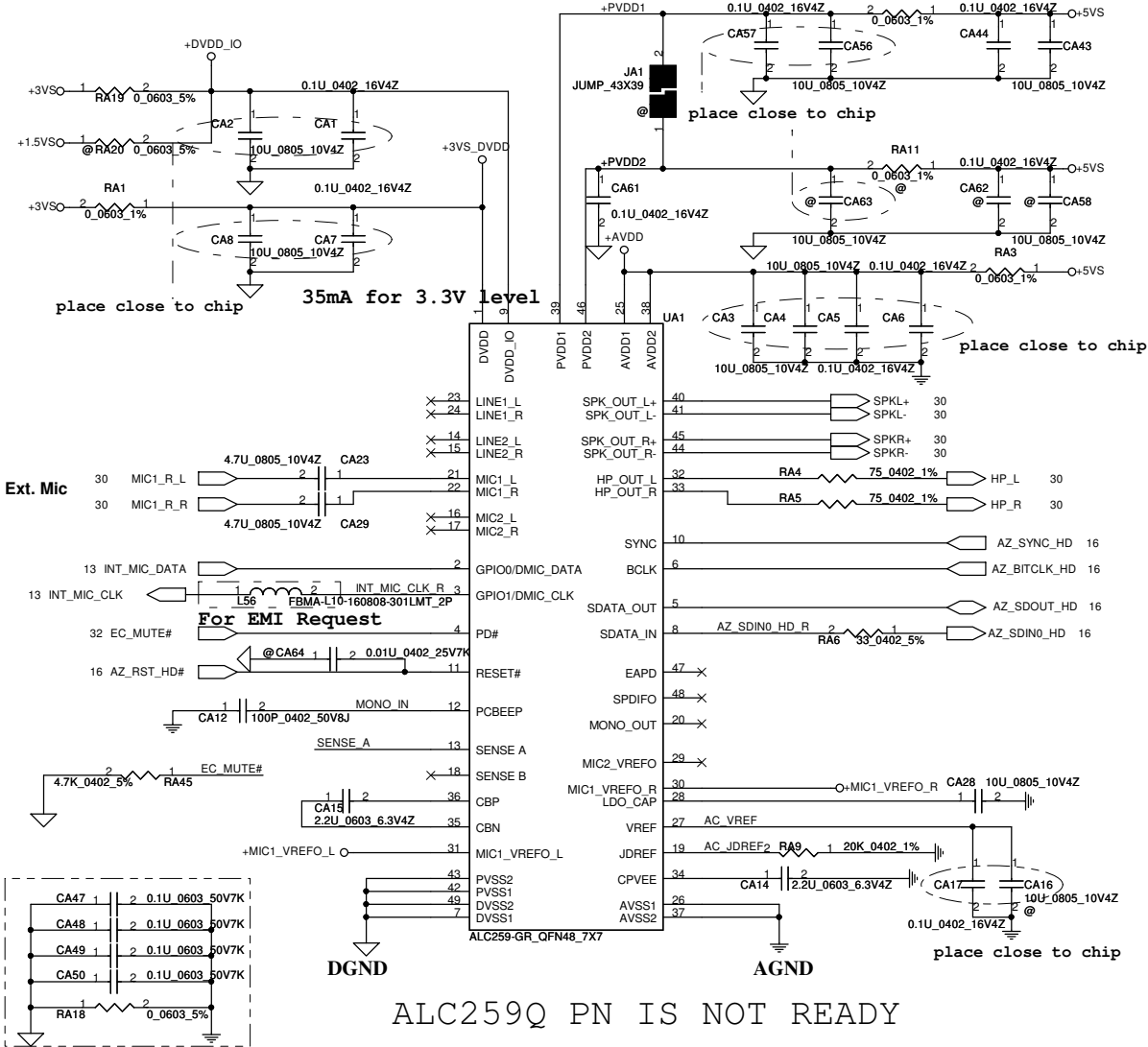


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			Size Document Number	Rev 1.0
			NALAA LA-6041P M/B	
			Date: Tuesday, April 13, 2010	Sheet 27 of 48

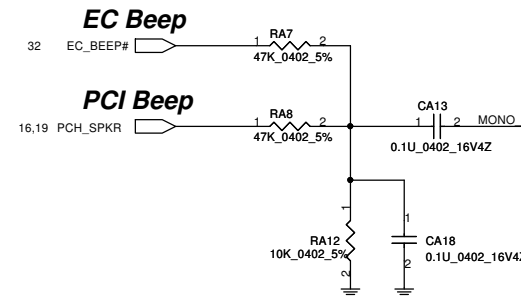


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						Size	Document Number				Rev
						Custom	NALAA LA-6041P M/B				1.0
						Date:	Tuesday, April 13, 2010		Sheet	28	of

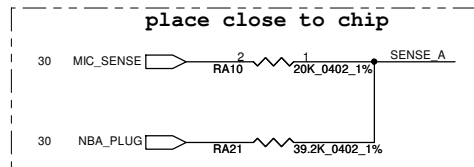
Codec



Beep sound

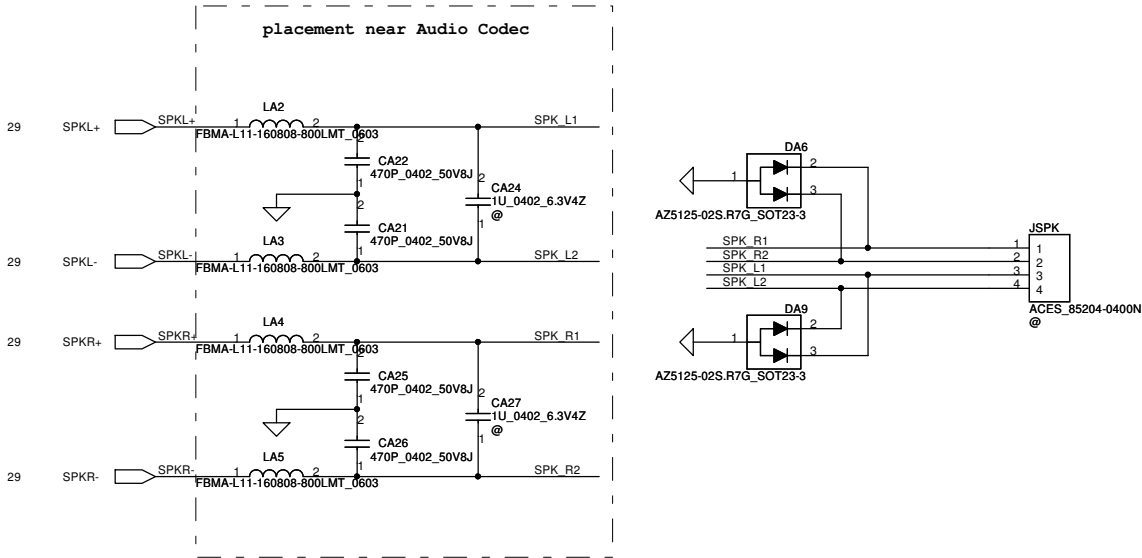


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

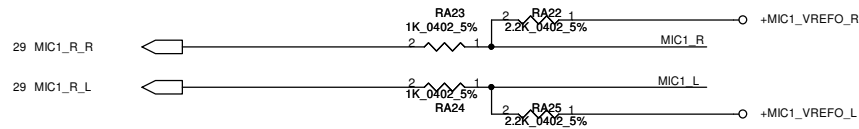


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				Rev	1.0

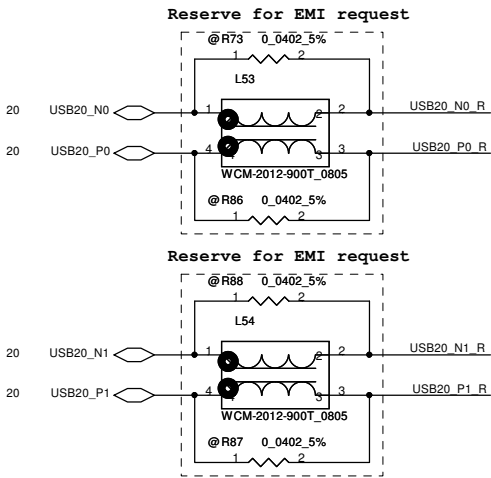
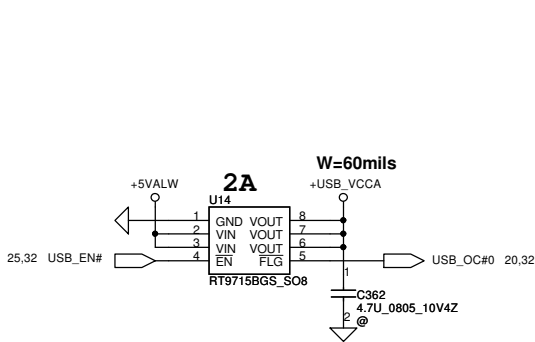
Speaker Connector



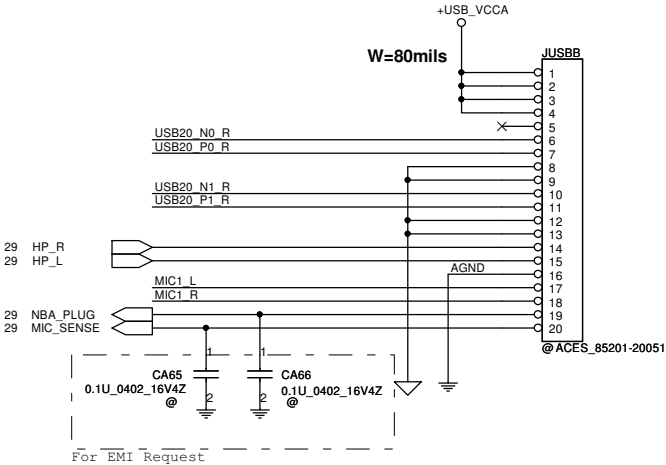
Ext.MIC/LINE IN



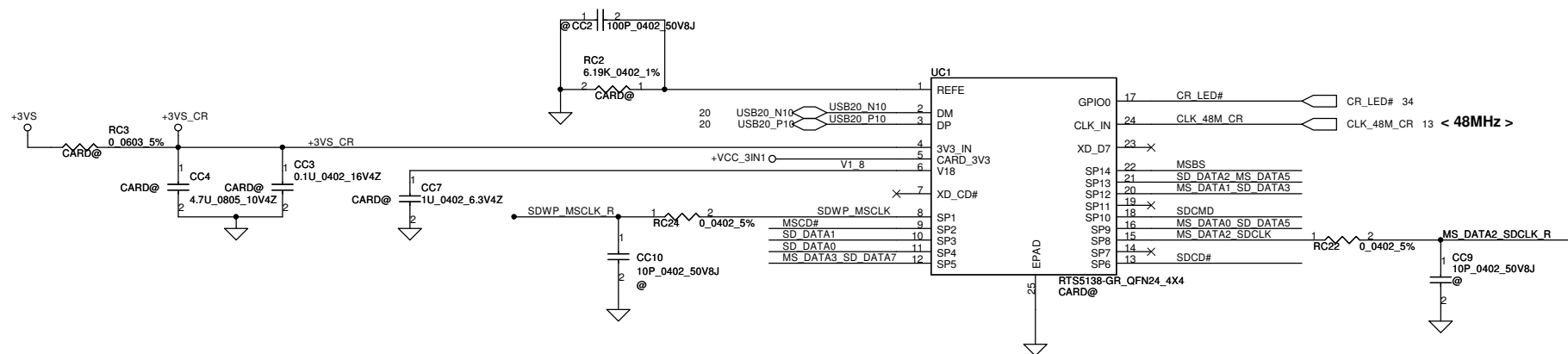
USB Board



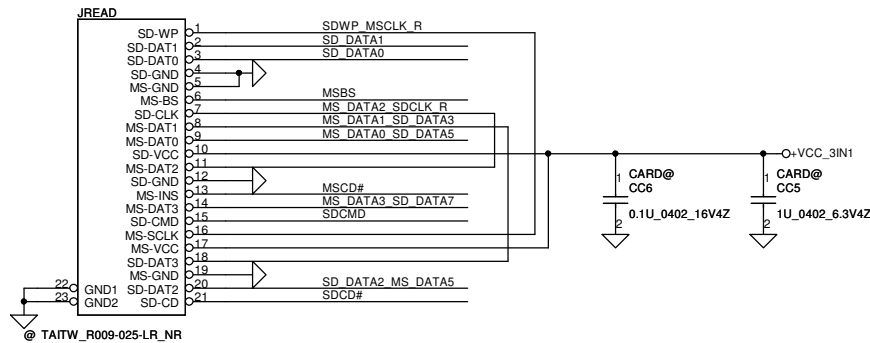
Audio & USB Sub-Board Conn.



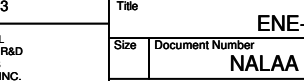
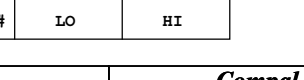
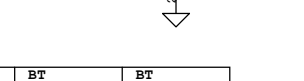
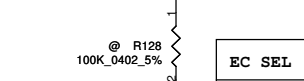
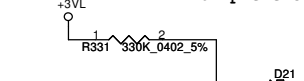
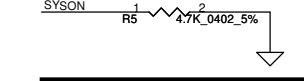
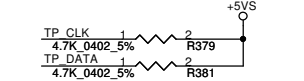
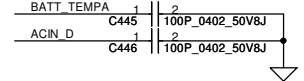
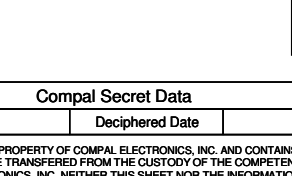
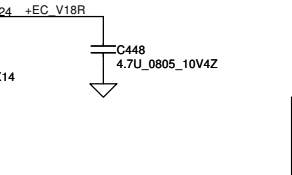
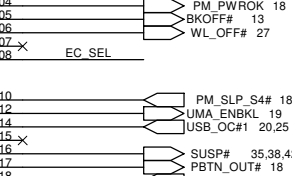
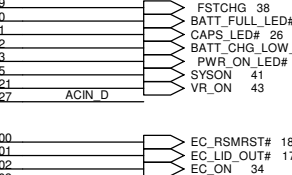
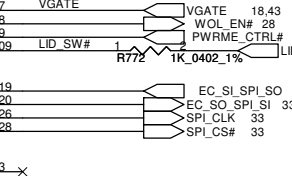
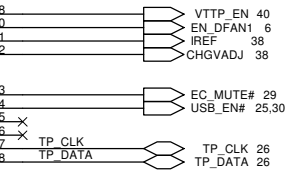
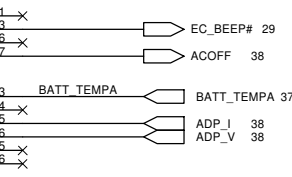
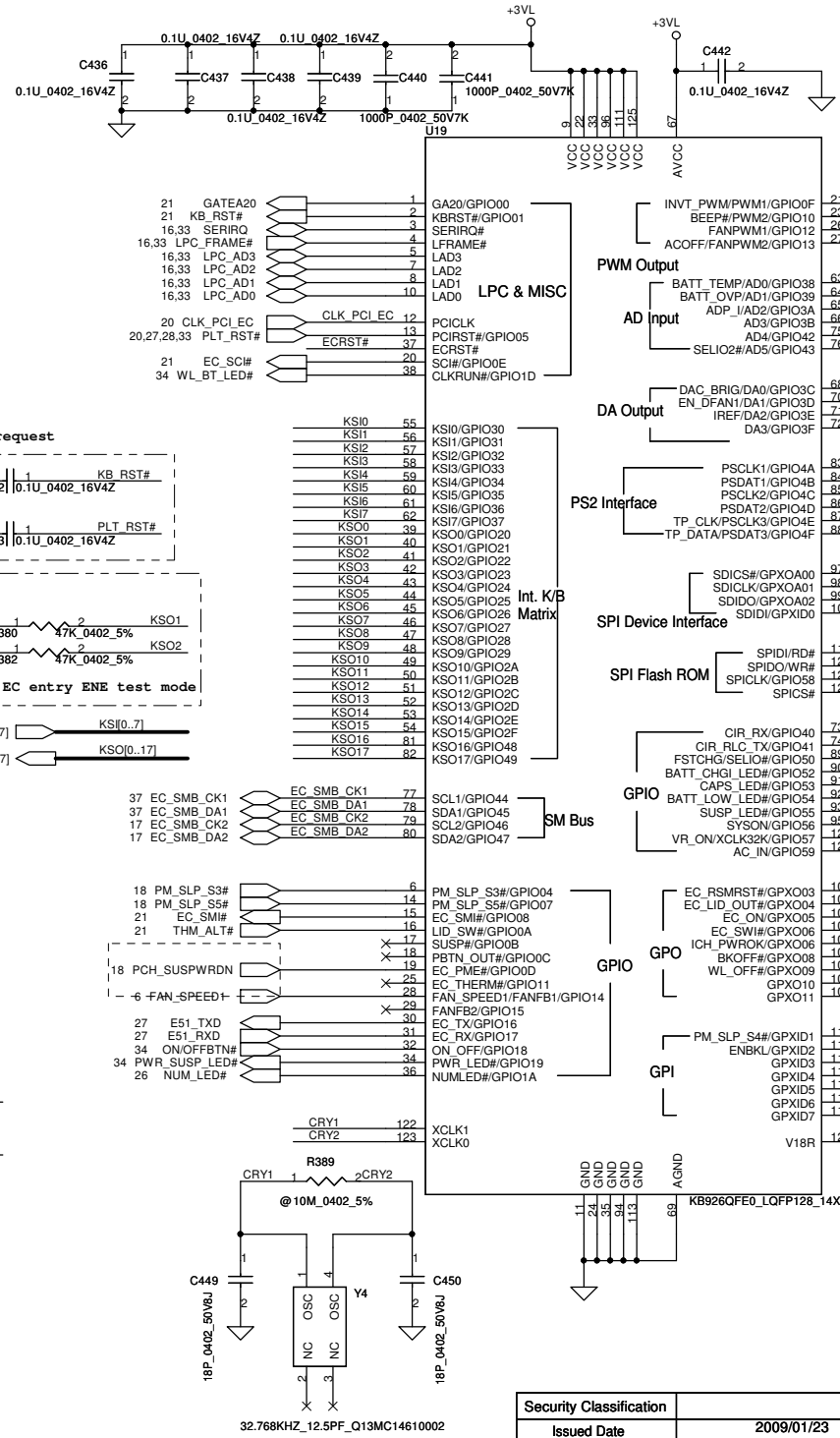
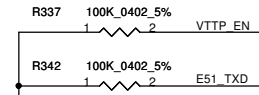
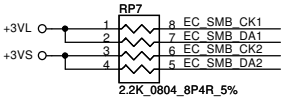
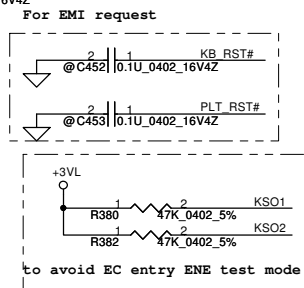
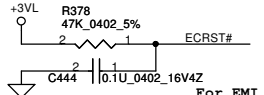
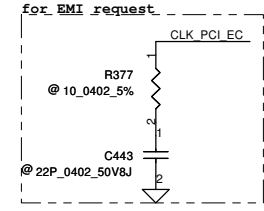
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title
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< 3 in 1 Card Reader >



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Size	Custom	Document Number	NALAA LA-6041P M/B	Rev	1.0
Date:	Tuesday, April 13, 2010	Sheet	31	of	48

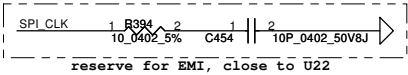
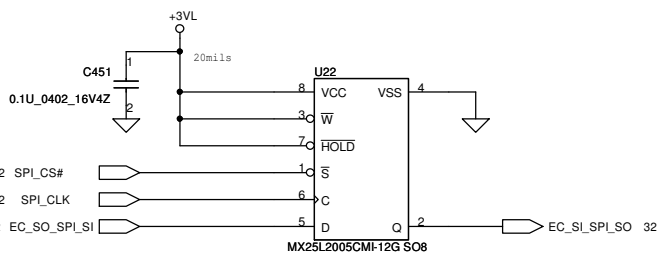


EC SEL	EC Version
High	KB926D3
Low	KB926E0

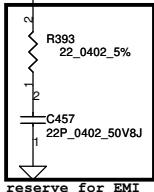
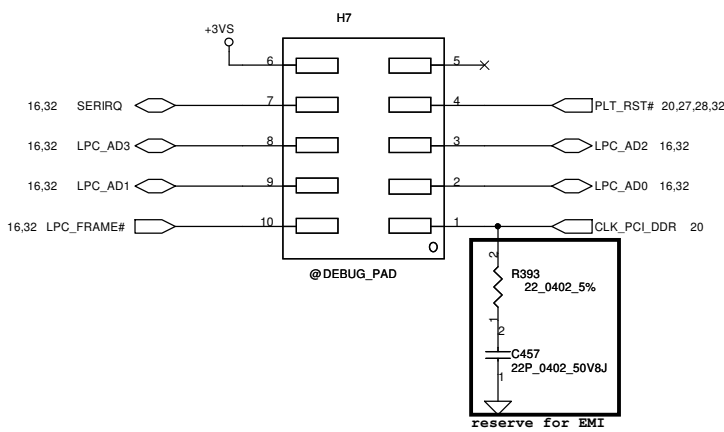
	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

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SPI Flash (256KB)
Socket: SP07000F500 & SP07000H900

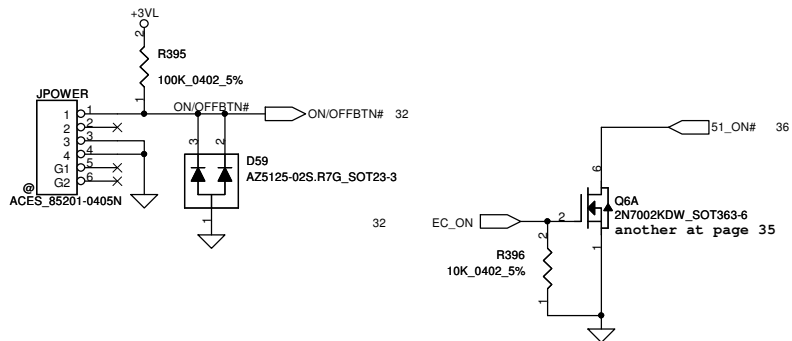


LPC Debug Port
Please place the PAD under DDR DIMM.

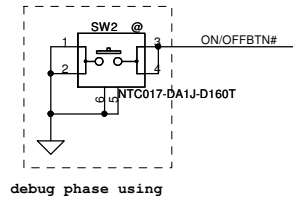


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Power Button

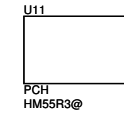
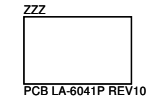


Debug Button

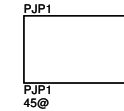


ISPD

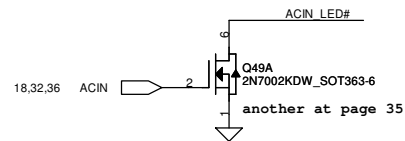
PCB



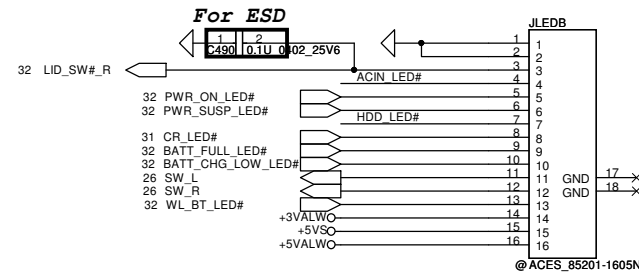
DC-IN
17



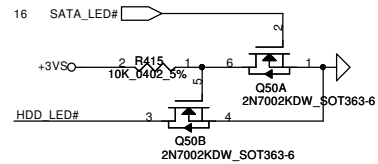
DC-IN LED Control Circuit



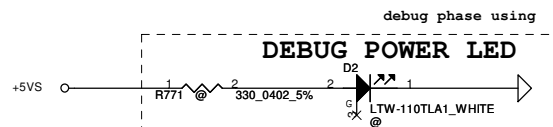
LED/B Conn.



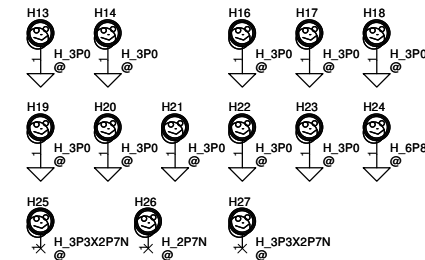
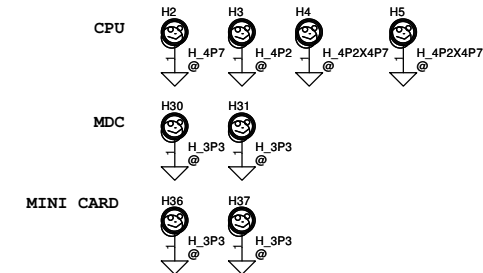
HDD LED Control Circuit



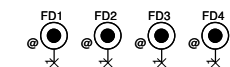
POWER LED Control Circuit



Screw Hole

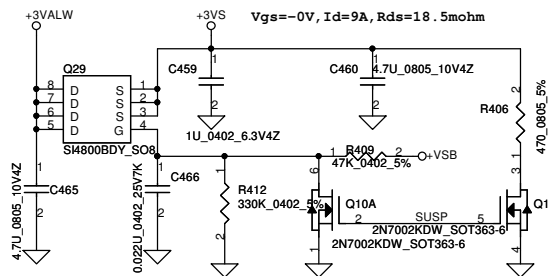


PCB Fedical Mark PAD

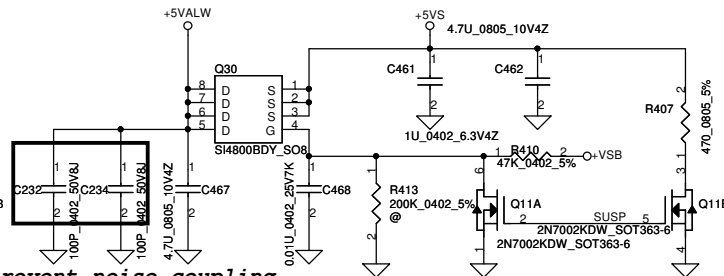


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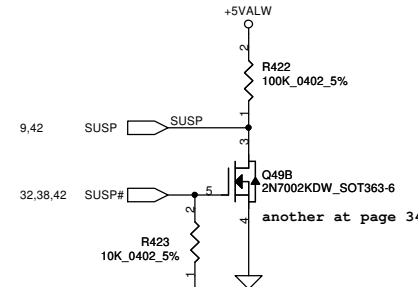
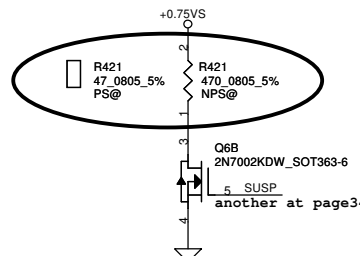
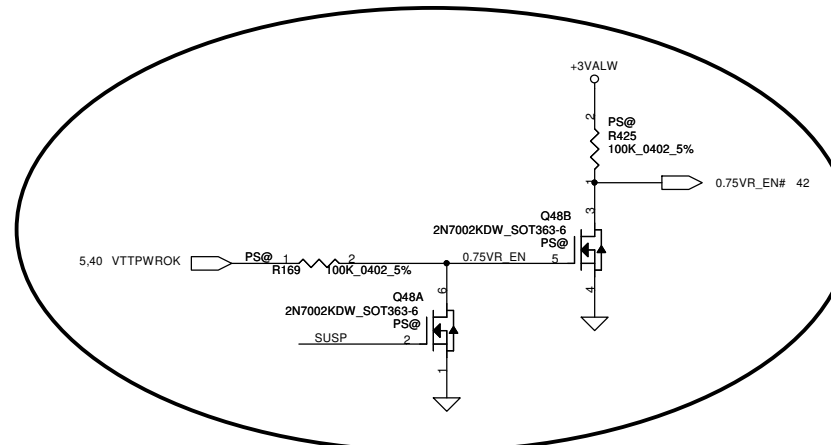
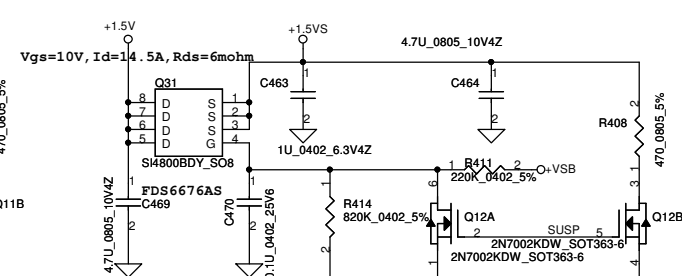
+3VALW TO +3VS



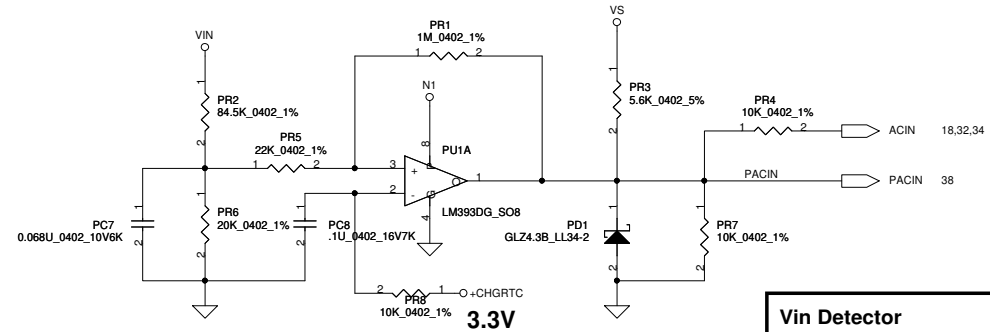
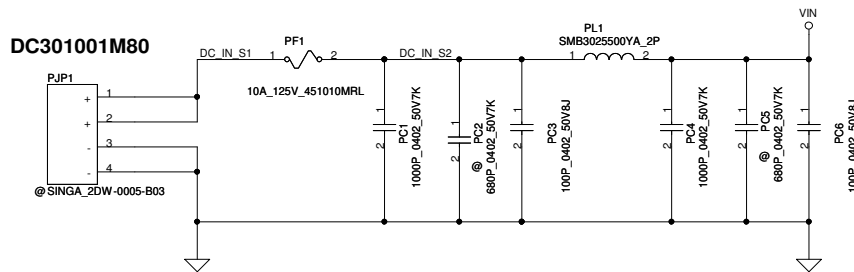
+5VALW TO +5VS



+1.5V to +1.5VS

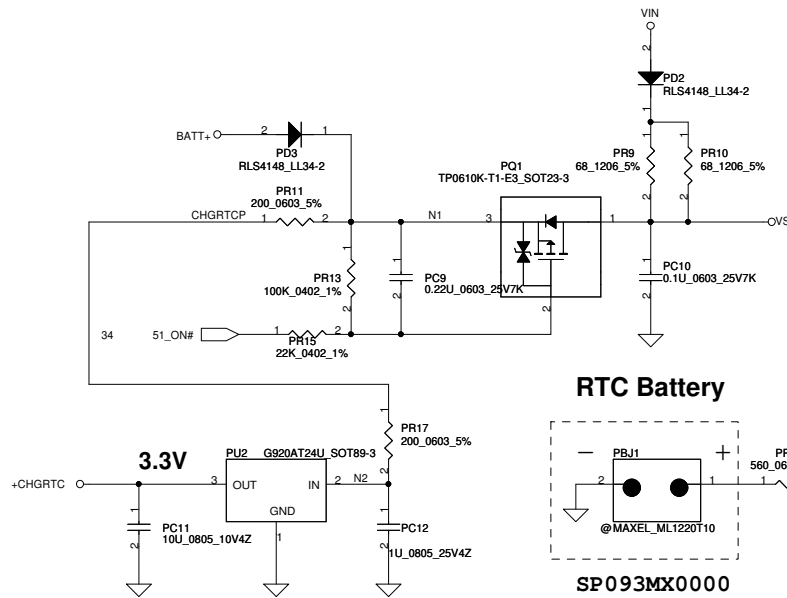


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Size		Document Number		Rev	
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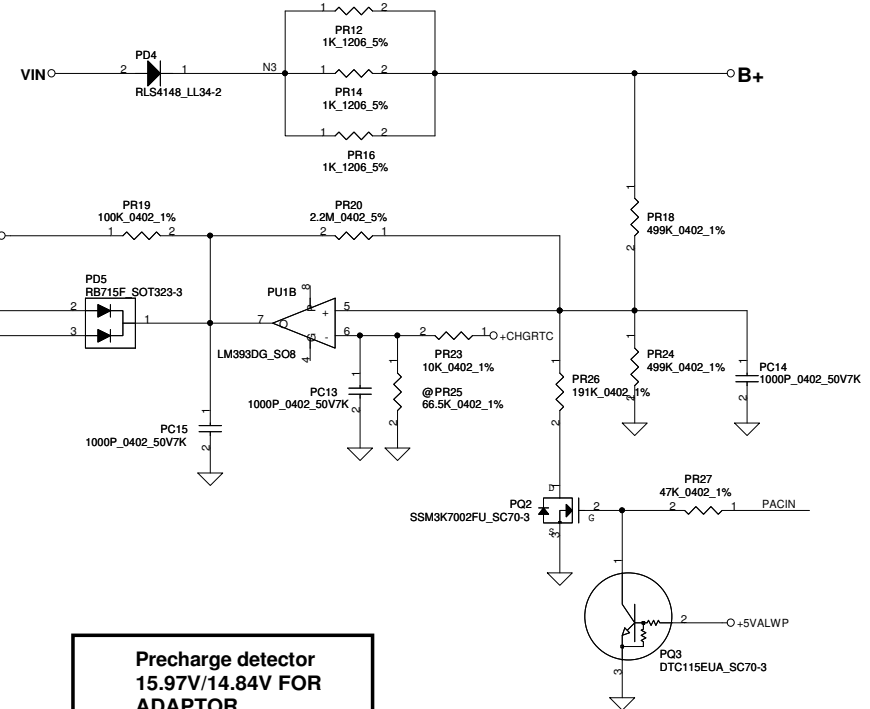
Vin Detector

High 18.384 17.901 17.430
Low 17.728 17.257 16.976

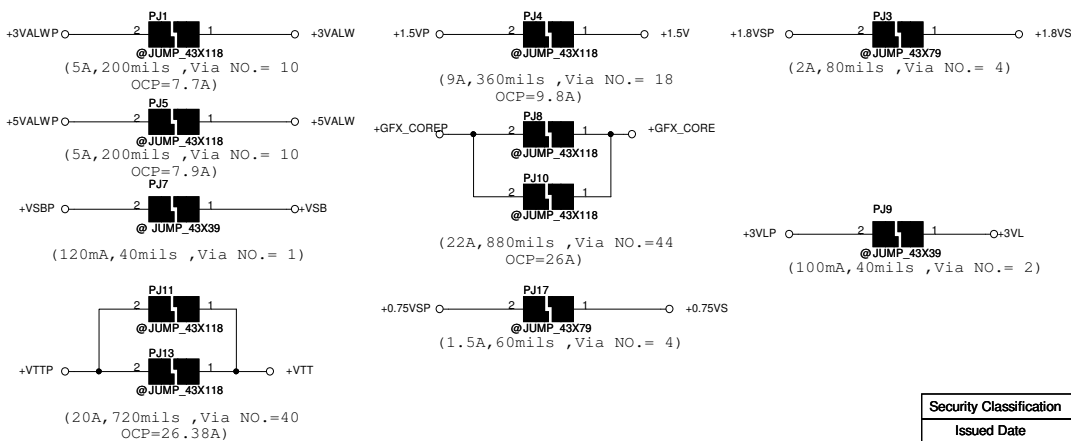


RTC Battery

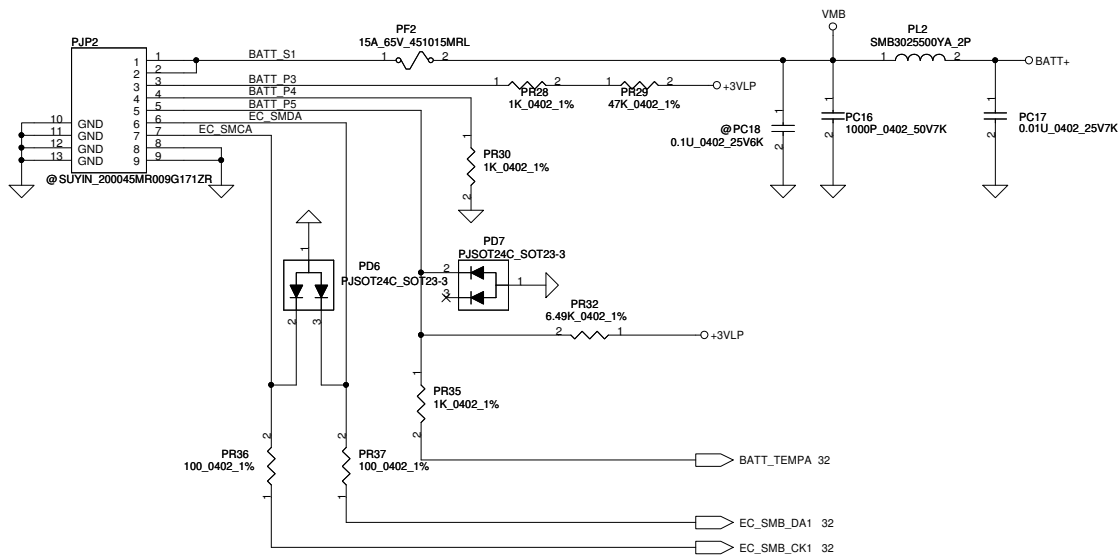
SP093MX0000



Precharge detector
15.97V/14.84V FOR
ADAPTOR



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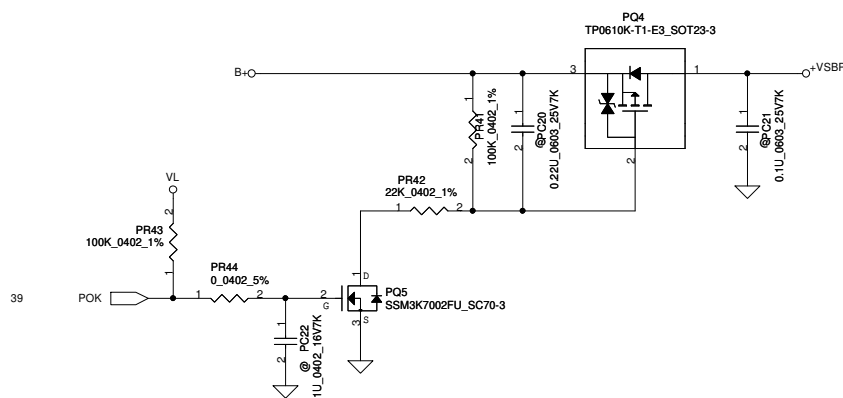
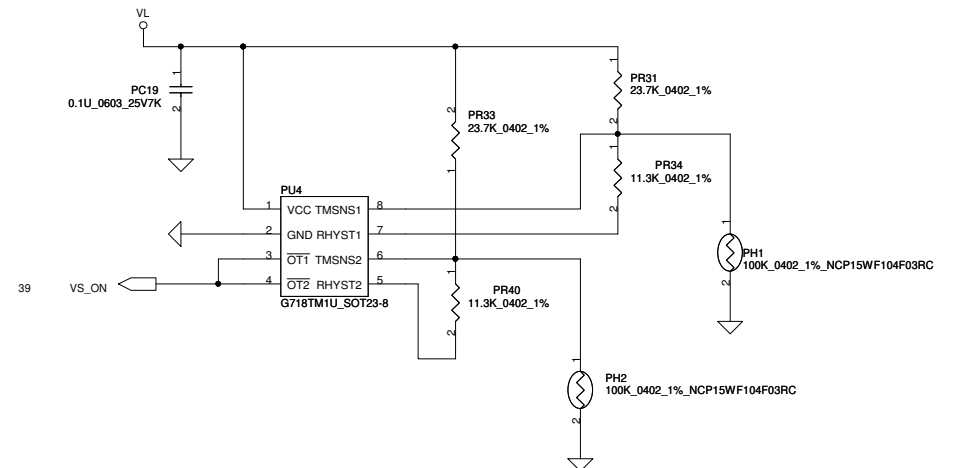


PH1 under CPU botten side :

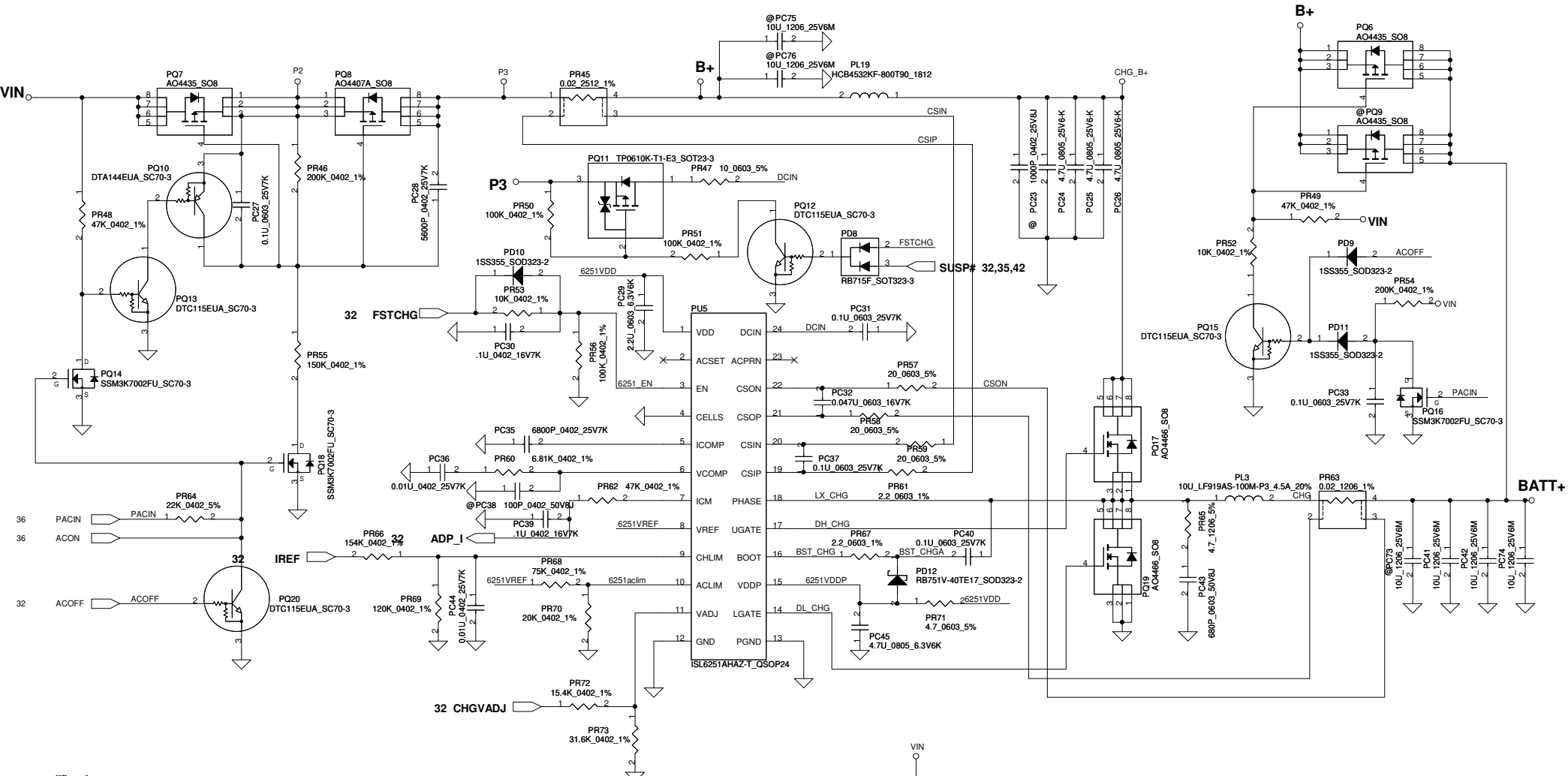
CPU thermal protection at 90 degree C
Recovery at 56 degree C

PH2 near main Battery CONN :

BAT. thermal protection at 90 degree C
Recovery at 56 degree C



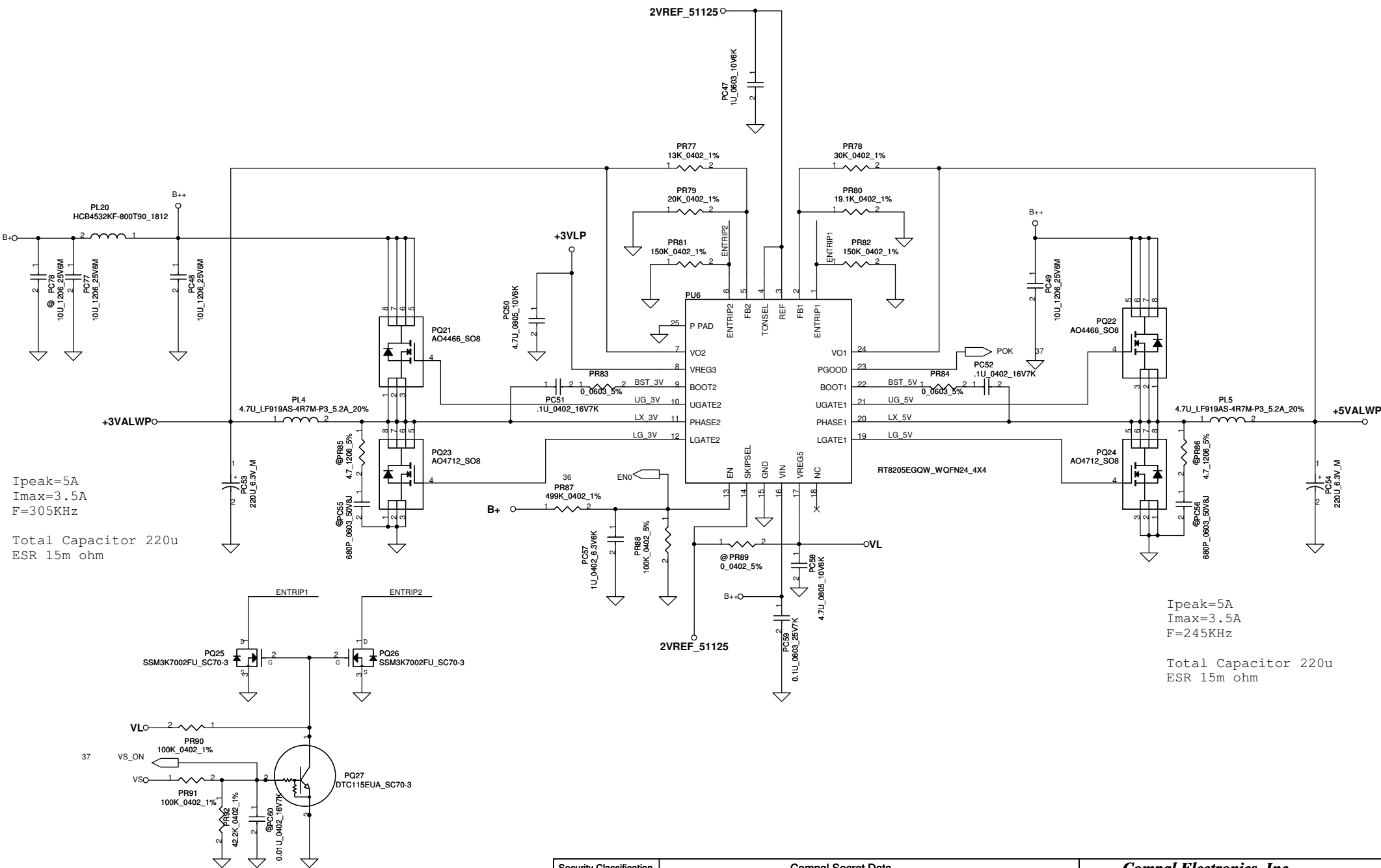
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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CP mode
 $I_{ada} = 0 \sim 3.42A (65W)$ $CP = 92\% \cdot I_{ada}$; $CP = 3.147A$
 $V_{acim} = 1.08V (65W)$ $PR68 = 75k$ $PR45 = 0.02$

CC=0.25A~3A
 $I_{REF} = 1.016 \cdot I_{charge}$
 $I_{REF} = 0.254V \sim 3.048V$
VCHLIM need over 95mV

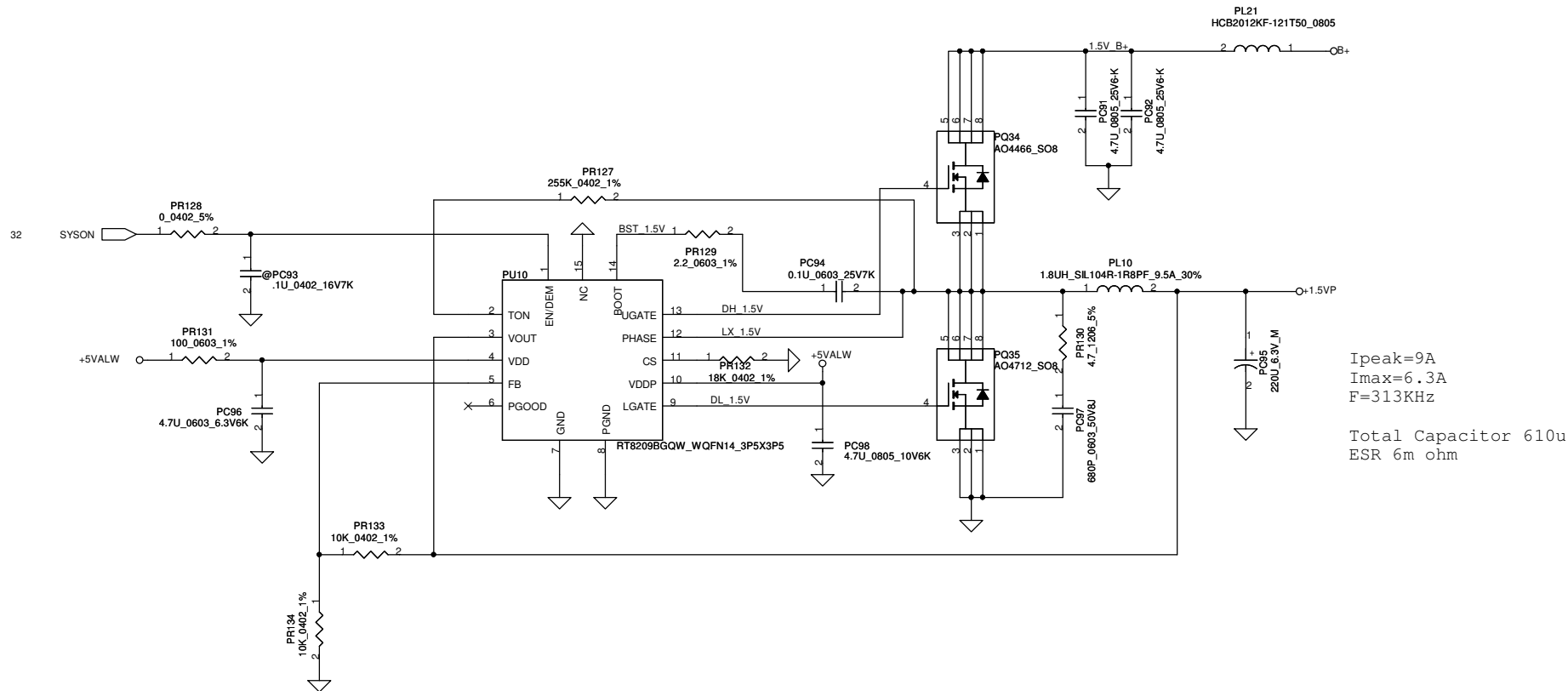
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V



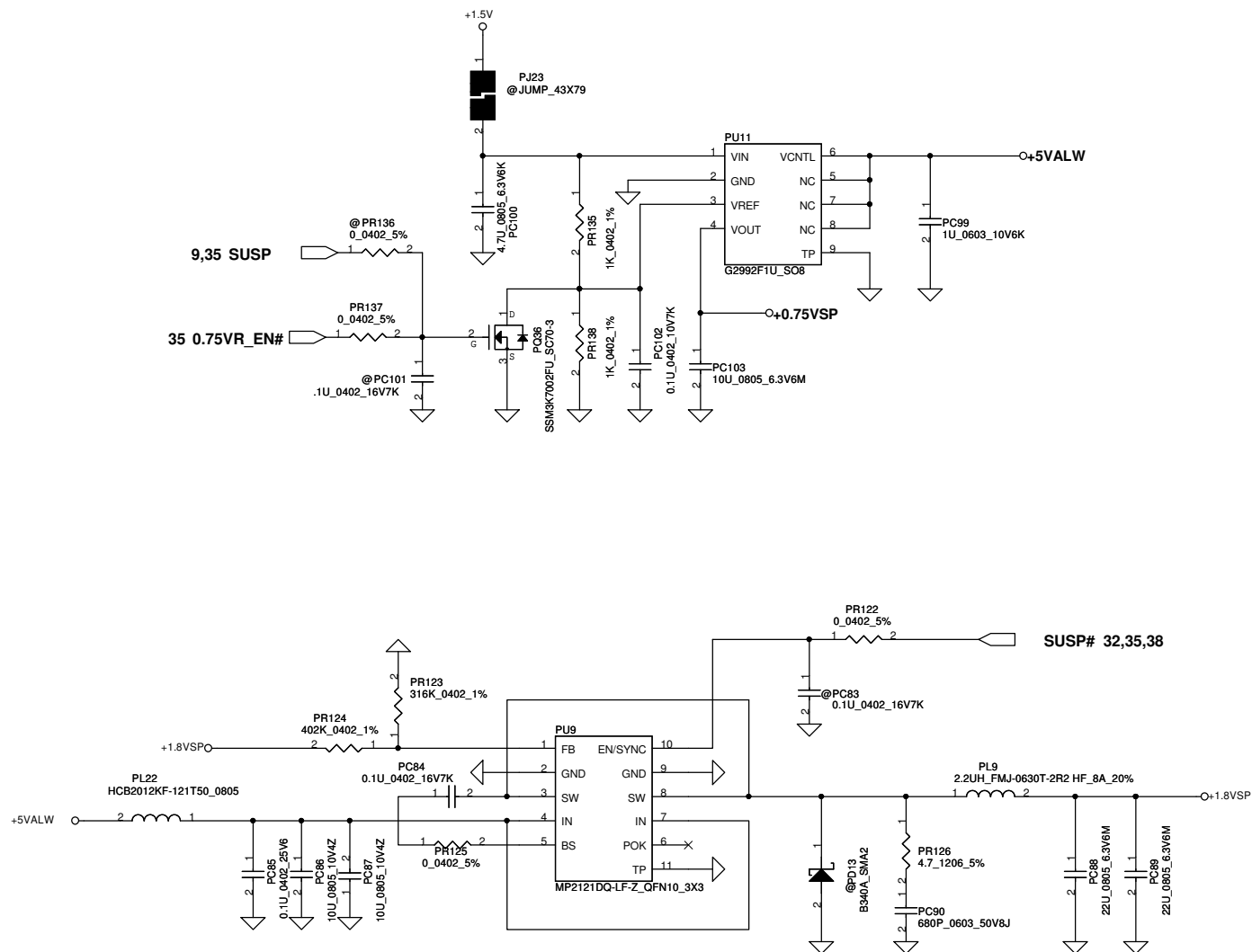
Ipeak=5A
Imax=3.5A
F=305KHz
Total Capacitor 220u
ESR 15m ohm

Ipeak=5A
Imax=3.5A
F=245KHz
Total Capacitor 220u
ESR 15m ohm

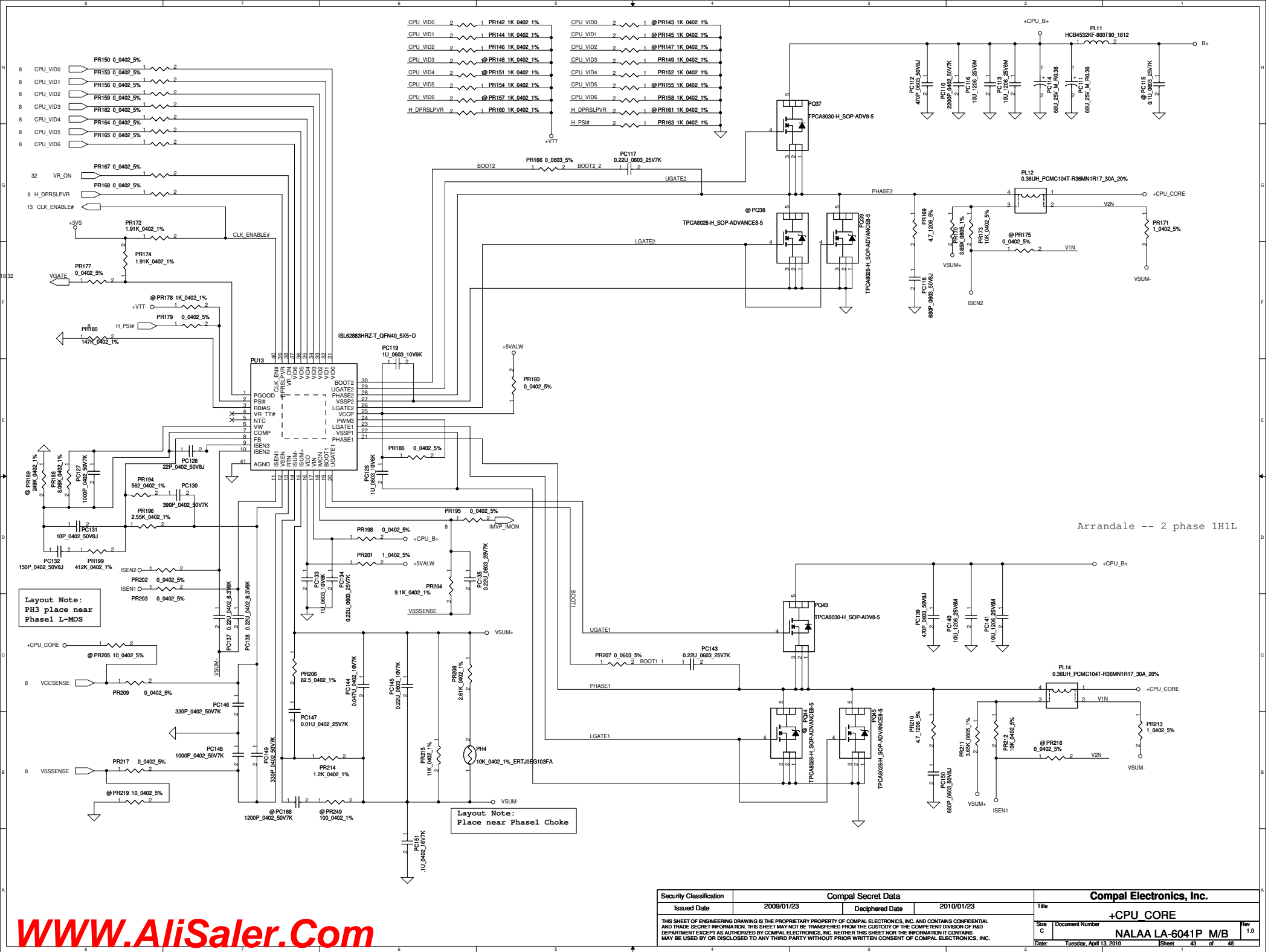
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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PIR (Product Improve Record)

NALAA LA-6041P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
11/26	34		Change C296,C299,C300,CA64,CM1,CM7 from SE072103280 to SE068103K80	For reduce BOM type
12/09	34		Connect JLEDB.15&16 to GND	For T/P SW issue
12/09	25,30		Change U14 & U15 from SA00002XX00 to SA000033H00	For material issue
12/16	15		Change R159 from IHDMI@ to @	For HDMI level shift disable function
12/16	31		Change CC2 from CARD@ to @	For Card Reader issue
12/16	34		Modify JLEDB pin define	For customer concern
12/16	21		Del R222 and connect PCH GPIO45 to GND	For LVDS_SEL (Dual-Channel)
12/16	13		Change U5 from SA00003HQ00 to SA00003HQ10	For CLK GEN update
12/16	27		Add R22 and Net BT_PWR#_R to connect JWLAN Pin5	For BT/WLAN combo Mini Card
12/16	16		Change U13 footprint to M25P80-VMW6TP_SO8 and delete BOM structure.	For delete ROM socket
12/16	34		Change H36, H37 from H_3P3 to H_3P8.	For ME modify
12/16	26		Reverse JBT pin definition	For ME modify
12/16	31		Change CC2 from 0.1u to 100P (SE071101J80) and add BOM structure @.	For Card Reader issue
12/16	34		Change JPOWER footprint to ACES_85201-0405N_4P.	For ME modify
12/16	26		Change JTPB footprint to P-TWO_161011-04021_4P-T.	For ME modify
12/16	34		Change JLEDB footprint to ACES_85201-1605N_16P	For ME modify
12/16	30		Change JUSBB footprint to ACES_85201-20051_20P	For ME modify
12/16	34		Del H15	For ME modify
12/21	34		Change H36,H37 from H_3P8 to H_3P3	For ME modify
12/21	13		Change +LCD_INV from JLVDS.35 to JLVDS.40	For prevent burn issue
12/21	13		Change BKOFF#_R from JLVDS.40 to JLVDS.35	For prevent burn issue
12/23	16,32		Change net name from PWRME_CTRL to PWRME_CTRL#	For signal is LOW active
12/23	08		Add C125 SF000002Y00	For co-lay with C123
12/23	09		Del C128	For del co-lay with C185
12/23	09		Del C140	For del co-lay with C217
12/23	17		Change Y2 P/N from SJ125P0M200 to SJ100003300	For cost down plan
12/23	27		Delete R22 and BT_PWR#_R and add Q25 and BT_CTRL at JWLAN pin5	For BT/WLAN combo Mini Card
12/24	29		Change RA26 to L56 bead 300 ohm FBMA-L10-160808-301LMT(SM010017710)	For EMI issue
12/24	15		Add R96 1K ohm to connect HDMI_HPD and U9.1	For prevent U9 ESD damage issue
12/24	30		Change LA2,LA3,LA4,LA5 to 80 Ohm bead FBMA-L11-160808-800LMT (SM010015410)	For EMI request
12/24	30		Change CA21,CA22,CA25,CA26 to 470P (SE071471J80)	For EMI request
12/24	26		Del R361 BOM structure BT@ (always mount)	For BT function
12/28	26		Change R392 BOM structure from BT@ to @.	For BT function
12/28	26		Change C159,C160,C185,C217,C268 footprint from C_PXC6P3VC220MF60 to C_MP2VU390MC5R7.	
12/28	25		Change JODDB footprint to ACES_88058-120N_12P-T.	For DFX request
12/29	13		Del C292	Only for NSWAA
12/29	28		Change UL3 P/N from SP050005W00 to SP050005V00	For EMI request
12/29	28		Change UL1 P/N from SA00003PO00 to SA00003PO10	For IC chip revise version
01/05	06		Change C4 from SE068102J80 to SE074102K80	For component common design

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NALAA LA-6041P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01/19	13		Change BKOFF#_R from JLVDS.35 to JLVDS.33	For prevent burn issue
01/27	32		Add pull down R40 10Kohm at VR_ON.	For prevent leakage for CPU_CORE
01/27	25		Change D18 from SCA00000A00 to SC600001600	For ESD request
01/27	13,26,30,34		Change D57,D58,D59,DA6,DA9 from SCA00000G00 to SCA00001A00	For ESD request
01/27	15		Add pull down R148 2.2Kohm at HDMI_TXC-.	For UMA HDMI level shift display compatibility issue
01/27	28		Change UL3 from SP050005W00 to SP050005V00	For ESD request
01/27	29		Change UA1 from SA00003QR00 to SA00003QR10	For Realtek update
01/27	32		Change R128 BOM structure from mount to un-mount.	For EC update
01/27	32		Change R130 BOM structure from un-mount to mount.	For EC update
01/27	32		Change U19 from SA00001J580 to SA00001J5A0.	For EC update
02/01	30		Change JSPK pin define	For common SPK material
02/01	16		Add D19 & R133 between +RTCVCC and RTCVREF.	For prevent RTC empty then can not boot up issue
02/01	19		Change R77 from SD028100280 to SD028100380	For INTEL issue (pending interrupts from the PCH for unused HDMI ports)
02/01	05		Add C225	For prevent noise issue
02/04	22		Change L12 from SM010028480 to SHI00002K00	For CRT wave issue
02/04	28		Change LL1 from SHI00004T00 to SHI0000AA00	For package limitation, Realtek criteria, 2ND source reason
02/04	28		Change CL13 from SE000000I10 to SE107475K80	For package limitation, Realtek criteria, 2ND source reason

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NALAA LA-6041P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
02/23	15		Change R167 BOM structure from @ to IHDMI@.	For reduce HDMI choke plan
02/23	15		Change R163 BOM structure from IHDMI@ to @.	For reduce HDMI choke plan
02/23	15		Change R160 from SD028330180 (3.3K ohm) to SD034390180 (3.9K ohm).	For reduce HDMI choke plan
02/23	15		Change L8,L9,L10,L11 BOM structure from IHDMI@ to @.	For reduce HDMI choke plan
02/23	15		Change R157,R173,R175,R180,R182,R183,R187,R188 BOM structure from @ to IHDMI@.	For reduce HDMI choke plan
02/23	22		Change L12 from SHI00002K00 (10UH +-20%) to SD008100B80 (1 ohm +-1% 0805).	For CRT wave issue
02/23	16		Delete D19 & R133	For prevent RTC empty then can not boot up issue
02/23	23		Change U54,C2,C18 BOM structure to @.	For reserve HDA power rail to +1.5V
02/23	26,34		Change SW2,SW4 from SN100000F00 to SN100002Y00 and add BOM structure @ at SW2.	For cost concern
03/09	29,32		Add Net EC_MUTE# from EC pin 83 to codec Pin4	For system has abnormally noise after S3 resume.
03/09	29		Add pull Low RA45 4.7K ohm.	For system has abnormally noise after S3 resume.
03/09	29		Change CA16 BOM structure to @.	For system has abnormally noise after S3 resume.
03/11	22		Add L57.	For prevent EMI and CRT wave issue.
03/11	25,30		Change U14,U15 from SA000033H00 to SA00002XX00.	For sourcer suggestion.
03/11	25,30		Change ZZZ from DA60000GC00 to DAZ0CK00100.	For Pre-MP phase.
03/11	06		Change U1 from SA00002XA00 to SA000035G00.	For voltage drop issue.
03/11	34		Change R771,D2 BOM structure to @.	For Pre-MP phase.
03/11	22		Add net name +3VS_VCCADAC_R	For net nameing rule
03/15	34		Add R772 & C490 and net name LID_SW#_R	For prevent ESD damage
03/15	22		Change L12 from SD008100B80 to SD014100B80.	For package size
03/16	29		Change CA12.1, RA12.2, CA18.2 connect to GNDA	For high frequency noise issue at S0
03/16	13		Add C231	For prevent noise coupling
03/17	35		Add C232,C234	For prevent noise coupling
03/17	31		Add CC9,CC10,RC22,RC24	For EMI request
03/17	31		Del RC2,RC3,CC7,CC8	For EMI request
03/20	13		Change C213 from SE070104Z80 to SE000000K80.	For prevent noise coupling
03/20	13		Change C231 from SE071101J80 to SE000000K80.	For prevent noise coupling
03/23	25		Change D18 BOM structure to @.	For EMI remove

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2009/10/20		45-54	Release	
2009/12/21		39	Change PR92 to 42.2K ohm	circuit modify
2009/12/21		40	Change PR95 to 2.43K ohm,PR101,PC71,PC72 to unmount ,PR98 to 6.49K ohm	circuit modify
2009/12/21		42	Change PR136 to unmount,PR137 to mount,PC90 toSE024681J80	circuit modify
2009/12/21		43	Change PQ44 to unmount,PQ45 to mount	EMI request
2009/12/28		43	Change PC111,PC114 to 68U	DFB request
2009/12/29		37	Change PR31 and PR33 to19.6K ohm, PR34 to 8.66K ohm,PR40 to 7.87K ohm	circuit modify
2009/12/29		38	Add PR139(0_0402_5%)	EMI test request
2009/12/29		44	Change PH5 to SL200000500	circuit modify
2010/01/05		43	Change PR169,PR210,PC118 and PC150 to mount	EMI request
2010/01/05		44	Change PR235 and PC163 to mount	EMI request
2010/02/03			Change PR196 to 2.55K ohm,PR204 to 9.1K ohm	circuit modify
2010/02/03		38	Change PC24,PC25,PC26 to 10U_1206,PR67 to 2.2 ohm PC74 to mount,PC23 to 1000P	EMI request
			Delete PR139	circuit modify
2010/02/03		39	Change PQ27 to DTC115EUA_SC70-3 Add PC77	EMI request
2010/02/26		37	Change PR31,PR33 to 23.7K ohm,PR34,PR40 to 11.3K ohm Add PD6,PD7	Thermal request EMI request
2010/03/16		38	Change PC24,PC25,PC26 to 4.7U_0805, PC75,PC76 to unmount,	For PCB noise ossue
2010/03/18		40	Change PR247 to 47K ohm	Modify GFX load line
2010/04/02		40	Change PR98 to 9.76K ohm	circuit modify(cut in AON6718L)

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