Compal Confidential

Model Name : VIUS3/S4
File Name : LA-8952PR01
BOM P/N:43

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VIUS3/S4 M/B Schematics Document

Intel Ivy Bridge ULV Processor + Panther Point PCH
AMD Seymour XT

2013-01-07

REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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File Name :VIUS3/VIUS4

Chief River

AMD Seymour XT
23mm *23mm
VRAM 128MB*16
gDDR3*4

PCI-E X16
Gen 2
UP TO 1G

Intel
IVY Bridge SV/ULV
(Sandy Bridge)
Processor
BGA1023

DDR3-SO-DIMM X1
BANK 0, 1

Dual Channel
DDR3-1066/1333(1.5V) for Sandy Bridge
DDR3-1600(1.5V) for Ivy Bridge

FDI *8
100MHz
2.7GT/s

DMI2 *4
100MHz
5GT/s

Std HDMI Connector
HDMI 1.4a

LVDS Connector
PX 5.0

Intel
Panther Point
HM77/HM70
FCBGA 989 Balls
25mm*25mm

6*SATA
(port0,1 Support SATA3)
SATA3.0 HDD CONN
SATA3.0 HDD (SSD)

4*USB3.0
14*USB2.0
USB PORT 3.0 x1 (Left)
USB PORT 2.0 x2 (Right)
IO Board
Card Reader RTS 5178 (2in1)
IO Board
CMOS Camera
BlueTooth CONN
WLAN/WiMAX
WWAN
Touch Screen

PCI Express (Half)
Mini card Slot 1
WLAN/WiMAX
USB(WiMAX)
PCI-E(WLAN)

PCI Express (Full)
Mini card Slot 2
SSD
mSATA(SSD)
Gen 2

6*PCI-E x1

WLAN/WiMAX

LAN(10/100/Giga)
Realtek
8105E-VD (10/100)
8111F-VL (Giga)

RJ45 CONN

SPI ROM
BIOS
4MB*1
2MB*1

LPC BUS

EC
ENE KB9012

Int.KBD

Touch Pad

Thermal Sensor
EMC1403

HD Audio

Audio Codec
RealTek
ALC259-VC2

2Channel Speaker
Single Digital MIC
Audio Combo Jack
(APPLE type)
HeadPhone Output
Microphone Input
IO Board

Sub-borad
POWER BOARD
LED BOARD
IO Board

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V +1.5V_IO	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

EC SM Bus1 address

Address

Device	
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

AMD-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

USB Port Table

USB 3.0	USB 2.0		Port	3 External USB Port
xHCI1	EHCI1	UHCI0	0	
xHCI2			1	USB 3.0 Port (Left Side)
xHCI3		UHCI1	2	Mini Card(WLAN)
xHCI4			3	Touch Panel
		UHCI2	4	X (USB PORT disabled on HM70)
			5	X (USB PORT disabled on HM70)
		UHCI3	6	X (USB PORT disabled on HM70)
			7	X (USB PORT disabled on HM70)
	EHCI2	UHCI4	8	USB/B (Right Side USB-BD)
			9	USB/B (Right Side USB-BD)
		UHCI5	10	USB Port (Right Side CR-BD)
			11	Camera (LVDS)
		UHCI6	12	X (USB PORT disabled on HM70)
			13	X (USB PORT disabled on HM70)

12/12/24

HM70 Disable xHCI3,xHCI4

BOM Structure Table

BTO Item	BOM Structure
INTEL UMA only	UMA@
GPU:Seymour XT	PX@
HDMI	HDMI@
HDD1 (HM77 SATA 3.0)	HDD1@
HDD2 (HM70 SATA 2.0)	HDD2@
Intel-USB3.0	USB3@
PCH HM77@	HM77@
PCH HM70@	HM70@
10/100 LAN	8105@
GIGA LAN	8111@
AOAC	AOAC@
CMOS	CMOS@
Deep S3	DS3@
mSATA SSD	mSATA@
Connector	ME@
45 LEVEL	45@
Unpop	@

SATA Port Table

	HM77	HM70	
SATA P0	GEN3/2/1	GEN3/2/1	SSD
SATA P1	GEN3/2/1	Disable	HDD (HM77)
SATA P2	GEN2/1	GEN2/1	HDD (HM70)
SATA P3	GEN2/1	Disable	
SATA P4	GEN2/1	GEN2/1	
SATA P5	GEN2/1	GEN2/1	

HM70 Disable P1,P3

PCIe Port Table

	HM77	HM70	
PCIe P1	Enable	Enable	LAN
PCIe P2	Enable	Enable	WLAN
PCIe P3	Enable	Enable	
PCIe P4	Enable	Enable	
PCIe P5	Enable	Disable	
PCIe P6	Enable	Disable	
PCIe P7	Enable	Disable	
PCIe P8	Enable	Disable	

HM70 Disable P5,P6,P7,P8

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Power-Up/Down Sequence

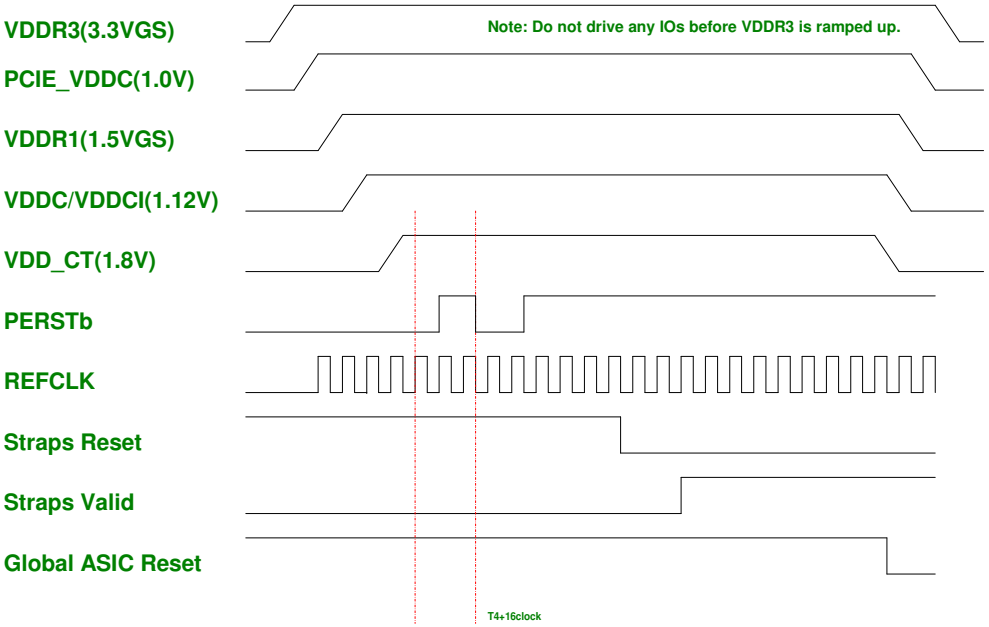
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



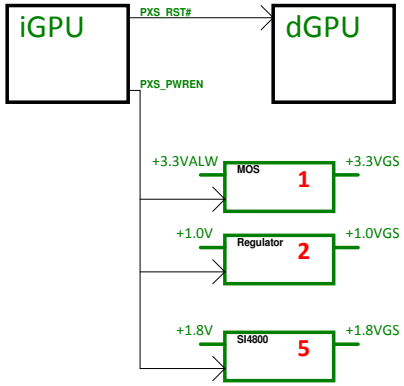
Without BACO option :

PXS_RST# : Low -> Reset dGPU ; High ->Normal operation
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PXS_RST# : High ->Normal operation (dGPU is not reset on BACO mode)
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	~~1679mA~~
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode) BIF_VDDC=VGA_CORE When GPU enable BIF_VDDC=1.0V When BACO	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



CPU part

UCPU1 CPU1@ — I3_3217 1.8G — SA00005L5D0
UCPU1 CPU2@ — I5_3427 1.8G — SA00005L950
UCPU1 CPU3@ — I5_2557 1.4G — SA00004VZ50
UCPU1 CPU4@ — 977_1.4G — SA00005BJ40
UCPU1 CPU5@ — I5_3317U 1.7G — SA00005K6E0
UCPU1 CPU6@ — I5_2537 1.4G — SA00004H910
UCPU1 CPU13@ — 987 1.4G — SA00005QH30
UCPU1 CPU15@ — I7-3517U — SA00005K5C0
UCPU1 CPU7@ — I5_2467M 1.6G — SA000004X000
UCPU1 CPU8@ — I3_2367M 1.4G — SA000051H70
UCPU1 CPU9@ — I3_2357M 1.3G — SA00004Q220
UCPU1 CPU10@ — 967_1.3G — SA000051J20
UCPU1 CPU11@ — 957_1.2G — SA00004AY20
UCPU1 CPU12@ — I7-3667U 2G — SA00005LAD0
UCPU1 CPU14@ — I3-2377M 1.5G — SA00005MX80
UCPU1 CPU16@ — I3-2365M — SA00005UH10

PCB part

ZZZ5 — PCB 0R LA-8951P REV0 M/B — DAZ0S900100
ZZZ2 — Hynix S512@ — X7641338L01
ZZZ1 — Hynix H512@ — X7641338L02
ZZZ3 — Hynix SYG@ — X7641338L03
ZZZ4 — Hynix HYG@ — X7641338L04

PCH part

U13 HM70@ — PCH_HM70 — SA00005MQ80

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Title	VGA Notes List		
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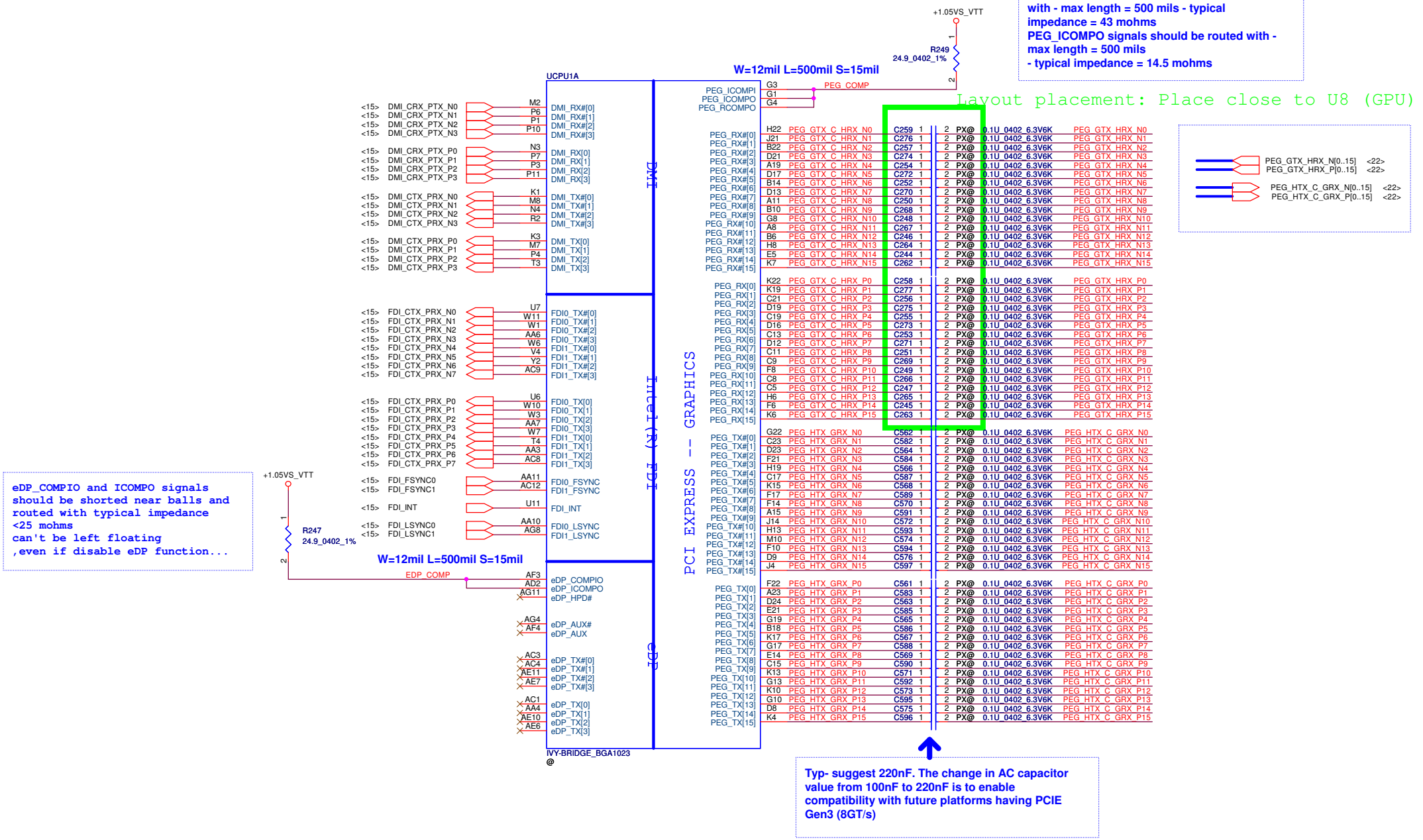

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PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:部ok後請CPU做reset

Follow DG 1.5& Tacoma_Fall2 1.0

reserve

C614 2 @ 1 0.1U_0402_16V4Z H_CPUPWRGD_R

R292 2 1 10K_0402_5%

PROC_SELECT#
PH VCPLL and connect to PCH DF_TVS

<17> H_SNB_IVB#

偵測CPU有無安裝

XBOX 三紅功能

T33 PAD @ H_CATERR#

follow Checklist 1.5

<18,37> H_PECI

+1.05VS_VTT R534 2 1 62_0402_5%

<37,42> H_PROHOT#

R533 56_0402_5%

<18> H_THERMTRIP#

UCPU1B

F49 PROC_SELECT#
C57 PROC_DETECT#
C49 CATERR#
A48 PECI
C45 PROCHOT#
D45 THERMTRIP#

MISC THERMAL

<15> H_PM_SYNC

C48 PM_SYNC

UNCOREPWRGOOD:非CORE外的電OK

<18> H_CPUPWRGD

R305 @ 0_0402_5%

B46 UNCOREPWRGOOD

SM_DRAMPWROK:DRAM power ok

R237 130_0402_1%

BE45 SM_DRAMPWROK

BUF_CPU_RST#

D44 RESET#

PWR MANAGEMENT

IVY-BRIDGE_BGA1023

CLOCKS

BCLK J3 H2 BCLK#
CLK_CPU_DMI <14>
CLK_CPU_DMI# <14>

DPLL_REF_CLK AG3 AG1 DPLL_REF_CLK#
CLK_CPU_DPLL
CLK_CPU_DPLL#

SM_RCOMP0,SM_RCOMP1
W=20mil L=500mil S=13mil

SM_RCOMP2
W=15mil L=500mil S=13mil

DDR3 MISC

SM_DRAMRST# AT30 SM_DRAMRST#

SM_RCOMP[0] BF44 SM_RCOMP0 R272 2 1 140_0402_1%
SM_RCOMP[1] BE43 SM_RCOMP1 R273 2 1 25.5_0402_1%
SM_RCOMP[2] BG43 SM_RCOMP2 R267 2 1 200_0402_1%

DDR3 Compensation Signals

@ C82 1 2 100P_0402_50V8J

SM_DRAMRST# <7>

ESD
C Reserve

JTAG & BPM

PRDY# N53 XDP_PRDY#
PREQ# N55 XDP_PREQ#
T97 T98

TCK L56 XDP_TCK
TMS L55 XDP_TMS
TRST# J58 XDP_TRST#

TDI M60 XDP_TDI
TDO L59 XDP_TDO

0301 Add test point

0419 ESD request to reserve

DBR# K58 XDP_DBRESET#

C2278 1 @ 2 1000P_0402_50V7K

BPM#[0] G58 XDP_BPM#0 T49
BPM#[1] E55 XDP_BPM#1 T90
BPM#[2] E59 XDP_BPM#2 T91
BPM#[3] G55 XDP_BPM#3 T92
BPM#[4] G59 XDP_BPM#4 T93
BPM#[5] H60 XDP_BPM#5 T94
BPM#[6] J59 XDP_BPM#6 T95
BPM#[7] J61 XDP_BPM#7 T96

0301 Add test point

PU/PD for JTAG signals

+1.05VS_VTT

XDP_TMS R20 2 1 51_0402_5%
XDP_TDI R39 2 1 51_0402_5%
XDP_TDO R37 2 1 51_0402_5%

XDP_TCK R40 2 1 51_0402_5%
XDP_TRST# R28 2 1 51_0402_5%

+3VS

XDP_DBRESET# R312 2 1 1K_0402_5%

Tacoma_Fall2 1.0 PH 1K +3VS
Check list 1.5 PH 1K +3VS
Debug port DG1.1-1.3 50~5K ohm

+1.05VS_VTT

CLK_CPU_DPLL# R517 2 1 1K_0402_5%
CLK_CPU_DPLL R516 2 1 1K_0402_5%

Checklist1.5 P.67 Graphis Disable Guide
DIS only SKU eDP disable
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT

+3VALW

+3VS R34 10K_0402_5%

R35 @ 10K_0402_5%

C228 0.1U_0402_16V4Z

U22

<15> SYS_PWROK

<15> PM_DRAM_PWRGD

4PM_SYS_PWRGD_BUF

74AHC1G09GW_TSSOP5

+1.5V_CPU_VDDQ

R238 200_0402_5%

@ R38 39_0402_5%

<10> RUN_ON_CPU1.5VS3#

RUN_ON_CPU1.5VS3#

Q4 2N7002K_SOT23-3

Buffered reset to CPU

+3VS

+1.05VS_VTT

C617 0.1U_0402_16V4Z

R546 75_0402_5%

R544 43_0402_5%

BUF_CPU_RST#

BUFO_CPU_RST#

U45

SN74LVC1G07DCKR_SC70-5

2PCH_PLTRST#

PCH_PLTRST# <17>

C43 0.1U_0402_16V4Z @

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Title: PROCESSOR(3/7) DDRIII

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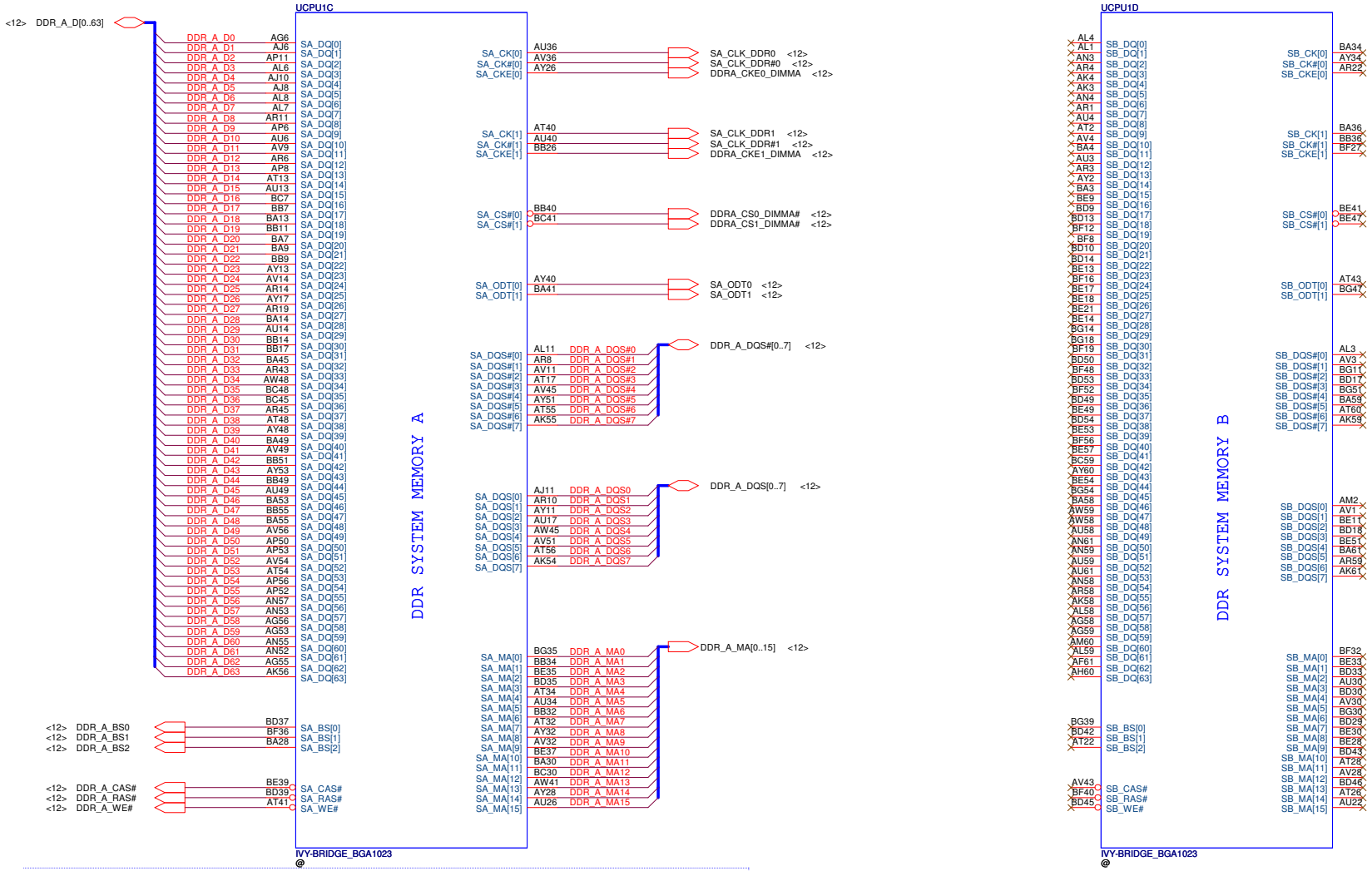

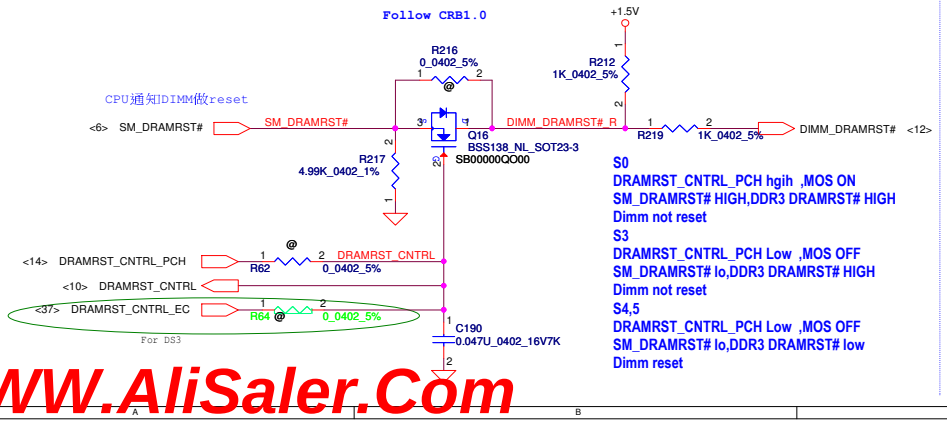

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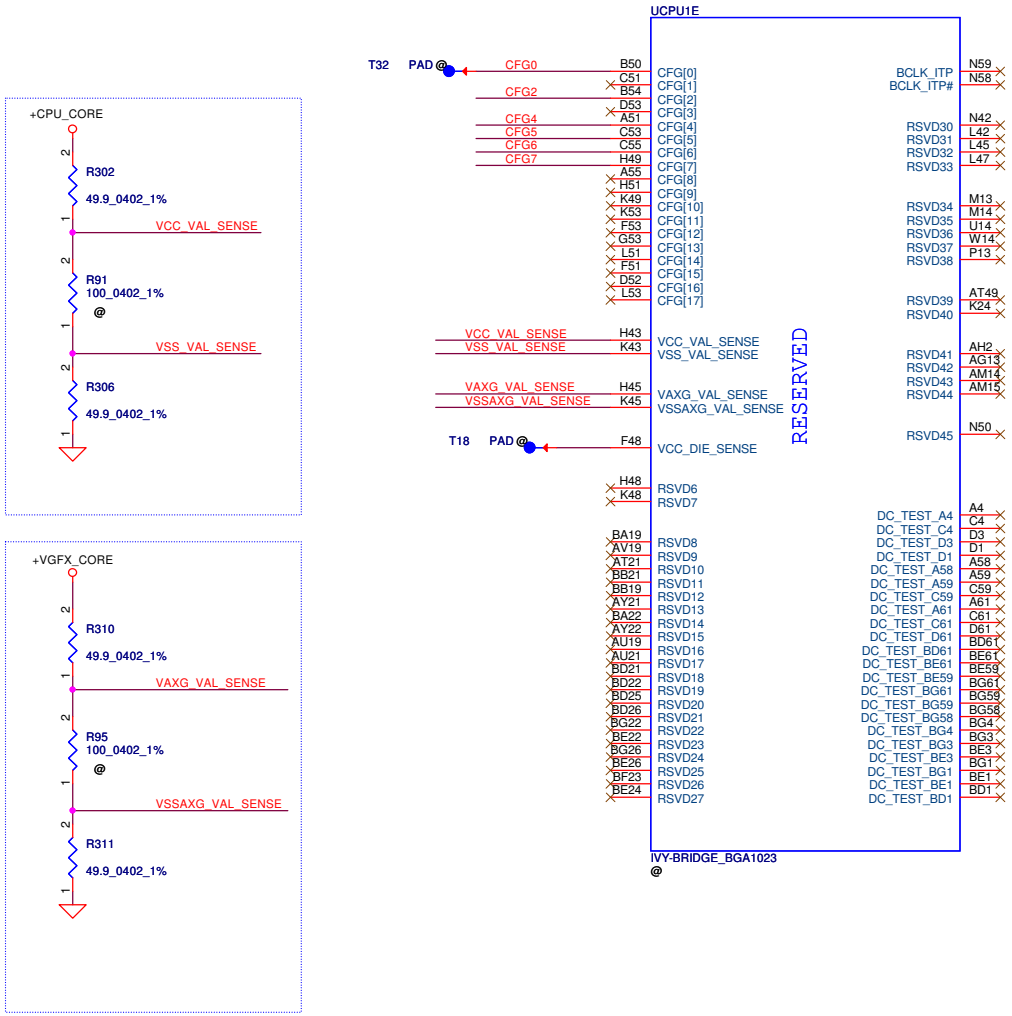
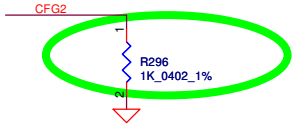


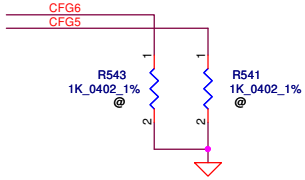
These pins are for solder joint reliability and non-critical to function. For BGA only.

CFG Straps for Processor

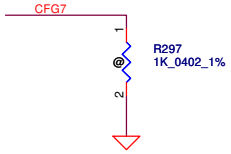


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

eDP enable	
CFG4	* 1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	Tacoma_Fall2 1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.			
Title	PROCESSOR(4/7) RSVD,CFG		
Size: Custom	Document Number: LA-8952P		Rev: 0.1
Date: Thursday, January 10, 2013	Sheet 8 of 55		

POWER

UCPU1F

ULV type
DC 33A

8.5A

+CPU_CORE

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at Power side

CORE SUPPLY

VCC[1] A26
VCC[2] A29
VCC[3] A31
VCC[4] A34
VCC[5] A35
VCC[6] A38
VCC[7] A39
VCC[8] A42
VCC[9] C26
VCC[10] C27
VCC[11] C32
VCC[12] C34
VCC[13] C37
VCC[14] C39
VCC[15] C42
VCC[16] D27
VCC[17] D32
VCC[18] D34
VCC[19] D37
VCC[20] D39
VCC[21] D42
VCC[22] E26
VCC[23] E28
VCC[24] E32
VCC[25] E34
VCC[26] E37
VCC[27] E38
VCC[28] F25
VCC[29] F26
VCC[30] F28
VCC[31] F32
VCC[32] F34
VCC[33] F37
VCC[34] F38
VCC[35] F42
VCC[36] G42
VCC[37] H25
VCC[38] H26
VCC[39] H28
VCC[40] H29
VCC[41] H32
VCC[42] H34
VCC[43] H35
VCC[44] H37
VCC[45] H38
VCC[46] H40
VCC[47] J25
VCC[48] J26
VCC[49] J28
VCC[50] J29
VCC[51] J32
VCC[52] J34
VCC[53] J35
VCC[54] J37
VCC[55] J38
VCC[56] J40
VCC[57] J42
VCC[58] K26
VCC[59] K27
VCC[60] K29
VCC[61] K32
VCC[62] K34
VCC[63] K35
VCC[64] K37
VCC[66] K39
VCC[67] K42
VCC[68] L25
VCC[69] L28
VCC[70] L33
VCC[71] L36
VCC[72] L40
VCC[73] N26
VCC[74] N30
VCC[75] N34
VCC[76] N38

PEG IO AND DDR IO

+1.05VS_VTT

For DDR

VCCIO[1] AF46
VCCIO[3] AG48
VCCIO[4] AG50
VCCIO[5] AG51
VCCIO[6] AJ17
VCCIO[7] AJ21
VCCIO[8] AJ25
VCCIO[9] AJ43
VCCIO[10] AJ47
VCCIO[11] AK50
VCCIO[12] AK51
VCCIO[13] AL14
VCCIO[14] AL15
VCCIO[15] AL16
VCCIO[16] AL20
VCCIO[17] AL22
VCCIO[18] AL26
VCCIO[19] AL45
VCCIO[20] AL48
VCCIO[21] AM16
VCCIO[22] AM17
VCCIO[23] AM21
VCCIO[24] AM43
VCCIO[25] AM47
VCCIO[26] AN20
VCCIO[27] AN42
VCCIO[28] AN45
VCCIO[29] AN48

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at Power side

For PEG

VCCIO[30] AA14
VCCIO[31] AA15
VCCIO[32] AB17
VCCIO[33] AB20
VCCIO[34] AC13
VCCIO[35] AD16
VCCIO[36] AD18
VCCIO[37] AD21
VCCIO[38] AE14
VCCIO[39] AE15
VCCIO[40] AF16
VCCIO[41] AF18
VCCIO[42] AF20
VCCIO[43] AG15
VCCIO[44] AG16
VCCIO[45] AG17
VCCIO[46] AG20
VCCIO[47] AG21
VCCIO[48] AJ14
VCCIO[49] AJ15

+1.05VS_VTT

VCCIO[50] W16
VCCIO[51] W17

+3VS

R521 10K_0402_5%

VCCIO_SEL

R522 10K_0402_5% @

VCCIO_SEL after Ivy bridge ES2 Voltage support		
BC22	*	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

VCCIO_SEL

BC22 VCCIO_SEL

QUIET RAILS

+1.05VS_VTT

VCCPQE[1] AM25
VCCPQE[2] AN22

C553 1U_0402_6.3V6K

+1.05VS_VTT

R531 130_0402_5%

+1.05VS_VTT

R529 75_0402_5%

Place the PU resistors close to CPU

SVID

VIDALERT# A44 H_CPU_SVIDALRT#
VIDSCLK B43 H_CPU_SVIDCLK
VIDSOUT C44 H_CPU_SVIDDAT

R528 43_0402_1%
@R527 0_0402_5%
@R530 0_0402_5%

VR_SVID_ALRT# <50>
VR_SVID_CLK <50>
VR_SVID_DAT <50>

Place the PU resistors close to VR

+CPU_CORE

R79 100_0402_1% @

R281 100_0402_1%

SENSE LINES

VCC_SENSE F43 VCCSENSE_R
VSS_SENSE G43 VSSSENSE_R

@R282 0_0402_5%
@R289 0_0402_5%

VCCSENSE <50>
VSSSENSE <50>

R288 100_0402_1%

R513 10_0402_5%

+1.05VS_VTT

VCCIO_SENSE AN16
VSS_SENSE_VCCIO AN17

VCCIO_SENSE <47>
VSSIO_SENSE_L <47>

R512 10_0402_5%

Check list 1.5

Should change to connect form power circuit & layout differential with VCCIO_SENSE.

IVY-BRIDGE_BGA1023

@

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Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom	LA-8952P	0.1

Date: Thursday, January 10, 2013 Sheet 9 of 55

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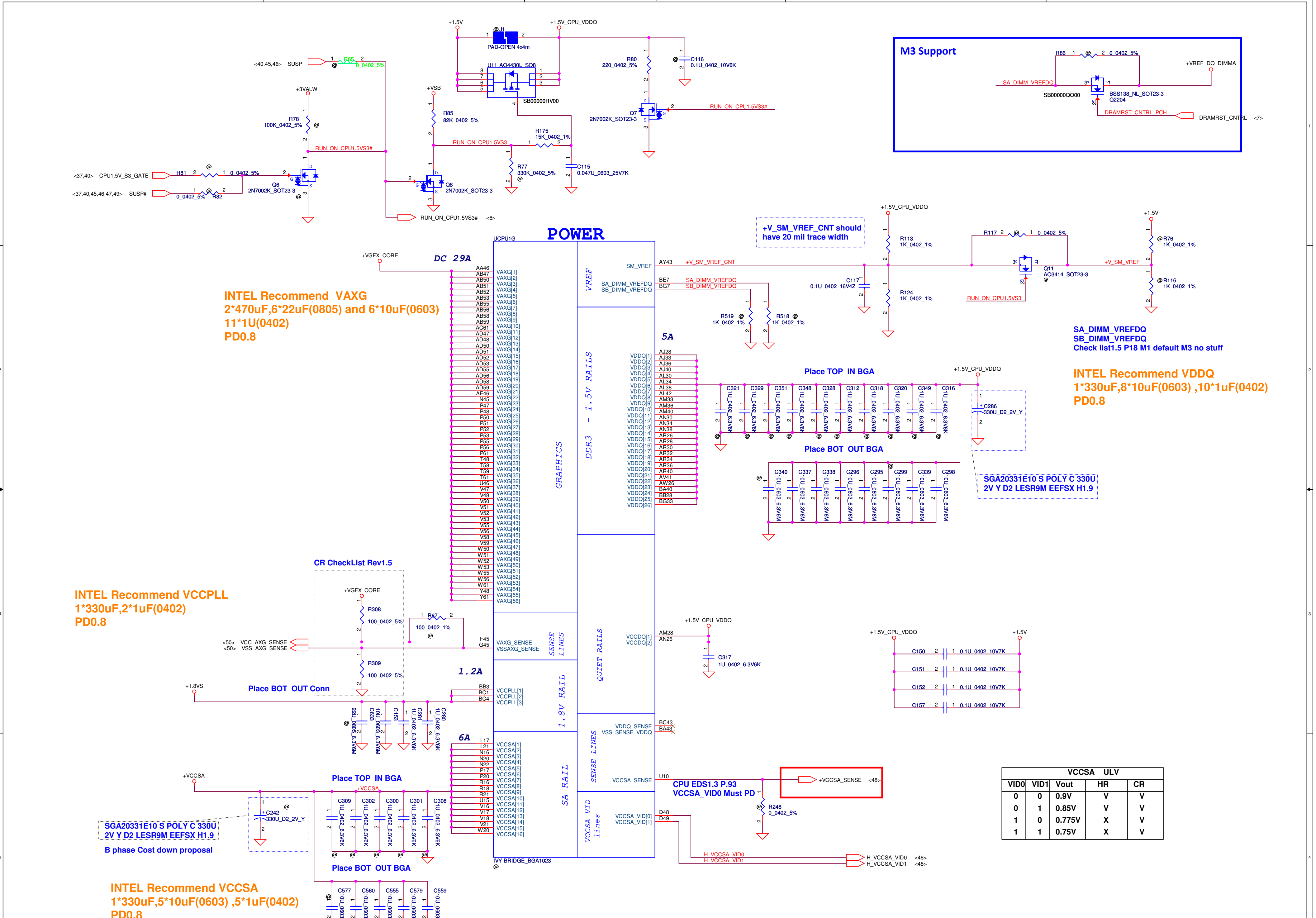

VCCSA ULV				
VID0	VID1	Vout	HR	CR
0	0	0.9V	V	V
0	1	0.85V	V	V
1	0	0.775V	X	V
1	1	0.75V	X	V

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

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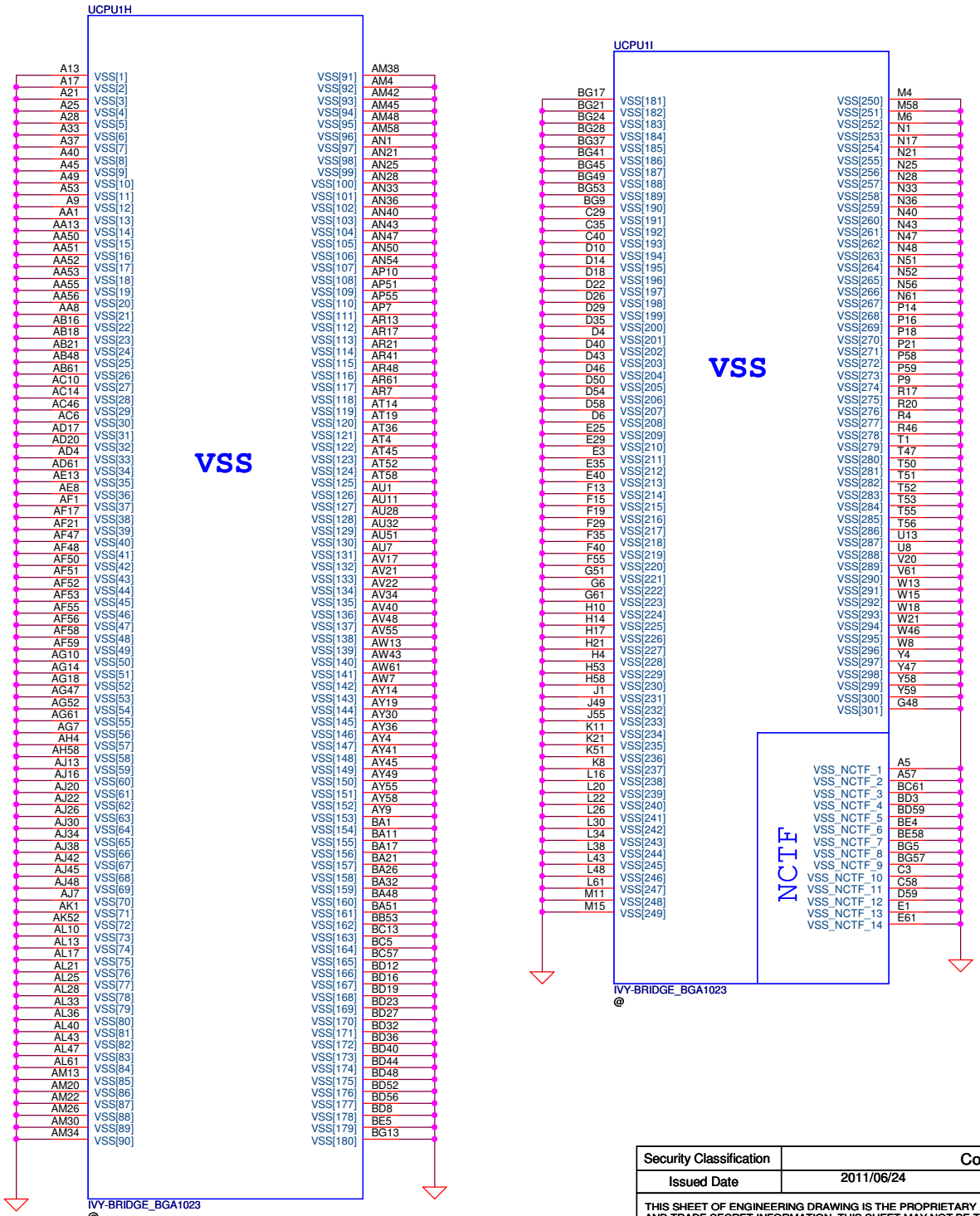

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number: LA-8952P | Rev: 0.1

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All VREF traces should have 10 mil trace width

DDR_A_DQS#[0..7] <7>
DDR_A_DQS[0..7] <7>
DDR_A_D[0..63] <7>
DDR_A_MA[0..15] <7>

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1.203,204

JDIMM1
TYCO_2-2013022-1
ME@

Channel A

<Address: SA1:SA0=00>

DIMM_1 Standard H:4.0mm

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: DDRIII DIMMB

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Date: Thursday, January 10, 2013 | Sheet 12 of 55

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RTCRST close to RAM door

+RTCBATT
C439 1U_0402_6.3V6K
R501 0_0603_5%
PCH_RTCRST#
R356 20K_0402_5%
PCH_SRTCRST#
R357 20K_0402_5%
R372 0_0603_5%
C440 1U_0402_6.3V6K

+RTCBATT
R358 1M_0402_5% SM_INTRUDER#
R355 330K_0402_5% PCH_INTVRMEN

INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS
R109 1K_0402_5% HDA_SPKR
HIGH= Enable (No Reboot)Disable TCO timer system reboot feature
★ LOW= Disable (Default internal PD)

+3V_PCH
R46 1K_0402_5%
R73 0_0402_5%
<37> ME_FLASH
HDA_SDOUT_PCH

HDA_SDO
ME debug mode,this signal has a weak internal PD
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH
R47 1K_0402_5% HDA_SYNC_PCH
This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
★1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

<36> HDA_BITCLK_AUDIO R75 33_0402_5% R30 HDA_BITCLK_PCH
<36> HDA_SYNC_AUDIO R74 33_0402_5% HDA_SYNC_PCH_R
<36> HDA_RST_AUDIO# R72 33_0402_5% HDA_RST_PCH#
<36> HDA_SDOUT_AUDIO HDA_SDOUT_PCH

+3V_PCH
R134 200_0402_5% PCH_JTAG_TDO
R143 200_0402_5% PCH_JTAG_TMS
R137 200_0402_5% PCH_JTAG_TDI
R141 100_0402_1%
R140 100_0402_1%
R142 100_0402_1%

PCH_RTCX1
R406 10M_0402_5%
PCH_RTCX2
Y2 32.768KHZ_12.5PF_9H032000019 SJ10000BM00
18P_0402_50V8J
C452
C451 18P_0402_50V8J

Prevent back drive issue.

+5VS
SB00000QO00 Q3 BSS138_NL_SOT23-3
HDA_SYNC_PCH_R R48 0_0402_5%
<36> HDA_SPKR
R29 1M_0402_5%
<36> HDA_SDIN0

U13A

PCH_RTCX1	A20	RTCX1	RTC	
PCH_RTCX2	C20	RTCX2		
PCH_RTCRST#	D20	RTCRST#		
PCH_SRTCRST#	G22	SRTCRST#		
SM_INTRUDER#	K22	INTRUDER#		
PCH_INTVRMEN	C17	INTVRMEN		
HDA_BITCLK_PCH	N34	HDA_BCLK	IHDA	
HDA_SYNC_PCH	L34	HDA_SYNC		
HDA_SPKR	T10	SPKR		
HDA_RST_PCH#	K34	HDA_RST#		
HDA_SDIN0	E34	HDA_SDIN0		
	G34	HDA_SDIN1		
	C34	HDA_SDIN2		
	A34	HDA_SDIN3		
HDA_SDOUT_PCH	A36	HDA_SDO		
PCH_GPIO33	C36	HDA_DOCK_EN# / GPIO33		
PCH_GPIO13	N32	HDA_DOCK_RST# / GPIO13		
PCH_JTAG_TCK	J3	JTAG_TCK	JTAG	
PCH_JTAG_TMS	H7	JTAG_TMS		
PCH_JTAG_TDI	K5	JTAG_TDI		
PCH_JTAG_TDO	H1	JTAG_TDO		
SPI_CLK_PCH_R	T3	SPI_CLK	SPI	
SPI_SB_CS0#	Y14	SPI_CS0#		
SPI_SB_CS1#	T1	SPI_CS1#		
SPI_SI	V4	SPI_MOSI		
SPI_SO_R	U3	SPI_MISO		

R162 1K_0402_1% PCH_GPIO33
+3V_PCH R341 10K_0402_5% PCH_GPIO13
R100 51_0402_5% PCH_JTAG_TCK

PANTHER_FCBGA989
HM77@

FWH0 / LAD0	C38	LPC_AD0	LPC_AD0	<31,37>
FWH1 / LAD1	A38	LPC_AD1	LPC_AD1	<31,37>
FWH2 / LAD2	B37	LPC_AD2	LPC_AD2	<31,37>
FWH3 / LAD3	C37	LPC_AD3	LPC_AD3	<31,37>
FWH4 / LFRAME#	D36	LPC_FRAME#	LPC_FRAME#	<31,37>
LDRQ0#	E36			
LDRQ1# / GPIO23	K36			
SERIRQ	V5	SERIRQ	SERIRQ	<37>

+3VS
SERIRQ R118 10K_0402_5%

SATA0RXN	AM3						
SATA0RXP	AM1						
SATA0TXN	AP7	SATA_PTX_DRX_C_N0	2	1 C1185 0.01U_0402_16V7K	SATA_PRX_DTX_C_N0	<31>	
SATA0TXP	AP5	SATA_PTX_DRX_C_P0	2	1 C1208 0.01U_0402_16V7K	SATA_PRX_DTX_C_P0	<31>	
					SATA_PTX_DRX_N0	<31>	
					SATA_PTX_DRX_P0	<31>	
SATA1RXN	AM10	SATA_DTX_C_R_PRX_N1	R148	HDD1@ 2 1 0_0402_5%	SATA_DTX_C_PRX_N1	<35>	
SATA1RXP	AM8	SATA_DTX_C_R_PRX_P1	R149	HDD1@ 2 1 0_0402_5%	SATA_DTX_C_PRX_P1	<35>	
SATA1TXN	AP11	SATA_PTX_DRX_N1	R150	HDD1@ 2 1 0_0402_5% SATA_PTX_R_DRX_N1_C 2 1 C1209 0.01U_0402_16V7K	SATA_PTX_R_DRX_N1	<35>	
SATA1TXP	AP10	SATA_PTX_DRX_P1	R151	HDD1@ 2 1 0_0402_5% SATA_PTX_R_DRX_P1_C 2 1 C1223 0.01U_0402_16V7K	SATA_PTX_R_DRX_P1	<35>	
SATA2RXN	AD7	SATA_DTX_C_R_PRX_N2	R154	HDD2@ 2 1 0_0402_5%	SATA_DTX_C_PRX_N1		
SATA2RXP	AD5	SATA_DTX_C_R_PRX_P2	R157	HDD2@ 2 1 0_0402_5%	SATA_DTX_C_PRX_P1		
SATA2TXN	AH5	SATA_PTX_DRX_N2	R160	HDD2@ 2 1 0_0402_5%	SATA_PTX_R_DRX_N1_C0		
SATA2TXP	AH4	SATA_PTX_DRX_P2	R161	HDD2@ 2 1 0_0402_5%	SATA_PTX_R_DRX_P1_C0		
SATA3RXN	AB8						
SATA3RXP	AB10						
SATA3TXN	AF3						
SATA3TXP	AF1						
SATA4RXN	Y7						
SATA4RXP	Y5						
SATA4TXN	AD3						
SATA4TXP	AD1						
SATA5RXN	Y3						
SATA5RXP	Y1						
SATA5TXN	AB3						
SATA5TXP	AB1						
SATAICOMPO	Y11						
SATAICOMPI	Y10	SATA_COMP	R121	37.4_0402_1%			
SATA3RCOMPO	AB12						
SATA3COMPI	AB13	SATA3_COMP	R126	49.9_0402_1%			
SATA3RBIAS	AH1	RBIAS_SATA3	R440	750_0402_1%			
SATALED#	P3	PCH_SATALED#					
SATA0GP / GPIO21	V14	PCH_GPIO21					
SATA1GP / GPIO19	P1	BBS_BIT0_R					

SSD
HDD0 w/ HM77
Disable w/ HM70
HDD1 w/ HM70
Disable w/ HM70
L=500mil S=15mil
+1.05VS_VTT
L=500mil S=15mil
+1.05VS_VTT
No use PH 10K +3VS

GPIO19 has internal Pull up
GPIO21 Debug Port DG 1.2 PH 4.7K +3VS
+3VS
BBS_BIT0_R R466 10K_0402_5%
PCH_SATALED# R429 10K_0402_5%
PCH_GPIO21 R136 10K_0402_5%

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

2MB SPI ROM FOR ME
& Non-share ROM.

+3VS
R266 2_SPI_WP#1 3.3K_0402_5%
R221 2SPI_HOLD#1 3.3K_0402_5%
R127 2_SPI_WP# 3.3K_0402_5%
R171 2SPI_HOLD# 3.3K_0402_5%

SPI_SB_CS1# R172 0_0402_5%
SPI_SO_R R188 33_0402_5%
U46 16M W25Q16BVSSIG SOIC 8P
CS# SO WP# GND VCC HOLD# SCLK SI
SPI_HOLD#1 SPI_CLK1 SPI_SI1
R199 0_0402_5% SPI_CLK_PCH_R
SPI_SI R196 33_0402_5%

Reserve for EMI
C459 10P_0402_50V8J
R434 33_0402_5% SPI_CLK_PCH_R

U6 Rersver 4M+2M Solution

SPI_SB_CS0#2 R173 0_0402_5%
SPI_SO_R R169 33_0402_5%
U44 32M W25Q32BVSSIG SOIC 8P
CS# SO WP# GND VCC HOLD# SCLK SI
SPI_HOLD# SPI_CLK_PCH SPI_SI_R
+3VS C191 0.1U_0402_16V4Z
R168 0_0402_5% SPI_CLK_PCH_R
SPI_SI R170 33_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: LA-8952P | Rev: 0.1
Date: Thursday, January 10, 2013 | Sheet 13 of 55

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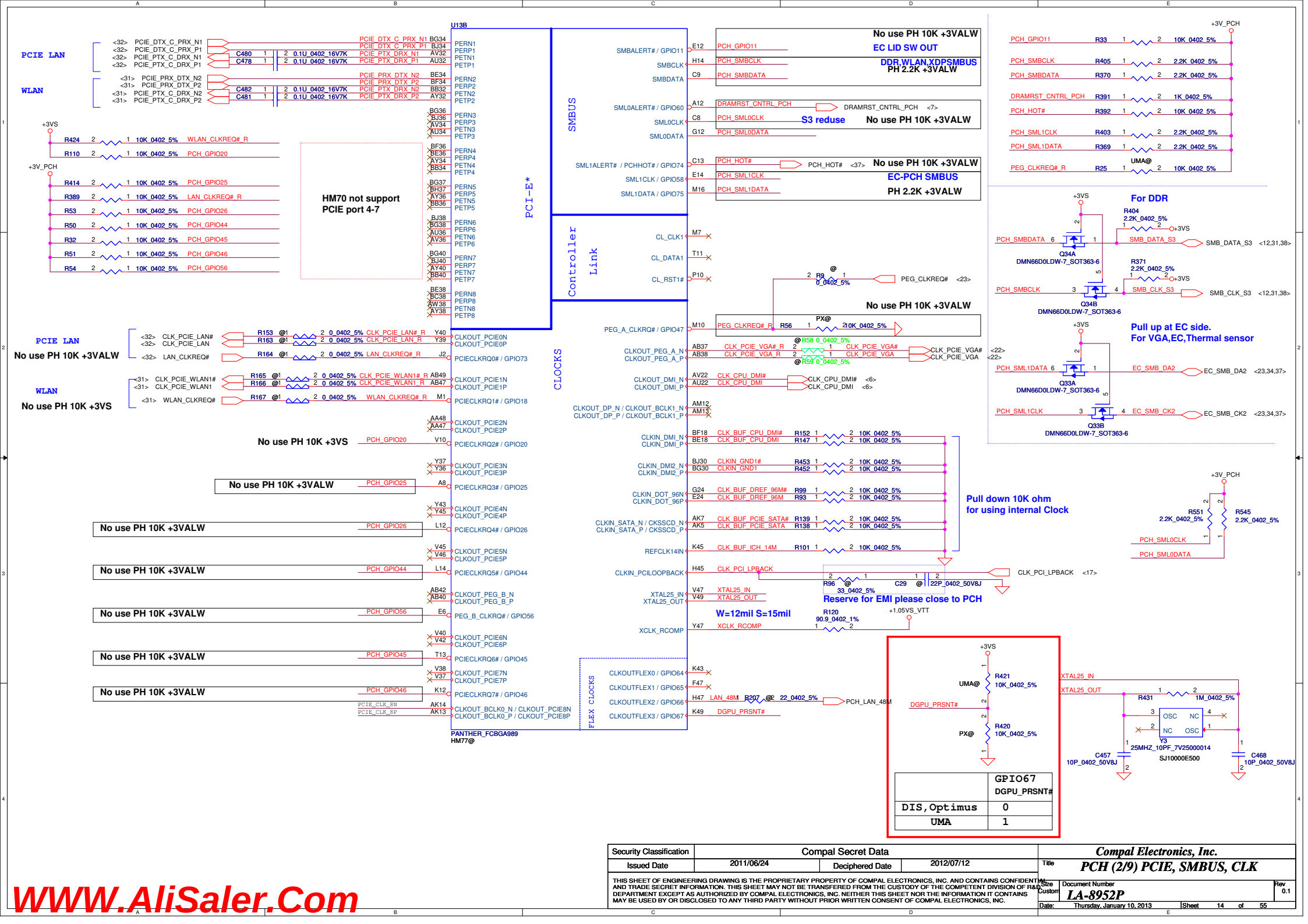

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Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title: PCH (2/9) PCIE, SMBUS, CLK

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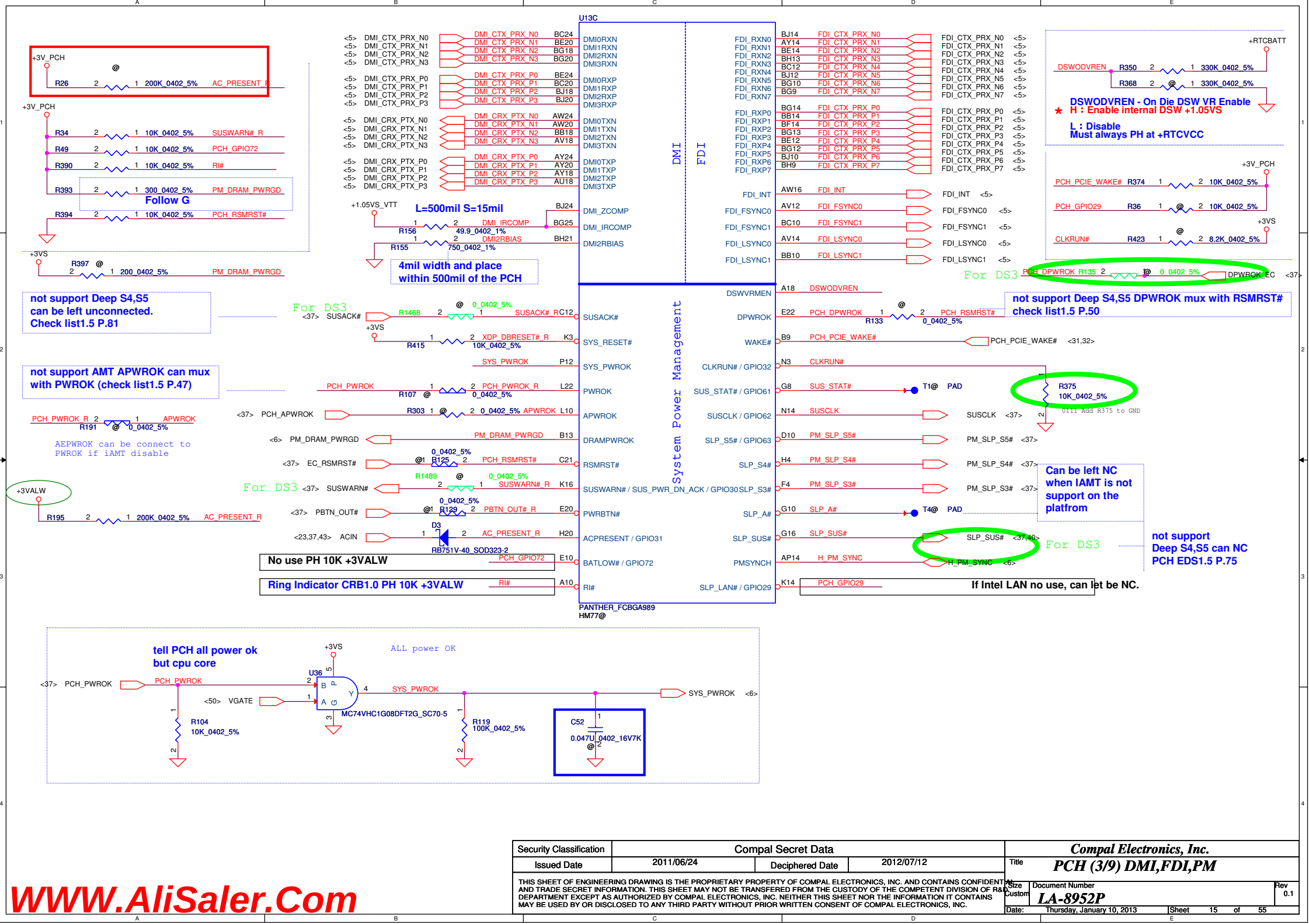
Size: Custom	Document Number: LA-8952P		Rev: 0.1
Date: Thursday, January 10, 2013	Sheet 14 of 55		



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Security Classification	Compal Secret Data		
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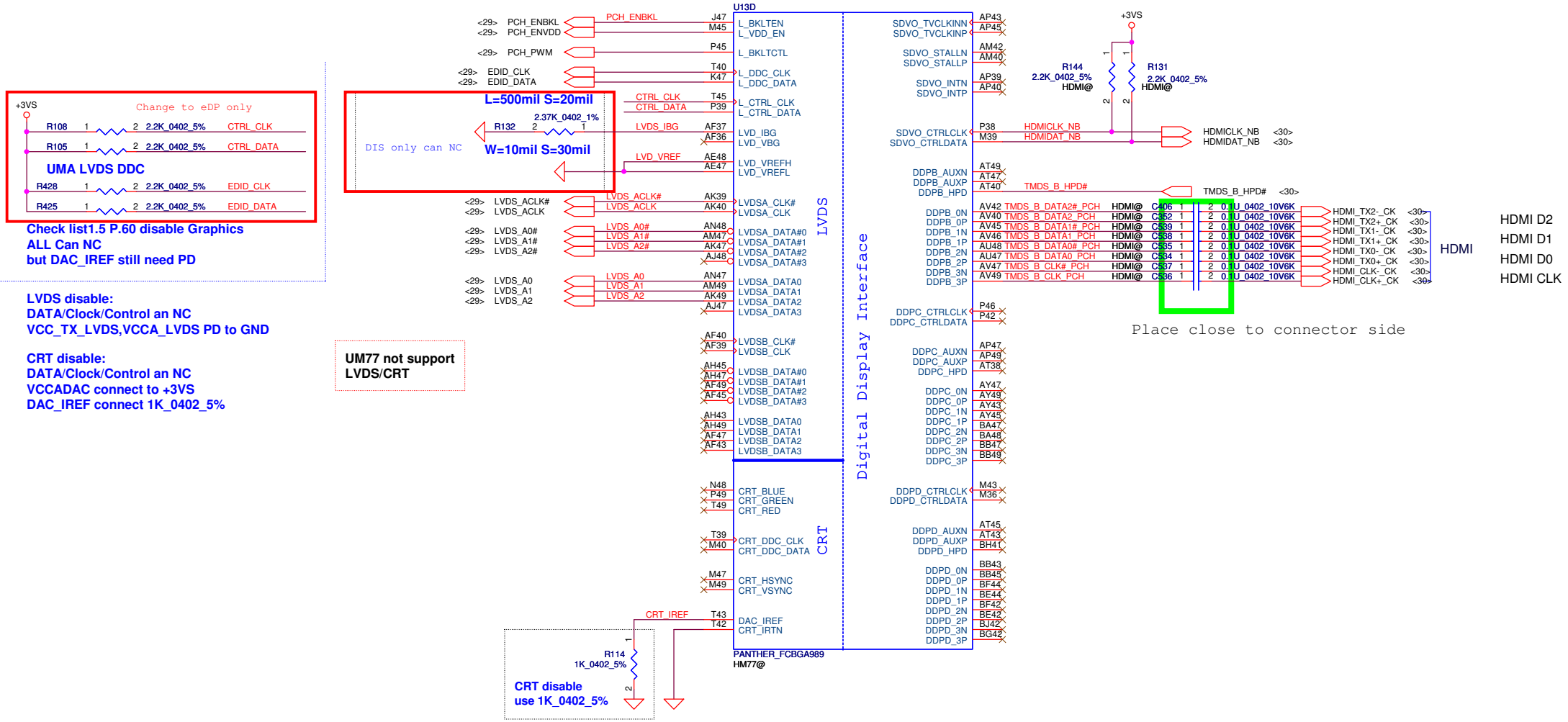
Compal Electronics, Inc.			
Title: PCH (3/9) DMI,FDI,PM			
Size: Custom	Document Number: LA-8952P		Rev: 0.1
Date: Thursday, January 10, 2013	Sheet 15 of 55		



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.			
Title	PCH (4/9) LVDS,CRT,DP,HDMI		
Size	Document Number		Rev
Custom	LA-8952P		0.1
Date:	Thursday, January 10, 2013	Sheet	16 of 55

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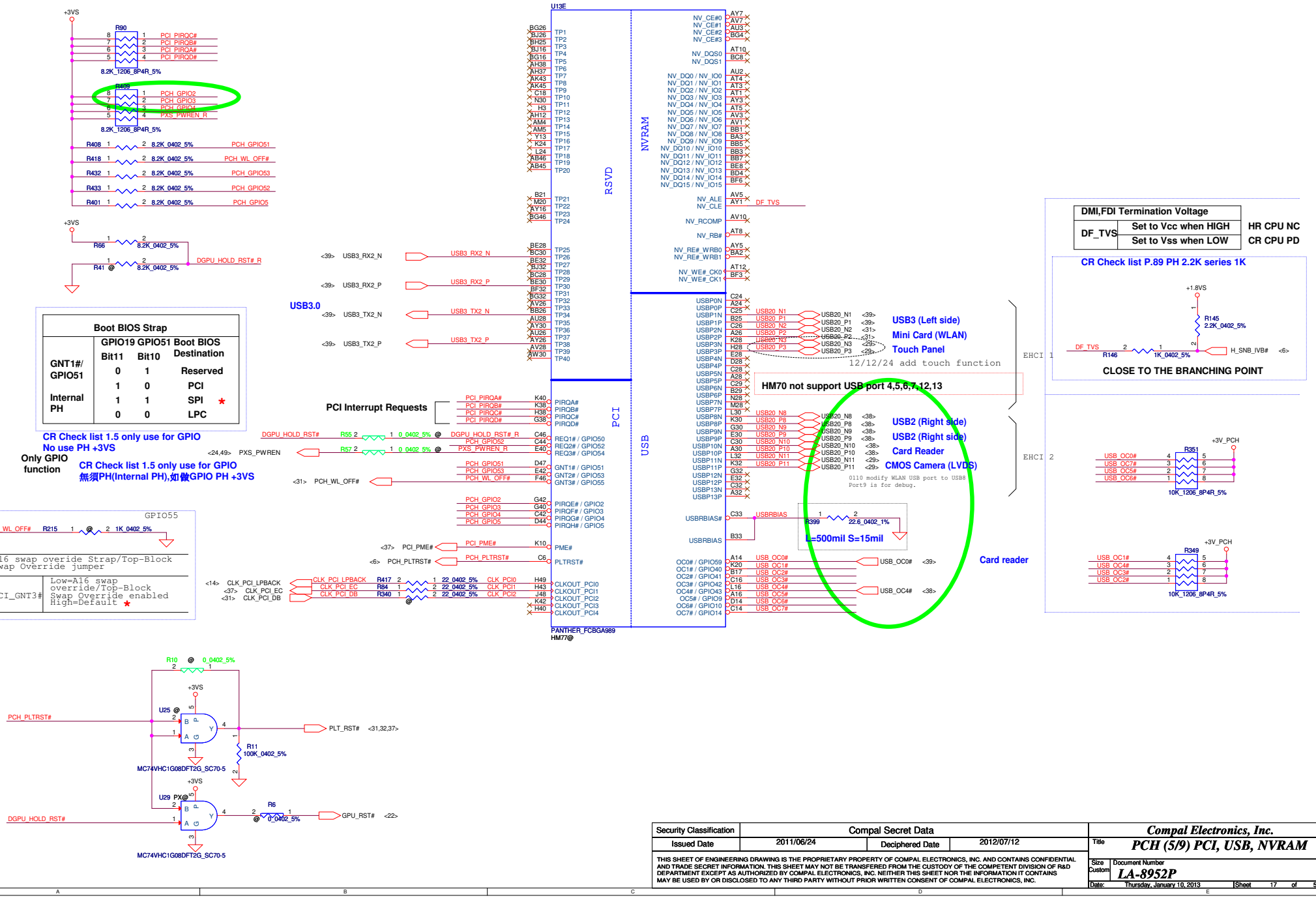

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: **PCH (5/9) PCI, USB, NVRAM**

Size	Document Number	Rev
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Date: Thursday, January 10, 2013 Sheet 17 of 55

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HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+3V_PCH
R411 10K_0402_5%
PCH_GPIO28
R413 1K_0402_5% @
Debug Port DG 1.2 PH 4.7K +3VALW_PCH

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal

+3VALW
For DS3
R208 @ 10K_0402_5%
R83 @ 10K_0402_5%
PCH_GPIO27

+3V_PCH
R261 @ 1K_0402_5% EC_SMI#

SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled
after PLTRST# de-asserts)
NOTE: This signal should NOT be
pulled high when strap is sampled

+3VS
R112 10K_0402_5% PCH_GPIO0
R402 10K_0402_5% PCH_GPIO1
R70 10K_0402_5% PCH_GPIO6
R115 10K_0402_5% MSATA_DET#
R71 10K_0402_5% VGA_PWRGD_R
R419 10K_0402_5% PCH_GPIO39
R97 10K_0402_5% BT_DISABLE
R416 10K_0402_5% PCH_BT_ON#
R128 10K_0402_5% PCH_GPIO48
R111 10K_0402_5% PCH_GPIO49

+3V_PCH
R376 10K_0402_5% PCH_GPIO12
R412 1K_0402_5% PCH_GPIO15
R52 10K_0402_5% PCH_GPIO57
R92 10K_0402_5% PCH_GPIO24
For DDR3L control
<37,46> DDR3L_EN# R63 @ 0_0402_5% PCH_GPIO24

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration
register bits are not cleared by
CF9h reset event.
CRB1.0 PH10K to +3VALW

PCH_GPIO69	Function
0	non DS3
1	DS3

+3VS
R67 @ 10K_0402_5% PCH_GPIO69
R42 10K_0402_5%
R69 10K_0402_5%@ PCH_GPIO70
R44 200K_0402_5%

PCH_GPIO70	Function
0	13/14"
1	NA
PCH_GPIO71	
0	USB3.0
1	USB2.0

+3VS
R68 10K_0402_5% USB2@ PCH_GPIO71
R43 200K_0402_5% USB3@

Fan Tachometer Inputs
TACH1~7 only on server
can insted to GPIO

No use PH 10K +3VS — PCH_GPIO0
No use PH 10K +3VS — PCH_GPIO1
No use PH 10K +3VS — PCH_GPIO6
No use PH 10K +3VS — <37> EC_SCI# — EC_SCI#
No use PH 10K +3VALW — <37> EC_SMI# — EC_SMI#
No use PH +3VALW — PCH_GPIO12
No use PH +3VALW — <37> EC_LID_OUT# — EC_LID_OUT# — R69 @ 0_0402_5% — PCH_GPIO15
No use PH +3VS — mSATA_DET#
No use PH +3VS — <22,49> VGA_PWRGD — R45 @ 0_0402_5% — VGA_PWRGD_R
No use PH 10K +3VS — Blue Booth — <31> BT_DISABLE — BT_DISABLE
No use PH 10K +3VALW — DDR3 — PCH_GPIO24
No use PD 10K to GND — <22> EC_WAKE# — EC_WAKE# — R61 @ 0_0402_5% — PCH_GPIO27
No use PH 10K +3VALW — PCH_GPIO28
No use PH 10K +3VS — BT ON/OFF — <31> PCH_BT_ON# — PCH_BT_ON#
No use can NC — R243 10K_0402_5% — PCH_GPIO35
Can't PH — <31> INTEL_BT_OFF# — INTEL_BT_OFF#
Can't PH — PCH_GPIO37
No use PH 10K +3VS — Optimus(L)/ non optimus(H) — OPTIMUS_EN#
No use PH 10K +3VS — PCH_GPIO39
No use PH 10K +3VS — PCH_GPIO48
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS — PCH_GPIO49
No use PH +3VALW — PCH_GPIO57

+3VS
UMA@ R427 10K_0402_5% OPTIMUS_EN#
PX@ R426 10K_0402_5%

*	GPIO38 OPTIMUS_EN#
Muxless	0
nonMuxless	1

+3VS
R244 10K_0402_5% @ PCH_GPIO37 — R881 10K_0402_5%
R245 10K_0402_5% @ INTEL_BT_OFF# — R552 10K_0402_5%

U13F

GPIO:
T7 GPIO0 / BMBUSY#
A42 GPIO1 / TACH1
H36 GPIO6 / TACH2
E38 GPIO7 / TACH3
C10 GPIO8
C4 GPIO12 / LAN_PHY_PWR_CTRL
G2 GPIO15
U2 GPIO16 / SATA4GP
D40 GPIO17 / TACH0
T5 GPIO22 / SCLOCK
E8 GPIO24 / MEM_LED
E16 GPIO27
P8 GPIO28
K1 GPIO34 / STP_PCI#
K4 GPIO35
V8 GPIO36 / SATA2GP
M5 GPIO37 / SATA3GP
N2 GPIO38 / SLOAD
M3 GPIO39 / SDATAOUT0
V13 GPIO48 / SDATAOUT1
V3 GPIO49 / SATA5GP
D6 GPIO57

CPU/MISC:
C40 TACH4 / GPIO68 — PCH_GPIO68
B41 TACH5 / GPIO69 — PCH_GPIO69
C41 TACH6 / GPIO70 — PCH_GPIO70
A40 TACH7 / GPIO71 — PCH_GPIO71
P4 A20GATE — GATEA20 <37>
AU16 PECI — PCH_PECI_R — 0_0402_5% R158 — H_PECI <37,6>
P5 RCIN# — EC_KBRST# — KBRST# <37>
AY11 PROCPWRGD — H_CPUPWRGD <6>
AY10 THRMTRIP# — PCH_THRMTRIP#_R R159 390_0402_5% — H_THERMTRIP# <6>
T14 INIT3_3V#

+3VS
R106 10K_0402_5%

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut down

INIT3_3V Checklist1.5 P.69
This signal has weak internal
PU, can't pull low,leave NC

AH8 NC_1
AK11 NC_2
AH10 NC_3
AK10 NC_4
P37 NC_5

TS_VSS1~4
PD to GND

EC_KBRST# R103 10K_0402_5%
PCH_GPIO68 R400 10K_0402_5%

0419 ESD request to reserve
PCH_THRMTRIP#_R
C1324 1000P_0402_50V7K @

NCTF:
A4 VSS_NCTF_1
A44 VSS_NCTF_2
A45 VSS_NCTF_3
A46 VSS_NCTF_4
A5 VSS_NCTF_5
A6 VSS_NCTF_6
B3 VSS_NCTF_7
B47 VSS_NCTF_8
BD1 VSS_NCTF_9
BD49 VSS_NCTF_10
BE1 VSS_NCTF_11
BE49 VSS_NCTF_12
BF1 VSS_NCTF_13
BF49 VSS_NCTF_14
BG2 VSS_NCTF_15
BG48 VSS_NCTF_16
BH3 VSS_NCTF_17
BH47 VSS_NCTF_18
BJ4 VSS_NCTF_19
BJ44 VSS_NCTF_20
BJ45 VSS_NCTF_21
BJ46 VSS_NCTF_22
BJ5 VSS_NCTF_23
BJ6 VSS_NCTF_24
C2 VSS_NCTF_25
C48 VSS_NCTF_26
D1 VSS_NCTF_27
D49 VSS_NCTF_28
E1 VSS_NCTF_29
E49 VSS_NCTF_30
F1 VSS_NCTF_31
F49 VSS_NCTF_32

9/15 Layout
request remove
Test point
They will route
by itself

9/15 Layout
request remove
Test point
They will route
by itself

PANTHER_FCBGA989
HM77@

GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.
Title: PCH (6/9) GPIO, CPU, MISC
Size: Custom
Document Number: LA-8952P
Rev: 0.1
Date: Thursday, January 10, 2013
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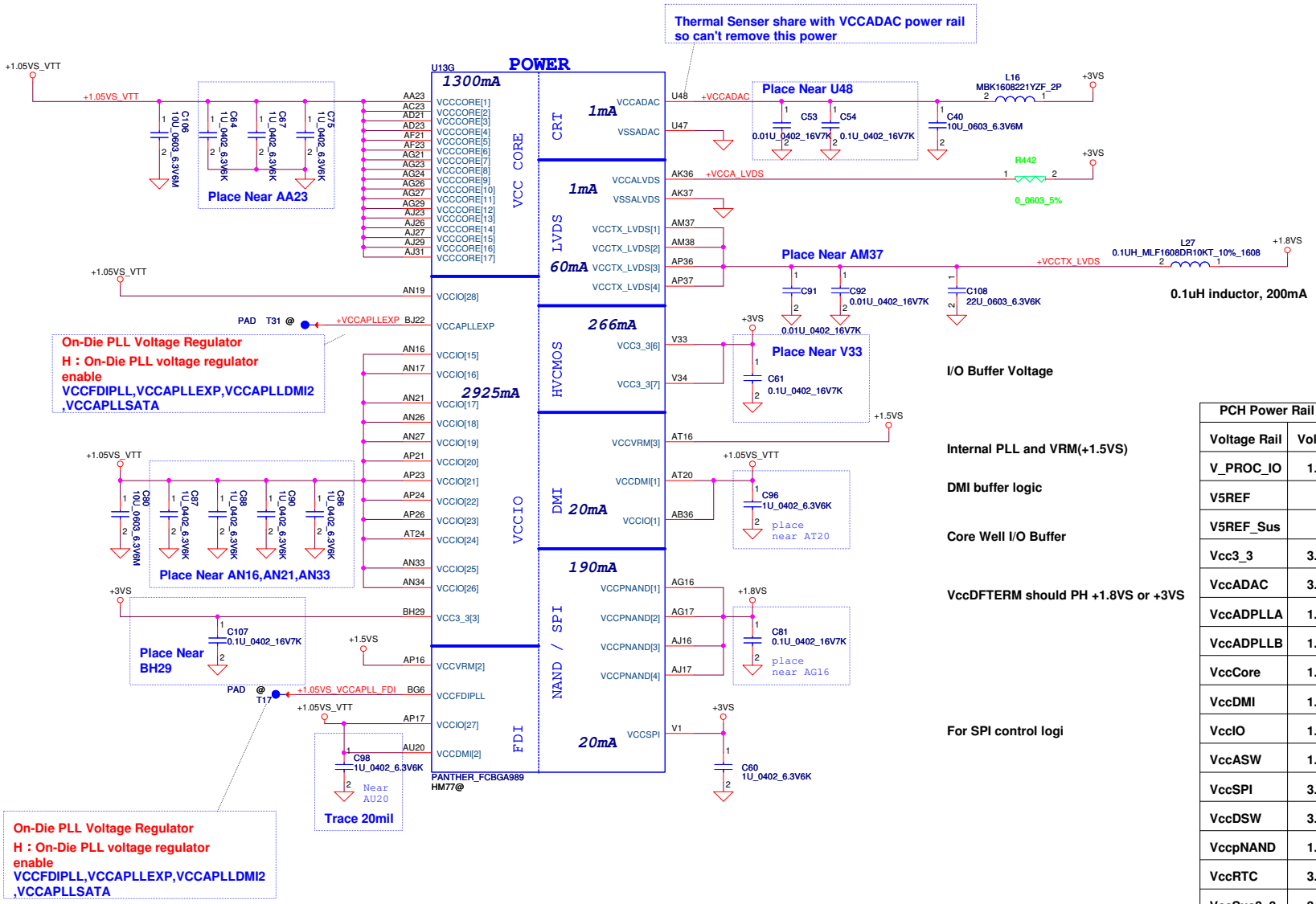

PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-8952P | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 19 of 55

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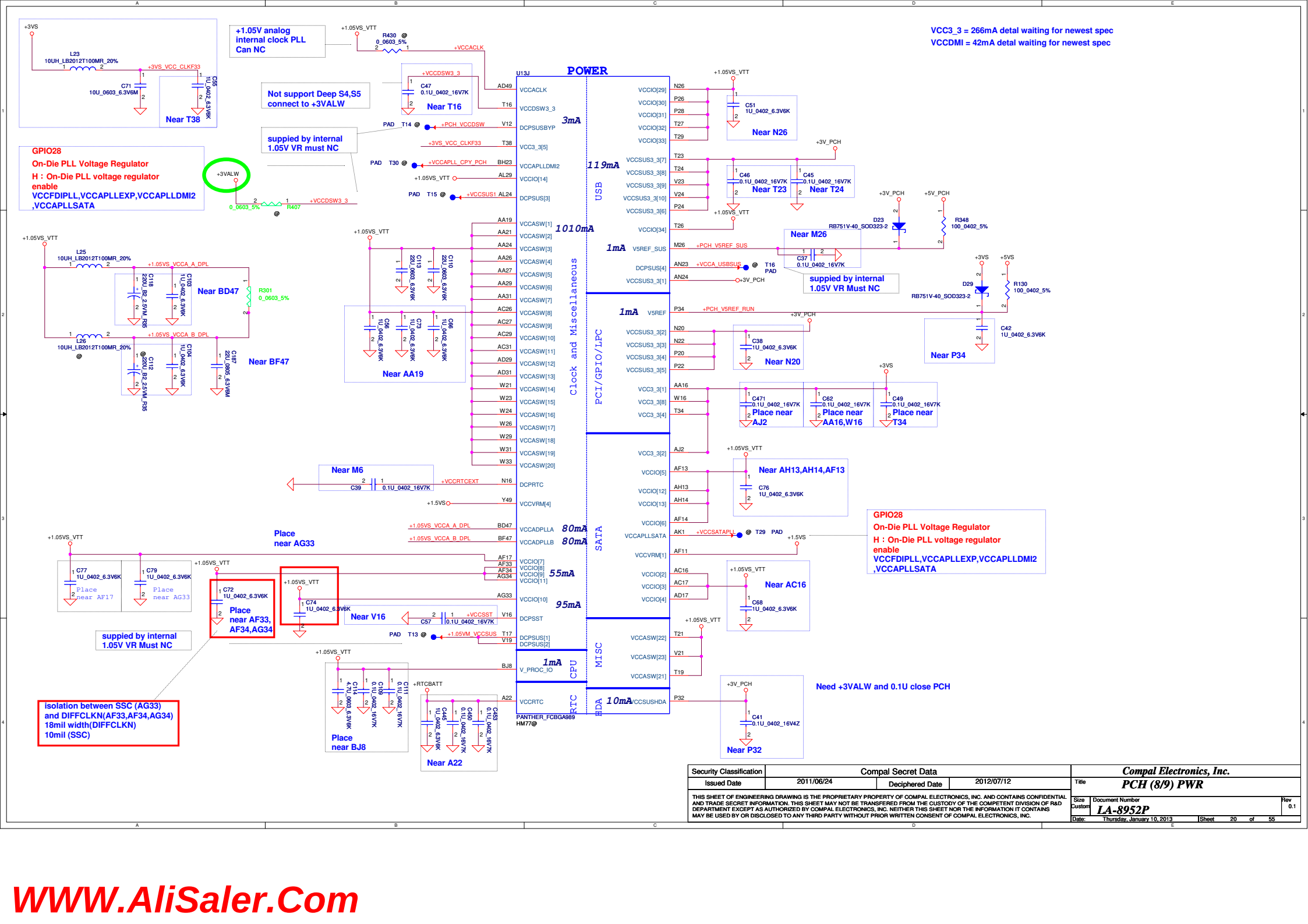

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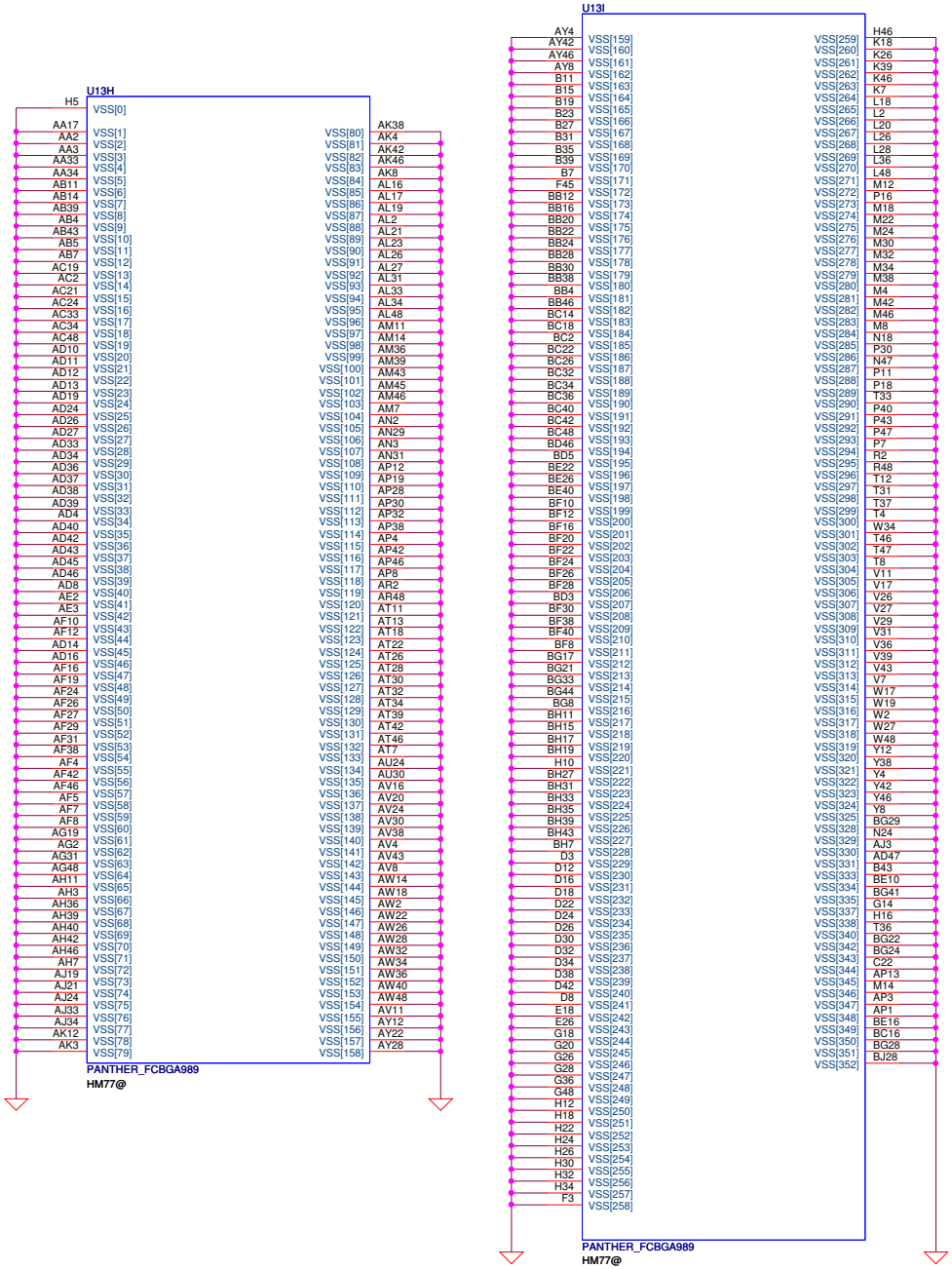

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: LA-8952P | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 21 of 55

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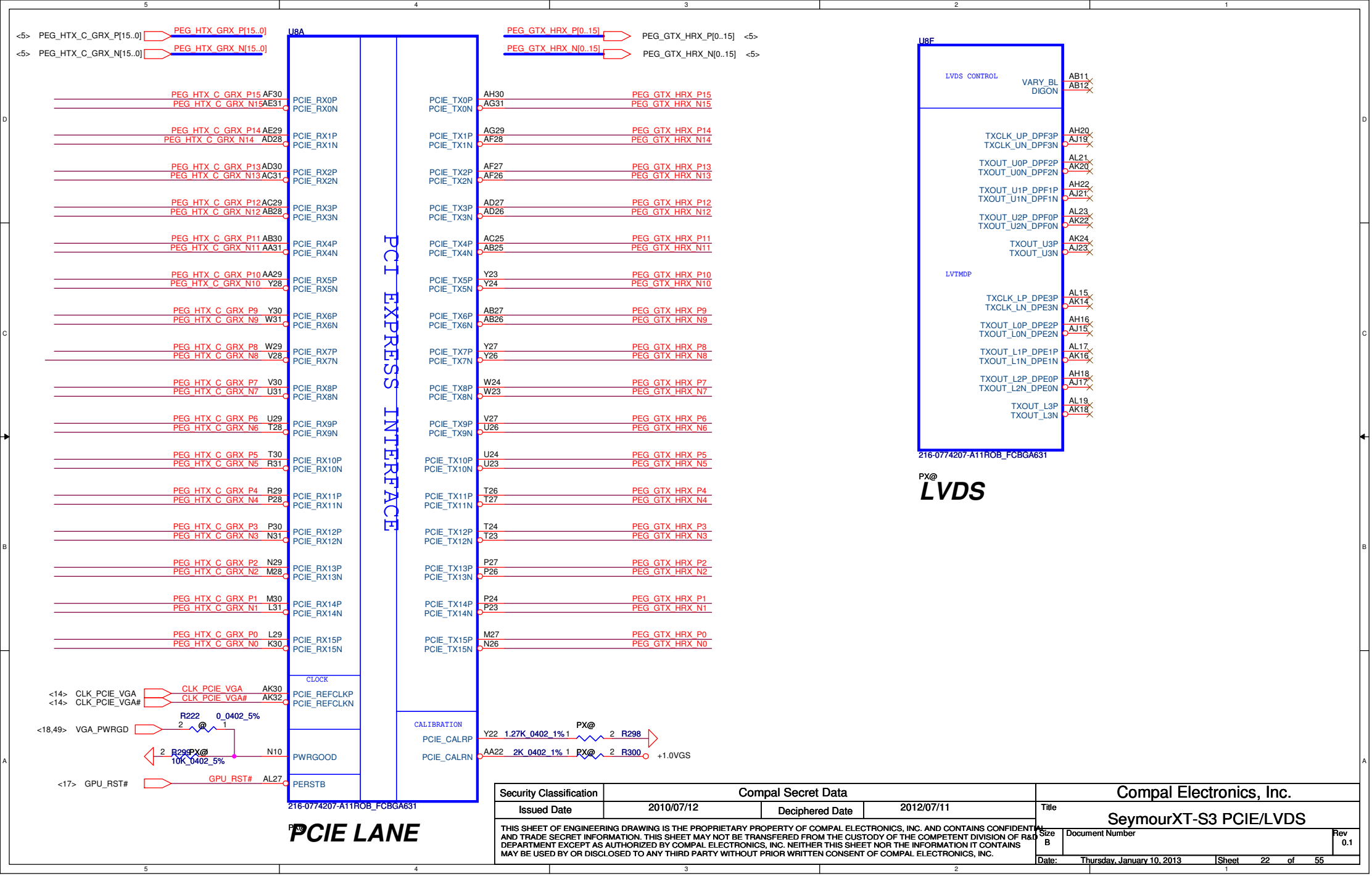

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: SeymourXT-S3 PCIE/LVDS

Size	Document Number	Rev
B		0.1

Date: Thursday, January 10, 2013 Sheet 22 of 55

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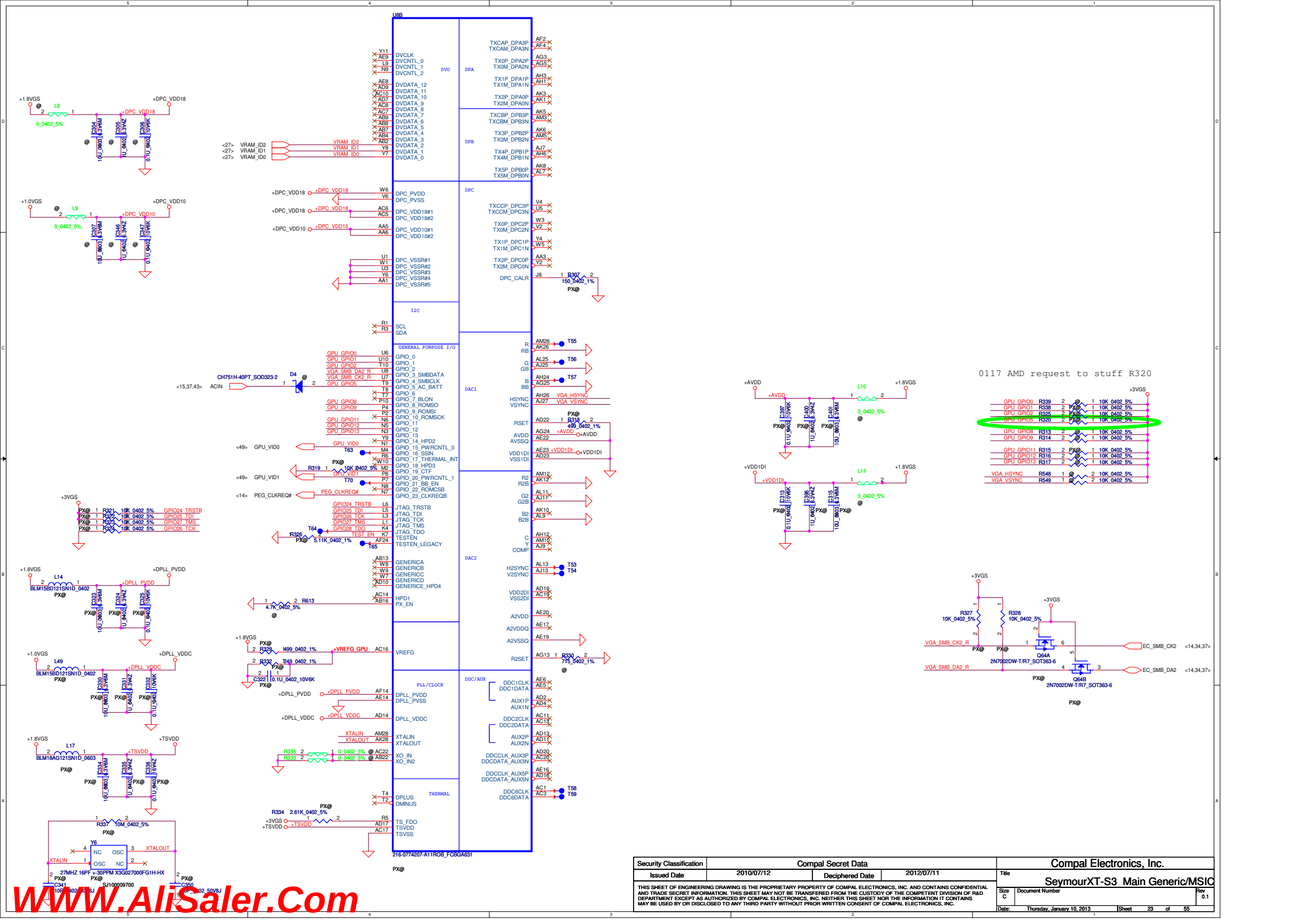

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Compal Electronics, Inc.

Title: SeymourXT-S3 Main Generic/MSIC

Size	Document Number	Rev
C		0.1

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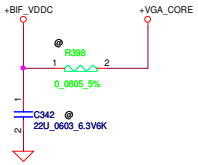
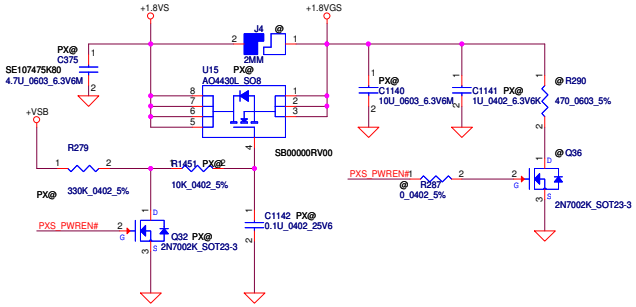
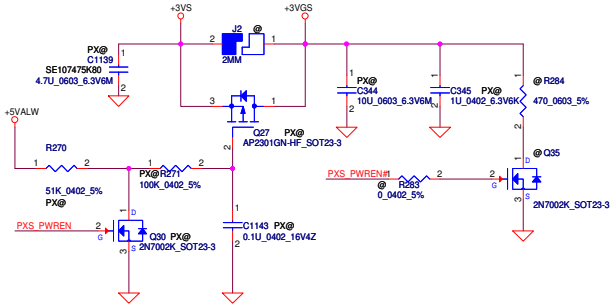
55mA@1.0V, in BACO mode

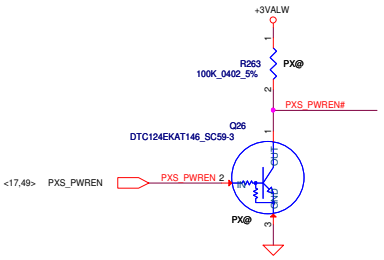


+1.8VS TO +1.8VGS

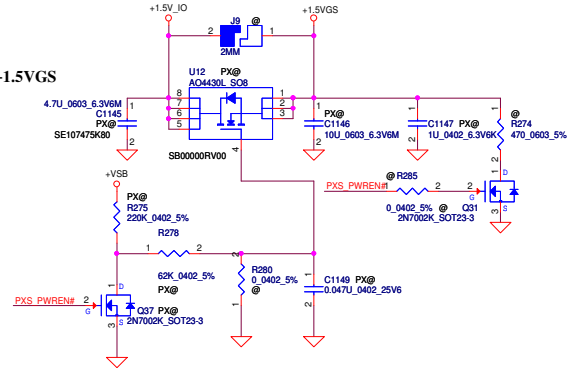


+3VS TO +3VGS





+1.5V TO +1.5VGS



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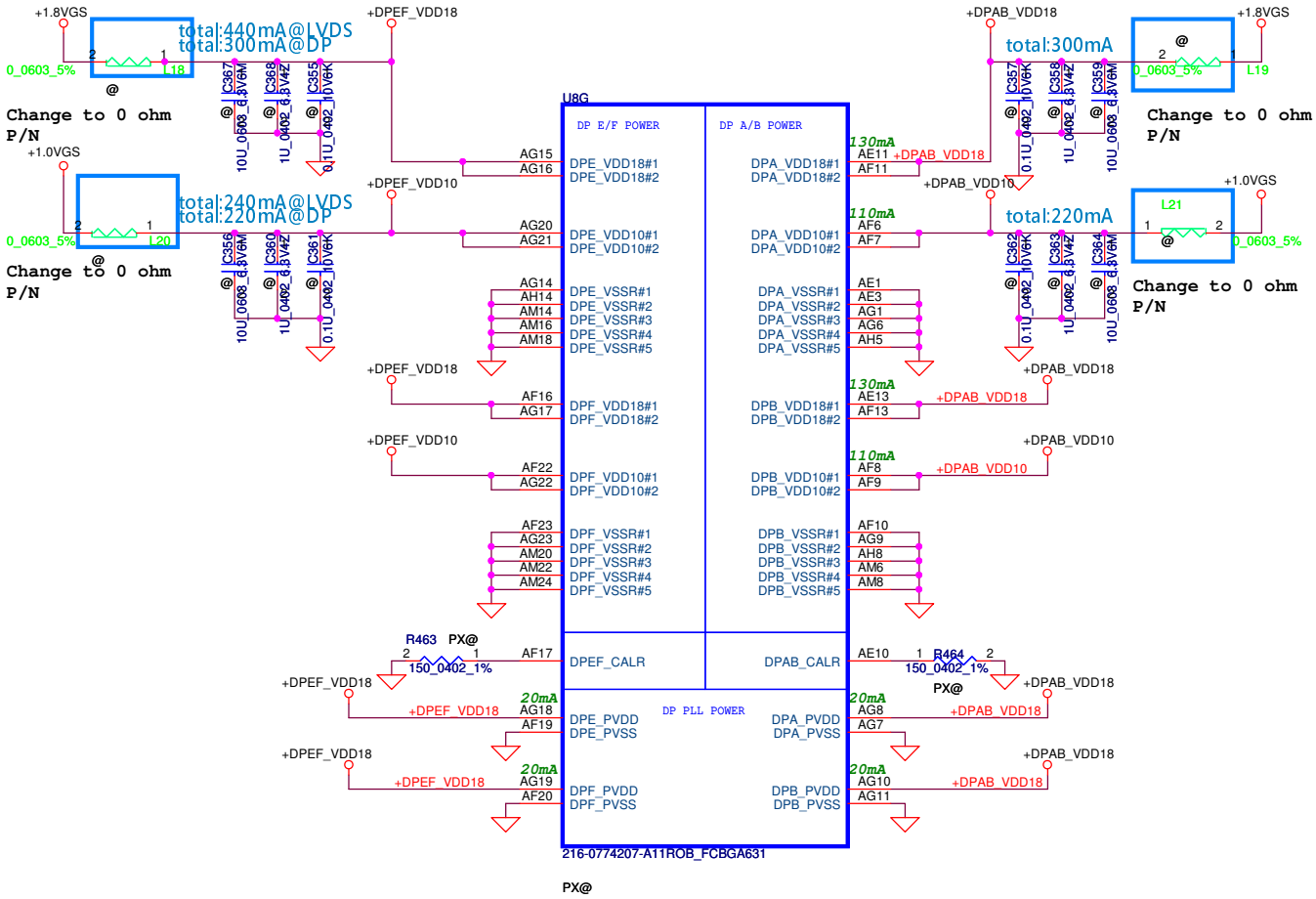
Compal Electronics, Inc.			
Title	SeymourXT_S3_BACO POWER		
Size C	Document Number LA-8952P		Rev 0.1
Date: Thursday, January 10, 2013		Sheet 24 of 55	



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: SeymourXT-S3 DP PWR

Size: B | Document Number | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 25 of 55

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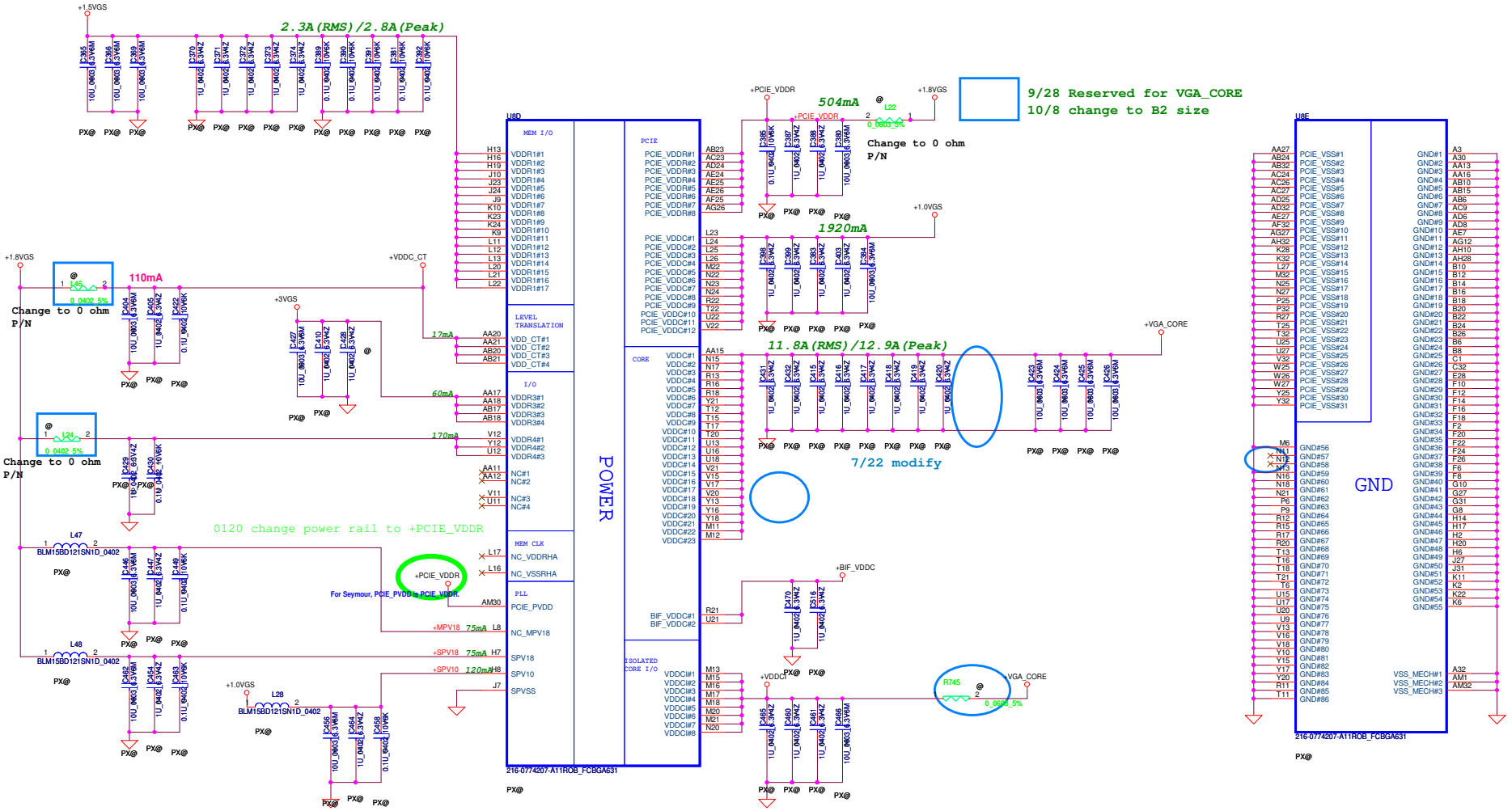

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: SeymourXT-S3 PWR/GND

Size	Document Number	Rev
C		0.1

Date: Thursday, January 10, 2013 Sheet 26 of 55

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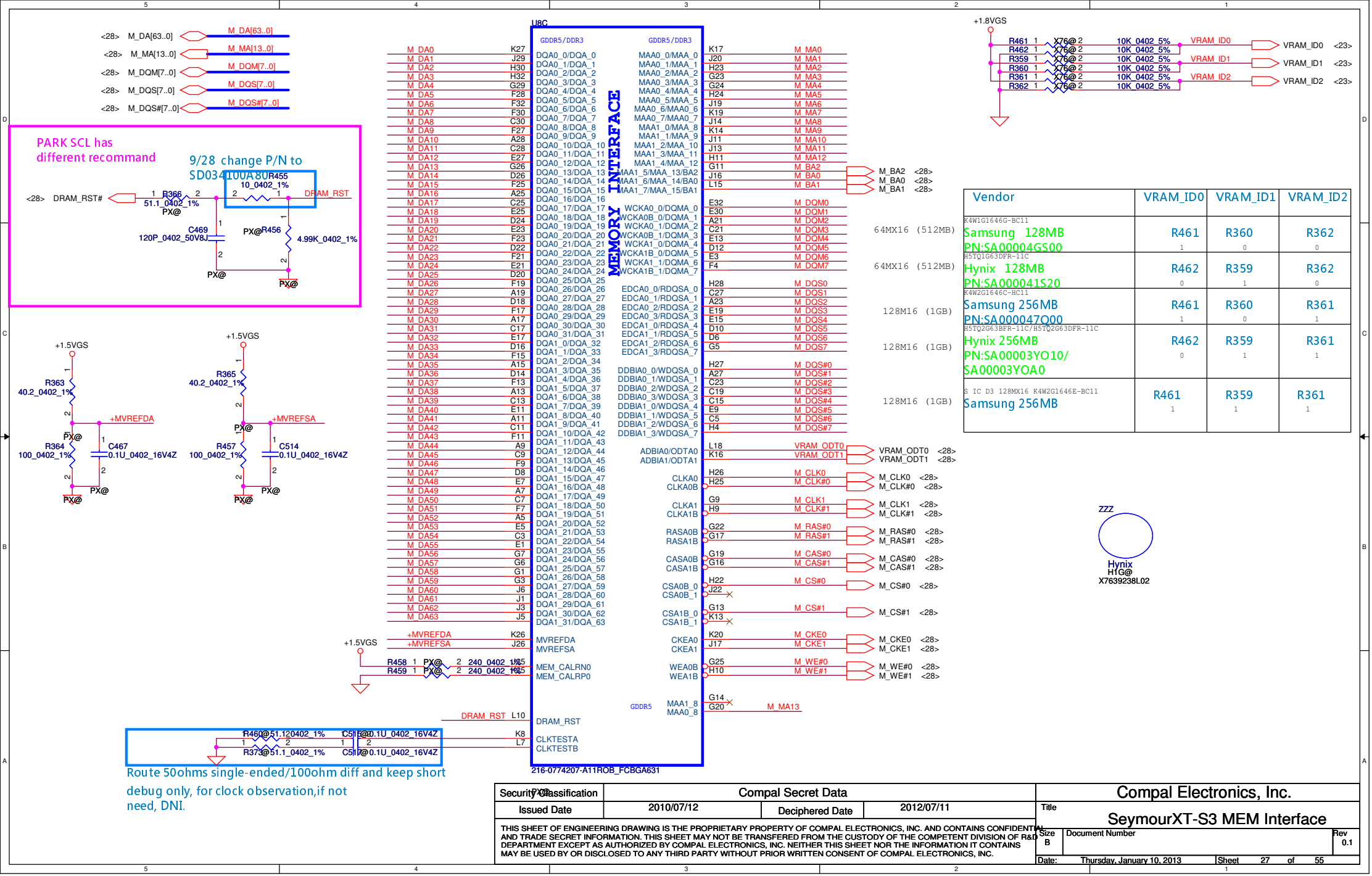

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Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: SeymourXT-S3 MEM Interface

Size	Document Number	Rev
B		0.1

Date: Thursday, January 10, 2013 Sheet 27 of 55

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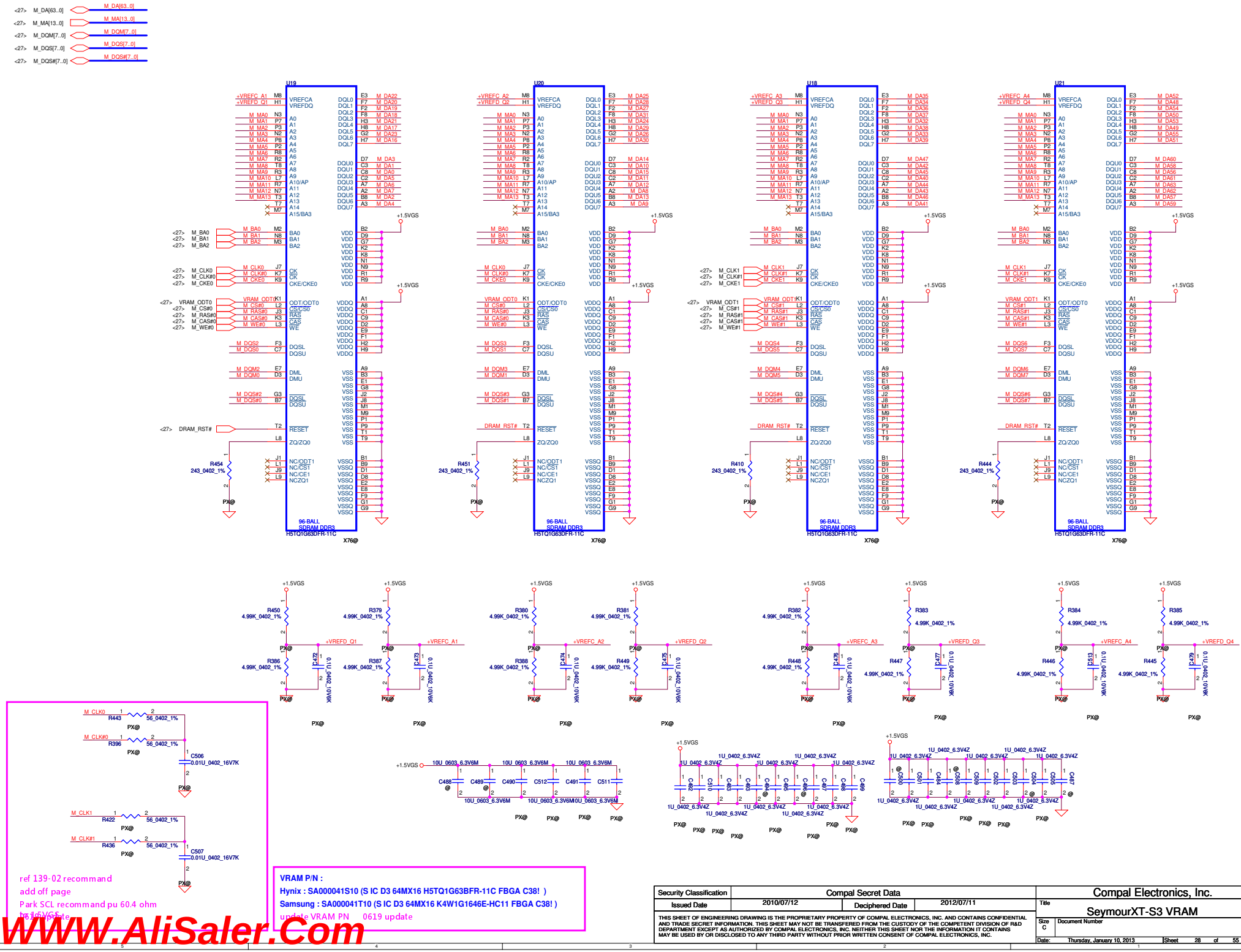

ref 139-02 recommand
add off page
Park SCL recommand pu 60.4 ohm
by 1.5VGS

VRAM P/N :
Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38!)
update VRAM PN 0619 update

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Issued Date	2010/07/12	Deciphered Date	2012/07/11

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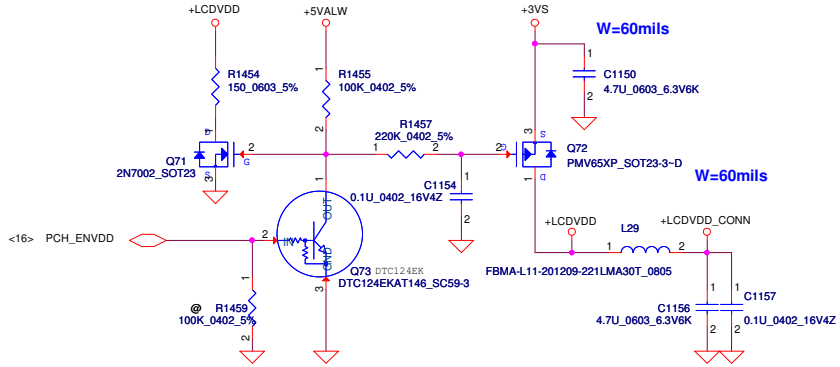
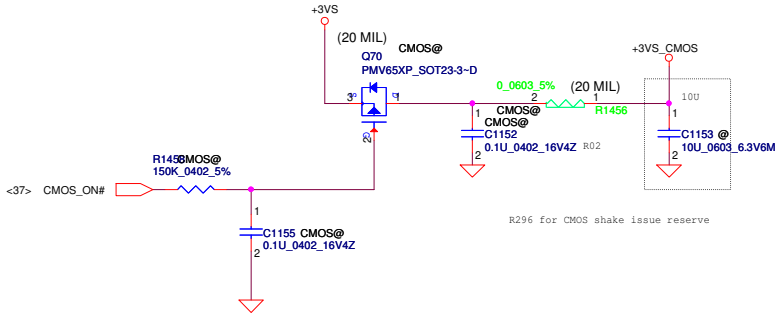
Compal Electronics, Inc.			
Title	SeymourXT-S3 VRAM		
Size C	Document Number		Rev 0.1
Date: Thursday, January 10, 2013	Sheet 28 of 55		

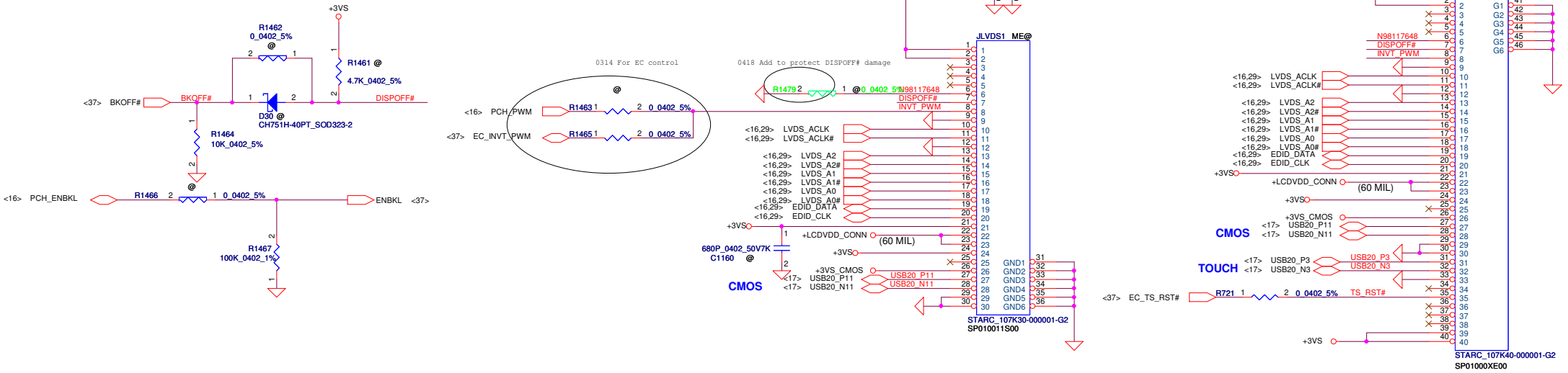
LCD POWER CIRCUIT



CMOS Camera



VGA LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.			
Title: LVDS/CAMERA			
Size: Custom	Document Number: LA-8952P		Rev: 0.1
Date: Thursday, January 10, 2013	Sheet 29 of 55		

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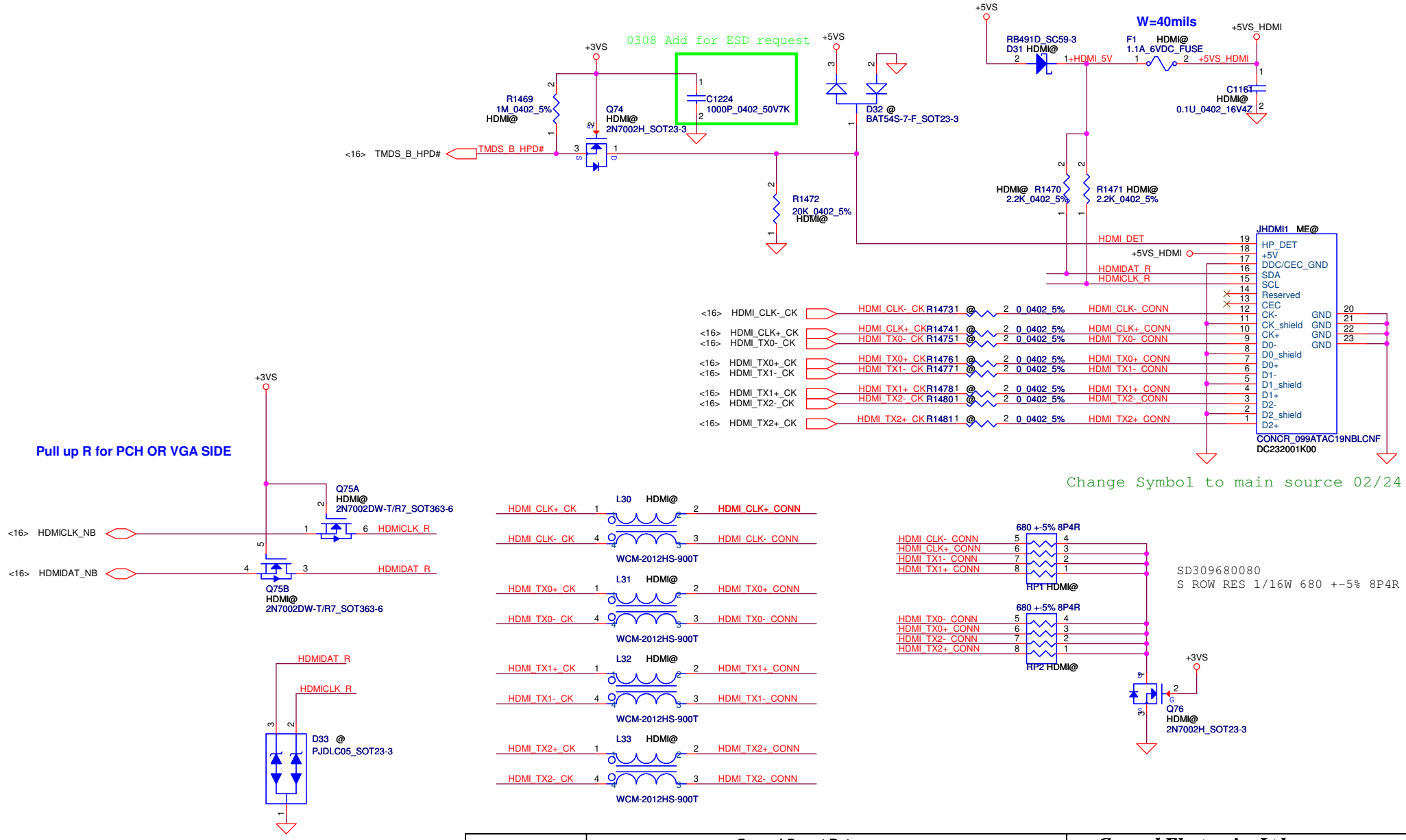

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
B	LA-8952P	0.1

Date: Thursday, January 10, 2013 Sheet 30 of 55

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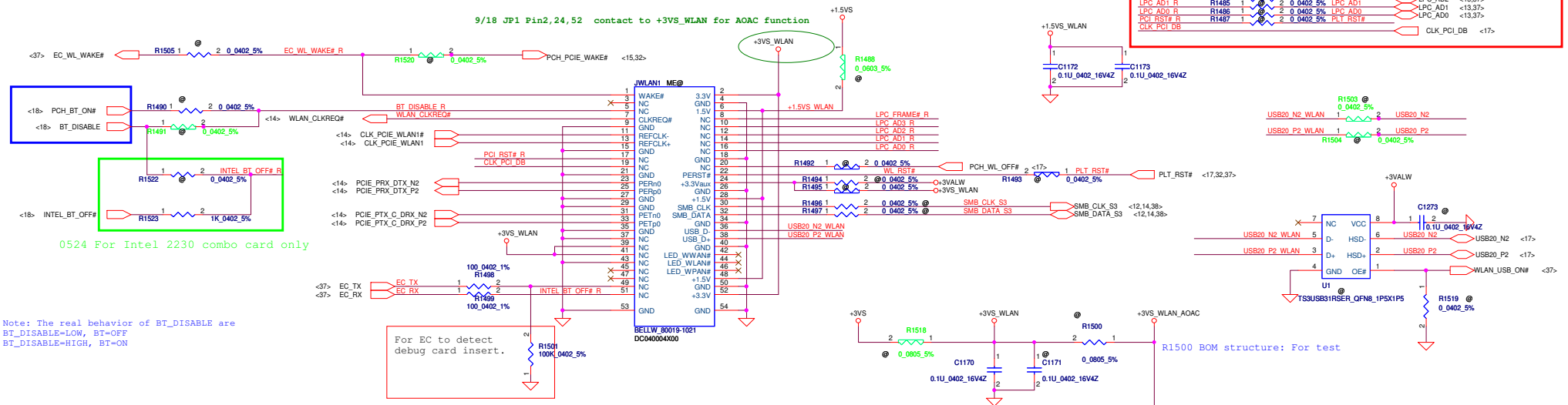
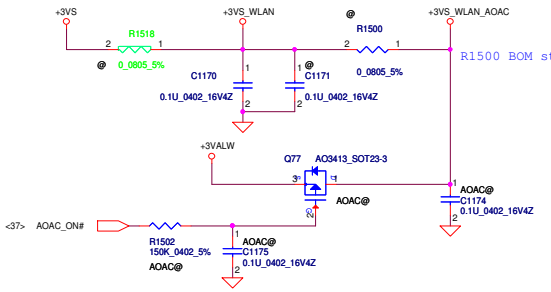
Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

Mini-Express Card(WLAN/WiMAX)

9/18 JP1 Pin2,24,52 contact to +3VS_WLAN for AOAC function



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

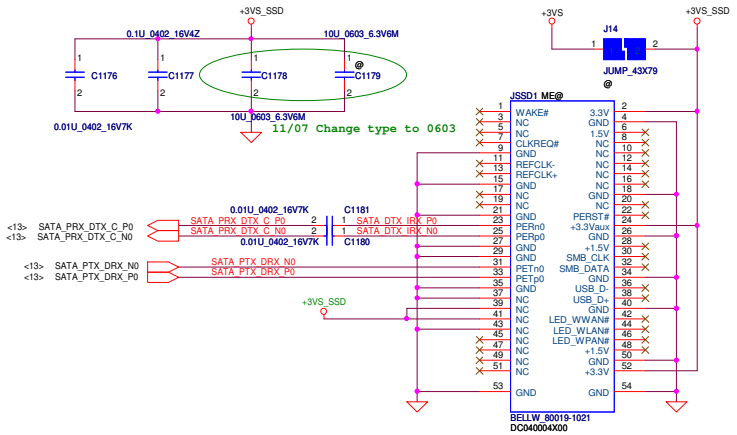


R1500 BOM structure: For test

9/18 Increase for Intel AOAC function

Mini-Express Card(SSD)

SSD Active:4.5W(1.5A)



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Security Classification	Compal Secret Data		
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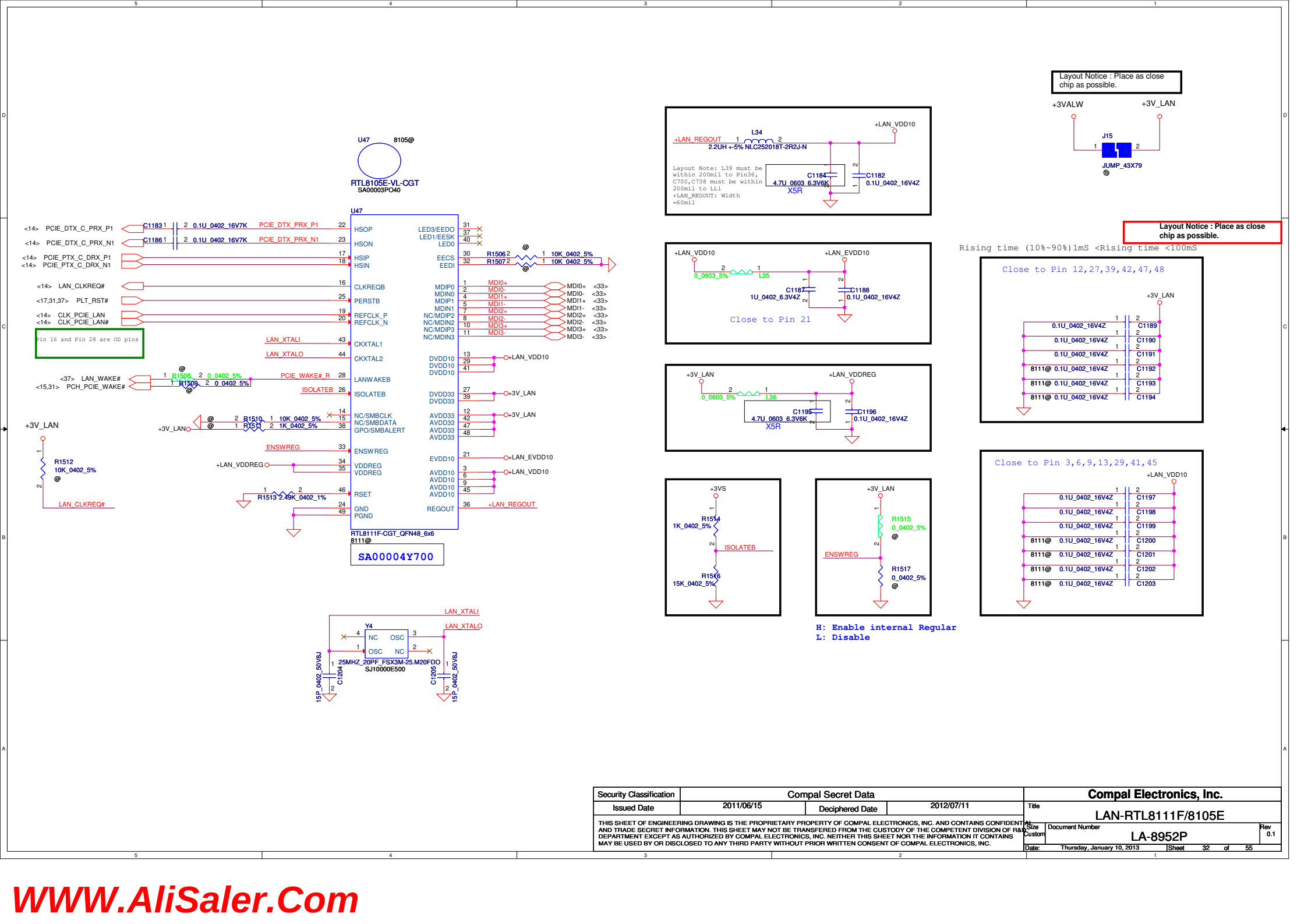
Compal Electronics, Inc.			
Title: Mini-Card			
Size	Document Number: LA-8952P		Rev: 0.1
Date: Thursday, January 10, 2013		Sheet 31 of 55	



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: LAN-RTL8111F/8105E

Size: Custom | Document Number: LA-8952P | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 32 of 55

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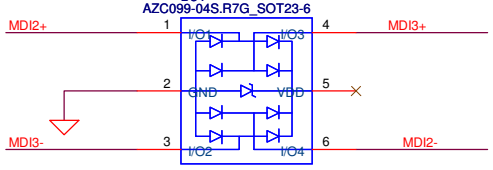
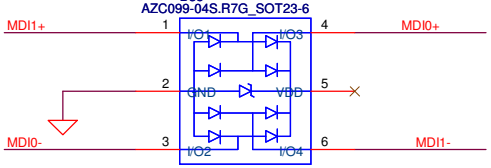
Reserve gas tube for EMI go rural solution

@
D34
AZC099-04S.R7G_SOT23-6



Place Close to T71

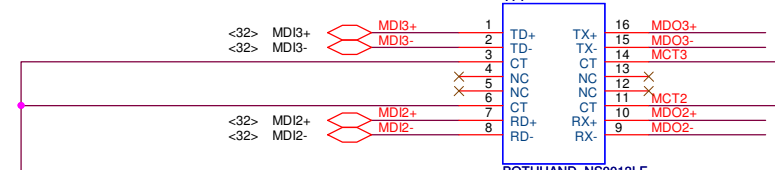
@
D35
AZC099-04S.R7G_SOT23-6



Place Close to T72

D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00

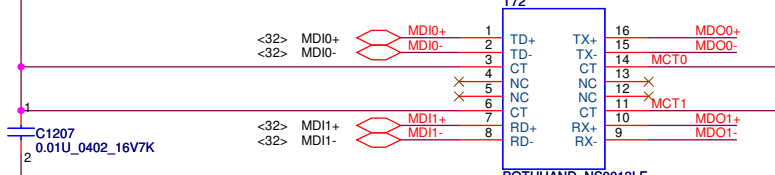
SP050007J00
T71



BOTHHAND_NS0013LF
8111@

R02

T72



BOTHHAND_NS0013LF
SP050007J00

C1207
0.01U_0402_16V7K

Place Close to T1,T2

R1521
75_0805_5%

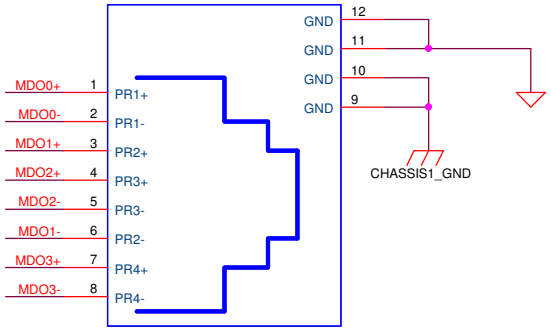
C1206
10P_0603_50V8-J

CHASSIS1_GND

DL2
BS4200N-C-LV_SMB-F2
GAS@
SCV00001D00

0320 EMI request to stuff

JRJ1 ME@



SANTA_130460-3
DC231112261

Reserve for EMI go rural solution

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: LAN_Transformer

Size: B | Document Number: LA-8952P | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 33 of 55

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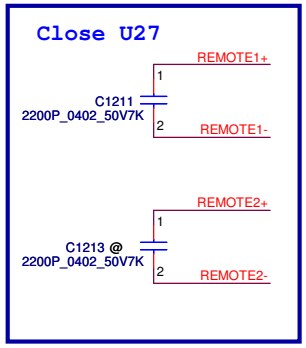
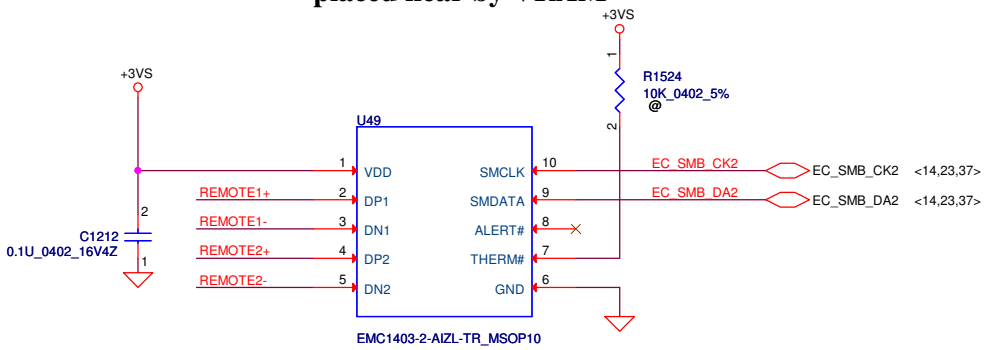
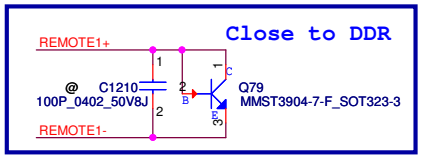
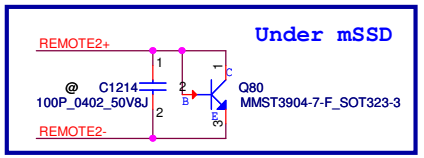
SMSC thermal sensor placed near by VRAM





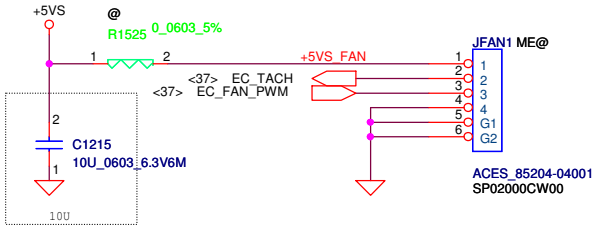
Address 1001_101xb





REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



R

H25 HOLEA — H_2P5X3P1N
H17 HOLEA — H_2P5X3P1N

E

FD1 FD2 FD3 FD4

M/B 橢圓孔

M/B KB 橢圓孔

0418 Add for LAN screw hole

H9 HOLEA — H_2P5
H6 HOLEA — CHASSIS1_GND, H_3P0
H10 HOLEA — H_2P5
H11 HOLEA — H_2P5
H7 HOLEA — H_2P5
H8 HOLEA — H_2P5
H13 HOLEA — H_2P5
H15 HOLEA — H_2P5N
H29 HOLEA — H_4P0
H26 HOLEA — H_1P5N
H27 HOLEA — H_1P5N

R

H14 HOLEA — H_5P4X2P5
H16 HOLEA — H_5P9X3P0
H12 HOLEA — H_5P4X2P5

A

2P5 * 9 pcd

F G

H18 HOLEA — H_4P0
H19 HOLEA — H_4P0
H20 HOLEA — H_4P0
H21 HOLEA — H_3P3
H22 HOLEA — H_3P3
H23 HOLEA — CHASSIS1_GND, H_3P3
H24 HOLEA — H_3P3

B CPU C GPU D LAN

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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics,Ltd.

Title: Fintek-Thermal IC/FAN/screw

Size: B | Document Number: LA-8952P | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 34 of 55

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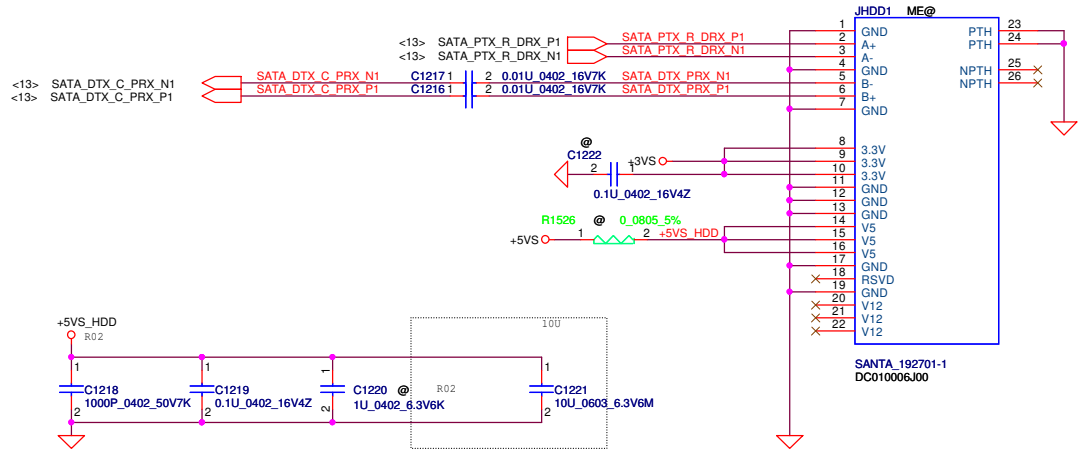
SATA HDD Conn.



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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: **HDD/ODD/BT Connector**

Size	Document Number	Rev
Custom	LA-8952P	0.1

Date: Thursday, January 10, 2013 | Sheet 35 of 55

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600ohms @100MHz 1A
P/N: SM01000BU00

600ohms @100MHz 2A
P/N: SM01000EE00

Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage

U50
ALC259Q-VC2-GR_QFN48_6X6

Vendor recommend. 2.2u
Vendor recommend. 2.2K
external MIC
Internal Speaker
Headphone
0110 delete R1539
0425 EMI request to add these two bead.
0522 EMI request to add C83 and C84

MIC Sense
R939 place near pin13

Capless HP Sense
R940 place near pin34

Place near Pin25
Place near Pin38
Place near Pin1
Place near Pin9
Place next to pin 27

Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

wide 25MIL

Reserve for ESD request.

Combo Jack detect (normal open)

EMI

PC Beep

GND
GNDA

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Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

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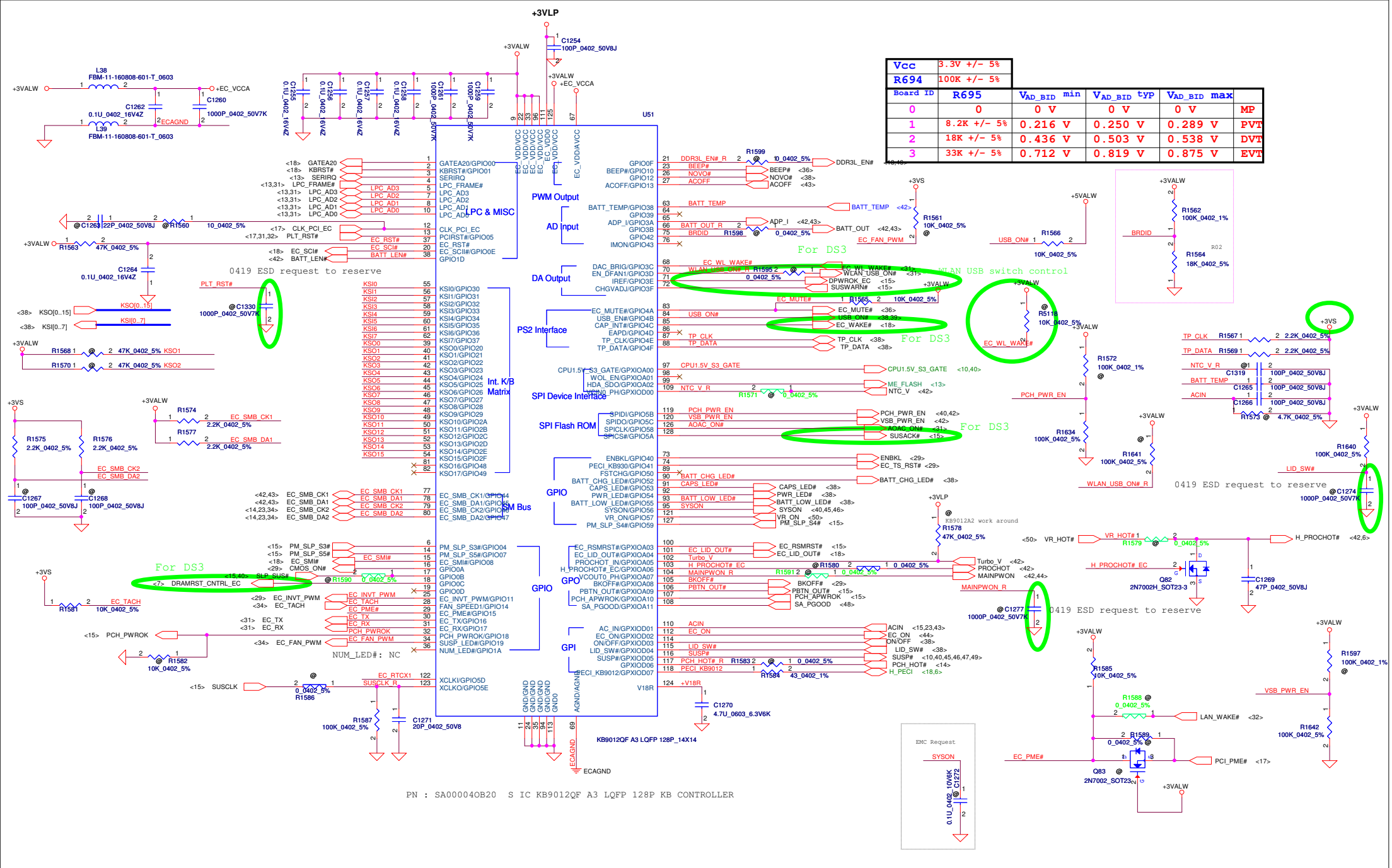
Compal Electronics,Ltd.
Title: HD Audio Codec_ALC259Q-VC
Size: C | Document Number: LA-8952P | Rev: 0.1
Date: Thursday, January 10, 2013 | Sheet 36 of 55



Vcc	3.3V +/- 5%
R694	100K +/- 5%

Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: BIOS & EC I/O Port

Size: Custom | Document Number: LA-8952P | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 37 of 55

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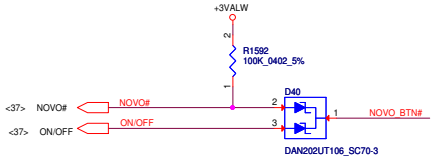
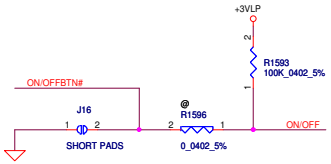
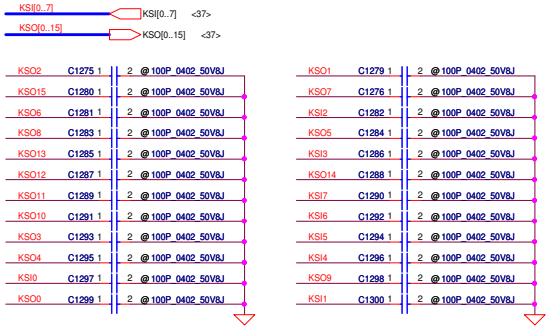
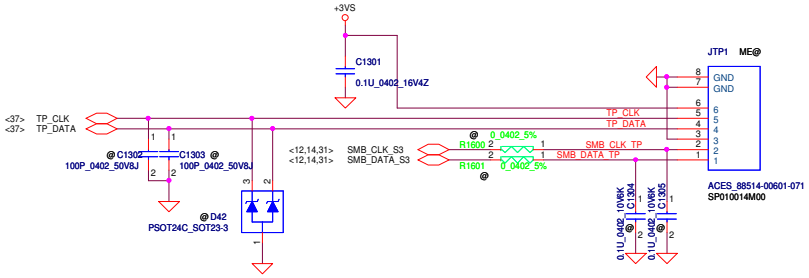
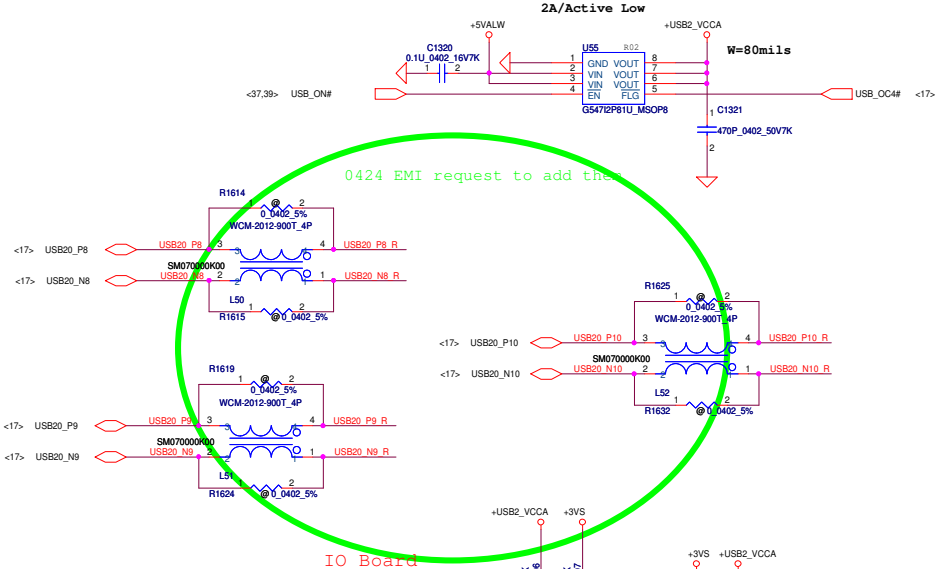


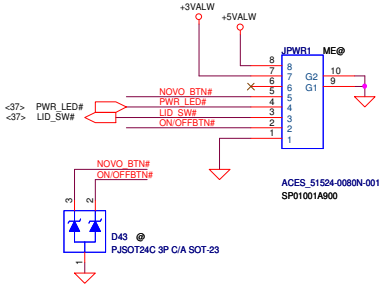




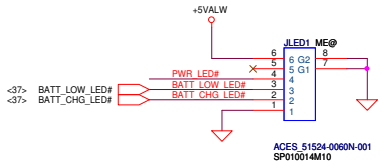




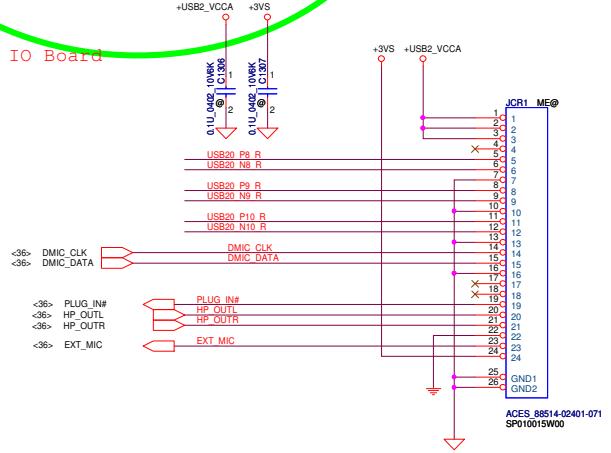
Power Board



LED Board



IO Board



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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.			
Title	ROM/KBD/PWR/CR/LED/TP Conn.		
Size C	Document Number LA-8952P		Rev 0.1
Date: Thursday, January 10, 2013	Sheet 38 of 55		

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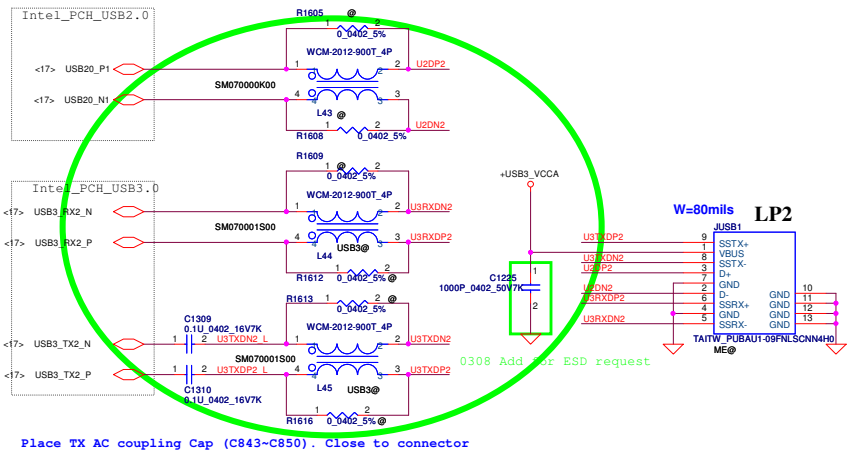
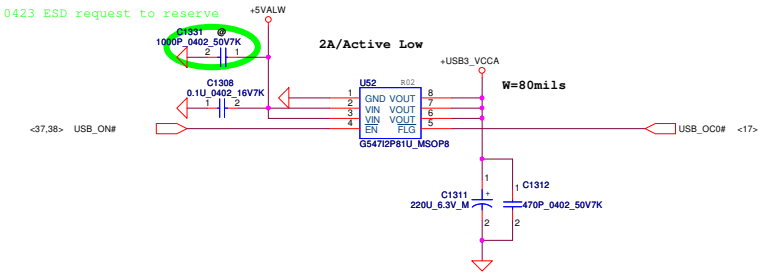
0424 EMI request to add them

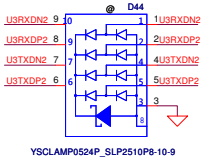


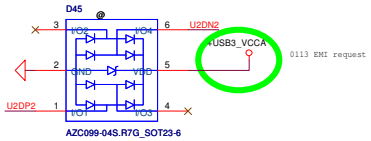
0308 Add for ESD request

Place TX AC coupling Cap (C843~C850). Close to connector

0423 ESD request to reserve







For EMI request

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Compal Electronics, Inc.

Title: USB3.0/Left USB Ports

Size	Document Number	Rev
Custom		0.1

Date: Thursday, January 10, 2013 Sheet 39 of 55

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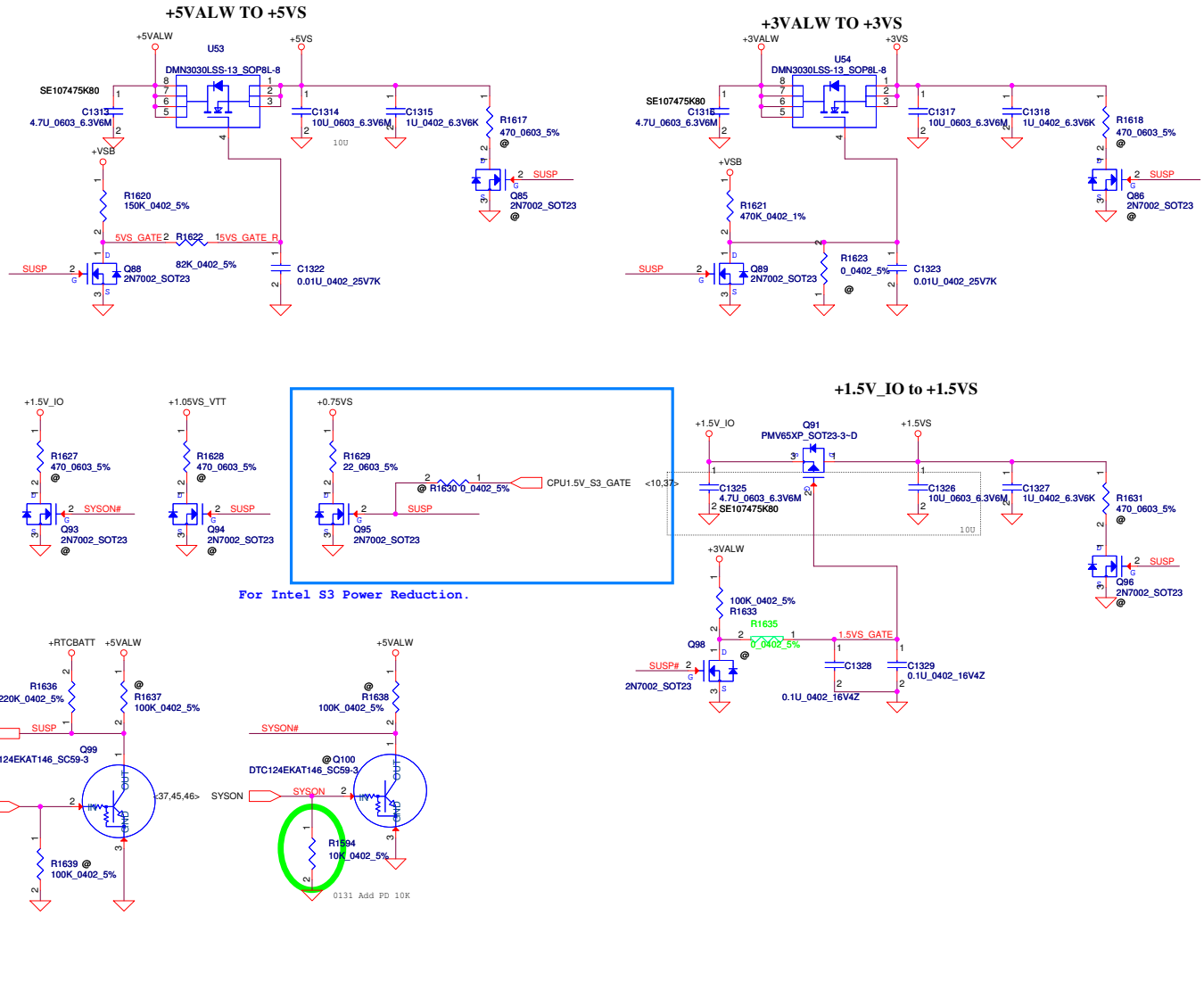

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Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA-8952P | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 40 of 55

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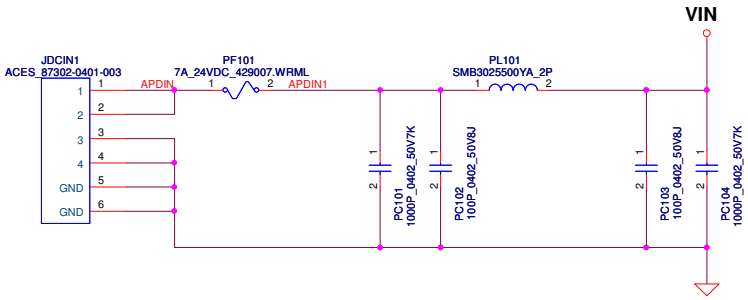

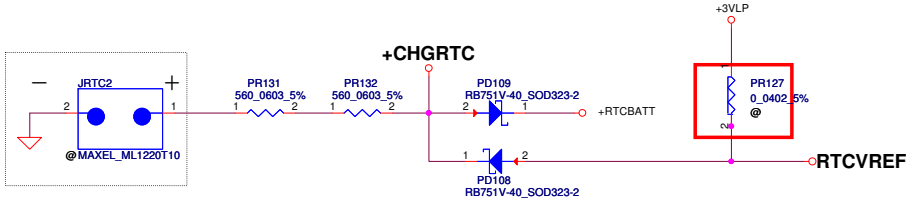

RTC Battery

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: PWR DCIN

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 41 of 55

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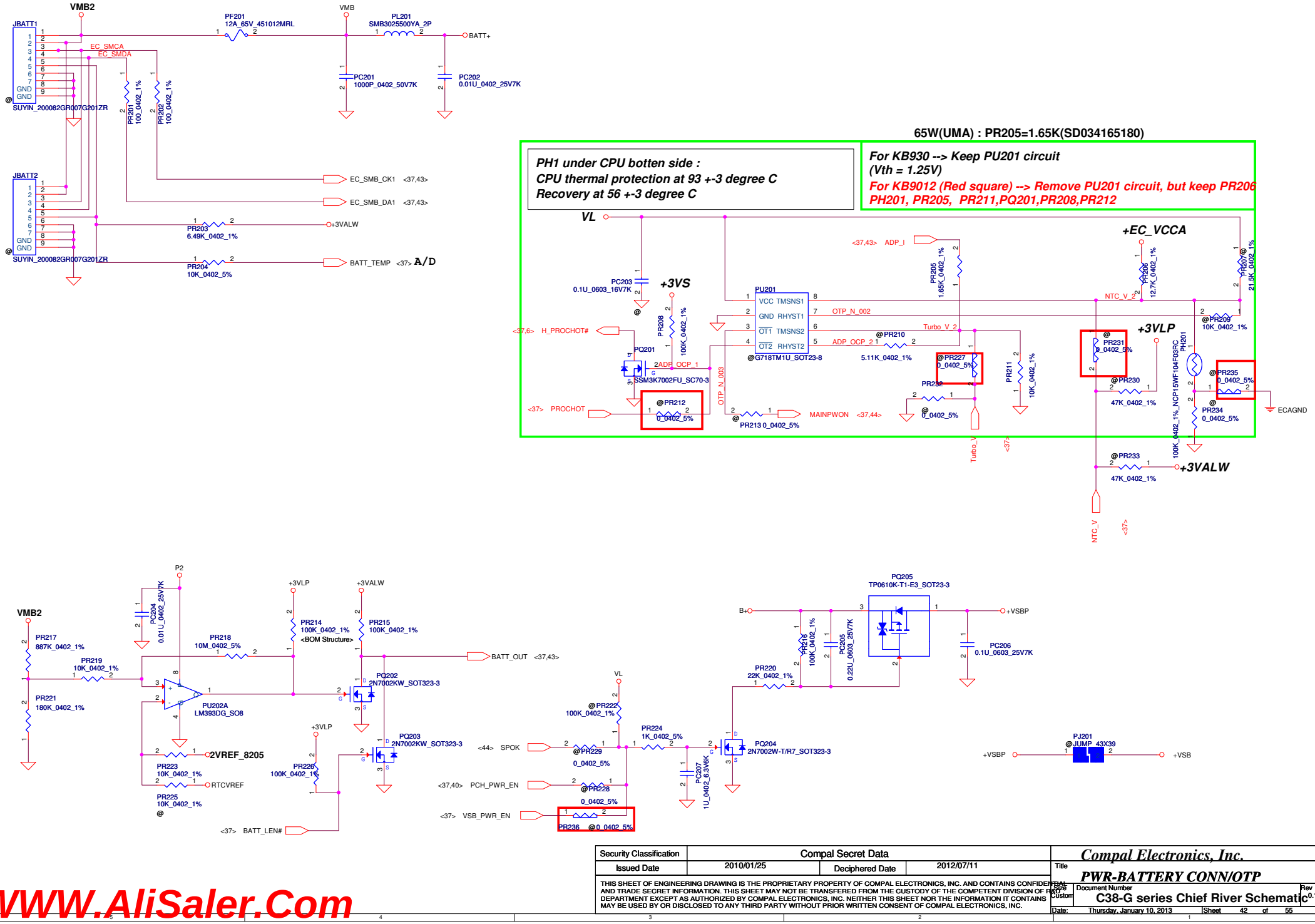

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 42 of 55

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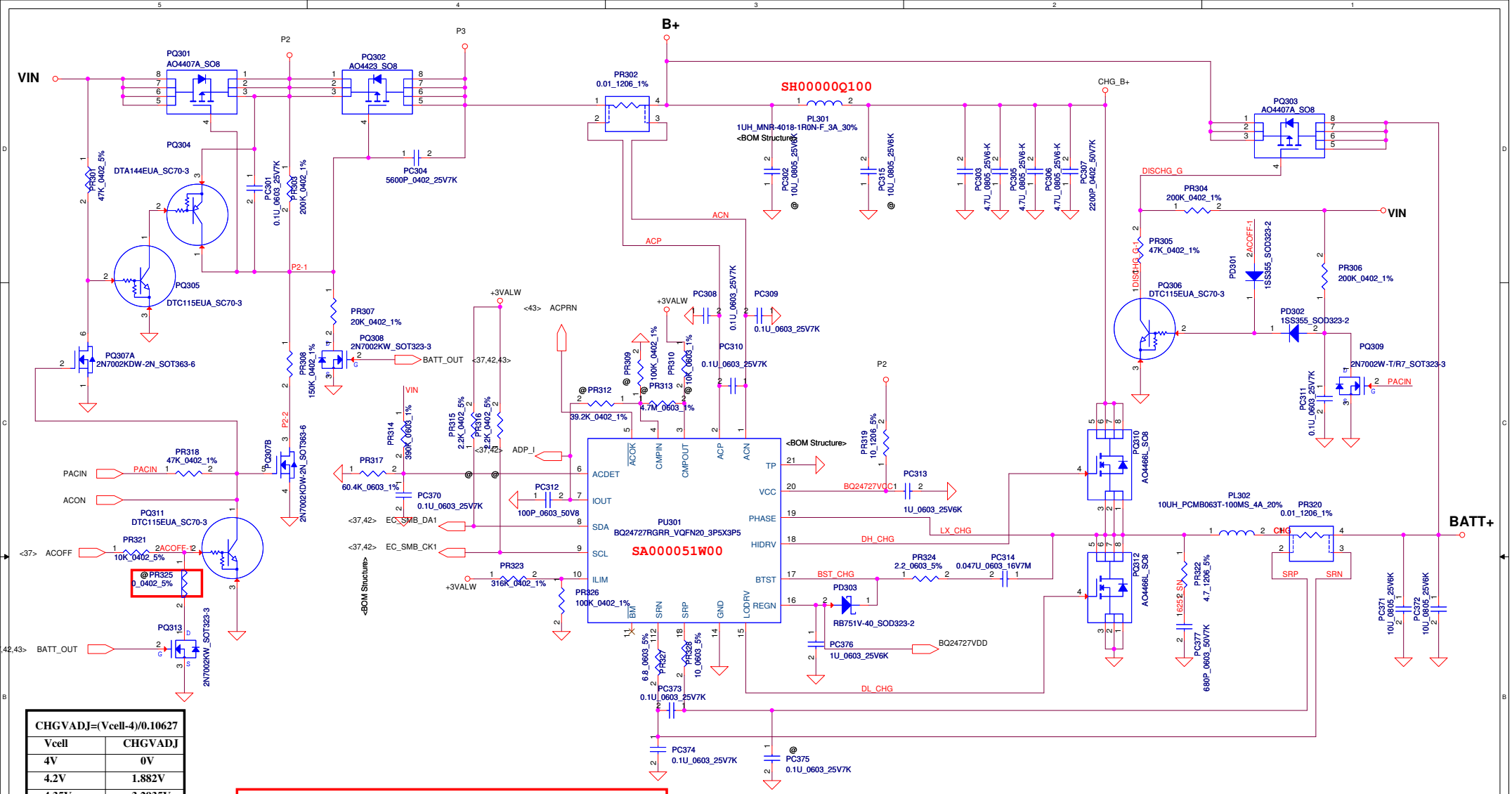

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 43 of 55

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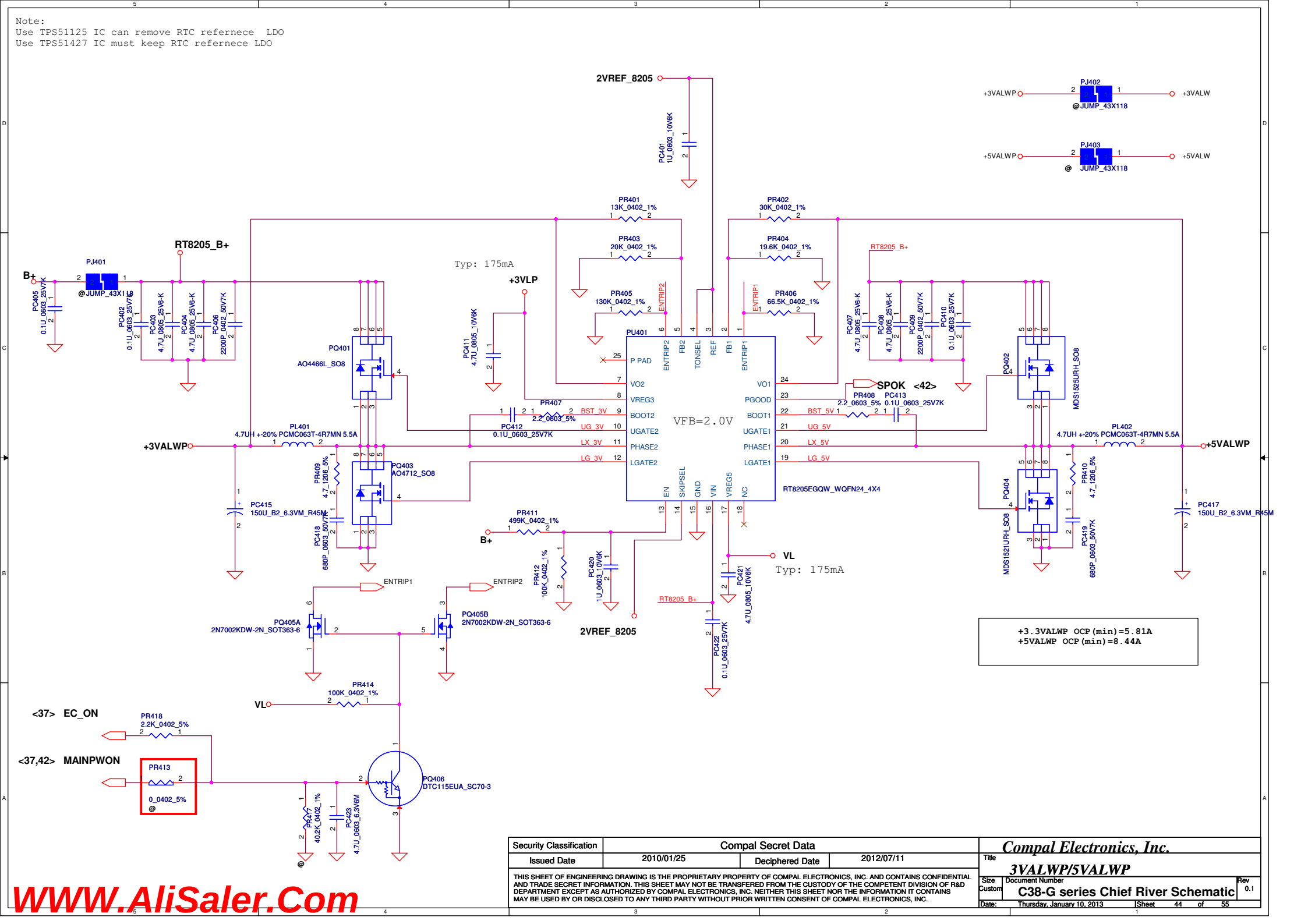
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 44 of 55

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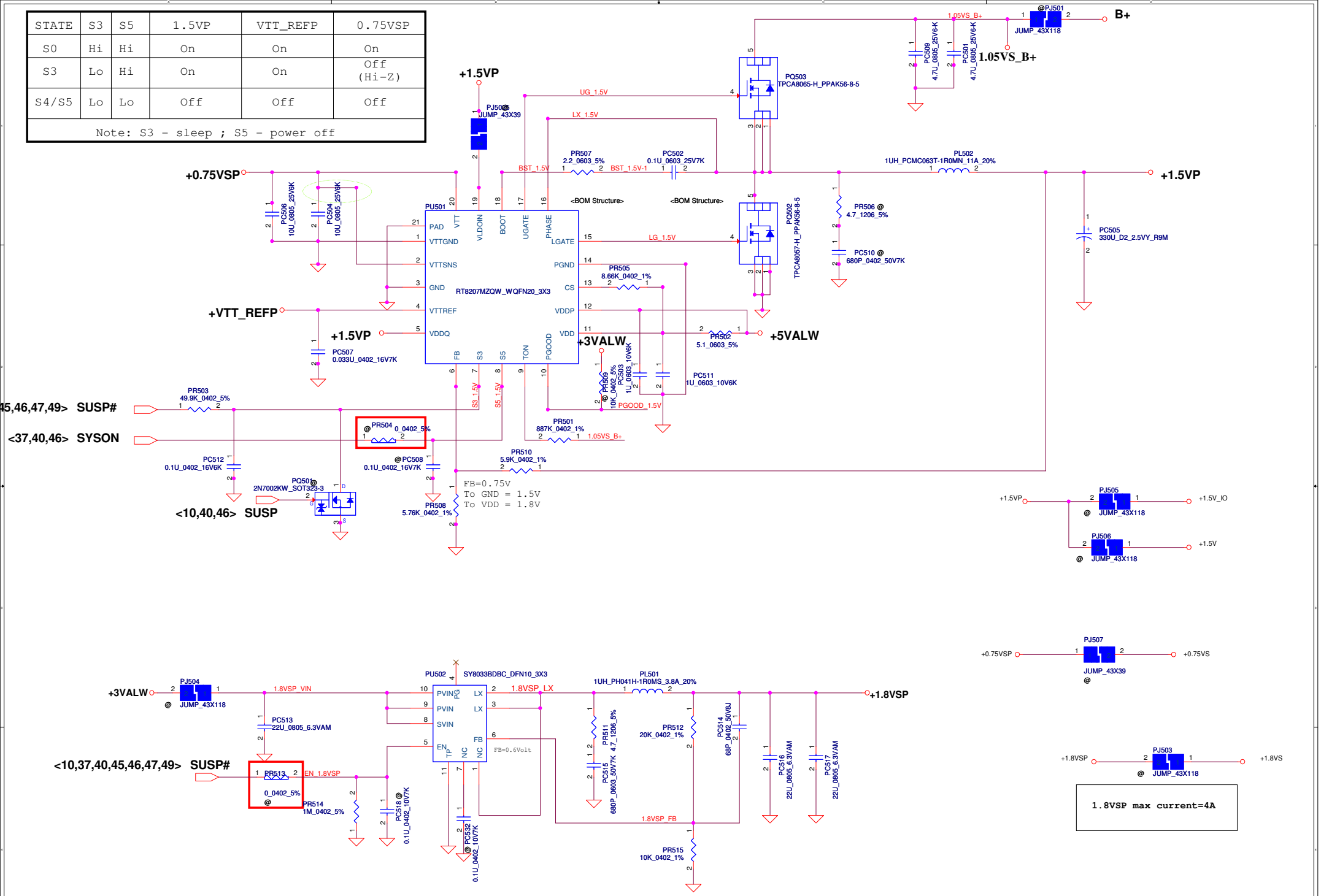
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off



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Issued Date	2010/01/25	Deciphered Date	2012/07/11

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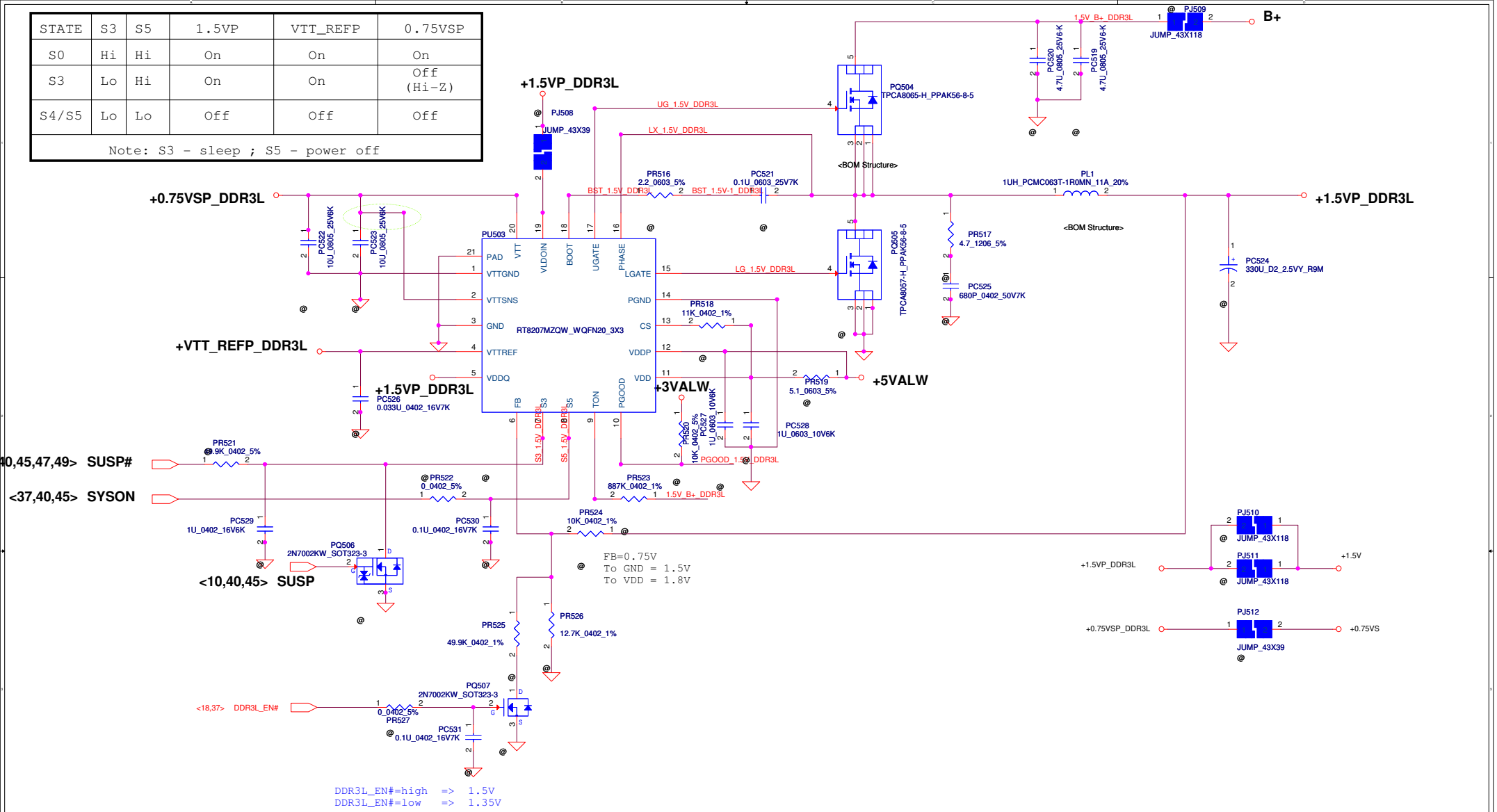
Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 45 of 55

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



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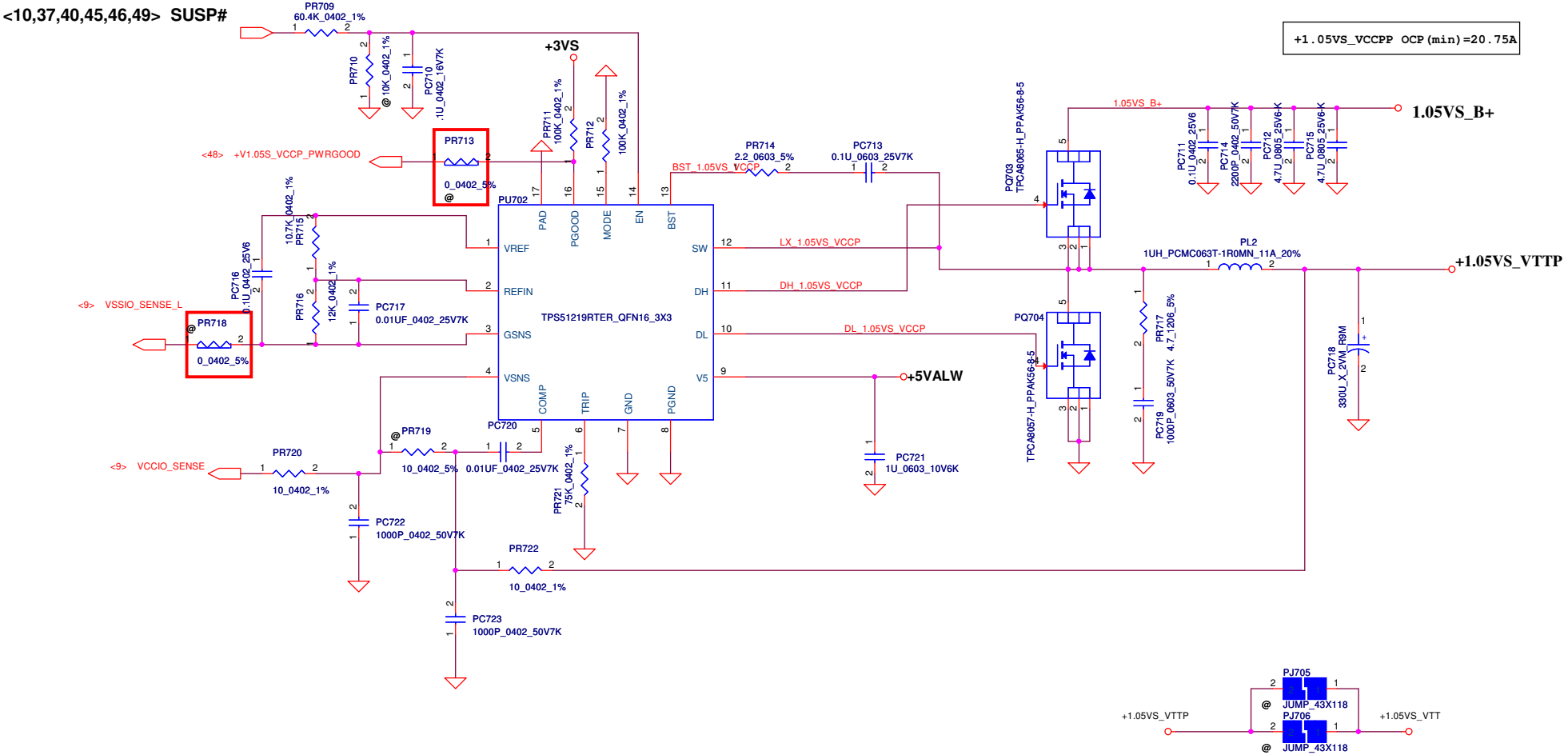
Compal Electronics, Inc.			
Title: PWR-+1.5VP/+1.8VSP			
Size: Custom	Document Number: C38-G series Chief River Schematic		Rev: 0.1
Date: Thursday, January 10, 2013		Sheet 46 of 55	



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 47 of 55

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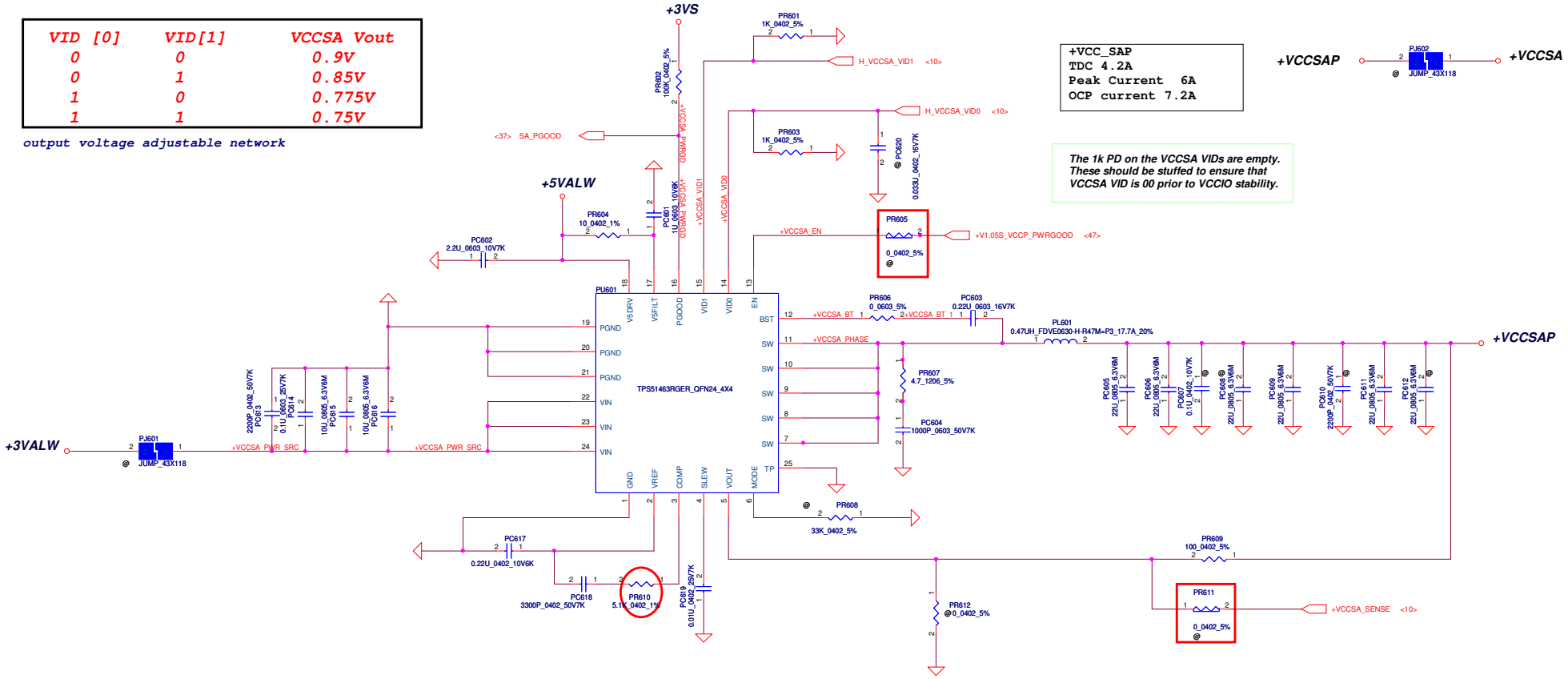
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



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Issued Date	2010/01/25	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: PWR +VCCSAP

Size	Document Number	Rev
C	C38-G series Chief River Schematic	0.1

Date: Thursday, January 10, 2013 Sheet 48 of 55

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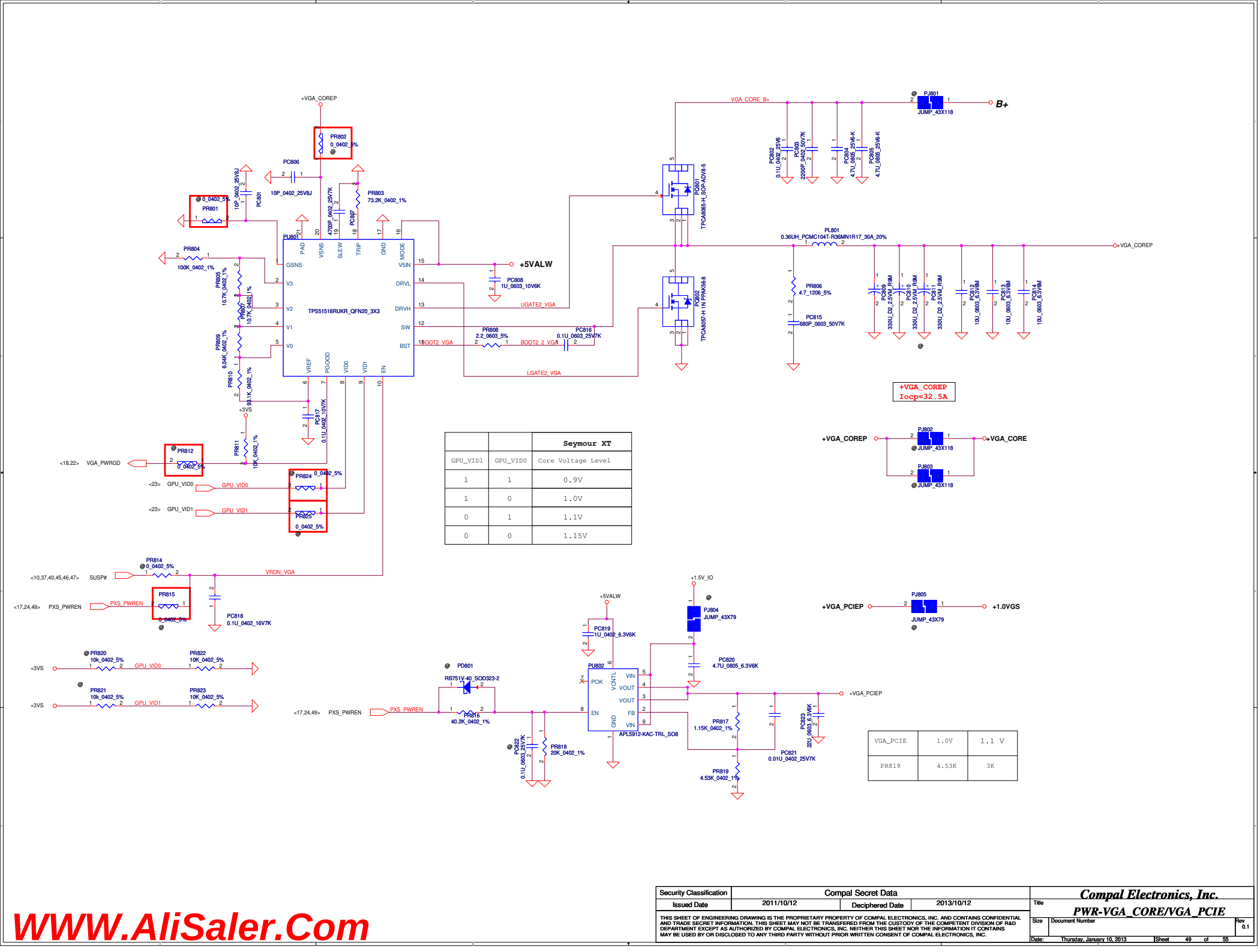

		Seymour XT
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.1V
0	0	1.15V

VGA_PCIE	1.0V	1.1 V
PR819	4.53K	3K

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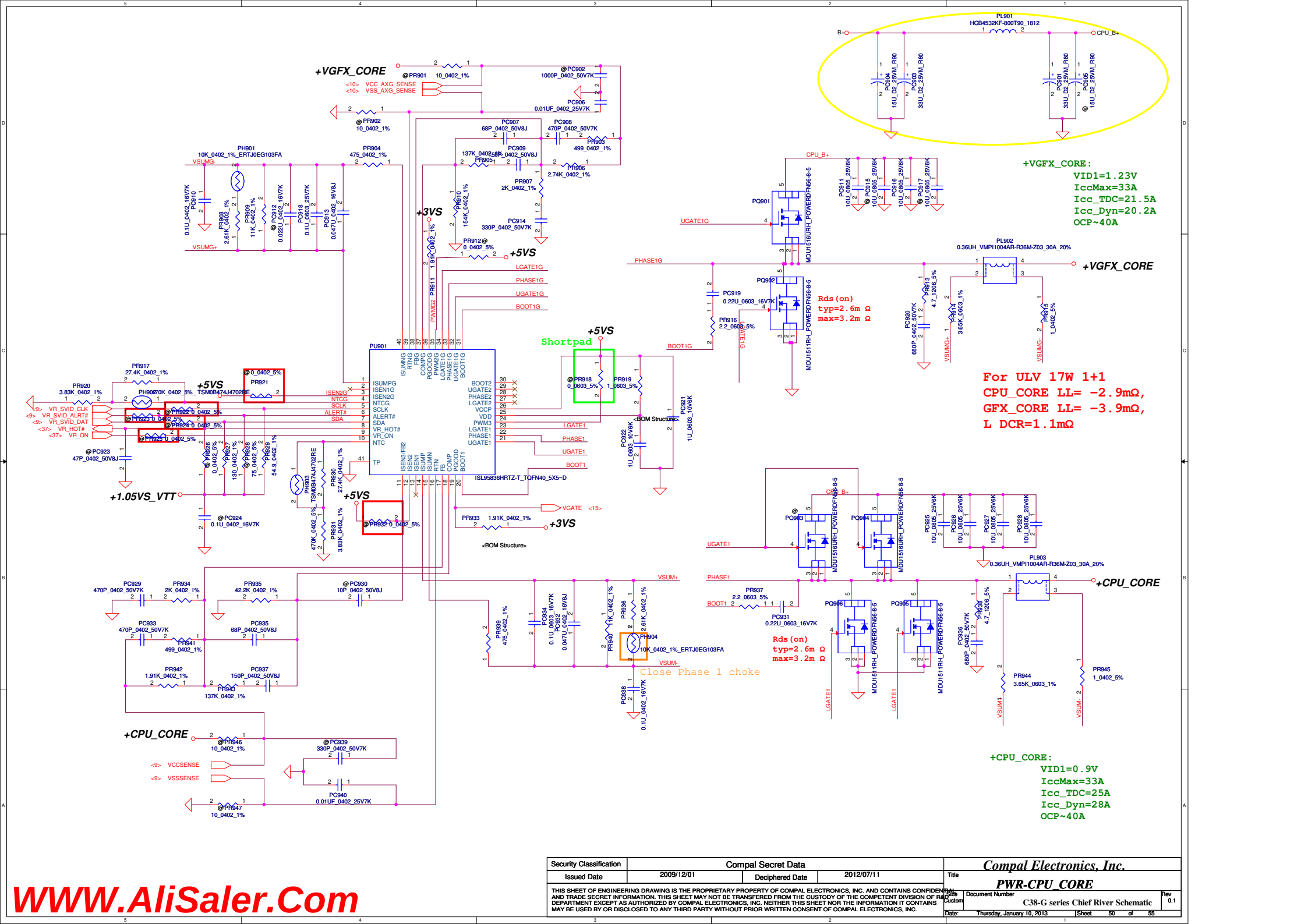
Compal Electronics, Inc.		
Title	PWR-VGA_CORE/VGA_PCIE	
Size	Document Number	Rev 0.1
Date: Thursday, January 10, 2013	Sheet 49 of 55	



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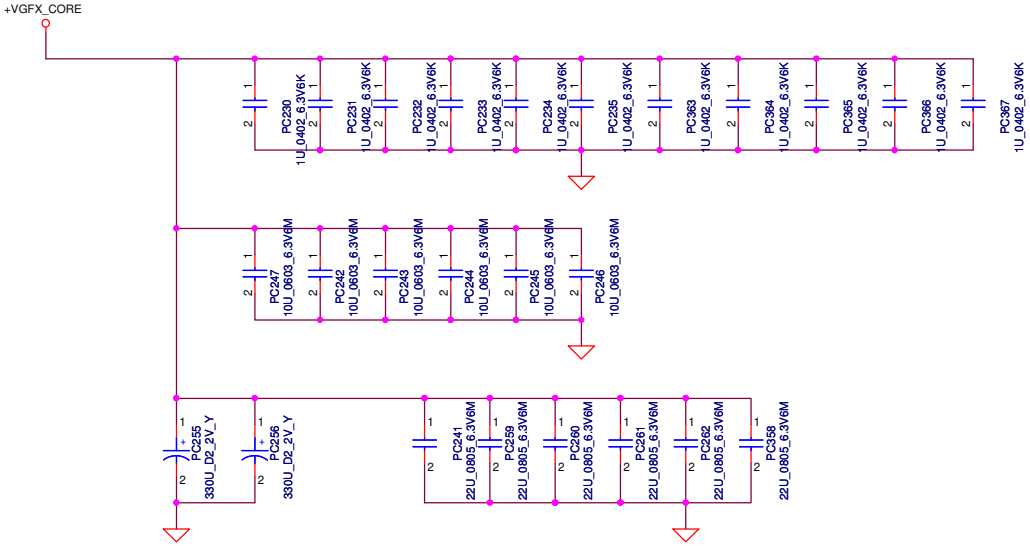
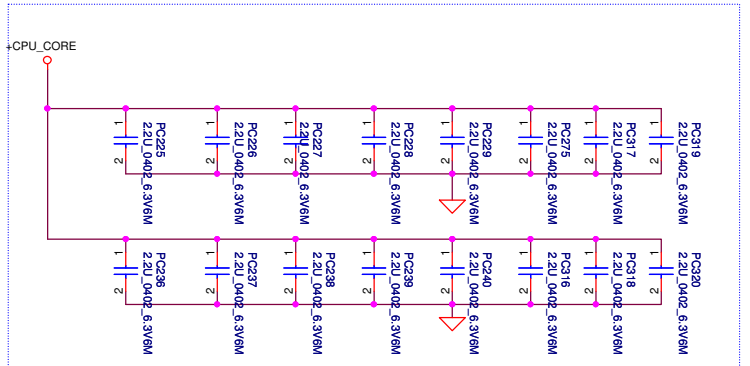
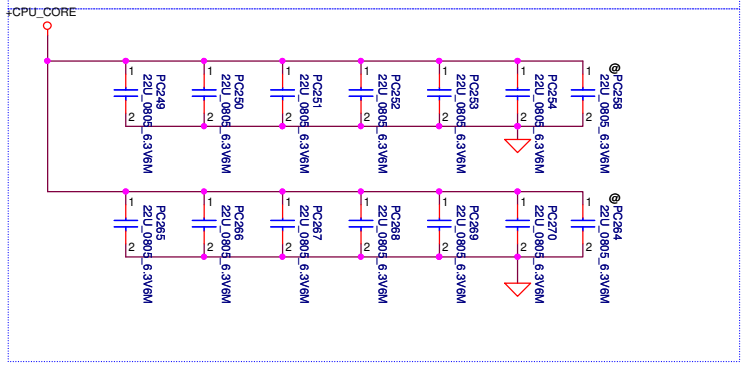
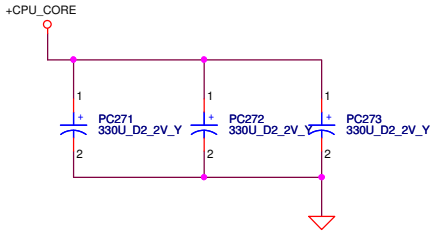


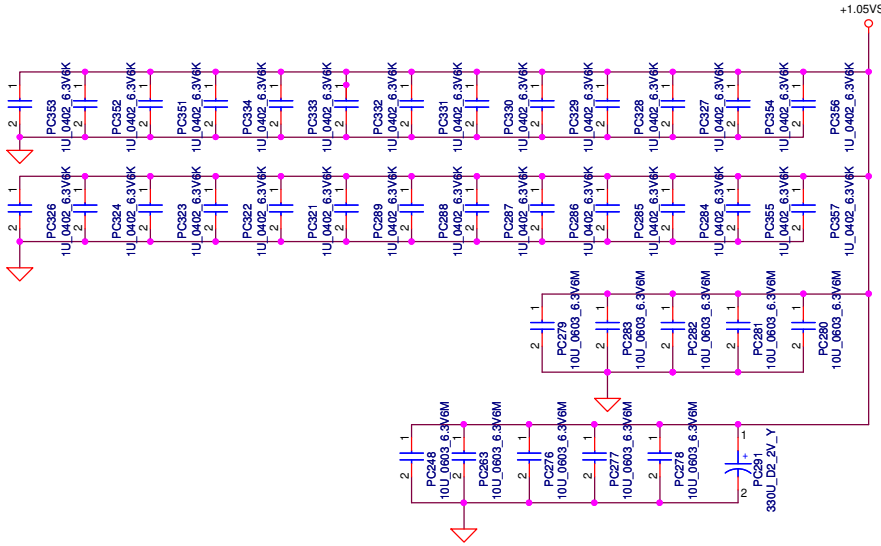


For BOT side



For TOP side





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Compal Electronics, Inc.

Title: CPU_CORE_CAP

Size: Custom | Document Number | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 51 of 55

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Version change list (P.I.R. List)

Item	Modify List	PG#	Reason for change	Date	Phase
1	Reserve support DDR3L circuit	P46	For Coustom request	2012.1.19	EVT
2	co-lay 1.8VSP for SY8033 and SY8035	P45		2012.2.24	DVT
3	Remove PX_mode signal	P49	For HW request	2012.3.12	DVT
4	Change PR503 form 0ohm to 49.9Kohm. Change PC512 from 1U to 0.1U.	P45	For S3 resum will shutdown issue.	2012.3.12	DVT
5	Change PR805 form 11.8Kohm to 10.7Kohm. Change PR807 from 5.11K to 10.7K. Change PR809 from 7.68K to 6.04K. Change PR810 from 97.6K to 93.1K.	P49	For AMD request to adjust VGA_CORE voltage.	2012.3.12	DVT
6	Add Batt_out to KB9012 pin66	P43	For Battery learning reserve.	2012.3.12	DVT
7	Remove DDR3L circurt.	P46	For reserve circuit.	2012.5.28	SVT
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Security Classification	Compal Secret Data		
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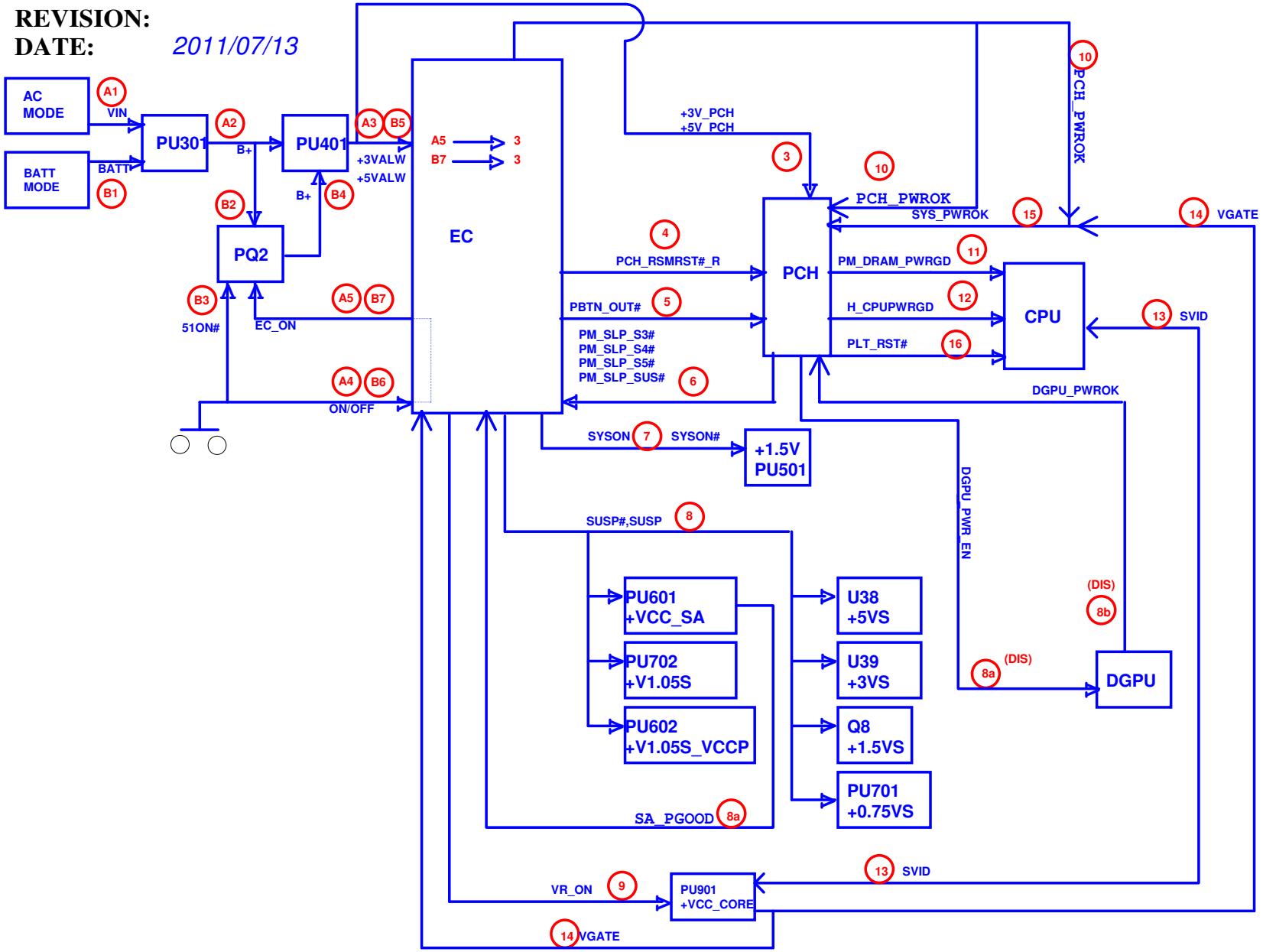
Compal Electronics, Inc.			
Title	PIR (PWR)		
Size: Custom	Document Number: C38-G series Chief River Schematic		Rev: 0.1
Date: Thursday, January 10, 2013	Sheet 52 of 55		

COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



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Compal Electronics, Inc.

Title: Power sequence

Size: Custom | Document Number: LA-8951P | Rev: 1.0

Date: Thursday, January 10, 2013 | Sheet 53 of 55

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Initial：co-lay JLVDS2 (40pin) from LA-8951PR30				EVT
2	For touch screen function	P.29	adding JLVDS2、R721	2013/01/07	EVT
3	For touch screen function	P.17 P.29 P.37	adding nets EC_TS_RST#、TS_RST#、USB20_P3、USB20_N3	2013/01/07	EVT
4					
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Compal Electronics, Inc.

Title: HW-PIR1

Size: Custom | Document Number: LA-8952P | Rev: 0.1

Date: Thursday, January 10, 2013 | Sheet 54 of 55