Model Name : EA/EG50_CX (Z5WE1)
File Name : LA-9535P

Compal Confidential

EA/EG50_CX (Z5WE1) M/B Schematics Document

Intel Ivy Bridge ULV Processor + Panther Point PCH

Nvidia N14M-GE & N14P-GV2

2013-06-07

REV:1.0

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Compal Electronics, Inc.		
Title: Cover Page		
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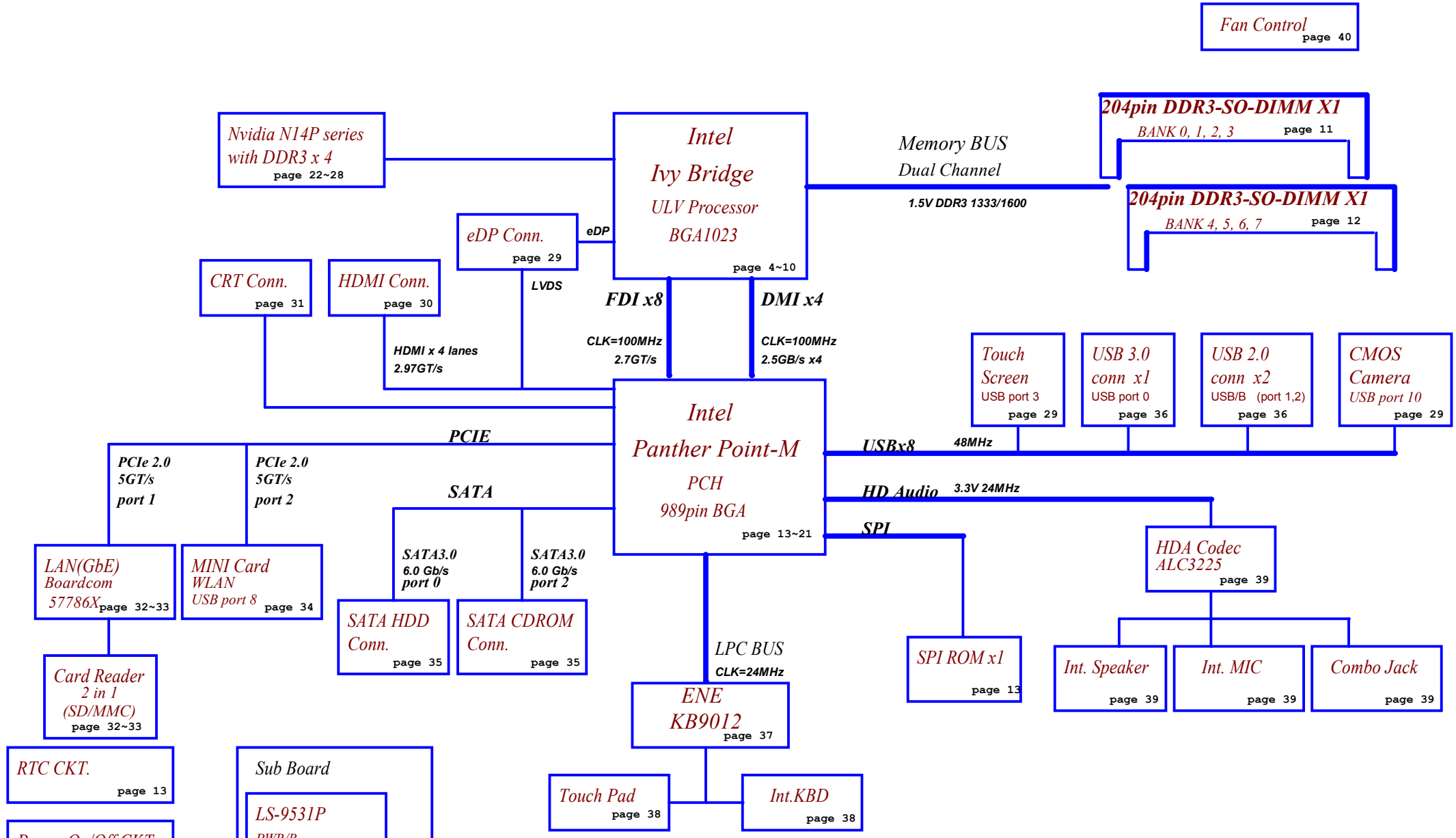

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Compal Electronics, Inc.			
Title	Block Diagrams		
Size: Custom	Document Number: LA-9535P M/B Schematics		Rev: 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+0.75VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	+0.95VSDGPUP to +0.95VSDGPU switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.35VP to +1.35V power rail for DDRIIIL	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VSDGPUP to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	+3VS to 1.8V switched power rail to CPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU switched power rail for GPU	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X

EC SM Bus2 address

Device	Address
VGA Internal Thermal Senser	1001 111x (0x9E)

PCH SM Bus address

Device		Address	
ChannelA	DIMM0	1001 000x	JDIMM1
ChannelB	DIMM1	1001 010x	JDIMM2

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

USB Port Table

USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Left 3.0)
	1	USB Port(Right 2.0)
	2	USB Port(Right 2.0)
	3	Touch Screen
	4	
	5	
	6	
	7	

USB 2.0	Port	
EHCI2	8	Mini Card (WLAN+BT)
	9	
	10	Camera
	11	
	12	
	13	

USB 3.0	Port	
XHCI	0	USB Port(Left 3.0)
	1	
	2	
	3	

BTO Option Table

BTO Item	BOM Structure
Unpop	@
Connector	CONN@
PCH RTC CMOS	SP@
TEST PAD	TP@
Unpop SPI2	SPI2@
Unpop CPU	CPU@
Unpop GPU	GPU@
Unpop VRAM	VRAM@
Back light	BL@
IOAC	IOAC@
Celeron 847	847@
Celeron 1007	1007@
I3-3227M	I33227@
I5-3337M	I53337@
I7-3537M	I73537@
UMA ONLY GPIO	UMAO@
EDP	EDP@
LVDS	LVDS@
EMC POP	EMC@
EMC NON POP	XEMC@
N14M-GE option	N14MGE@
N14P-GT option	N14PGT@
N14P-GV2 option	N14PGV2@
N14P-GT/GV2 Strap	GV2GT@
VGA SKU	VGA@
VRAM x 8pcs	128@
PEG 16X	16X@
PEG 8X	8X@
GC6	GC6@
NON GC6	NGC6@

BOM Config

UMAO: EDP@/IOAC@/BL@/EMC@/UMAO@/		CPU config
DIS GV2: EDP@/IOAC@/BL@/EMC@/VGA@/	GC6@/N14PGV2@/GV2GT@/8X@/	CPU config + X76
DIS GE: EDP@/IOAC@/BL@/EMC@/VGA@/	GC6@/N14MGE@/8X@/	CPU config + X76

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Compal Electronics, Inc.

Title: Notes List

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ZZZ

Part Number	Description
DAZ10O00100	PCB Z5WE1 LA-9535P LS-9531P/LS-9532P
LA9535_PCB	

REV0 DA6000ZK000
REV1 DA6000ZK010

UCPU1
I33227@ S IC AV8063801119500 SR0XF L1 1.9G ABO!
SA00006D990
AV8063801119500 SR0XF L1 1.9G ABO!

UCPU1
I53337@ S IC AV8063801129900 SR0XL L1 1.8G ABO!
SA00006D860
AV8063801129900 SR0XL L1 1.8G ABO!

UCPU1
I73537@ S IC AV8063801119700 SR0XG L1 2G ABO!
SA00006DB90
AV8063801119700 SR0XG L1 2G ABO!

UCPU1
847@ S IC AV8062700852800 SR08N Q0 1.1G ABO!
SA00005VK20
AV8062700852800 SR08N Q0 1.1G ABO!

UCPU1
1007@ S IC AV8063801118700 SR109 P0 1.5G ABO!
SA00006EW30
AV8063801118700 SR109 P0 1.5G ABO!

IVY BRIDGE

UCPU1
1017@ S IC AV8063801130300 SR10A P0 1.6G ABO!
SA00006UH50
AV8063801130300 SR10A P0 1.6G ABO!

UCPU1
2117@ S IC AV8063801058800 SR0VQ P0 1.8G ABO!
SA000061240
AV8063801058800 SR0VQ P0 1.8G ABO!

UCPU1
2127@ S IC AV8063801119100 SR105 P0 1.9G ABO!
SA00006UG30
AV8063801119100 SR105 P0 1.9G ABO!

UCPU1
I33217@ S IC AV8063801058401 SR0N9 L1 1.8G ABO!
SA00005L5C0
AV8063801058401 SR0N9 L1 1.8G ABO!

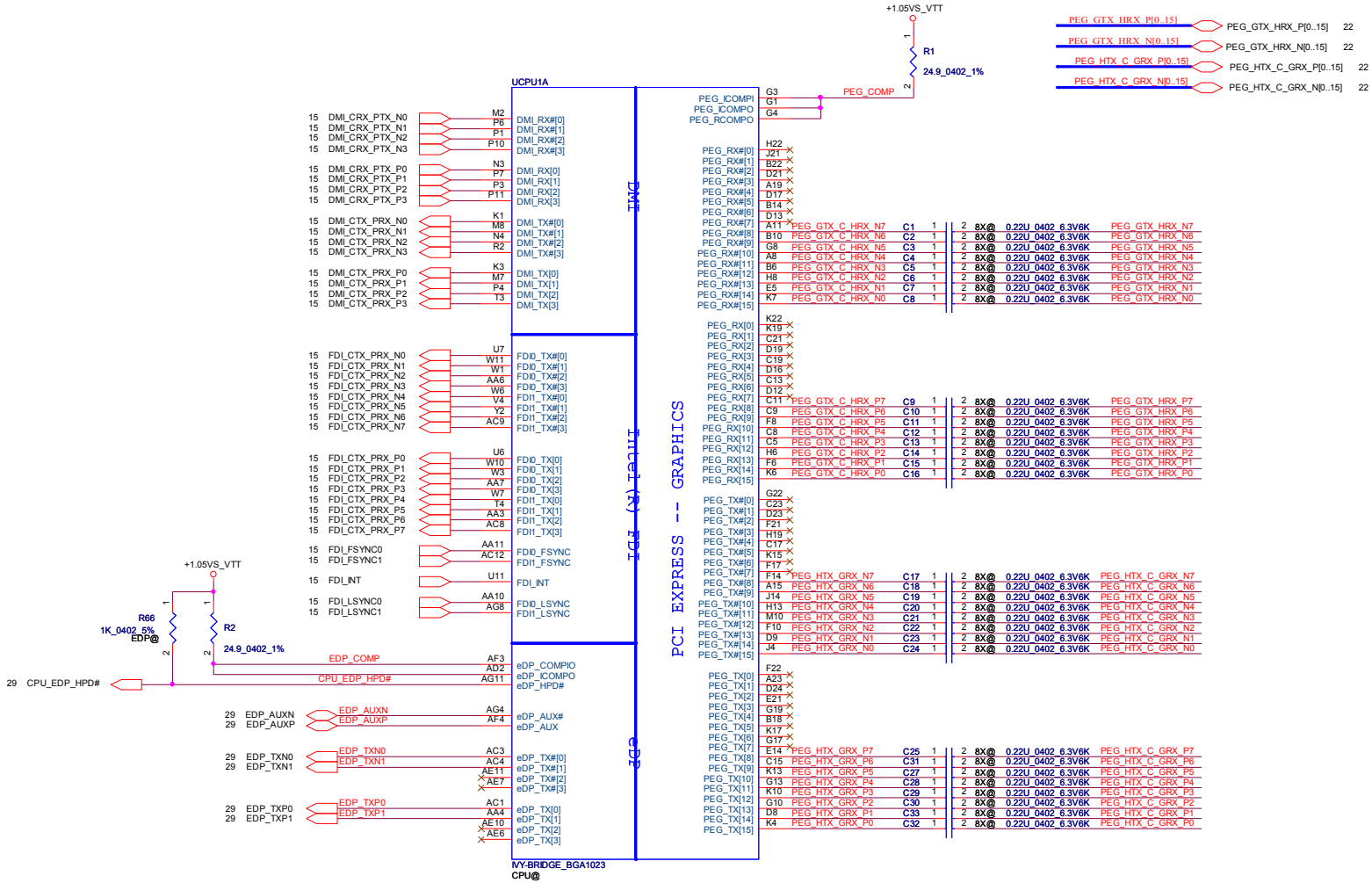
U1010
HM77@ S IC BD82HM77 SLJ8C C1 BGA 989P PCH ABO!
SA00005AGI0
BD82HM77 SLJ8C C1 BGA 989P PCH ABO!

U1010
HM70@ S IC BD82HM70 SJTNV C1 BGA 989P PCH ABO !
SA00005MQ60
BD82HM70 SJTNV C1 BGA 989P PCH ABO !

U1010
NM70@ S IC BD82NM70 SLJTA C1 BGA 989P PCH ABO!
SA00005WU20
BD82NM70 SLJTA C1 BGA 989P PCH ABO!

PCH

1. PEG_RCOMPO and PEG_ICOMPI should be connected together with 4-mil width first. Then be connected to R1 from ball of PEG_ICOMPI.
2. PEG_ICOMPO should be connected to R1 with width 12-mil.
3. No longer than 500-mil to above two.



eDP_COMPIO and eDP_ICOMPO should be connected to R247 respectively.

eDP_COMPIO
Trace Width to R2= 4-mil
Trace Spacing to Other Signals= 15-mil
Max. Routing Length= 500-mil

eDP_ICOMPO
Trace Width to R2= 12-mil
Trace Spacing to Other Signals= 15-mil
Routing Length= 500-mil

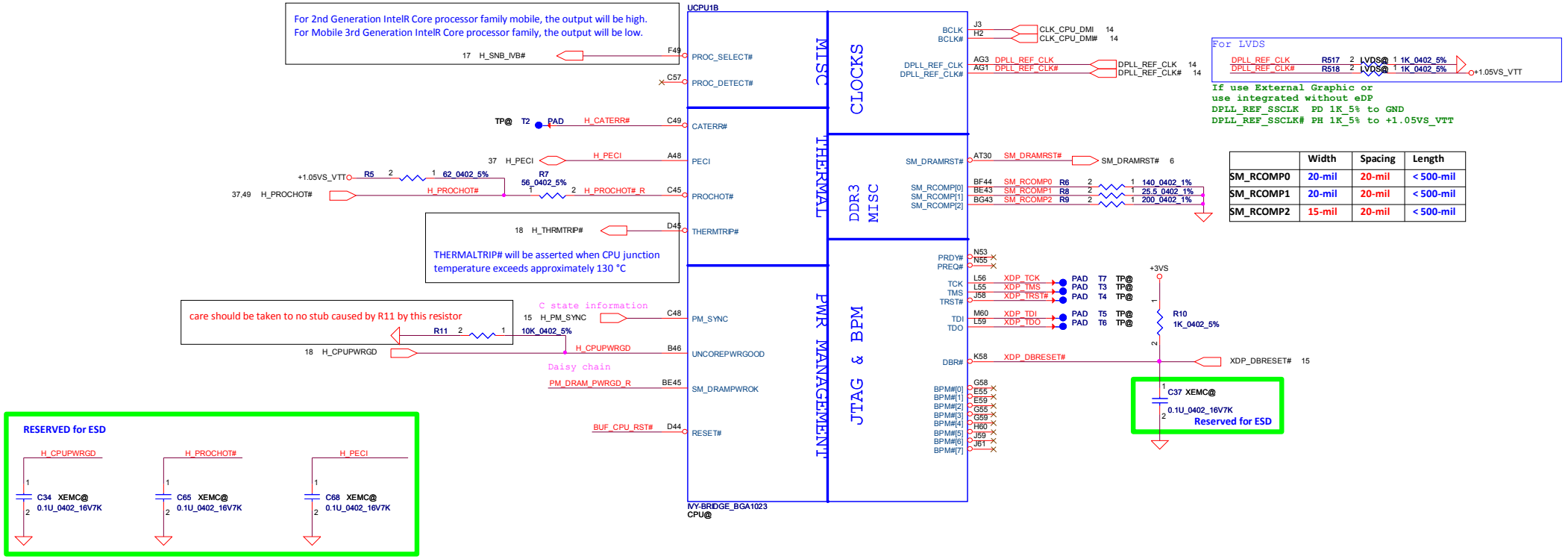
Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

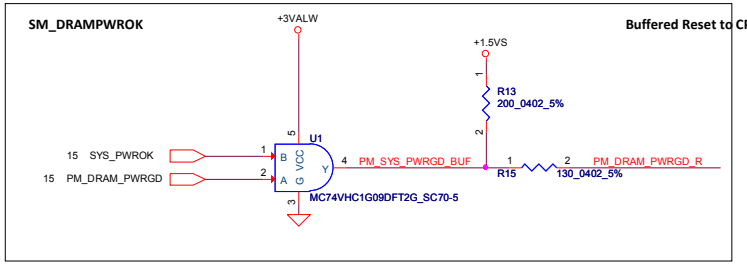
Title: PROCESSOR(1/7) DMI,FDI,PEG

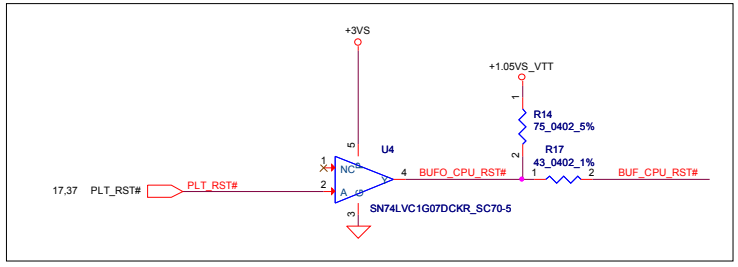
Size	Document Number	Rev
Custom	LA-9535P M/B Schematics	1.0

Date: Friday, June 07, 2013 | Sheet 4 of 55



	Width	Spacing	Length
SM_RCOMP0	20-mil	20-mil	< 500-mil
SM_RCOMP1	20-mil	20-mil	< 500-mil
SM_RCOMP2	15-mil	20-mil	< 500-mil





Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: PROCESSOR(2/7) PWR MANAGMENT

Size	Document Number	Rev
Custom	LA-9535P M/B Schematics	1.0

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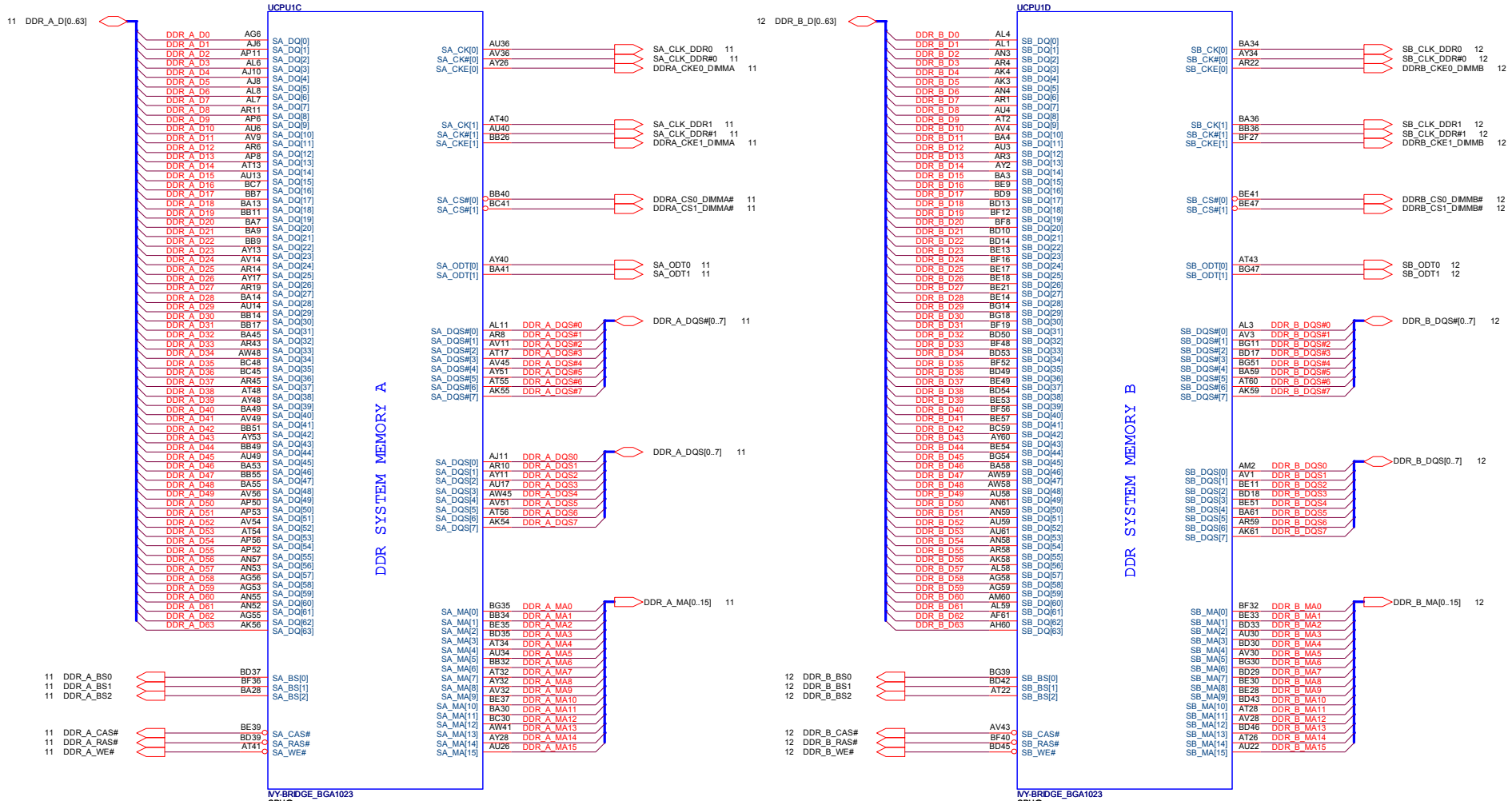

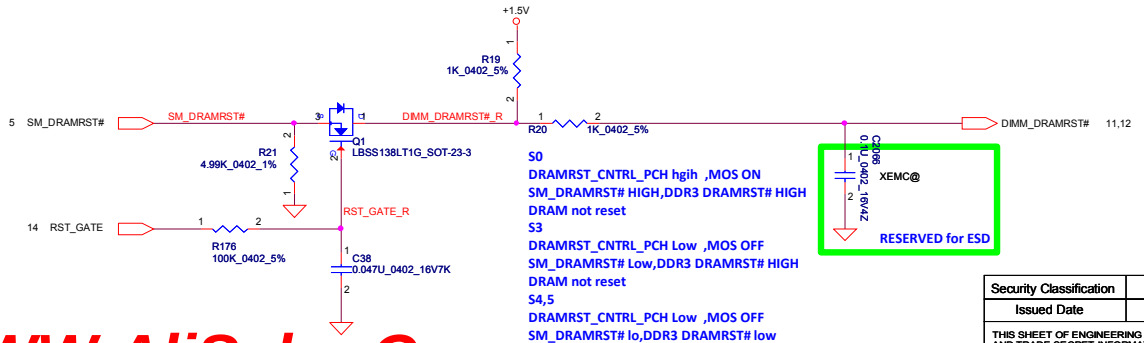

S0
DRAMRST_CNTRL_PCH hgih ,MOS ON
SM_DRAMRST# HIGH,DDR3 DRAMRST# HIGH
DRAM not reset
S3
DRAMRST_CNTRL_PCH Low ,MOS OFF
SM_DRAMRST# Low,DDR3 DRAMRST# HIGH
DRAM not reset
S4,5
DRAMRST_CNTRL_PCH Low ,MOS OFF
SM_DRAMRST# lo,DDR3 DRAMRST# low
DRAM reset

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.			
Title	PROCESSOR(3/7) DDRIII		
Size: Custom	Document Number: LA-9535P M/B Schematics		Rev: 1.0
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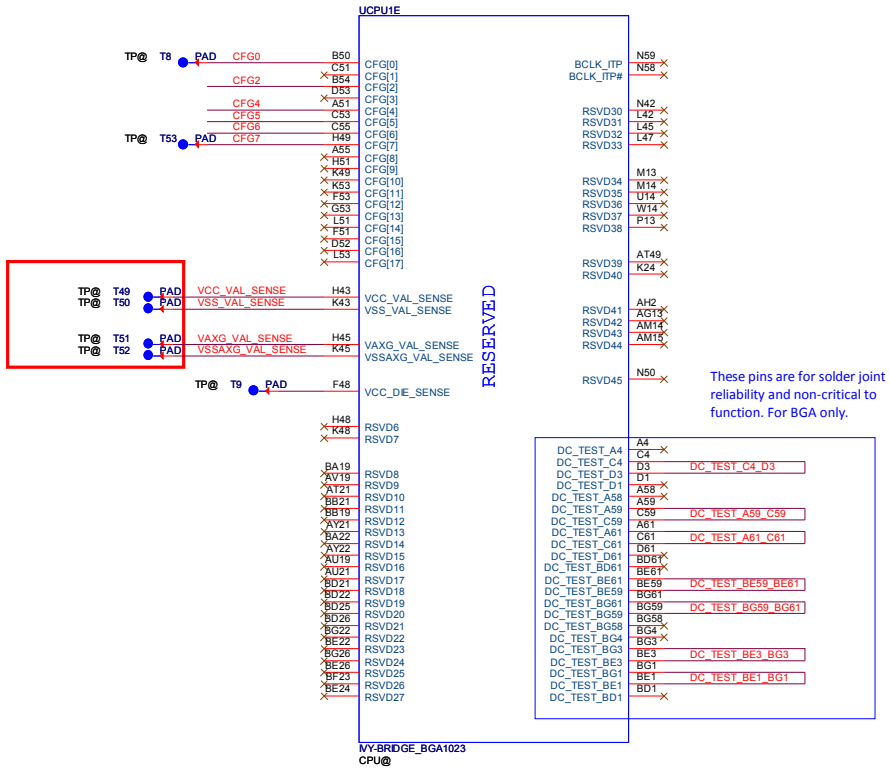
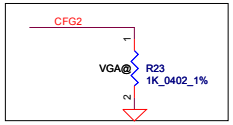
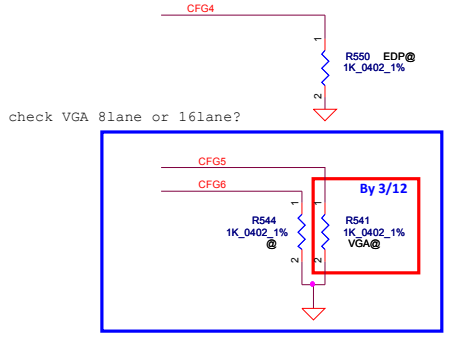


These pins are for solder joint reliability and non-critical to function. For BGA only.

CFG Straps for Processor



PCIe Static x16 Lane Numbering Reversal	
CFG2	1: (Default)Normal Operation Lane # definition matches socket pin map definition * 0: Lane Reversed



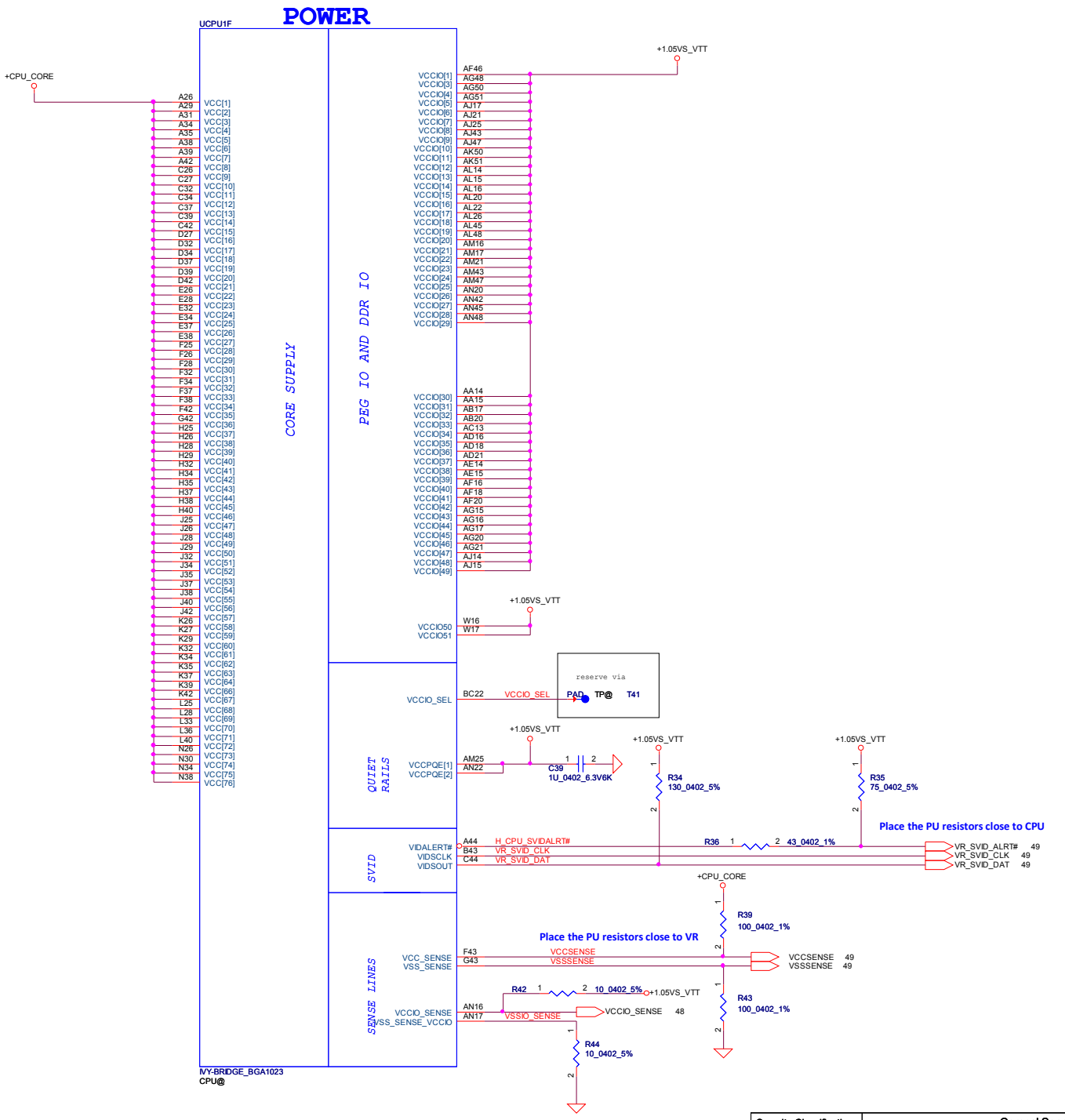
eDP Enable Strap	
CFG4	1: (Default)Disable *0: Enable

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) 1x16 PCI Express *10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express

PEG DEFER TRAINING Tacoma_Fall2 1.0 P.12	
CFG7	* 1: (Default) PEG Trains immediately and follows xxRESETB de-assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.			
Title	PROCESSOR(4/7) RSVD,CFG		
Size: Custom	Document Number: LA-9535P M/B Schematics		Rev: 1.0
Date: Friday, June 07, 2013	Sheet 7 of 55		



CPU Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
VCC	0.65~1.2	33	Processor Core Voltage
VCCIO	1.05	8.5	Processor Uncore Voltage
VDDQ	1.5	5	Memory Controller Voltage
VCCSA	0.675~0.9	4	System Agent Voltage
VCCPLL	1.8	1.2	Processor PLL Voltage
VAXG	0.65~1.25	29	Processor Graphics Voltage

Refer to Mobile 3rd Generation IntelR Core Processor Family External Design Specification (EDS) Volume 1 of 2 Revision 2.2

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

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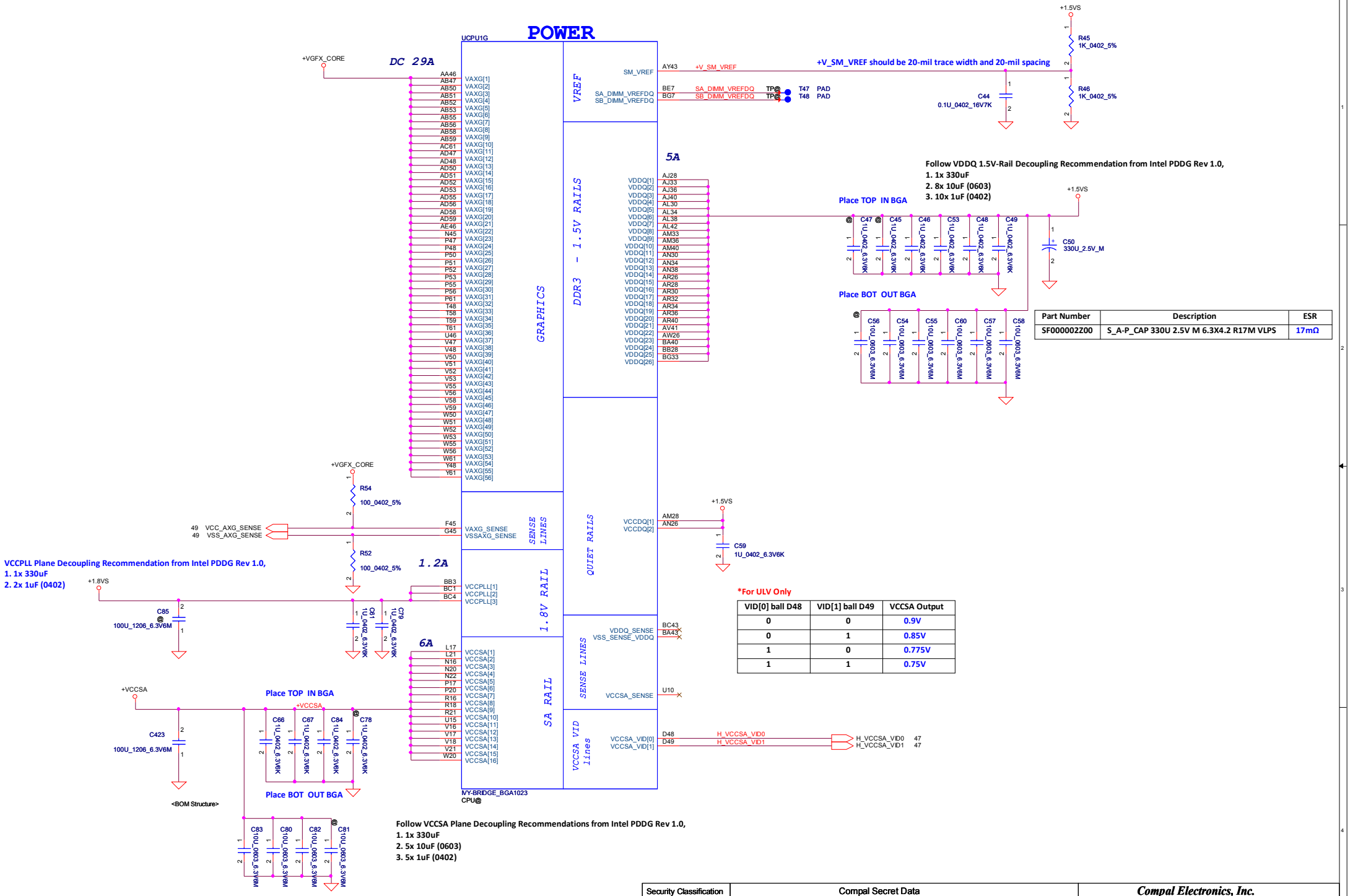
POWER



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Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

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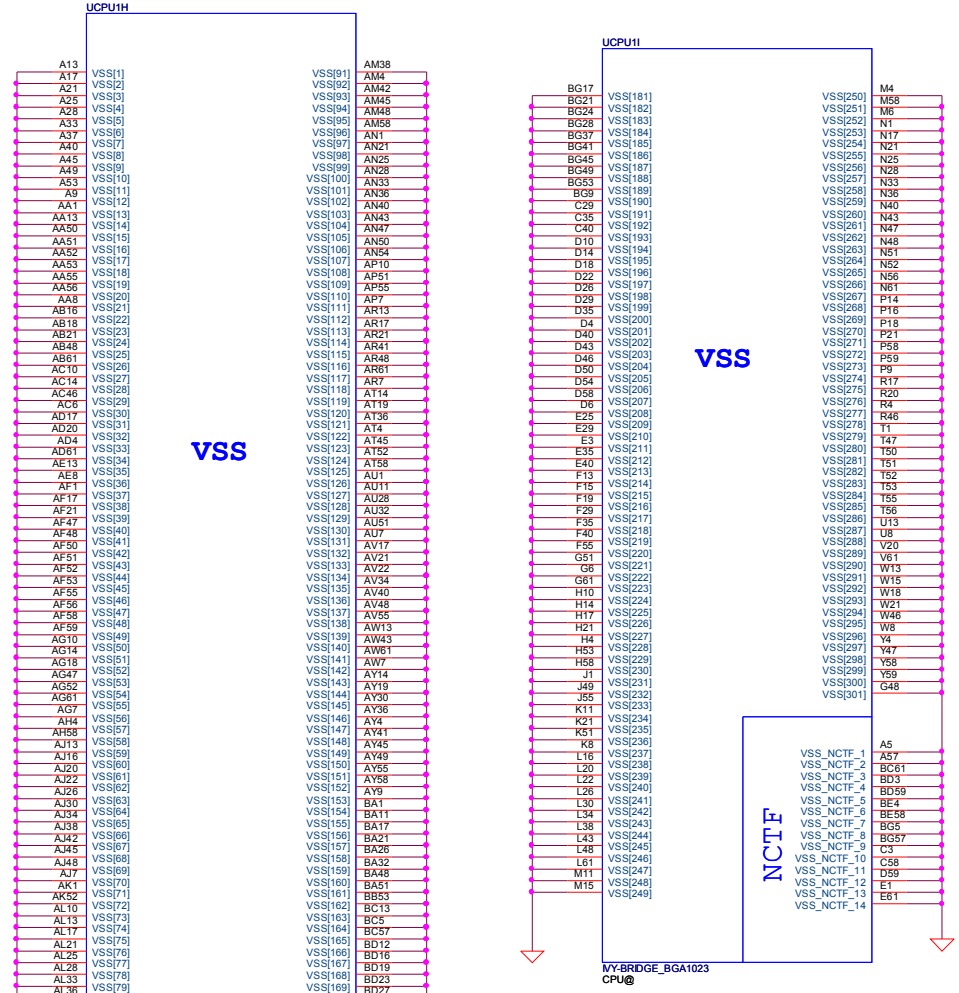

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Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.		
Title	PROCESSOR(7/7) VSS	
Size: Custom	Document Number: LA-9535P M/B Schematics	Rev: 1.0
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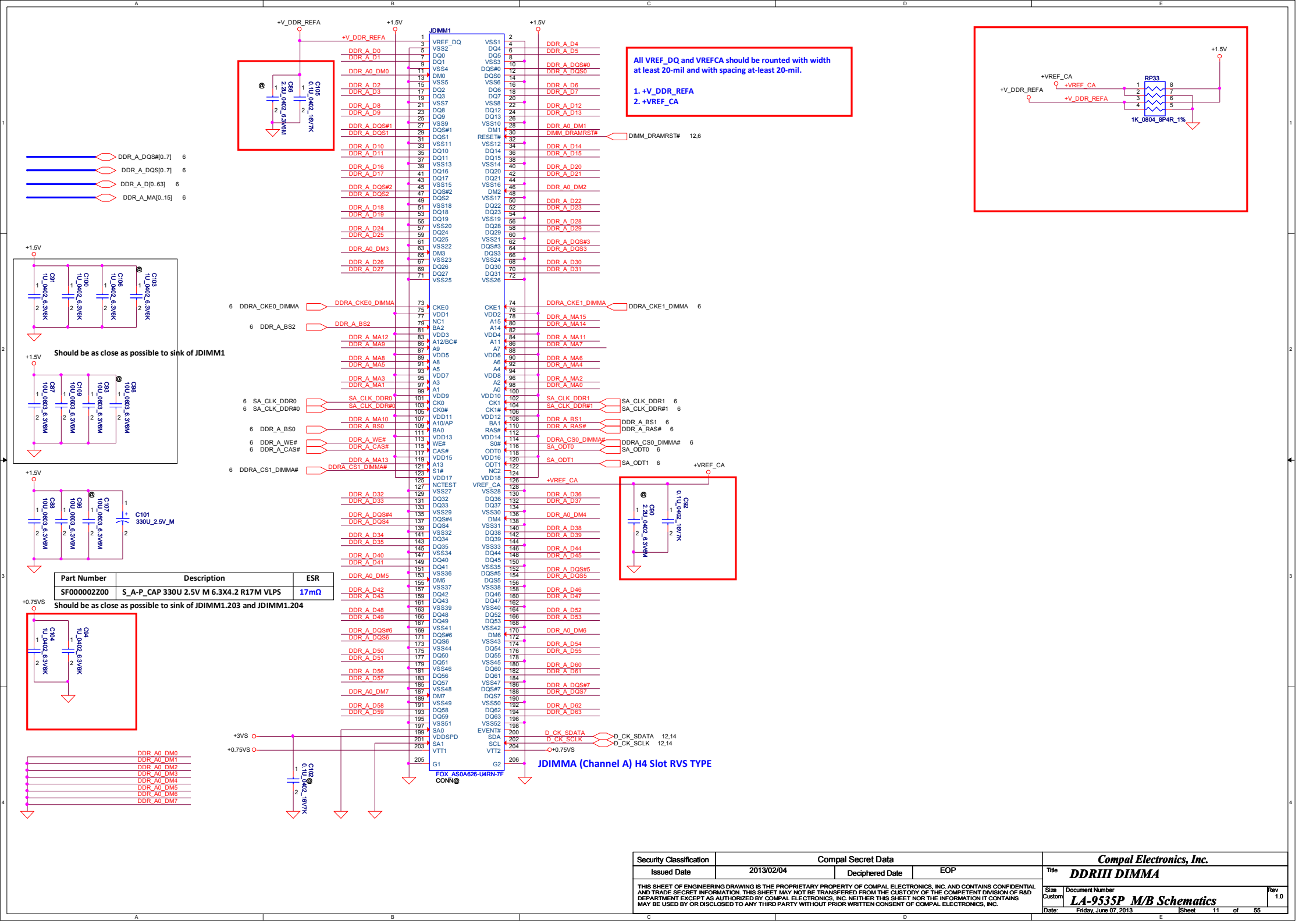

Part Number	Description	ESR
SF000002Z00	S_A-P_CAP 330U 2.5V M 6.3X4.2 R17M VLPS	17mΩ

Security Classification	Compal Secret Data		
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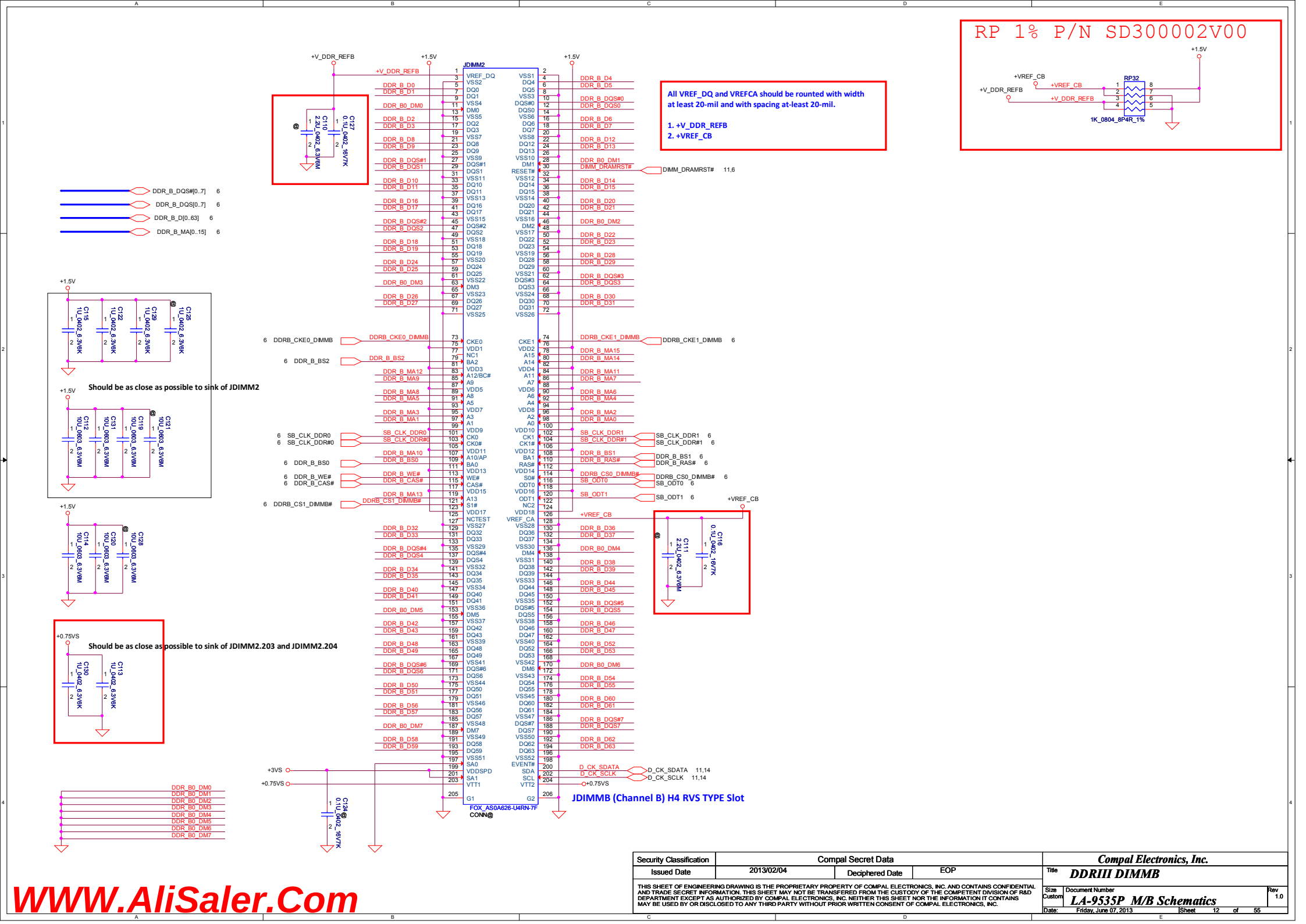
Compal Electronics, Inc.

Title: DDRIII DIMMA

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

Date: Friday, June 07, 2013 | Sheet 11 of 55



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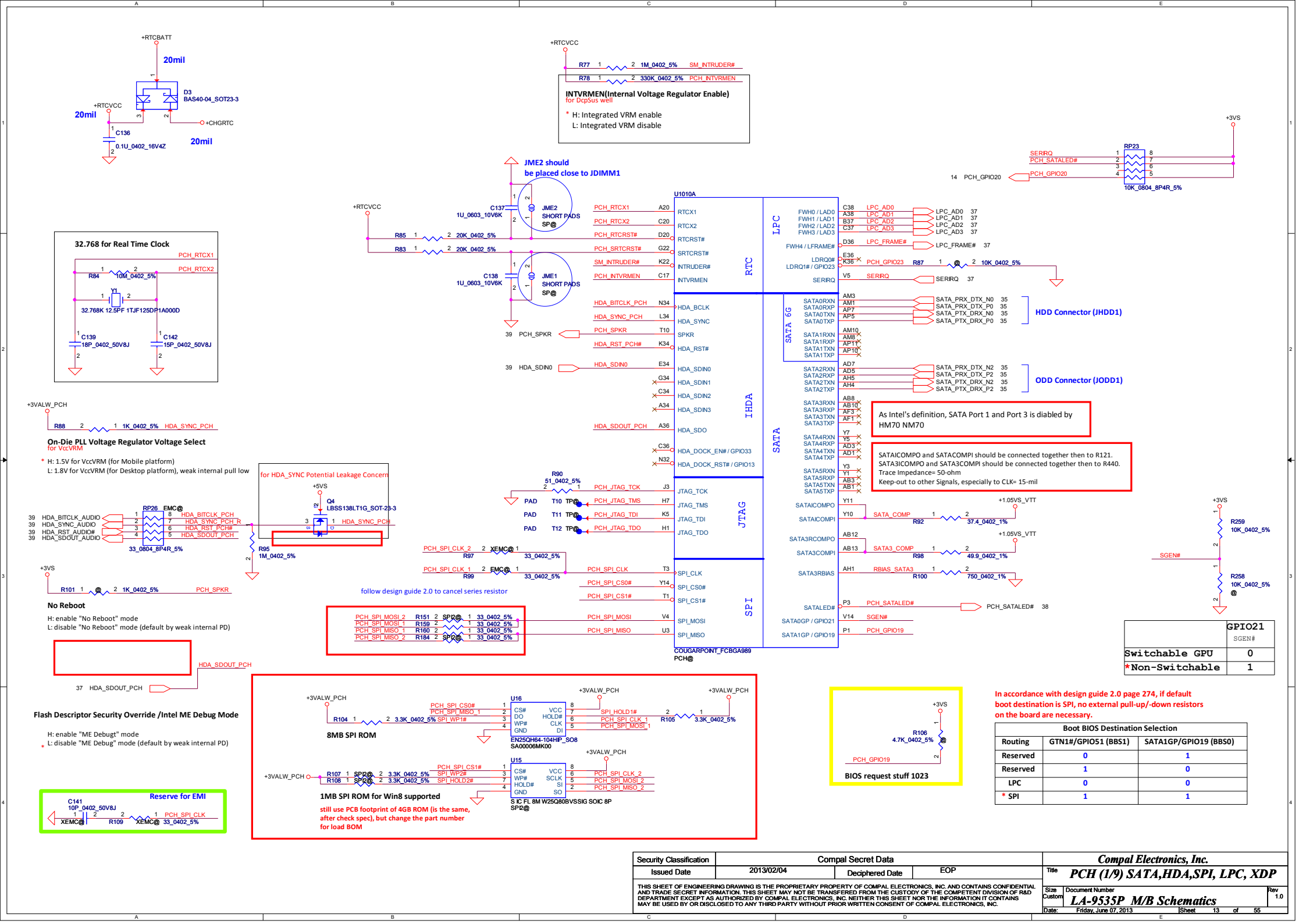
Compal Electronics, Inc.

Title: DDRIII DIMMB

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

Date: Friday, June 07, 2013 | Sheet 12 of 55



	GPIO21 SGEN#
Switchable GPU	0
*Non-Switchable	1

Boot BIOS Destination Selection		
Routing	GTN1#/GPIO51 (BBS1)	SATA1GP/GPIO19 (BBS0)
Reserved	0	1
Reserved	1	0
LPC	0	0
* SPI	1	1

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.			
Title	PCH (1/9) SATA,HDA,SPI, LPC, XDP		
Size: Custom	Document Number: LA-9535P M/B Schematics		Rev: 1.0
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PCIE LAN

WLAN

PCIe Port[8:5] is not supported by HM70 NM70

U1010B

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

COUGARPOINT_FCBGA989

PCH@

Directly to WLAN on JMINI1

for S3 Power Reduction

for CPU eDP

No use, pull-up with 10K to +3VALW_PCH

No use, pull-up with 10K to +3VS

for WLAN(JMIN1)

for 10/100 LAN

Can depop by bios set to GPO

DRAM on Slot

1. Thermal Sensor for VGA
2. EC

NOT used in Full Clock Integration mode

CLKIN_GND1_P (BG30) and CLKIN_GND1_N (BJ30) can share the same PD resistor. <Design Guide 2.0 Page 395>

Reserved for EMI, need to place as close as possible to PCH ball.

Need to inform BIOS team to configure it, follow ME FW Bring Up Guide.

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

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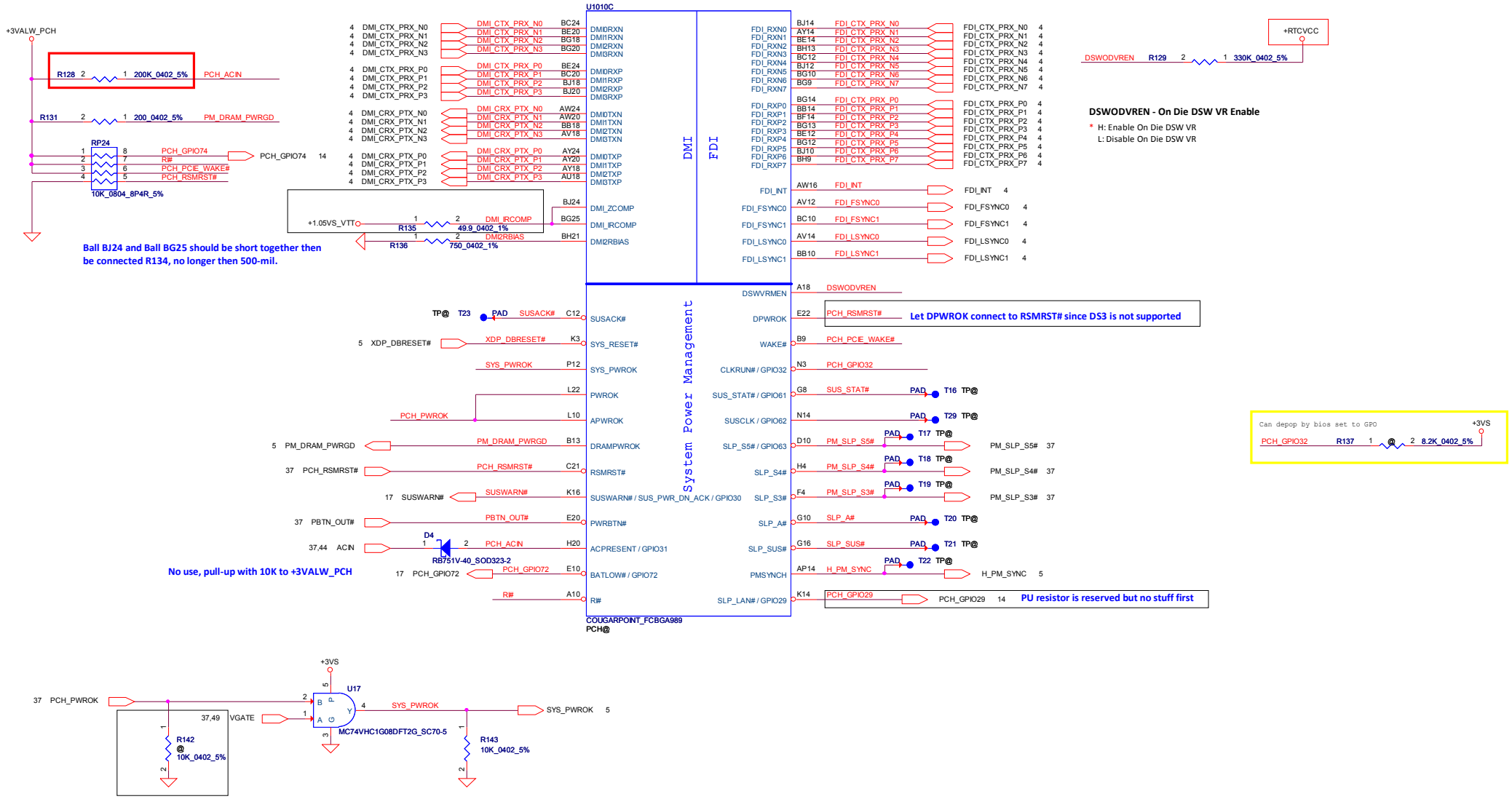
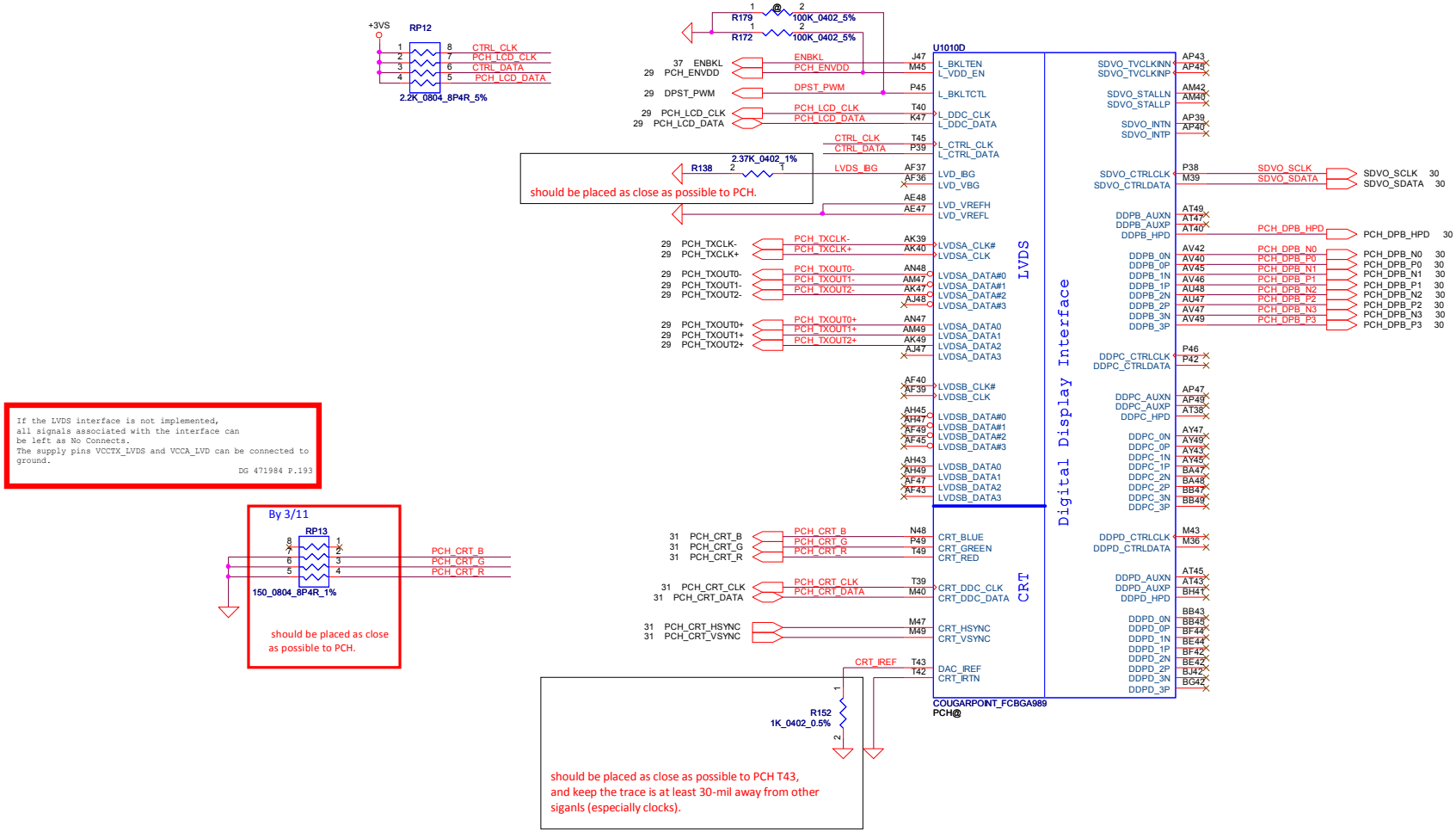
Date: Friday, June 07, 2013 | Sheet 14 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.			
Title	PCH (3/9) DMI,FDI,PM		
Size: Custom	Document Number: LA-9535P M/B Schematics		Rev: 1.0
Date: Friday, June 07, 2013	Sheet 15 of 55		



Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
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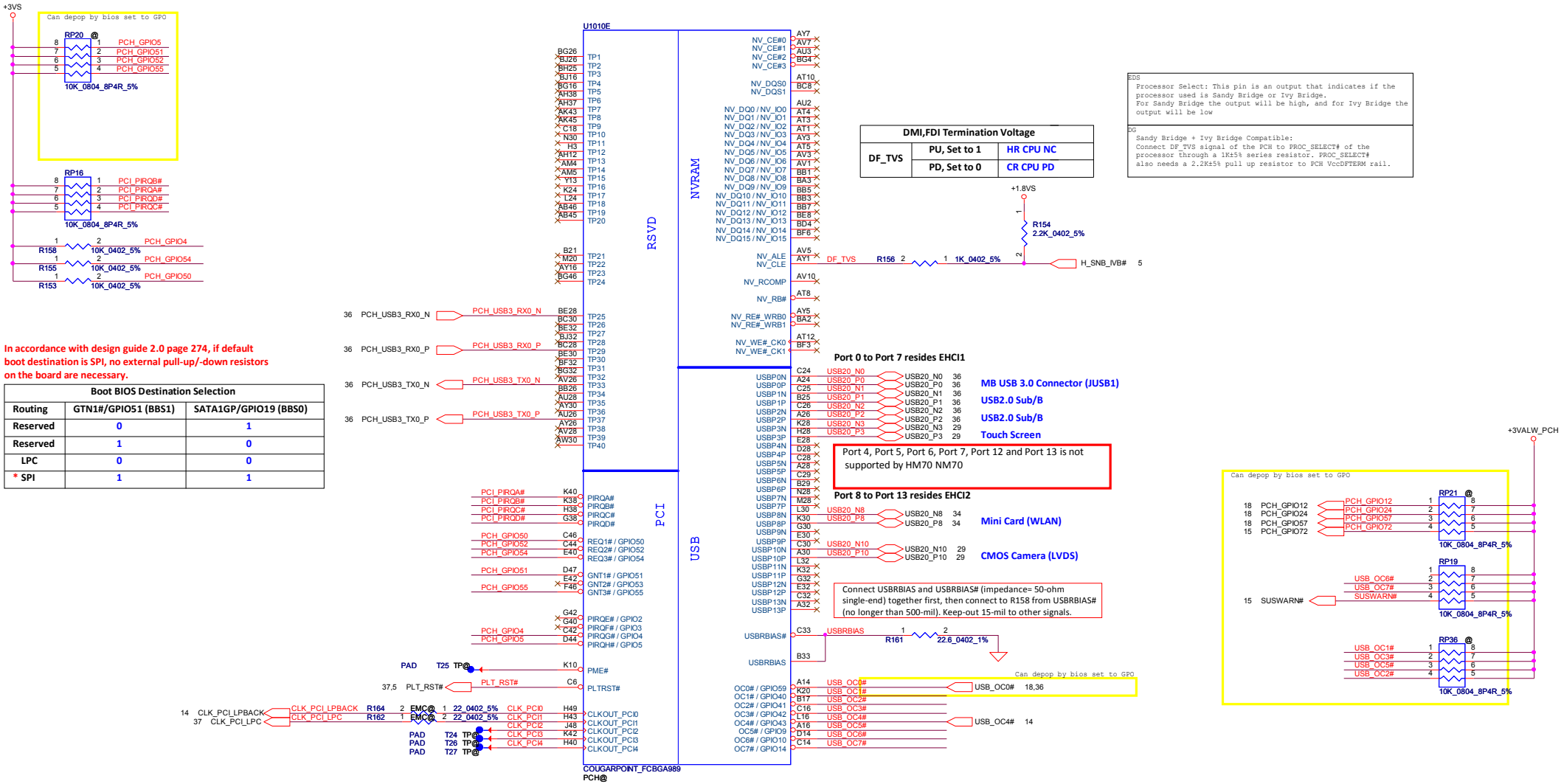

	HM77	HM70	NM70	Note
USB2.0	14	8	8	HM70/NM70 USB port 4, 5, 6,7,12 and 13 are disabled on 8 port SKUs.
USB3.0	4	2	0	USB 3.0 port 3 and 4 are disabled on HM70 USB 3.0 are all disabled on NM70
PCIE	8	4	4	HM70/NM70 PCIe port 5–8 are disabled on this SKU.
SATA	6	4	4	HM70/NM70 SATA port 1 and 3 are disabled on 4 port SKUs. HM70/NM70 SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s & 1.5 Gb/s HM77 SATA 6 Gb/s support on port 0 & port 1. SATA port 0 and 1 also support 3 Gb/s & 1.5 Gb/s.

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.	
Title	PCH (5/9) PCI, USB, NVRAM
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On-Die PLL Voltage Regulator
for VccVRM

* H: enable On-Die PLL Voltage Regulator
L: disable On-Die PLL Voltage Regulator

+3VALW_PCH — R168 4.7K_0402_5% — PCH_GPIO28

For common BIOS code

+3VS — R174 10K_0402_5% @ — PCH_GPIO68 — R178 10K_0402_5%
+3VS — R166 10K_0402_5% @ — PCH_GPIO69 — R169 10K_0402_5%
+3VS — R167 10K_0402_5% @ — PCH_GPIO70 — R170 10K_0402_5%

Project ID	GPIO68	GPIO69	GPIO70
Q5WE0	1	0	0
Q7YE0	1	0	1
Q5Wxx-QC	1	1	0
V5VT1	1	1	1
*Z5WE1_CR	0	0	0

+3VALW_PCH — R171 10K_0402_5% @ — R173 10K_0402_5% @ — PCH_GPIO27

+3VS — R175 10K_0402_5% EC_KBRST# — R180 10K_0402_5% PCH_GPIO1 — R182 10K_0402_5% EC_SC# — R183 10K_0402_5% PCH_GPIO16

U1010F

No use, pull-up with 10K to +3VS — PCH_GPIO0 — T7 — BMBUSY# / GPIO0
No use, pull-up with 10K to +3VS — PCH_GPIO1 — A42 — TACH1 / GPIO1
No use, pull-up with 10K to +3VS — PCH_GPIO6 — H36 — TACH2 / GPIO6
37 EC_SC# — EC_SC# — E38 — TACH3 / GPIO7
37 EC_SMI# — EC_SMI# — C10 — GPIO8
No use, pull-up with 10K to +3VALW_PCH — 17 PCH_GPIO12 — PCH_GPIO12 — C4 — LAN_PHY_PWR_CTRL / GPIO12
37 EC_LID_OUT# — EC_LID_OUT# — G2 — GPIO15
No use, pull-up with 10K to +3VS — PCH_GPIO16 — U2 — SATA4GP / GPIO16
37,50 VGA_PWROK — R110 1 @ 2 0_0402_5% — D40 — TACH0 / GPIO17
On Board DRAM Flag — PCH_GPIO22 — T5 — SCLOCK / GPIO22
No use, pull-up with 10K to +3VALW_PCH — 17 PCH_GPIO24 — PCH_GPIO24 — E8 — GPIO24 / MEM_LED
PCH_GPIO27 — E16 — GPIO27
PCH_GPIO28 — P8 — GPIO28
T40 TP@ — PAD — K1 — STP_PCI# / GPIO34
T30 TP@ — PAD — K4 — GPIO35
T43 TP@ — PAD — V8 — SATA2GP / GPIO36
T44 TP@ — PAD — M5 — SATA3GP / GPIO37
OPTIMUS_EN# — N2 — SLOAD / GPIO38
On Board DRAM Flag — PCH_GPIO39 — M3 — SDATAOUT0 / GPIO39
On Board DRAM Flag — PCH_GPIO48 — V13 — SDATAOUT1 / GPIO48
T45 TP@ — PAD — V3 — SATA5GP / GPIO49
No use, pull-up with 10K to +3VALW_PCH — 17 PCH_GPIO57 — PCH_GPIO57 — D6 — GPIO57

GPIO

TACH4 / GPIO68 — C40 — PCH_GPIO68
TACH5 / GPIO69 — B41 — PCH_GPIO69
TACH6 / GPIO70 — C41 — PCH_GPIO70
TACH7 / GPIO71 — A40 — PCH_GPIO71 — 29 For eDP/LVDS detect

CPU/MISC

A20GATE — P4 — R177 2 10K_0402_5% +3VS — TP@ T42 PAD — GATEA20 37
PECI — AU16
RCIN# — P5 — EC_KBRST# — EC_KBRST# 37 — Ctrl+Alt+Del
PROCPWRGD — AY11 — H_CPUPWRGD 5
THRMTRIP# — AY10 — PCH_THRMTRIP#_R R181 390_0402_5% — H_THRMTRIP# — H_THRMTRIP# 5
INIT3_3V# — T14

NC_1 — AH8
NC_2 — AK11
NC_3 — AH10
NC_4 — AK10
NC_5 — P37

NCTF

VSS_NCTF_1 — A4
VSS_NCTF_2 — A44
VSS_NCTF_3 — A45
VSS_NCTF_4 — A46
VSS_NCTF_5 — A5
VSS_NCTF_6 — A6
VSS_NCTF_7 — B3
VSS_NCTF_8 — B47
VSS_NCTF_9 — BD1
VSS_NCTF_10 — BD49
VSS_NCTF_11 — BE1
VSS_NCTF_12 — BE49
VSS_NCTF_13 — BF1
VSS_NCTF_14 — BF49
VSS_NCTF_15 — BG2
VSS_NCTF_16 — BG48
VSS_NCTF_17 — BH3
VSS_NCTF_18 — BH47
VSS_NCTF_19 — BJ4
VSS_NCTF_20 — BJ44
VSS_NCTF_21 — BJ45
VSS_NCTF_22 — BJ46
VSS_NCTF_23 — BJ5
VSS_NCTF_24 — BJ6
VSS_NCTF_25 — C2
VSS_NCTF_26 — C48
VSS_NCTF_27 — D1
VSS_NCTF_28 — D49
VSS_NCTF_29 — E1
VSS_NCTF_30 — E49
VSS_NCTF_31 — F1
VSS_NCTF_32 — F49

COUGARPOINT_FCBGA989
PCH@

+3VALW_PCH
R186 1K_0402_5% EC_SM#
use pull up to +3V LAN — R188 @ 10K_0402_5% LAN_CLKREQ# — LAN_CLKREQ# 14,32
R187 1K_0402_5% EC_LID_OUT#
RP29 10K_0804_8P4R_5%
PCH_GPIO26 — PCH_GPIO26 14
USB_OC0# — USB_OC0# 17,36
SMB_ALERT# — SMB_ALERT# 14

in accordance with Chief River check list 1.7, when Unused as GPIO or SATA*GP Use 8.2K-10K pull-down to ground

+3VS — R623 10K_0402_5% OPTIMUS_EN#
R639 VGA@ 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
DIS Only	1

Can depop by bios set to GPO

PCH_GPIO48 — RP35 @ — +3VS
PCH_GPIO0
PCH_GPIO22
PCH_GPIO39
10K_0804_8P4R_5%

PCH_GPIO6 — R185 @ 10K_0402_5% — +3VS

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Compal Electronics, Inc.
Title: PCH (6/9) GPIO, CPU, MISC
Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0
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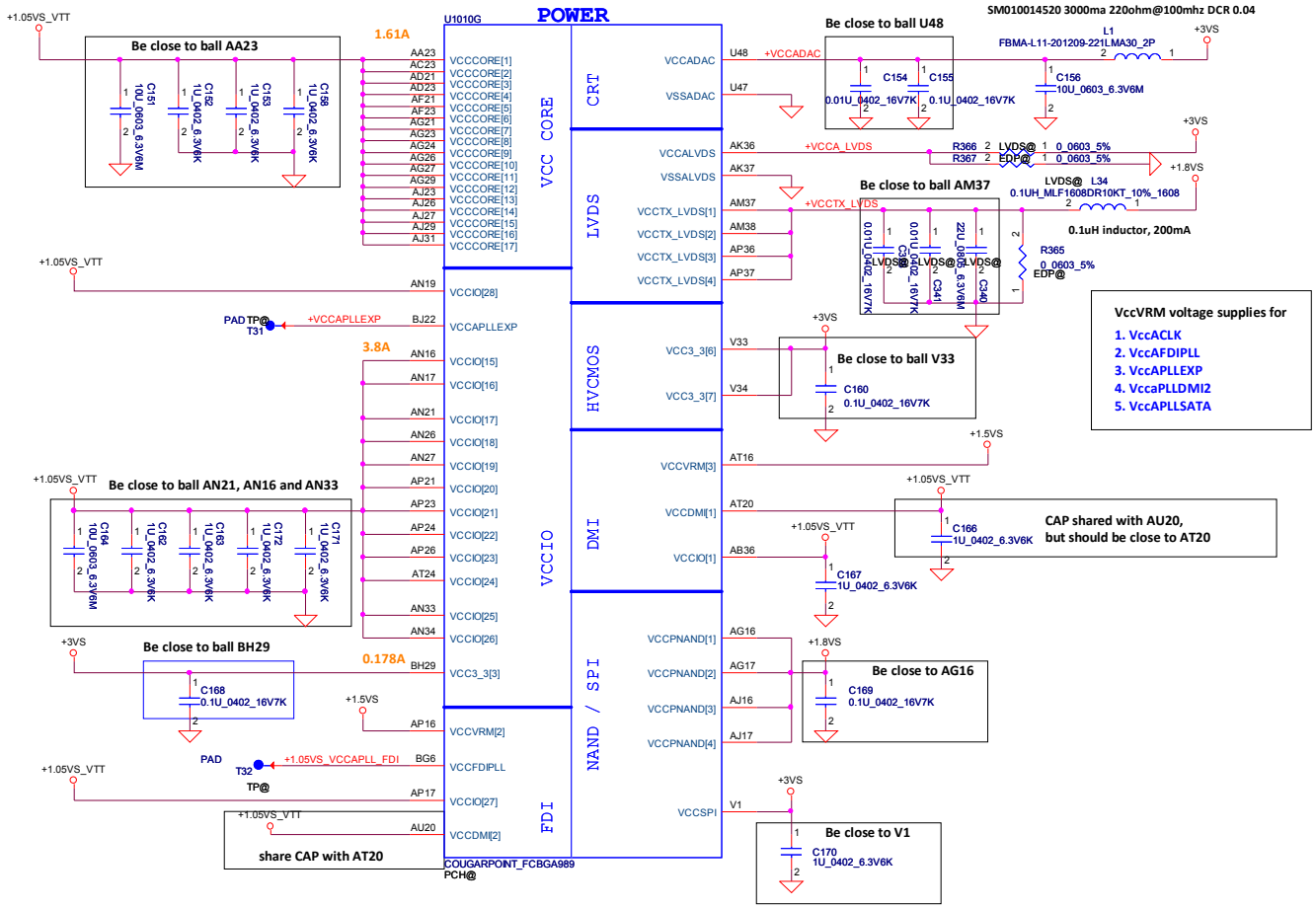

Refer to IntelR 7 Series / C216 Chipset Family Platform Controller Hub (PCH) External Design Specification (EDS) Revision 2.1

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.002	Processor I/O
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.178	I/O Buffer Voltage
VccADAC	3.3	0.063	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.075	Display PLL A power
VccADPLLB	1.05	0.075	Display PLL B power
VccCore	1.05	1.73	Internal Logic Voltage
VccDMI	1.05	0.047	DMI Voltage
VccIO	1.05	3.799	Core Well I/O buffers
VccASW	1.05	0.803	1.05 V Supply for Intel Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW3_3	3.3	0.001	3.3v supply for Deep Sx well
VccDFTERN (VccPNAND)	1.8	0.002	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	RTC Battery Voltage
VccSus3_3	3.3	0.065	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.5	0.147	1.5 V Internal PLL and VRMs
VccCLKDMI	1.05	0.075	DMI differential Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.05	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.04	I/O power supply for LVDS (Mobile Only)

Compal Electronics, Inc.

Title: PCH (7/9) PWR

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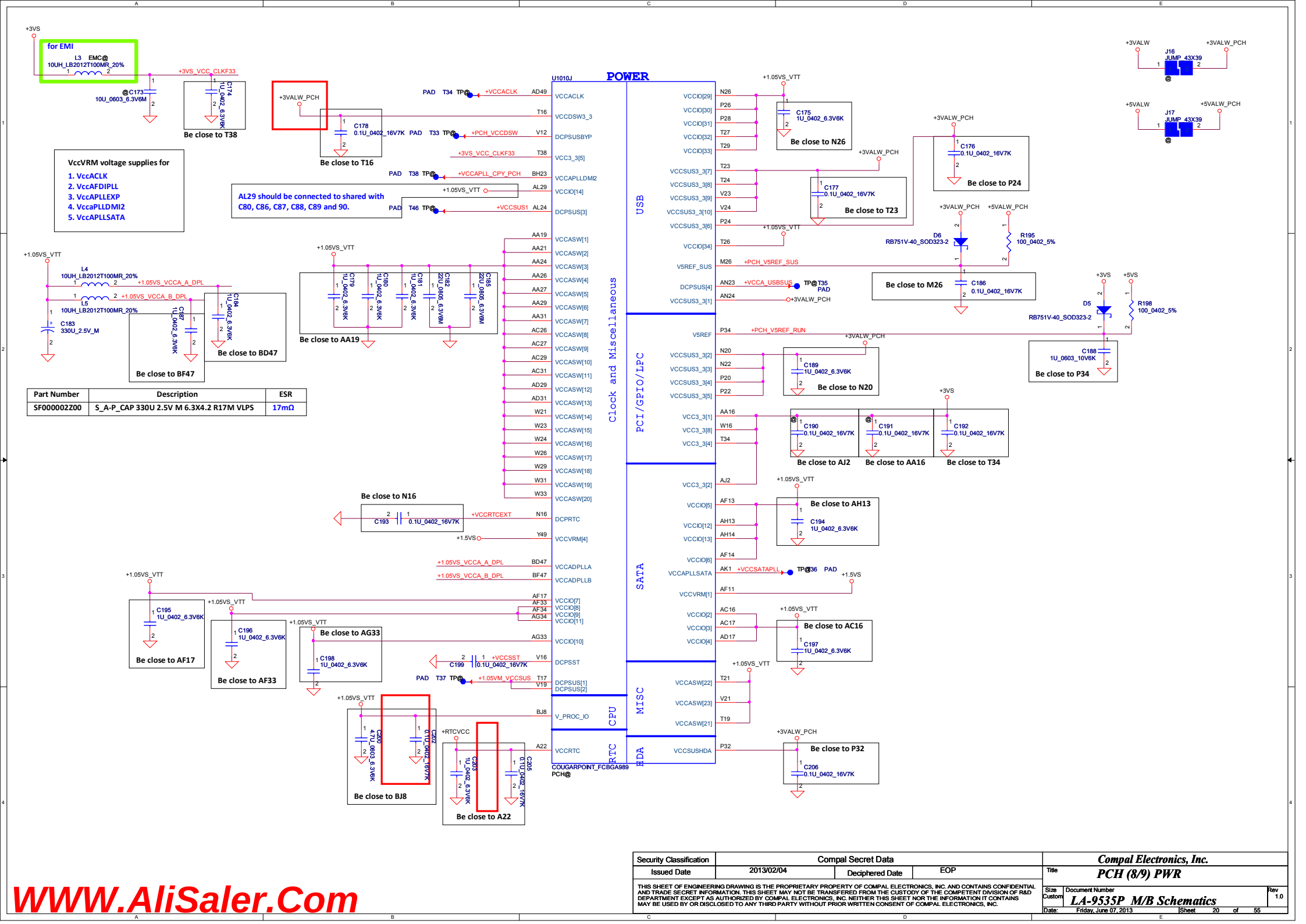

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Title: PCH (8/9) PWR

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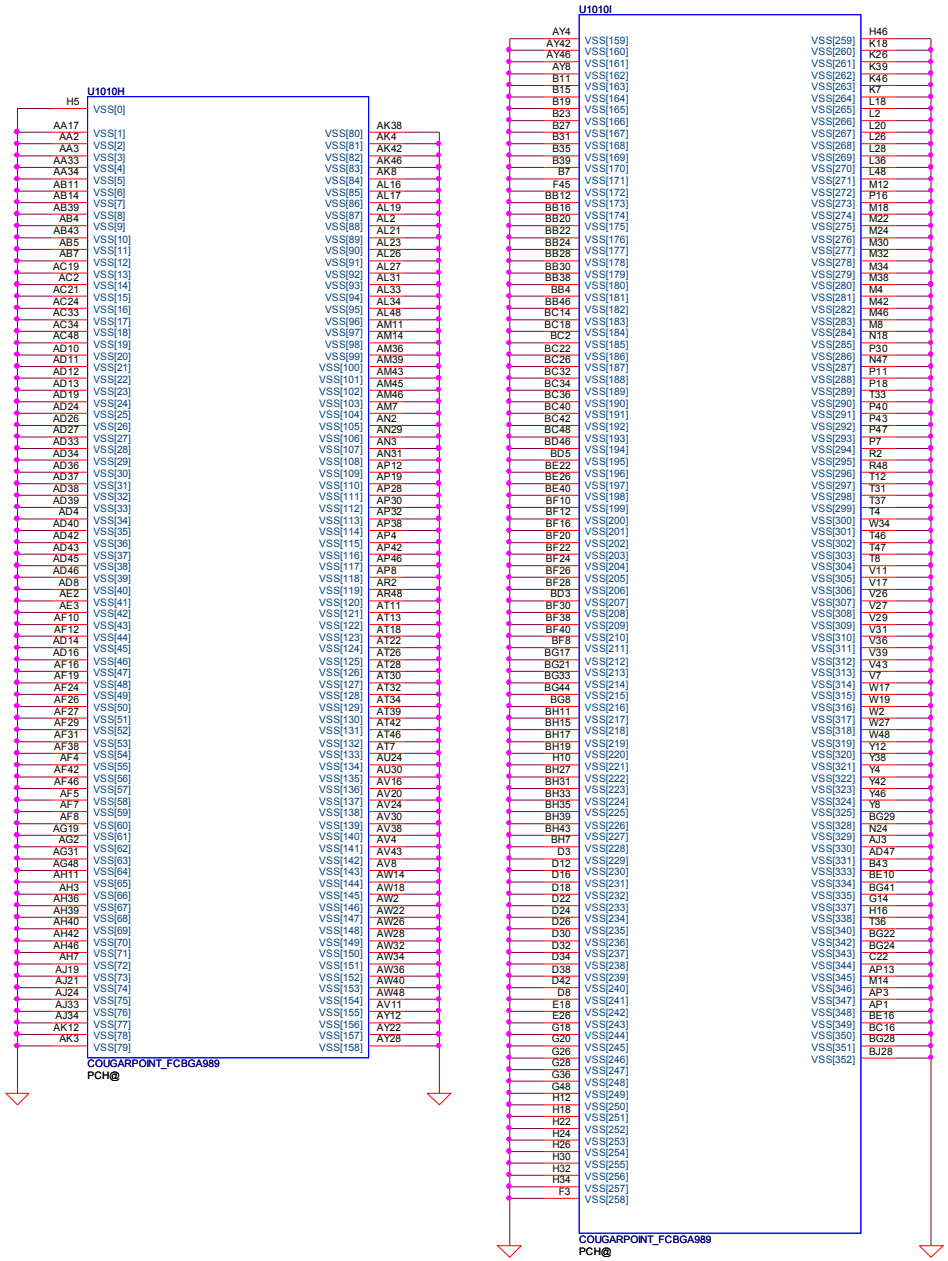

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Compal Electronics, Inc.		
Title: PCH (9/9) VSS		
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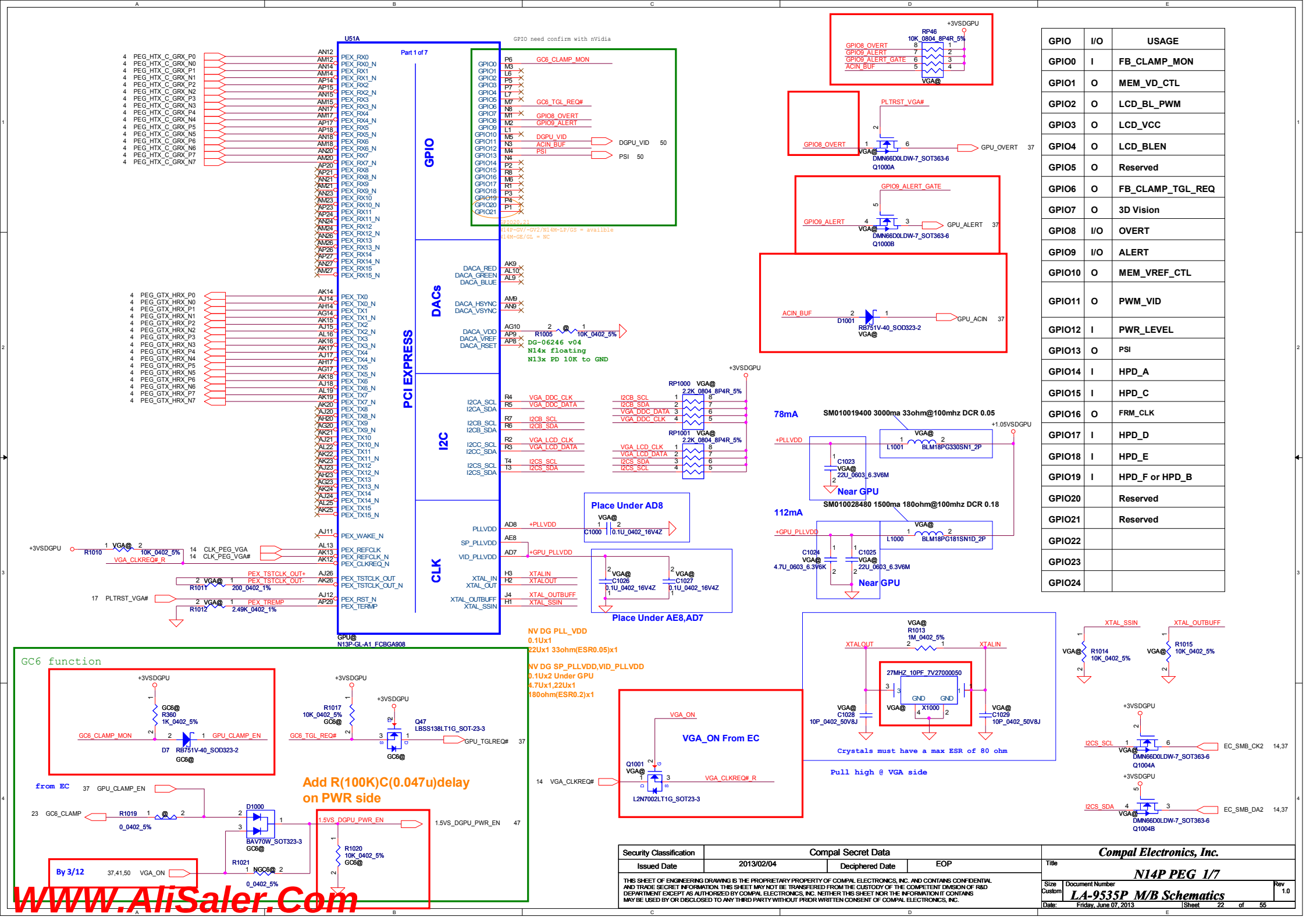

GPIO	I/O	USAGE
GPIO0	I	FB_CLAMP_MON
GPIO1	O	MEM_VD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	Reserved
GPIO6	O	FB_CLAMP_TGL_REQ
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	O	FRM_CLK
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21		Reserved
GPIO22		
GPIO23		
GPIO24		

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: N14P PEG 1/7

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

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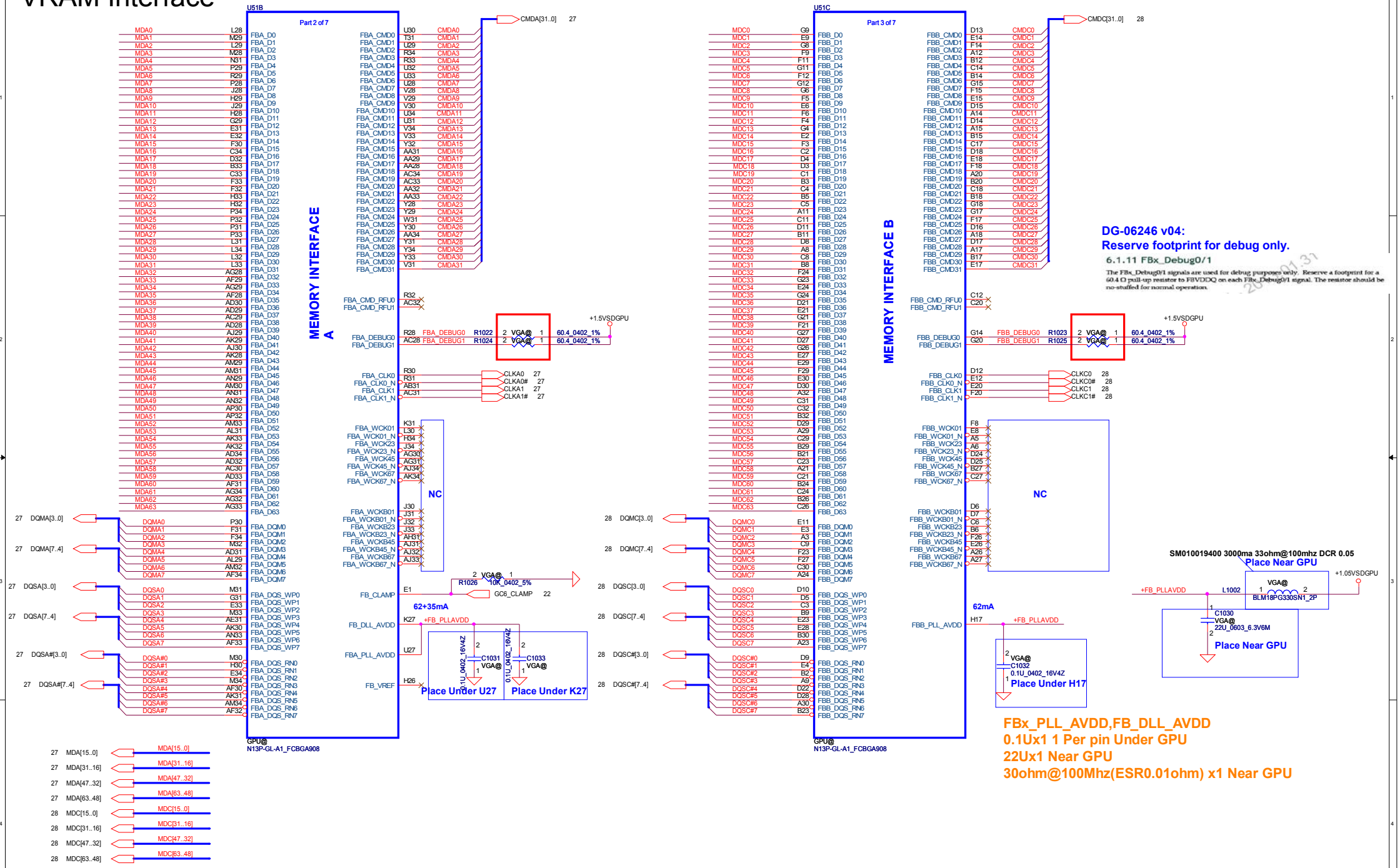
VRAM Interface



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Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.			
Title	N14P VRAM 2/7		
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U51D

Part 4 of 7

LVDS/TMDS

NC

TEST

SERIAL

GENERAL

GPU@
N13P-GL-A1_FCBGA908

U51 N14P-GV2-A1 N14PGV2@ SA00006B530 R3

U51 N14P-GT-A2 N14PGT@ SA00005W200 R1

U51 N14M-GE-A2 N14MGE@ SA000068A10 R3

MULTI LEVEL STRAPS

Straps

+3VSDGPU

N14P-GV2/GT VRAM Strap

+3VSDGPU

ZZZ X76M1G@ N14M-GE 1G MB X76 X76402BOL11|X76402BOL12
N14M-GE 1G VRAM X76

ZZZ X76M2G@ N14M-GE 2G MB X76 X76402BOL13
N14M-GE 2G VRAM X76

ZZZ X76P2G@ N14P-GV2 2G MB X76 X76402BOL14|X76402BOL15
N14P-GV2 VRAM X76

N14P-GV2 VRAM Strap R1041 15K_0402_1% P2GAFR@ R1041 10K_0402_1% P2GMCN@

For N14P-GV2 strap table Decive ID : 0x1292

For N14P-GT strap table Decive ID : 0xFE4

GPU	Freq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GV2	900 MHZ 900 MHZ	128M *16* 4 1GB 128M *16* 4 1GB	0x4: HYNIX SA00006H430 R3 H5TC2G63FFR-11C 0x6: HYNIX SA00003YO90 R3 H5TQ2G63DFR-11C	R PU 45.3K	R PD 34.8K	R PD 15K	R PD 4.99K	R PD 20K	PD 34.8K PD 24.9K	R PU 4.99K	R PU 4.99K
	900 MHZ 900 MHZ	256M *16* 4 2GB 256M *16* 4 2GB	0x1: MICRON SA000065D10 R3 MT41K256M16HA-107G:E 0x2: HYNIX SA00006E840 R3 H5TC4G63AFR-11C			PD 10K PD 15K			PD 10K PD 15K		
N14P-GT	900 MHZ 900 MHZ	128M *16* 4 1GB 256M *16* 4 2GB	Hynix SA00003YO90 Micron SA000065D10			R PD 24.9K			PD 34.8K PH 30.1K		R PD 15K

Resistor Values	Pull-up to +3V	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Strap Name	Bit3	Bit2	Bit1	Bit0
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GNE3	PCIE_MAX_SPEED	DP_PLL_VDD33V

SUB_VENDOR
0:No Video BIOS ROM*
1:BIOS ROM is present

PEX_PLL_EN_TERM
0:Disable*
1:Enable

FB[1:0]
0:Reserved
1:Reserved
2:256MB*
3:Reserved

SMB_ALT_ADDR
0:0x9E(Default)*
1:0x9C(Multi-GPU usage)

VGA_DEVICE
0:3D Device*
1:VGA Device

DP_PLL_VDD33V
0:Reserved
1:Default*

3GIO_PADCFG[3:0]
0110:GEN1/GEN2 support only*
0000:GEN3 support

SOR[3:0]_EXPOSED
Define audio on each digital display port
0000:Not in Use*

PCIE_SPEED_CHANGE_GNE3
0:Disable PCIE Gen3 operation*
0:Enable PCIE Gen3 operation

PCIE_MAX_SPEED
0:Limit booting to PCIE Gen1
1:Allow booting to PCIE Gen2/3*

For N14M-GE Binary strap table Decive ID : 0x1140

GPU	Freq.	Memory Size	Memory Config	strap3	strap2	strap1	strap0	strap4	ROM_SCLK	ROM_SI	ROM_SO
N14M-GE	900MHz	128Mx16x4	0x6: HYNIX SA00003YO90 R3 H5TQ2G63DFR-11C	PD10K	PH10K	PH10K	PD10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
	900MHz	128Mx16x4	0xC: HYNIX SA00006H430 R3 H5TC2G63FFR-11C	PH10K	PD10K	PD10K	PD10K				
	900MHz	256Mx16x4	0xD: MICRON SA000065D10 R3 MT41K256M16HA-107G:E 0x3: HYNIX SA00006DG30 R3 H5TC4G63MFR-11C 0x4: HYNIX SA00006E840 R3 H5TC4G63AFR-11C	PH10K PD10K PD10K	PD10K PH10K PH10K	PD10K PH10K PH10K	PH10K PH10K PD10K				

N14M-GE VRAM Strap

HYNIX 128 H5TQ2G63DFR-11C
0X6 strap3 0 strap2 1 strap1 1 strap0 0
R1029 10K_0402_1% M1GDFR@
R1028 10K_0402_1% M1GDFR@
R1039 10K_0402_1% M1GDFR@
R1036 10K_0402_1% M1GDFR@

HYNIX 128 H5TQ2G63FFR-11C
0XC strap3 1 strap2 1 strap1 0 strap0 0
R1030 10K_0402_1% M1GFFR@
R1029 10K_0402_1% M1GFFR@
R1037 10K_0402_1% M1GFFR@
R1036 10K_0402_1% M1GFFR@

HYNIX 256 H5TQ4G63AFR-11C
0X4 strap3 0 strap2 1 strap1 0 strap0 0
R1029 10K_0402_1% M2GAFR@
R1039 10K_0402_1% M2GAFR@
R1037 10K_0402_1% M2GAFR@
R1036 10K_0402_1% M2GAFR@

MICRON 256 MT41K256M16HA-107G:E
0XD strap3 1 strap2 1 strap1 0 strap0 1
R1030 10K_0402_1% M2GMCN@
R1029 10K_0402_1% M2GMCN@
R1027 10K_0402_1% M2GMCN@
R1037 10K_0402_1% M2GMCN@

HYNIX 256 H5TQ4G63MFR-11C
0X3 strap3 0 strap2 0 strap1 1 strap0 1
R1028 10K_0402_1% M2GMFR@
R1027 10K_0402_1% M2GMFR@
R1039 10K_0402_1% M2GMFR@
R1035 10K_0402_1% M2GMFR@

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M*16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
				MT41J128M16JT-107G:K	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
				K4W2G1646E-BC11	900	1204	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production ready
				H5TQ2G63DFR-11C	900	N/A	Production ready
		0xC	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Post-production candidate

Table 5. N14M-G5/LP and N14P-GV2 DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128M*16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production ready
				K4W2G1646E-BC11	900	1204	Production ready
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production ready
				MT41J128M16JT-107G:K	900	1150	Production ready
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-H0C	1000	N/A	Production ready
				H5TQ2G63DFR-11C	900	N/A	Production ready
		0x4	1.5V/ 1.5V	H5TC2G63FFR-11C	1000	N/A	Production ready

Binary	Hexadecimal	Bom structure
0000	0x0	P2GMCN@
0001	0x1	P2GAFR@
0010	0x2	
0011	0x3	M2GMFR@
0100	0x4	P1GFFR@,M2GAFR@
0101	0x5	
0110	0x6	M1GDFR@,P1GDFR@
0111	0x7	
1000	0x8	
1001	0x9	
1010	0xA	
1011	0xB	
1100	0xC	M1GFFR@
1101	0xD	M2GMCN@
1110	0xE	
1111	0xF	

Table 123 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SUB_VENDOR	10k Ω	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

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Compal Electronics, Inc.

Title: N14P LVDS 3/7

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NV 14x DG FBVDDQ(DDR3) GB4-128
0.1Ux4,1Ux4,4.7Ux4 Under GPU
10Ux2,22Ux2 Near GPU

NV DG PEX_IOVVD/Q combined
1Ux4 Under GPU
4.7Ux2 Near GPU
10Ux4,22Ux4 Midway GPU & Power supply

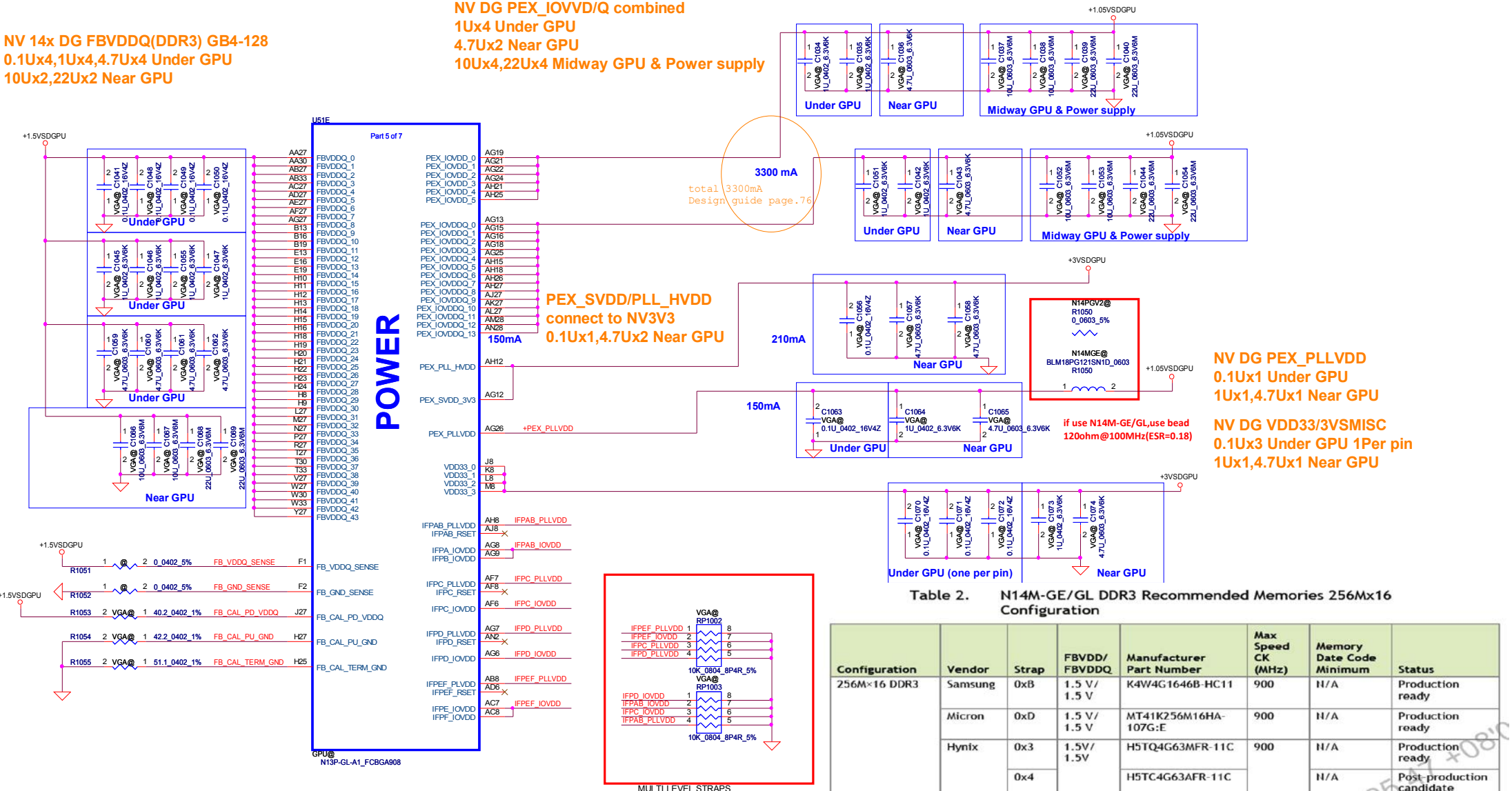

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256M×16 DDR3	Samsung	0xB	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0xD	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x3	1.5V/ 1.5V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4		H5TC4G63AFR-11C		N/A	Post-production candidate

Table 7. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production ready
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production ready
	Hynix	0x2	1.5V/ 1.5V	H5TC4G63AFR-11C	900	N/A	Production ready

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Compal Electronics, Inc.

Title: N14P POWER & GND 4/9

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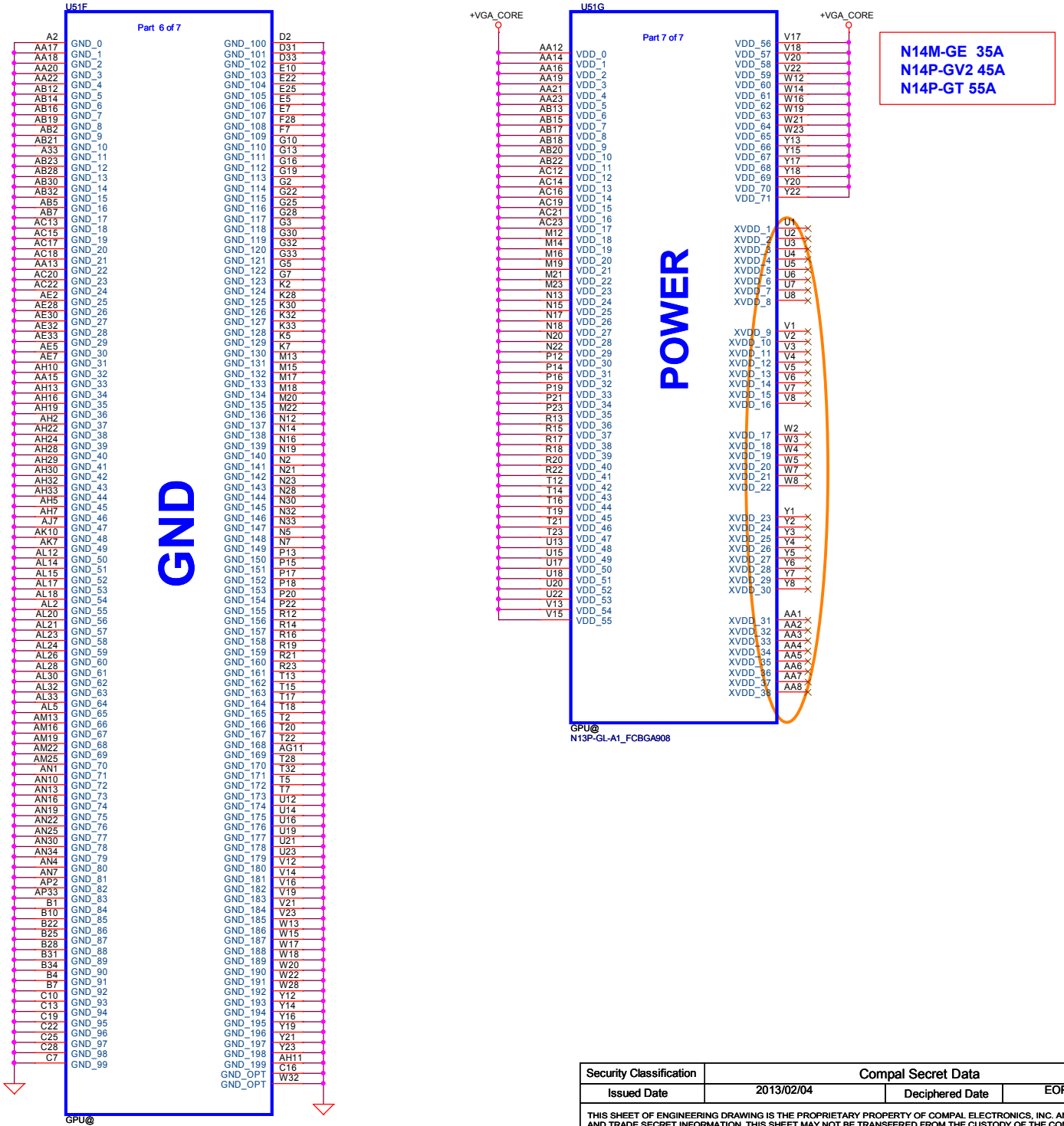

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: N14P POWER & GND 5/7

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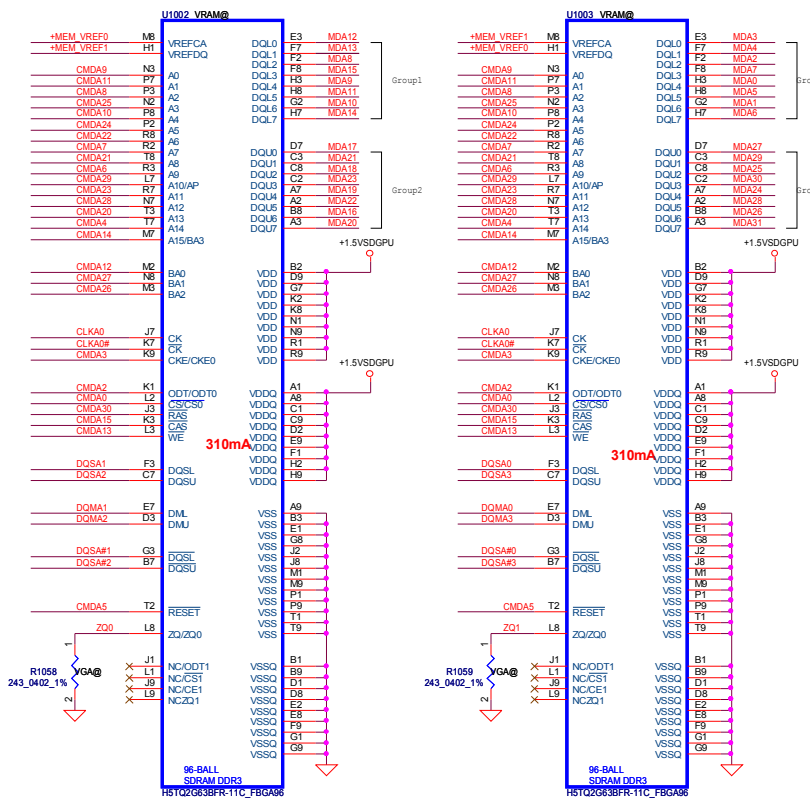
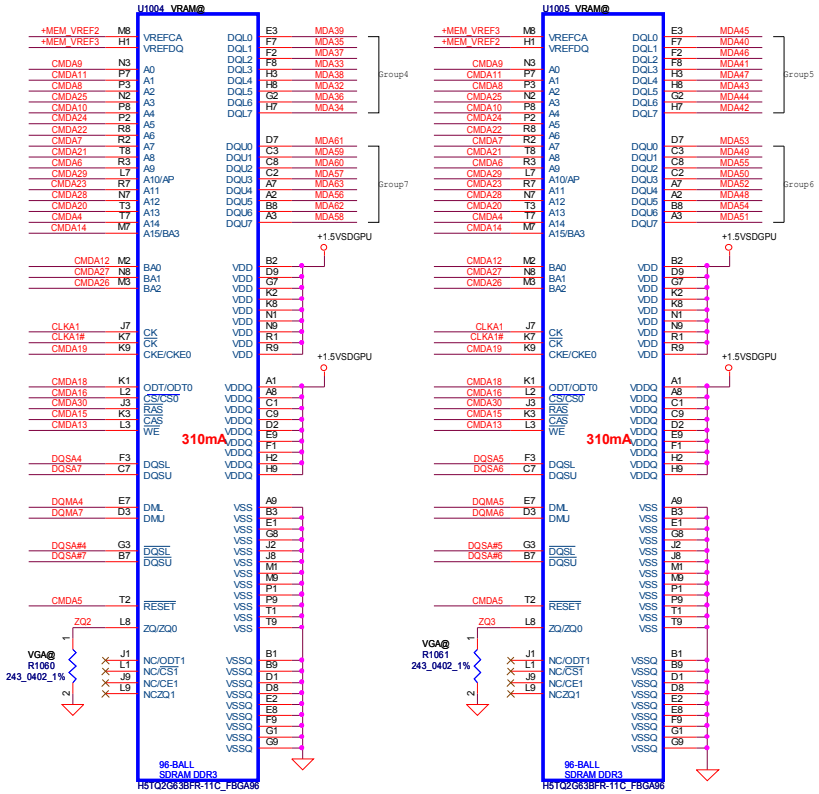
VRAM DDR3 chips

128Mx16 DDR3 *8==>2GB
256Mx16 DDR3 *8==>4GB

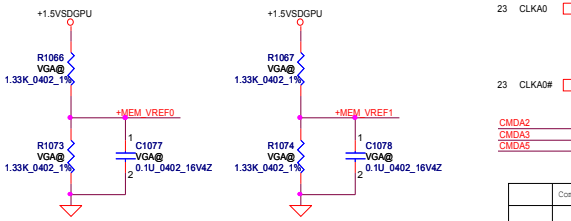
Low 32

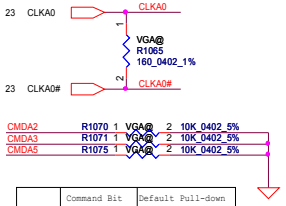
High 32



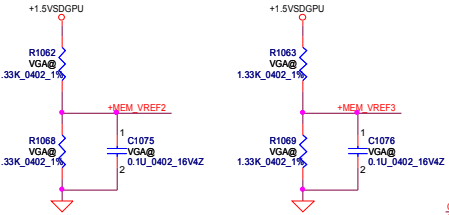


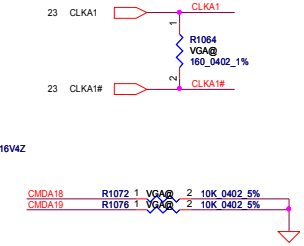
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

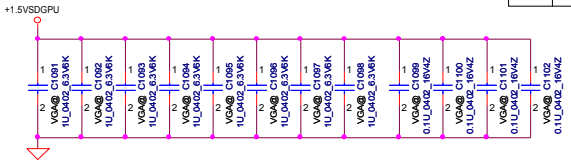


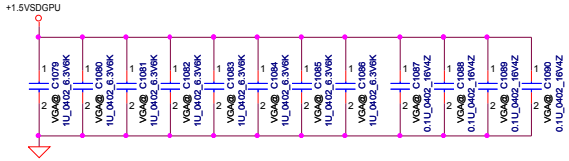


	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination









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Compal Electronics, Inc.

Title: N14P DDR3 6/7

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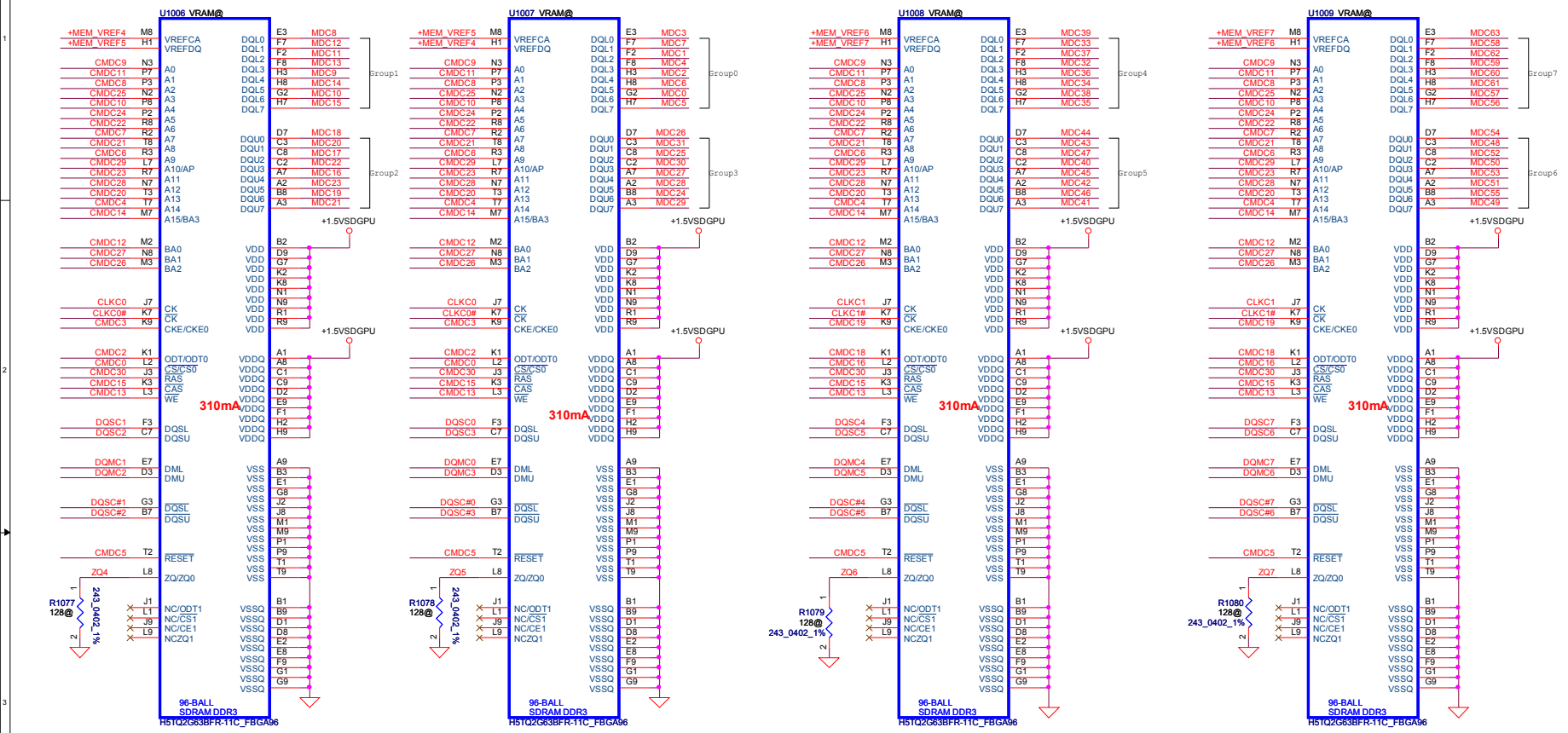
VRAM DDR3 chips

128Mx16 DDR3 *8==>2GB
256Mx16 DDR3 *8==>4GB

23 DQSC[7..0] → DQSC[7..0]
23 DQSC#[7..0] → DQSC#[7..0]
23 DQMC[7..0] → DQMC[7..0]
23 MDC[63..0] → MDC[63..0]
23 CMDC[30..0] → CMDC[30..0]

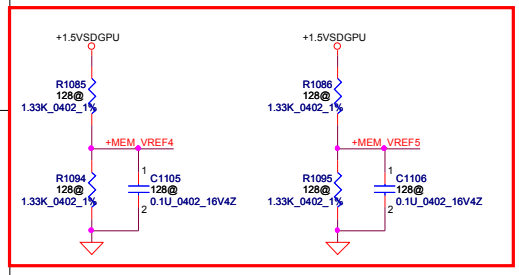
Low 32

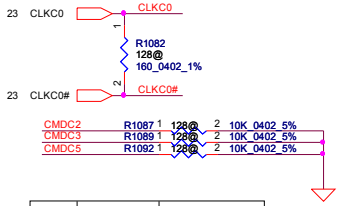
High 32



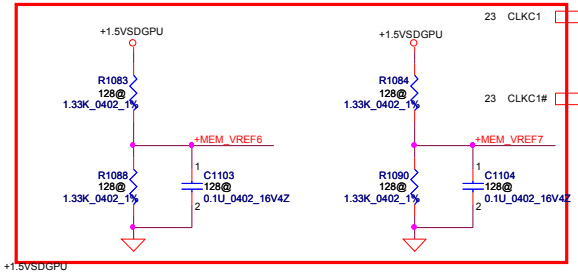
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

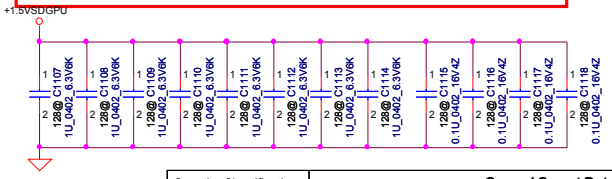
LOW HIGH

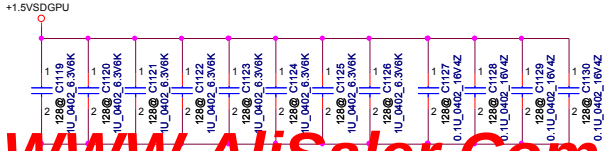




	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination







U1006	SA00003YO90 H5TQ2G63DFR-11C GTHYDFR@	U1006	SA000065D10 MT41K256M16HA GTMTHA@
U1007	SA00003YO90 H5TQ2G63DFR-11C GTHYDFR@	U1007	SA000065D10 MT41K256M16HA GTMTHA@
U1008	SA00003YO90 H5TQ2G63DFR-11C GTHYDFR@	U1008	SA000065D10 MT41K256M16HA GTMTHA@
U1009	SA00003YO90 H5TQ2G63DFR-11C GTHYDFR@	U1009	SA000065D10 MT41K256M16HA GTMTHA@

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Title: N14P DDR3 7/7

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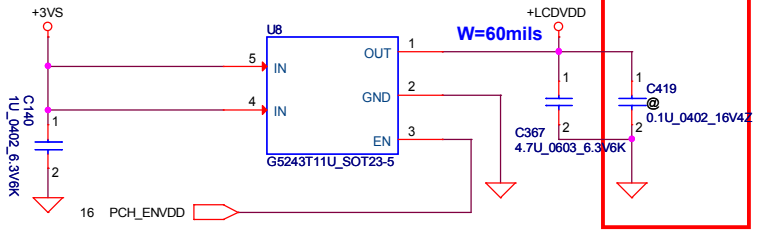
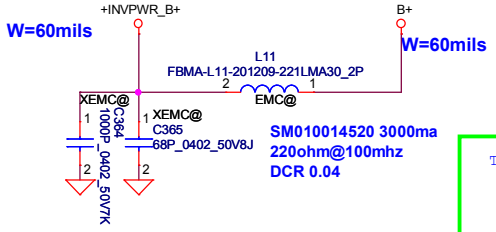
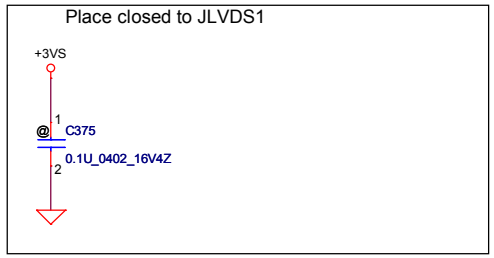
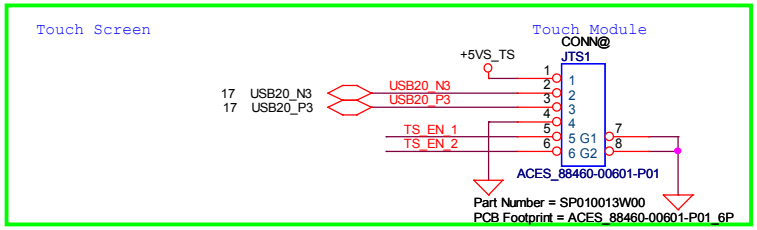
LCD POWER CIRCUIT

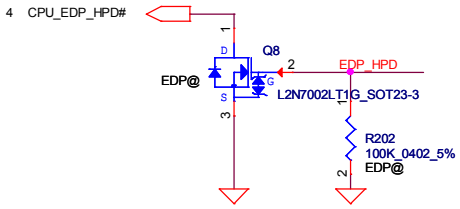


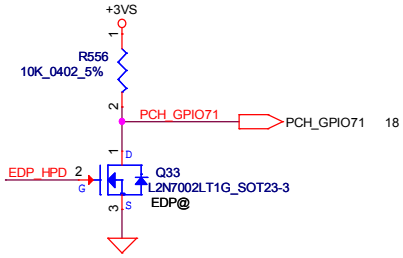






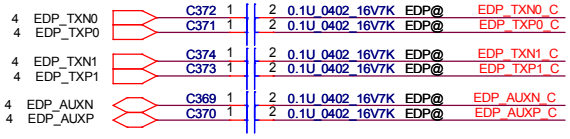
HPD

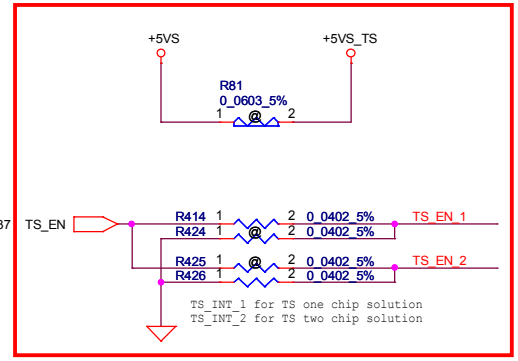




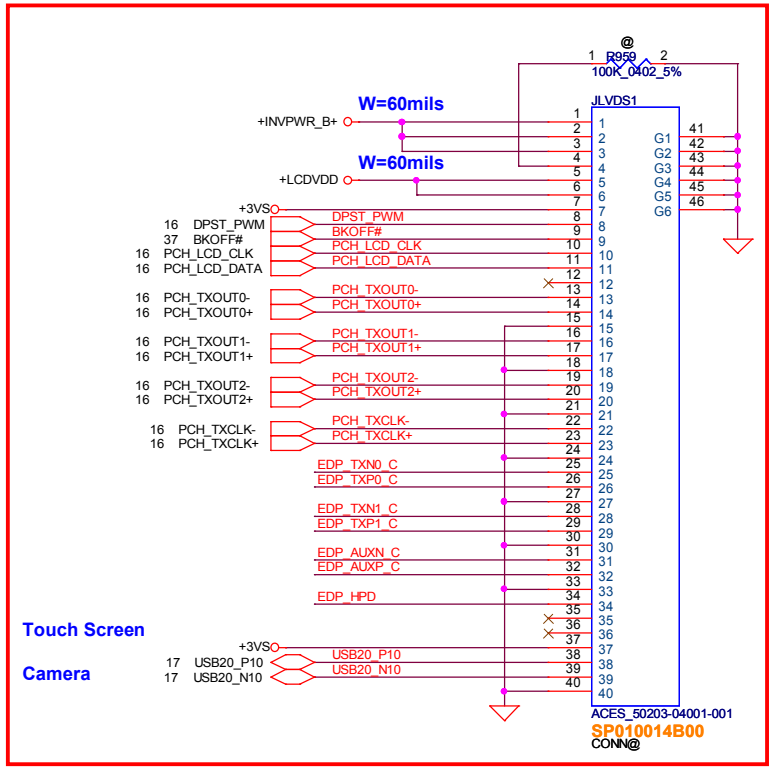
	GPIO71 PCH_GPIO71
eDP	0
LVDS	1

eDP





LCD/ LED PANEL Conn.



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Title: eDP Connector

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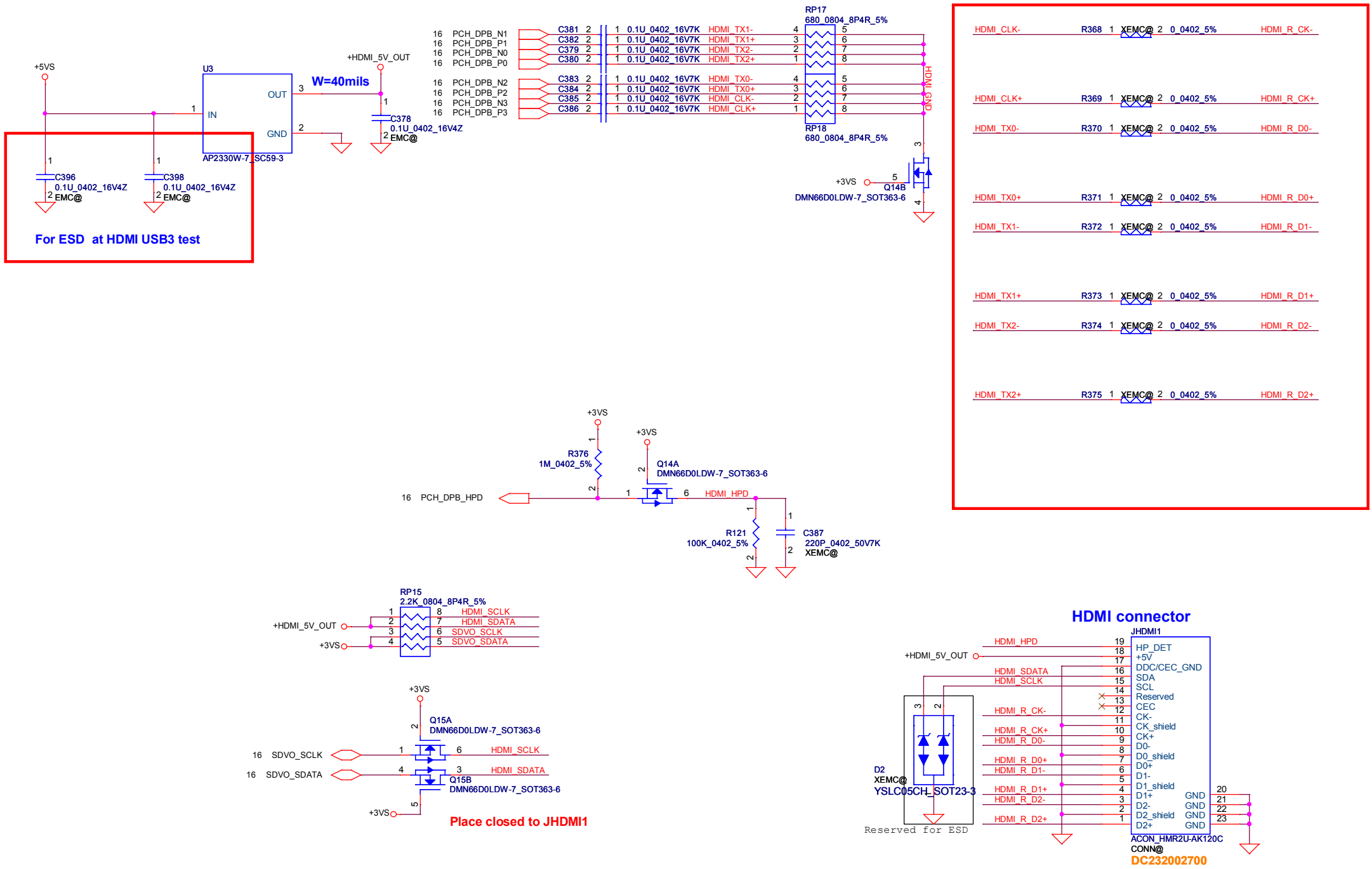

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: HDMI_Conn

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

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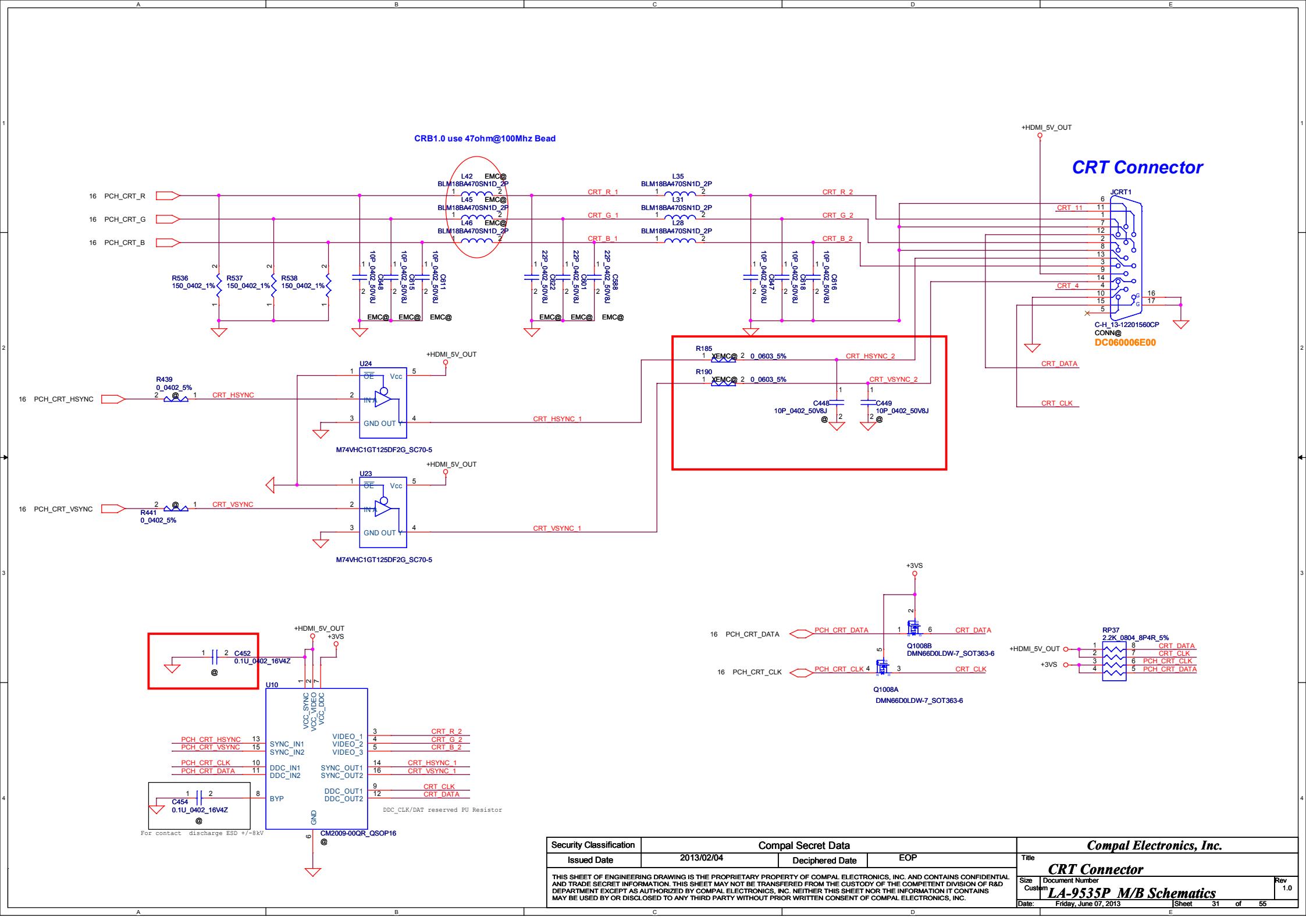

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

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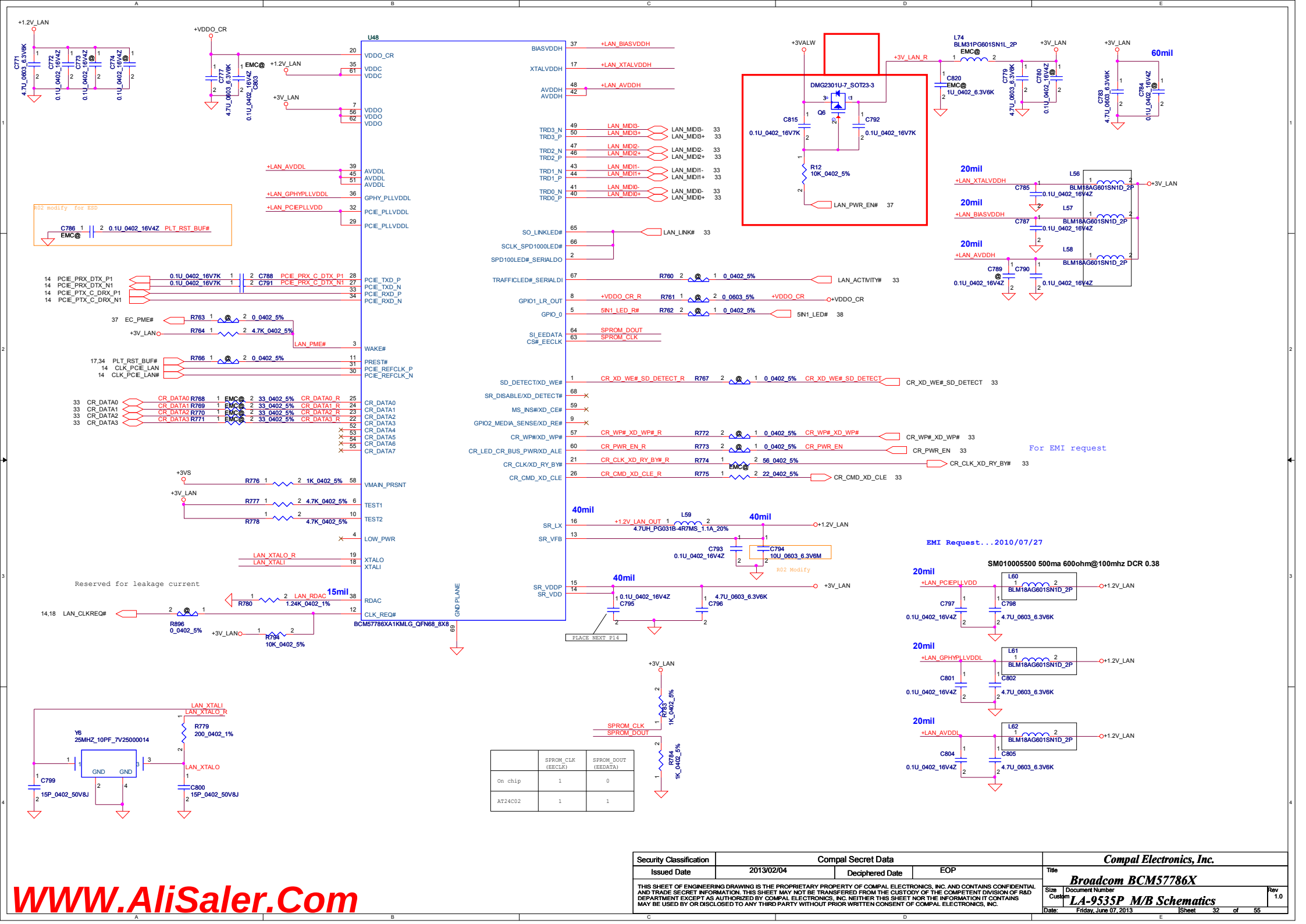

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

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Compal Electronics, Inc.

Title: Broadcom BCM57786X

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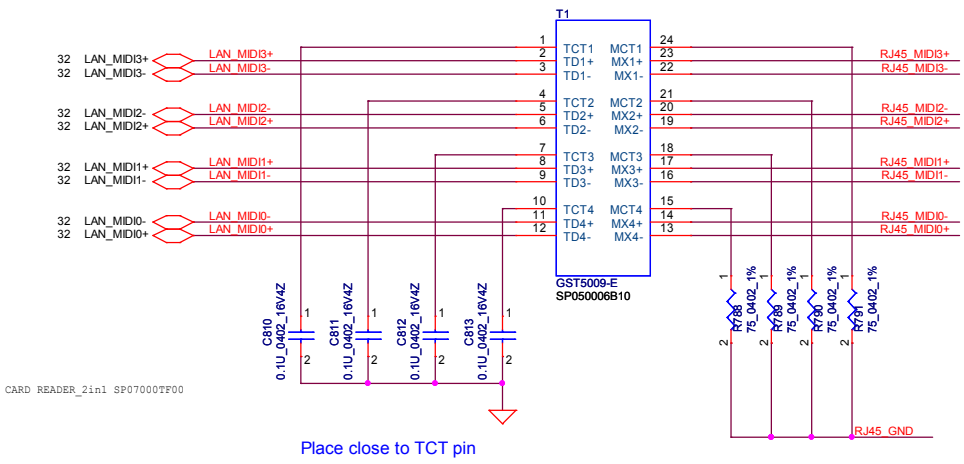
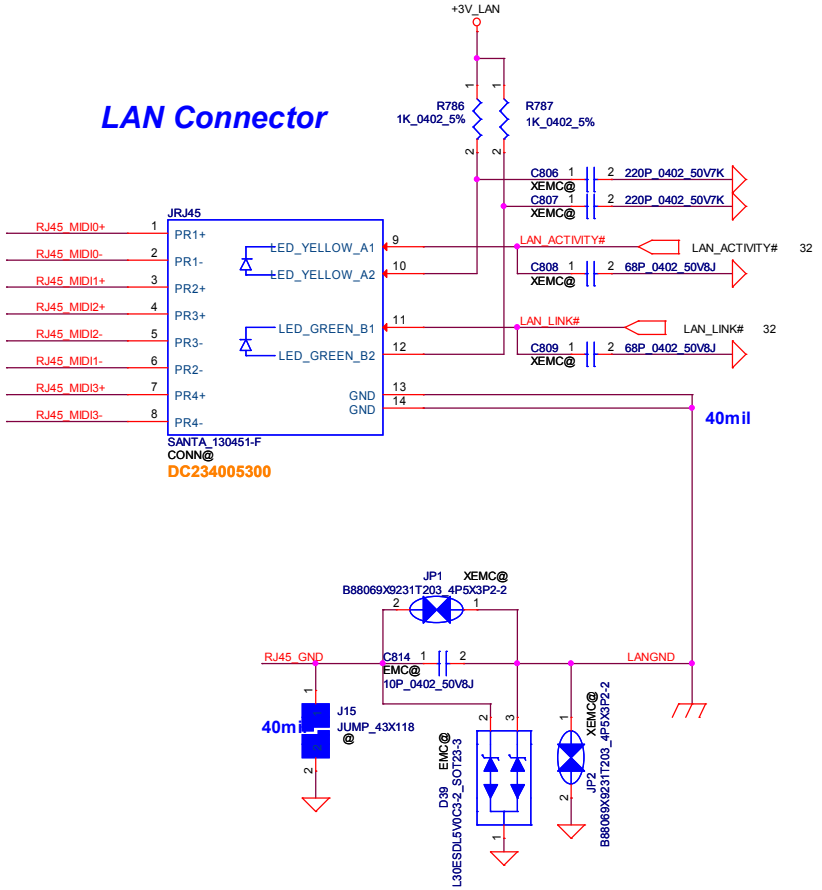


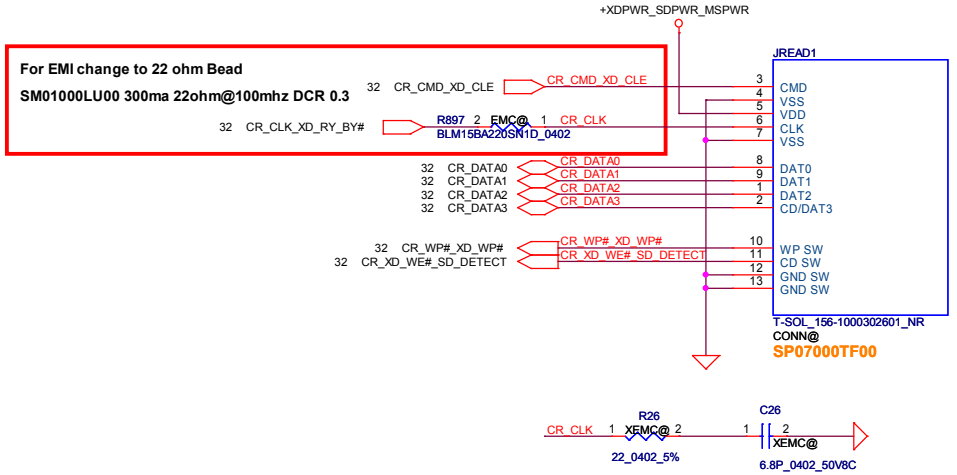
Place close to TCT pin

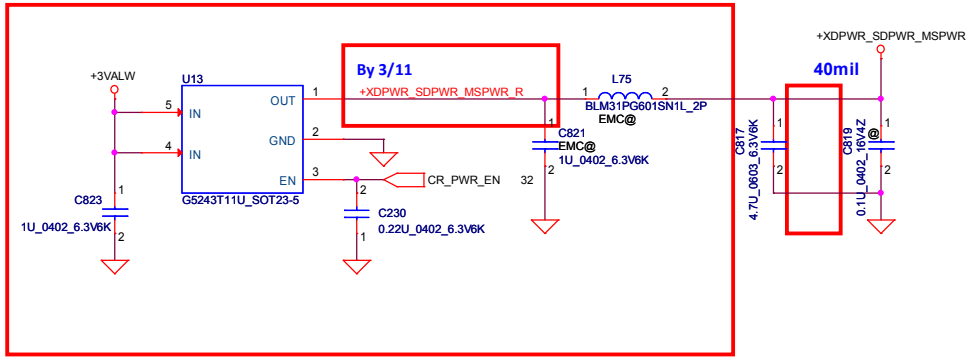
BOTHHAND: S X'FORM_ GST5009-E LF LAN, SP050006B10
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00
FCE:S X'FORM_ NS892407 1G , SP050006800

LAN Connector



Card Reader Connector





Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

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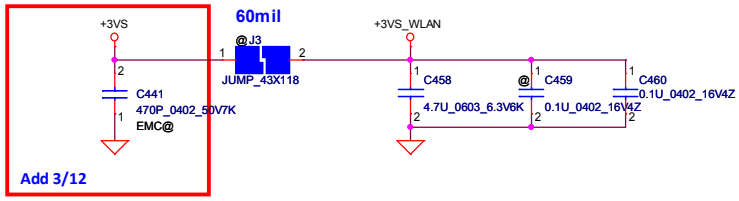
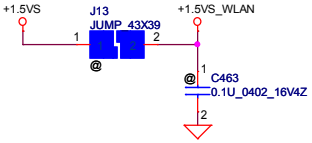
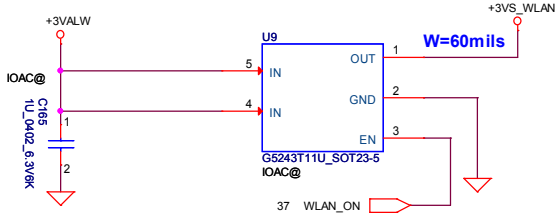
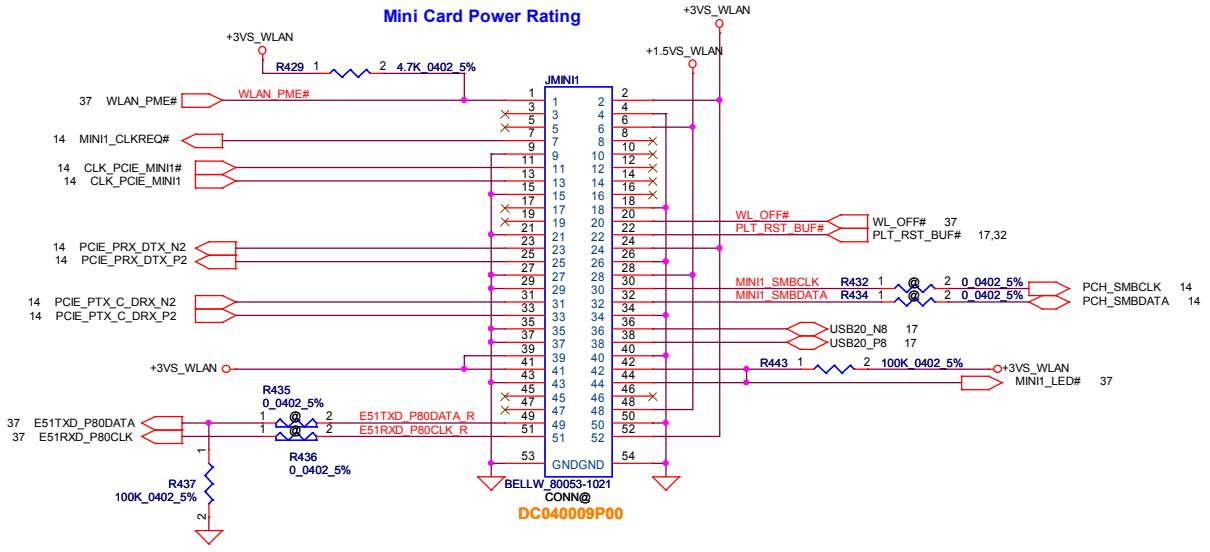
For Wireless LAN







Mini Card Power Rating



Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: MINI CARD (WLAN)

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

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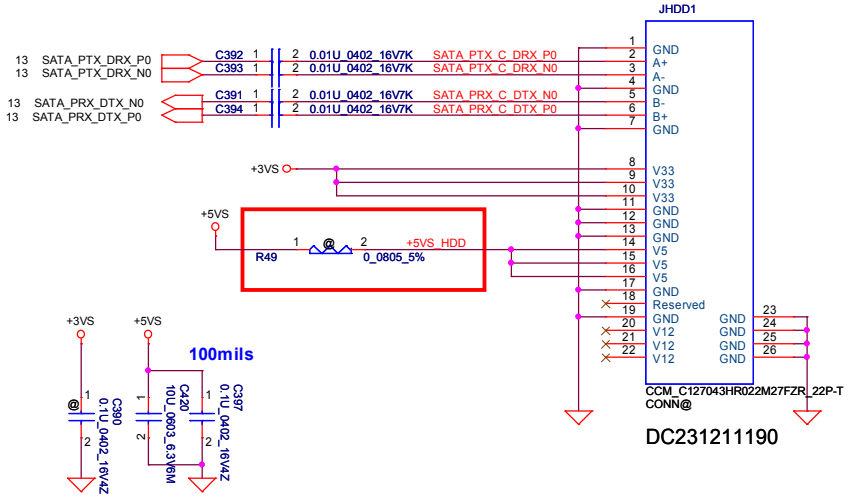
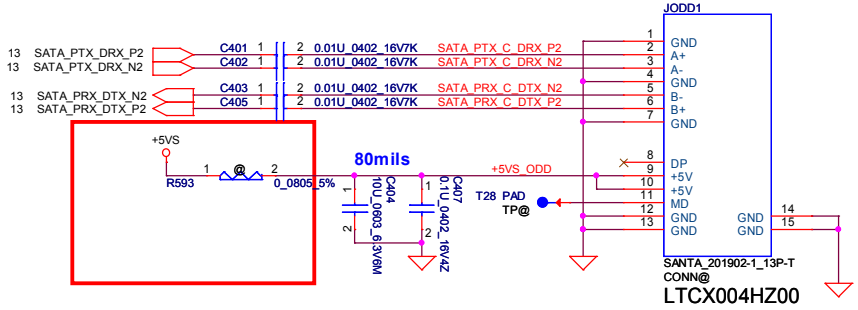
SATA HDD Conn.



DC231211190

SATA ODD Conn.



LTCX004HZ00

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Compal Electronics, Inc.

Title: HDD/ODD

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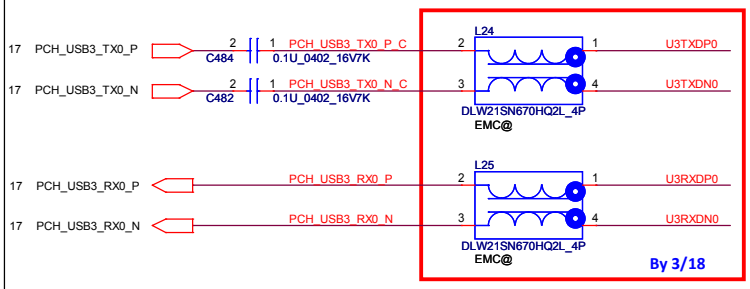

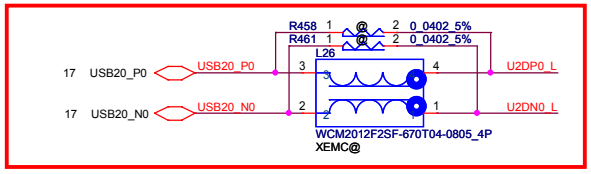

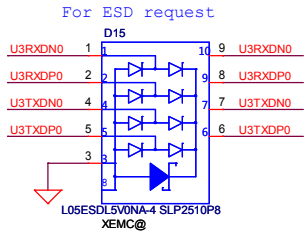

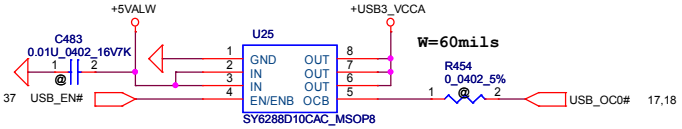

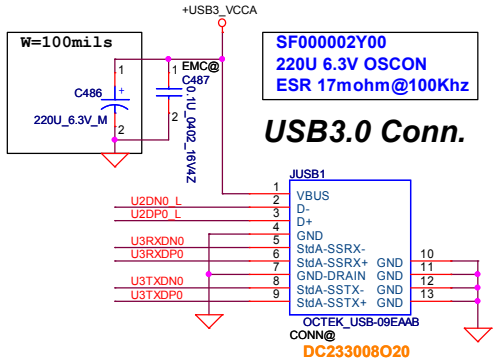

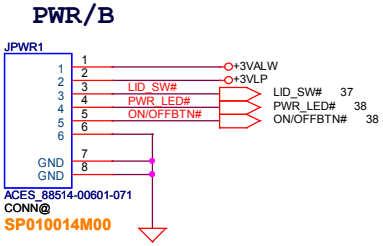

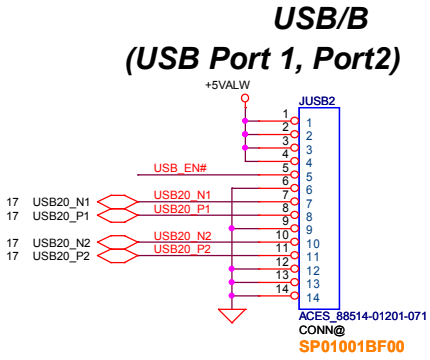

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: USB3.0 Conn/USB_B/PWR_B

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

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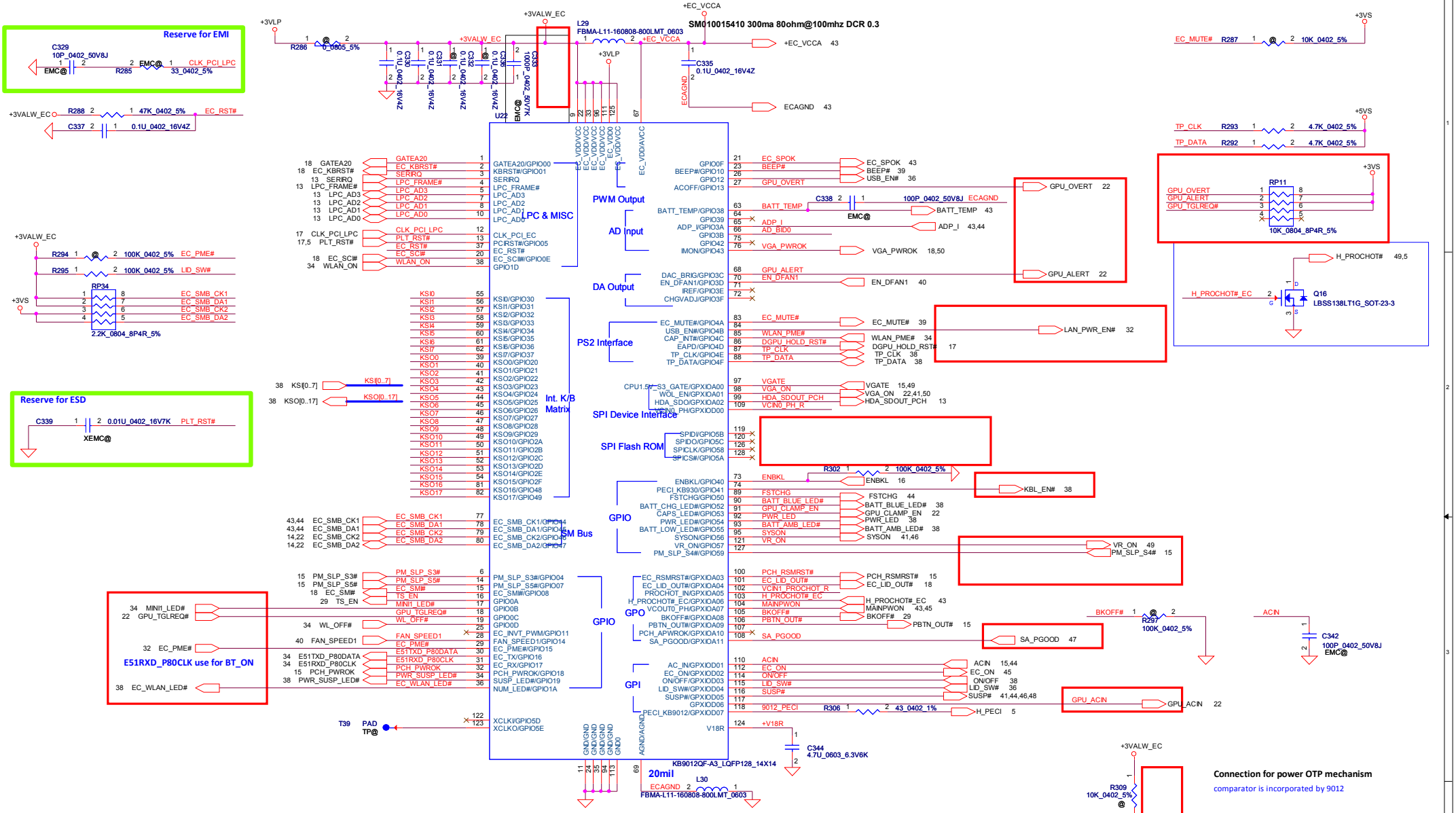
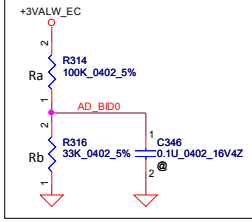


Board ID

See definition no Notes page, NEED to check EVERY TIME before new gerber-out



Phase	Revision	BID0	BID1
EVT	0.1	0	X
* PVT	0.2	1	X
PVT2	0.3	2	X
MP	1.0	3	X

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: **EC ENE-KB9012**

Size: Custom | Document Number: **LA-9535P M/B Schematics** | Rev: 1.0

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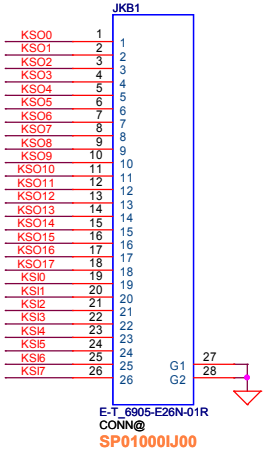
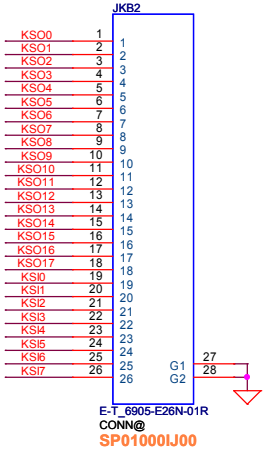
KB Conn.



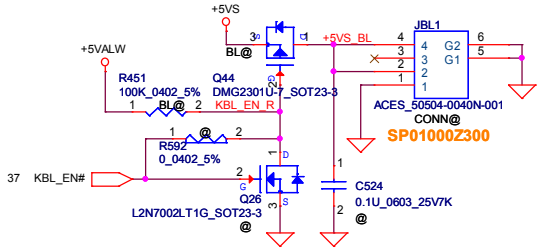
KSI[0..7] → KSI[0..7] 37

KSO[0..17] → KSO[0..17] 37

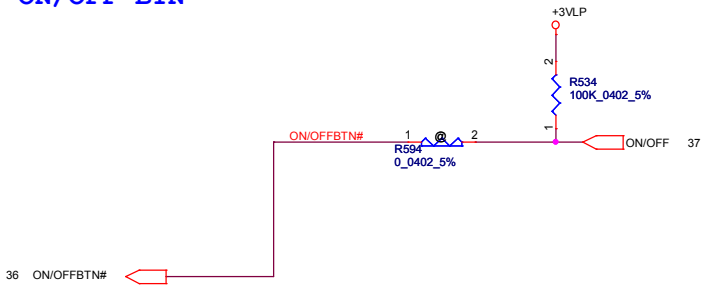
KB Conn.

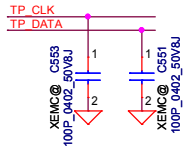


KB BackLight Conn.

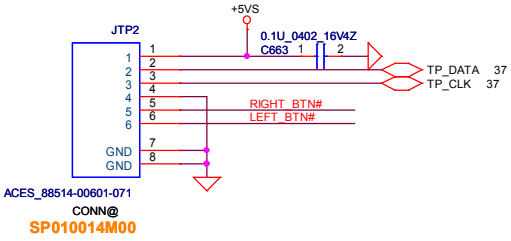


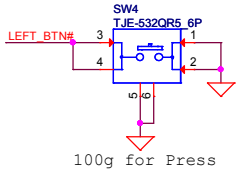
ON/OFF BTN

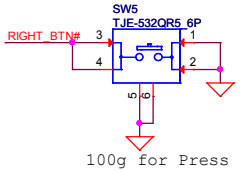


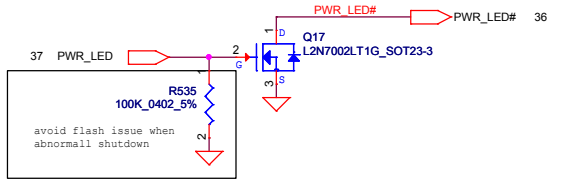


To TP/B Conn.

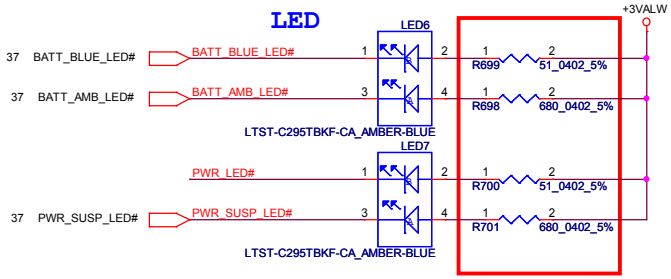




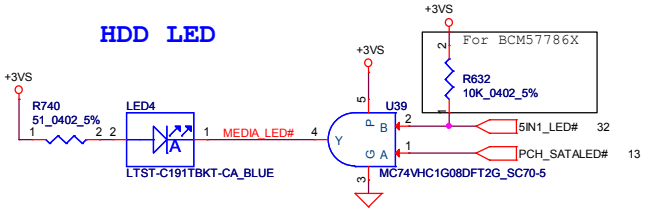


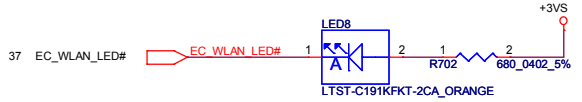


LED



HDD LED





Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: KB & TP & LED

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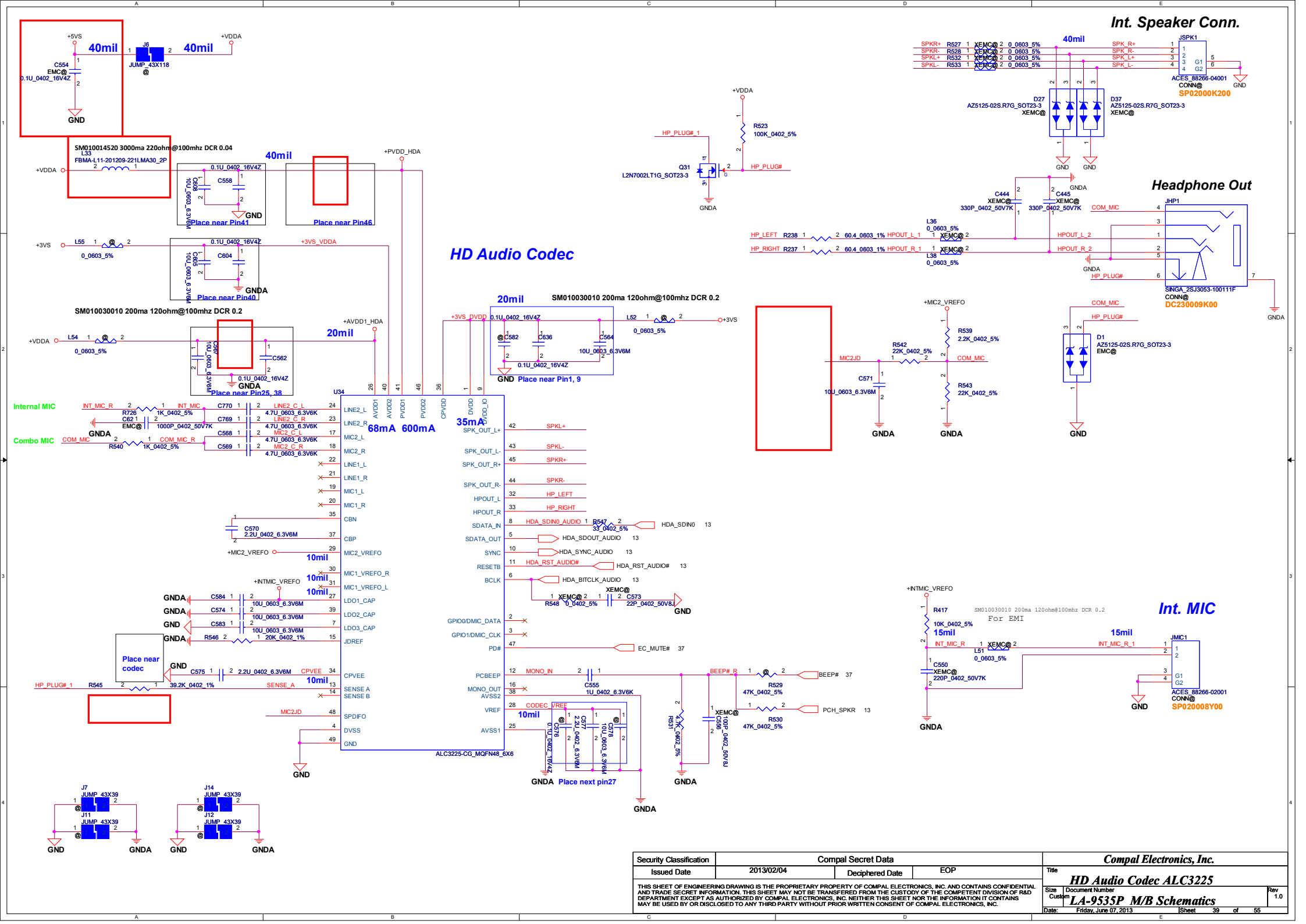
Int. Speaker Conn.
HD Audio Codec
Headphone Out
Int. MIC
Internal MIC
Combo MIC
U34
ALC3225-CG_MQFN48_6X6
SP02000K200
DC230009K00
SP02008Y00
Place near Pin41
Place near Pin46
Place near Pin40
Place near Pin25, 38
Place near Pin1, 9
Place near codec
Place next pin27
68mA 600mA
35mA
SM010030010 200ma 120ohm@100mhz DCR 0.2
SM010014520 3000ma 220ohm@100mhz DCR 0.04
For EMI
Security Classification
Compal Secret Data
Issued Date
2013/02/04
Deciphered Date
EOP
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HD Audio Codec ALC3225
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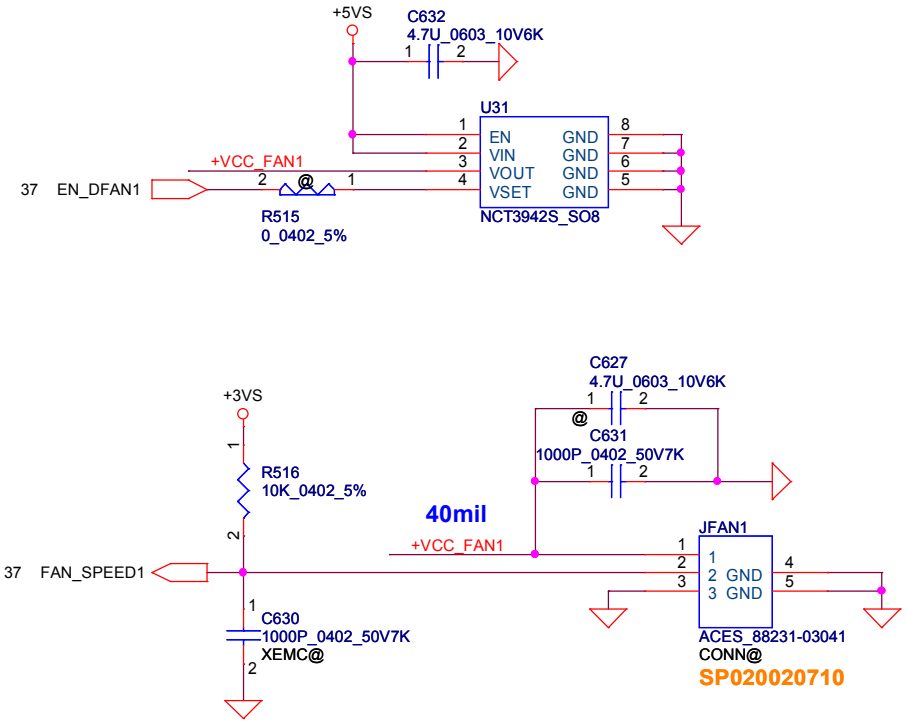
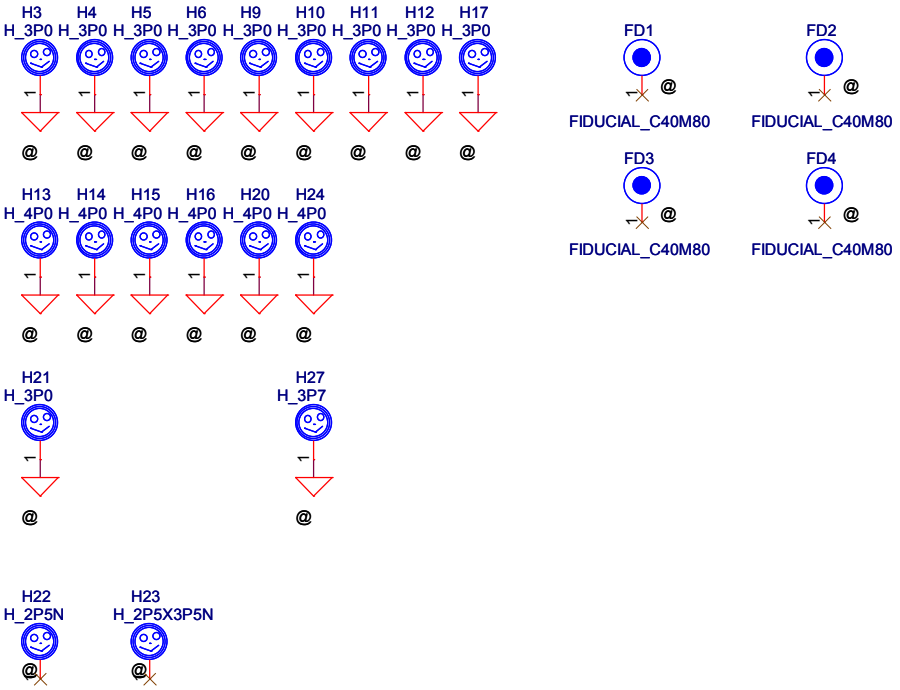
FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: FAN & Screw Hole & G-Sensor

Size	Document Number	Rev
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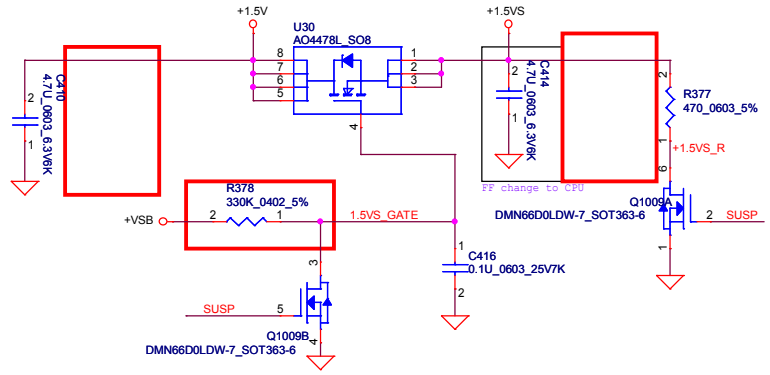
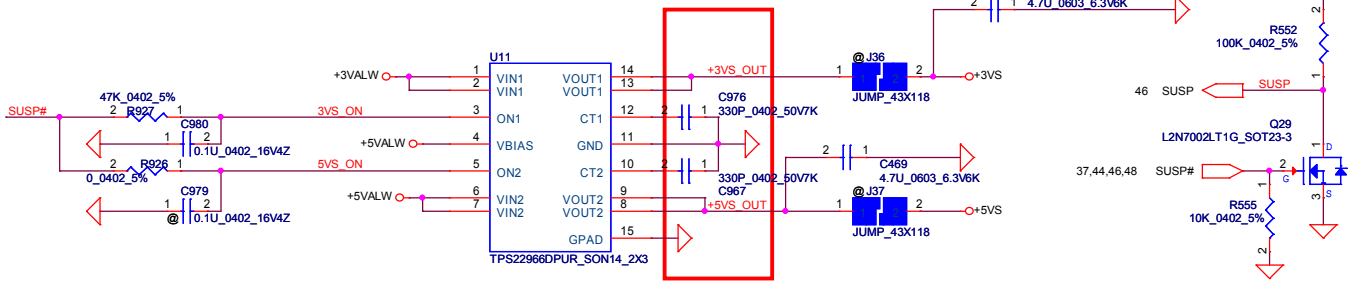
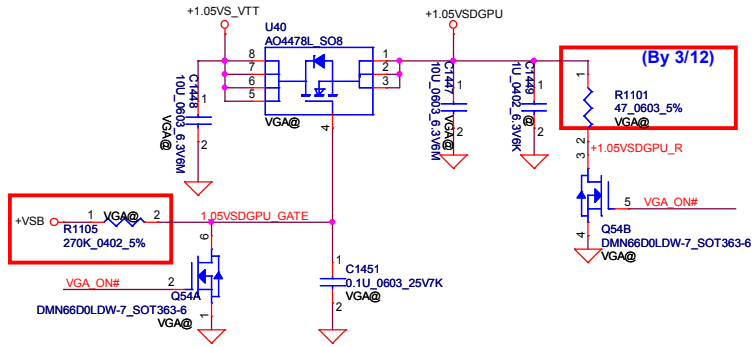
+1.5V to +1.5VS

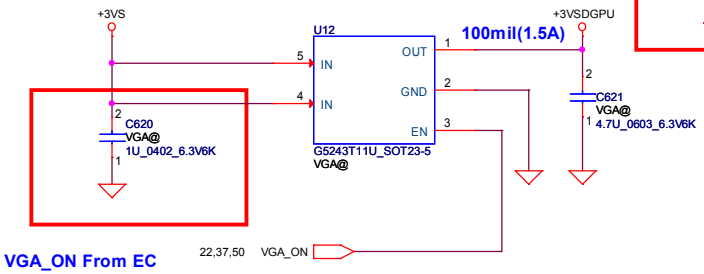


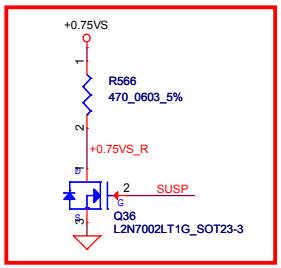


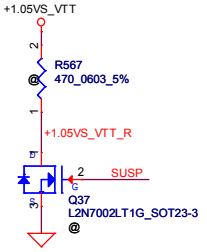
+1.05VS_VTT to +1.05VSDGPU

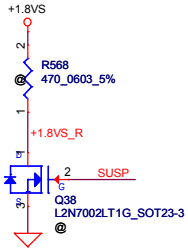


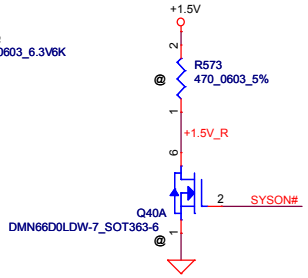
+3VS to +3VSDGPU for GPU

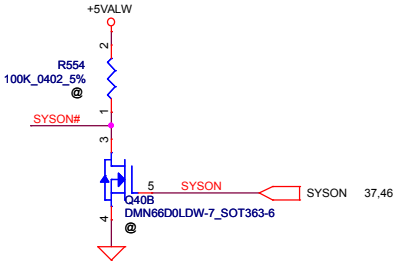




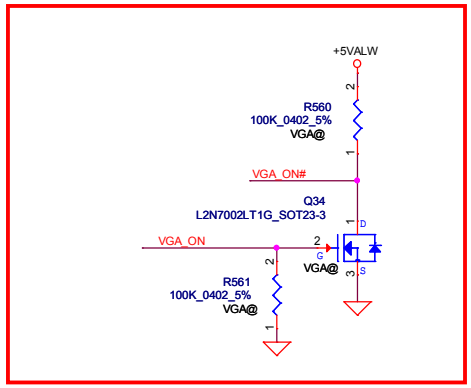








注意S3 reduce
+0.75V sequence



Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: DC Interface

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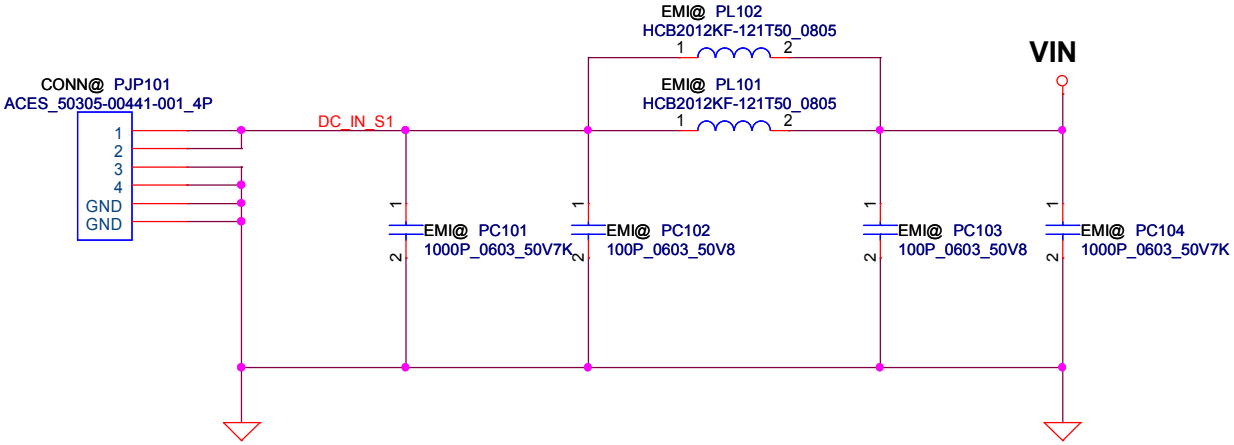
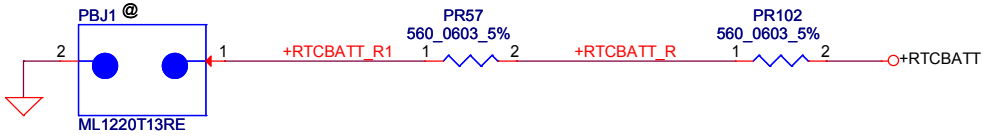
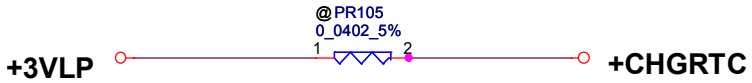






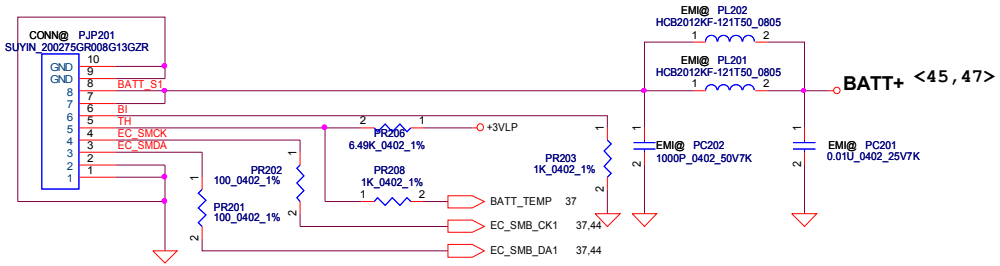
Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

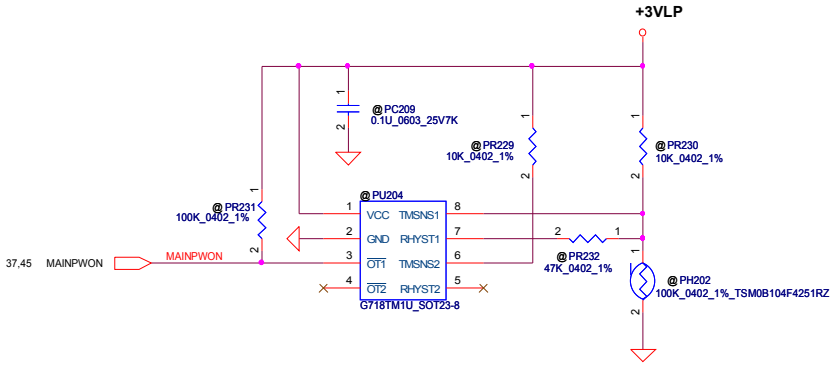
Compal Electronics, Inc.

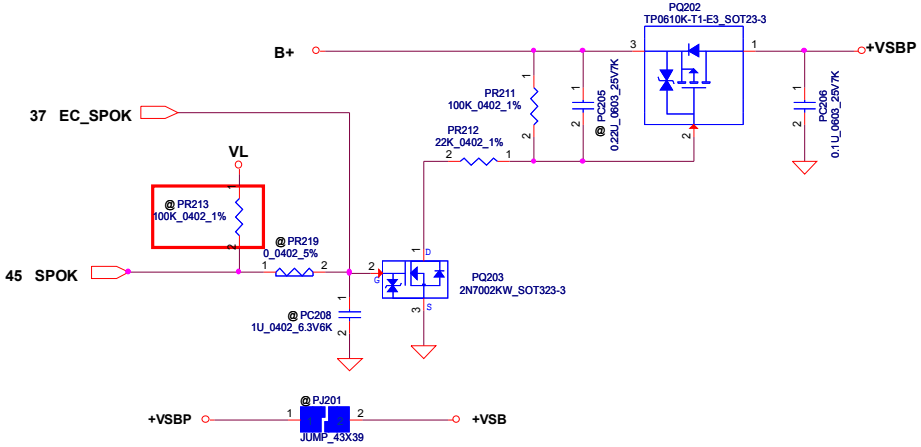
Title: DCIN

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

Date: Friday, June 07, 2013 | Sheet 42 of 55



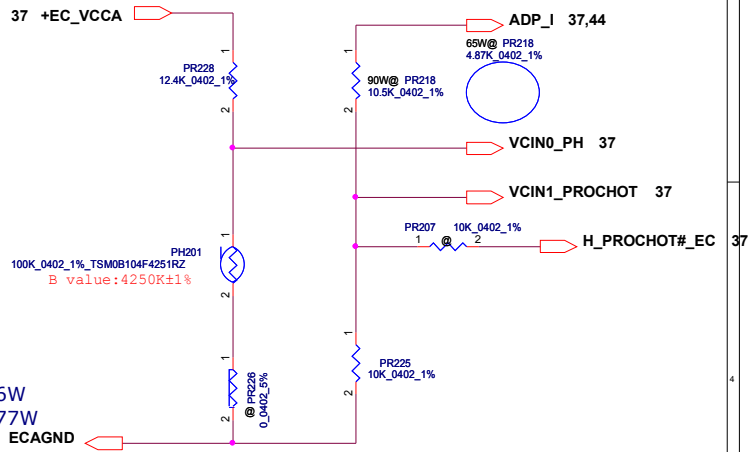




For KB9012 OTP	
92℃	1.2V, Active
56℃	2.255V, Recovery

For KB9012 sense 20mΩ	Active	Recovery
65W	84W,1.2V	56W,0.793V
90W	117W,1.2V	77W,0.791V
120W		

PH201 under CPU botten side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C



For 65W adapter==>action 84W , Recovery 56W
For 90W adapter==>action 117W , Recovery 77W

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
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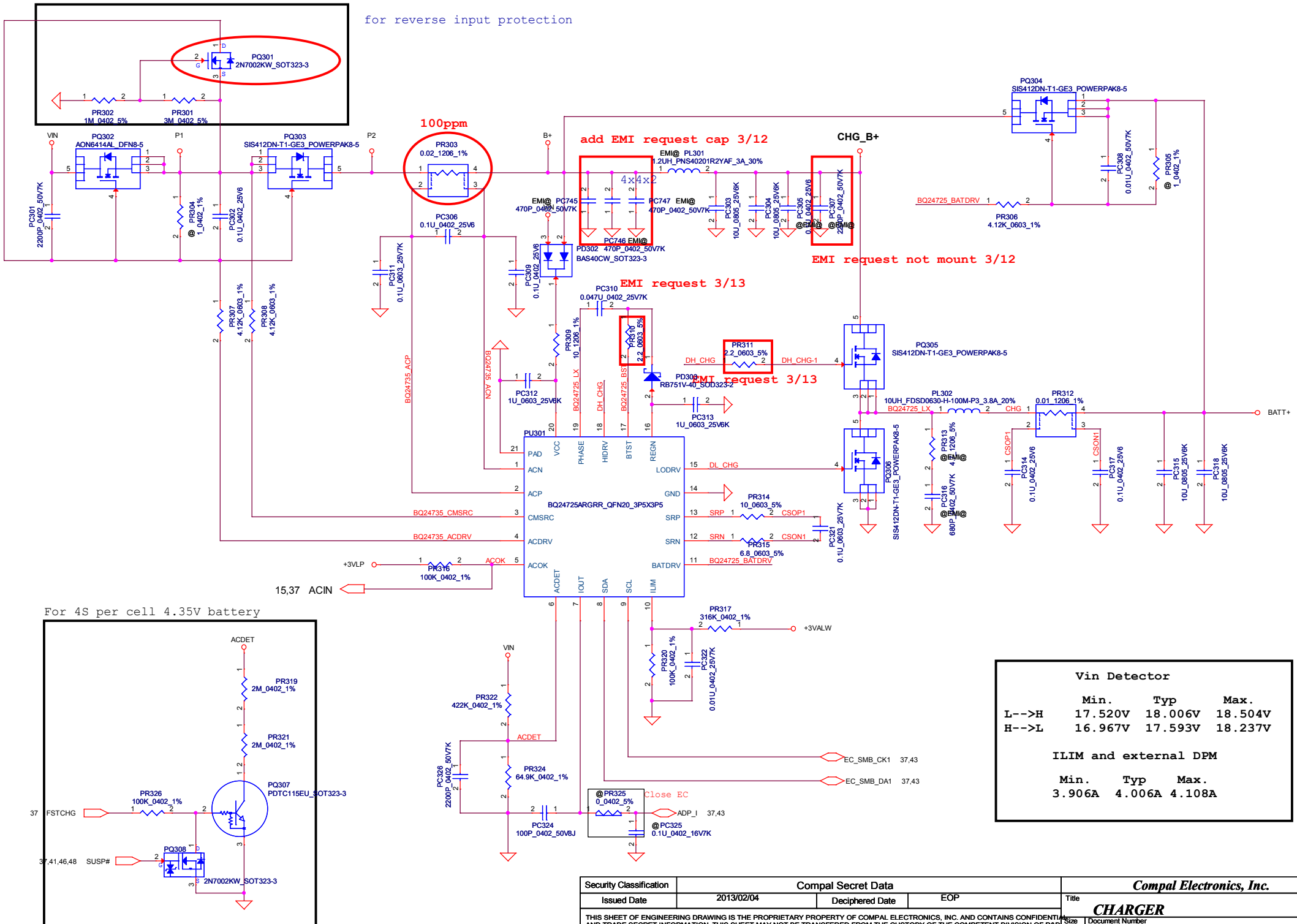


Vin Detector

	Min.	Typ	Max.
L-->H	17.520V	18.006V	18.504V
H-->L	16.967V	17.593V	18.237V

ILIM and external DPM

Min.	Typ	Max.
3.906A	4.006A	4.108A

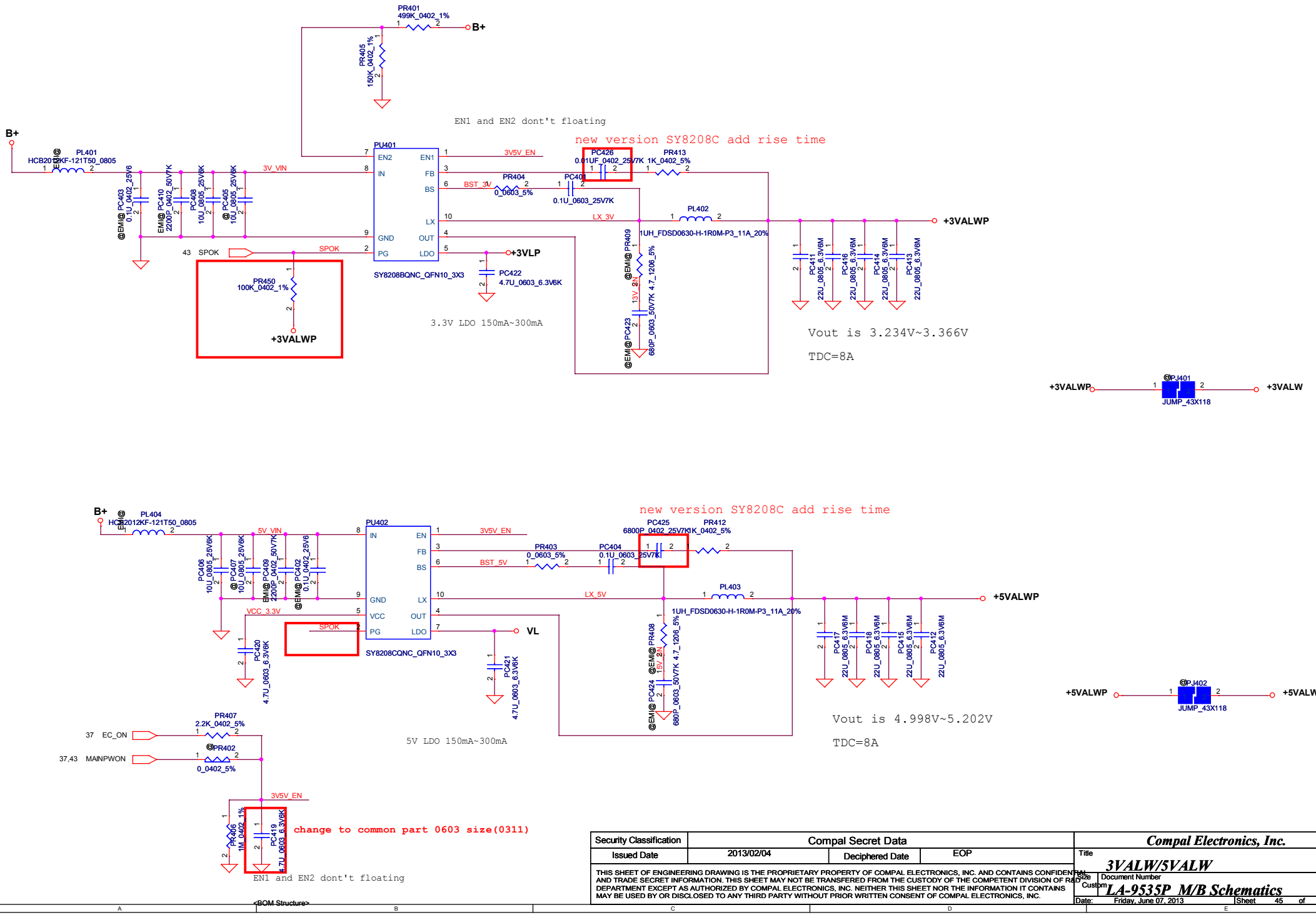
Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

Date: Friday, June 07, 2013 | Sheet 44 of 55



Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

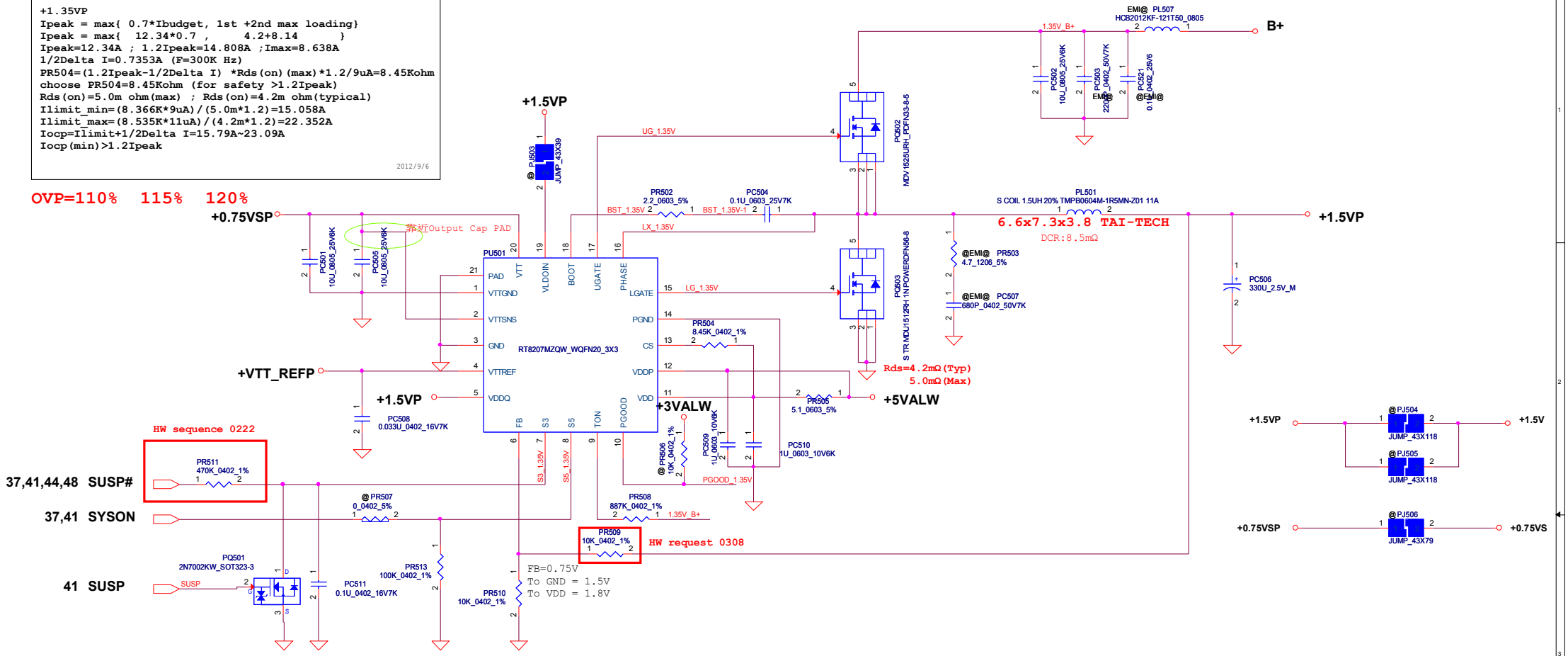
Date: Friday, June 07, 2013 | Sheet 45 of 55

<BOM Structure>

```
+1.35VP
Ipeak = max{ 0.7*Ibudget, 1st +2nd max loading}
Ipeak = max{  12.34*0.7 ,      4.2+8.14       }
Ipeak=12.34A ; 1.2Ipeak=14.808A ;Imax=8.638A
1/2Delta I=0.7353A (F=300K Hz)
PR504=(1.2Ipeak-1/2Delta I) *Rds(on)(max)*1.2/9uA=8.45Kohm
choose PR504=8.45Kohm (for safety >1.2Ipeak)
Rds(on)=5.0m ohm(max) ; Rds(on)=4.2m ohm(typical)
Ilimit_min=(8.366K*9uA)/(5.0m*1.2)=15.058A
Ilimit_max=(8.535K*11uA)/(4.2m*1.2)=22.352A
Iocp=Ilimit+1/2Delta I=15.79A~23.09A
Iocp(min)>1.2Ipeak
```

2012/9/6

OVP=110% 115% 120%


+1.5VP
+0.75VSP
B+
+1.35V_B+
EMI@ PL507
HCB2012KF-121T50_0805
PC502 10U_0805_25V6K
PC503 220U_0402_50V7K
PC521 0.1U_0402_25V6
@EMI@
PQ502 MDV1525URH_PDFN33-8-5
PQ503 MDU1512RH 1N POWERDFN56-8
PR502 2.2_0603_5%
PC504 0.1U_0603_25V7K
BST_1.35V
BST_1.35V-1
UG_1.35V
LX_1.35V
LG_1.35V
PL501
S COIL 1.5UH 20% TMPB0604M-1R5MN-Z01 11A
6.6x7.3x3.8 TAI-TECH
DCR:8.5mΩ
@EMI@ PR503 4.7_1206_5%
@EMI@ PC507 680P_0402_50V7K
PC506 330U_2.5V_M
Rds=4.2mΩ(Typ)
5.0mΩ(Max)
PU501
RT8207MZQW_WQFN20_3X3
PAD
VTT
VLDOIN
BOOT
UGATE
PHASE
VTTGND
VTTSNS
GND
VTTREF
VDDQ
LGATE
PGND
CS
VDDP
VDD
PGOOD
FB
S3
S5
TON
PC501 10U_0805_25V6K
PC505 10U_0805_25V6K
PC508 0.033U_0402_16V7K
PR504 8.45K_0402_1%
PR505 5.1_0603_5%
+VTT_REFP
+3VALW
+5VALW
PC509 1U_0603_10V6K
PC510 1U_0603_10V6K
@PR506 10K_0402_1%
PGOOD_1.35V
S3_1.35V
S5_1.35V
@PJ504
@PJ505
@PJ506
JUMP_43X118
JUMP_43X79
+1.5V
+0.75VS
HW sequence 0222
37,41,44,48 SUSP#
37,41 SYSON
41 SUSP
PR511 470K_0402_1%
@PR507 0_0402_5%
PR508 887K_0402_1%
PR509 10K_0402_1%
HW request 0308
PQ501 2N7002KW_SOT323-3
PC511 0.1U_0402_16V7K
PR513 100K_0402_1%
PR510 10K_0402_1%
FB=0.75V
To GND = 1.5V
To VDD = 1.8V
```

| STATE | S3 | S5 | 1.35VP | VTT_REFP | 0.675VSP |
|---|---|---|---|---|---|
| S0 | Hi | Hi | On | On | On |
| S3 | Lo | Hi | On | On | Off (Hi-Z) |
| S4/S5 | Lo | Lo | Off (Discharge) | Off (Discharge) | Off (Discharge) |

Note: S3 - sleep ; S5 - power off



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2013/02/04 | Deciphered Date | EOP |



Compal Electronics, Inc.

Title: 1.5VP/0.75VSP

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```

VFB= 0.704V
Vo=VFB*(1+11.5K/10K)= 1.5V
Freq=290KHz(typ)

Cesr= 15m ohm
Ipeak= 4.7A Imax= 3.29A Iocp=5.64A
Iocp= 5.72A~6.43A

HW sequence (0311)

Resistance(KΩ)	Frequency(KHz)
470	290
200	340
100	380
39	430

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

Rds=13.5mΩ(Typ)
16.5mΩ(Max)

Imax= 4.2A, Ipeak= 6A
FB=0.6V

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: +VCCSAP/+1.5VSDGPUP

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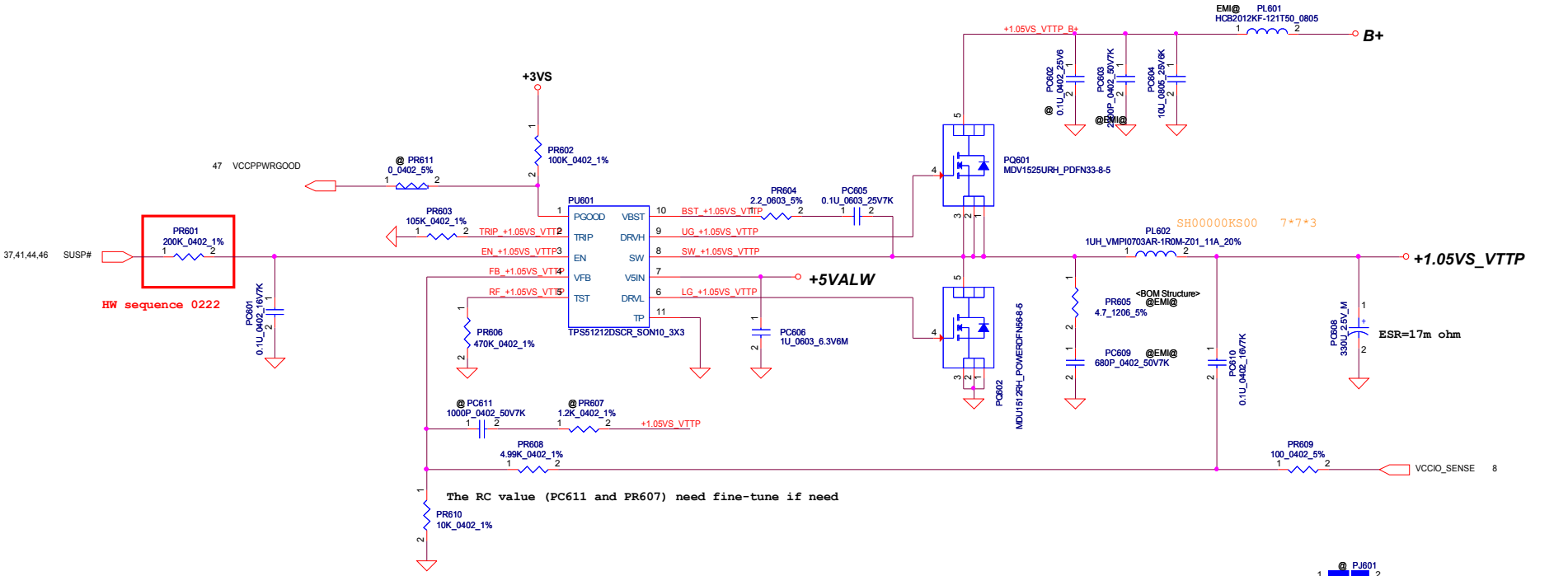
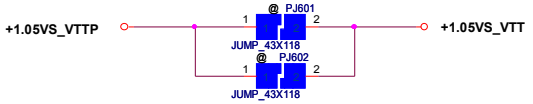
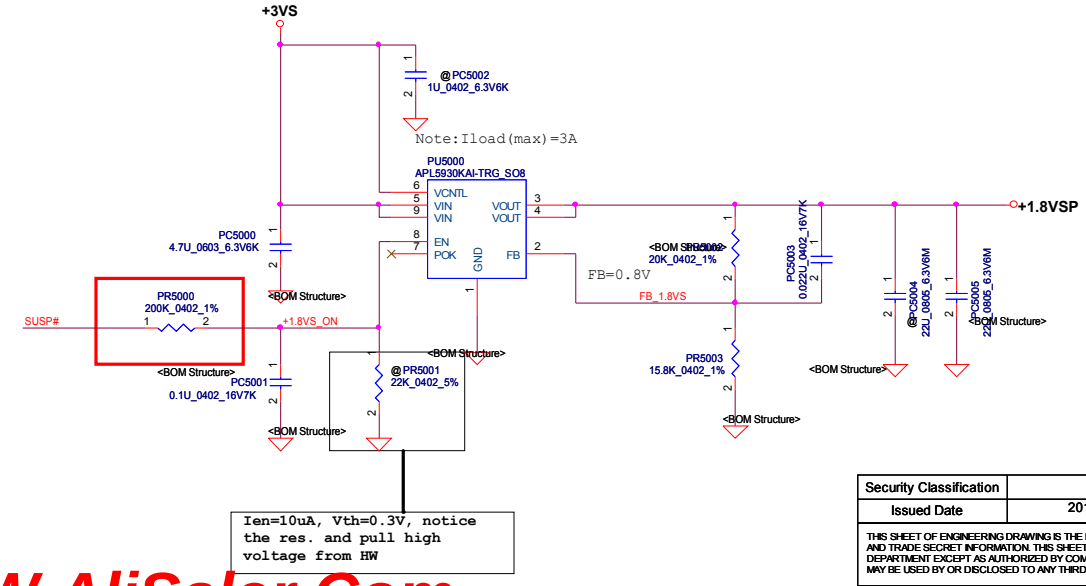
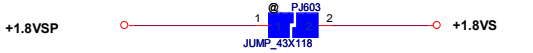
+1.05VSP Ipeak=5.36A ; Imax=3.752A ; 1.2Ipeak=6.432
Delta I=0.xxxxA=>1/2Delta I=0.xxxxA,F= 800K Hz(typ)









Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: +1.05VS_VTTP/+1.8VSP

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Layout Note
SVID routing
1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.
2. SVID spacing requirement is 18mils(0.475mm).
3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).
4. The SVID bus must be ground reference, It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.
5. Avoid routing under noisy circuit, e.g. switch node , Gate driver, B+, Vin, high speed signal.
6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

Layout Note
Reduce Acoustic Noise
1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
2. Input ceramic caps must place on symmetry same location on top side and bottom side.

VDD source use +5VS and PGOOD source use +3VS
Please confirm power on and down sequence, make sure VGATE after CPU_CORE on.

OCP setting=39.9~44.99A

MDV1525 Vds=30V
Rds(on)=11.5~14m ohm@Vgs=4.5V

0.22uH DCR= 0.97+-5% m ohm, Idc~Isat= 25~34A

transient request 0218

MDU1511 Vds=30V
Rds(on)=2.7~3.3m ohm@Vgs=4.5V

Height 8 mm

0.22uH DCR= 0.97+-5% m ohm, Idc~Isat= 25~34A

OCP setting=39.9~44.99A

Close GFX choke

Close GFX L/S MOS

Close CPU L/S MOS

Close CPU choke

PR716 and PR724
27.4K ohm for 100 degree
61.9K ohm for 110 degree

PL701 PL702 Footprint用SH00000HQ00代替,因為SH00000NM00_R22為2PIN 2012/07/05

Security Classification	<BOM Structure> Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: CPU_CORE/VGFX_CORE

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

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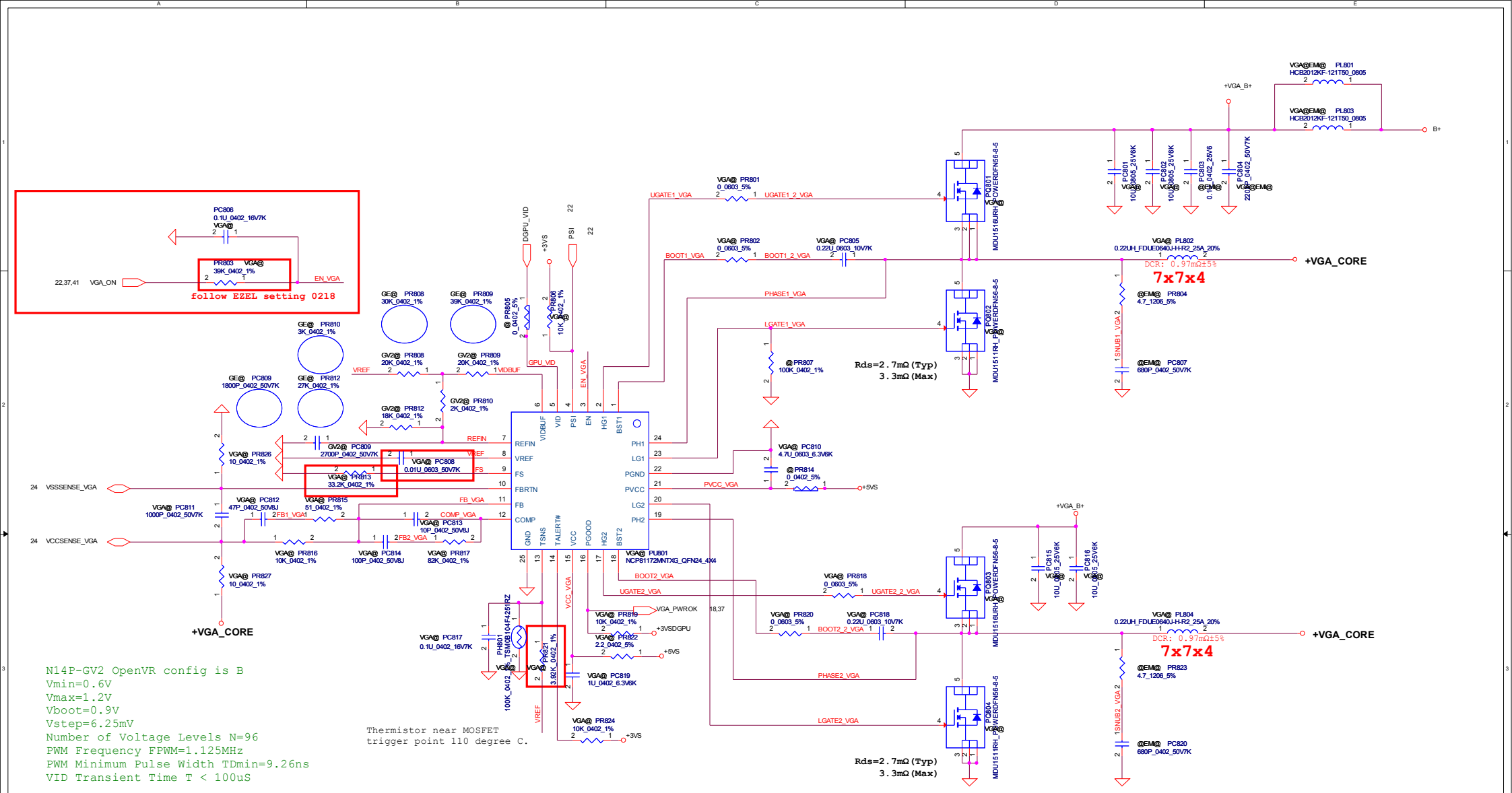

N14P-GV2 OpenVR config is B
Vmin=0.6V
Vmax=1.2V
Vboot=0.9V
Vstep=6.25mV
Number of Voltage Levels N=96
PWM Frequency FPWM=1.125MHz
PWM Minimum Pulse Width TDmin=9.26ns
VID Transient Time T < 100uS

N14P-GE OpenVR config is C
Vmin=0.65V
Vmax=1.15V
Vboot=0.9V
Vstep=25mV
Number of Voltage Levels N=20
PWM Frequency FPWM=0.676MHz
PWM Minimum Pulse Width TDmin=74ns
VID Transient Time T < 100uS

N14P-GV2 TDP 25W
Ipeak=55A
Imax=25A
Iocp=72A
Fsw=450KHz
bulk cap 560uF*2

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: +VGA_CORE

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PWR Rule 17W@ULV(CR BGA1023_GT2) CPU2.9m GFx3.9m
CPU 330uF/9m *3, 22uF(0805) *12, 2.2uF(0402)*16
GFX 330uF/9m*2, 22uF(0805)*6, 10uF(0603)*6, 1uF(0402)*11
1.05V 330uF*2,10uF(0603)*10,1uF(0402)*26

+VGFX_CORE

PC901 1U_0402_6.3V6K
PC910 @ 1U_0402_6.3V6K
PC911 @ 1U_0402_6.3V6K
PC912 @ 1U_0402_6.3V6K
PC913 @ 1U_0402_6.3V6K
PC914 1U_0402_6.3V6K
PC915 1U_0402_6.3V6K
PC916 @ 1U_0402_6.3V6K
PC917 1U_0402_6.3V6K
PC918 1U_0402_6.3V6K
PC919 1U_0402_6.3V6K

PC928 10U_0603_6.3V6M
PC929 10U_0603_6.3V6M
PC930 @ 10U_0603_6.3V6M
PC931 10U_0603_6.3V6M
PC932 @ 10U_0603_6.3V6M
PC933 10U_0603_6.3V6M

ESR=9m ohm

PC941 330U_D2_2V_Y
PC942 330U_D2_2V_Y

PC943 22U_0805_6.3V6M
PC944 @ 22U_0805_6.3V6M
PC945 22U_0805_6.3V6M
PC946 22U_0805_6.3V6M
PC947 @ 22U_0805_6.3V6M
PC948 22U_0805_6.3V6M

Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

+1.05VS_VTT

PC956 1U_0402_6.3V6K
PC957 1U_0402_6.3V6K
PC958 1U_0402_6.3V6K
PC959 1U_0402_6.3V6K
PC960 1U_0402_6.3V6K
PC961 1U_0402_6.3V6K
PC962 1U_0402_6.3V6K
PC963 1U_0402_6.3V6K
PC964 1U_0402_6.3V6K
PC965 1U_0402_6.3V6K
PC966 1U_0402_6.3V6K
PC967 1U_0402_6.3V6K
PC968 1U_0402_6.3V6K

PC972 1U_0402_6.3V6K
PC973 1U_0402_6.3V6K
PC974 1U_0402_6.3V6K
PC975 1U_0402_6.3V6K
PC976 1U_0402_6.3V6K
PC977 1U_0402_6.3V6K
PC978 1U_0402_6.3V6K
PC979 1U_0402_6.3V6K
PC980 1U_0402_6.3V6K
PC981 1U_0402_6.3V6K
PC982 1U_0402_6.3V6K
PC983 1U_0402_6.3V6K
PC984 1U_0402_6.3V6K

PC985 @ 10U_0603_6.3V6M
PC986 10U_0603_6.3V6M
PC987 10U_0603_6.3V6M
PC988 @ 10U_0603_6.3V6M
PC989 @ 10U_0603_6.3V6M

PC990 @ 10U_0603_6.3V6M
PC991 @ 10U_0603_6.3V6M
PC992 10U_0603_6.3V6M
PC993 10U_0603_6.3V6M
PC994 10U_0603_6.3V6M
PC995 330U_D2_2V_Y

ESR=9m ohm

+CPU_CORE

PC902 2.2U_0402_6.3V6M
PC903 2.2U_0402_6.3V6M
PC904 2.2U_0402_6.3V6M
PC905 2.2U_0402_6.3V6M
PC906 2.2U_0402_6.3V6M
PC907 2.2U_0402_6.3V6M
PC908 @ 2.2U_0402_6.3V6M
PC909 2.2U_0402_6.3V6M

PC920 @ 2.2U_0402_6.3V6M
PC921 2.2U_0402_6.3V6M
PC922 @ 2.2U_0402_6.3V6M
PC923 @ 2.2U_0402_6.3V6M
PC924 @ 2.2U_0402_6.3V6M
PC925 @ 2.2U_0402_6.3V6M
PC926 2.2U_0402_6.3V6M
PC927 2.2U_0402_6.3V6M

For BOT side

+CPU_CORE

PC934 22U_0805_6.3V6M
PC935 22U_0805_6.3V6M
PC936 22U_0805_6.3V6M @
PC937 22U_0805_6.3V6M @
PC938 22U_0805_6.3V6M @
PC939 22U_0805_6.3V6M @
PC940 22U_0805_6.3V6M

PC949 22U_0805_6.3V6M
PC950 22U_0805_6.3V6M
PC951 22U_0805_6.3V6M
PC952 22U_0805_6.3V6M
PC953 22U_0805_6.3V6M @
PC954 22U_0805_6.3V6M
PC955 @ 22U_0805_6.3V6M

For TOP side

+CPU_CORE

+-20% SGA00006100 ESR=9m ohm

PC969 330U_D2_2V_Y
PC970 330U_D2_2V_Y
PC971 330U_D2_2V_Y

ESR=9m ohm

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: CPU_CORE_CAP

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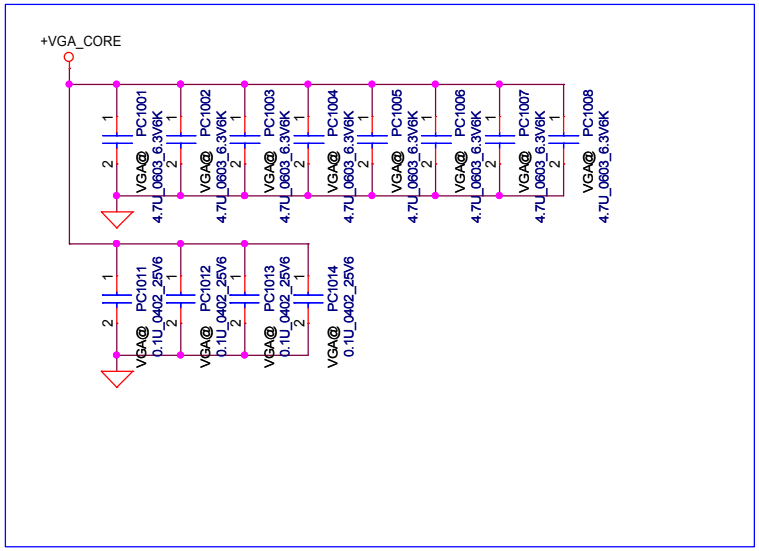
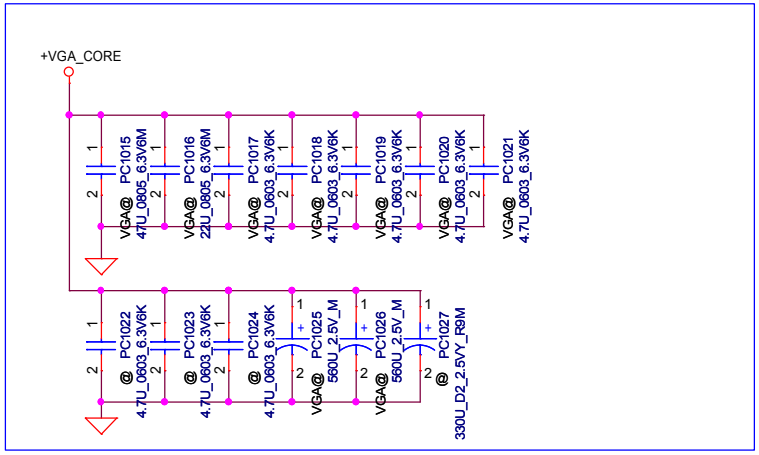


nVidia GB4-128 package
Under GPU
4.7uF 0603 * 10
0.1uF 0402 * 4



nVidia GB4-128 package
Near GPU
47uF 0805 *1
22uF 0805 *1
4.7uF 0805 *5 (0603)
330uF POS *1 <6mΩ

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: VGA CORE CAP

Size: Custom | Document Number: LA-9535P M/B Schematics | Rev: 1.0

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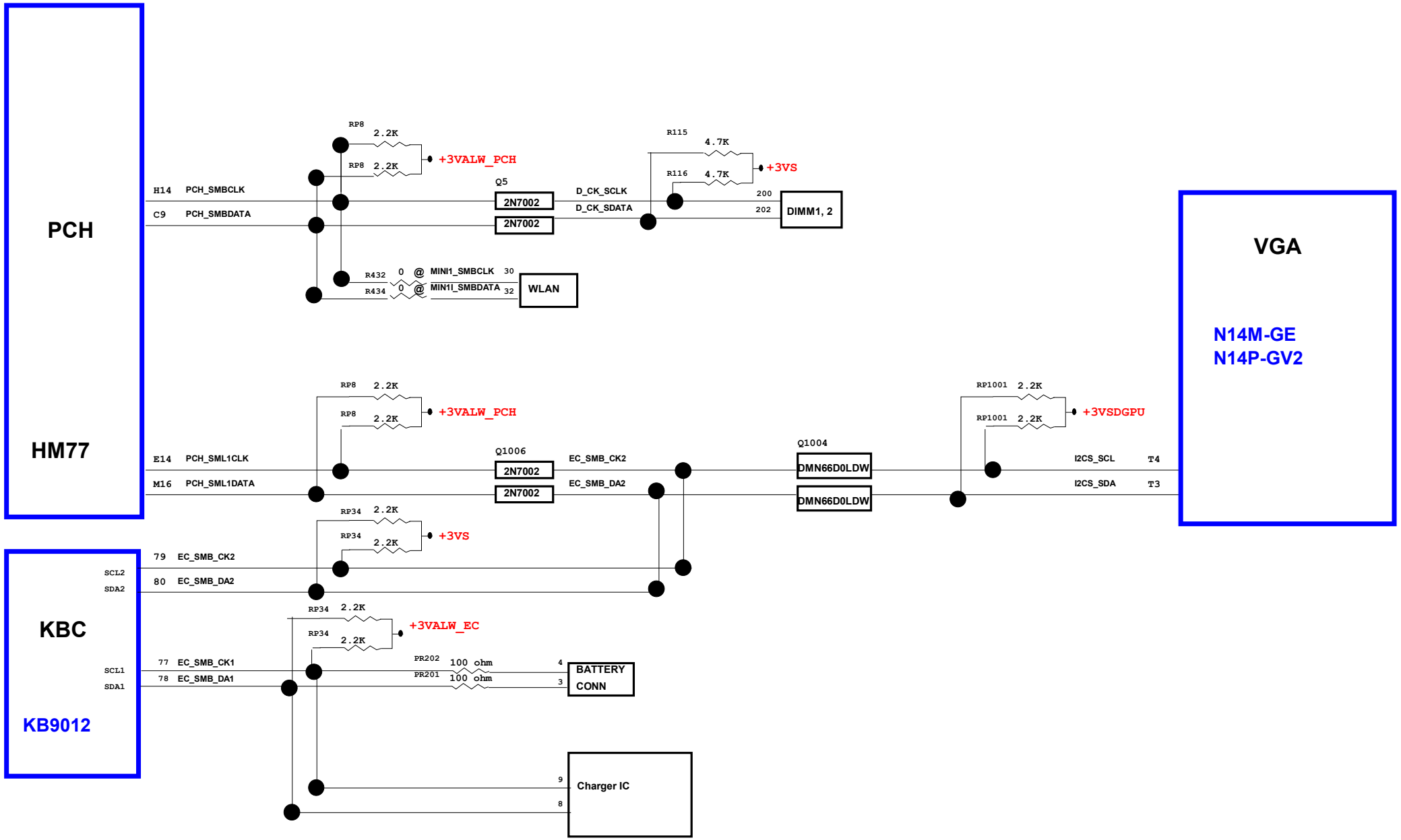

Security Classification	Compal Secret Data		
Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.

Title: SMBUS Block diagram

Size	Document Number	Rev
Custom	LA-9535P M/B Schematics	1.0

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	For 4S battery request	44	mount PR319,PR321,PR326,PQ307,PQ308	0310	C
2	change size to common part	45	PC419 change to 0603 common part	0310	C
3	HW sequence request	47	PR1003 to 30k	0311	C
4	EMI request	44	not mount PC307	0312	C
5	EMI request	44	add PC745 PC746 PC747	0313	C
6	EMI request	44	change PR311 PR310 to 2.2Ohm	0313	C
7	GFX_OCP	49	change PR707 to 576hm	0314	C
8					
9					
10					
11					
12					
13				3/5	EVT
14				3/5	EVT
15					
16					
17					
18					
19					
20					

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Issued Date	2013/02/04	Deciphered Date	EOP

Compal Electronics, Inc.
Title: PW PIR
Size: A3 | Document Number: LA-9535P M/B Schematics | Rev: 1.0
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03/06
Change R1033 from 4.99K to 10K(ROM_SO VGA_DEVICE)
Change U51 N14P-GV2 from SA00006B500 to SA00006B510
Change Y6 P/N to SJ10000E800(合併用料)

03/11
Add net +XDPWR_SDPWR_MSPWR_R
Add share rom feature
  Add R112 R140 R141 R144
  Add EC_SPI_MISO_1 , PCH_SPI_MISO_1
  Add EC_SPI_CS0# , PCH_SPI_CS0#
  Add EC_SPI_CLK_1 , PCH_SPI_CLK_1
  Add EC_SPI_MOSI_1 , PCH_SPI_MOSI_1
R541 pop 1K VGA@
R1101 470-->47 SD013470A80
D1000.3 VGA_PWROK changes into VGA_ON

SW3 @ 拿掉不上
Removed U15,R107,R108
Removed R151,R159,R160,R184,R97
Removed R524,R525,R526 換 RP13 5%--->1%

03/12
Add C441 470pF(SE074471K80),EMC@, EMI solution
Change U51 N14P-GV2 SA00006B510-->SA00006B530 R3 P/N
Change U51 N14M-GE SA000068A00-->SA000068A10 R3 P/N

0313a
Combine with PWR_Z5WE1_LA9535PR02_PWR_0313.DSN

0313b
Remove RP14,
 PCH_GPIO2 不接
 PCH_GPIO3 不接
 PCH_GPIO53 不接

RP13 5%--->1%(SD300002Y00)

0313C
2nd rom 加回去
Add U15,R107,R108
Add R97 R151 R159 R160 R184
Del R112 R140 R141 R144

0314
R285 XEMC@-->EMC@
C329 22P-->10P, XEMC@-->EMC@

Add C230 0.1U for card reader enable

Board ID
R316 0ohm 改 8.2K 上件
R314 @-->改上件
C346 @-->改上件

0314C
R774 change from 10 to 56ohm
R1027,R1028,R1029,R1030,R1035,R1036,R1039,R1033,R1042
at N14M-GE SKU 10K_0402_5% change to 10K_0402_1%

0314d
L33 changes into SM010014520

0315a
Add net CRT_4, CRT_11 for 測點
R541 bom structure--->VGA@
C346 board ID cap改@ 不上

0318
L24,L25 change from SM070001600 (12ohm USB3.0 common mode choke)
to SM070001R00 (Murata 67ohm)

0419
Add Touch screen feature and JTS1

0422
Remove PEG 16X

0425
Add HM70 NM70 文字敘述
Add FFR VRAM strap for N14M-GE N14P-GV2

0502
Update CPU,PCH,VRAM P/N

0505
Pop RP16 for LAN loopback

0528
N14M-GE ROM_SO keep 10K pull low.
N14P-GV2 need change be to EVT R1033 as 4.99K_0402_1%

C142-->15pF(SE071150J80) to meet off mode timing

0604
Correct page1 date code
Update page24 3D device/vga device notice

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Compal Electronics, Inc.
Title: HW PIR
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