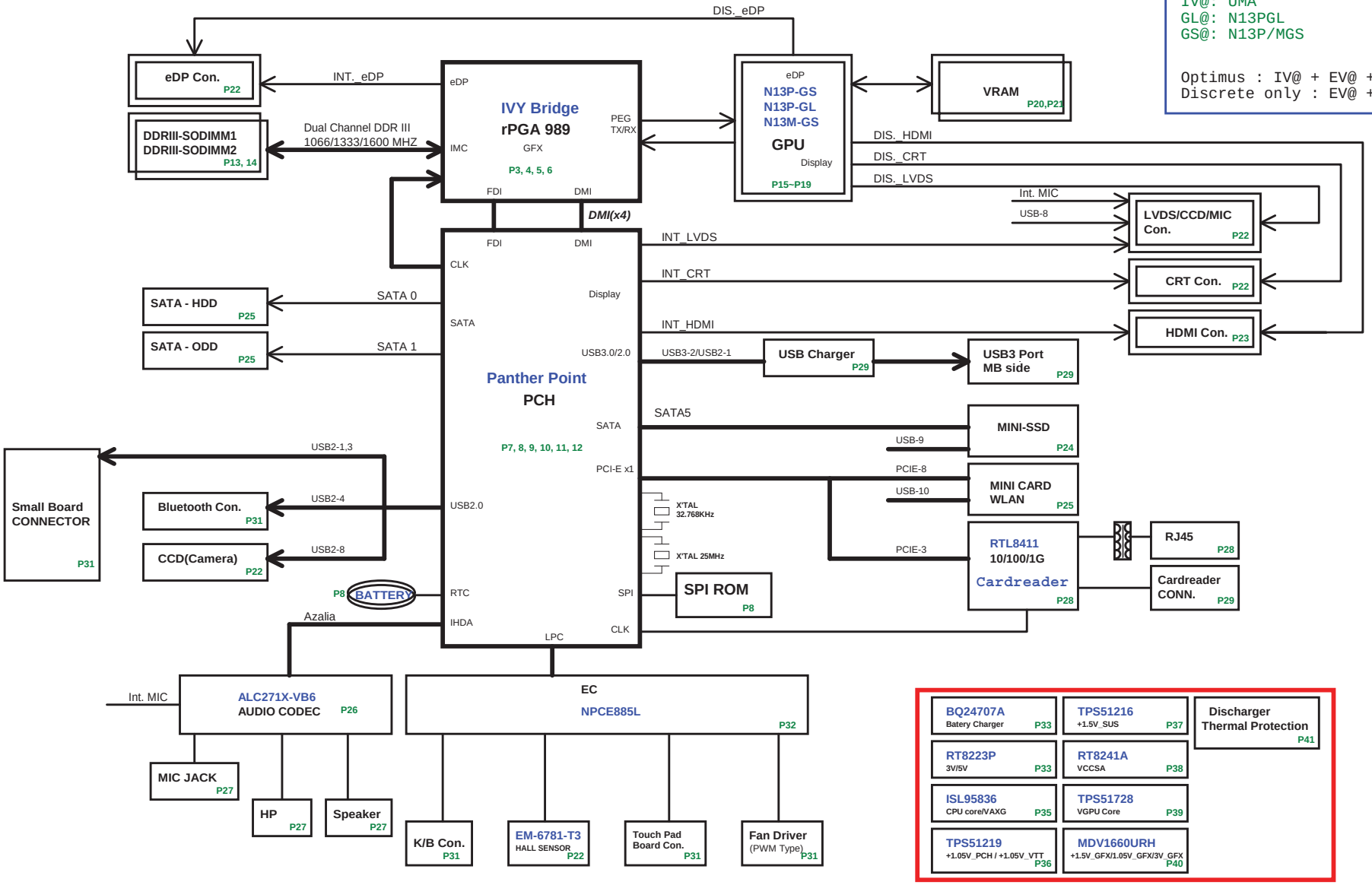
ZQTA/ZQSA CRV SYSTEM BLOCK DIAGRAM

BOM

IV@ : iGPU
EV@ : dGPU
OP@ : Optimus
DO@ : Discrete only
SP@ : Special
SNP@: N13PGS/GL
IV@: UMA
GL@: N13PGL
GS@: N13P/MGS

Optimus : IV@ + EV@ + OP@
Discrete only : EV@ + DO@



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PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	Block Diagram	1A

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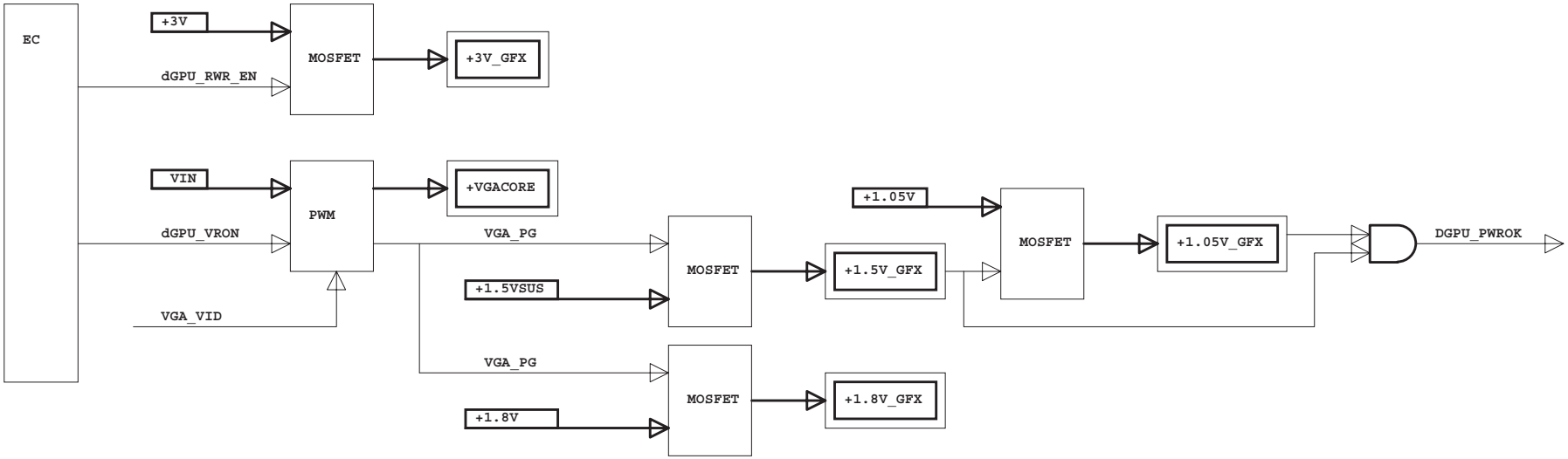
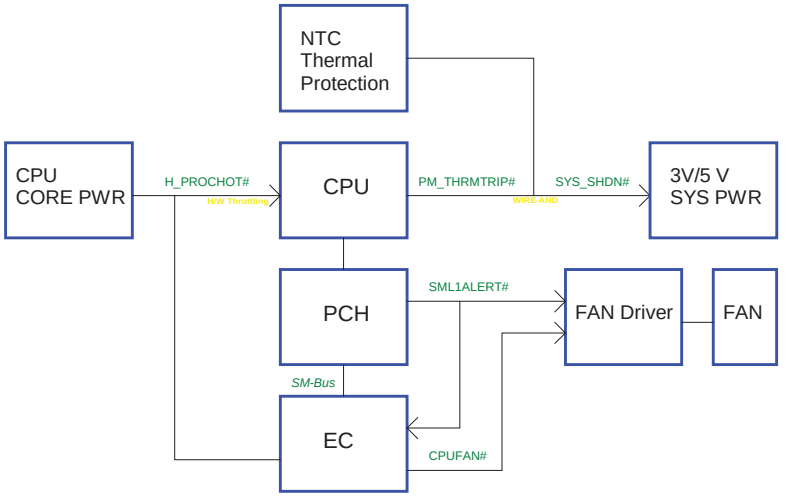
VGA power up sequence



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	VRON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER/IVY/SNB bridge VCCIO	MAINON	S0
+VCCSA	+0.9V	CPU POWER	HWPG_VTT	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
			MAINON	S0

Thermal Follow Chart



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PROJECT : ZQTA/ZQSA			
Size	Document Number: PWR Status & GPU PWR CRL & THRM		Rev 1A
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IVY Bridge Processor (DMI,PEG,FDI)

For Sandy Bridge processor only implementation:
PROC_SELECT can be left NC.

For IVY/Sandy processor compatibility:
Needs a pull-up resistor to PCH VccDFTERM rail (1.8V) through a 2.2 K±5% pull-up resistor.
Connect to the DF_TVS of PCH though a 1K±5% series resistor.

U16A

DMI
DMI_TXN0 B27 DMI_RX#[0]
DMI_TXN1 B25 DMI_RX#[1]
DMI_TXN2 A25 DMI_RX#[2]
DMI_TXN3 B24 DMI_RX#[3]
DMI_TXP0 B28 DMI_RX[0]
DMI_TXP1 B26 DMI_RX[1]
DMI_TXP2 A24 DMI_RX[2]
DMI_TXP3 B23 DMI_RX[3]
DMI_RXN0 G21 DMI_TX#[0]
DMI_RXN1 E22 DMI_TX#[1]
DMI_RXN2 F21 DMI_TX#[2]
DMI_RXN3 D21 DMI_TX#[3]
DMI_RXP0 G22 DMI_TX[0]
DMI_RXP1 D22 DMI_TX[1]
DMI_RXP2 E20 DMI_TX[2]
DMI_RXP3 C21 DMI_TX[3]

Intel(R) FDI
FDI_TXN0 A21 FDI0_TX#[0]
FDI_TXN1 H19 FDI0_TX#[1]
FDI_TXN2 E19 FDI0_TX#[2]
FDI_TXN3 F18 FDI0_TX#[3]
FDI_TXN4 B21 FDI1_TX#[0]
FDI_TXN5 C20 FDI1_TX#[1]
FDI_TXN6 D18 FDI1_TX#[2]
FDI_TXN7 E17 FDI1_TX#[3]
FDI_TXP0 A22 FDI0_TX[0]
FDI_TXP1 G19 FDI0_TX[1]
FDI_TXP2 E20 FDI0_TX[2]
FDI_TXP3 G18 FDI0_TX[3]
FDI_TXP4 B20 FDI1_TX[0]
FDI_TXP5 C19 FDI1_TX[1]
FDI_TXP6 D19 FDI1_TX[2]
FDI_TXP7 F17 FDI1_TX[3]
FDI_FSYNC0 J18 FDI0_FSYNC
FDI_FSYNC1 J17 FDI1_FSYNC
FDI_INT H20 FDI_INT
FDI_LSYNC0 J19 FDI0_LSYNC
FDI_LSYNC1 H17 FDI1_LSYNC

eDP
eDP_COMP A18 eDP_COMPIO
eDP_ICOMPO A17 eDP_ICOMPO
INT_eDP_HPD_Q B16 eDP_HPD
EDP-AUX+ C15 eDP_AUX
EDP-AUX- D15 eDP_AUX#
EDP-ML0+ C17 eDP_TX[0]
E16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
EDP-ML0- C18 eDP_TX#[0]
E16 eDP_TX#[1]
D16 eDP_TX#[2]
E15 eDP_TX#[3]
TP59
TP58

PCI EXPRESS* - GRAPHICS
PEG_ICOMPI J22 PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22
PEG_COMP connect to PIN H22&J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.

PEG_RX#[0] K33 PEG_RX#0 [15]
PEG_RX#[1] M35 PEG_RX#1 [15]
PEG_RX#[2] L34 PEG_RX#2 [15]
PEG_RX#[3] J35 PEG_RX#3 [15]
PEG_RX#[4] J32 PEG_RX#4 [15]
PEG_RX#[5] H34 PEG_RX#5 [15]
PEG_RX#[6] H31 PEG_RX#6 [15]
PEG_RX#[7] G33 PEG_RX#7 [15]
PEG_RX#[8] G30 PEG_RX#8 [15]
PEG_RX#[9] F35 PEG_RX#9 [15]
PEG_RX#[10] E34 PEG_RX#10 [15]
PEG_RX#[11] E32 PEG_RX#11 [15]
PEG_RX#[12] D33 PEG_RX#12 [15]
PEG_RX#[13] D31 PEG_RX#13 [15]
PEG_RX#[14] B33 PEG_RX#14 [15]
PEG_RX#[15] C32 PEG_RX#15 [15]

PEG_RX[0] J33 PEG_RX0 [15]
PEG_RX[1] L35 PEG_RX1 [15]
PEG_RX[2] K34 PEG_RX2 [15]
PEG_RX[3] H35 PEG_RX3 [15]
PEG_RX[4] H32 PEG_RX4 [15]
PEG_RX[5] G34 PEG_RX5 [15]
PEG_RX[6] G31 PEG_RX6 [15]
PEG_RX[7] F33 PEG_RX7 [15]
PEG_RX[8] F30 PEG_RX8 [15]
PEG_RX[9] E35 PEG_RX9 [15]
PEG_RX[10] E33 PEG_RX10 [15]
PEG_RX[11] F32 PEG_RX11 [15]
PEG_RX[12] D34 PEG_RX12 [15]
PEG_RX[13] E31 PEG_RX13 [15]
PEG_RX[14] C33 PEG_RX14 [15]
PEG_RX[15] B32 PEG_RX15 [15]

PEG_TX#[0] M29 R_PEG_TX#0 C395 EV@0.22u/6.3V_4 PEG_TX#0 [15]
PEG_TX#[1] M32 R_PEG_TX#1 C400 PEG_TX#1 [15]
PEG_TX#[2] M31 R_PEG_TX#2 C402 PEG_TX#2 [15]
PEG_TX#[3] L32 R_PEG_TX#3 C405 PEG_TX#3 [15]
PEG_TX#[4] L29 R_PEG_TX#4 C407 PEG_TX#4 [15]
PEG_TX#[5] K31 R_PEG_TX#5 C413 PEG_TX#5 [15]
PEG_TX#[6] K28 R_PEG_TX#6 C414 PEG_TX#6 [15]
PEG_TX#[7] J30 R_PEG_TX#7 C418 PEG_TX#7 [15]
PEG_TX#[8] J28 R_PEG_TX#8 C421 PEG_TX#8 [15]
PEG_TX#[9] H29 R_PEG_TX#9 C424 PEG_TX#9 [15]
PEG_TX#[10] G27 R_PEG_TX#10 C425 PEG_TX#10 [15]
PEG_TX#[11] E29 R_PEG_TX#11 C430 PEG_TX#11 [15]
PEG_TX#[12] F27 R_PEG_TX#12 C431 PEG_TX#12 [15]
PEG_TX#[13] D28 R_PEG_TX#13 C434 PEG_TX#13 [15]
PEG_TX#[14] F26 R_PEG_TX#14 C439 PEG_TX#14 [15]
PEG_TX#[15] E25 R_PEG_TX#15 C440 PEG_TX#15 [15]

PEG_TX[0] M28 R_PEG_TX0 C398 EV@0.22u/6.3V_4 PEG_TX0 [15]
PEG_TX[1] M33 R_PEG_TX1 C401 PEG_TX1 [15]
PEG_TX[2] M30 R_PEG_TX2 C404 PEG_TX2 [15]
PEG_TX[3] L31 R_PEG_TX3 C406 PEG_TX3 [15]
PEG_TX[4] L28 R_PEG_TX4 C408 PEG_TX4 [15]
PEG_TX[5] K30 R_PEG_TX5 C409 PEG_TX5 [15]
PEG_TX[6] K27 R_PEG_TX6 C417 PEG_TX6 [15]
PEG_TX[7] J29 R_PEG_TX7 C419 PEG_TX7 [15]
PEG_TX[8] J27 R_PEG_TX8 C420 PEG_TX8 [15]
PEG_TX[9] H28 R_PEG_TX9 C422 PEG_TX9 [15]
PEG_TX[10] G28 R_PEG_TX10 C427 PEG_TX10 [15]
PEG_TX[11] E28 R_PEG_TX11 C428 PEG_TX11 [15]
PEG_TX[12] F28 R_PEG_TX12 C433 PEG_TX12 [15]
PEG_TX[13] D27 R_PEG_TX13 C436 PEG_TX13 [15]
PEG_TX[14] E26 R_PEG_TX14 C437 PEG_TX14 [15]
PEG_TX[15] D25 R_PEG_TX15 C444 PEG_TX15 [15]

Ivy Bridge_rPGA_2DPC_Rev0p61

HPD disable
This signal can be left as no connect if entire eDP interface is disabled.

DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

IVY Bridge Processor (CLK,MISC,JTAG)

wo eDP and dGPU
Connect DPLL_REF_SSCLK on Processor to GND through 1K ± 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K ± 5% resistor

U16B

MISC
[8] H_SNB_IVB# H_SNB_IVB# C26 PROC_SELECT#
TP45 SKTOCC# AN34 SKTOCC#

THERMAL
TP11 TP_CATERR# AL33 CATERR#
[32] EC_PECI AN33 PECI
[32,35] H_PROCHOT# H_PROCHOT# R124 56_4 H_PROCHOT#_R AL32 PROCHOT#
[10] PM_THRMTRIP# PM_THRMTRIP# AN32 THERMTRIP#

PWR MANAGEMENT
Intel recommended UNCOREPWRGOOD routing on one layer
[7] PM_SYNC PM_SYNC AM34 PM_SYNC
apply C5205 for nosie
C165 0.1u/10V_4
[10] H_PWRGOOD H_PWRGOOD AP33 UNCOREPWRGOOD
R116 10K_4
PM_DRAM_PWRGD_R V8 SM_DRAMPWROK
+1.05V
R107 75_4 R113 43_4 CPU_PLTRST#_R AR33 RESET#
CPU_PLTRST#
R115 *750/F_4
[9] PCI_PLTRST# R114 *1.5K/F_4
+3V
C167 0.1u/10V_4
U3 NC VCC IN GNDOUT 74LVC1G07GW
CPU_PLTRST#

Ivy Bridge_rPGA_2DPC_Rev0p61

CLOCKS
BCLK A28 CLK_CPU_BCLKP CLK_CPU_BCLKP [9]
BCLK# A27 CLK_CPU_BCLKN CLK_CPU_BCLKN [9]
DPLL_REF_CLK A16 CLK_DPLL_SSCLKP_R Ra CLK_DPLL_SSCLKP [9]
DPLL_REF_CLK# A15 CLK_DPLL_SSCLKN_R R440 1V@0_4P2R CLK_DPLL_SSCLKN [9]
Rb R442 DO@1K_4 +1.05V
Rc R438 DO@1K_4

DDR3 MISC
SM_DRAMRST# R8 CPU_DRAMRST# CPU_DRAMRST# [4]
SM_RCOMP[0] AK1 SM_RCOMP_0 R173 140/F_4
SM_RCOMP[1] A5 SM_RCOMP_1 R458 25.5/F_4
SM_RCOMP[2] A4 SM_RCOMP_2 R460 200/F_4
CRB 1.0 : SM_RCOMP[2..0] W:20mils, S:15mils, L 500mils

	EV	UMA/OPT.
Ra	NA	0 ohm
Rb	1K	NA
Rc	1K	NA

JTAG & BPM
PRDY# AP29 XDP_PRDY#
PREQ# AP27 XDP_PREQ#
TCK AR26 XDP_TCLK
TMS AR27 PCH_JTAG_TMS
TRST# AP30 XDP_TRST#
TDI AR28 PCH_JTAG_TDI
TDO AP26 PCH_JTAG_TDO
DBR# AL35 XDP_DBRST# [7]
BPM#[0] AT28 XDP_BPM0
BPM#[1] AP29 XDP_BPM1
BPM#[2] AR30 XDP_BPM2
BPM#[3] AT30 XDP_BPM3
BPM#[4] AP32 XDP_BPM4
BPM#[5] AR31 XDP_BPM5
BPM#[6] AT31 XDP_BPM6
BPM#[7] AR32 XDP_BPM7
TP53 TP18 TP20 TP19 TP12 TP56 TP54 TP55 TP51 TP52 TP49 TP47 TP50 TP46
For XDP

CRB 1.0 : change to +3V(S0)
+3V_S5
C516 0.1u/10V_4
U18 74AHC1G09
[7] SYS_PWROK
[7] PM_DRAM_PWRGD
PM_DRAM_PWRGD_Q
+1.5V_CPU
R461 200/F_4
R459 130/F_4 PM_DRAM_PWRGD_R
R462 *39_4
Q30 *2N7002K
MAINON_ON_G MAINON_ON_G [5,41]

FDI Disabling (Discrete Only)

9/26 add

FDI_INT
R444 DO@0_4 FDI_FSYNC0
R446 DO@0_4 FDI_FSYNC1
R443 DO@0_4 FDI_LSYNC0
FDI_LSYNC1
R441 DO@1K/F_4
R447 DO@1K/F_4
FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

DP & PEG Compensation

+1.05V
Routed within 25 mils
R433 24.9/F_4 eDP_COMP
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V
Routed within 500 mils
R439 24.9/F_4 PEG_COMP
PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms
PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up(CPU)

+1.05V
H_PROCHOT# R122 62_4
PCH_JTAG_TDO R134 51_4
PCH_JTAG_TMS R135 51_4
PCH_JTAG_TDI R430 51_4
XDP_PREQ# R132 *51_4
XDP_TCLK R137 51_4
XDP_TRST# R128 51_4
9/27 modify

[7,35] IMVP_PWRGD
Q4 FDV301N
R86 1K_4
Q5 MMBT3904
PM_THRMTRIP#
SYS_SHDN# [34,41]
[5,7,8,9,11,22,32,35,36,40,41] +1.05V
[7,8,9,10,11,13,14,19,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V

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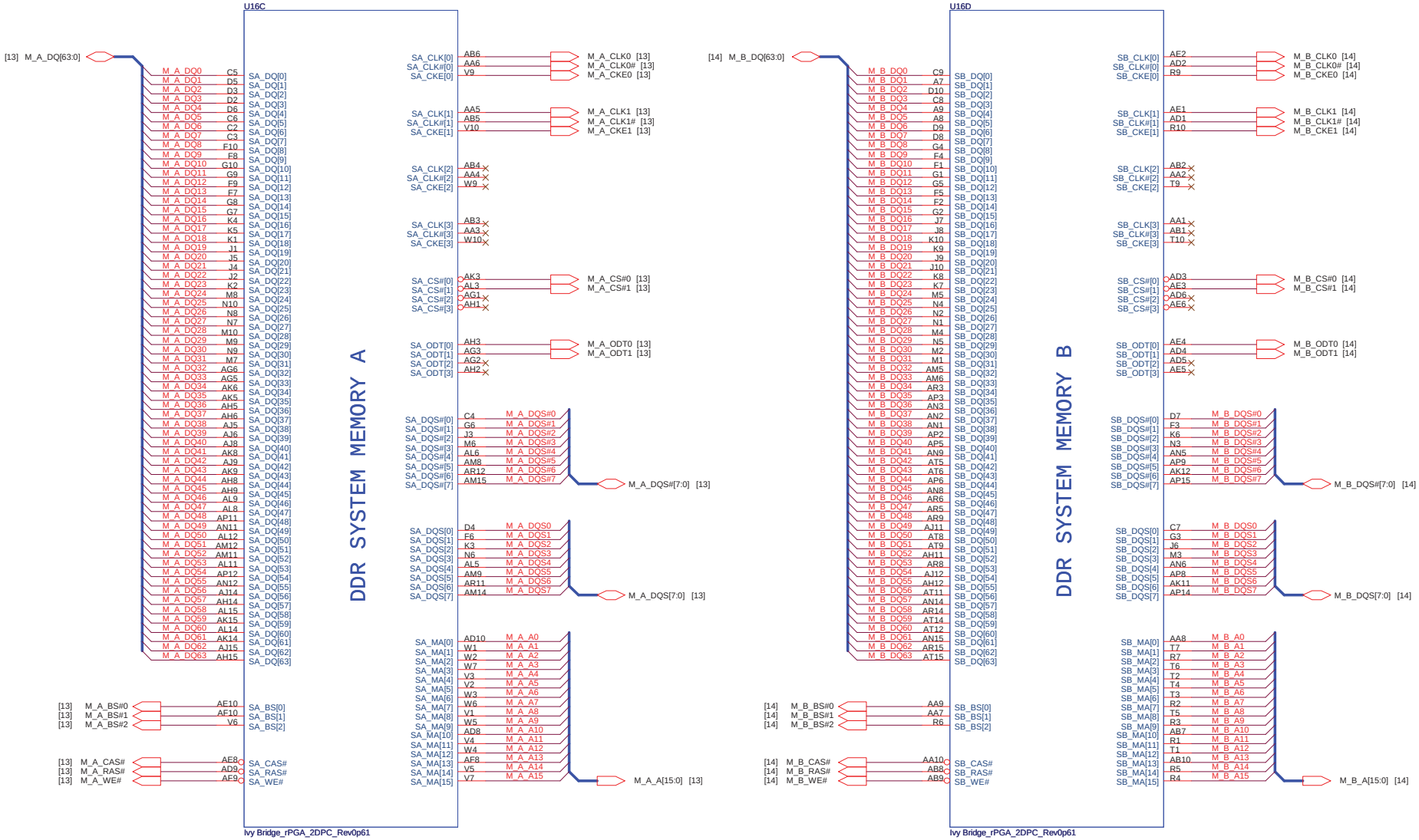
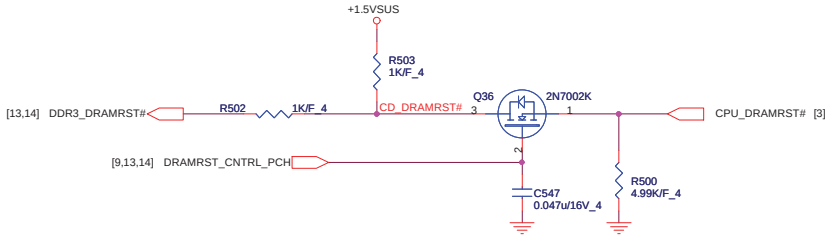
IVY Bridge Processor (DDR3)





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IVY Processor (POWER)

IVY Bridge Processor (GRAPHIC POWER)

POWER

0929 change value by CRB

CPU Core Power
IVY 45W:TDC 52A

IVY SPEC
22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4
total : 10uF x 10 , RSVD x 1
total : 22uF x 16 , RSVD x 3
tatal : 470u x 4, RSVD x2

SNB : Spec	Cose down
470uF/4mohm x 4	330uF x2
22uF x 16	22uF x 4
10uF x 10	10uF x 20 reserved x 5

CPU VTT
IVY 45W:8.5A

SNB : Spec	Cose down
330uF/6mohm x 2	330uF x1
22uF x 12	22uF x 2
22uF x 7 (Non-stuff)	10uF x 10 reserved x 4

CPU VGT
IVY 45W:TDC 38A

Spec	Cose down
470uF/4mohm x 2	330uF x1
22uF x 12	22uF x 4
	10uF x 10

IVY SPEC
22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

U16F

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

U16G

SENSE LINES

VREF

DDR3 - 1.5V RAILS

GRAPHICS

SA RAIL

1.8V RAIL

MISC

IVY SPEC
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

	DIS. VGA	UMA/ Optimus
Ra	0 ohm	NA

CPU VCCPL
IVY 45W:1.5A

Spec	Real
330uF/7mohm x 1	10uF x 1
10uF x 1	1uF x 2
1uF x 2	

IVY SPEC
330uF x1, 10uF_8 x1, 1uF_4 x2 Socket BOT edge.

10uF (Reserved)

4.5A

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK
Remove PU resistor 54.9/F, stuff at IMVP7 page

SVID DATA
Remove PU resistor 130/F, stuff at IMVP7 page

SVID ALERT

Place PU resistor close to CPU

Trace Route to Power IC area.

IVY SPEC
330uF x1, 10uF_8 x1 Socket BOT edge, 10uF_8 x2 Socket BOT cavity.

CPU SA
IVY 45W: 6A

Spec	Real
330uF/7mohm x 1	10uF x 3
10uF x 3	

CPU MCH
IVY 45W: 5A

Spec	
330uF/6mohm x 1	
10uF x 6	
Real	
10uF x 8	

IVY SPEC
330uF x1, 10uF_8 x6 Socket BOT edge.

10 mil

For M3 solution need Rb4, Rd1 W/O M3 then NC ball B4 and D1

Voltage selection for VCCIO:
this pin must be pulled high on the motherboard

On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

Ivy Bridge_rPGA_2DPC_Rev0p61

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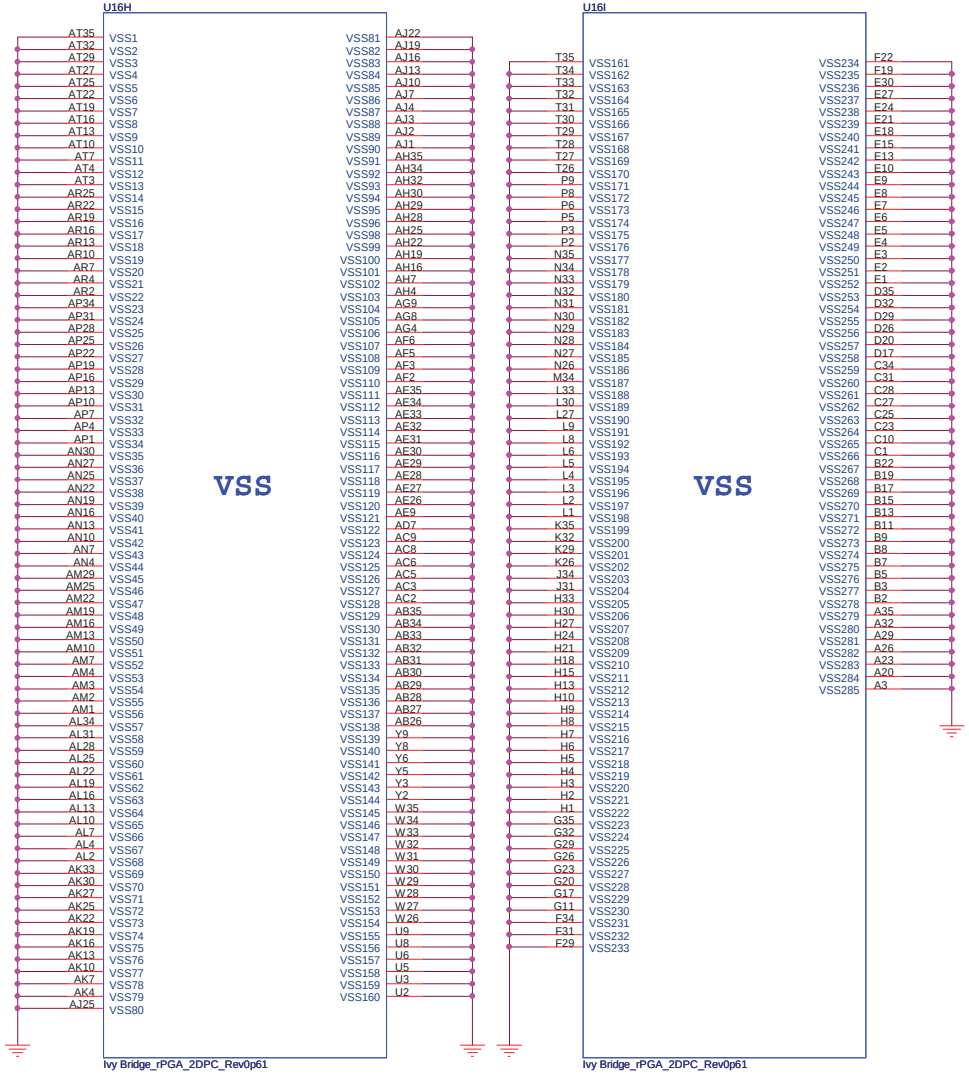
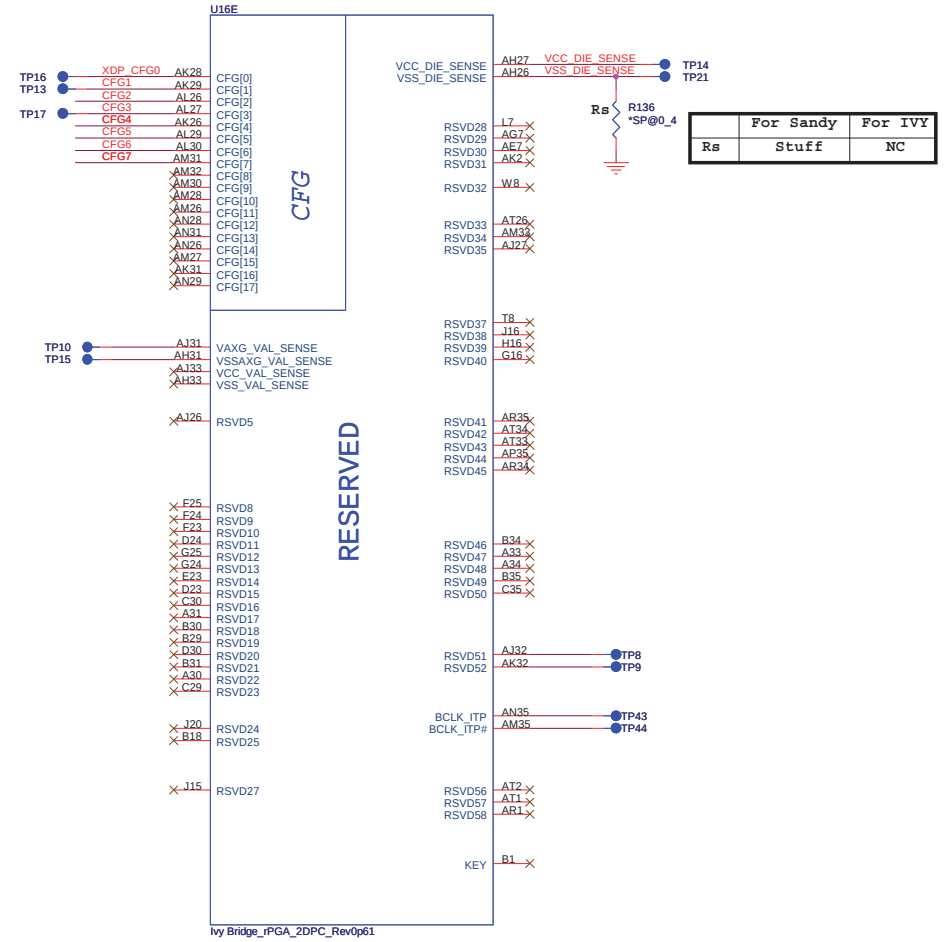
IVY Bridge Processor (GND)



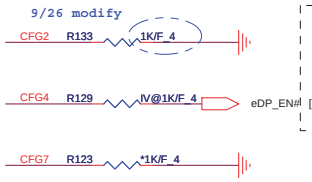
IVY Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	**Lane Reversed**
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

CFG5 R130 *1K/F_4
CFG6 R127 *1K/F_4

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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[3,5,8,9,11,22,32,35,36,40,41] +1.05V
[3,8,9,10,11,15,28,30,31,34,35,36,41,42] +3V_S5

CPT/PPT (DMI,FDI,PM)

U20C

DMI_RXN0 [3] BC24 DMIDRXN
DMI_RXN1 [3] BE20 DMI1RXN
DMI_RXN2 [3] BG18 DMI2RXN
DMI_RXN3 [3] BG20 DMI3RXN

DMI_RXP0 [3] BE24 DMIDRXP
DMI_RXP1 [3] BC20 DMI1RXP
DMI_RXP2 [3] BJ18 DMI2RXP
DMI_RXP3 [3] BJ20 DMI3RXP

DMI_TXN0 [3] AW24 DMI0TXN
DMI_TXN1 [3] AW20 DMI1TXN
DMI_TXN2 [3] BB18 DMI2TXN
DMI_TXN3 [3] AV18 DMI3TXN

DMI_TXP0 [3] AY24 DMI0TXP
DMI_TXP1 [3] AY20 DMI1TXP
DMI_TXP2 [3] AY18 DMI2TXP
DMI_TXP3 [3] AU18 DMI3TXP

DMI_ZCOMP BJ24
+1.05V R521 49.9/F_4 DMI_COMP BG25 DMI_IRCOMP
R527 750/F_4 BH21 DMI2RBIAS

DMI

FDI_RXN0 BJ14 FDI_TXN0 [3]
FDI_RXN1 AY14 FDI_TXN1 [3]
FDI_RXN2 BE14 FDI_TXN2 [3]
FDI_RXN3 BH13 FDI_TXN3 [3]
FDI_RXN4 BC12 FDI_TXN4 [3]
FDI_RXN5 BJ12 FDI_TXN5 [3]
FDI_RXN6 BG10 FDI_TXN6 [3]
FDI_RXN7 BG9 FDI_TXN7 [3]

FDI_RXP0 BG14 FDI_TXP0 [3]
FDI_RXP1 BB14 FDI_TXP1 [3]
FDI_RXP2 BF14 FDI_TXP2 [3]
FDI_RXP3 BG13 FDI_TXP3 [3]
FDI_RXP4 BE12 FDI_TXP4 [3]
FDI_RXP5 BG12 FDI_TXP5 [3]
FDI_RXP6 BJ10 FDI_TXP6 [3]
FDI_RXP7 BH9 FDI_TXP7 [3]

FDI_INT AW16 FDI_INT [3]
FDI_FSYNC0 AV12 FDI_FSYNC0 [3]
FDI_FSYNC1 BC10 FDI_FSYNC1 [3]
FDI_LSYNC0 AV14 FDI_LSYNC0 [3]
FDI_LSYNC1 BB10 FDI_LSYNC1 [3]

FDI

DSWVRMEN A18 DSWVREN [8]
SUS_PWR_ACK R539 *0_4 SUSACK#_R C12 SUSACK#
[3] XDP_DBRST# XDP_DBRST# K3 SYS_RESET#
C607 *1u/10V_6
SYS_PWROK P12 SYS_PWROK
R583 *0_4 L22 PWROK
PWROK_EC L10 APWROK
[3] PM_DRAM_PWRGD PM_DRAM_PWRGD B13 DRAMPWROK
[32] PCH_RSMRST# PCH_RSMRST# C21 RSMRST#
SUS_PWR_ACK K16 SUSWARN#/SUSPWRDNACK/GPIO30
[32] DNBSWON# E20 PWRBTN#
AC_PRESENT H20 ACPRESENT / GPIO31
PM_BATLOW# E10 BATLOW# / GPIO72
PM_R# A10 R#

DPWROK F22 PCH_RSMRST#
WAKE# B9 PCIE_WAKE# PCIE_WAKE# [28]
CLKRUN# / GPIO32 N3 CLKRUN# CLKRUN# [32]
SUS_STAT# / GPIO61 G8 SUS_STAT# T15
SUSCLK / GPIO62 N14 PCH_SUSCLK T12
SLP_S5# / GPIO63 D10 PCH_SLP_S5# T14
SLP_S4# H4 SUSC# [32]
SLP_S3# F4 SUSB# [32]
SLP_A# G10 SLP_A# SLP_A# [32]
SLP_SUS# G16 SLP_SUS# T10
PMSYNCH AP14 PM_SYNC [3]
SLP_LAN# / GPIO29 K14 SLP_LAN#

System Power Management

+3V_S5 +3V_S5 +3V_S5 +3V_S5 +3V DSW +3V_S5 +3V_S5

10/31 modify

PANTHER POINT

CPT/PPT (LVDS,DDI)

U20D

[22] INT_LVDS_BLON J47 L_BKLTEN
[22] INT_LVDS_DIGON M45 L_VDD_EN
[22] INT_LVDS_BRIGHT P45 L_BKLTCTL
[22] INT_LVDS_EDIDCLK T40 L_DDC_CLK
[22] INT_LVDS_EDIDDATA K47 L_DDC_DATA
+3V R164 2.2K_4 R188 2.2K_4 T45 L_CTRL_CLK P39 L_CTRL_DATA
R186 2.37K/F_4 T7 AF37 LVD_IBG AF36 LVD_VBG
AE48 LVD_VREFH AE47 LVD_VREFL

[22] INT_TXLCLKOUT- AK39 LVDSA_CLK#
[22] INT_TXLCLKOUT+ AK40 LVDSA_CLK
[22] INT_TXLOUT0- AN48 LVDSA_DATA#0
[22] INT_TXLOUT1- AM47 LVDSA_DATA#1
[22] INT_TXLOUT2- AK47 LVDSA_DATA#2
AJ48 LVDSA_DATA#3
[22] INT_TXLOUT0+ AN47 LVDSA_DATA0
[22] INT_TXLOUT1+ AM49 LVDSA_DATA1
[22] INT_TXLOUT2+ AK49 LVDSA_DATA2
AJ47 LVDSA_DATA3
AF40 LVDSB_CLK#
AF39 LVDSB_CLK
AH45 LVDSB_DATA#0
AH47 LVDSB_DATA#1
AF49 LVDSB_DATA#2
AF45 LVDSB_DATA#3
AH43 LVDSB_DATA0
AH49 LVDSB_DATA1
AF47 LVDSB_DATA2
AF43 LVDSB_DATA3

LVDS

[22] INT_CRT_BLU N48 CRT_BLUE
[22] INT_CRT_GRN P49 CRT_GREEN
[22] INT_CRT_RED T49 CRT_RED
[22] INT_CRT_DDCCLK T39 CRT_DDC_CLK
[22] INT_CRT_DDCDAT M40 CRT_DDC_DATA
[22] INT_HSYNC R126 IV@33_4 INT_CRT_HSYNC_R M47 CRT_HSYNC
[22] INT_VSYNC R125 IV@33_4 INT_CRT_VSYNC_R M49 CRT_VSYNC
DAC_IREF T43 DAC_IREF
T42 CRT_IRTN
R187 1K/F_4

CRT

The required series-resistors are:
• Direct Connect - 33 Ω
• Docking Topology - 20 Ω

R place close to PCH
R483 IV@150/F_4 INT_CRT_BLU
R482 IV@150/F_4 INT_CRT_GRN
R484 IV@150/F_4 INT_CRT_RED

PANTHER POINT

Digital Display Interface

SDVO_TVCLKINN AP43
SDVO_TVCLKINP AP45
SDVO_STALLN AM42
SDVO_STALLP AM43
SDVO_INTN AP39
SDVO_INTP AP40
SDVO_CTRLCLK P38 HDMI_DDCCLK_SW [23]
SDVO_CTRLDATA M39 HDMI_DDCDATA_SW [23]

DDPB_AUXN AT49
DDPB_AUXP AT47
DDPB_HPD AT40 HDMI_HP [23]
DDPB_0N AV42 INT_HDMITX2N_R RP18 INT_HDMITX2N [23]
DDPB_0P AV40 INT_HDMITX2P_R INT_HDMITX2P [23]
DDPB_1N AV45 INT_HDMITX1N_R RP19 INT_HDMITX1N [23]
DDPB_1P AV46 INT_HDMITX1P_R INT_HDMITX1P [23]
DDPB_2N AU48 INT_HDMITX0N_R RP20 INT_HDMITX0N [23]
DDPB_2P AU47 INT_HDMITX0P_R INT_HDMITX0P [23]
DDPB_3N AV47 INT_HDMICLK-_R RP21 INT_HDMICLK- [23]
DDPB_3P AV49 INT_HDMICLK+_R INT_HDMICLK+ [23]
IV@0_4P2R

INT. HDMI

DDPC_CTRLCLK P46 DDPC_HPD_PU
DDPC_CTRLDATA P42

DDPC_AUXN AP47
DDPC_AUXP AP49
DDPC_HPD AT36
DDPC_0N AY47
DDPC_0P AY49
DDPC_1N AY43
DDPC_1P AY45
DDPC_2N BA47
DDPC_2P BA48
DDPC_3N BB47
DDPC_3P BB49

DDPD_CTRLCLK M43 DDPD_HPD_PU
DDPD_CTRLDATA M36

DDPD_AUXN AT45
DDPD_AUXP AT43
DDPD_HPD BH43
DDPD_0N BB43
DDPD_0P BB45
DDPD_1N BF44
DDPD_1P BE44
DDPD_2N BF42
DDPD_2P BE42
DDPD_3N BJ42
DDPD_3P BG42

DDPC_HPD_PU R169 *2.2K_4
DDPD_HPD_PU R197 *2.2K_4
0 : Port not detected

PCH Pull-high/low(CLG)

+3V
CLKRUN# R584 8.2K_4
XDP_DBRST# R567 4.99K/F_4
R554 *1K_4
PCH_RSMRST# R219 10K_4
SYS_PWROK R601 *10K_4

+3V_S5
CRB 1.0 change R8315 to 1K
PM_R# R545 10K_4
PM_BATLOW# R282 8.2K_4
PCIE_WAKE# R261 10K_4
SLP_LAN# R230 *10K_4
SUS_PWR_ACK R538 10K_4
AC_PRESENT R220 10K_4
PM_DRAM_PWRGD R232 200/F_4
wo S3 leakage, remove R

System PWR_OK(CLG)

IMVP_PWRGD PU +3V
PWROK_EC PD
so AND gate output dont need PD again

+3V_S5
C629 *0.1u/10V_4
to PCH Pin12, XDP and EE debug
U24
[3] SYS_PWROK SYS_PWROK
TC7SH08FU
IMVP_PWRGD [3,35]
PWROK_EC [32]
R594 100K_4

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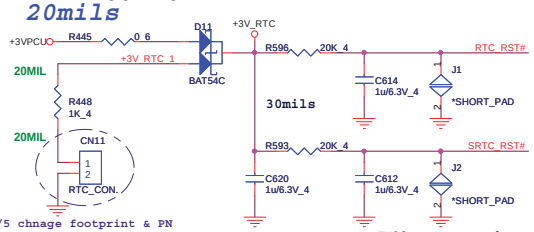
RTC Circuitry(RTC)

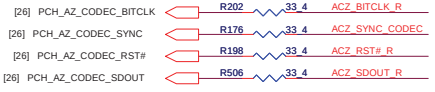
20mils



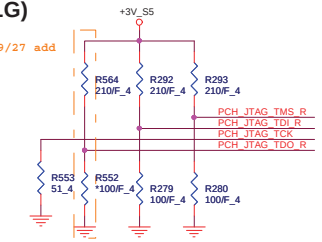
10/5 chnage footprint & PN

CN13 battery
DFWF02MS118 AHL03003022
AHL03003024

HDA Bus(CLG)

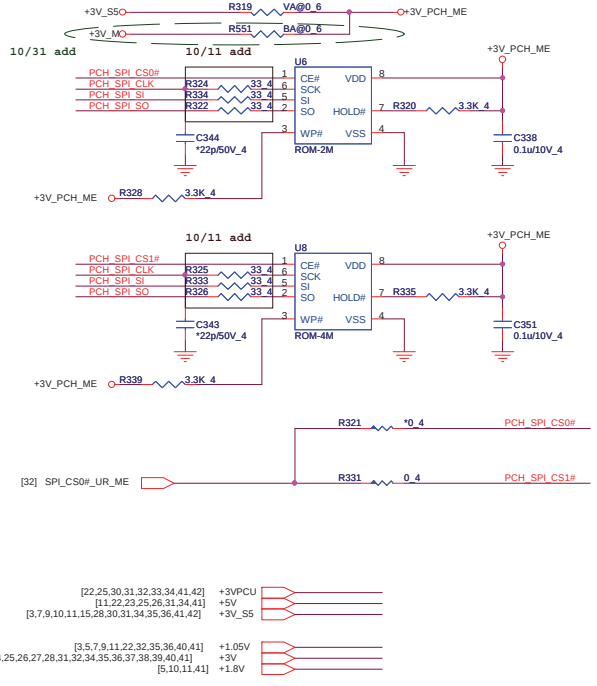


PCH JTAG Debug (CLG)



PCH Dual SPI (CLG) (Default for WIN8)

W25Q32BVSSIG / AKE391P0N00------>4MB
W25Q16BVSSIG / AKE38FP0N01------>2MB
for BA W25Q64BVSSIG / AKE3EFP0N00------>8MB

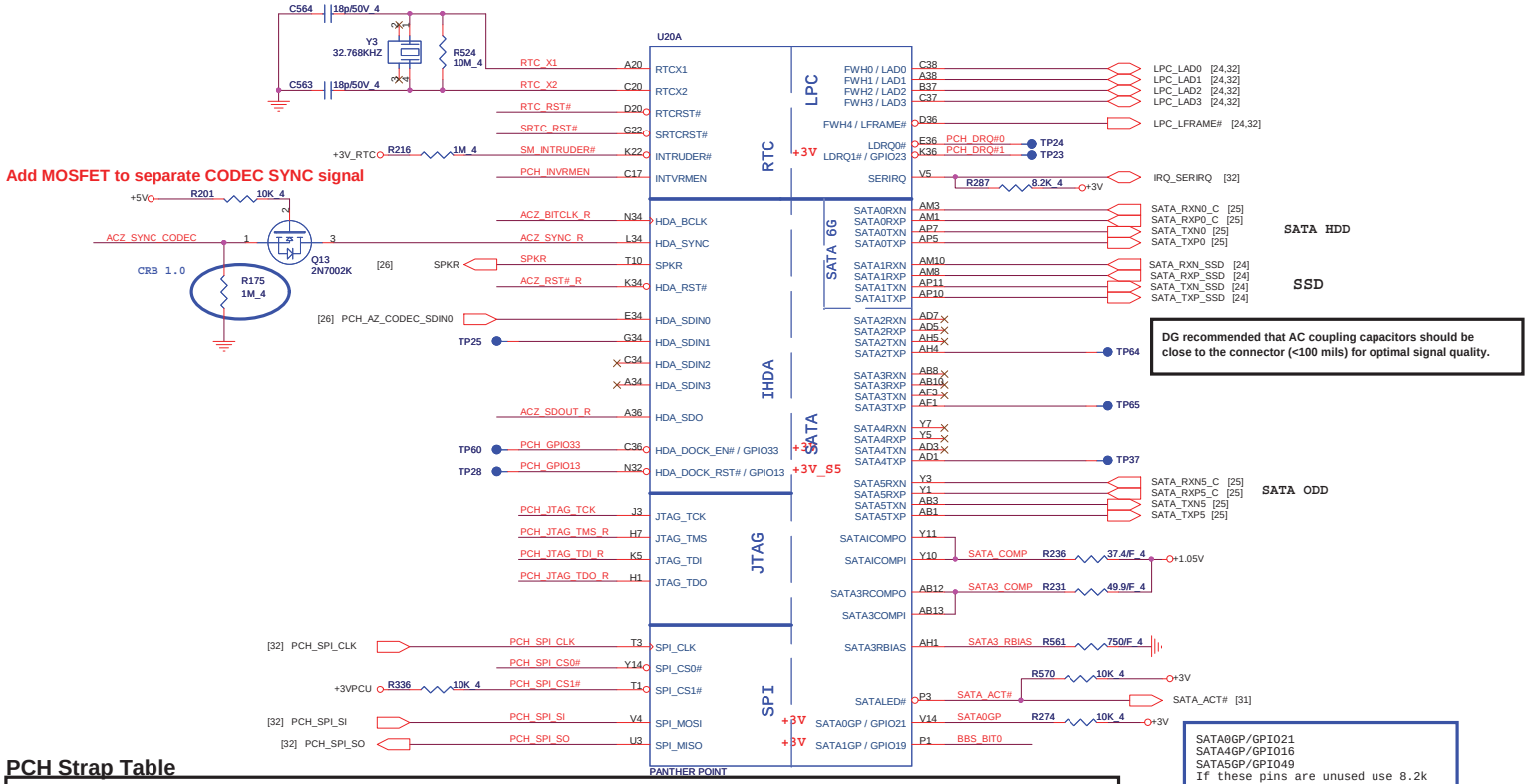


[22,25,30,31,32,33,34,41,42] +3VPCU
[11,22,23,25,26,31,34,41] +5V
[3,7,9,10,11,15,28,30,31,34,35,36,41,42] +3V_S5

[3,5,7,9,11,22,32,35,36,40,41] +1.05V
[23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V
[5,10,11,41] +1.8V

PCH2 (CLG)

CPT/PPT (HDA,JTAG,SATA)

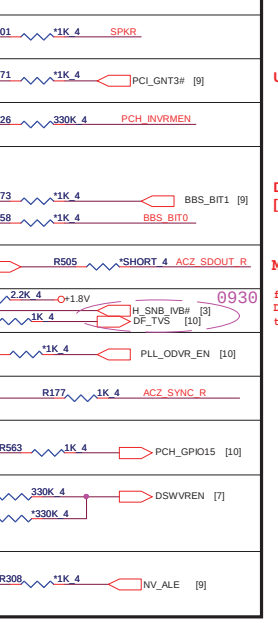


DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

SATA0GP/GPIO21
SATA4GP/GPIO16
SATA5GP/GPIO49
If these pins are unused use 8.2k to 10k pull-up to +Vcc3_3 or 8.2k to 10k pull-down to ground

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI *; 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)



Used as GPIO only. at chklist 1.2

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

ME_WR default EC setting folating

for future CPU, Sandy Bridge NC
DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhm ±5% - R8361 change to 0 or not??

Needs to be pulled High for Huron River platform. chklist 1.2

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CPT/PPT (PCI,USB,NVRAM)

U20E

PANTHER POINT

TX AC cap place at connector side, AC cap to connector < 400mils

USB3.0

[30] USB30_RX3- → TP62 → USB30_RX3- / USB30_RX4-
[30] USB30_RX3+ → TP61 / TP30 → USB30_RX3+ / USB30_RX4+ / USB30_TX1-
[30] USB30_TX3- → TP26 / TP29 → USB30_TX3- / USB30_TX4- / USB30_TX1+
[30] USB30_TX3+ → TP27 → USB30_TX3+ / USB30_TX4+

Port1 and port9 can be used on debug mode

XHCI for USBP0-3

EHCI1

- T41 / T40 Reserve for USB I/O function
- USBP1- / USBP1+ USB/B-USB1-1/USB debug
- USBP2- / USBP2+ MB USB
- USBP3- / USBP3+ Mini-SSD
- USBP4- / USBP4+ BLUETOOTH
- T39 / T38 Reserve for SIM card

USB port6/7 may not be available on all PCH sku (HM55 support 12port only)

EHCI2

- USBP8- / USBP8+ Camera
- USBP9- / USBP9+ USB/B-USB1-2
- USBP10- / USBP10+ Mini Card (WLAN)
- Reserve for card reader
- Reserve for Touch pad
- Reserve for FP

USB_BIAS R507 22.6/F_4

PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD# → PIRQA# PIRQB# PIRQC# PIRQD#

dGPU_EDIDSEL# dGPU_SELECT# REQ#3 → REQ1# / GPIO50 +3V, REQ2# / GPIO52 +3V, REQ3# / GPIO54 +3V

BBS_BIT1 BOARD_ID2 PCI_GNT3# → GNT1# / GPIO51 +3V, GNT2# / GPIO53 +3V, GNT3# / GPIO55 +3V

11/2 modify

G_SENSOR_INT# PCH [25] → PIRQE# / GPIO2 +3V
dGPU_PWR_EN [40] → PIRQF# / GPIO3 +3V
DGPU_HOLD_RST# [15] → PIRQG# / GPIO4 +3V
EXTTS_SNI_DRV1_PCH → PIRQH# / GPIO5 +3V

TP32 PCI_PME# → PME#
[3] PCI_PLTRST# → PCI_PLTRST# → PLTRST#

TP22 CLK_PCI_FB → R485 22_4 CLK_PCI_FB_C
[24] CLK_LPC_DEBUG → R183 22_4 CLK_LPC_DEBUG_C
[32] CLK_PCI_775 → R184 22_4 CLK_PCI_775_C

CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4 → H49 H43 J46 K42 H40

OC0# / GPIO59 +3V_S5, OC1# / GPIO40 +3V_S5, OC2# / GPIO41 +3V_S5, OC3# / GPIO42 +3V_S5, OC4# / GPIO43 +3V_S5, OC5# / GPIO9 +3V_S5, OC6# / GPIO10 +3V_S5, OC7# / GPIO14 +3V_S5

USB_OC0# [30] USB_OC1# [30]

NV_ALE [8]

CPT/PPT (PCI-E,SMBUS,CLK)

U20B

PANTHER POINT

LAN

[28] PCIE_RX3- / [28] PCIE_RX3+ → C252 0.1u/10V_4 PCIE_TXN3_C, C249 0.1u/10V_4 PCIE_TXP3_C
[28] PCIE_TX3- / [28] PCIE_TX3+

Wireless

[24] PCIE_RX8- / [24] PCIE_RX8+ → C250 0.1u/10V_4 PCIE_TXN8_C, C253 0.1u/10V_4 PCIE_TXP8_C
[24] PCIE_TX8- / [24] PCIE_TX8+

SMBUS

+3V_S5 SMBALERT# / GPIO11 → E12 SMBALERT#
SMBCLK → H14 SMB_PCH_CLK
SMBDATA → C9 SMB_PCH_DAT

+3V_S5 SML0ALERT# / GPIO60 → A12 DRAMRST_CNTRL_PCH → DRAMRST_CNTRL_PCH [4,13,14]
SML0CLK → C8 SMB_ME0_CLK
SML0DATA → G12 SMB_ME0_DAT — For LAN

+3V_S5 SML1ALERT# / PCHHOT# / GPIO74 → C13 SML1ALERT# R R536 *0_4 → SML1ALERT# [10,31]
+3V_S5 SML1CLK / GPIO58 → E14 SMB_ME1_CLK
+3V_S5 SML1DATA / GPIO75 → M16 SMB_ME1_DAT — For EC

Controller Link

CL_CLK1 → M7 CL_CLK1 → TP33
CL_DATA1 → T11 CL_DATA1 → TP36
CL_RST1# → P10 CL_RST1# → TP35

CLOCKS

+3V_S5 PEG_A_CLKRQ# / GPIO47 → M10 CLK_PEGA_REQ# → CLK_PEGA_REQ# [15]

CLKOUT_PEG_A_N AB37 → CLK_PCIE_VGA# [15]
CLKOUT_PEG_A_P AB38 → CLK_PCIE_VGA [15]

CLKOUT_DMI_N AV22 → CLK_CPU_BCLKN [3]
CLKOUT_DMI_P AU22 → CLK_CPU_BCLKP [3]

CLKOUT_DP_N AM12 → CLK_DPLL_SSCLKN [3]
CLKOUT_DP_P AM13 → CLK_DPLL_SSCLKP [3]

CLKIN_DMI_N BE18 → CLK_BUF_PCIE_3GPLLN
CLKIN_DMI_P BE18 → CLK_BUF_PCIE_3GPLLP

CLKIN_GND1_N BJ30 → CLK_BUF_BCLKN
CLKIN_GND1_P BG30 → CLK_BUF_BCLKP

CLKIN_DOT_96N G24 → CLK_BUF_DREFCLKN
CLKIN_DOT_96P E24 → CLK_BUF_DREFCLKP

CLKIN_SATA_N AK7 → CLK_BUF_DREFSSCLKN
CLKIN_SATA_P AK5 → CLK_BUF_DREFSSCLKP

REFCLK14IN K45 → CLK_PCI_14M
CLKIN_PCILOOPBACK H45 → CLK_PCI_FB

XTAL25_IN V47 → XTAL25_IN
XTAL25_OUT V49 → XTAL25_OUT
C538 27p/50V_4, Y2 25MHz, R486 1M_4, C539 27p/50V_4

XCLK_RCOMP Y47 → XCLK_RCOMP R478 90.9/F_4 → +1.05V

PCIE_CLK_USB30_REQ# → J2 → PCIECLKRQ0# / GPIO73 +3V_S5
PCIE_CLKREQ1# → M1 → PCIECLKRQ1# / GPIO18 +3V
PCIE_CLKREQ2# → V10 → PCIECLKRQ2# / GPIO20 +3V
PCIE_CLKREQ3# → A8 → PCIECLKRQ3# / GPIO25 +3V_S5
PCIE_CLKREQ4# → L12 → PCIECLKRQ4# / GPIO26 +3V_S5
PCIE_CLKREQ5# → L14 → PCIECLKRQ5# / GPIO44 +3V_S5
PCIE_CLKREQ6# → T13 → PCIECLKRQ6# / GPIO45 +3V_S5
CLK_PCIE_REQ7# → K12 → PCIECLKRQ7# / GPIO46 +3V_S5

CLKOUT_PCIE0N Y40, CLKOUT_PCIE0P Y39
CLKOUT_PCIE1N AB49, CLKOUT_PCIE1P AB47
CLKOUT_PCIE2N AA48, CLKOUT_PCIE2P AA47
CLKOUT_PCIE3N Y37, CLKOUT_PCIE3P Y36
CLKOUT_PCIE4N Y43, CLKOUT_PCIE4P Y45
CLKOUT_PCIE5N V45, CLKOUT_PCIE5P V46
CLKOUT_PEG_B_N AB42, CLKOUT_PEG_B_P AB40 → PEG_B_CLKRQ# / GPIO56 +3V_S5
CLKOUT_PCIE6N V40, CLKOUT_PCIE6P V42
CLKOUT_PCIE7N V38, CLKOUT_PCIE7P V37
CLKOUT_ITPXDP_N AK14, CLKOUT_ITPXDP_P AK13

[24] CLK_PCH_SRC5# / [24] CLK_PCH_SRC5
[24] PCIE_CLK_REQ5#
[28] CLK_PCIE_LOM# / [28] CLK_PCIE_LOM
[28] CLK_PCIE_LAN_REQ#
T6 CLK_PCH_SRC6P
T8 CLK_PCH_SRC7P
T11 CLK_ITPN / T13 CLK_ITPP

For XDP

CLKOUTFLEX0 / GPIO64 → K43 SKU_ID1
CLKOUTFLEX1 / GPIO65 → F47 CLK_FLEX1 → T5
CLKOUTFLEX2 / GPIO66 → H47 BOARD_ID4 [10,31]
CLKOUTFLEX3 / GPIO67 → K49 48M_CLK_CR → T37

PLTRST#(CLG)

+3V, 10/11 modify, C605 0.1u/10V_4
PCI_PLTRST# → U22 TC7SH08FU → PLTRST# [15,24,28,32]
R582 100K_4

PCI/USBOC# Pull-up(CLG)

+3V_S5 R534 10K 10P8R: USB_OC1# USB_OC4# USB_OC2# USB_OC3# ↔ USB_OC6# USB_OC0# USB_OC7# USB_OC5#

PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD# → R161 R191 R469 R170 8.2K_4

11/2 modify

R479 10K_10P8R: G_SENSOR_INT# PCH, REQ#3, dGPU_PWR_EN ↔ DGPU_HOLD_RST#, EXTTS_SNI_DRV1_PCH, dGPU_EDIDSEL#, dGPU_SELECT#

+3V R495 *SP@1K_4 R496 SP@100K_4 → dGPU_PW_CTRL# [10]
+3V R166 OP@10K_4 R162 SP@10K_4 → SKU_ID1
+3V R571 EV@10K_4 R559 SP@10K_4 → SKU_ID0 [10]

	dGPU_PW_CTRL# (GPIO68) CTL : dGPU_VRON	SKU_ID1 (GPIO54)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
dGPU Only	0	0	1	GPU	Hidden	GPU boot
Switchable (Mux)				UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

dGPU_PW_CTRL#
1 = GPU power is control by H/W (pure Discrete SKU)
0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
--->(Default)

CLK_REQ/Strap Pin(CLG)

+3V_S5: R565 R549 R294 R225 R306 R278 R281 10K_4 → PCIE_CLK_USB30_REQ#, PCIE_CLKREQ3#, PCIE_CLKREQ4#, PCIE_CLKREQ5#, CLK_PCIE_LAN_REQ#, CLK_PCIE_REQ6#, CLK_PCIE_REQ7#
+3V: R556 R273 10K_4 → PCIE_CLKREQ1#, PCIE_CLK_REQ2#

9/26 modify: R586 *10K_4 CLK_PEGA_REQ#

CLK_BUF_BCLKN R514, CLK_BUF_BCLKP R513 10K_4

CLK_BUF_PCIE_3GPLLN R532, CLK_BUF_PCIE_3GPLLP R531, CLK_BUF_DREFCLKN R211, CLK_BUF_DREFCLKP R205, CLK_BUF_DREFSSCLKN R240, CLK_BUF_DREFSSCLKP R244, CLK_PCH_14M R163 10K_4

CLOCK TERMINATION for FCIM

SMBus(EC)

+3V_S5 R149 2.2K_4 Q7 2N7002K: [32] 2ND_MBCLK ↔ SMB_ME1_CLK
+3V_S5 R150 2.2K_4 Q8 2N7002K: [32] 2ND_MBDATA ↔ SMB_ME1_DAT

SMBus(PCH)

S5: +3V R603 4.7K_4 Q41 2N7002K: SMB_PCH_DAT ↔ CLK_SDATA [13,14,24,25,31]
S0: +3V R602 4.7K_4 Q40 2N7002K: SMB_PCH_CLK ↔ CLK_SCLK [13,14,24,25,31]

+3V_S5: R246 1K_4 → DRAMRST_CNTRL_PCH
R295 10K_4 → SMBALERT#
R590 2.2K_4 → SMB_PCH_CLK
R591 2.2K_4 → SMB_PCH_DAT
R296 2.2K_4 → SMB_ME0_CLK
R283 2.2K_4 → SMB_ME0_DAT
R537 10K_4 → SML1ALERT# R

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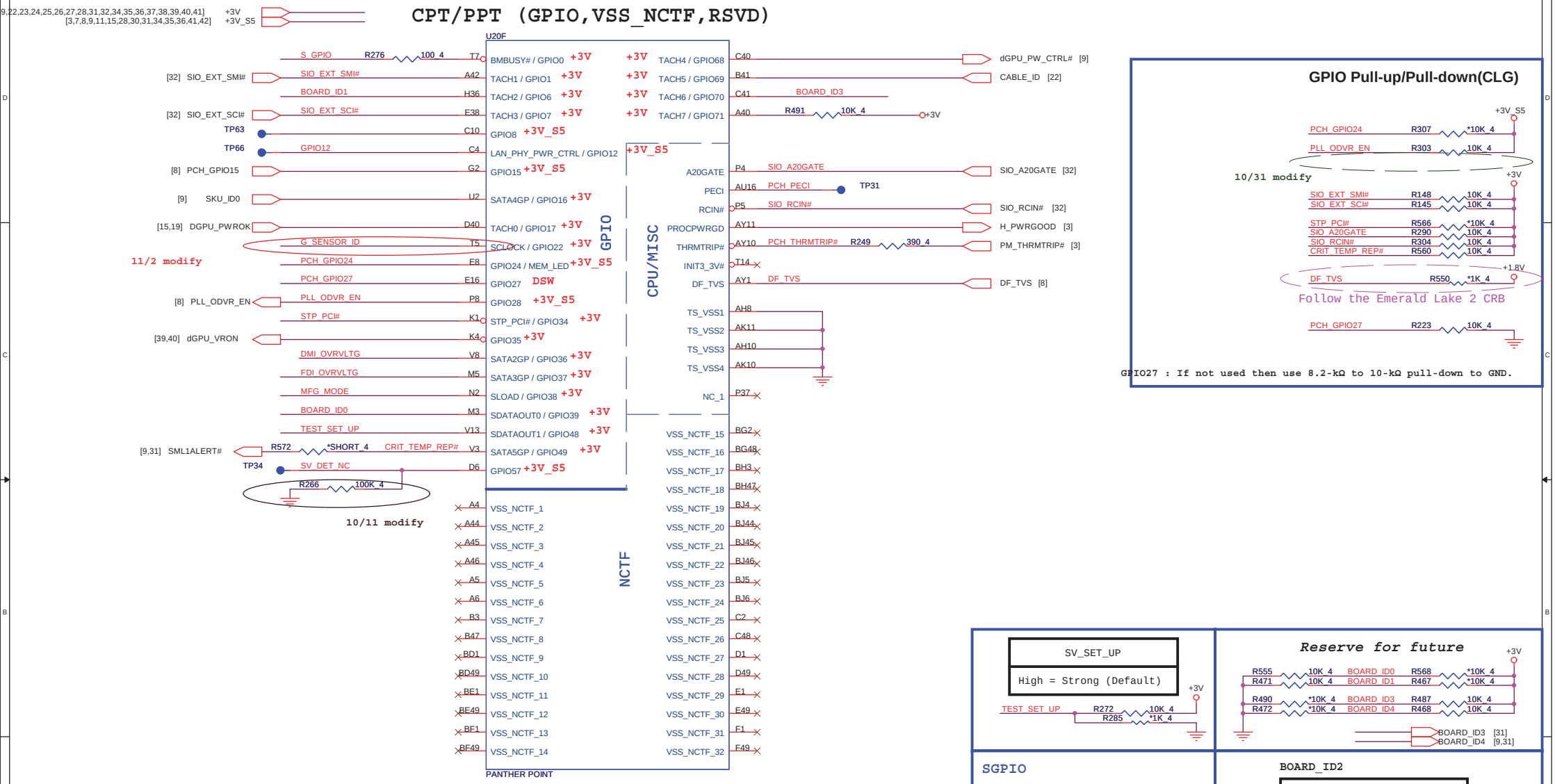
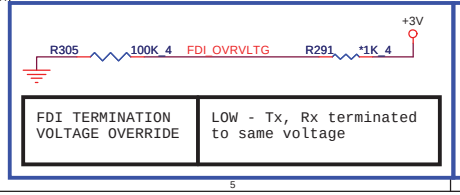
CPT/PPT (GPIO,VSS_NCTF,RSVD)



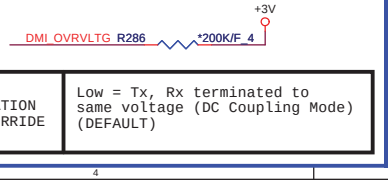
GPIO Pull-up/Pull-down(CLG)

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

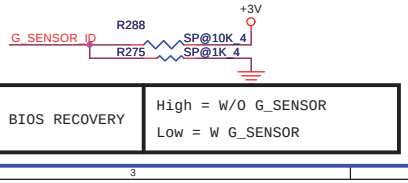
SATA2GP : strap for reserved at chklist 1.2
SATA3GP : strap for reserved at chklist 1.2
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.



FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage



DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



BIOS RECOVERY	High = W/O G_SENSOR Low = W G_SENSOR

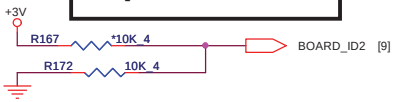
SV_SET_UP
High = Strong (Default)

Reserve for future

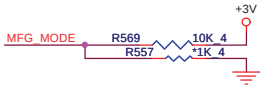
SGPIO

BOARD_ID2

8 Layer ------->High * 6 Layer ------->Low



MFG-TEST



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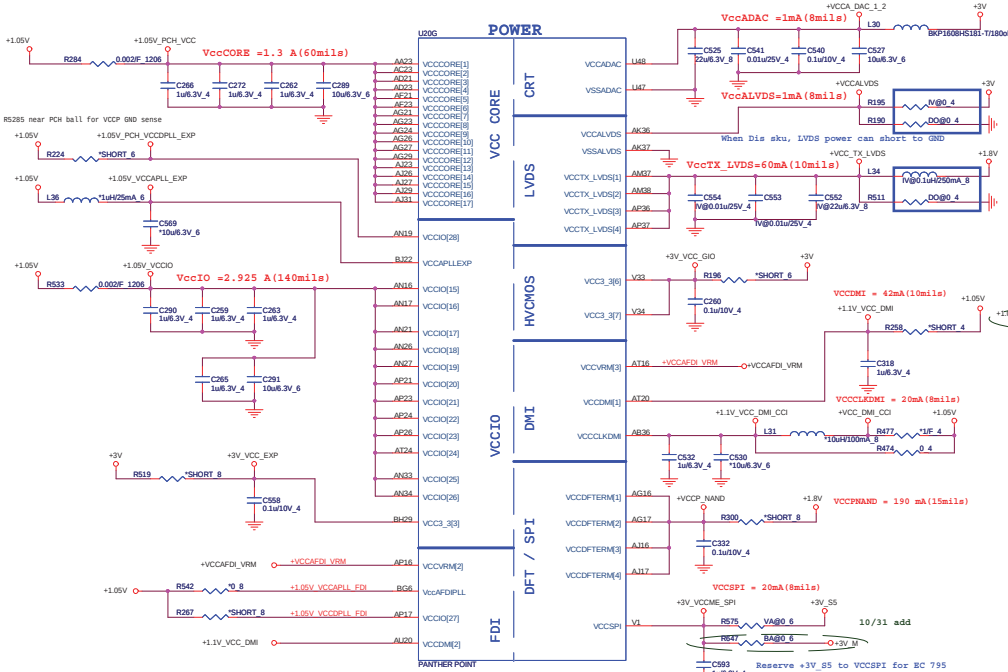
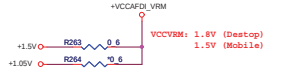
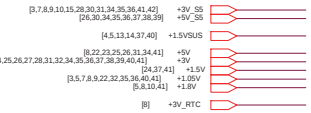
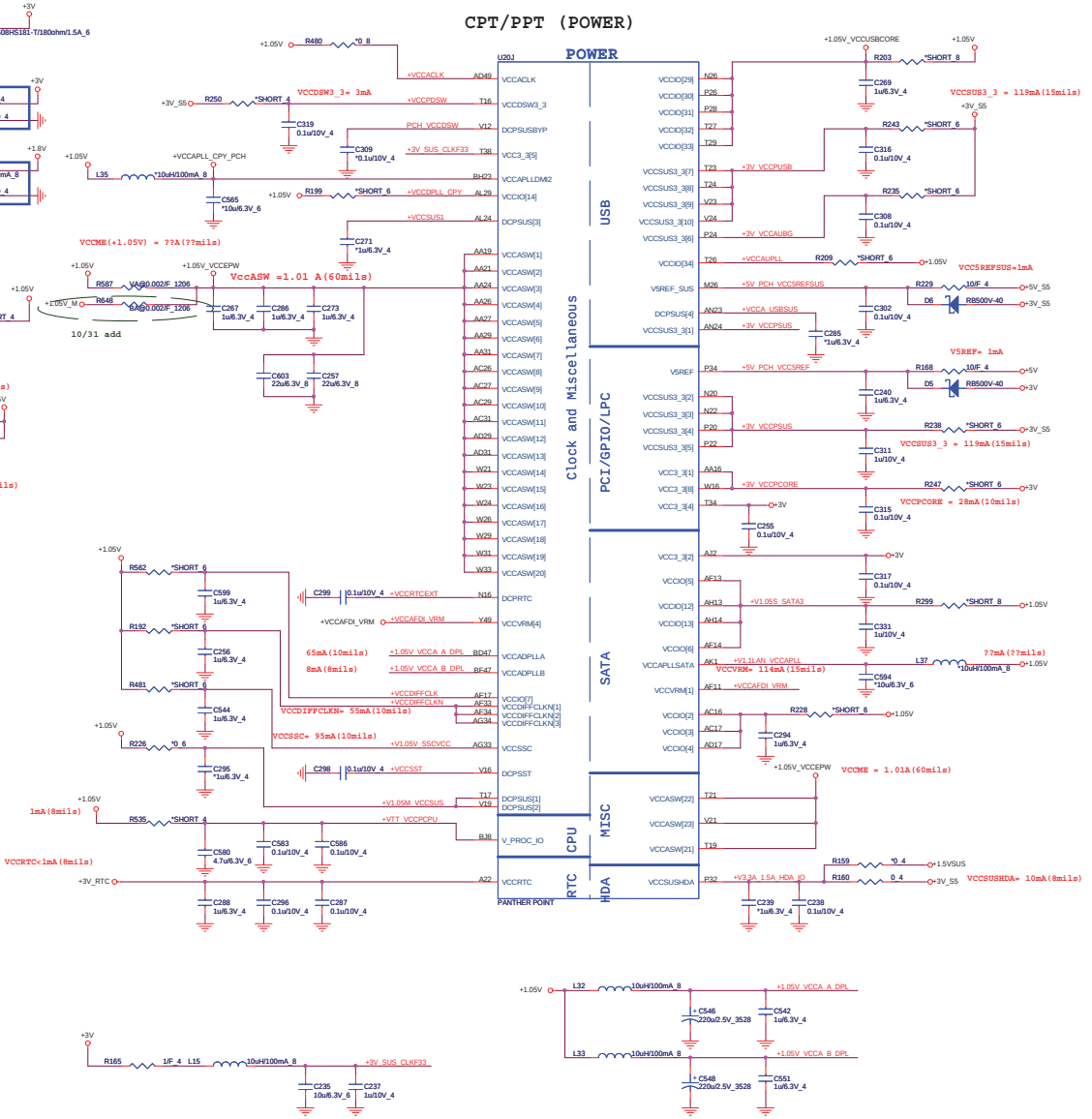
CPT/PPT (POWER)









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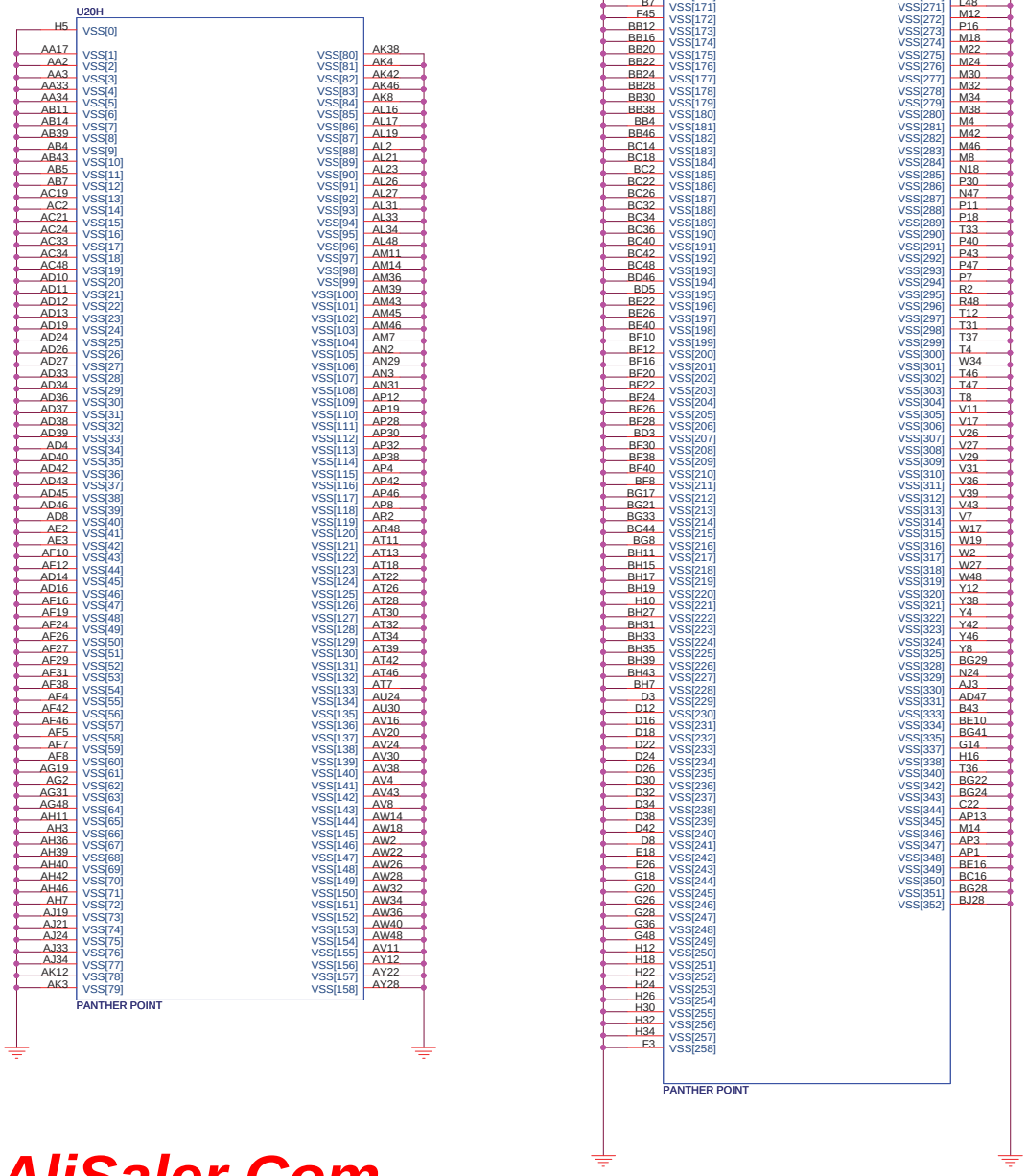
IBEX PEAK-M (GND)



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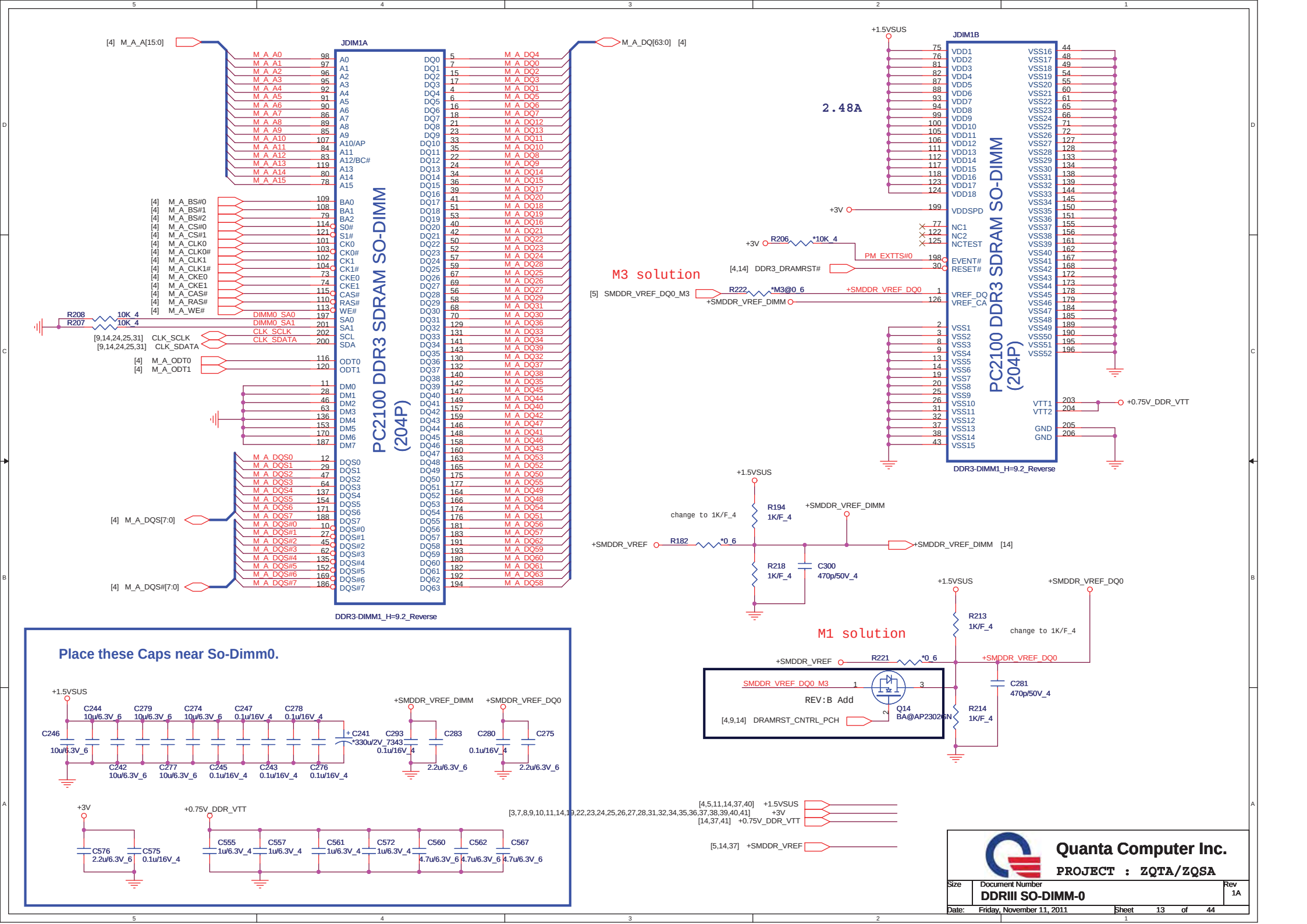
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=9.2_Reverse
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=9.2_Reverse
2.48A
M3 solution
M1 solution
REV:B Add
Q14 BA@AP2302GN
Place these Caps near So-Dimm0.
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DDRIII SO-DIMM-0
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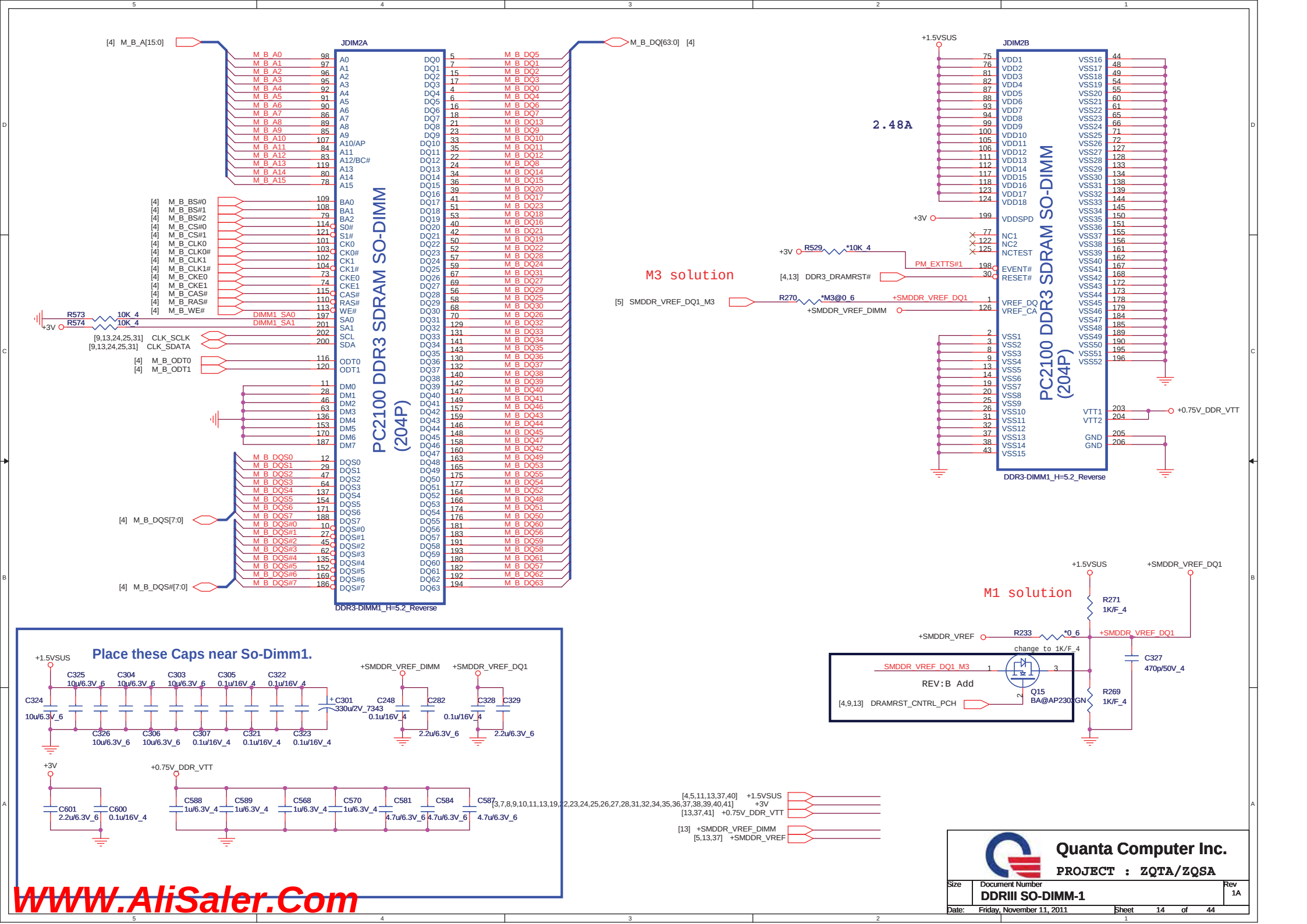
JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=5.2_Reverse
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=5.2_Reverse
2.48A
M3 solution
M1 solution
Place these Caps near So-Dimm1.
REV:B Add
change to 1K/F_4
WWW.AliSaler.Com
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DDRIII SO-DIMM-1
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N13P-GL	AJ0N13P0T02
N13P-GS	AJ0N13P0T07
N13M-GS	AJ0N13M0T08

IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

1000mA

+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C435	EV@22u/6.3V_8
C441	EV@22u/6.3V_8
C388	EV@10u/6.3V_6
C392	EV@10u/6.3V_6
C74	EV@4.7u/6.3V_6
C91	EV@1u/6.3V_4
C98	EV@1u/6.3V_4

PLACE UNDER BGA
PLACE NEAR BALLS

+1.05V_GFX

To be placed no further from the GPU than bewteen the PS and GPU

C443	EV@22u/6.3V_8
C432	EV@22u/6.3V_8
C114	EV@10u/6.3V_6
C109	EV@10u/6.3V_6
C52	EV@4.7u/6.3V_6
C86	EV@1u/6.3V_4
C78	EV@1u/6.3V_4

PLACE UNDER BGA
PLACE NEAR BALLS

2500mA

U15A

[PEG Interface]

AG19	PEX_IOVDD_1
AG21	PEX_IOVDD_2
AG22	PEX_IOVDD_3
AG24	PEX_IOVDD_4
AH21	PEX_IOVDD_5
AH25	PEX_IOVDD_6
AG13	PEX_IOVDDQ_1
AG15	PEX_IOVDDQ_2
AG16	PEX_IOVDDQ_3
AG18	PEX_IOVDDQ_4
AG25	PEX_IOVDDQ_5
AH15	PEX_IOVDDQ_6
AH18	PEX_IOVDDQ_7
AH26	PEX_IOVDDQ_8
AH27	PEX_IOVDDQ_9
AJ27	PEX_IOVDDQ_10
AK27	PEX_IOVDDQ_11
AL27	PEX_IOVDDQ_12
AM28	PEX_IOVDDQ_13
AN28	PEX_IOVDDQ_14

PEX_RX0	AN12	PEG_TX15
PEX_RX0_N	AM12	PEG_TX#15
PEX_RX1	AN14	PEG_TX14
PEX_RX1_N	AM14	PEG_TX#14
PEX_RX2	AP14	PEG_TX13
PEX_RX2_N	AP15	PEG_TX#13
PEX_RX3	AN15	PEG_TX12
PEX_RX3_N	AM15	PEG_TX#12
PEX_RX4	AN17	PEG_TX11
PEX_RX4_N	AM17	PEG_TX#11
PEX_RX5	AP17	PEG_TX10
PEX_RX5_N	AP18	PEG_TX#10
PEX_RX6	AN18	PEG_TX9
PEX_RX6_N	AM18	PEG_TX#9
PEX_RX7	AN20	PEG_TX8
PEX_RX7_N	AM20	PEG_TX#8
PEX_RX8	AP20	PEG_TX7
PEX_RX8_N	AP21	PEG_TX#7
PEX_RX9	AN21	PEG_TX6
PEX_RX9_N	AM21	PEG_TX#6
PEX_RX10	AN23	PEG_TX5
PEX_RX10_N	AM23	PEG_TX#5
PEX_RX11	AP23	PEG_TX4
PEX_RX11_N	AP24	PEG_TX#4
PEX_RX12	AN24	PEG_TX3
PEX_RX12_N	AM24	PEG_TX#3
PEX_RX13	AN26	PEG_TX2
PEX_RX13_N	AM26	PEG_TX#2
PEX_RX14	AP26	PEG_TX1
PEX_RX14_N	AP27	PEG_TX#1
PEX_RX15	AN27	PEG_TX0
PEX_RX15_N	AM27	PEG_TX#0

PEX_RX0	AN12	PEG_TX15		PEG_TX15 [3]
PEX_RX0_N	AM12	PEG_TX#15		PEG_TX#15 [3]
PEX_RX1	AN14	PEG_TX14		PEG_TX14 [3]
PEX_RX1_N	AM14	PEG_TX#14		PEG_TX#14 [3]
PEX_RX2	AP14	PEG_TX13		PEG_TX13 [3]
PEX_RX2_N	AP15	PEG_TX#13		PEG_TX#13 [3]
PEX_RX3	AN15	PEG_TX12		PEG_TX12 [3]
PEX_RX3_N	AM15	PEG_TX#12		PEG_TX#12 [3]
PEX_RX4	AN17	PEG_TX11		PEG_TX11 [3]
PEX_RX4_N	AM17	PEG_TX#11		PEG_TX#11 [3]
PEX_RX5	AP17	PEG_TX10		PEG_TX10 [3]
PEX_RX5_N	AP18	PEG_TX#10		PEG_TX#10 [3]
PEX_RX6	AN18	PEG_TX9		PEG_TX9 [3]
PEX_RX6_N	AM18	PEG_TX#9		PEG_TX#9 [3]
PEX_RX7	AN20	PEG_TX8		PEG_TX8 [3]
PEX_RX7_N	AM20	PEG_TX#8		PEG_TX#8 [3]
PEX_RX8	AP20	PEG_TX7		PEG_TX7 [3]
PEX_RX8_N	AP21	PEG_TX#7		PEG_TX#7 [3]
PEX_RX9	AN21	PEG_TX6		PEG_TX6 [3]
PEX_RX9_N	AM21	PEG_TX#6		PEG_TX#6 [3]
PEX_RX10	AN23	PEG_TX5		PEG_TX5 [3]
PEX_RX10_N	AM23	PEG_TX#5		PEG_TX#5 [3]
PEX_RX11	AP23	PEG_TX4		PEG_TX4 [3]
PEX_RX11_N	AP24	PEG_TX#4		PEG_TX#4 [3]
PEX_RX12	AN24	PEG_TX3		PEG_TX3 [3]
PEX_RX12_N	AM24	PEG_TX#3		PEG_TX#3 [3]
PEX_RX13	AN26	PEG_TX2		PEG_TX2 [3]
PEX_RX13_N	AM26	PEG_TX#2		PEG_TX#2 [3]
PEX_RX14	AP26	PEG_TX1		PEG_TX1 [3]
PEX_RX14_N	AP27	PEG_TX#1		PEG_TX#1 [3]
PEX_RX15	AN27	PEG_TX0		PEG_TX0 [3]
PEX_RX15_N	AM27	PEG_TX#0		PEG_TX#0 [3]

PEX_TX0	AK14	R_PEG_RX15	C133	EV@0.22u/6.3V_4
PEX_TX0_N	AJ14	R_PEG_RX#15	C138	EV@0.22u/6.3V_4
PEX_TX1	AH14	R_PEG_RX14	C140	EV@0.22u/6.3V_4
PEX_TX1_N	AG14	R_PEG_RX#14	C145	EV@0.22u/6.3V_4
PEX_TX2	AK15	R_PEG_RX13	C128	EV@0.22u/6.3V_4
PEX_TX2_N	AJ15	R_PEG_RX#13	C130	EV@0.22u/6.3V_4
PEX_TX3	AL16	R_PEG_RX12	C120	EV@0.22u/6.3V_4
PEX_TX3_N	AK16	R_PEG_RX#12	C123	EV@0.22u/6.3V_4
PEX_TX4	AK17	R_PEG_RX11	C112	EV@0.22u/6.3V_4
PEX_TX4_N	AJ17	R_PEG_RX#11	C119	EV@0.22u/6.3V_4
PEX_TX5	AH17	R_PEG_RX10	C106	EV@0.22u/6.3V_4
PEX_TX5_N	AG17	R_PEG_RX#10	C111	EV@0.22u/6.3V_4
PEX_TX6	AK18	R_PEG_RX9	C100	EV@0.22u/6.3V_4
PEX_TX6_N	AJ18	R_PEG_RX#9	C105	EV@0.22u/6.3V_4
PEX_TX7	AL19	R_PEG_RX8	C99	EV@0.22u/6.3V_4
PEX_TX7_N	AK19	R_PEG_RX#8	C95	EV@0.22u/6.3V_4
PEX_TX8	AK20	R_PEG_RX7	C93	EV@0.22u/6.3V_4
PEX_TX8_N	AJ20	R_PEG_RX#7	C89	EV@0.22u/6.3V_4
PEX_TX9	AH20	R_PEG_RX6	C87	EV@0.22u/6.3V_4
PEX_TX9_N	AG20	R_PEG_RX#6	C84	EV@0.22u/6.3V_4
PEX_TX10	AK21	R_PEG_RX5	C81	EV@0.22u/6.3V_4
PEX_TX10_N	AJ21	R_PEG_RX#5	C77	EV@0.22u/6.3V_4
PEX_TX11	AL22	R_PEG_RX4	C76	EV@0.22u/6.3V_4
PEX_TX11_N	AK22	R_PEG_RX#4	C71	EV@0.22u/6.3V_4
PEX_TX12	AK23	R_PEG_RX3	C64	EV@0.22u/6.3V_4
PEX_TX12_N	AJ23	R_PEG_RX#3	C62	EV@0.22u/6.3V_4
PEX_TX13	AH23	R_PEG_RX2	C55	EV@0.22u/6.3V_4
PEX_TX13_N	AG23	R_PEG_RX#2	C54	EV@0.22u/6.3V_4
PEX_TX14	AK24	R_PEG_RX1	C61	EV@0.22u/6.3V_4
PEX_TX14_N	AJ24	R_PEG_RX#1	C59	EV@0.22u/6.3V_4
PEX_TX15	AL25	R_PEG_RX0	C57	EV@0.22u/6.3V_4
PEX_TX15_N	AK25	R_PEG_RX#0	C56	EV@0.22u/6.3V_4

PEX_TX0	AK14	R_PEG_RX15	C133	EV@0.22u/6.3V_4
PEX_TX0_N	AJ14	R_PEG_RX#15	C138	EV@0.22u/6.3V_4
PEX_TX1	AH14	R_PEG_RX14	C140	EV@0.22u/6.3V_4
PEX_TX1_N	AG14	R_PEG_RX#14	C145	EV@0.22u/6.3V_4
PEX_TX2	AK15	R_PEG_RX13	C128	EV@0.22u/6.3V_4
PEX_TX2_N	AJ15	R_PEG_RX#13	C130	EV@0.22u/6.3V_4
PEX_TX3	AL16	R_PEG_RX12	C120	EV@0.22u/6.3V_4
PEX_TX3_N	AK16	R_PEG_RX#12	C123	EV@0.22u/6.3V_4
PEX_TX4	AK17	R_PEG_RX11	C112	EV@0.22u/6.3V_4
PEX_TX4_N	AJ17	R_PEG_RX#11	C119	EV@0.22u/6.3V_4
PEX_TX5	AH17	R_PEG_RX10	C106	EV@0.22u/6.3V_4
PEX_TX5_N	AG17	R_PEG_RX#10	C111	EV@0.22u/6.3V_4
PEX_TX6	AK18	R_PEG_RX9	C100	EV@0.22u/6.3V_4
PEX_TX6_N	AJ18	R_PEG_RX#9	C105	EV@0.22u/6.3V_4
PEX_TX7	AL19	R_PEG_RX8	C99	EV@0.22u/6.3V_4
PEX_TX7_N	AK19	R_PEG_RX#8	C95	EV@0.22u/6.3V_4
PEX_TX8	AK20	R_PEG_RX7	C93	EV@0.22u/6.3V_4
PEX_TX8_N	AJ20	R_PEG_RX#7	C89	EV@0.22u/6.3V_4
PEX_TX9	AH20	R_PEG_RX6	C87	EV@0.22u/6.3V_4
PEX_TX9_N	AG20	R_PEG_RX#6	C84	EV@0.22u/6.3V_4
PEX_TX10	AK21	R_PEG_RX5	C81	EV@0.22u/6.3V_4
PEX_TX10_N	AJ21	R_PEG_RX#5	C77	EV@0.22u/6.3V_4
PEX_TX11	AL22	R_PEG_RX4	C76	EV@0.22u/6.3V_4
PEX_TX11_N	AK22	R_PEG_RX#4	C71	EV@0.22u/6.3V_4
PEX_TX12	AK23	R_PEG_RX3	C64	EV@0.22u/6.3V_4
PEX_TX12_N	AJ23	R_PEG_RX#3	C62	EV@0.22u/6.3V_4
PEX_TX13	AH23	R_PEG_RX2	C55	EV@0.22u/6.3V_4
PEX_TX13_N	AG23	R_PEG_RX#2	C54	EV@0.22u/6.3V_4
PEX_TX14	AK24	R_PEG_RX1	C61	EV@0.22u/6.3V_4
PEX_TX14_N	AJ24	R_PEG_RX#1	C59	EV@0.22u/6.3V_4
PEX_TX15	AL25	R_PEG_RX0	C57	EV@0.22u/6.3V_4
PEX_TX15_N	AK25	R_PEG_RX#0	C56	EV@0.22u/6.3V_4

AC6	NC_1	
AJ28	NC_2	
AJ4	NC_3	
AJ5	NC_4	
AL11	NC_5	
C15	NC_6	
D19	NC_7	
D20	NC_8	
D23	NC_9	
D26	NC_10	
H31	NC_11	
T8	NC_12	
V32	NC_13	

+3V_GFX

J8	VDD33_1
K8	VDD33_2
L8	VDD33_3
M8	VDD33_4

PEX_REFCLK	AL13	CLK_PCIE_VGA	CLK_PCIE_VGA [9]
PEX_REFCLK_N	AK13	CLK_PCIE_VGA#	CLK_PCIE_VGA# [9]

PEX_TSTCLK_OUT	AJ26	PEX_TSTCLK	R53 *EV@200_4
PEX_TSTCLK_OUT_N	AK26	PEX_TSTCLK#	

PEX_WAKE	AJ11		TP5
PEX_RST_N	AJ12	PEGX_RST#	

PEX_CLKREQ_N	AK12	PEX_CLKREQ#	R390 EV@1K_4	+3V_GFX

10/11 change to 1k

PEX_TERMP	AP29	PEX_TERMP	R372	EV@2.49K/F_4
TESTMODE	AK11	TESTMODE	R393	EV@10K/F_4
PEX_PLLVDD	AG26	PEX_PLLVDD	R46 GSS@0_6	+1.05V_GFX
			L3 GL@160808-120	
			C47 EV@4.7u/6.3V_6	PLACE NEAR BGA CLOSE TO CAPS
PEX_PLL_HVDD	AH12		C48 EV@1u/6.3V_4	PLACE UNDER BGA
PEX_SVDD_3V3	AG12		C63 EV@0.1u/10V_4	PLACE NEAR BALLS
3.3V_AUX_NC	P8			
VDD_SENSE	L4		C124 EV@0.1u/10V_4	+3V_GFX
			C459 EV@4.7u/6.3V_6	
			C447 EV@4.7u/6.3V_6	
GND_SENSE	L5			PLACE NEAR BGA

12~16 mils width

for N13P/M-GS	for N13P-GL
Stuff--> R	Reserve--> R
Reserve -->L	Stuff--> L

+3V_GFX PLACE CLOSE TO BGA

C154	EV@4.7u/6.3V_6
C159	EV@1u/10V_6
C143	EV@0.1u/10V_4
C142	EV@0.1u/10V_4
C144	EV@0.1u/10V_4
C141	EV@0.1u/10V_4

PLACE CLOSE TO GPU BALLS

EV@N13x

N13P

GPUVCC_SENSE [39]
GPUVSS_SENSE [39]

[16,17,19,40] +1.05V_GFX
[17,18,19,39,40] +3V_GFX
[3,7,8,9,10,11,28,30,31,34,35,36,41,42] +3V_S5
[3,7,8,9,10,11,13,14,19,22,23,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V

10/31 modify

[10,19] DGPU_PWROK

R649 *EV@10K/F_4

R384 EV@10K/F_4

+3V_GFX

+3V_S5

R589 10K/F_4

CLK_PEGA_REQ# [9]

Q39 EV@DTC144EUA

PEX_CLKREQ#

Q22 EV@PDTC143TT

10/11 chnage type

+3V_GFX

10/5 modify

C390 EV@0.1u/10V_4

[9,24,28,32] PLTRST#

[9] DGPU_HOLD_RST#

U14 EV@MC74VHC1G08DFT2G

PEGX_RST#

R374 EV@100K_4

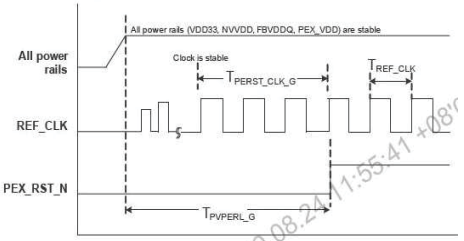
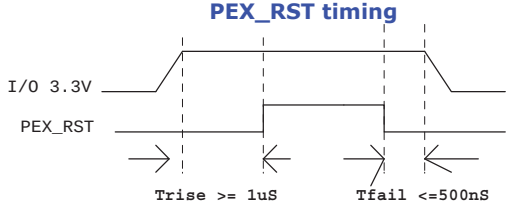


Figure 3-18. PEX_RST_N Timing for GPU

Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T_{PVPERL_G}	$T_{PVPERL\_G} \geq 1us$	
$T_{PERST\_CLK\_G}$	$T_{PERST\_CLK\_G} \geq 1T_{REF\_CLK}$	

PEX_RST timing



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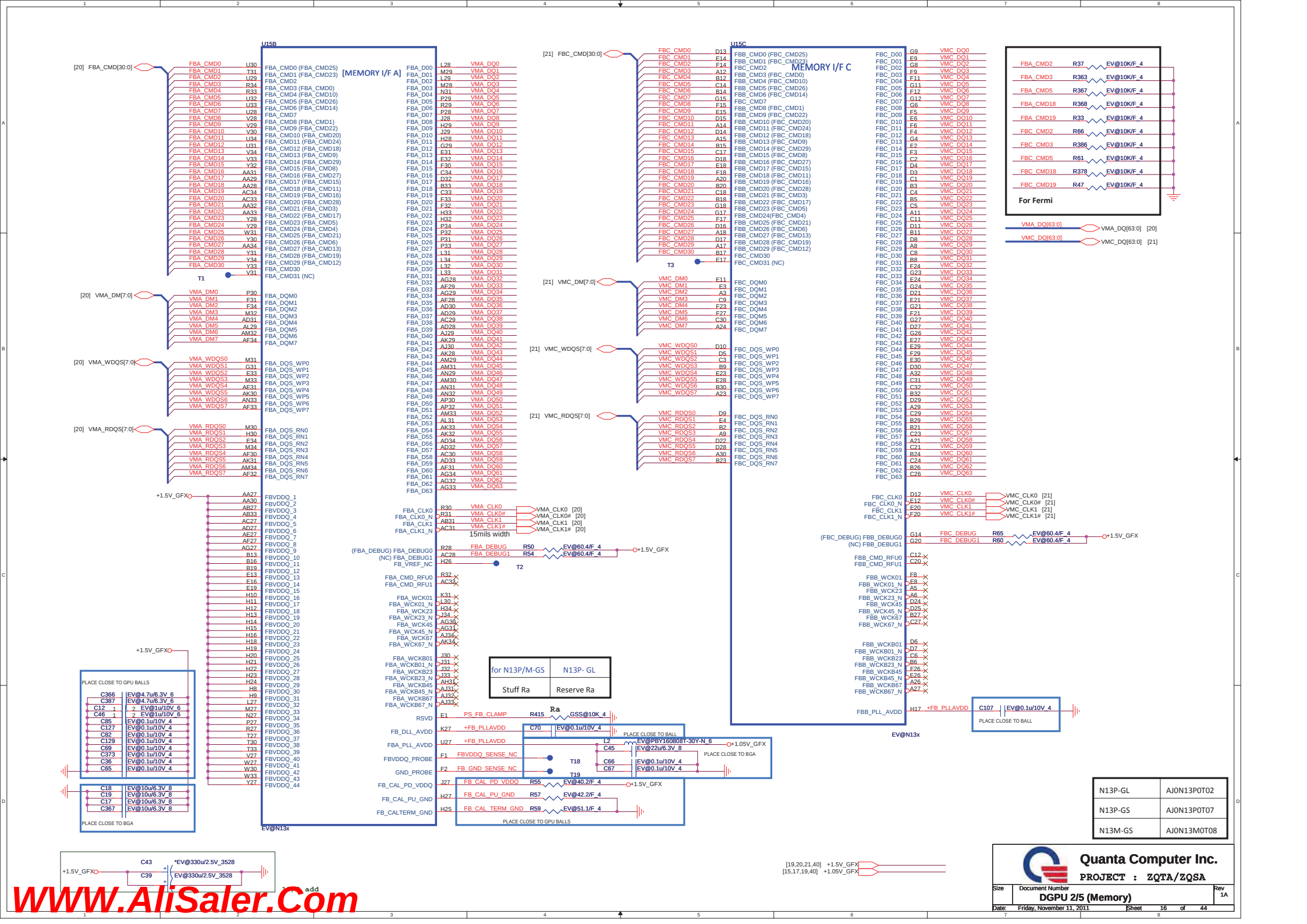
U15B
[MEMORY I/F A]
U15C
MEMORY I/F C
T1
T2
T3
T18
T19
EV@N13x
PLACE CLOSE TO GPU BALLS
PLACE CLOSE TO BGA
PLACE CLOSE TO BALL
PLACE CLOSE TO BGA
PLACE CLOSE TO GPU BALLS
15mils width
for N13P/M-GS
N13P- GL
Stuff Ra
Reserve Ra
For Fermi
N13P-GL AJ0N13P0T02
N13P-GS AJ0N13P0T07
N13M-GS AJ0N13M0T08
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DGPU 2/5 (Memory)
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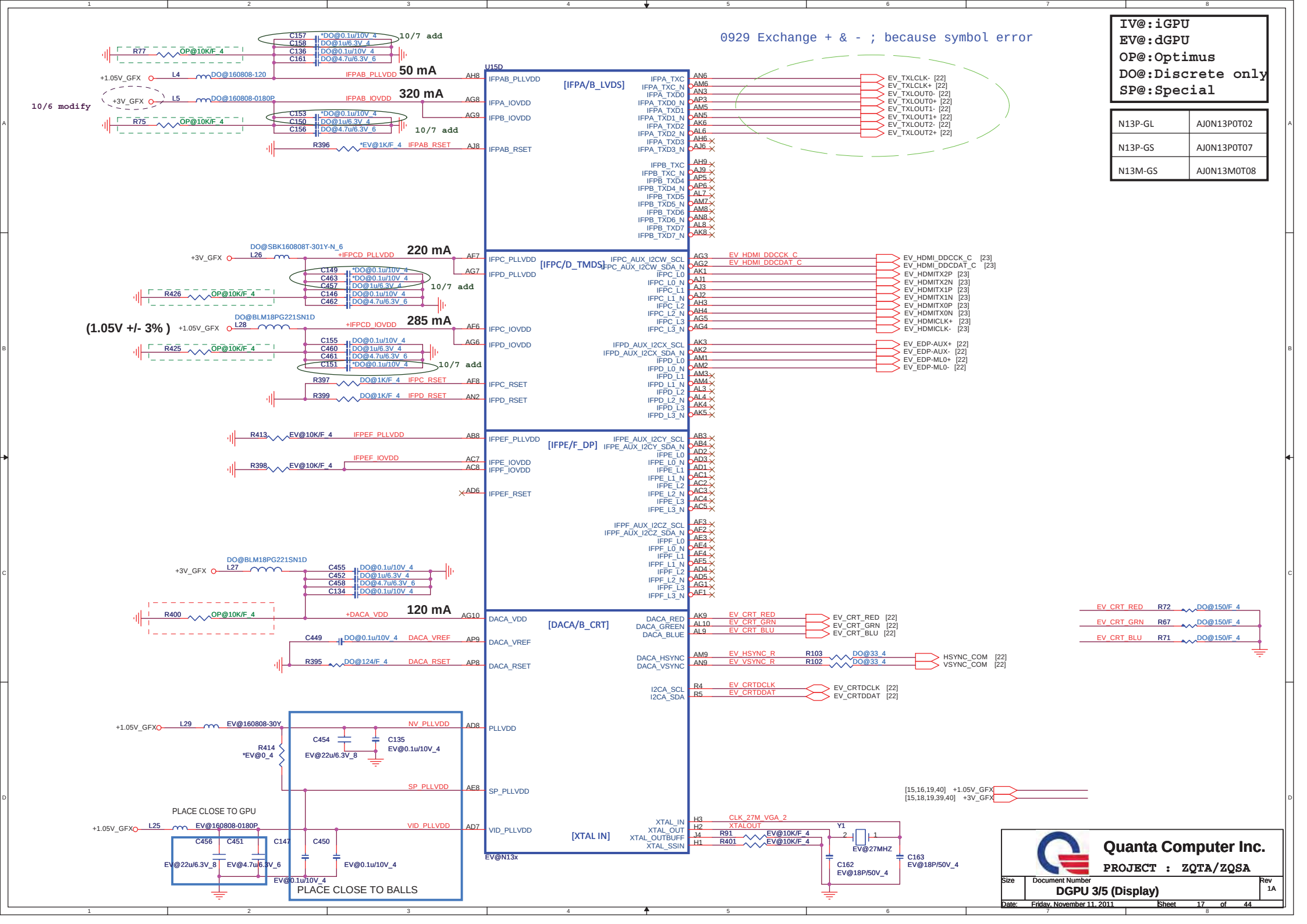
0929 Exchange + & - ; because symbol error
IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special
N13P-GL AJ0N13P0T02
N13P-GS AJ0N13P0T07
N13M-GS AJ0N13M0T08
10/6 modify
10/7 add
50 mA
320 mA
220 mA
285 mA
120 mA
(1.05V +/- 3%)
U15D
[IFPA/B_LVDS]
[IFPC/D_TMDS]
[IFPE/F_DP]
[DACA/B_CRT]
[XTAL IN]
PLACE CLOSE TO GPU
PLACE CLOSE TO BALLS
EV@N13x
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DGPU 3/5 (Display)
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Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1110
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0010
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	0011

N13P-GL	AJ0N13P0T02
N13P-GS	AJ001070T00
N13M-GS	AJ001170T00

[15,17,19,39,40] +3V_GFX

STRAP2
N13P-GL (1001) ---> 10k PU
N13P-GS (1011) ---> 20K PU

STRAP1
N13P-GL (0111) ---> 45.3k PD
N13P-GS (0110) ---> 34.8K PD

STRAP3
Optimus ---> 4.99k PD
Discrete only ---> 15K PD

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
34.8K---> CS33482FB22
45.3K ---> CS34532FB18

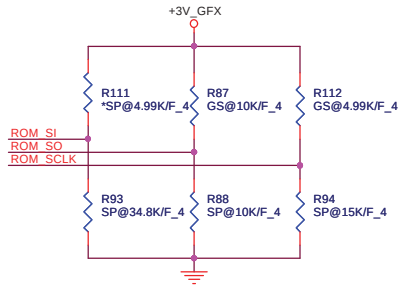
U15E

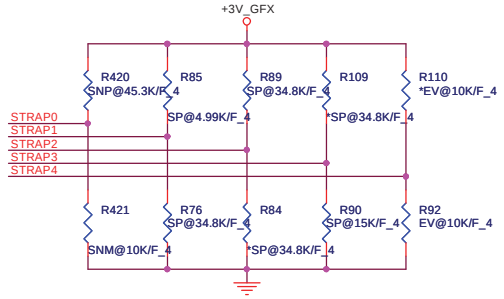
[MIOA]

[MIOB]

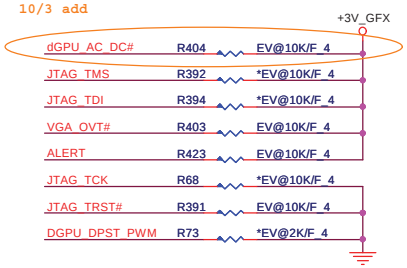
[MISC_GPIO/I2C/JTAG/THER]

[MISC2_ROM]





10/3 add



N13P-GS/-GL Straping table

ROM_SI	ROM_SO	ROM_SCLK
1G Hynix 64Mx16 -->15K PD	N13P-GL --> 10K PD	N13P-GL (0010) ---> 15k PD
1G Micron 64Mx16 -->20K PD	N13P-GS --> 10K PU	N13P-GS (1000) ---> 4.99K PU
2G Hynix 128Mx16 -->35K PD (Default)		
2G Micron 128Mx16 -->45K PD		

N13M-GS Straping table

Pin Name	Strap Mapping	Value
ROM_SCLK	SMB_ALT_ADDR	0
ROM_SI	SUB_VENDOR	0
ROM_SO	VGA_DEVICE	0
STRAP[3..0]	RAM_CFG[3..0]	0010(Hynix 64Mx16) 0110(Hynix 128Mx16)
STRAP[4]	PCIE_MAX_SPEED	0

Remark :
0 -> 10K PD
1 -> 10K PU

10/3 modify

R422	
N13P-GS/GL	40.2K
N13M-GS	NC

for N13P/M-GS	for N13P- GL
Reserve R108	Stuff R108

GFx SMBus Isolation * *

11/8 change for GPU temp detect

EV@N13x

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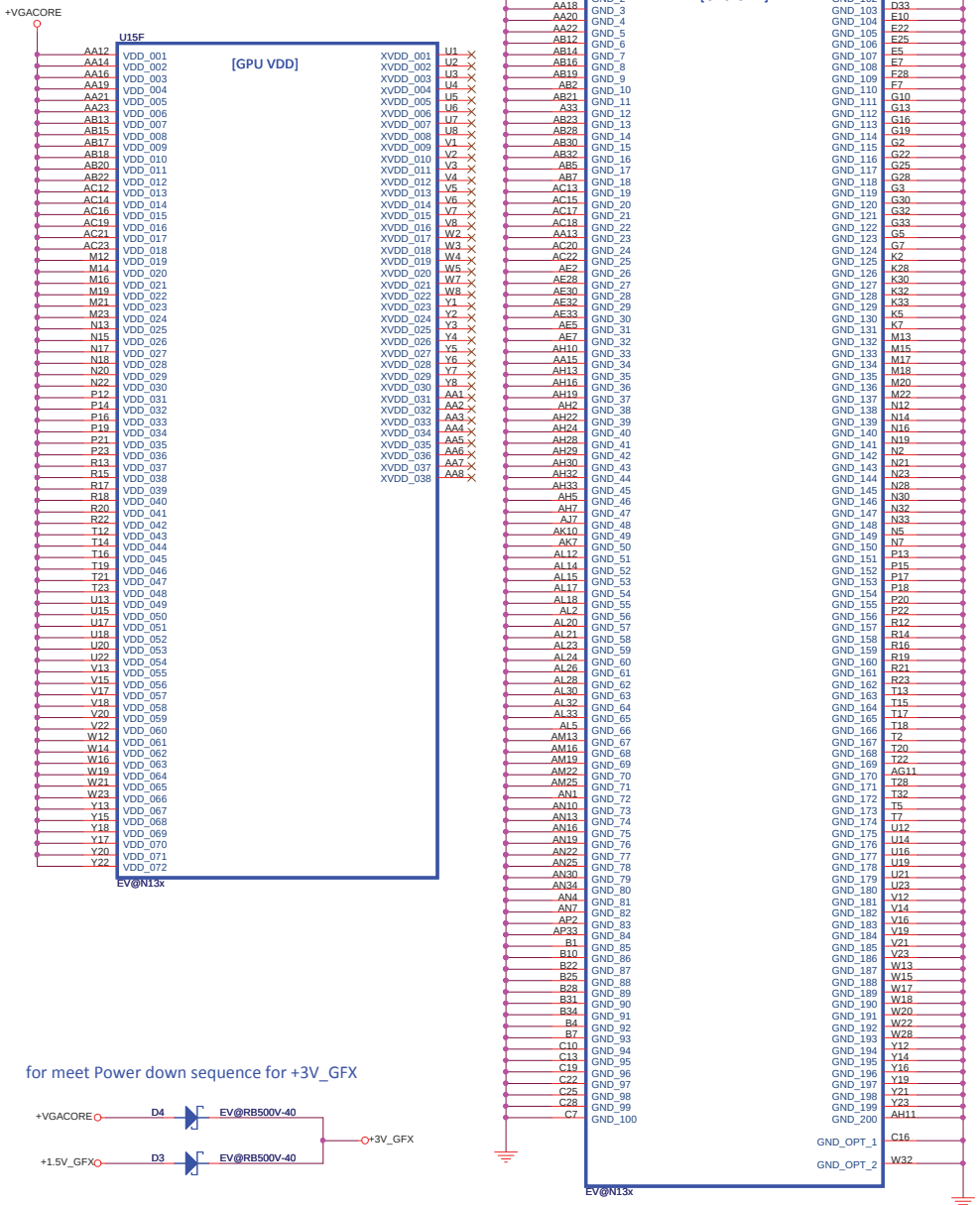
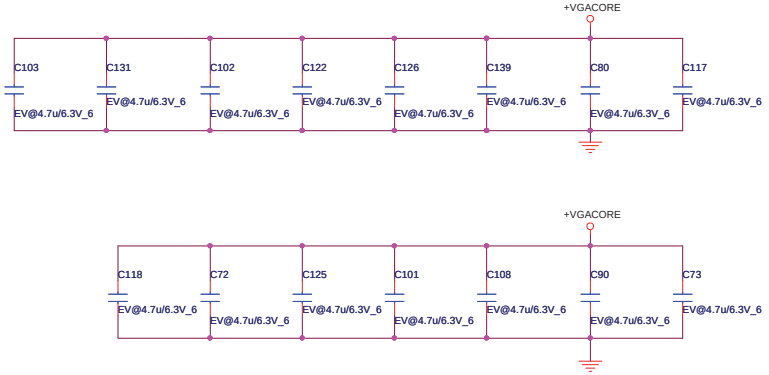
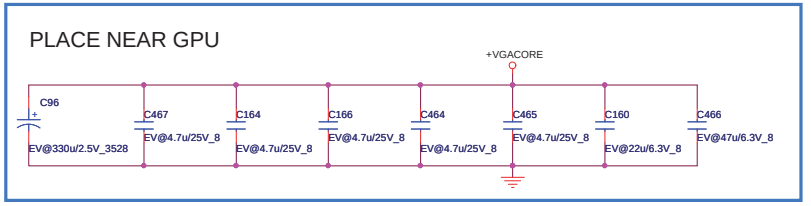
N13P-GL	AJ0N13P0T02
N13P-GS	AJ0N13P0T07
N13M-GS	AJ0N13M0T08

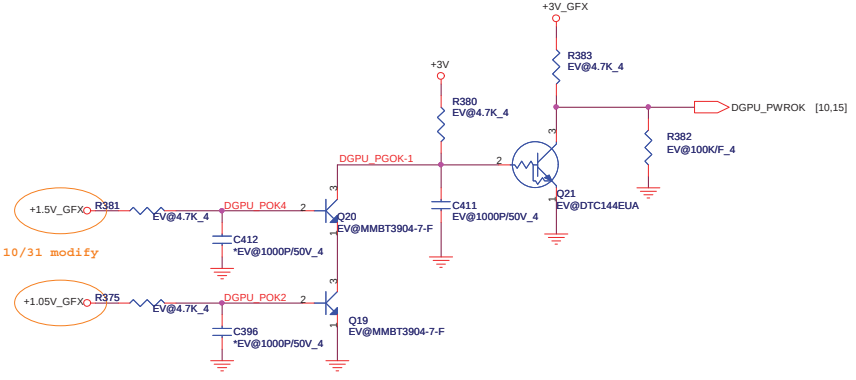


PLACE UNDER GPU

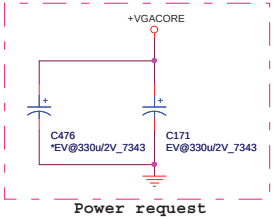


PLACE NEAR GPU





for meet Power down sequence for +3V_GFX



Power request

ESR

9/27 add

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HYNIX 900MHz 1G AKD5LZWTW02
HYNIX 900MHz 2G AKD5MGWTW00

CHANNEL A: 256MB/512MB DDR3

[16] VMA_DQ[63..0]
[16] VMA_DM[7..0]
[16] VMA_WDQS[7..0]
[16] VMA_RDQS[7..0]

VRAM2 / VRAM5 / VRAM1 / VRAM6

10/12 SWAP Pin

Should be 240 Ohms +-1%

R43 EV@243/F_4
R364 EV@243/F_4
R34 EV@243/F_4
R373 EV@243/F_4

96-BALL SDRAM DDR3
EV@VRAM_DDR3

+1.5V_GFX

R371 EV@162/F_4

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R366 EV@1.33K/F_4
R365 EV@1.33K/F_4
C376 EV@0.1u/10V_4
R39 EV@1.33K/F_4
R38 EV@1.33K/F_4
C34 EV@0.1u/10V_4

[16] FBA_CMD17 → TP1
[16] FBA_CMD1 → TP2
10/14 modify

R41 EV@162/F_4

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R36 EV@1.33K/F_4
R35 EV@1.33K/F_4
C24 EV@0.1u/10V_4
R370 EV@1.33K/F_4
R369 EV@1.33K/F_4
C380 EV@0.1u/10V_4

C30 C27 C374 C25 EV@1u/10V_4
C369 C379 C382 C23 C29 C32 EV@10u/6.3V_8 / EV@1u/10V_4
C416 C26 C375 C28 EV@10u/6.3V_8 / EV@1u/10V_4
C37 C33 C31 C371 EV@1u/10V_4
C386 C368 EV@10u/6.3V_8
C381 C35 C377 C378 C370 EV@0.1u/10V_4
C44 C88 EV@10u/6.3V_8
C372 C385 C383 EV@0.1u/10V_4

[16,19,21,40] +1.5V_GFX

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HYNIX 900MHz 1G AKD5LZWTW02
HYNIX 900MHz 2G AKD5MGWTW00

[16] VMC_DQ[63..0]
[16] VMC_DM[7..0]
[16] VMC_WDQS[7..0]
[16] VMC_RDQS[7..0]

CHANNEL B: 256MB/512MB DDR3

VRAM8 / VRAM4 / VRAM3 / VRAM7

10/12 SWAP Pin

+1.5V_GFX

Should be 240 Ohms +-1%

R385 SNP@243/F_4 (VRAM8)
R64 SNP@243/F_4 (VRAM4)
R52 SNP@243/F_4 (VRAM3)
R379 SNP@243/F_4 (VRAM7)

96-BALL SDRAM DDR3
SNP@VRAM _DDR3

R388 SNP@162/F_4 (VMC_CLK0 / VMC_CLK0#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R62 SNP@1.33K/F_4, R63 SNP@1.33K/F_4, C121 SNP@0.1u/10V_4 (VREFC_VMC1)
R74 SNP@1.33K/F_4, R70 SNP@1.33K/F_4, C148 SNP@0.1u/10V_4 (VREFD_VMC1)

R49 SNP@162/F_4 (VMC_CLK1 / VMC_CLK1#)

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R56 SNP@1.33K/F_4, R58 SNP@1.33K/F_4, C79 SNP@0.1u/10V_4 (VREFC_VMC3)
R376 SNP@1.33K/F_4, R377 SNP@1.33K/F_4, C403 SNP@0.1u/10V_4 (VREFD_VMC3)

C137 C384 C68 C423 SNP@1u/10V_4
C152 C448 C446 C394 C58 C429 SNP@10u/6.3V_8 / SNP@1u/10V_4
C21 C445 C132 C393 C397 C399 C442 C50 SNP@0.1u/10V_4
C53 C410 C51 C22 C97 C426 C391 C389 SNP@1u/10V_4

[16] FBC_CMD17 — FBC_CMD17 — TP3
[16] FBC_CMD1 — FBC_CMD1 — TP4

[16,19,20,40] +1.5V_GFX

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	DGPU Memory 2/2 (DDR3)	1A
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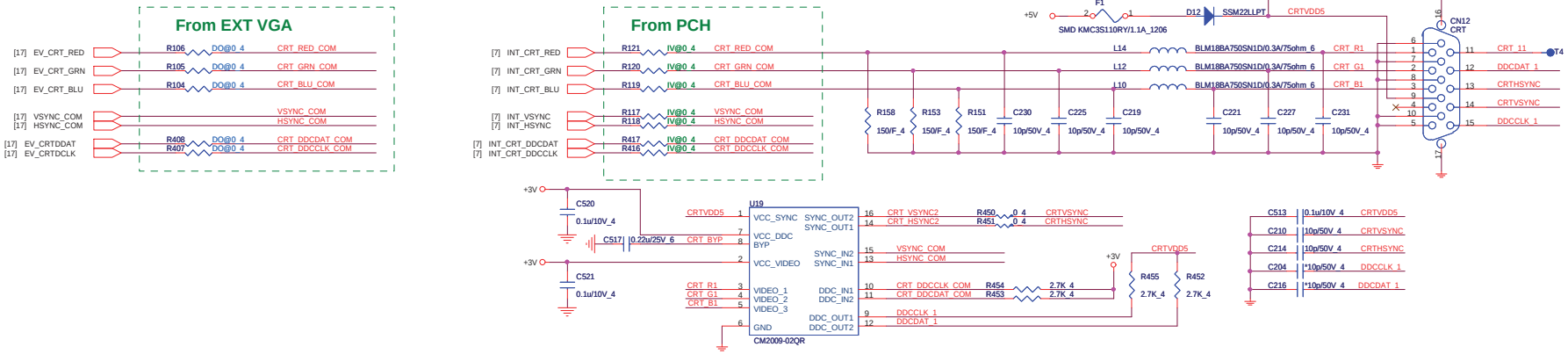
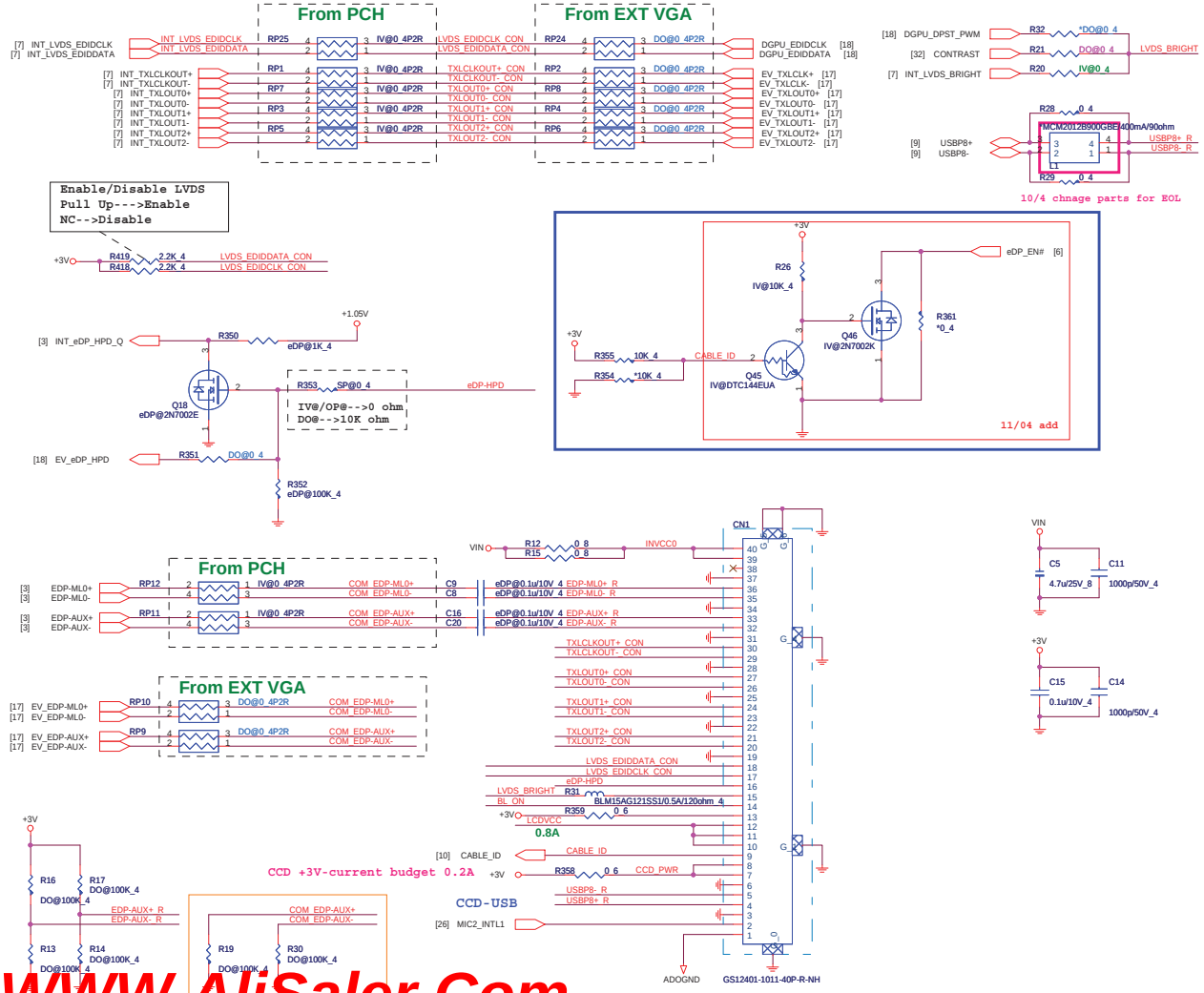
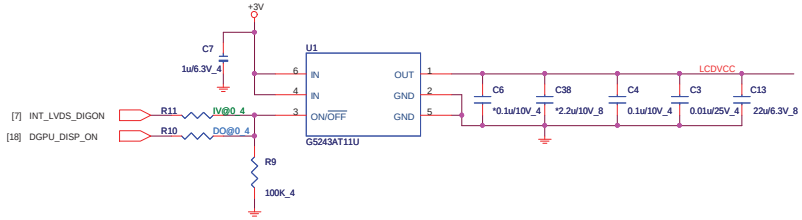
CRT



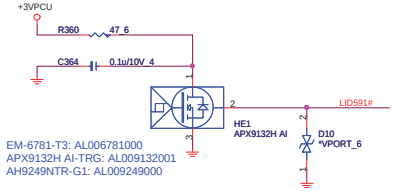
LVDS & eDP



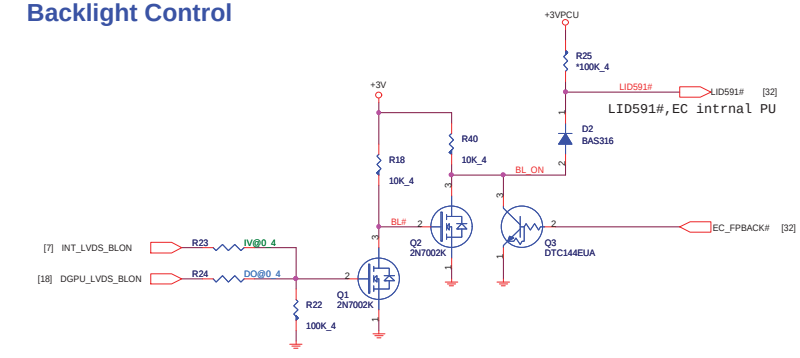
LCD Power



Lid Switch (Hall sensor)



Backlight Control



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	CRT/LVDS/CAMERA/LID	1A

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HDMI

From PCH

[7] INT_HDMITX2N — C270 0.1u/10V_4 — INT_HDMITX2N_C
[7] INT_HDMITX2P — C284 0.1u/10V_4 — INT_HDMITX2P_C
[7] INT_HDMITX1N — C258 0.1u/10V_4 — INT_HDMITX1N_C
[7] INT_HDMITX1P — C261 0.1u/10V_4 — INT_HDMITX1P_C
[7] INT_HDMITX0N — C264 0.1u/10V_4 — INT_HDMITX0N_C
[7] INT_HDMITX0P — C268 0.1u/10V_4 — INT_HDMITX0P_C
[7] INT_HDMICLK+ — C254 0.1u/10V_4 — INT_HDMICLK+_C
[7] INT_HDMICLK- — C251 0.1u/10V_4 — INT_HDMICLK-_C

DO@--->499 ohm
P/N:CS14992FB24
IV@/OP@--->680 ohm
P/N:CS16802JB27

R512 SP@680_4 R515 SP@680_4 R522 SP@680_4 R520 SP@680_4 R518 SP@680_4 R516 SP@680_4 R525 SP@680_4 R523 SP@680_4

+5V — R517 *100K/F_4 — Q38 2N7002E

From EXT VGA

[17] EV_HDMITX2N — RP14 — DO@0_4P2R — INT_HDMITX2N
[17] EV_HDMITX2P — INT_HDMITX2P
[17] EV_HDMITX1N — RP15 — DO@0_4P2R — INT_HDMITX1N
[17] EV_HDMITX1P — INT_HDMITX1P
[17] EV_HDMITX0N — RP16 — DO@0_4P2R — INT_HDMITX0N
[17] EV_HDMITX0P — INT_HDMITX0P
[17] EV_HDMICLK- — RP17 — DO@0_4P2R — INT_HDMICLK-
[17] EV_HDMICLK+ — INT_HDMICLK+

IV@:iGPU
EV@:dGPU
OP@:Optimus
DO@:Discrete only
SP@:Special

HDMI connector

CN13 HDMI CONN
INT_HDMITX2P_C — D2+
INT_HDMITX2N_C — D2 Shield
INT_HDMITX1P_C — D2-
INT_HDMITX1N_C — D1+
INT_HDMITX0P_C — D1 Shield
INT_HDMITX0N_C — D1-
INT_HDMICLK+_C — D0+
D0 Shield
INT_HDMICLK-_C — D0-
CK+
CK Shield
CK-
CE Remote
NC
HDMI_DDCCLK_MB — DDC CLK
HDMI_DDCDATA_MB — DDC DATA
GND
+5V
HP DET
SHELL1 SHELL2

+5V — SMD KMC3S110RY/1.1A_1206 F2 — HDMI_5V_R — D19 SSM22LLPT — HDMI_5V
C545 470p/50V_4
HDMI_MB_HP — R178 0_4 — HP_DET_CN
R179 100K_4

9/22 change parts

HDMI-detect

+3V — R174 10K_4
+3V — R181 10K_4
[32] HDMI_HPD_EC#
+5V — R180 *10K_4 — HDMI_MB_HP
Q11 2N7002E
Q12 2N7002E
R185 IV@0_4 — HDMI_HP [7]
R189 DO@0_4 — EV_HDMI_HPD [18]

I2C

UMA	R239 R245	CS22202JB18
DIS	R239 R245	CS24702JB38

From EXT VGA

[17] EV_HDMI_DDCCK_C — R493 DO@0_4 — HDMI_DDCCLK_COM
[17] EV_HDMI_DDCDAT_C — R508 DO@0_4 — HDMI_DDCDATA_COM

From PCH

[7] HDMI_DDCCLK_SW — R501 IV@0_4 — HDMI_DDCCLK_COM
[7] HDMI_DDCDATA_SW — R504 IV@0_4 — HDMI_DDCDATA_COM

+5V — D20 RB501V-40 — R494 2.2K_4 — HDMI_DDCCLK_MB
+3V — R489 SP@2.2K_4 — Q35 BSN20
+5V — D21 RB501V-40 — R509 2.2K_4 — HDMI_DDCDATA_MB
+3V — R510 SP@2.2K_4 — Q37 BSN20

EMI

INT_HDMITX2P_C — R212 *100/F_4 — INT_HDMITX2N_C
INT_HDMITX1P_C — R200 *100/F_4 — INT_HDMITX1N_C
INT_HDMITX0P_C — R204 *100/F_4 — INT_HDMITX0N_C
INT_HDMICLK+_C — R193 *100/F_4 — INT_HDMICLK-_C

[3,7,8,9,10,11,13,14,19,22,24,25,26,27,28,31,32,34,35,36,37,38,39,40,41] +3V
[8,11,22,25,26,31,34,41] +5V

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	HDMI (PS8101)	1A

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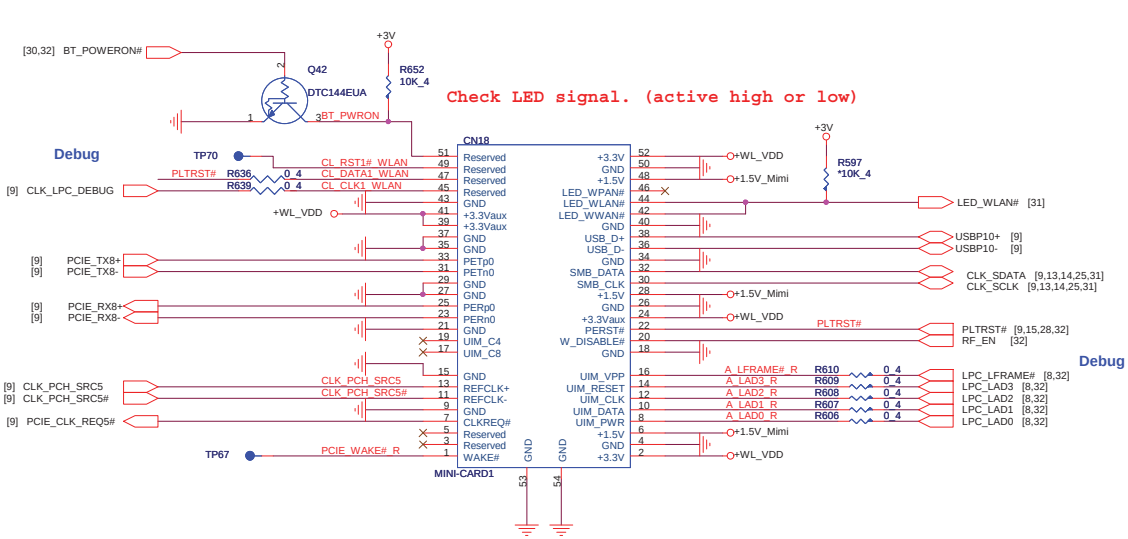
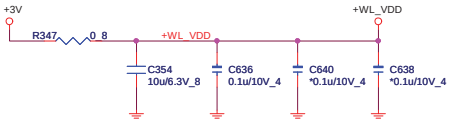
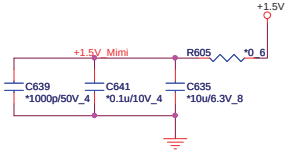
MINI-CARD WLAN(MPC)

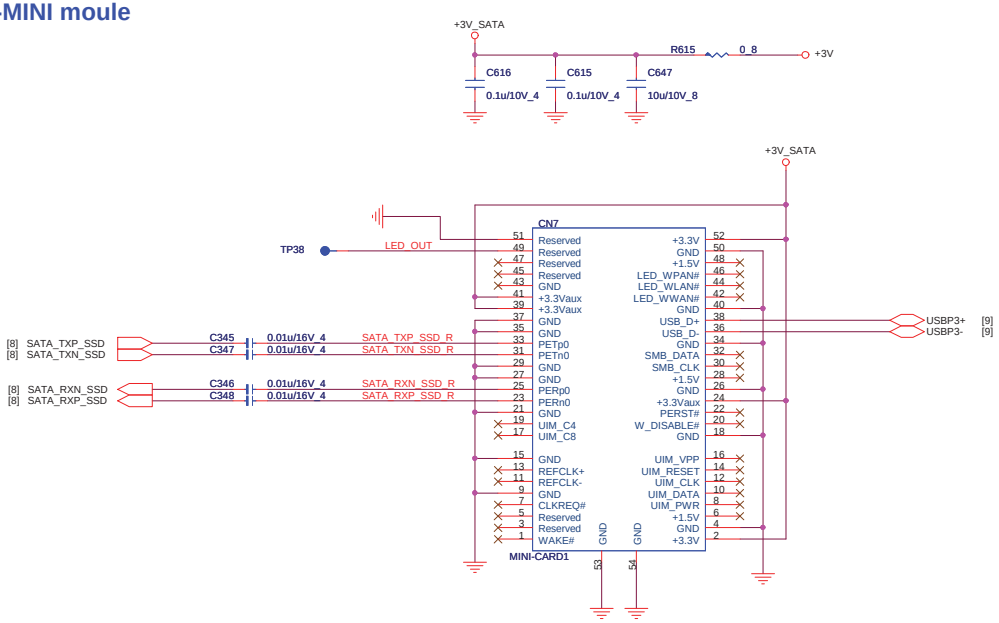
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA





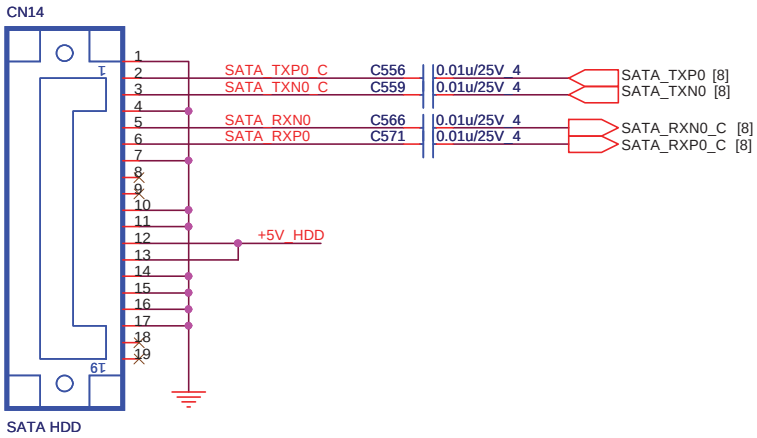


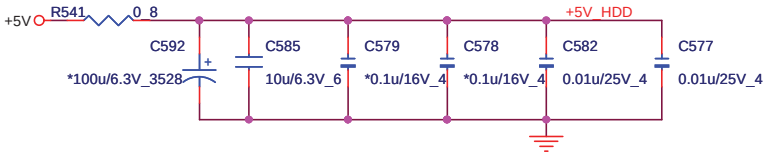
SSD-MINI moule



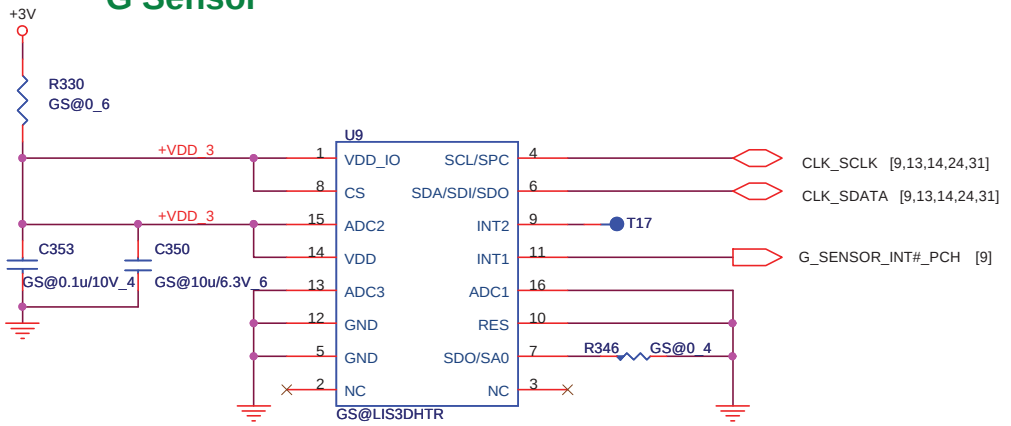
Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: MINI PCI-E / SSD	Rev: 1A
Date: Friday, November 11, 2011	Sheet 24 of 44	

MAIN SATA HDD(HDD)



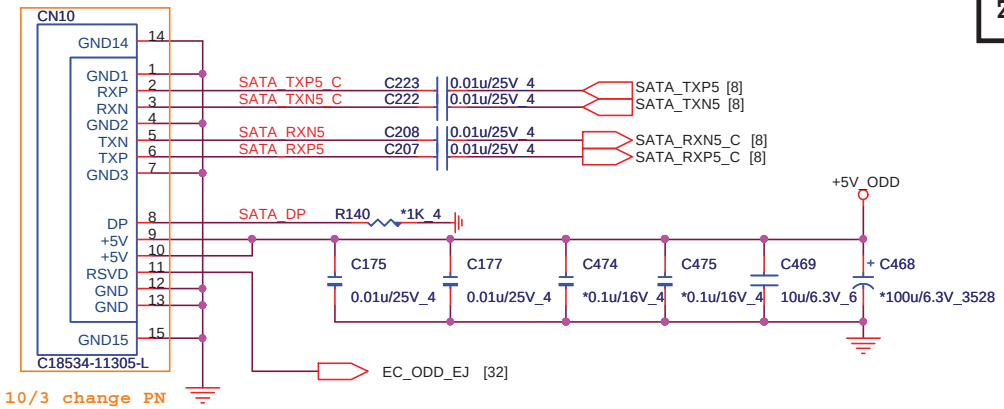


G Sensor



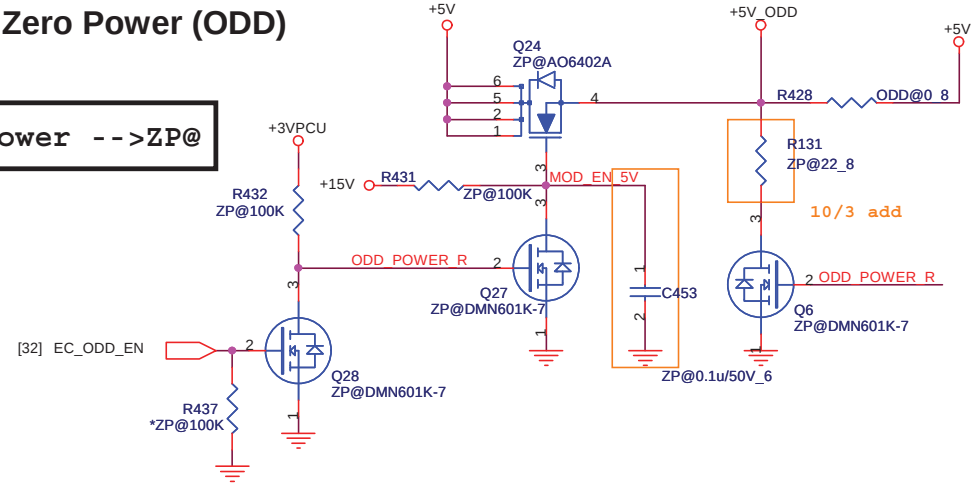
G-Sensor -->GS@

ODD (ODD)



Zero Power (ODD)

Zero Power -->ZP@



Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: SATA-HDD/ODD/G Sensor	Rev 1A
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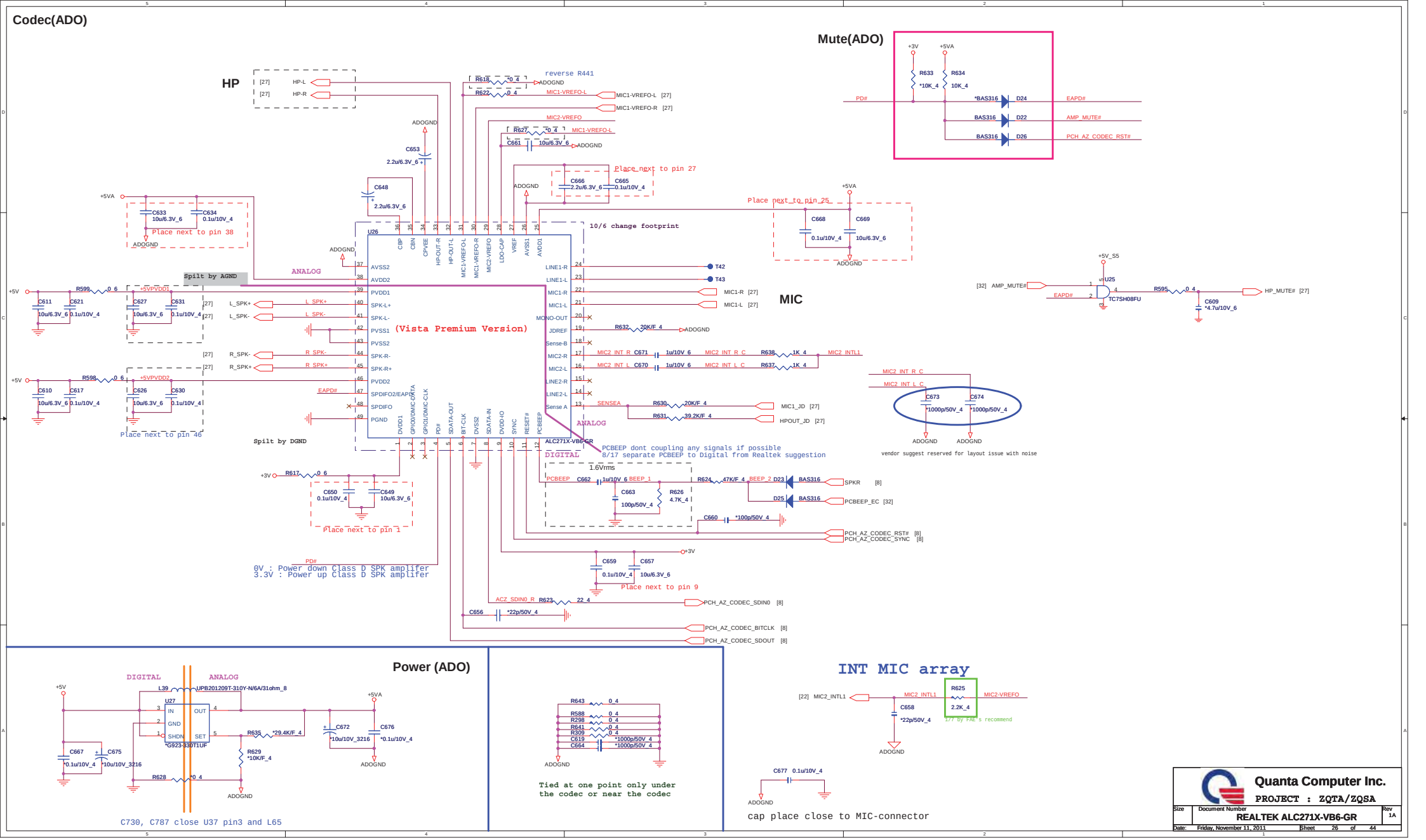
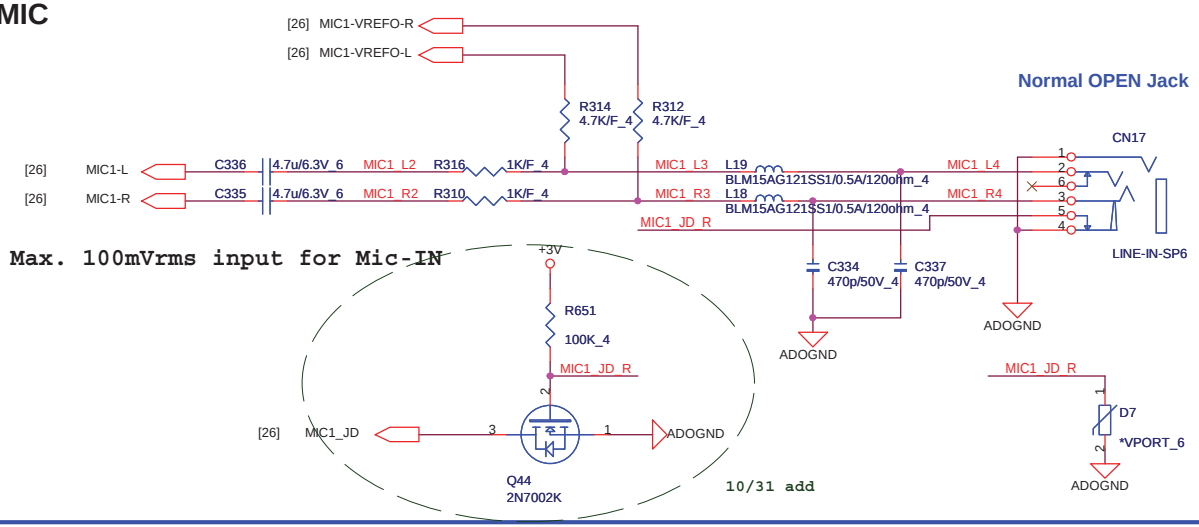
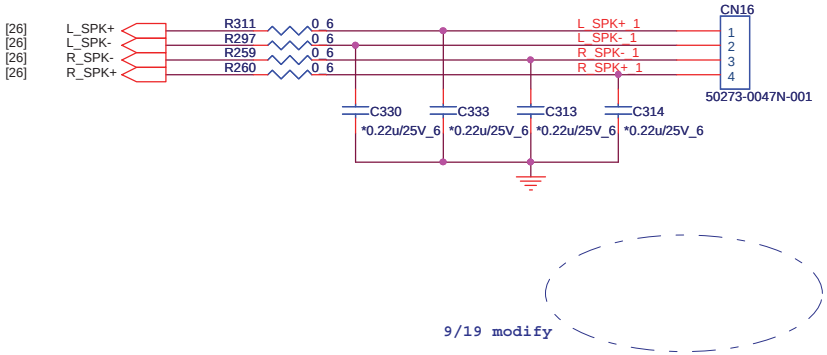
Codec(ADO)



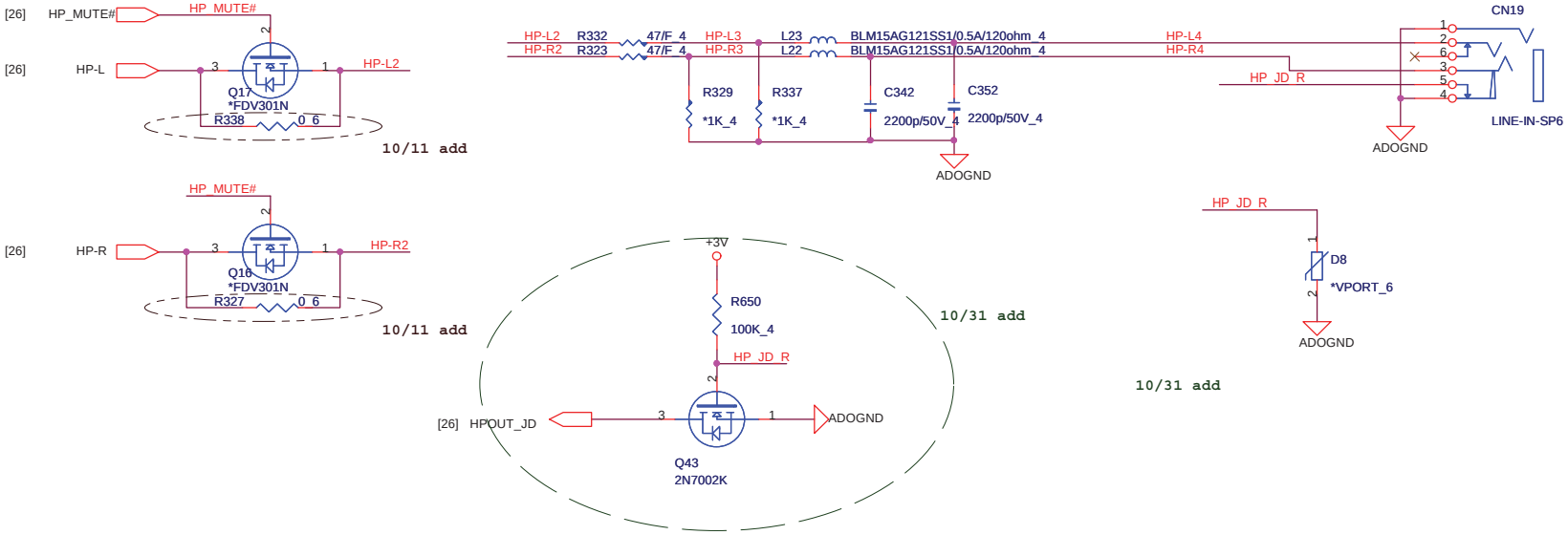
MIC



Internal Speaker

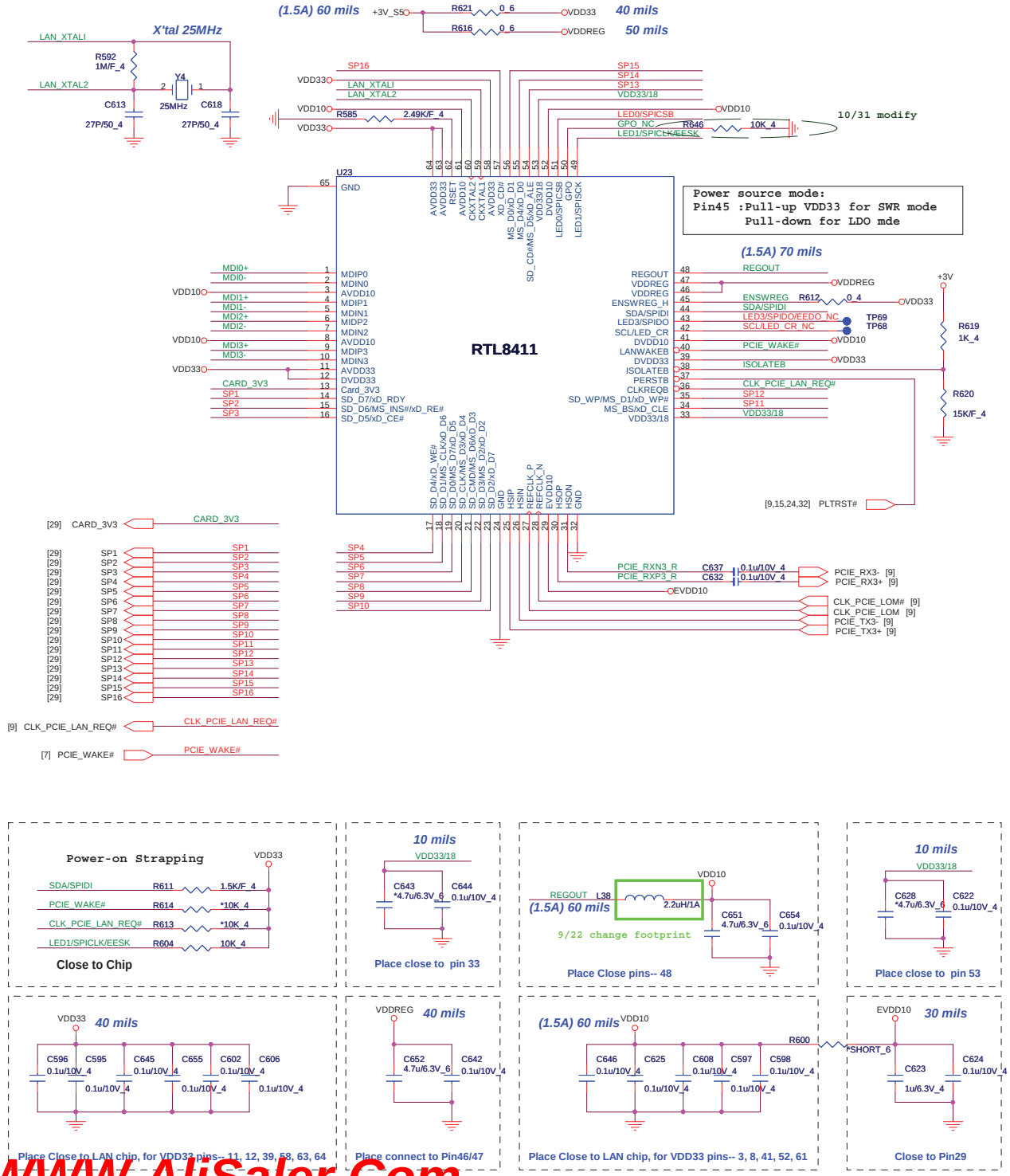


HP

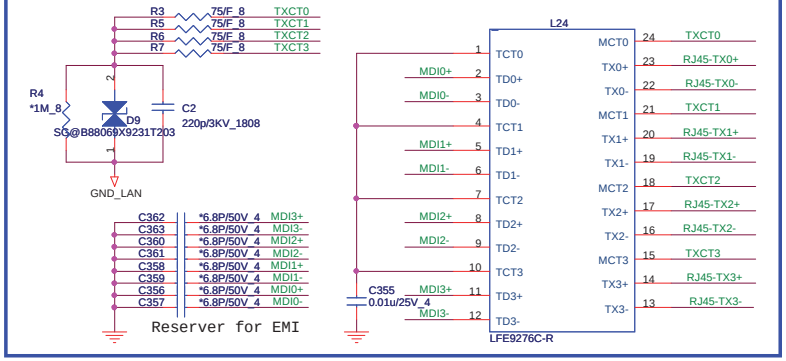


Quanta Computer Inc.		
PROJECT : ZQTA/ZQSA		
Size	Document Number: AUDIO JACK CONN	Rev 1A
Date: Friday, November 11, 2011	Sheet 27 of 44	

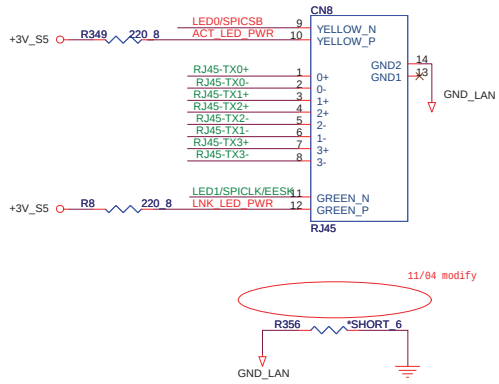
LAN/Card reader



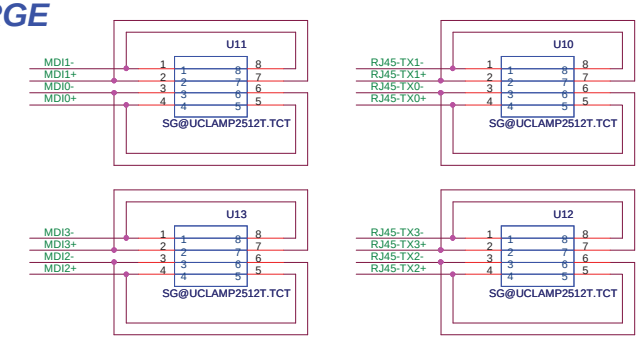
Transformer



RJ45



SURGE



[3,7,8,9,10,11,15,30,31,34,35,36,41,42] +3V_S5

Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	LAN-RTL8411/CARD READER	1A
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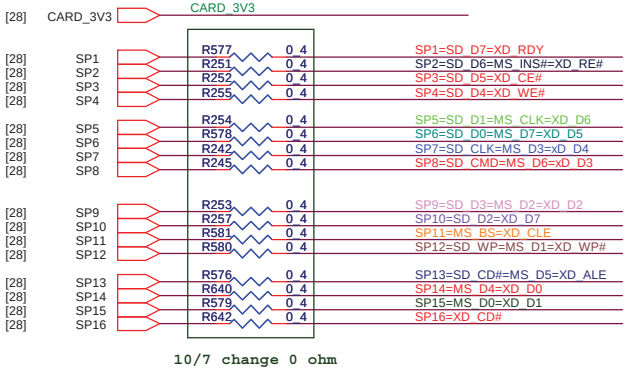
CARD READER CONNECTOR

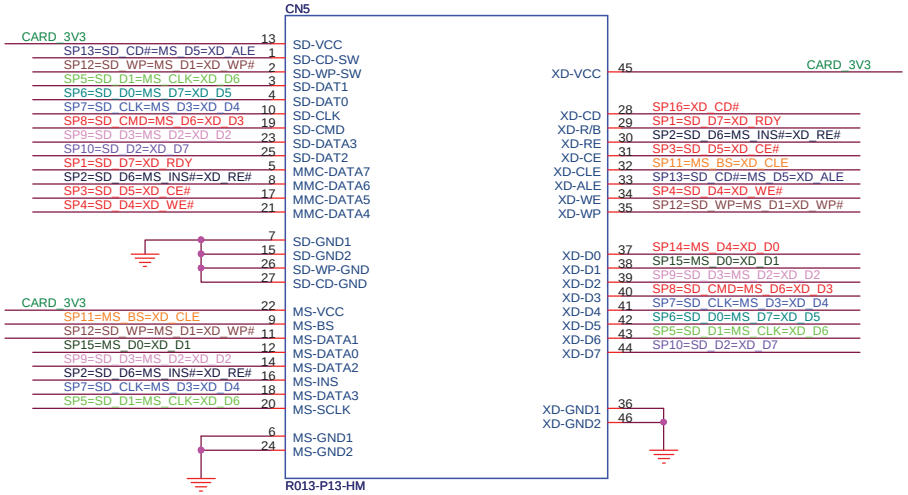
XD,MMC 4.2/SD,MS/MSP
7 IN1 CARD READER

Share Pin

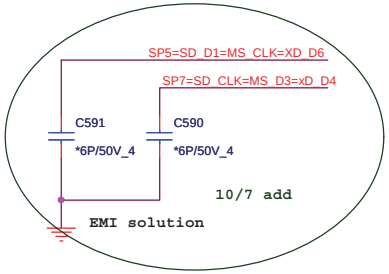
SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#

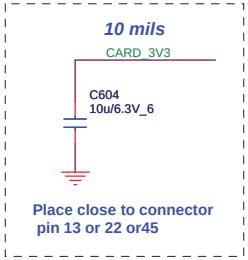


10/7 change 0 ohm



1 : DFHS44FR012
2 : :DFHS44FR014





Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	CARD READER CONNECTOR	1A
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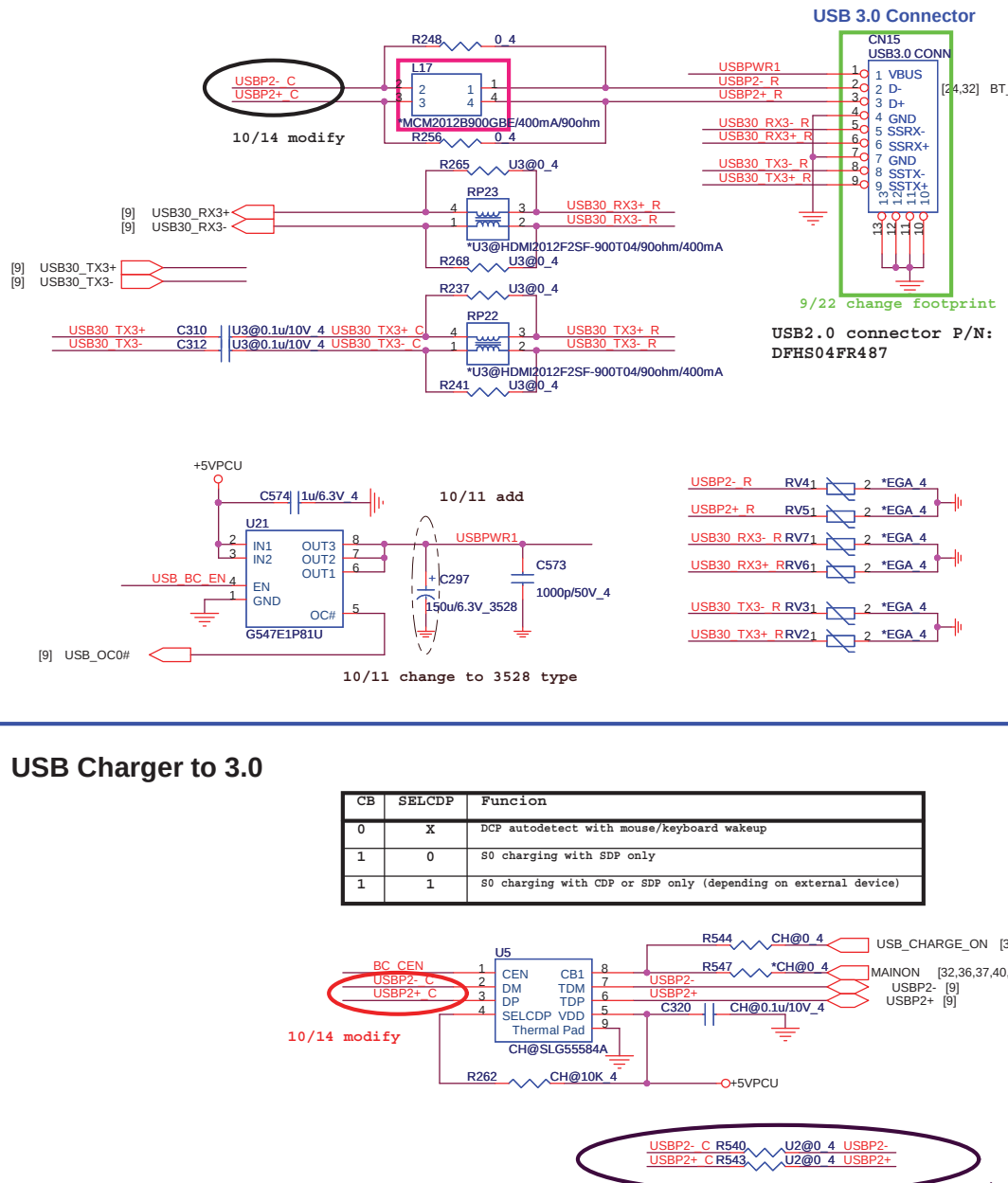
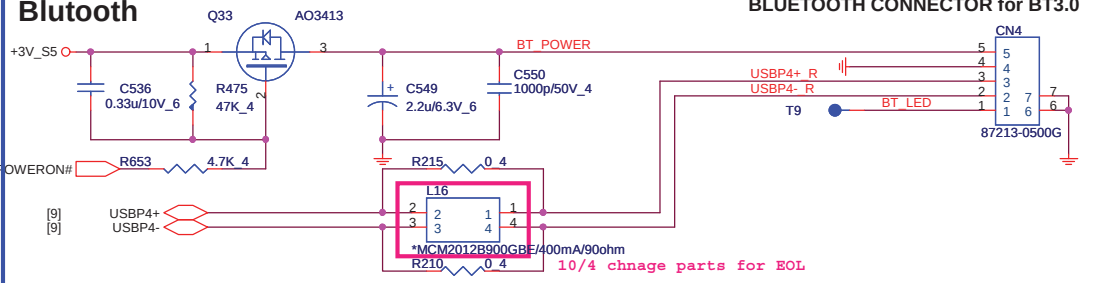
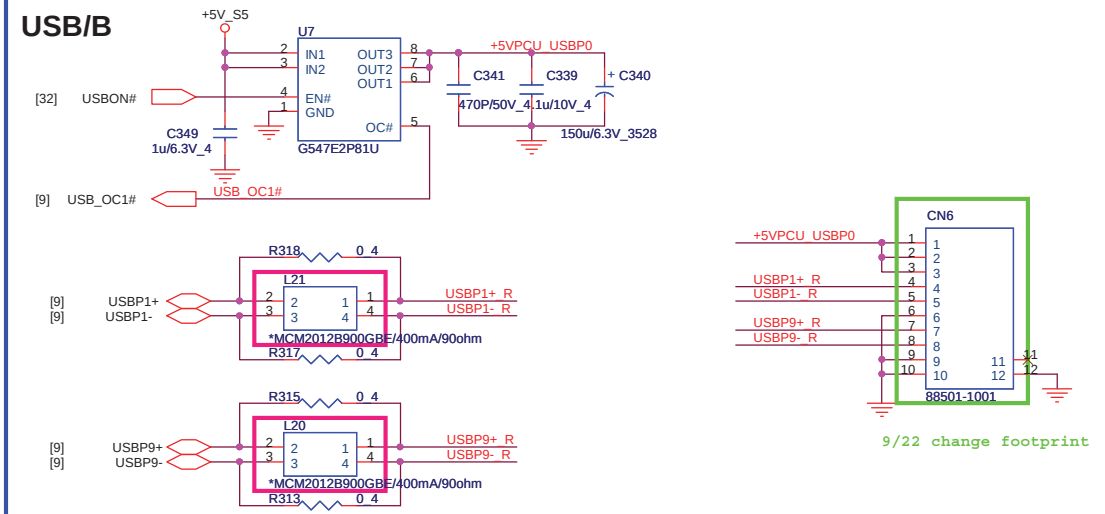
USB3.0/2.0



Blutooth



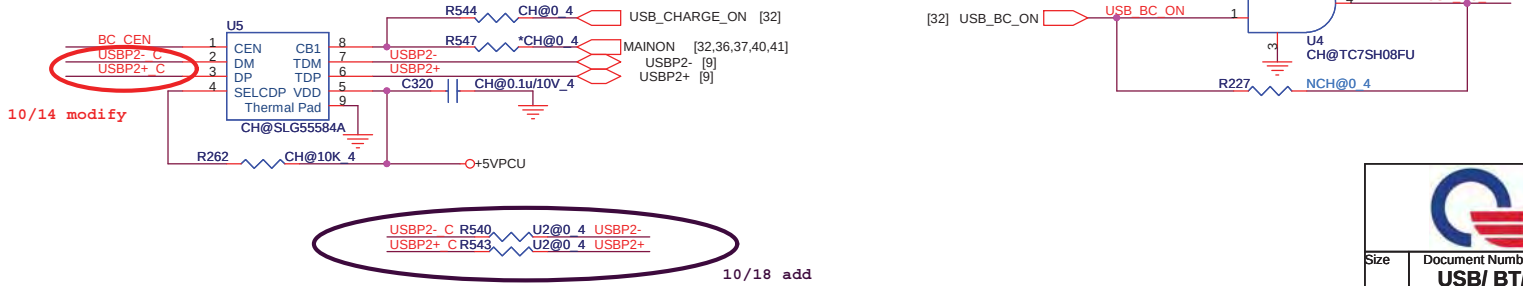
USB/B



USB Charger to 3.0

CB	SELCDP	Funcion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

USB Charger -->CH@
None Charger--> NCH@



Quanta Computer Inc.	
PROJECT : ZQTA/ZQSA	
Size	Document Number: USB/ BT/CHARGER — Rev: 1A
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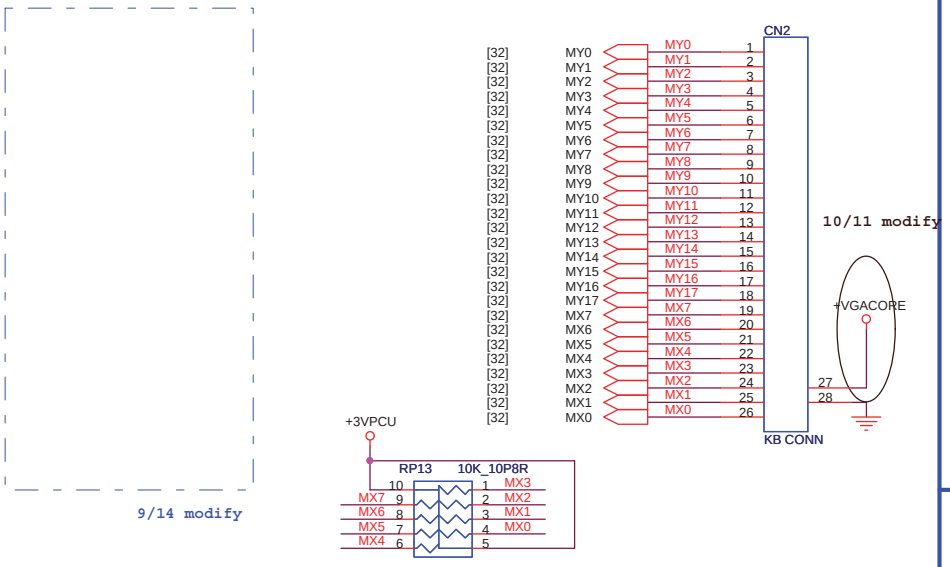
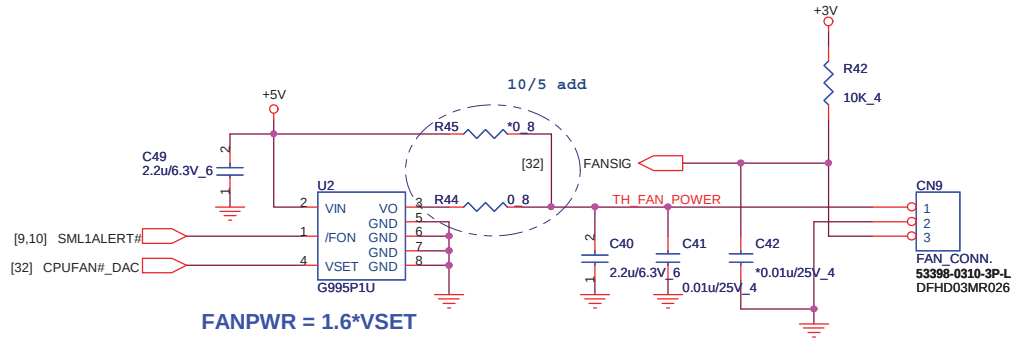
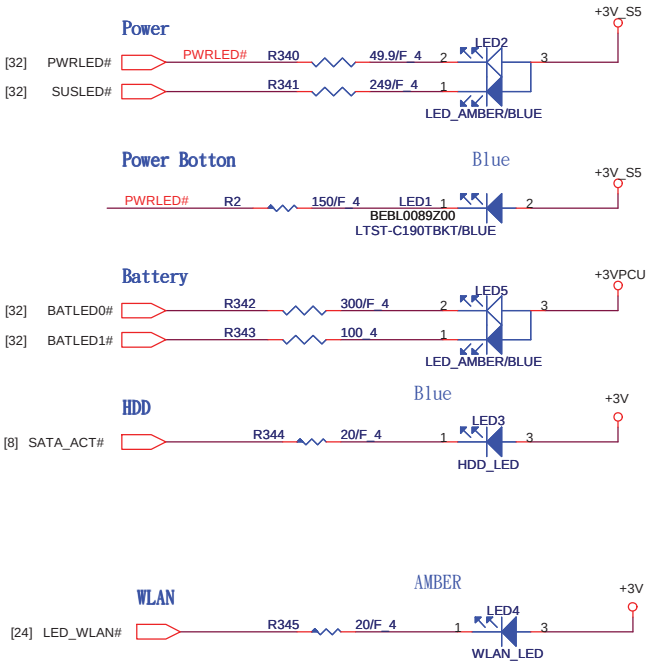
K/B



CPU FAN

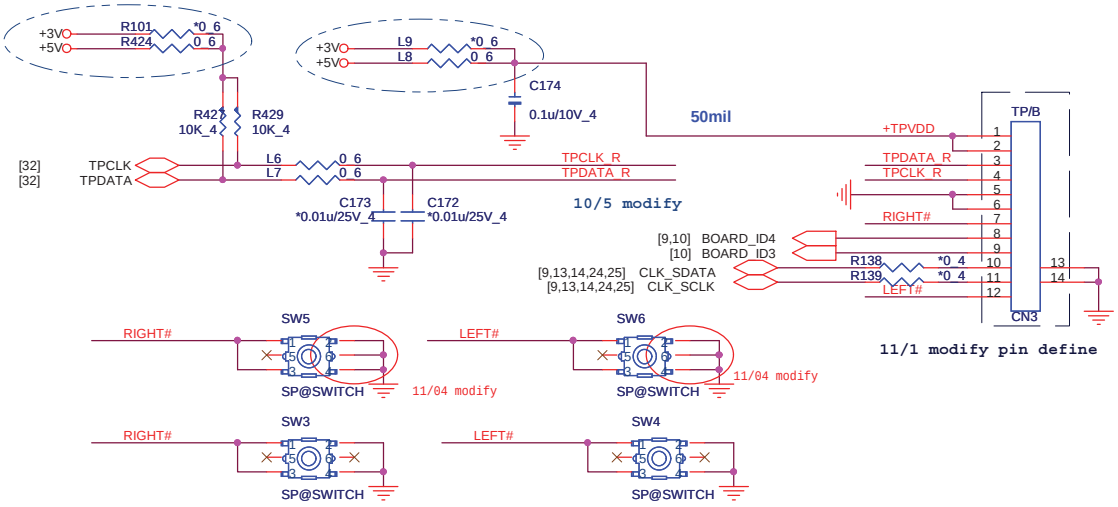


LED

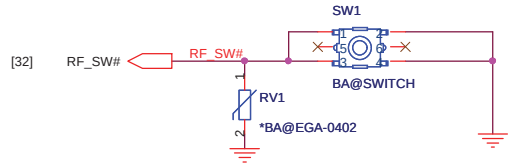


TOUCHPAD & Switch CONN.

Model EA/EG/BA---->SW3,SW4
VA/VG--------->SW5,SW6



For BA WLAN function



Quanta Computer Inc.
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	KB/FAN/TP+FP/LED	1A
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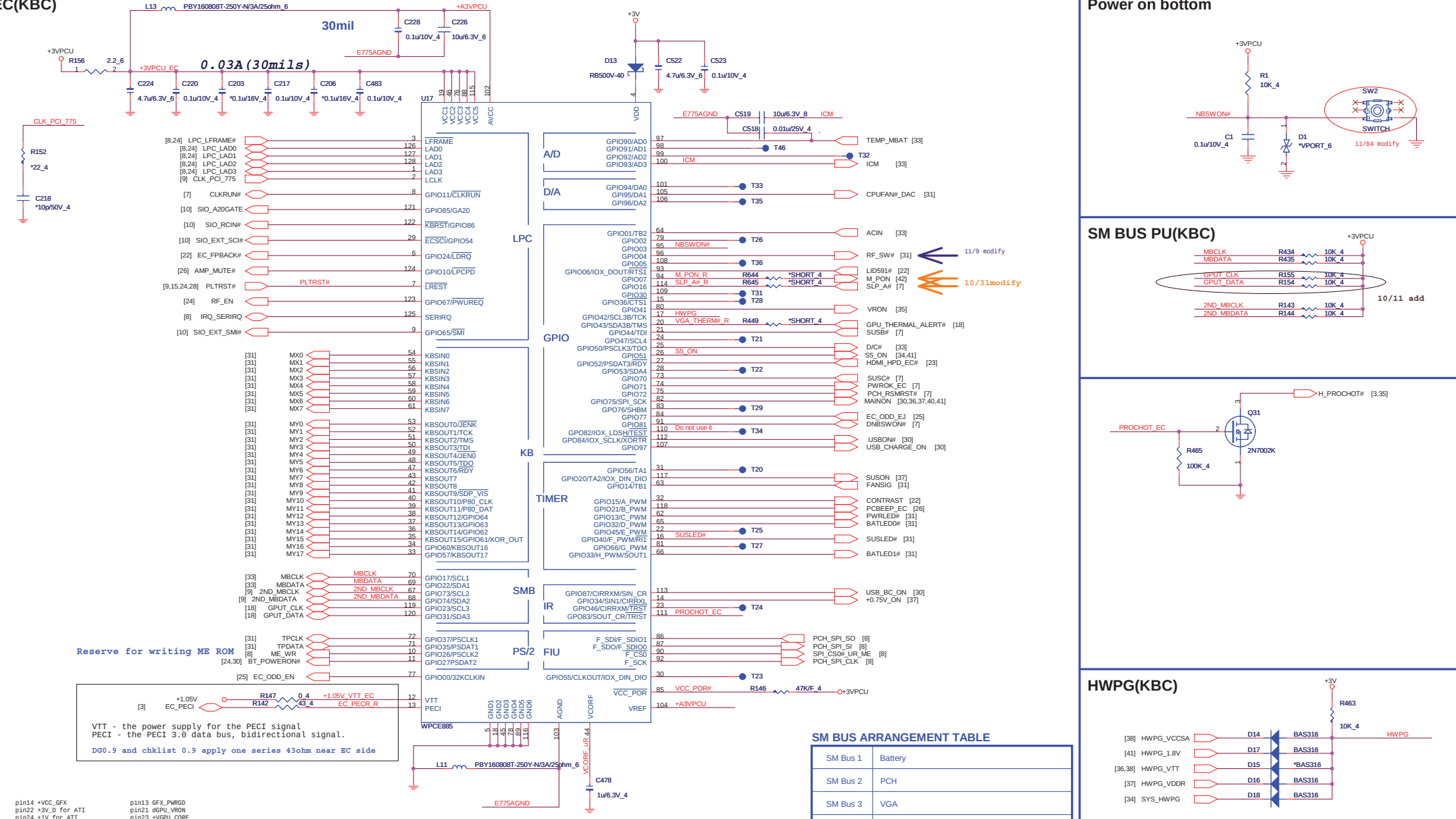
EC(KBC)



SM BUS ARRANGEMENT TABLE

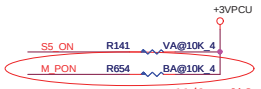
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA
SM Bus 4	HDMI

pin14 +VCC_GFX
pin22 +3V_D for ATI
pin24 +1V for ATI
pin26 +1.8V_GPU for ATI
pin28 GPU_RST#
pin13 GFX_PWRGD
pin21 dGPU_VRON
pin23 +VGPU_CORE
pin25 +1.5V_GPU
pin27 dGPU_PWROK

Power on bottom

SM BUS PU(KBC)

HWPG(KBC)



Quanta Computer Inc.			
PROJECT : ZQTA/ZQSA			
Size	Document Number		Rev
	WPCE885 & FLASH		1A
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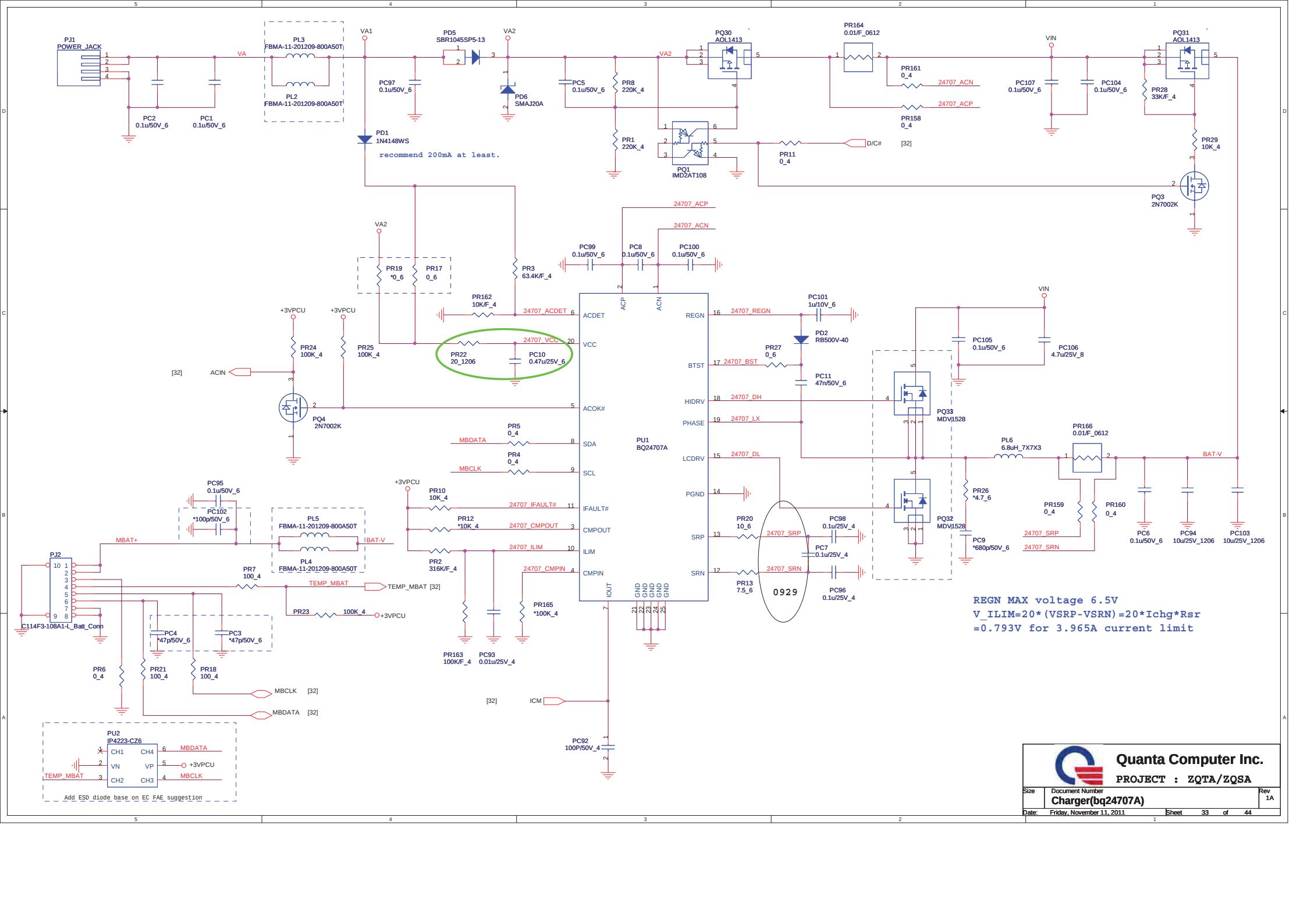
PJ1
POWER_JACK
VA
PC2
0.1u/50V_6
PC1
0.1u/50V_6
PL3
FBMA-11-201209-800A50T
PL2
FBMA-11-201209-800A50T
VA1
PC97
0.1u/50V_6
PD5
SBR1045SP5-13
VA2
PD6
SMAJ20A
PC5
0.1u/50V_6
PR8
220K_4
PR1
220K_4
PD1
1N4148WS
recommend 200mA at least.
PQ30
AOL1413
PQ1
IMD2AT108
PR164
0.01/F_0612
PR161
0_4
PR158
0_4
24707_ACN
24707_ACP
D/C#
[32]
PR11
0_4
VIN
PC107
0.1u/50V_6
PC104
0.1u/50V_6
PQ31
AOL1413
PR28
33K/F_4
PR29
10K_4
PQ3
2N7002K
24707_ACP
24707_ACN
PC99
0.1u/50V_6
PC8
0.1u/50V_6
PC100
0.1u/50V_6
PR19
*0_6
PR17
0_6
PR3
63.4K/F_4
PR162
10K/F_4
24707_ACDET
PR22
20_1206
24707_VCC
PC10
0.47u/25V_6
PR24
100K_4
PR25
100K_4
+3VPCU
[32]
ACIN
PQ4
2N7002K
ACDET
VCC
ACOK#
SDA
SCL
IFAULT#
CMPOUT
ILIM
CMPIN
IOUT
ACP
ACN
PU1
BQ24707A
REGN
BTST
HIDRV
PHASE
LCDRV
PGND
SRP
SRN
24707_REGN
24707_BST
24707_DH
24707_LX
24707_DL
24707_SRP
24707_SRN
PC101
1u/10V_6
PD2
RB500V-40
PR27
0_6
PC11
47n/50V_6
PR5
0_4
PR4
0_4
MBDATA
MBCLK
PR10
10K_4
24707_IFAULT#
PR12
*10K_4
24707_CMPOUT
PR2
316K/F_4
24707_ILIM
24707_CMPIN
PR165
*100K_4
PR163
100K/F_4
PC93
0.01u/25V_4
PR20
10_6
PR13
7.5_6
PC98
0.1u/25V_4
PC7
0.1u/25V_4
PC96
0.1u/25V_4
0929
PC95
0.1u/50V_6
PC102
*100p/50V_6
PL5
FBMA-11-201209-800A50T
PL4
FBMA-11-201209-800A50T
MBAT+
IBAT-V
PJ2
C114F3-108A1-L_Batt_Conn
PR7
100_4
TEMP_MBAT
TEMP_MBAT [32]
PR23
100K_4
+3VPCU
PC4
*47p/50V_6
PC3
*47p/50V_6
PR6
0_4
PR21
100_4
PR18
100_4
MBCLK [32]
MBDATA [32]
PU2
IP4223-CZ6
CH1
CH2
CH3
CH4
VN
VP
Add ESD diode base on EC FAE suggestion
[32]
ICM
PC92
100P/50V_4
PQ33
MDV1528
PQ32
MDV1528
PC105
0.1u/50V_6
PC106
4.7u/25V_8
PL6
6.8uH_7X7X3
PR166
0.01/F_0612
BAT-V
PR26
*4.7_6
PC9
*680p/50V_6
PR159
0_4
PR160
0_4
PC6
0.1u/50V_6
PC94
10u/25V_1206
PC103
10u/25V_1206
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
Quanta Computer Inc.
PROJECT : ZQTA/ZQSA
Size
Document Number
Charger(bq24707A)
Rev
1A
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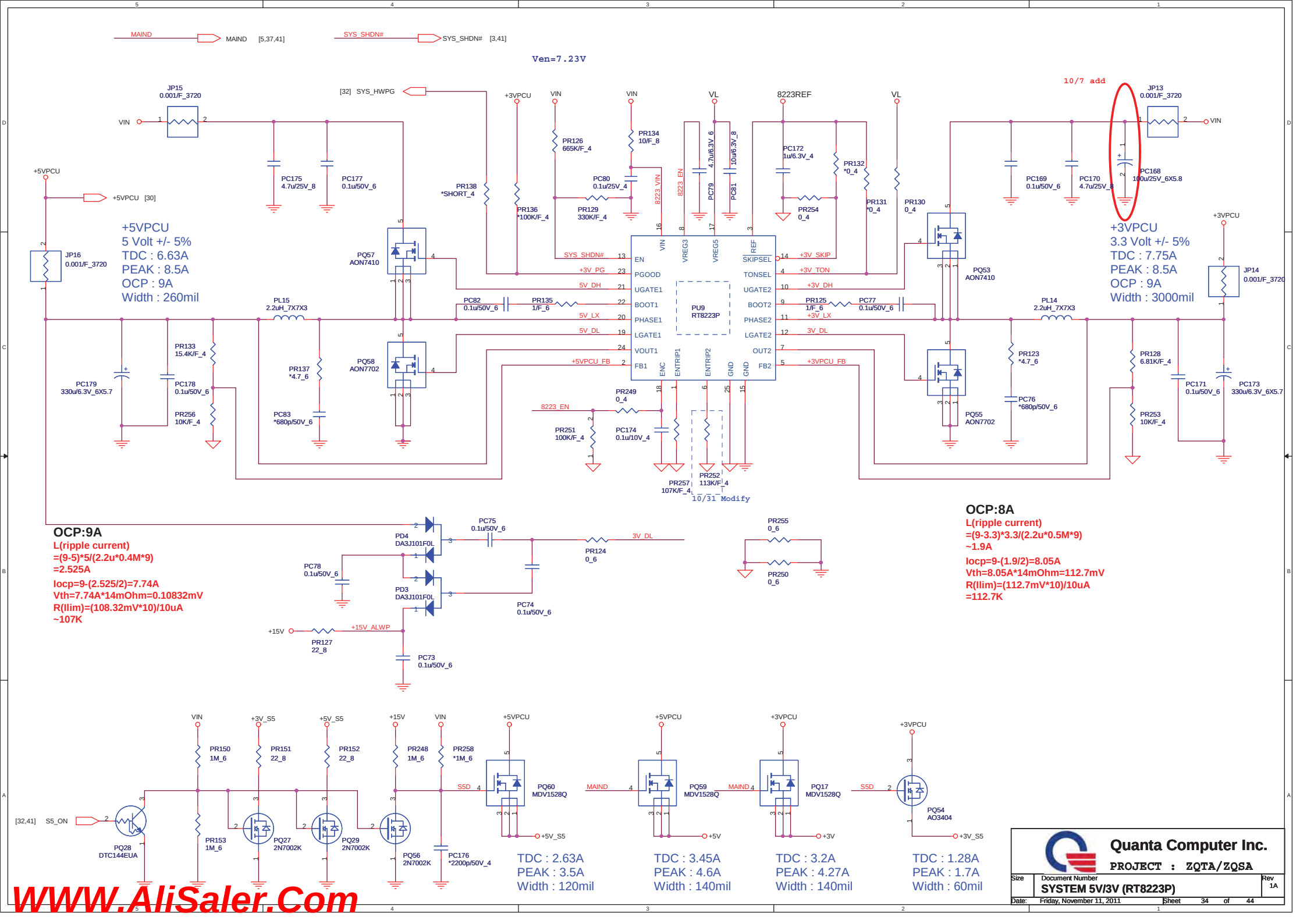

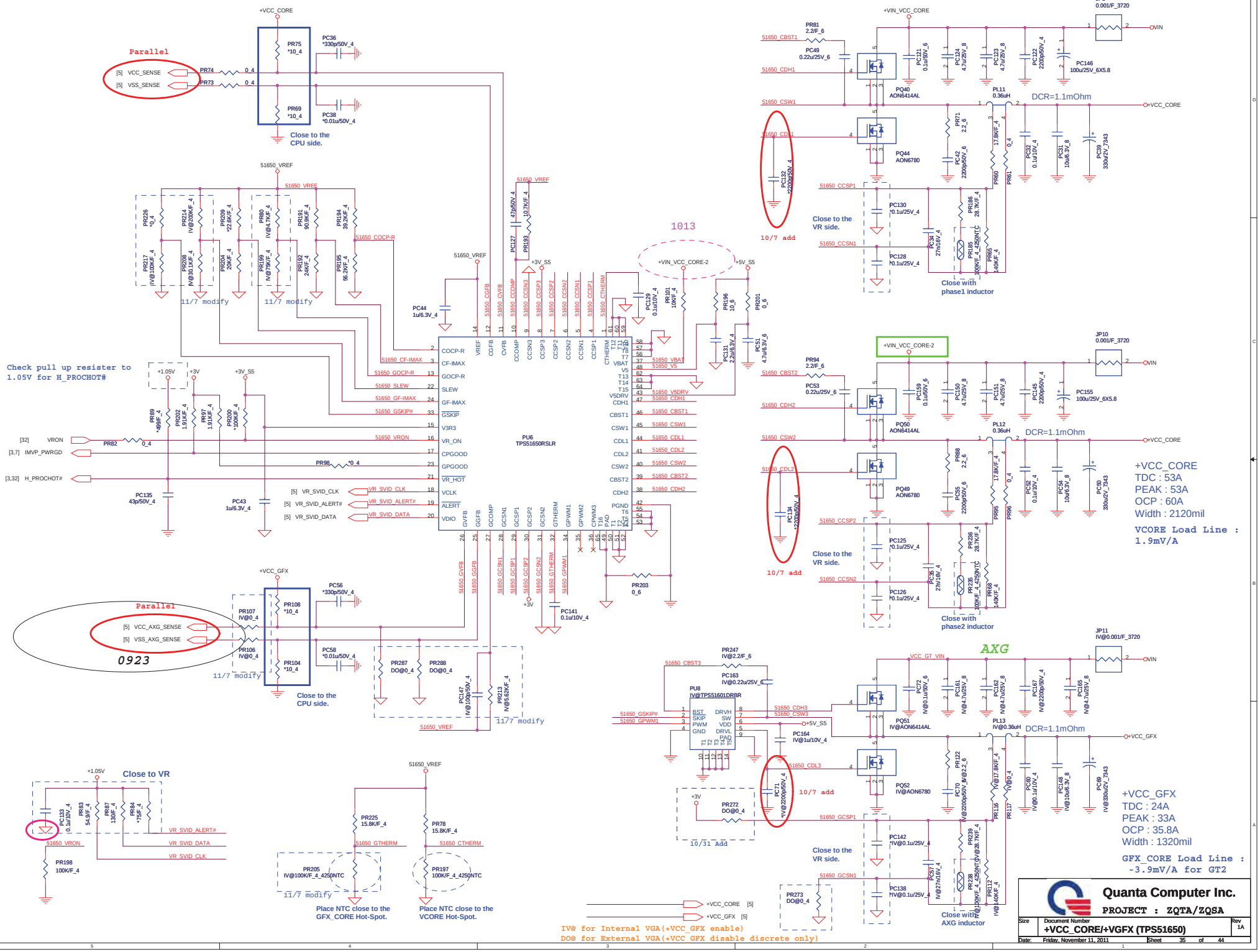
Parallel
[5] VCC_SENSE
[5] VSS_SENSE
PR74 0_4
PR73 0_4
+VCC_CORE
PR75 *10_4
PR69 *10_4
PC36 *330p/50V_4
PC38 *0.01u/50V_4
Close to the CPU side.
51650_VREF
PR226 *0_4
PR214 IV@200K/F_4
PR209 *22.6K/F_4
PR80 IV@4.7K/F_4
PR191 90.9K/F_4
PR184 39.2K/F_4
PR217 IV@100K/F_4
PR208 IV@30.1K/F_4
PR204 20K/F_4
PR199 IV@75K/F_4
PR192 24K/F_4
PR185 55.2K/F_4
51650_COCP-R
11/7 modify
11/7 modify
PC44 1u/6.3V_4
PC127 47p/50V_4
PR193 10.7K/F_4
+3V_S5
1013
+VIN_VCC_CORE-2
+5V_S5
PC129 0.1u/10V_4
PR101 10K/F_4
PR196 10_6
PR201 0_6
PC131 2.2u/6.3V_4
PC51 4.7u/6.3V_6
Check pull up resister to 1.05V for H_PROCHOT#
+1.05V
+3V
+3V_S5
PR89 *499/F_4
PR202 1.91K/F_4
PR97 1.91K/F_4
PR200 *100K/F_4
[32] VRON
[3,7] IMVP_PWRGD
[3,32] H_PROCHOT#
PR82 0_4
PR98 *0_4
PC135 43p/50V_4
PC43 1u/6.3V_4
PU6
TPS51650RSLR
51650_CF-IMAX
51650_GOCP-R
51650_SLEW
51650_GF-IMAX
51650_GSKIP#
51650_VRON
51650_VBAT
51650_V5
51650_V5DRV
51650_CDH1
51650_CBST1
51650_CSW1
51650_CDL1
51650_CDL2
51650_CSW2
51650_CBST2
51650_CDH2
[5] VR_SVID_CLK
[5] VR_SVID_ALERT#
[5] VR_SVID_DATA
PR203 0_6
PC141 0.1u/10V_4
+VCC_GFX
PC56 *330p/50V_4
Parallel
[5] VCC_AXG_SENSE
[5] VSS_AXG_SENSE
0923
PR107 IV@0_4
PR106 IV@0_4
PR108 *10_4
PR104 *10_4
PC58 *0.01u/50V_4
11/7 modify
Close to the CPU side.
PR287 DO@0_4
PR288 DO@0_4
PC147 IV@100p/50V_4
PR213 IV@5.62K/F_4
11/7 modify
51650_VREF
+1.05V
Close to VR
PC133 0.1u/10V_4
PR83 54.9K/F_4
PR87 130K/F_4
PR84 *75K/F_4
51650_VRON
PR198 100K/F_4
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
51650_VREF
PR225 15.8K/F_4
PR78 15.8K/F_4
51650_GTHERM
51650_CTHERM
PR205 IV@100K/F_4_4250NTC
PR197 100K/F_4_4250NTC
11/7 modify
Place NTC close to the GFX_CORE Hot-Spot.
Place NTC close to the VCORE Hot-Spot.
+VCC_CORE [5]
+VCC_GFX [5]
IV@ for Internal VGA(+VCC_GFX enable)
DO@ for External VGA(+VCC_GFX disable discrete only)
+VIN_VCC_CORE
PR81 2.2/F_6
PC49 0.22u/25V_6
51650_CBST1
51650_CDH1
51650_CSW1
51650_CDL1
PQ40 AON6414AL
PQ44 AON6780
PC132 *2200p/50V_4
10/7 add
PL11 0.36uH
DCR=1.1mOhm
+VCC_CORE
PR71 2.2_6
PC42 2200p/50V_6
PR60 17.8K/F_4
PR61 0_4
PC32 0.1u/10V_4
PC31 10u/6.3V_8
PC39 330u/2V_7343
51650_CCSP1
51650_CCSN1
PC130 *0.1u/25V_4
PC128 *0.1u/25V_4
PC34 27n/10V_4
PR185 100K/F_4_4250NTC
PR65 140K/F_4
PR186 28.7K/F_4
Close to the VR side.
Close with phase1 inductor
JP8 0.001/F_3720
VIN
PC121 0.1u/50V_6
PC124 4.7u/25V_8
PC123 4.7u/25V_8
PC122 220u/50V_4
PC146 100u/25V_6X5.8
+VIN_VCC_CORE-2
PR94 2.2/F_6
PC53 0.22u/25V_6
51650_CBST2
51650_CDH2
51650_CSW2
51650_CDL2
PQ50 AON6414AL
PQ49 AON6780
PC134 *2200p/50V_4
10/7 add
PL12 0.36uH
DCR=1.1mOhm
+VCC_CORE
PR88 2.2_6
PC55 2200p/50V_6
PR95 17.8K/F_4
PR96 0_4
PC52 0.1u/10V_4
PC54 10u/6.3V_8
PC50 330u/2V_7343
51650_CCSP2
51650_CCSN2
PC125 *0.1u/25V_4
PC126 *0.1u/25V_4
PC35 27n/10V_4
PR235 100K/F_4_4250NTC
PR63 140K/F_4
PR236 28.7K/F_4
Close to the VR side.
Close with phase2 inductor
JP10 0.001/F_3720
VIN
PC159 0.1u/50V_6
PC150 4.7u/25V_8
PC151 4.7u/25V_8
PC145 220u/50V_4
PC155 100u/25V_6X5.8
+VCC_CORE
TDC : 53A
PEAK : 53A
OCP : 60A
Width : 2120mil
VCORE Load Line : 1.9mV/A
AXG
PR247 IV@2.2/F_6
PC163 IV@0.22u/25V_6
51650_CBST3
51650_CDH3
51650_CSW3
51650_CDL3
51650_GSKIP#
51650_GPWM1
PU8 IV@TPS51601DRBR
BST SKIP PWM GND DRVH SW VDD DRVL PAD
+5V_S5
PC164 IV@1u/10V_4
PC71 *IV@2200p/50V_4
10/7 add
+3V
PR272 DO@0_4
10/31 Add
VCC_GT_VIN
PQ51 IV@AON6414AL
PQ52 IV@AON6780
PL13 IV@0.36uH
DCR=1.1mOhm
+VCC_GFX
PC72 IV@0.1u/50V_6
PC161 IV@4.7u/25V_8
PC162 IV@4.7u/25V_8
PC147 IV@2200p/50V_4
PC165 IV@4.7u/25V_8
PR122 IV@2.2_6
PC70 IV@2200p/50V_4
PR116 IV@17.8K/F_4
PR117 IV@0_4
PC60 IV@0.1u/10V_4
PC148 IV@10u/6.3V_8
PC69 IV@330u/2V_7343
51650_GCSP1
51650_GCSN1
PC142 *IV@0.1u/25V_4
PC138 *IV@0.1u/25V_4
PC57 IV@27n/10V_4
PR239 IV@28.7K/F_4
PR238 IV@100K/F_4_4250NTC
PR113 IV@140K/F_4
PR273 DO@0_4
Close to the VR side.
Close with AXG inductor
JP11 IV@0.001/F_3720
VIN
+VCC_GFX
TDC : 24A
PEAK : 33A
OCP : 35.8A
Width : 1320mil
GFX_CORE Load Line : -3.9mV/A for GT2
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PROJECT : ZQTA/ZQSA
Size
Document Number
+VCC_CORE/+VGFX (TPS51650)
Rev 1A
Date: Friday, November 11, 2011
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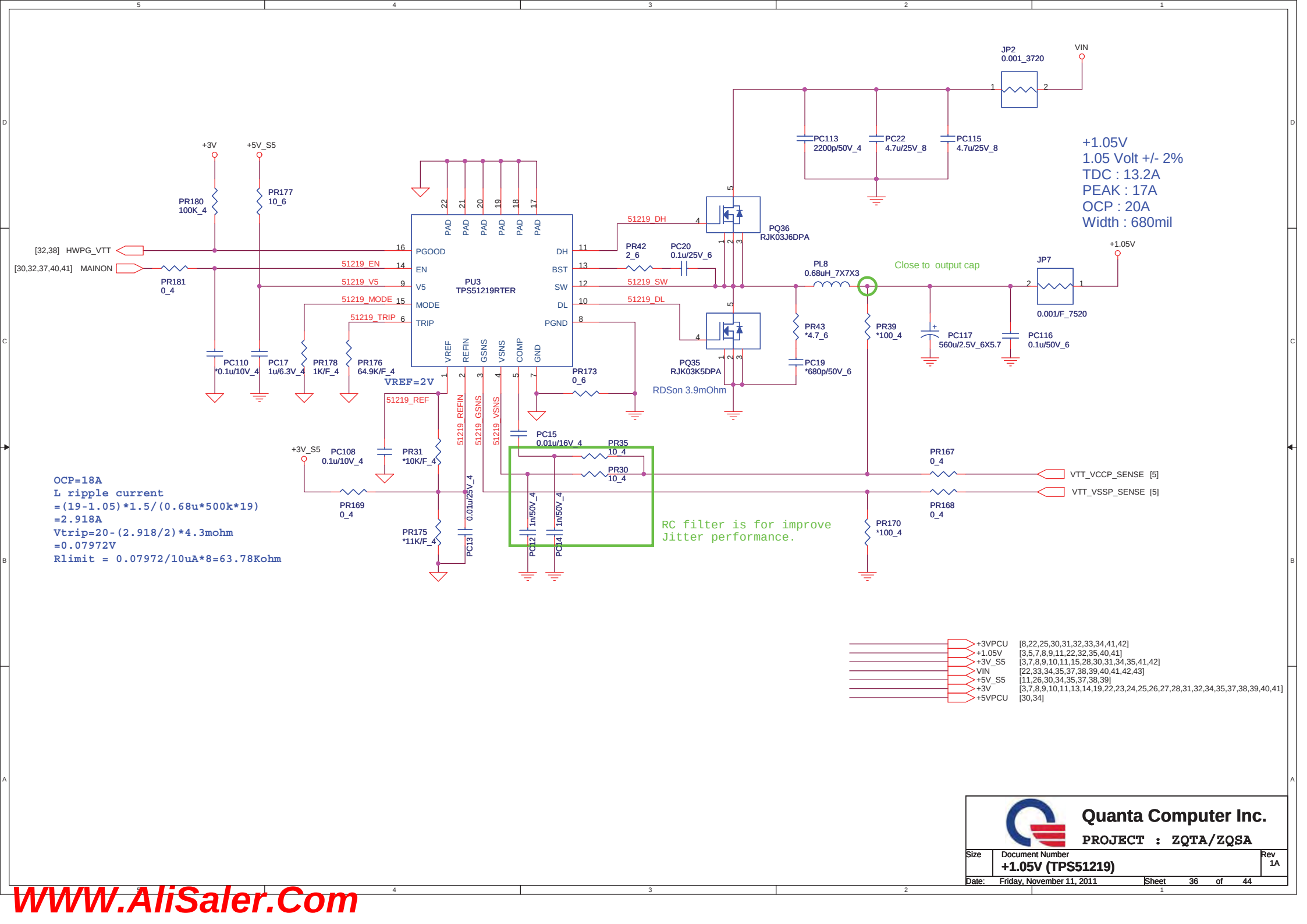

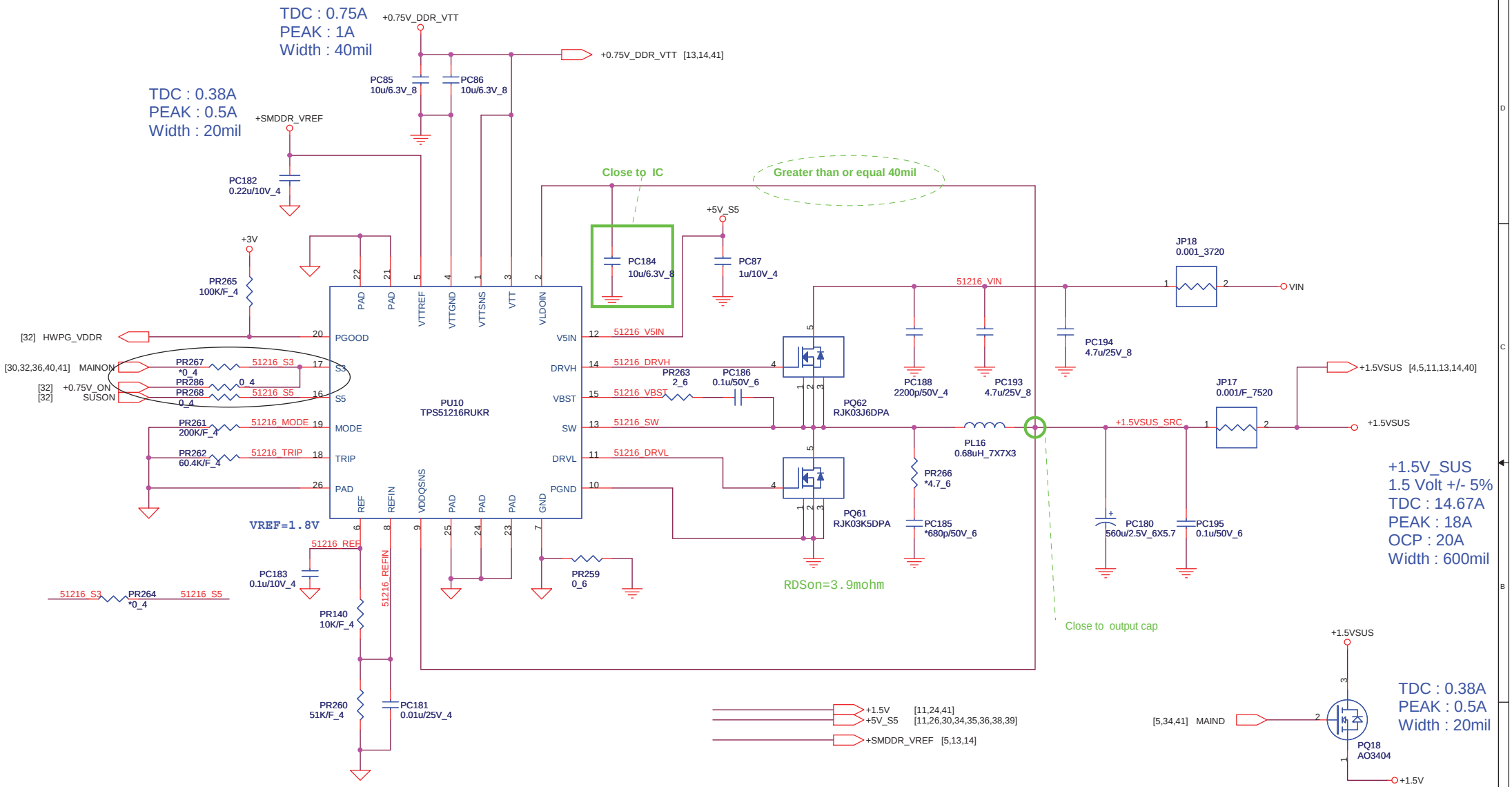

OCP=20A
L ripple current
=(19-1.5)*1.5/(0.68u*400k*19)
=5.079A
Vtrip=20-(5.079/2)*4.3mohm
=0.07508V
Rlimit=0.07508/10uA*8=60.063Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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Size	Document Number	Rev
	DDR 1.5V(TPS51216)	1A
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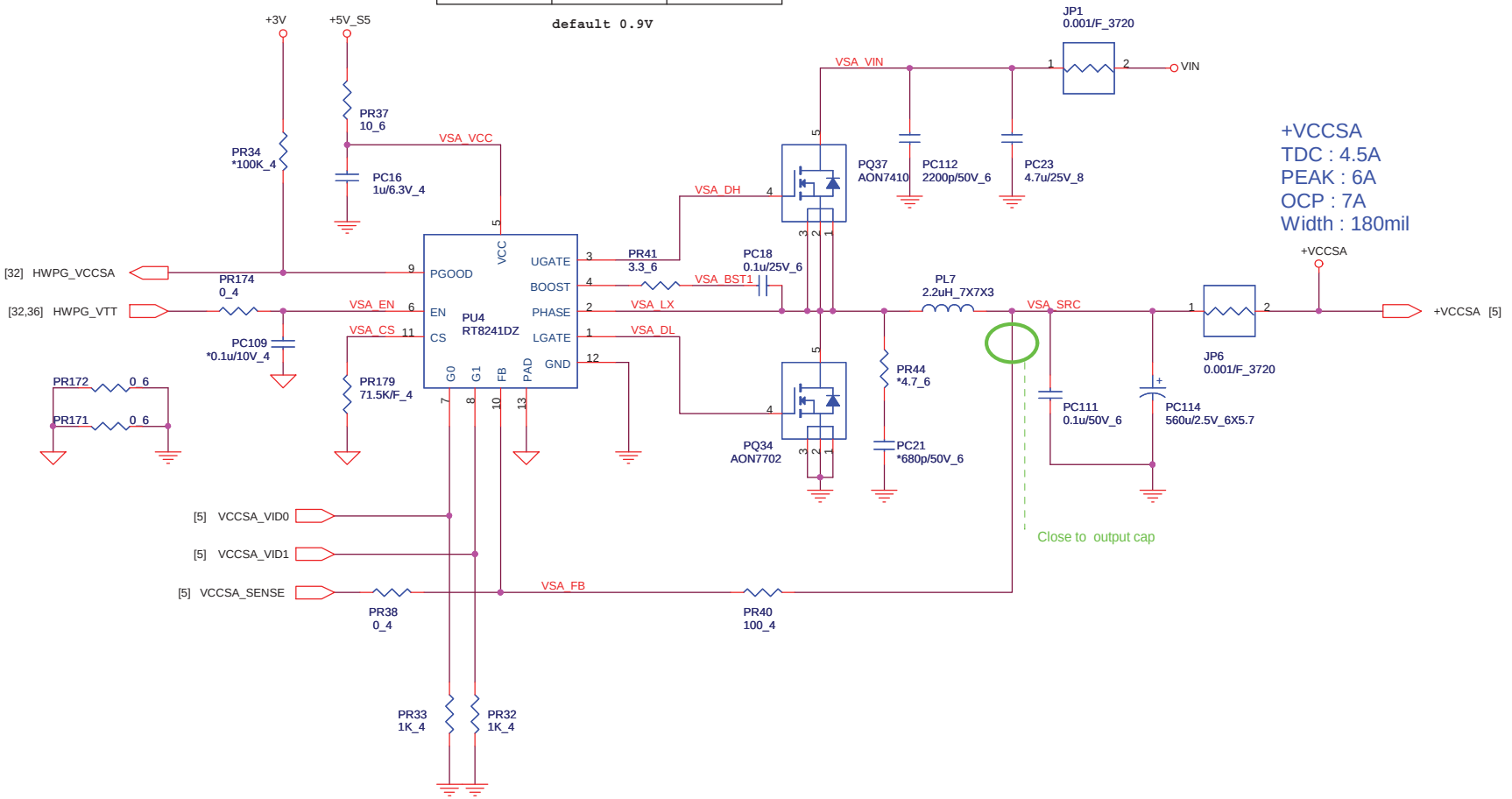
G0	G1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V



+VCCSA
TDC : 4.5A
PEAK : 6A
OCP : 7A
Width : 180mil

OCP=7A
Iripple=(19-0.9)*0.9/(2.2u*300K*19)
=1.299A
Rth=14mohm*8*(7-0.65)/10uA
=71.125K
Ipeak=8.299A

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PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	VCCSA(RT8241DZ)	1A
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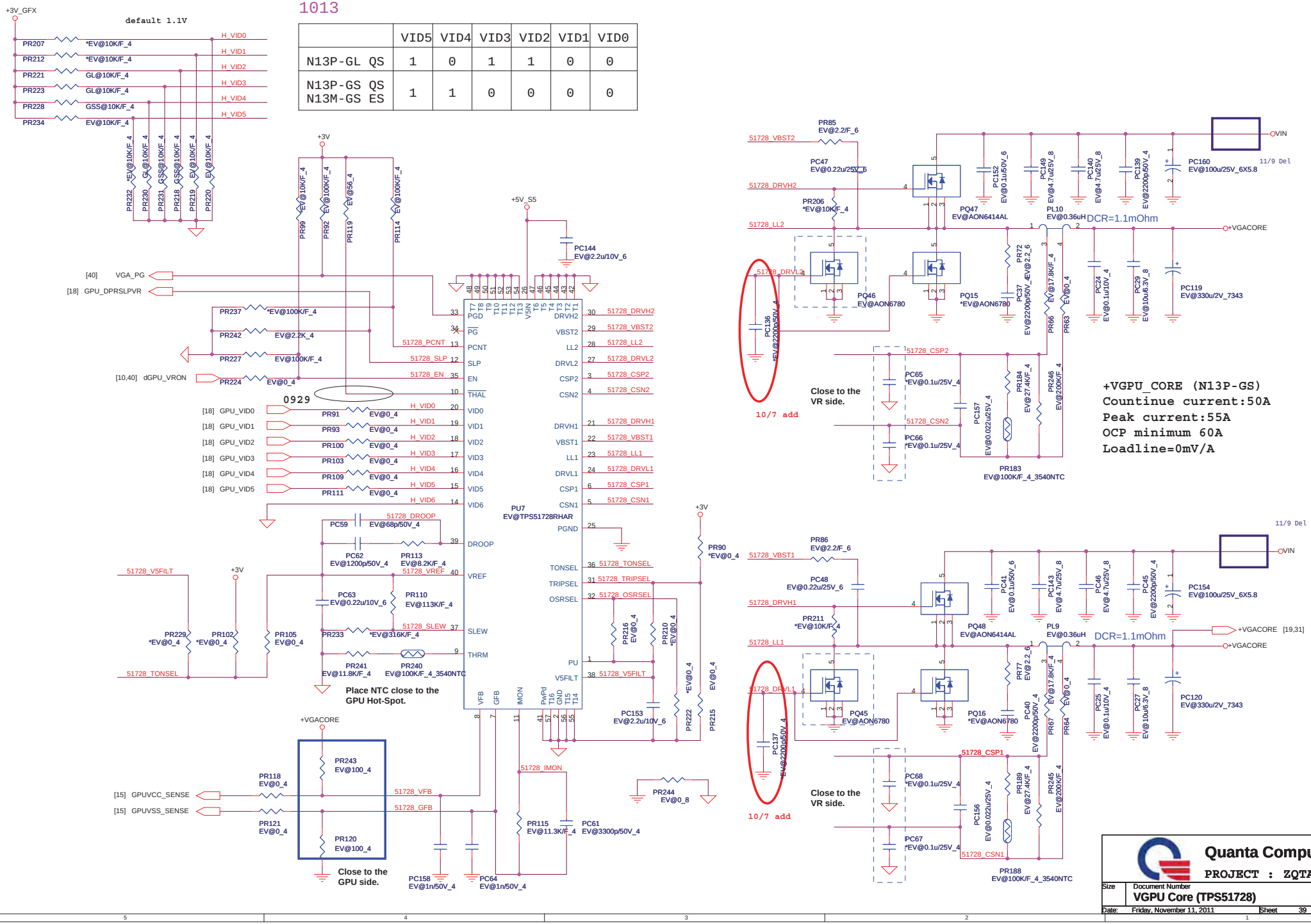
1013

	VID5	VID4	VID3	VID2	VID1	VID0
N13P-GL QS	1	0	1	1	0	0
N13P-GS QS N13M-GS ES	1	1	0	0	0	0



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PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	VGPU Core (TPS51728)	1A

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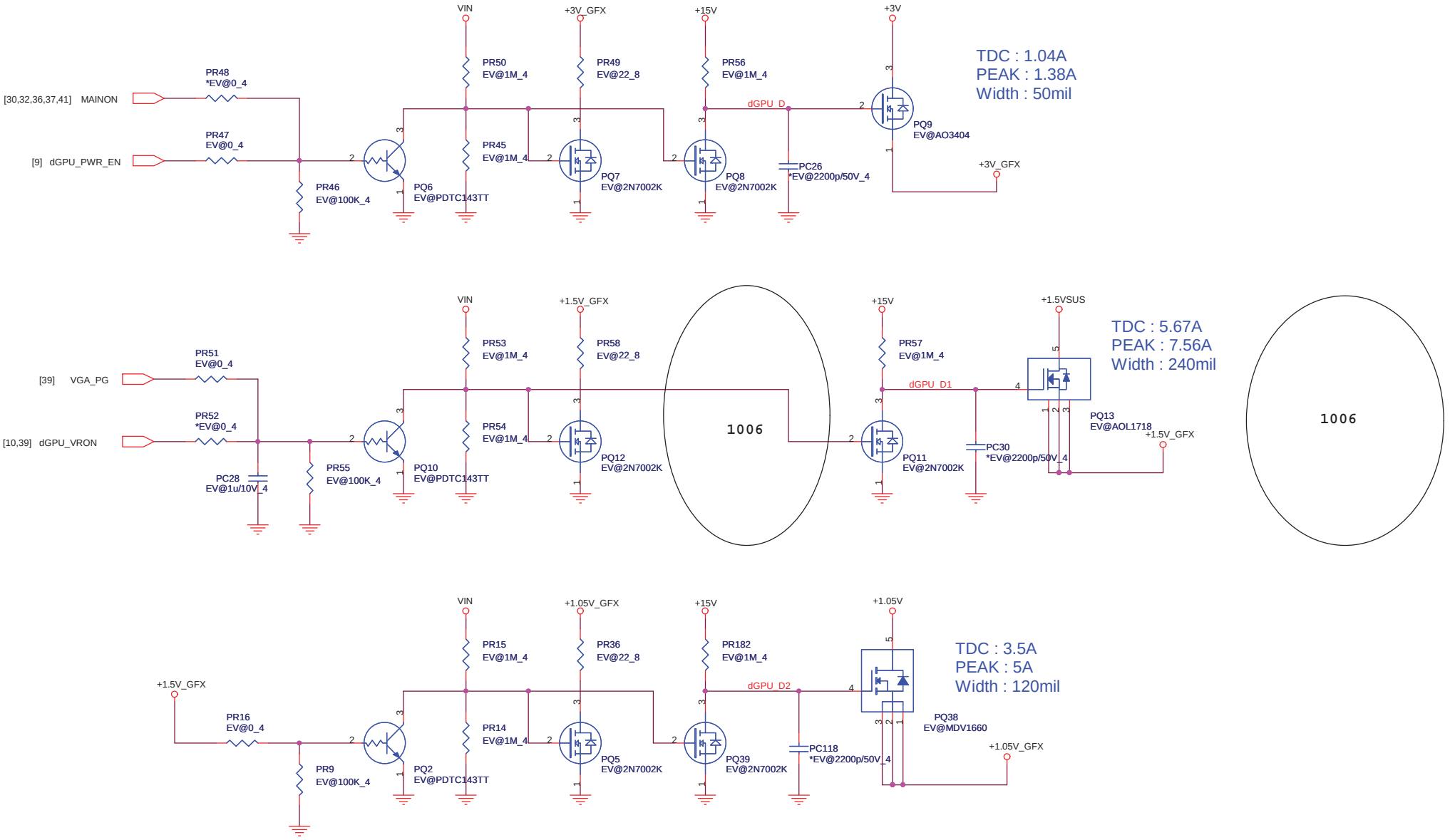

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PROJECT : ZQTA/ZQSA		
Size	Document Number: GPU_PWR	Rev: 1A
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+1.8V
1.8 Volt +/- 5%
TDC : 1.61A
PEAK : 2A
Width : 60mil

+3VPCU
PC187 10u/6.3V_8
PC190 0.1u/25V_4
PU11 TPS54318RTER
VIN PH BOOT PWRGD GND AGND VSNS COMP RT/CLK SS PAD
[30,32,36,37,40] MAINON
PR154 *100K/F_4
PC89 1000p/50V_4
54418-1_VFB
PR271 10K/F_4
PR270 121K/F_4
PC192 *100p/50V_4
PC196 1200p/50V_4
PC191 0.01u/25V_4
PR269 0_6
PC189 0.1u/50V_6
PL1 1uH_7X7X3
HWPG_1.8V [32]
PR155 *100K/F_4
+3V_S5
+1.8V
JP5 0.001/F_3720
R1
PR157 100K/F_4
PC88 0.1u/25V_4
PC90 10u/6.3V_8
PC91 10u/6.3V_8
54418-1_VFB
R2
PR156 78.7K/F_4
V0=0.8*(R1+R2)/R2

Thermal protection

VIN
PD7 DA2J10100L
PR190 1M_6
PQ41 AO3409
[32,34] S5_ON
S5_ON
PQ42 DTC144EUA
PR59 0_6
VL VL
PR70 1.74K/F_4
PR76 200K/F_4
PR187 10K_6_NTC
2.469V
PC166 0.1u/50V_6
PR62 200K_6
PU5A BA10393F
PR79 200K/F_4
PC33 0.1u/50V_6
S5_ON
PQ43 2N7002K
PQ14 2N7002K
SYS_SHDN# [3,34]
PU5B BA10393F

VIN +3V +5V +0.75V_DDR_VTT +1.5V +1.05V +1.8V +15V
PR143 1M_4
PR146 22_8
PR145 22_8
PR148 22_8
PR147 22_8
PR144 22_8
PR149 22_8
PR139 1M_4
[3,5] MAINON_ON_G
MAINON_ON_G
MAIND
MAIND [5,34,37]
MAINON
PQ19 DTC144EUA
PR142 1M_4
PR141 *100K/F_6
PQ22 2N7002K
PQ21 2N7002K
PQ25 2N7002K
PQ24 2N7002K
PQ20 2N7002K
PQ26 2N7002K
PQ23 2N7002K
PC84 *2200p/50V_4
[13,14,37] +0.75V_DDR_VTT

For EC control thermal protection (output 3.3V)

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Size	Document Number	Rev
	+1.8V/Discharge/Thermal	1A

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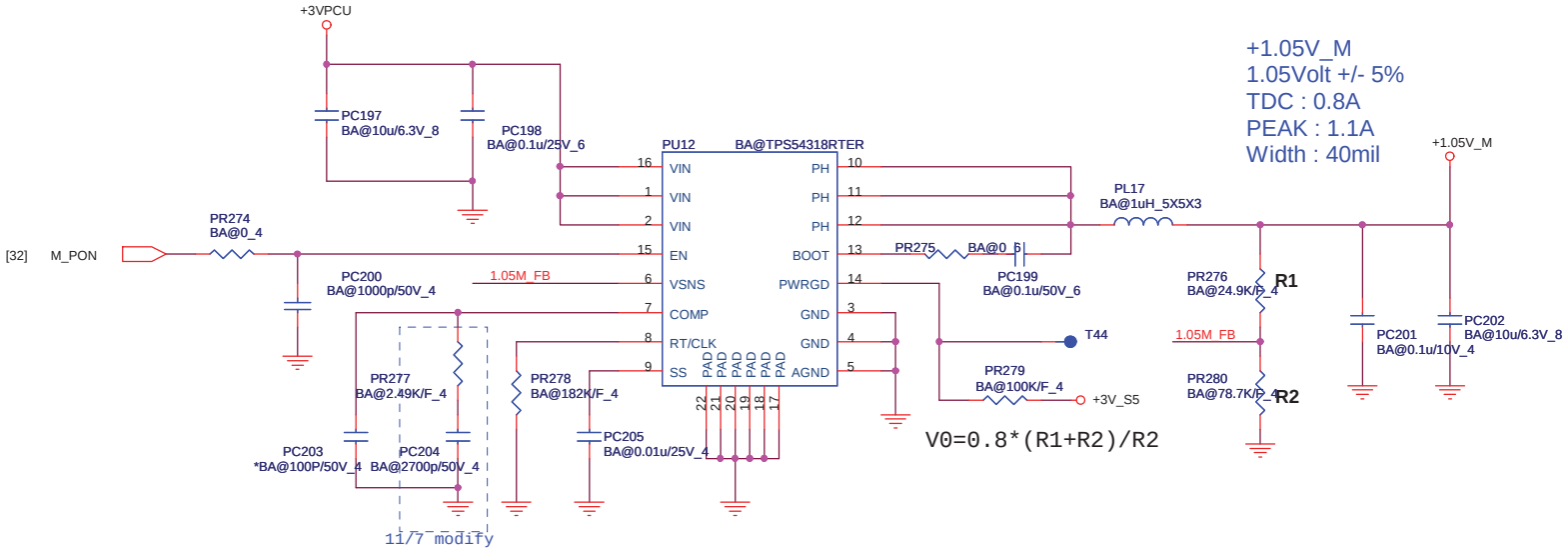

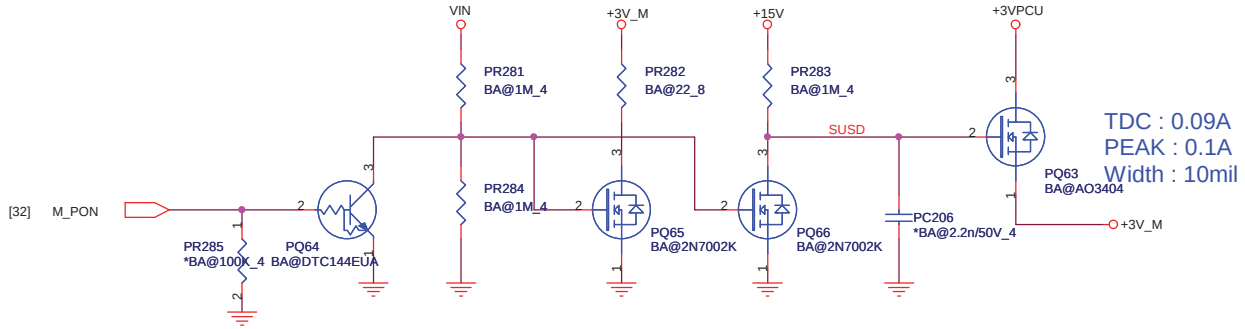

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PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	+1.05V_M/+3V_M	1A
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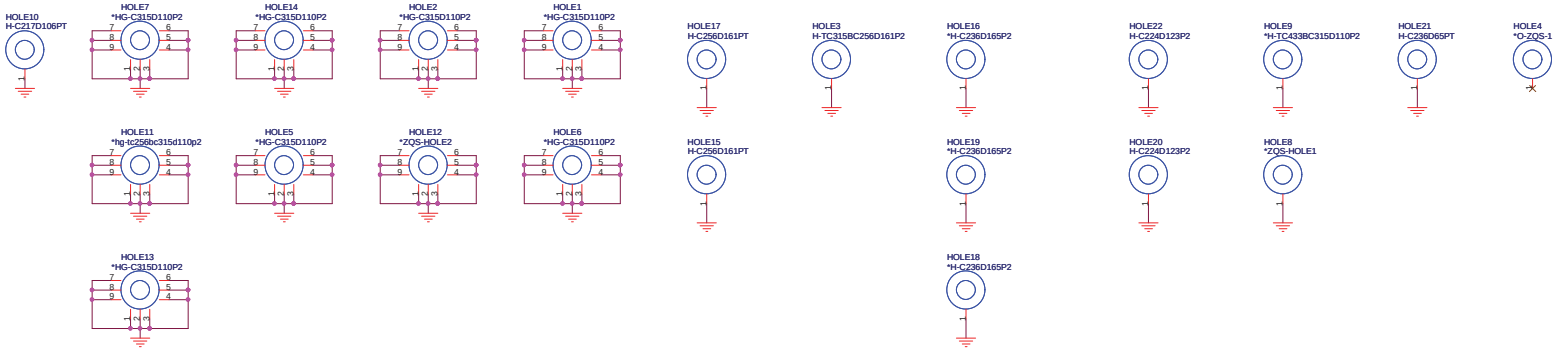
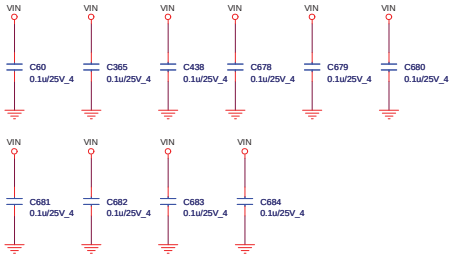
Hole





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PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	Hole	1A

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Model	date	CHANGE LIST
ZASA/ZSQTA	9/26	page3 : add R511,R525,R527,R528,R529 for Discrete Only &PCH_JTAG_TDO net change pull-up from +3V_S5 to +1.05 rail
	9/27	Update power circuit Page19 : add C3777,C3778
	9/30	Page18 : add Q3508 for U7 GPU_THERMAL_ALERT net Page31 : Del CN1
	10/3	Page18 : add dGPU_ACDC# net to U7 GPIO04 & add R347 Page22 : add R557,R554 to pull-down & R548,R547 stuff for Discrete only Page25 : add R3693,C116 for ODD zero power circuit
	10/4	Page31 : CN8 add board id3 & board id4 net for touch pad ID control
	10/5	Page31 : CN8.2,CN8.3 add CLK_SDATA & CLK_SCLK net for touch pad & add R278,R279 Page15 : U41 Power rail change to +3V_GFX Page24 : Del Q16 no't support wake up function Page18 : add Q3509 for dGPU_ACDC# net Page31 : add L35,R3694,R3695 for touch pad 5V & 3V option & add R297,R295 Fan PWR option
	10/6	Page17 : IFPAB_PLLVDD rail change from +1.8V_GFX to +3V_GFX Page27 : U6 change footprint Page39 : PWR engineer add PQ3006,PQ3005 Page40 : PWR engineer Del PR193,PQ51,PQ54
	10/7	Page16 :add C3779,C3780 Page29 :add C542,C530 for EMI solution & C544 change to 4.7u 0603 type Page35 :PWR engineer add PC3037,PC3038,PC3039 Page35 :PWR engineer add PC3035,PC3036
	10/11	Page8 :add R376,R381,R393,R407,R421,R434 for Dual SPI ROM Page9 :U13 power rail change to +3V Page10 :SV_DET_NC net add R250 to pull-down Page27 :add R133,R235 Page30 :C443 change to 3528 type & add C366,R340 Page31 :CN2.27 pin change to +VGACORE Page32 :add R330,R328 pull-up +3VPCU for GPUT_CLK,GPUT_DATA net
	10/14	Page20 :add C3781,C3782,R3569,R3570,R3571,R3576 Page21 :add C3783,C3784,R3577,R3578,R3579,R3581

Quanta Computer Inc. PROJECT : ZQTA/ZQSA Size: Document Number: Change list; Rev: 1A Date: Friday, November 11, 2011; Sheet 44 of 44	DOC NO.	PROJECT MODEL :	ZQTA/ZQSA	APPROVED BY:	DATE:
		PART NUMBER:		DRAWING BY:	REVISON: