Compal Confidential

A4WAS MB Schematic Document

LA-C611P

Rev: 1.0

2015.07.17

DAX

Part Number	Description
DAZ1DR00100	PCB A4WAS LA-C611P LS-C341P

A4WAS_PCB_REV10

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DP x 2 lanes

HDMI Conn.

HDMI
PS8407A
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DDI2
HDMI x 4 lanes

eDP

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eDP

DDI

Intel Skylake U

Skylake U
Skylake PCH-LP(MCP)
(SKL-U_2+2)

Processor

Dual Core + GT2

15W
1356pin BGA
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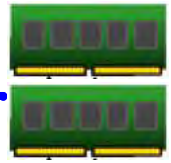
Memory BUS
Dual Channel
1.35V DDR3L 1333/1600

Interleaved Memory



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PCIe 1.0
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port 5

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6.0 Gb/s
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(SATA0)

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CLK=24MHz

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Touch Pad
PS2 (from EC) / I2C (from SOC)

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Title: Block Diagrams

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BOM Structure Table

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
EMC requirement	EMC@
EMC requirement depop	@EMC@
CODEC(ALC255)	255@
CODEC(ALC283)	283@
SPI ROM 8M*2	8M_DUAL@
SPI ROM 8M*1	8M_SINGLE@
UMA only	UMA@
TPM	TPM@
For Intel CMC	CMC@
For ES Sampel Only	ES@
Keyboard backlight	KB@
LPC MODE for EC	LPC@
ESPI MODE for EC	ESPI@
BA Serial	BA@
EA Serial	HDD@

BOM Option Table	
Item	BOM Structure
dGPU	VGA@
N16S-GT	SGT@
N16V-GM SKU	VGM@
GPU CG6 / Non GC6	NGC6@ / GC6@
VRAM BOM Select	X76@/X7601@ ~ X7614@
Single/Dual Rank	SR@/DR@
Memory Door/ No Memory Door	MDY@/ MDN@
DMIC*1	1DMIC@
DMIC*2	2DMIC@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
CPU Code	PreES:QH7Y@ ES:QHMF@, QHMG@ QS:QJFC@, QJ8N@, QJ8L@ MP:SR2EU@, SR2EY@, SR2EZ@

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)	Reserved (Touch Panel)			
I2C_1 (+3VS)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x15		
SOC_SMBCLK +3VS	DIMM1	0xA0		
	DIMM2	0xA4		
	LIS3DHTR(G-Sensor)	0x30		
SOC_SML1CLK +3VS	N16S-GT (VGA)	0x9E		
	PCH-LP (SOC)	0x90		
EC_SMB_CK1 +3VLP	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.675VS_VTT	DDR +0.675VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.35V_VDDQ	DDRIIIL +1.35V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF
+VGA_CORE	Core power for descrete GPU	ON	OFF	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.

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Title: Notes List

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Title: **Power Map**

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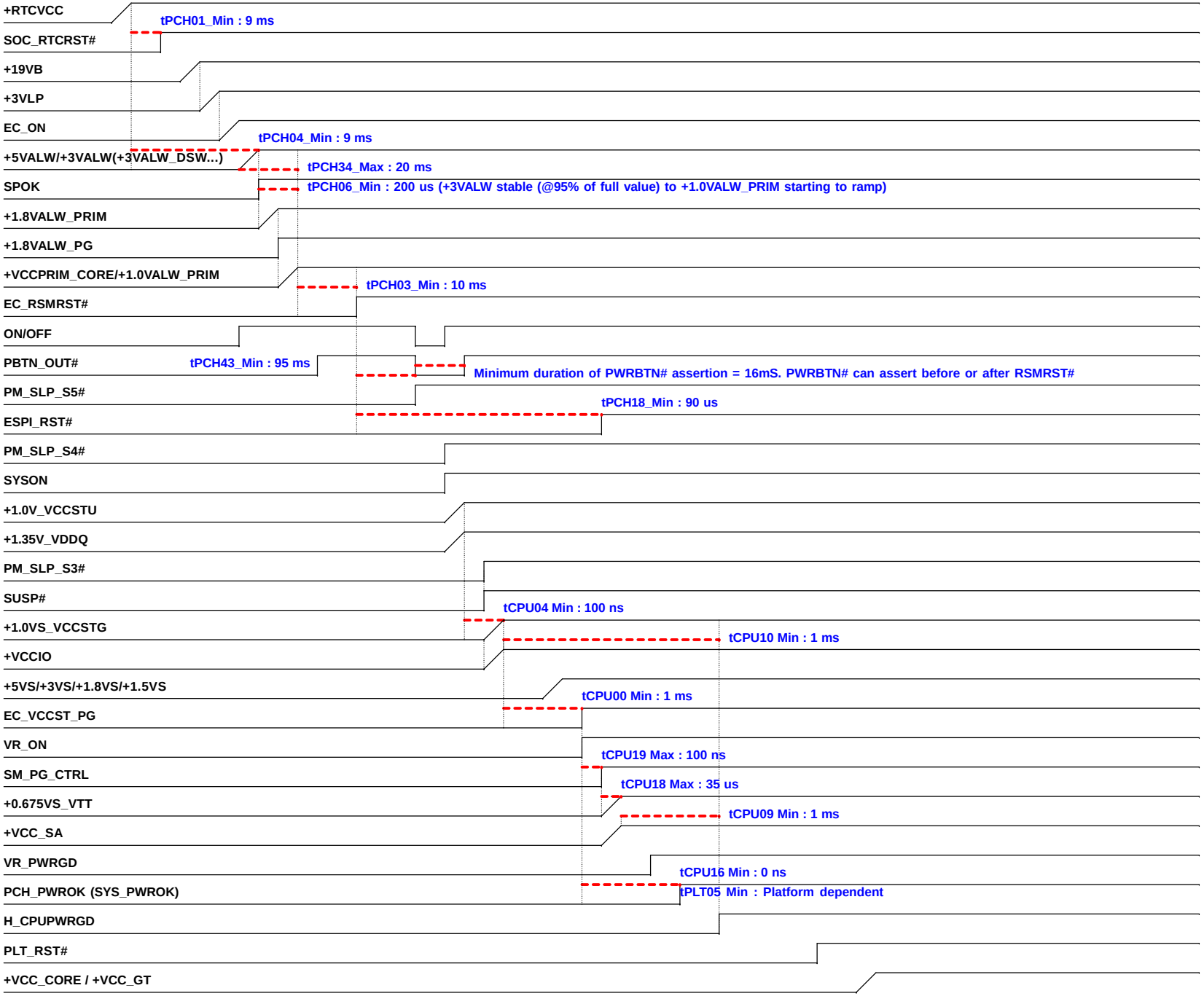
PWR Sequence_SKL-U2+2_DDR3L_NON CS



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Compal Electronics, Inc.

Title: Power Sequence

Size	Document Number	Rev
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Functional Strap Definitions

#543016 PDG0.9 P.775

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port is not detected.
1 =Port is detected.

COMPENSATION PU FOR eDP

+VCCIO — RC1 1 — 2 EDP_COMP 24.9_0402_1%

#543016 PDG0.9 P.186
Trace width=20 mils,Spacing=25mil,Max length=100mils

SPI touch RST follow CRB #544669 P.8

+1.0V_VCCST — RC2 1 — 2 H_THERMTRIP# 1K_0402_5%

#543016 PDG0.9 P.753
PH 1K to VCCST
CPU over 130 degree will output low force S0->S5

+3VS — RC157 1 — 2 100K_0402_5% TP_INT#

CC52 @EMC@ .1U_0402_16V7K 2 1 H_PECI
CC53 @EMC@ .1U_0402_16V7K 2 1 H_PROCHOT#_R
Reserved for ESD 2014/9/17

<DP to VGA>

31 SOC_DP1_N0 — E55 DDI1_TXN[0]
31 SOC_DP1_P0 — F55 DDI1_TXP[0]
31 SOC_DP1_N1 — E58 DDI1_TXN[1]
31 SOC_DP1_P1 — F58 DDI1_TXP[1]
G53 DDI1_TXN[2]
F56 DDI1_TXP[2]
G56 DDI1_TXN[3]
DDI1_TXP[3]

<HDMI>

30 SOC_DP2_N0 — C50 DDI2_TXN[0]
30 SOC_DP2_P0 — D50 DDI2_TXP[0]
30 SOC_DP2_N1 — C52 DDI2_TXN[1]
30 SOC_DP2_P1 — D52 DDI2_TXP[1]
30 SOC_DP2_N2 — A50 DDI2_TXN[2]
30 SOC_DP2_P2 — B50 DDI2_TXP[2]
30 SOC_DP2_N3 — D51 DDI2_TXN[3]
30 SOC_DP2_P3 — C51 DDI2_TXP[3]

UC1A SKL-U Rev_0.53

DDI — EDP — DISPLAY SIDEBANDS

EDP_TXN[0] C47 — EDP_TXN0 29
EDP_TXP[0] C46 — EDP_TXP0 29
EDP_TXN[1] D46 — EDP_TXN1 29
EDP_TXP[1] C45 — EDP_TXP1 29
EDP_TXN[2] A45 — EDP_TXN2 29
EDP_TXP[2] B45 — EDP_TXP2 29
EDP_TXN[3] A47 — EDP_TXN3 29
EDP_TXP[3] B47 — EDP_TXP3 29
<eDP>

EDP_AUXN E45 — EDP_AUXN 29
EDP_AUXP F45 — EDP_AUXP 29
EDP_DISP_UTIL B52

DDI1_AUXN G50 — SOC_DP1_AUXN — SOC_DP1_AUXN 31
DDI1_AUXP F50 — SOC_DP1_AUXP — SOC_DP1_AUXP 31
DP Aux (Port B for VGA)
DDI2_AUXN E48
DDI2_AUXP B48
DDI3_AUXN C46
DDI3_AUXP D46

+3VS — R4955 2 — 1 2.2K_0402_5% SOC_DP1_CTRL_DATA — L13 GPP_E18/DDPB_CTRLCLK
L12 GPP_E19/DDPB_CTRLDATA
HDMI DDC (Port C) 30 SOC_DP2_CTRL_CLK — SOC_DP2_CTRL_CLK — N7 GPP_E20/DDPC_CTRLCLK
30 SOC_DP2_CTRL_DATA — SOC_DP2_CTRL_DATA — N8 GPP_E21/DDPC_CTRLDATA
N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA
EDP_COMP — E52 EDP_RCOMP

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@

GPP_E13/DDPB_HPD0 — L9 SOC_DP1_HPD — SOC_DP1_HPD 31
GPP_E14/DDPC_HPD1 — L7 SOC_DP2_HPD — SOC_DP2_HPD 30
GPP_E15/DDPD_HPD2 — L6 EC_SCI# — EC_SCI# 38
GPP_E16/DDPE_HPD3 — N9 CPU_EDP_HPD — CPU_EDP_HPD 29
GPP_E17/EDP_HPD — L10
From VGA Trans.
From HDMI
From eDP

EDP_BKLTEN R12 — ENBKL — ENBKL 38
EDP_BKLTCTL R11 — SOC_BKL_PWM — SOC_BKL_PWM 29
EDP_VDDEN U13 — SOC_ENVDD — SOC_ENVDD 29

+3VS — RC212 10K_0402_5% 1 @ 2 — EC_SCI#
EC_SCI# SOC internal PU

+1.0VS_VCCSTG — RC3 1K_0402_5% 1 2
38,45 H_PROCHOT# — RC4 1 — 2 499_0402_1%

Reserved CATERR# for sightings issue check

@ T166 — H_CATERR# — H_CATERR# D63
H_PECI A54
H_PROCHOT#_R C65
H_THERMTRIP# C63
A65

@ T160 — XDP_BPM#0 — XDP_BPM#0 C55
@ T161 — XDP_BPM#1 — XDP_BPM#1 D55
B54
C56

+3VS — R615 1 — 2 100K_0402_5% I2C_TS_INT#
SPI touch INT follow CRB
29 I2C_TS_INT# — I2C_TS_INT# A6
38,39 EC_TP_INT# — D22 RB751V-40_SOD323-2 1 2 — TP_INT# A7
B45
AY5

RC137 2 — @ — 1 0_0402_5%
RC5 2 — 1 49.9_0402_1% CPU_POPIRCOMP — AT16
RC6 2 — 1 49.9_0402_1% PCH_OPIRCOMP — AU16
RC7 2 — 1 49.9_0402_1% EDRAM_OPIO_RCOMP — H66
RC8 2 — 1 49.9_0402_1% EOPIO_RCOMP — H65

PDG0.9 P.771
PROC_POPIRCOMP/PCH_OPIRCOMP
PD 50ohm

#544669 CRB RVP7 1.0
EDRAM_OPIO_RCOMP/EOPIO_RCOMP
PD50ohm

UC1D SKL-U Rev_0.53

CATERR# — CPU MISC — JTAG
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

PROC_TCK — B61 CPU_XDP_TCK0
PROC_TDI — D60 SOC_XDP_TDI
PROC_TDO — A61 SOC_XDP_TDO
PROC_TMS — C60 SOC_XDP_TMS
PROC_TRST# — B59 SOC_XDP_TRST#
PCH_JTAG_TCK — B56 PCH_JTAG_TCK1
PCH_JTAG_TDI — D59 SOC_XDP_TDI
PCH_JTAG_TDO — A56 SOC_XDP_TDO
PCH_JTAG_TMS — C59 SOC_XDP_TMS
PCH_TRST# — C61 SOC_XDP_TRST#
JTAGX — A59 CPU_XDP_TCK0

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SKL-U_BGA1356
@

#545659 PCH EDS 0.7 P.108
SCI capability is available on all GPIOs, while NMI and SMI capability is available on selected GPIOs only.
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:
- **GPP_B14, GPP_B20, GPP_B23**
- **GPP_C[23:22]**
- **GPP_D[4:0]**
- **GPP_E[8:0], GPP_E[16:13]**

APS CONN

+3VALW +3VALW_PRIM — JAPS1

10,38,42 PM_SLP_S3#
10 PM_SLP_S5#
10,38,42 PM_SLP_S4#
10 PM_SLP_A#
10 SOC_RTCRST# — PBTN_OUT#_R2
10 SYS_RESET#
10,38 PM_SLP_S0#
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 GND GND
ACES_50506-01841-P01
CONN@
ACES_50506-01841-P01_18P-NPM

Place to CPU side

+1.0VS_VCCSTG
RC11 2 CMC@ 1 51_0402_5% SOC_XDP_TMS
RC13 2 CMC@ 1 51_0402_5% SOC_XDP_TDI
RC15 2 CMC@ 1 51_0402_5% SOC_XDP_TDO
RC17 2 CMC@ 1 51_0402_5% SOC_XDP_TDO

CMC@ RPC2
SOC_XDP_TMS 1 — 8 XDP_TMS
SOC_XDP_TDI 2 — 7 XDP_TDI
SOC_XDP_TRST# 3 — 6 XDP_TRST#
SOC_XDP_TDO 4 — 5 XDP_TDO
0_0804_8P4R_5%

+1.0V_XDP
RC31 1 CMC@ 2 1K_0402_5% XDP_ITP_PMODE
RC43 2 @ 1 0_0402_5% XDP_PRSENT_CPU
RC46 2 @ 1 0_0402_5% XDP_PRSENT_PCH
RC35 2 CMC@ 1 51_0402_1% CPU_XDP_TCK0
RC37 2 @ 1 51_0402_5% PCH_JTAG_TCK1
RC151 2 @ 1 1K_0402_5% CFG0

Place to CPU side

17 XDP_ITP_PMODE — CFG3 XDP_ITP_PMODE — RC55 1 CMC@ 2 0_0402_5% XDP_PRSENT_CPU
RC56 1 CMC@ 2 0_0402_5% XDP_HOOK6

8 XDP_SPI_SI
8 XDP_SPI_IO2

CMC@ RPC15
XDP_SPI_SI 1 — 8 XDP_HOOK3
PCH_JTAG_TCK1 2 — 7 XDP_TCK1
CPU_XDP_TCK0 3 — 6 XDP_TCK0
XDP_SPI_IO2 4 — 5 XDP_PRSENT_PCH
0_0804_8P4R_5%

10,38 EC_RSMRST# — EC_RSMRST# — RC23 1 CMC@ 2 1K_0402_5% XDP_HOOK0

Follow 544924_Skylake_EDS_Vol_1_Rev_0.93

+3VALW_PRIM
RC9 1 CMC@ 2 1K_0402_5% XDP_SPI_SI

XDP CONN

+1.0VALW_PRIM — RC12 1 @ 2 0_0603_5% — +1.0V_XDP

JPCMC1 CMC_DEBUG_36P

OBS DATA | JTAG/RC/HOOKS

17 CFG0 — CFG0 1 — DATA_0
17 CFG1 — CFG1 3 — DATA_1
17 CFG2 — CFG2 5 — DATA_2
17 CFG3 — CFG3 7 — DATA_3
17 CFG4 — CFG4 9 — DATA_4
17 CFG5 — CFG5 11 — DATA_5
17 CFG6 — CFG6 13 — DATA_6
17 CFG7 — CFG7 15 — DATA_7
17 CFG17 — CFG17 17 — DATA_CLK_1P
17 CFG16 — CFG16 21 — DATA_CLK_1N
17 CFG8 — CFG8 2 — DATA_8
17 CFG9 — CFG9 4 — DATA_9
17 CFG10 — CFG10 6 — DATA_10
17 CFG11 — CFG11 8 — DATA_11
17 CFG12 — CFG12 10 — DATA_12
17 CFG13 — CFG13 12 — DATA_13
17 CFG14 — CFG14 14 — DATA_14
17 CFG15 — CFG15 16 — DATA_15
17 CFG19 — CFG19 18 — DATA_CLK_2P
17 CFG18 — CFG18 20 — DATA_CLK_2N

VCCOBS_AB 22 — +1.0V_XDP

XDP_TRST* 29 — XDP_TRST# 28
XDP_TDI 29 — XDP_TDI 29
XDP_TMS 30 — XDP_TMS 30
XDP_TCK0 32 — XDP_TCK0 32
XDP_TCK1 31 — XDP_TCK1 31
XDP_TDO 35 — XDP_TDO 35
XDP_PREQ* 33 — XDP_PREQ# 33 — XDP_PREQ# 12
XDP_PRDY* 34 — XDP_PRDY# 34 — XDP_PRDY# 12
HOOK_0 27 — XDP_HOOK0 27
HOOK_3 25 — XDP_HOOK3 25
HOOK_6 26 — XDP_HOOK6 26
XDP_PRSNT_PCH* 24 — XDP_PRSENT_PCH 24
XDP_PRSNT_CPU* 23 — XDP_PRSENT_CPU 23
GND 19
<MT> GND 36

INTEL_CMC_PRIMARY
CONN@

10,38 PBTN_OUT# — RC53 2 @ 1 0_0402_5% PBTN_OUT#_R2
38,39 ON/OFFBTN# — RC54 2 @ 1 0_0402_5%

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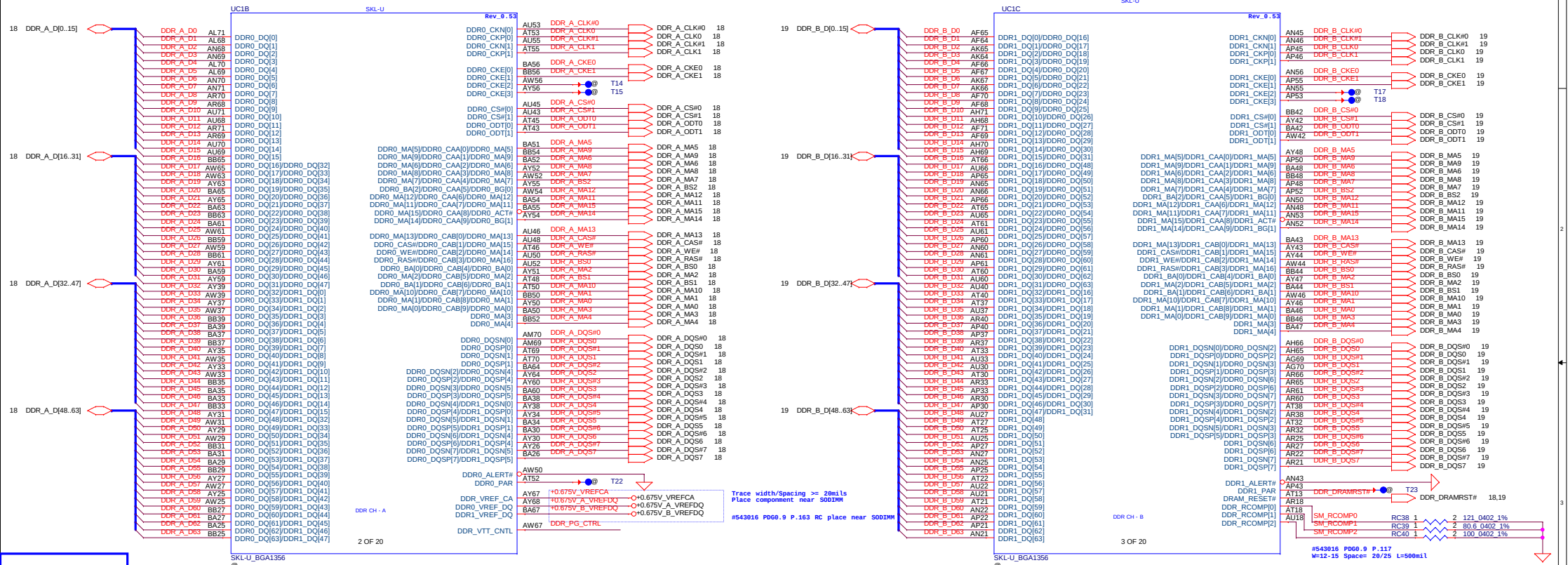
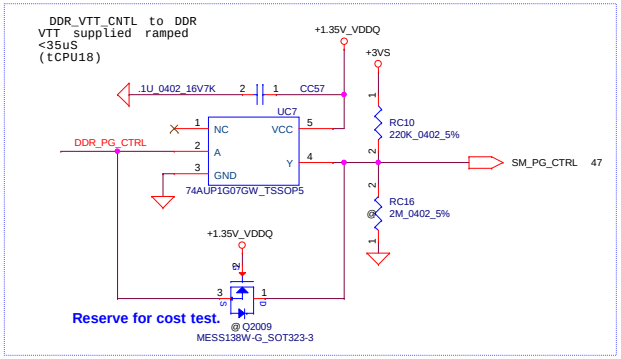
Interleaved Memory





Pre_ES Sample

UC1: CPU_QH7Y_A2_1.6G, QH7Y@, SA00008A400

ES Sample

UC1: CPU_QHMF_C0_2.3G, QHMF@, SA00008M420

UC1: CPU_QHMG_C0_1.6G, QHMG@, SA00008M320

QS Sample

UC1: CPU_i3-6100U_D0_2.3G, QJFC@, SA000092N30

UC1: CPU_i5-6200U_D0_2.3G, QJ8N@, SA000092O30

UC1: CPU_i7-6500U_D0_2.5G, QJ8L@, SA000092P20

MP Sample Add on 7/14

UC1: CPU_i3-6100U_D1_2.3G, SR2EU@, SA000092NB0

UC1: CPU_i5-6200U_D1_2.3G, SR2EY@, SA000092OB0

UC1: CPU_i7-6500U_D1_2.5G, SR2EZ@, SA000092P90

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Custom	A4WAS M/B LA-C611P	1.0

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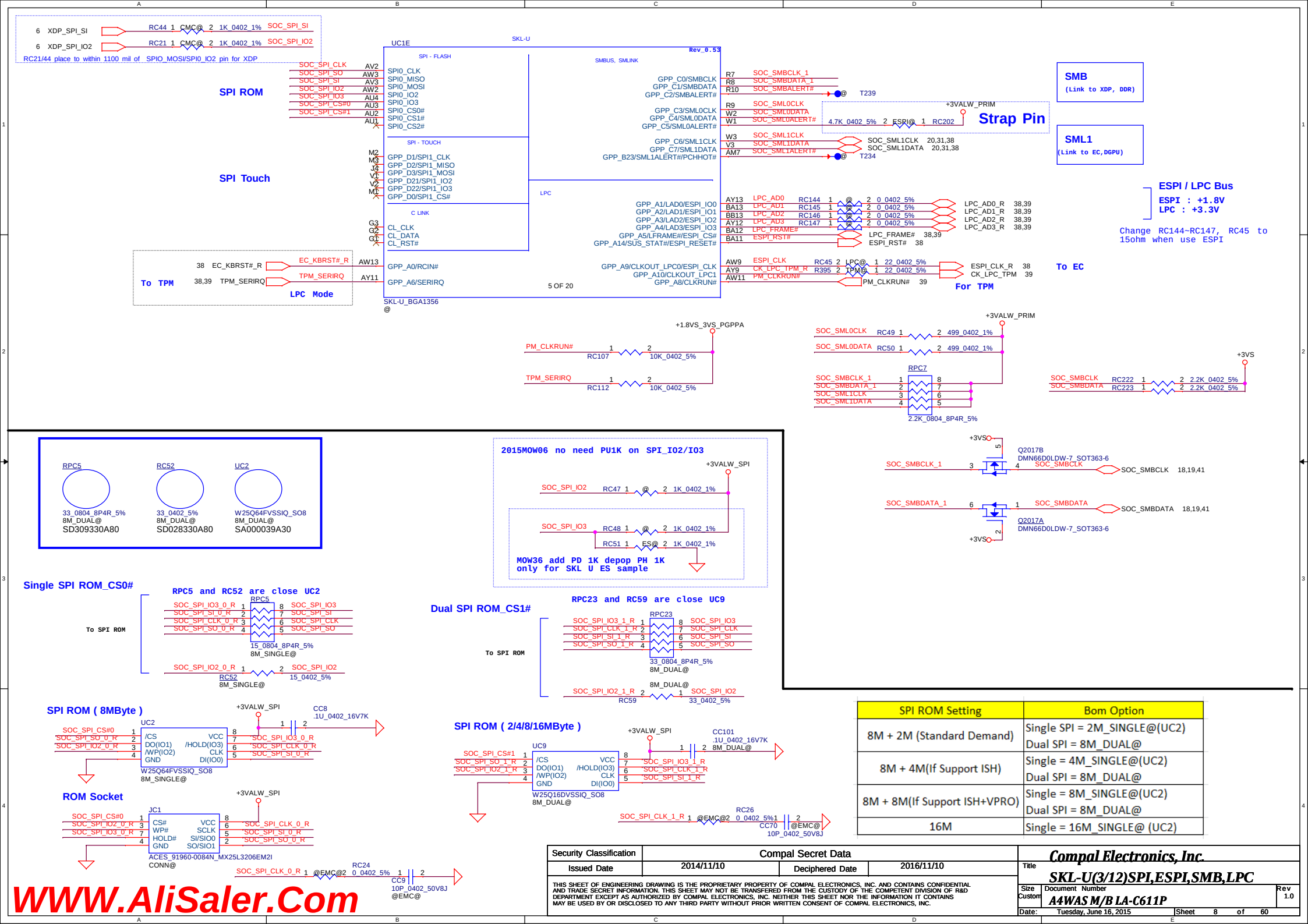


SPI ROM Setting	Bom Option
8M + 2M (Standard Demand)	Single SPI = 2M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 4M(If Support ISH)	Single = 4M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
8M + 8M(If Support ISH+VPRO)	Single = 8M_SINGLE@(UC2) Dual SPI = 8M_DUAL@
16M	Single = 16M_SINGLE@ (UC2)

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,ESPI,SMB,LPC

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 8 of 60

#545659 SKL_PCH_EDS_R0.7 P.84

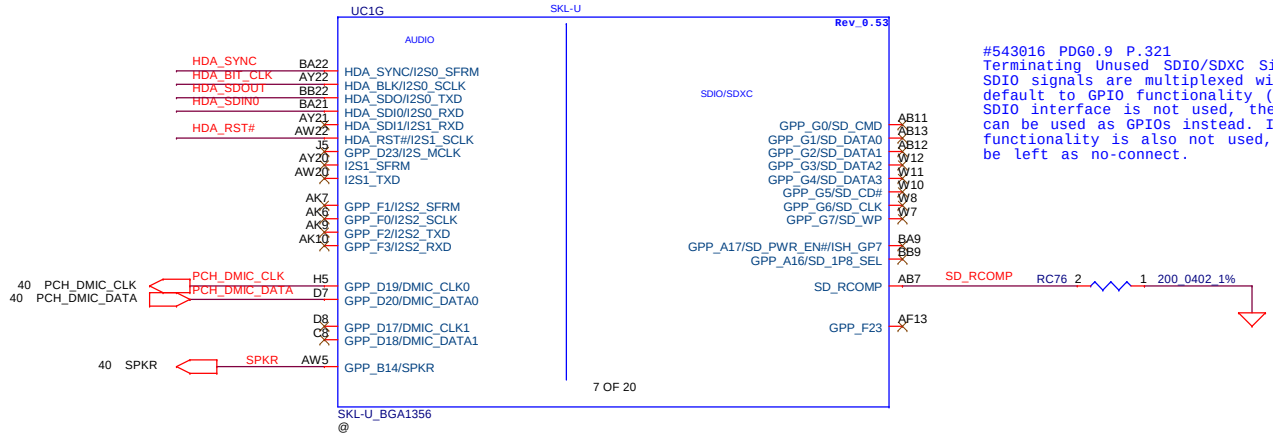
11.7.3 Intel HD Audio link capabilities

- Two SDI signals to support two external codecs.
- Drives variable frequency (6 MHz to 24 MHz) BCLK to support:
  - SDO double pumped up to 48 Mb/s
  - SDI's single pumped up to 24 Mb/s
- Provides cadence for 44.1 kHz-based sample rate output.
- Supports 1.5V, 1.8V and 3.3V modes.

Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
0 = Disable TOP Swap mode.---> AAX05 Use
1 = Enable TOP Swap Mode.



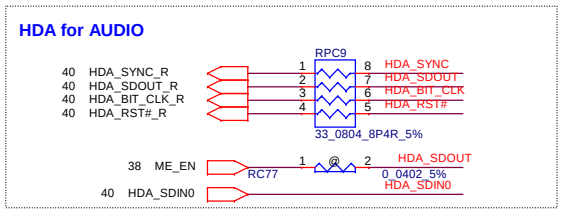
#543016 PDG0.9 P.321
Terminating Unused SDIO/SDXC Signals
SDIO signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDIO interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

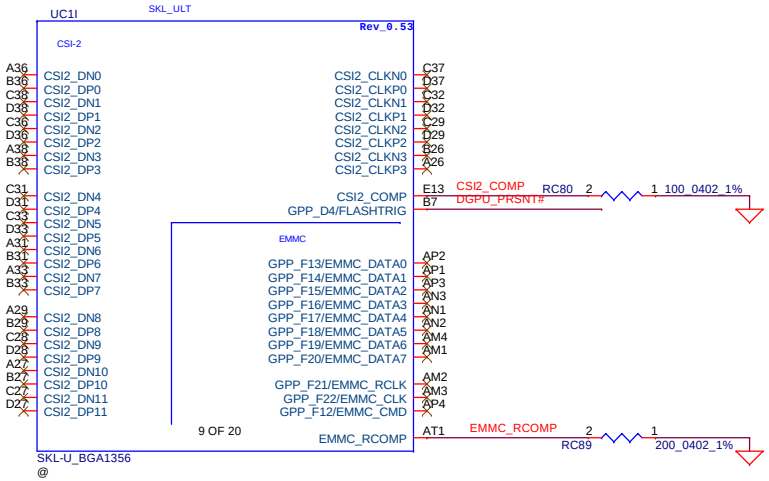
62.3.38 RCOMP Checklist

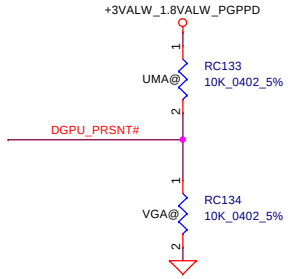
Table 62-48. RCOMP Checklist

Component	Value	✔
NOA_RCOMP	49.9 ohm +/- 1% pull down termination to GND	
PEG_COMP	24.9ohm +/- 1% pull down termination to GND	
SD_RCOMP	200ohms termination to GND.	
EMMC_RCOMP	200ohms termination to GND.	
PCIE_RCOMPP/N	100 ohm +/- 1%. Differential between RCOMPP/RCOMPN	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	

SD_RCOMP	200ohms termination to GND.	
EMMC_RCOMP	200ohms termination to GND.	
PCH_POPIRCOMP	DC resistance <0.2ohm. 49.9 ohm termination resistor to GND.	
PCIE_RCOMPP/N	100 ohm +/- 1%. Differential between RCOMPP/RCOMPN	
CSI2_COMP	100 ohm +/- 1% termination resistor to GND; DC resistance <0.5ohm.	
USB2_COMP	113 Ohm +/- 1% differential termination to GND; DC resistance <0.5ohm.	







	GPIO67 DGPU_PRSNT#
DIS,Optimus	0
UMA	1

Compal Electronics, Inc.
Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2
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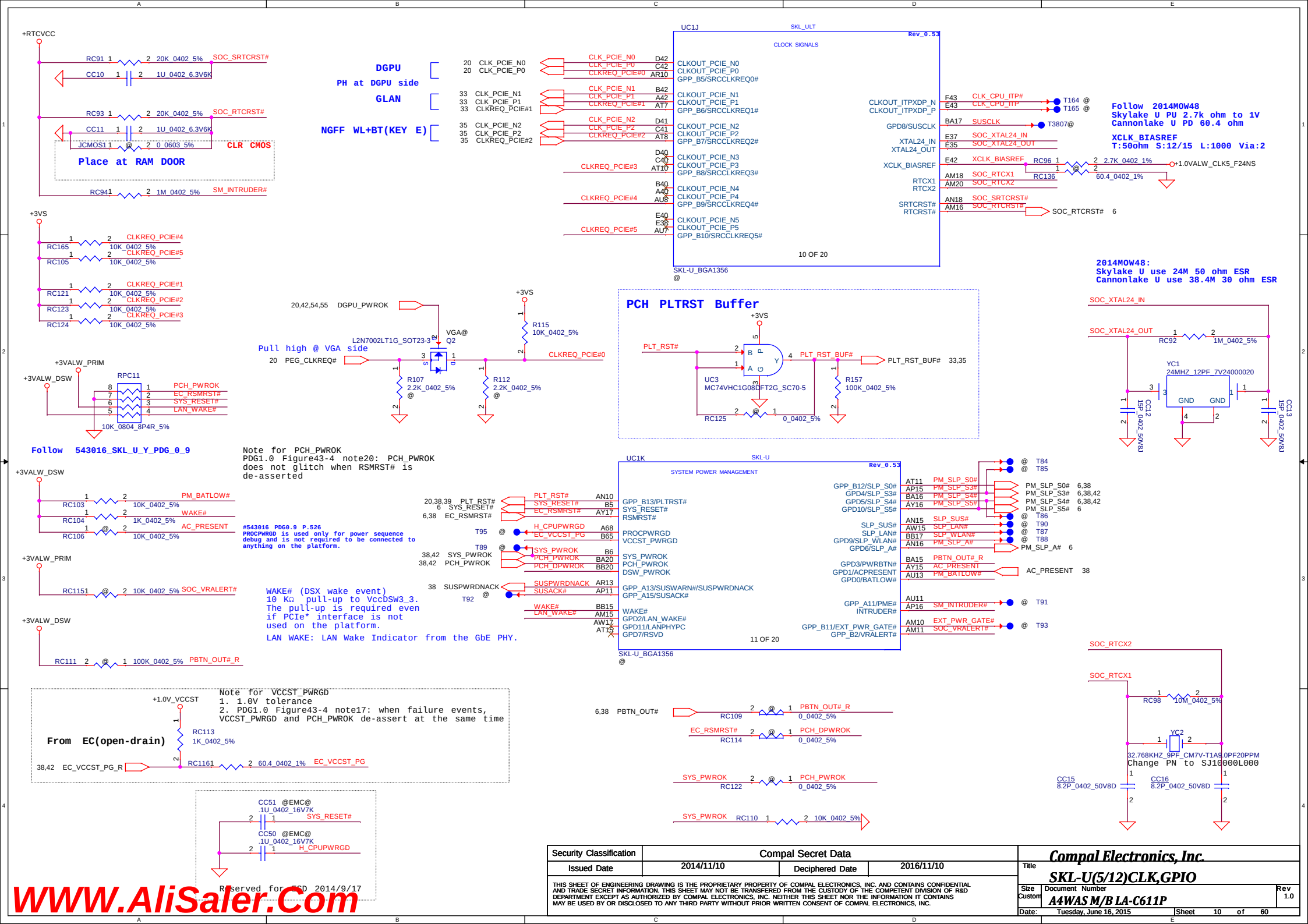

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SKL-U(5/12)CLK,GPIO

Size	Document Number	Rev
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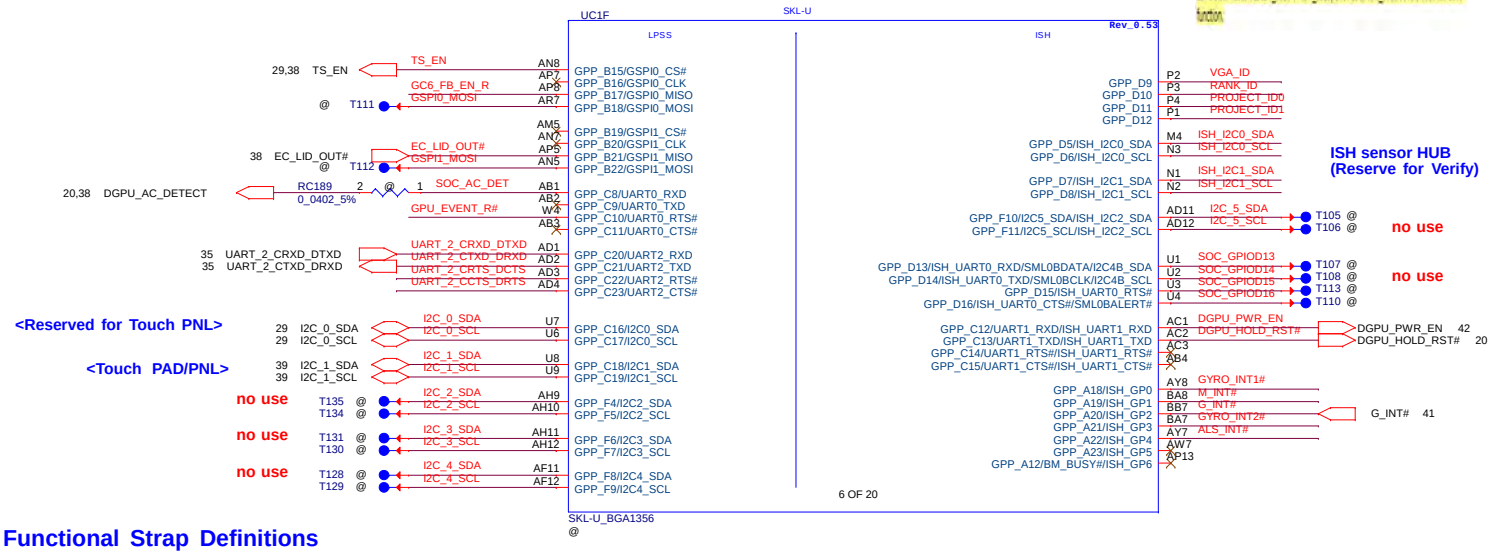
543016 SKY PDG 0.9 P.401

The sensors are connected to ISH through ISH I2C interface and ISH GPIO. Sensors can be connected to ISH_I2C0 or ISH_I2C1, but not to ISH_I2C2 as it is used for other function.



ISH sensor HUB (Reserve for Verify)

no use

no use

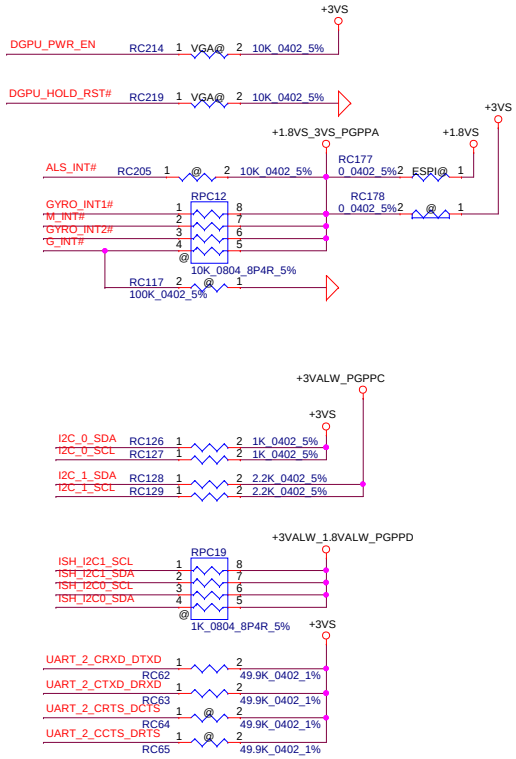
<Reserved for Touch PNL>

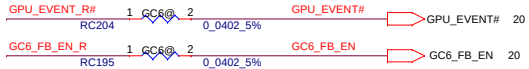
<Touch PAD/PNL>

no use

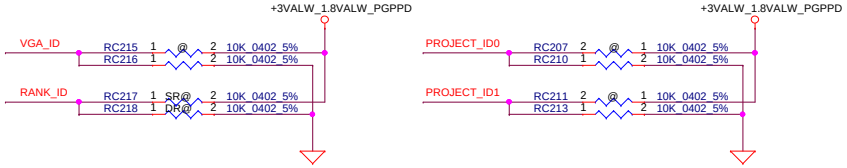
no use

no use





TO DGPU



Functional Strap Definitions

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

TOP Swap Override
*** 0 = Disable TOP Swap mode.---> AAX05 Use**
1 = Enable TOP Swap Mode.

GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

*** 0 = Disable No Reboot mode. --> AAX05 Use**
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
*** 0 = SPI Mode --> AAX05 Use**
1 = LPC Mode

SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
*** 0 = LPC is selected for EC --> For KB9022/9032 Use**
1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

TLS Confidentiality
*** 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).**
1 = Enable Intel ME Crypto (TLS) (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

VGA_ID	GPP_D9
GL	0
GM	1

RANK_ID	GPP_D10
DR	0
SR	1

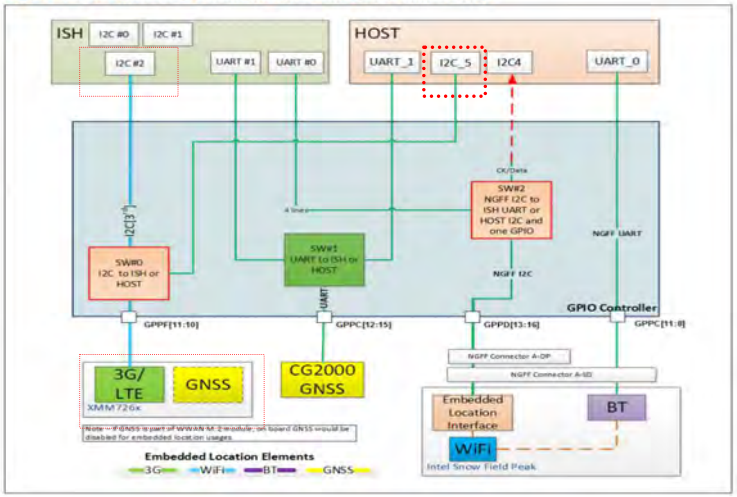
Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
*A4WAS	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

HDA_SDO/I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

DDPB_CTRLDATA/ GPP_E19 (Internal Pull Down):
DDPC_CTRLDATA/ GPP_E21 (Internal Pull Down):
DDPD_CTRLDATA/ GPP_E23 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)
Display Port B/C/D Detected
0 =Port D is not detected.
1 =Port D is detected.

I2C/ISH Port(From PDG 0.9)

Figure 64-1. Embedded Location - Host and ISH Connectivity



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: SKL-U(6/12)GPIO			
Size: Custom	Document Number: A4WAS M/B LA-C611P		Rev: 1.0
Date: Tuesday, June 16, 2015	Sheet 11 of 60		

UC1H

SKL-U

Rev_0.53

PCIE/USB3/SATA

SSIC / USB3

DGPU

20 PCIE_CRX_GTX_N1
20 PCIE_CRX_GTX_P1
20 PCIE_CTX_C_GRX_N1
20 PCIE_CTX_C_GRX_P1
CC17 VGA@1 2 0.22U_0402_16V7K
CC21 VGA@1 2 0.22U_0402_16V7K
PCIE_CRX_GTX_N1 H13
PCIE_CRX_GTX_P1 G13
PCIE_CTX_GRX_N1 B17
PCIE_CTX_GRX_P1 A17
PCIE1_RXN/USB3_5_RXN
PCIE1_RXP/USB3_5_RXP
PCIE1_TXN/USB3_5_TXN
PCIE1_TXP/USB3_5_TXP

20 PCIE_CRX_GTX_N2
20 PCIE_CRX_GTX_P2
20 PCIE_CTX_C_GRX_N2
20 PCIE_CTX_C_GRX_P2
CC18 VGA@1 2 0.22U_0402_16V7K
CC19 VGA@1 2 0.22U_0402_16V7K
PCIE_CRX_GTX_N2 G11
PCIE_CRX_GTX_P2 F11
PCIE_CTX_GRX_N2 D16
PCIE_CTX_GRX_P2 C16
PCIE2_RXN/USB3_6_RXN
PCIE2_RXP/USB3_6_RXP
PCIE2_TXN/USB3_6_TXN
PCIE2_TXP/USB3_6_TXP

20 PCIE_CRX_GTX_N3
20 PCIE_CRX_GTX_P3
20 PCIE_CTX_C_GRX_N3
20 PCIE_CTX_C_GRX_P3
CC20 VGA@1 2 0.22U_0402_16V7K
CC22 VGA@1 2 0.22U_0402_16V7K
PCIE_CRX_GTX_N3 H16
PCIE_CRX_GTX_P3 G16
PCIE_CTX_GRX_N3 D17
PCIE_CTX_GRX_P3 C17
PCIE3_RXN
PCIE3_RXP
PCIE3_TXN
PCIE3_TXP

20 PCIE_CRX_GTX_N4
20 PCIE_CRX_GTX_P4
20 PCIE_CTX_C_GRX_N4
20 PCIE_CTX_C_GRX_P4
CC23 VGA@1 2 0.22U_0402_16V7K
CC24 VGA@1 2 0.22U_0402_16V7K
PCIE_CRX_GTX_N4 G15
PCIE_CRX_GTX_P4 F15
PCIE_CTX_GRX_N4 B19
PCIE_CTX_GRX_P4 A19
PCIE4_RXN
PCIE4_RXP
PCIE4_TXN
PCIE4_TXP

GLAN+CR

33 PCIE_CRX_DTX_N5
33 PCIE_CRX_DTX_P5
33 PCIE_CTX_C_DRX_N5
33 PCIE_CTX_C_DRX_P5
CC25 2 1 .1U_0402_16V7K
CC26 2 1 .1U_0402_16V7K
PCIE_CRX_DTX_N5 F16
PCIE_CRX_DTX_P5 E16
PCIE_CTX_DRX_N5 C19
PCIE_CTX_DRX_P5 D19
PCIE5_RXN
PCIE5_RXP
PCIE5_TXN
PCIE5_TXP

NGFF WLAN+BT(Key E)

35 PCIE_CRX_DTX_N6
35 PCIE_CRX_DTX_P6
35 PCIE_CTX_C_DRX_N6
35 PCIE_CTX_C_DRX_P6
C3803 1 2 .1U_0402_16V7K
C3804 1 2 .1U_0402_16V7K
PCIE_CRX_DTX_N6 G18
PCIE_CRX_DTX_P6 F18
PCIE_CTX_DRX_N6 D20
PCIE_CTX_DRX_P6 C20
PCIE6_RXN
PCIE6_RXP
PCIE6_TXN
PCIE6_TXP

HDD

36 SATA_CRX_DTX_N0
36 SATA_CRX_DTX_P0
36 SATA_CTX_DRX_N0
36 SATA_CTX_DRX_P0
F20
E20
B21
A21
PCIE7_RXN/SATA0_RXN
PCIE7_RXP/SATA0_RXP
PCIE7_TXN/SATA0_TXN
PCIE7_TXP/SATA0_TXP

ODD

36 SATA_CRX_DTX_N1
36 SATA_CRX_DTX_P1
36 SATA_CTX_DRX_N1
36 SATA_CTX_DRX_P1
G21
F21
D21
C21
PCIE8_RXN/SATA1A_RXN
PCIE8_RXP/SATA1A_RXP
PCIE8_TXN/SATA1A_TXN
PCIE8_TXP/SATA1A_TXP

When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

+3VALW_PRIM
10K_0402_5% 2 @ 1 RC135 PIRQA#

#543016 P.239 PCIE_RCOMPN/PCIE_RCOMPP
BO=4 W=12 S=12 R=100ohm
RC1201 2 100_0402_1%
PCIE_RCOMPN F5
PCIE_RCOMPP E5
PCIE_RCOMPN
PCIE_RCOMPP

6 XDP_PRDY#
6 XDP_PREQ#
XDP_PRDY# D56
XDP_PREQ# D61
PIRQA# BB11
PROC_PRDY#
PROC_PREQ#
GPP_A7/PIRQA#

E22
E23
B23
A23
PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP

F25
E25
D23
C23
PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP

E28
E27
D24
C24
E30
F30
A25
B25
PCIE11_RXN/SATA1B_RXN
PCIE11_RXP/SATA1B_RXP
PCIE11_TXN/SATA1B_TXN
PCIE11_TXP/SATA1B_TXP
PCIE12_RXN/SATA2_RXN
PCIE12_RXP/SATA2_RXP
PCIE12_TXN/SATA2_TXN
PCIE12_TXP/SATA2_TXP

USB2

USB3_1_RXN H8
USB3_1_RXP G8
USB3_1_TXN C13
USB3_1_TXP D13
USB3_CRX_DTX_N1 37
USB3_CRX_DTX_P1 37
USB3_CTX_DRX_N1 37
USB3_CTX_DRX_P1 37
USB3 MB

USB3_2_RXN/SSIC_1_RXN J6
USB3_2_RXP/SSIC_1_RXP H6
USB3_2_TXN/SSIC_1_TXN B13
USB3_2_TXP/SSIC_1_TXP A13
USB3_CRX_DTX_N2 37
USB3_CRX_DTX_P2 37
USB3_CTX_DRX_N2 37
USB3_CTX_DRX_P2 37
USB3 MB

USB3_3_RXN/SSIC_2_RXN J10
USB3_3_RXP/SSIC_2_RXP H10
USB3_3_TXN/SSIC_2_TXN B15
USB3_3_TXP/SSIC_2_TXP A15

USB3_4_RXN E10
USB3_4_RXP F10
USB3_4_TXN C15
USB3_4_TXP D15

USB2N_1 AB9 USB20_N1
USB2P_1 AB10 USB20_P1
USB20_N1 37
USB20_P1 37
USB3 MB

USB2N_2 AD6 USB20_N2
USB2P_2 AD7 USB20_P2
USB20_N2 37
USB20_P2 37
USB3 MB

USB2N_3 AH3 USB20_N3
USB2P_3 AJ3 USB20_P3
USB20_N3 37
USB20_P3 37
USB2/B

USB2N_4 AD9
USB2P_4 AD10

USB2N_5 AJ1 USB20_N5
USB2P_5 AJ2 USB20_P5
USB20_N5 35
USB20_P5 35
BT

USB2N_6 AF6 USB20_N6
USB2P_6 AF7 USB20_P6
USB20_N6 29
USB20_P6 29
TS

USB2N_7 AH1 USB20_N7
USB2P_7 AH2 USB20_P7
USB20_N7 29
USB20_P7 29
Camera

USB2N_8 AF8
USB2P_8 AF9

USB2N_9 AG1
USB2P_9 AG2

USB2N_10 AH7
USB2P_10 AH8

AG3,AG4 PD1K for DCI warm boot fail issue (follow PCH EDS1.2)
2015MOW10, USB2_ID Connected to GND Directly

USB2_COMP AB6 USB2_COMP RC119 1 2 113_0402_1%
USB2_ID AG3 USB2_ID RC130 1 2 0_0402_5%
USB2_VBUSSENSE AG4 USB2_VBUSSENSE RC131 1 2 0_0402_5%

GPP_E9/USB2_OC0# A9 USB_OC0#
GPP_E10/USB2_OC1# C9 USB_OC1#
GPP_E11/USB2_OC2# D9
GPP_E12/USB2_OC3# B9
USB_OC0# 37
USB_OC1# 37

GPP_E4/DEVSLP0 J1
GPP_E5/DEVSLP1 J2
GPP_E6/DEVSLP2 J3

GPP_E0/SATAXPCIE0/SATAGP0 H2
GPP_E1/SATAXPCIE1/SATAGP1 H3
GPP_E2/SATAXPCIE2/SATAGP2 G4

GPP_E8/SATALED# H1

8 OF 20

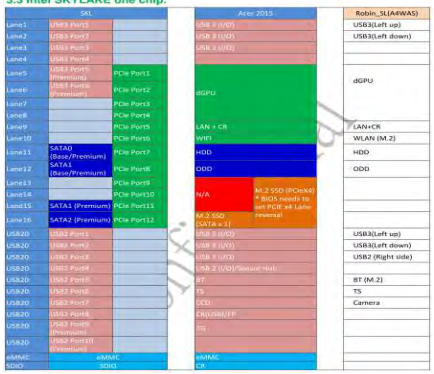
SKL-U_BGA1356
@

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA

High Speed I/O (HSIO) Lane Multiplexing in SKL U

Acer HSIO def i ne
3.3 Intel SKYLAKE one chip.



GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	USB2 Port 2
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

+3VALW_PRIM
USB_OC0# RC1321 2 10K_0402_5%
USB_OC1# RC2001 2 10K_0402_5%

DEVSLP[2:0] Implementation
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.
•When high, DEVSLP requests the SATA device to enter into the DEVSLP power state.
•When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals
•The processor provides three SATA general purpose input signals,SATAGP[2:0] for SKL U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.
•When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
•If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

Compal Electronics, Inc.
Title: SKL-U(7/12)PCIE,USB,SATA
Size: Custom Document Number: A4WAS M/B LA-C611P Rev: 1.0
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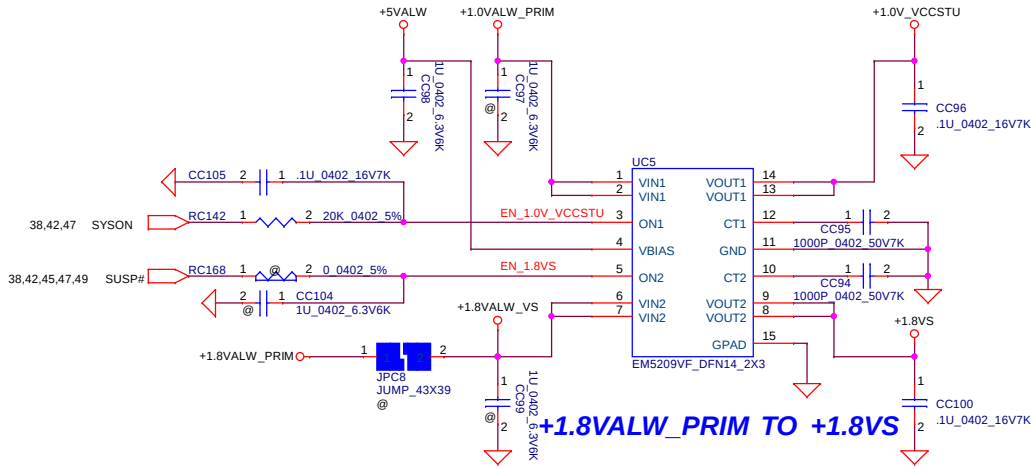
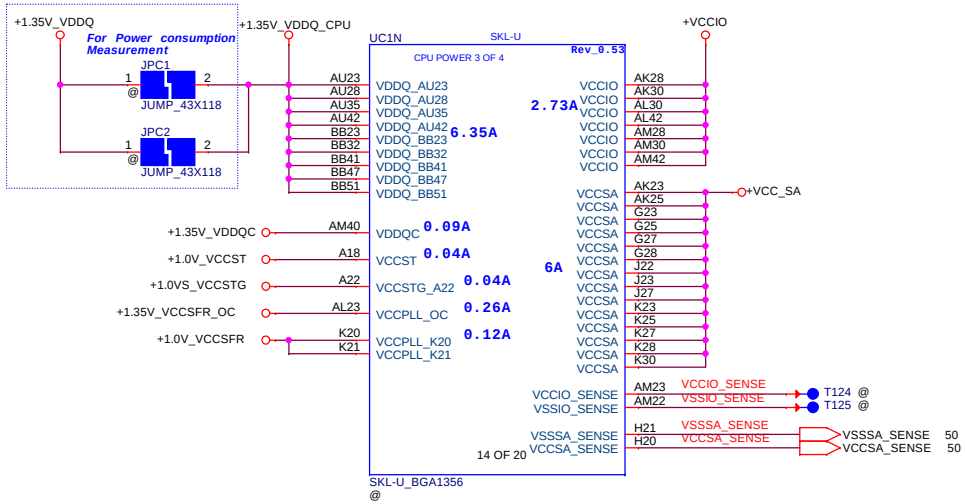
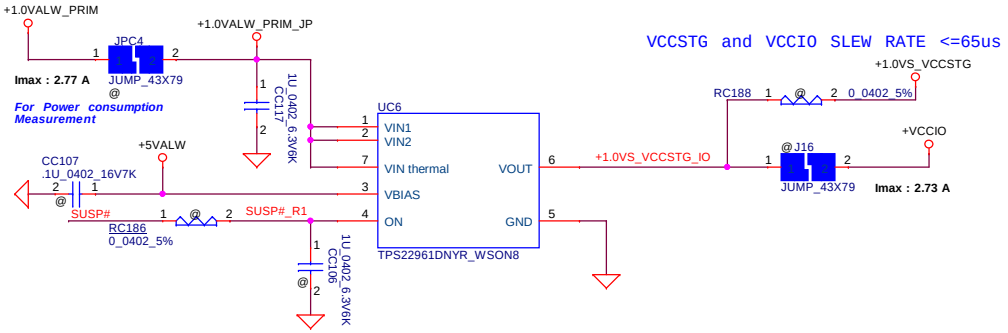
+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

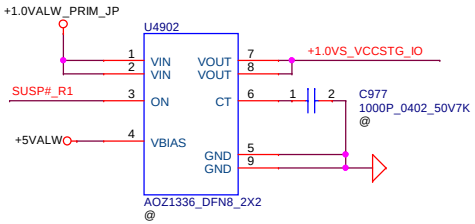


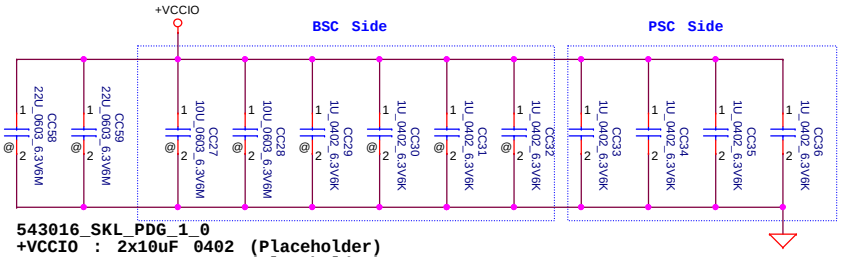
+1.8VALW_PRIM TO +1.8VS



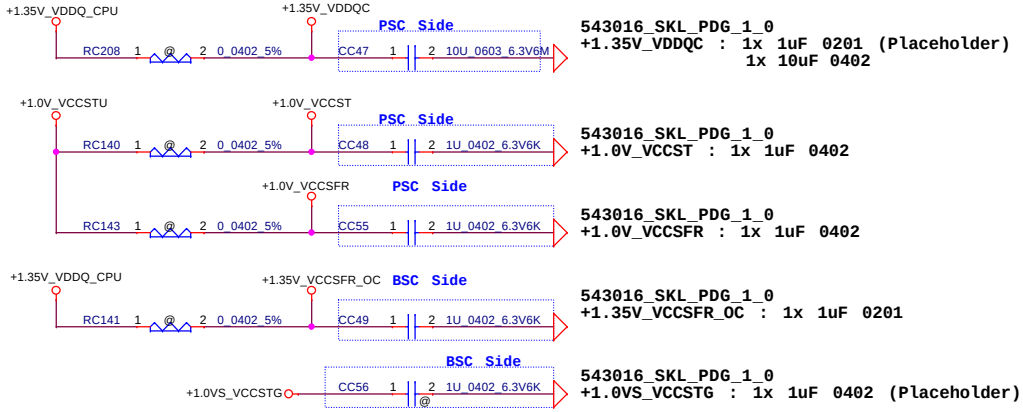
+1.0VALW_PRIM TO +1.0VS_VCCSTG

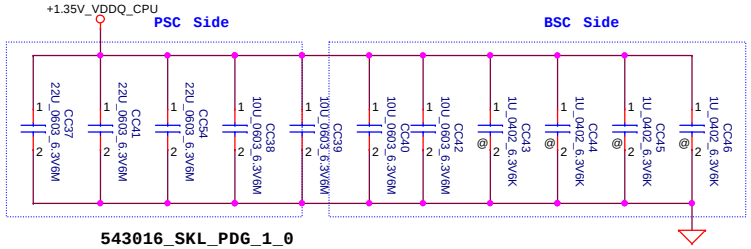






543016_SKL_PDG_1_0
+VCCIO : 2x10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 1uF 0402





543016_SKL_PDG_1_0
+1.35V_VDDQ_CPU : 2x 10uF 0402 (Placeholder)
4x 1uF 0201 (Placeholder)
4x 10uF 0402
3x 22uF 0603

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SKL-U(8/12)Power

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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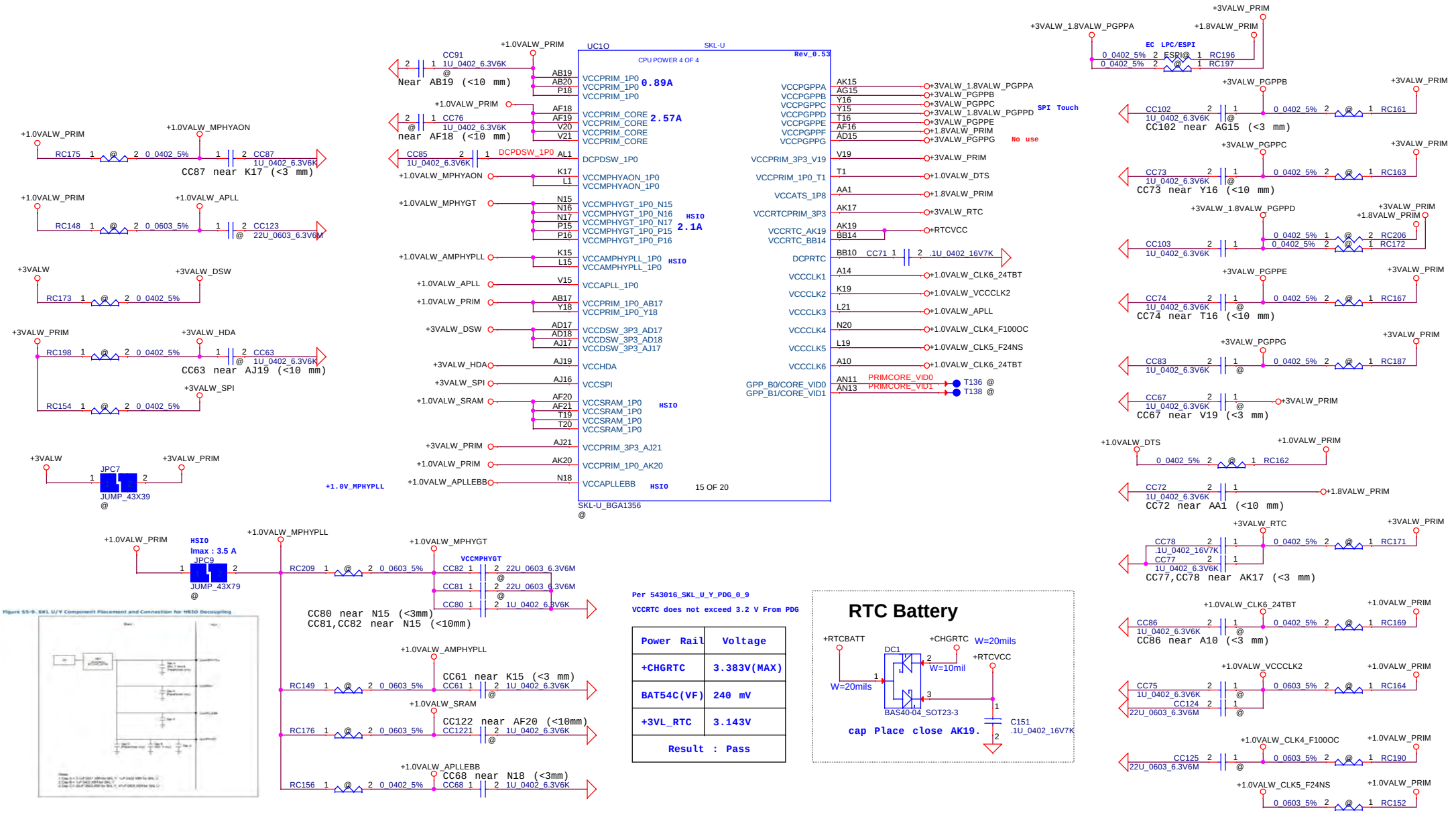

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: SKL-U(9/12)Power			
Size: Custom	Document Number: A4WAS M/B LA-C611P		Rev: 1.0
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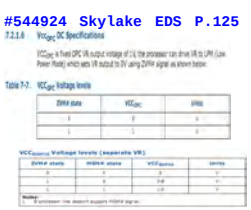
VCC 27A (U 15W Dual Core GT2)

#544924 Skylake EDS P.125



#544924 Skylake EDS P.125
VCCOPC 1V 2.8A
VCC_OPC_1P8 1.8V 50mA
VCCEOPIO 0V,0.8V,1V 2.9A

For CPU2+3e SKU

+VCC_CORE

UC1L SKL-U Rev_0.53
CPU POWER 1 OF 4

A30	VCC_A30	VCC_G32	G32
A34	VCC_A34	VCC_G33	G33
A39	VCC_A39	VCC_G35	G35
A44	VCC_A44	VCC_G37	G37
AK33	VCC_AK33	VCC_G38	G38
AK35	VCC_AK35	VCC_G40	G40
AK37	VCC_AK37	VCC_G42	G42
AK38	VCC_AK38	VCC_J30	J30
AK40	VCC_AK40	VCC_J33	J33
AL33	VCC_AL33	VCC_J37	J37
AL37	VCC_AL37	VCC_J40	J40
AL40	VCC_AL40	VCC_K33	K33
AM32	VCC_AM32	VCC_K35	K35
AM33	VCC_AM33	VCC_K37	K37
AM35	VCC_AM35	VCC_K38	K38
AM37	VCC_AM37	VCC_K40	K40
AM38	VCC_AM38	VCC_K42	K42
G30	VCC_G30	VCC_K43	K43
K32	RSVD_K32	VCC_SENSE	E32
AK32	RSVD_AK32	VSS_SENSE	E33
AB62	VCCOPC_AB62	VIDALERT#	B63
P62	VCCOPC_P62	VIDSCK	A63
V62	VCCOPC_V62	VIDSOUT	D64
H63	VCC_OPC_1P8_H63	VCCSTG_G20	G20
G61	VCC_OPC_1P8_G61		
AC63	VCCOPC_SENSE		
AE63	VSSOPC_SENSE		
AE62	VCCEOPIO		
AG62	VCCEOPIO		
AL63	VCCEOPIO_SENSE		
AJ62	VSSEOPIO_SENSE		

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SKL-U_BGA1356
@

For CPU2+3e SKU

T132 @ VCCOPC_SENSE
T133 @ VSSOPC_SENSE

T137 @ VCCEOPIO_SENSE
T139 @ VSSEOPIO_SENSE

#544924 Skylake EDS P.120
VCC U(15W)-dual core GT2 27A(Typ)-33A(MAX)
0.55-1.15V

Trace Length < 25 mils

VCCSENSE 50
VSSSENSE 50

SOC_SVID_ALERT#
SOC_SVID_CLK
SOC_SVID_DAT
SOC_SVID_CLK 50

+1.0VS_VCCSTG
+1.0VS(SUSP#)

Table 2-1. Package Sensing Recommendations

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
Vcc_SENSE / Vss_SENSE	100Ω	50Ω	<25 mils
VccGT_SENSE / VssGT_SENSE			
VccGTx_SENSE / VssGTx_SENSE			
VccSA_SENSE / VssSA_SENSE		NA	
VccIO_SENSE / VssIO_SENSE [1]			

Note: [1] Does not apply when rails are merged.

To minimize any stray noise pickup to the Vcc_SENSE/Vss_SENSE lines
- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain a 25-mil separation distance away from any other dynamic signals

VCCGT / VCCGTX(2+3e only) 40A(need confirm)

#544924 Skylake EDS P.121
VCCGT U(15W)-dual core GT2 40A(MAX)
0.55-1.15V

+VCC_GT

UC1M SKL-U Rev_0.53
CPU POWER 2 OF 4

A48	VCCGT	VCCGT	N70
A53	VCCGT	VCCGT	N71
A58	VCCGT	VCCGT	R63
A62	VCCGT	VCCGT	R64
A66	VCCGT	VCCGT	R65
AA63	VCCGT	VCCGT	R66
AA64	VCCGT	VCCGT	R67
AA66	VCCGT	VCCGT	R68
AA67	VCCGT	VCCGT	R69
AA69	VCCGT	VCCGT	R70
AA70	VCCGT	VCCGT	R71
AA71	VCCGT	VCCGT	T62
AC64	VCCGT	VCCGT	U65
AC65	VCCGT	VCCGT	U68
AC66	VCCGT	VCCGT	U71
AC67	VCCGT	VCCGT	W63
AC68	VCCGT	VCCGT	W64
AC69	VCCGT	VCCGT	W65
AC70	VCCGT	VCCGT	W66
AC71	VCCGT	VCCGT	W67
J43	VCCGT	VCCGT	W68
J45	VCCGT	VCCGT	W69
J46	VCCGT	VCCGT	W70
J48	VCCGT	VCCGT	W71
J50	VCCGT	VCCGT	Y62
J52	VCCGT		
J53	VCCGT	VCCGTX_AK42	AK42
J55	VCCGT	VCCGTX_AK43	AK43
J56	VCCGT	VCCGTX_AK45	AK45
J58	VCCGT	VCCGTX_AK46	AK46
J60	VCCGT	VCCGTX_AK48	AK48
K48	VCCGT	VCCGTX_AK50	AK50
K50	VCCGT	VCCGTX_AK52	AK52
K52	VCCGT	VCCGTX_AK53	AK53
K53	VCCGT	VCCGTX_AK55	AK55
K55	VCCGT	VCCGTX_AK56	AK56
K56	VCCGT	VCCGTX_AK58	AK58
K58	VCCGT	VCCGTX_AK60	AK60
K60	VCCGT	VCCGTX_AK70	AK70
L62	VCCGT	VCCGTX_AL43	AL43
L63	VCCGT	VCCGTX_AL46	AL46
L64	VCCGT	VCCGTX_AL50	AL50
L65	VCCGT	VCCGTX_AL53	AL53
L66	VCCGT	VCCGTX_AL56	AL56
L67	VCCGT	VCCGTX_AL60	AL60
L68	VCCGT	VCCGTX_AM48	AM48
L69	VCCGT	VCCGTX_AM50	AM50
L70	VCCGT	VCCGTX_AM52	AM52
L71	VCCGT	VCCGTX_AM53	AM53
M62	VCCGT	VCCGTX_AM56	AM56
N63	VCCGT	VCCGTX_AM58	AM58
N64	VCCGT	VCCGTX_AU58	AU58
N66	VCCGT	VCCGTX_AU63	AU63
N67	VCCGT	VCCGTX_BB57	BB57
N69	VCCGT	VCCGTX_BB66	BB66
J70	VCCGT_SENSE	VCCGTX_SENSE	AK62
J69	VSSGT_SENSE	VSSGTX_SENSE	AL61

13 OF 20

SKL-U_BGA1356
@

For CPU2+3e SKU

50 VCCGT_SENSE
50 VSSGT_SENSE

VCCGT_SENSE
VSSGT_SENSE

VCCGTX_SENSE
VSSGTX_SENSE

T155 @
T219 @

Trace Length < 25 mils

SVID ALERT

+1.0V_VCCST

Place the PU resistors close to CPU

RC179
56_0402_5%

SOC_SVID_ALERT# 1 RC180 2 220_0402_5% SOC_SVID_ALERT#_R 50 (To VR)

SVID DATA

+1.0V_VCCST

Place the PU resistors close to CPU

RC181
100_0402_1%

SOC_SVID_DAT SOC_SVID_DAT 50 (To VR)

543016 PDG0.9 P.189 Need check

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_ST [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDSCK							100	100	0	10	
VIDALERT#							56	Empty	220	0	

Processor Power Rails

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
V_{CCGT}	Processor Graphics Power Rails	SVID
V_{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V_{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V_{CCIO}	IO Power Rail	Fixed
V_{CCST}	Sustain Power Rail	Fixed
V_{CCPLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V_{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V_{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CCEOPIO}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SKL-U(10/12)Power,SVID

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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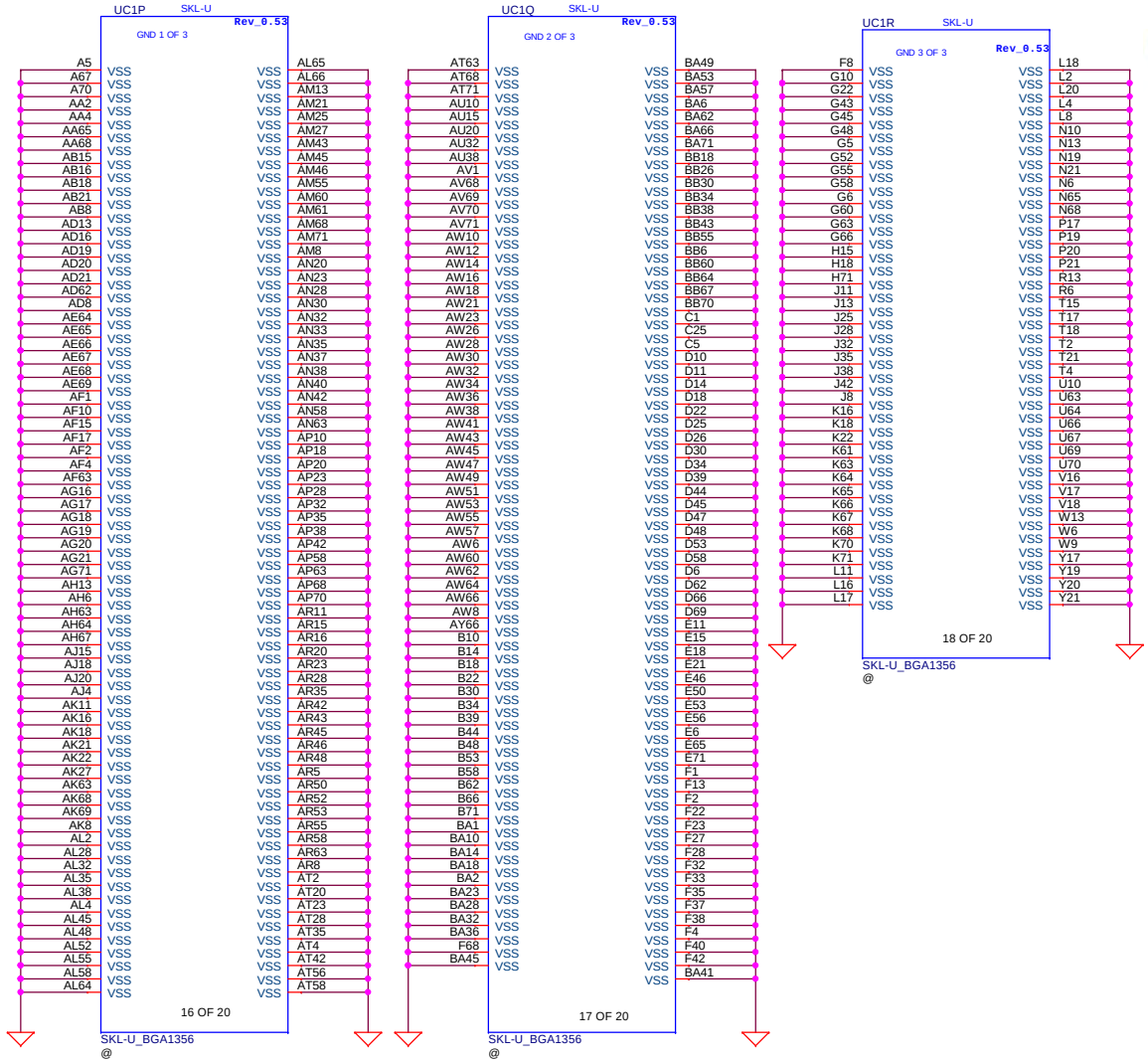
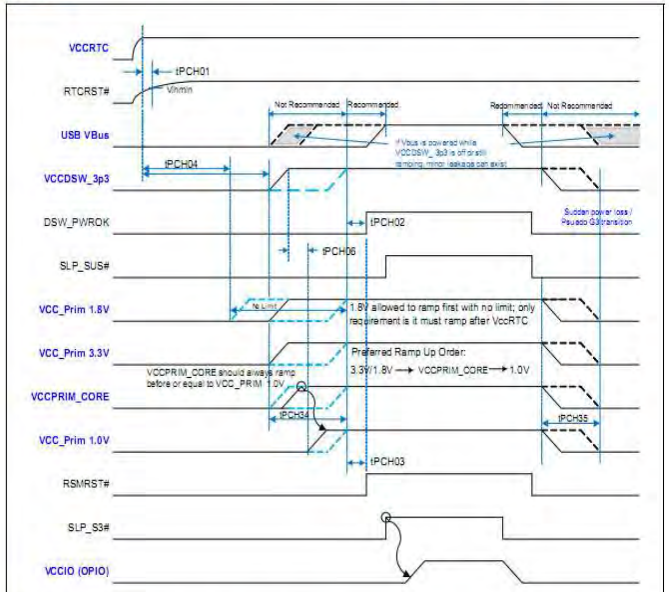


Figure 46-18.SKL-U/Y Rail-to-Rail Sequencing Requirement for Non-Deep Sx Configured System



Notes:

1. VCC_PRIM 1.8 V includes VCCPGPPF, VCCATS and may include VCCPGPPA, VCCPGPPB, VCCPGPPC, VCCPGPPD, VCCPGPPE, VCCPGPPG, VCCHDA and/or VCCSPI if the rails are 1.8 V.
2. VCC_PRIM 3.3 V includes VCCPRIM_3p3 and VCCRTCPRIM_3p3.
3. VCCPRIM_CORE is only applicable on SKL U/Y. For SKL H, the rail is merged with VCCPRIM_1p0.
4. VCC_PRIM 1.0 V may include the following rails: VCCPRIM_1p0, VCCSRAM_1p0, VCCMPHYAON_1p0, VCCMPHYGT_1p0, VCCMPHYPLL_1p0, VCCAPLL_1p0, VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK5, VCCCLK6.

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.		
Title	SKL-U(11/12)GND	
Size: Custom	Document Number: A4WAS M/B LA-C611P	Rev: 1.0
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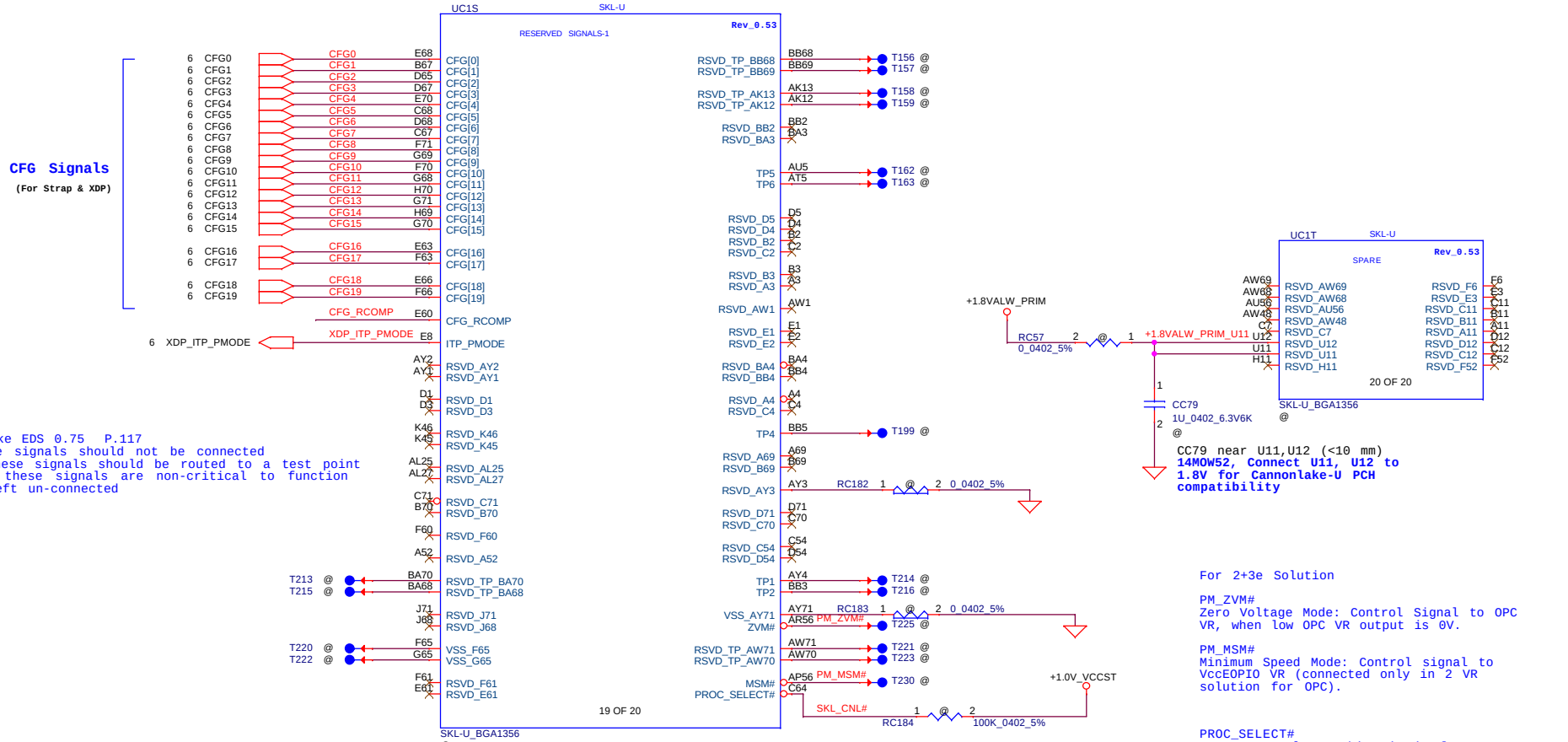

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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Reverse Type

2-3A to 1 DIMMs/channel

Place near to SO-DIMM connector.

10mils

CAD NOTE
PLACE THE CAP NEAR TO
DIMM RESET PIN

2015MOW02, Can't install Cap on DRAMRST

From CPU to CHB

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

Follow MA51

SGA00009S00
330U 2V H1.9
9mohm POLY

Layout Note:
Place near JDIMM1.203,204

Layout Note:
Place near JDIMM1.199

BELLW_80001-1021
SP07000P700
CONN@

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: DDR3L_DIMMA

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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Standard Type

2-3A to 1 DIMMs/channel

7 DDR_B_DQS#[0..7]
7 DDR_B_D[0..63]
7 DDR_B_DQS[0..7]
7 DDR_B_MA[0..15]
7 DDR_B_BS0 — DDR_B_BS0
7 DDR_B_BS1 — DDR_B_BS1
7 DDR_B_BS2 — DDR_B_BS2
7 DDR_B_WE# — DDR_B_WE#
7 DDR_B_CAS# — DDR_B_CAS#
7 DDR_B_RAS# — DDR_B_RAS#
7 DDR_B_CLK0 — DDR_B_CLK0
7 DDR_B_CLK#0 — DDR_B_CLK#0
7 DDR_B_CLK1 — DDR_B_CLK1
7 DDR_B_CLK#1 — DDR_B_CLK#1
7 DDR_B_CKE0 — DDR_B_CKE0
7 DDR_B_CKE1 — DDR_B_CKE1
7 DDR_B_CS#0 — DDR_B_CS#0
7 DDR_B_CS#1 — DDR_B_CS#1
8,18,41 SOC_SMBDATA — SOC_SMBDATA
8,18,41 SOC_SMBCLK — SOC_SMBCLK
7 DDR_B_ODT0 — DDR_B_ODT0
7 DDR_B_ODT1 — DDR_B_ODT1

Layout Note: Place near JDIMM2

+1.35V_VDDQ
CD32 1U_0402_6.3V6K
CD33 1U_0402_6.3V6K @
CD34 1U_0402_6.3V6K
CD35 1U_0402_6.3V6K @
CD36 1U_0402_6.3V6K
CD37 1U_0402_6.3V6K @

+1.35V_VDDQ
CD38 10U_0603_6.3V6M
CD39 10U_0603_6.3V6M
CD40 10U_0603_6.3V6M @
CD41 10U_0603_6.3V6M
CD42 10U_0603_6.3V6M
CD43 10U_0603_6.3V6M @
CD44 10U_0603_6.3V6M
CD45 10U_0603_6.3V6M

Layout Note: Place near JDIMM2.203,204

+0.675VS_VTT
CD52 1U_0402_6.3V6K
CD53 1U_0402_6.3V6K

Layout Note: Place near JDIMM2.199

+3VS
CD55 2.2U_0402_6.3V6M @

+1.35V_VDDQ
+0.675V_DDRB_VREFDQ
10mils
RD13 1.8K_0402_1%
RD14 2_0402_1%
RD15 1.8K_0402_1%
RD16 24.9_0402_1%
CD31 0.022U_0402_16V7K
CD28 .1U_0402_16V7K

Place near to SO-DIMM connector.

JDIMM2

	VREF_DQ	1	2	VSS1	
DDR_B_D11	VSS2	3	4	DQ4	DDR_B_D12
DDR_B_D13	DQ0	5	6	DQ5	DDR_B_D8
	DQ1	7	8	VSS3	
	VSS4	9	10	DQS#0	DDR_B_DQS#1
	DM0	11	12	DQS0	DDR_B_DQS1
DDR_B_D15	VSS5	13	14	VSS6	
DDR_B_D14	DQ2	15	16	DQ6	DDR_B_D9
	DQ3	17	18	DQ7	DDR_B_D10
DDR_B_D5	VSS7	19	20	VSS8	
DDR_B_D1	DQ8	21	22	DQ12	DDR_B_D4
	DQ9	23	24	DQ13	DDR_B_D0
DDR_B_DQS#0	VSS9	25	26	VSS10	
DDR_B_DQS0	DQS#1	27	28	DM1	
	DQS1	29	30	RESET#	DDR_DRAMRST#
DDR_B_D3	VSS11	31	32	VSS12	
DDR_B_D2	DQ10	33	34	DQ14	DDR_B_D6
	DQ11	35	36	DQ15	DDR_B_D7
DDR_B_D16	VSS13	37	38	VSS14	
DDR_B_D17	DQ16	39	40	DQ20	DDR_B_D21
	DQ17	41	42	DQ21	DDR_B_D20
DDR_B_DQS#2	VSS15	43	44	VSS16	
DDR_B_DQS2	DQS#2	45	46	DM2	
	DQS2	47	48	VSS17	
DDR_B_D18	VSS18	49	50	DQ22	DDR_B_D19
DDR_B_D22	DQ18	51	52	DQ23	DDR_B_D23
	DQ19	53	54	VSS19	
	VSS20	55	56	DQ28	DDR_B_D29
DDR_B_D24	DQ24	57	58	DQ29	DDR_B_D28
DDR_B_D25	DQ25	59	60	VSS21	
	VSS22	61	62	DQS#3	DDR_B_DQS#3
	DM3	63	64	DQS3	DDR_B_DQS3
DDR_B_D27	VSS23	65	66	VSS24	
DDR_B_D26	DQ26	67	68	DQ30	DDR_B_D30
	DQ27	69	70	DQ31	DDR_B_D31
	VSS25	71	72	VSS26	
+1.35V_VDDQ				+1.35V_VDDQ	
DDR_B_CKE0	CKE0	73	74	CKE1	DDR_B_CKE1
	VDD1	75	76	VDD2	
DDR_B_BS2	NC1	77	78	A15	DDR_B_MA15
	BA2	79	80	A14	DDR_B_MA14
DDR_B_MA12	VDD3	81	82	VDD4	
DDR_B_MA9	A12/BC#	83	84	A11	DDR_B_MA11
	A9	85	86	A7	DDR_B_MA7
DDR_B_MA8	VDD5	87	88	VDD6	
DDR_B_MA5	A8	89	90	A6	DDR_B_MA6
	A5	91	92	A4	DDR_B_MA4
DDR_B_MA3	VDD7	93	94	VDD8	
DDR_B_MA1	A3	95	96	A2	DDR_B_MA2
	A1	97	98	A0	DDR_B_MA0
DDR_B_CLK0	VDD9	99	100	VDD10	
DDR_B_CLK#0	CK0	101	102	CK1	DDR_B_CLK1
	CK0#	103	104	CK1#	DDR_B_CLK#1
DDR_B_MA10	VDD11	105	106	VDD12	
DDR_B_BS0	A10/AP	107	108	BA1	DDR_B_BS1
	BA0	109	110	RAS#	DDR_B_RAS#
DDR_B_WE#	VDD13	111	112	VDD14	
DDR_B_CAS#	WE#	113	114	S0#	DDR_B_CS#0
	CAS#	115	116	ODT0	DDR_B_ODT0
DDR_B_MA13	VDD15	117	118	VDD16	
DDR_B_CS#1	A13	119	120	ODT1	DDR_B_ODT1
	S1#	121	122	NC2	
	VDD17	123	124	VDD18	
	NCTEST	125	126	VREF_CA	
DDR_B_D36	VSS27	127	128	VSS28	
DDR_B_D37	DQ32	129	130	DQ36	DDR_B_D32
	DQ33	131	132	DQ37	DDR_B_D33
DDR_B_DQS#4	VSS29	133	134	VSS30	
DDR_B_DQS4	DQS#4	135	136	DM4	
	DQS4	137	138	VSS31	
DDR_B_D35	VSS32	139	140	DQ38	DDR_B_D39
DDR_B_D34	DQ34	141	142	DQ39	DDR_B_D38
	DQ35	143	144	VSS33	
	VSS34	145	146	DQ44	DDR_B_D41
DDR_B_D45	DQ40	147	148	DQ45	DDR_B_D40
DDR_B_D44	DQ41	149	150	VSS35	
	VSS36	151	152	DQS#5	DDR_B_DQS#5
	DM5	153	154	DQS5	DDR_B_DQS5
	VSS37	155	156	VSS38	
DDR_B_D43	DQ42	157	158	DQ46	DDR_B_D47
DDR_B_D42	DQ43	159	160	DQ47	DDR_B_D46
	VSS39	161	162	VSS40	
DDR_B_D49	DQ48	163	164	DQ52	DDR_B_D52
DDR_B_D48	DQ49	165	166	DQ53	DDR_B_D53
	VSS41	167	168	VSS42	
DDR_B_DQS#6	DQS#6	169	170	DM6	
DDR_B_DQS6	DQS6	171	172	VSS43	
	VSS44	173	174	DQ54	DDR_B_D54
DDR_B_D50	DQ50	175	176	DQ55	DDR_B_D51
DDR_B_D55	DQ51	177	178	VSS45	
	VSS46	179	180	DQ60	DDR_B_D61
DDR_B_D56	DQ56	181	182	DQ61	DDR_B_D60
DDR_B_D57	DQ57	183	184	VSS47	
	VSS48	185	186	DQS#7	DDR_B_DQS#7
	DM7	187	188	DQS7	DDR_B_DQS7
	VSS49	189	190	VSS50	
DDR_B_D59	DQ58	191	192	DQ62	DDR_B_D62
DDR_B_D58	DQ59	193	194	DQ63	DDR_B_D63
	VSS51	195	196	VSS52	
	SA0	197	198	EVENT#	
	VDDSPD	199	200	SDA	SOC_SMBDATA
DDR_B_SA1	SA1	201	202	SCL	SOC_SMBCLK
	VTT1	203	204	VTT2	+0.675VS_VTT
	G1	205	206	G2	

LCN_DAN06-K4406-0100
CONN@
SP07000N300

+3VS R229 2 1 10K_0402_5% +0.675VS_VTT
DDR_B_SA1

DDR_DRAMRST# 7,18 From CPU
CD30 .1U_0402_16V7K @

CAD NOTE
PLACE THE CAP NEAR TO
DIMM RESET PIN
2015MOW02, Can't install Cap on DRAMRST

+1.35V_VDDQ
+0.675V_DDRB_VREFCA
+0.675V_DDR_VREFCA
10mils
RD17 0_0402_5%
RD18 1.8K_0402_1%
RD19 2_0402_1%
RD20 1.8K_0402_1%
+0.675V_VREFCA
CD47 .1U_0402_16V7K
CD49 0.022U_0402_16V7K
RD21 24.9_0402_1%

Place near to SO-DIMM connector.

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: DDR3L DIMMB

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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Note: NGC6 3VSDGPU_MAIN_EN is no function

GPIO	I/O	USAGE
GPIO0	I	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BL_EN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16		RESERVED
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		
GPIO24		

GC6 2.0 function

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.	
Title	N16X PEG 1/9
Size: Custom	Document Number: A4WAS M/B LA-C611P
Rev	1.0
Date: Tuesday, June 16, 2015	Sheet 20 of 60

VRAM Interface

UGPU1
N16S-GT
SGT@
SA000087F10

UGPU1
N16V-GM
VGM@
SA000088R20

25,26 MDA[15..0] MDA[15..0]
25,26 MDA[31..16] MDA[31..16]
27,28 MDA[47..32] MDA[47..32]
27,28 MDA[63..48] MDA[63..48]

UGPU1B
Part 2 of 6
MEMORY INTERFACE A
GM108-ES-S-A1_FCBGA595
@

MDA	FBA_D	FBA_CMD	CMDA	DQMA	DQSA
MDA0 E18	FBA_D00	FBA_CMD0 C27	CMDA0	DQMA0	DQSA#0
MDA1 F18	FBA_D01	FBA_CMD1 C26	CMDA1	DQMA1	DQSA#1
MDA2 E16	FBA_D02	FBA_CMD2 E24	CMDA2	DQMA2	DQSA#2
MDA3 F17	FBA_D03	FBA_CMD3 F24	CMDA3	DQMA3	DQSA#3
MDA4 D20	FBA_D04	FBA_CMD4 D27	CMDA4	DQMA4	DQSA#4
MDA5 D21	FBA_D05	FBA_CMD5 D26	CMDA5	DQMA5	DQSA#5
MDA6 F20	FBA_D06	FBA_CMD6 F25	CMDA6	DQMA6	DQSA#6
MDA7 E21	FBA_D07	FBA_CMD7 F26	CMDA7	DQMA7	DQSA#7
MDA8 E15	FBA_D08	FBA_CMD8 F23	CMDA8		
MDA9 D15	FBA_D09	FBA_CMD9 G22	CMDA9		
MDA10 F15	FBA_D10	FBA_CMD10 G23	CMDA10		
MDA11 F13	FBA_D11	FBA_CMD11 G24	CMDA11		
MDA12 C13	FBA_D12	FBA_CMD12 F27	CMDA12		
MDA13 B13	FBA_D13	FBA_CMD13 G25	CMDA13		
MDA14 E13	FBA_D14	FBA_CMD14 G27	CMDA14		
MDA15 D13	FBA_D15	FBA_CMD15 G26	CMDA15		
MDA16 B15	FBA_D16	FBA_CMD16 M24	CMDA16		
MDA17 C16	FBA_D17	FBA_CMD17 M23	CMDA17		
MDA18 A13	FBA_D18	FBA_CMD18 K24	CMDA18		
MDA19 A15	FBA_D19	FBA_CMD19 K23	CMDA19		
MDA20 B18	FBA_D20	FBA_CMD20 M27	CMDA20		
MDA21 A18	FBA_D21	FBA_CMD21 M26	CMDA21		
MDA22 A19	FBA_D22	FBA_CMD22 M25	CMDA22		
MDA23 C19	FBA_D23	FBA_CMD23 K26	CMDA23		
MDA24 B24	FBA_D24	FBA_CMD24 K22	CMDA24		
MDA25 C23	FBA_D25	FBA_CMD25 J23	CMDA25		
MDA26 A25	FBA_D26	FBA_CMD26 J25	CMDA26		
MDA27 A24	FBA_D27	FBA_CMD27 J24	CMDA27		
MDA28 A21	FBA_D28	FBA_CMD28 K27	CMDA28		
MDA29 B21	FBA_D29	FBA_CMD29 K25	CMDA29		
MDA30 C20	FBA_D30	FBA_CMD30 J27	CMDA30		
MDA31 C21	FBA_D31	FBA_CMD31 J26	CMDA31		
MDA32 R22	FBA_D32	FBA_DQM0 D19	DQMA0		
MDA33 R24	FBA_D33	FBA_DQM1 D14	DQMA1		
MDA34 T22	FBA_D34	FBA_DQM2 C17	DQMA2		
MDA35 R23	FBA_D35	FBA_DQM3 C22	DQMA3		
MDA36 N25	FBA_D36	FBA_DQM4 P24	DQMA4		
MDA37 N26	FBA_D37	FBA_DQM5 W24	DQMA5		
MDA38 N23	FBA_D38	FBA_DQM6 AA25	DQMA6		
MDA39 N24	FBA_D39	FBA_DQM7 U25	DQMA7		
MDA40 V23	FBA_D40				
MDA41 V22	FBA_D41	FBA_DQS_RN0 F19	DQSA#0		
MDA42 T23	FBA_D42	FBA_DQS_RN1 C14	DQSA#1		
MDA43 U22	FBA_D43	FBA_DQS_RN2 A16	DQSA#2		
MDA44 Y24	FBA_D44	FBA_DQS_RN3 A22	DQSA#3		
MDA45 AA24	FBA_D45	FBA_DQS_RN4 P25	DQSA#4		
MDA46 Y22	FBA_D46	FBA_DQS_RN5 W22	DQSA#5		
MDA47 AA23	FBA_D47	FBA_DQS_RN6 AB27	DQSA#6		
MDA48 AD27	FBA_D48	FBA_DQS_RN7 T27	DQSA#7		
MDA49 AB25	FBA_D49				
MDA50 AD26	FBA_D50	FBA_DQS_WP0 E19	DQSA0		
MDA51 AC25	FBA_D51	FBA_DQS_WP1 C15	DQSA1		
MDA52 AA27	FBA_D52	FBA_DQS_WP2 B16	DQSA2		
MDA53 AA26	FBA_D53	FBA_DQS_WP3 B22	DQSA3		
MDA54 W26	FBA_D54	FBA_DQS_WP4 R25	DQSA4		
MDA55 Y25	FBA_D55	FBA_DQS_WP5 W23	DQSA5		
MDA56 R26	FBA_D56	FBA_DQS_WP6 AB26	DQSA6		
MDA57 T25	FBA_D57	FBA_DQS_WP7 T26	DQSA7		
MDA58 N27	FBA_D58				
MDA59 R27	FBA_D59				
MDA60 V26	FBA_D60				
MDA61 V27	FBA_D61				
MDA62 W27	FBA_D62				
MDA63 W25	FBA_D63				

CMDA[31..0] 25,26,27,28
DQMA[3..0] 25,26
DQMA[7..4] 27,28
DQSA#[3..0] 25,26
DQSA#[7..4] 27,28
DQSA[3..0] 25,26
DQSA[7..4] 27,28

PVT modify 01/13
DQSA, DQSA# reverse

FBA_CLK0 D24 FBA_CLK0_N D25 — CLKA0 25,26 CLKA0# 25,26
FBA_CLK1 N22 FBA_CLK1_N M22 — CLKA1 27,28 CLKA1# 27,28

FBA_WCK01 D18 FBA_WCK01_N C18 FBA_WCK23 D17 FBA_WCK23_N D16 FBA_WCK45 T24 FBA_WCK45_N U24 FBA_WCK67 V24 FBA_WCK67_N V25

F16 FB_PLLAVDD_1
P22 FB_PLLAVDD_2
T97 @ D23 FB_VREF_PROBE
H22 FB_DLLAVDD
F3 FB_CLAMP
F22 FBA_CMD34
J22 FBA_CMD35

NV 15x DG-06803-V03

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

SM010019400 3000ma 33ohm@100mhz DCR 0.05

+1.05VSDGPU — VGA@ — L2002 CHILISIN PBY160808T-330Y-N — +FB_PLLAVDD

15+55mA

C2008 VGA@ 22U_0603_6.3V6M
C2011 VGA@ 1U_0402_16V7
C2010 VGA@ 1U_0402_16V7
C2009 VGA@ 1U_0402_16V7

Place Near GPU Place Under F16 P22 H22

1 VGA@ 2 FB_CLAMP
10K_0402_5% R2028

change to 1.35VSDGPU

+1.5VSDGPU — 60.4_0402_1% R2020 FBA_CMD34 — 60.4_0402_1% R2022 FBA_CMD35

+1.5VSDGPU

A5MUB exchange

RP33: CMDA23, CMDA21
RP42: CMDA24, CMDA26
RP43: CMDA10, CMDA22
RP44: CMDA4, CMDA12
RP45: CMDA8, CMDA14
RP46: CMDA9, CMDA29
RP47: CMDA5, CMDA13
RP48: CMDA6, CMDA7
RP49: CMDA27, CMDA30
RP50: CMDA28, CMDA25
RP51: CMDA15, CMDA11

VGA@ 100_0804_8P4R_5%

+1.5VSDGPU
C2084 C2083 C2086 C2085 C2088 C2087 C2090 C2089 C2091 C2092 C2093
.1U_0402_16V7K @

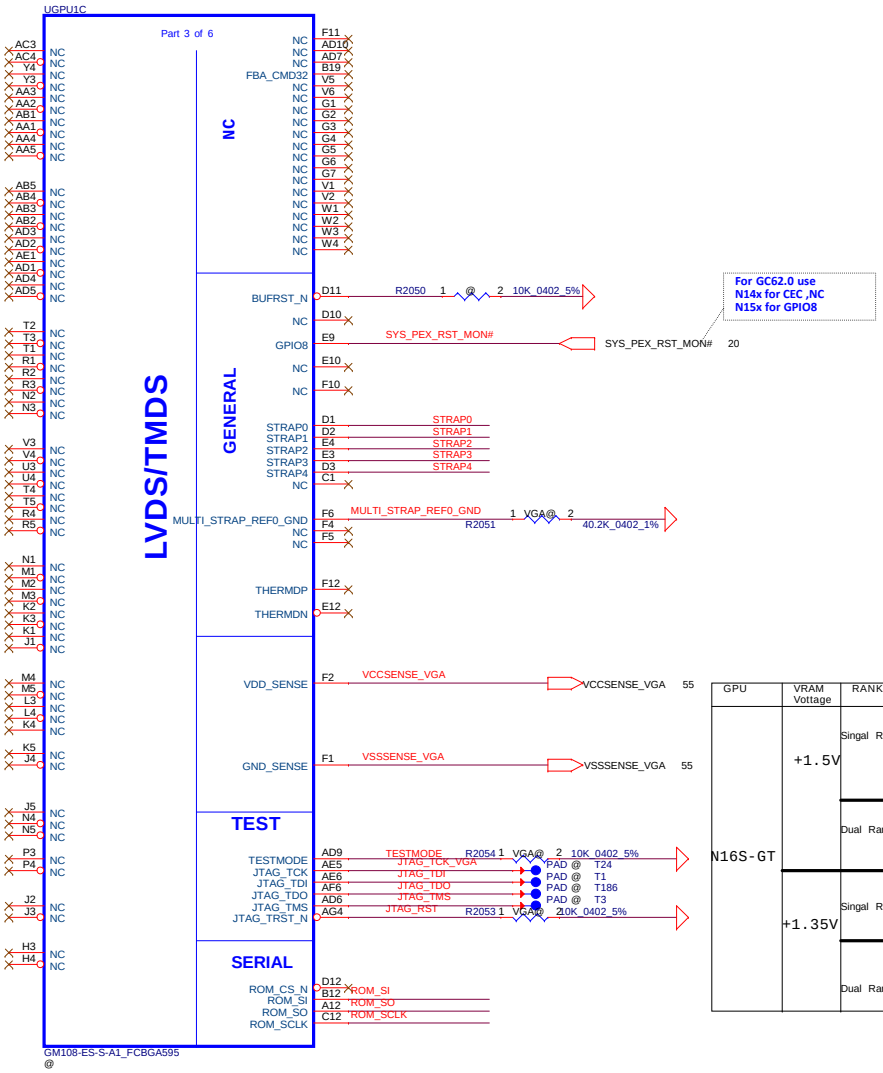
Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

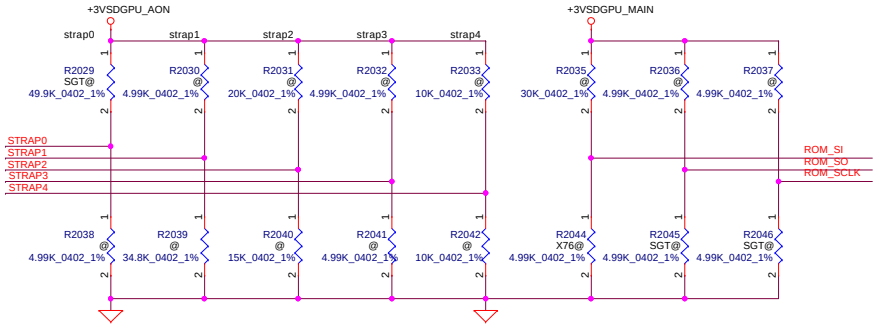
Title: N16X VRAM 2/9

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 21 of 60



MULTI LEVEL STRAPS



N16VGM Option Component

```
STRAP0  --->  R2029 2 VGM@ 1  45.3K_0402_1%  SD034453280
STRAP1  --->  R2039 2 VGM@ 1  45.3K_0402_1%  SD034453280
STRAP2  --->  R2031 2 VGM@ 1  10K_0402_1%    SD034100280
STRAP3  --->  R2041 2 VGM@ 1  4.99K_0402_1%  SD034499180
STRAP4  --->  R2042 2 VGM@ 1  45.3K_0402_1%  SD034453280
ROM_SO  --->  R2036 2 VGM@ 1  4.99K_0402_1%  SD034499180
ROM_SCLK--->  R2037 2 VGM@ 1  4.99K_0402_1%  SD034499180

ROM_SI pull down 15kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x2
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x4
ROM_SI pull up 35kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0xE
ROM_SI pull up 30kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0xD
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
ROM_SI pull up 25kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0xC
```

N16SGT Option Component

```
ROM_SI pull down 4.99kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x0
ROM_SI pull down 10kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x1
ROM_SI pull down 15kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x2
ROM_SI pull down 20kohm to GND for DDR3 Hynix 256mx16 VRAM, strap 0x3
ROM_SI pull down 25kohm to GND for DDR3 Micron 256mx16 VRAM, strap 0x4
ROM_SI pull down 30kohm to GND for DDR3 Samsung 256mx16 VRAM, strap 0x5
```

For N16S-GT Multi strap table

Decive ID : 0x1347

GPU	VRAM Vottage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16S-GT	+1.5V	Singal Rank	X76629B0L07	1GHz	256Mx16x4 2GB	0x5 (SA00008DN10) Hynix H5TC4G63CFR-N0C	PU 50K	NC	NC	NC	NC	PD 30K	PD 4.99K	PD 4.99K
			X76629B0L08			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629B0L09			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
			X76629B0L14			0x4 (SA000076PB0) Samsung K4W4G1646E-BC1A						PD 24.9K		
		Dual Rank	X76629B0L10	1GHz	256Mx16x8 4GB	0xC (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 24.9K		
			X76629B0L11			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629B0L12			0x2 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 15K		
	+1.35V	Singal Rank		900MHz	256Mx16x4 2GB	0x2 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PD 15K		
						0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 24.9K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		
		Dual Rank		900MHz	256Mx16x8 4GB	0xE (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 35K		
						0x4 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 24.9K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		

For N16V-GM Multi strap table

Decive ID : 0x1299

GPU	VRAM Vottage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N16V-GM	+1.5V	Singal Rank	X76629B0L01	1GHz	256Mx16x4 2GB	0x9 (SA00008DN10) Hynix H5TC4G63CFR-N0C	PU 45.3K	PD45.3K	PU 10K	PD 4.99K	PD 45.3K	PU 10K	PU 4.99K	PU 4.99K
			X76629B0L02			0x1 (SA000077K20) Micron MT41J256M16HA-093G:E						PD 10K		
			X76629B0L03			0x4 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 24.9K		
			X76629B0L13			0xA (SA000076PB0) Samsung K4W4G1646E-BC1A						PU 15K		
	+1.35V	Singal Rank		900MHz	256Mx16x4 2GB	0x0 (SA00008DN10) Hynix H5TC4G63CFR-N0C						PD 5K		
						0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 30K		
						0x5 (SA000076P20) Samsung K4W4G1646D-BC1A						PD 30K		
		Dual Rank	X76629B0L04	900MHz	256Mx16x8 4GB	0xA (SA00008DN10) Hynix H5TC4G63CFR-N0C						PU 15K		
			X76629B0L05			0xD (SA000077K20) Micron MT41J256M16HA-093G:E						PU 30K		
			X76629B0L06			0xC (SA000076P20) Samsung K4W4G1646D-BC1A						PU 24.9K		

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: N16X STRAPS 3/9

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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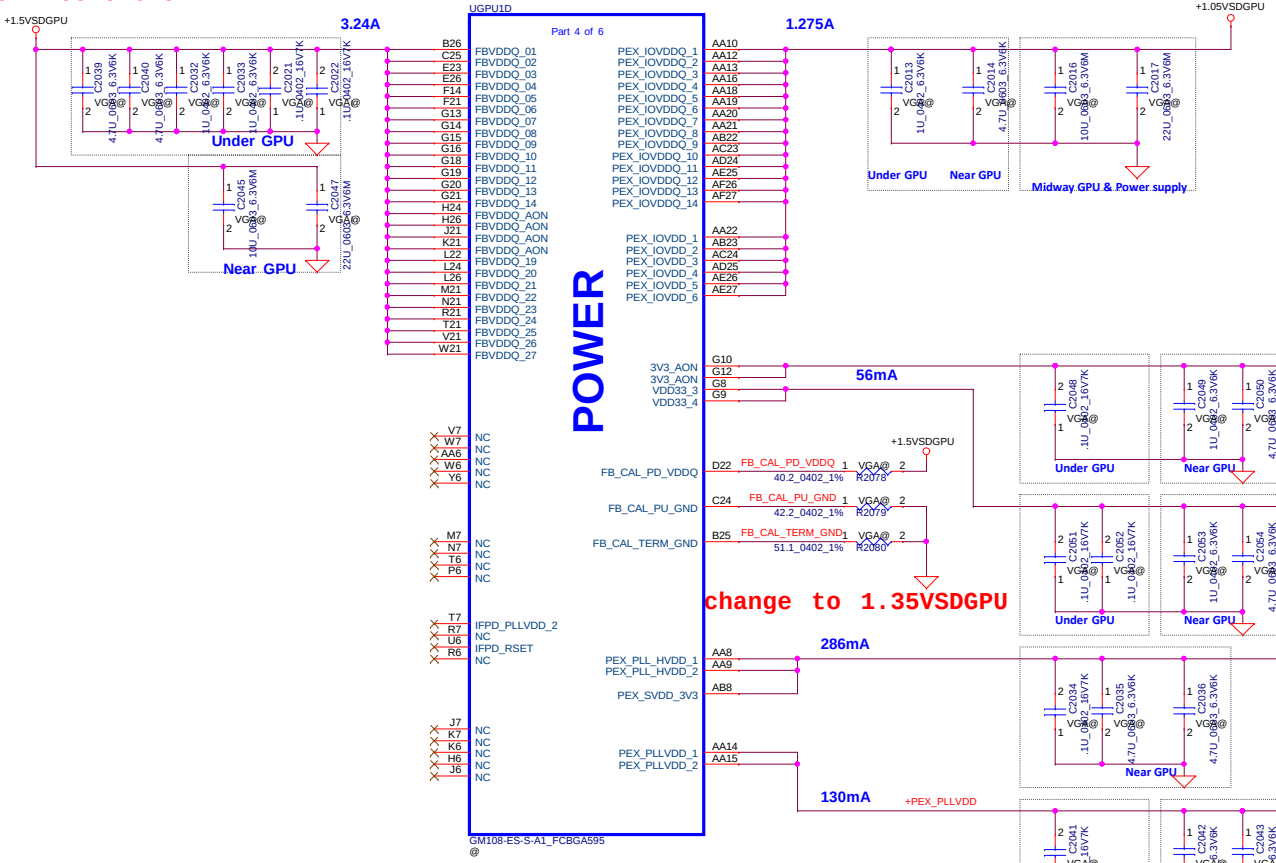
NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64 DDR3	0.1μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply

change to 1.35VSDGPU



GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1μF	X6S	0402	2	2	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X5R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X6S	0402	1	Under GPU
1.0 μF	X5R	0603	1	Near GPU
4.7 μF	X5R	0805	1	Near GPU

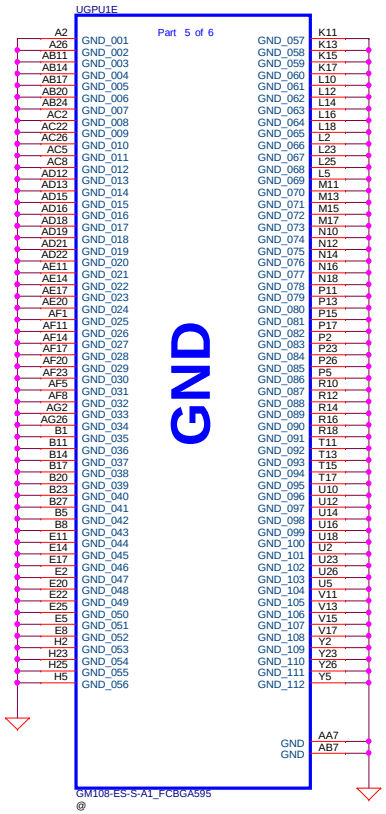
Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

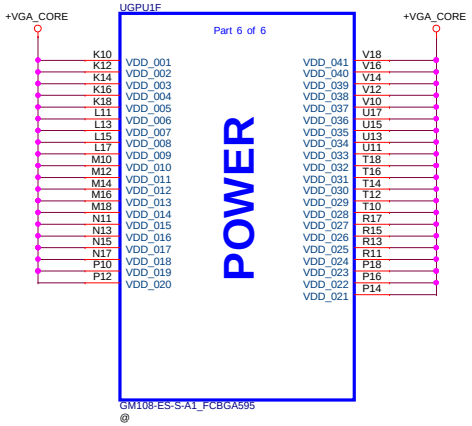
Compal Electronics, Inc.

Title: N16X POWER & GND 4/9

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 23 of 60





NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core — (A)	FB Total 1.5/1.35V (A)	1.05V Total 1.05V (A)
~~N15S-GM~~	~~DDR3/L~~	~~48.11~~	~~4.23~~	~~0.91~~
N15S-GT	DDR3/L	60.07	4.26	0.91

DA-06925-V05

Table 6. EDP-Peak at T_J = 102°C

Power Supply Rail	N15V-GM-S DDR3/L
(V)	(A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

DA07075-V01

Table 7. EDP-Peak at T_J = 102°C

Power Supply Rail	N15V-GL DDR3
(V)	(A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: N16X POWER & GND 5/9

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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VRAM DDR3 chips

21,26,27,28 DQSA[7..0] → DQSA[7..0]
21,26,27,28 DQSA#[7..0] → DQSA#[7..0]
21,26,27,28 DQMA[7..0] → DQMA[7..0]
21,26,27,28 MDA[63..0] → MDA[63..0]
21,26,27,28 CMDA[30..0] → CMDA[30..0]

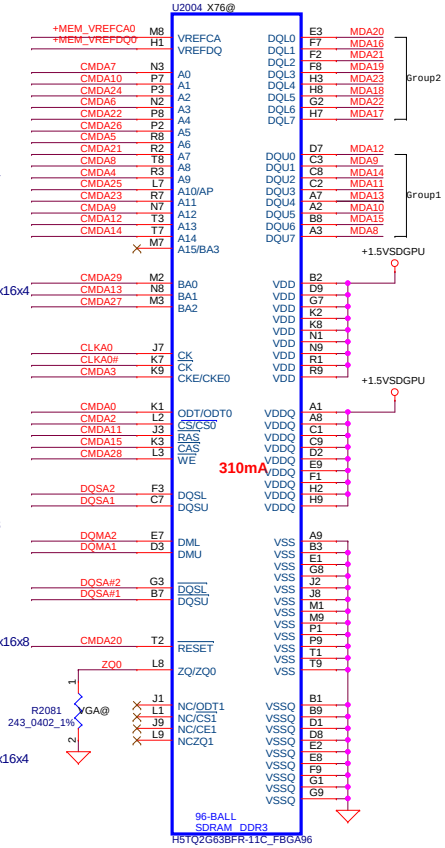
Lower Rank 0 BOT SIDE

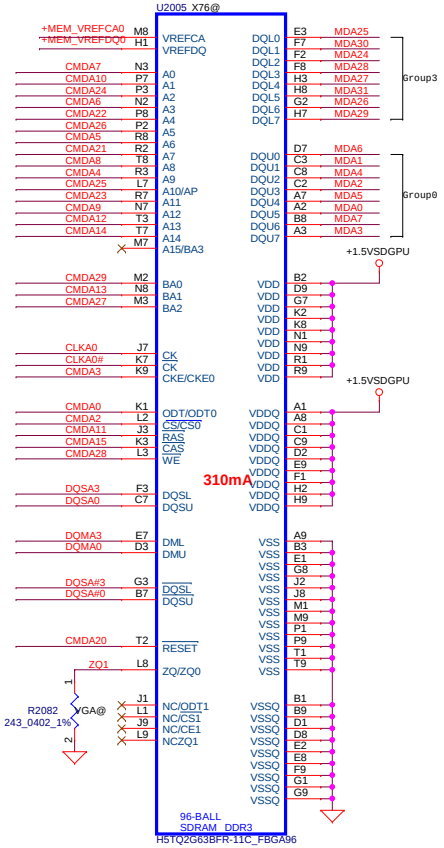
X76 for VGM

- X7601@ — X76629BOL01 — 2Gb Hynix 256Mx16x4
- X7602@ — X76629BOL02 — 2Gb Micron 256Mx16x4
- X7603@ — X76629BOL03 — 2Gb Samsung-D 256Mx16x4
- X7604@ — X76629BOL04 — 4Gb Hynix 256Mx16x8
- X7605@ — X76629BOL05 — 4Gb Micron 256Mx16x8
- X7606@ — X76629BOL06 — 4Gb Samsung-D 256Mx16x8
- X7613@ — X76629BOL13 — 2Gb Samsung-E 256Mx16x4

X76 for SGT

- X7607@ — X76629BOL07 — 2Gb Hynix 256Mx16x4
- X7608@ — X76629BOL08 — 2Gb Micron 256Mx16x4
- X7609@ — X76629BOL09 — 2Gb Samsung-D 256Mx16x4
- X7610@ — X76629BOL10 — 4Gb Hynix 256Mx16x8
- X7611@ — X76629BOL11 — 4Gb Micron 256Mx16x8
- X7612@ — X76629BOL12 — 4Gb Samsung-D 256Mx16x8
- X7614@ — X76629BOL14 — 2Gb Samsung-E 256Mx16x4



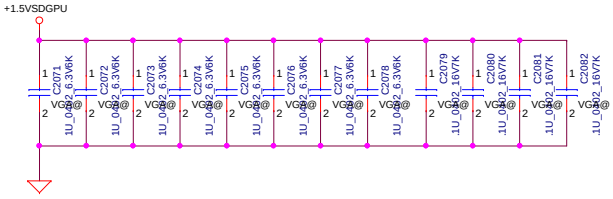


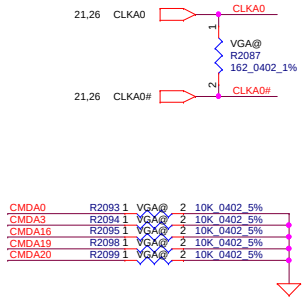
Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

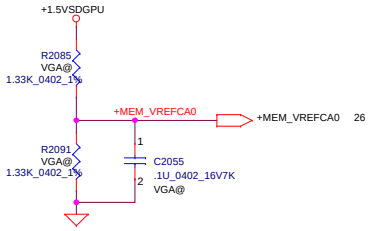
	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

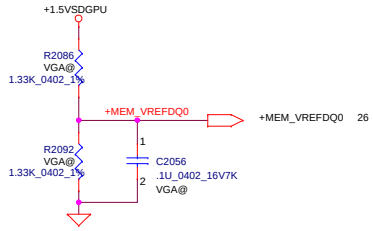
Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population FBVDDQ	Population FBVDD	Location
FBVDD/Q Combined					
0.1 µF	X7R	0402	2		Under DRAM
1.0 µF	X7R	0603	4		Under DRAM
10 µF	X5R	0805	0		Close to DRAM









Security Classification	Compal Secret Data	
Issued Date	2014/11/10	Deciphered Date 2016/11/10

Compal Electronics, Inc.

Title: N16X Upper Rank0 6/9

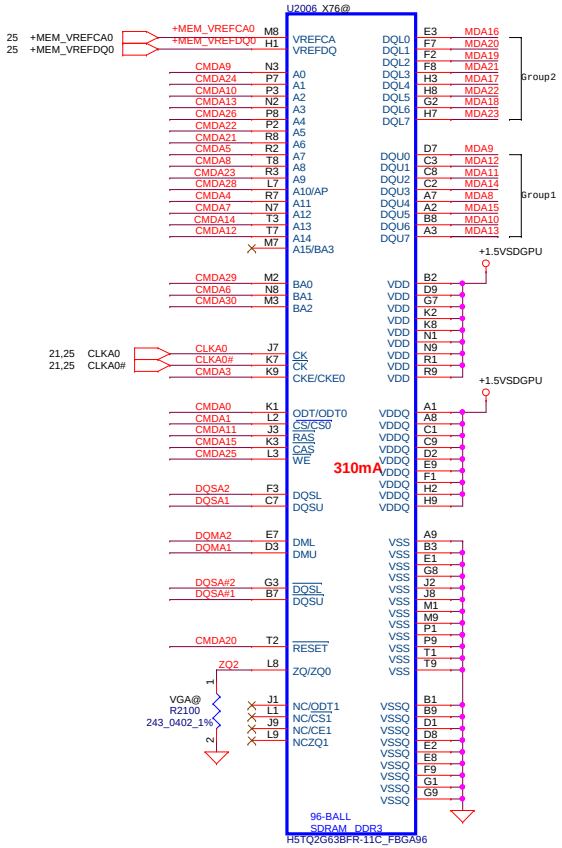
Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

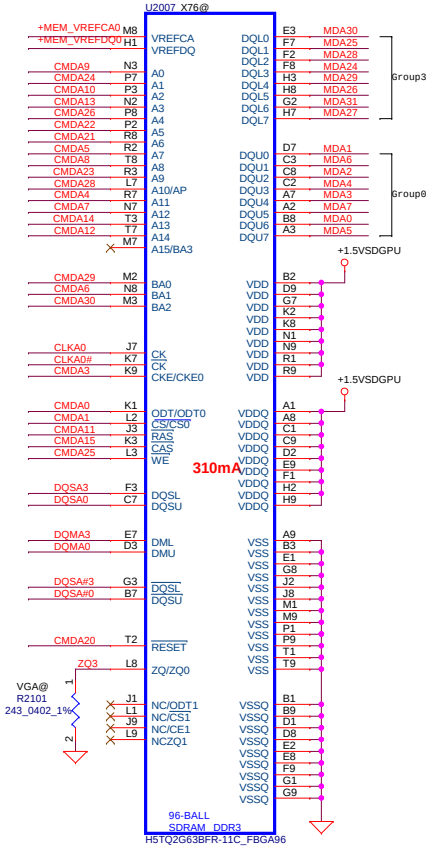
Date: Tuesday, June 16, 2015 | Sheet 25 of 60

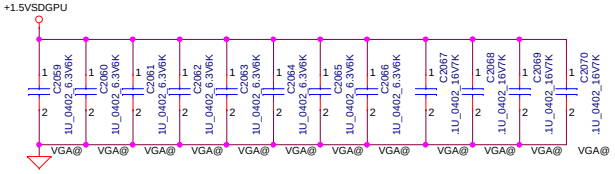
VRAM DDR3 chips

21,25,27,28 DQSA[7..0] → DQSA[7..0]
21,25,27,28 DQSA#[7..0] → DQSA#[7..0]
21,25,27,28 DQMA[7..0] → DQMA[7..0]
21,25,27,28 MDA[63..0] → MDA[63..0]
21,25,27,28 CMDA[30..0] → CMDA[30..0]

Lower Rank 1 TOP SIDE







Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: N16X Upper Rank1 7/9

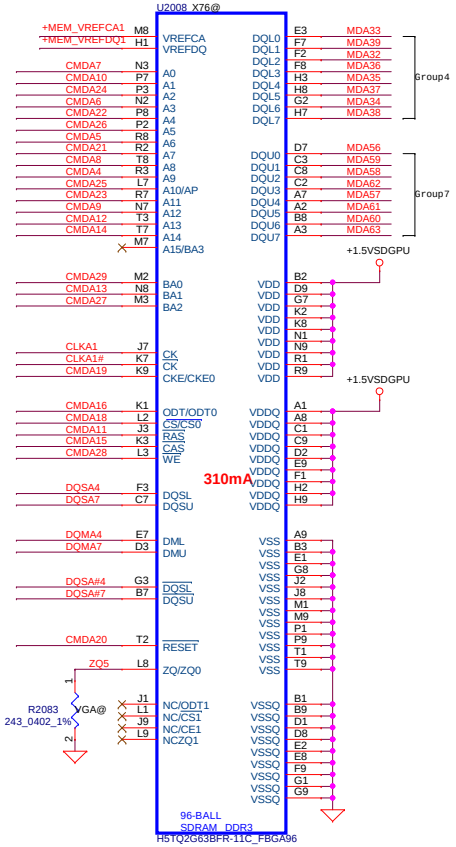
Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

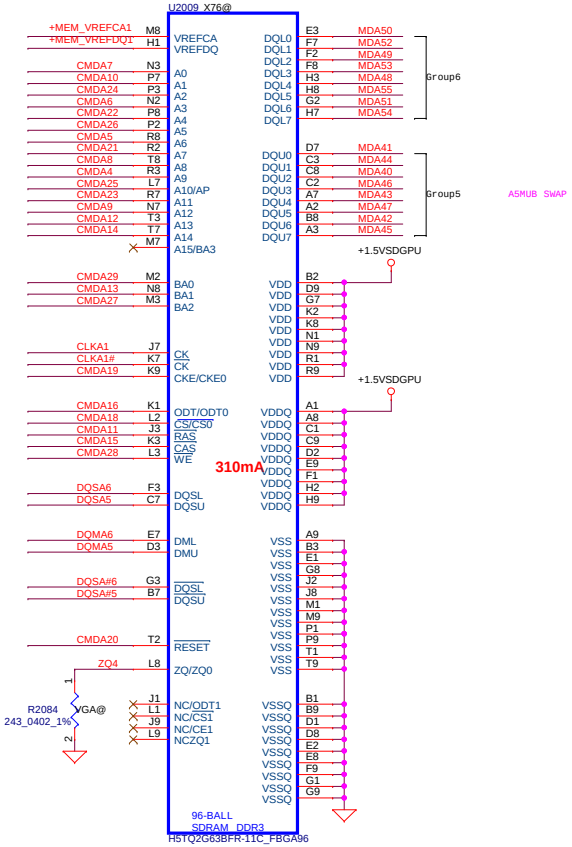
Date: Tuesday, June 16, 2015 | Sheet 26 of 60

VRAM DDR3 chips

21,25,26,28 DQSA[7..0] → DQSA[7..0]
21,25,26,28 DQSA#[7..0] → DQSA#[7..0]
21,25,26,28 DQMA[7..0] → DQMA[7..0]
21,25,26,28 MDA[63..0] → MDA[63..0]
21,25,26,28 CMDA[30..0] → CMDA[30..0]

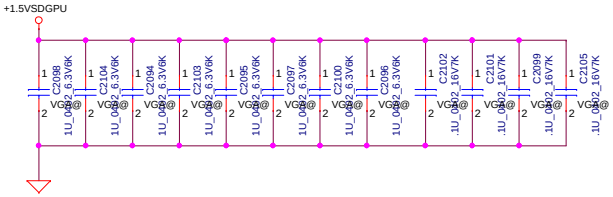
Upper Rank 0 BOT SIDE

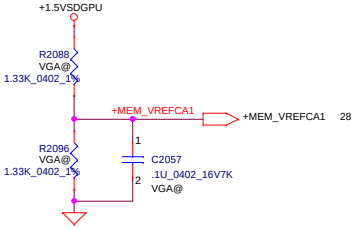


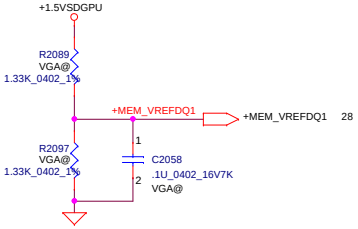


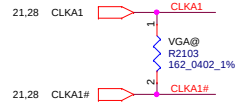
Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination









Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: N16X Lower Rank0 8/9

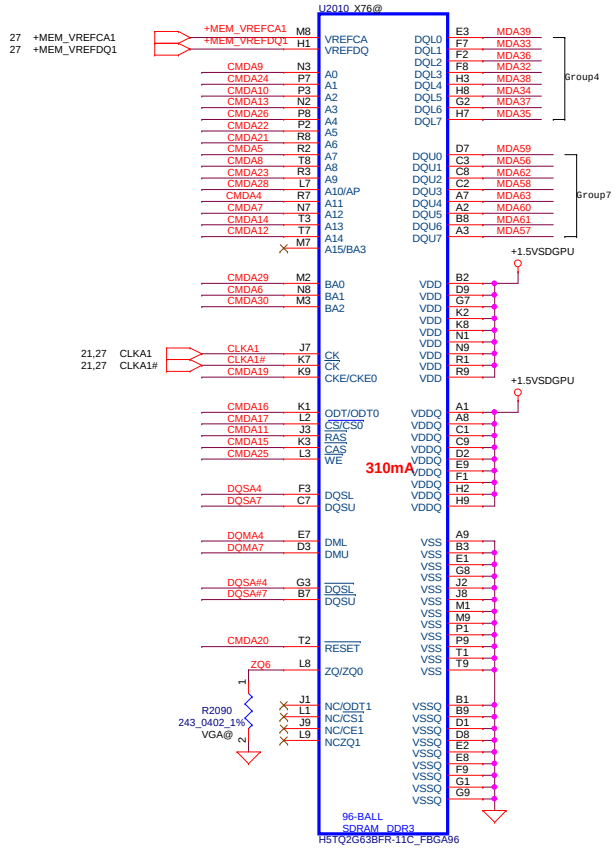
Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

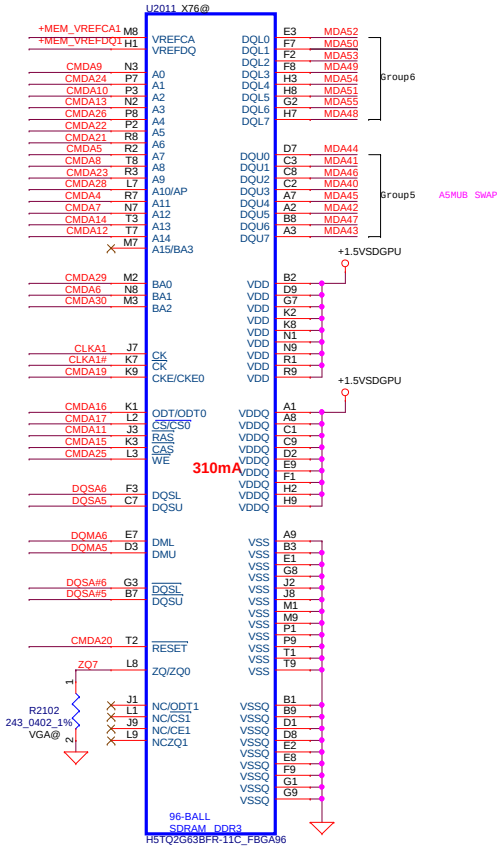
Date: Tuesday, June 16, 2015 | Sheet 27 of 60

VRAM DDR3 chips

21,25,26,27 DQSA[7..0] → DQSA[7..0]
21,25,26,27 DQSA#[7..0] → DQSA#[7..0]
21,25,26,27 DQMA[7..0] → DQMA[7..0]
21,25,26,27 MDA[63..0] → MDA[63..0]
21,25,26,27 CMDA[30..0] → CMDA[30..0]

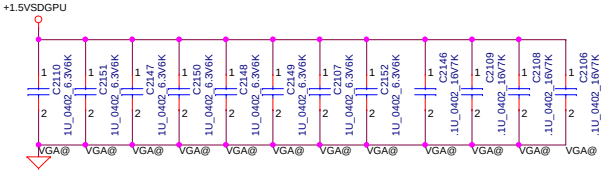
Upper Rank 1 TOP SIDE





Mode E Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1*	
CMD2	CS0*			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS*	RAS*	RAS*	RAS*
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS*	CAS*	CAS*	CAS*
CMD16		ODT		ODT
CMD17				CS1*
CMD18		CS0*		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE*	WE*
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE*	WE*	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2
Not Available				

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

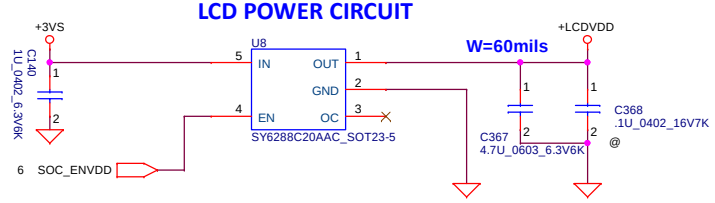
Compal Electronics, Inc.

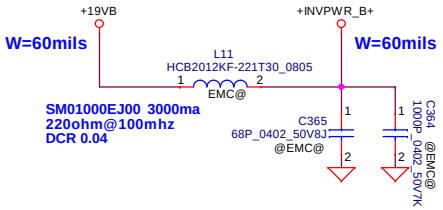
Title: N16X Lower Rank1 9/9

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

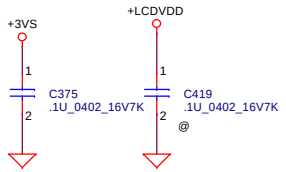
Date: Tuesday, June 16, 2015 | Sheet 28 of 60

LCD POWER CIRCUIT

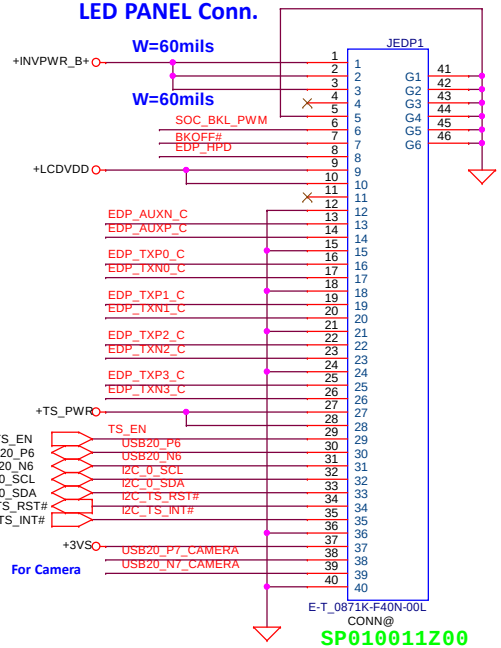


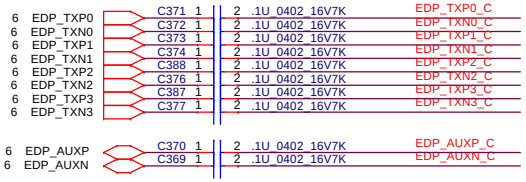


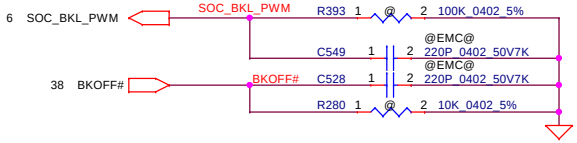
Place closed to JEDP1

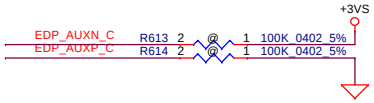


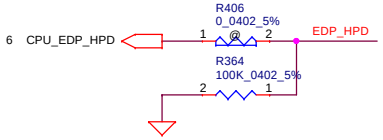
LED PANEL Conn.



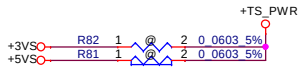




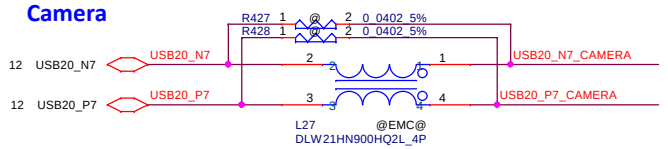




I2C Touch Screen



Camera



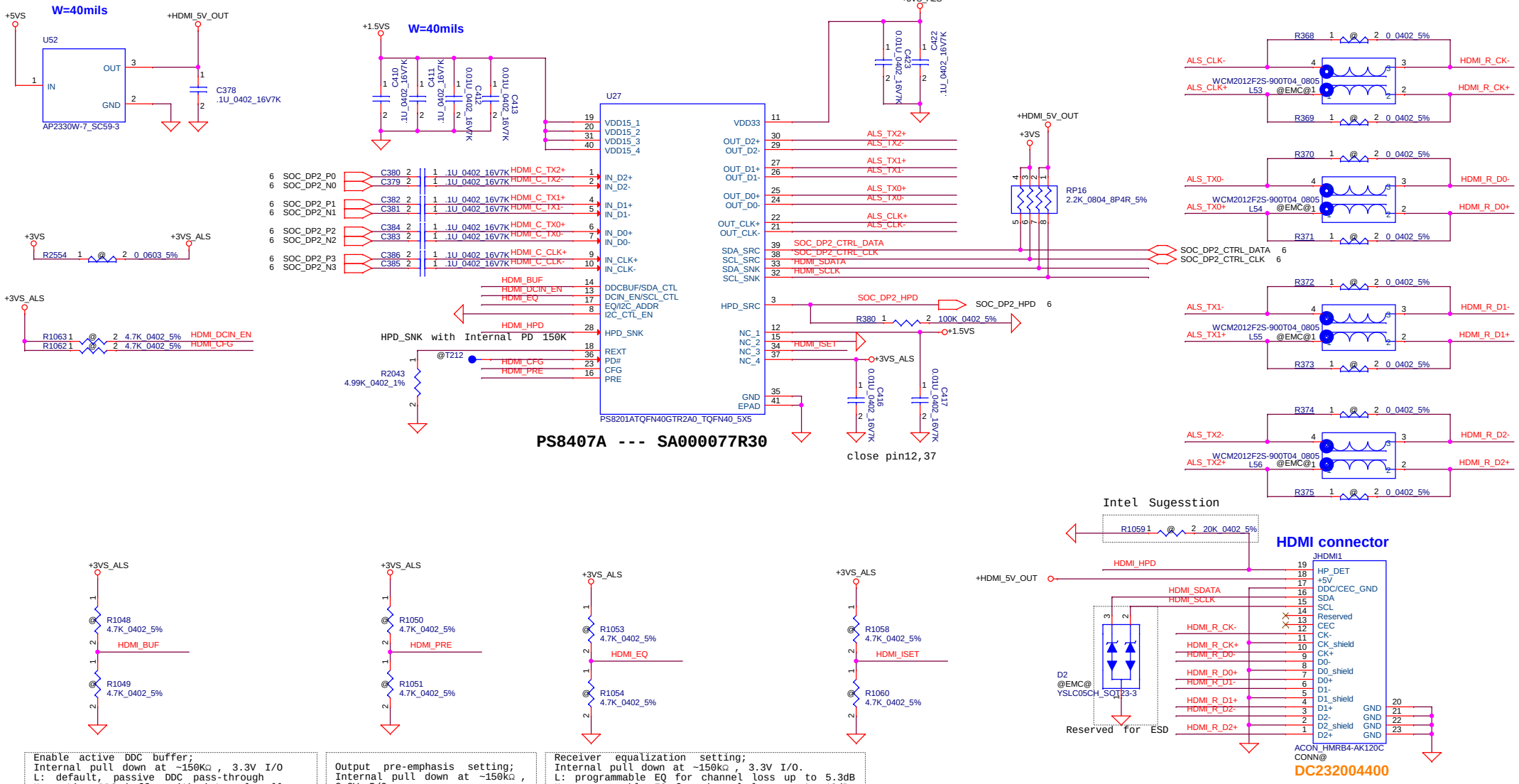
Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: **eDP Connector**

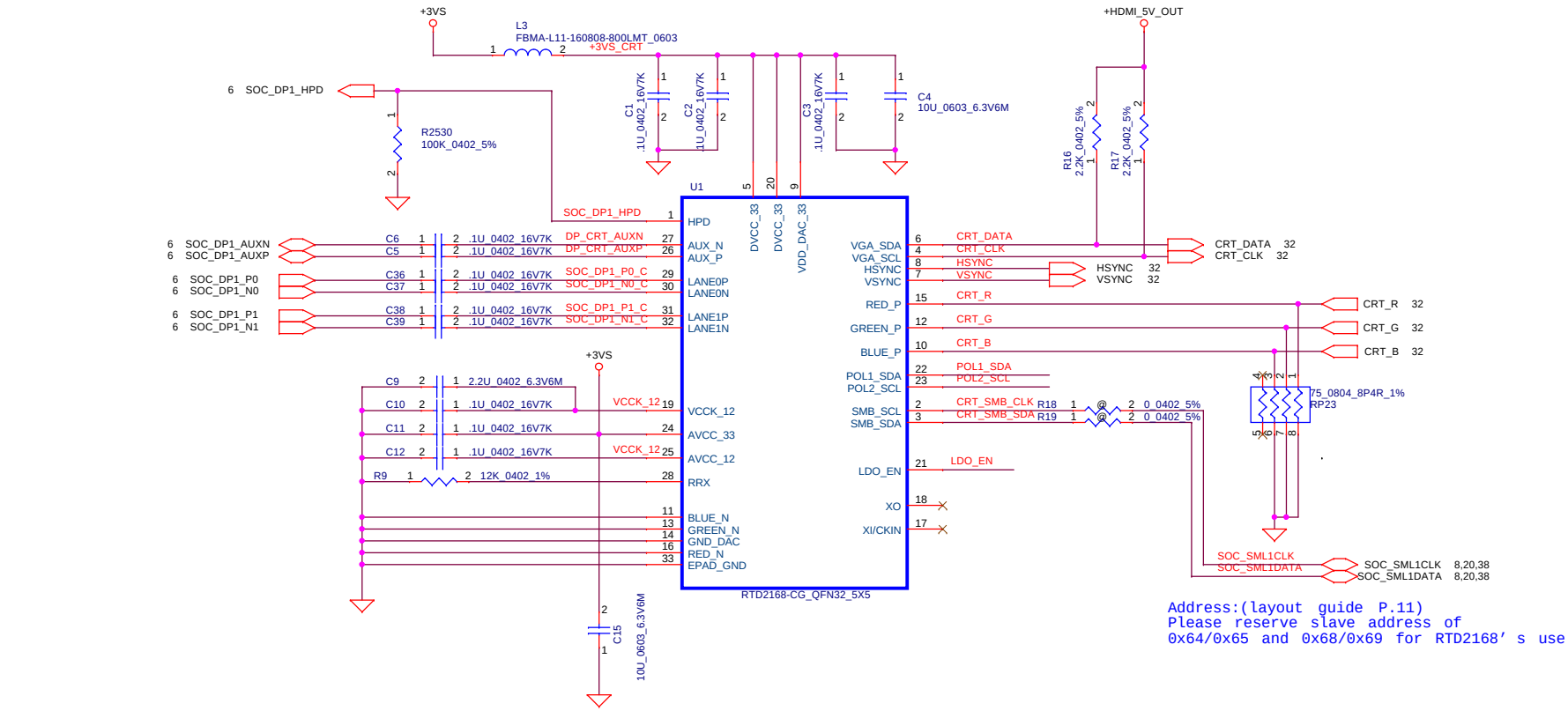
Size	Document Number	Rev
Custom	A4WAS M/B LA-C611P	1.0

Date: Tuesday, June 16, 2015 Sheet 29 of 60

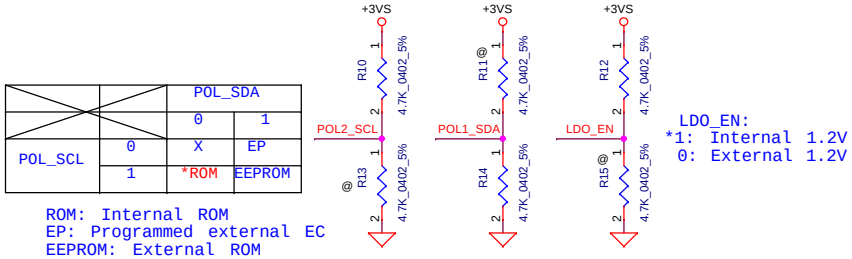


Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title	HDMI CONN.		
Size	Document Number		Rev
Custom	A4WAS M/B LA-C611P		1.0
Date:	Tuesday, June 16, 2015	Sheet	30 of 60



Address:(layout guide P.11)
Please reserve slave address of
0x64/0x65 and 0x68/0x69 for RTD2168' s use



		POL_SDA	
		0	1
POL_SCL	0	X	EP
	1	*ROM	EEPROM

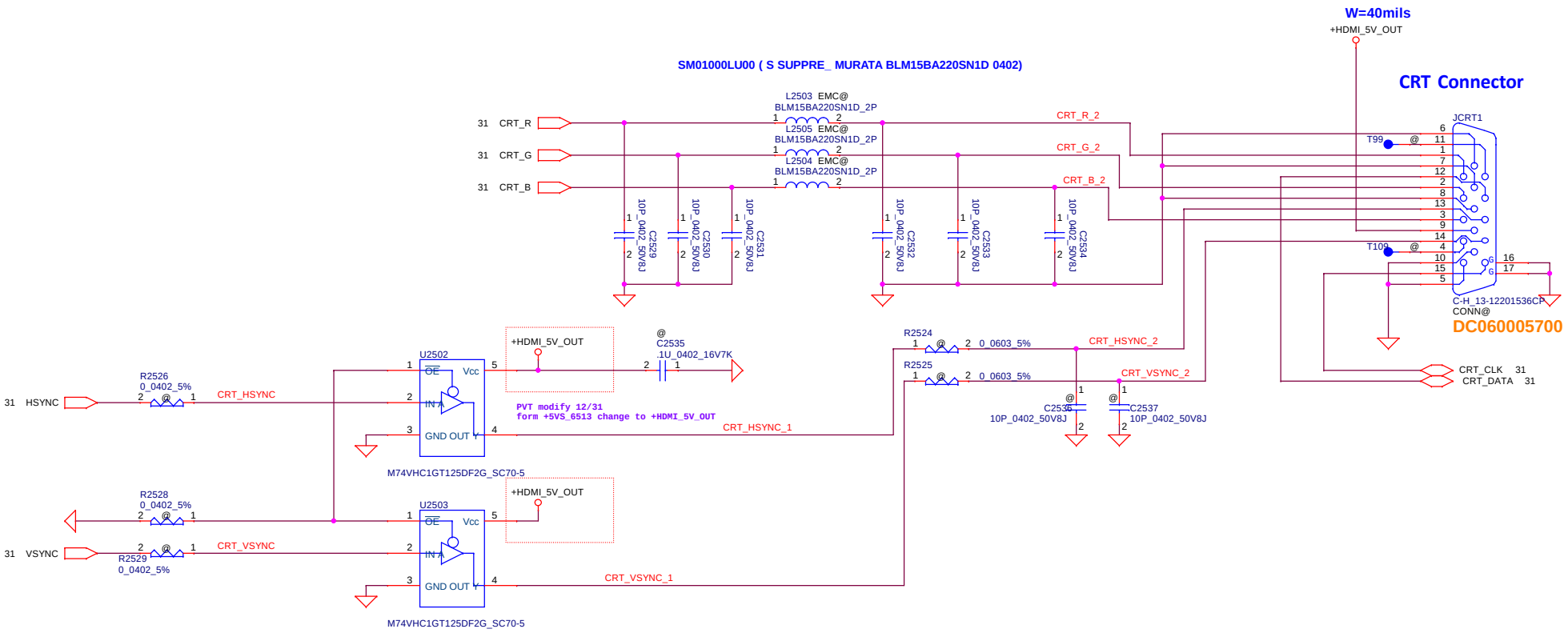
ROM: Internal ROM
EP: Programmed external EC
EEPROM: External ROM

LDO_EN:
*1: Internal 1.2V
0: External 1.2V

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title	Realtek RTD2168		
Size	Document Number		Rev
Custom	A4WAS M/B LA-C611P		1.0
Date:	Tuesday, June 16, 2015	Sheet 31 of 60	

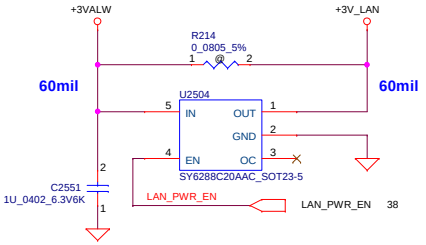
CRT conn.



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: CRT Connector			
Size: Custom	Document Number: A4WAS M/B LA-C611P		Rev: 1.0
Date: Tuesday, June 16, 2015	Sheet 32 of 60		

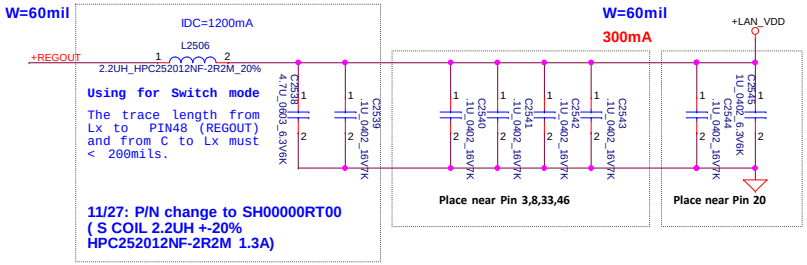
LAN-RTL8411B

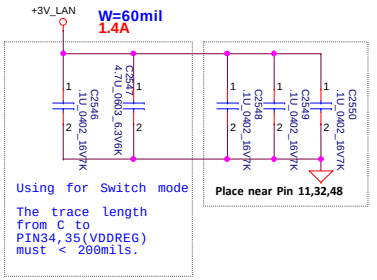


From EC

High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

+3V_LAN Rising time must >0.5ms and <100ms

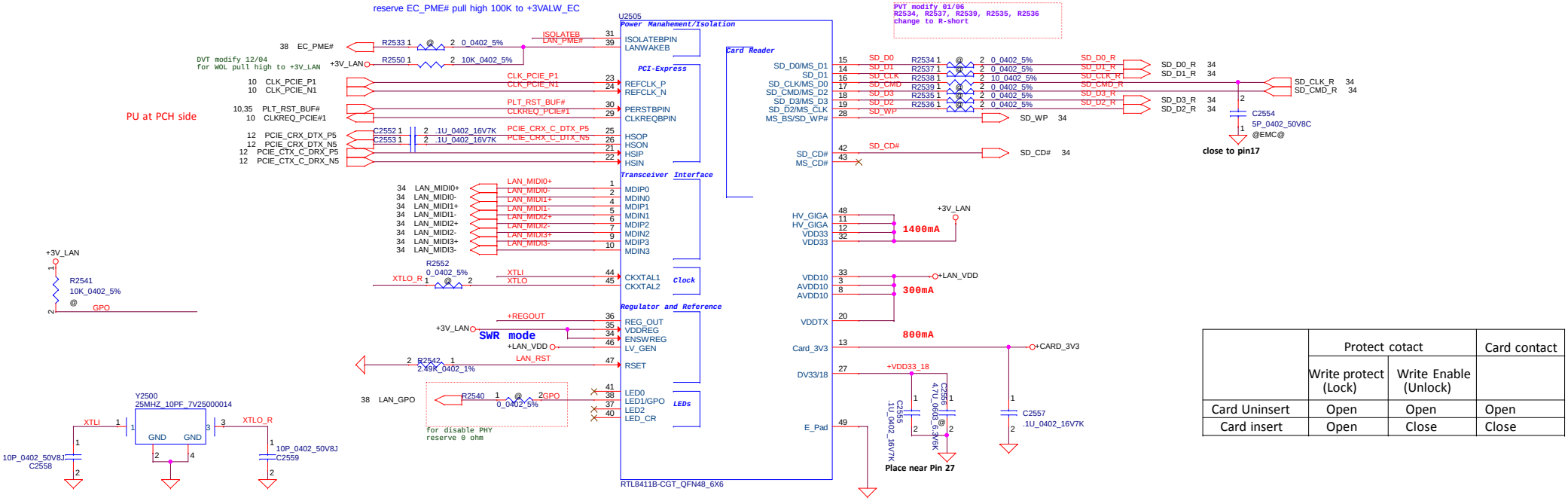


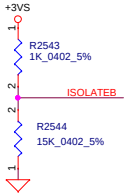


reserve EC_PME# pull high 100K to +3VALW_EC

PU at PCH side

PVT modify 01/06
R2534, R2537, R2539, R2535, R2536
change to R-short





	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: LAN RTL8411B

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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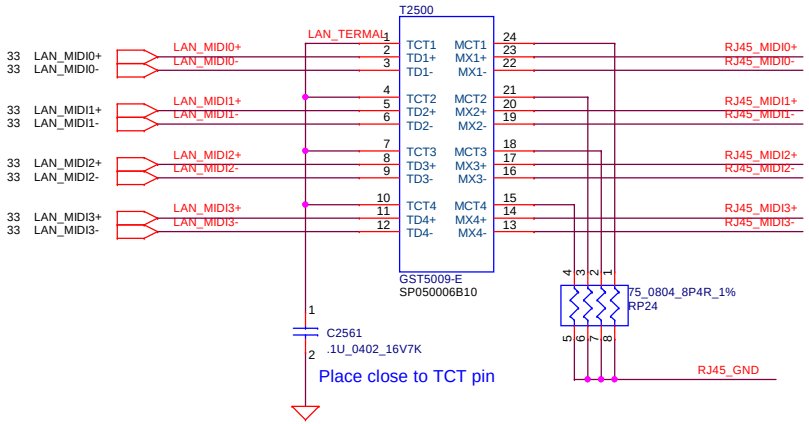
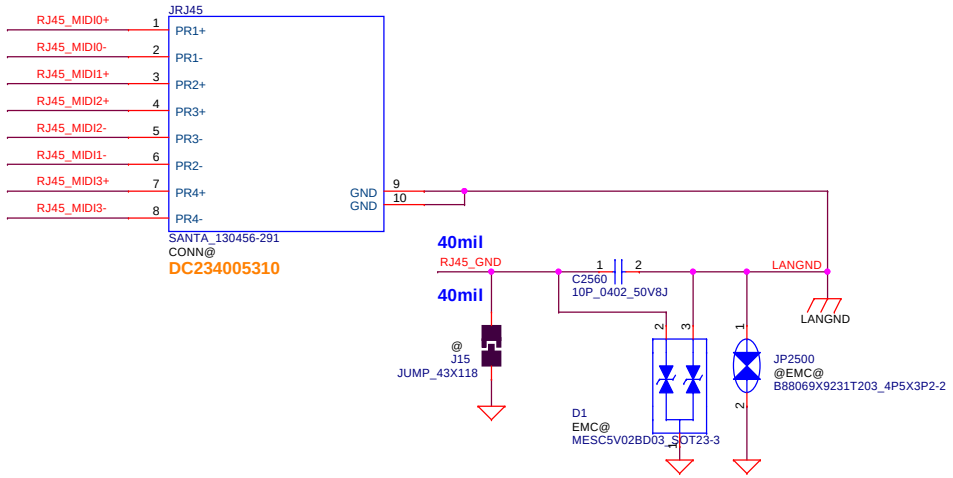
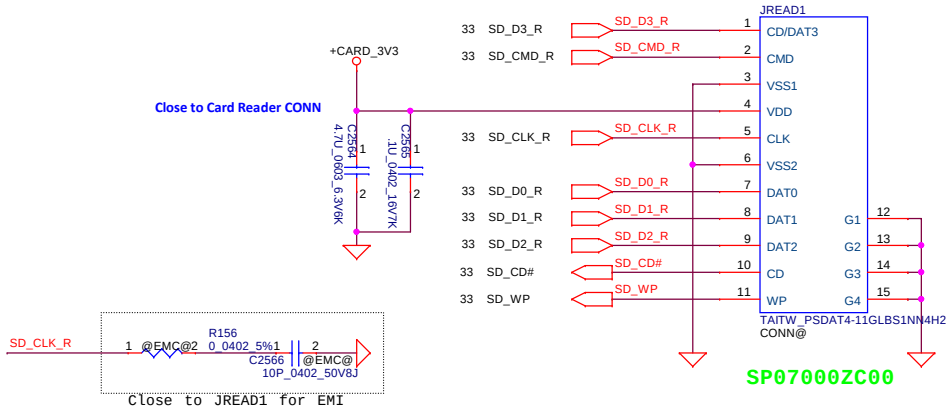
LAN Connector





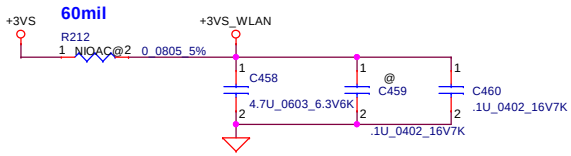
Card Reader Connector

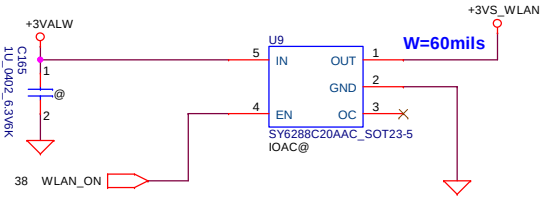


Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: LAN RJ45/CR SD Connector			
Size: Custom	Document Number: A4WAS M/B LA-C611P		Rev: 1.0
Date: Tuesday, June 16, 2015	Sheet 34 of 60		

Wireless LAN

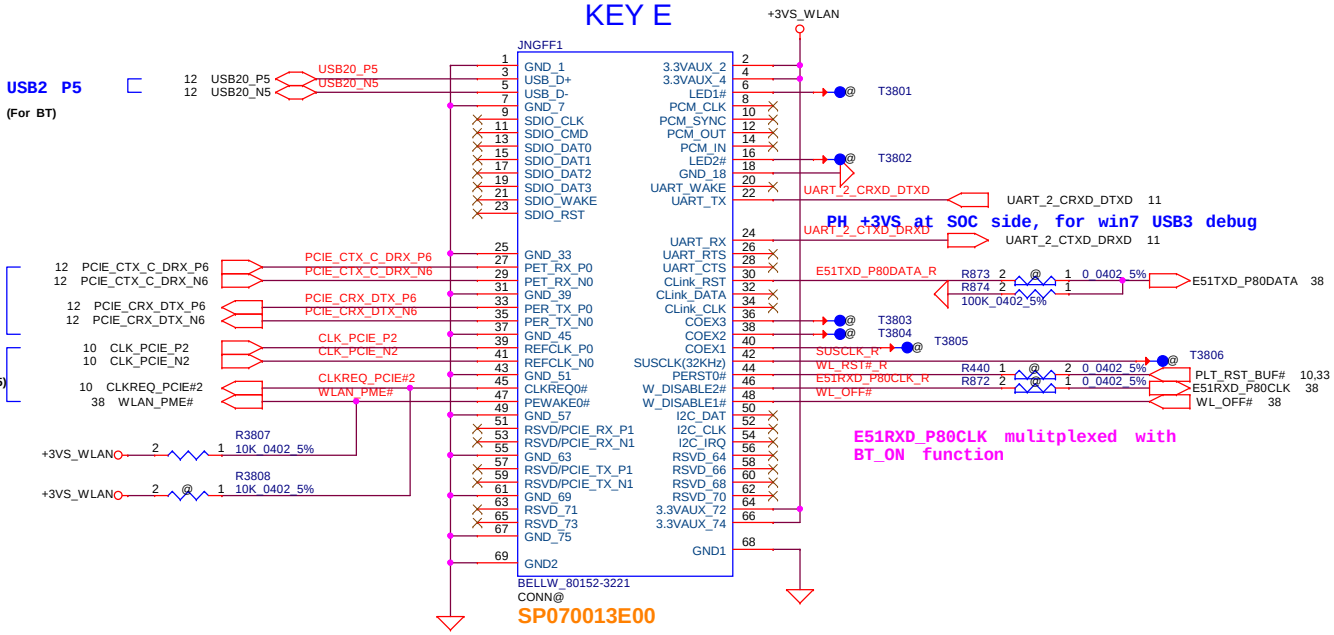




NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UIM_Power_SRC/GPIO1/PEWake1#	RESERVED/REFCLKP1	71
68	UIM_Power_SNK/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (I)(0/3.3)	GND	63
60	I2C CLK (O)(0/3.3)	Reserved/PETn1	61
58	I2C DATA (I/O)(0/3.3)	Reserved/PETp1	59
56	W_DISABLE#1 (O)(0/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (O)(0/3.3V)	PEWake0# (IO)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (IO)(0/3.3V)	53
50	SUSCLK(32kHz) (O)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKN0	49
46	COEX2(I/O)(0/1.8V)	REFCLKP0	47
44	COEX3(I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0/1.8V)	PETn0	37
34	UART CTS (I)(0/1.8V)	PETp0	35
32	UART Tx (O)(0/1.8V)	GND	33
	[redacted]	[redacted]	
22	UART Rx (I)(0/1.8V)	SDIO Reset# (O)(0/1.8V)	23
20	UART Wake# (I)(0/3.3V)	SDIO Wake# (I)(0/1.8V)	21
18	GND	SDIO DATA3(IO)(0/1.8V)	19
16	LED#2 (I)(OD)	SDIO DATA2(IO)(0/1.8V)	17
14	PCM_OUT/I2S SD_OUT (O)(0/1.8V)	SDIO DATA1(IO)(0/1.8V)	15
12	PCM_IN/I2S SD_IN (I)(0/1.8V)	SDIO DATA0(IO)(0/1.8V)	13
10	PCM_SYNC/I2S WS (O)(0/1.8V)	SDIO CMD(I/O)(0/1.8V)	11
8	PCM_CLK/I2S SCK (O)(0/1.8V)	SDIO CLK(O)(0/1.8V)	9
6	LED#1 (I)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

KEY E



3.1.8.1.3.1.7.1. UART Wakeup

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

- ~~RDX~~ UART_RXD (Input): Receive Data
- ~~RTX~~ UART_TXD (Output): Transmit Data
- UART_RTS (Input): Request to Send (Host Flow Control)
- UART_CTS (Output): Clear to Send (Device Flow Control)
- ~~Host Wake Up~~UART_Wake# (Output): Host wake-up line is optional in case the host support in band wake-up

Compal Electronics, Inc.

Title: **M.2 Key E (WLAN)**

Size	Document Number	Rev
Custom	A4WAS M/B LA-C611P	1.0

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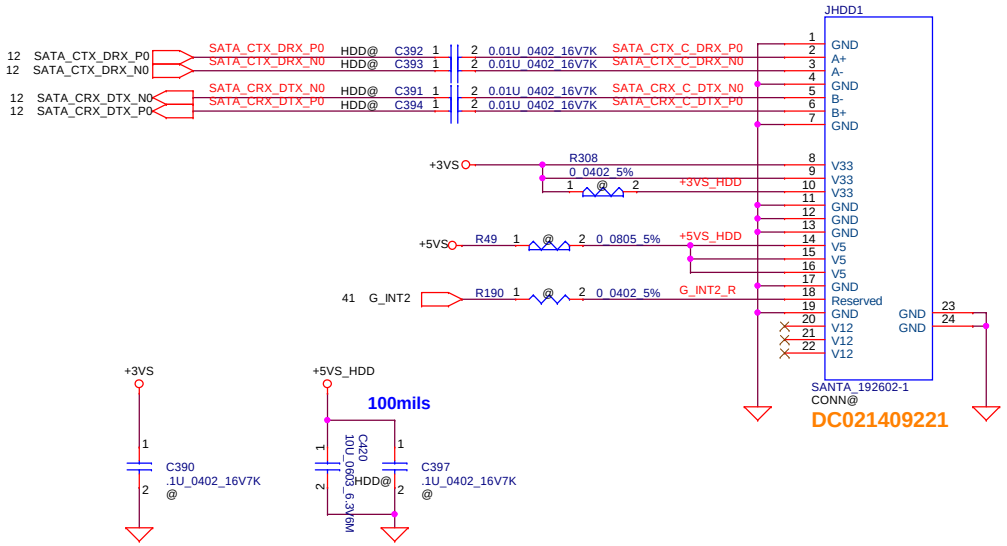
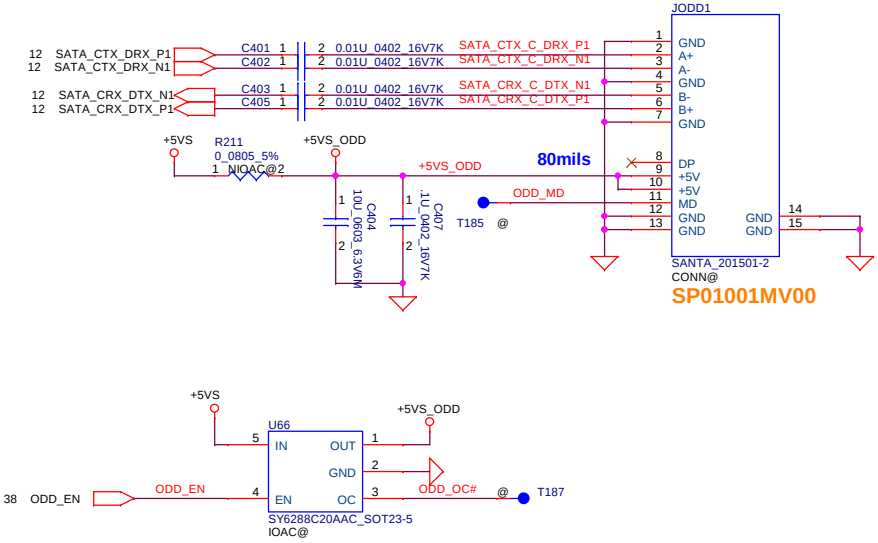
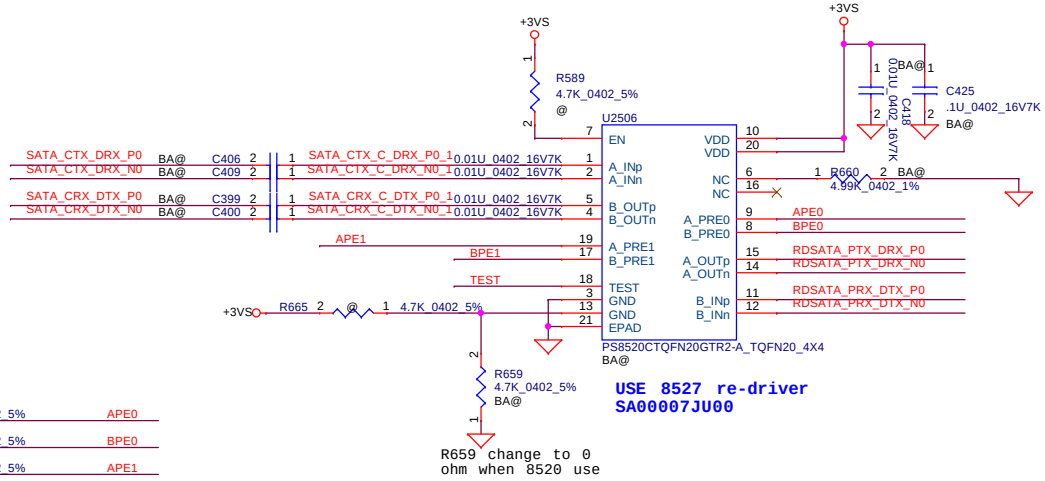
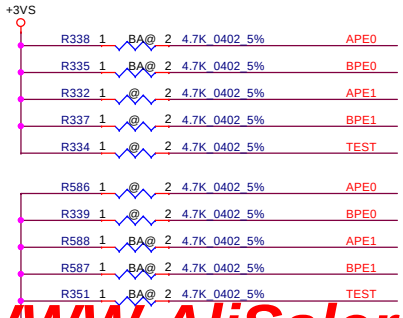
SATA HDD Conn.



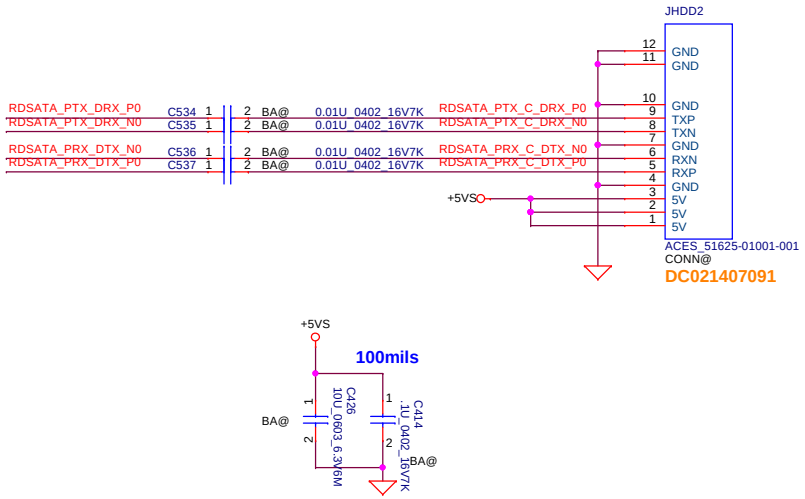
SATA ODD Conn.







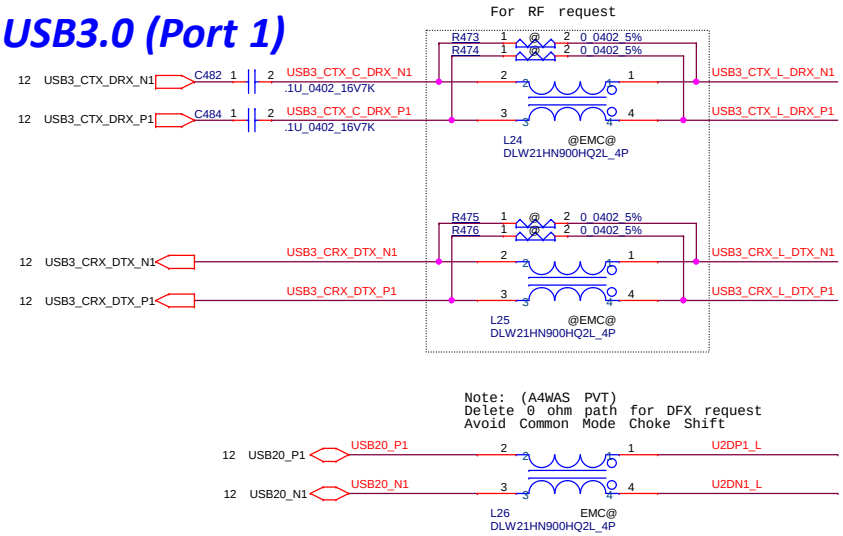
SATA HDD Conn.

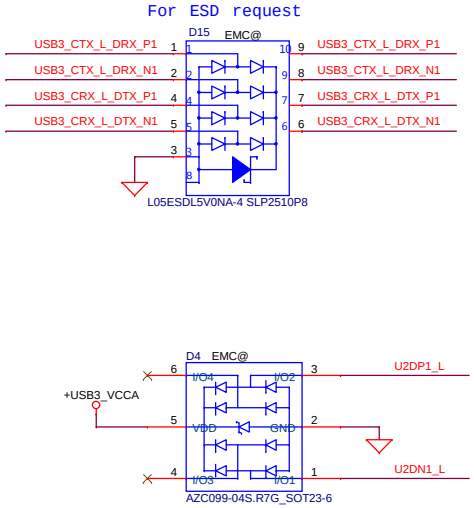


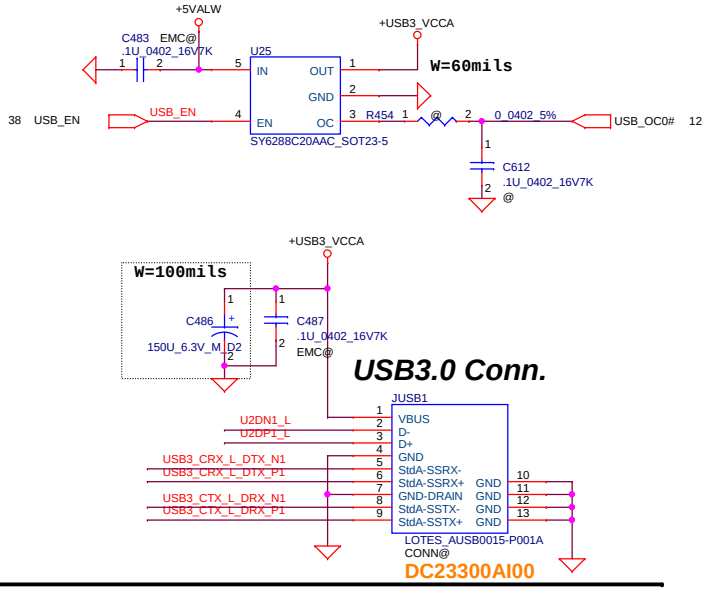
Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: HDD/ODD/ HDD Re-Driver			
Size: Custom	Document Number: A4WAS M/B LA-C611P		Rev: 1.0
Date: Tuesday, June 16, 2015	Sheet 36 of 60		

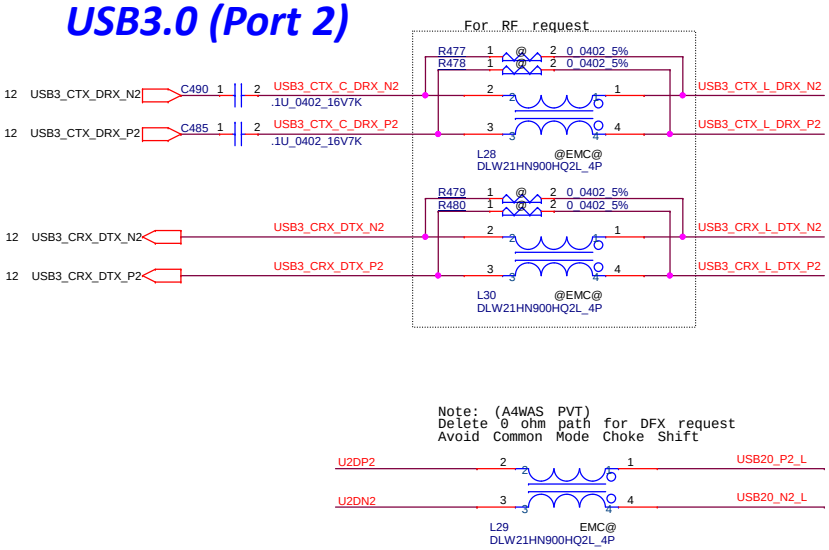
USB3.0 (Port 1)

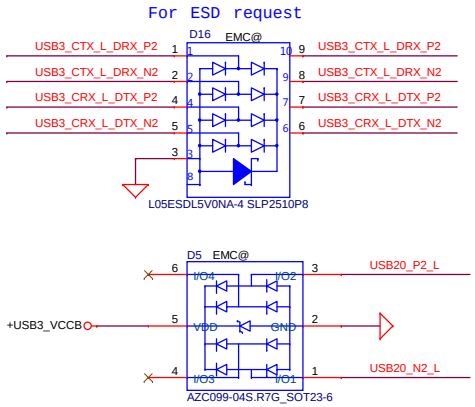


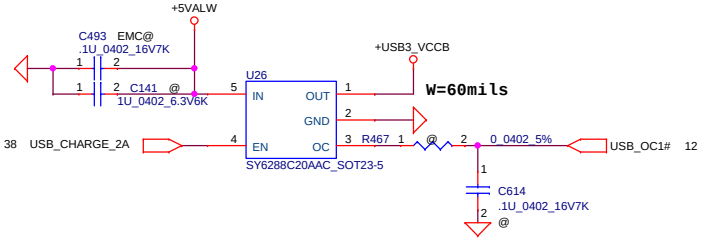


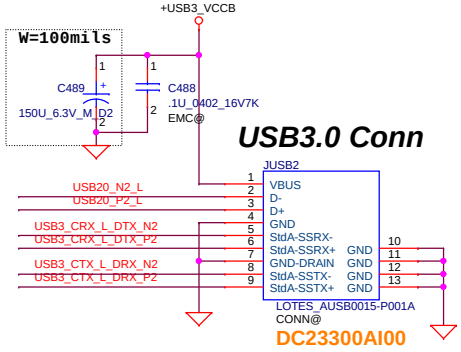


USB3.0 (Port 2)



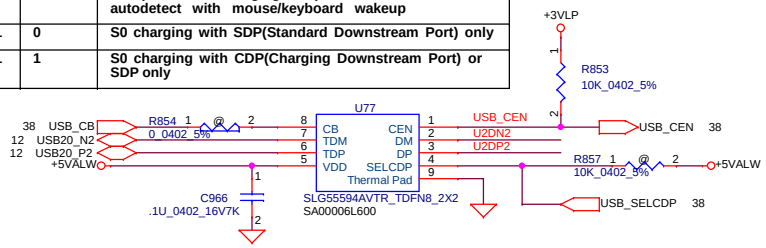


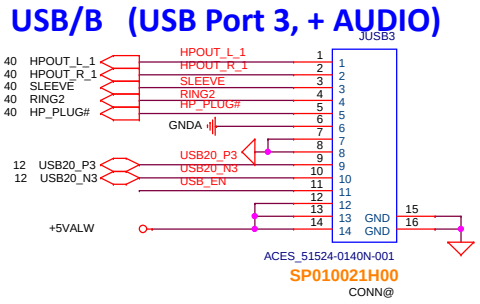




USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



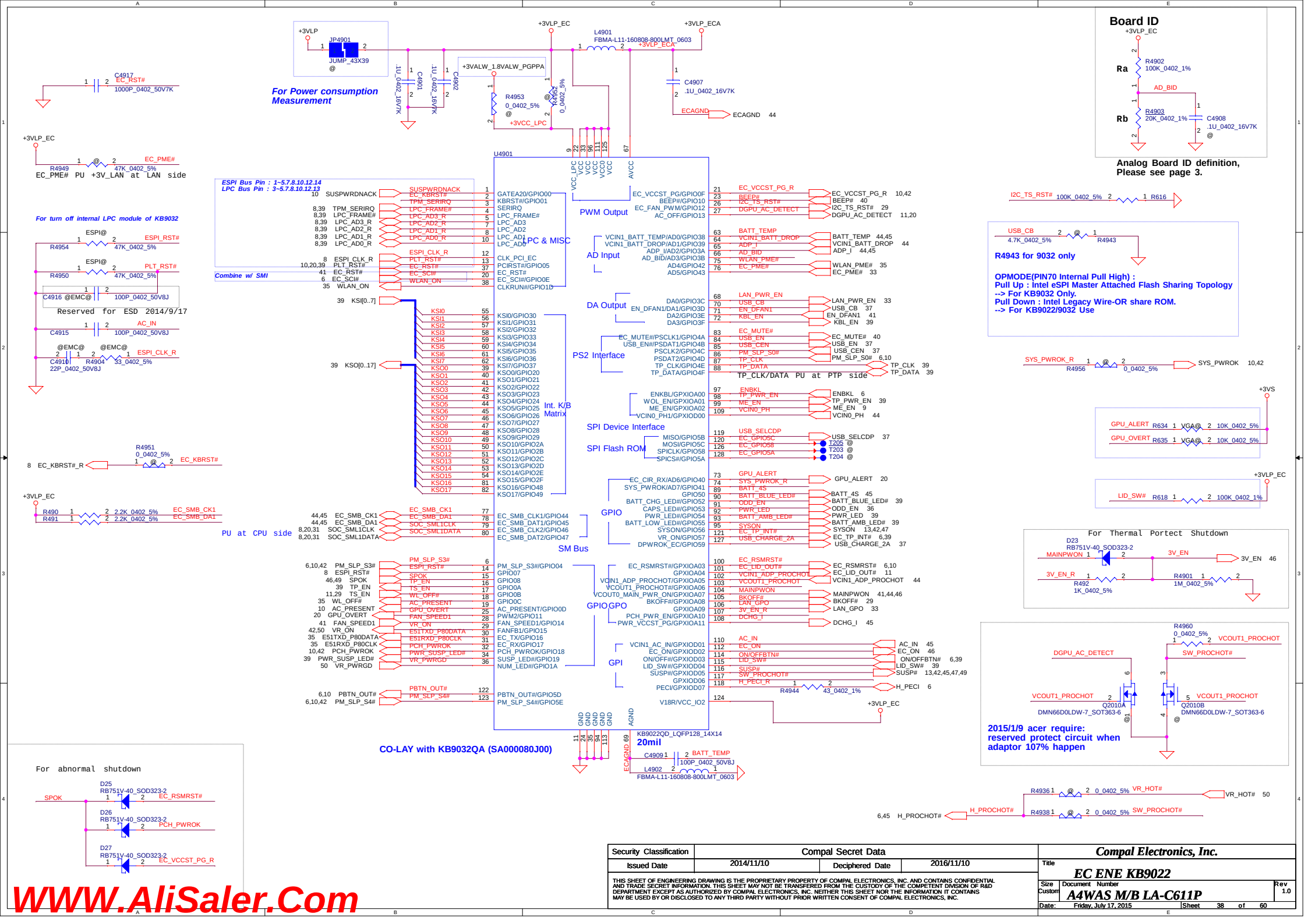


Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: **USB3.0 Conn/USB_B**

Size	Document Number	Rev
Custom	A4WAS M/B LA-C611P	1.0
Date: Tuesday, June 16, 2015	Sheet 37 of 60	



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

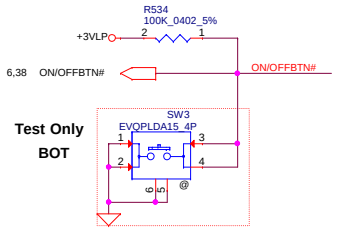
Title: EC ENE KB9022

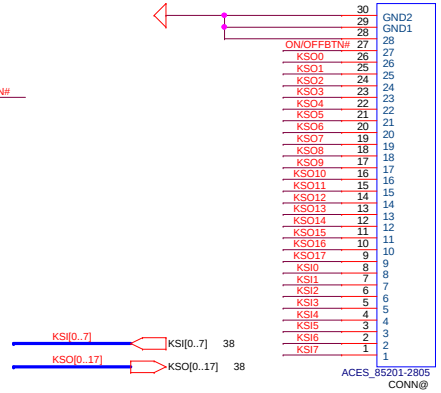
Size	Document Number	Rev
Custom	A4WAS M/B LA-C611P	1.0

Date: Friday, July 17, 2015 Sheet 38 of 60

KB Conn.

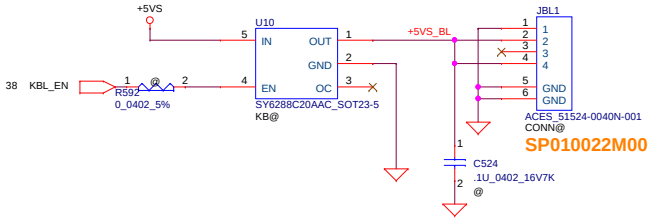
ON/OFF BTN





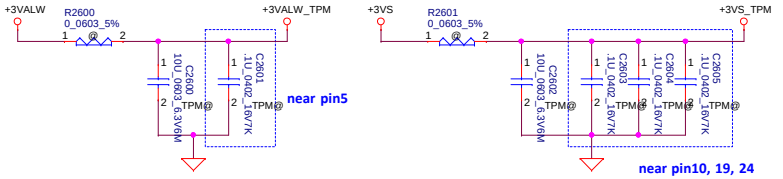
SP01000GO00

KB BackLight Conn. Reserve

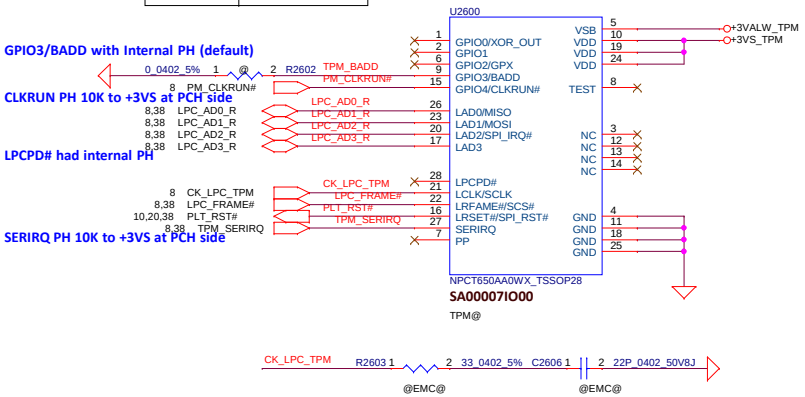


SP010022M00

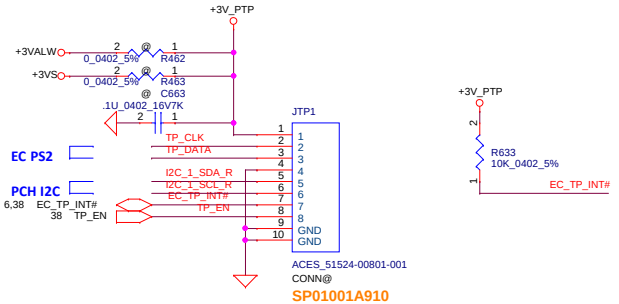
TPM Board for 2015



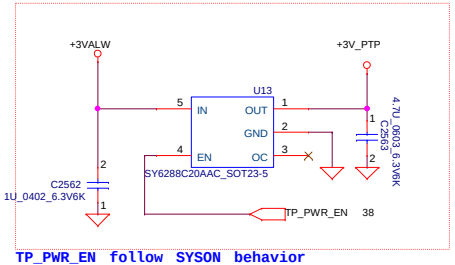
BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh



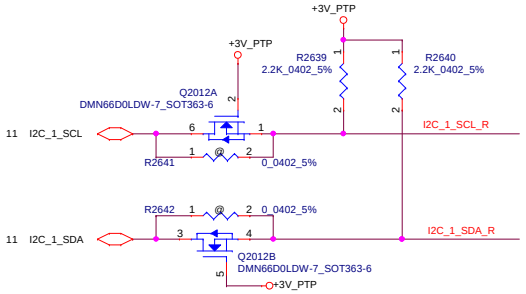
TP/B Conn.

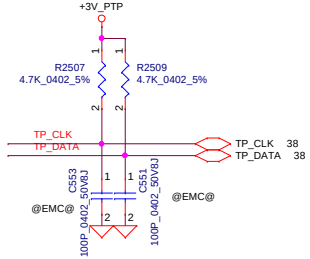


SP01001A910

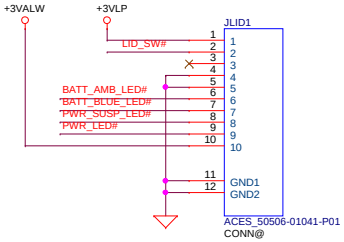


TP_PWR_EN follow SYSON behavior





Lid Switch 2 (reserve for 15")

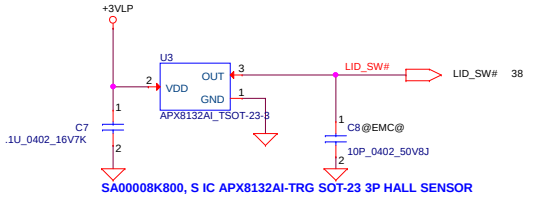


SP01001ER00

ACES_50506-01041-P01_10P-NPM

Lid Switch

(Hall Effect Switch)



SA00008K800, S IC APX8132AI-TRG SOT-23 3P HALL SENSOR

LED

Dual Amber+Blue

LTST-S115TBKF-CA (SC50000C500)

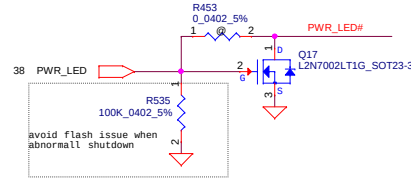
Vf @ 5 mA :

UD5: 1.7 ~ 2.3V
(3.3-1.7)/300=5.71 mA
(3.3-2.3)/300=3.57 mA
R min: 100 ohm
R max 700 ohm

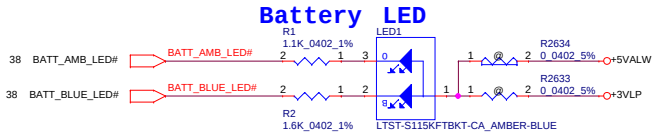
CB5: 2.65~3.05V
(3.3-2.65)/50=13.00 mA
(3.3-3.05)/100=5.0 mA
R min: 50 ohm
R max:475 ohm

100 1% :SD034100080
150 1% :SD034150080
301 1% :SD034301080
680 1% :SD034680080

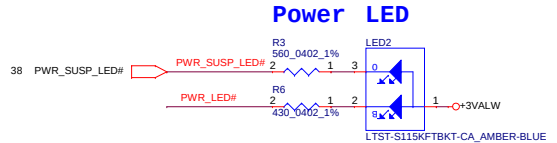
120 5% :SD028120080
560 5% :SD028560080
200 5% :SD028200080



Battery LED



Power LED



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

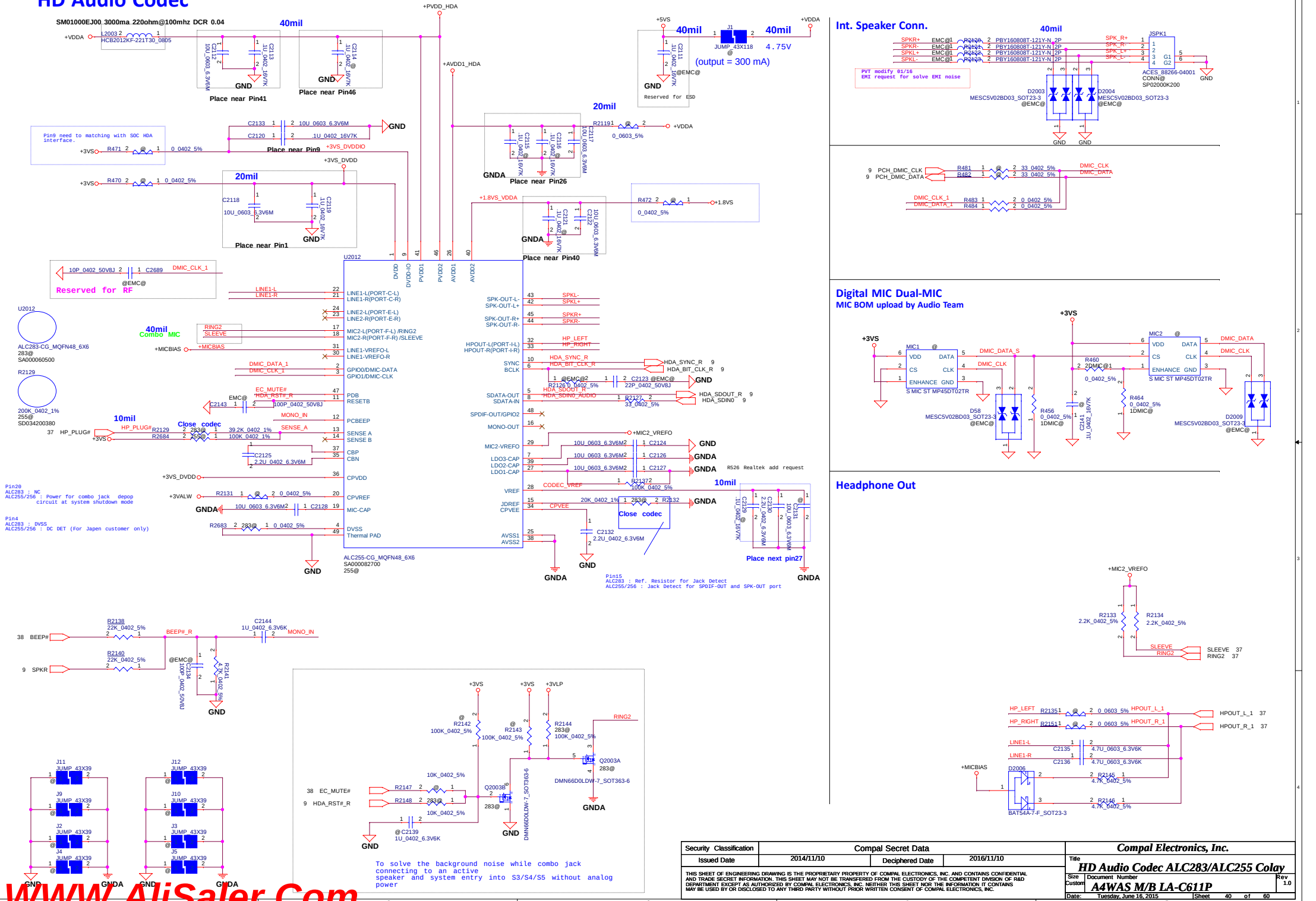
Compal Electronics, Inc.

Title: KB & TP & TPM Connector & LED

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Monday, June 22, 2015 | Sheet 39 of 60

HD Audio Codec



Int. Speaker Conn.

Digital MIC Dual-MIC

MIC BOM upload by Audio Team

Headphone Out

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

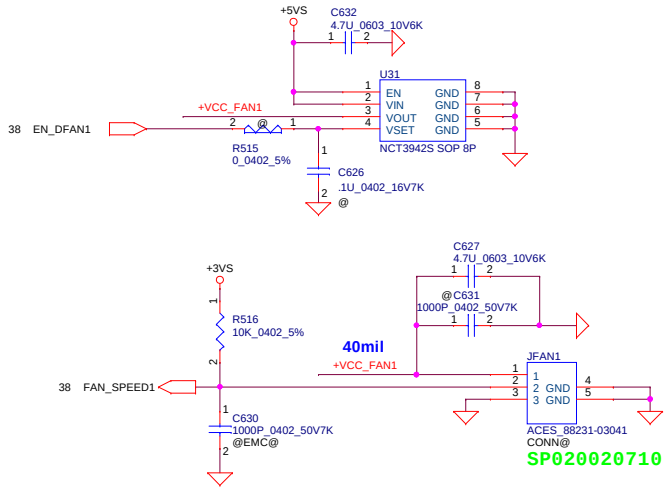
Compal Electronics, Inc.

Title: HD Audio Codec ALC283/ALC255 Colay

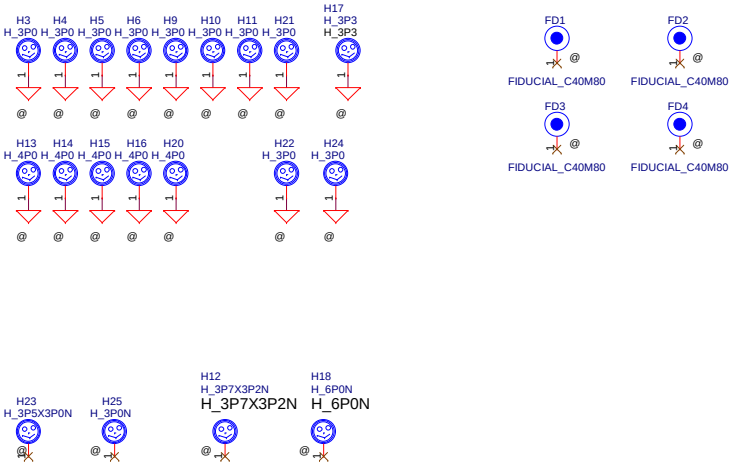
Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Tuesday, June 16, 2015 | Sheet 40 of 60

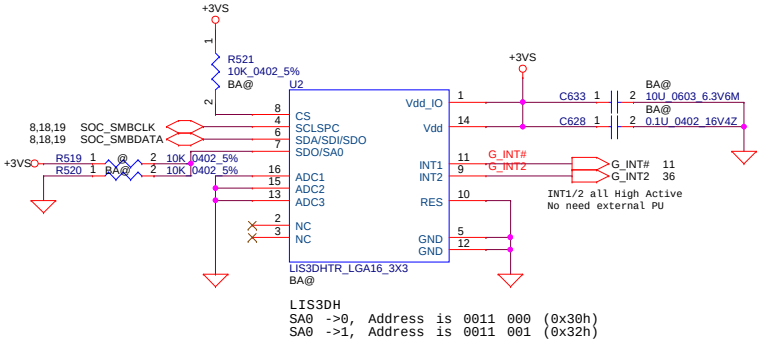
FAN1 Conn



Screw Hole

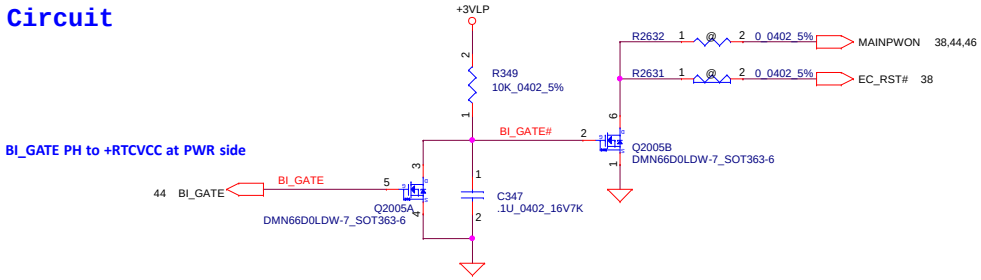


G-Sensor reserved for BA serial



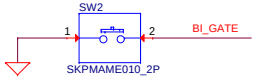
LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

Reset Circuit

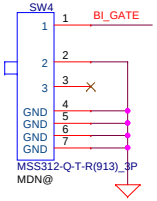


Debug SW

Reset Button



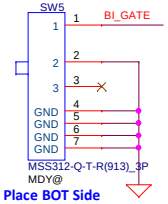
BI SW



Place TOP Side

1-2 : Battery Off
2-3 : Battery ON

BI SW



Place BOT Side

Reserved for memory door only

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: FAN & Screw Hole & G-Sensor

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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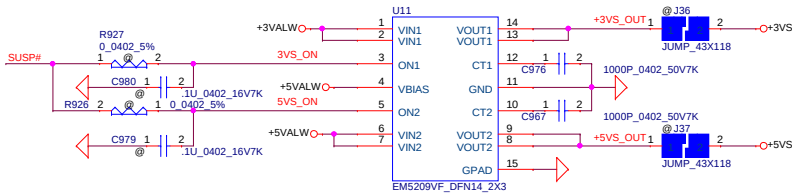
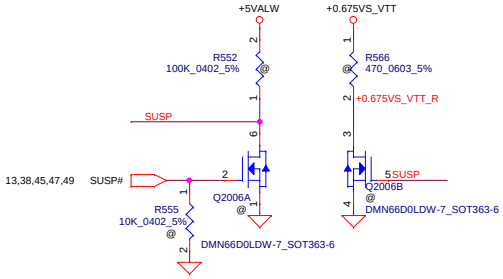
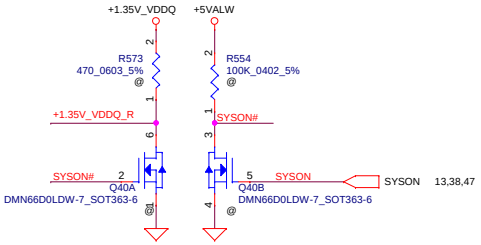
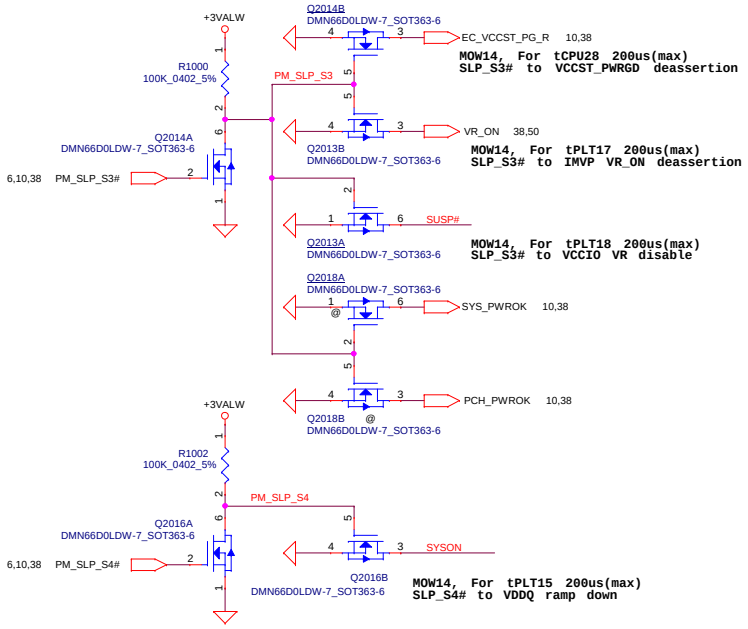
DC & VGA Interface



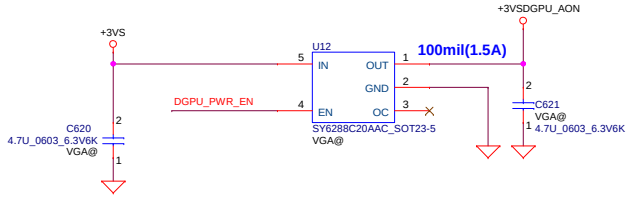


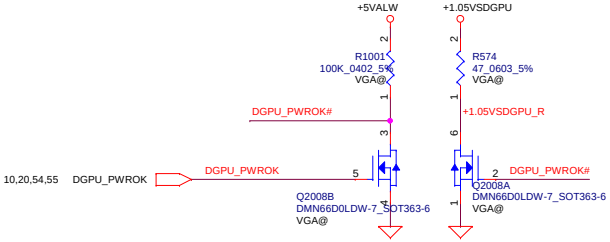


For Power ON/Off Sequence

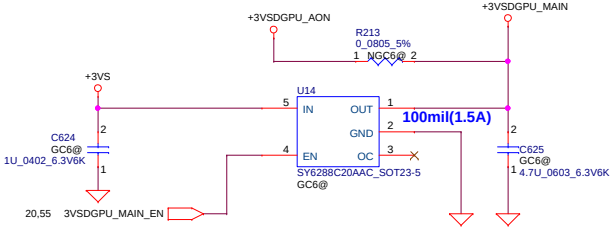


+3VS to +3VSDGPU_AON for GPU

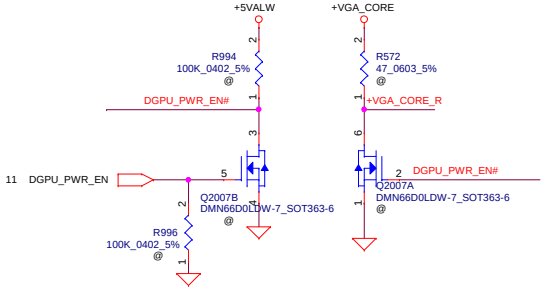


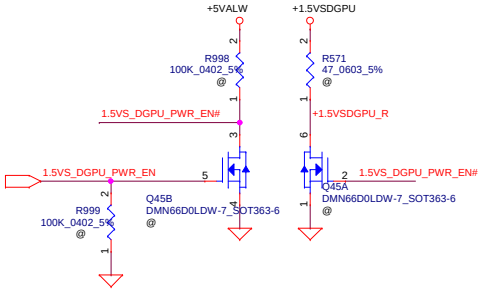


+3VS to +3VSDGPU_MAIN for GC6-2.0



3VSDGPU_MAIN_EN From GPU





Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	A4WAS M/B LA-C611P	1.0

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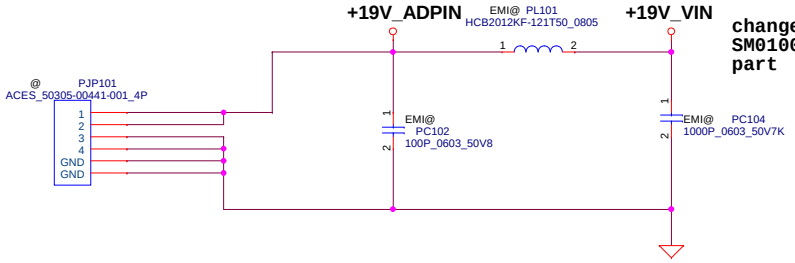
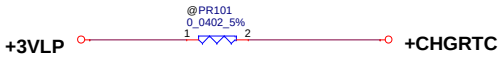
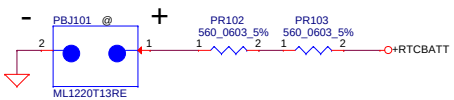


change PL101 SM01000C000 to comm part SM01000P200

2011/10/13
for EN9012 application, delete the 51_ON# circuit

2011/10/12
delete the pre-CHG circuit





Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size	Document Number	Rev
Custom	A4WAS M/B LA-C611P	1.0

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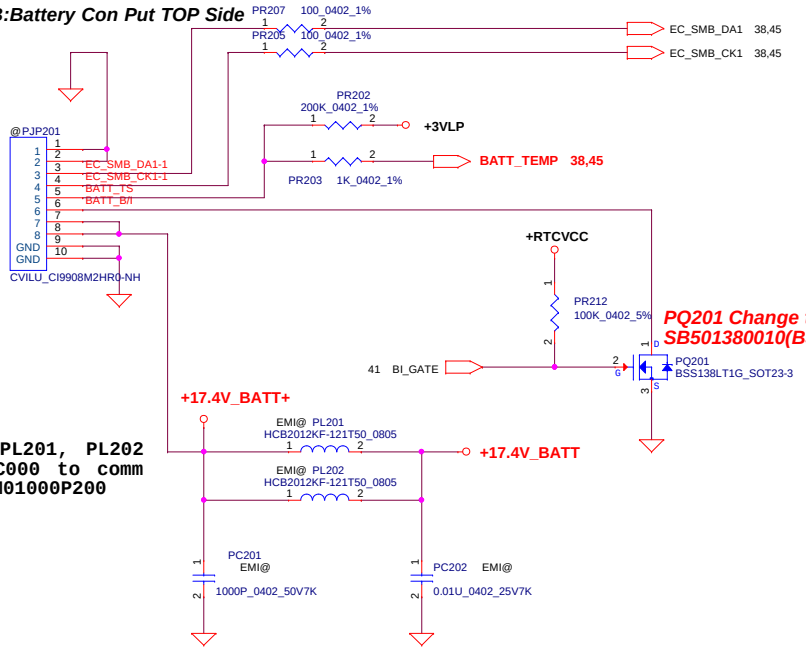
2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1

MB:Battery Con Put TOP Side

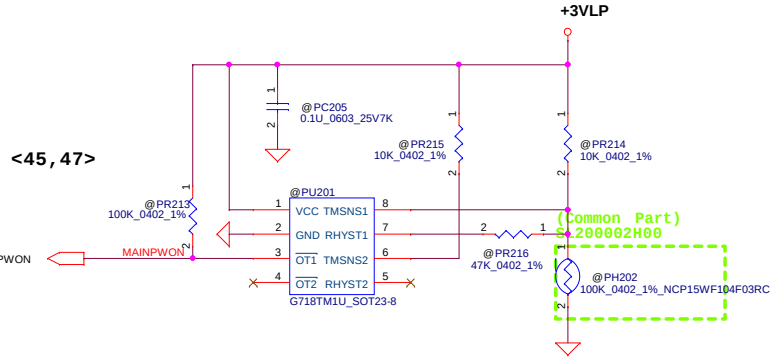
Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+



PQ201 Change to SB00000QO00, SB501380010(BSS138LT1G Del)

change PL201, PL202 SM01000C000 to comm part SM01000P200



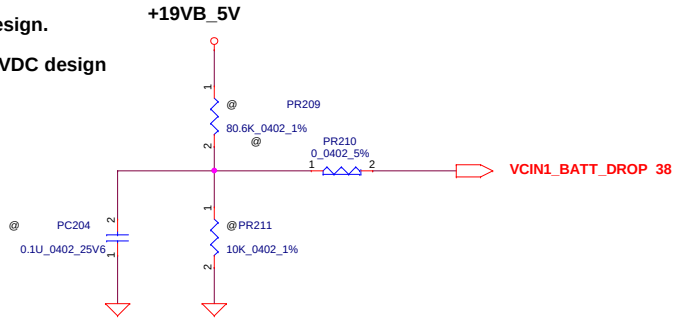
2014/09/25 update

For KB9022 sense 20mΩ	Active	Recovery
45W PR206 10K ohm SD034100280	58.5W,0.61V	45W,0.47V
65W PR206 19.1K ohm SD034191280	84.5W,0.61V	65W,0.47V

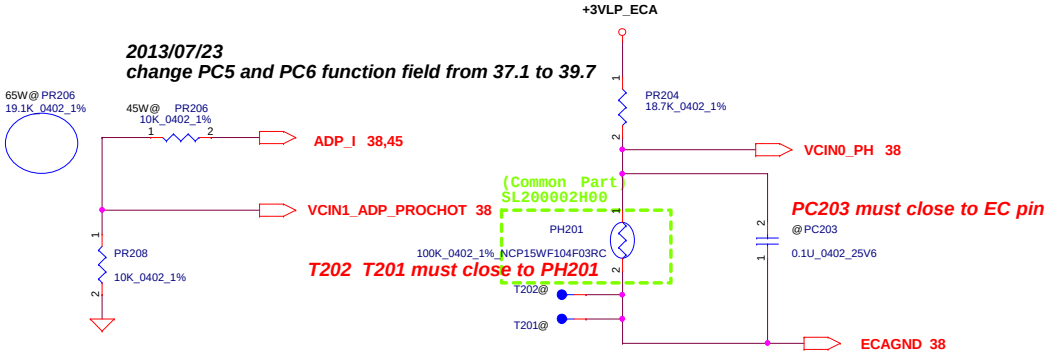
PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V



2013/07/23
change PC5 and PC6 function field from 37.1 to 39.7



PC203 must close to EC pin
T202 T201 must close to PH201

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
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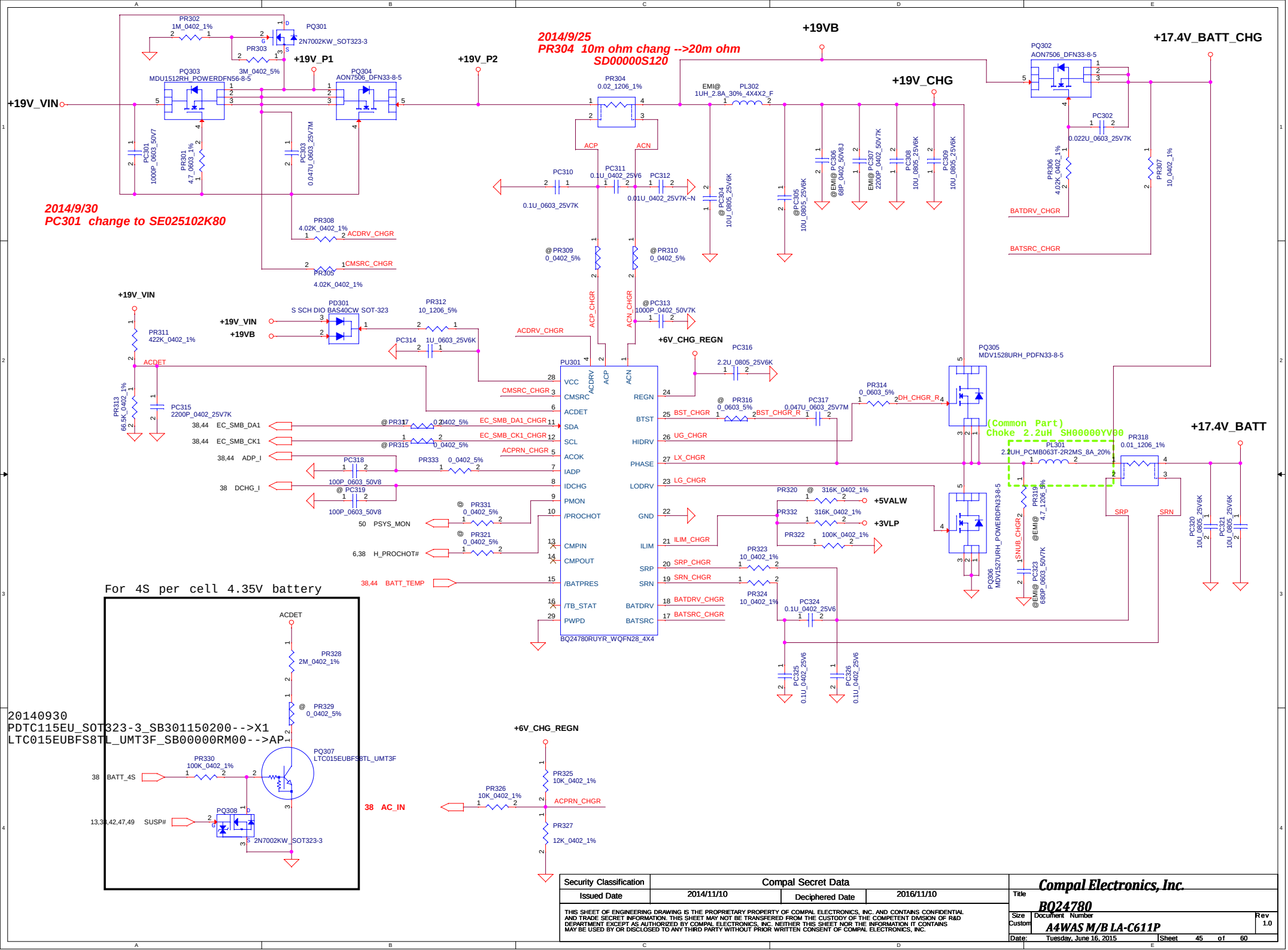
2014/9/25
PR304 10m ohm chang -->20m ohm
SD00000S120
2014/9/30
PC301 change to SE025102K80
+19V_VIN
+19V_P1
+19V_P2
+19VB
+19V_CHG
+17.4V_BATT_CHG
+17.4V_BATT
+6V_CHG_REGN
PR302 1M_0402_1%
PQ301 2N7002KW_SOT323-3
PR303 3M_0402_5%
PQ303 MDU1512RH_POWERDFN56-8-5
PQ304 AON7506_DFN33-8-5
PR304 0.02_1206_1%
PL302 1UH_2.8A_30%_4X4X2_F
PQ302 AON7506_DFN33-8-5
PC301 1000P_0603_50V7
PR301 4.7_0603_1%
PC303 0.047U_0603_25V7M
PR308 4.02K_0402_1%
ACDRV_CHGR
CMSRC_CHGR
PR305 4.02K_0402_1%
PC310 0.1U_0603_25V7K
PC311 0.1U_0402_25V6
PC312 0.01U_0402_25V7K~N
PC304 10U_0805_25V6K
PC305 10U_0805_25V6K
PC306 68P_0402_50V8J
PC307 2200P_0402_50V7K
PC308 10U_0805_25V6K
PC309 10U_0805_25V6K
PC302 0.022U_0603_25V7K
PR306 4.02K_0402_1%
PR307 10_0402_1%
BATDRV_CHGR
BATSRC_CHGR
ACP
ACN
ACP_CHGR
ACN_CHGR
@PR309 0_0402_5%
@PR310 0_0402_5%
@PC313 1000P_0402_50V7K
PD301 S SCH DIO BAS40CW SOT-323
PR312 10_1206_5%
PC314 1U_0603_25V6K
PR311 422K_0402_1%
ACDET
PR313 66.5K_0402_1%
PC315 2200P_0402_25V7K
PU301
BQ24780RUYR_WQFN28_4X4
VCC
CMSRC
ACDET
SDA
SCL
ACOK
IADP
IDCHG
PMON
/PROCHOT
CMPIN
CMPOUT
/BATPRES
/TB_STAT
PWPD
REGN
BTST
HIDRV
PHASE
LODRV
GND
ILIM
SRP
SRN
BATDRV
BATSRC
PC316 2.2U_0805_25V6K
PR314 0_0603_5%
DH_CHGR_R
PR316 0_0603_5%
BST_CHGR
BST_CHGR_R
PC317 0.047U_0603_25V7M
UG_CHGR
LX_CHGR
LG_CHGR
ILIM_CHGR
SRP_CHGR
SRN_CHGR
BATDRV_CHGR
BATSRC_CHGR
PQ305 MDV1528URH_PDFN33-8-5
PQ306 MDV1527URH_POWERDFN33-8-5
(Common Part)
Choke 2.2uH SH00000YV00
PL301 2.2UH_PCMB063T-2R2MS_8A_20%
PR318 0.01_1206_1%
PR319 4.7_1206_5%
SNUB_CHGR
PC320 10U_0805_25V6K
PC321 10U_0805_25V6K
PR320 316K_0402_1%
PR332 316K_0402_1%
PR322 100K_0402_1%
+5VALW
+3VLP
PR323 10_0402_1%
PR324 10_0402_1%
PC324 0.1U_0402_25V6
PC325 0.1U_0402_25V6
PC326 0.1U_0402_25V6
PC318 100P_0603_50V8
PR333 0_0402_5%
PC319 100P_0603_50V8
PR331 0_0402_5%
PR321 0_0402_5%
PR317 0_0402_5%
PR315 0_0402_5%
EC_SMB_DA1_CHGR
EC_SMB_CK1_CHGR
ACPRN_CHGR
38,44 EC_SMB_DA1
38,44 EC_SMB_CK1
38,44 ADP_I
38 DCHG_I
50 PSYS_MON
6,38 H_PROCHOT#
38,44 BATT_TEMP
SRP
SRN
For 4S per cell 4.35V battery
20140930
PDTC115EU_SOT323-3_SB301150200-->X1
LTC015EUBFS8TL_UMT3F_SB00000RM00-->AP
PR328 2M_0402_1%
PR329 0_0402_5%
PR330 100K_0402_1%
PQ307 LTC015EUBFS8TL_UMT3F
PQ308 2N7002KW_SOT323-3
38 BATT_4S
13,30,42,47,49 SUSP#
38 AC_IN
PR325 10K_0402_1%
PR326 10K_0402_1%
PR327 12K_0402_1%
Security Classification
Compal Secret Data
Issued Date
2014/11/10
Deciphered Date
2016/11/10
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BQ24780
Size
Custom
Document Number
A4WAS M/B LA-C611P
Rev
1.0
Date:
Tuesday, June 16, 2015
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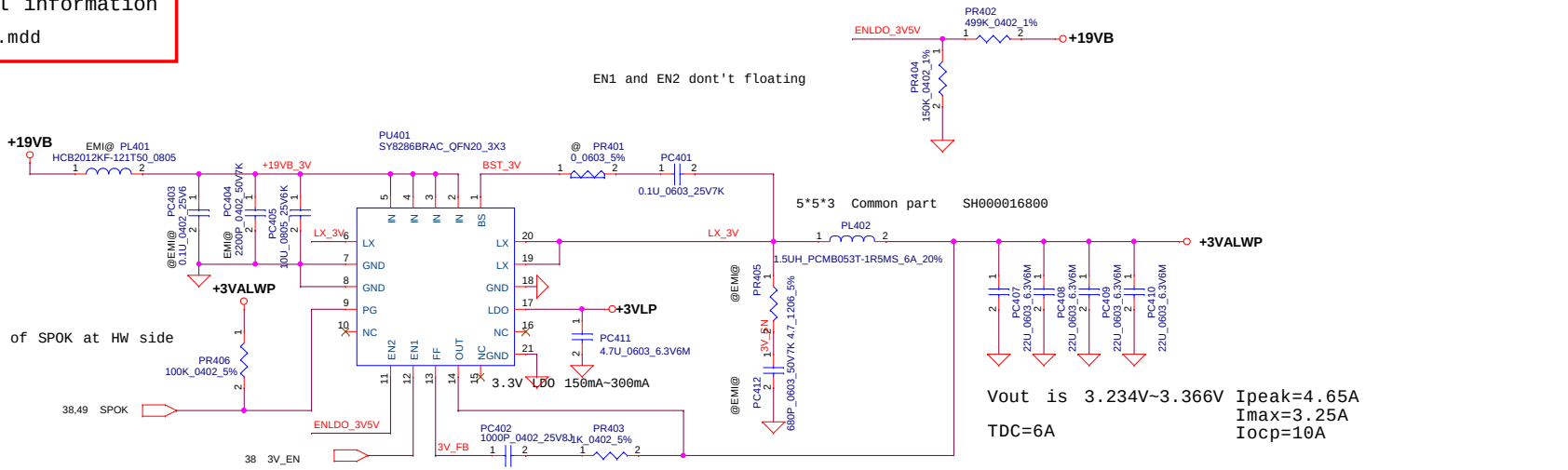
Module model information

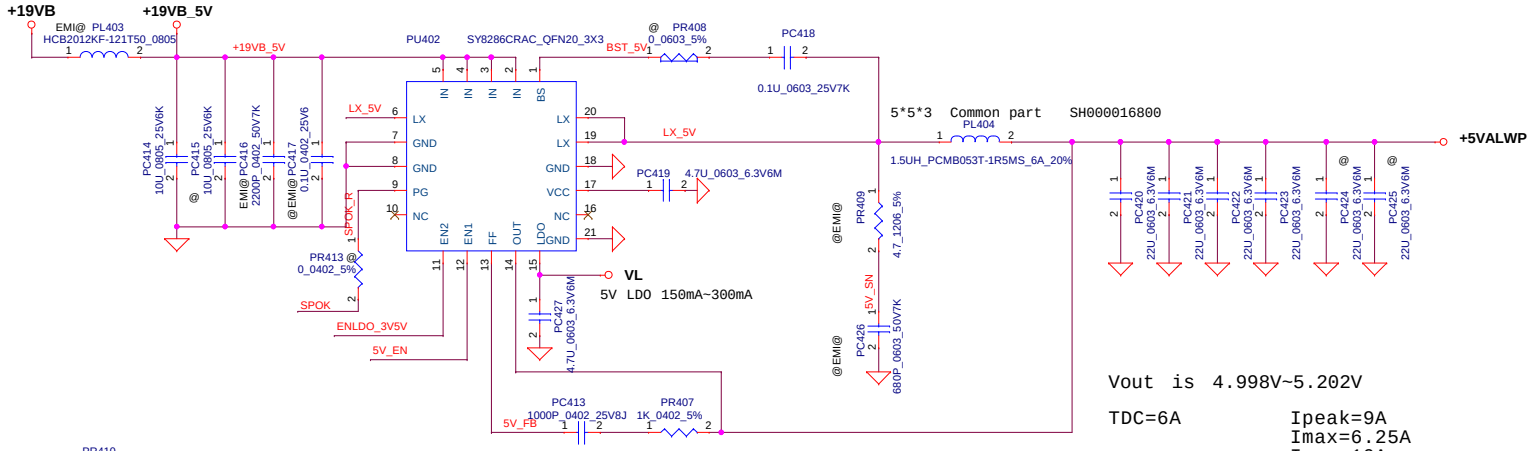
TPS51225C_V1.mdd

EN1 and EN2 dont't floating



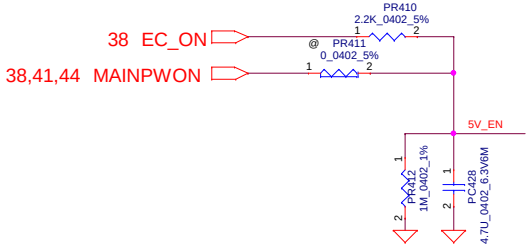
Check pull up resistor of SPOK at HW side

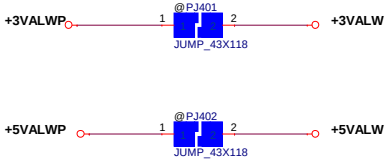
Vout is 3.234V~3.366V Ipeak=4.65A
Imax=3.25A
TDC=6A Iocp=10A



Vout is 4.998V~5.202V

TDC=6A Ipeak=9A
Imax=6.25A
Iocp=10A





Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

+19VB_CPU

change PL501 SM01000C000 to comm part SM01000P200

EMI@ PL501 HCB2012KF-121T50_0805

+19VB_1.35VP

@EMI@ PC502 0.1U_0402_25V6
EMI@ PC503 2200P_0402_50V7K
PC504 10U_0805_25V6K
PC505 10U_0805_25V6K

Choke 1.5uH SH000016700
Common Part 7*7*3

PL502 1.5UH_PCMC063T-1R5MN_9A_20%

+1.35VP

PC510 330U_2.5V_M

Update Pc510 change to Common Part SF000006S00 20141227

@EMI@ PR504 4.7_1206_5%
@EMI@ PC518 680P_0402_50V7K

PQ503 MDV1528URH_PDFN33-8-5
PQ502 SI7716ADN-T1-GE3_POWERPAK8-5

PC506 0.1U_0603_25V7K

PR502 2.2_0603_5%
BST_1.35VP_R
BST_1.35VP
UG_1.35VP
LX_1.35VP
LG_1.35VP

PU501 RT8207MZQW_WQFN20_3X3

PHASE UGATE BOOT VLDOIN VTT
LGATE PGND CS VDDP VDD PGOOD TON SS S3 FB
PAD VTTGND VTTSNS GND VTTREF VDDQ

+1.35VP
+0.675VSP

PC507 10U_0603_6.3V6M
PC508 10U_0603_6.3V6M

PR503 13.7K_0402_1%
CS_1.35VP
PC509 1U_0402_10V6K
VDD_1.35VP

PR505 5.1_0603_5%
+5VALW

PC517 1U_0402_10V6K
PR511 2.2_0402_1%

VTTREF_1.35VP
PC516 0.033U_0402_16V7K

change PQ502 form 7506 to 7716, 20150108

453Kohm-->455KHz

PR507 887K_0402_1%
+19VB_1.35VP

TON_1.35VP
EN_1.35VP
EN_0.675VSP
FB_1.35VP

PR506 8.2K_0402_1%
PR508 10K_0402_1%

Vout=0.75V* (1+Rup/Rdown)
=0.75*(1+(8.06/10))
=1.354V 0.2%
Vout=0.75V* (1+Rup/Rdown)
=0.75*(1+(8.2/10))
=1.365V 1.1%

13,38,42 SYSON
@ PR501 0_0402_5%
@PC501 0.1U_0402_10V7K

13,38,42,45,49 SUSP#
@PR509 0_0402_5%

7 SM_PG_CTRL
@ PR510 0_0402_5%

@PC519 0.1U_0402_10V7K

@PJ501 JUMP_43X118
+1.35VP
+1.35V_VDDQ

@PJ502 JUMP_43X39
+0.675VSP
+0.675VS_VTT

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
VFB=0.75V, Vout=1.3545V
MOSFET footprint: SIS412DN

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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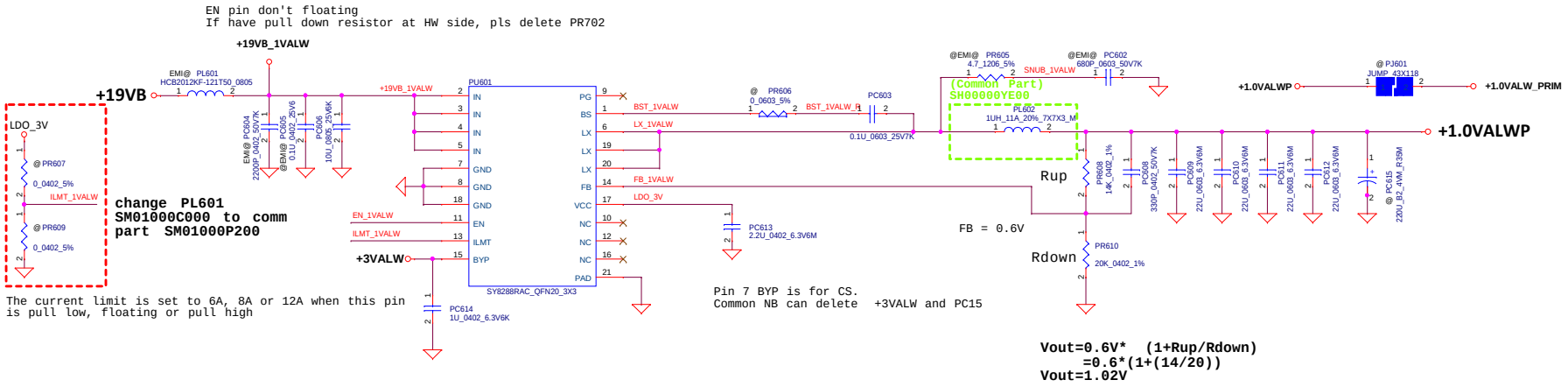
Module model information

SYX196D_V3.mdd



Function Field :
VCCEDPIO : IC-35.21 , others - 35.22
VCCEDRAM : IC-35.25 , others - 35.26

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: VCCP

Size	Document Number	Rev
C	A4WAS M/B LA-C611P	1.0

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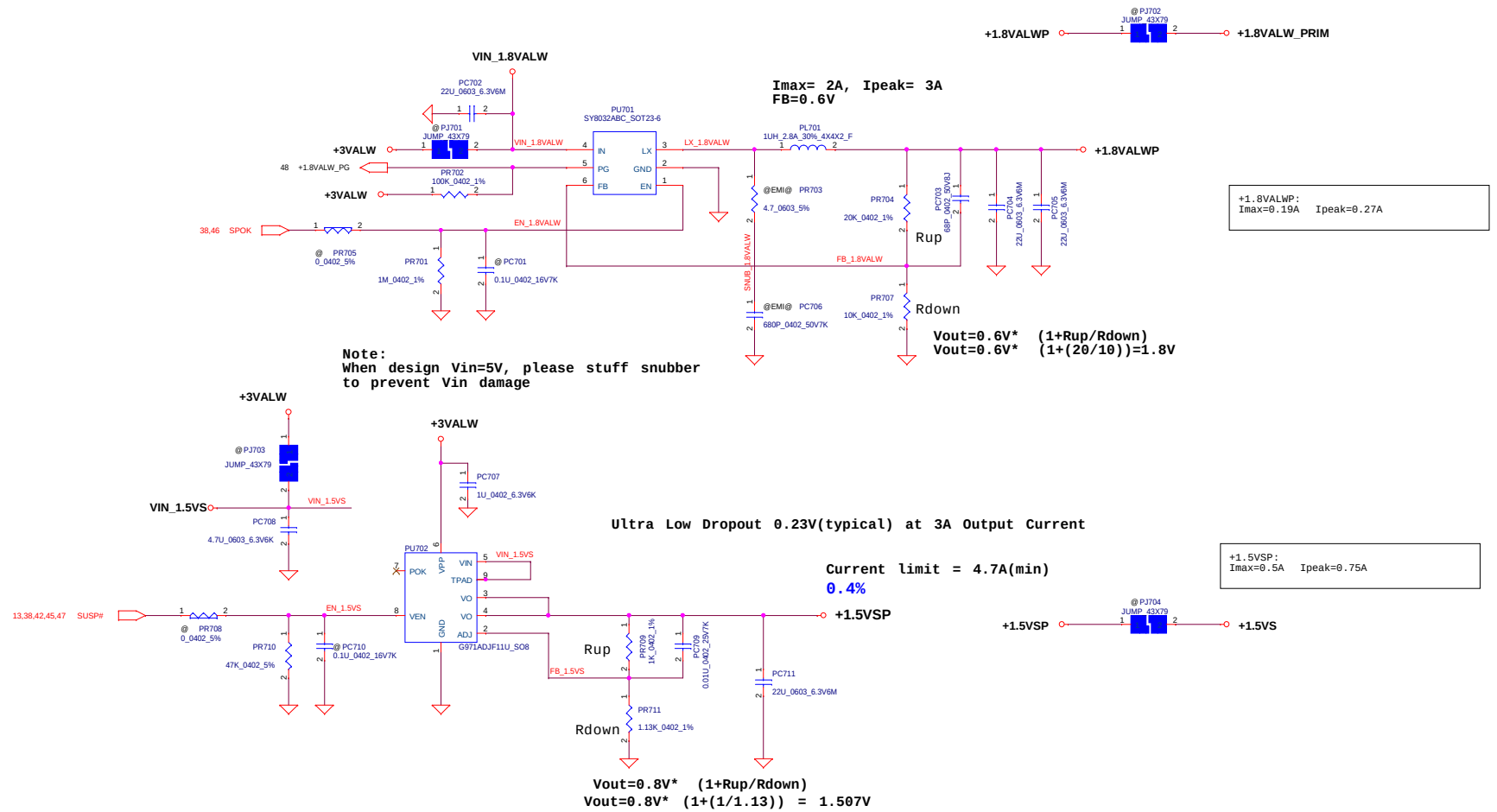
Module model information

SY8032_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C	A4WAS M/B LA-C611P	1.0

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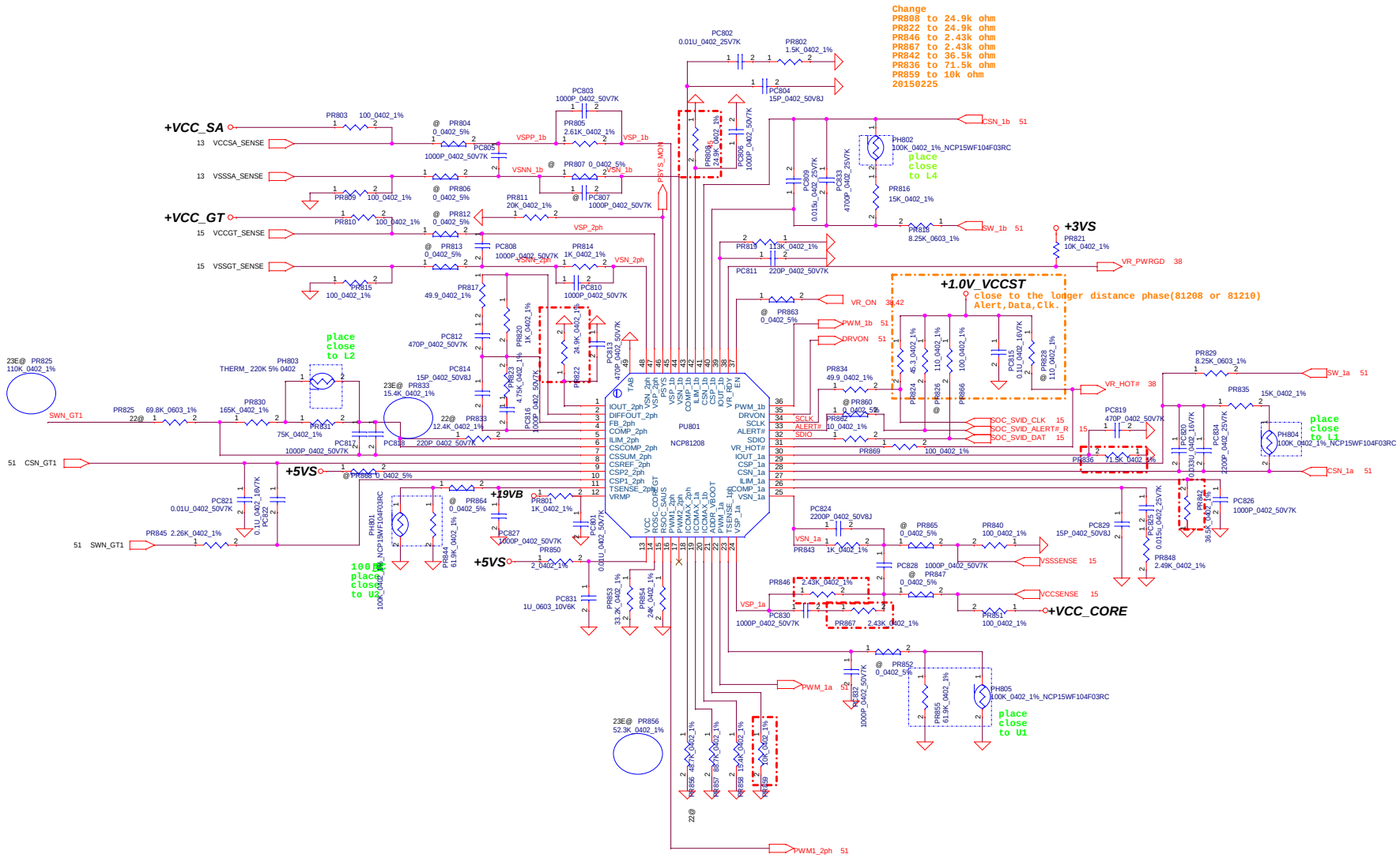

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: IMVP8, NCP81206

Size	Document Number	Rev
C	A4WAS M/B LA-C611P	1.0

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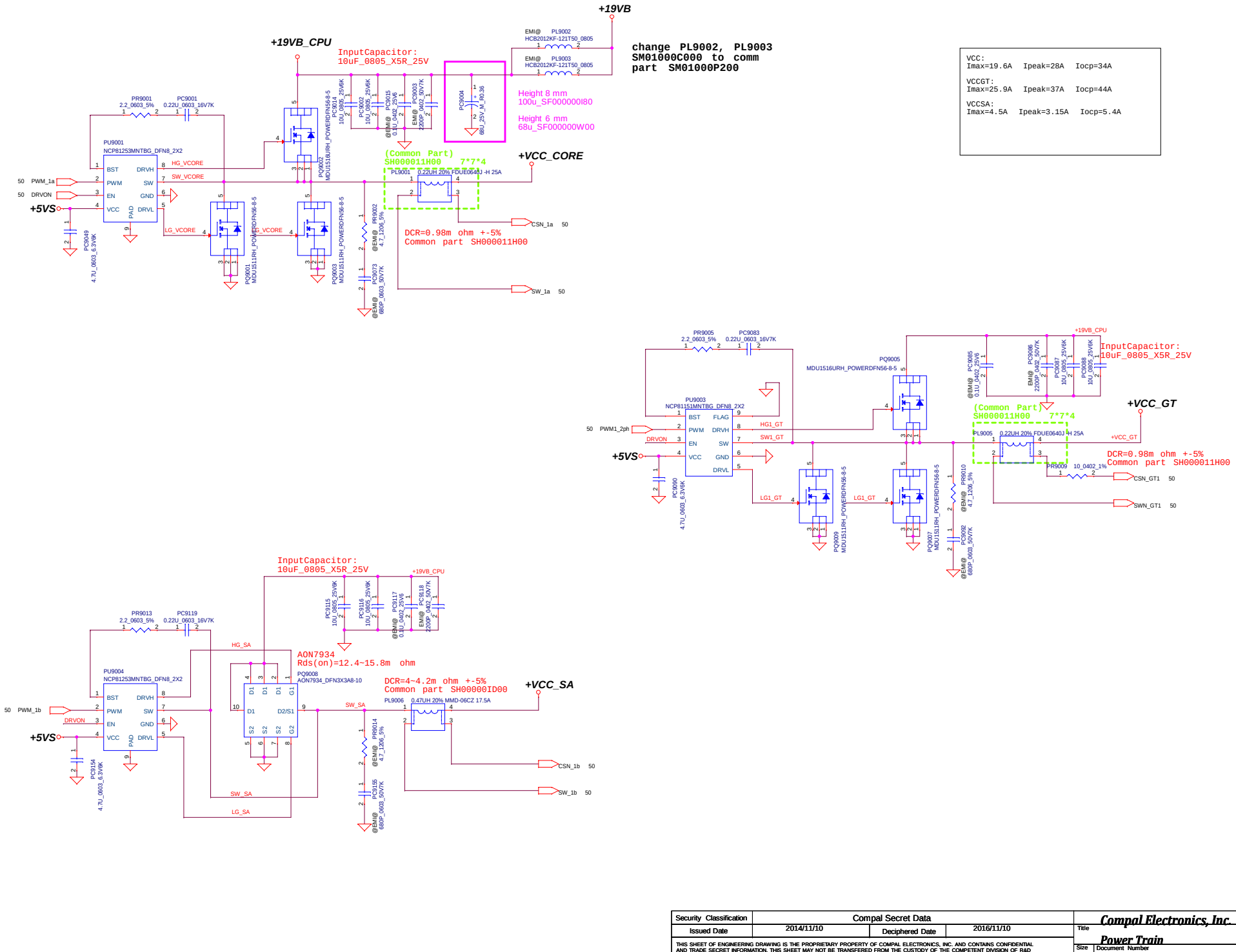

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	A4WAS M/B LA-C611P	1.0

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543016_543016_SKL_PDG_UY_1_0_pub
Total VCORE Output Capacitor:
2014/09/23
22uF_0603_33PCS
1uF_30201_35PCS
UNPOP
0603_3PCS 0201_3PCS
330uF_R9_2PCS

20140703
23E: D2*2 22uF_0603*29 1uF_0201*12
22: D2*1 22uF_0603*26 1uF_0201*12

20140923
D2*1 22uF_0603*38 1uF_0201*14
unpop: 22uF_0603*10 1uF_0201*6

20150504
D2*1 22uF_0603*32 1uF_0201*14
unpop: 22uF_0603*16 1uF_0201*6

20140703
22uF_0603*12 1uF_0201*7

+VCC_CORE

+VCC_GT

+VCC_SA

(Common Part)
SGA00009S00

(Common Part)
SGA00009S00

1u_0201 SE00000U200
1u_020 1 SE00000UC00.

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	A4WAS M/B LA-C611P	1.0

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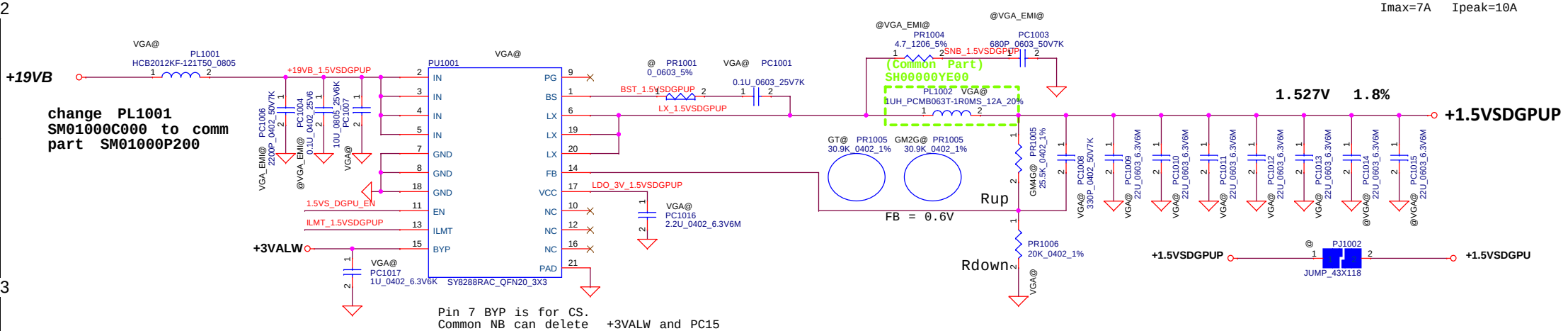

VGA	Brand Name	VRAM Size	Voltage
N16S-GT	NV940	2GB	1.5V(or 1.35V)
		4GB	1.5V(or 1.35V)
N16V-GM	NV920	2GB	1.5V(or 1.35V)
		4GB	Only 1.35V

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1.365V

Vout=0.6V* (1+(25.5/20))=1.356

Vout=0.6V* (1+(30.9/20))=1.527

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: 1.5VSDGPUP

Size: A3 | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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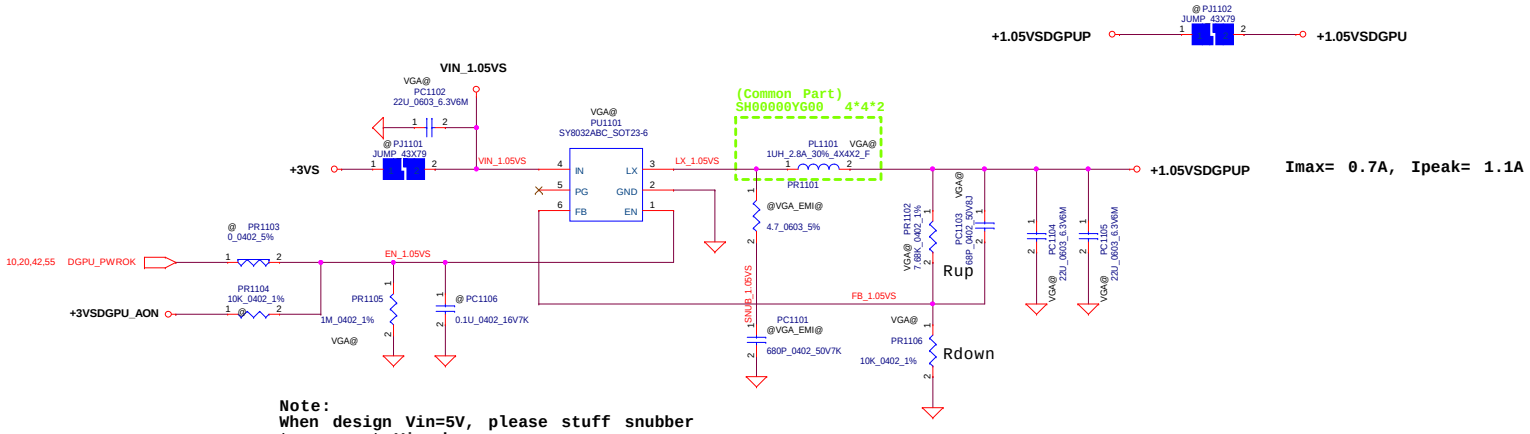
Module model information

SY8032_V2.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
=>0.6V*(1+(7.68/10)=1.061 (1.01%)
=>0.6V*(1+(7.87/10)=1.072 (2.1%)

Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C	A4WAS M/B LA-C611P	1.0

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PSI :
1 phase with DEM 0V to 0.8V
1 phase with CCM 1.2V to 1.8V
2 phase with CCM 2.4V to 5.5V

EN High Threshold = 1.6V

unmount PRV5 for 2 phase select

change PL1201 SM01000C000 to comm part SM01000P200

N16S-GT EDP continuous:26A peak: 51A
L side Rds(on): 3mohm(Typ), 3.8mohm(Max)
Idsm: 11A@Ta=25C, 14A@Ta=70C

CHOKE:0.36uH, DCR 1.4m ohm, L/2 over 36A

FSW = 304Khz
(R=499K-->304khz) (R=620K-->245khz)
Imax=35A
Ipeak-51A
OCP = 61A
OVP=Vout*(145%~155%)

Remove GPU OTP circuit for HW request

PWM-VID Spec and component Values

PWM-VID Spec		Config B	Config C	Config D
Vmin		0.6V	0.65V	0.9V
Vmax		1.2V	1.15V	1.15V
Vboot		0.9V	0.9V	1.028V
Voltage step		6.25mV	25mV	12.5mV
N of Voltage level		96	20	20
Rrefadj	PR	20K	39K	27K
Rref1	PR	20K	30K	7.5K
Rboot	PR	2K	3K	0
Rref2=PR1209 +PR1212	PR	18K	24K	6.2K
	PR	0	3K	1.74K
C	PC	2.7nf	1.8nf	5.6nf

N16S-GT
N16V-GM

+VGA_CORE Under GPU Core GB2-64 package

+VGA_CORE Near GPU Core

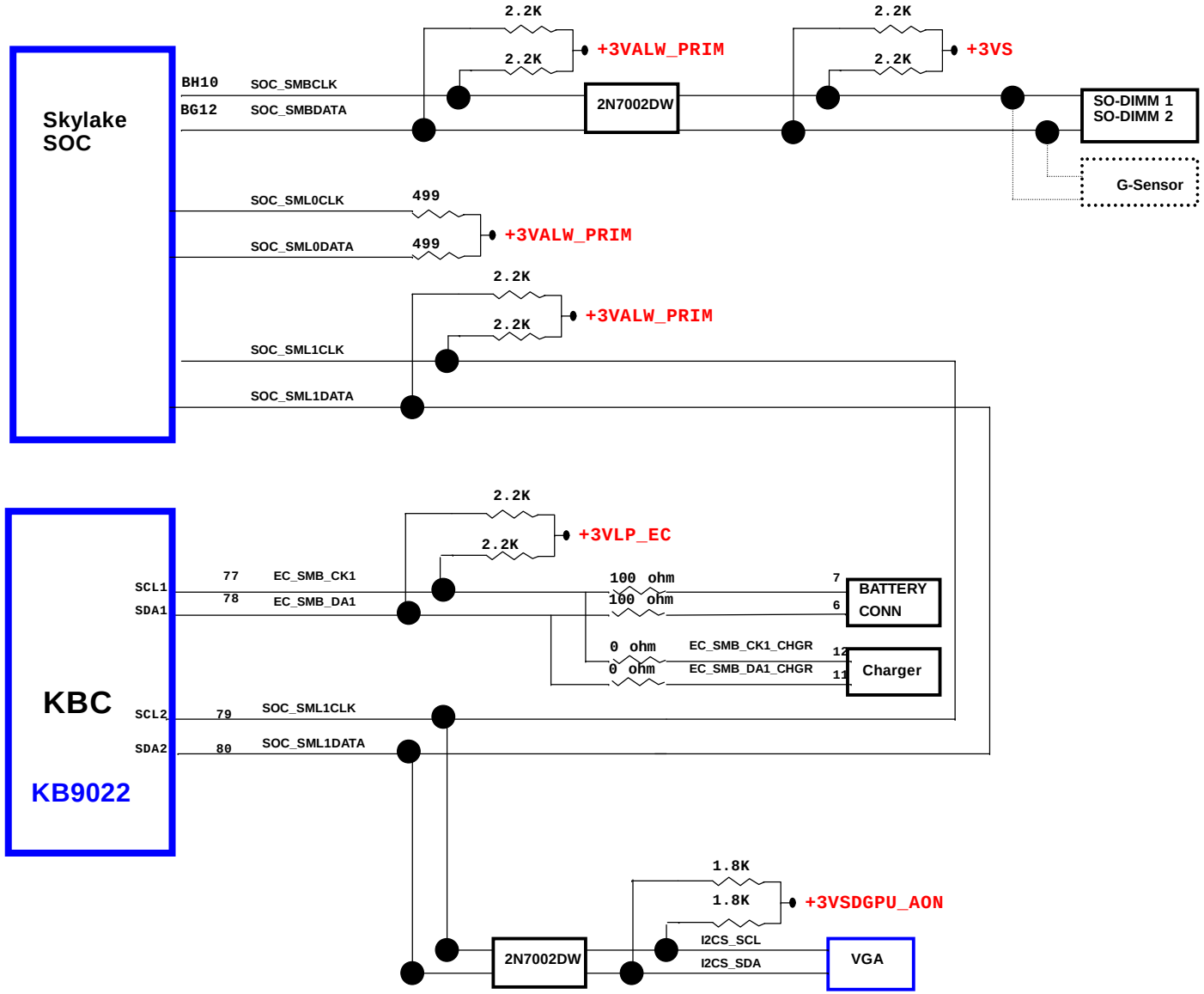
Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: NVIDIA VGA CORE

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

Date: Monday, June 22, 2015 | Sheet 55 of 60



Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: SMBUS Routing Table

Size: Custom | Document Number: A4WAS M/B LA-C611P | Rev: 1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	Design Change.	change to the latest 2015 for MOSFET application.	01	45	change PQ305 to MDV1528 & PQ306 MDV1527		EVT
02	Design Change.	change to the latest 2015 for MOSFET application.	01	47	change PQ503 to MDV1528		EVT
03	Design Change.	change to the latest 2015 for MOSFET application.	01	51	change PQ9002 & PQ9005 to MDU1516		EVT
04	Design Change.	change to the latest 2015 for MOSFET application.	01	51	change PQ9001, PQ9003, PQ9007 & PQ9009 to MDV1511		EVT
05	Design Change.	change to the latest 2015 for MOSFET application.	01	57	change PQ1201 & PQ1203 to MDU1516		EVT
06	Design Change.	change to the latest 2015 for MOSFET application.	01	57	change PQ1202 & PQ1204 to MDU1511		EVT
07	power off pulse issue when S0 -> S5.	+0.675VS have a pulse when S0->S5 as attached.	01	47	change Pu501 8207P to 8207M		EVT
08	power off pulse issue when S0 -> S5.	8207M output cap is use 330uF poscap	01	47	Delete PC510~PC515 22u*6		EVT
09	power off pulse issue when S0 -> S5.	8207M output cap is use 330uF poscap	01	47	Add PC510 330u*1		EVT
10	power off pulse issue when S0 -> S5.	8207M frequency is different with 8207P	02	47	change PR507 to 887k ohm		DVT
11	Design Change.	Tune +1.5VSDGPUP enable time	02	53	change PR1002 to 40.2k ohm		DVT
12	Stop use Anpec LDO	Anpec LDO is EOL	02	49	change Pu702 to G971		DVT
13	DFB request	pin is too small, avoid open solder	02	44	Change PJP201 SP021210250 (ACES_50458-00801-001_8P-T) to SP020017H00 (CVILU_CI9908M2HR0-NH_8P)		DVT
14	Tune CPU transient	Tune CPU transient	02	50	Change PR808 to 24.9k ohm PR822 to 24.9k ohm PR846 to 2.4k ohm PR867 to 2.4k ohm PR842 to 36.5k ohm PR836 to 69.8k ohm PR859 to 10k ohm		DVT
15	Design Change.		02	45	Change PC315 0.1u to 2200p		DVT
16	Design Change.	change 1V output from 1.011V to 1.02V	02	48	Change PR608 13.7k to 14k ohm		DVT
17	Tune CPU transient	Tune CPU transient	02	50	Change PR846 to 2.43k ohm PR867 to 2.43k ohm PR836 to 71.5k ohm		DVT
18	Design Change	Change to common part	02	53	Change PL9002, PL9003, PL1001 & PL1201 to common part (HCB2012KF-121T50_0805)		DVT
19	thermal request	change PH1 from 92degree to 89degree	02	44	Change PR204 from 16.9k ohm to 18.7k ohm		

Compal Electronics, Inc.
Title: PIR
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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	11	CPU	1/9	NA	Reserved RC189(0 ohm) for DGPU_AC_DETECT	DVT	0.2
2	38	EC	1/9	Reserved protect circuit when adaptor 107% happen, requrie from Acer	Change net from VCOUT1_PROCHOT# to VCOUT1_PROCHOT Change U4901.117 from SEN_DET# to SW_PROCHOT# Reserved Q2010A/B for SW_PROCHOT# and DGPU_AC_DETECT Add R4960 for SW_PROCHOT# and VCOUT1_PROCHOT Rename R4938.2 to SW_PROCHOT#	DVT	0.2
3	38	EC	1/9	Remove unuse part	Delete R4905, R619, R4958	DVT	0.2
4	10	CPU	1/12	SYS_RESET# Pull-up to ALWAYS power rails	Change RPC11.6 to +3VALW_PRIM	DVT	0.2
5	11	CPU	1/12	Reserved PD for G_INT#	Reserved RC117 for G_INT#	DVT	0.2
6	11	CPU	1/12	NA	Move RC212 to Page06 and add note for EC_SCI#	DVT	0.2
7	11	CPU	1/12	Separate RPC18 for easy PU	Change RPC18 to RC126, RC127 (1K) and RC128, RC129 (2.2K)	DVT	0.2
8	17	CPU	1/12	Reserved for Cannonlake-U (2014MOW52)	Connect UC1.U11/U12 to +1.8VALW_PRIM and reserved CC79 for UC1.U11/U12	DVT	0.2
9	18, 19	Memory	1/12	Change CIS Symbol and Footprint	Change CD16,CD46 PN to SGA00009S00	DVT	0.2
10	29, 37	USB	1/12	Change CIS Symbol and Footprint	Change L24,L25,L26,L28,L29,L30, L27 CIS Symbol to SM070003Y00	DVT	0.2
11	33	LAN	1/12	Reserved path for +3V_LAN	Reserved R214 0_0850 for +3V_LAN	DVT	0.2
12	35	WLAN	1/12	Disconnect SUSCK to M.2 connector to avoid leakage current	R426 change to 0_0402 @	DVT	0.2
13	37, 38	USB	1/12	Control USB Charger behavior when disabel USB charger funct i on	Change R854.1 from SUSP# to USB_CB and U4901.70 from OPMODE to USB_CB	DVT	0.2
14	38	EC	1/12	Board ID change to DVT	Change R4903 from 0_0402_5% to 12K_0402_5%	DVT	0.2
15	38	EC	1/12	Remove unuse part	Delete R4957, R4959	DVT	0.2
16	39	LED	1/12	LED light adjust	Change R3 to 560 ohm and change R6 to 430 ohm Change R2633.2 to +3VLP	DVT	0.2
17	39	LID	1/12	Change Hall Sensor IC	Change U3 to SA00008K800 (ANPEC)	DVT	0.2
18	39 11	PTP	1/12	Add level shift for PTP I2C interface	Add Q2012A/B, R2641, R2642, R2639, R2640 Change RC128,RC129 PU to +3VALW_PGPPC	DVT	0.2
19	41	Others	1/12	Follow DFX requriement	Change H17 from 3P2 to 3P3	DVT	0.2
20	42	Sequence	1/12	For power off sequence	Add R1000, R1002, Q2013, Q2014, Q2016 for tCPU17, tCPU18, tCPU28, tPLT15	DVT	0.2
21	06	Debug	1/15	Reserved for power on select	Reserved RC53, RC54 for JAPS1.11	DVT	0.2
22	36	HDD	1/15	Pin def i nit on modf y	JHDD2.10 connect to GND	DVT	0.2
23	39	Others	1/15	Pin def i nit on modf y	JLID1.2 change to LID_SW#, JLID1.3 NC	DVT	0.2
24	08	SPI	1/20	Remove/Un-Pop unuse part	Del RC203 and change un-pop RPC6	DVT	0.2
25	09, 40	DMIC	1/20	Reserved DMIC path from SOC	Reserved R481, R482 for PCH_DMIC_CLK/DATA from UC1.H5/D7 Add R483, R484 0_0402 for Audio DMIC	DVT	0.2
26	22	NV	1/20	Update HYNIX C die straps table	Update HYNIX C die straps table	DVT	0.2
27	30	Others	1/20	Remove unuse part	Del R377, R378, R376	DVT	0.2
28	35	WLAN	1/20	Separate M.2 pin32 and 46 for Intel WLAN 3165	JNGFF1.32 change to NC (for Intel 3165)	DVT	0.2
29	38	Sequence	1/20	For power down sequence	Add D27 for EC_VCCST_PG_R	DVT	0.2
30	39	LED	1/20	Update CIS Symbol and Footprint	Update LED1, LED2 CIS Symbol	DVT	0.2
31	40	Audio	1/20	Update BOM Structure	Change R2135, R2151 to EMC@	DVT	0.2
32	40	Audio	1/20	Adjust MONO_IN input voltage	Change R2140 to 27K and R2138 to 27K(@)	DVT	0.2
33	41	Others	1/20	Change reset signal	Mount R2631 and un-mount R2632	DVT	0.2
34		Others	1/20	Change 0 ohm to R-Short	0_0603 to R-Short: R2075, R81, RC176, RC209 0_0402 to R-Short: R2131, RC172, R472, R927, R2552, R4953, R4956, RC178, RC197, R427,R428	DVT	0.2
35	20	NV	1/28	Remove unuse part	Del D2002, R2055	DVT	0.2
36	30	HDMI	1/28	Remove unuse part	DEL ZZZ1 (HDMI ROYALTY)	DVT	0.2
37	30	HDMI	1/28	Change U52 main source (HDMI power switch)	U52 change to SA00004ZA00	DVT	0.2
38	38	EC	1/28	Un-use part change to @	R4943 change to @	DVT	0.2
40	06	CMC	2/4	Change XDP to CMC	Change JXDP1 CIS symbol to CMC CIS Symbol(JPCMC1) Del RPC3, RC22, RC25, RC20, RC14, CC120, CC121, RPC4 Rerout i ng RPC2, RPC4, RPC15, RC23, RC151 Add RC17, RC55, RC56 Change RC37 to @ Change XDP@ to CMC@	DVT	0.2
41	08	LPC	2/4	Change 0 ohm to R-Short	Change RPC8 to RC144~ RC147 0 ohm R-short	DVT	0.2

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
42	10		2/4	Remove unuse part	Del RC108	DVT	0.2
43	10	SOC	2/4	Add T164/T165 for CLK_CPU_ITP/CLK_CPU_ITP#	Add T164/T165 for CLK_CPU_ITP/CLK_CPU_ITP#	DVT	0.2
44	10	SOC	2/4	Change Material of AND gate	Change UC3 to SA00000OH00	DVT	0.2
45	12	SOC	2/4	Follow PCH EDS1.2 add PD resistor when un-use USB	Add RC130, RC131 for USB2_ID and USB2_VBUSSENSE	DVT	0.2
46	10	SOC	2/5	Reserved PD resistor (2014MOW48)	Reserved RC136 for Cannonlake-U	DVT	0.2
47	13	SOC	2/5	Reserved path for VCCIO	Reserved U4902, C977	DVT	0.2
48	06	SOC	2/9	Reserved path for TP_INT#	Reserved RC137	DVT	0.2
49	17	SOC	2/9	Reserved power source for U11/U12	Add RC57 for UC1.U11/U12	DVT	0.2
50	19	DIMM	2/9	Remove un-use part	Del CD46	DVT	0.2
51	29,37	USB Chock	2/9	Swap net because update CIS Symbol	SWAP net of L24,L25,L26,L28,L29,L30,L27	DVT	0.2
52	10	Crystal	2/11	Update 32.768KHz Crystal to 9pF	Change YC2 PN to SJ10000L000	DVT	0.2
53	41	D-Cover	2/25	Reserved SW5 for memory door on D-Cover	Reserved SW5(@)	DVT	0.2
54	14	PCH	2/26	Reserved for Intel PDG1.2 Table52-9	Reserved CC123, CC124,CC125	DVT	0.2
55	40	DMIC	3/2	Follow PDG1.2 Table28-3	R481,R482 change to 33 ohm	DVT	0.2
56	08	SPI	3/3	2015MOW06 no need PU1K on SPI_IO2/IO3	Un-Mount RC47	DVT	0.2
57	08	Crystal	3/3	Modify for 9pF Cyrstal	Change CC15,CC16 to 8.2pF	DVT	0.2
58	18,19	Memory	3/3	Mount decoupling capacitor	Mount and change CD1, CD17, CD28, CD47 to 0.1U_0402	DVT	0.2
59	35	SUSCLK	3/3	Del SUSCLK and reserved TP(Reqruie from Acer)	Del R426, C85 and add T3806	DVT	0.2
60	39	Others	3/3	Un-mount un-use part	Un-mount SW3	DVT	0.2
61	08	SMBUS	3/3	Add level shift for SOC_SMBCLK/SOC_SMBDATA	change RC202, RC49, RC50, RPC7 PU to +3VALW_PRIM add Q2017, RC220, RC221, RC222, RC223 change net name from SOC_SMBCLK/SOC_SMBDATA to SOC_SMBCLK_1/SOC_SMBDATA_1 change RPC7 PU to 2.2K	DVT	0.2
62	08	Others	4/1	Delete reserved component	Del RPC8, RC45, RPC6	PVT	0.3
63	08	SMBUS	4/1	Add BOM Structure for SPI ROM	Change RPC5 and RC52 to 15 ohm with 8M_SINGLE@ Add RPC5 and RC52 33 ohm with 8M_DUAL@ Add reserved component UC2 with 8M_DUAL@	PVT	0.3
64	08	SMBUS	4/1	Delete EC SPI path	Del RPC6	PVT	0.3
65	08	SPI	4/1	MOW36 QS sample no need to PD	Change RC51 to ES@	PVT	0.3
66	13,39,41	Others	4/1	Change 0 ohm to R-Short	0_0402 to R-Short: R2631, R2634, RC168, RC186	PVT	0.3
67	37	Others	4/1	SMT require delete un-use 0 ohm to avoid USB chock solder issue	Del R458, R461, R465, R466	PVT	0.3
68	38	LID	4/1	For 2nd source hall sensor soultion	Mount R618	PVT	0.3
69	30,31	Others	4/1	PD for HPD signal	Add R380 PD100K, Mount R2530	PVT	0.3
70	38	Others	4/1	Board ID Change for PVT	change R4903 to 15K	PVT	0.3
71	42	Others	4/8	Add discharge circuit for +1.05VSDGPU	Mount Q2008, R574, R1001	PVT	0.3
72	30,37,40	Others	4/14	Change 0 ohm to R-Short	0_0402 to R-Short: R368,R369, R370, R371, R372,R373, R374, R375 R473, R474, R475, R476, R477, R478, R479, R480 0_0603 to R-Short: R2135, R2151	PVT	0.3
73	37,38	Others	4/16	Change U77 pin4 control by EC GPIO	link U77.4 to U4901.119 Un-mount R857	PVT	0.3
74	12	CPU	4/17	Follow MOW10, USB2_ID/USB2_VBUSSENSE connect to GND	Change RC130, RC131 to 0 ohm	PVT	0.3
75	40	Audio	4/17	Beep Sound Path from EC	Change R2138, R2140 to 22K and mount R2138	PVT	0.3
76	06	CPU	4/22	Add test point for CATERR#	Add T166	PVT	0.3
77	06	Others	4/22	Cancel JAPS1 Mask to avoide soldering issue	change JAPS1 footprint to ACES_50506-01841-P01_18P-NPM	PVT	0.3
78	22, 25	GPU	4/30	Add Samsung E-Die VRAM Information	Add X76629BOL13/X76629BOL14	PVT	0.3
79	03, 07	CPU	4/30	Add QS sample CPU for BOM Selection	Add UC1 with QJFC@/QJ8N@/QJ8L@	PVT	0.3

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
80	42	Others	5/14	BOM Error	Change R574, R1001, Q2008 to VGA@	Pre-MP	1.0
81	38	Others	5/28	For abnormal shutdown	Mount D26	Pre-MP	1.0
82	38	Others	5/28	Board ID change to Rev1.0	Change R4903 to 20K_0402_1%	Pre-MP	1.0
83	01	Others	6/17	Update PCB Rev10 PN	Update PCB PN to DAZ1DR00100	Pre-MP	1.0
84	39	Others	6/22	Cancel the MASK of JLID1	Change JLID1 to ACES_50506-01041-P01_10P-NPM	Pre-MP	1.0
85	38	Others	7/14	Add C4917 for EC_RST#	Add C4917	Pre-MP	1.0
86	39	Others	7/14	Add S spec number for i3/i5/i7 CPU	add SR2EU@/SR2EY@/SR2EZ@ for UC1 MP number	Pre-MP	1.0

Security Classification	Compal Secret Data		
Issued Date	2013/10/30	Deciphered Date	2014/05/24

Compal Electronics, Inc.			
Title	PIR-HW		
Size: Custom	Document Number: Z5WAH M/B LA-B161P		Rev: 1.0
Date: Friday, July 17, 2015	Sheet 60 of 60		