Compal Confidential

C5V01 MB Schematic Document

LA-E892P

Rev: 1.A

2017.04.18

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Compal Electronics, Inc.		
Title: Cover Sheet		
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HDMI Conn.

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DDI1
HDMI x 4 lanes

eDP

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eDP

DDI

Intel Kabylake U

Kabylake U
Kabylake PCH-LP(MCP)
(KBL-U_2+2)
(KBL-RU_4+2)

Processor

Dual Core + GT2
Quad Core + GT2

Memory BUS
Dual Channel

1.2V DDR4 1866/2133

Interleaved Memory

DDR4-ON BOARD 4G 8Gbx16

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260pin DDR4-SO-DIMM X1

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eMMC

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eMMC

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Nvidia N16S-GTR /
N17S-G1
with GDDR5 x2

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PCIe 3.0 x 4
8GT/s
port 1-4

PCIE 3.0 x4
8GT/s
Port 9-12

Flexible IO
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Premium-U PCIE3.0

USB 3.0
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USB3 port 1
USB2 port 1

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conn x2
USB2 port3,4
on Sub/B

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CMOS
Camera
USB2 port 7

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USB TypeC
conn x1
USB3 port 2,3
USB2 port2

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USBx8 48MHz

HD Audio 3.3V 24MHz

NGFF
WLAN
USB2 port 5

PCIe 1.0
2.5GT/s
port 6

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PCIe 1.0
2.5GT/s
port 5

LAN(GbE)
Realtek 8411B

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SATA3.0
6.0 Gb/s
port 7
(SATA0)

SATA HDD
Conn.

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SATA3.0
6.0 Gb/s
port 8
(SATA1)

SATA CDROM
Conn.

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15W
1356pin BGA

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SPI ROM
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HDA Codec
ALC255 page 32

Touch
Screen

USB2 port 6

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SD conn.

RJ45 conn.

LPC/eSPI BUS

CLK=24MHz

ENE
KB9022

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Int. DMIC
on Camera

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UAJ
on Sub/B

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RTC CKT.

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Power On/Off CKT.

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Sub Board

LS-E891
IO/B

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DC/DC Interface CKT.

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LS-E892
Hall Sensor/B

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Power Circuit DC/DC

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Int.KBD

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Touch Pad
PS2 (from EC) / I2C (from SOC)
USB2 port 8 (FP)

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Title: Block Diagrams

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 1%

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3	PCB Revision
0	0	0 V	0 V	0.300 V	0x00 - 0x13	0.1(EVT)
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	1.0(DVT)
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	1.A(PVT)
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	1.A(MP)
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	1.A(EA17PVT)
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	1.A(EA17MP)
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VS_1.0VSDGPU	+1.05VS power rail for N16X/ +1.0VS power rail for N17S	ON*2	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON*2	OFF	OFF
+3VS_1.8VSDGPU_AON	+3VS power rail for N16X/ +1.8VS power rail for N17S(AON)	ON*2	OFF	OFF
+3VS_1.8VSDGPU_MAIN	+3VS power rail for N16X/ +1.8VS power rail for N17S(MAIN)	ON*2	OFF	OFF
+VGA_CORE	Core power for descrete GPU	ON*2	OFF	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.
ON*2 power plane is ON when DGPU turn on

BOM Structure Table

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
Acer BYOC	BYOC@ / NBYOC@
CODEC(ALC255)	255@
EC Mode Select	LPC@ / ESPI@
For Intel CMC	CMC@
LAN Mode Select	SWR@ / LDO@
EMI requirement	EMI@ / @EMI@
ESD requirement	ESD@ / @ESD@
RF requirement	@RF@
CPU Selection	U42@/U22@
SkyLake or KabyLake	SKL@ / KBL@
TPM	TPM@
Finger Print	FP@/FPEMC@
UMA or DGPU	UMA@/VGA@
DGPU Serial Select	N16X@/N17S@

BOM Option Table

Item	BOM Structure
MB Stage	EVT@/DVT@/PVT@/MP@
ODD Support	ODD@
G Sensor	BA@
For over 3 cell battery	3S@
C5V01, D5PR1	EA15@
D7W01	EA17@
D7W01 MB Stage	EA17PVT@/EA17MP@
N16SGTR or N17SG1	N16SGTR@ / N17SG1@
BOM Select	X76@
VRAM BOM Select	X7604@ ~ X7609@
Memory Select	X7601@ ~ X7603@
Memory Mode	SDP@ / DDP@
CPU Code	SR2UW@ QLDP@/QLDM@/QLDN@ QLYK@/QLYJ@/QLYH@ SR2ZW@/SR2ZU@/SR2ZV@ SR343@/SR342@/SR341@ QN5D@/QN5C@

43 level BOM table

43 Level	Description	BOM Structure
431A7EBOL07	SMT MB AE892 C5V01 N172G I36006 HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N17S@/N17SG1@/NBYOC@/SR2UW@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@
431A7EBOL08	SMT MB AE892 C5V01 N172G I57200 1.4HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N17S@/N17SG1@/NBYOC@/SR2ZU@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@
431A7EBOL10	SMT MB AE892 C5V01 N172G I77500 1.4HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N17S@/N17SG1@/NBYOC@/SR2ZV@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@
431A7EBOL11	SMT MB AE892 C5V01 SGT2G I3-6006U HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N16SGTR@/N16X@/NBYOC@/SR2UW@/U22@/VGA@/X7601@/X7604@/X4E01@/EA15@
431A7EBOL15	SMT MB AE892 C5V01 SGT2G I77500 1.4HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N16SGTR@/N16X@/NBYOC@/SR2ZV@/U22@/VGA@/X7601@/X7604@/X4E01@/EA15@
431A7EBOL16	SMT MB AE892 C5V01 SGT2G I3-7100U HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N16SGTR@/N16X@/NBYOC@/SR343@/U22@/VGA@/X7601@/X7604@/X4E01@/EA15@
431A7EBOL17	SMT MB AE892 C5V01 SGT2G I5-7200U HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N16SGTR@/N16X@/NBYOC@/SR342@/U22@/VGA@/X7601@/X7604@/X4E01@/EA15@
431A7EBOL18	SMT MB AE892 C5V01 SGT2G I7-7500U HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N16SGTR@/N16X@/NBYOC@/SR341@/U22@/VGA@/X7601@/X7604@/X4E01@/EA15@
431A7EBOL19	SMT MB AE892 C5V01 N172G I3-7100U HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N17S@/N17SG1@/NBYOC@/SR343@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@
431A7EBOL20	SMT MB AE892 C5V01 N172G I5-7200U HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N17S@/N17SG1@/NBYOC@/SR342@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@
431A7EBOL21	SMT MB AE892 C5V01 N172G I7-7500U HDMI	255@/3S@/CHG@/CMC@/MP@/KBL@/LDO@/LPC@/N17S@/N17SG1@/NBYOC@/SR341@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@

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Title: Notes List

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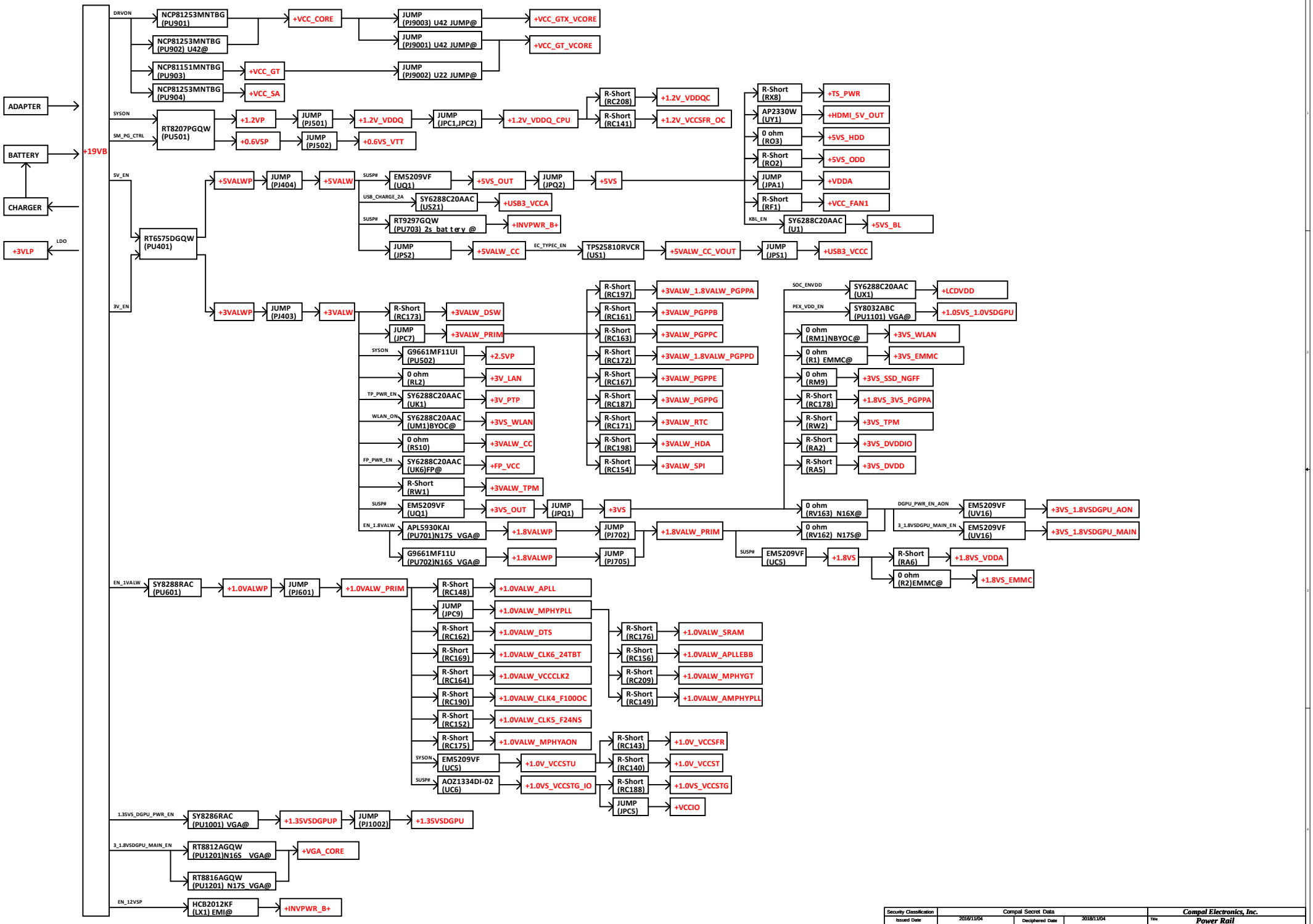

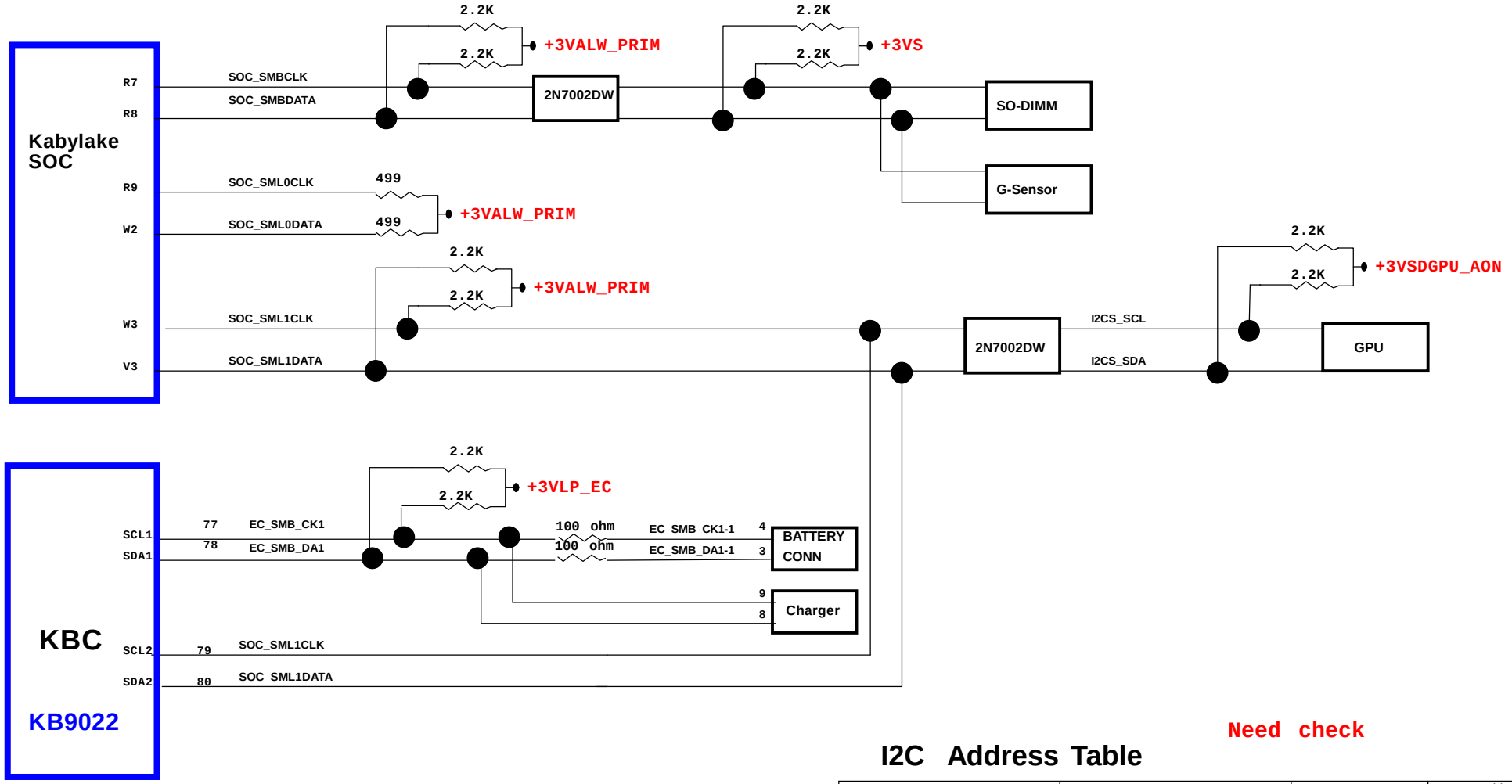

Need check

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Reserved			
I2C_1 (+3VALW_PGPPC)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x15		
SOC_SMBCLK +3VS	SO-DIMM	0xA4		
	G-Sensor	0x30		
SOC_SML1CLK +3VALW_PRIM	VGA	0x9E		
	EC			
EC_SMB_CK1 +3VLP	BQ24735 (Charger IC)	0x12		
	BATTERY PACK	0x16		

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Title: SMBUS Routing Table

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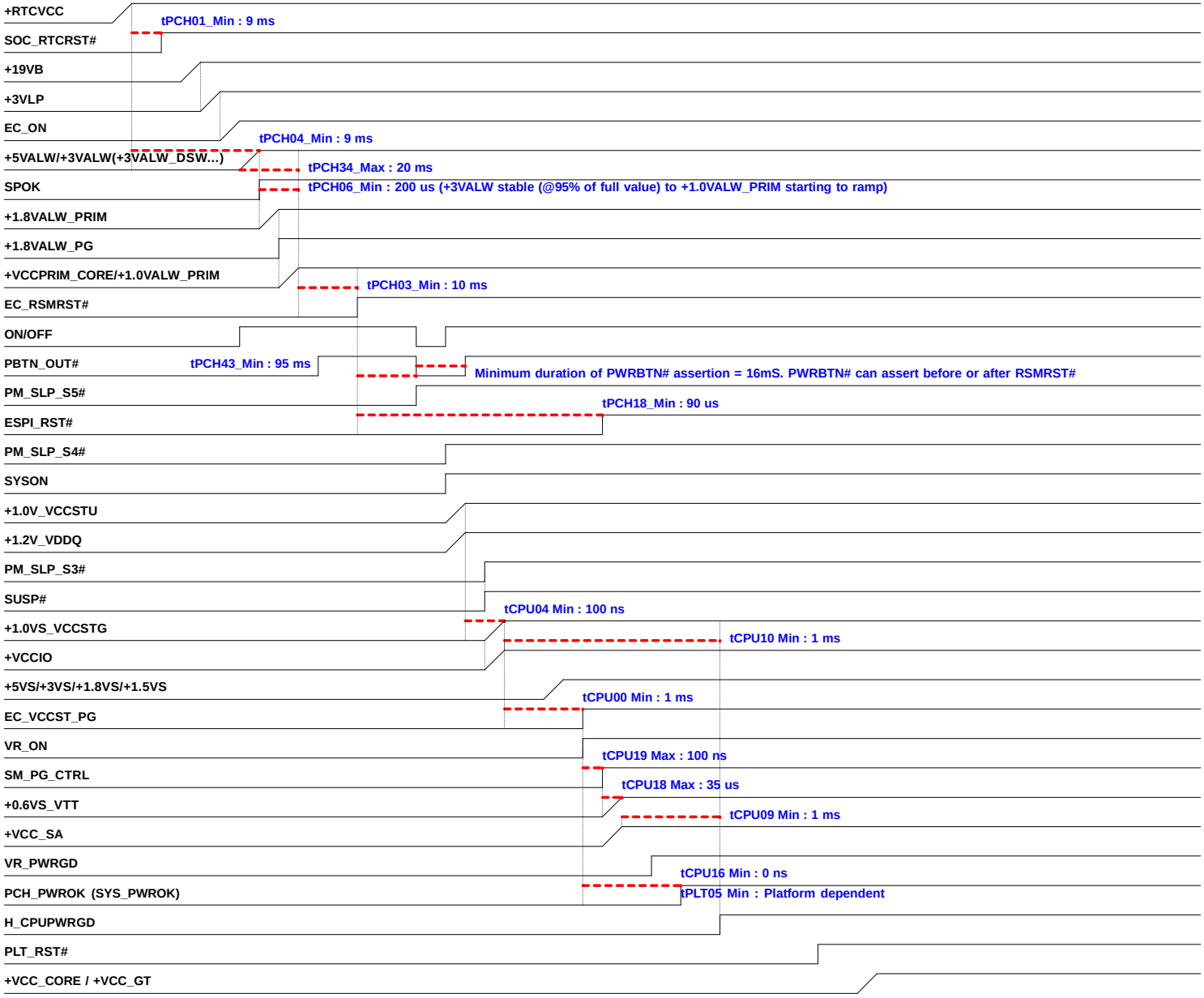
PWR Sequence_SKL-U2+2_DDR3L_Value_NON CS



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Title: Power Sequence

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Functional Strap Definitions

#543016 PDG2.0 P.844

DDPB_CTRLDATA
DDPC_CTRLDATA
Display Port B/C Detected
NC =Port is not detected.
PU =Port is detected.

+VCCIO
RC1 1 2 24.9_0402_1% EDP_COMP

#543016 PDG2.0 P.225
COMPENSATION PU for eDP
Trace width=5 mils,Spacing=25mil,Max length=600mils

+1.0V_VCCST
#543016 PDG2.0 P.857
PU 1K to VCCST
RC2 1 2 1K_0402_5% H_THERMTRIP#
CC132 1K 2 ESD@ 1000P_0402_50V7K

CC52 @ESD@ .1U_0402_16V7K 2 1 H_PECI
ESD@ CC53 1000P_0402_50V7K H_PROCHOT#_R
DVT 02/13

+1.0VS_VCCSTG
For Intel debug, place to CPU side.
#543016 PDG2.0 P.629
RC11 2 CMC@ 1 51_0402_5% SOC_XDP_TMS
RC13 2 @ 1 51_0402_5% SOC_XDP_TDI
RC15 2 CMC@ 1 51_0402_5% SOC_XDP_TDO
RC35 2 CMC@ 1 51_0402_5% CPU_XDP_TCK0

HDMI

UC1A SKL-U Rev_0.53

29 SOC_DP1_N0 E55 DDI1_TXN[0]
29 SOC_DP1_P0 F55 DDI1_TXP[0]
29 SOC_DP1_N1 E58 DDI1_TXN[1]
29 SOC_DP1_P1 F58 DDI1_TXP[1]
29 SOC_DP1_N2 F53 DDI1_TXN[2]
29 SOC_DP1_P2 G53 DDI1_TXP[2]
29 SOC_DP1_N3 F56 DDI1_TXN[3]
29 SOC_DP1_P3 G56 DDI1_TXP[3]
C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]
DDI

EDP_TXN[0] C47 EDP_TXN0 28
EDP_TXP[0] C46 EDP_TXP0 28
EDP_TXN[1] D46 EDP_TXN1 28
EDP_TXP[1] C45 EDP_TXP1 28
EDP_TXN[2] A45 EDP_TXN2 28
EDP_TXP[2] B45 EDP_TXP2 28
EDP_TXN[3] A47 EDP_TXN3 28
EDP_TXP[3] B47 EDP_TXP3 28
eDP
EDP_AUXN E45 EDP_AUXN 28
EDP_AUXP F45 EDP_AUXP 28
EDP
EDP_DISP_UTIL B52
DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46
DISPLAY SIDEBANDS

HDMI DDC (Port B)
29 SOC_DP1_CTRL_CLK SOC_DP1_CTRL_CLK L13 GPP_E18/DDPB_CTRLCLK
29 SOC_DP1_CTRL_DATA SOC_DP1_CTRL_DATA L12 GPP_E19/DDPB_CTRLDATA
N7 GPP_E20/DDPC_CTRLCLK
N8 GPP_E21/DDPC_CTRLDATA
N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA
EDP_COMP E52 EDP_RCOMP
1 OF 20
SKL-U_BGA1356
@

GPP_E13/DDPB_HPD0 L9 SOC_DP1_HPD SOC_DP1_HPD 29 **From HDMI**
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 N9 EC_SCI# CPU_EDP_HPD EC_SCI# 37 CPU_EDP_HPD 28 **From eDP**
GPP_E17/EDP_HPD L10
EDP_BKLTEN R12 ENBKL ENBKL 37
EDP_BKLTCTL R11 SOC_BKL_PWM SOC_BKL_PWM 28
EDP_VDDEN U13 SOC_ENVDD SOC_ENVDD 28

+1.0VS_VCCSTG
RC3 1K_0402_5%
RC4 499_0402_1%
37 H_PROCHOT#
Reserved CATERR# for sighti ngs issue check
@ T166 H_CATERR# D63 CATERR#
H_PECI A54 PECI
37 H_PECI
H_PROCHOT#_R C65 PROCHOT#
H_THERMTRIP# C63 THERMTRIP#
A65 SKTOCC#
CPU MISC
@ T160 XDP_BPM#0 C55 BPM#[0]
@ T161 XDP_BPM#1 D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]
A6 GPP_E3/CPU_GP0
A7 GPP_E7/CPU_GP1
37,38 EC_TP_INT# RC137 2 @ 1 0_0402_5% TP_INT# BA5 GPP_B3/CPU_GP2
AY5 GPP_B4/CPU_GP3
RC5 2 1 49.9_0402_1% CPU_POPIRCOMP AT16 PROC_POPIRCOMP
RC6 2 1 49.9_0402_1% PCH_OPIRCOMP AU16 PCH_OPIRCOMP
RC7 2 1 49.9_0402_1% EDRAM_OPIO_RCOMP H66 OPCE_RCOMP
RC8 2 1 49.9_0402_1% EOPIO_RCOMP H65 OPC_RCOMP
4 OF 20
SKL-U_BGA1356
@

UC1D SKL-U Rev_0.53
JTAG
PROC_TCK B61 CPU_XDP_TCK0
PROC_TDI D60 SOC_XDP_TDI
PROC_TDO A61 SOC_XDP_TDO
PROC_TMS C60 SOC_XDP_TMS
PROC_TRST# B59 SOC_XDP_TRST# T194 @
PCH_JTAG_TCK B56 PCH_JTAG_TCK1
PCH_JTAG_TDI D59 SOC_XDP_TDI T195 @
PCH_JTAG_TDO A56 SOC_XDP_TDO
PCH_JTAG_TMS C59 SOC_XDP_TMS
PCH_TRST# C61 SOC_XDP_TRST#
JTAGX A59 CPU_XDP_TCK0

#543016 PDG2.0 P.873
PROC_POPIRCOMP/PCH_OPIRCOMP
PD 50ohm

#544669 CRB1.1 P.52
EDRAM_OPIO_RCOMP/EOPIO_RCOMP
PD 50ohm

RC212 10K_0402_5% +3VS
EC_SCI# 1 @ 2
EC_SCI# SOC internal PU

#545659 PCH EDS1.51 P.131
SCI capability is available on all GPIOs, while NMI and SMI capability is available on only select GPIOs.
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:
- **GPP_B14 GPP_B20 GPP_B23**
- **GPP_C [23 : 22]**
- **GPP_D [4 : 0]**
- **GPP_E [8 : 0], GPP_E [16 : 13]**

@ESD@ CC81 .1U_0402_16V7K
SOC_XDP_TRST# 1 2

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Compal Electronics, Inc.

Title: **SKL-U(1/12)DDI,MSIC,XDP,EDP**

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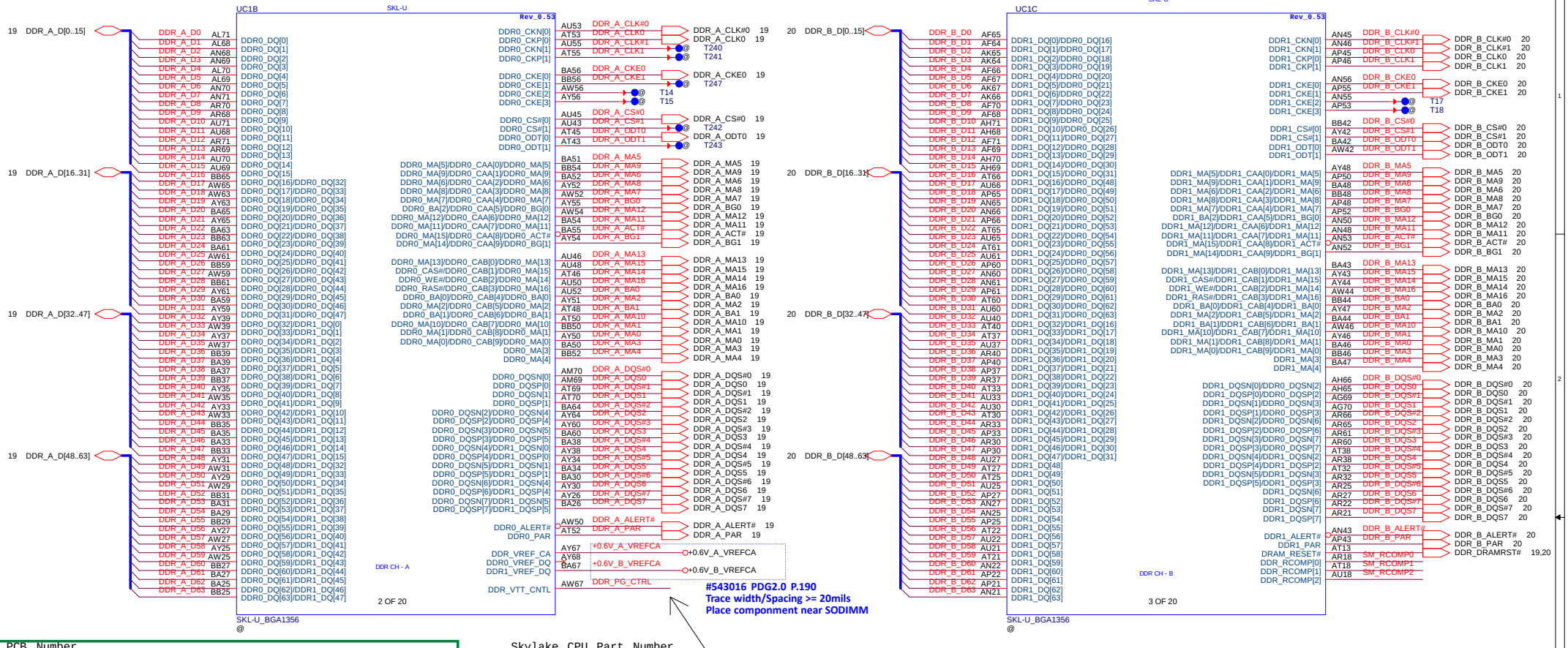
Interleaved Memory



#543016 PDG2.0 P.190
Trace width/Spacing >= 20mils
Place component near SODIMM

PCB Number

PVT 03/13

ZZZ	ZZZ	ZZZ
PCB C5V01 LA-E892P LS-E891P/E892P	PCB D7W01 LA-E892P LS-E892P/E893P	PCB 20X LA-E892P REV1A MB 2
DAZ20X00203	DAZ24C00100	DA8001AU01A
EA15@	EA17@	@

Kabylake U42 CPU Part Number

UC1	UC1
CPU_KBL_Y0_U42_I5_1.4G	CPU_KBL_Y0_U42_I7_1.8G
QN5D@	QN5C@
SA0000AR010	SA0000AQZ10

Skylake CPU Part Number

UC1
CPU_SKL_D1_i3-6006U_2.0G
SR2UW@
SA0000ACL30

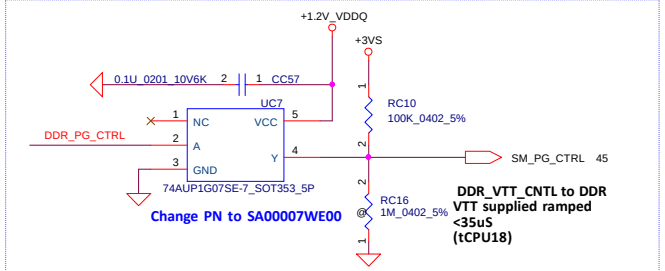
Kabylake CPU Part Number

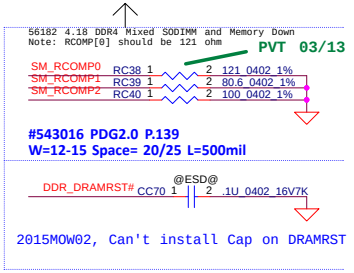
UC1 HDCP1.4	UC1 HDCP1.4	UC1 HDCP1.4
CPU_KBL_H0_i3-7100U_2.4G	CPU_KBL_H0_i5-7200U_2.5G	CPU_KBL_H0_i7-7500U_2.7G
QLDP@	QLDM@	QLDN@
SA0000A3820	SA0000A3720	SA0000A3400
UC1 HDCP2.2	UC1 HDCP2.2	UC1 HDCP2.2
CPU_KBL_H0_i3-7100U_2.4G	CPU_KBL_H0_i5-7200U_2.5G	CPU_KBL_H0_i7-7500U_2.7G
QLYK@	QLYJ@	QLYH@
SA0000A38K0	SA0000A37L0	SA0000A34J0

DVT 02/07

Kabylake CPU Part Number

UC1 HDCP1.4	UC1 HDCP1.4	UC1 HDCP1.4
CPU_KBL_H0_i3-7100U_2.4G	CPU_KBL_H0_i5-7200U_2.5G	CPU_KBL_H0_i7-7500U_2.7G
SR2ZW@	SR2ZU@	SR2ZV@
SA0000A3860	SA0000A3760	SA0000A3450
UC1 HDCP2.2	UC1 HDCP2.2	UC1 HDCP2.2
CPU_KBL_H0_i3-7100U_2.4G	CPU_KBL_H0_i5-7200U_2.5G	CPU_KBL_H0_i7-7500U_2.7G
SR343@	SR342@	SR341@
SA0000A38M0	SA0000A37N0	SA0000A34L0





Intel DOC: 549352

3. RCOMP[0] value for SDP is 200+/-1% ohm, and for DDP is 121+/- 1% ohm

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SKL-U(2/12)DDR4

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

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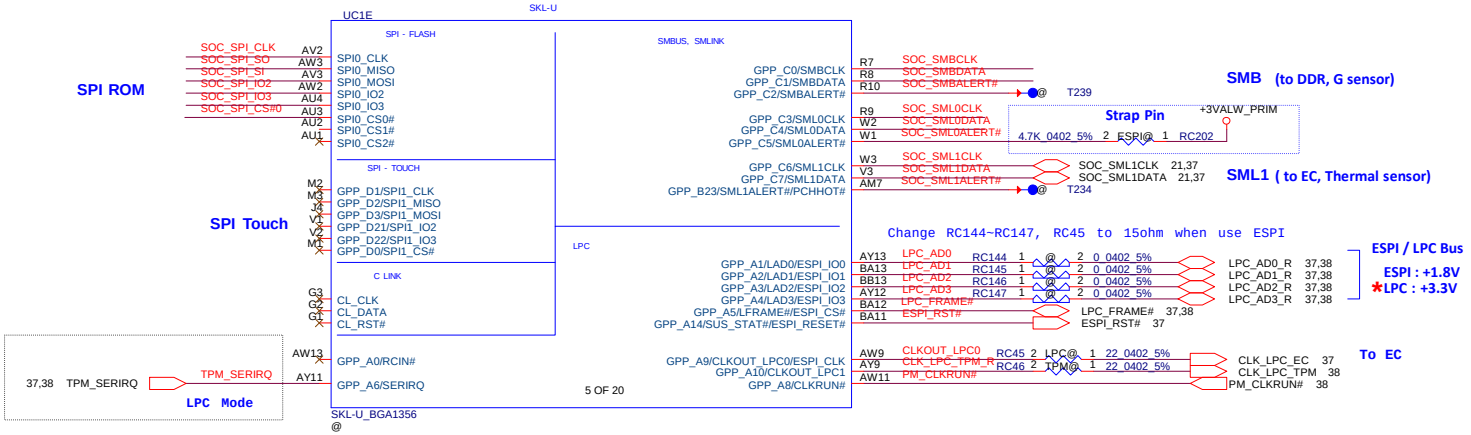
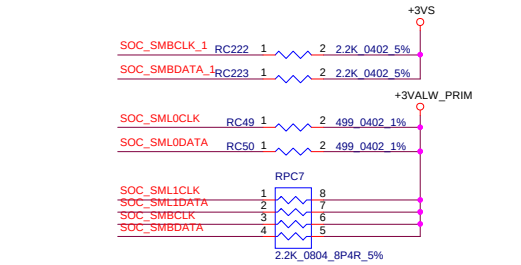
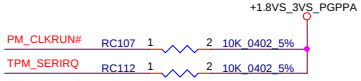




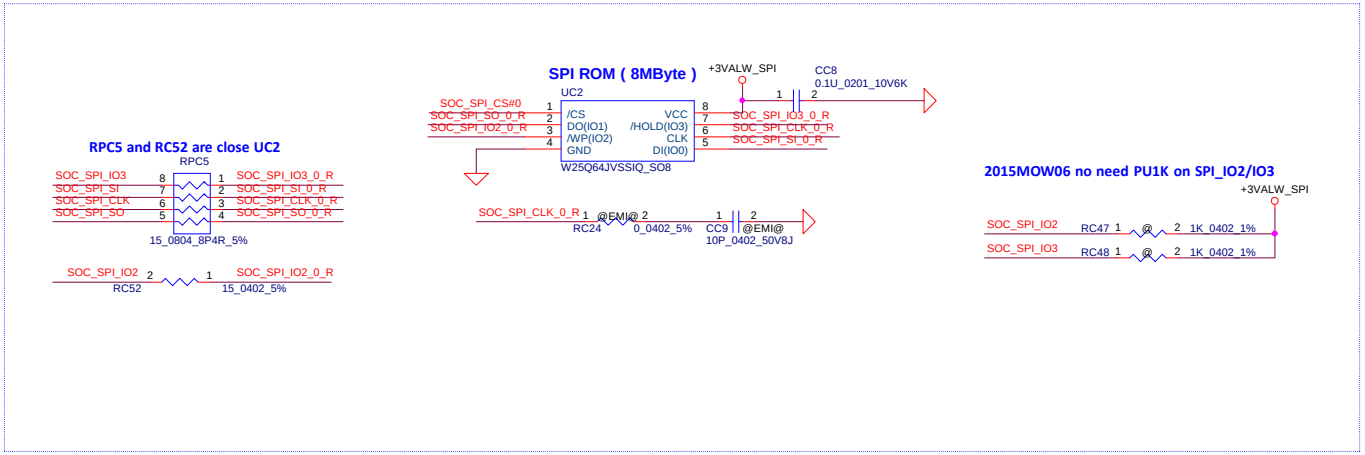


SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

eSPI or LPC
*0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

TLS Confidentiality
*0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)
1 = Enable Intel ME Crypto (TLS) (with confidentiality).
Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,ESPI,SMB,LPC

Size	Document Number	Rev
Custom	C5V01 M/B LA-E892P	1.A

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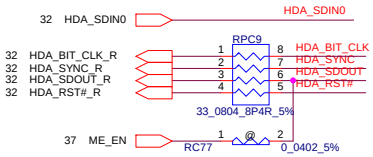
HDA for AUDIO



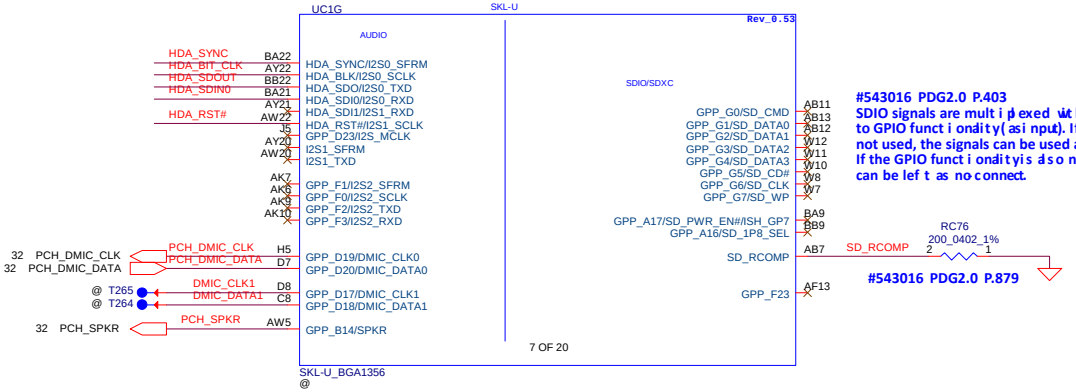
HDA_SDO / I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures defined in the flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external

pull-up in manufacturing/debug environments ONLY.

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

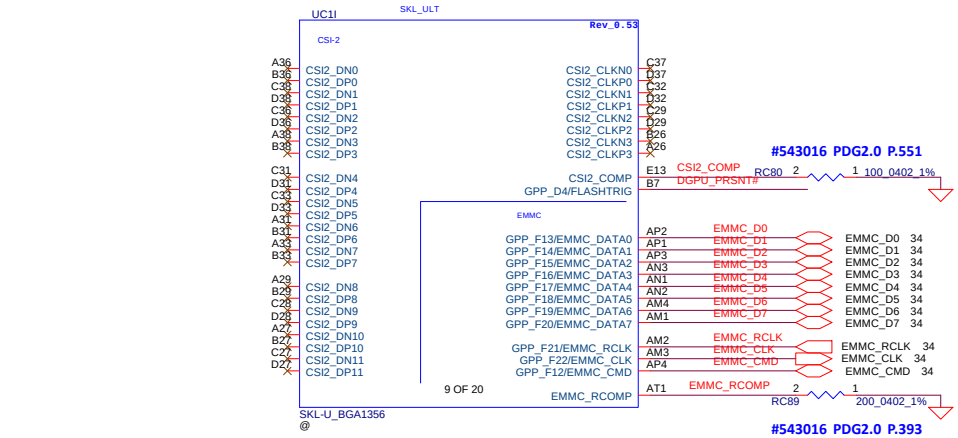
TOP Swap Override
*** 0 = Disable TOP Swap mode.**
1 = Enable TOP Swap Mode.

Intel HD Audio link capabilities
> Two SDI signals to support two external codecs.
> Drivers variable requency (5MHz to 24MHz) BCLK to support:
-- SDO double pumped up to 48 Mb/s
-- SDI's single pumped up to 24 Mb/s
> Provides cadence for 44.1 kHz based sample rate output.
> Support 1.5V, 1.8V, and 3.3V modes.



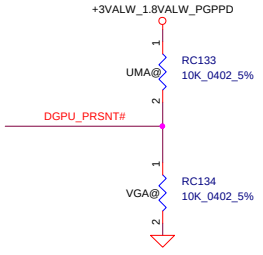
#543016 PDG2.0 P.403
SDIO signals are multiplexed with GPIOs and default to GPIO functionality(as input). If SDIO Interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, these signals can be left as no connect.

#543016 PDG2.0 P.879



#543016 PDG2.0 P.551

#543016 PDG2.0 P.393



	DGPU_PRSNT#
DIS,Optimus	0
UMA	1

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

Size	Document Number	Rev
Custom	C5V01 M/B LA-E892P	1.A

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PVT 03/20

563377 Intel MOW 33

DGPU

GLAN

WLAN

M.2/SSD

Place at RAM DOOR

CLR CMOS

From EC(open-drain)

Note for VCCST_PWRGD
1. 1.0V tolerance
2. PDG2.0 P.598 Figure43-5 note17: when failure events, VCCST_PWRGD and PCH_PWROK de-assert at the same t i me

WAKE# (DSX wake event)
10 KΩ pull- upt o VccDSW3_3
The pull-up is required even if PCIe* interface is not used on the plat f or m

DVT 01/23

DVT 02/13

DVT 02/13

#543016 PDG2.0 P.599
PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the plat f or m

Follow 2014MOW48
Skylake U PU 2.7k ohm to 1V
Cannonlake U PD 60.4 ohm

XCLK_BIASREF
T:50ohm S:12/15 L:1000 Via:2

2014MOW48:
Skylake-U use 24M 50 ohm ESR
Cannonlake U use 38.4M 30 ohm ESR

PCH PLTRST Buffer

Reserved for ESD place near UC2.1

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SKL-U(5/12)CLK,GPIO

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

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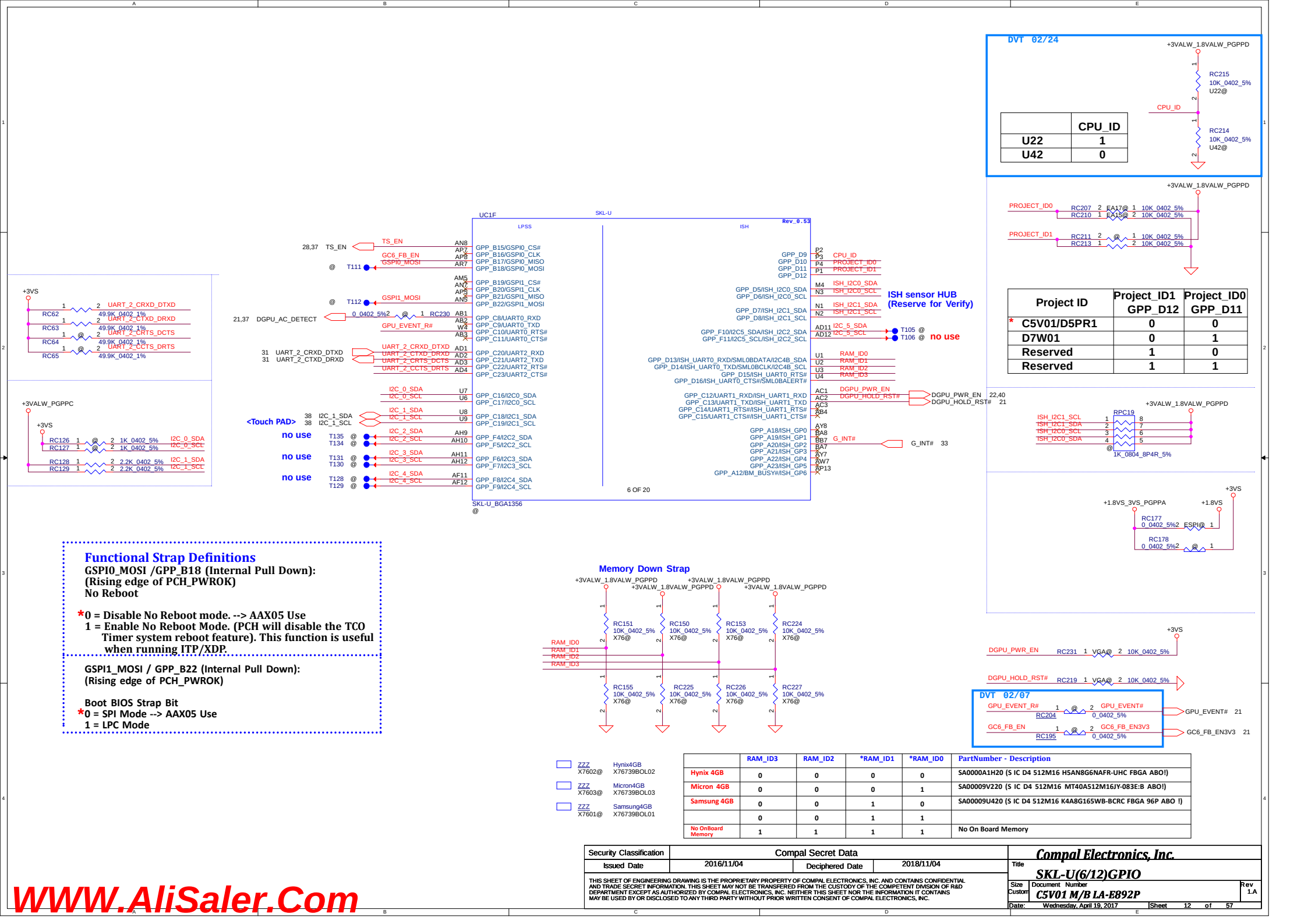
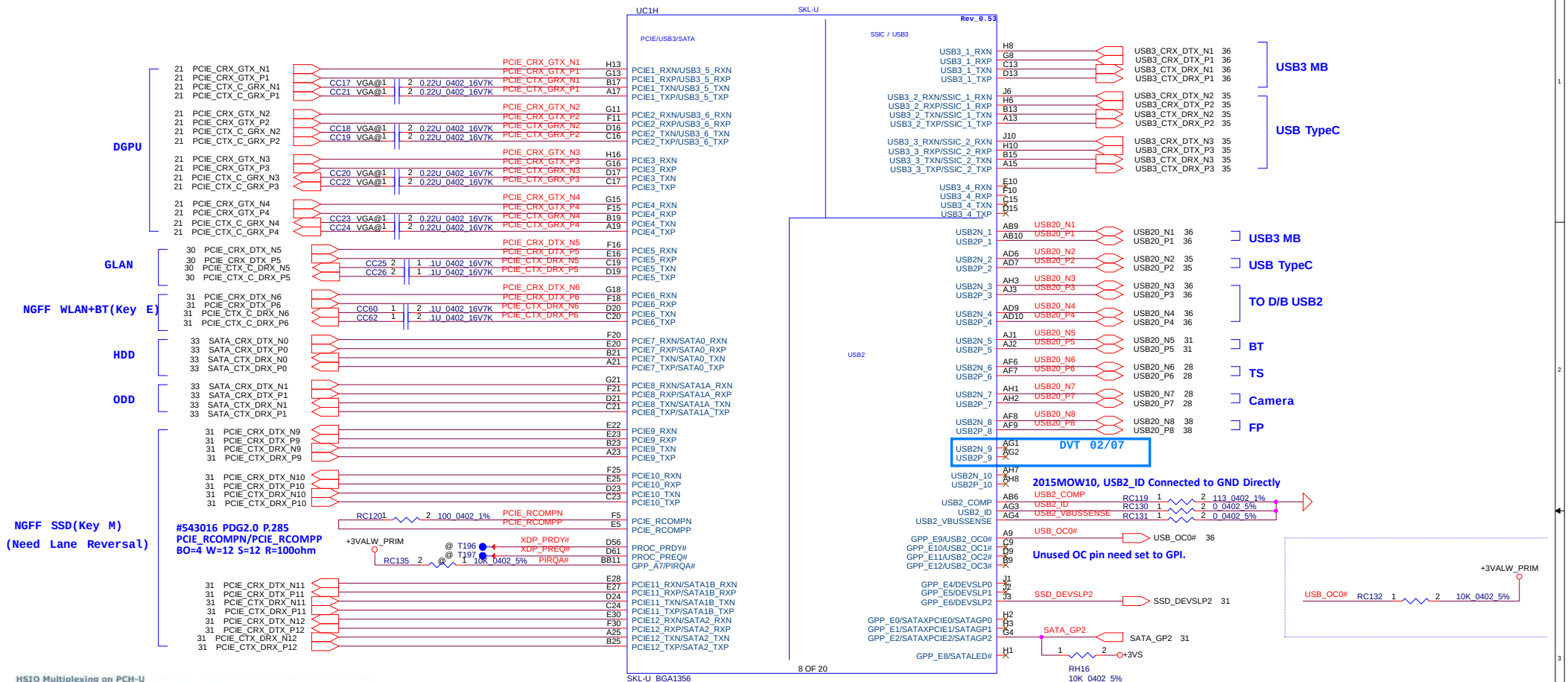
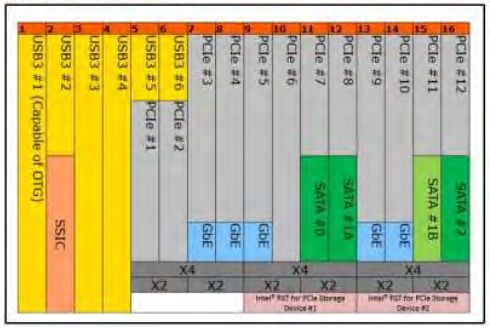




HSIO Multiplexing on PCH-U



PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RF1								RF3			
	2x2	RF1		RF3		RF5				RF5		RP11	
	1x2+2x1	RF1		RF3	RP4	RF5				RF5		RP11	RP12
	2x1+1x2	RP4	RP3	RF1		RP8	RP7			RP12	RP11	RF5	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6			RP9	RP10	RP11	RP12
Premium-U	1x4	RF1				RF5				RF5			
	2x2	RP1		RF3		RF5		RP7	RP8	RF5		RP11	
	1x2+2x1	RP1		RP3	RP4	RF5		RP7	RP8	RF5		RP11	RP12
	2x1+1x2	RP4	RP3	RF1		RP8	RP7	RF5		RP12	RP11	RF5	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation

DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.

The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.

- When high, DEVSLP requests the SATA device to enter into the DEVSLP power state
- When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals

- The processor provides three SATA general purpose input signals, SATAGP[2:0] for SKL U

These signals can be configured as interlock switch inputs corresponding to a given SATA port.

- When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.

If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

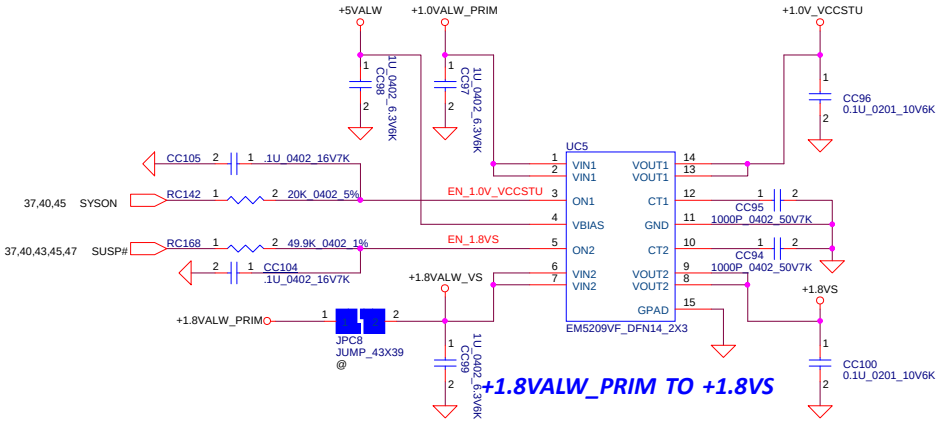
Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

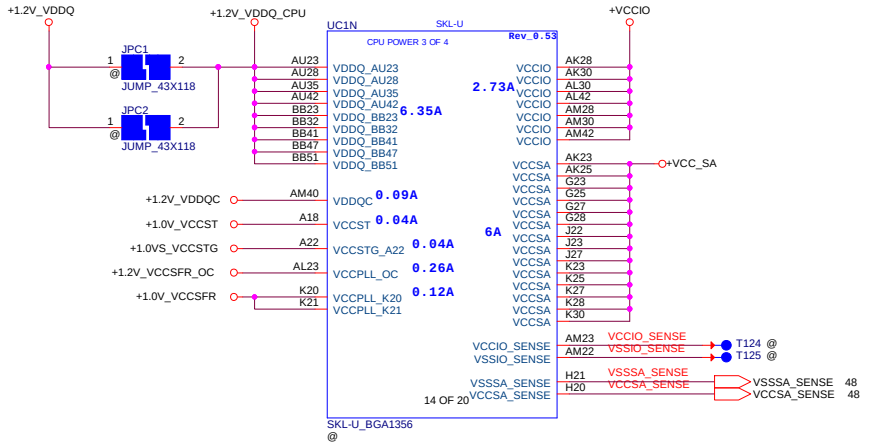
Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

Date: Tuesday, April 18, 2017 | Sheet 13 of 57

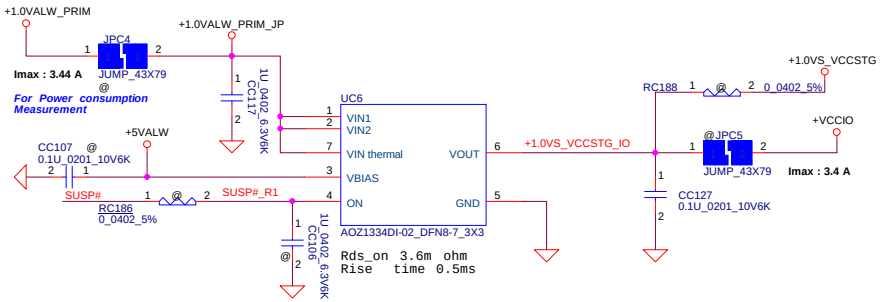
+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

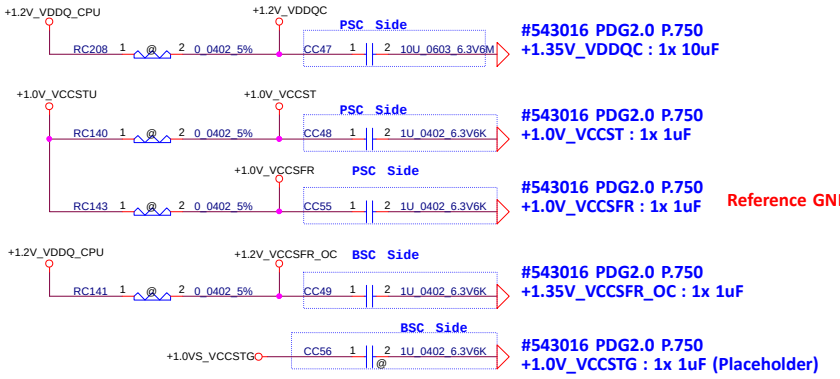


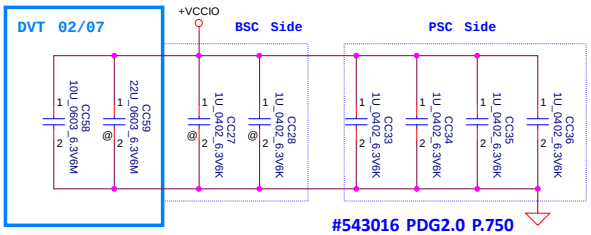
+1.8VALW_PRIM TO +1.8VS

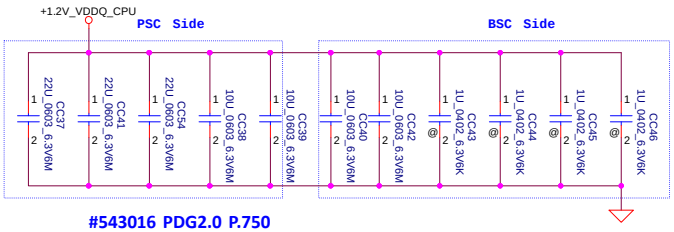


+1.0VALW_PRIM TO +1.0VS_VCCSTG









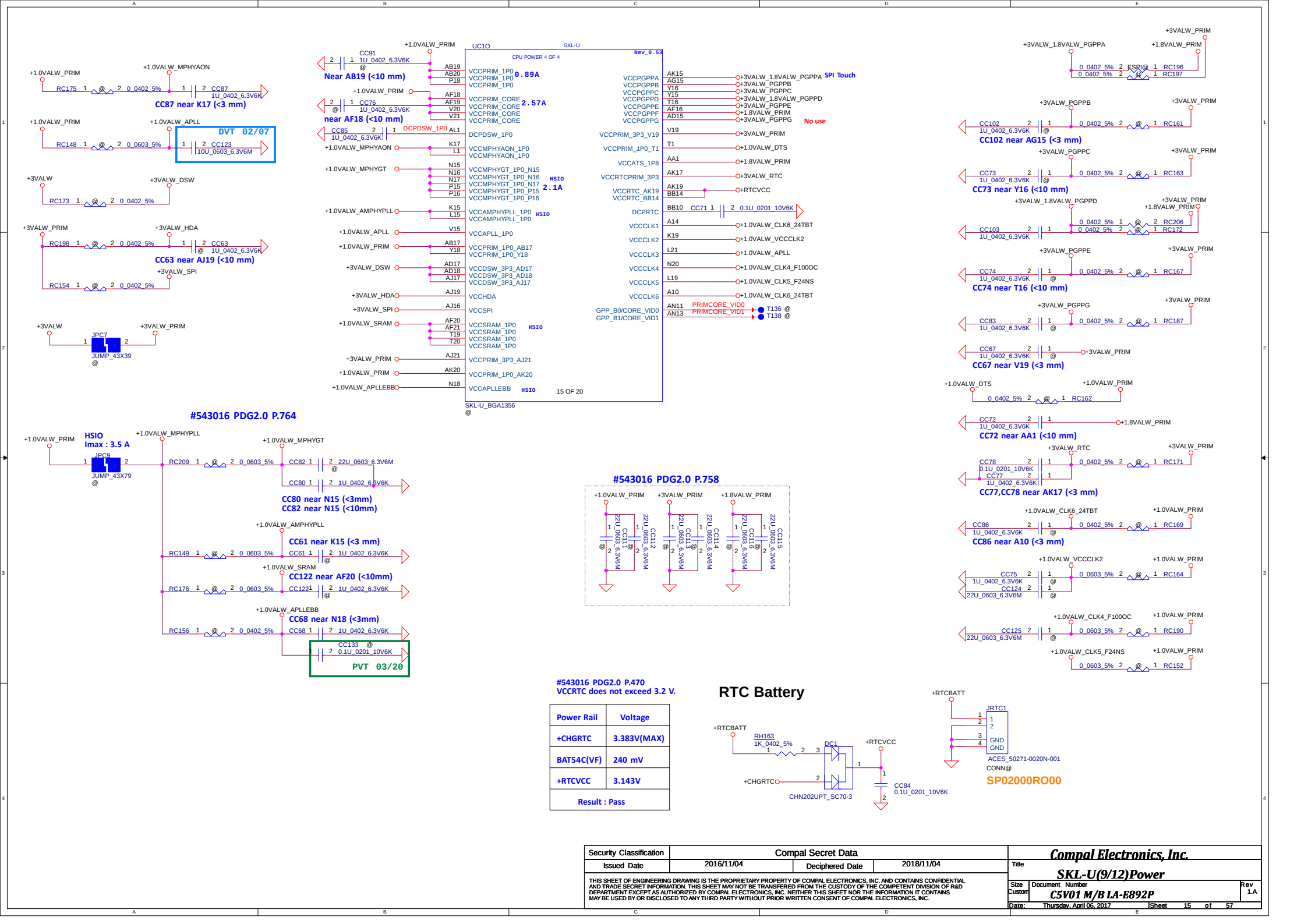
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SKL-U(8/12)Power

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

Date: Thursday, April 06, 2017 | Sheet 14 of 57



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SKL-U(9/12)Power

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

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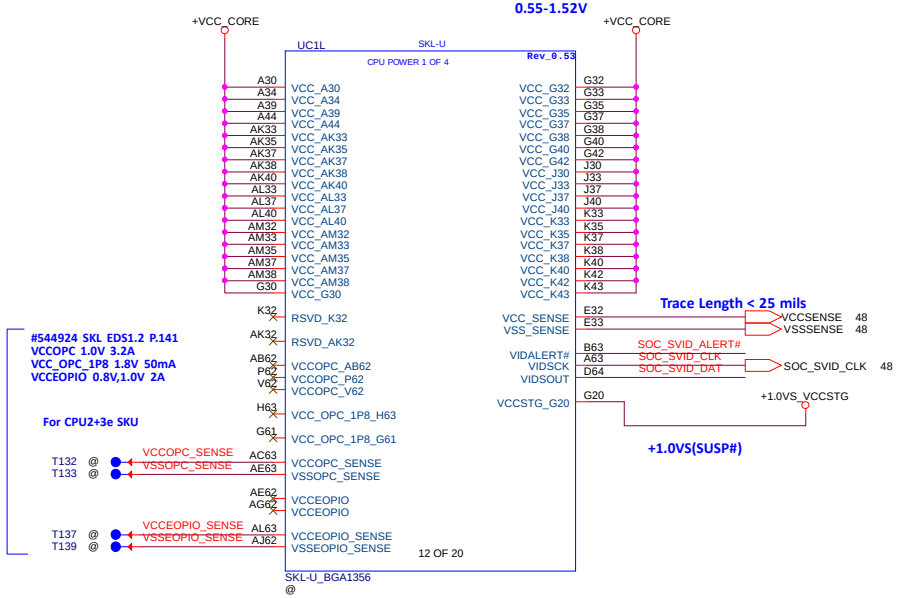
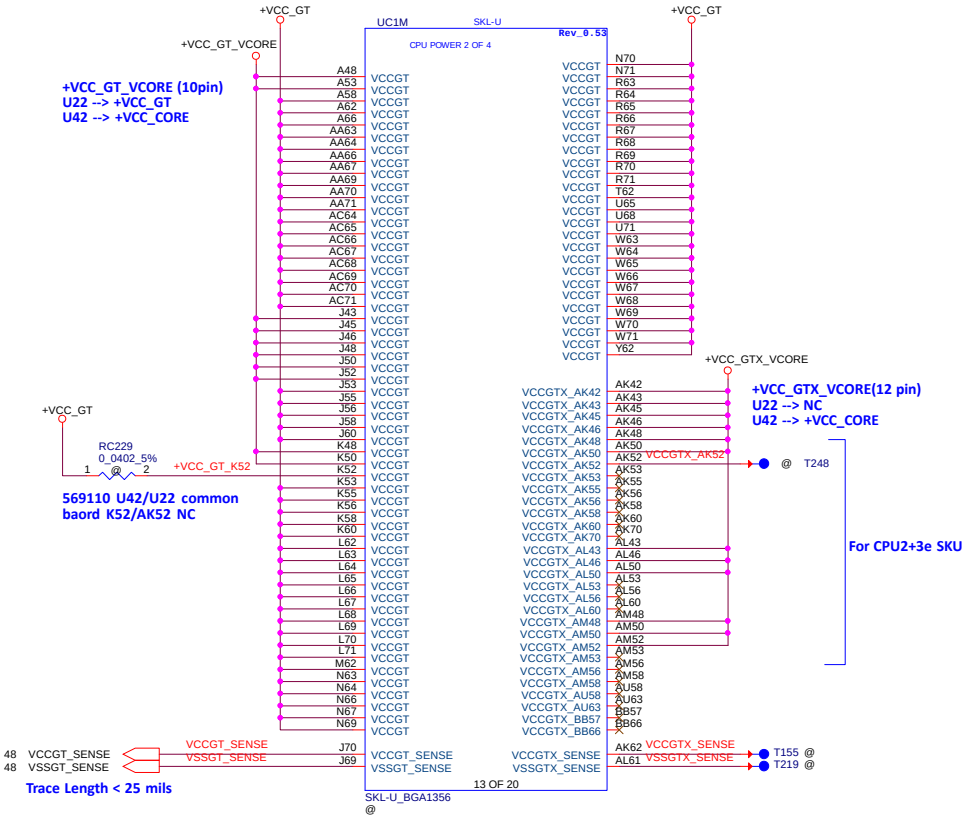
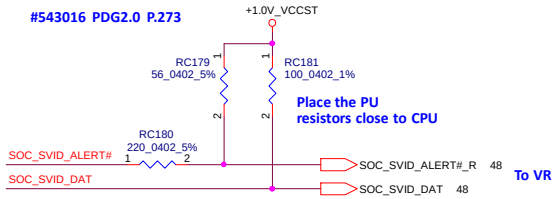
#544924 SKL EDS1.2 P.134
VCC U(15W)-dual core GT2 29A(MAX)
0.55-1.52V



#544924 SKL EDS1.2 P.136
VCCGT U(15W)-dual core GT2 31A(MAX)
0.55-1.5V



#543016 PDG2.0 P.273



Processor Power Rails

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

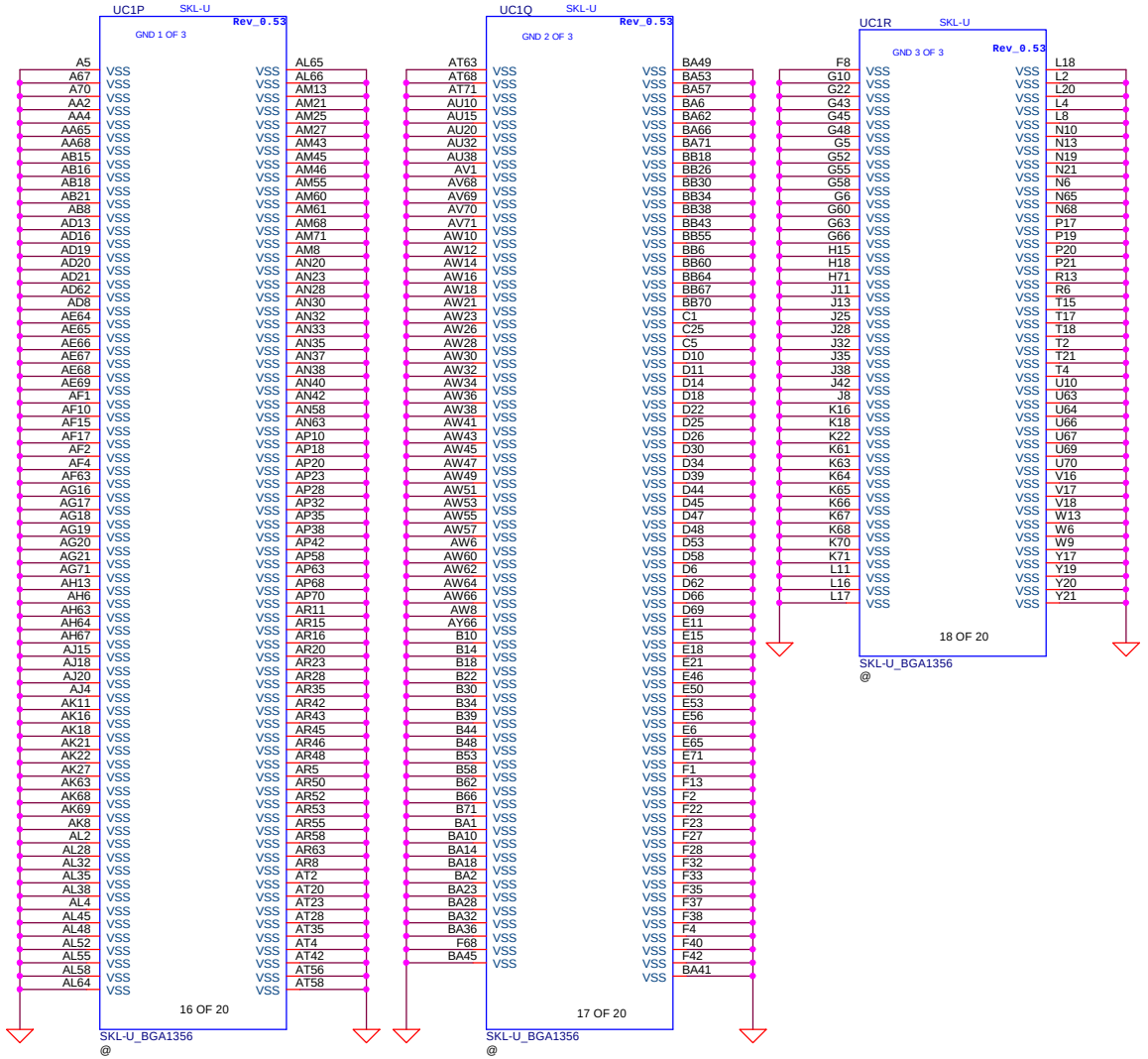
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SKL-U(10/12)Power,SVID

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

Date: Thursday, April 06, 2017 | Sheet 16 of 57



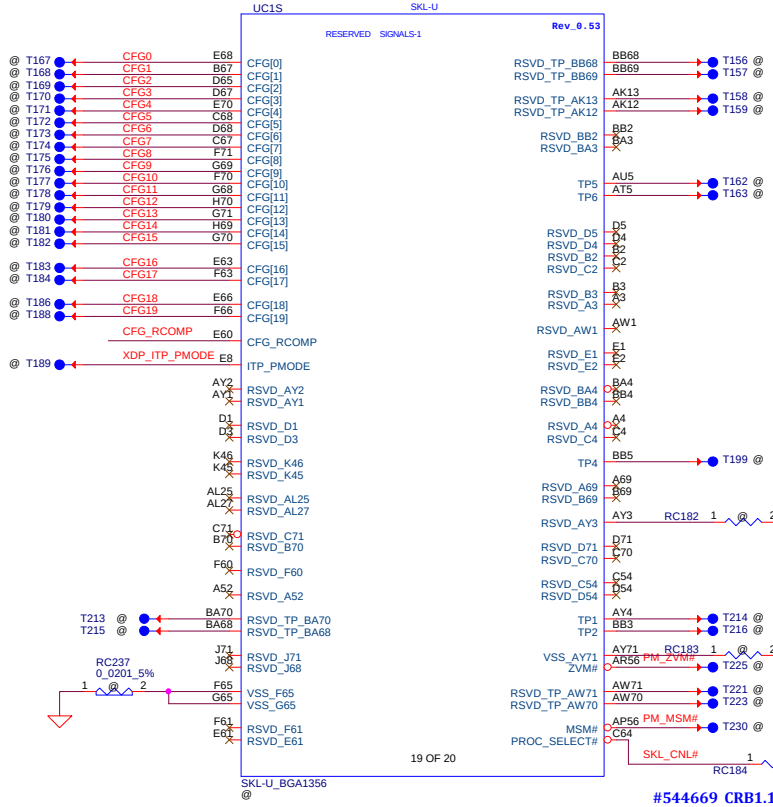
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

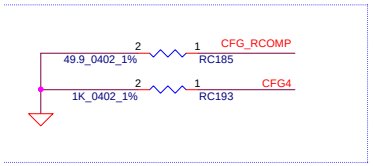
Compal Electronics, Inc.

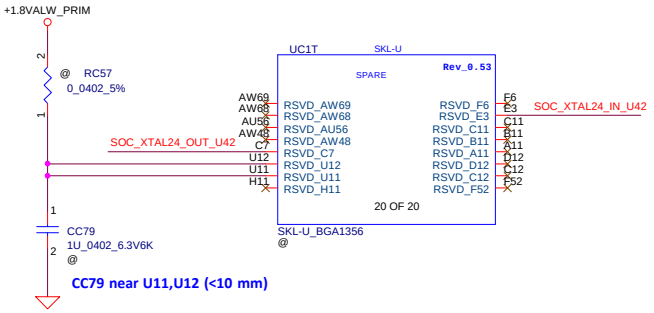
Title: **SKL-U(11/12)GND**

Size	Document Number	Rev
Custom	C5V01 M/B LA-E892P	1.A

Date: Thursday, April 06, 2017 Sheet 17 of 57







CC79 near U11,U12 (<10 mm)

14MOW52, Connect U11, U12 to 1.8V for Cannonlake-U PCH compat i bility

For 2+3e Solut i on

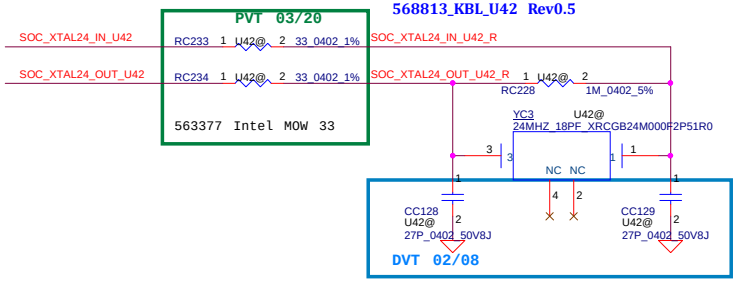
PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

PM_MSM#
Minimum Speed Mode: Control signal to VccEOPIO VR (connected only in 2 VR solut i on f or OPQ.

#544669 CRB1.1 P.54
#544924 SKL EDS1.2 P.125
PROC_SELECT#
This pin is for compatibility with future platforms. It should be unconnected for the processor.

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

568813_KBL_U42 Rev0.5



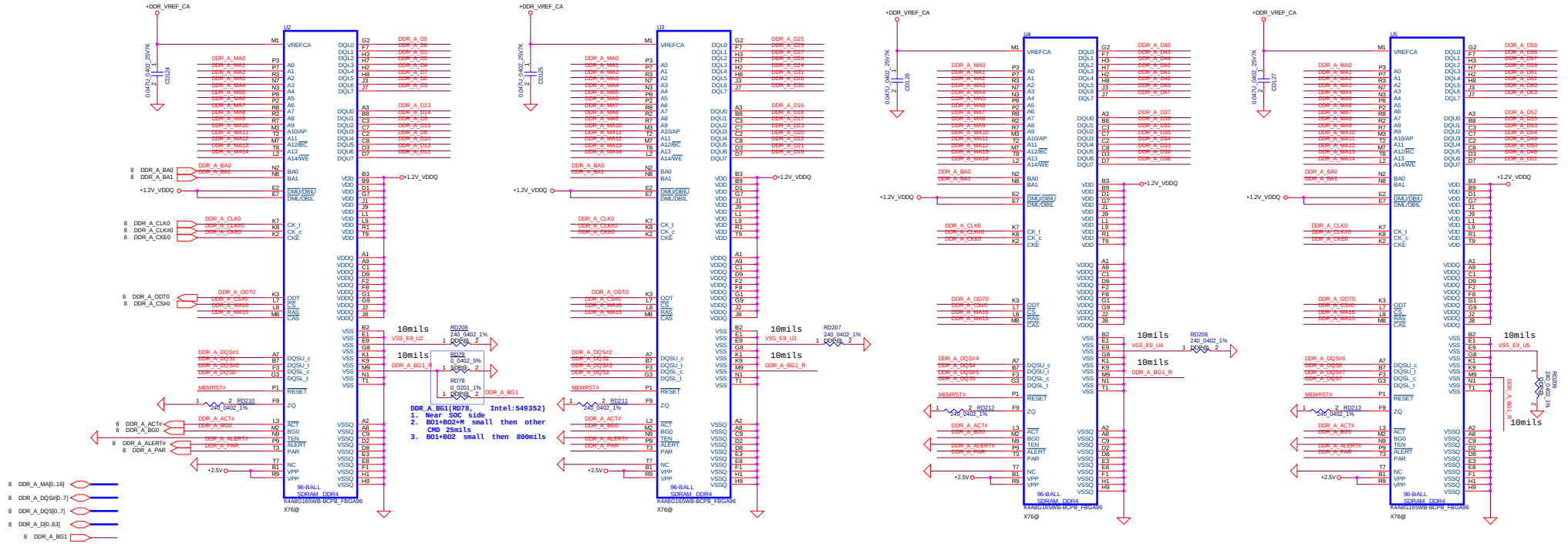
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SKL-U(12/12)RSVD

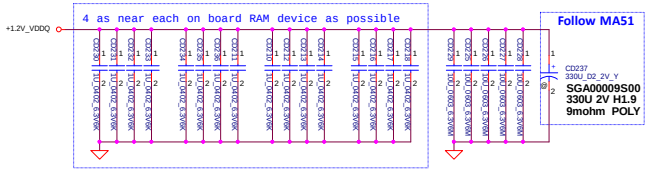
Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

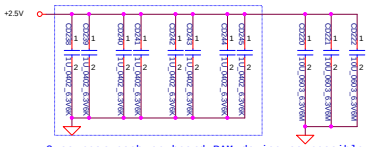
Date: Thursday, April 06, 2017 | Sheet 18 of 57

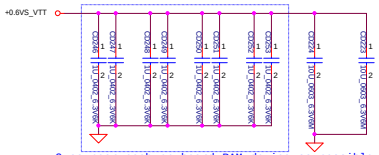


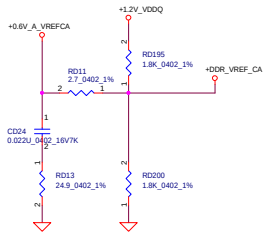
TERMINATION

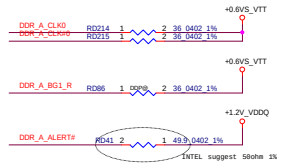
DDR4 mapping	SDP	DDP
E9	VSS	UZQ
M9	VSS	BG1
T7	NC	VSS
RCOMP[0] (SOC side)	200_1%	121_1%

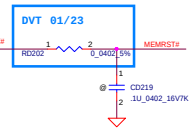


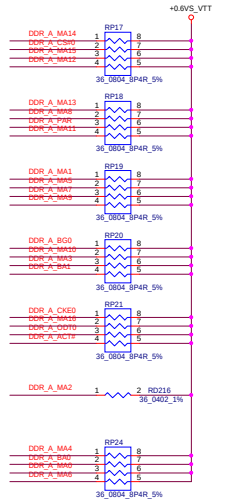












	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hynix 4GB	0	0	0	0	SA0000A1H20 (S IC D4 512M16 H5AN8G6NAFR-UHC FBGA ABO!)
Micron 4GB	0	0	0	1	SA00009V220 (S IC D4 512M16 MT40A512M16JY-083E:B ABO!)
Samsung 4GB	0	0	1	0	SA00009U420 (S IC D4 512M16 K4A8G165WB-BCRC FBGA 96P ABO !)
	0	0	1	1	
No OnBoard Memory	1	1	1	1	No On Board Memory

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: DDR4 ON BOARD CHIPS

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

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Standard Type

2-3A to 1 DIMMs/channel

8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DQS[0..7]

8 DDR_B_MA[0..16]
8 DDR_B_BA0 — DDR_B_BA0
8 DDR_B_BA1 — DDR_B_BA1
8 DDR_B_BG0 — DDR_B_BG0
8 DDR_B_BG1 — DDR_B_BG1
8 DDR_B_ACT# — DDR_B_ACT#
8 DDR_B_ALERT# — DDR_B_ALERT#
8 DDR_B_PAR — DDR_B_PAR

8 DDR_B_CLK0 — DDR_B_CLK0
8 DDR_B_CLK#0 — DDR_B_CLK#0
8 DDR_B_CLK1 — DDR_B_CLK1
8 DDR_B_CLK#1 — DDR_B_CLK#1

8 DDR_B_CKE0 — DDR_B_CKE0
8 DDR_B_CKE1 — DDR_B_CKE1
8 DDR_B_CS#0 — DDR_B_CS#0
8 DDR_B_CS#1 — DDR_B_CS#1

9,33 SOC_SMBDATA_1 — SOC_SMBDATA_1
9,33 SOC_SMBCLK_1 — SOC_SMBCLK_1

8 DDR_B_ODT0 — DDR_B_ODT0
8 DDR_B_ODT1 — DDR_B_ODT1

+3VS
RD52 0_0402_5%@
RD54 0_0402_5%@
RD56 0_0402_5%@
DDR_B_SA2
DDR_B_SA1
DDR_B_SA0

JDIMM2A
STD

DDR_B_CLK0	137	CK0(T)	DQ0	8	DDR_B_D10
DDR_B_CLK#0	139	CK0#(C)	DQ1	7	DDR_B_D14
DDR_B_CLK1	138	CK1(T)	DQ2	20	DDR_B_D9
DDR_B_CLK#1	140	CK1#(C)	DQ3	21	DDR_B_D12
			DQ4	4	DDR_B_D11
DDR_B_CKE0	109	CKE0	DQ5	3	DDR_B_D15
DDR_B_CKE1	110	CKE1	DQ6	16	DDR_B_D13
			DQ7	17	DDR_B_D8
DDR_B_CS#0	149	S0#	DQS0(T)	13	DDR_B_DQS1
DDR_B_CS#1	157	S1#	DQS0#(C)	11	DDR_B_DQS#1
	162	S2#/C0			
	165	S3#/C1	DQ8	28	DDR_B_D1
			DQ9	29	DDR_B_D0
DDR_B_ODT0	155	ODT0	DQ10	41	DDR_B_D7
DDR_B_ODT1	161	ODT1	DQ11	42	DDR_B_D2
			DQ12	24	DDR_B_D5
DDR_B_BG0	115	BG0	DQ13	25	DDR_B_D4
DDR_B_BG1	113	BG1	DQ14	38	DDR_B_D3
DDR_B_BA0	150	BA0	DQ15	37	DDR_B_D6
DDR_B_BA1	145	BA1	DQS1(T)	34	DDR_B_DQS0
			DQS1#(C)	32	DDR_B_DQS#0
DDR_B_MA0	144	A0			
DDR_B_MA1	133	A1	DQ16	50	DDR_B_D17
DDR_B_MA2	132	A2	DQ17	49	DDR_B_D21
DDR_B_MA3	131	A3	DQ18	62	DDR_B_D19
DDR_B_MA4	128	A4	DQ19	63	DDR_B_D23
DDR_B_MA5	126	A5	DQ20	46	DDR_B_D16
DDR_B_MA6	127	A6	DQ21	45	DDR_B_D20
DDR_B_MA7	122	A7	DQ22	58	DDR_B_D18
DDR_B_MA8	125	A8	DQ23	59	DDR_B_D22
DDR_B_MA9	121	A9	DQS2(T)	55	DDR_B_DQS2
DDR_B_MA10	146	A10_AP	DQS2#(C)	53	DDR_B_DQS#2
DDR_B_MA11	120	A11			
DDR_B_MA12	119	A12	DQ24	70	DDR_B_D25
DDR_B_MA13	158	A13	DQ25	71	DDR_B_D28
DDR_B_MA14	151	A14_WE#	DQ26	83	DDR_B_D31
DDR_B_MA15	156	A15_CAS#	DQ27	84	DDR_B_D27
DDR_B_MA16	152	A16_RAS#	DQ28	66	DDR_B_D24
			DQ29	67	DDR_B_D29
DDR_B_ACT#	114	ACT#	DQ30	79	DDR_B_D30
			DQ31	80	DDR_B_D26
DDR_B_PAR	143	PARITY	DQS3(T)	76	DDR_B_DQS3
DDR_B_ALERT#	116	ALERT#	DQS3#(C)	74	DDR_B_DQS#3
DDR_B_EVENT#	134	EVENT#			
DDR_DRAMRST#	108	RESET#	DQ32	174	DDR_B_D37
			DQ33	173	DDR_B_D32
SOC_SMBDATA_1	254	SDA	DQ34	187	DDR_B_D39
SOC_SMBCLK_1	253	SCL	DQ35	186	DDR_B_D35
			DQ36	170	DDR_B_D36
DDR_B_SA2	166		DQ37	169	DDR_B_D33
DDR_B_SA1	260	SA2	DQ38	183	DDR_B_D38
DDR_B_SA0	256	SA1	DQ39	182	DDR_B_D34
		SA0	DQS4(T)	179	DDR_B_DQS4
			DQS4#(C)	177	DDR_B_DQS#4
	92	CB0_NC			
	91	CB1_NC	DQ40	195	DDR_B_D41
	101	CB2_NC	DQ41	194	DDR_B_D45
	105	CB3_NC	DQ42	207	DDR_B_D46
	88	CB4_NC	DQ43	208	DDR_B_D42
	87	CB5_NC	DQ44	191	DDR_B_D40
	100	CB6_NC	DQ45	190	DDR_B_D44
	104	CB7_NC	DQ46	203	DDR_B_D43
DDR_B_DQS8	97	DQS8(T)	DQ47	204	DDR_B_D47
DDR_B_DQS#8	95	DQS8#(C)	DQS5(T)	200	DDR_B_DQS5
			DQS5#(C)	198	DDR_B_DQS#5
				216	DDR_B_D53
			DQ48	215	DDR_B_D49
	12	DM0#/DBI0#	DQ49	228	DDR_B_D54
	33	DM1#/DBI1#	DQ50	229	DDR_B_D51
	54	DM2#/DBI2#	DQ51	211	DDR_B_D48
	75	DM3#/DBI3#	DQ52	212	DDR_B_D52
	178	DM4#/DBI4#	DQ53	224	DDR_B_D55
	199	DM5#/DBI5#	DQ54	225	DDR_B_D50
	220	DM6#/DBI6#	DQ55	221	DDR_B_DQS6
	241	DM7#/DBI7#	DQS6(T)	219	DDR_B_DQS#6
	96	DM8#/DBI8#	DQS6#(C)		
				237	DDR_B_D61
			DQ56	236	DDR_B_D57
			DQ57	249	DDR_B_D58
			DQ58	250	DDR_B_D63
			DQ59	232	DDR_B_D60
			DQ60	233	DDR_B_D56
			DQ61	245	DDR_B_D59
			DQ62	246	DDR_B_D62
			DQ63	242	DDR_B_DQS7
			DQS7(T)	240	DDR_B_DQS#7
			DQS7#(C)		

FOX_AS0A821-H4SB-7H
CONN@
SP07001GA00

+1.2V_VDDQ
RD63 2 — 1 240_0402_1%
8,19 DDR_DRAMRST#
RD1 1 — 2 470_0402_5%
CD30 2 — 1 .1U_0402_16V7K @ESD@

RD61 2 — 1 240_0402_1%
RD62 2 — 1 240_0402_1%

+0.6V_B_VREFCA
RD46 1K_0402_1%
RD49 2_0402_1%
RD47 1K_0402_1%
RD50 24.9_0402_1%
CD66 0.022U_0402_16V7K
+0.6V_DDRB_VREFCA
10mils
CD65 0.1U_0201_10V6K

Place near to SO-DIMM connector.

JDIMM2B
STD

	111	VDD1	VDD11	141	
	112	VDD2	VDD12	147	
	117	VDD3	VDD13	148	
	118	VDD4	VDD14	153	
	123	VDD5	VDD15	154	
	124	VDD6	VDD16	159	
	129	VDD7	VDD17	160	
	130	VDD8	VDD18	163	
	135	VDD9	VDD19		
	136	VDD10			
+3VS	255	VDDSPD	VTT	258	+0.6VS_VTT
	164	VREFCA	VPP1	257	+2.5V
			VPP2	259	
	1	VSS	VSS	99	
	2	VSS	VSS	102	
	5	VSS	VSS	103	
	6	VSS	VSS	106	
	9	VSS	VSS	107	
	10	VSS	VSS	167	
	14	VSS	VSS	168	
	15	VSS	VSS	171	
	18	VSS	VSS	172	
	19	VSS	VSS	175	
	22	VSS	VSS	176	
	23	VSS	VSS	180	
	26	VSS	VSS	181	
	27	VSS	VSS	184	
	30	VSS	VSS	185	
	31	VSS	VSS	188	
	35	VSS	VSS	189	
	36	VSS	VSS	192	
	39	VSS	VSS	193	
	40	VSS	VSS	196	
	43	VSS	VSS	197	
	44	VSS	VSS	201	
	47	VSS	VSS	202	
	48	VSS	VSS	205	
	51	VSS	VSS	206	
	52	VSS	VSS	209	
	56	VSS	VSS	210	
	57	VSS	VSS	213	
	60	VSS	VSS	214	
	61	VSS	VSS	217	
	64	VSS	VSS	218	
	65	VSS	VSS	222	
	68	VSS	VSS	223	
	69	VSS	VSS	226	
	72	VSS	VSS	227	
	73	VSS	VSS	230	
	77	VSS	VSS	231	
	78	VSS	VSS	234	
	81	VSS	VSS	235	
	82	VSS	VSS	238	
	85	VSS	VSS	239	
	86	VSS	VSS	243	
	89	VSS	VSS	244	
	90	VSS	VSS	247	
	93	VSS	VSS	248	
	94	VSS	VSS	251	
	98	VSS	VSS	252	
	262	GND	GND	261	

FOX_AS0A821-H4SB-7H
CONN@
SP07001GA00

Layout Note:
Place near JDIMM2

+1.2V_VDDQ
CD32 1U_0402_6.3V6K
CD33 1U_0402_6.3V6K
CD34 1U_0402_6.3V6K
CD35 1U_0402_6.3V6K
CD36 1U_0402_6.3V6K
CD37 1U_0402_6.3V6K
CD69 1U_0402_6.3V6K
CD70 1U_0402_6.3V6K

+1.2V_VDDQ
CD38 10U_0603_6.3V6M
CD39 10U_0603_6.3V6M
CD40 10U_0603_6.3V6M
CD41 10U_0603_6.3V6M
CD42 10U_0603_6.3V6M
CD43 10U_0603_6.3V6M
CD44 10U_0603_6.3V6M
CD45 10U_0603_6.3V6M

Layout Note:
Place near JDIMM1.258

+0.6VS_VTT
CD64 10U_0603_6.3V6M
CD62 1U_0402_6.3V6K
CD63 1U_0402_6.3V6K

Layout Note:
Place near JDIMM1.257,259

+2.5V
CD68 10U_0603_6.3V6M
CD67 1U_0402_6.3V6K

Layout Note:
Place near JDIMM2.255

+3VS
CD55 2.2U_0402_6.3V6M

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: DDR4 DIMMB

Size	Document Number	Rev
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N16 GPU

GPIO	I/O	USAGE
GPIO0	O	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	3V3_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D Vision
GPIO8	I	SYS_PEX_RST_MON#
GPIO9	I/O	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	I	FRAME_LOCK#
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20		Reserved
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		

N17 GPU

GPIO	I/O	USAGE
GPIO0	O	PWM_VID
GPIO1	O	GC6_FB_EN
GPIO2	I	GPU_EVENT#
GPIO3	I/O	NVVDDS_PWM
GPIO4	O	1V8_MAIN_EN
GPIO5	I	FRAME_LOCK#
GPIO6	O	PSI
GPIO7	O	LCD_BL_PWM
GPIO8	O	MEM_VDD_CTL
GPIO9	I/O	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	LCD_VDD
GPIO12	I	PWR_LEVEL
GPIO13	O	LCD_BLEN
GPIO14	I	HPD_IFPA
GPIO15	I	HPD_IFPB
GPIO16		Reserved
GPIO17	I	HPD_IFPD
GPIO18	I	HPD_IFPE
GPIO19	O	3D_VISION
GPIO20		Reserved
GPIO21		Reserved (OC_WARN)
GPIO22		Reserved
GPIO23		Reserved

GC6 2.0 function

Table 15-8. I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E (Default)
1	0x9C (multi-GPU usage)

10.2.2 I²CS Slave Address

N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: N16X PEG 1/9

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

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VRAM Interface

DVT 02/07
UGPU1
S IC N16S-GTR-S-A2 BGA 595P GPU ABO !
N16SGTR@
SA00009FP40

PVT 03/13
UGPU1
S IC N17S-G1-A1 BGA 595P GPU ABO !
N17SG1@
SA0000ANV10

26 MDA[15..0] MDA[15..0]
26 MDA[31..16] MDA[31..16]
27 MDA[47..32] MDA[47..32]
27 MDA[63..48] MDA[63..48]

UGPU1B
Part 2 of 6
MEMORY INTERFACE A
GM108-ES-S-A1_FCBGA595
@

CMDA[31..0] 26,27

+1.35VSDGPU

CMDA14 RV87 2 VGA@ 1 10K_0402_5%
CMDA30 RV88 2 VGA@ 1 10K_0402_5%
CMDA13 RV89 2 VGA@ 1 10K_0402_5%
CMDA29 RV90 2 VGA@ 1 10K_0402_5%

+3VS

RV106 10K_0402_5% @
RV108 10K_0402_5% @
QV7A PJT138KA 2N SOT363-6
QV7B PJT138KA 2N SOT363-6 @

DVT 01/23
Power Side PU to +3VS_1.8VSDGPU_AON
RV188 0_0402_5% 1 VGA@ 2 VGA_CORE_PG

UV10 N16X@ MC74VHC1G08DFT2G_SC70-5 SA00000OH00
VCC: 2.0 ~ 5.5V
Push Pull Output

DVT 02/09
DV10 N17S@ RB751S40T1G_SOD523-2
RV103 10K_0402_1%
21,40 3_1.8VSDGPU_MAIN_EN
DGPU_MAIN_EN
CV231 @ .1U_0402_16V7K
DVT 01/23

+3VS_1.8VSDGPU_AON
VCC: 1.65 ~ 5.5V
Push Pull Output
PEX_VDD_EN PEX_VDD_EN 40,52
UV10 N17S@ NL17SZ08DFT2G_SC70-5
DGPU_PWR_EN 12,40

21,37 GPU_OVERT# GPU_OVERT#
DV7 RB751S40T1G_SOD523-2 VGA@
RV189 N17S@ 2.2K_0402_5% SD028220180
PVT 03/09
RV189 1 N16X@ 2 1K_0402_1% NVVDD_EN 53
N17S@ DV11 RB751S40T1G_SOD523-2
CV263 .1U_0402_16V7K VGA@

+3VS_1.8VSDGPU_AON
CV230 0.1U_0201_10V6K VGA@
21 PLTRST_VGA# PLTRST_VGA#
+3VS_1.8VSDGPU_AON RV102 10K_0402_5%
21 GC6_FB_EN1V8
QV6A PJT138KA 2N SOT363-6 N17S@
QV6B PJT138KA 2N SOT363-6 N17S@
UV9 NL17SZ08DFT2G_SC70-5 N17S@
VCC: 1.65 ~ 5.5V
Push Pull Output
VGA_CORE_PG VGA_CORE_PG 53

DVT 02/10
Near Power PWM IC

Thermal shutdown protection

UV9 N16X@ MC74VHC1G08DFT2G_SC70-5 SA00000OH00
QV6 N16X@ 2N7002KDW_SOT363-6 SB00000EO00
VCC: 2.0 ~ 5.5V
Push Pull Output

+FB_PLLAVDD
R2029 10K_0402_5% N16X@
FB_CLAMP
R2020 60.4_0402_1%
R2022 60.4_0402_1%
+1.35VSDGPU
T97 @

+PEX_IOVDDQ
15+55mA
Place Under F16 P22
L2002 PBY160808T-300Y-N_2P
C2008 VGA@ 22U_0603_6.3V6M
C2011 VGA@ 1U_0402_16V7K
C2010 VGA@ 1U_0402_16V7K
+FB_PLLAVDD
C2009 N17S@ 0.1U_0201_10V6K
C2736 N17S@ 0.1U_0201_10V6K
Place Near GPU
Place Under H22
SM010008A00 3000ma 30ohm@100mhz DCR 0.03

DA-08329-001_V01
Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FB PLL Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	4	Under GPU
	22 µF	X6S	0805	1	1	Near GPU
	Bead Type					
	30 Ω (ESR=0.010 Ω)		0603	1	1	Near GPU

NV 15x DG-06803-V03
NV 16x DG-07158-V04

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: N16X VRAM 2/9

Size	Document Number	Rev
Custom	C5V01 M/B LA-E892P	1.A

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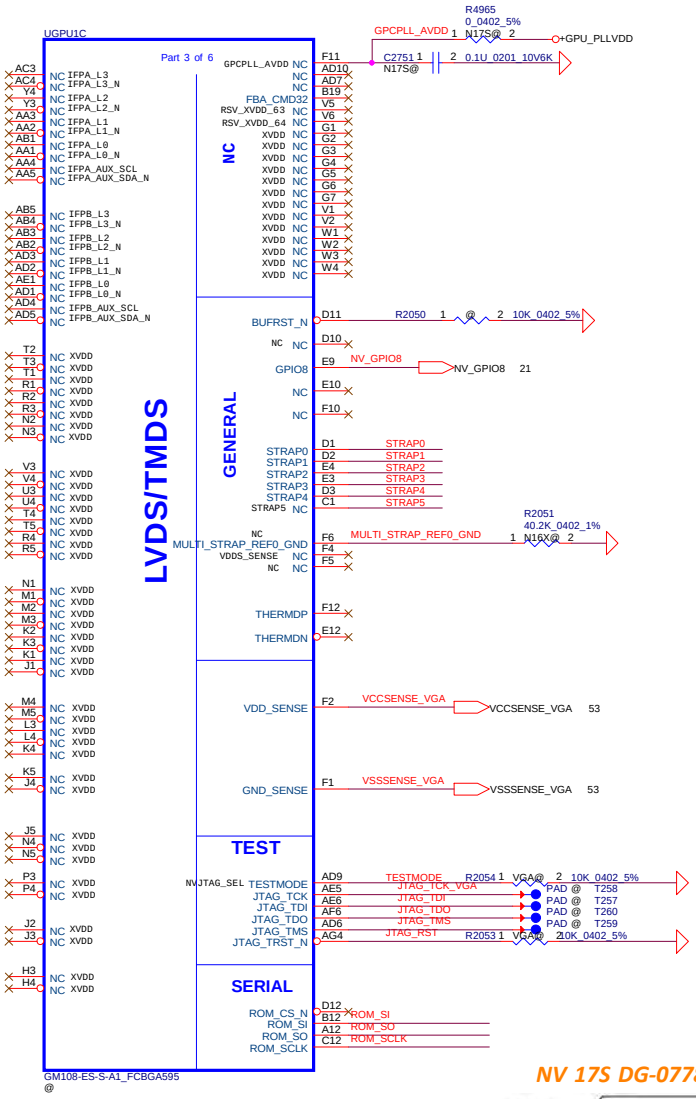
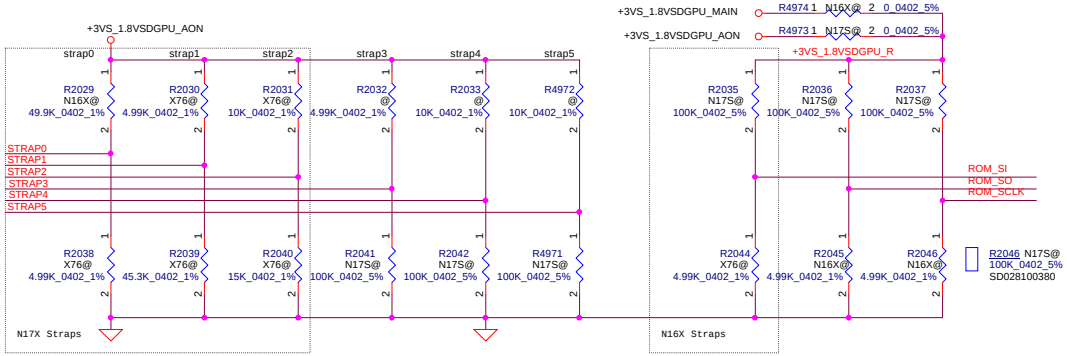




Multi strap table

Decive ID : N16S-GTR 0x134D

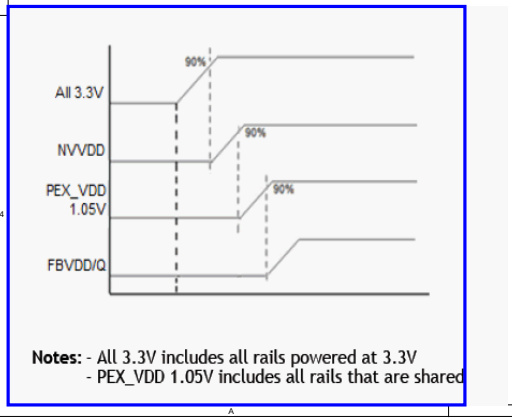
GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	strap5	ROM_SI	ROM_SO	ROM_SCLK
N16S-GTR	+1.35V			2.5GHz	128Mx32x2 1G	0x7 (SA00009TT30) Samsung K4G41325FE-HC28	PU 49.9K	NC	NC	NC	NC	NC	PD 45.3K	PD 4.99K	PD 4.99K
						0x6 (SA000085V70) Hynix H5GC4H24AJR-T2C							PD 34.8K		
						0x3 (SA00007D880) Samsung K4G41325FC-HC03							PD 20K		
						0x4 () Micron							PD 24.9K		
			X76739BOL04		256Mx32x2 2G	0x0 (SA000094R30) Samsung K4G80325FB-HC03							PD 4.99K		
			X76739BOL05			0x5(SA00009ZG20) Hynix H5GC8H24MJR-T2C							PD 30.1K		
			X76739BOL06			0x1 (SA000096K30) Micron MT51J256M32HF-60:A							PD 10K		

Multi strap table

Decive ID : N17S-G1-A1 0x1D10

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	strap5	ROM_SI	ROM_SO	ROM_SCLK
N17S-G1	+1.35V			3.0GHz	128Mx32x2 1G	0x7 (SA00009TT30) Samsung K4G41325FE-HC28	PU 100K	PU 100K	PU 100K	PD 100K	PU 100K	PU 100K	PU 100K	PU 100K	PU 100K
						0x6 (SA00008HQ10) Hynix H5GC4H24AJR-R0C	PD 100K	PU 100K	PU 100K						PD 100K
						0x8 (SA00009E300) Micron EDW4032BABG-70-F-R	PU 100K PD 100K	PD 100K	PD 100K						
			X76739BOL07		256Mx32x2 2G	0x0 (SA000092D00) Samsung K4G80325FB-HC28	PD 100K	PD 100K	PD 100K						
			X76739BOL08			0x2 (SA00009U110) Hynix H5GC8H24MJR-R0C	PD 100K	PU 100K	PD 100K						
			X76739BOL09			0x1 (SA00009TV10) Micron MT51J256M32HF-70:A	PU 100K	PD 100K	PD 100K						

VGA Power Sequence (N16X)



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

NV 17S DG-07785-001_V07

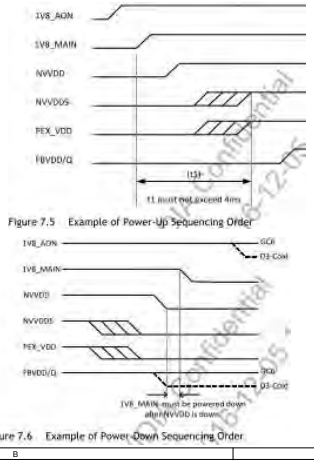


Figure 7.5 Example of Power-Up Sequencing Order

Figure 7.6 Example of Power-Down Sequencing Order

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Table 3-4. GPU Core Sensing Line Routing Constrains

Constraint Parameter	Requirement
Single-ended impedance	25 Ω ± 10%
Differential Trace Impedance	50 Ω ± 15%
Reference Plane	GND Reference
Routing Type	Stripline[1] or Microstrip
Dielectric spacing	Stripline: ≥ 3.0x dielectric Microstrip: ≥ 4.0x dielectric
Intrapair skew	≤ 5 ps
Via stub	
Trace length	GPU to R_S/R_G ≤ 250 mm (9842.5 mil) R_S/R_B to VR ≤ 50 mm (1968.5 mil)

Note:
1. Stripline is recommended to minimize EMI. Do not route over any voids.

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

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Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population N16	Population N17	Location
PLLVDD (N17: XS_PLLVDD) Supply Rail					
GB2B-64, GB2C-64	0.1 µF X7R	0402	1	1	Under GPU
	22 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=30 Ω (ESR=0.05 Ω)	0402	1	0	Near GPU
SP_PLLVDD and VID_PLLVDD Combined Supply Rails					
GB2B-64, GB2C-64	0.1 µF X7R	0402	2	2	Under GPU
	10 µF X5R	0603	1	0	Near GPU
	47 µF X5R	0805	1	0	Near GPU
	Bead Type				
	L2=300 Ω (ESR=0.2 Ω)	0603	1	0	Near GPU
NC (N17: GPCPLL_AVDD) Supply Rail					
GB2C-64	0.1 µF X7R	0402	N/A	1	Under GPU
	4.7 µF X5S	0603	N/A	1	Near GPU
	22 µF X6S	0805	N/A	1	Near GPU
	Bead Type				
	L=30 Ω (ESR=0.01Ω)	0603	N/A	1	Near GPU

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Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

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Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 μF	X7R	0402	2	0	Under GPU
	1 μF	X7R	0603	2	8	Under GPU
	4.7 μF	X6S	0603	2	0	Under GPU
	10 μF	X6S	0603	0	2	Under GPU
	10 μF	X6S	0603	1	1	Near GPU
	22 μF	X6S	0603W	1	3	Near GPU

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Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply

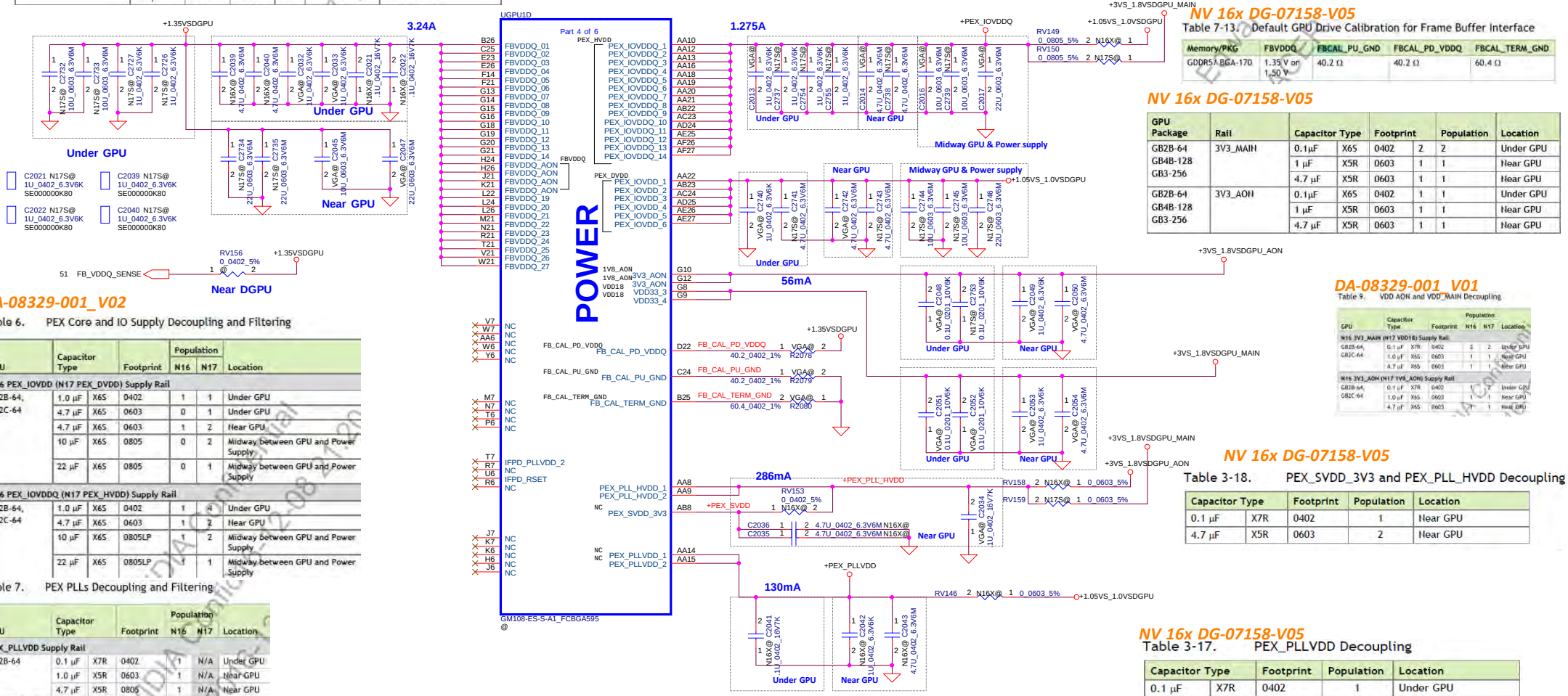

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Table 7-13. Default GPU Drive Calibration for Frame Buffer Interface

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
GDDR5 / BGA-170	1.35 V or 1.50 V	40.2 Ω	40.2 Ω	60.4 Ω

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GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1μF	X6S	0402	2	2	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

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Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 μF	X6S	0402	1	1	Under GPU
	4.7 μF	X6S	0603	0	1	Under GPU
	4.7 μF	X6S	0603	1	2	Near GPU
	10 μF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 μF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 μF	X6S	0402	1	4	Under GPU
	4.7 μF	X6S	0603	1	2	Near GPU
	10 μF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 μF	X6S	0805LP	1	1	Midway between GPU and Power Supply

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
PEX_PLLVDD Supply Rail						
GB2B-64	0.1 μF	X7R	0402	1	N/A	Under GPU
	1.0 μF	X5R	0603	1	N/A	Near GPU
	4.7 μF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail						
GB2B-64	4.7 μF	X5R	0603	2	N/A	Near GPU
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 μF	X7R	0402	1	1	Near GPU

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Table 9. VDD AON and VDD_MAIN Decoupling

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Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μF	X7R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

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Table 3-17. PEX_PLLVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μF	X7R	0402	1	Under GPU
1.0 μF	X5R	0603	1	Near GPU
4.7 μF	X5R	0805	1	Near GPU

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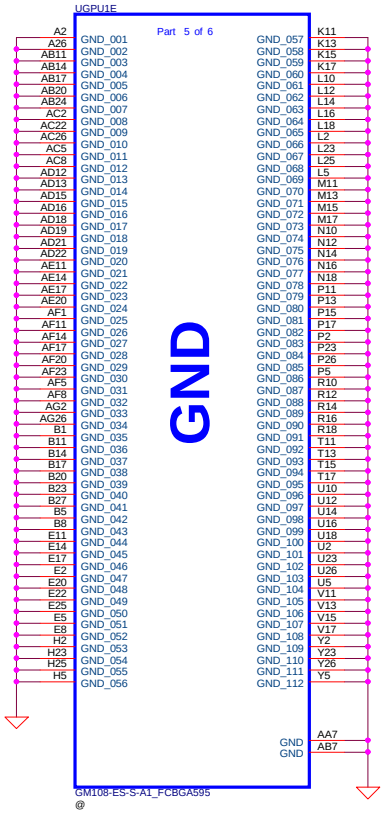

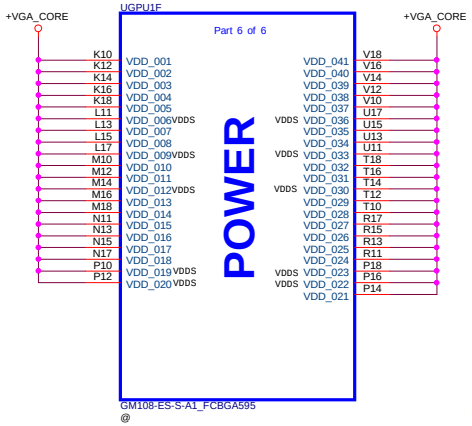

NV 16x DG-07158-V05

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64 / GB2-64	4.7 µF	X6S	0603	10	10	Under GPU	
	1 µF	X6S	0402	4	4	Under GPU	
	47 µF	X5R	0805	1	1	Near GPU	
	22 µF	X5R	0805	1	1	Near GPU	
	4.7 µF	X5R	0805	5	5	Near GPU	
	330 µF	POS	7343	1	1	Near GPU	ESR ≤ 6 mΩ

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Table 3. NVVDD and NVVDDS Decoupling and Filtering

GPU	Capacitor Type		Footprint	Population N16	Population N17	Location
NVVDD Supply Net						
GB2B-64, GB2C-64	4.7 µF	X6S	0603	10	8	Under GPU
	1 µF	X6S	0402	4	3	Under GPU
	47 µF	X5R	0805	1	-	Near GPU
	10 µF	X7R	0805	-	4	Near GPU
	22 µF	X5R	0805	1	3	Near GPU
	4.7 µF	X5R	0805	1	4	Near GPU
	330 µF	POS	7343	1	1	Near GPU
NVVDDS Supply Net						
GB2C-64 Only	4.7 µF	X6S	0603	N/A	4	Under GPU
	1 µF	X6S	0402	N/A	2	Under GPU
	10 µF	X6S	0805	N/A	7	Near GPU
	22 µF	X6S	0805LP	N/A	1	Near GPU
	330 µF	POS	7343	N/A	1	Near GPU

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Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core — (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)	3.3V Total 3.3V [4] (A)
N16S-GMR	GDDR5	19.0	–	2.0	–	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	–	2.0	–	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	–	2.0	–	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core — (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)
N16S-GMR	GDDR5	34.0	–	2.9	–	6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	–	2.9	–	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	–	3.1	–	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1

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Table 5. EDP-Continuous [3]

Product	VRAM Type	GPU Core — (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [2] 1.05V [4] (A)	3.3V Total 3.3V [4] (A)
N16V-GMR1	GDDR5 @ 2.0 GHz	18.5	–	2.0	–	4.2	0.8	0.06
	GDDR5 @ 2.5 GHz	18.5	–	2.0	–	4.7	0.8	0.06
	DDR3/L	19.0	1.4	1.4	2.4	2.3	0.8	0.06

Table 6. EDP-Peak [3]

Products	VRAM Type	GPU Core — (A)	GPU FBIO 1.5V [4] (A)	GPU FBIO 1.35V [4] (A)	FB Total [1,5] 1.5V [4] (A)	FB Total [1,5] 1.35V [4] (A)	1.05V Total [4] 1.05V [4] (A)
N16V-GMR1	GDDR5 @ 2.0 GHz	30.0	–	2.9	–	6.8	2.1
	GDDR5 @ 2.5 GHz	31.0	–	3.1	–	7.2	2.1
	DDR3/L	28.5	2.6	2.3	4.1	3.9	2.1

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Table 7. Output EDP-Continuous

Product	NVVDD — (A)	GPU FBIO 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-G1	30.0	2.0	3.4	0.1	0.3

Table 8. Output EDP-Peak

Product	NVVDD — (A)	GPU FBIO 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-G1	60.1	3.2	6.6	0.2

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Title	N16X POWER & GND 5/9
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VRAM GDDR5 chips

22,27 MDA[63..0] → MDA[63..0]

22,27 CMDA[31..0] → CMDA[31..0]

X76 for N16X 2G VRAM

- ZZZ X7604@ — Samsung_256Mx32x2 X76739BOL04
- ZZZ X7605@ — Hynix_256Mx32x2 X76739BOL05
- ZZZ X7606@ — Micron_256Mx32x2 X76739BOL06

X76 for N17S 2G VRAM

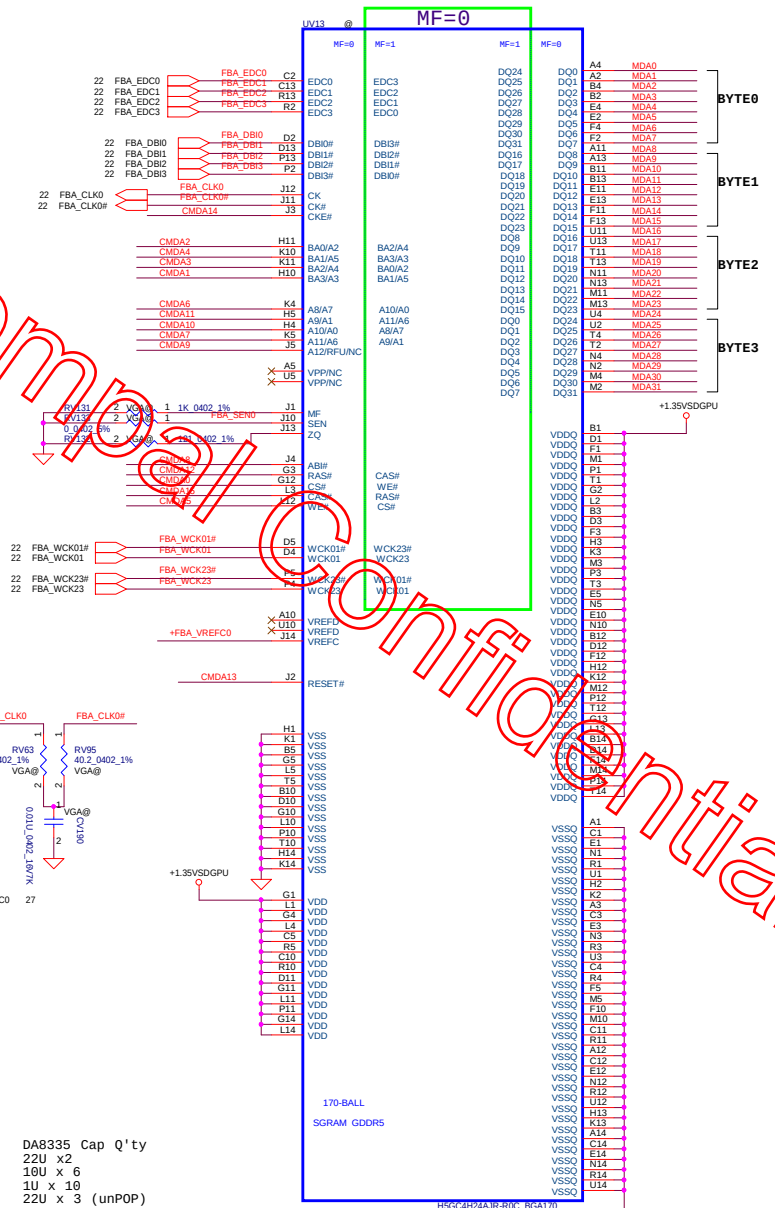
DVT 02/07

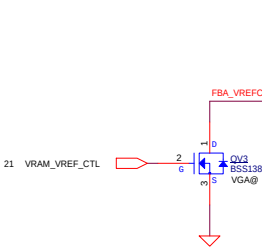
- ZZZ X7607@ — Samsung_256Mx32x2 X76739BOL07
- ZZZ X7608@ — Hynix_256Mx32x2 X76739BOL08
- ZZZ X7609@ — Micron_256Mx32x2 X76739BOL09

GDDR5 Mode H Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

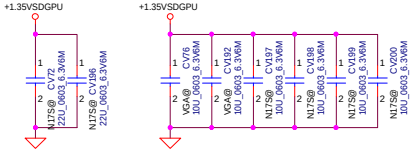
Channel 0 BOT SIDE

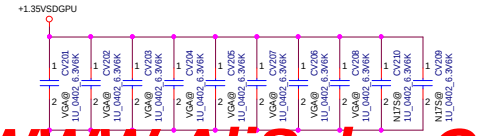


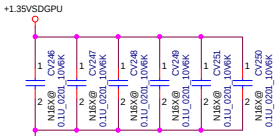


DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

N16X Cap Q'ty
10U x2
1U x 8
0.1U x 6







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VRAM GDDR5 chips

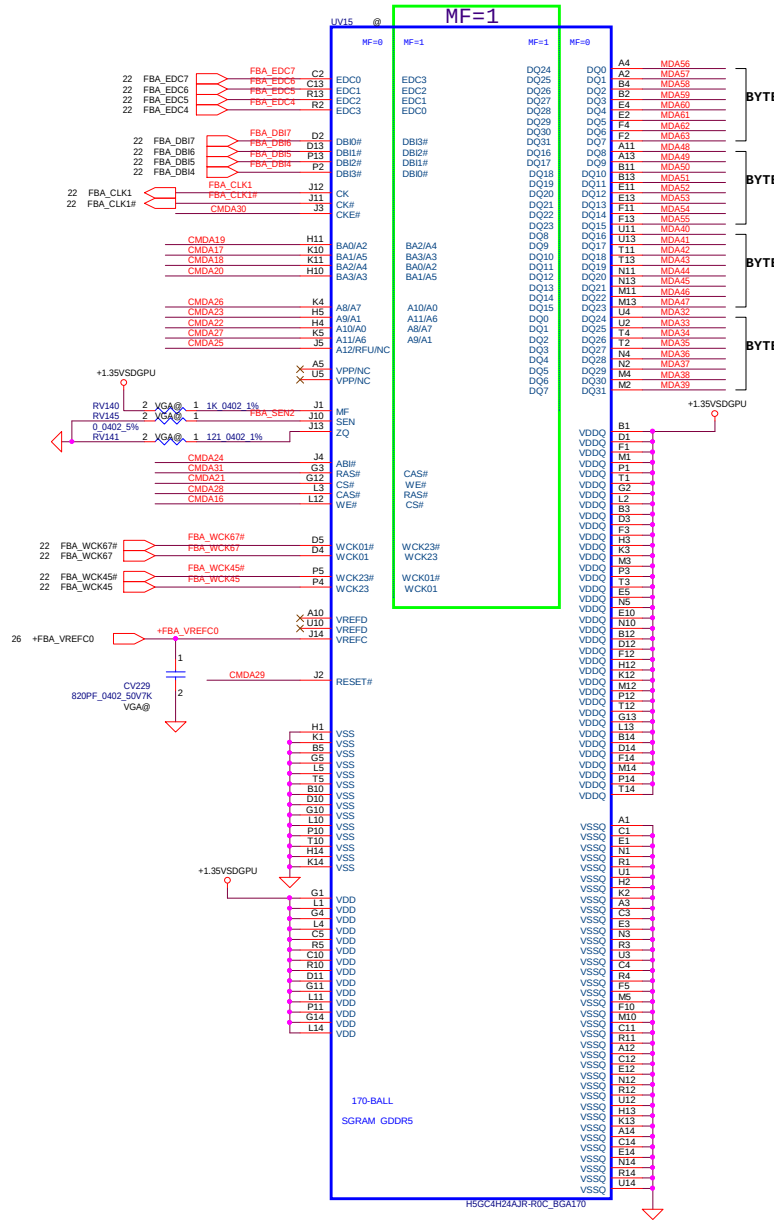
22,26 MDA[63..0] — MDA[63..0]

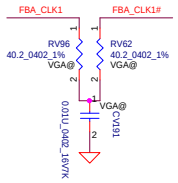
22,26 CMDA[31..0] — CMDA[31..0]

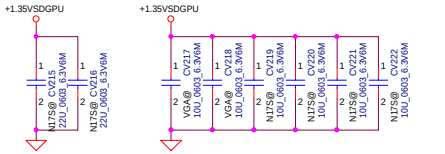
GDDR5 Mode H Mapping

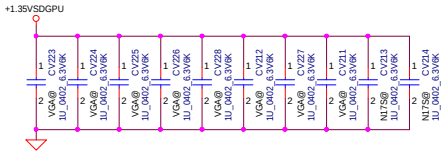
	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

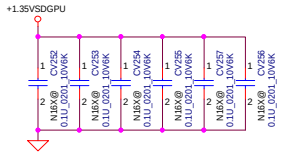
Channel 1 BOT SIDE











DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

N16X Cap Q'ty
10U x2
1U x 8
0.1U x 6

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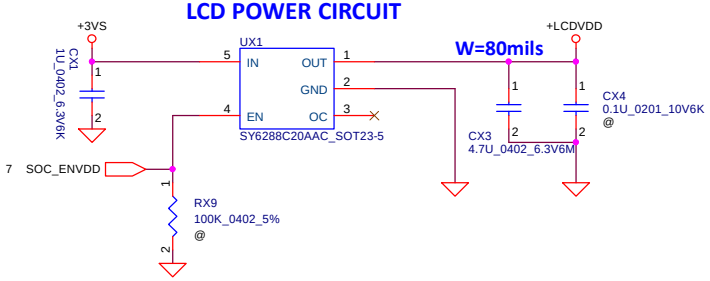
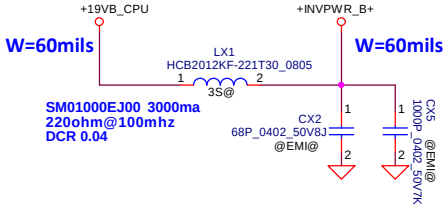
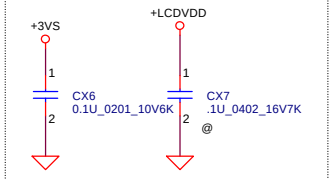
LCD POWER CIRCUIT

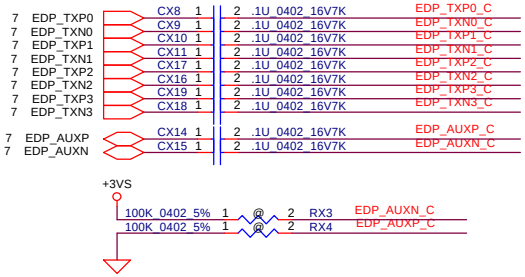


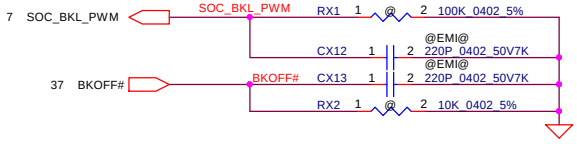


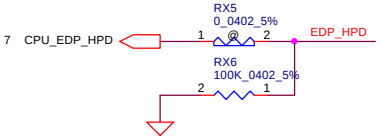
Note: Unmount LX1 when panel boost circuit was use. (2S battery cell)

Place closed to JEDP1

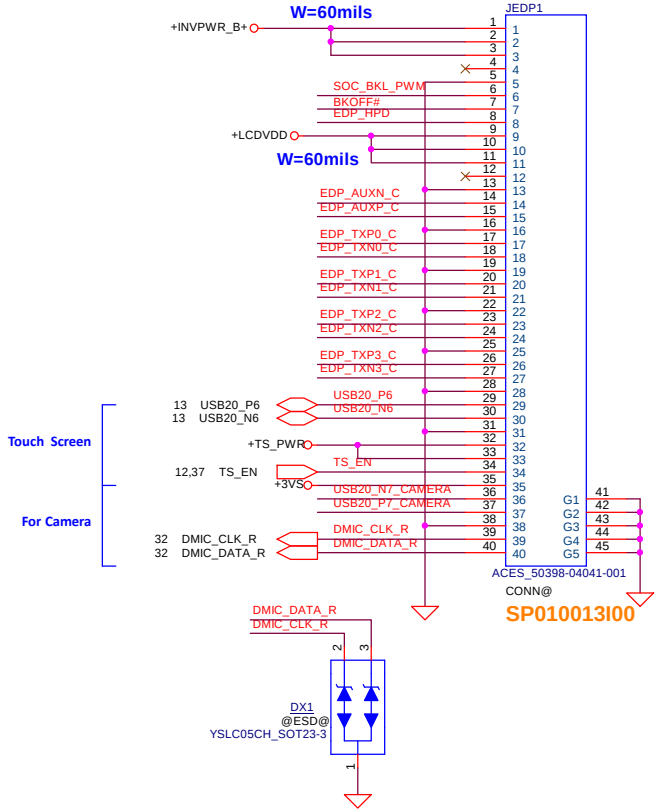




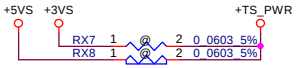




LED PANEL Conn.



Touch Screen



Camera

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: eDP Connector

Size	Document Number	Rev
Custom	C5V01 M/B LA-E892P	1.A

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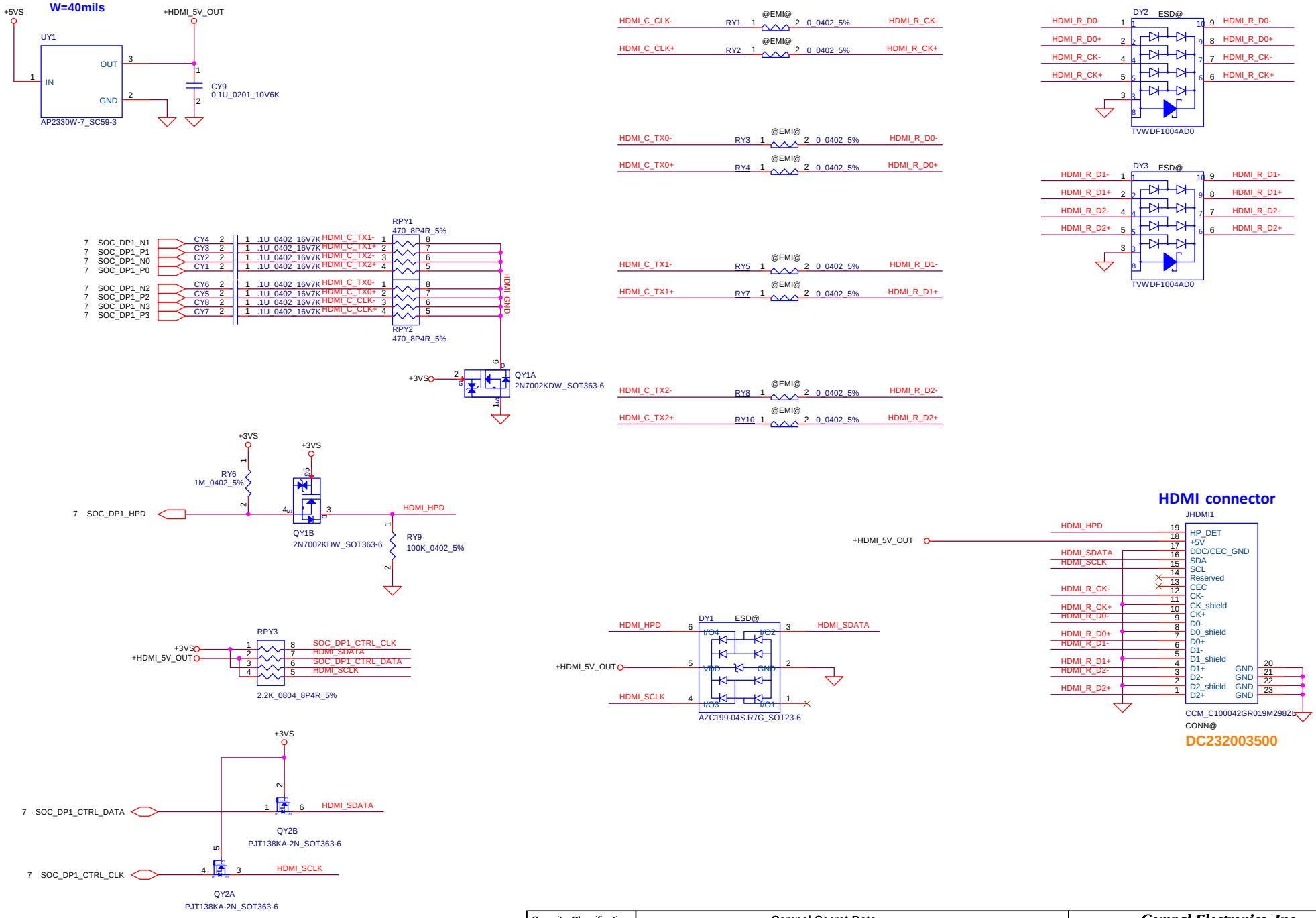

Intel spec Ron/Cout : 3ohm/10pF.
SB000016K00, S TR PJT138KA 2N SOT363-6

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: **HDMI CONN.**

Size: Custom | Document Number: **C5V01 M/B LA-E892P** | Rev: 1.A

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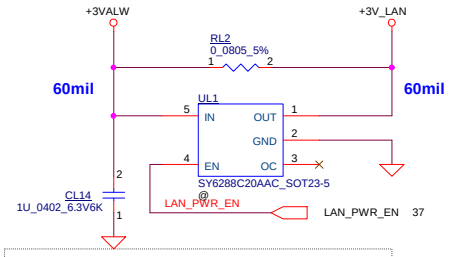
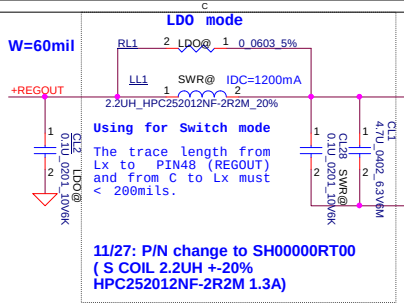
LAN-RTL8411B

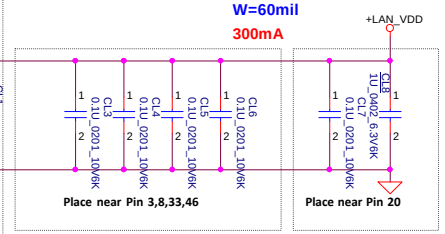


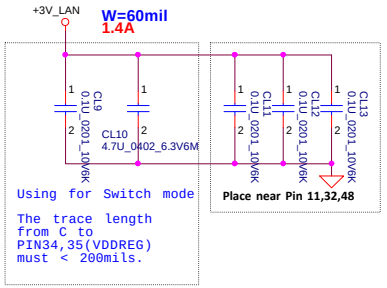
From EC

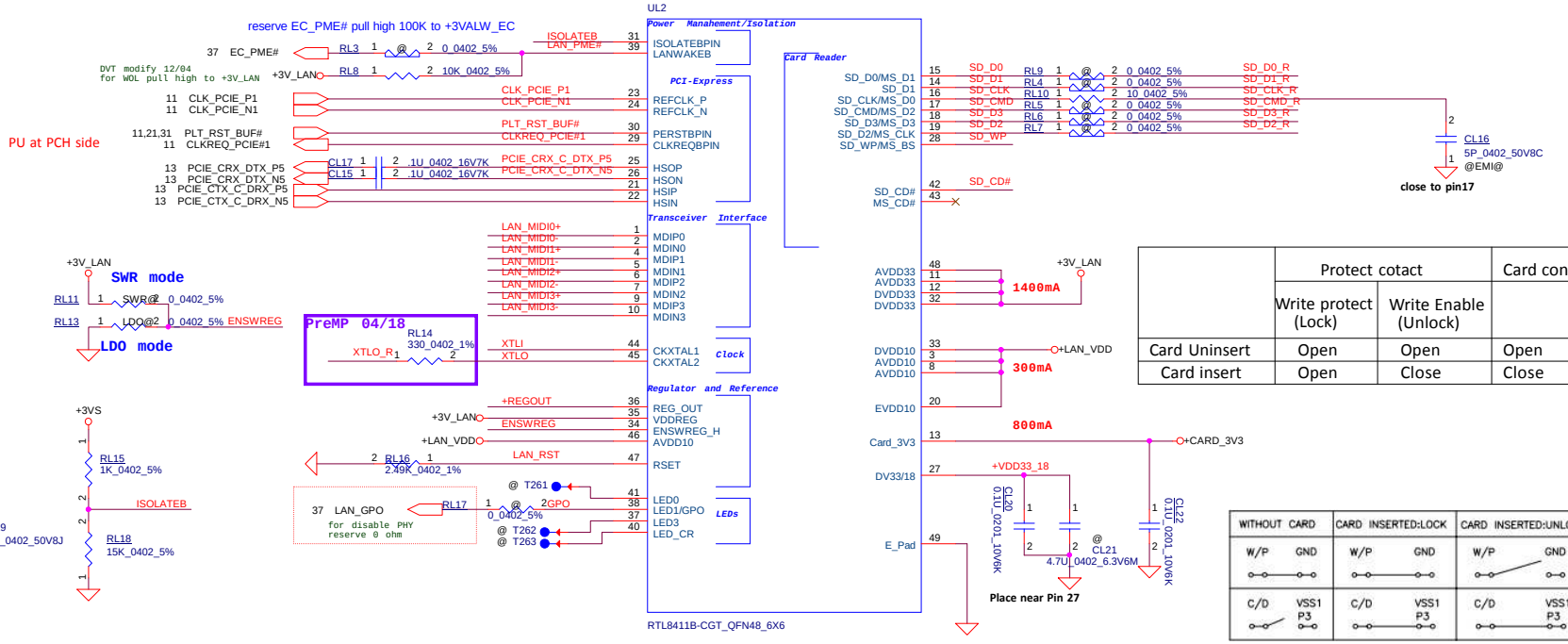
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A

+3V_LAN Rising time must >0.5ms and <100ms



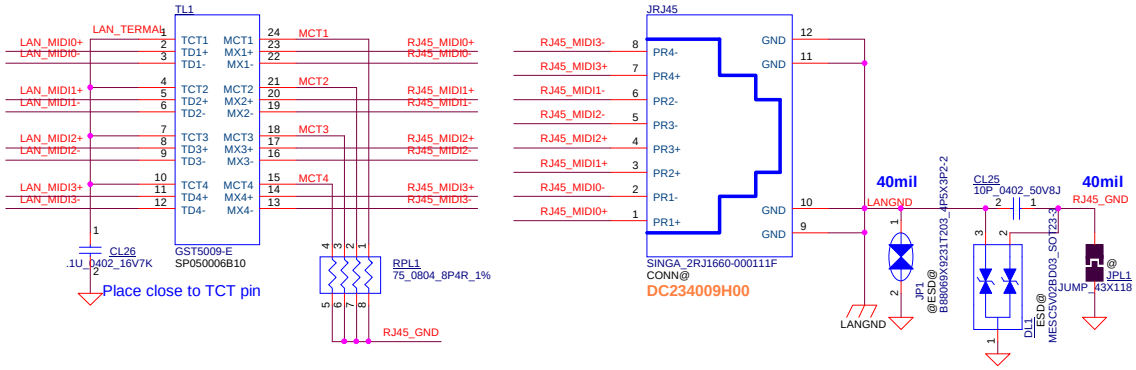




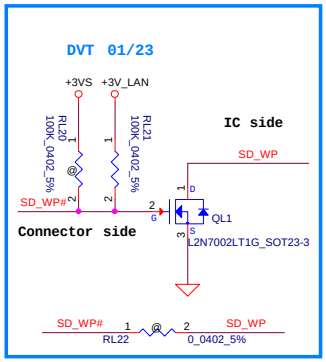


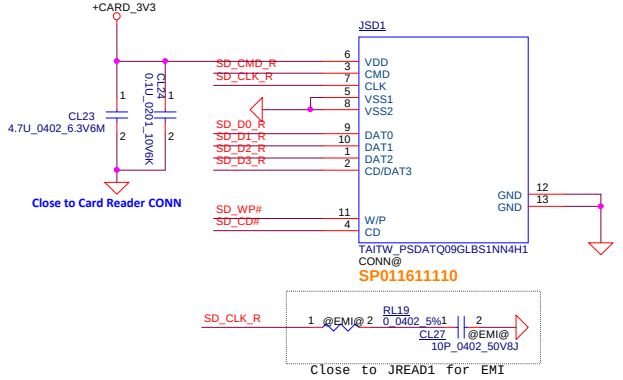
	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

LAN Connector



SD Write protect inverter circuit





Card Reader Connector

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: LAN RTL8411B

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

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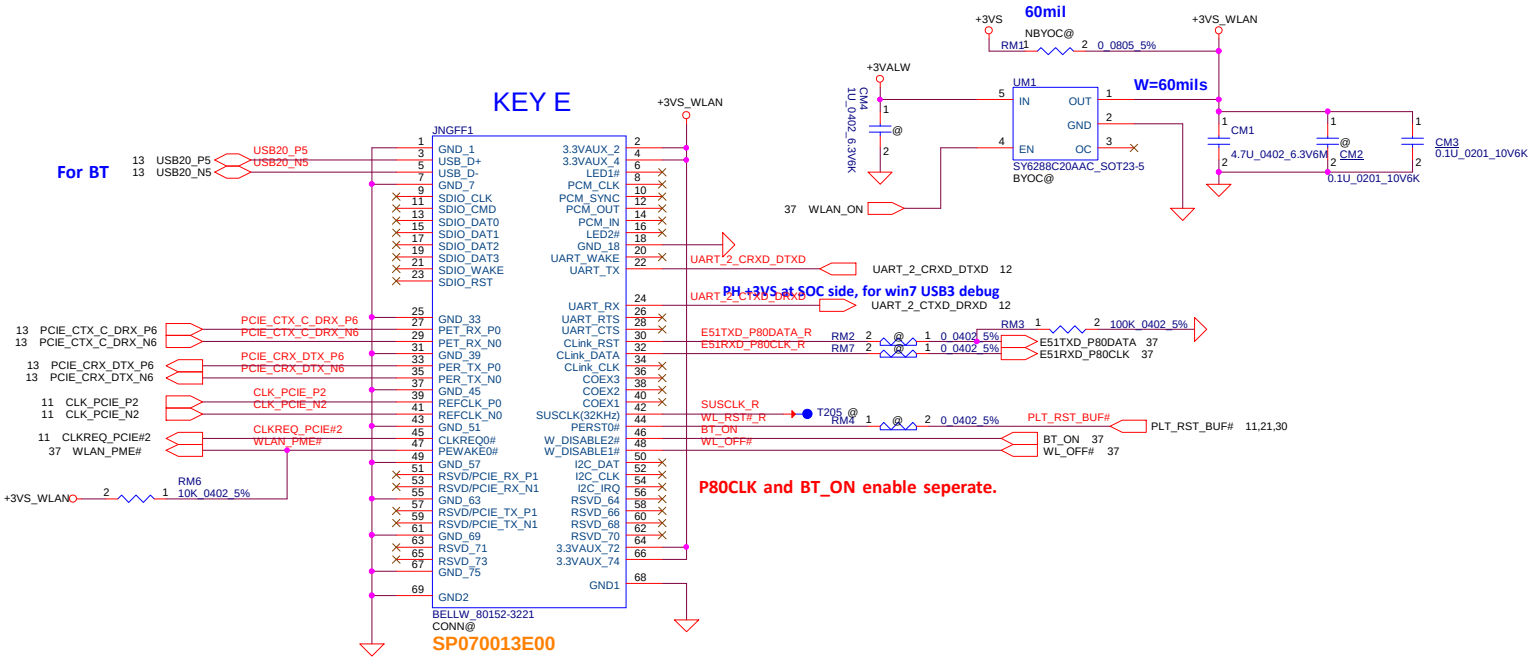
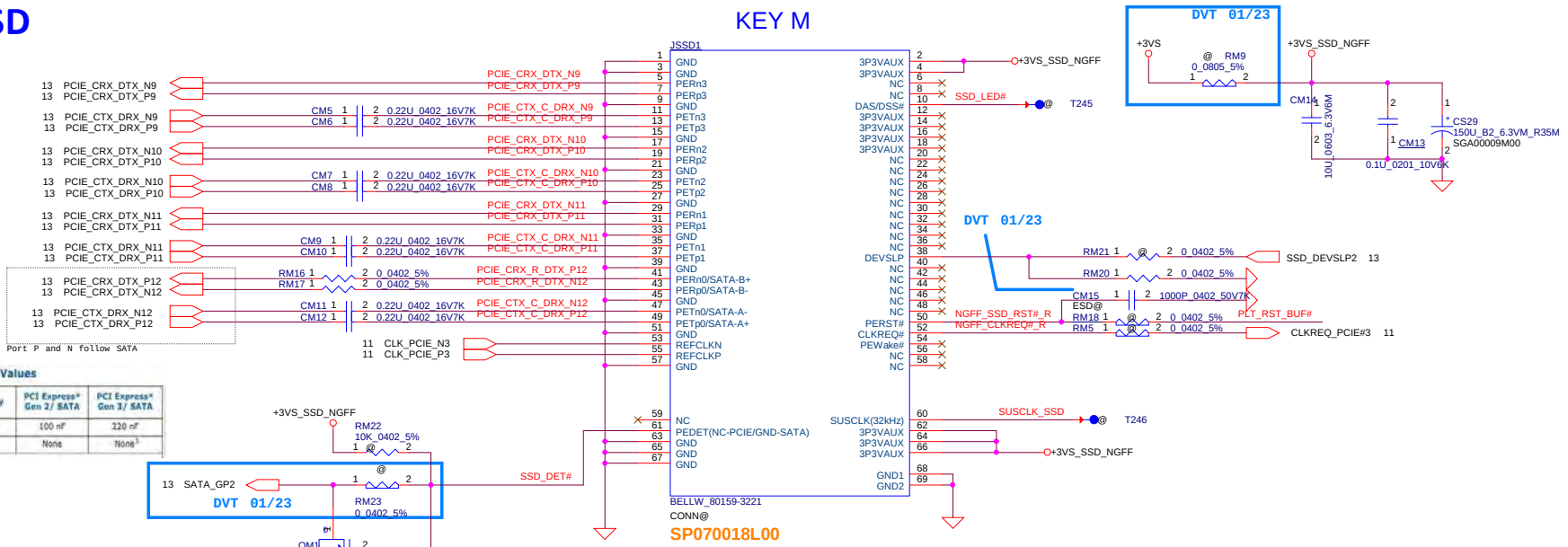
Wireless LAN

NGFF WL+BT (KEY E)



mSATA/SSD



PETp0/SATA-A+	49
PETn0/SATA-A-	47
GND	45
PERp0/SATA-B-	43
PERn0/SATA-B+	41

Port P and N follow SATA

Table 35-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

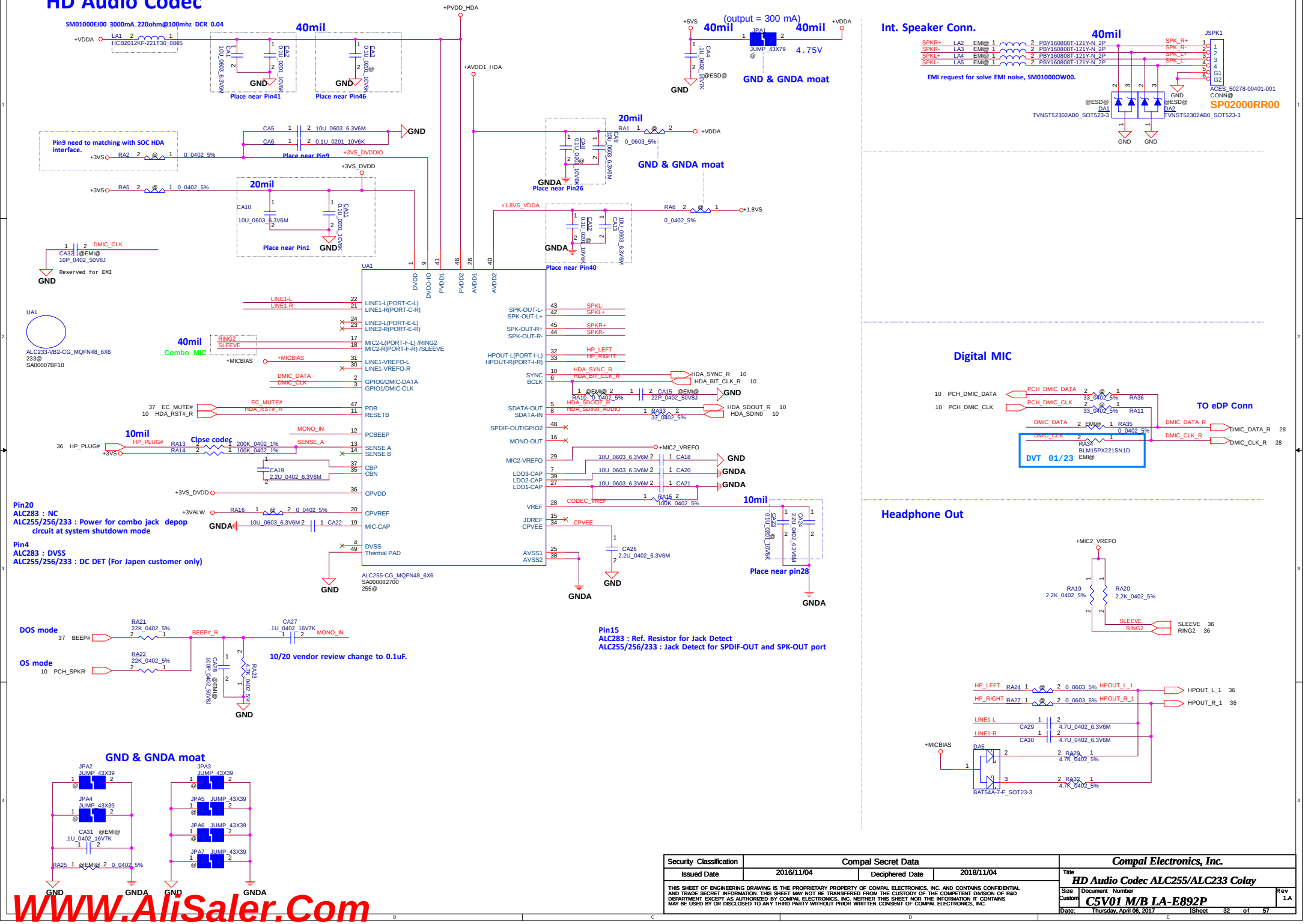
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

SSD_DET# (SATA_GP0)
SATA Device 0
PCIE Device 1

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.	
Title	M.2 Key E (WLAN)/Key M(SSD)
Size: Custom	Document Number: C5V01 M/B LA-E892P
Rev: 1.A	
Date: Thursday, April 06, 2017	Sheet 31 of 57

HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: HD Audio Codec ALC255/ALC233 Colay

Size	Document Number	Rev
Custom	C5V01 M/B LA-E892P	1.A

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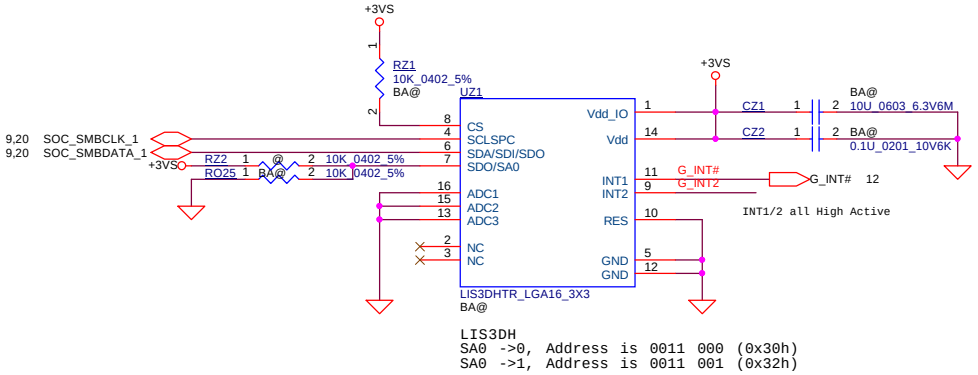
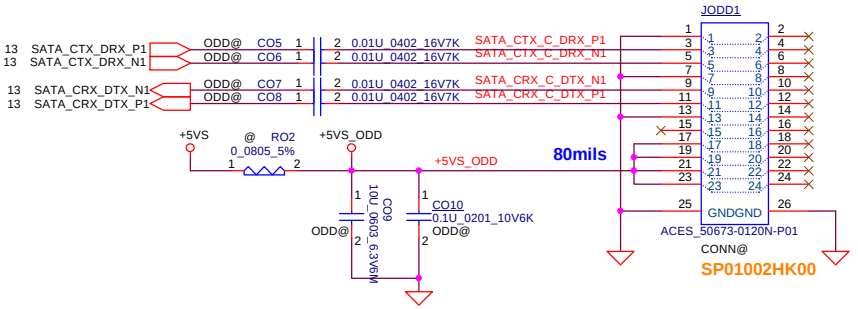
G-Sensor reserved for BA serial

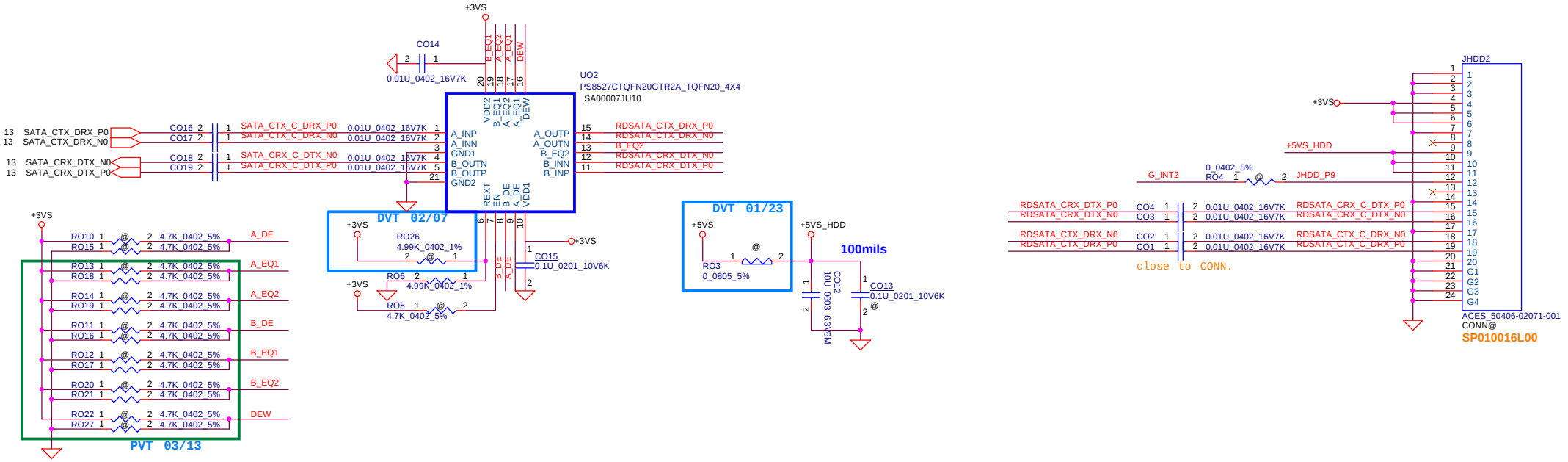


LIS3DH
SA0 ->0, Address is 0011 000 (0x30h)
SA0 ->1, Address is 0011 001 (0x32h)

SATA ODD Conn.
(Reserved)



SATA Re-Driver and cable HDD Conn.



PS8527C EQ and DE

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
* L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

A_DE	De_Emphasis
* M	-3.5dB(Default)
L	0dB
H	-6dB

Compal Electronics, Inc.

Title: HDD/ODD/ HDD Re-Driver

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

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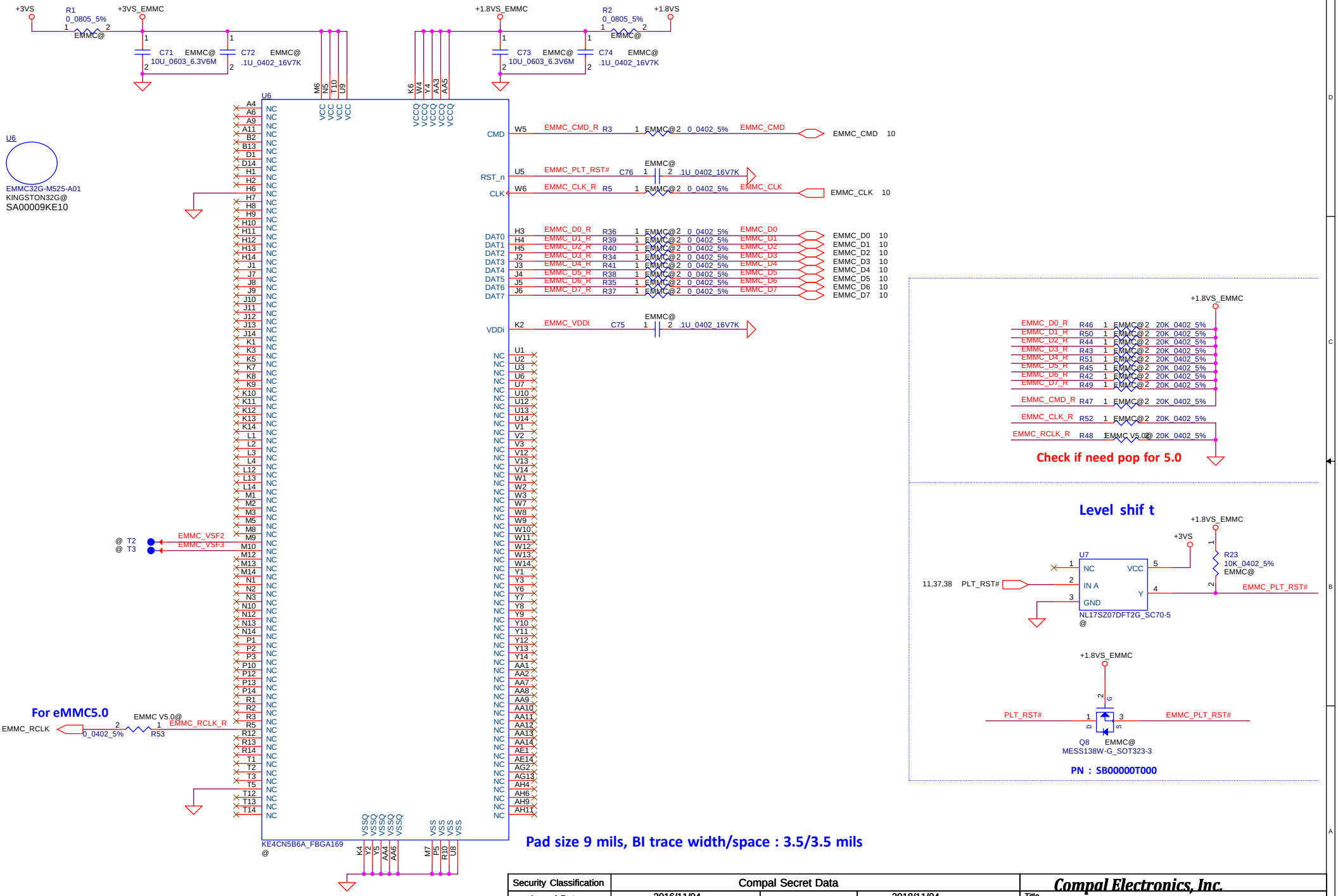

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Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: EMMC STORAGE

Size	Document Number	Rev
Custom	C5V01 M/B LA-E892P	1.A

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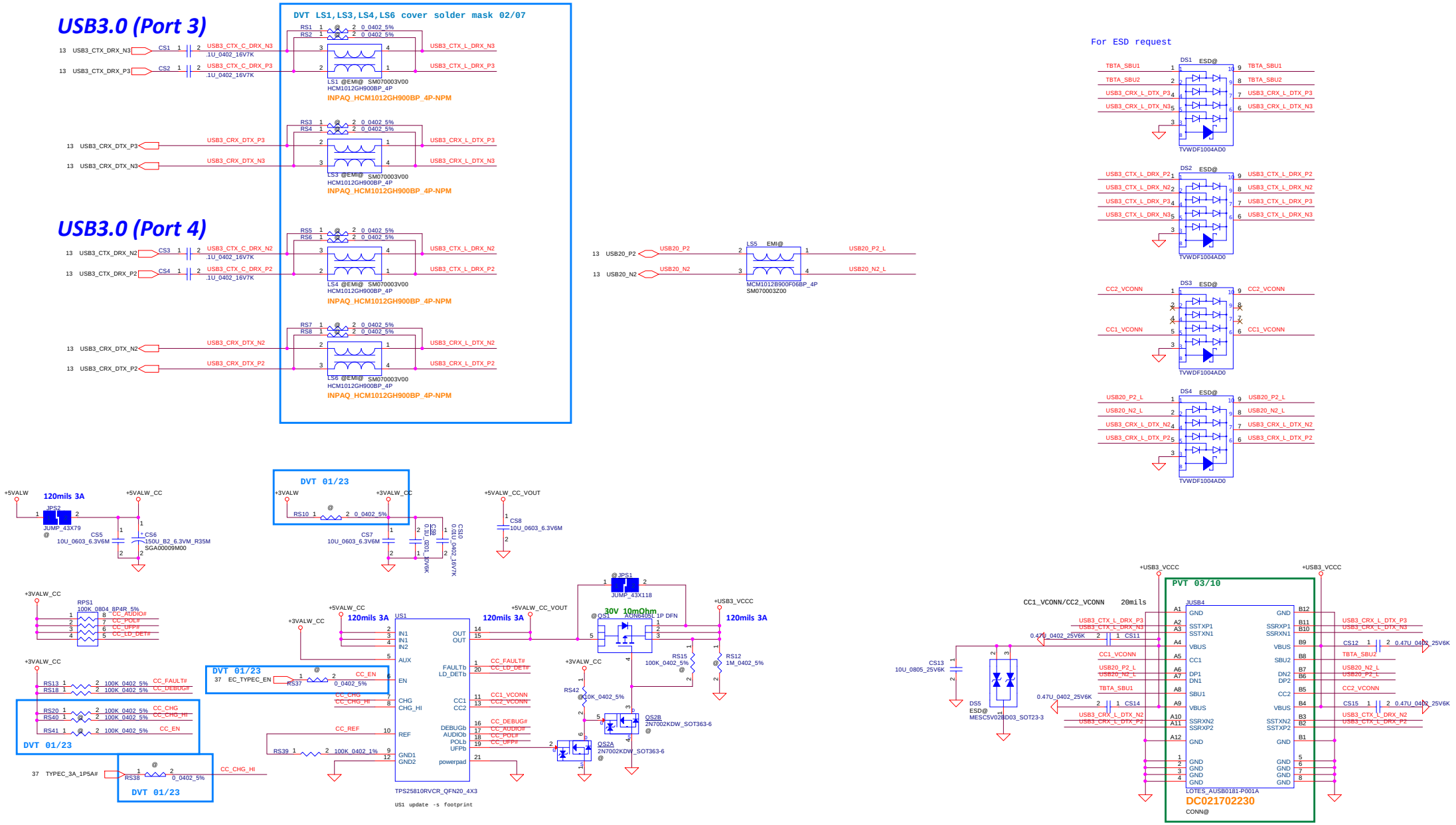

Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

EC_TYPEC_EN	S0	S3	S5
AC Mode (Adapter In)	On	On	Off
DC Mode (Battery Only)	On	On[1]	Off

Note 1: Stop charge current when the battery capacity is below a specified percentage.

Note : 2017 BIOS SPEC define DC mode 30% stop charge

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: CC+USB TYPE C

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

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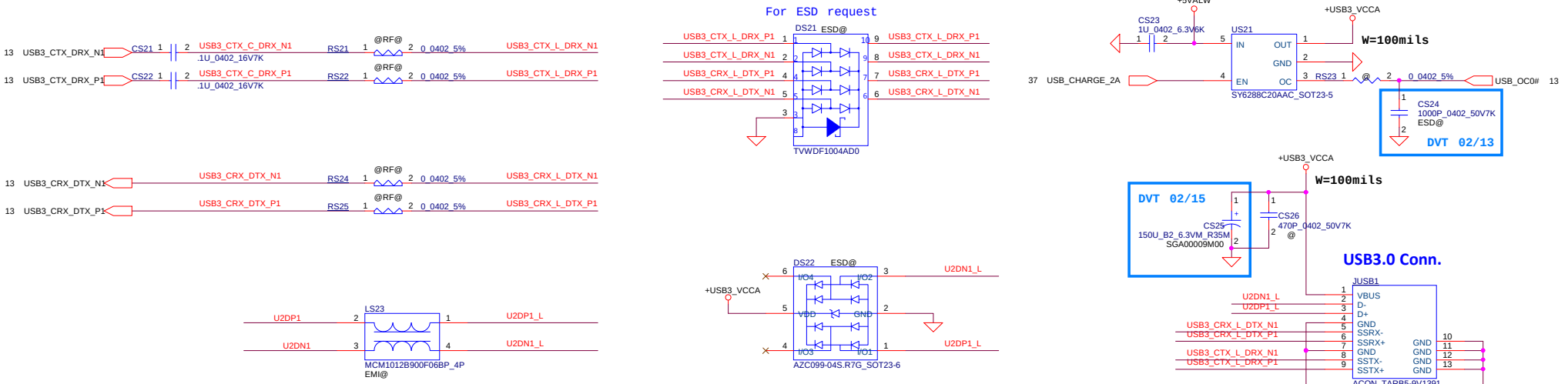
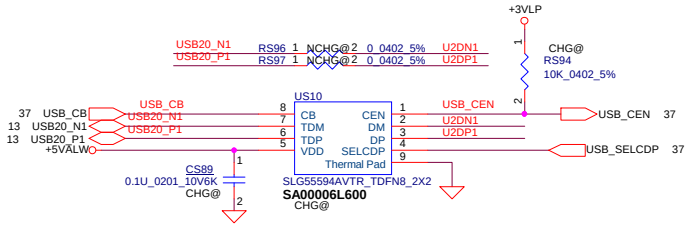
USB3.0 (Port 1)

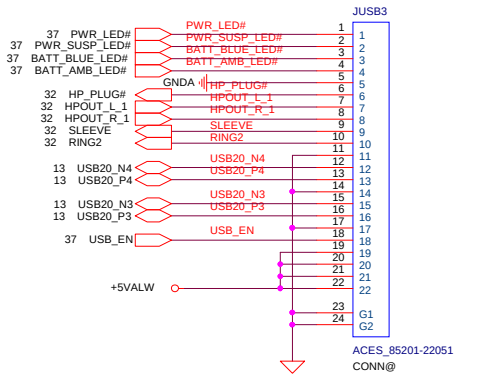


USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



USB/B (USBx2, AUDIO, LEDx2)



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: **USB Conn/USB_B**

Size	Document Number	Rev
Custom	C5V01 M/B LA-E892P	1.A

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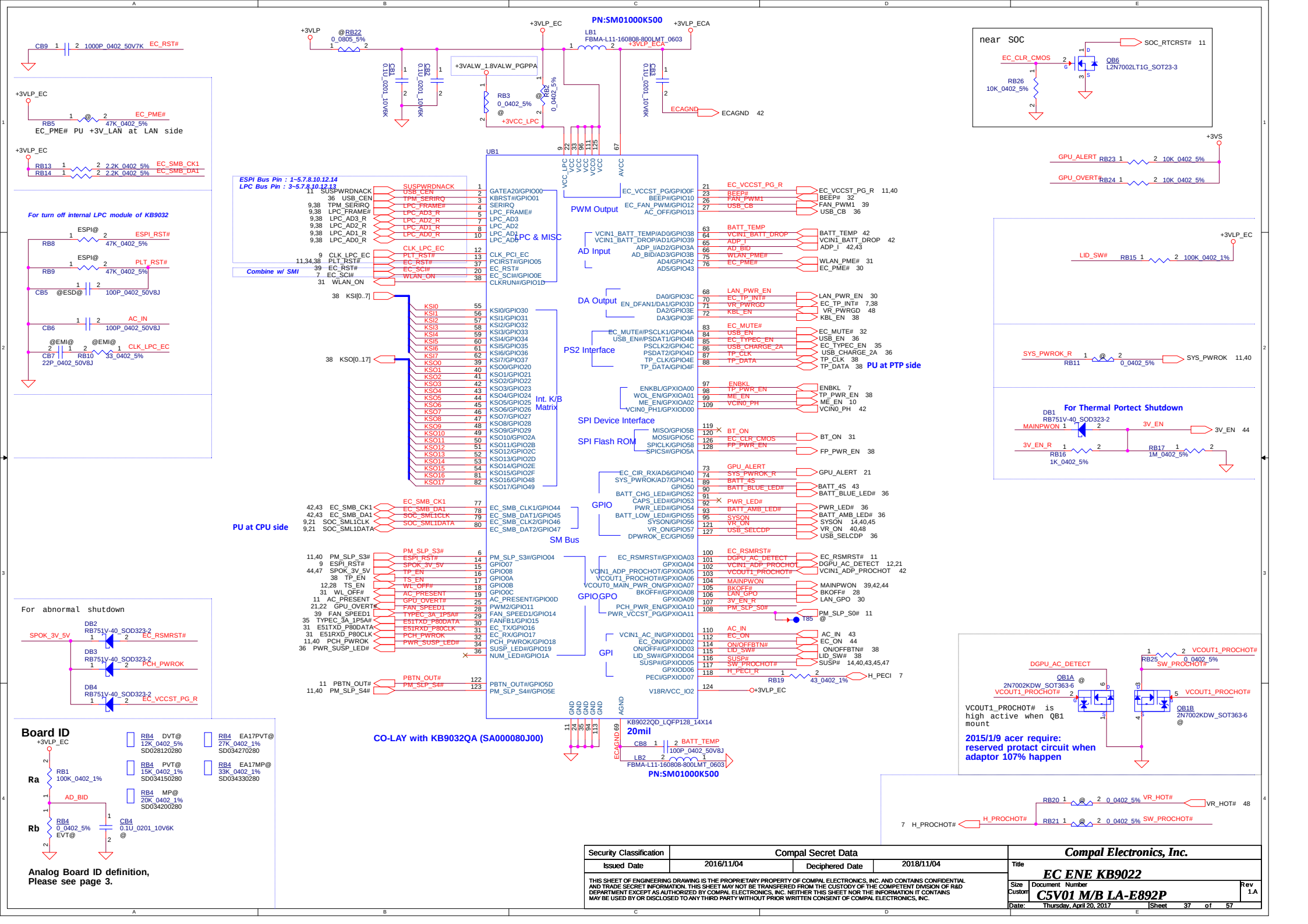
PN:SM01000K500
UB1
KB9022QD_LQFP128_14X14
20mil
CO-LAY with KB9032QA (SA000080J00)
ESPI Bus Pin : 1~5,7,8,10,12,14
LPC Bus Pin : 3~5,7,8,10,12,13
Combine w/ SMI
PWM Output
LPC & MISC
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
PU at CPU side
PU at PTP side
For turn off internal LPC module of KB9032
For abnormal shutdown
EC_PME# PU +3V_LAN at LAN side
near SOC
For Thermal Portect Shutdown
VCOUT1_PROCHOT# is high active when QB1 mount
2015/1/9 acer require: reserved protact circuit when adaptor 107% happen
Board ID
Analog Board ID definition, Please see page 3.
Security Classification
Compal Secret Data
Issued Date
2016/11/04
Deciphered Date
2018/11/04
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Size
Custom
Document Number
C5V01 M/B LA-E892P
Rev
1.A
Date:
Thursday, April 20, 2017
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37
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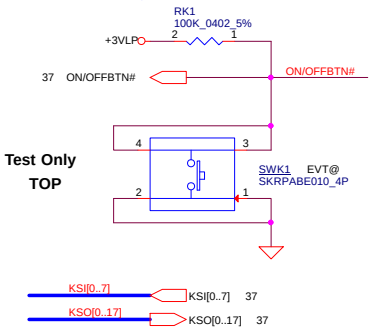
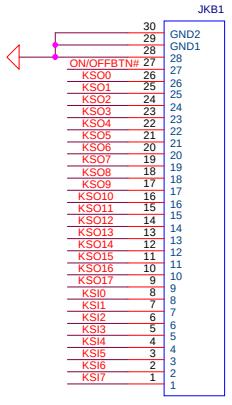
KB Conn.

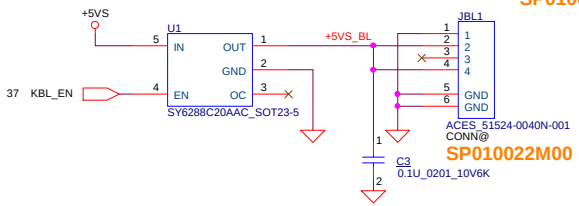
ON/OFF BTN





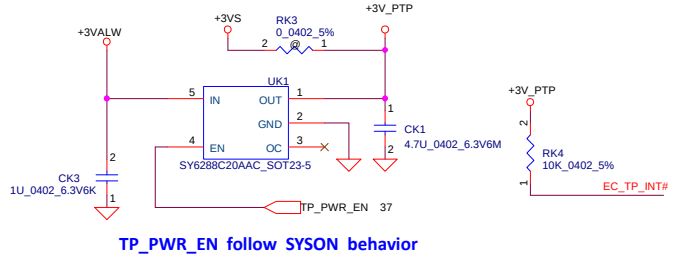
SP01000GO00

KB BackLight

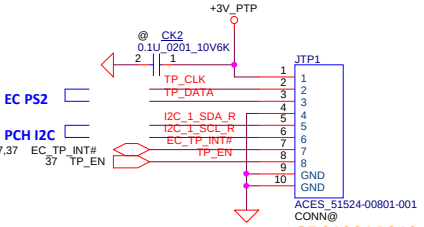


SP010022M00

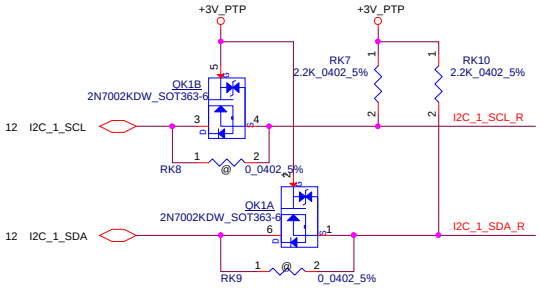
TP/B Conn.

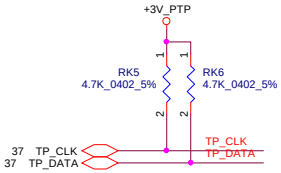


TP_PWR_EN follow SYSON behavior

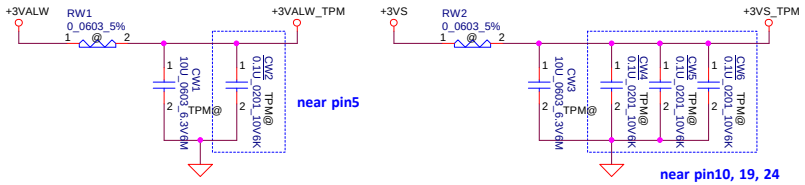


SP01001A910

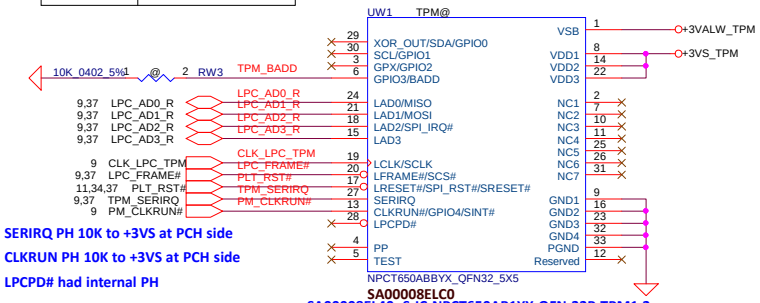




TPM



BADD	SELECTION
* 1	AEh(write), AFh(read)



SERIRQ PH 10K to +3VS at PCH side

CLKRUN PH 10K to +3VS at PCH side

LPCPD# had internal PH

SA00008ELC0

SA00008EL40, S IC NPCT650AB1YX QFN 32P TPM1.2

SA00008ELB0, S IC NPCT650AB2YX QFN 32P TPM1.2 FW 5.81.2.1

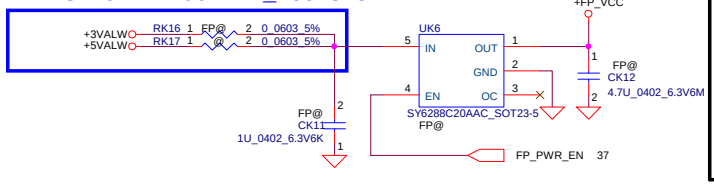
SA00008ELC0, S IC NPCT650ABBYX QFN 32P TPM2.0 FW 1.3.1.0

Finger Print

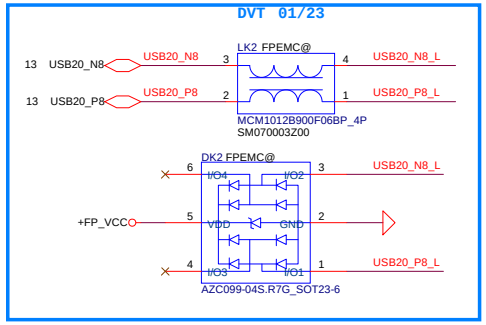
Power Souce Check

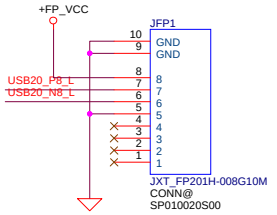
EGIS ETU801 +FP_VCC=5V

ELAN SA464K-2200 +FP_VCC=3.3V



DVT 01/23

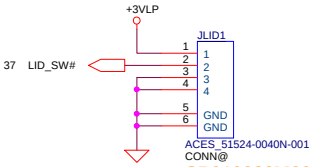




PIN	ETU801	SA464K-2200
1	+FP_VCC(5V)	+FP_VCC(3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

Lid Switch

(Hall Effect Switch)



SP010022M00

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

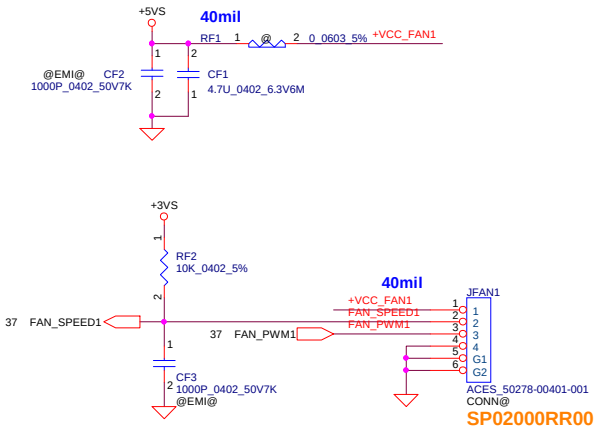
Compal Electronics, Inc.

Title: KB & TP & TPM & LID & FP

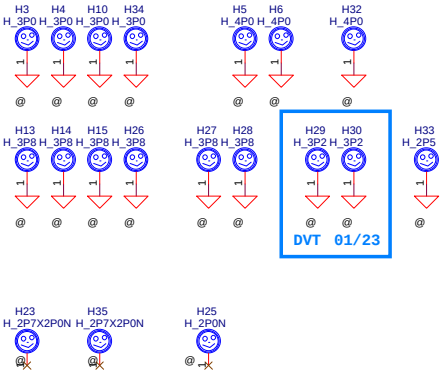
Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 1.A

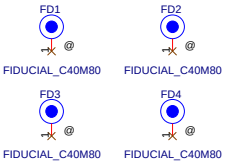
Date: Thursday, April 06, 2017 | Sheet 38 of 57

FAN1 Conn

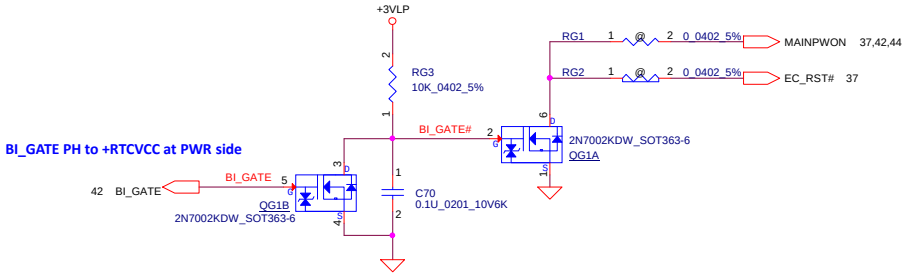


Screw Hole

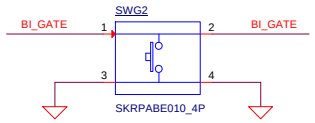




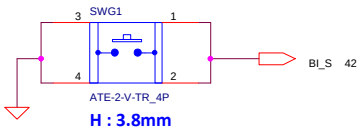
Reset Circuit



Reset Button



BI SW



H : 3.8mm

Release : Battery Off
Push : Battery ON

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

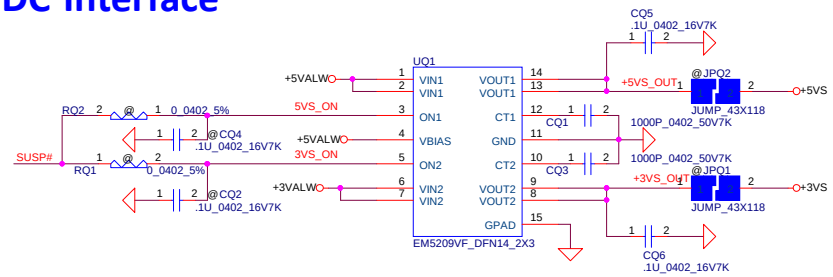
Compal Electronics, Inc.

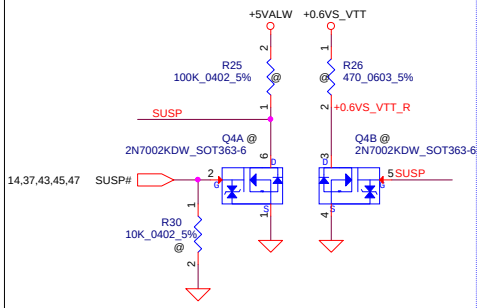
Title: **FAN & Screw Hole & Reset**

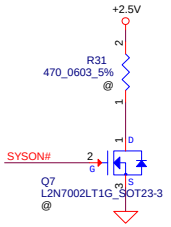
Size	Document Number	Rev
Custom	C5V01 M/B LA-E892P	1.A

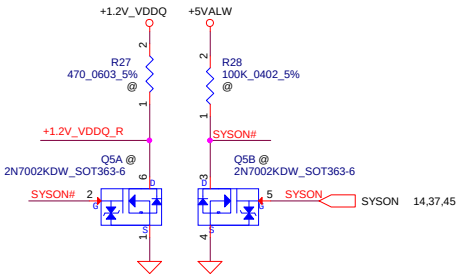
Date: Thursday, April 06, 2017 Sheet 39 of 57

DC Interface

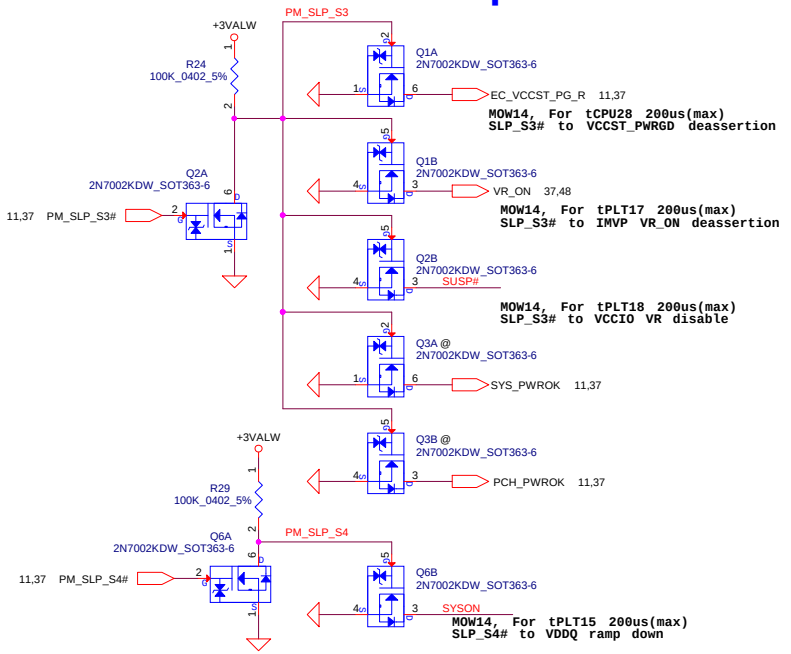


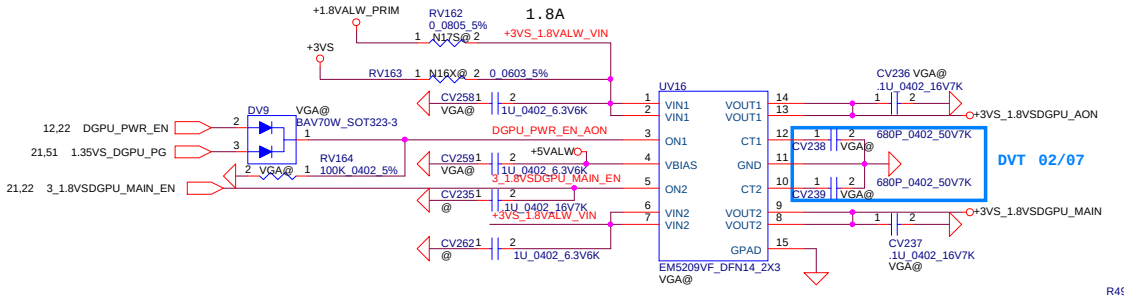


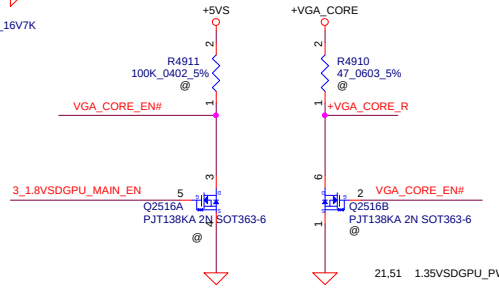


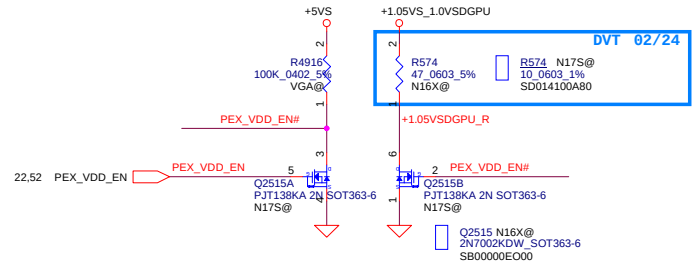


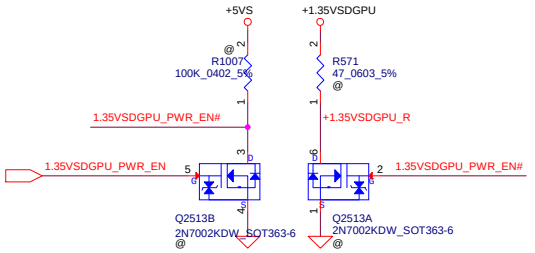
For Power ON/Off Sequence











+3VS to +3VSDGPU_AON for GPU

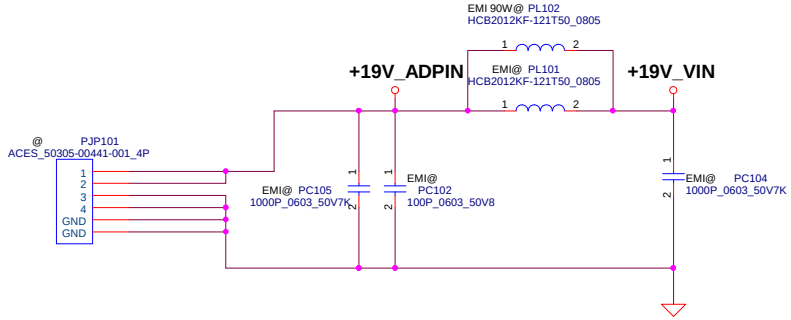
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

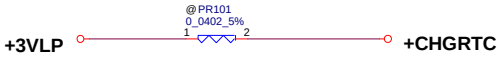
Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	C5V01 M/B LA-E892P	1.A

Date: Thursday, April 06, 2017 Sheet 40 of 57





Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

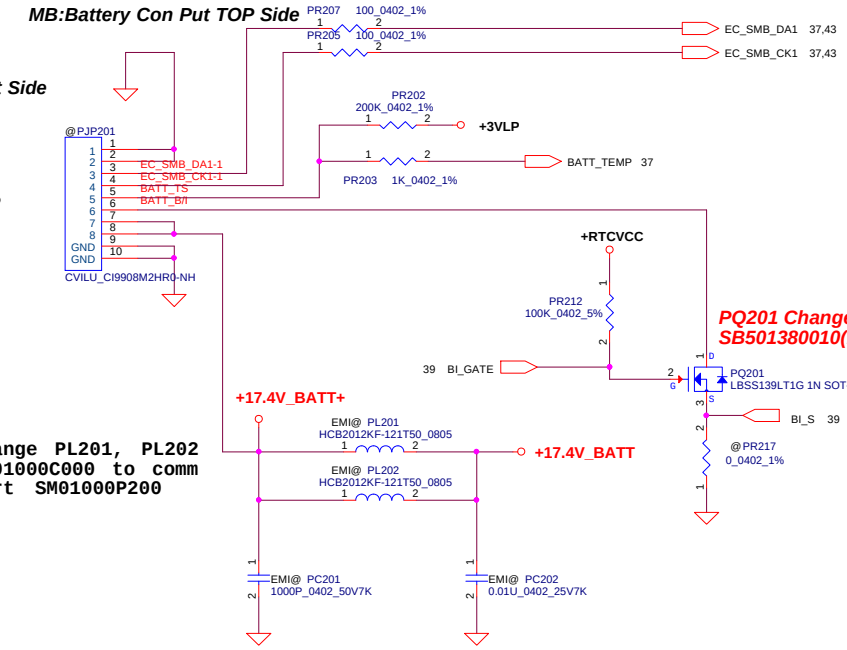
Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 0.1

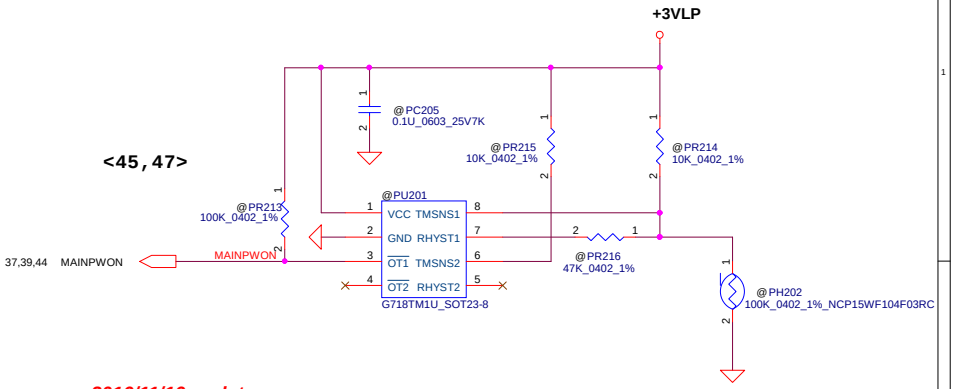
Date: Thursday, April 06, 2017 | Sheet 41 of 57

2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1



change PL201, PL202 SM01000C000 to comm part SM01000P200

PQ201 Change to SB00000QO00, SB501380010(BSS138LT1G Del)



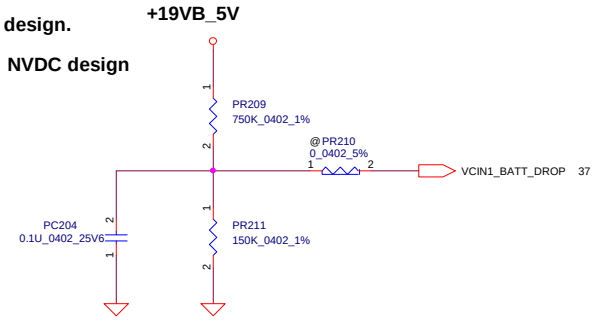
2016/11/16 update

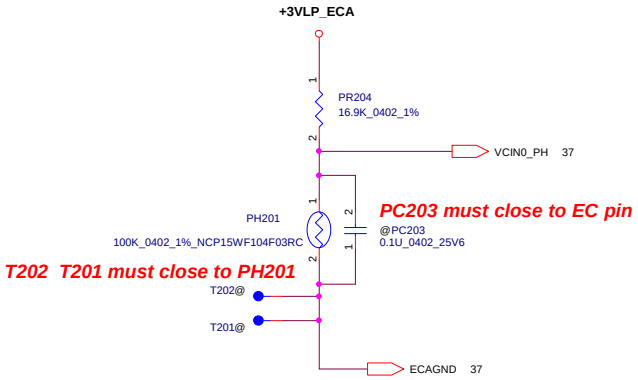
For KB9022 sense 20mΩ	Active	Recovery
45W PR206 10K ohm	58.5W,0.61V	Active=recovery
65W PR206 19.1K ohm	84.5W,0.61V	Active=recovery
90W PR206 30.1K ohm	117W,0.61V	Active=recovery
PH1	2V	1V

PH1 under CPU botten side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C

2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

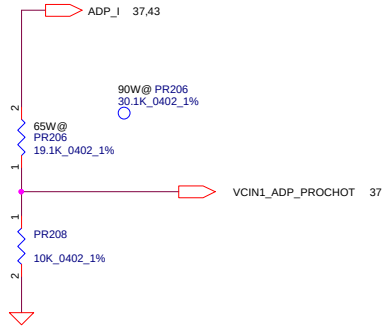
VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V





PC203 must close to EC pin

T202 T201 must close to PH201



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size	Document Number		Rev
Custom	C5V01 M/B LA-E892P		0.1
Date:	Thursday, April 06, 2017	Sheet	42 of 57

Protection for reverse input

Need check the SOA for inrush

Vgs = 20V
Vds = 60V
Id = 250mA

PQ301 2N7002KW_SOT323-3

PR301 1M_0402_5%

PR302 3M_0402_5%

+19V_VIN

PQ302 AON6366E_DFN5X6-8-5

+19V_P1

PQ303 AON7506_DFN33-8-5

+19V_P2

PR303 0.02_1206_1%

EMI@ PL301 5A_Z120_25M_0805_2P

+19VB

+19VB_CHG

PC303 10U_0805_25V6K

PC304 10U_0805_25V6K

PC305 2200P_0402_25V7K EMI@

PC306 0.1U_0402_25V6 EMI@

PQ304 AON7506_DFN33-8-5

PC307 0.01U_0402_50V7K

BQ24725A_BATDRV

BQ24725A_BATDRV_1

PR305 4.12K_0603_1%

PC301 2200P_0402_50V7K

PR304 0_0402_5% @

PC302 0.1U_0402_25V6

BQ24725A_ACDRV_1

PD301 BAS40CW_SOT323-3

VF = 0.5V

PC308 0.1U_0402_25V6

PC309 0.1U_0402_25V6

PC310 0.1U_0402_25V6

PR306 10_1206_1%

PC311 0.047U_0402_25V7K

VF = 0.37V

PD302 RB751V-40_SOD323-2

PR307 2.2_0603_5%

Rds(on) = 30mohm max
Vgs = 20V
Vds = 30V
ID = 7A (Ta=70C)

PQ305 AON7506_DFN33-8-5

5*5*3

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VSRP-VSRN spec < 81.28mV

@PR308 0_0603_5%

DH_CHG

PC312 1U_0603_25V6K

PC313 1U_0603_25V6K

PR309 4.12K_0603_1%

PR310 4.12K_0603_1%

BQ24725A_ACP

BQ24725A_ACN

BQ24725A_VCC

BQ24725A_LX

DH_CHG

BQ24725A_BST

BQ24725A_REGN

PL302 4.7UH_5.5A_20%_7X7X3_M

PR311 0.01_1206_1%

+17.4V_BATT

BQ24725A_LX

CHG

CSOP1

CSON1

PC316 0.1U_0402_25V6

PC317 0.1U_0402_25V6

PC314 10U_0805_25V6K

PC315 10U_0805_25V6K

PC324 10U_0805_25V6K

PQ306 AON7506_DFN33-8-5

PR312 4.7_1206_5% @EMI@

PC318 680P_0402_50V7K @EMI@

PU301 BQ24735RGRR_QFN20_3P5X3P5

PAD VCC PHASE HIDRV BTST REGN

ACN LODRV

ACP GND

CMSRC SRP

ACDRV SRN

ACOK BATDRV

ACDET IOUT SDA SCL ILIM

DL_CHG

PR313 10_0603_1%

PR314 6.8_0603_1%

PC319 0.1U_0603_16V7K

BQ24725A_CMSRC

BQ24725A_ACDRV

BQ24725A_BATDRV

+3VLP

PR315 100K_0402_1%

37 AC_IN

BQ24725A_ACDET

BQ24725A_IOUT

BQ24725A_ILIM

PR324 316K_0402_1%

PR317 100K_0402_1%

PC320 0.01U_0402_25V7K

PR318 422K_0402_1%

+19V_VIN

PC321 2200P_0402_50V7K

PR319 66.5K_0402_1%

PC322 100P_0402_50V8J

PR320 499_0402_1%

EC_SMB_CK1 37,42

EC_SMB_DA1 37,42

ADP_I 37,42

PC323 2.2U_0402_6.3V6M

Close EC chip

For 4S per cell 4.35V battery

BQ24725A_ACDET

PR321 2M_0402_1%

PR322 @ 0_0402_5%

PQ307 LTC015EUBFS8TL_UMT3F

PR323 100K_0402_1%

37 BATT_4S

PQ308 2N7002KW_SOT323-3

14,37,40,45,47 SUSP#

Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+316)/20/0.01
= 3.966 A

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: Common Circuit | Rev: 0.1

Date: Thursday, April 06, 2017 | Sheet 43 of 57

Module model information

RT6575D_DMOS_single_V1.mdd
RT6575D_DMOS_dual_V1.mdd

H/S Rds(on):typ:12.4mOhm, max:15.8mOhm
Idsm(TA=25)=13A, Idsm(TA=70)=7.8A
Ploss=0.42W

L/S Rds(on):typ:9.1mOhm, max:11.6mOhm
Idsm(TA=25)=15A, Idsm(TA=70)=9A
Ploss=0.14W

CHOKE:4.7uH, DCR 35mOhm
Ploss=1.77W

Output capacitor ESR need follow below equation to make sure feed back loop stability
ESR=20mV*L*fsw/2V

POK need pull high, it will pull high on VS transfer circuit

5V-OCP=13.5A
3V-OCP=8.9A

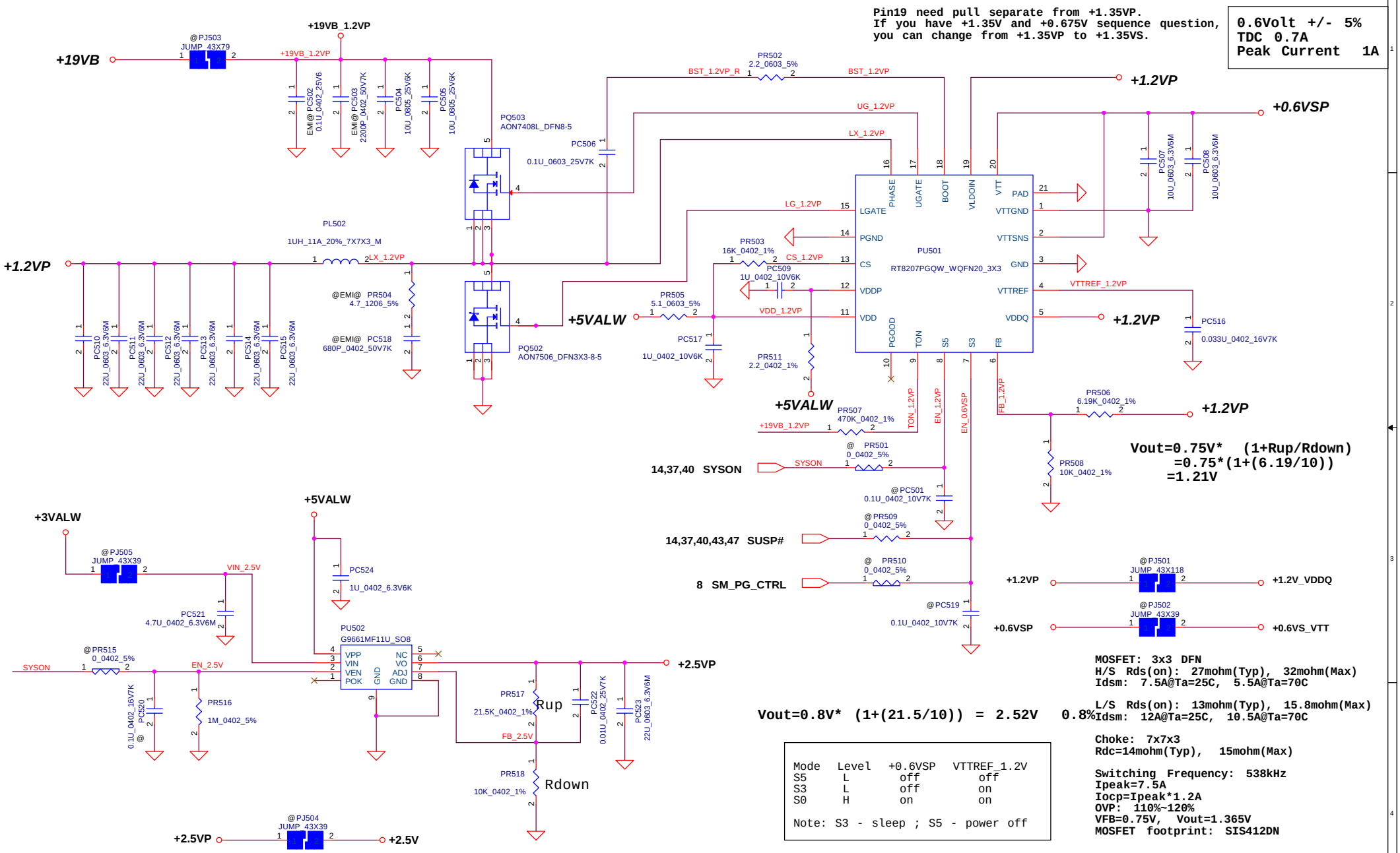
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: PWR-3.3VALWP/5VALWP

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 0.1

Date: Thursday, April 06, 2017 | Sheet 44 of 57



Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

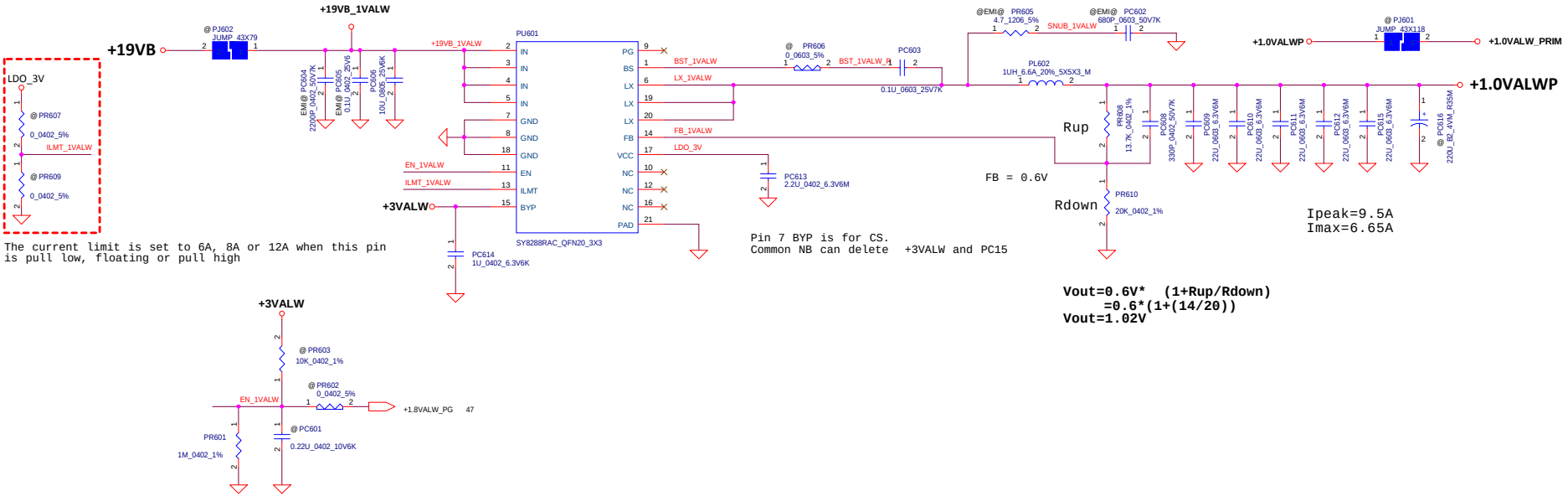
Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number: C5V01 M/B LA-E892P | Rev: 0.1

Date: Thursday, April 06, 2017 | Sheet 45 of 57

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

FB = 0.6V

Ipeak=9.5A
Imax=6.65A

Vout=0.6V* (1+Rup/Rdown)
=0.6*(1+(14/20))
Vout=1.02V

Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

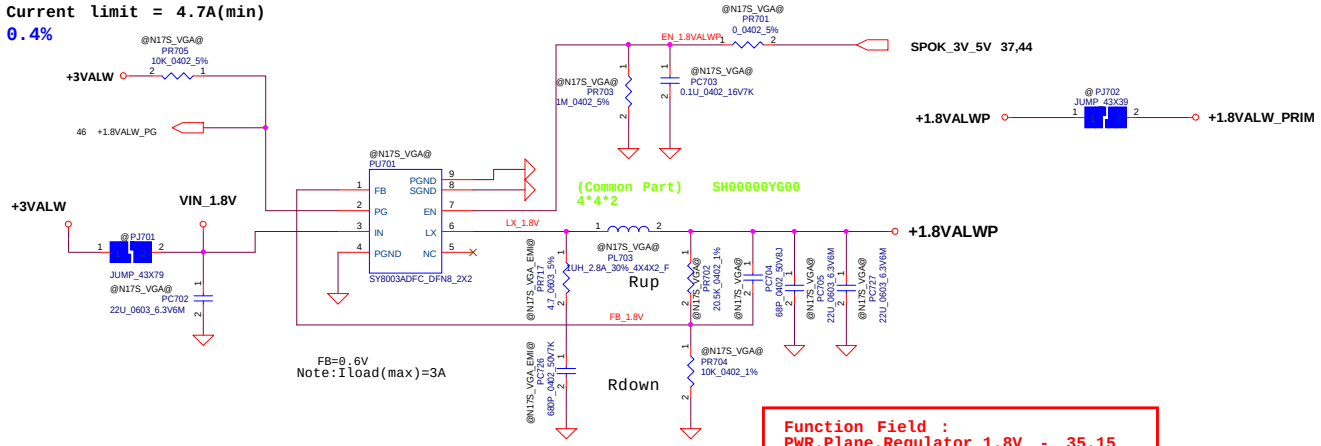
Compal Electronics, Inc.

Title: VCCP

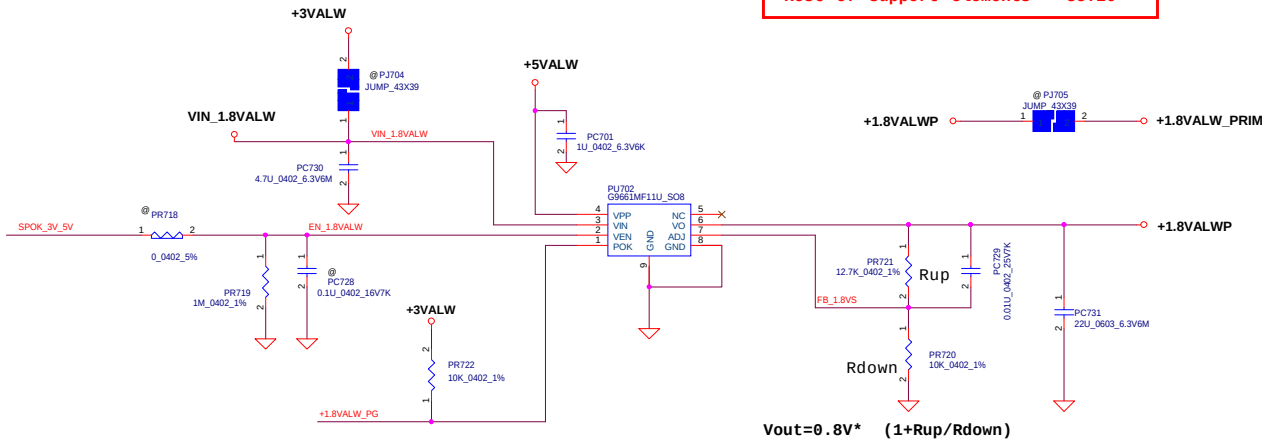
Size	Document Number	Rev
C	C5V01 M/B LA-E892P	0.1

Date: Thursday, April 06, 2017 Sheet 46 of 57

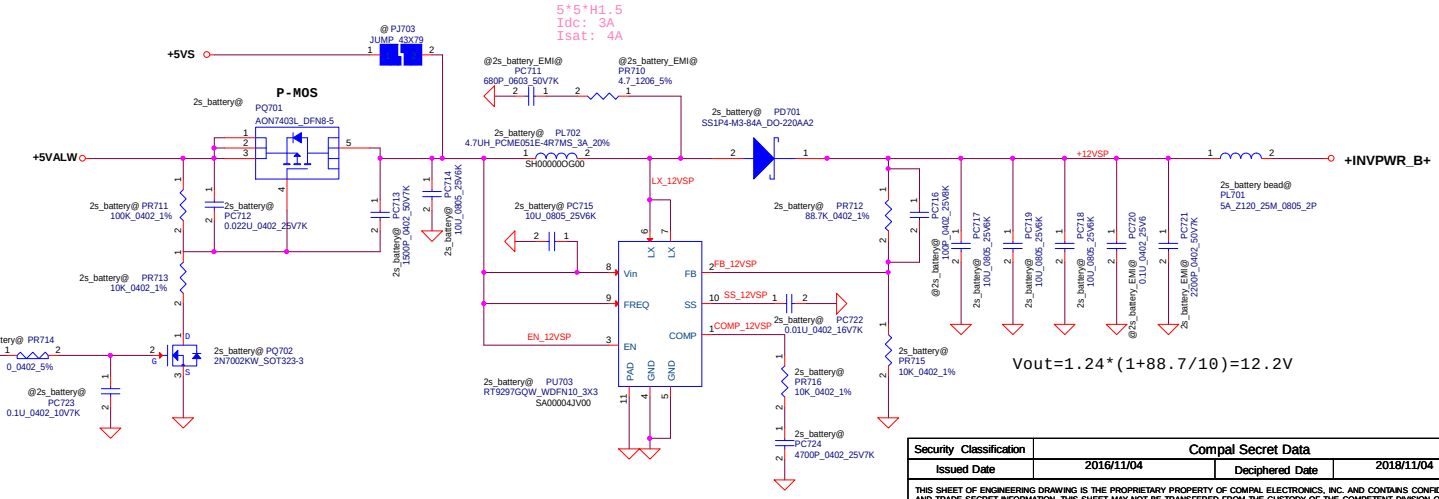
Current limit = 4.7A(min)
0.4%



Function Field :
PWR.Plane.Regulator_1.8V - 35.15
Rest of support elements - 35.16



Vout=0.8V* (1+Rup/Rdown)
Vout=0.8V* (1+(12.7/10)) = 1.816V



Vout=1.24*(1+88.7/10)=12.2V

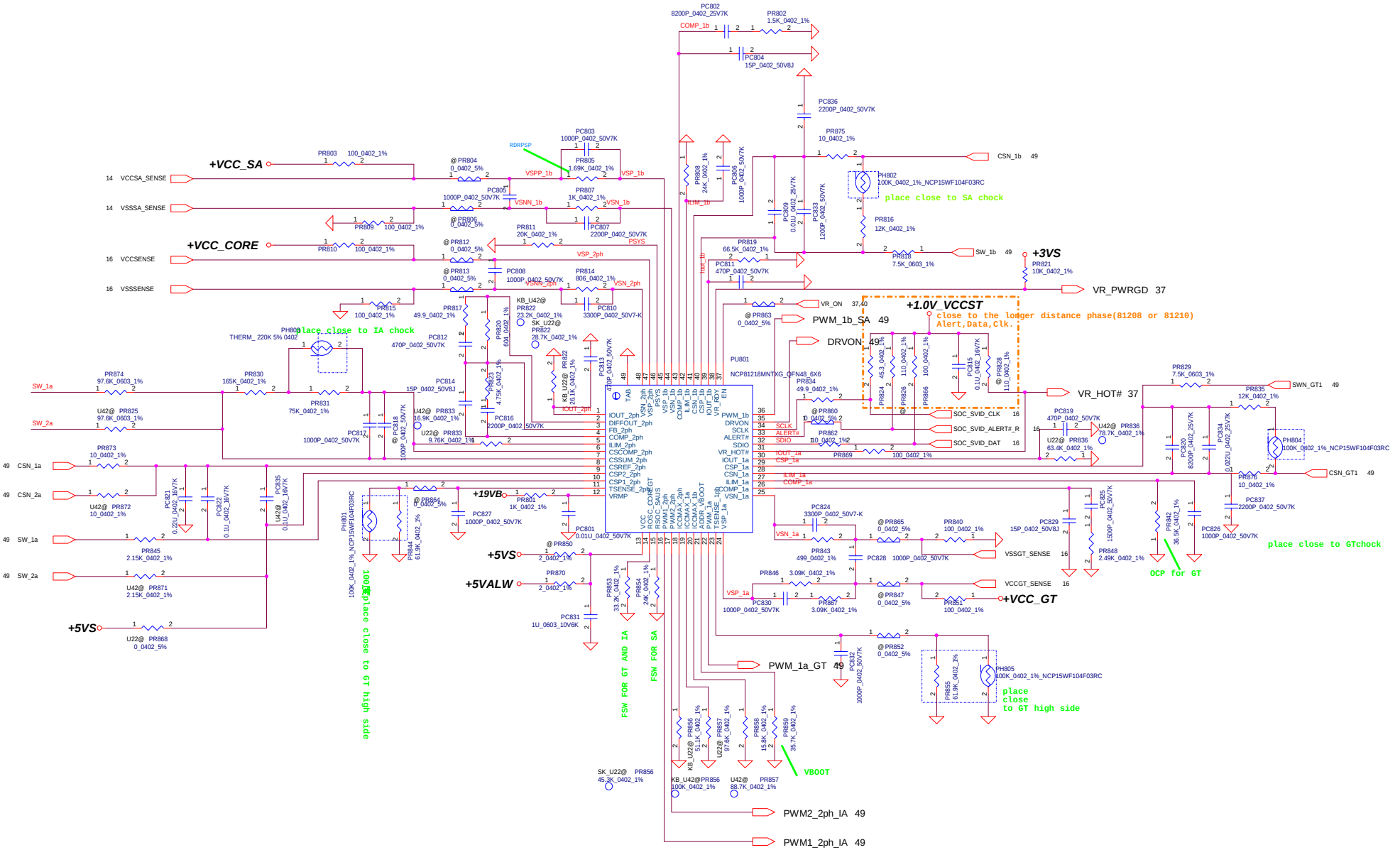
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C	C5V01 M/B LA-E892P	0.1

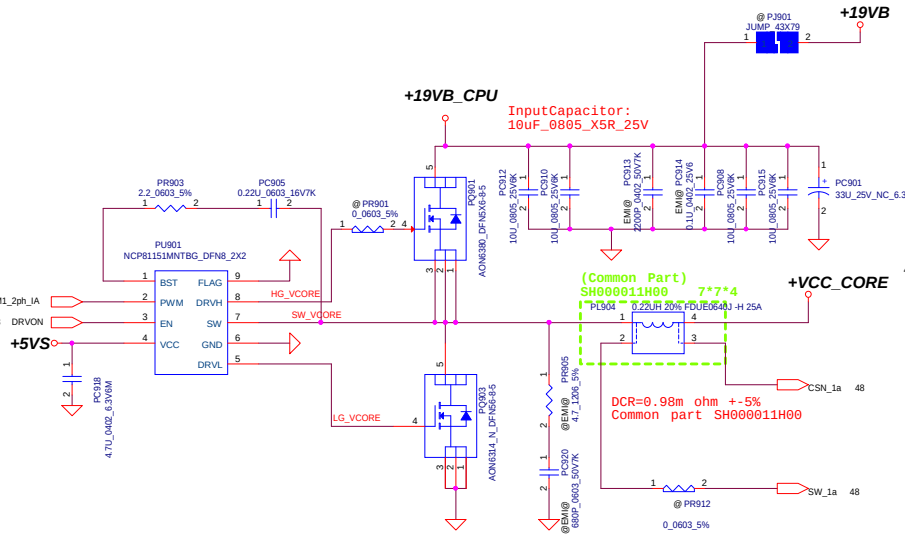
Date: Thursday, April 06, 2017 Sheet 47 of 57

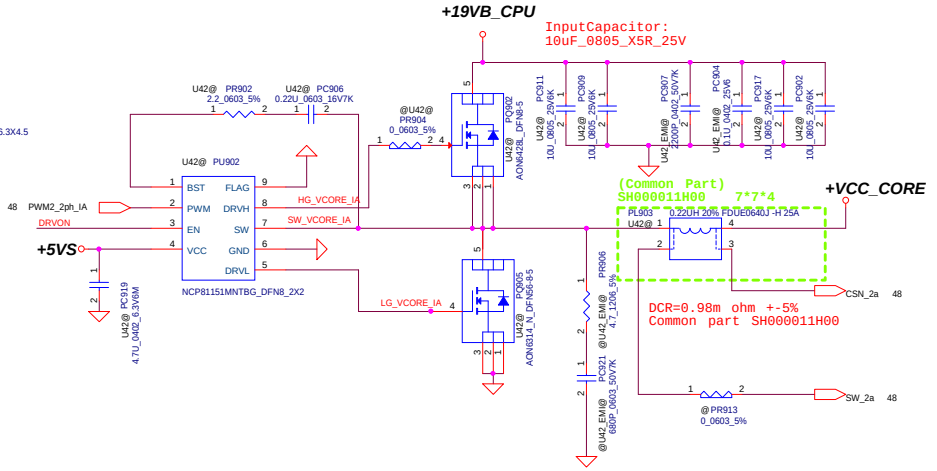


Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

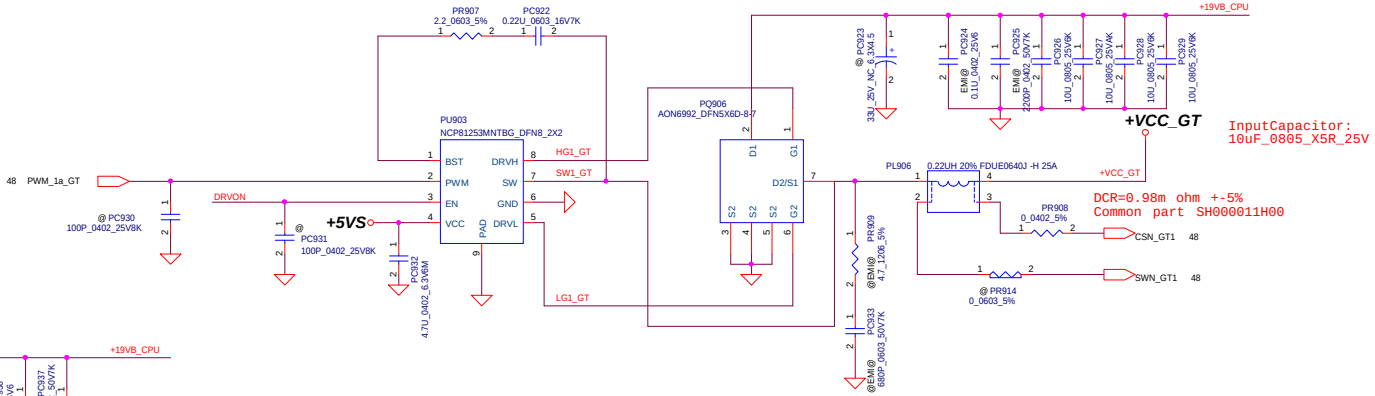
Compal Electronics, Inc.			
Title: IMVP8, NCP81206			
Size: C	Document Number: C5V01 M/B LA-E892P		Rev: 0.1
Date: Thursday, April 06, 2017		Sheet 48 of 57	

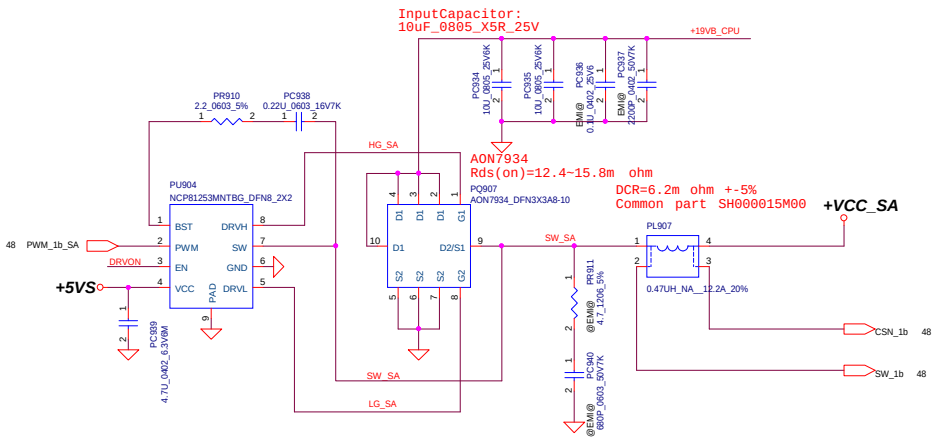
change PL9002, PL9003
SM01000C000 to comm
part SM01000P200





U22			
VCC:			
Imax=21A	Ipeak=32A	Iocp=40A	
U42			
VCC:			
Imax=42A	Ipeak=64A	Iocp=70A	
VCCGT:			
Imax=18A	Ipeak=31A	Iocp=39A	
VCCSA:			
Imax=4A	Ipeak=5A	Iocp=9.5A	





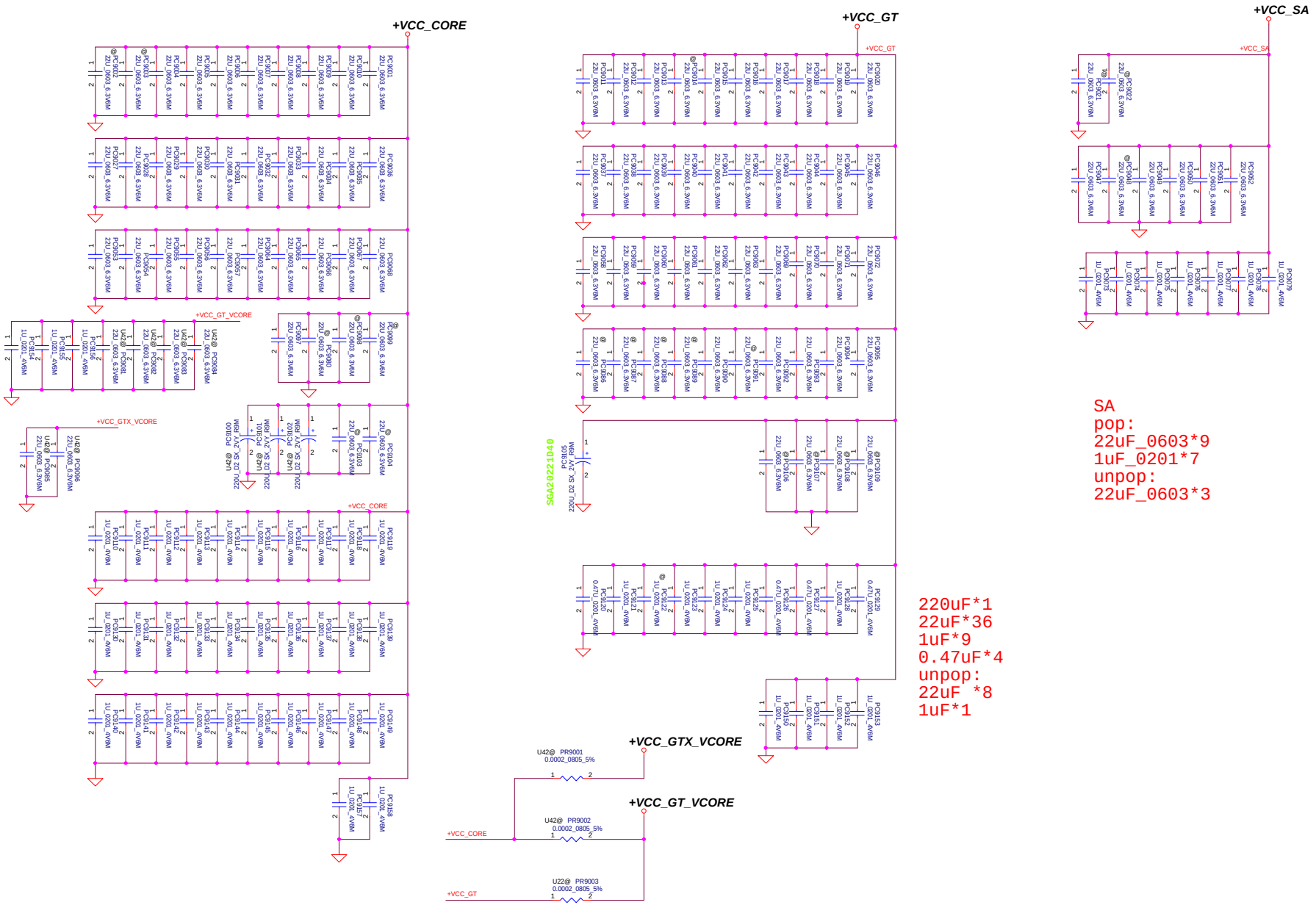
Security Classification	Compal Secret Data		
Issued Date	2016/11/04	Deciphered Date	2018/11/04

Compal Electronics, Inc.

Title: Power Train

Size	Document Number	Rev
C	C5V01 M/B LA-E892P	0.1

Date: Thursday, April 06, 2017 Sheet 49 of 57



2016/10/26
VCORE Output Capacitor:
U42
22uF_0603*39
1uF_0201*35
220uF *3
UNPOP
1uF_0201*3

2016/10/26
VCORE Output Capacitor:
U22
22uF_0603*33
1uF_0201*35
UNPOP
22_0603*9
220uF *3

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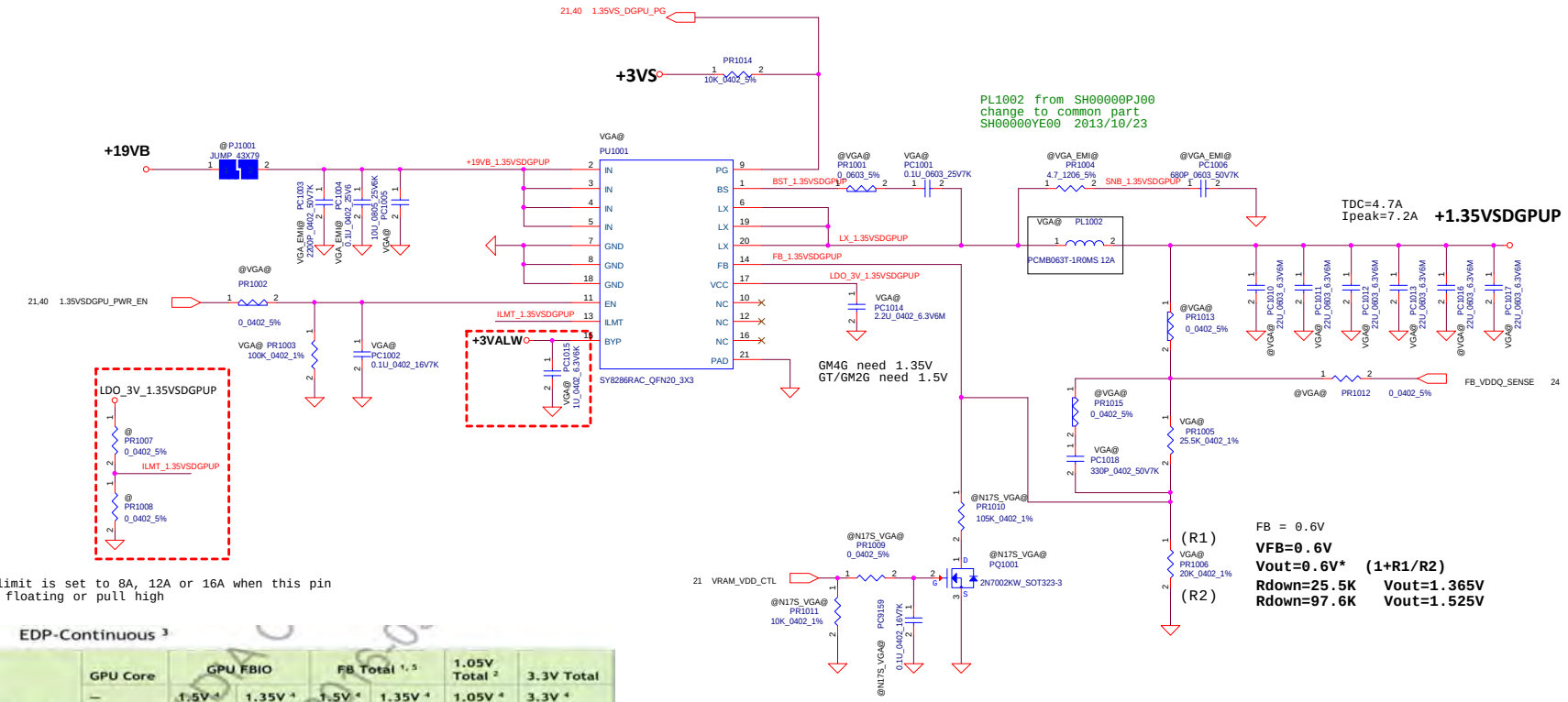
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]	3.3V Total
		—	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	—	2.0	—	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	—	2.0	—	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GXR	GDDR5	35.4	—	2.4	—	4.9	2.6	0.40

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1,5]		1.05V Total [2]
		—	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]
		(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	34.0	—	2.9	—	6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	—	2.9	—	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	—	3.1	—	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1
N16S-GXR	GDDR5	54.0	—	4.6	—	9.5	2.9

Table 7. Output EDP-Continuous

Product	NVVDD	GPU FBIO	FB Total[5]	1.0V Total[1]	1.8V Total[2]
	—	1.35V[4]	1.35V[4]	1.0V[4]	1.8V[4]
	(A)	(A)	(A)	(A)	(A)
N17S-G1	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.4	1.6	2.8	0.1	0.2

Table 8. Output EDP-Peak

Product	NVVDD	GPU FBIO	FB TOTAL[4]	1.0V Total[1]
	—	1.35V[3]	1.35V[3]	1.0V[3]
	(A)	(A)	(A)	(A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

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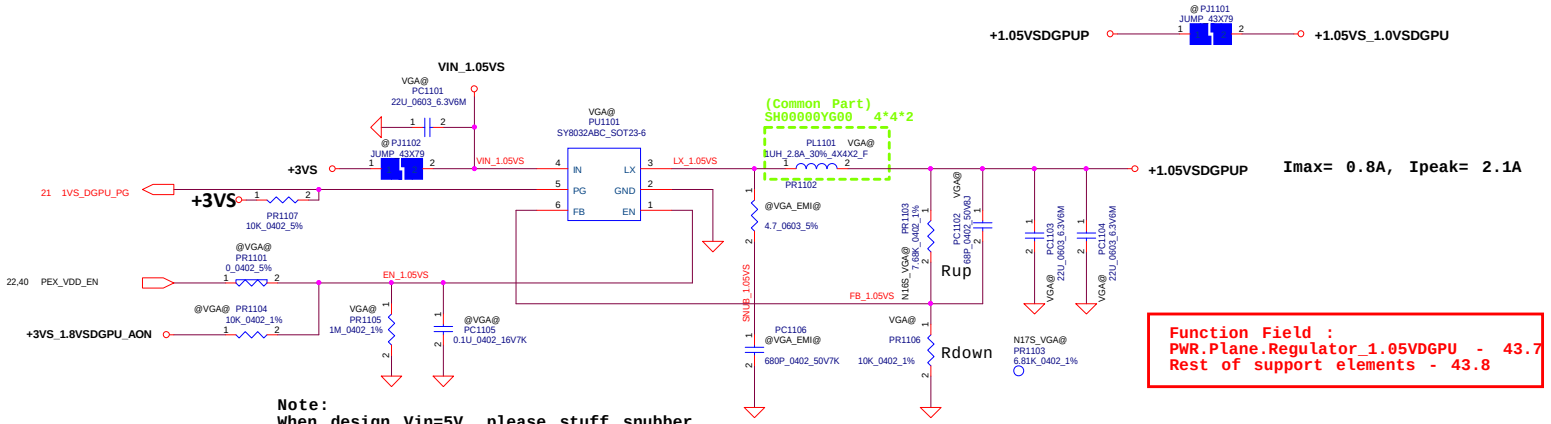
Module model information

SY8032_V2.mdd



Function Field :
PWR.Plane.Regulator_1.05VDGPU - 43.7
Rest of support elements - 43.8

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)
=>0.6V*(1+(7.68/10)=1.061 (1.01%)
=>0.6V*(1+(7.87/10)=1.072 (2.1%)

Vout=0.6V*(1+(6.81/10)=1.0086V

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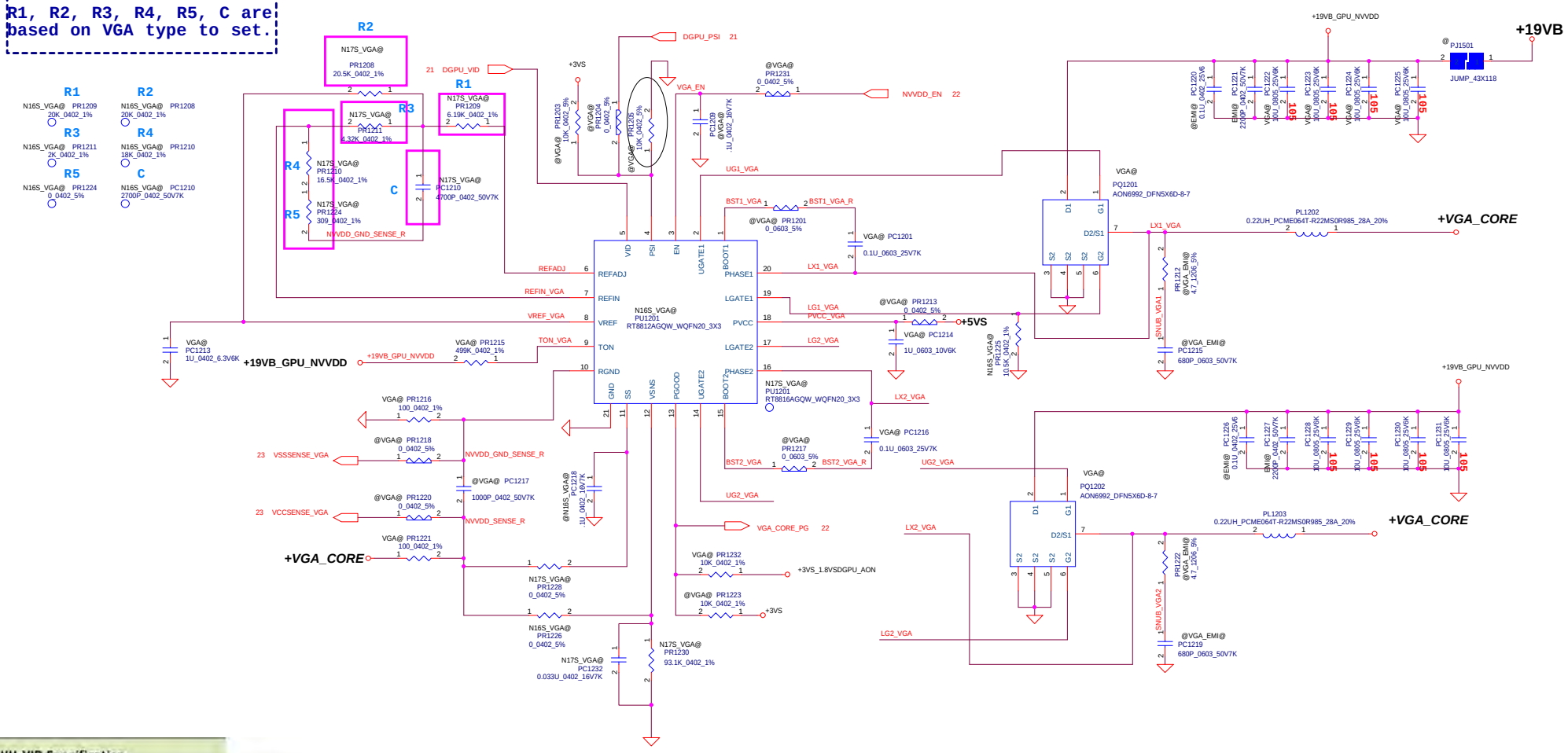
R1, R2, R3, R4, R5, C are based on VGA type to set.

unmount PRV5 for 2 phase select



PWM-VID Specification		Config B
Vmin	V	0.6
Vmax	V	1.2
Vboot	V	0.9
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	96
PWM Frequency F_{PWM}	MHz	1.125
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	20
R2 (1%)	KΩ	20
R3 (1%)	KΩ	2
R4 (1%)	KΩ	18
R5 (1%)	KΩ	0
C	nF	2.7

N17x DG-07875-001_v08.pdf:

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

Table 6. EDP-Continuous [3]

Products	VRAM Type	GPU Core – (A)
N16S-GMR	GDDR5	19.0
	DDR3/L	21.0
N16S-GTR	GDDR5 @ 2.0 GHz	26.5
	GDDR5 @ 2.5 GHz	26.5
	DDR3/L	26.0
N16S-GXR	GDDR5	35.4

Table 7. EDP-Peak [3]

Products	VRAM Type	GPU Core – (A)
N16S-GMR	GDDR5	34.0
	DDR3/L	39.5
N16S-GTR	GDDR5 @ 2.0 GHz	53.0
	GDDR5 @ 2.5 GHz	53.0
	DDR3/L	51.0
N16S-GXR	GDDR5	54.0

Table 7. Output EDP-Continuous

Product	NVVDD – (A)	GPU FBIO 1.35V[4] (A)	FB Total[5] 1.35V[4] (A)	1.0V Total[1] 1.0V[4] (A)	1.8V Total[2] 1.8V[4] (A)
N17S-G1	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.4	1.6	2.8	0.1	0.2

Table 8. Output EDP-Peak

Product	NVVDD – (A)	GPU FBIO 1.35V[3] (A)	FB TOTAL[4] 1.35V[3] (A)	1.0V Total[1] 1.0V[3] (A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

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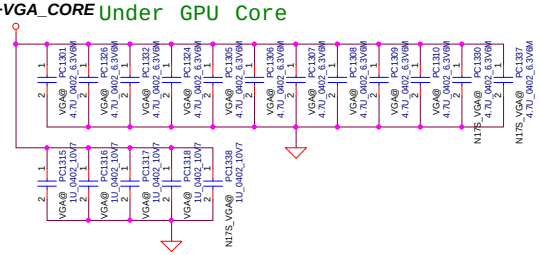
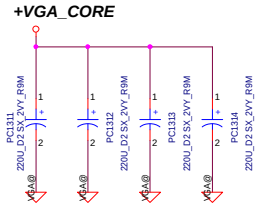
GB4-128 package

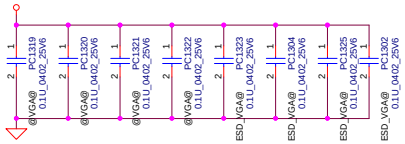
+VGA_CORE Under GPU Core



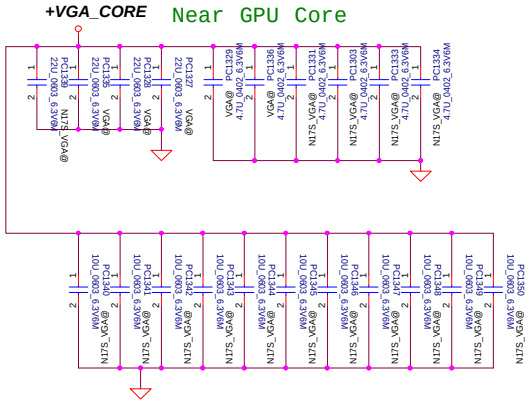
+VGA_CORE



+VGA_CORE



+VGA_CORE Near GPU Core



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	prevent part damage				PC410 and PC411 change to 0603 size	1/23	DVT
02	reduce part count				PR515,PR804,PR806,PR812,PR813,PR865,PR847,PR860,PR876, PR863,PR852 ,PR864 ,PR875,PR901,PR912,PR904,PR913,PR914 change to R-short	1/23	DVT
03	voltage level too high	3.37V change to 3.33V			PR402 change to 13.3K from 13.7K	1/23	DVT
04	SPOK voltage level				PR407 change to 20K from 100K	1/23	DVT
05	SMT	close SMT stencil problem			PJ9001, PJ9002, PJ9003 change to 0.2m ohm	1/23	DVT
06	DC S5 power consumption	meet DC S5 2.5mA spec			PR209 change to 750K from 10K PR211 change to 150K from 2K	1/23	DVT
07	prevent shortage				PL907 change to common part SH00001ED00 PQ502 change to AON7506	1/23	DVT
08	For N17s colay N16S				add PR1015 0ohm and PC1018 for transient PR1009 change to 0ohm from R-Short PR1013 change to 0ohm from 100 ohm	1/23	DVT
09	For power sequence				PC1218 change to unpop for rise time PR1231 change to 1K from 20K for sequence PR1003 change to 100K from 1M PR1002 change to 0ohm from 40.2K	1/23	DVT
10	For EMI request				PJ301 change to PL301	1/23	DVT
11	CPU transient	meet CPU spec			PR805 change to 1.69K from 1.78K PR814 change to 806ohm from 1K PR874 change to 97.6k from 93.1K PC821 change to 0.22u from 0.1uF PC820 change to 8200P from 0.01uF PR836 change to 63.4K from 69.8K PR846 and PR867 change to 3.09K from 3.32K PC9002.PC9003,PC9099,PC9098.PC9014,PC9091.PC9048 change to dummy	2/8	
12		1. prevent N17S design change 2. 5V voltage change to 5.2V 3. HW request 4. add filter 5. for mode change			1. PR701,,PR1204,PR718,PR1201,PR1217 change to 0ohm from R-short 2. PR401 change to 31.6K from 30.9K 3. add PR1232 for VGA_CORE_PG and PU to +3VS_1.8VSDGPU_AON. 4. PR1223 change to un-pop PC836 and PC837 change to pop PR875 and PR876 change to 10ohm PR908 change to 0 ohm 5. PU901 and PU902 change toNCP81151MNTBG_DFN8_2X2 PU903 change to NCP81253MNTBG_DFN8_2X2	2/9	
13		power squence			PC1209 change to unpop PR1231 change to R-short	2/10	
14		5V OCP level change			PR406 change 105K from 107K	2/19	
15		VGA Voltage overshot reduce part count VRAM fix 1.35V			add PC1232 0.033uF PR718,PR1015,PR1013,PR1101,PR1204,PR1201,PR1217,PR1002change to R-short PR1010,PQ1001,PR1009,PR1011 remove from BOM	3/15	
16		component rating Add RC delay			PC1215 and PC1219 size change to 0603 from 0402 PR320 change to 499 ohm PC323 change to pop 2.2uF	3/24	

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Item	Page	Date	Rev.	Reason for change	Modify Item
1	35	1/23	1.0	Type-C change connector	JUSB4 Symbol change to LOTES_AUSB0249-P001A_24P-T
2	38	1/23	1.0	Modify BOM structure	LK2, DK2 Change to FPEMC@
3	39	1/23	1.0	ME Drawing update	H30,H29 Change to H_3P2
4	30	1/23	1.0	Update for SD Card write protect issue	Add QL1 & RL20, RL21, RL22 for SD_WP inverter circuit
5	31,33,35	1/23	1.0	Change 0 ohm to R-Short	RM9,RO3,RS10,RM23,RS37,RS38 Change to R-short
6	19 11 11 15	1/23	1.0	For acer lesson learnt V1.7	RD202 Change to 0 ohm (DDR_DRAMRST#) Reserve CC131 on EC_VCCST_PG Add RC20 10_0402_5% ohm (PCH_PWROK) POP CC123 AND Change to 10U_0603
7	36	1/23	1.0	Cap. package Change	CS24 Change to 0402 package
8	33	1/23	1.0	Remove un-use connector	Del JHDD1
9	31	1/23	1.0	Follow ESD request	POP CM15 with 1000pf
10	22	1/23	1.0	Update VGA Power Sequence(+1.05VS_1.0VSDGPU)	Unpop RV103, CV231 Add RV188 from VGA_CORE_PG
11	32	1/23	1.0	EMI Requirement change to 220ohm bead	Change RA34 to SM01000NY00(BLM15PX221SN1D) with EMI@
12	22 22 22 26	2/7	1.0	Add N17S Component for BOM Select	Add UGPU1 SA0000ANV00 with N17SG1@ Change BOM structure from GTR@ to N16SGTR@ Del UGPU1 for GMR1@ Add X7607@,X7608@,X7609@
13	12,35	2/7	1.0	Change 0 ohm to R-Short	RC195, RC204, RS1,RS2,RS3,RS4,RS5,RS6,RS7,RS8 change to R-Short
14	33	2/7	1.0	Adjust SATA TX redirver EQ for Parada IC	RO17, RO18 and RO19 change to X76PAR@
15	33	2/7	1.0	Update SATA redriver circuit for TI IC	Reserved RO26, RO27 with BOM strurture @ Add RO17, RO18 (4.7K), RO19, RO21 (0 ohm) with X76TI@
16	29,22	2/7	1.0	BOM Change	Pop CC58 with 10uF, unpop CC59
17	40	2/7	1.0	Update VGA Power Sequence	CV238, CV239 change to 680PF
18	8	2/7	1.0	Add CPU PN for DVT	Add UC1 PN for Intel i3,i5,i7 CPU
19	13,35	2/7	1.0	Remove un-use USB port(Port9)	Del LS24
20	35	2/7	1.0	Bom Change , pull up resistor change to 100K ohm	RS20, RS40,RS41 value change to 100k ohm
21	36	2/7	1.0	Cancel solder mask on co-lay pin	LS1,LS3,LS4,LS6 cover solder mask (footprint update)
22	36	2/8	1.0	For acer lesson learnt V1.7	CC65.1 change to PCH_PWROK_R
23	18	2/8	1.0	Adjust Crystal Cap value	CC128,CC129 change to 27pF
24	8	2/8	1.0	Update PCB PN	Add DAZ20X00201 and DA8001AU010 for PCB
25	32	2/8	1.0	Update BOM Structure	Change RA35 BOM Structure to EMI@
26	22	2/10	1.0	For N17S GC6 Discharge Sequence	Add DV10 Add RV189, CV263, DV11
27	9	2/10	1.0	Remove BIOM ROM socket (Debug only)	Del JC1
28	7,11,36	2/13	1.0	For acer lesson learnt V1.7	Add CC132 Change to 1000pF --> CC50, CC53,CC131,CS24,CC65
29	36	2/13	1.0	Change Cap material for Z-High issue	Change CS25 to SGA00009M00
30	21,30	2/15	1.0	Change R for 25M/27M Crystal	Change R4961 and RL14 to 1K
31	21	2/16	1.0	Change 27MHz Material	X2000 change from SJ10000UI00 to SJ10000TQ00
32	18	2/16	1.0	Connect UC1.F65/G65 to GND, Change AY3, AY71 NC	Add RC237, Change RC182,RC183 to 0 ohm(@)

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HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
33	40	2/24	1.0	BOM Error	Add R574 with 10 ohm for N17S@, 47 ohm for N16X@
34	12	2/24	1.0	BOM Structure Update	RC215 with U22@, RC214 with U42@
35	22	3/9	1.A	Update for N17S power down sequence	Change RV189 from 15K to 2.2K for N17S
36	35	3/9	1.A	Update Type-c footprint	JUSB4 change symbol to LOTES_AUSB0181-P001A
37	8	3/13	1.A	RCOMP[0] 121 ohm for Mixed MD and SO-DIMM	RC38 121 ohm and cancel DDP@ and SDP@
38	33	3/13	1.A	Cancel SATA X76 level	Change RO22 to @ Del X76TI@ component (UO2, RO17, RO18 , RO19, RO21) Cancel X76PAR@ (RO17, RO18, RO19, RO21,UO2)
39	22	3/13	1.A	Change N17S IC to R3 PN	UGPU1 PN change to SA0000ANV10
40	8	3/13	1.A	Update PCB (DAZ, DA) Part number Add U42 CPU PN	Update DAZ to DAZ20X00203, DAZ24C00100, DA to DA8001AU01A Add UC1 for QN5C@/QN5D@
41	15	3/20	1.A	For acer lesson learnt V1.7	Reserved CC133 0.1U_0201
42	11 18 21 21	3/20	1.A	Crystal dampling resistor adjust	RC235,RC236 change to 33 ohm 1% RC233,RC234 change to 33 ohm 1% R4961 Change to N16X@ Add R4961 Opt ion Component for N17S@
43	29	3/31	1.A	Update Material	Change DY1 to SC300002900
44	30 21 21	4/18	1.A	Crystal dampling resistor adjust	Change RL14 to 330 ohm Change R4961 to 0 ohm for N17S Change R4961 to 680 ohm for N16S
45	12	4/18	1.A	Add BOM Structure for C5V01/D5PR1/D7W01	Change RC207 with EA17@ and RC210 with EA15@
46	37	4/18	1.A	Board ID update for D7W01	Add opt ion RB4 for D7W01

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