1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DESIGN: X502/MLB_CATZ

LAST CHANGE: Tue Aug 9 17:02:57 2016

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
1	0006782329	ENGINEERING RELEASED	2016-08-10

LAST_MODIFICATION=Tue Aug 9 17:03:06 2016

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7	7	CPU LPDDR3 Interface	PAULM	06/15/2015
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LAST_MODIFICATION=Tue Aug 9 17:03:06 2016

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49	63	JACK CODEC	AHAAGE	09/22/2015
50	64	SPEAKER AMP	AHAAGE	03/23/2016
51	66	JACK TRANSLATORS		
52	69	DC-IN & BATTERY CONNECTORS		
53	70	PBUS Supply & Battery Charger		
54	71	VReg CPU VCC Cntl		
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56	73	IMVP VCCSA		
57	74	GT IMVP VCCGT		
58	76	VR - 5V S4, 3.3V S5		
59	77	VR - OPC (EDRAM)		
60	78	PMIC IC & Power Control		
61	79	PMIC VCCPCH VCCIO 1.8V		
62	80	PMIC 1.2V 1.0V 0.6V		
63	81	RAIL DESENSE CAPS		
64	82	Power FETs		
65	84	LCD Backlight Driver		
66	85	eDP Display Connector	X362	06/23/2015
67	86	SSD MODULE	PAULM	06/15/2015
68	99	DEVELOPMENT ONLY	PAULM	06/15/2015
69	100	Power Aliases	X502-EXP	12/03/2015
70	102	NC_ AND NO_TEST SIGNALS	PAULM	06/15/2015
71	103	Memory Signal Swaps	X502-EXP	12/03/2015
72	104	FCT, ICT PROPERTIES	PAULM	06/15/2015
73	500	=LAST SCHEMATIC PAGE=	MICHKLEE	06/23/2015

DOCUMENTS / BOARDS / ASSEMBLIES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-02265	1	SCHEM,MLB_CATZ,X502	SCH		
820-00875	1	PCBF,MLB_CATZ,X502	MLB	CRITICAL	
639-03266		PCBA,MLB_CATZ,XXXXX,X502			
685-00125	1	COMMON PARTS,MLB_CATZ,X502	CBOM		CMN_PARTS_BOM
985-00239	1	DEV PARTS,MLB_CATZ,X502	DEV1		DEVELOPMENT_LIST

BOM_COST_GROUP=NO COST ITEMS

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DRAWING TITLE: SCHEM,MLB-CATZ,X502

Apple Inc.

DRAWING NUMBER: 051-02265 SIZE: D

REVISION: 1.0.0

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Major ICs

CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-00235	1	IC,CPU,SKL-ULT,2+3E,42X24MM,BGA1356	U0500	CRITICAL	CPU_SKL:BASE
998-04195	1	INTERPOSER,VTT ADAPTER,SKL-U,BGA1356	U0500	CRITICAL	CPU_SKL:VTT_INTERPOSER
337S00168	1	CPU,SKYU,QJ8N,D0,QS,2/2,2.3,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_2_QS_2.3
337S00170	1	CPU,SKYU,QJ8K,D0,QS,2/2,2.6,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_2_QS_2.6
337S00149	1	CPU,SKYU,QJ57,J0,ES0,2/3,1.6,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_ES0_GD
337S00150	1	CPU,SKYU,QJ58,J0,ES0,2/3,1.6,28W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_ES0_BT
337S00219	1	CPU,SKYU,QK2T,K1,SQS,1.8,15W,.95,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_1G8
337S00220	1	CPU,SKYU,QKBY,K1,SQS,2.2,15W,1.05,BG1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G2
337S00222	1	CPU,SKYU,QK33,K1,SQS,2.0,15W,1.0,BG1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G0
337S00233	1	CPU,SKYU,QK32,K1,SQS,2.4,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G4
337S00232	1	CPU,SKY,SR2JC,K1,PRQ,1.8,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_1G8
337S00239	1	CPU,SKY,SR2JM,K1,PRQ,2.0,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_2G0
337S00234	1	CPU,SKYU,SR2JL,K1,PRQ,2.4,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_2G4

ACE

353S00422	2	IC,CD3215,USB PWR SWITCH,A0,6X6MM,BGA96	U3100,U3200	CRITICAL	ACE:A0	
353S00660	2	IC,CD3215,ACE,A1,USB PWR SWITCH,BGA96	U3100,U3200	CRITICAL	ACE:A1	
353S00807	2	IC,CD3215,ACE,B0,USB PWR SWITCH,BGA96	U3100,U3200	CRITICAL	ACE:B0	
353S00887	2	IC,CD3215,ACE,B0,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:B0_B	(BOOT CODE: 0002.08.07)
353S00888	2	IC,CD3215,ACE,B0,USB PWR SW,OTP=2,BGA96	U3100,U3200	CRITICAL	ACE:B0_2	(BOOT CODE: 0002.08.07)
353S00926	2	IC,CD3215,ACE,B03,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:B0_3	(BOOT CODE: 0002.08.08)
353S00961	2	IC,CD3215,ACE,C00,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:C0	

TBT ALPINE RIDGE

338S00160	1	IC,TBT,ALPINE RIDGE DP,QSJV,B1,6X6MM,BGA96	U2800	CRITICAL	TBT_AR:B1_QS
998-04160	1	IC,TBT,ALP-RIDGE DP,SLL44-TRAY,B1,CSP337	U2800	CRITICAL	TBT_AR:B1_PRQ_TRAY
338S00176	1	IC,TBT,ALPN-RIDGE DP,SLL43-T&R,B1,CSP337	U2800	CRITICAL	TBT_AR:B1_PRQ
338S00229	1	IC,TBT,ALPINE RIDGE,QSTY,QS,C0,CSP337	U2800	CRITICAL	TBT_AR:C0_QS
338S00249	1	IC,TBT,ALPINE RIDGE,QT5S,QS,C1,CSP337	U2800	CRITICAL	TBT_AR:C1_QS
338S00254	1	IC,TBT,ALPINE RIDGE,SLLSM,PRQ,C1,CSP337	U2800	CRITICAL	TBT_AR:C1_PRQ

WIRELESS MODULE

339S0250	1	MODULE,WIFI/BT,STELLA CIDRE,MUR,LGA80	U3700	CRITICAL	WIRELESS:MURATA
339S0251	1	MODULE,WIFI/BT,STELLA CIDRE,USI,LGA80	U3700	CRITICAL	WIRELESS:USI

Programmables (All Builds)

SMC

338S1231	1	IC,SMC12,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC:BLANK
341S00334	1	IC,SMC-B1,EXT (V2.31A18) POC,X502	U5000	CRITICAL	SMC:POC
341S00429	1	IC,SMC-B1,EXT (V2.35A4) PROTO 1,X502	U5000	CRITICAL	SMC:PROTO1
341S00517	1	IC,SMC-B1,EXT (V2.35A51) PROTO 2,X502	U5000	CRITICAL	SMC:PROTO2
341S00562	1	IC,SMC-B1,EXT (V2.36A2) EVT,X502	U5000	CRITICAL	SMC:EVT
341S00611	1	IC,SMC-B1,EXT (V2.36A33) PRE-DVT,X502	U5000	CRITICAL	SMC:PREDVT
341S00633	1	IC,SMC-B1,EXT (V2.36A48) DVT,X502	U5000	CRITICAL	SMC:DVT
341S00662	1	IC,SMC-B1,EXT (V2.36F58) PVT,X502	U5000	CRITICAL	SMC:PVT

EFI ROM

335S0959	1	IC,SPI SERIAL FLASH,64M BITS,3V,CSP,QE=1	U6100	CRITICAL	BOOTROM:BLANK	MICRON	
335S00006	335S0959	ALT_CMN	ALL	MACRONIX			
341S00389	1	IC,EFI (V0072) PROTO 0,X502	U6100	CRITICAL	BOOTROM:PROTO0		
341S00452	1	IC,EFI (V0093) PROTO 0,X502	U6100	CRITICAL	BOOTROM:PROTO1		
341S00513	1	IC,EFI (V0114) PROTO 2,X502	U6100	CRITICAL	BOOTROM:PROTO2		
341S00543	1	IC,EFI (V0130) PROTO 2.2,X502	U6100	CRITICAL	BOOTROM:PROTO2_2		
341S00573	1	IC,EFI (V0143) EVT,X502	U6100	CRITICAL	BOOTROM:EVT		
341S00673	1	IC,EFI (V0173) PVT,X502	U6100	CRITICAL	BOOTROM:PVT		

BT ROM

335S00024	1	IC,FLASH,USON8,512KBIT,75MHZ	U3770	CRITICAL	BT_ROM:BLANK
335S0837	335S00024	ALT_CMN	ALL	ALTERNATE	
341S00196	1	IC,BT ROM (V53) DVT,X261	U3770	CRITICAL	BT_ROM:X261
341S00397	1	IC,BT ROM (V53) PROTO0,X502	U3770	CRITICAL	BT_ROM:PROTO0
341S00397	1	IC,BT ROM (V53) PROTO0,X502	U3770	CRITICAL	BT_ROM:PVT

WIFI ROM

335S0956	1	IC,MEMORY,EEPROM,4K,1.7V-5.5V,UDFN8	U3780	CRITICAL	WIFI-ROM:BLANK
335S00145	335S0956	ALT_CMN	ALL	ALTERNATE	
341S00607	1	WIFI ROM (P175) PRE-DVT,WW1,X502	U3780	CRITICAL	WIFI-ROM:MURATA-FCC
341S00608	1	WIFI ROM (P175) PRE-DVT,WW2,X502	U3780	CRITICAL	WIFI-ROM:MURATA-ETSI
341S00609	1	WIFI ROM (P175) PRE-DVT,WW3,X502	U3780	CRITICAL	WIFI-ROM:MURATA-APAC
341S00610	1	WIFI ROM (P175) PRE-DVT,IND,X502	U3780	CRITICAL	WIFI-ROM:MURATA-IND
341S00636	1	WIFI ROM (P177) USI-WW1,X502	U3780	CRITICAL	WIFI-ROM:USI-FCC
341S00637	1	WIFI ROM (P177) USI-WW2,X502	U3780	CRITICAL	WIFI-ROM:USI-ETSI
341S00638	1	WIFI ROM (P177) USI-WW3,X502	U3780	CRITICAL	WIFI-ROM:USI-APAC
341S00639	1	WIFI ROM (P177) USI-IND,X502	U3780	CRITICAL	WIFI-ROM:USI-IND

TBT ROM

335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U2890	CRITICAL	AR_ROM:BLANK
341S00451	1	IC,NVM / AR (V0.8.15.E1) PROTO 1,X502	U2890	CRITICAL	AR_ROM:PROTO1
341S00512	1	IC,NVM (VB1-10.11-E2.6.3) PROTO 2,X502	U2890	CRITICAL	AR_ROM:PROTO2
341S00559	1	IC,NVM (V16.8) EVT,X502	U2890	CRITICAL	AR_ROM:EVT
341S00606	1	IC,NVM (V1.5) PRE-DVT,X502	U2890	CRITICAL	AR_ROM:PREDVT
341S00628	1	IC, NVM (V3.8), DVT, X502	U2890	CRITICAL	AR_ROM:DVT
341S00661	1	IC, NVM (VTBD), PVT, X502	U2890	CRITICAL	AR_ROM:PVT

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
REVISION 1.0.0
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Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00101	4	IC,LPDDR3-1866,16GB,512MX32,25NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:HYNIX_8GB_1866
333S0784	4	IC,LPDDR3-1866,32GBIT,25NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:HYNIX_16GB_1866
333S00097	4	IC,LPDDR3-1866,16GB,512MX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:MICRON_8GB_1866
333S00098	4	IC,LPDDR3-1866,32GB,1GX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:MICRON_16GB_1866
333S00099	4	IC,LPDDR3-1866,16GB,512MX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:SAMSUNG_8GB_1866
333S00049	4	IC,SDRAM,LPDDR3-1866,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:SAMSUNG_16GB_1866

Main DRAM SPD Straps

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

	RAMCFG1	RAMCFG0
HYNIX	0 (STUFF R)	0 (STUFF R)
MICRON	0 (STUFF R)	1 (OPEN)
SAMSUNG	1 (OPEN)	0 (STUFF R)
-RESERVED-	1 (OPEN)	1 (OPEN)

	RAMCFG2
8GB	0 (STUFF R)
16GB	1 (OPEN)

	RAMCFG3
2133	0 (STUFF R)
1867	1 (OPEN)

	RAMCFG4
DIE A	0 (STUFF R)
DIE B	1 (OPEN)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0006	4	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1331,R1332,R1334		DRAM:HYNIX_8GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1331,R1334		DRAM:HYNIX_16GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1331,R1332,R1334		DRAM:MICRON_8GB_1866
117S0006	2	RES,MF,1/20W,1K OHM,5,0201,SMD	R1331,R1334		DRAM:MICRON_16GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1332,R1334		DRAM:SAMSUNG_8GB_1866
117S0006	2	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1334		DRAM:SAMSUNG_16GB_1866

MLB VERSION ID STRAPS

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE	INVERT TO VALUE
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:POC	<11111>	<00000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:PROTO0	<11110>	<00001>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:PRE_PROTO1	<11101>	<00010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:PROTO1	<11100>	<00011>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:PROTO2	<11011>	<00100>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:PROTO2_2	<11010>	<00101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:EVT	<11001>	<00110>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:PREDVT	<11000>	<00111>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:DVT	<10111>	<01000>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:DVT3	<10110>	<01001>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:PVT	<10101>	<01010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:PRQ1	<10100>	<01011>

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
107S00015	107S00011	ALT_CMN	ALL		TFT
107S00087	107S00029	ALT_CMN	ALL		YAGEO
107S00033	107S00034	ALT_CMN	ALL		TFT
107S00071	107S00053	ALT_CMN	ALL		YAGEO
107S00044	107S00076	ALT_CMN	ALL		CYNTEC
107S00070	107S0085	ALT_CMN	ALL		TDK
107S0248	107S0250	ALT_CMN	ALL		TFT
107S0249	107S0251	ALT_CMN	ALL		TFT
128S00009	128S00015	ALT_CMN	ALL		KEMET
128S00070	128S00015	ALT_CMN	ALL		PANASONIC
128S00010	128S00011	ALT_CMN	ALL		PANASONIC
128S00026	128S00011	ALT_CMN	ALL		NEC
128S00031	128S00011	ALT_CMN	ALL		ROHM
128S00058	128S00018	ALT_CMN	ALL		ROHM
128S00069	128S00067	ALT_CMN	ALL		ROHM
128S00062	128S00067	ALT_CMN	ALL		NEC
128S0364	128S0264	ALT_CMN	ALL		SANYO 2ND FACTORY
128S0311	128S0329	ALT_CMN	ALL		NEC ALT TO SANYO
128S0325	128S0397	ALT_CMN	ALL		PANASONIC
131S00134	131S00041	ALT_CMN	ALL		TAIYO YUDEN
132S00064	132S0409	ALT_CMN	ALL		MURATA
138S00077	138S00035	ALT_CMN	ALL		TAIYO YUDEN
138S00093	138S00035	ALT_CMN	ALL		KYOCERA
138S00084	138S00060	ALT_CMN	ALL		TAIYO YUDEN
138S0703	138S0648	ALT_CMN	ALL		MURATA
138S0700	138S0641	ALT_CMN	ALL		MURATA
138S0689	138S0701	ALT_CMN	ALL		MURATA
138S0864	138S0709	ALT_CMN	ALL		MULTIPLE
138S1103	138S0719	ALT_CMN	ALL		TAIYO YUDEN
138S0706	138S0739	ALT_CMN	ALL		MURATA
138S00106	138S0754	ALT_CMN	ALL		KYOCERA
138S00015	138S0777	ALT_CMN	ALL		MULTIPLE
138S0846	138S0811	ALT_CMN	ALL		SAMSUNG
138S00032	138S0831	ALT_CMN	ALL		TAIYO YUDEN
138S00049	138S0831	ALT_CMN	ALL		KYOCERA
138S0775	138S0860	ALT_CMN	ALL		SAMSUNG
138S00086	138S0884	ALT_CMN	ALL		TAIYO YUDEN
138S0738	138S1101	ALT_CMN	ALL		SAMSUNG
152S00381	152S1129	ALT_CMN	ALL		CHILISIN
152S00343	152S1682	ALT_CMN	ALL		MURATA
152S00363	152S00048	ALT_CMN	ALL		NEC
152S00358	152S00208	ALT_CMN	ALL		CHILISIN
152S00367	152S00266	ALT_CMN	ALL		NEC
152S00403	152S00322	ALT_CMN	ALL		CHILISIN
152S1872	152S00361	ALT_CMN	ALL		MURATA
155S0659	155S0382	ALT_CMN	ALL		MURATA
155S0694	155S0387	ALT_CMN	ALL		MURATA
155S00155	155S0441	ALT_CMN	ALL		TDK
155S0660	155S0513	ALT_CMN	ALL		MURATA
155S00007	155S0667	ALT_CMN	ALL		TAIYO YUDEN
155S00034	155S0706	ALT_CMN	ALL		MURATA
155S00203	155S0894	ALT_CMN	ALL		TAIYO YUDEN
155S00115	155S00114	ALT_CMN	ALL		MURATA

More Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
197S00046	197S00036	ALT_CMN	ALL		EPSON
197S00047	197S00036	ALT_CMN	ALL		KYOCERA
197S00048	197S00036	ALT_CMN	ALL		MURATA
197S00053	197S00050	ALT_CMN	ALL		KYOCERA
197S00054	197S00050	ALT_CMN	ALL		NDK
197S00055	197S00050	ALT_CMN	ALL		MURATA
311S00008	311S0271	ALT_CMN	ALL		DIODES INC
311S00060	311S0273	ALT_CMN	ALL		DIODES INC
311S00004	311S0370	ALT_CMN	ALL		ON SEMI
311S00013	311S0508	ALT_CMN	ALL		DIODES INC
311S00122	311S0543	ALT_CMN	ALL		DIODES INC
311S0596	311S0593	ALT_CMN	ALL		TI
311S00097	311S00036	ALT_CMN	ALL		DIODES INC
353S00711	353S2073	ALT_CMN	ALL		ON SEMI
353S00712	353S2216	ALT_CMN	ALL		ON SEMI
353S00107	353S3239	ALT_CMN	ALL		ON SEMI
353S00854	353S4342	ALT_CMN	ALL		ST MICRO
353S00769	353S4398	ALT_CMN	ALL		DIODES INC
353S00525	353S4471	ALT_CMN	ALL		VISHAY
371S0713	371S0558	ALT_CMN	ALL		DIODES INC
371S00074	371S0602	ALT_CMN	ALL		INFINEON
371S0704	371S00077	ALT_CMN	ALL		NXP
371S00089	371S00085	ALT_CMN	ALL		DIODES INC
372S0186	372S0185	ALT_CMN	ALL		NXP
372S00016	372S00015	ALT_CMN	ALL		DIODES INC
376S1053	376S0604	ALT_CMN	ALL		DIODES INC
376S1106	376S0678	ALT_CMN	ALL		FAIRCHILD
376S00014	376S0761	ALT_CMN	ALL		TOSHIBA
376S00086	376S0761	ALT_CMN	ALL		DIODES INC.
376S1080	376S0820	ALT_CMN	ALL		DIODES INC
376S00074	376S0855	ALT_CMN	ALL		TOSHIBA
376S00146	376S1061	ALT_CMN	ALL		ROHM
376S1089	376S1128	ALT_CMN	ALL		NXP
377S00031	377S0178	ALT_CMN	ALL		ON SEMI
377S00048	377S00017	ALT_CMN	ALL		ST MICRO
377S0155	377S00011	ALT_CMN	ALL		ON SEMI
740S0144	740S0118	ALT_CMN	ALL		LITTELFUSE
740S00028	740S0118	ALT_CMN	ALL		BUSSMANN
740S00003	740S0135	ALT_CMN	ALL		AEM, INC.
740S00027	740S0159	ALT_CMN	ALL		BOURNS
740S00033	740S00002	ALT_CMN	ALL		THINKING
740S00007	740S00019	ALT_CMN	ALL		BOURNS

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB_CATZ
LAST CHANGE: Fri Aug 5 13:34:33 2016

PAGE TITLE
BOM Configuration

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MOUNTING HOLES

998-03850

SH0400
4.0R3.6-NSP

SH0401
4.0R3.6-NSP

FAN MOUNTING HOLE

998-03850

SH0410
TH-NSP
SL-2.6X2.0-4.7X4.1

PLATED HOLES

SH0420
TH-NSP
LARGER SLOT, NEAR ANTENNA
SL-3.38X2.1-5.88X4.6
998-06494

SH0421
TH-NSP
SL-3.36X2.1-5.86X4.6
998-03823

SH0425
TH-NSP
SL-3.36X2.1-5.86X4.6

SH0426
TH-NSP
SL-3.36X2.1-5.86X4.6
998-03823

POGO PINS

870-01680

SH0430
POGO-2.30D-4.1H-SM

SH0431
POGO-2.30D-4.1H-SM

SH0437
POGO-2.30D-4.1H-SM

870-02068

SH0432
POGO-2.00D-2.95H-SM-1

SH0434
POGO-2.30D-4.1H-SM

SH0435
POGO-2.30D-4.1H-SM

SH0436
POGO-2.30D-4.1H-SM

SH0433
POGO-2.00D-2.95H-SM-1

TOP STANDOFFS

860-00385

SH0450
2.80D1.2ID-1.44H-SM

SH0451
2.80D1.2ID-1.44H-SM

SH0452
2.80D1.2ID-1.44H-SM

SH0453
2.80D1.2ID-1.44H-SM

SH0455
2.80D1.2ID-1.44H-SM

SH0457
2.80D1.2ID-1.44H-SM

BOTTOM STANDOFFS

860-00468

SH0460
2.80D1.2ID-3.0H-SM

SH0461
2.80D1.2ID-3.0H-SM

SHIELD CANS

MEMORY CAN - TOP

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07887	1	SHIELD CAN FENCE,DRAM,MN,X520	SHLD4	CRITICAL	SHIELD_CAN_MEMORY_TOP

MEMORY CAN - BOTTOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-08894	1	SHIELD FENCE,BOT DRAM,SUS,PRE-MN,X520	SHLD1	CRITICAL	SHIELD_CAN_MEMORY_BOT

WIRELESS CAN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07886	1	SHIELD CAN,EMI,WIFI,SYM,MN,TALL,X520	SHLD2	CRITICAL	SHIELD_CAN_WIFI

USB-C CAN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07885	1	SHIELD CAN,AR,USB-C,THRU,X520	SHLD3	CRITICAL	SHIELD_CAN_USBC

BOM_COST_GROUP=MECHANICALS

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PD Parts

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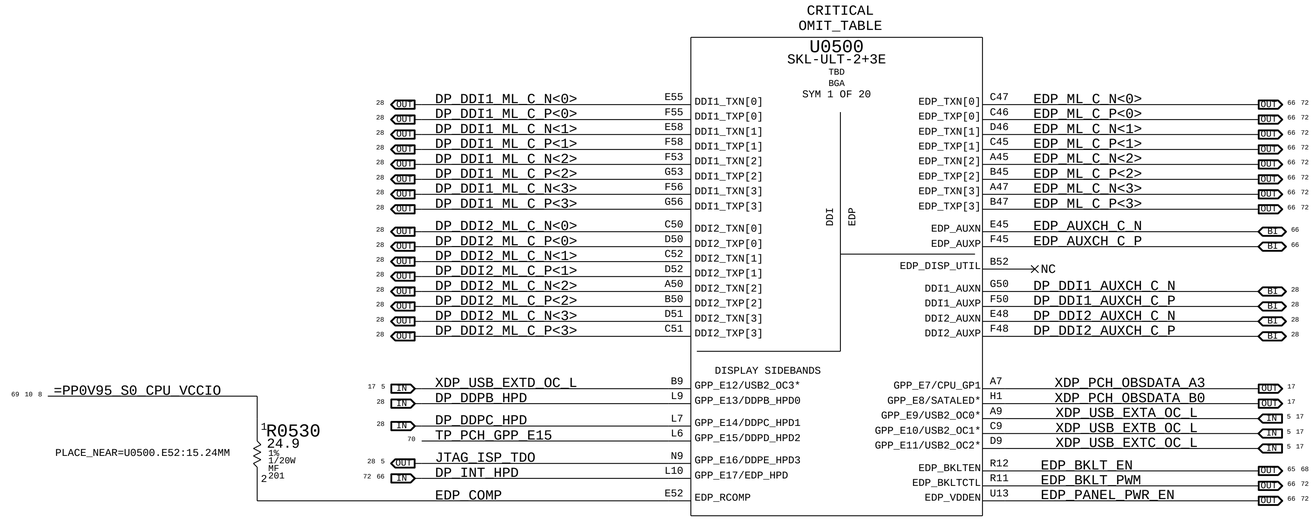

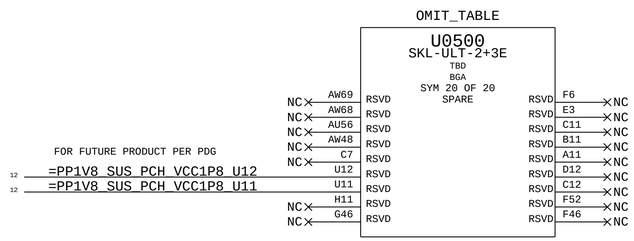

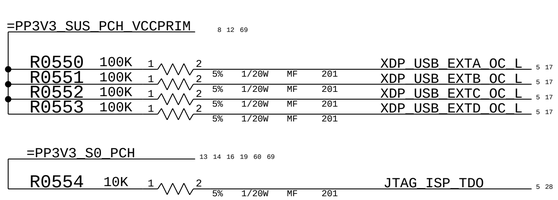

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
CPU GFX

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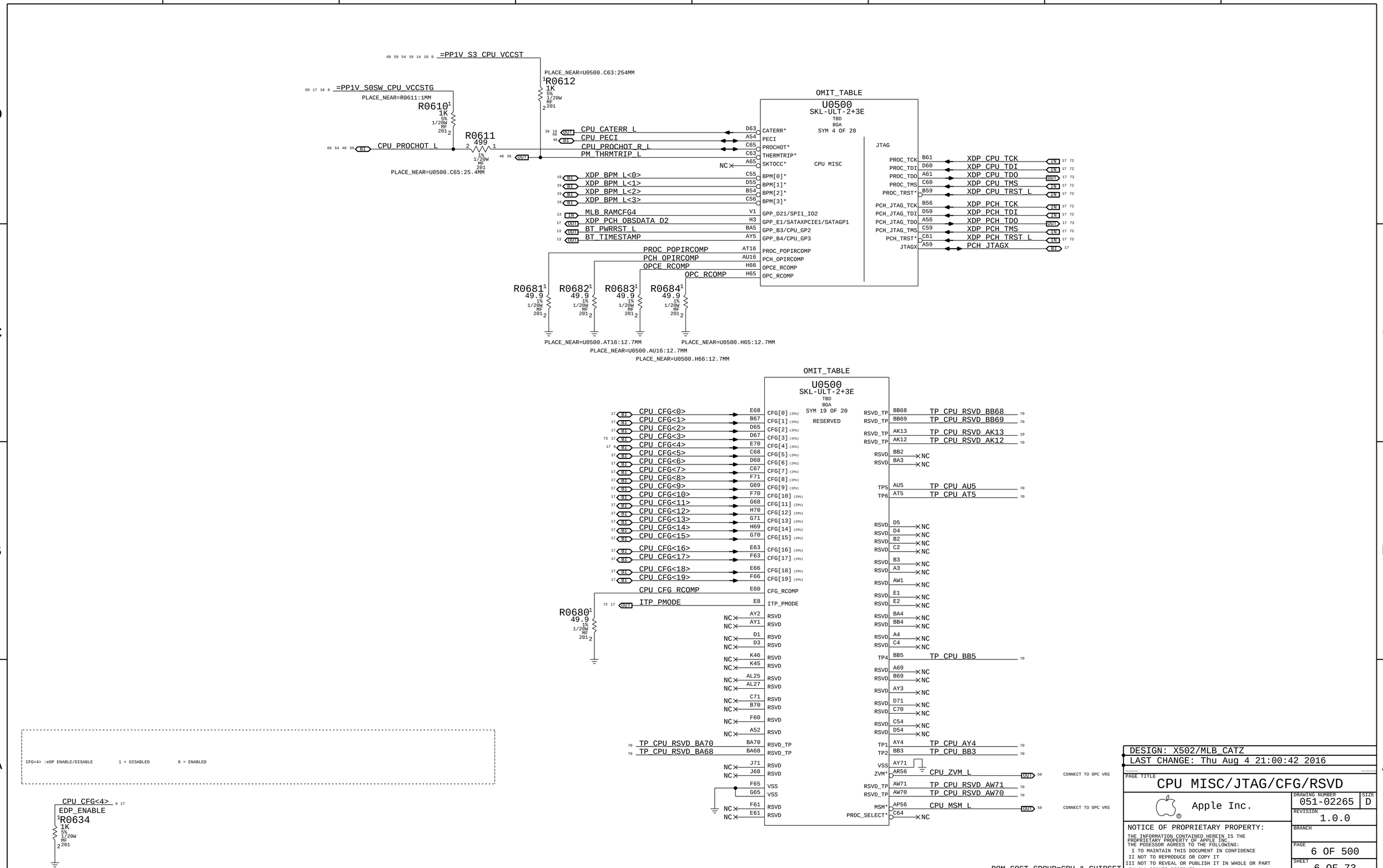

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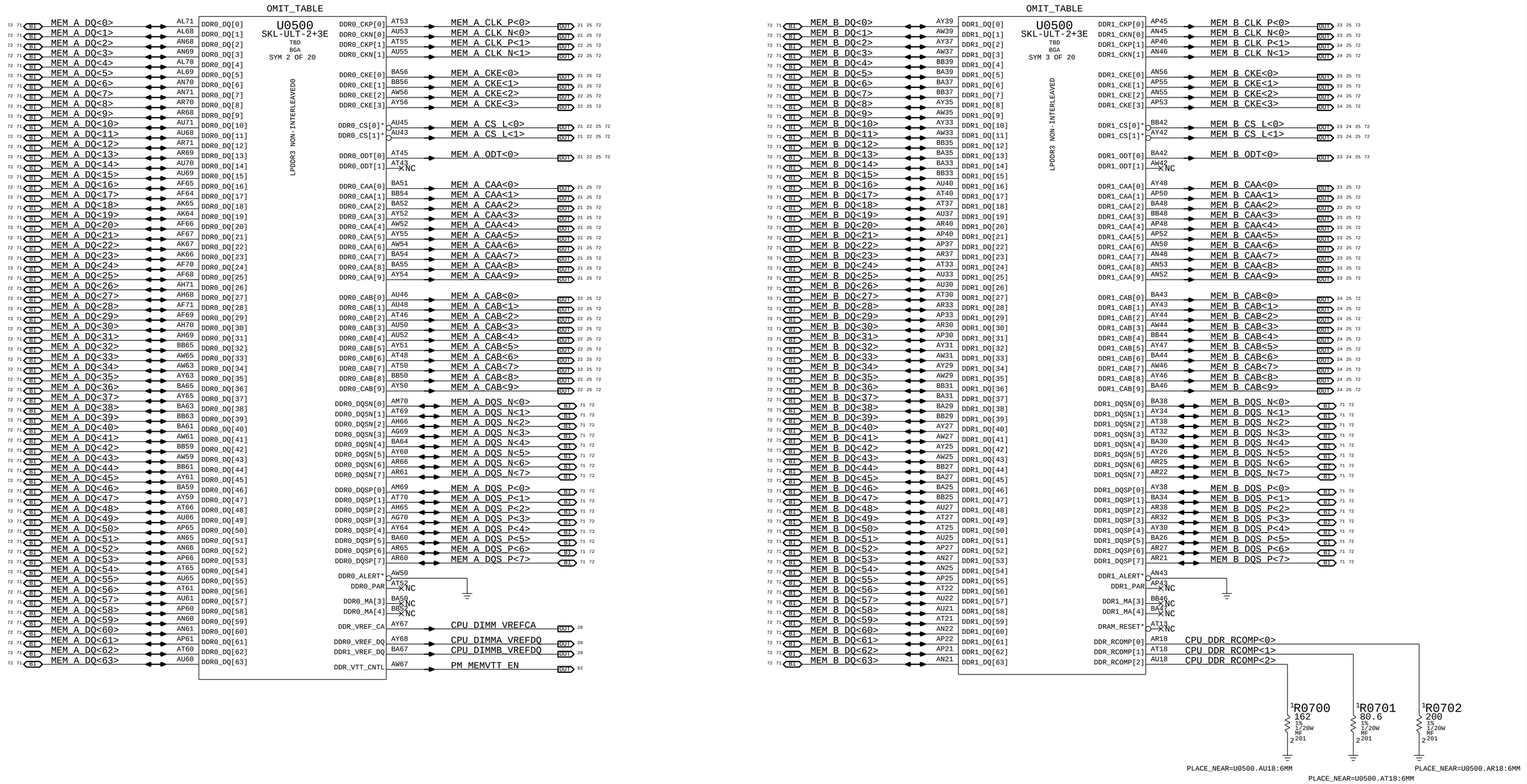

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE

CPU LPDDR3 Interface

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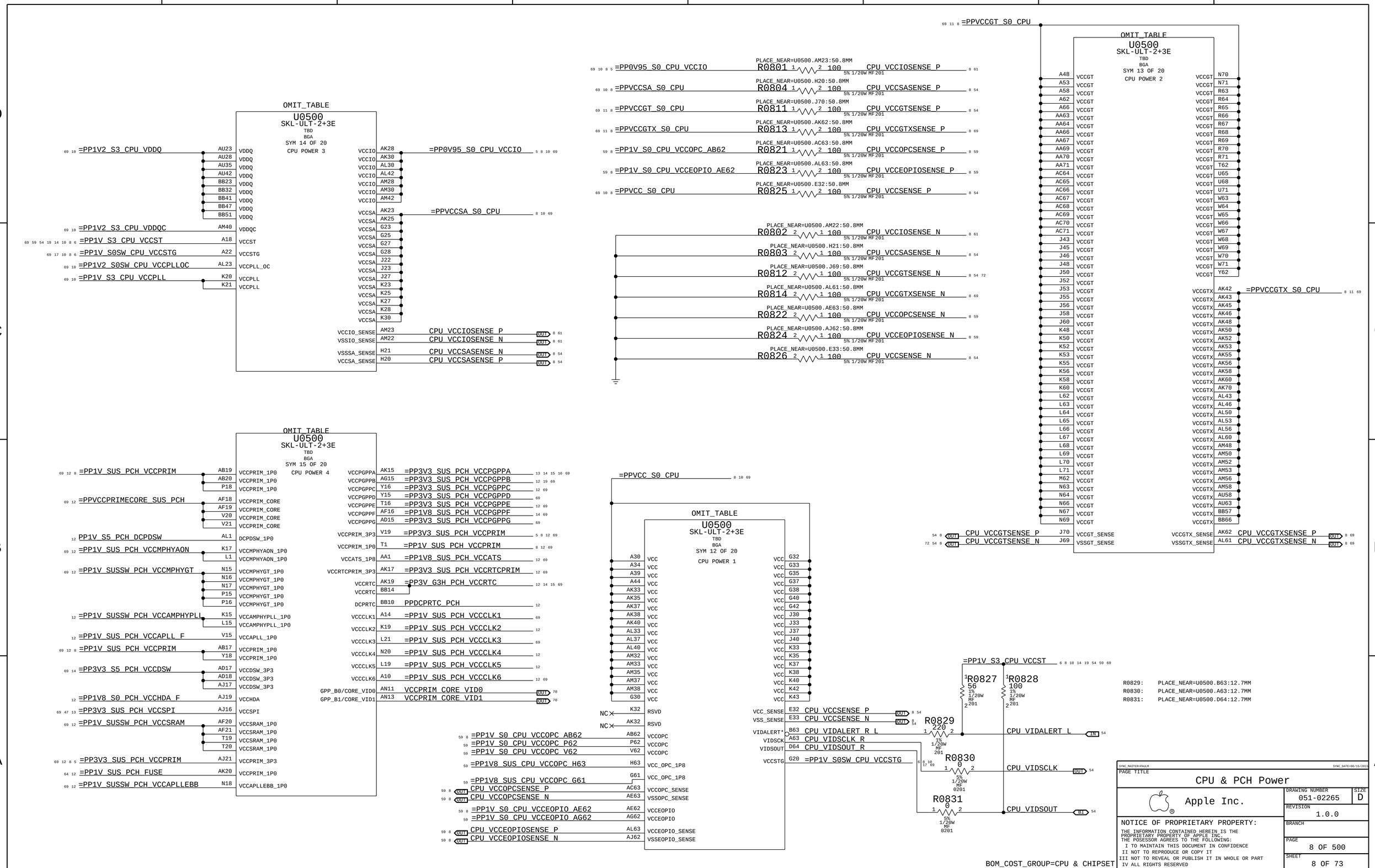

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OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 16 OF 20
GND1

70 TP_CPU_NCTFVSS_A5	A5 VSS	VSS AL65	
	A67 VSS	VSS AL66	
70 TP_CPU_NCTFVSS_A70	A70 VSS	VSS AM13	
	AA2 VSS	VSS AM21	
	AA4 VSS	VSS AM25	
	AA65 VSS	VSS AM27	
	AA68 VSS	VSS AM43	
	AB15 VSS	VSS AM45	
	AB16 VSS	VSS AM46	
	AB18 VSS	VSS AM55	
	AB21 VSS	VSS AM60	
	AB8 VSS	VSS AM61	
	AD13 VSS	VSS AM68	
	AD16 VSS	VSS AM71	
	AD19 VSS	VSS AM8	
	AD20 VSS	VSS AN20	
	AD21 VSS	VSS AN23	
	AD62 VSS	VSS AN28	
	AD8 VSS	VSS AN30	
	AE64 VSS	VSS AN32	
	AE65 VSS	VSS AN33	
	AE66 VSS	VSS AN35	
	AE67 VSS	VSS AN37	
	AE68 VSS	VSS AN38	
	AE69 VSS	VSS AN40	
	AF1 VSS	VSS AN42	
	AF10 VSS	VSS AN58	
	AF15 VSS	VSS AN63	
	AF17 VSS	VSS AP10	
	AF2 VSS	VSS AP18	
	AF4 VSS	VSS AP20	
	AF63 VSS	VSS AP23	
	AG16 VSS	VSS AP28	
	AG17 VSS	VSS AP32	
	AG18 VSS	VSS AP35	
	AG19 VSS	VSS AP38	
	AG20 VSS	VSS AP42	
	AG21 VSS	VSS AP58	
	AG71 VSS	VSS AP63	
	AH13 VSS	VSS AP68	
	AH6 VSS	VSS AP70	
	AH63 VSS	VSS AR11	
	AH64 VSS	VSS AR15	
	AH67 VSS	VSS AR16	
	AJ15 VSS	VSS AR20	
	AJ18 VSS	VSS AR23	
	AJ20 VSS	VSS AR28	
	AJ4 VSS	VSS AR35	
	AK11 VSS	VSS AR42	
	AK16 VSS	VSS AR43	
	AK18 VSS	VSS AR45	
	AK21 VSS	VSS AR46	
	AK22 VSS	VSS AR48	
	AK27 VSS	VSS AR5	
	AK63 VSS	VSS AR50	
	AK68 VSS	VSS AR52	
	AK69 VSS	VSS AR53	
	AK8 VSS	VSS AR55	
	AL2 VSS	VSS AR58	
	AL28 VSS	VSS AR63	
	AL32 VSS	VSS AR8	
	AL35 VSS	VSS AT2	
	AL38 VSS	VSS AT20	
	AL4 VSS	VSS AT23	
	AL45 VSS	VSS AT28	
	AL48 VSS	VSS AT35	
	AL52 VSS	VSS AT4	
	AL55 VSS	VSS AT42	
	AL58 VSS	VSS AT56	
	AL64 VSS	VSS AT58	

OMIT_TABLE

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TBD
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GND2

	AT63 VSS	VSS BA49	
	AT68 VSS	VSS BA53	
	AT71 VSS	VSS BA57	
	AU10 VSS	VSS BA6	
	AU15 VSS	VSS BA62	
	AU20 VSS	VSS BA66	
	AU32 VSS	VSS BA71	TP_CPU_NCTFVSS_BA71 70
	AU38 VSS	VSS BB18	
70 TP_CPU_NCTFVSS_AV1	AV1 VSS	VSS BB26	
	AV68 VSS	VSS BB30	
	AV69 VSS	VSS BB34	
	AV70 VSS	VSS BB38	
	AV71 VSS	VSS BB43	
	AW10 VSS	VSS BB55	
	AW12 VSS	VSS BB6	
	AW14 VSS	VSS BB60	
	AW16 VSS	VSS BB64	
	AW18 VSS	VSS BB67	
	AW21 VSS	VSS BB70	TP_CPU_NCTFVSS_BB70 70
	AW23 VSS	VSS C1	TP_CPU_NCTFVSS_C1 70
	AW26 VSS	VSS C25	
	AW28 VSS	VSS C5	
	AW30 VSS	VSS D10	
	AW32 VSS	VSS D11	
	AW34 VSS	VSS D14	
	AW36 VSS	VSS D18	
	AW38 VSS	VSS D22	
	AW41 VSS	VSS D25	
	AW43 VSS	VSS D26	
	AW45 VSS	VSS D30	
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	AW51 VSS	VSS D44	
	AW53 VSS	VSS D45	
	AW55 VSS	VSS D47	
	AW57 VSS	VSS D48	
	AW6 VSS	VSS D53	
	AW60 VSS	VSS D58	
	AW62 VSS	VSS D6	
	AW64 VSS	VSS D62	
	AW66 VSS	VSS D66	
	AW8 VSS	VSS D69	
	AY66 VSS	VSS E11	
	B10 VSS	VSS E15	
	B14 VSS	VSS E18	
	B18 VSS	VSS E21	
	B22 VSS	VSS E46	
	B30 VSS	VSS E50	
	B34 VSS	VSS E53	
	B39 VSS	VSS E56	
	B44 VSS	VSS E6	
	B48 VSS	VSS E65	
	B53 VSS	VSS E71	
	B58 VSS	VSS F1	
	B62 VSS	VSS F13	
	B66 VSS	VSS F2	
70 TP_CPU_NCTFVSS_B71	B71 VSS	VSS F22	
70 TP_CPU_NCTFVSS_BA1	BA1 VSS	VSS F23	
	BA10 VSS	VSS F27	
	BA14 VSS	VSS F28	
	BA18 VSS	VSS F32	
	BA2 VSS	VSS F33	
	BA23 VSS	VSS F35	
	BA28 VSS	VSS F37	
	BA32 VSS	VSS F38	
	BA36 VSS	VSS F4	
	F68 VSS	VSS F40	
	BA45 VSS	VSS F42	
		VSS BA41	

OMIT_TABLE

U0500
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GND 3

F8 VSS	VSS L18	
G10 VSS	VSS L2	
G22 VSS	VSS L20	
G43 VSS	VSS L4	
G45 VSS	VSS L8	
G48 VSS	VSS N10	
G5 VSS	VSS N13	
G52 VSS	VSS N19	
G55 VSS	VSS N21	
G58 VSS	VSS N6	
G6 VSS	VSS N65	
G60 VSS	VSS N68	
G63 VSS	VSS P17	
G66 VSS	VSS P19	
H15 VSS	VSS P20	
H18 VSS	VSS P21	
H71 VSS	VSS R13	
J11 VSS	VSS R6	
J13 VSS	VSS T15	
J25 VSS	VSS T17	
J28 VSS	VSS T18	
J32 VSS	VSS T2	
J35 VSS	VSS T21	
J38 VSS	VSS T4	
J42 VSS	VSS U10	
J8 VSS	VSS U63	
K16 VSS	VSS U64	
K18 VSS	VSS U66	
K22 VSS	VSS U67	
K61 VSS	VSS U69	
K63 VSS	VSS U70	
K64 VSS	VSS V16	
K65 VSS	VSS V17	
K66 VSS	VSS V18	
K67 VSS	VSS W13	
K68 VSS	VSS W6	
K70 VSS	VSS W9	
K71 VSS	VSS Y17	
L11 VSS	VSS Y19	
L16 VSS	VSS Y20	
L17 VSS	VSS Y21	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE
CPU & PCH Grounds

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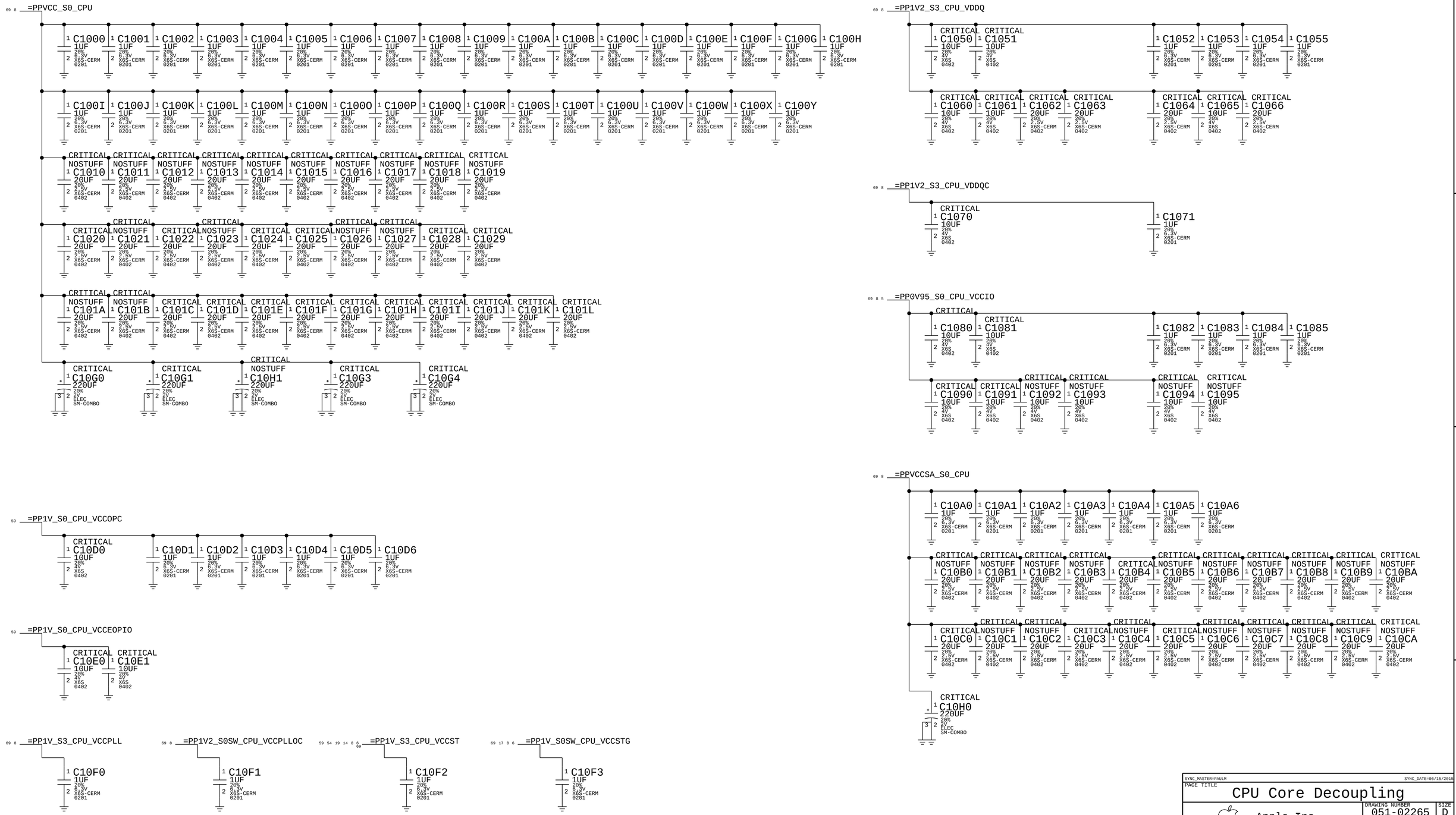

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE

CPU Core Decoupling

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DRAWING NUMBER 051-02265 SIZE D

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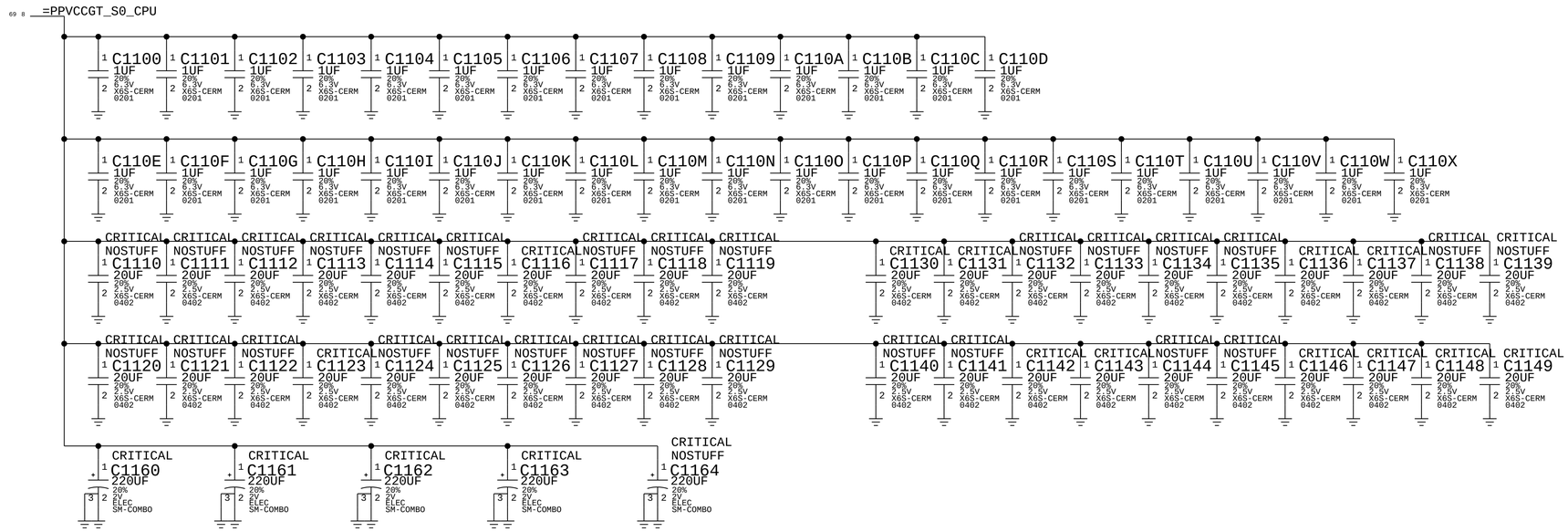

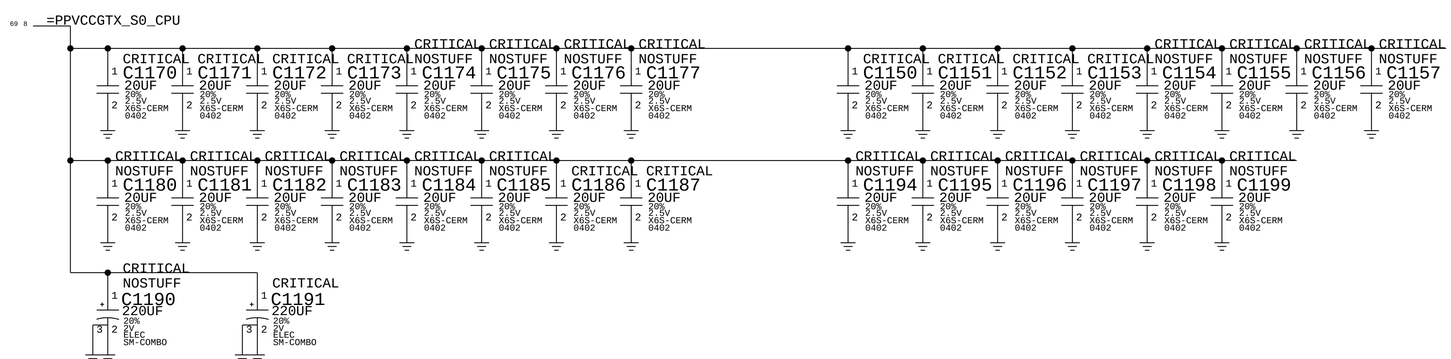

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PAGE TITLE	CPU GT Decoupling
	Apple Inc.
DRAWING NUMBER	051-02265
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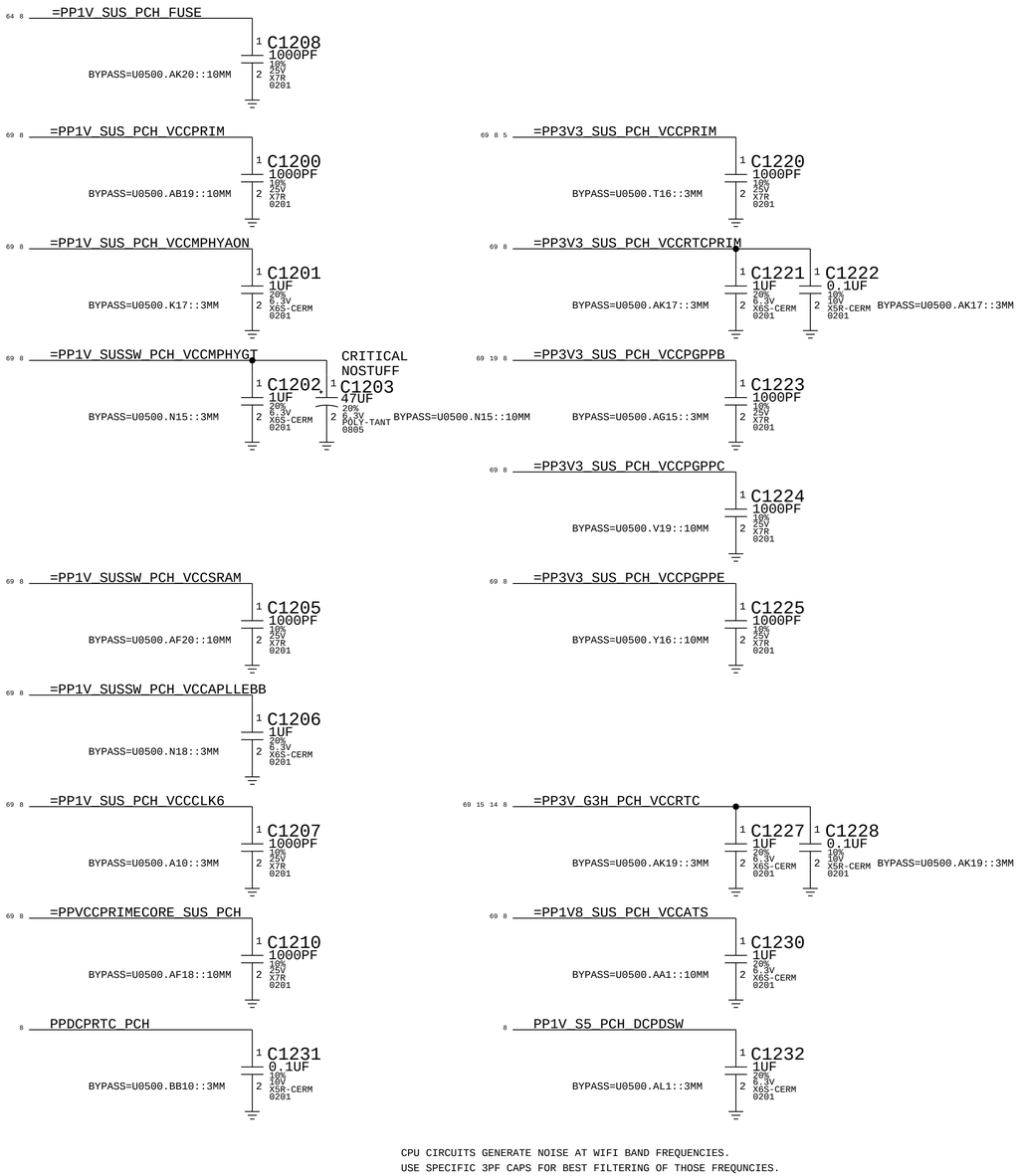
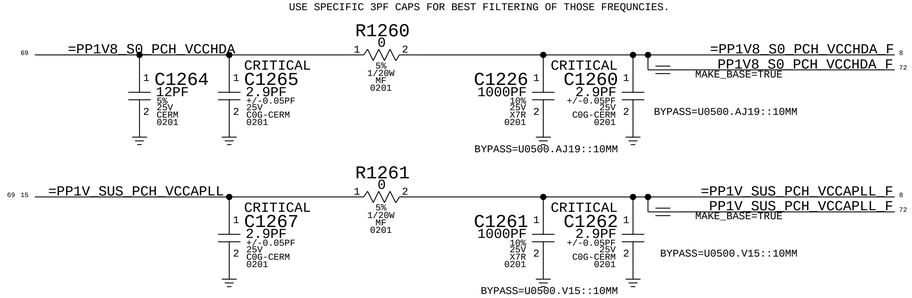
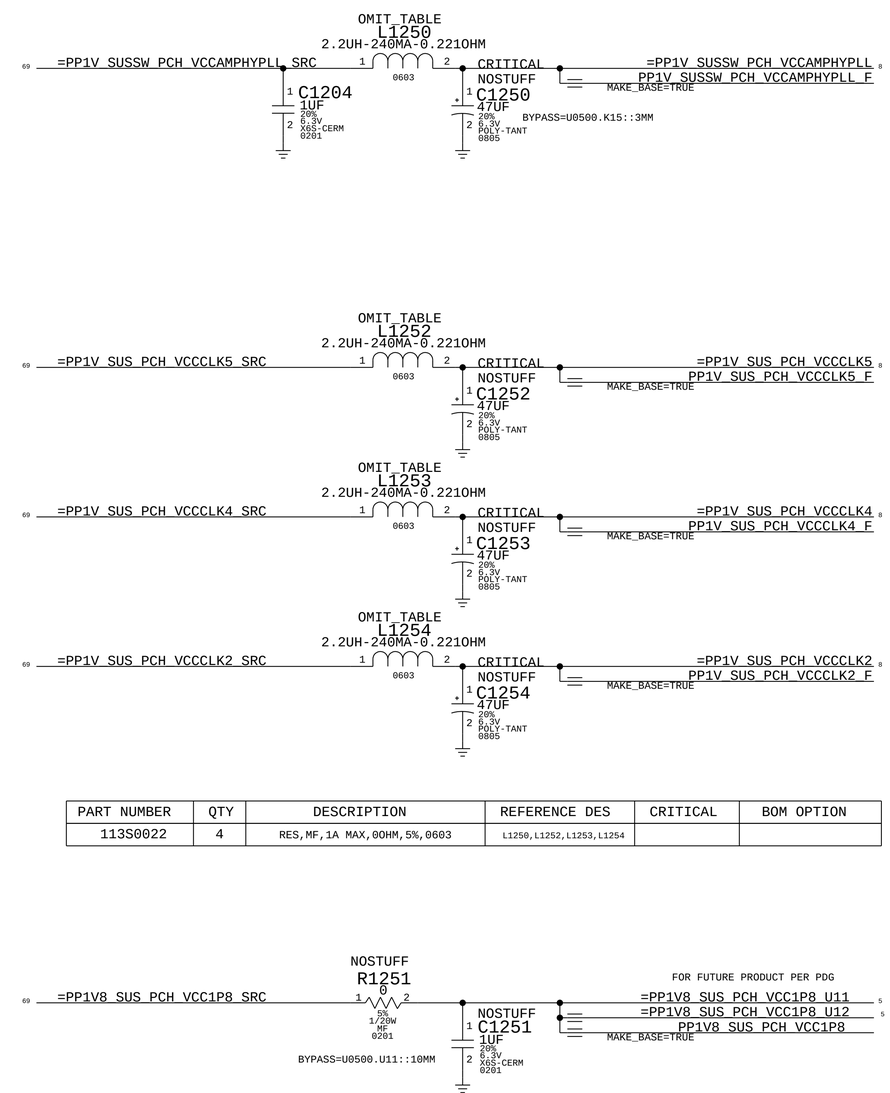


CPU CIRCUITS GENERATE NOISE AT WIFI BAND FREQUENCIES.
USE SPECIFIC 3PF CAPS FOR BEST FILTERING OF THOSE FREQUNCIES.



FILTER PLACEHOLDERS ONLY



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
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BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH Decoupling

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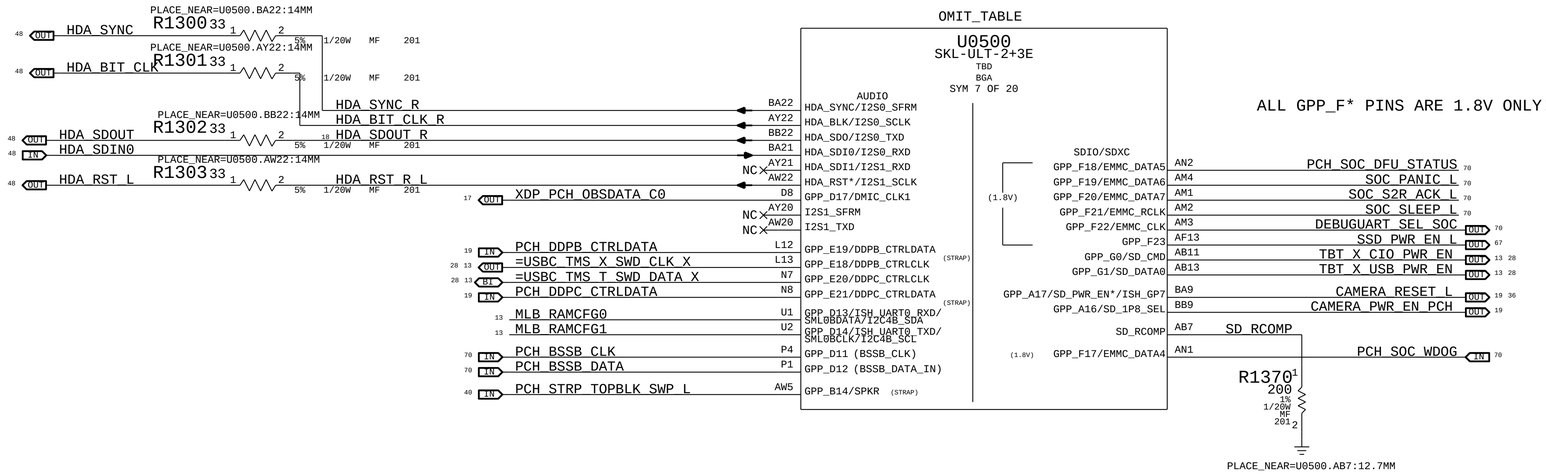
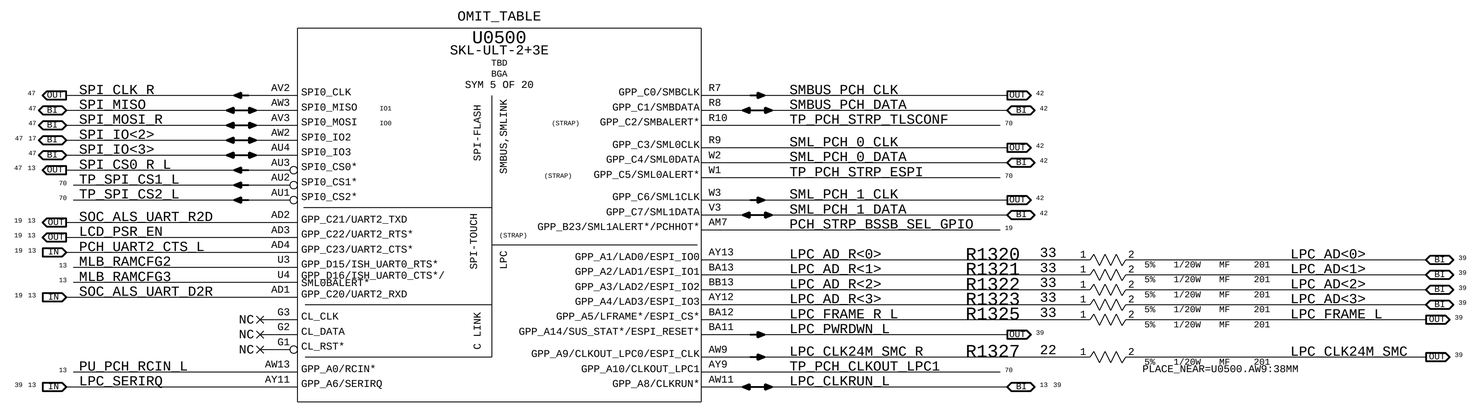
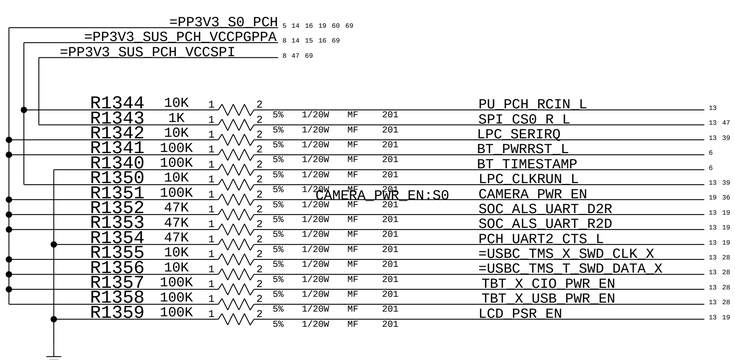
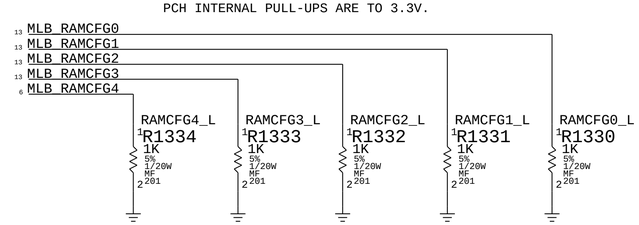






MEMORY CONFIGURATION STRAPS.

PCH INTERNAL PULL-UPS ARE TO 3.3V.



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L,RAMCFG0_L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PCH Audio/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER 051-02265 | SIZE D
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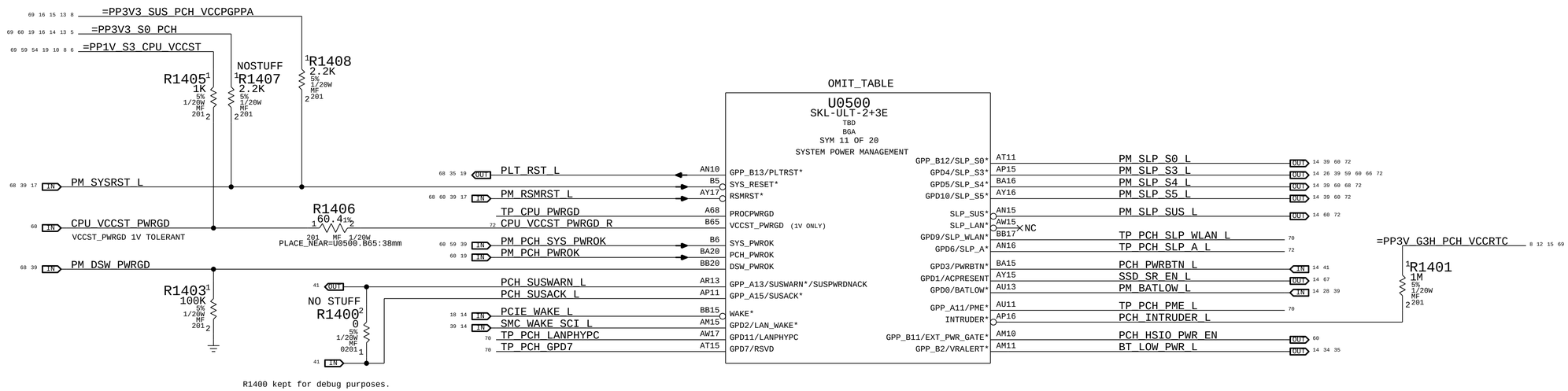
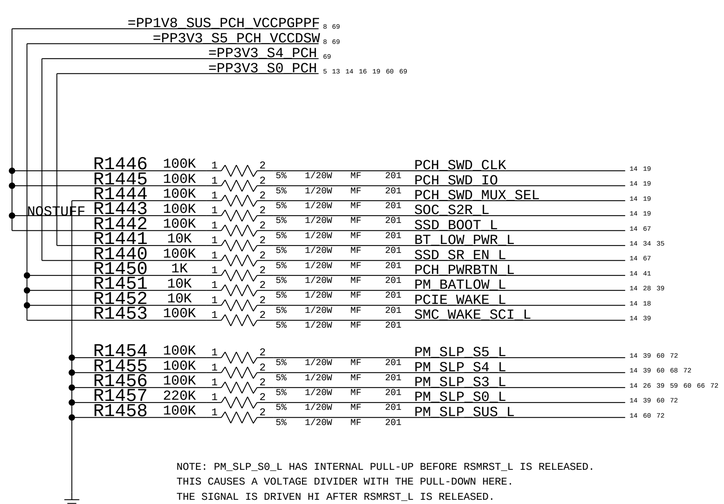
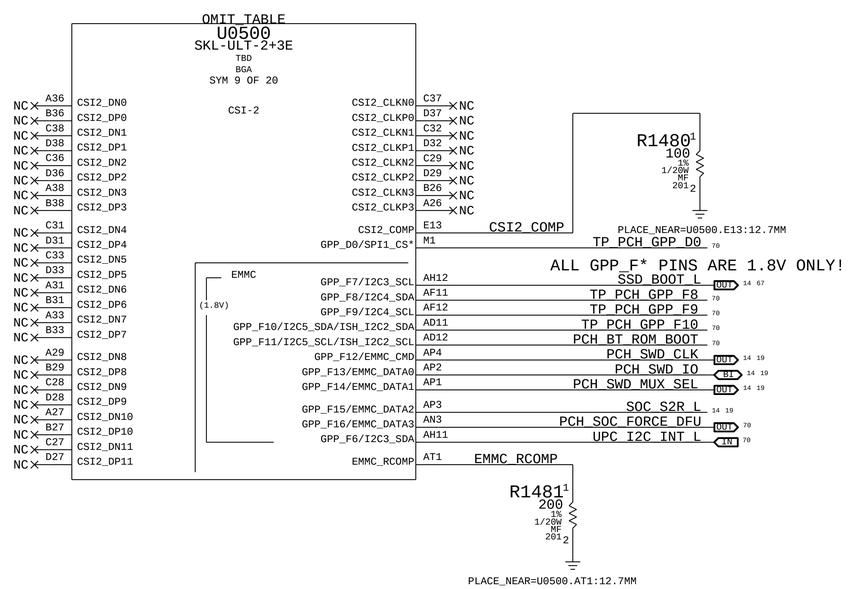
PCH Reset Button







BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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PCH Power Management

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PCIe Port Assignments:

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 8 OF 20

Signal	Pin	Dir	Lane
PCIE_SSD_D2R_N<0>	H13	IN	SSD LANE 0
PCIE_SSD_D2R_P<0>	G13	IN	SSD LANE 0
PCIE_SSD_R2D_C_N<0>	B17	OUT	SSD LANE 0
PCIE_SSD_R2D_C_P<0>	A17	OUT	SSD LANE 0
PCIE_SSD_D2R_N<1>	G11	IN	SSD LANE 1
PCIE_SSD_D2R_P<1>	F11	IN	SSD LANE 1
PCIE_SSD_R2D_C_N<1>	D16	OUT	SSD LANE 1
PCIE_SSD_R2D_C_P<1>	C16	OUT	SSD LANE 1
PCIE_SSD_D2R_N<2>	H16	IN	SSD LANE 2
PCIE_SSD_D2R_P<2>	G16	IN	SSD LANE 2
PCIE_SSD_R2D_C_N<2>	D17	OUT	SSD LANE 2
PCIE_SSD_R2D_C_P<2>	C17	OUT	SSD LANE 2
PCIE_SSD_D2R_N<3>	G15	IN	SSD LANE 3
PCIE_SSD_D2R_P<3>	F15	IN	SSD LANE 3
PCIE_SSD_R2D_C_N<3>	B19	OUT	SSD LANE 3
PCIE_SSD_R2D_C_P<3>	A19	OUT	SSD LANE 3
PCIE_TBT_X_D2R_N<0>	F16	IN	Thunderbolt X lane 0
PCIE_TBT_X_D2R_P<0>	E16	IN	Thunderbolt X lane 0
PCIE_TBT_X_R2D_C_N<0>	C19	OUT	Thunderbolt X lane 0
PCIE_TBT_X_R2D_C_P<0>	D19	OUT	Thunderbolt X lane 0
PCIE_TBT_X_D2R_N<1>	G18	IN	Thunderbolt X lane 1
PCIE_TBT_X_D2R_P<1>	F18	IN	Thunderbolt X lane 1
PCIE_TBT_X_R2D_C_N<1>	D20	OUT	Thunderbolt X lane 1
PCIE_TBT_X_R2D_C_P<1>	C20	OUT	Thunderbolt X lane 1
PCIE_TBT_X_D2R_N<2>	F20	IN	Thunderbolt X lane 2
PCIE_TBT_X_D2R_P<2>	E20	IN	Thunderbolt X lane 2
PCIE_TBT_X_R2D_C_N<2>	B21	OUT	Thunderbolt X lane 2
PCIE_TBT_X_R2D_C_P<2>	A21	OUT	Thunderbolt X lane 2
PCIE_TBT_X_D2R_N<3>	G21	IN	Thunderbolt X lane 3
PCIE_TBT_X_D2R_P<3>	F21	IN	Thunderbolt X lane 3
PCIE_TBT_X_R2D_C_N<3>	D21	OUT	Thunderbolt X lane 3
PCIE_TBT_X_R2D_C_P<3>	C21	OUT	Thunderbolt X lane 3
PCIE_AP_D2R_N	E22	IN	AirPort
PCIE_AP_D2R_P	E23	IN	AirPort
PCIE_AP_R2D_C_N	B23	OUT	AirPort
PCIE_AP_R2D_C_P	A23	OUT	AirPort
PCIE_CAMERA_D2R_N	F25	IN	CAMERA
PCIE_CAMERA_D2R_P	E25	IN	CAMERA
PCIE_CAMERA_R2D_C_N	D23	OUT	CAMERA
PCIE_CAMERA_R2D_C_P	C23	OUT	CAMERA
PCH_PCIE_RCOMP_N	F5		
PCH_PCIE_RCOMP_P	E5		
XDP_CPU_PRDY_L	D56	OUT	
XDP_CPU_PREQ_L	D61	IN	
SMC_RUNTIME_SCI_L	BB11	IN	
PCIE_TBT_T_D2R_N<0>	E28	IN	Thunderbolt T lane 0
PCIE_TBT_T_D2R_P<0>	E27	IN	Thunderbolt T lane 0
PCIE_TBT_T_R2D_C_N<0>	D24	OUT	Thunderbolt T lane 0
PCIE_TBT_T_R2D_C_P<0>	C24	OUT	Thunderbolt T lane 0
PCIE_TBT_T_D2R_N<1>	E30	IN	Thunderbolt T lane 1
PCIE_TBT_T_D2R_P<1>	F30	IN	Thunderbolt T lane 1
PCIE_TBT_T_R2D_C_N<1>	A25	OUT	Thunderbolt T lane 1
PCIE_TBT_T_R2D_C_P<1>	B25	OUT	Thunderbolt T lane 1

PCIE/USB3/SATA

Signal	Pin
PCIE1_RXN/USB3_5_RXN	
PCIE1_RXP/USB3_5_RXP	
PCIE1_TXN/USB3_5_TXN	
PCIE1_TXP/USB3_5_TXP	
PCIE2_RXN/USB3_6_RXN	
PCIE2_RXP/USB3_6_RXP	
PCIE2_TXN/USB3_6_TXN	
PCIE2_TXP/USB3_6_TXP	
PCIE3_RXN	
PCIE3_RXP	
PCIE3_TXN	
PCIE3_TXP	
PCIE4_RXN	
PCIE4_RXP	
PCIE4_TXN	
PCIE4_TXP	
PCIE5_RXN	
PCIE5_RXP	
PCIE5_TXN	
PCIE5_TXP	
PCIE6_RXN	
PCIE6_RXP	
PCIE6_TXN	
PCIE6_TXP	
PCIE7_RXN/SATA0_RXN	
PCIE7_RXP/SATA0_RXP	
PCIE7_TXN/SATA0_TXN	
PCIE7_TXP/SATA0_TXP	
PCIE8_RXN/SATA1A_RXN	
PCIE8_RXP/SATA1A_RXP	
PCIE8_TXN/SATA1A_TXN	
PCIE8_TXP/SATA1A_TXP	
PCIE9_RXN	
PCIE9_RXP	
PCIE9_TXN	
PCIE9_TXP	
PCIE10_RXN	
PCIE10_RXP	
PCIE10_TXN	
PCIE10_TXP	
PCIE_RCOMPN	
PCIE_RCOMPP	
PROC_PRDY*	
PROC_PREQ*	
GPP_A7/PIRQA*	
PCIE11_RXN/SATA1B_RXN	
PCIE11_RXP/SATA1B_RXP	
PCIE11_TXN/SATA1B_TXN	
PCIE11_TXP/SATA1B_TXP	
PCIE12_RXN/SATA2_RXN	
PCIE12_RXP/SATA2_RXP	
PCIE12_TXN/SATA2_TXN	
PCIE12_TXP/SATA2_TXP	

SSIC/USB3

Signal	Pin	Dir	Note
USB3_1_RXN	H8	IN	USB3 EXTA D2R N
USB3_1_RXP	G8	IN	USB3 EXTA D2R P
USB3_1_TXN	C13	OUT	USB3 EXTA R2D C N
USB3_1_TXP	D13	OUT	USB3 EXTA R2D C P
USB3_2_RXN/SSIC_RXN	J6	IN	USB3 EXTB D2R N
USB3_2_RXP/SSIC_RXP	H6	IN	USB3 EXTB D2R P
USB3_2_TXN/SSIC_TXN	B13	OUT	USB3 EXTB R2D C N
USB3_2_TXP/SSIC_TXP	A13	OUT	USB3 EXTB R2D C P
USB3_3_RXN	J10		TP_USB3_03_D2RN
USB3_3_RXP	H10		TP_USB3_03_D2RP
USB3_3_TXN	B15		TP_USB3_03_R2DN
USB3_3_TXP	A15		TP_USB3_03_R2DP
USB3_4_RXN	E10		TP_USB3_04_D2RN
USB3_4_RXP	F10		TP_USB3_04_D2RP
USB3_4_TXN	C15		TP_USB3_04_R2DN
USB3_4_TXP	D15		TP_USB3_04_R2DP

EXT A (SS,DCI)

EXT B (SS)

USB2

Signal	Pin	Note
USB2N_1	AB9	USB_EXTA_N
USB2P_1	AB10	USB_EXTA_P
USB2N_2	AD6	USB_EXTB_N
USB2P_2	AD7	USB_EXTB_P
USB2N_3	AH3	USB_CAMERA_DFR_N
USB2P_3	AJ3	USB_CAMERA_DFR_P
USB2N_4	AD9	TP_USB_TESTERN
USB2P_4	AD10	TP_USB_TESTERP
USB2N_5	AJ1	NC_USB2_05N
USB2P_5	AJ2	NC_USB2_05P
USB2N_6	AF6	NC_USB2_06N
USB2P_6	AF7	NC_USB2_06P
USB2N_7	AH1	NC_USB2_07N
USB2P_7	AH2	NC_USB2_07P
USB2N_8	AF8	NC_USB2_08N
USB2P_8	AF9	NC_USB2_08P
USB2N_9	AG1	NC_USB2_09N
USB2P_9	AG2	NC_USB2_09P
USB2N_10	AH7	NC_USB2_10N
USB2P_10	AH8	NC_USB2_10P
USB2_COMP	AB6	PCH_USB2_COMP
USB2_ID	AG3	
USB2_VBUSSENSE	AG4	PCH_USB2_VBUSSENSE

EXT A (LS/FS/HS)

EXT B (LS/FS/HS)

GROUNDED PER SKYLAKE MOW 2015WW10.

Signal	Pin	Dir
GPP_E3/CPU_GP0	A6	IN
GPP_E4/DEVSLP0	J1	IN
GPP_E5/DEVSLP1	J2	IN
GPP_E6/DEVSLP2	J3	IN
GPP_D22/SPI1_IO3	V2	IN
GPP_D23/I2S_MCLK	J5	IN
GPP_E0/SATAXPCIE0/SATAGP0	H2	IN
GPP_D18/DMIC_DATA1	C8	IN
GPP_D19/DMIC_CLK0	H5	IN
GPP_D20/DMIC_DATA0	D7	IN
GPP_E2/SATAXPCIE2/SATAGP2	G4	IN

Signal	Pin
XDP_PCH_OBSFN_C1	
XDP_JTAG_ISP_TCK	
XDP_JTAG_ISP_TDI	
XDP_PCH_OBSDATA_A2	
SPKR_ID0	
XDP_PCH_OBSDATA_D0	
XDP_PCH_OBSDATA_D1	
XDP_PCH_OBSDATA_C1	
XDP_PCH_OBSDATA_C2	
XDP_PCH_OBSDATA_C3	
XDP_PCH_OBSDATA_D3	

R1504 100 1% 1/20W MF 201 — PLACE_NEAR=U0500.F5:12.7mm

R1503 1K 5% 1/20W MF 201 — PLACE_NEAR=U0500.AG4:12.7MM

R1501 113 1% 1/20W MF 201 — PLACE_NEAR=U0500.AB6:12.7MM

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 10 OF 20

CLOCK SIGNALS

ANY CLKREQ CAN MAP TO ANY CLK.
ANY CLKREQ OR CLK CAN MAP TO ANY PCIE PORT.
UNUSED CLKREQS AND CLKS SHOULD BE DISABLED.
PER SKYLAKE PDG, SKYLAKE PCH EDS.

Signal	Pin	Dir
PCIE_CLK100M_SSD_N	D42	OUT
PCIE_CLK100M_SSD_P	C42	OUT
=SSD_CLKREQ_L	AR10	IN
PCIE_CLK100M_TBT_X_N	B42	OUT
PCIE_CLK100M_TBT_X_P	A42	OUT
=TBT_X_CLKREQ_L	AT7	IN
PCIE_CLK100M_TBT_T_N	D41	OUT
PCIE_CLK100M_TBT_T_P	C41	OUT
=TBT_T_CLKREQ_L	AT8	IN
PCIE_CLK100M_AP_N	D40	OUT
PCIE_CLK100M_AP_P	C40	OUT
=AP_CLKREQ_L	AT10	IN
PCIE_CLK100M_CAMERA_N	B40	OUT
PCIE_CLK100M_CAMERA_P	A40	OUT
=CAMERA_CLKREQ_L	AU8	IN
TP_PCIE_CLK100M5N	E40	
TP_PCIE_CLK100M5P	E38	
TP_PCH_CLKREQ5_L	AU7	

Signal	Pin	Dir
CLKOUT_PCIE_N0		
CLKOUT_PCIE_P0		
GPP_B5/SRCCLKREQ0*		
CLKOUT_PCIE_N1		
CLKOUT_PCIE_P1		
GPP_B6/SRCCLKREQ1*		
CLKOUT_PCIE_N2		
CLKOUT_PCIE_P2		
GPP_B7/SRCCLKREQ2*		
CLKOUT_PCIE_N3		
CLKOUT_PCIE_P3		
GPP_B8/SRCCLKREQ3*		
CLKOUT_PCIE_N4		
CLKOUT_PCIE_P4		
GPP_B9/SRCCLKREQ4*		
CLKOUT_PCIE_N5		
CLKOUT_PCIE_P5		
GPP_B10/SRCCLKREQ5*		
CLKOUT_ITPXDP_N	F43	
CLKOUT_ITPXDP_P	E43	
GPD8/SUSCLK	BA17	
XTAL24_IN	E37	
XTAL24_OUT	E35	
XCLK_BIASREF	E42	
RTCX1	AM18	
RTCX2	AM20	
SRTCRST*	AN18	
RTCRST*	AM16	

Signal	Pin	Dir
TP_ITPXDP_CLK100MN		
TP_ITPXDP_CLK100MP		
PM_CLK32K_SUSCLK_R		OUT
PCH_CLK24M_XTALIN		IN
PCH_CLK24M_XTALOUT		OUT
PCH_DIFFCLK_BIASREF		
PCH_CLK32K_RTCX1		IN
PCH_CLK32K_RTCX2		OUT
PCH_SRTCRST_L		
RTC_RESET_L		

=PP1V_SUS_PCH_VCCAPLL — PLACE_NEAR=U0500.E42:2.54mm — R1520 2.7K 1% 1/20W MF 201

=PP3V_G3H_PCH_VCCRTC — R1530 20K 1% 1/20W MF 201 — R1531 20K 1% 1/20W MF 201

C1530 1UF 20% 6.3V X6S-CERM 0201 — C1531 1UF 20% 6.3V X6S-CERM 0201

=PP3V3_SUS_PCH_VCCPGPPA — R1550 100K 5% 1/20W MF 201 — SMC_RUNTIME_SCI_L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PCH PCIE/USB/CLKS

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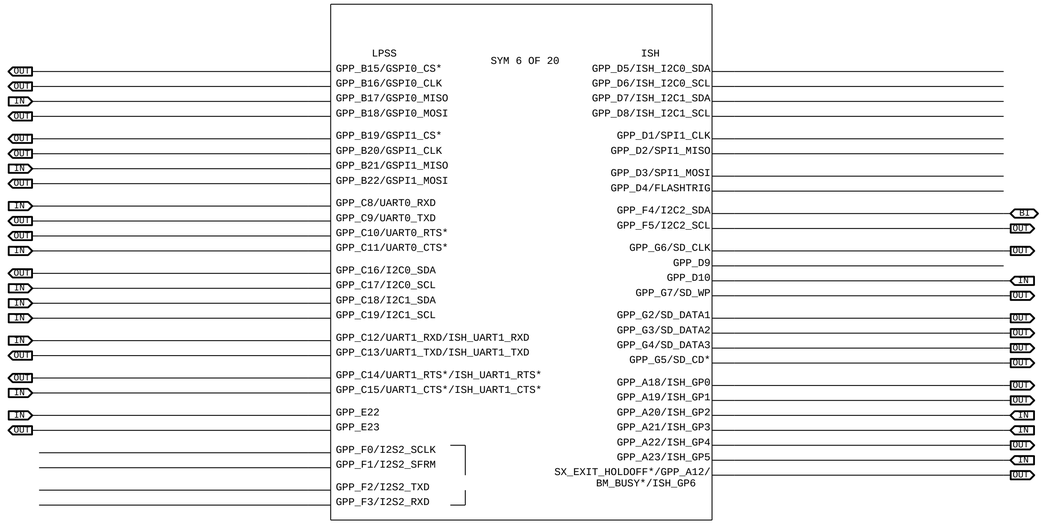

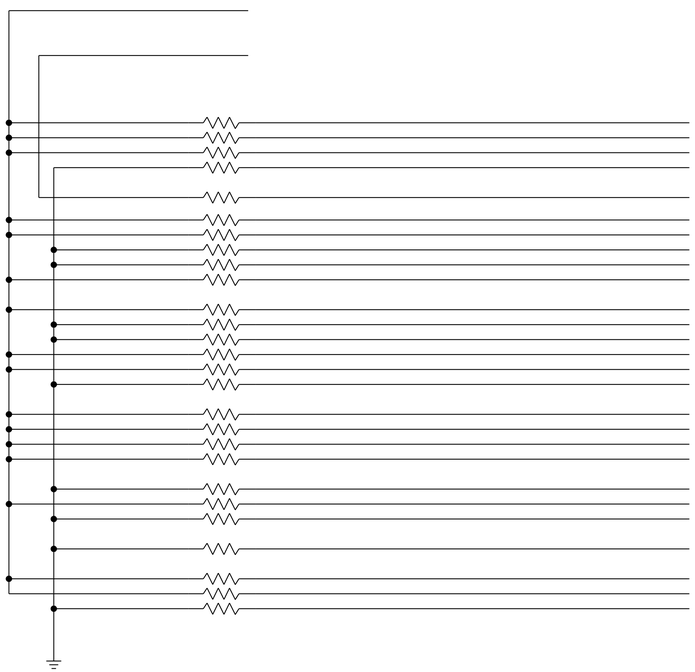

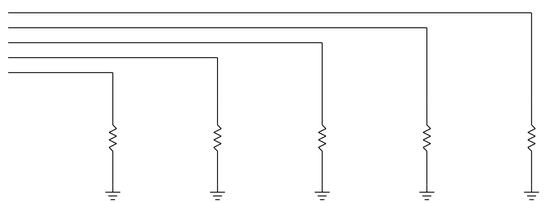

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION

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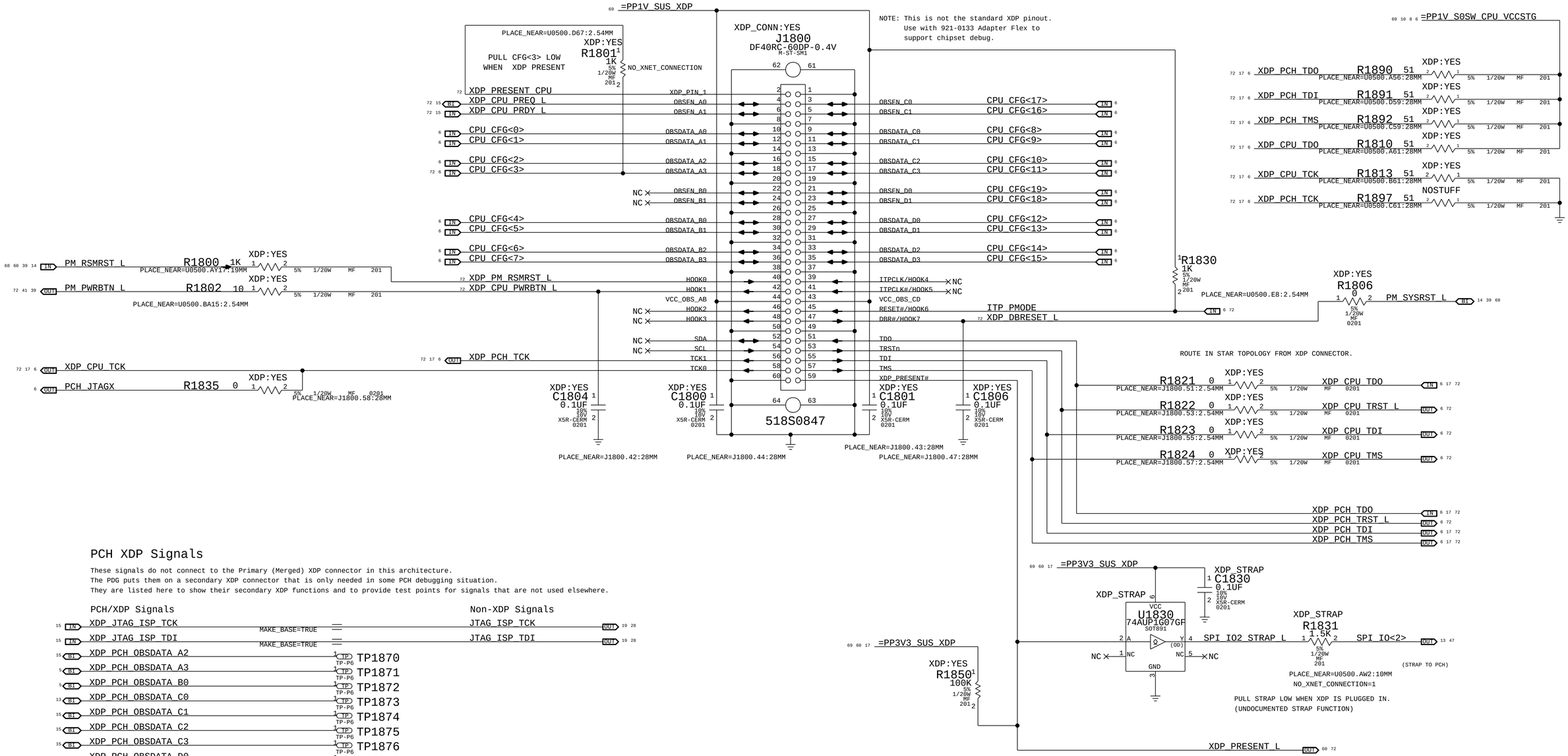
Primary / Merged (CPU/PCH) Micro2-XDP



PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals			Non-XDP Signals
XDP_JTAG_ISP_TCK	MAKE_BASE=TRUE		JTAG_ISP_TCK
XDP_JTAG_ISP_TDI	MAKE_BASE=TRUE		JTAG_ISP_TDI
XDP_PCH_OBSDATA_A2		TP1870	
XDP_PCH_OBSDATA_A3		TP1871	
XDP_PCH_OBSDATA_B0		TP1872	
XDP_PCH_OBSDATA_C0		TP1873	
XDP_PCH_OBSDATA_C1		TP1874	
XDP_PCH_OBSDATA_C2		TP1875	
XDP_PCH_OBSDATA_C3		TP1876	
XDP_PCH_OBSDATA_D0		TP1877	
XDP_PCH_OBSDATA_D1		TP1878	
XDP_PCH_OBSDATA_D2		TP1879	
XDP_PCH_OBSDATA_D3		TP1880	
XDP_PCH_OBSFN_C1		TP1881	
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE		USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE		USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	MAKE_BASE=TRUE		USB_EXTC_OC_L
XDP_USB_EXTD_OC_L	MAKE_BASE=TRUE		USB_EXTD_OC_L

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

BOM_COST_GROUP=DEBUG

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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CPU/PCH Merged XDP

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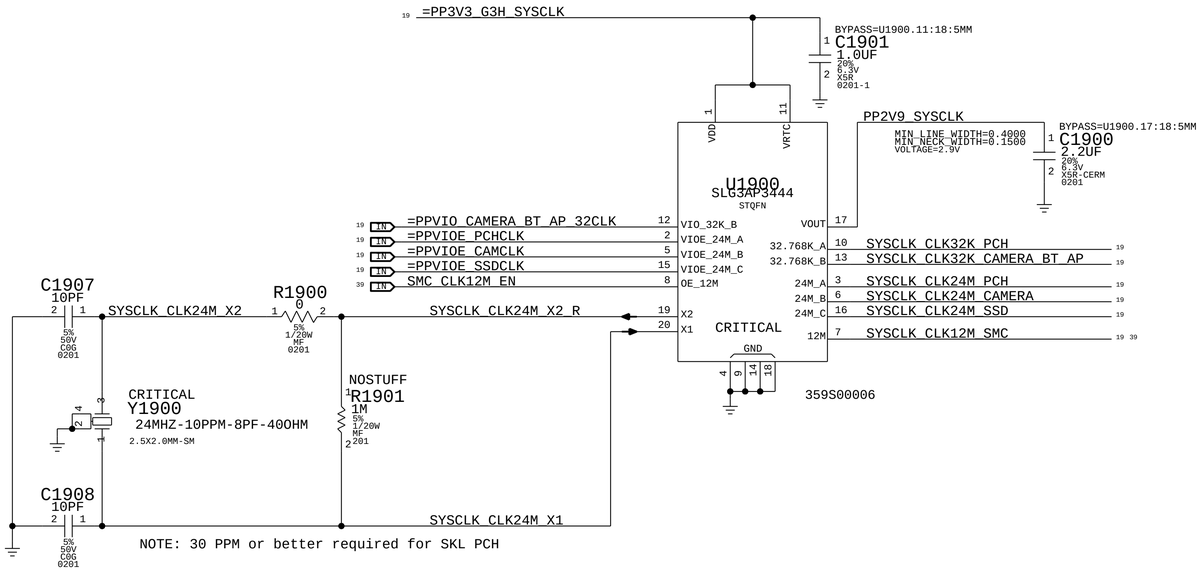
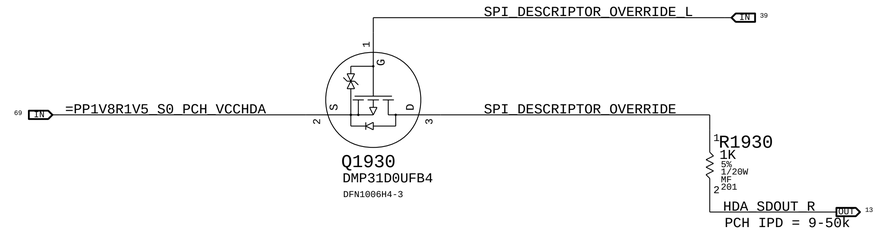
System 32kHz / 12MHz / 24MHz Clock Generator

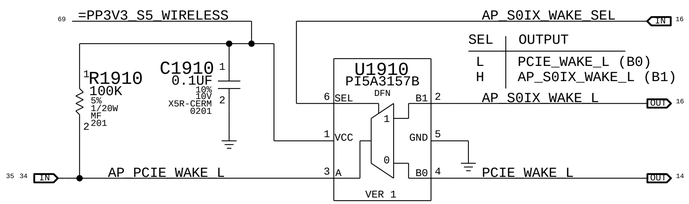


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

BOM_COST_GROUP=CPU & CHIPSET

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OPTION STRAPS

PROJECT DEPENDANT

STUFF PULL-UPS TO ENABLE INTERNAL GPU DP PORTS.
NOSTUFF / DELETE TO ALLOW INTERNAL PULL-DOWNS TO DISABLE.

=PP3V3_S0_PCH 5 13 14 16 19 60 69

R2020 2.2K 5% 1/20W MF 201 — IG_DDI1_EN (STRAP-OPTION) — PCH_DDPB_CTRLDATA 13
R2021 2.2K 5% 1/20W MF 201 — IG_DDI2_EN (STRAP-OPTION) — PCH_DDPC_CTRLDATA 13

STUFF PULL-UP TO ENABLE BSSB (DCI) CLK/DI ON GPP_D11, _D12.
NOSTUFF / DELETE TO ALLOW INTERNAL PULL-DOWN FOR BSSB ON USB-SS.

=PP3V3_SUS_PCH_VCCPGPPB 8 12 69

R2022 1K 5% 1/20W MF 201 — BSSB_ON_GPIOS (STRAP-OPTION) — PCH_STRP_BSSB_SEL_GPIO 13

GREENCLK CLOCK CONNECTIONS.

18 =PP3V3_G3H_SYSCLK — PP3V3_G3H 28 41 42 47 51 52 53 60 68 69 72

19 18 =PPVIO_CAMERA_BT_AP_32CLK — PPVIO_BT_AP_32CLK (MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.1000; MIN_NECK_WIDTH=0.0800) — =PP3V3_S4_WLAN 34 69

BT_CLK32K:YES
R2030 0 5% 1/20W MF 0201

BT_CLK32K:NO
R2031[1] 100K 5% 1/20W MF 201

XW2000 SM

18 =PPVIOE_SSDCLK — PD_PPVIOE_SSDCLK (MAKE_BASE=TRUE)

XW2002 SM

19 18 =PPVIOE_CAMCLK — PPVIOE_CAMCLK (MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.1000; MIN_NECK_WIDTH=0.0800) — =PPVDDIO_S0_CAMCLK 36

PCH 24MHz VIOE Options

XW2065 SM

72 69 64 63 62 PP1V_S5G — PP1V_S5G_PCHCLK (VOLTAGE=1V; MIN_LINE_WIDTH=0.1000; MIN_NECK_WIDTH=0.0800)

PCH24M:SUS
R2065 0 5% 1/20W MF 0201 — =PPVIOE_PCHCLK 18 19

PP1V_SUSRS0SW_PCHCLK (VOLTAGE=1V; MIN_LINE_WIDTH=0.1000; MIN_NECK_WIDTH=0.0800; MAKE_BASE=TRUE)

PCH24M:S0SW
R2066 0 5% 1/20W MF 0201 — PP1V_S0SW_PCHCLK (VOLTAGE=1V; MIN_LINE_WIDTH=0.1000; MIN_NECK_WIDTH=0.0800)

PCH24M:S0SW
Q2065 DMN32D2LFB4 SYM VER 3 DEN1006H4-3 CRITICAL
PM_SLP_S0S3_L IN 60 68 72

19 18 =PPVIO_CAMERA_BT_AP_32CLK 18 19
=PPVIOE_PCHCLK 18 19
=PPVIOE_CAMCLK 18 19

BYPASS=U1900.12:18:5MM
BYPASS=U1900.02:18:5MM
BYPASS=U1900.05:18:5MM

C2004 0.1UF 10% 10V X5R-CERM 0201
C2005 0.1UF 10% 10V X5R-CERM 0201
C2006 0.1UF 10% 10V X5R-CERM 0201

18 IN SYSCLK_CLK32K_PCH — PCH_CLK32K_RTCX1 OUT 15
70 (MAKE_BASE=TRUE) TP_PCH_CLK32K_RTCX2 — PCH_CLK32K_RTCX2 IN 15

BT_CLK32K:YES
R2032 0 5% 1/20W MF 0201

18 IN SYSCLK_CLK32K_CAMERA_BT_AP — SYSCLK_CLK32K_BT_AP OUT 34
SYSCLK_CLK32K_BT_AP_R (MAKE_BASE=TRUE)

18 IN SYSCLK_CLK24M_PCH — PCH_CLK24M_XTALIN OUT 15
70 (MAKE_BASE=TRUE) TP_PCH_CLK24M_XTALOUT — PCH_CLK24M_XTALOUT IN 15

18 IN SYSCLK_CLK24M_SSD — TP_SYSCLK_CLK24M_SSD (MAKE_BASE=TRUE) 70

18 IN SYSCLK_CLK24M_CAMERA — CLK25M_CAM_CLKP (MAKE_BASE=TRUE) OUT 36

39 18 IN SYSCLK_CLK12M_SMC OUT

=PP3V3_S0_PCH 5 13 14 16 19 60 69

R2071 47K 5% 1/20W MF 201 — SSD_CLKREQ_L 19 67
R2072 47K 5% 1/20W MF 201 — TBT_X_CLKREQ_L 19 26
R2074 47K 5% 1/20W MF 201 — AP_CLKREQ_L 19 34 35
R2075 47K 5% 1/20W MF 201 — CAMERA_CLKREQ_L 19 36

SERIES R FOR VOLTAGE DIVIDER WHEN PCH IS DRIVING IN L1 SUB-STATE.

15 OUT =SSD_CLKREQ_L — SSD_CLKREQ_R_L (MAKE_BASE=TRUE) — R2001 1K 1/20W 5% 201 MF — SSD_CLKREQ_L IN 19 67
15 OUT =AP_CLKREQ_L — AP_CLKREQ_R_L (MAKE_BASE=TRUE) — R2002 1K 1/20W 5% 201 MF — AP_CLKREQ_L IN 19 34 35
15 OUT =CAMERA_CLKREQ_L — CAMERA_CLKREQ_R_L (MAKE_BASE=TRUE) — R2003 1K 1/20W 5% 201 MF — CAMERA_CLKREQ_L IN 19 36
15 OUT =TBT_X_CLKREQ_L — TBT_X_CLKREQ_R_L (MAKE_BASE=TRUE) — R2004 1K 1/20W 5% 201 MF — TBT_X_CLKREQ_L IN 19 26

UNUSED PCH XDP SIGNALS NEED TEST POINTS.

28 17 IN JTAG_ISP_TCK — TP2070 (TP-P6)
28 17 IN JTAG_ISP_TDI — TP2071 (TP-P6)
17 IN USB_EXTD_OC_L — TP2072 (TP-P6)
17 IN USB_EXTC_OC_L — TP2073 (TP-P6)

EXTRA BPM TESTPOINTS

6 IN XDP_BPM_L<1> — (MAKE_BASE=TRUE) — TP_XDP_BPM_L<1> 70
6 IN XDP_BPM_L<2> — (MAKE_BASE=TRUE) — TP_XDP_BPM_L<2> 70
6 IN XDP_BPM_L<3> — (MAKE_BASE=TRUE) — TP_XDP_BPM_L<3> 70

IFDIM TRIGGERS USING R2055 & R2056 PADS
ASK DC/DC GROUP FOR DETAILS.

6 IN XDP_BPM_L<0> — NOSTUFF R2055 100K 5% 1/16W MF-LF 402
6 IN TP_CPU_RSVD_AK13 — (MAKE_BASE=TRUE) — CPU_RSVD_AK13 — NOSTUFF R2056 100K 5% 1/16W MF-LF 402

UNUSED GPIO SIGNALS

16 IN SOC_UART_D2R — (MAKE_BASE=TRUE) — PU_SOC_UART_D2R
16 IN SOC_UART_R2D — (MAKE_BASE=TRUE) — PU_SOC_UART_R2D
16 IN SOC_UART_RTS_L — (MAKE_BASE=TRUE) — PU_SOC_UART_RTS_L
16 IN SOC_UART_CTS_L — (MAKE_BASE=TRUE) — PD_SOC_UART_CTS_L
16 IN TBT_T_PLUG_EVENT_L — (MAKE_BASE=TRUE) — PU_TBT_T_PLUG_EVENT_L
14 IN PCH_SWD_CLK — (MAKE_BASE=TRUE) — PU_PCH_SWD_CLK
14 BI PCH_SWD_IO — (MAKE_BASE=TRUE) — PU_PCH_SWD_IO
14 IN PCH_SWD_MUX_SEL — (MAKE_BASE=TRUE) — PD_PCH_SWD_MUX_SEL
13 IN LCD_PSR_EN — (MAKE_BASE=TRUE) — PD_LCD_PSR_EN
16 IN AUD_SPI_CS_L — (MAKE_BASE=TRUE) — PU_AUD_SPI_CS_L
16 IN AUD_SPI_CLK — (MAKE_BASE=TRUE) — PD_AUD_SPI_CLK
16 OUT AUD_SPI_MISO — (MAKE_BASE=TRUE) — PD_AUD_SPI_MISO
16 IN AUD_SPI_MOSI — (MAKE_BASE=TRUE) — PU_AUD_SPI_MOSI
15 OUT SPKR_ID0 — (MAKE_BASE=TRUE) — TP_SPKR_ID0 70
16 OUT SPKR_ID1 — (MAKE_BASE=TRUE) — TP_SPKR_ID1

13 IN CAMERA_PWR_EN_PCH — R2060 0 5% 1/20W MF 0201 — CAMERA_PWR_EN OUT 13 19 36

69 59 54 14 10 8 6 =PP1V_S3_CPU_VCCST — R2061 51 5% 1/20W MF 201 — 68 39 6 OUT CPU_CATERR_L

14 IN SOC_S2R_L — (MAKE_BASE=TRUE) — SOC_WAKE_L

69 60 19 16 14 13 5 =PP3V3_S0_PCH
C2040 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
U2040 74LVC1G08 SOT891

60 14 IN PM_PCH_PWROK — 08 — 4 PM_PCH_PWROK_BUF
NC

R2040 100K 5% 1/20W MF 201 — AUD_PWR_EN 16 49
R2041 100K 5% 1/20W MF 201 — CAMERA_PWR_EN 13 19 36

BOM_COST_GROUP=CPU & CHIPSET

RESETS

68 35 14 IN PLT_RST_L
R2014[1] 470K 5% 1/20W MF 201

R2010 100K 5% 1/20W MF 201 — CAMERA_RESET_L OUT 13 36
R2011 100K 5% 1/20W MF 201 — AP_RESET_L OUT 16 34 35
R2012 100K 5% 1/20W MF 201 — SSD_RESET_L OUT 16 67
R2013 100K 5% 1/20W MF 201 — TBT_X_PCI_RESET_L OUT 16 19 28
R2015 33 5% 1/20W MF 201 — SMC_LRESET_L OUT 39

26 PM_PLT_RST_TBT_X_L — TBT_X_PCI_RESET_L (MAKE_BASE=TRUE) 16 19 28

S3X SSD CONTROL

PCH — S3X SSD DOWN

60 OUT SSD_PWR_REQ — STORAGE_LATCH (MAKE_BASE=TRUE) IN 67

UNUSED GPIO SIGNALS

13 IN SOC_ALS_UART_R2D — PU_SSD_UART_R2D (MAKE_BASE=TRUE)
13 OUT SOC_ALS_UART_D2R — PU_SSD_UART_D2R (MAKE_BASE=TRUE)
13 IN PCH_UART2_CTS_L — PD_SSD_UART_CTS_L (MAKE_BASE=TRUE)

PROBE POINTS

28 15 IN PCIE_TBT_X_R2D_C_P<0>
28 15 IN PCIE_TBT_X_R2D_C_N<0>

NO_XNET_CONNECTION=1
NOSTUFF
PLACE_NEAR=C3040.1:1MM
C2090 0.22UF 20% 6.3V X5R 0201 — TBTXR2DP0 PLACE_NEAR=C2090.2:1MM — R2090 51 5% 1/20W MF 201 — NOSTUFF
C2091 0.22UF 20% 6.3V X5R 0201 — TBTXR2DN0 PLACE_NEAR=C3040.1:1MM — R2091 51 5% 1/20W MF 201 — NOSTUFF

28 26 OUT DP_X_SNK1_ML_C_P<0>
28 26 IN DP_X_SNK1_ML_C_N<0>

NO_XNET_CONNECTION=1
NOSTUFF
PLACE_NEAR=C3040.1:1MM
C2092 0.1UF 10% 10V X5R-CERM 0201 — DPX1P0 PLACE_NEAR=C2090.2:6MM — R2092 51 5% 1/20W MF 201 — NOSTUFF
C2093 0.1UF 10% 10V X5R-CERM 0201 — DPX1N0 PLACE_NEAR=C2090.2:5MM — R2093 51 5% 1/20W MF 201 — NOSTUFF

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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Chipset Support 2

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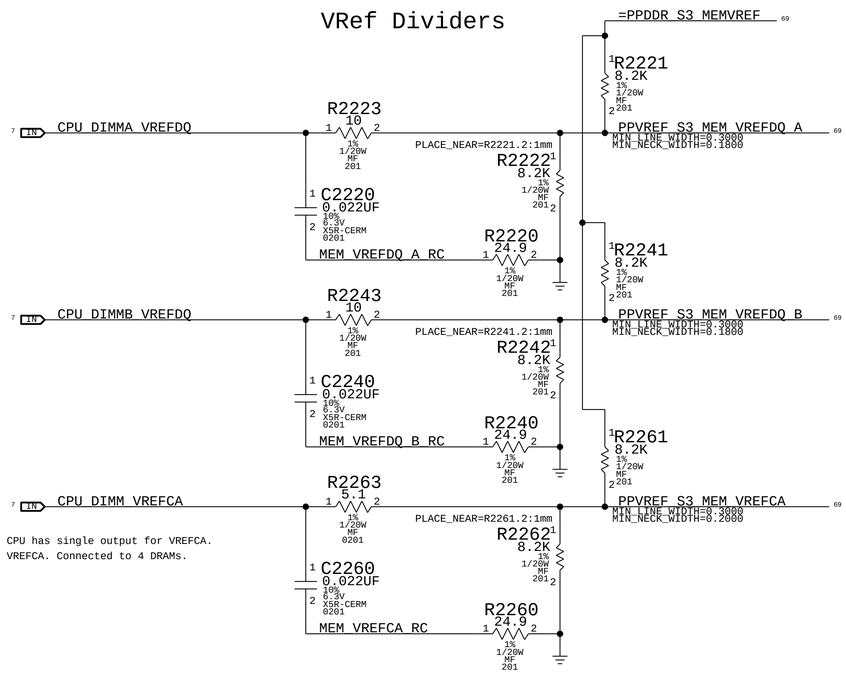
CPU-Based Margining

VRef Dividers



NOTE: CPU has single output for VREFCA.
VREFCA. Connected to 4 DRAMs.

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 VREF Margining

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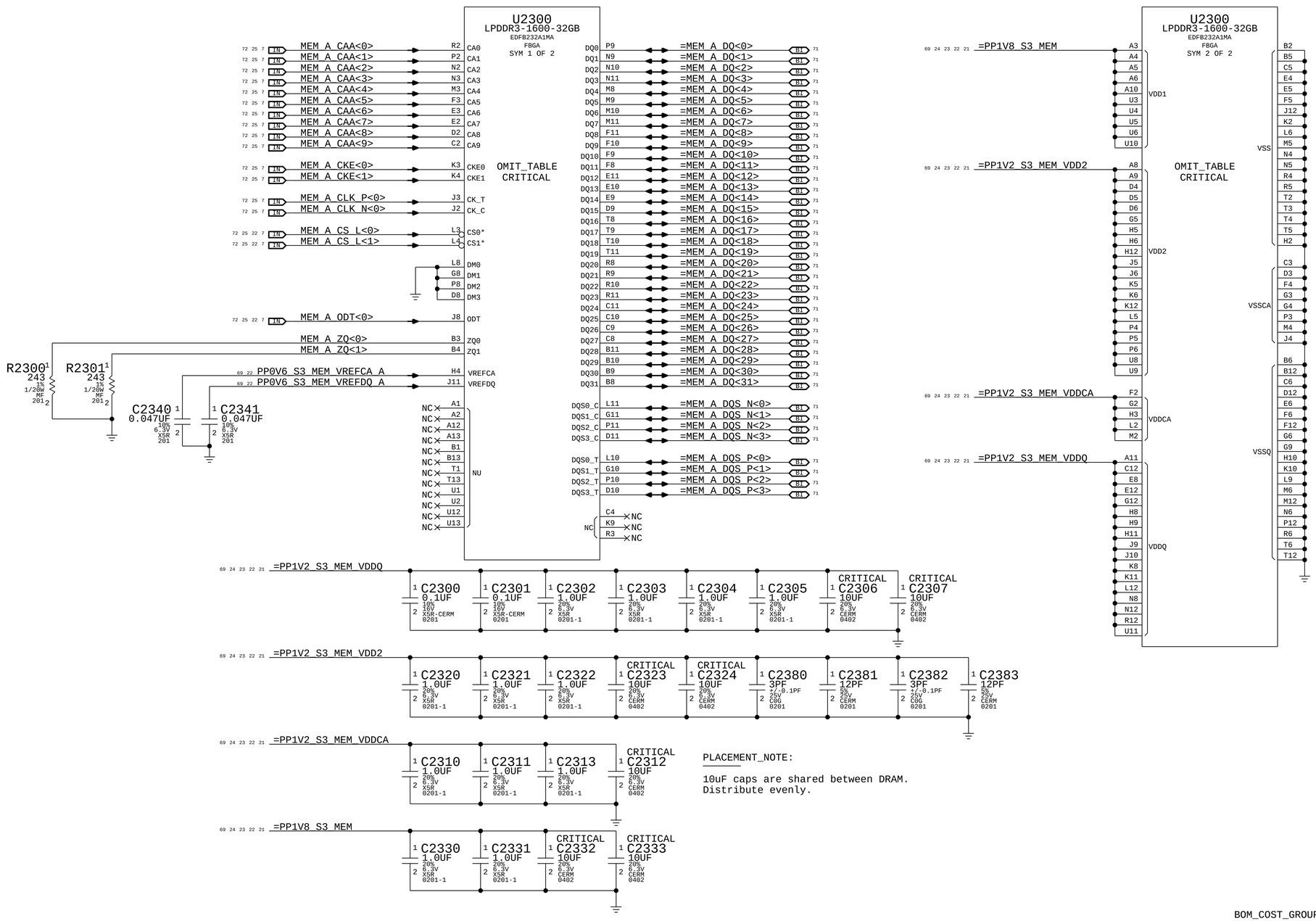
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 DRAM Channel A (00-31)

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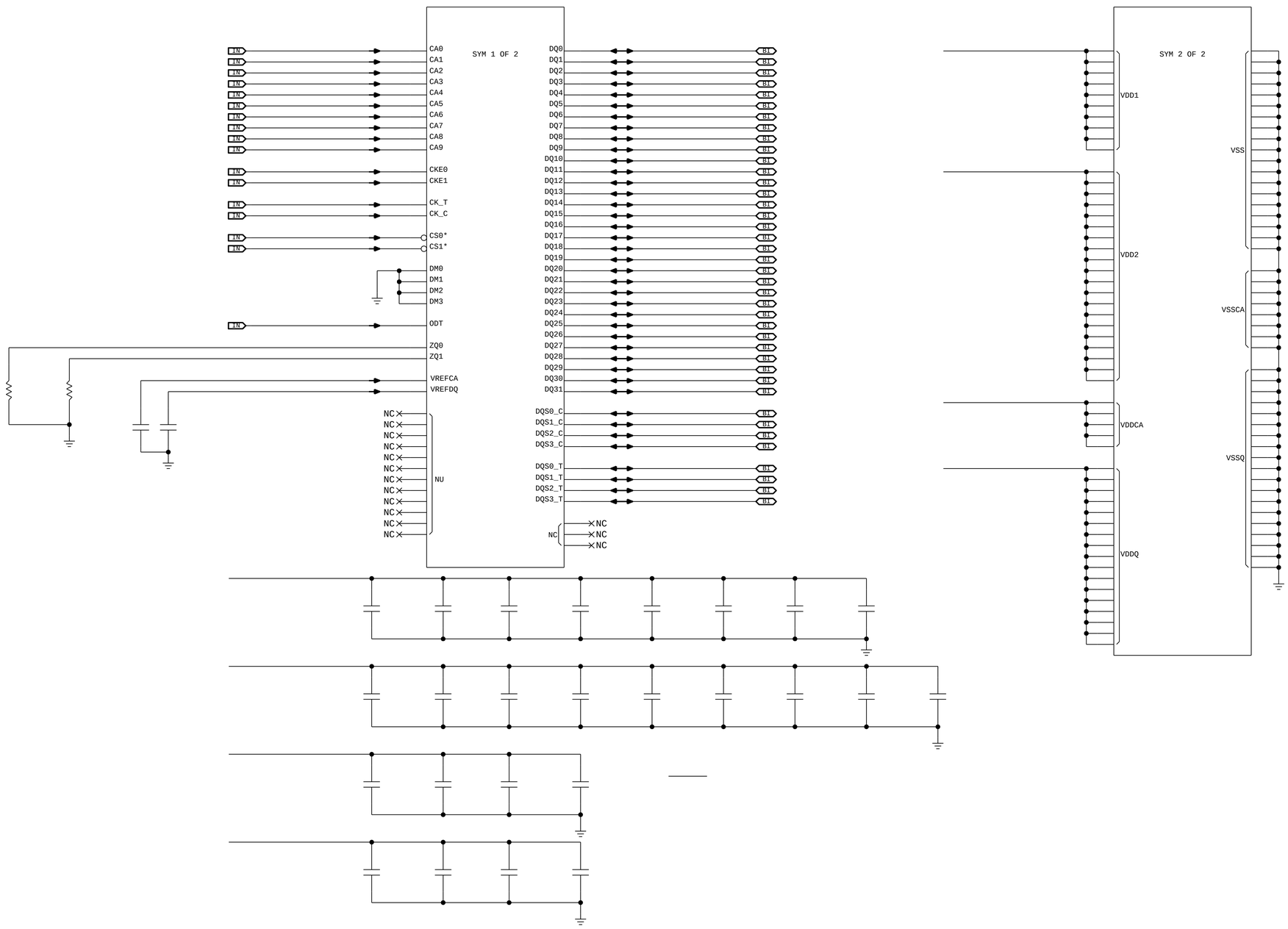

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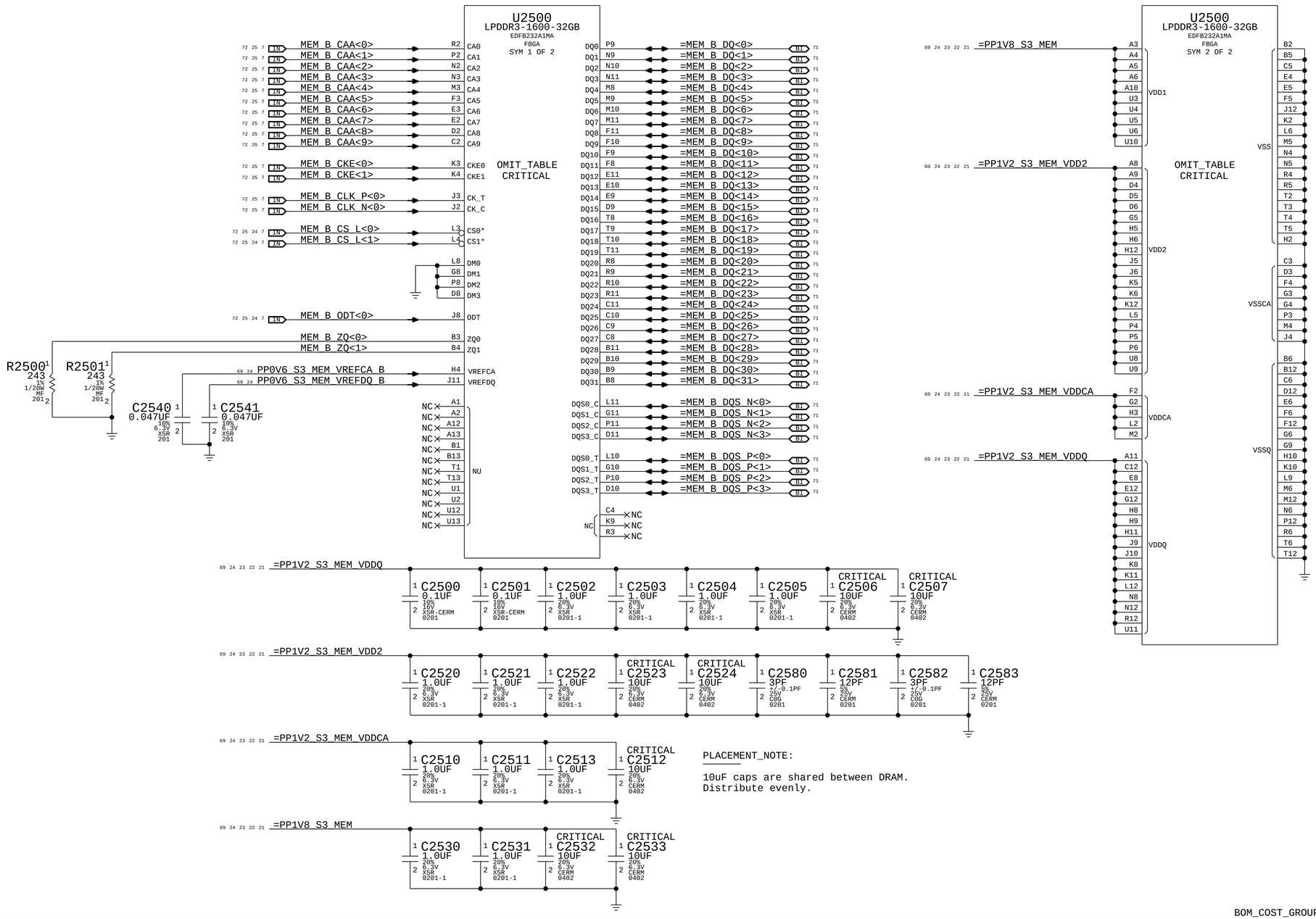
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 DRAM Channel B (00-31)

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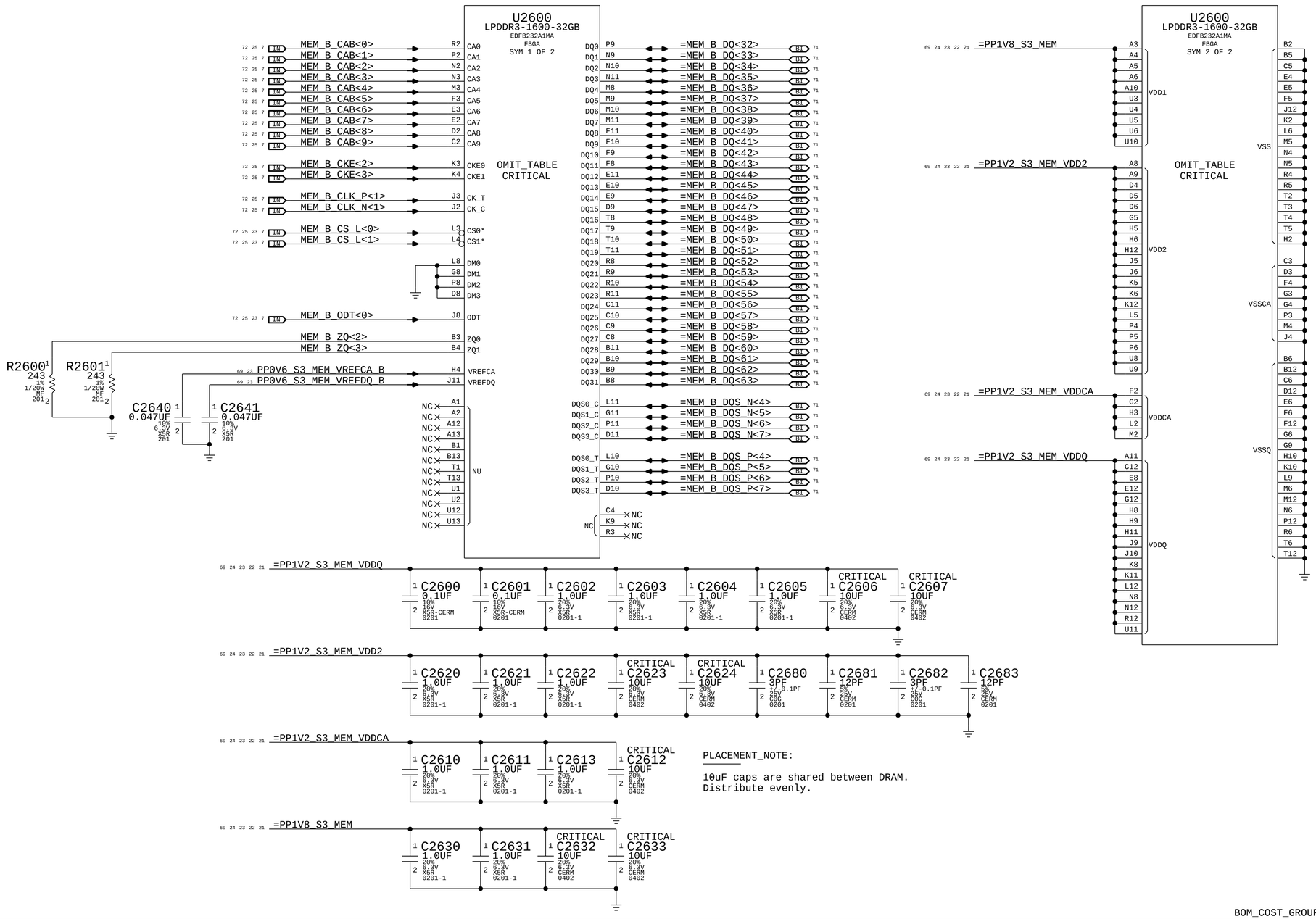
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

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Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

69 =PP0V6_S0_MEM_VTT_A

72 21 7	IN	MEM_A_CAA<9>	R2700	68	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CAA<8>	R2701	68	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CAA<6>	R2702	68	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CAA<7>	R2703	68	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CAA<5>	R2704	68	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CLK_P<0>	R2705	39	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CLK_N<0>	R2706	39	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CKE<1>	R2707	82	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CKE<0>	R2708	82	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CAA<4>	R2709	68	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CAA<3>	R2710	68	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CAA<2>	R2711	68	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CAA<1>	R2712	68	1%	1/20W	201	MF
72 21 7	IN	MEM_A_CAA<0>	R2713	68	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CAB<9>	R2714	68	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CAB<8>	R2715	68	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CAB<6>	R2716	68	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CAB<7>	R2717	68	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CAB<5>	R2718	68	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CLK_P<1>	R2719	39	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CLK_N<1>	R2720	39	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CKE<2>	R2721	82	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CKE<3>	R2722	82	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CAB<4>	R2723	68	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CAB<2>	R2724	68	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CAB<3>	R2725	68	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CAB<1>	R2726	68	1%	1/20W	201	MF
72 22 7	IN	MEM_A_CAB<0>	R2727	68	1%	1/20W	201	MF
72 22 21 7	IN	MEM_A_CS_L<0>	R2728	82	1%	1/20W	201	MF
72 22 21 7	IN	MEM_A_CS_L<1>	R2729	82	1%	1/20W	201	MF
72 22 21 7	IN	MEM_A_ODT<0>	R2730	82	1%	1/20W	201	MF

C2700	0.47UF	20% 4V CERM-X5R-1 201	C2730	12PF 5% 25V CERM 0201
C2701	0.47UF	20% 4V CERM-X5R-1 201	C2702	0.47UF 20% 4V CERM-X5R-1 201
C2703	0.47UF	20% 4V CERM-X5R-1 201	C2704	0.47UF 20% 4V CERM-X5R-1 201
C2705	0.47UF	20% 4V CERM-X5R-1 201	C2706	0.47UF 20% 4V CERM-X5R-1 201
C2707	0.47UF	20% 4V CERM-X5R-1 201	C2708	0.47UF 20% 4V CERM-X5R-1 201
C2709	0.47UF	20% 4V CERM-X5R-1 201	C2722	3PF +/-0.1PF 25V C0G 0201
CRITICAL C2720	20UF	20% 6.3V CERM-X5R 0402	NOSTUFF CRITICAL C2721	20UF 20% 6.3V CERM-X5R 0402

69 =PP0V6_S0_MEM_VTT_B

72 23 7	IN	MEM_B_CAA<9>	R2740	68	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CAA<8>	R2741	68	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CAA<7>	R2742	68	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CAA<6>	R2743	68	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CAA<5>	R2744	68	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CLK_P<0>	R2745	39	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CLK_N<0>	R2746	39	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CKE<1>	R2747	82	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CKE<0>	R2748	82	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CAA<4>	R2749	68	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CAA<2>	R2750	68	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CAA<3>	R2751	68	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CAA<1>	R2752	68	1%	1/20W	201	MF
72 23 7	IN	MEM_B_CAA<0>	R2753	68	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CAB<9>	R2754	68	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CAB<8>	R2755	68	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CAB<7>	R2756	68	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CAB<6>	R2757	68	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CAB<5>	R2758	68	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CLK_N<1>	R2759	39	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CLK_P<1>	R2760	39	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CKE<2>	R2761	82	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CKE<3>	R2762	82	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CAB<4>	R2763	68	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CAB<2>	R2764	68	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CAB<3>	R2765	68	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CAB<1>	R2766	68	1%	1/20W	201	MF
72 24 7	IN	MEM_B_CAB<0>	R2767	68	1%	1/20W	201	MF
72 24 23 7	IN	MEM_B_CS_L<0>	R2768	82	1%	1/20W	201	MF
72 24 23 7	IN	MEM_B_CS_L<1>	R2769	82	1%	1/20W	201	MF
72 24 23 7	IN	MEM_B_ODT<0>	R2770	82	1%	1/20W	201	MF

C2710	0.47UF	20% 4V CERM-X5R-1 201	C2731	12PF 5% 25V CERM 0201
C2711	0.47UF	20% 4V CERM-X5R-1 201	C2712	0.47UF 20% 4V CERM-X5R-1 201
C2713	0.47UF	20% 4V CERM-X5R-1 201	C2714	0.47UF 20% 4V CERM-X5R-1 201
C2715	0.47UF	20% 4V CERM-X5R-1 201	C2716	0.47UF 20% 4V CERM-X5R-1 201
C2717	0.47UF	20% 4V CERM-X5R-1 201	C2718	0.47UF 20% 4V CERM-X5R-1 201
C2719	0.47UF	20% 4V CERM-X5R-1 201	C2742	3PF +/-0.1PF 25V C0G 0201
CRITICAL C2740	20UF	20% 6.3V CERM-X5R 0402	NOSTUFF CRITICAL C2741	20UF 20% 6.3V CERM-X5R 0402

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D

REVISION 1.0.0

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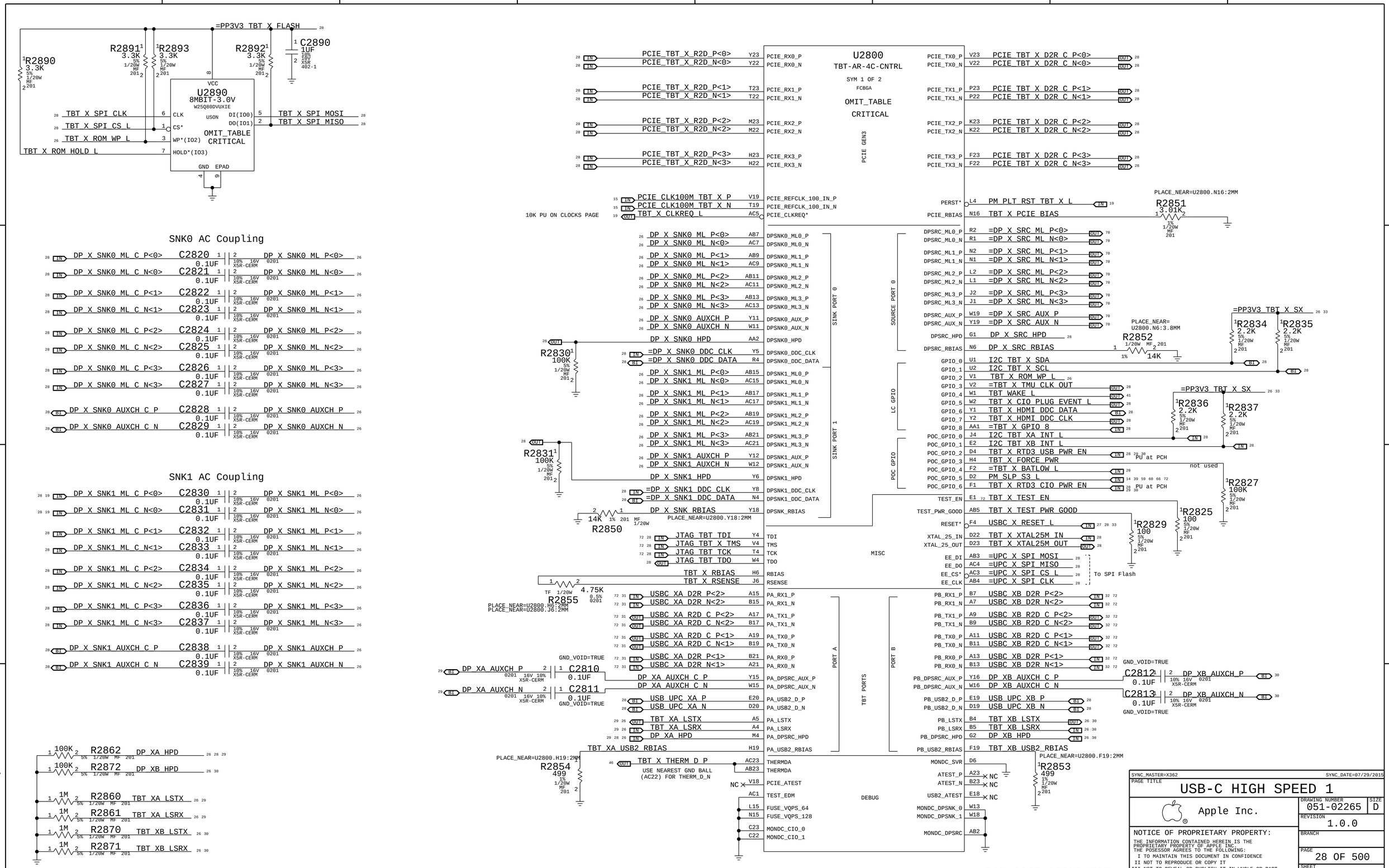

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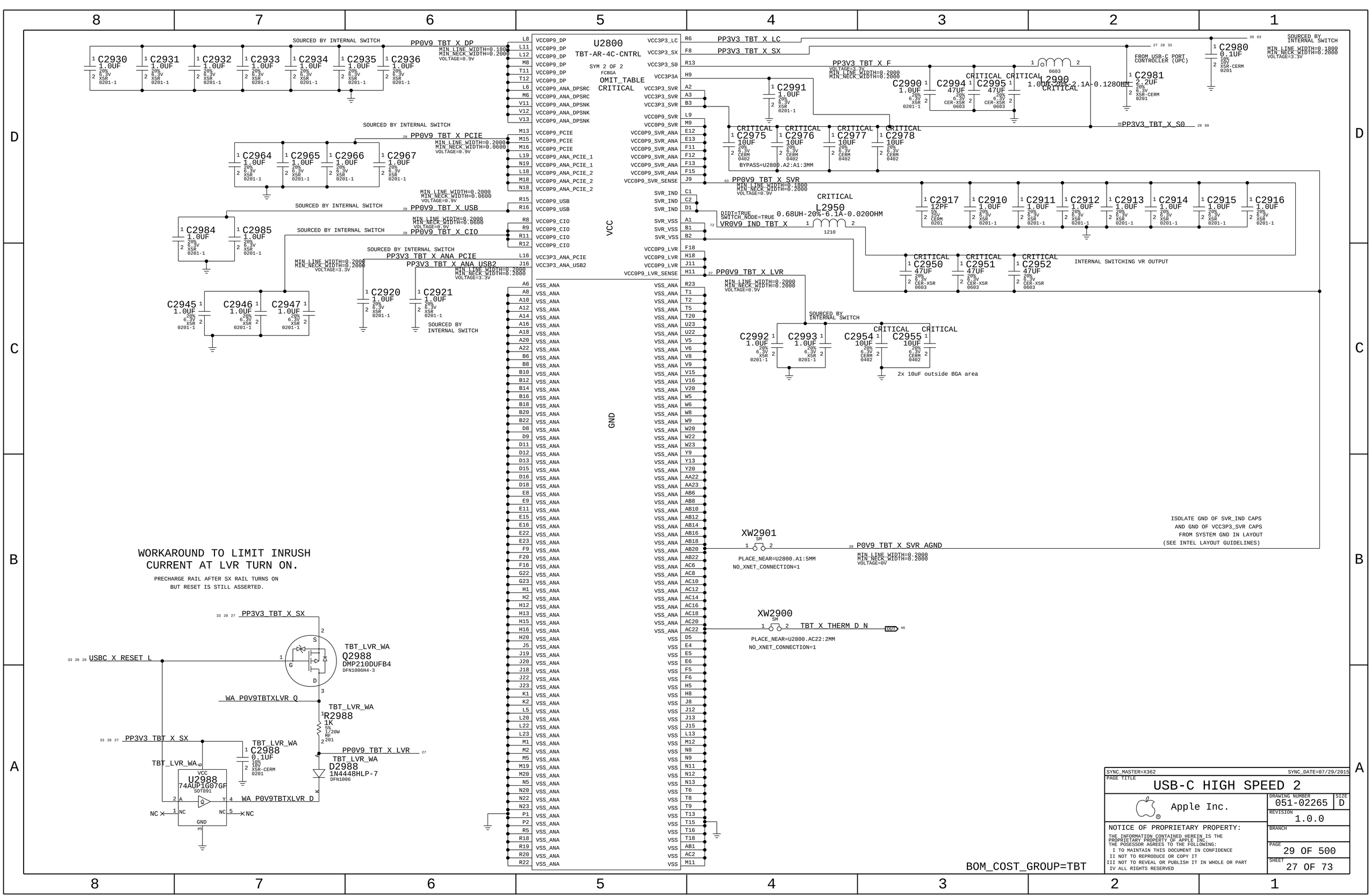
U2800
TBT-AR-4C-CNTRL
SYM 2 OF 2
FCBGA
OMIT_TABLE
CRITICAL
VCC
GND
SOURCED BY INTERNAL SWITCH
PP0V9_TBT_X_DP
PP0V9_TBT_X_PCIE
PP0V9_TBT_X_USB
PP0V9_TBT_X_CIO
PP3V3_TBT_X_ANA_PCIE
PP3V3_TBT_X_ANA_USB2
PP3V3_TBT_X_LC
PP3V3_TBT_X_SX
PP3V3_TBT_X_F
FROM USB-C PORT CONTROLLER (UPC)
=PP3V3_TBT_X_S0
PP0V9_TBT_X_SVR
PP0V9_TBT_X_LVR
VR0V9_IND_TBT_X
L2950
0.68UH-20%-6.1A-0.0200HM
L2990
1.0UH-20%-2.1A-0.1280HM
INTERNAL SWITCHING VR OUTPUT
2x 10uF outside BGA area
XW2901
PP0V9_TBT_X_SVR_AGND
XW2900
TBT_X_THERM_D_N
ISOLATE GND OF SVR_IND CAPS
AND GND OF VCC3P3_SVR CAPS
FROM SYSTEM GND IN LAYOUT
(SEE INTEL LAYOUT GUIDELINES)
WORKAROUND TO LIMIT INRUSH
CURRENT AT LVR TURN ON.
PRECHARGE RAIL AFTER SX RAIL TURNS ON
BUT RESET IS STILL ASSERTED.
PP3V3_TBT_X_SX
USBC_X_RESET_L
TBT_LVR_WA
Q2988
DMP210DUFB4
DFN1006H4-3
WA_P0V9TBTXLVR_Q
R2988
1K
PP0V9_TBT_X_LVR
D2988
1N4448HLP-7
DFN1006
U2988
74AUP1G07GF
SOT891
WA_P0V9TBTXLVR_D
BOM_COST_GROUP=TBT
SYNC_MASTER=X362
SYNC_DATE=07/29/2015
PAGE TITLE
USB-C HIGH SPEED 2
Apple Inc.
DRAWING NUMBER
051-02265
SIZE
D
REVISION
1.0.0
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RIDGE AC COUPLING

R2D

PCIE TBT X R2D C P<0>	C3040	0201 X5R 20% 6.3V 0.22UF		PCIE TBT X R2D P<0>
PCIE TBT X R2D C N<0>	C3041	0201 X5R 20% 6.3V 0.22UF		PCIE TBT X R2D N<0>
PCIE TBT X R2D C P<1>	C3042	0201 X5R 20% 6.3V 0.22UF		PCIE TBT X R2D P<1>
PCIE TBT X R2D C N<1>	C3043	0201 X5R 20% 6.3V 0.22UF	TBT_PCIE_4LANES	PCIE TBT X R2D N<1>
PCIE TBT X R2D C P<2>	C3044	0201 X5R 20% 6.3V 0.22UF	TBT_PCIE_4LANES	PCIE TBT X R2D P<2>
PCIE TBT X R2D C N<2>	C3045	0201 X5R 20% 6.3V 0.22UF	TBT_PCIE_4LANES	PCIE TBT X R2D N<2>
PCIE TBT X R2D C P<3>	C3046	0201 X5R 20% 6.3V 0.22UF	TBT_PCIE_4LANES	PCIE TBT X R2D P<3>
PCIE TBT X R2D C N<3>	C3047	0201 X5R 20% 6.3V 0.22UF	TBT_PCIE_4LANES	PCIE TBT X R2D N<3>

D2R

PCIE TBT X D2R C P<0>	C3050	0201 X5R 20% 6.3V 0.22UF		PCIE TBT X D2R P<0>
PCIE TBT X D2R C N<0>	C3051	0201 X5R 20% 6.3V 0.22UF		PCIE TBT X D2R N<0>
PCIE TBT X D2R C P<1>	C3052	0201 X5R 20% 6.3V 0.22UF		PCIE TBT X D2R P<1>
PCIE TBT X D2R C N<1>	C3053	0201 X5R 20% 6.3V 0.22UF		PCIE TBT X D2R N<1>
PCIE TBT X D2R C P<2>	C3055	0201 X5R 20% 6.3V 0.22UF	TBT_PCIE_4LANES	PCIE TBT X D2R P<2>
PCIE TBT X D2R C N<2>	C3056	0201 X5R 20% 6.3V 0.22UF	TBT_PCIE_4LANES	PCIE TBT X D2R N<2>
PCIE TBT X D2R C P<3>	C3057	0201 X5R 20% 6.3V 0.22UF	TBT_PCIE_4LANES	PCIE TBT X D2R P<3>
PCIE TBT X D2R C N<3>	C3054	0201 X5R 20% 6.3V 0.22UF	TBT_PCIE_4LANES	PCIE TBT X D2R N<3>

ACE RPD STRAPPING

CONNECT G1/G2 TO CC1/CC2 TO RECEIVE POWER UNDER DB CASE
CONNECT G1/G2 TO GND TO NOT RECEIVE POWER UNDER DB CASE

USBC XA RPD G1	R3026	0 5% 1/20W MF 0201	USBC XA CC1
USBC XA RPD G2	R3022	0 5% 1/20W MF 0201	USBC XA CC2
USBC XB RPD G1	R3011	0 5% 1/20W MF 0201	USBC XB CC1
USBC XB RPD G2	R3024	0 5% 1/20W MF 0201	USBC XB CC2

ACE BUSPOWERZ STRAPPING

R3017	0 5% 1/20W MF 0201	UPC XA BUSPOWERZ
R3019	0 5% 1/20W MF 0201	UPC XB BUSPOWERZ

PU BUSPOWERZ TO LDO_3V3 TO NOT PASS VBUS TO SYS UNDER DB CASE

PU BUSPOWERZ TO 1V8D TO PASS VBUS TO SYS UNDER DB CASE USES INT POWER PATH

GND BUSPOWERZ TO PASS VBUS TO SYS UNDER DB CASE USES EXT POWER PATH

RIDGE DEBUG CONN

J3099 505070-1220 M-ST-SM UPC_DBG_HDR

TBT X CIO PLUG EVENT L	1	2	TBT X PCI RESET L
DP X SNK0 HPD	3	4	USBC X RESET L
ARKANOID P5	5	6	PP3V3 TBT X SX
ARKANOID P7	7	8	PP0V9 TBT X PCIE
TBT POC RESET	9	10	PP0V9 TBT X USB
PP3V3 TBT X LC	11	12	PP0V9 TBT X CIO

13 14 15 16 516S00115

ACE DEBUG CONN

J3098 505070-1220 M-ST-SM UPC_DBG_HDR

I2C TBT XB INT L	1	2	I2C TBT XA INT L
=I2C UPC XA SCL2	3	4	I2C TBT X SDA
=I2C UPC XA SDA2	5	6	I2C TBT X SCL
SMC USBC INT L	7	8	I2C UPC XA DBG CTL SDA
TBT X SPI CLK DBG	9	10	I2C UPC XA DBG CTL SCL
UPC XA UART TX	11	12	UPC_XA_UART_RX

13 14 15 16 516S00115

DP X SNK1 HPD	ARKANOID:HPD	R3080	0 5% 1/20W MF 0201	ARKANOID P5
SMC DEBUGPRT RX L	ARKANOID:MOJO	R3081	0 5% 1/20W MF 0201	
DP XA HPD	ARKANOID:HPD	R3082	0 5% 1/20W MF 0201	ARKANOID P7
SMC DEBUGPRT TX L	ARKANOID:MOJO	R3083	0 5% 1/20W MF 0201	

F3000 CRITICAL 6AMP-32V-0.00950HM 0603
=PP20V USBC XA VBUS — PP20V USBC XA VBUS F

F3010 CRITICAL 6AMP-32V-0.00950HM 0603
=PP20V USBC XB VBUS — PP20V USBC XB VBUS F

POWER ALIASES

=PP3V3 G3H UPC XA	PP3V3 G3H UPC XA	R3000 0 5% 1/20W MF 0201	PP3V3 G3H
=PP3V3 G3H UPC XB	PP3V3 G3H UPC XB	R3001 0 5% 1/20W MF 0201	PP3V3 G3H

MAKE_BASE=TRUE

=PP20V USBC XA VBUS	PP20V USBC XA VBUS
=PP20V USBC XB VBUS	PP20V USBC XB VBUS
=UPC XA I2C STRAP	PP3V3 UPC XA LDO
=PP3V3R1V8 UPC XA	
=UPC XB I2C STRAP	PP3V3 UPC XB LDO
=PP3V3 TBT X FLASH	
=PP3V3R1V8 UPC XB	
=PP3V3 TBT X S0	PP3V3 TBT X S0
=PPHV INT G3H	

MISC ALIASES

=UPC X SPI CLK	UPC X SPI CLK
=UPC X SPI CS L	UPC X SPI CS L
=UPC X SPI MOSI	UPC X SPI MOSI
=UPC X SPI MISO	UPC X SPI MISO
USBC X POC RESET	TBT POC RESET
TBT X RTD3 CIO PWR EN	TBT X CIO PWR EN
TBT X RTD3 USB PWR EN	TBT X USB PWR EN
TBT X PLUG EVENT L	TBT X CIO PLUG EVENT L
=TBT X BATLOW L	PM BATLOW L
=USBC TMS X SWD CLK X	JTAG TBT X TMS
=USBC TMS T SWD DATA X	PU USBC TMS T SWD DATA X
JTAG TBT TDO	JTAG ISP TDO
=USBC XA RESET L	TP USBC XA RESET L
UPC XA SPI CLK	
UPC XA SPI CS L	
UPC XA SPI MISO	
UPC XA SPI MOSI	
UPC XA RESET	
UPC XB RESET	

MAKE_BASE=TRUE

XW3001 SM
PLACE_NEAR=U2800.A1:5MM
NO_XNET_CONNECTION=1
P0V9 TBT X SVR AGND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V

	UPC XA - U3100	
I2C TBT X SDA		=I2C UPC XA SDA1
I2C TBT X SCL		=I2C UPC XA SCL1
I2C TBT XA INT L	(WRITE: 0X70 READ: 0X71)	=I2C UPC XA INT1 L
I2C TBT XB INT L		=I2C UPC XB SDA1
	UPC XB - U3200	=I2C UPC XB SCL1
	(WRITE: 0X7E READ: 0X7F)	=I2C UPC XB INT1 L

TBT - MASTER
ALPINE RIDGE - U2800

	R3098 100 5% 1/20W MF 201	TBT X SPI CLK DBG
TBT X SPI CLK	R3090 15 5% 1/20W MF 201	UPC XB SPI CLK
TBT X SPI CS L	R3091 15 5% 1/20W MF 201	UPC XB SPI CS L
TBT X SPI MOSI	R3092 15 5% 1/20W MF 201	UPC XB SPI MOSI
TBT X SPI MISO	R3093 15 5% 1/20W MF 201	UPC XB SPI MISO
	R3094 15 5% 1/20W MF 201	=UPC X SPI CLK
	R3095 15 5% 1/20W MF 201	=UPC X SPI CS L
	R3096 15 5% 1/20W MF 201	=UPC X SPI MOSI
	R3097 15 5% 1/20W MF 201	=UPC X SPI MISO

TBT X XTAL25M OUT — C3002 20PF 5% 25V C0G 0201
NOSTUFF R3006 1M 5% 1/20W MF 201
CRITICAL Y3000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
TBT X XTAL25M IN — C3003 20PF 5% 25V C0G 0201

USB3 EXTA R2D C P	C3020 0201 X5R-CERM 10% 16V 0.1UF	USB3 EXTA R2D P	TP3091
USB3 EXTA R2D C N	C3021 0201 X5R-CERM 10% 16V 0.1UF	USB3 EXTA R2D N	TP3092
USB3 EXTA D2R P			TP3093
USB3 EXTA D2R N			TP3094

USBC XA USB TOP P		USBC XA USB DBG TOP P
USBC XA USB TOP N		USBC XA USB DBG TOP N
USBC XA USB BOT P		USBC XA USB DBG BOT P
USBC XA USB BOT N		USBC XA USB DBG BOT N

MAKE_BASE=TRUE

CRITICAL L3000 90-OHM-0.1A EXCX4CE 2X1.6MM

=USB UPC XA P	USB UPC XA F P	=USB UPC XA F P
=USB UPC XA N	USB UPC XA F N	=USB UPC XA F N

PLACE_NEAR=U3100.L5:5MM
PLACE_NEAR=U3100.K5:5MM

TP UPC XB SWD CLK — TSP UPC XB SWD CLK — TP3090

DP / USB SOURCE ALIASES

DP DDI1 ML C P<3..0>		DP X SNK1 ML C P<3..0>
DP DDI1 ML C N<3..0>		DP X SNK1 ML C N<3..0>
DP DDI1 AUXCH C P		DP X SNK1 AUXCH C P
DP DDI1 AUXCH C N		DP X SNK1 AUXCH C N
DP DDPB HPD		DP X SNK1 HPD
DP DDI2 ML C P<3..0>		DP X SNK0 ML C P<3..0>
DP DDI2 ML C N<3..0>		DP X SNK0 ML C N<3..0>
DP DDI2 AUXCH C P		DP X SNK0 AUXCH C P
DP DDI2 AUXCH C N		DP X SNK0 AUXCH C N
DP DDPC HPD		DP X SNK0 HPD

MAKE_BASE=TRUE

USB EXTB P		USB UPC PCH XA P	=USB UPC XA P
USB EXTB N		USB UPC PCH XA N	=USB UPC XA N
USB UPC XA P	R3012 0 5% 1/20W MF 0201		
USB UPC XA N	R3013 0 5% 1/20W MF 0201		
UPC XA FAULT L	R3008 0 5% 1/20W MF 0201		USB EXTA OC L
NC USB2 08P		USB UPC PCH XB P	=USB UPC XB P
NC USB2 08N		USB UPC PCH XB N	=USB UPC XB N
USB UPC XB P	R3014 0 5% 1/20W MF 0201		
USB UPC XB N	R3015 0 5% 1/20W MF 0201		
UPC XB FAULT L	R3018 0 5% 1/20W MF 0201		USB EXTB OC L

PP3V3 TBT X LC

R3071 100K 5% 1/20W MF 201	TBT X HDMI DDC CLK		
R3035 100K 5% 1/20W MF 201	JTAG TBT TCK	R3033 0 5% 1/20W MF 0201	JTAG ISP TCK
R3036 100K 5% 1/20W MF 201	JTAG TBT TDI	R3034 0 5% 1/20W MF 0201	JTAG ISP TDI
R3073 100K 5% 1/20W MF 201	UPC XA DBG3		
R3074 100K 5% 1/20W MF 201	UPC XA DBG4		
R3072 100K 5% 1/20W MF 201	TBT X HDMI DDC DATA		
R3066 100K 5% 1/20W MF 201	DP X SNK0 DDC DATA		=DP X SNK0 DDC DATA
R3067 100K 5% 1/20W MF 201	DP X SNK0 DDC CLK		=DP X SNK0 DDC CLK
R3069 100K 5% 1/20W MF 201	DP X SNK1 DDC CLK		=DP X SNK1 DDC CLK
R3070 100K 5% 1/20W MF 201	DP X SNK1 DDC DATA		=DP X SNK1 DDC DATA
R3040 100K 5% 1/20W MF 201	PD UPC XA GPIO5		UPC XA HPD RX
R3041 100K 5% 1/20W MF 201	PD UPC XB GPIO5		UPC XB HPD RX
R3042 100K 5% 1/20W MF 201	PD UPC XA GPIO6		UPC XA 5V EN (PD WHEN NOT USED)
R3043 100K 5% 1/20W MF 201	PD UPC XB GPIO6		UPC XB 5V EN
R3049 100K 5% 1/20W MF 201	PD TBT X TMU CLK OUT		=TBT X TMU CLK OUT
R3050 100K 5% 1/20W MF 201	PD TBT X GPIO 8		=TBT X GPIO 8
R3020 1M 5% 1/20W MF 201	DP X SRC HPD		

XPD JTAG ISOLATION

LOCAL BULK CAP
=PP5V_USBC
CRITICAL C3000 220UF-35MOHM 20% 6.3V POLY-TANT CASE-B2-SM1

UPC XA DBG1		SMC TCK
UPC XA DBG2		SMC TMS
UPC XB DBG1		SSD JTAG TCK
UPC XB DBG2		SSD JTAG TMS
UPC XB DBG3		SMC DEBUGPRT TX L
UPC XB DBG4		SMC DEBUGPRT RX L

MAKE_BASE=TRUE

BOM_COST_GROUP=USB-C

DESIGN: X502/MLB_CATZ
LAST CHANGE: Fri Aug 5 13:34:33 2016

PAGE TITLE: USB-C SUPPORT

Apple Inc.

DRAWING NUMBER: 051-02265 SIZE: D
REVISION: 1.0.0
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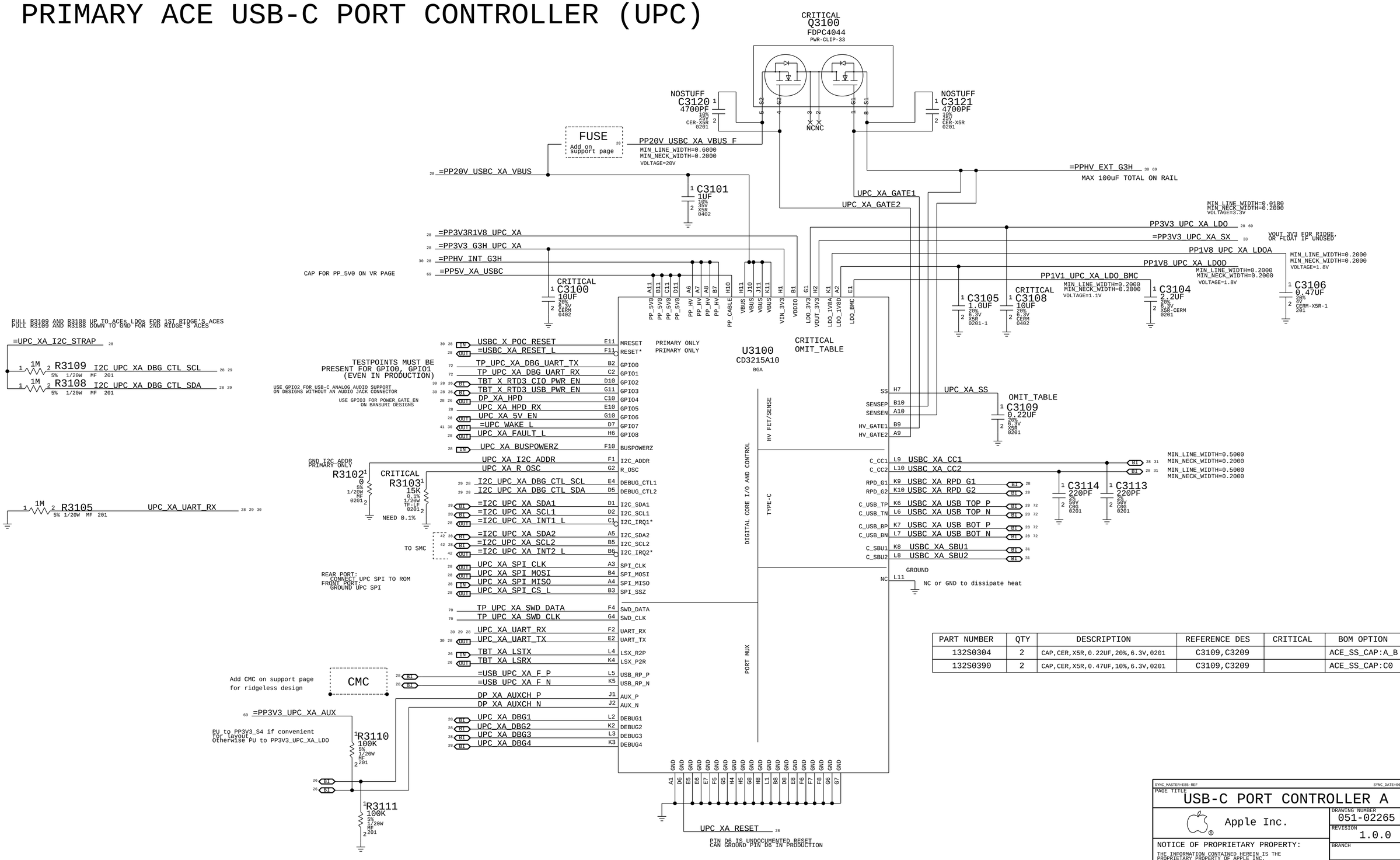
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S0304	2	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C3109,C3209		ACE_SS_CAP:A_B
132S0390	2	CAP,CER,X5R,0.47UF,10%,6.3V,0201	C3109,C3209		ACE_SS_CAP:C0

BOM_COST_GROUP=USB-C

SYNC_MASTER=E85-REF SYNC_DATE=06/17/2015

PAGE TITLE
USB-C PORT CONTROLLER A

Apple Inc.

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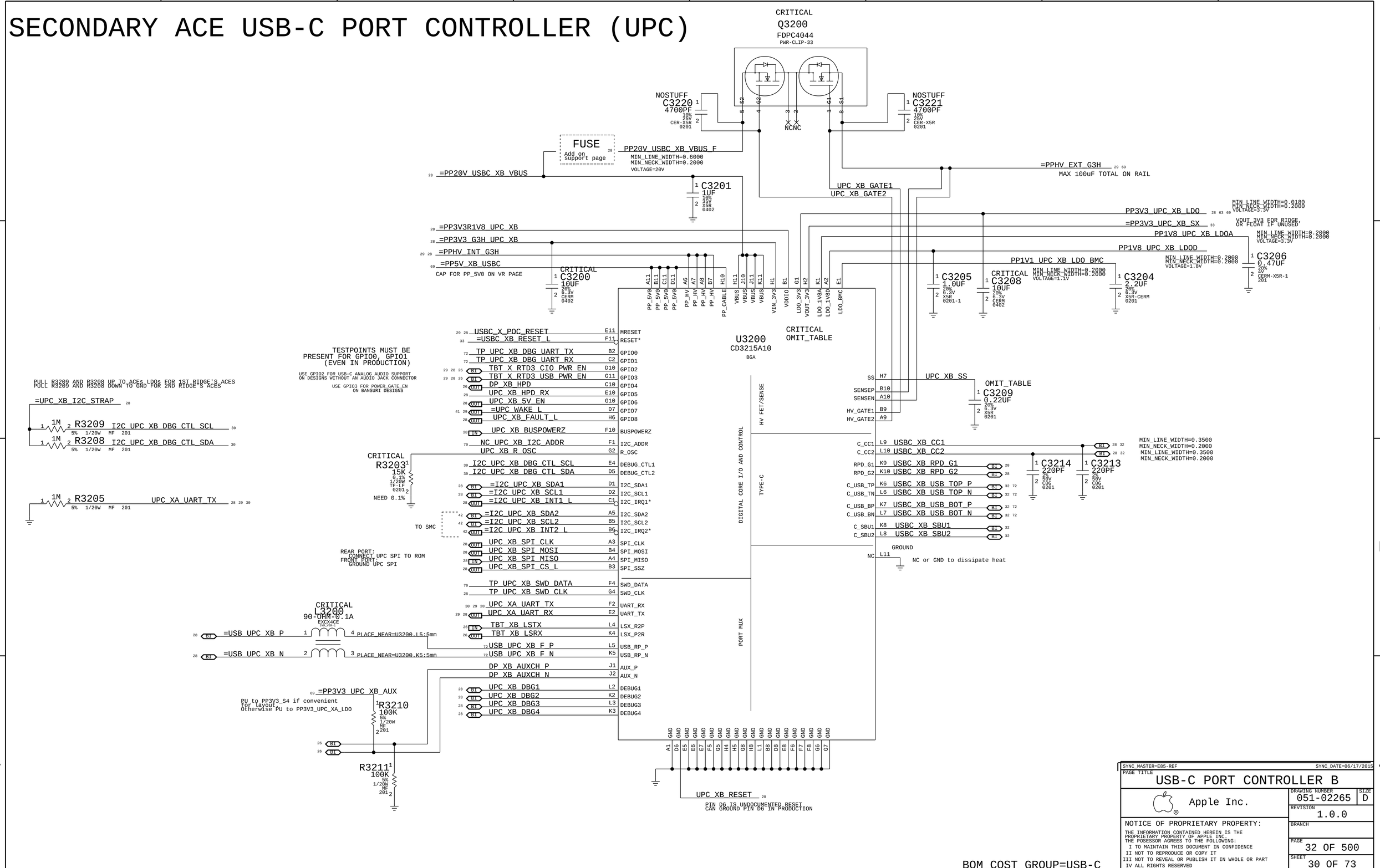
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



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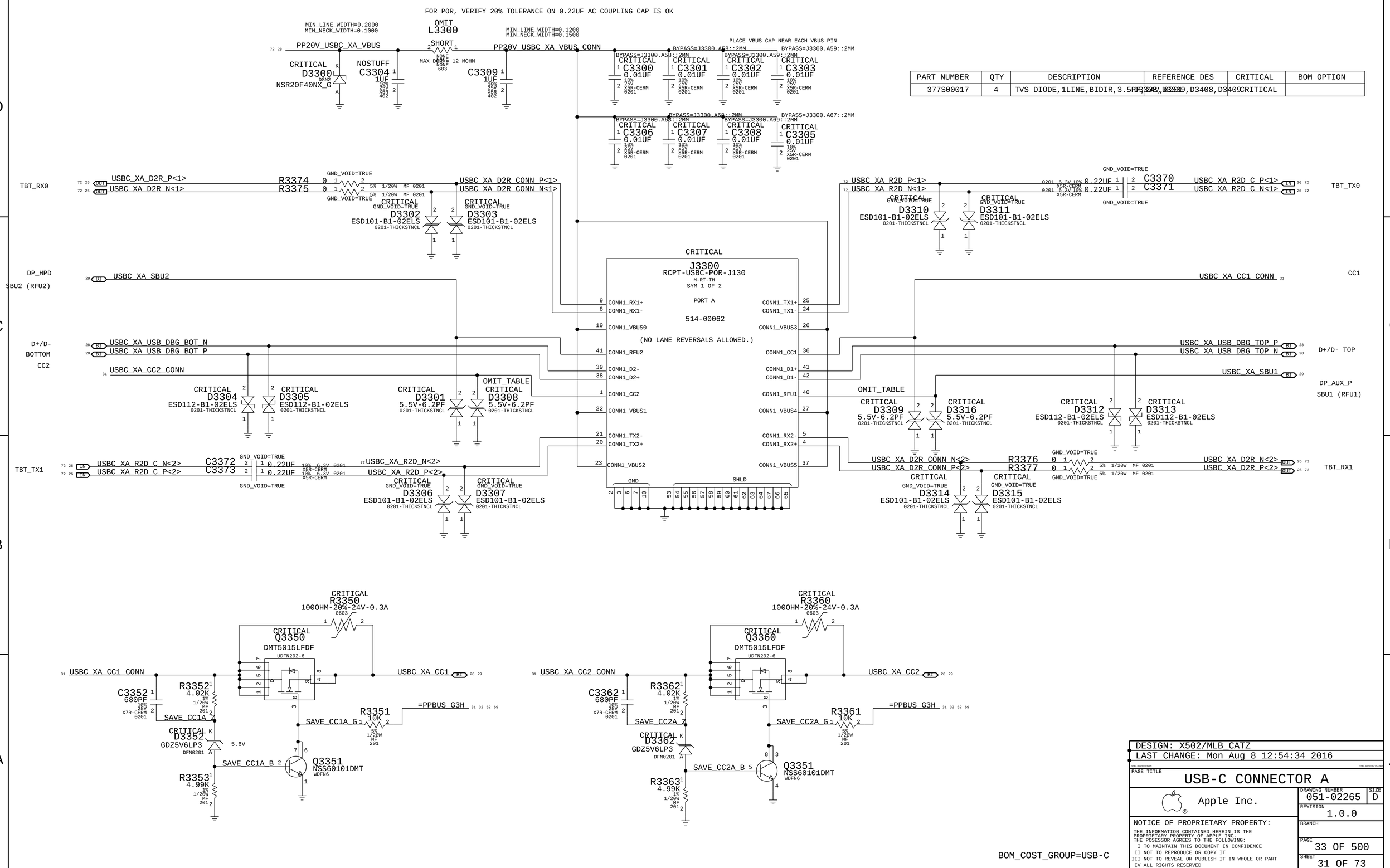

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
377S00017	4	TVS DIODE,1LINE,BIDIR,3.5PF,0201	D3301,D3309,D3408,D3409	CRITICAL	

DESIGN: X502/MLB_CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
USB-C CONNECTOR A

Apple Inc.

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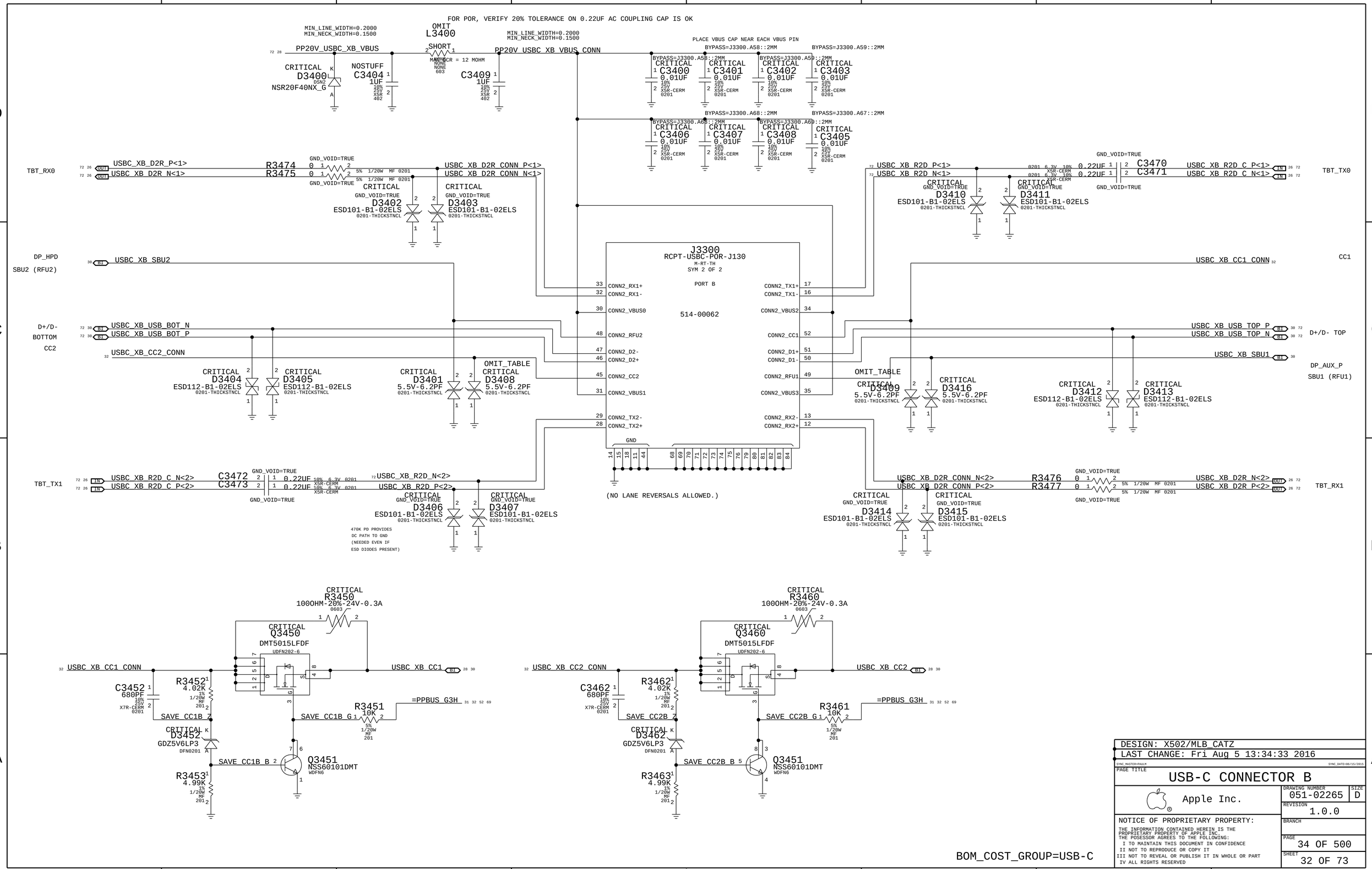

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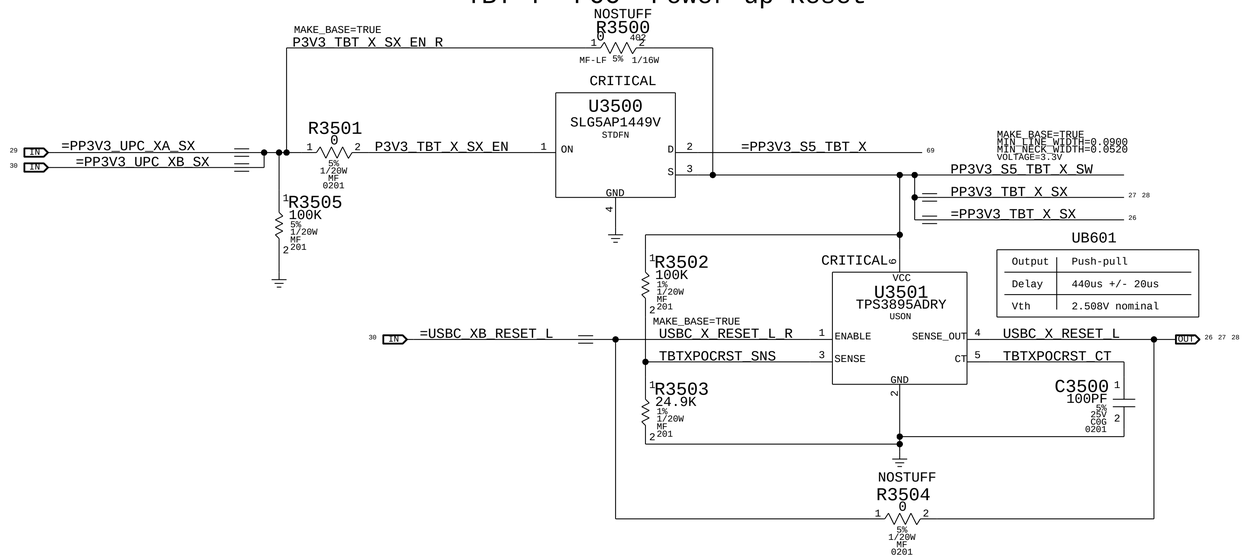
TBT T "POC" Power-up Reset



BOM_COST_GROUP=USB-C

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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USB-C SUPPORT 2

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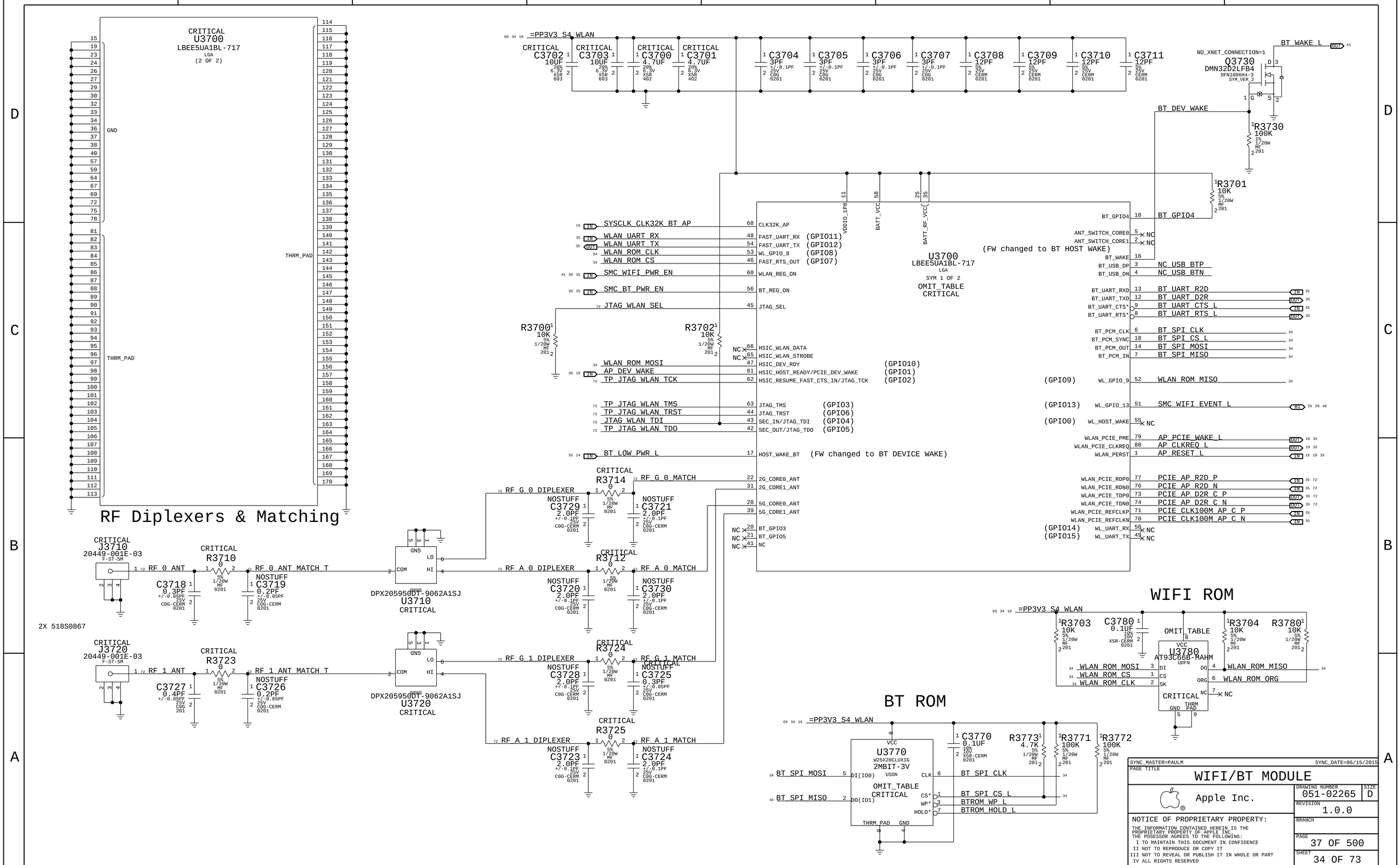

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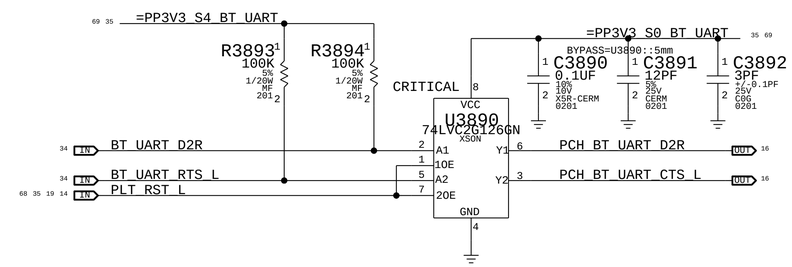
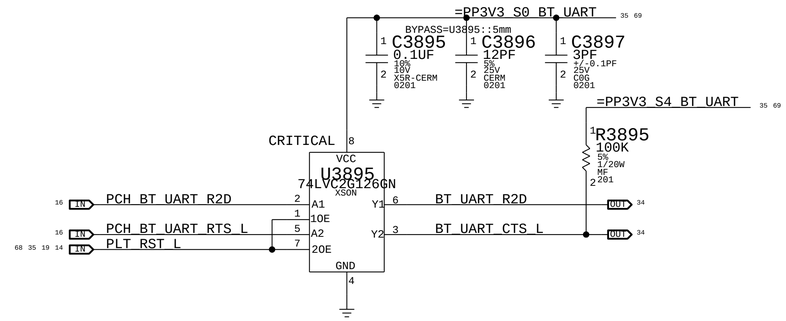
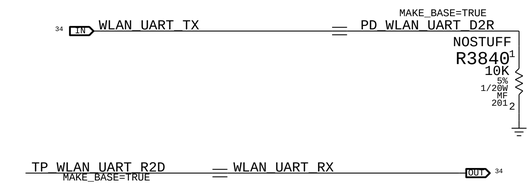
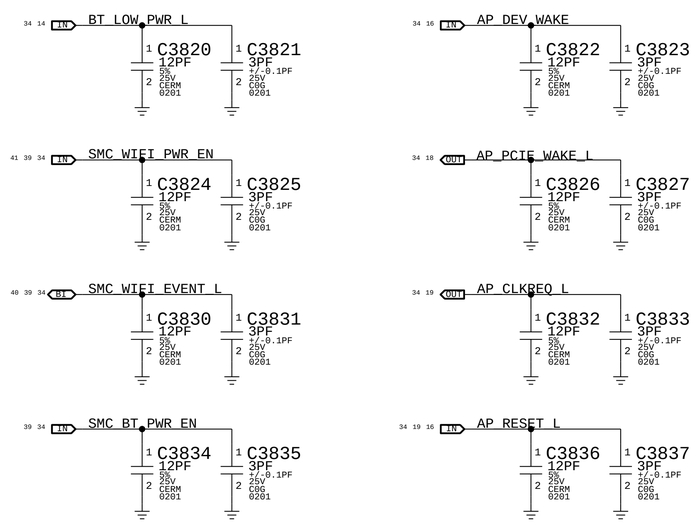
BT UART Isolation

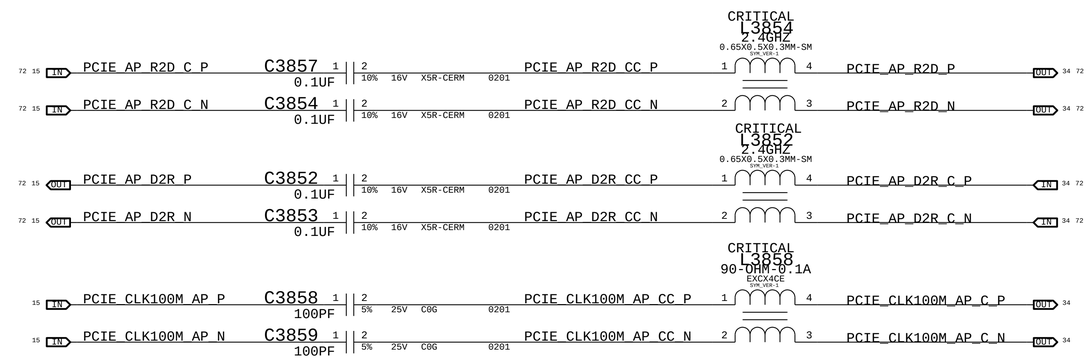




WIFI UART ISOLATION







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WIFI/BT Module Support

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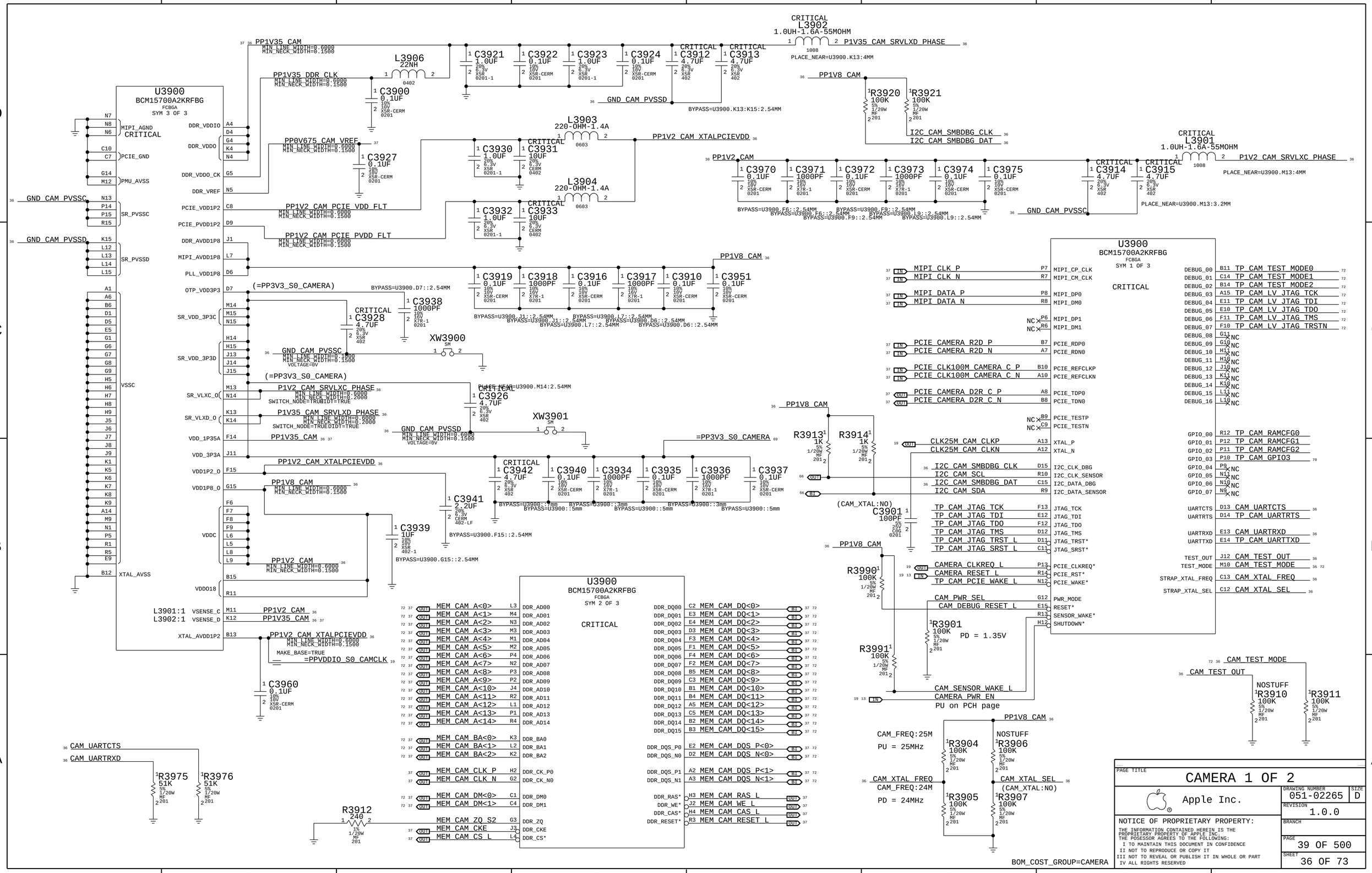

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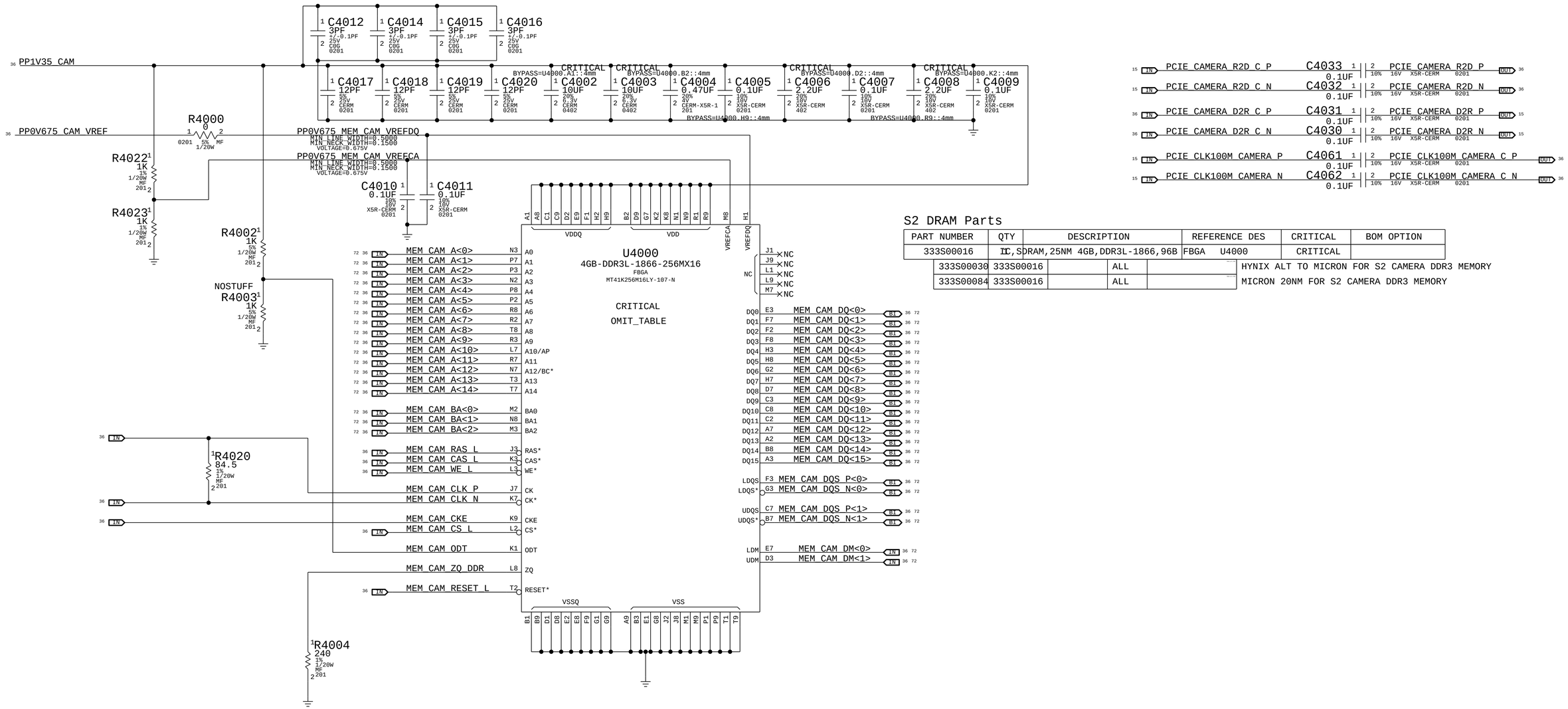
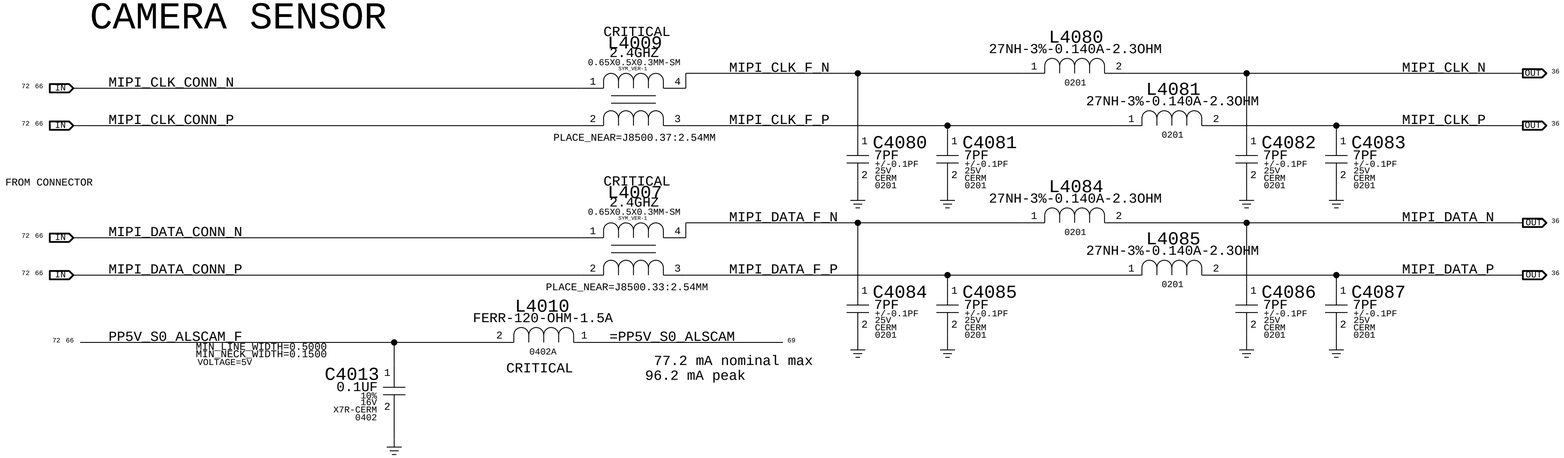


S2 DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00016	1	IC,SDRAM,25NM 4GB,DDR3L-1866,96B	FBGA U4000	CRITICAL	
333S00030	333S00016	ALL			HYNIX ALT TO MICRON FOR S2 CAMERA DDR3 MEMORY
333S00084	333S00016	ALL			MICRON 20NM FOR S2 CAMERA DDR3 MEMORY

CAMERA SENSOR



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PAGE TITLE: CAMERA 2 OF 2

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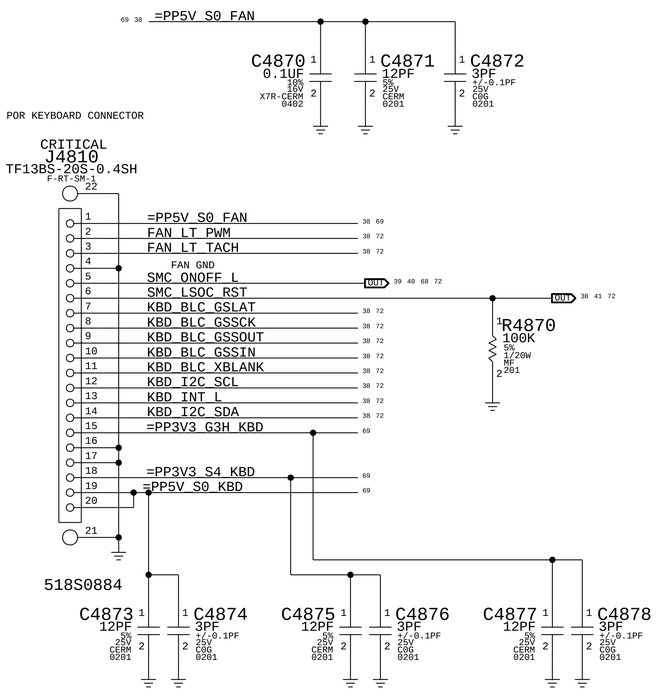

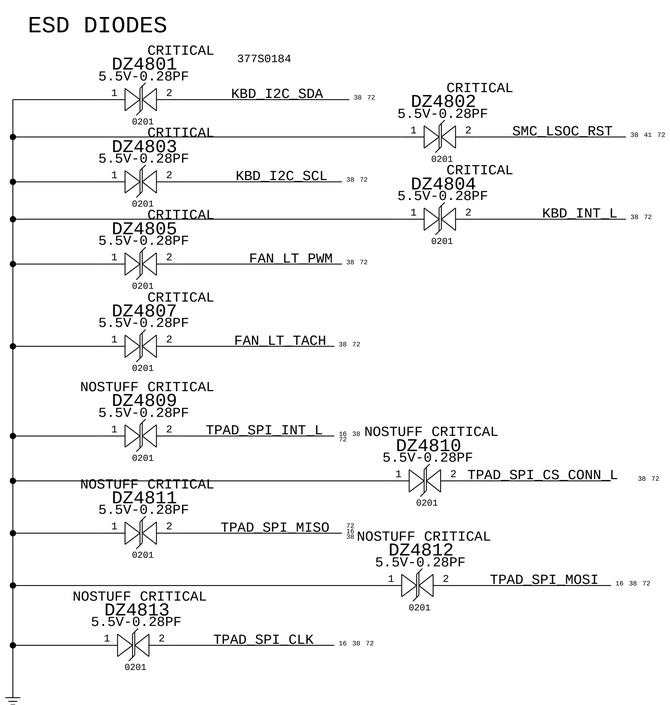

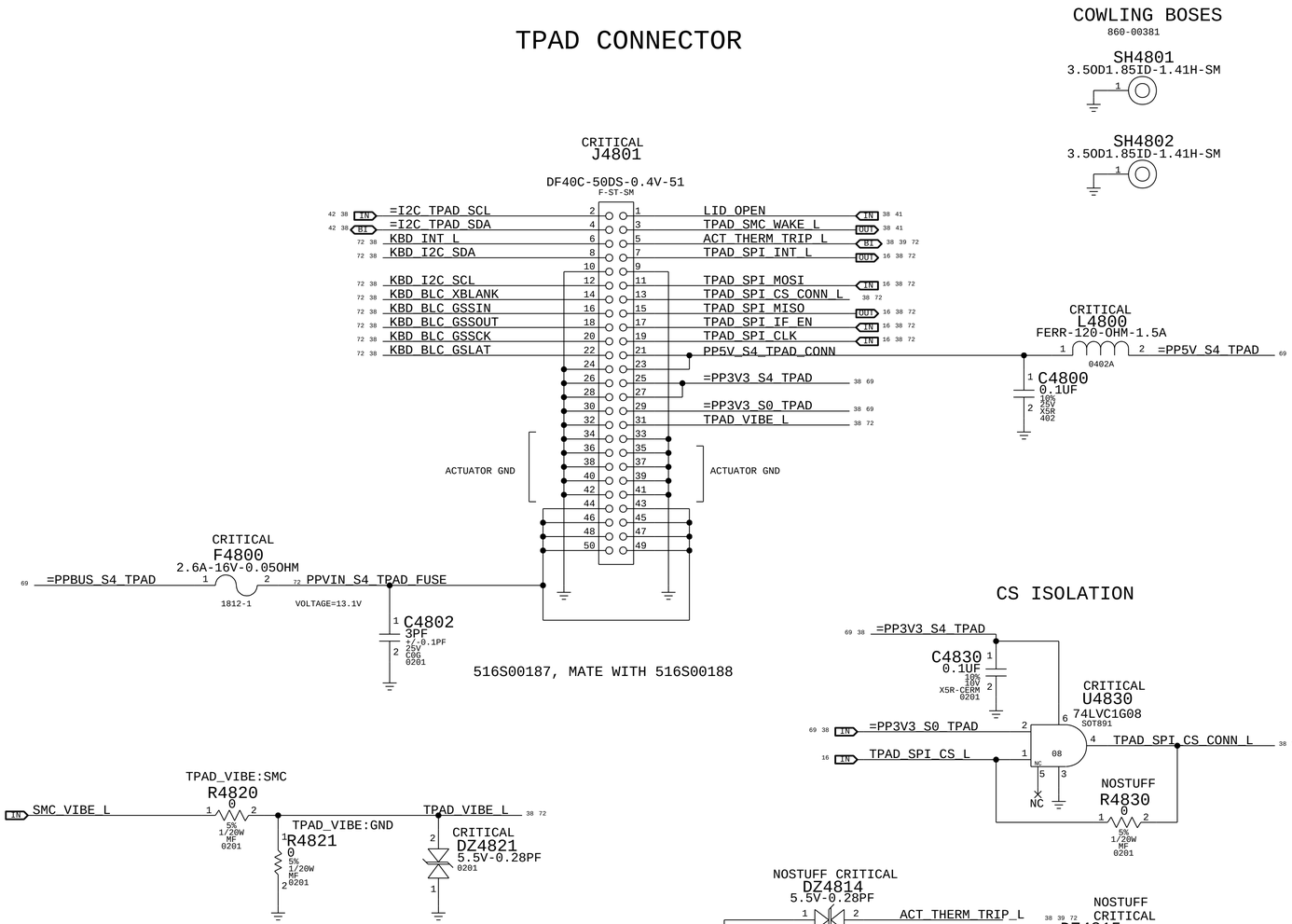

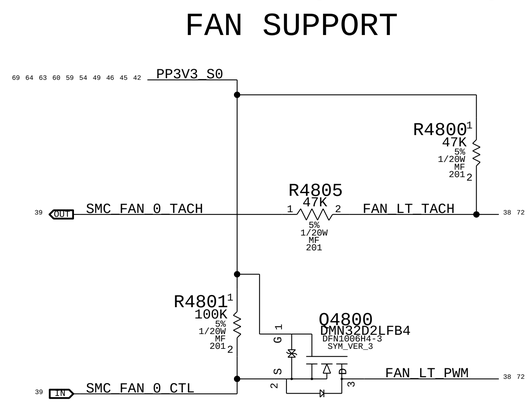

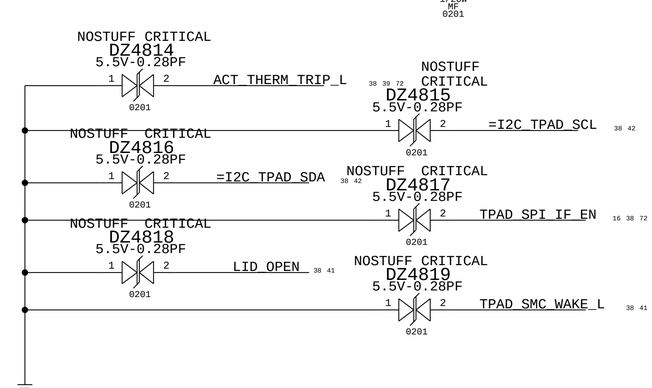

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P1:KEYBOARD & TRACKPAD CONN

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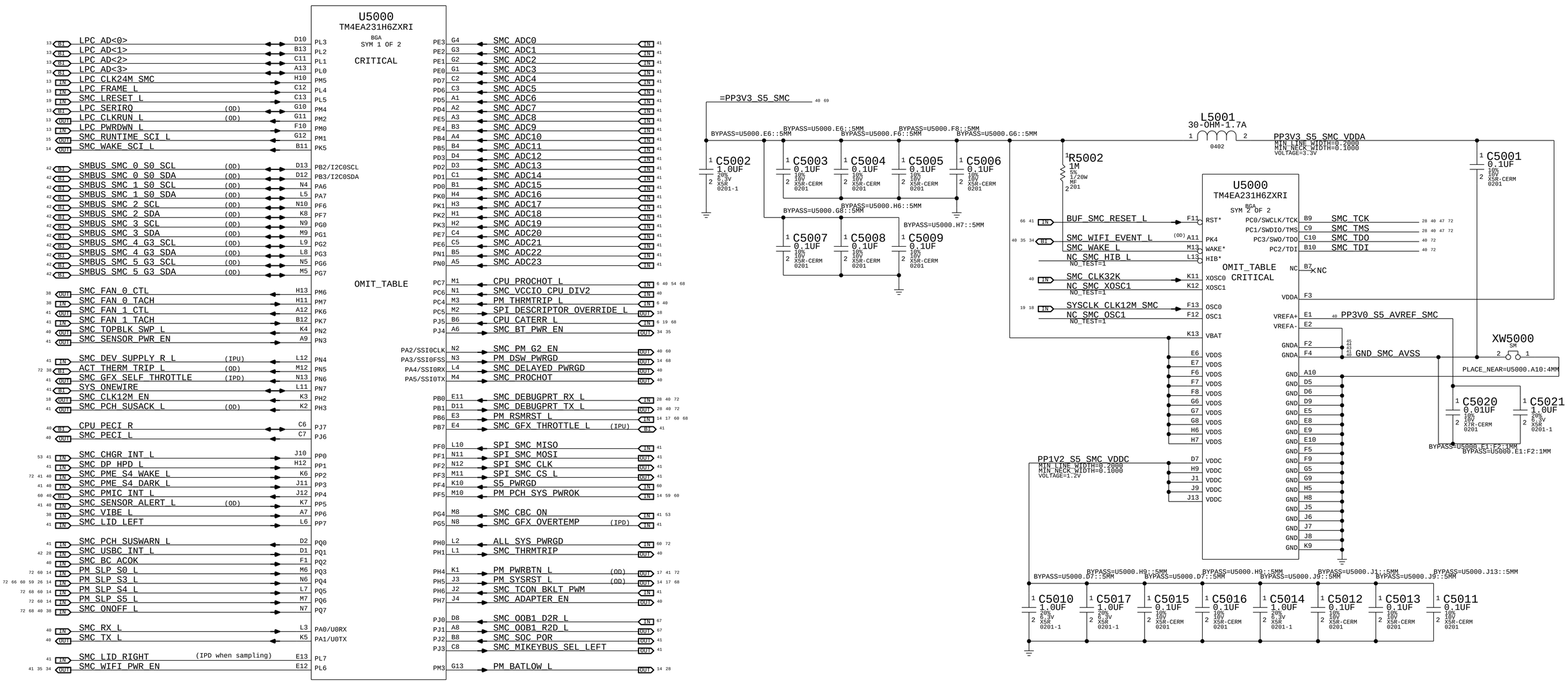

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

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SMC

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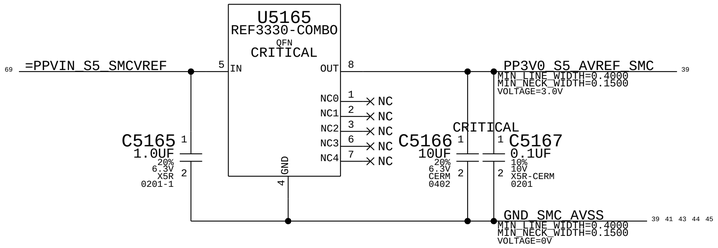
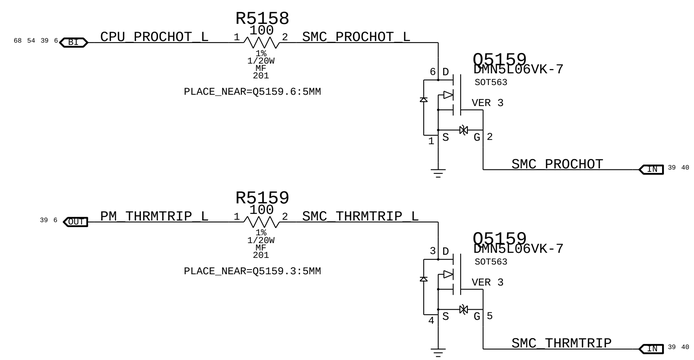
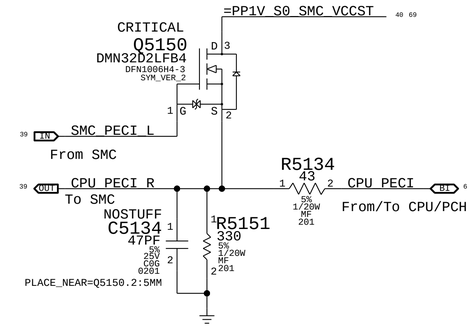
SMC AVREF Supply



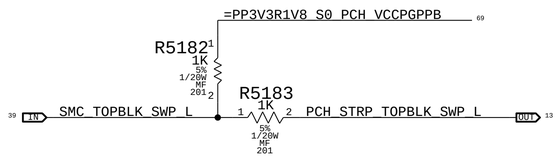
PROCHOT/THRMTRIP Support

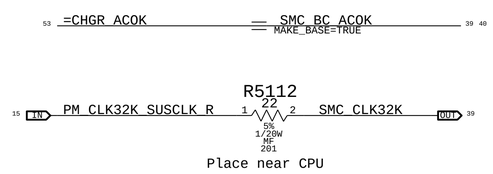


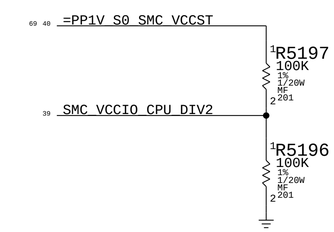
PECI Support

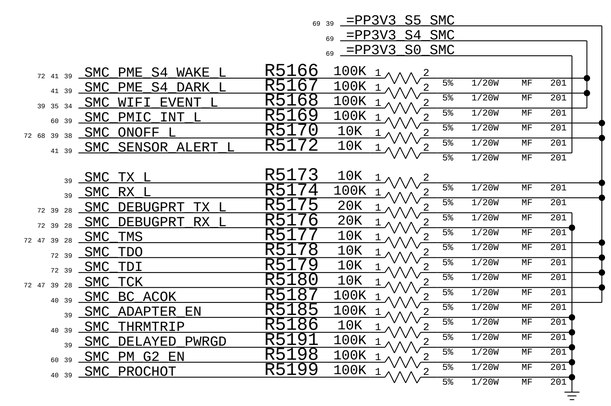


Top-Block Swap









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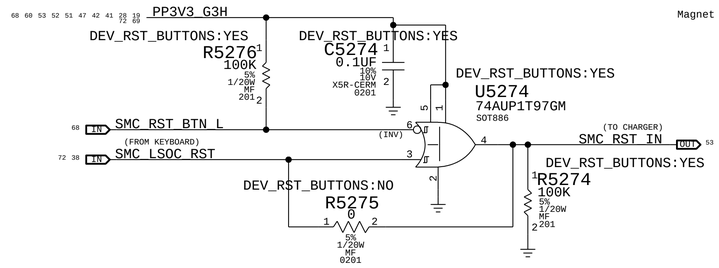
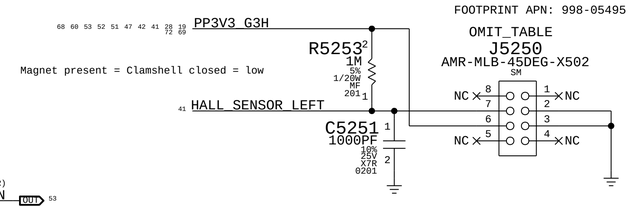
SMC ANALOG INPUTS

39 OUT	SMC_ADC0	MAKE_BASE=TRUE	SMC_DCIN_VSENSE	IN 43
39 OUT	SMC_ADC1	MAKE_BASE=TRUE	SMC_DCIN_ISENSE	IN 43
39 OUT	SMC_ADC2	MAKE_BASE=TRUE	SMC_PBUS_VSENSE	IN 43
39 OUT	SMC_ADC3	MAKE_BASE=TRUE	SMC_BMON_ISENSE	IN 43
39 OUT	SMC_ADC4	MAKE_BASE=TRUE	SMC_TPAD_ISENSE	IN 43
39 OUT	SMC_ADC5	MAKE_BASE=TRUE	SMC_CPU_HI_ISENSE	IN 43
39 OUT	SMC_ADC6	MAKE_BASE=TRUE	SMC_CPU_VSENSE	IN 45
39 OUT	SMC_ADC7	MAKE_BASE=TRUE	SMC_CPU_ISENSE	IN 45
39 OUT	SMC_ADC8	MAKE_BASE=TRUE	SMC_GT_VSENSE	IN 45
39 OUT	SMC_ADC9	MAKE_BASE=TRUE	SMC_GT_ISENSE	IN 45
39 OUT	SMC_ADC10	MAKE_BASE=TRUE	SMC_SA_ISENSE	IN 45
39 OUT	SMC_ADC11	MAKE_BASE=TRUE	SMC_1V55G_ISENSE	IN 44
39 OUT	SMC_ADC12	MAKE_BASE=TRUE	SMC_SSD_ISENSE	IN 43
39 OUT	SMC_ADC13	MAKE_BASE=TRUE	SMC_3V3SSD_ISENSE	IN 44
39 OUT	SMC_ADC14	MAKE_BASE=TRUE	SMC_1V2S3_ISENSE	IN 44
39 OUT	SMC_ADC15	MAKE_BASE=TRUE	SMC_CPU_IMON_ISENSE	IN 45
39 OUT	SMC_ADC16	MAKE_BASE=TRUE	SMC_GT_IMON_ISENSE	IN 45
39 OUT	SMC_ADC17	MAKE_BASE=TRUE	SMC_3V3LCD_ISENSE	IN 44
39 OUT	SMC_ADC18	MAKE_BASE=TRUE	SMC_3V3WLS_ISENSE	IN 44
39 OUT	SMC_ADC19	MAKE_BASE=TRUE	SMC_LCDBKLT_ISENSE	IN 43
39 OUT	SMC_ADC20	MAKE_BASE=TRUE	SMC_SA_IMON_ISENSE	IN 45
39 OUT	SMC_ADC21	MAKE_BASE=TRUE	SMC_5VS4_ISENSE	IN 44
39 OUT	SMC_ADC22	MAKE_BASE=TRUE	SMC_3V3S5_ISENSE	IN 44
39 OUT	SMC_ADC23	MAKE_BASE=TRUE	SMC_TBT_ISENSE	IN 45

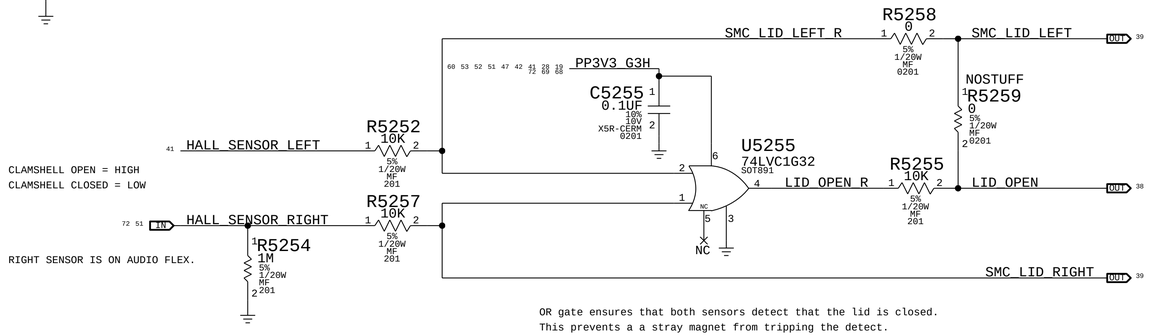
39 IN	SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_THROTTLE_L
39 IN	SMC_GFX_OVERTEMP	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_OVERTEMP
39 IN	SMC_FAN_1_CTL	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_1_CTL
39 IN	SMC_FAN_1_TACH	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_1_TACH
39 IN	SMC_SOC_POR	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_SOC_POR
39 IN	SMC_GFX_SELF_THROTTLE	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_SELF_THROTTLE
39 IN	SPI_SMC_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_CLK
39 IN	SPI_SMC_CS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_CS_L
39 IN	SPI_SMC_MISO	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_MISO
39 IN	SPI_SMC_MOSI	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_MOSI
39 IN	SMC_MIKEYBUS_SEL_LEFT	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_MIKEYBUS_SEL_LEFT
39 IN	SYS_ONEWIRE	MAKE_BASE=TRUE	NO_TEST=1	NC_SYS_ONEWIRE



AMR SENSOR PADS

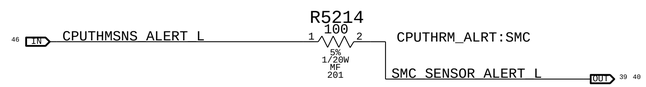


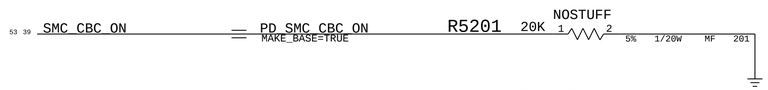
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-05143	1	SUBASSY (T&R) PCBA,HES INTERPOSER 45,X502	J5250	CRITICAL	



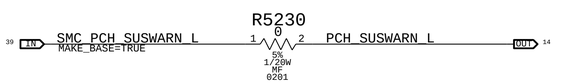
OR gate ensures that both sensors detect that the lid is closed.
This prevents a stray magnet from tripping the detect.

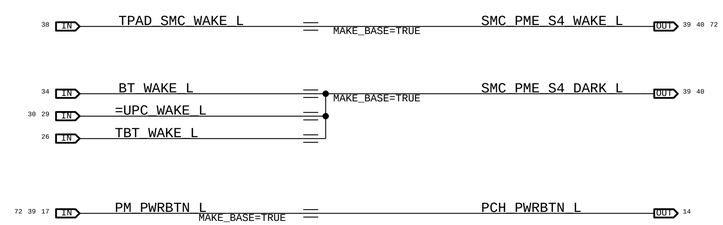
Thermal Alerts

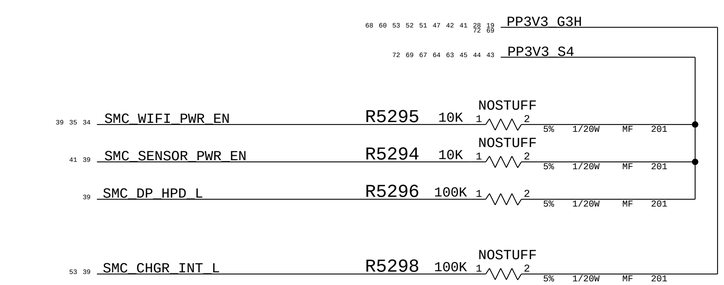


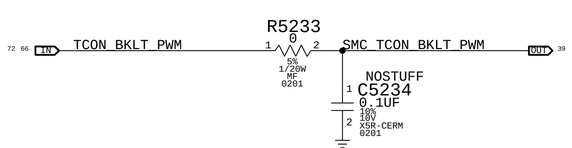


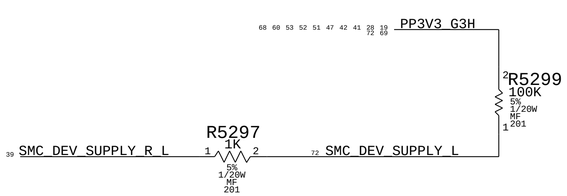
S4 SMC Wake Sources

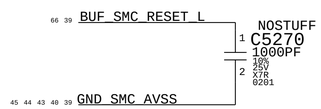












BOM_COST_GROUP=SMC

DESIGN: X502/MLB_CATZ
SYNC_MASTER=PAULM

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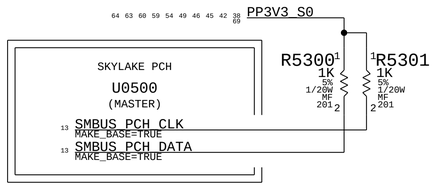
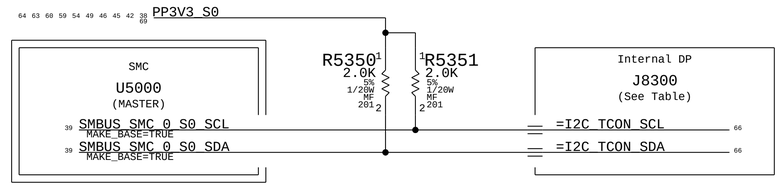
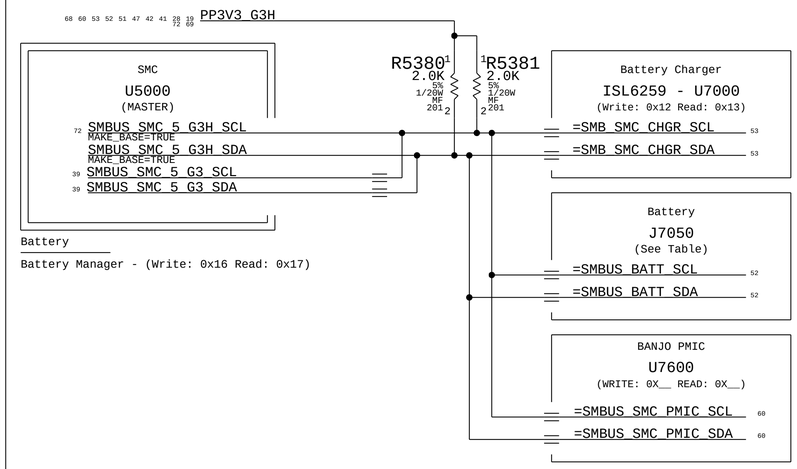
SKYLAKE PCH S0 "SMBUS 0" CONNECTIONS



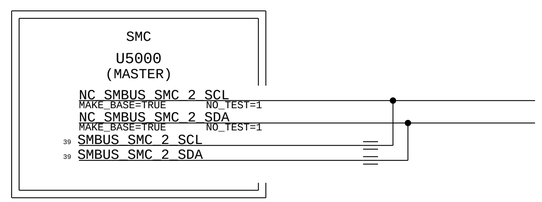
SMC SMBus "0" S0 Connections



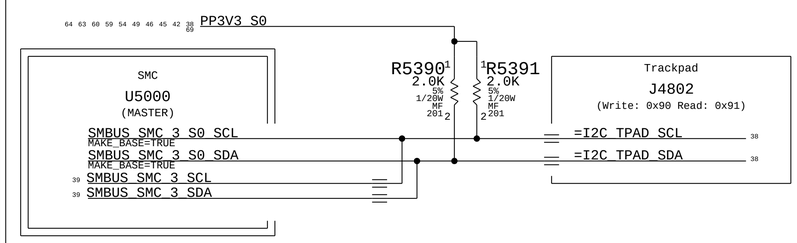
SMC SMBus "5" G3H Connections



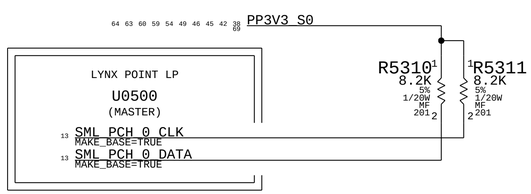
SMC SMBus "2" S3 Connections



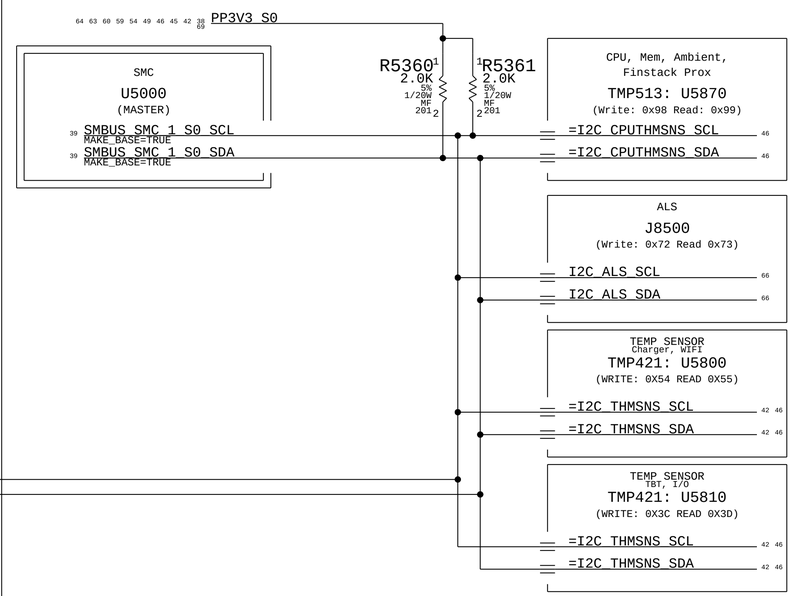
SMC SMBus "3" S0 Connections



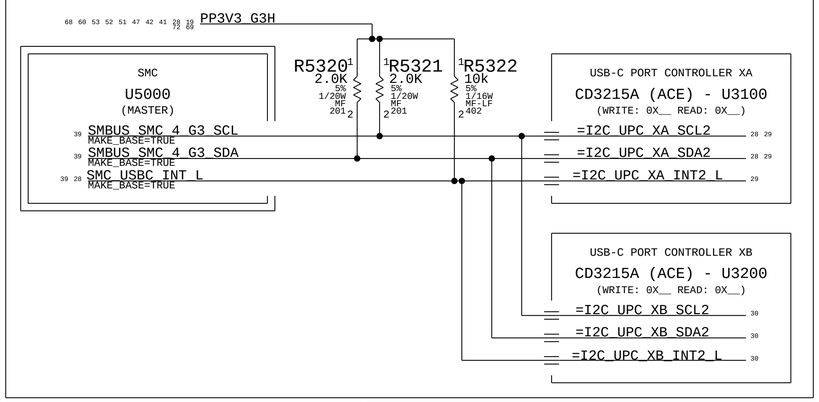
LYNX POINT LP S0 "SMLink 0" Connections



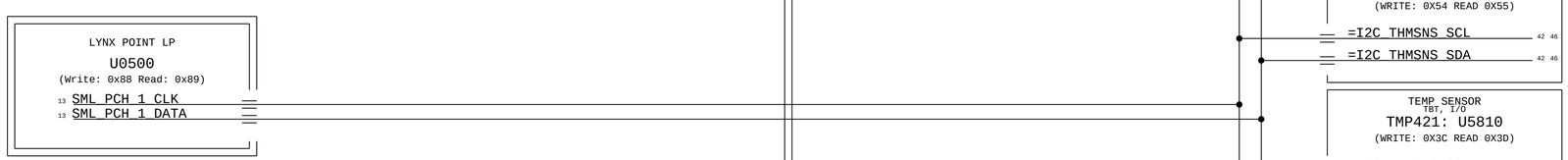
SMC SMBus "1" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to access PCH.

BOM_COST_GROUP=SMC

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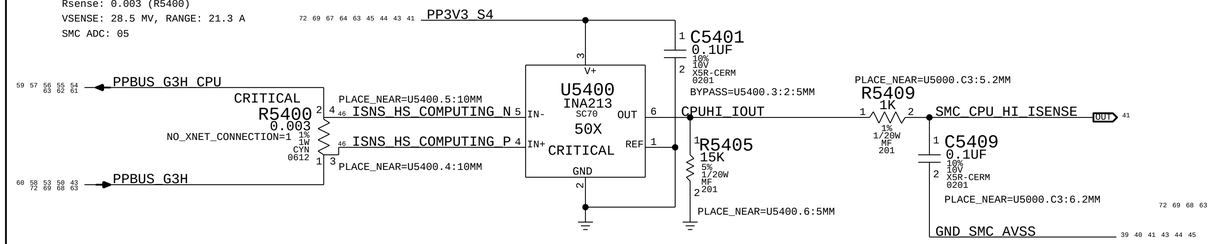
INA21X PARTS HAVE MINOR LEAKAGE PATH FROM INPUTS TO OUTPUT WHEN UNPOWERED. PULL-DOWN RESISTERS ON INA OUTPUTS BLEED OFF THE LEAKAGE CURRENT TO PREVENT SIGNAL PUMP-UP.

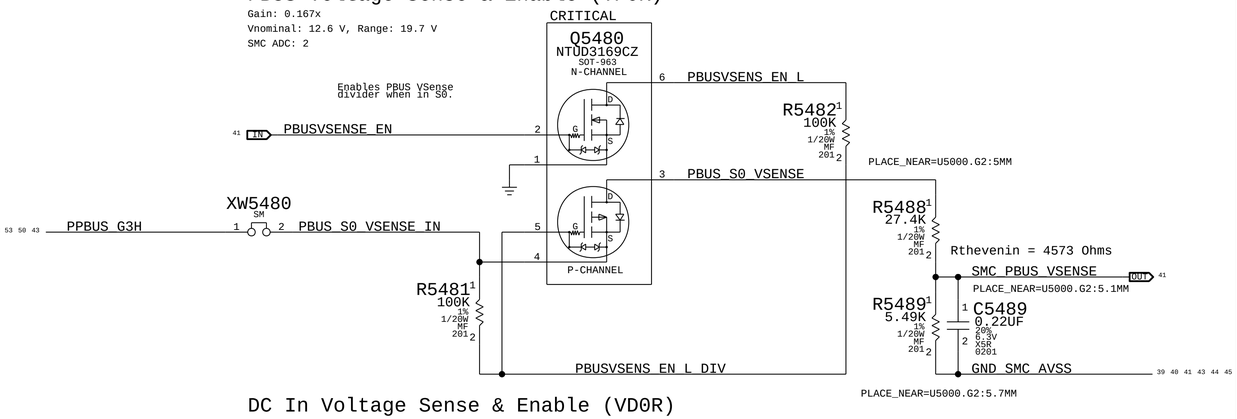
CPU High Side Current Sense (IC0R)

GAIN: 50X, EDP: 9.5 A
Rsense: 0.003 (R5400)
VSENSE: 28.5 MV, RANGE: 21.3 A
SMC ADC: 05



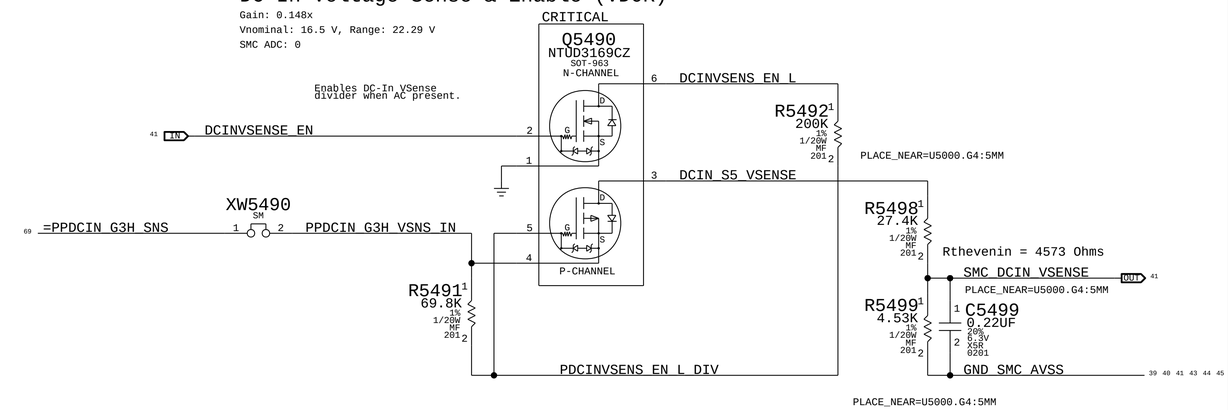
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 19.7 V
SMC ADC: 2



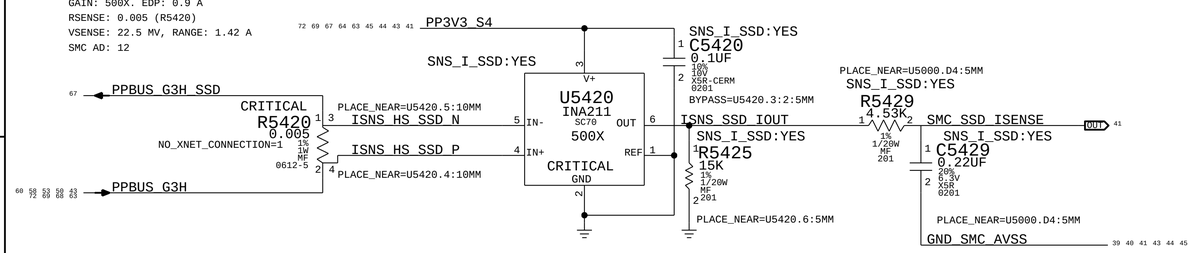
DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x
Vnominal: 16.5 V, Range: 22.29 V
SMC ADC: 0



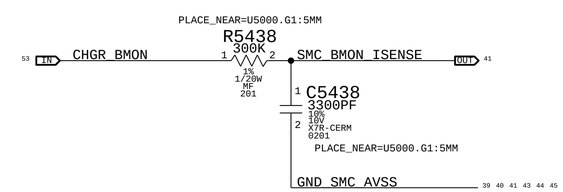
SSD NAND CURRENT SENSE (IHNC)

GAIN: 500X. EDP: 0.9 A
RSENSE: 0.005 (R5420)
VSENSE: 22.5 MV, RANGE: 1.42 A
SMC AD: 12



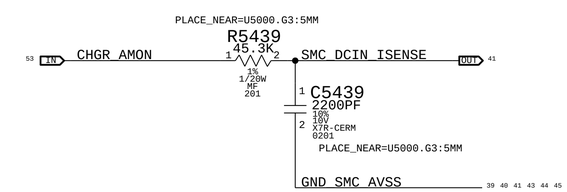
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
RSENSE: 0.005 (R7160)
SMC ADC: 03



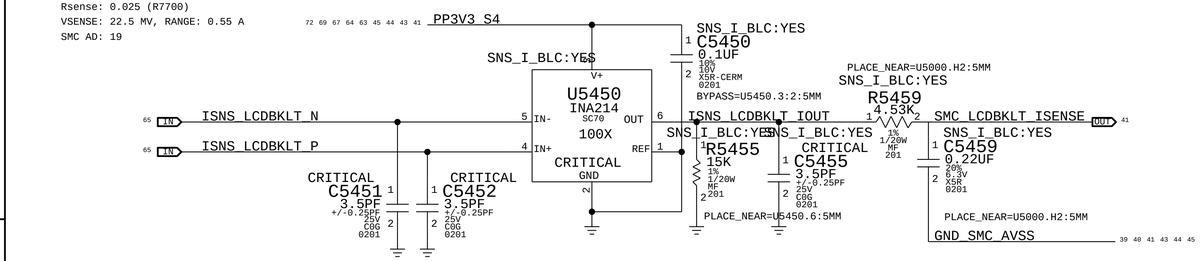
DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
RSENSE: 0.010 (R7120)
SMC ADC: 01



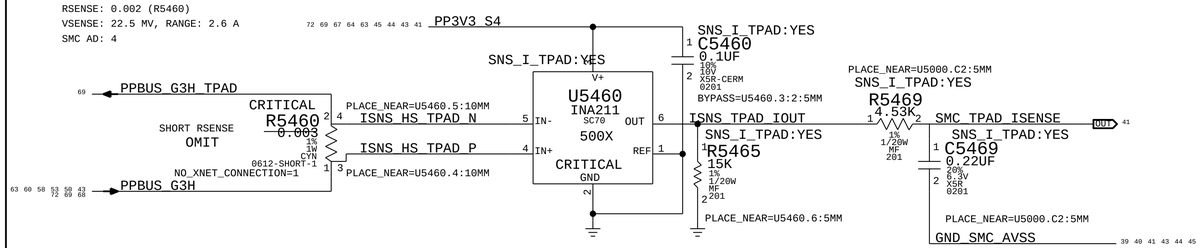
LCD BACKLIGHT CURRENT SENSE (IBLR)

GAIN: 100X. EDP: 0.9 A
Rsense: 0.025 (R7700)
VSENSE: 22.5 MV, RANGE: 0.55 A
SMC AD: 19



TRACKPAD ACTUATOR X239 CURRENT SENSE (ITAR)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R5460)
VSENSE: 22.5 MV, RANGE: 2.6 A
SMC AD: 4



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5429		SNS_I_SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		SNS_I_BLC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		SNS_I_TPAD:NO

BOM_COST_GROUP=SENSORS

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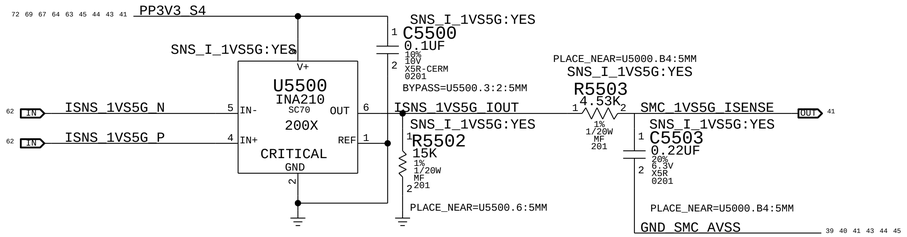
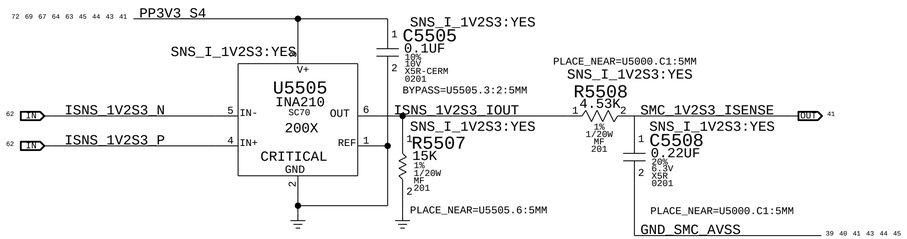
1V_S5G CURRENT SENSE (ISIC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R7700)
VSENSE: 22.5 MV, RANGE: 3.0 A
SMC AD: 11



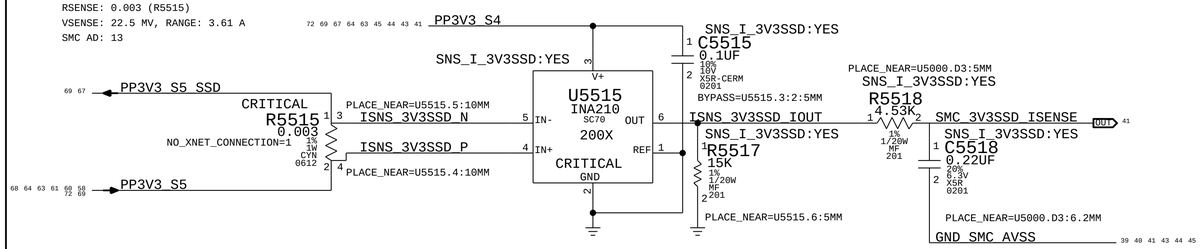
1V2_S3 CURRENT SENSE (IM0C)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 MV, RANGE: 7.67 A
SMC AD: 14



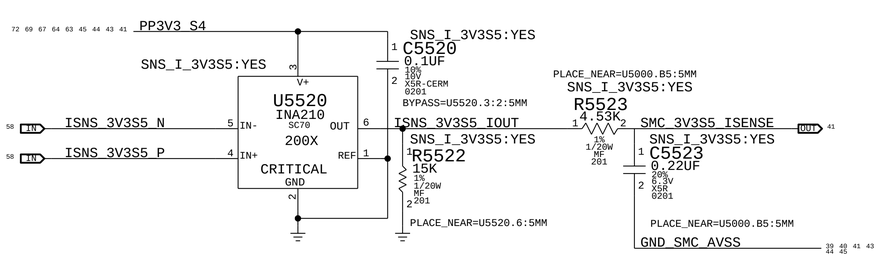
3V3_SSD CURRENT SENSE (IHCC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R5515)
VSENSE: 22.5 MV, RANGE: 3.61 A
SMC AD: 13



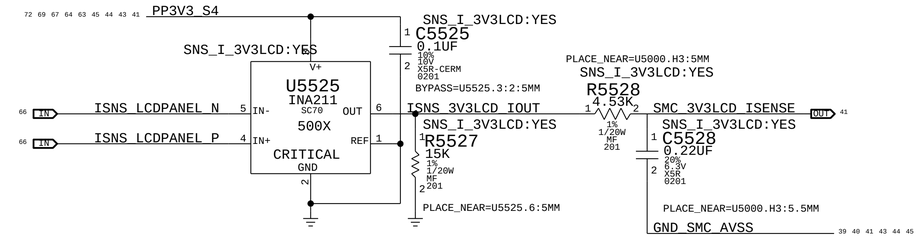
3V3_S5 CURRENT SENSE (IO3R) (HIGH-SIDE)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R7710)
VSENSE: 22.5 MV ?, RANGE: 4 A
SMC AD: 22



3V3_S0 LCD CURRENT SENSE (ILDC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R5525)
VSENSE: 22.5 MV, RANGE: 1.6 A
SMC AD: 17

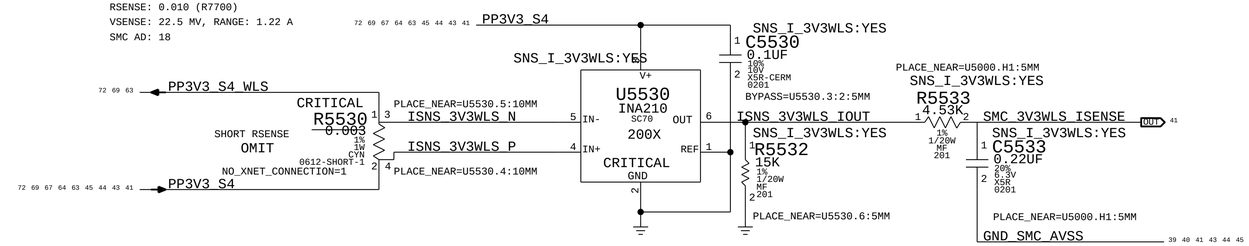


5V_S0 LCD CURRENT SENSE (I___)

GAIN: 500X. EDP: 0.9 A
RSENSE: 0.005 (R8520)
VSENSE: 22.5 MV, RANGE: 1.6 A
SMC AD: 17

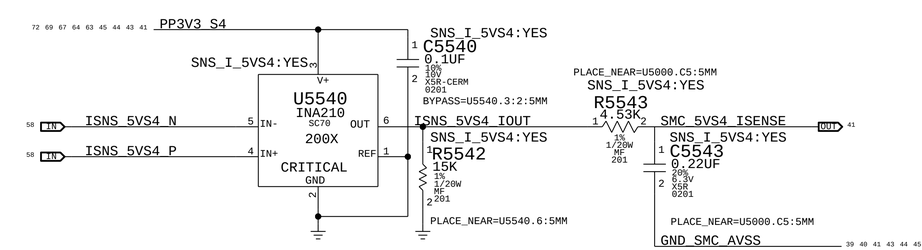
3V3_S4 WIRELESS CURRENT SENSE (IAPC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.010 (R7700)
VSENSE: 22.5 MV, RANGE: 1.22 A
SMC AD: 18



5V_S4 CURRENT SENSE (IO5R) (HIGH-SIDE)

GAIN: 200X. EDP: ?? A
RSENSE: 0.003 (R7900)
VSENSE: 22.5 MV ?, RANGE: 6.8 A
SMC AD: 21



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5503		SNS_I_1VS5G:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5508		SNS_I_1V2S3:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5518		SNS_I_3V3SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5523		SNS_I_3V3S5:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5528		SNS_I_3V3LCD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5533		SNS_I_3V3WLS:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5543		SNS_I_5VS4:NO

BOM_COST_GROUP=SENSORS

DESIGN: X502/MLB_CATZ
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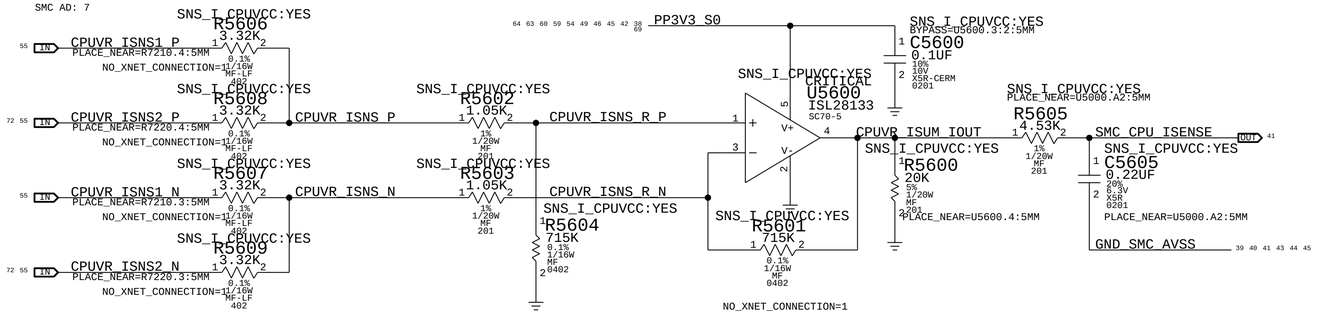
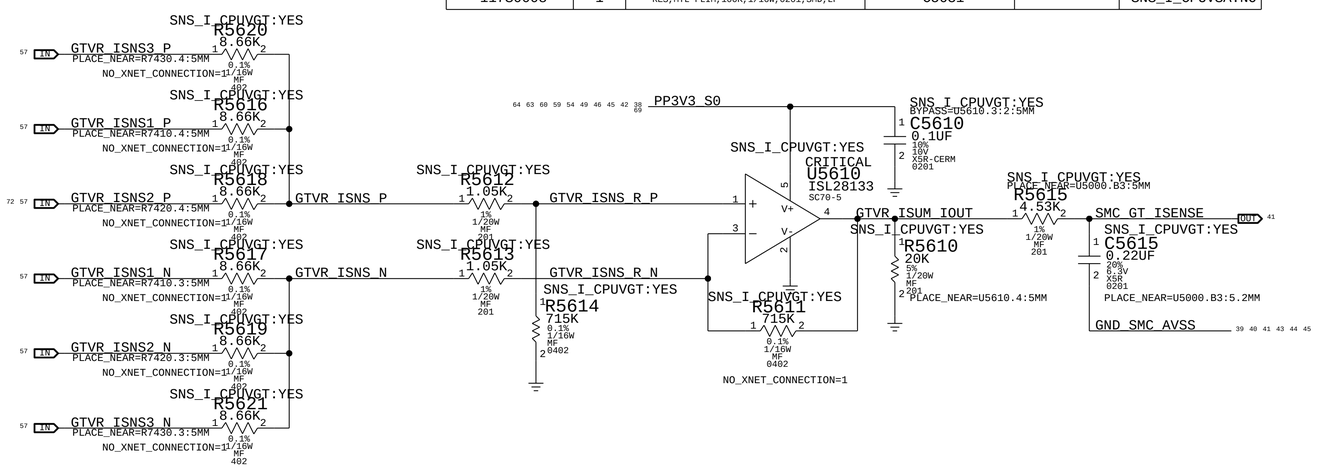
CPU VCC CURRENT SENSE (ICAC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 MV, RANGE: 2.27 A
SMC AD: 7



CPU GT CURRENT SENSE (ICGC)

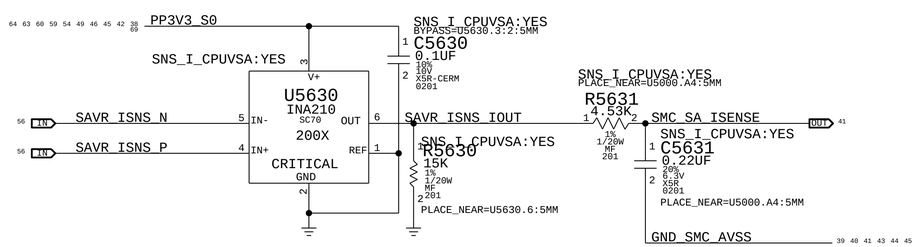
GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 MV, RANGE: 2.27 A
SMC AD: 9



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5605		SNS_I_CPUVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5615		SNS_I_CPUVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5631		SNS_I_CPUVSA:NO

CPU SA CURRENT SENSE (ICSC)

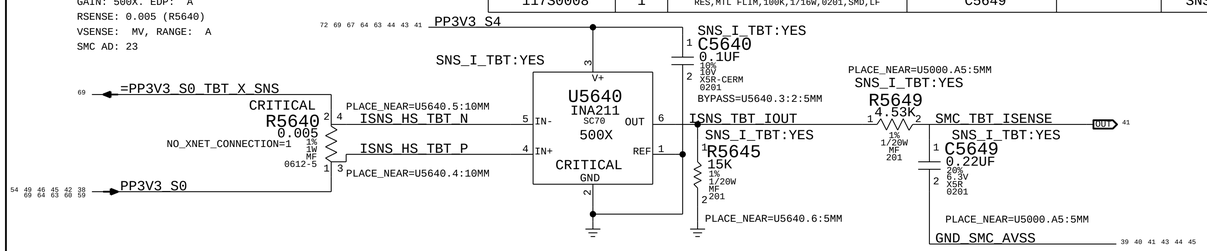
GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 MV, RANGE: 7.67 A
SMC AD: 10



TBT CURRENT SENSE (IULC)

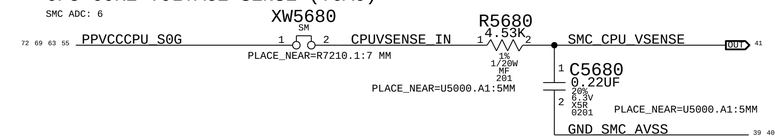
GAIN: 500X. EDP: A
RSENSE: 0.005 (R5640)
VSENSE: MV, RANGE: A
SMC AD: 23

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5649		SNS_I_TBT:NO



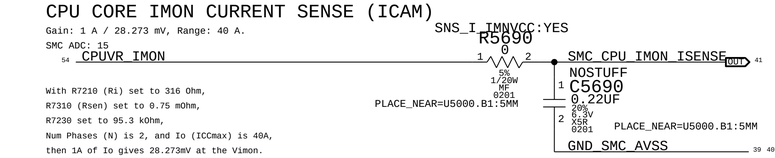
CPU CORE VOLTAGE SENSE (VCAC)

SMC ADC: 6



CPU CORE IMON CURRENT SENSE (ICAM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 15

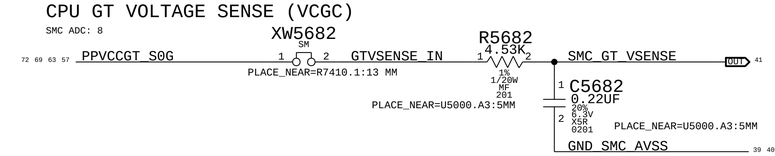


With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5690		SNS_I_IMNVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5692		SNS_I_IMNVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5691		SNS_I_IMNVSA:NO

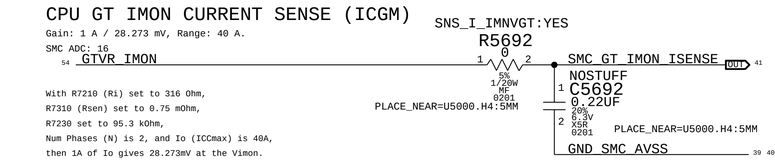
CPU GT VOLTAGE SENSE (VCGC)

SMC ADC: 8



CPU GT IMON CURRENT SENSE (ICGM)

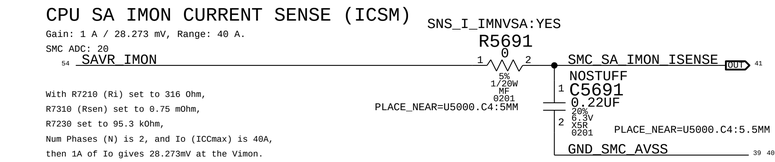
Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 16



With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

CPU SA IMON CURRENT SENSE (ICSM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 20



With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

BOM_COST_GROUP=SENSORS

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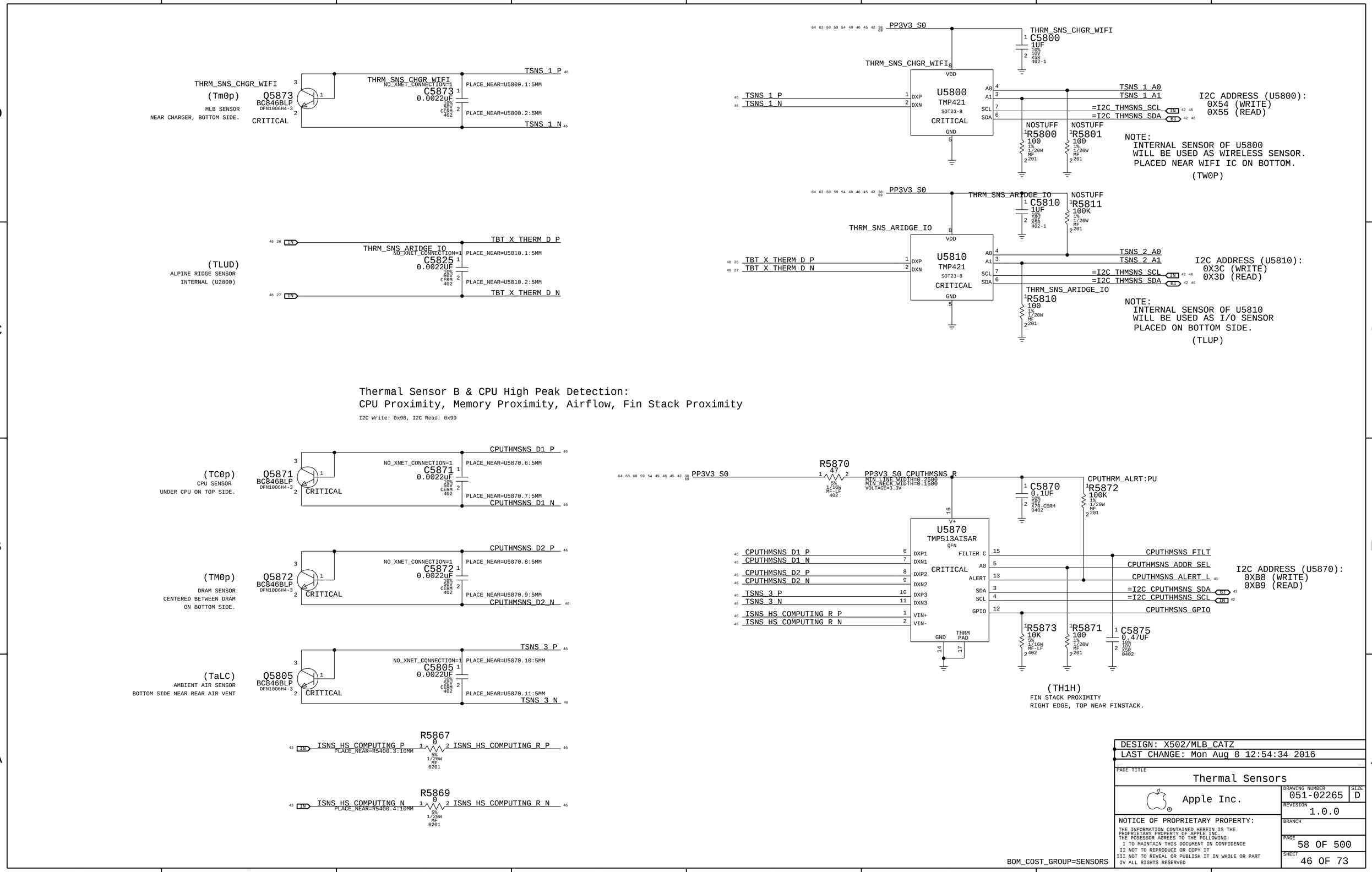

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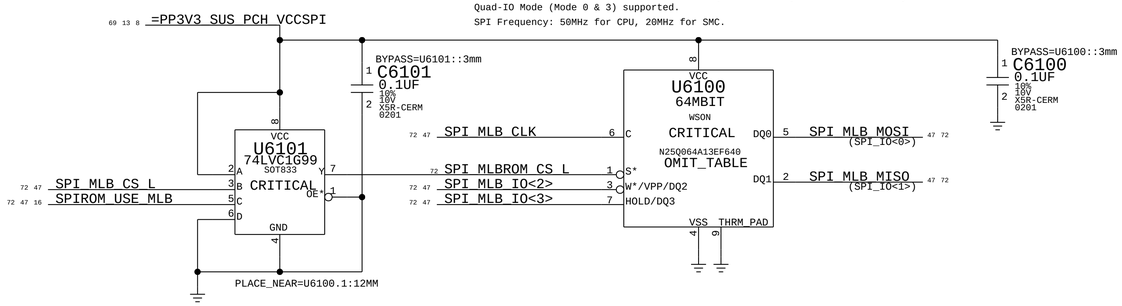
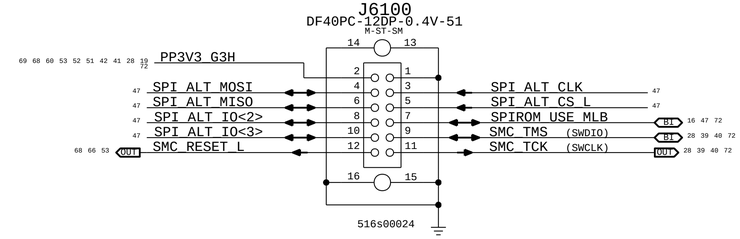
SPI ROM - Combo BGA Footprint (3 vendors)

Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.

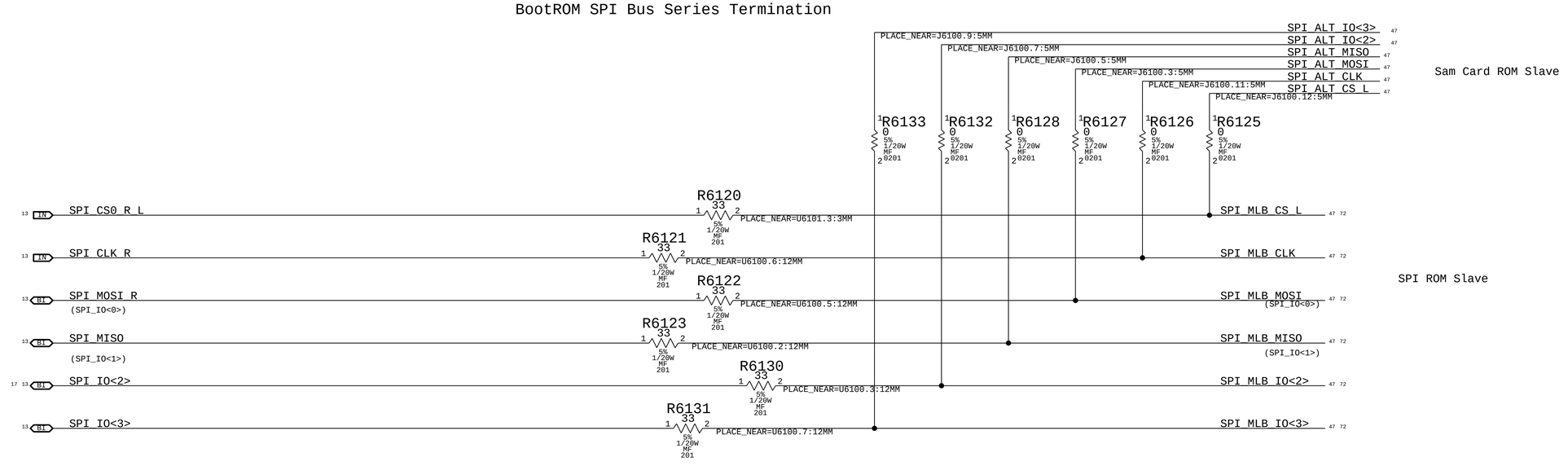


SPI+SWD SAM Connector

CRITICAL



BootROM SPI Bus Series Termination



BOM_COST_GROUP=CPU SUPPORT

DESIGN: X502/MLB_CATZ
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PAGE TITLE
SPI ROM & SWD Debug

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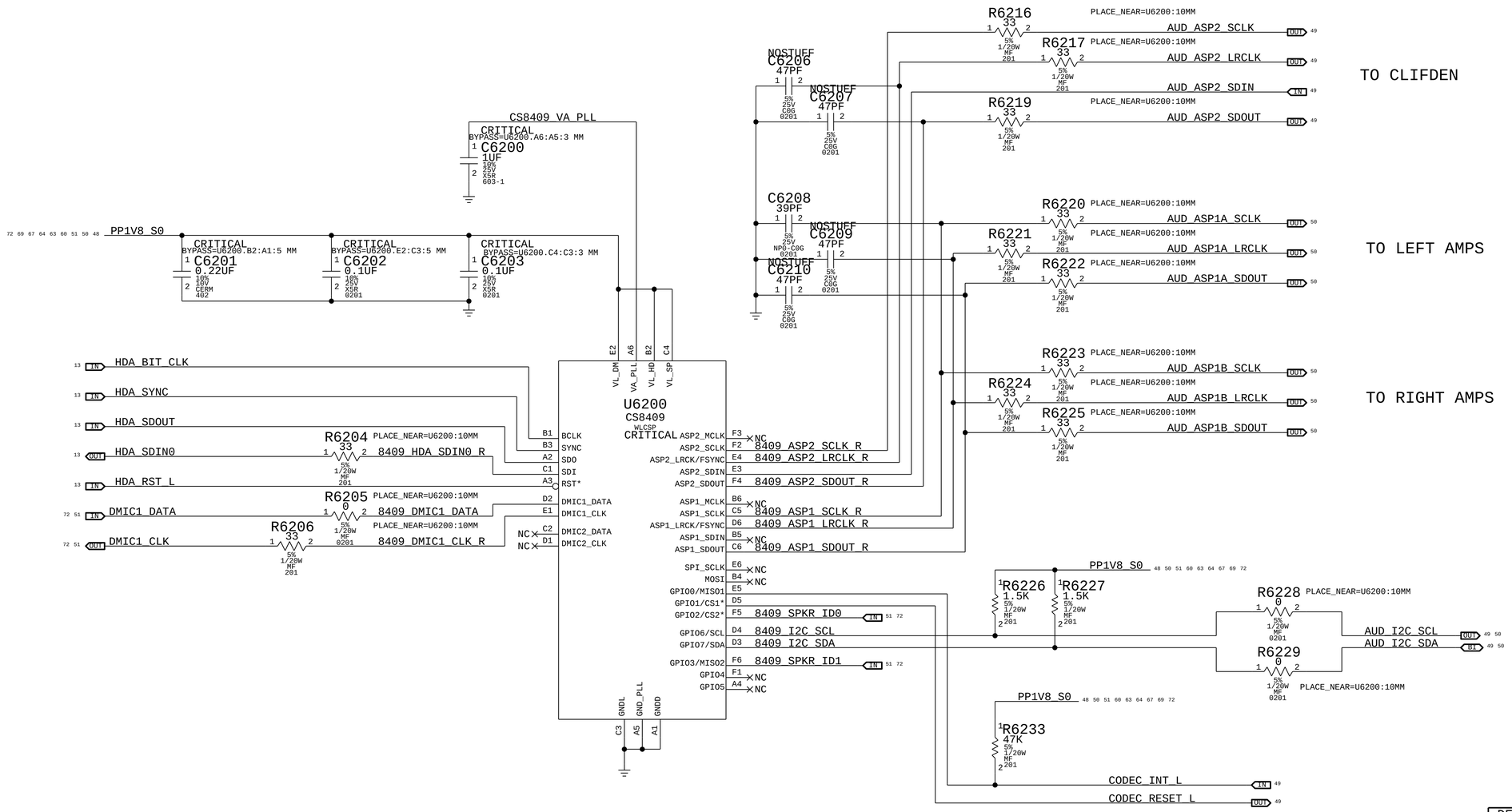

HELP BLOCK PHYSICAL DAMAGE TO U6200

C6299
4.7UF
20%
6.3V
X5R
402

CKPLUS_WAIVE=TERMSHORTED

BOM_COST_GROUP=AUDIO

DESIGN: X502/MLB_CATZ
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PAGE TITLE
HDA BRIDGE

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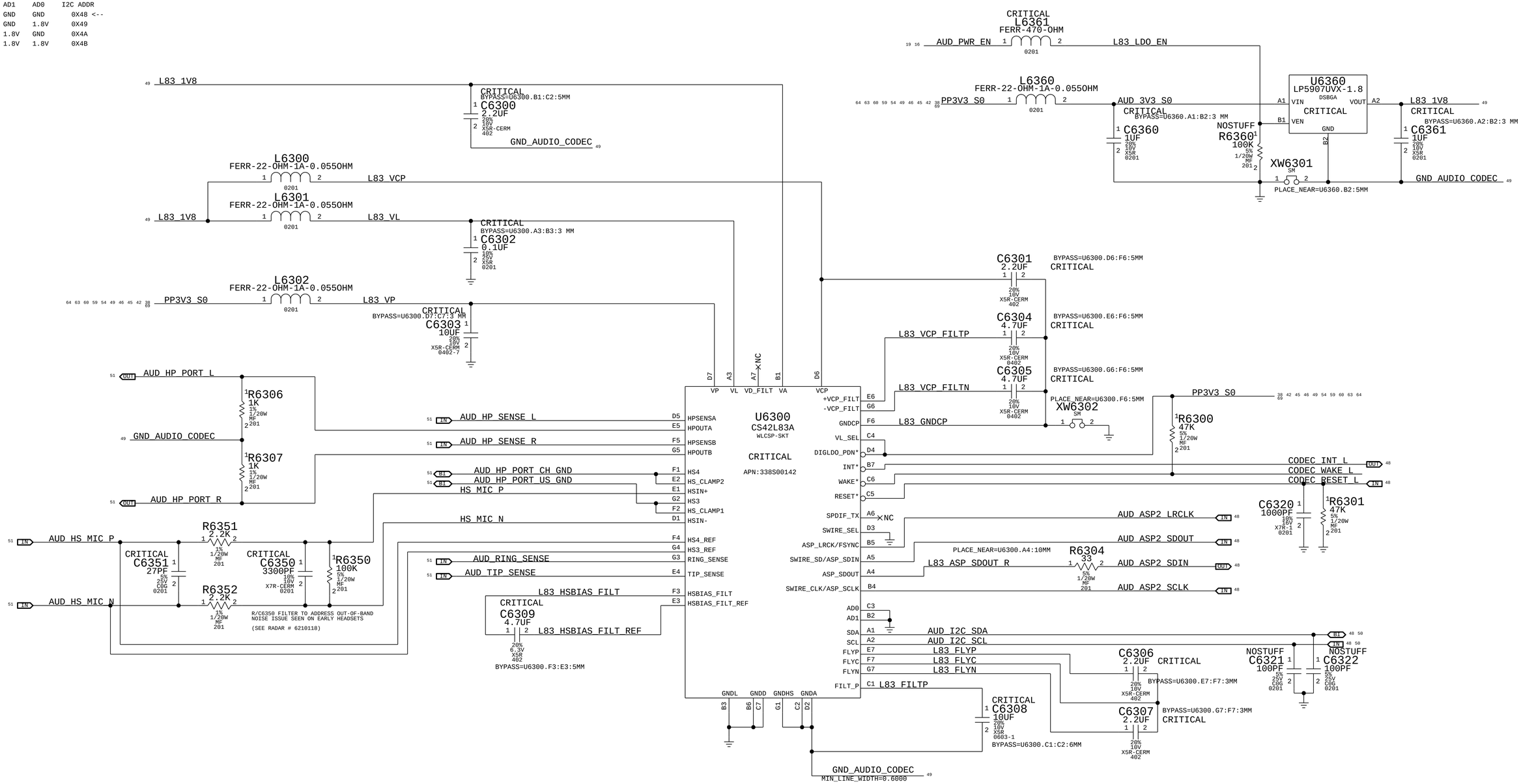
AD1	AD0	I2C ADDR
GND	GND	0X48 <--
GND	1.8V	0X49
1.8V	GND	0X4A
1.8V	1.8V	0X4B



BOM_COST_GROUP=AUDIO

DESIGN: X502/MLB_CATZ
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PAGE TITLE
JACK CODEC

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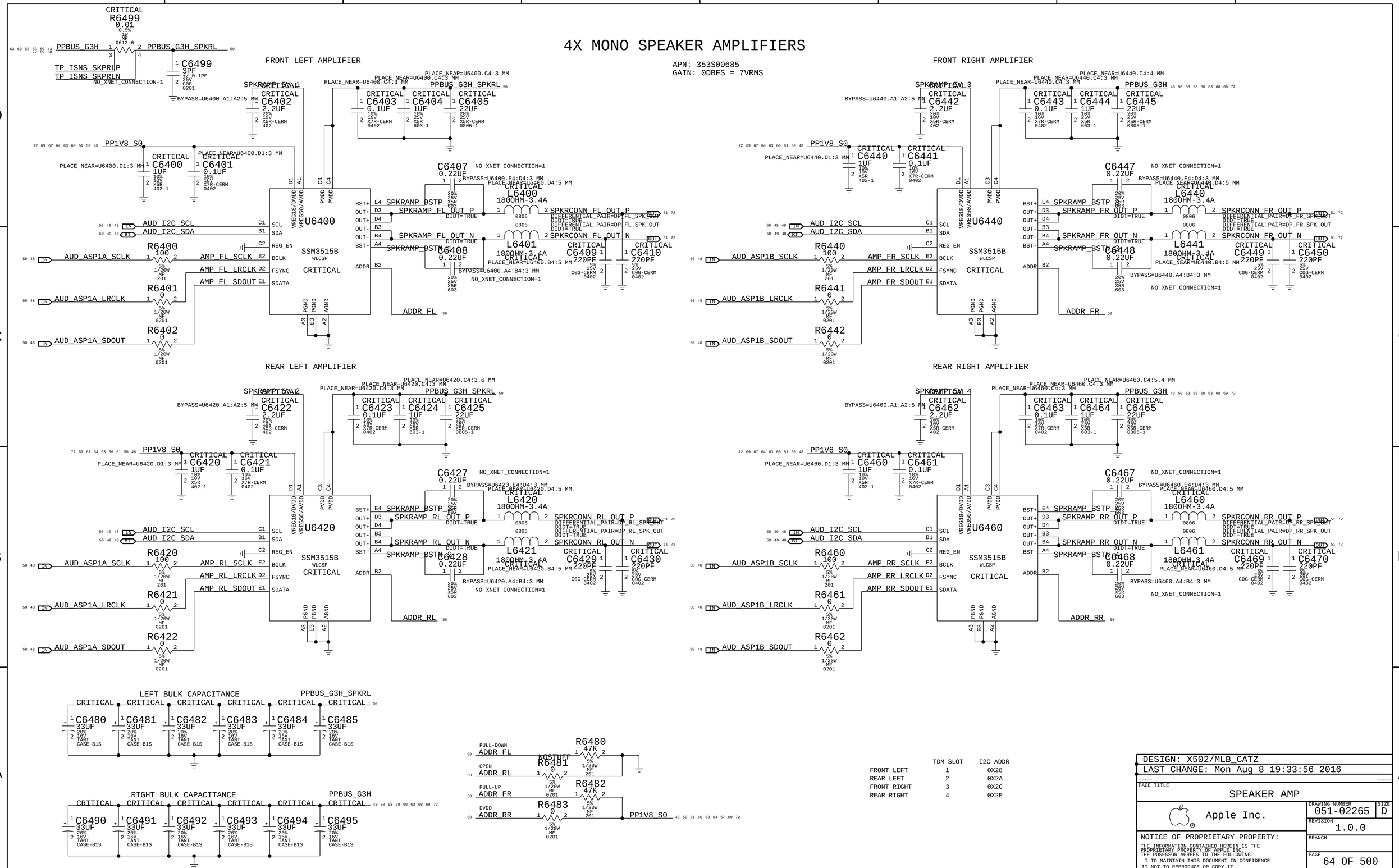
4X MONO SPEAKER AMPLIFIERS

APN: 353S00685
GAIN: 0DBFS = 7VRMS



	TDM SLOT	I2C ADDR
FRONT LEFT	1	0X28
REAR LEFT	2	0X2A
FRONT RIGHT	3	0X2C
REAR RIGHT	4	0X2E

BOM_COST_GROUP=AUDIO

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SPEAKER AMP

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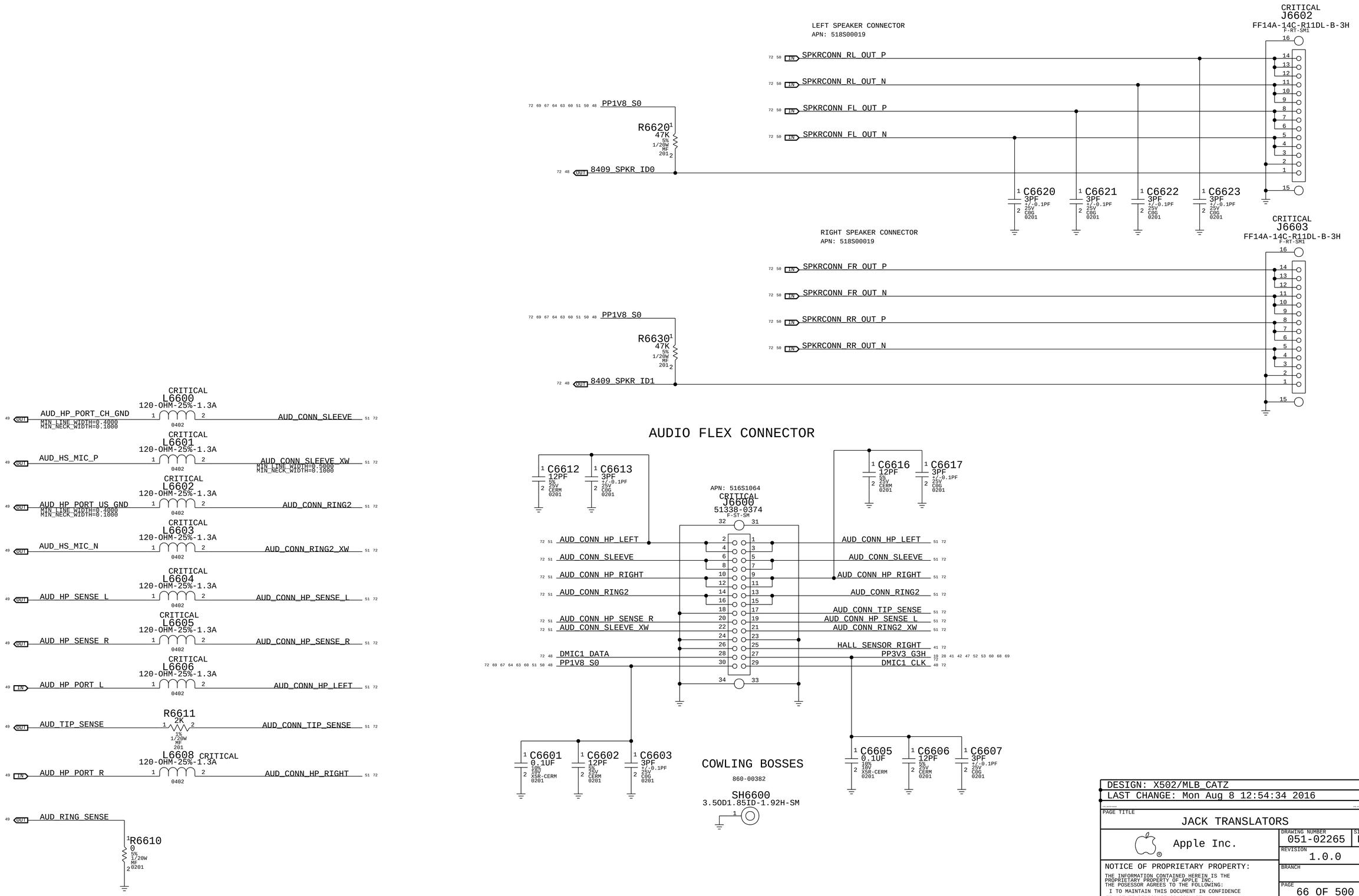
LEFT SPEAKER CONNECTOR
APN: 518S00019
CRITICAL
J6602
FF14A-14C-R11DL-B-3H
F-RT-SM1
SPKRCONN_RL_OUT_P
SPKRCONN_RL_OUT_N
SPKRCONN_FL_OUT_P
SPKRCONN_FL_OUT_N
PP1V8_S0
R6620
47K
5%
1/20W
MF
201
8409_SPKR_ID0
C6620
3PF
+/-0.1PF
25V
C0G
0201
C6621
3PF
+/-0.1PF
25V
C0G
0201
C6622
3PF
+/-0.1PF
25V
C0G
0201
C6623
3PF
+/-0.1PF
25V
C0G
0201
RIGHT SPEAKER CONNECTOR
APN: 518S00019
CRITICAL
J6603
FF14A-14C-R11DL-B-3H
F-RT-SM1
SPKRCONN_FR_OUT_P
SPKRCONN_FR_OUT_N
SPKRCONN_RR_OUT_P
SPKRCONN_RR_OUT_N
PP1V8_S0
R6630
47K
5%
1/20W
MF
201
8409_SPKR_ID1
AUDIO FLEX CONNECTOR
APN: 516S1064
CRITICAL
J6600
51338-0374
F-ST-SM
AUD_CONN_HP_LEFT
AUD_CONN_SLEEVE
AUD_CONN_HP_RIGHT
AUD_CONN_RING2
AUD_CONN_HP_SENSE_R
AUD_CONN_SLEEVE_XW
DMIC1_DATA
PP1V8_S0
AUD_CONN_TIP_SENSE
AUD_CONN_HP_SENSE_L
AUD_CONN_RING2_XW
HALL_SENSOR_RIGHT
PP3V3_G3H
DMIC1_CLK
C6612
12PF
5%
25V
CERM
0201
C6613
3PF
+/-0.1PF
25V
C0G
0201
C6616
12PF
5%
25V
CERM
0201
C6617
3PF
+/-0.1PF
25V
C0G
0201
C6601
0.1UF
10%
10V
X5R-CERM
0201
C6602
12PF
5%
25V
CERM
0201
C6603
3PF
+/-0.1PF
25V
C0G
0201
C6605
0.1UF
10%
10V
X5R-CERM
0201
C6606
12PF
5%
25V
CERM
0201
C6607
3PF
+/-0.1PF
25V
C0G
0201
COWLING BOSSES
860-00382
SH6600
3.5OD1.85ID-1.92H-SM
AUD_HP_PORT_CH_GND
AUD_CONN_SLEEVE
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1000
L6600
120-OHM-25%-1.3A
0402
AUD_HS_MIC_P
AUD_CONN_SLEEVE_XW
L6601
AUD_HP_PORT_US_GND
AUD_CONN_RING2
L6602
AUD_HS_MIC_N
AUD_CONN_RING2_XW
L6603
AUD_HP_SENSE_L
AUD_CONN_HP_SENSE_L
L6604
AUD_HP_SENSE_R
AUD_CONN_HP_SENSE_R
L6605
AUD_HP_PORT_L
AUD_CONN_HP_LEFT
L6606
AUD_TIP_SENSE
AUD_CONN_TIP_SENSE
R6611
2K
1%
1/20W
MF
201
AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
L6608
AUD_RING_SENSE
R6610
0
5%
1/20W
MF
0201
BOM_COST_GROUP=AUDIO
DESIGN: X502/MLB_CATZ
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PAGE TITLE
JACK TRANSLATORS
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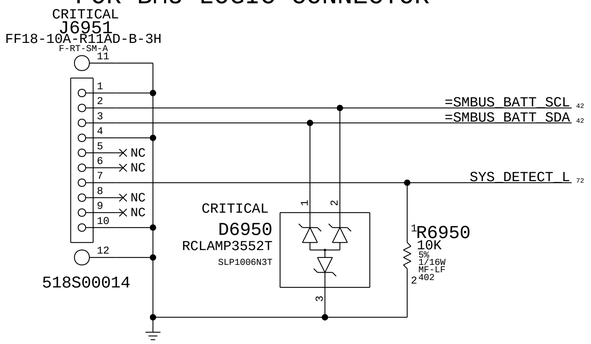
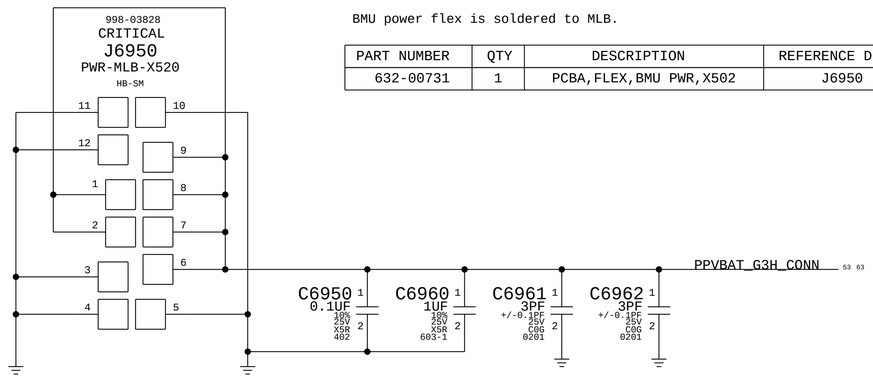
POR BMU LOGIC CONNECTOR



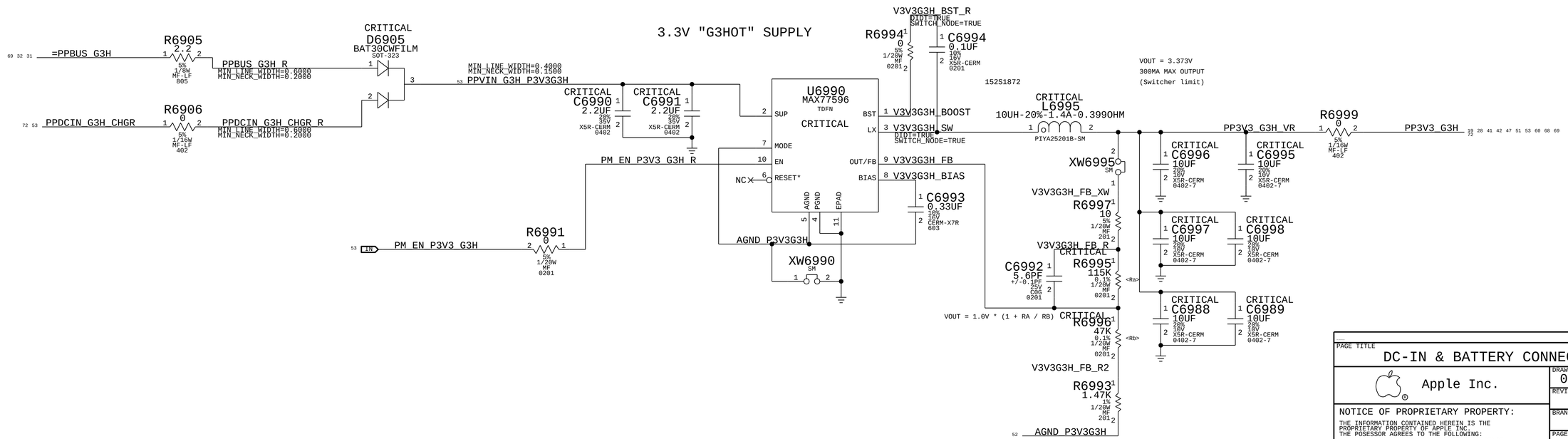
POR BATTERY (BMU) FLEX SOLDER PADS.



BMU power flex is soldered to MLB.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00731	1	PCBA,FLEX,BMU PWR,X502	J6950	CRITICAL	

3.3V "G3HOT" SUPPLY



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
DC-IN & BATTERY CONNECTORS

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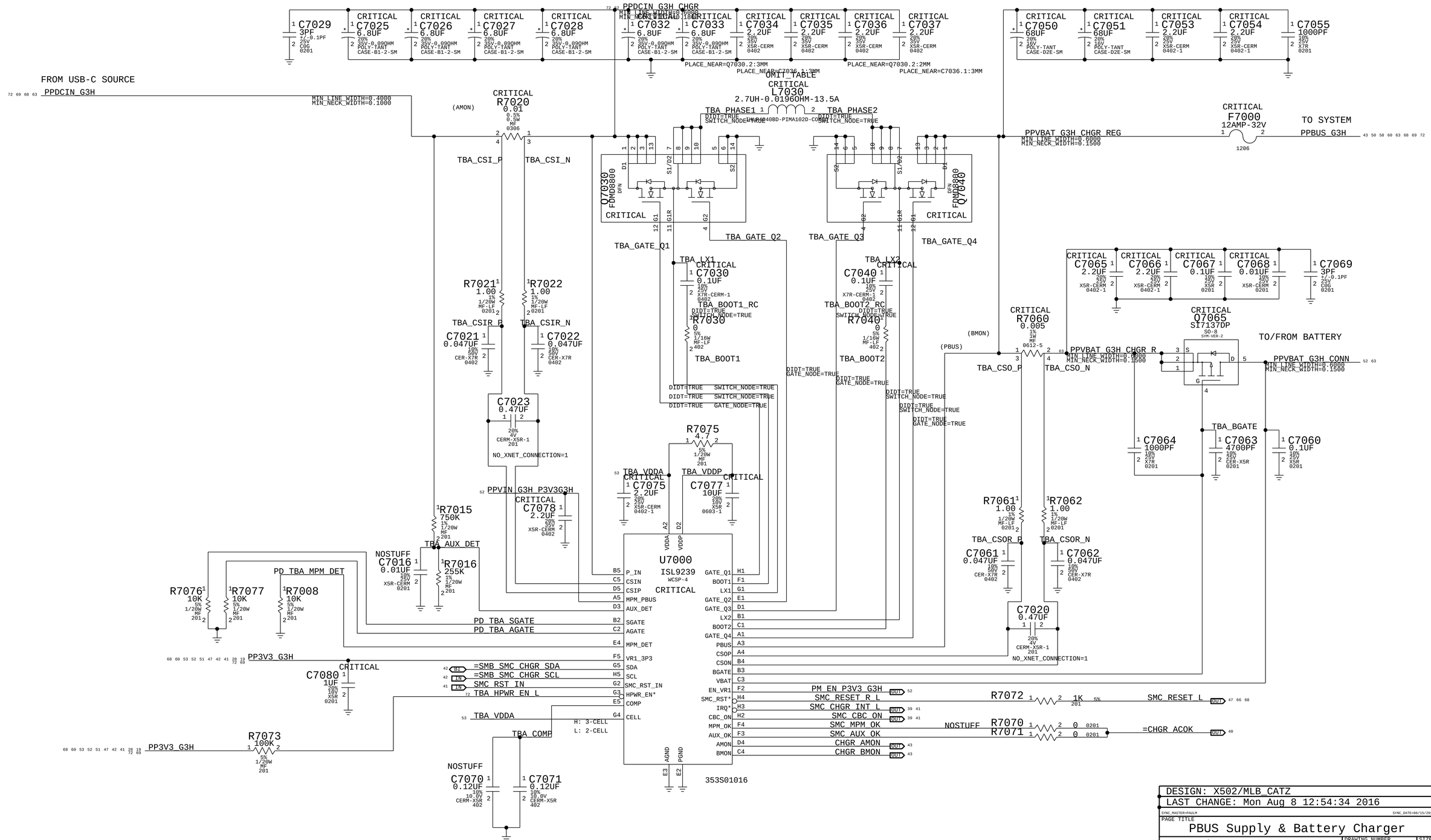

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00198	1	IND,MLD,2.7UH,19.6MO,12.5A,10.9X10X2.4MM	L7030	CRITICAL	

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PAGE TITLE
PBUS Supply & Battery Charger

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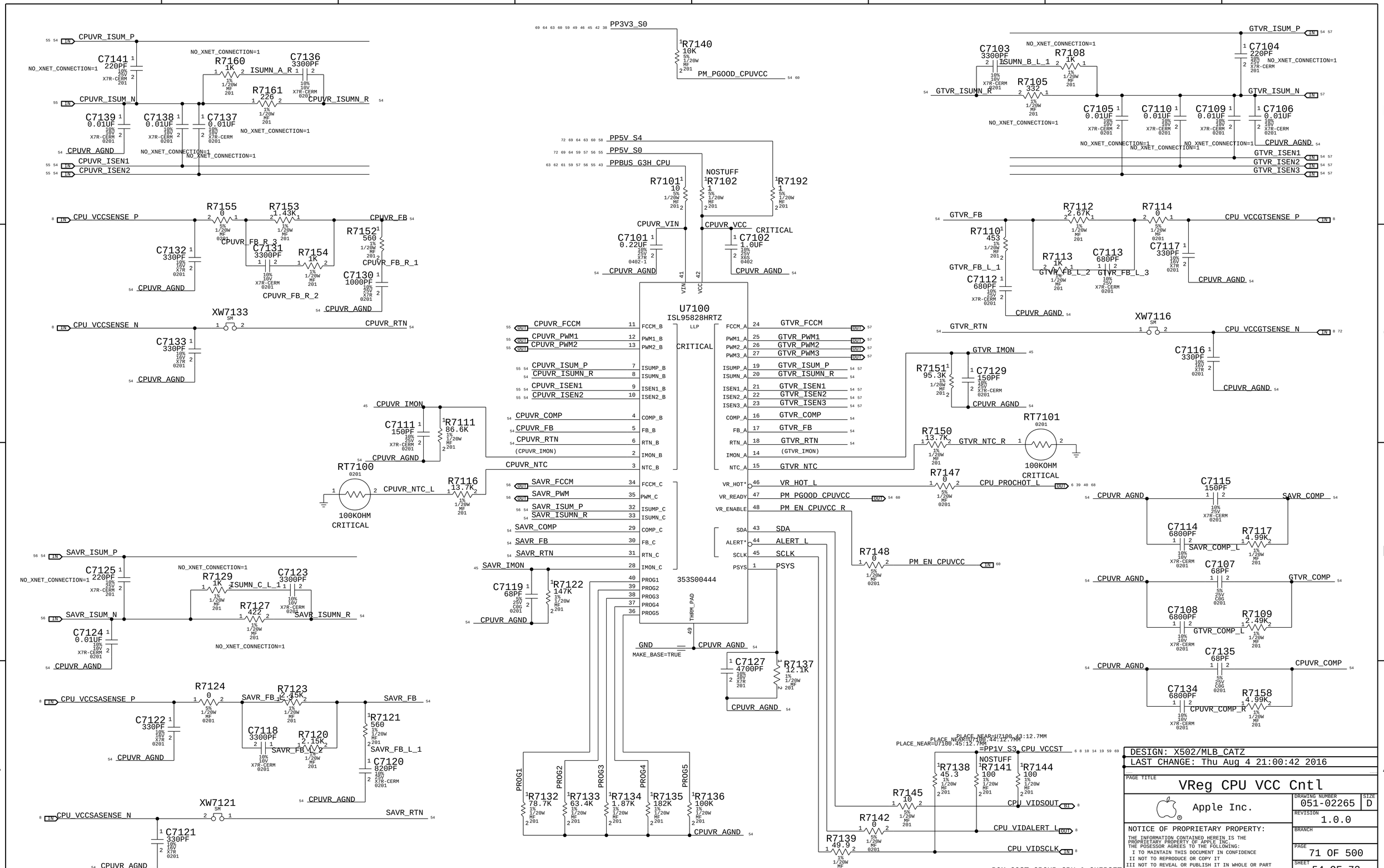

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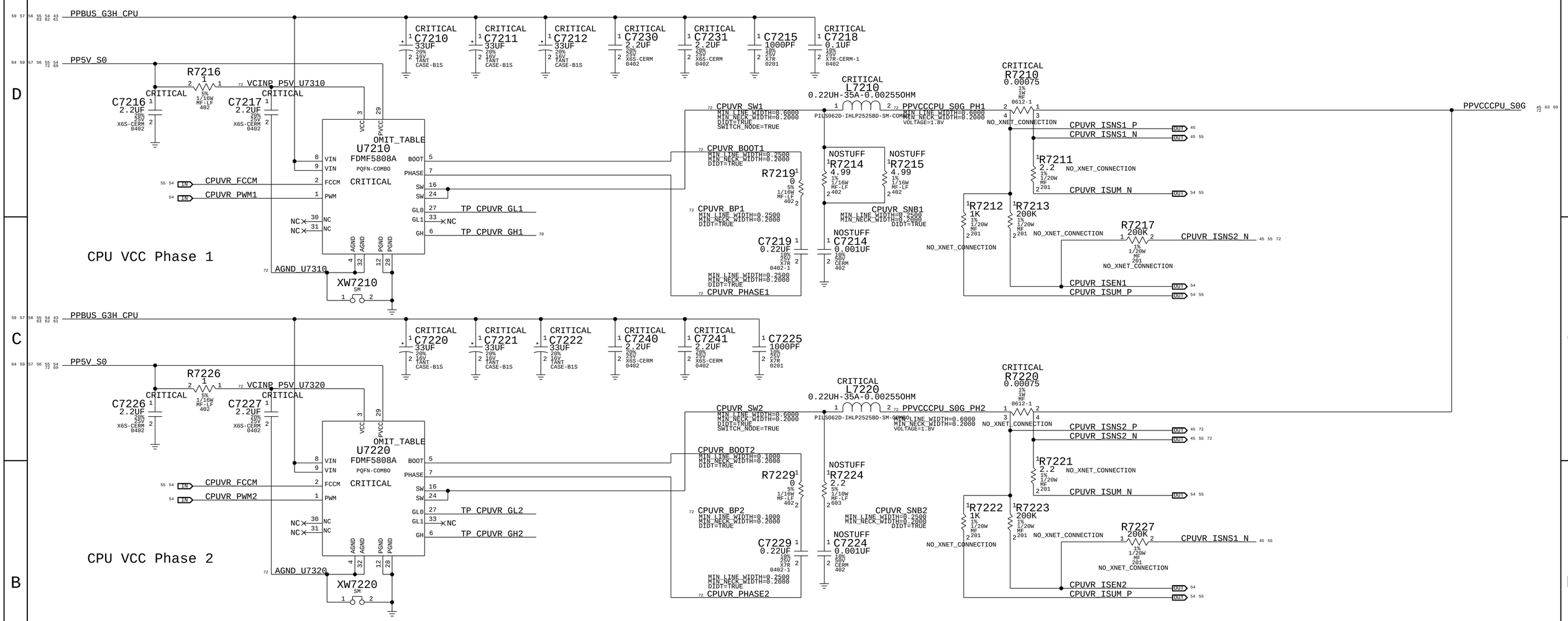

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353S00497	5	IC,SIC635,DR MOS,IMVP-8,40A,PQFN31,5X5	U7210,U7220,U7410,U7420,U7430	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

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PAGE TITLE
CPU IMVP VCC & VCCSA

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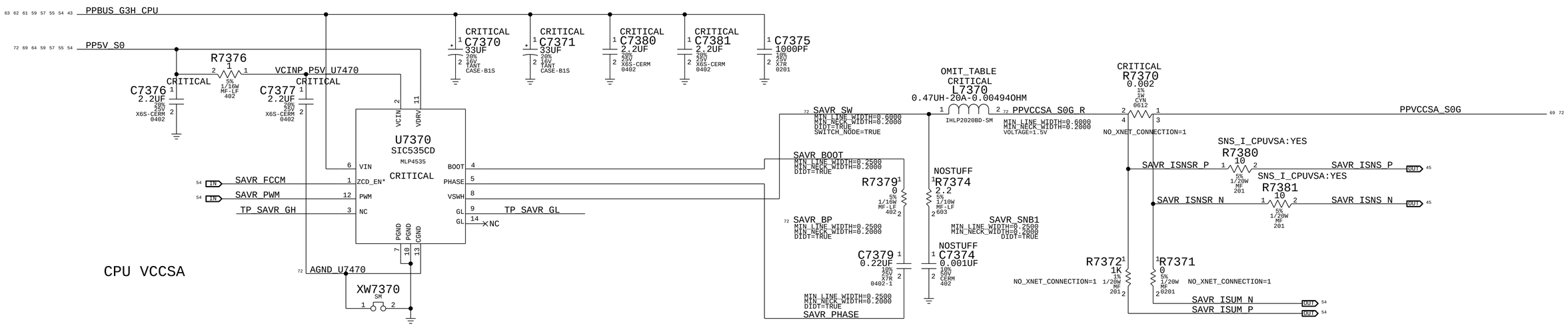
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00241	1	IND,MLD,0.47UH,4.9MO,17.5A,5.4X5.2X2.4MM	L7370	CRITICAL	



BOM_COST_GROUP=CPU & CHIPSET

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PAGE TITLE
IMVP VCCSA

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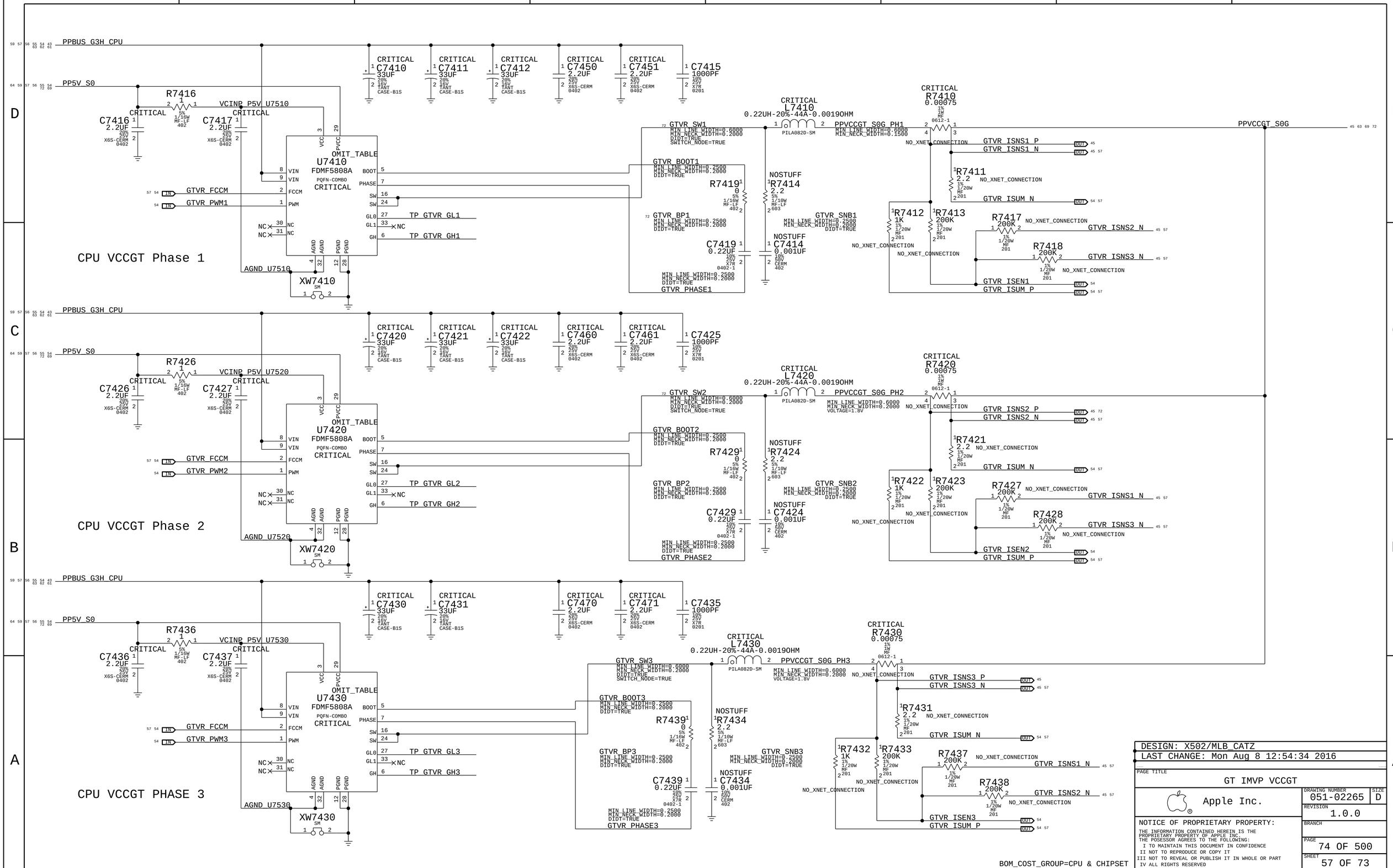

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PAGE TITLE: GT IMVP VCCGT

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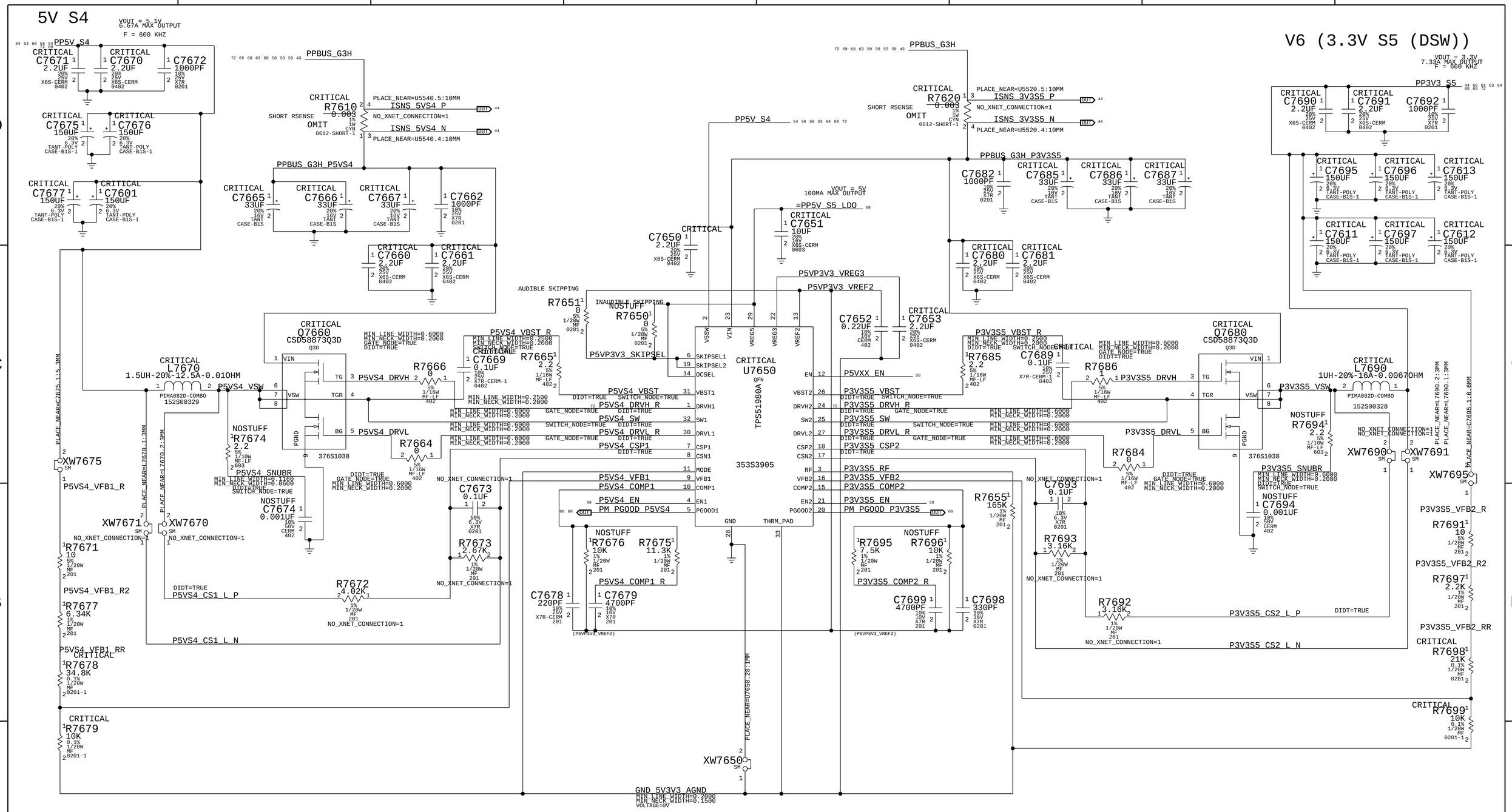

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PAGE TITLE: VR - 5V S4, 3.3V S5	
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BOM_COST_GROUP=PLATFORM POWER

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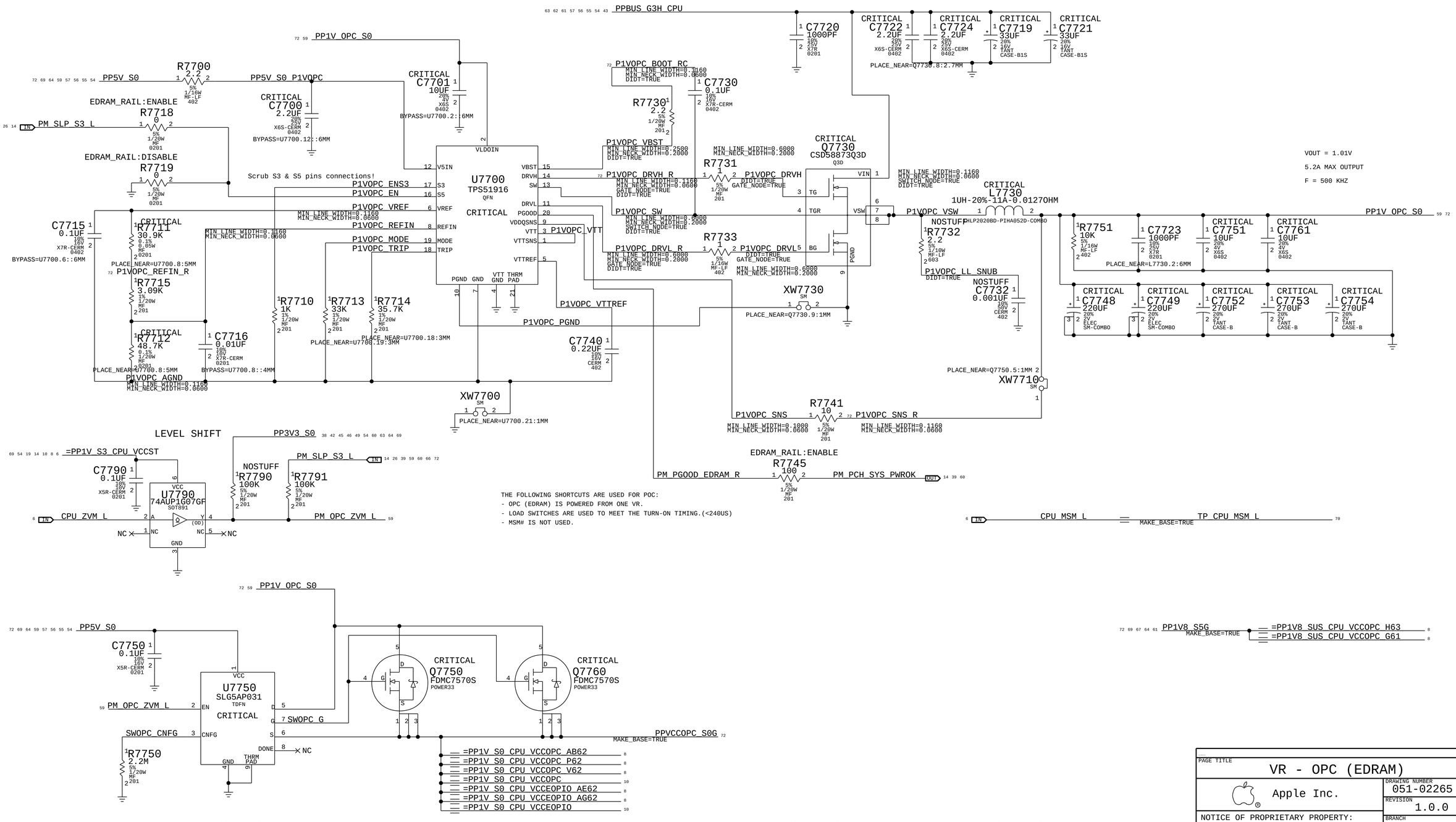
1V S0 REGULATOR FOR EDRAM (ON-PACKAGE CACHE)



PAGE TITLE
VR - OPC (EDRAM)

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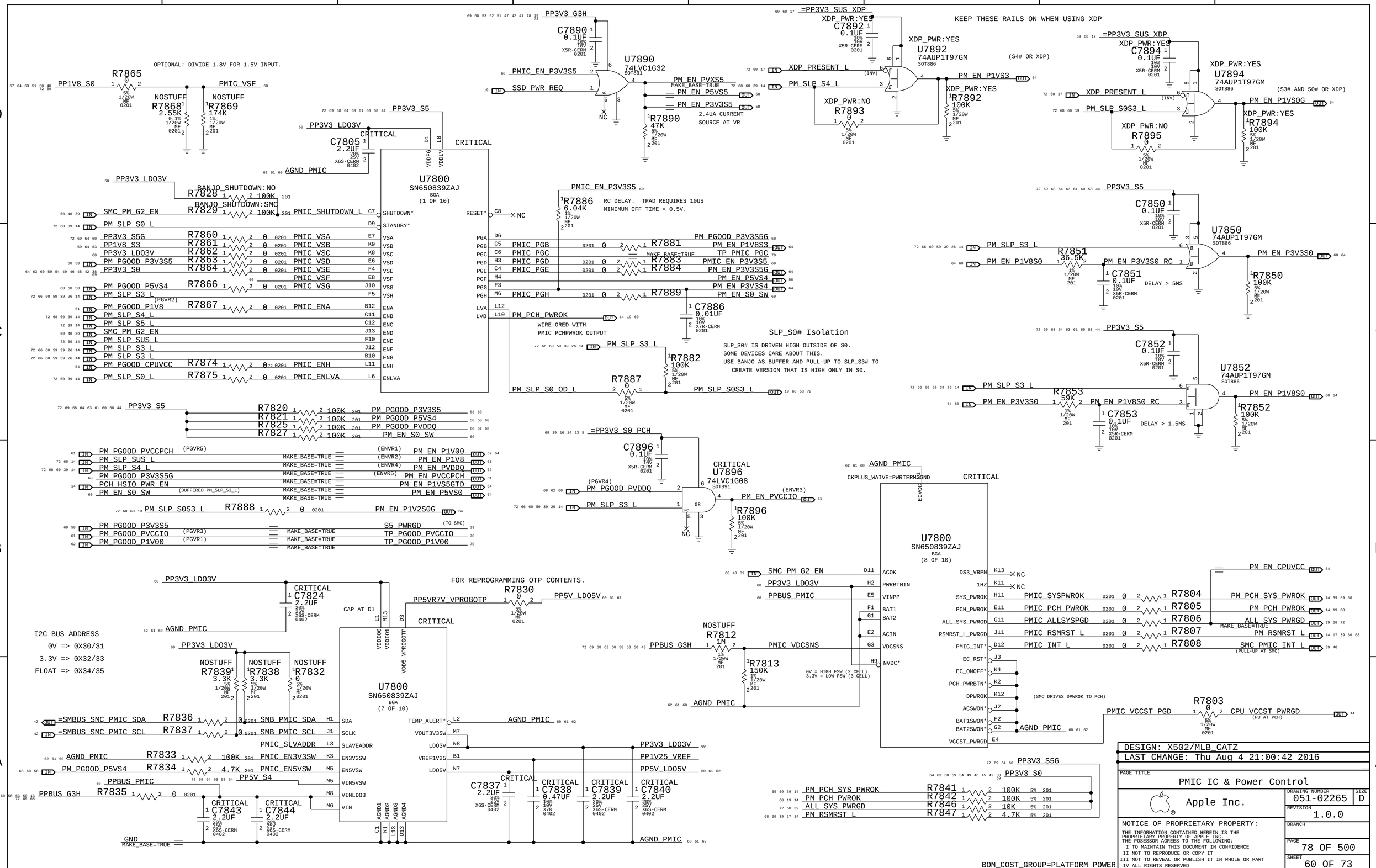

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PAGE TITLE
PMIC IC & Power Control

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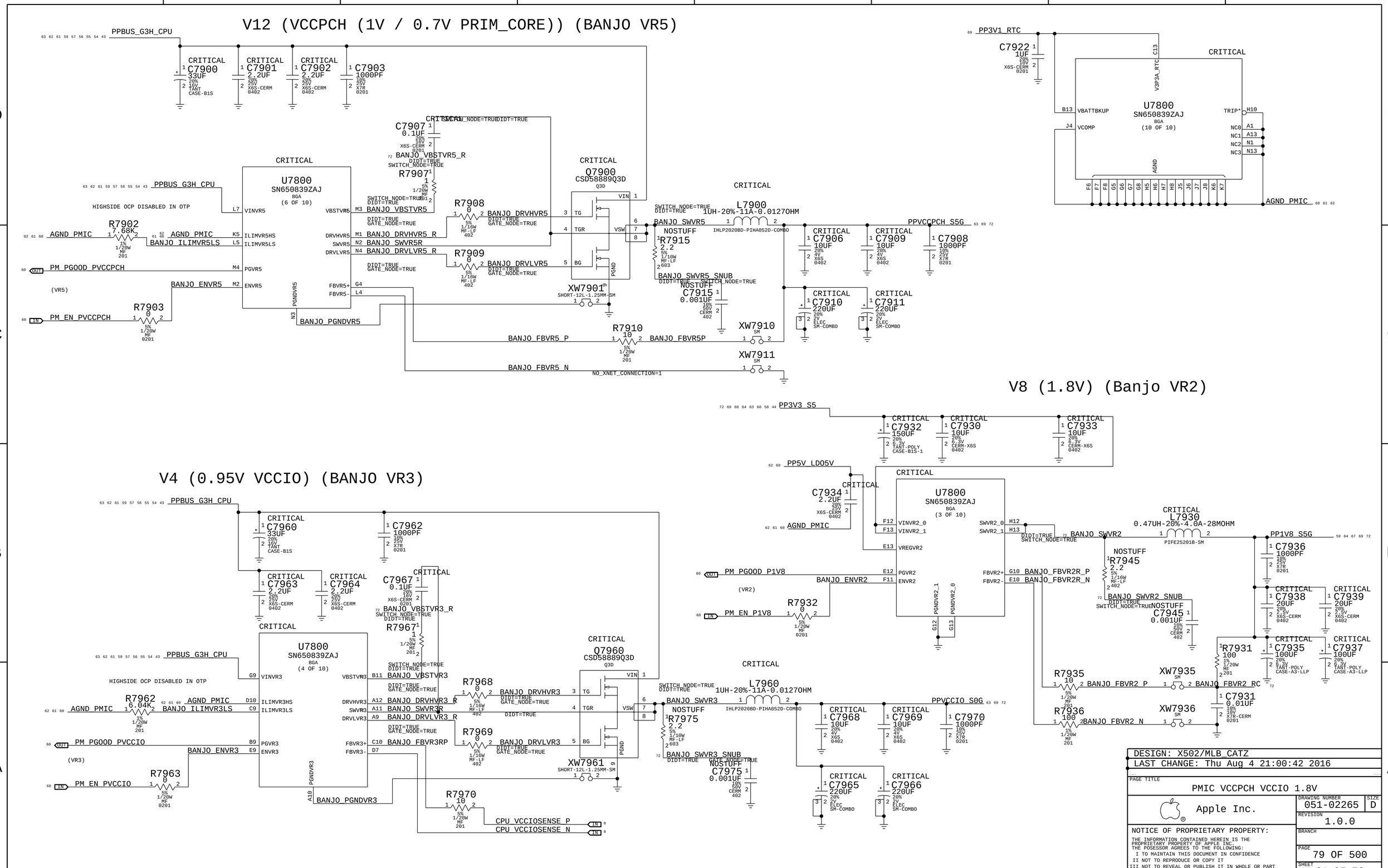

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PAGE TITLE
PMIC VCCPCH VCCIO 1.8V

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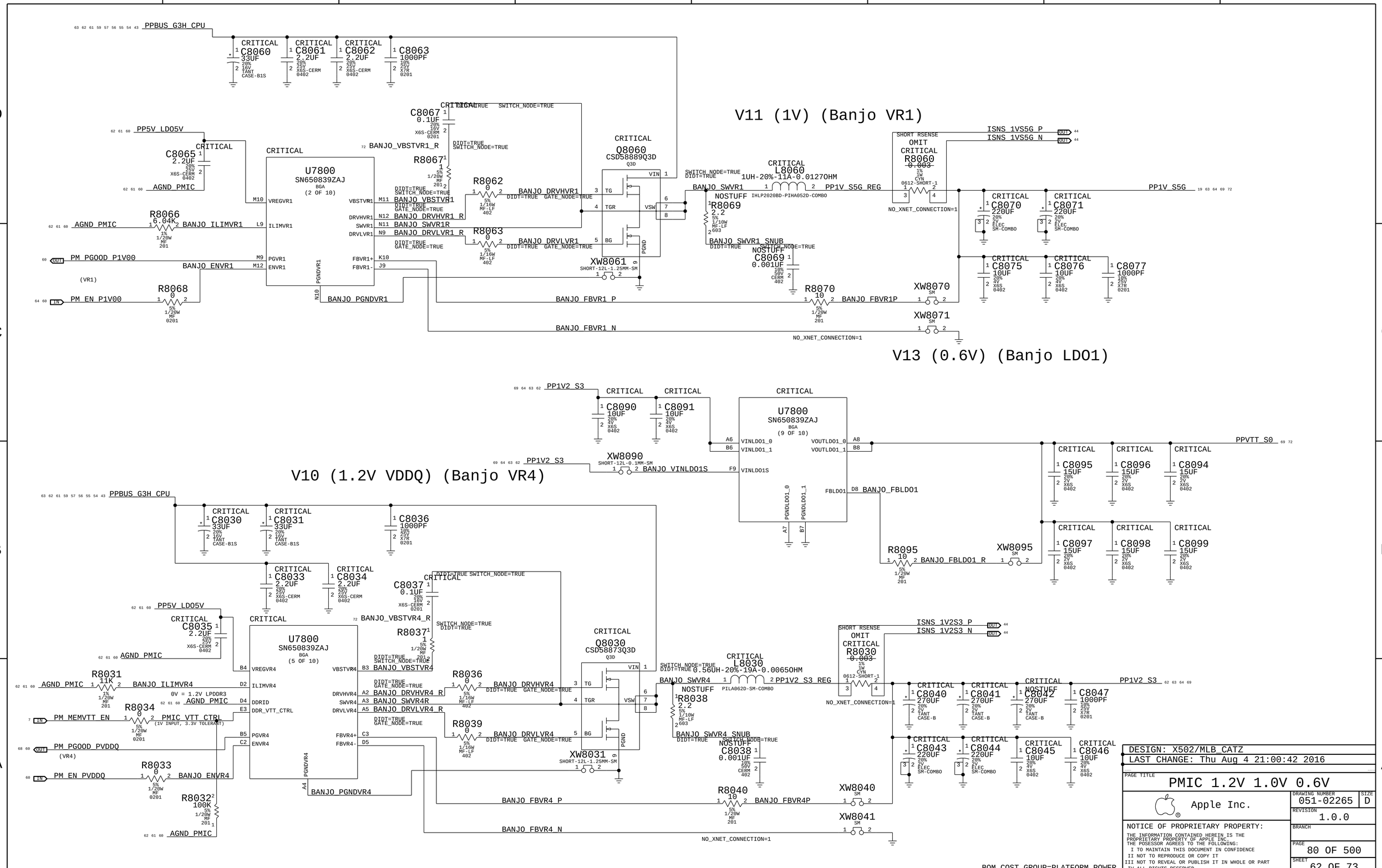

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PMIC 1.2V 1.0V 0.6V

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69 64 63 62	PP1V2_S3	C8100 12PF 5% 25V CERM 0201	CRITICAL C8101 3PF +/-0.1PF 25V C0G 0201
69 64 63 62	PP1V2_S3	C8102 3PF +/-0.1PF 25V C0G 0201	C8103 3PF +/-0.1PF 25V C0G 0201
69 64 63 62	PP1V2_S3	C8104 3PF +/-0.1PF 25V C0G 0201	C8105 3PF +/-0.1PF 25V C0G 0201
69 64 63 60	PP1V8_S3	C8106 3PF +/-0.1PF 25V C0G 0201	C8107 3PF +/-0.1PF 25V C0G 0201
72 69 67 64 63 45 44 43 41	PP3V3_S4	C8108 3PF +/-0.1PF 25V C0G 0201	C8109 3.5PF +/-0.25PF 25V C0G 0201
72 69 68 64 63 61 60 58 44	PP3V3_S5	C8110 12PF 5% 25V CERM 0201	C8111 3PF +/-0.1PF 25V C0G 0201
72 69 64 63 60 58 54	PP5V_S4	C8112 12PF 5% 25V CERM 0201	C8113 3.5PF +/-0.25PF 25V C0G 0201
72 69 64 63 60 58 54	PP5V_S4	C8114 3.5PF +/-0.25PF 25V C0G 0201	C8115 3.5PF +/-0.25PF 25V C0G 0201
72 69 64 63 60 58 54	PP5V_S4	C8116 12PF 5% 25V CERM 0201	C8117 3PF +/-0.1PF 25V C0G 0201
63 62 61 59 57 56 55 54 43	PPBUS_G3H_CPU	C8118 3PF +/-0.1PF 25V C0G 0201	C8119 3PF +/-0.1PF 25V C0G 0201
63 62 61 59 57 56 55 54 43	PPBUS_G3H_CPU	C8120 3PF +/-0.1PF 25V C0G 0201	C8121 3.5PF +/-0.25PF 25V C0G 0201
72 69 68 53	PPDCIN_G3H	C8122 12PF 5% 25V CERM 0201	C8123 3PF +/-0.1PF 25V C0G 0201
63 53	PPVBAT_G3H_CHGR_R	C8124 3PF +/-0.1PF 25V C0G 0201	C8125 3PF +/-0.1PF 25V C0G 0201
63 53	PPVBAT_G3H_CHGR_R	C8126 3PF +/-0.1PF 25V C0G 0201	C8127 3PF +/-0.1PF 25V C0G 0201
63 53 52	PPVBAT_G3H_CONN	C8128 12PF 5% 25V CERM 0201	C8129 3PF +/-0.1PF 25V C0G 0201
63 53 52	PPVBAT_G3H_CONN	C8130 3PF +/-0.1PF 25V C0G 0201	C8131 3PF +/-0.1PF 25V C0G 0201
72 69 55 45	PPVCCCPU_S0G	C8132 3PF +/-0.1PF 25V C0G 0201	C8133 3PF +/-0.1PF 25V C0G 0201
72 69 67 64 63 60 51 50 48	PP1V8_S0	C8134 12PF 5% 25V CERM 0201	FREQUENCY SPECIFIC CRITICAL C8135 3.0PF +/-0.1PF 25V NP0-C0G 0201
72 69 64 63 62 19	PP1V_S5G	C8137 3PF +/-0.1PF 25V C0G 0201	
72 69 64 63 62 19	PP1V_S5G	NOSTUFF C8138 3PF +/-0.1PF 25V C0G 0201	
72 69 67 64 63 45 44 43 41 72 69	PP3V3_S4	C8136 3PF +/-0.1PF 25V C0G 0201	PP3V3_S4 NOSTUFF C8139 3PF +/-0.1PF 25V C0G 0201
69 64 63 62	PP1V2_S3	NOSTUFF C8140 12PF 5% 25V CERM 0201	C8141 3PF +/-0.1PF 25V C0G 0201
69 64 63 62	PP1V2_S3	NOSTUFF C8142 12PF 5% 25V CERM 0201	C8143 3PF +/-0.1PF 25V C0G 0201
69 64 63 62	PP1V2_S3	NOSTUFF C8144 12PF 5% 25V CERM 0201	C8145 3PF +/-0.1PF 25V C0G 0201
69 64 63 62	PP1V2_S3	NOSTUFF C8146 12PF 5% 25V CERM 0201	C8147 3PF +/-0.1PF 25V C0G 0201
63 62 61 59 57 56 55 54 43	PPBUS_G3H_CPU	C8148 12PF 5% 25V CERM 0201	C8149 3PF +/-0.1PF 25V C0G 0201
69 64 63 60	PP1V8_S3	NOSTUFF C8150 12PF 5% 25V CERM 0201	C8151 3PF +/-0.1PF 25V C0G 0201
69 64 63 62	PP1V2_S3	C8152 3PF +/-0.1PF 25V C0G 0201	C8153 3PF +/-0.1PF 25V C0G 0201
69 64 63 60	PP1V8_S3	C8155 3PF +/-0.1PF 25V C0G 0201	
67	PPBUS_SSD_FLT	C8157 3.5PF +/-0.25PF 25V C0G 0201	
63 62 61 59 57 56 55 54 43	PPBUS_G3H_CPU	C8158 3PF +/-0.1PF 25V C0G 0201	C8159 3PF +/-0.1PF 25V C0G 0201
69 64 63	PP5V_S5	C8154 3PF +/-0.1PF 25V C0G 0201	
69 64 63	PP5V_S5	C8156 3PF +/-0.1PF 25V C0G 0201	
63 28 27	PP3V3_TBT_X_LC	C8160 12PF 5% 25V CERM 0201	C8161 3PF +/-0.1PF 25V C0G 0201
63 28 27	PP3V3_TBT_X_LC	C8162 12PF 5% 25V CERM 0201	C8163 3PF +/-0.1PF 25V C0G 0201
72 69 67 64 63 45 44 43 41	PP3V3_S4	C8164 3PF +/-0.1PF 25V C0G 0201	C8165 3PF +/-0.1PF 25V C0G 0201
72 69 67 64 63 45 44 43 41	PP3V3_S4	C8166 12PF 5% 25V CERM 0201	C8167 3PF +/-0.1PF 25V C0G 0201
28	PP3V3_TBT_X_S0	C8168 12PF 5% 25V CERM 0201	C8169 3PF +/-0.1PF 25V C0G 0201
72 69 61	PPVCCPCH_S5G	C8170 3PF +/-0.1PF 25V C0G 0201	C8171 3PF +/-0.1PF 25V C0G 0201
72 69 63 57 45	PPVCCGT_S0G	C8172 3PF +/-0.1PF 25V C0G 0201	C8173 3PF +/-0.1PF 25V C0G 0201
72 69 61	PPVCCIO_S0G	C8175 3PF +/-0.1PF 25V C0G 0201	
69 30 28	PP3V3_UPC_XB_LDO	C8176 12PF 5% 25V CERM 0201	C8177 3PF +/-0.1PF 25V C0G 0201
72 69 68 64 63 61 60 58 44	PP3V3_S5	C8178 12PF 5% 25V CERM 0201	C8179 3PF +/-0.1PF 25V C0G 0201
69	PP3V3_S5_SSD_SNS	C8174 3.5PF +/-0.25PF 25V C0G 0201	
72 69 63 57 45	PPVCCGT_S0G	C8181 3PF +/-0.1PF 25V C0G 0201	
72 69 67 64 63 45 44 43 41	PP3V3_S4	C8182 3PF +/-0.1PF 25V C0G 0201	C8183 3PF +/-0.1PF 25V C0G 0201
69 64 63 62	PP1V2_S3	C8185 3PF +/-0.1PF 25V C0G 0201	
72 69 68 60 58 53 50 43	PPBUS_G3H	C8187 3PF +/-0.1PF 25V C0G 0201	
27	PP0V9_TBT_X_SVR	C8188 12PF 5% 25V CERM 0201	C8189 3PF +/-0.1PF 25V C0G 0201
72 69 68 64 63 61 60 58 44	PP3V3_S5	C8180 3PF +/-0.1PF 25V C0G 0201	
63 62 61 59 57 56 55 54 43	PPBUS_G3H_CPU	C8191 3PF +/-0.1PF 25V C0G 0201	
72 69 64 63 60 58 54	PP5V_S4	C8192 12PF 5% 25V CERM 0201	C8193 3PF +/-0.1PF 25V C0G 0201
72 69 64 63 60 58 54	PP5V_S4	C8194 12PF 5% 25V CERM 0201	C8195 3PF +/-0.1PF 25V C0G 0201
72 69 64 63 60 58 54	PP5V_S4	C8197 3PF +/-0.1PF 25V C0G 0201	
69 64 63	PP5V_S5	C8199 3PF +/-0.1PF 25V C0G 0201	
72 69 64 63 60 58 54	PP5V_S4	C8196 12PF 5% 25V CERM 0201	C8198 12PF +/-0.1PF 25V C0G 0201
72 69 67 64 63 60 51 50 48	PP1V8_S0	CRITICAL C81A0 2.9PF +/-0.05PF 25V C0G-CERM 0201	CRITICAL C81A1 2.9PF +/-0.05PF 25V C0G-CERM 0201
72 69 67 64 63 60 51 50 48	PP1V8_S0	C81A3 2.9PF +/-0.05PF 25V C0G-CERM 0201	
72 69 67 64 63 45 44 43 41	PP3V3_S4	C81A5 3.5PF +/-0.25PF 25V C0G 0201	
72 69 44	PP3V3_S4_WLS	C81A7 3PF +/-0.1PF 25V C0G 0201	
69 64 60 59 54 49 46 45 42 38	PP3V3_S0	NOSTUFF C81A8 3PF +/-0.1PF 25V C0G 0201	NOSTUFF C81A9 3PF +/-0.1PF 25V C0G 0201

BOM_COST_GROUP=PLATFORM POWER

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
RAIL DESENSE CAPS

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
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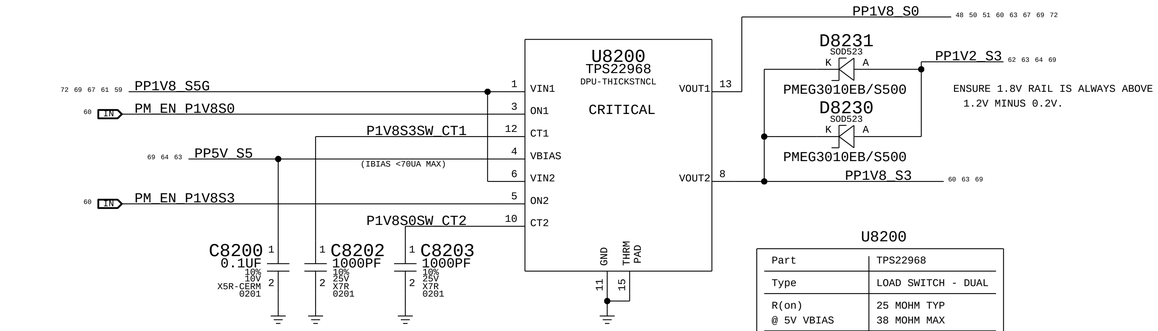
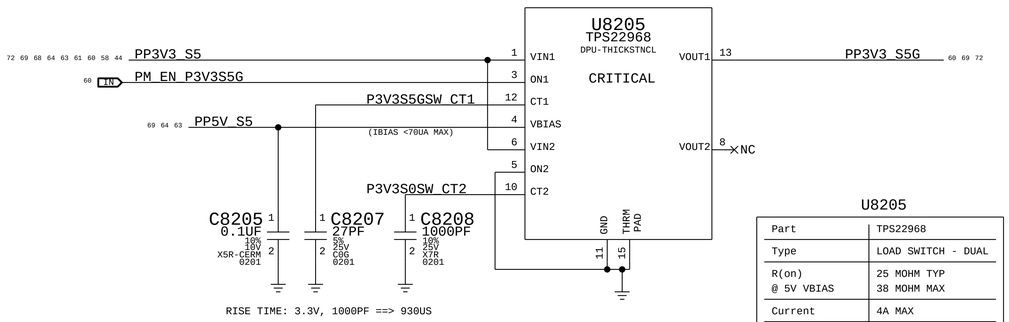


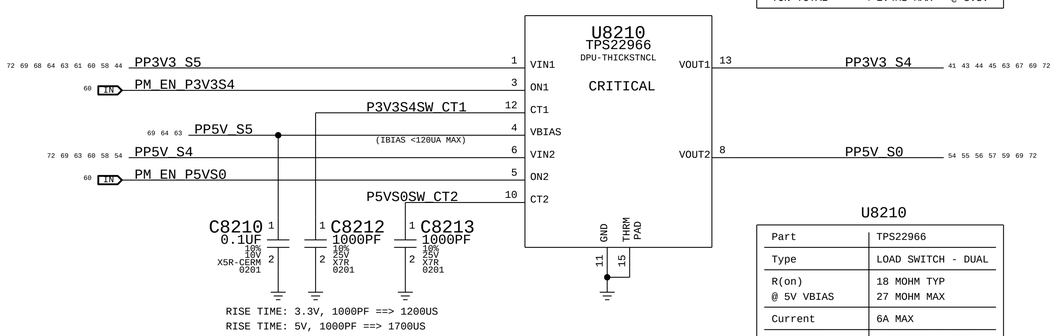
U8200

Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1MS MAX @ 1.8V



U8205

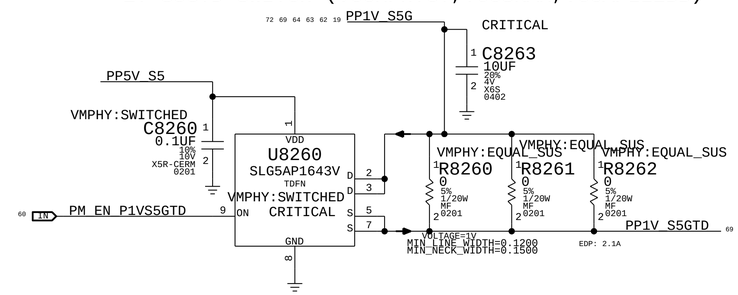
Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1.4MS MAX @ 3.3V



U8210

Part	TPS22966
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	18 MOHM TYP 27 MOHM MAX
Current	6A MAX
TON-TOTAL	1.7MS MAX @ 3,3V 2.4MS MAX @ 5V

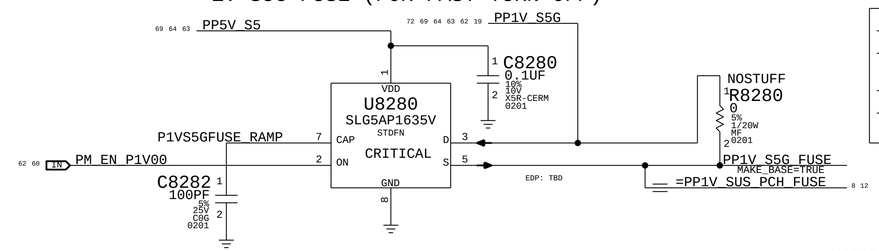
1V S5GTD SWITCH (VCCMPHYGT,VCCSRAM,VCCAPLLEBB)



U8260

Part	SLG5AP1643V
Type	Load Switch
R(on) @ 25C R(on) @ 70C	7.4 MOHM TYP 10.6 MOHM MAX
Current	6A MAX
TON-TOTAL	65US MAX @ 1V

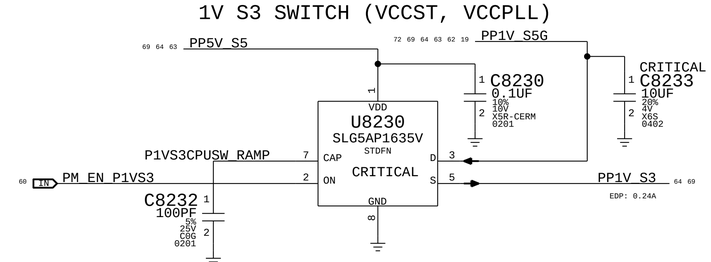
1V S5G FUSE (FOR FAST TURN OFF)



U8230

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

1V S3 SWITCH (VCCST, VCCPLL)

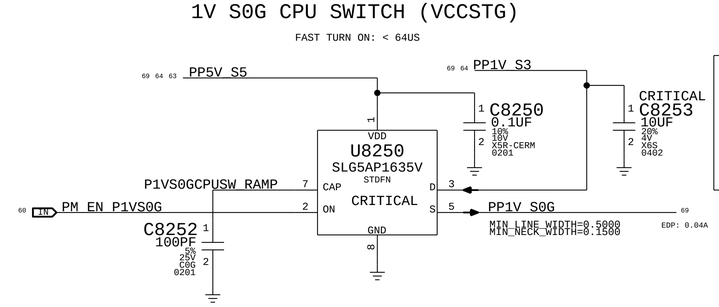


U8230

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

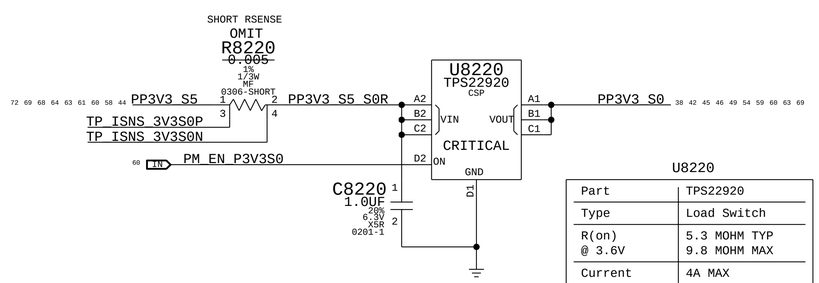
1V S0G CPU SWITCH (VCCSTG)

FAST TURN ON: < 64US



U8250

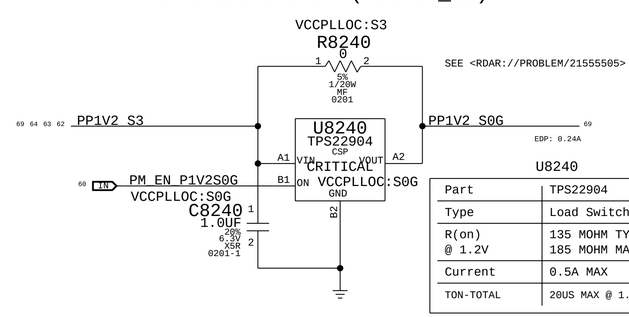
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V



U8220

Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.3 MOHM TYP 9.8 MOHM MAX
Current	4A MAX
TON-TOTAL	1.3MS MAX @ 3.6V

1V2 S0G SWITCH (VCCPLL_OC)



U8240

Part	TPS22904
Type	Load Switch
R(on) @ 1.2V	135 MOHM TYP 185 MOHM MAX
Current	0.5A MAX
TON-TOTAL	20US MAX @ 1.2V

BOM_COST_GROUP=PLATFORM POWER

DESIGN: X502/MLB_CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-02265 SIZE: D
REVISION: 1.0.0
BRANCH:
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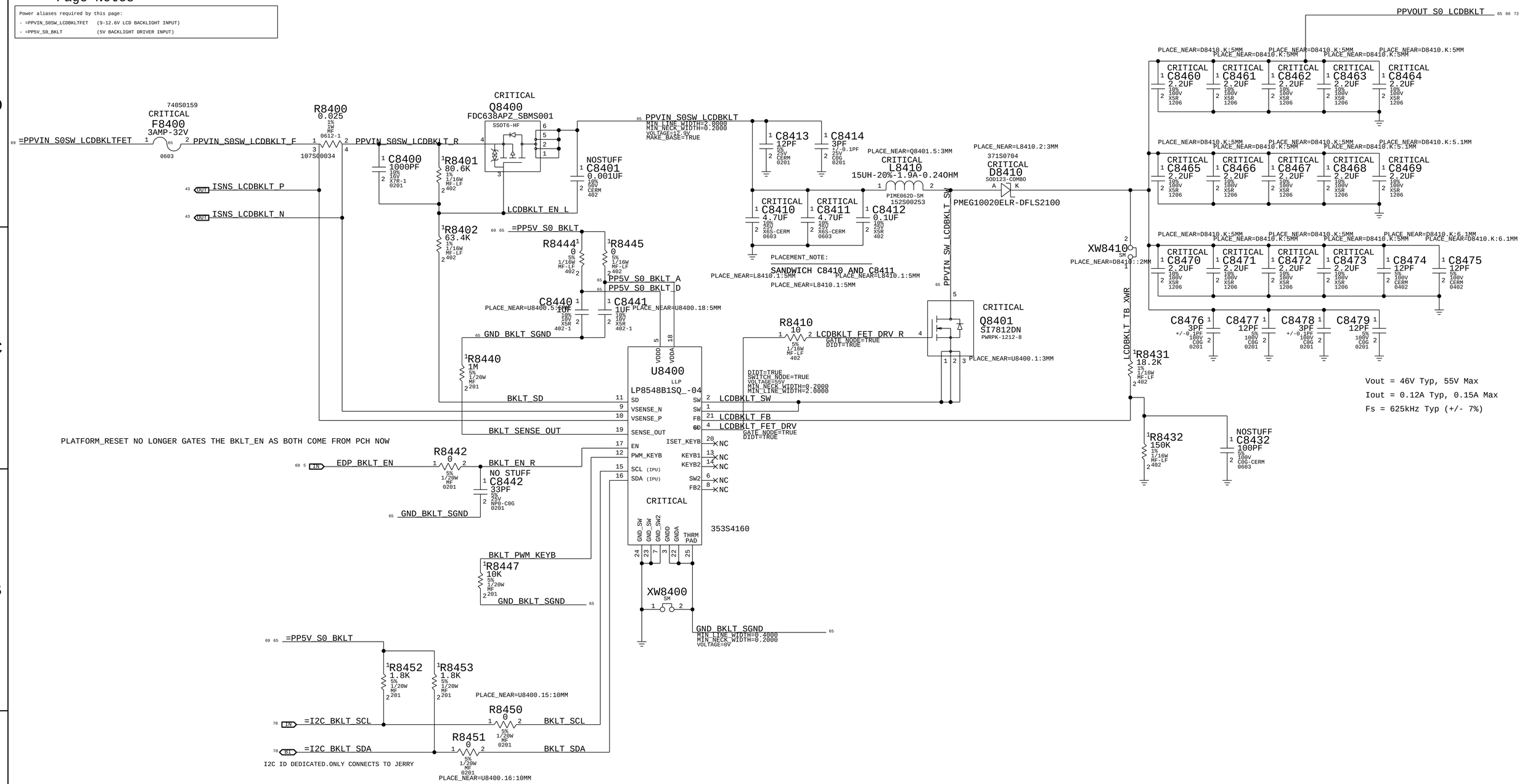
Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)



LINE WIDTHS

PP5V_S0_BKLT_A MIN_LINE_WIDTH=2.0000 MIN_NECK_WIDTH=0.2000 VOLTAGE=5V

PP5V_S0_BKLT_D MIN_LINE_WIDTH=2.0000 MIN_NECK_WIDTH=0.2000 VOLTAGE=5V

PBUS LINE WIDTHS

PPVIN_S0SW_LCDBKLT_F MIN_LINE_WIDTH=2.0000 MIN_NECK_WIDTH=0.2000 VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT_R MIN_LINE_WIDTH=2.0000 MIN_NECK_WIDTH=0.2000 VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT MIN_LINE_WIDTH=2.0000 MIN_NECK_WIDTH=0.2000 VOLTAGE=12.9V

LCD BKLT LINE WIDTHS

LCDBKLT_FET_DRV MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.2000 VOLTAGE=5V GATE_NODE=TRUE DIDT=TRUE

PPVIN_SW_LCDBKLT_SW MIN_LINE_WIDTH=2.0000 MIN_NECK_WIDTH=0.2000 VOLTAGE=55V SWITCH_NODE=TRUE DIDT=TRUE

PPVOUT_S0_LCDBKLT MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.2000 VOLTAGE=55V

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=X262 SYNC_DATE=06/25/2010

PAGE TITLE
LCD Backlight Driver

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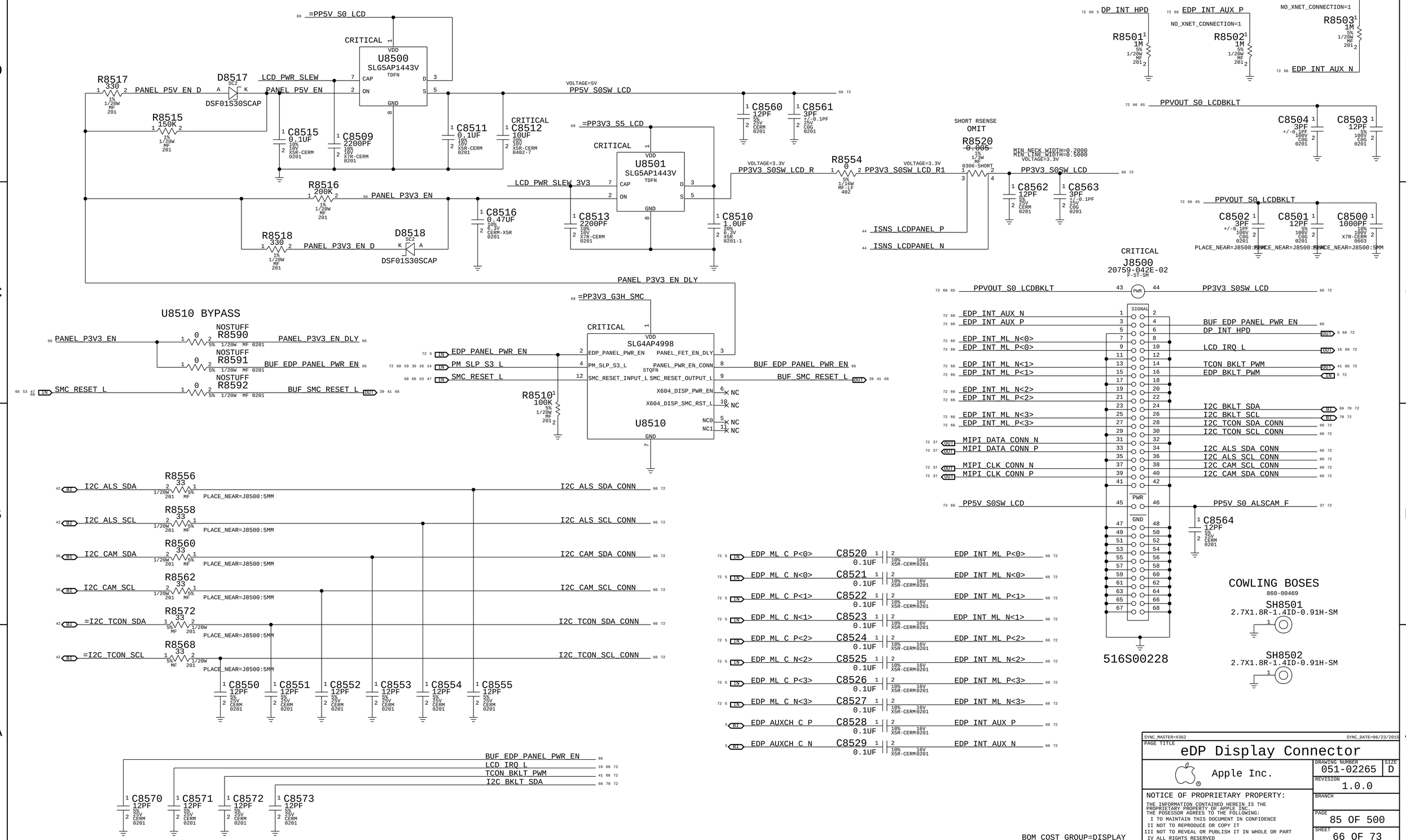
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



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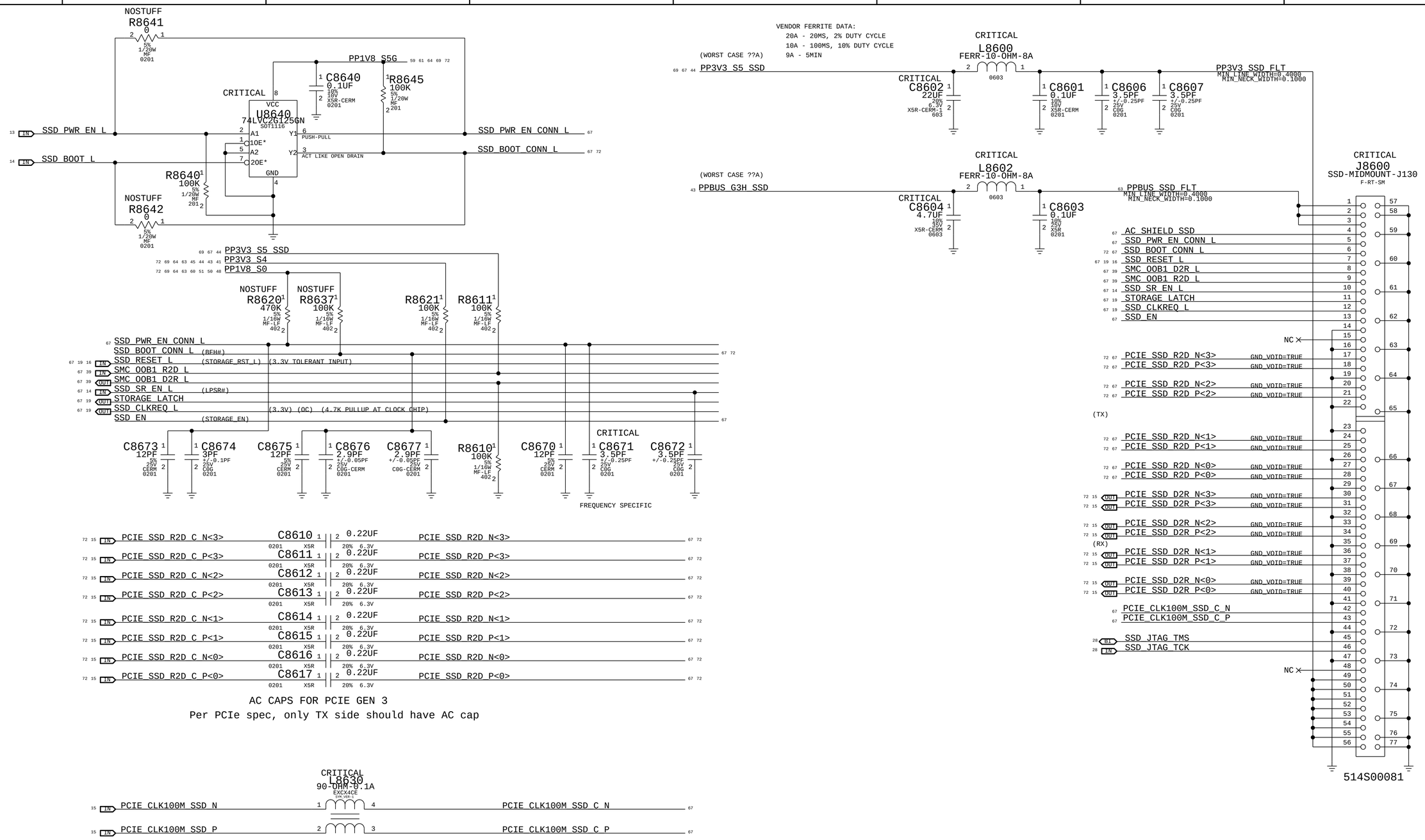
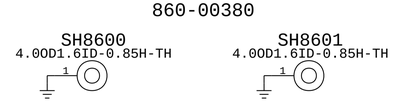


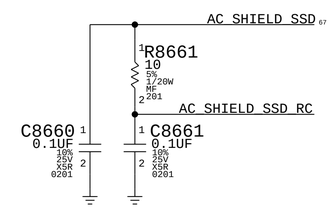
NOTES:

1. POWER-ON TO PERST_L DE-ASSERTION = 10MS MINIMUM
2. PP3V3_EN: PROVIDE 10MS EARLY WARNING TO SSD THAT POWER WILL BE OFF. (PIN 47, PP3V3_EN, IS NOT USED BY SAMSUNG UAX AND SANDISK SSD.)
3. PCIE CLK100M ARE 2.5V SIGNALS.
4. OOB SIGNALS: UART 3.3V, 115.2 KBAUD, 8B, NO PARITY, 1 STOP BIT.

SSD STANDOFFS

860-00380





BOM_COST_GROUP=SSD

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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SSD MODULE

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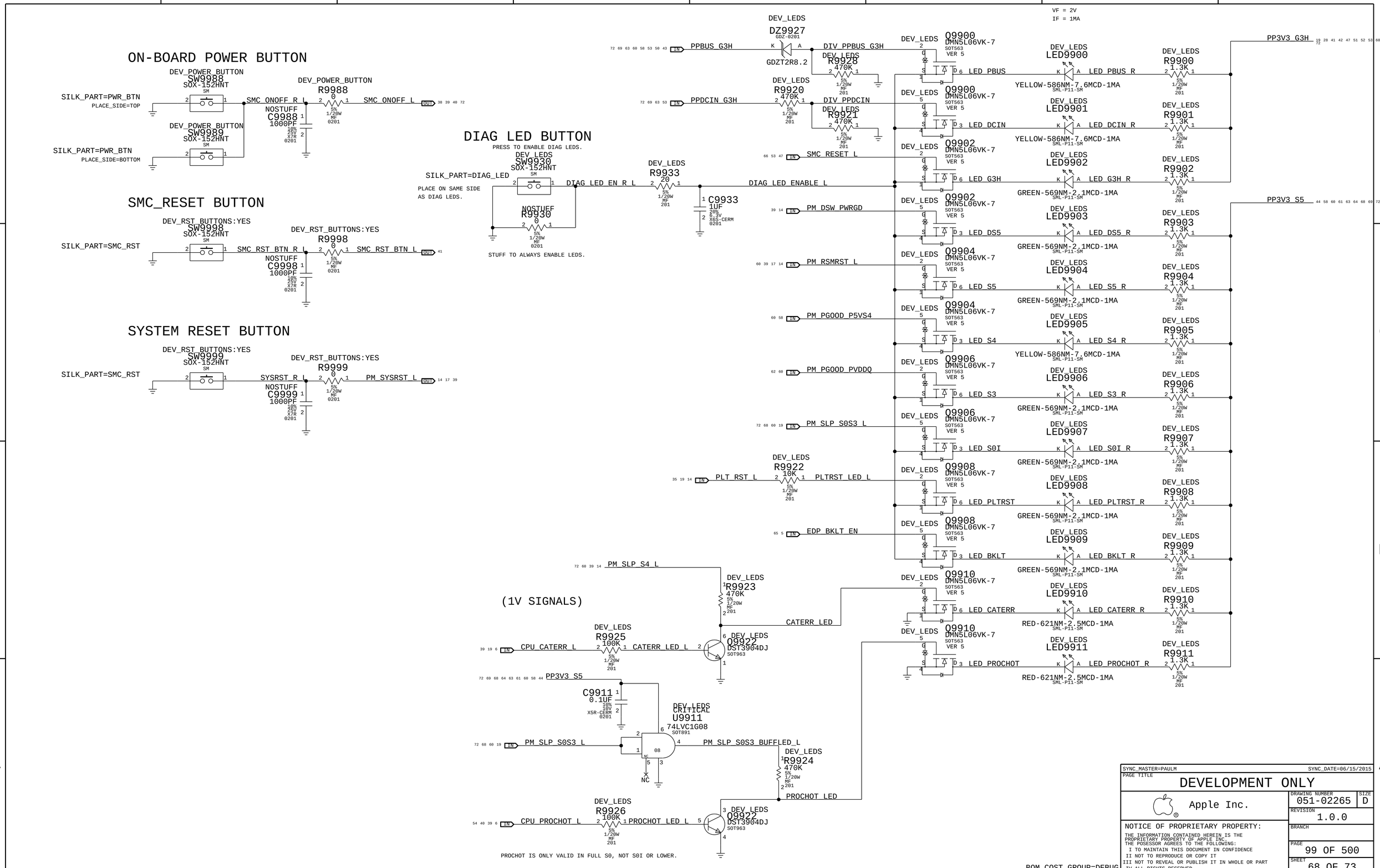

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52 32 31 =PPBUS_G3H	MAKE_BASE=TRUE	PPBUS_G3H	43 50 53 58 60 63 68 69 72
43 =PPDCIN_G3H_SNS	MAKE_BASE=TRUE	PPDCIN_G3H	53 63 68 69 72
58 =PP5V_S5_LDO	MAKE_BASE=TRUE	PP5V_S5	63 64
66 =PP3V3_G3H_SMC	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
40 39 =PP3V3_S5_SMC	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
40 =PP3V3_S4_SMC	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
40 =PP3V3_S0_SMC	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
40 =PPVIN_S5_SMCVREF	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
24 23 22 21 =PP1V8_S3_MEM	MAKE_BASE=TRUE	PP1V8_S3	60 63 64
24 23 22 21 =PP1V2_S3_MEM_VDD2	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
24 23 22 21 =PP1V2_S3_MEM_VDDCA	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
24 23 22 21 =PP1V2_S3_MEM_VDDQ	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
20 =PPDDR_S3_MEMVREF	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
25 =PP0V6_S0_MEM_VTT_A	MAKE_BASE=TRUE	PPVTT_S0	62 69 72
25 =PP0V6_S0_MEM_VTT_B	MAKE_BASE=TRUE	PPVTT_S0	62 69 72
20 PPVREF_S3_MEM_VREFDQ_A	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFDQ_A	21 22
69 20 PPVREF_S3_MEM_VREFCA	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFCA_A	21 22
20 PPVREF_S3_MEM_VREFDQ_B	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFDQ_B	23 24
69 20 PPVREF_S3_MEM_VREFCA	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFCA_B	23 24

CPU RAILS

10 8 =PPVCC_S0_CPU		PPVCCCPU_S0G	45 55 63 72
10 8 =PPVCCSA_S0_CPU	MAKE_BASE=TRUE	PPVCCSA_S0G	56 72
11 8 =PPVCCGT_S0_CPU	MAKE_BASE=TRUE	PPVCCGT_S0G	45 57 63 69 72
11 8 =PPVCCGTX_S0_CPU	MAKE_BASE=TRUE	PPVCCGT_S0G	45 57 63 69 72
69 10 8 =PP1V2_S3_CPU_VDDQ	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
10 8 =PP1V2_S3_CPU_VDDQC		=PP1V2_S3_CPU_VDDQ	8 10 69
10 8 5 =PP0V95_S0_CPU_VCCIO	MAKE_BASE=TRUE	PPVCCIO_S0G	61 63 72
59 54 19 14 10 8 6 =PP1V_S3_CPU_VCCST	MAKE_BASE=TRUE	PP1V_S3	64 69
40 =PP1V_S0_SMC_VCCST			
17 10 8 6 =PP1V_S0SW_CPU_VCCSTG	MAKE_BASE=TRUE	PP1V_S0G	64
10 8 =PP1V_S3_CPU_VCCPLL	MAKE_BASE=TRUE	PP1V_S3	64 69
10 8 =PP1V2_S0SW_CPU_VCCPLLOC	MAKE_BASE=TRUE	PP1V2_S0G	64

PCH RAILS

15 14 12 8 =PP3V_G3H_PCH_VCCRTC	MAKE_BASE=TRUE	PP3V1_RTC	61
14 8 =PP3V3_S5_PCH_VCCDSW	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
16 15 14 13 8 =PP3V3_SUS_PCH_VCCPGPPA	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
19 12 8 =PP3V3_SUS_PCH_VCCPGPPB	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
12 8 =PP3V3_SUS_PCH_VCCPGPPC	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
8 =PP3V3_SUS_PCH_VCCPGPPD	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
12 8 =PP3V3_SUS_PCH_VCCPGPPE	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
8 =PP3V3_SUS_PCH_VCCPGPPG	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
12 8 5 =PP3V3_SUS_PCH_VCCPRIM	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
47 13 8 =PP3V3_SUS_PCH_VCCSPI	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
12 8 =PP3V3_SUS_PCH_VCCRTCPRIM	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
69 12 8 =PP1V_SUS_PCH_VCCPRIM	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
12 8 =PP1V_SUS_PCH_VCCMPHYAON	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
8 =PP1V_SUS_PCH_VCCCLK1	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
12 =PP1V_SUS_PCH_VCCCLK2_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
8 =PP1V_SUS_PCH_VCCCLK3	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
12 =PP1V_SUS_PCH_VCCCLK4_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
12 =PP1V_SUS_PCH_VCCCLK5_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
12 8 =PP1V_SUS_PCH_VCCCLK6	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
15 12 =PP1V_SUS_PCH_VCCAPLL	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
14 8 =PP1V8_SUS_PCH_VCCPGPPF	MAKE_BASE=TRUE	PP1V8_S5G	49 61 64 67 69 72
12 8 =PP1V8_SUS_PCH_VCCATS	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
12 =PP1V8_SUS_PCH_VCC1P8_SRC	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
12 8 =PPVCCPRIMECORE_SUS_PCH	MAKE_BASE=TRUE	PPVCCPCH_S5G	61 63 72
12 =PP1V_SUSSW_PCH_VCCAMPHYPLL_SRC	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
12 8 =PP1V_SUSSW_PCH_VCCMPHYGT	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
12 8 =PP1V_SUSSW_PCH_VCCSRAM	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
12 8 =PP1V_SUSSW_PCH_VCCAPLLEBB	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
12 =PP1V8_S0_PCH_VCCHDA	MAKE_BASE=TRUE	PP1V8_S0	48 50 51 60 63 64 67 72
18 =PP1V8R1V5_S0_PCH_VCCHDA			
60 19 16 14 13 5 =PP3V3_S0_PCH	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
14 =PP3V3_S4_PCH	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
40 =PP3V3R1V8_S0_PCH_VCCPGPPB	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69

SSD RAILS

67 44 PP3V3_S5_SSD	MAKE_BASE=TRUE	PP3V3_S5_SSD_SNS	63
45 =PP3V3_S0_TBT_X_SNS		=PP3V3_TBT_X_S0	27 28

8 CPU_VCCGTXSENSE_P		PU_VSNS_CPU_VCCGTX_TP	
8 CPU_VCCGTXSENSE_N	MAKE_BASE=TRUE	PD_VSNS_CPU_VCCGTX_TN	
	MAKE_BASE=TRUE		
36 =PP3V3_S0_CAMERA		PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
37 =PP5V_S0_ALSCAM	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
	MAKE_BASE=TRUE		
66 =PP3V3_S0_LCD		PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
66 =PP3V3_S5_LCD	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
66 =PP5V_S0_LCD	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
	MAKE_BASE=TRUE		
35 =PP3V3_S0_BT_UART		PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
35 =PP3V3_S4_BT_UART	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
	MAKE_BASE=TRUE		
38 =PP3V3_G3H_KBD		PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
38 =PP3V3_S4_KBD	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
38 =PP5V_S0_KBD	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
	MAKE_BASE=TRUE		
34 19 =PP3V3_S4_WLAN		PP3V3_S4_WLS	44 63 72
18 =PP3V3_S5_WIRELESS	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
	MAKE_BASE=TRUE		
38 =PP3V3_S0_TPAD		PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
38 =PP3V3_S4_TPAD	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
38 =PP5V_S4_TPAD	MAKE_BASE=TRUE	PP5V_S4	54 58 60 63 64 69 72
38 =PPBUS_S4_TPAD	MAKE_BASE=TRUE	PPBUS_G3H_TPAD	43
17 =PP1V_SUS_XDP		=PP1V_SUS_PCH_VCCPRIM	8 12 69
60 17 =PP3V3_SUS_XDP	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
65 =PP5V_S0_BKLT		PP5V_S0	54 55 56 57 59 64 69 72
65 =PPVIN_S0SW_LCDBKLTFET	MAKE_BASE=TRUE	PPBUS_G3H	43 50 53 58 60 63 68 69 72
	MAKE_BASE=TRUE		
38 =PP5V_S0_FAN		PP5V_S0	54 55 56 57 59 64 69 72
	MAKE_BASE=TRUE		

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.0859
MIN_LINE_WIDTH=0.3000

USB-C GLOBAL POWER ALIASES

29 =PP3V3_UPC_XA_AUX		PP3V3_UPC_XA_LDO	28 29
30 =PP3V3_UPC_XB_AUX	MAKE_BASE=TRUE	PP3V3_UPC_XB_LDO	28 30 63
	MAKE_BASE=TRUE		
33 =PP3V3_S5_TBT_X		PP3V3_S5	44 58 60 61 63 64 68 69 72
29 =PP5V_XA_USBC	MAKE_BASE=TRUE	PP5V_S4	54 58 60 63 64 69 72
30 =PP5V_XB_USBC			
28 =PP5V_USBC			
30 29 =PPHV_EXT_G3H		PPDCIN_G3H	53 63 68 69 72
	MAKE_BASE=TRUE		

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB_CATZ
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Power Aliases

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UNUSED GPIOS, HSIO

8	IN	VCCPRIM_CORE_VID0	MAKE_BASE=TRUE	NO_TEST=1	NC_VCCPRIM_CORE_VID0
8	IN	VCCPRIM_CORE_VID1	MAKE_BASE=TRUE	NO_TEST=1	NC_VCCPRIM_CORE_VID1
16	IN	MLB_DEV_L	MAKE_BASE=TRUE	NO_TEST=1	NC_MLB_DEV_L
16	IN	I2C_UPC_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_UPC_SDA
16	IN	I2C_UPC_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_UPC_SCL
13	IN	PCH_BSSB_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_BSSB_CLK
13	IN	PCH_BSSB_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_BSSB_DATA
16	IN	TBT_X_DPMUX_SEL	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_X_DPMUX_SEL
16	IN	TBT_T_CIO_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_CIO_PWR_EN
16	IN	TBT_T_USB_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_USB_PWR_EN
16	IN	TBT_T_PCI_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_PCI_RESET_L
16	IN	TBT_T_DPMUX_SEL	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_DPMUX_SEL
15	OUT	=TBT_T_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_CLKREQ_L
15	IN	PCIE_CLK100M_TBT_T_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_TBT_TN
15	IN	PCIE_CLK100M_TBT_T_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_TBT_TP
15	OUT	PCIE_TBT_T_D2R_N<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RN0
15	OUT	PCIE_TBT_T_D2R_P<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RP0
15	IN	PCIE_TBT_T_R2D_C_N<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CN0
15	IN	PCIE_TBT_T_R2D_C_P<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CP0
15	OUT	PCIE_TBT_T_D2R_N<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RN1
15	OUT	PCIE_TBT_T_D2R_P<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RP1
15	IN	PCIE_TBT_T_R2D_C_N<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CN1
15	IN	PCIE_TBT_T_R2D_C_P<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CP1
15	B1	USB_CAMERA_DFR_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_03N
15	B1	USB_CAMERA_DFR_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_03P
13	IN	DEBUGUART_SEL_SOC	MAKE_BASE=TRUE	NO_TEST=1	NC_DEBUGUART_SEL_SOC
15	B1	USB3_EXTB_D2R_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_D2RN
15	B1	USB3_EXTB_D2R_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_D2RP
15	B1	USB3_EXTB_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_R2DCN
15	B1	USB3_EXTB_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_R2DCP
26	B1	=DP_X_SRC_ML_P<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_ML_CP<3..0>
26	B1	=DP_X_SRC_ML_N<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_ML_CN<3..0>
26	B1	=DP_X_SRC_AUX_P	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_AUXCHP
26	B1	=DP_X_SRC_AUX_N	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_AUXCHN
15	B1	USB_EXTA_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_01N
15	B1	USB_EXTA_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_01P
15	B1	NC_USB2_05N	NO_TEST=1
15	B1	NC_USB2_05P	NO_TEST=1
15	B1	NC_USB2_06N	NO_TEST=1
15	B1	NC_USB2_06P	NO_TEST=1
15	B1	NC_USB2_07N	NO_TEST=1
15	B1	NC_USB2_07P	NO_TEST=1
15	B1	NC_USB2_09N	NO_TEST=1
15	B1	NC_USB2_09P	NO_TEST=1
15	B1	NC_USB2_10N	NO_TEST=1
15	B1	NC_USB2_10P	NO_TEST=1
30	B1	NC_UPC_XB_I2C_ADDR	NO_TEST=1

GND
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.0850
VOLTAGE=0V

Digital Ground

65	B1	=I2C_BKLT_SCL	MAKE_BASE=TRUE	I2C_BKLT_SCL	B1 66 72
65	B1	=I2C_BKLT_SDA	MAKE_BASE=TRUE	I2C_BKLT_SDA	B1 66 72

16	IN	TP_BT_I2S_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_CLK
16	IN	TP_BT_I2S_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_D2R
16	IN	TP_BT_I2S_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_R2D
16	IN	TP_BT_I2S_SYNC	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_SYNC
36	IN	TP_CAM_GPIO3	MAKE_BASE=TRUE	NO_TEST=1	NC_CAM_GPIO3
6	IN	TP_CPU_AT5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AT5
6	IN	TP_CPU_AU5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AU5
6	IN	TP_CPU_AY4	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AY4
6	IN	TP_CPU_BB3	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_BB3
6	IN	TP_CPU_BB5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_BB5
59	IN	TP_CPU_MSM_L	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_MSM_L
9	IN	TP_CPU_NCTFVSS_A5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_A5
9	IN	TP_CPU_NCTFVSS_A70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_A70
9	IN	TP_CPU_NCTFVSS_AV1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_AV1
9	IN	TP_CPU_NCTFVSS_B71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_B71
9	IN	TP_CPU_NCTFVSS_BA1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BA1
9	IN	TP_CPU_NCTFVSS_BA71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BA71
9	IN	TP_CPU_NCTFVSS_BB70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BB70
9	IN	TP_CPU_NCTFVSS_C1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_C1
13	IN	TP_PCH_CLKOUT_LPC1	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLKOUT_LPC1
14	IN	TP_PCH_GPD7	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPD7
14	IN	TP_PCH_GPP_D0	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D0
16	IN	TP_PCH_GPP_D1	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D1
16	IN	TP_PCH_GPP_D3	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D3
16	IN	TP_PCH_GPP_D4	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D4
5	IN	TP_PCH_GPP_E15	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_E15
14	IN	TP_PCH_GPP_F8	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F8
14	IN	TP_PCH_GPP_F9	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F9
14	IN	TP_PCH_GPP_F10	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F10
14	IN	PCH_BT_ROM_BOOT	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F11
13	IN	PCH_SOC_DFU_STATUS	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F18
13	IN	SOC_PANIC_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F19
13	IN	SOC_S2R_ACK_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F20
13	IN	SOC_SLEEP_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F21
14	IN	TP_PCH_LANPHYPC	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_LANPHYPC
14	IN	TP_PCH_PME_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_PME_L
14	IN	TP_PCH_SLP_WLAN_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SLP_WLAN_L
13	IN	TP_PCH_STRP_ESPI	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_STRP_ESPI
13	IN	TP_PCH_STRP_TLSCONF	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_STRP_TLSCONF
60	IN	TP_PMIC_PGC	MAKE_BASE=TRUE	NO_TEST=1	NC_PMIC_PGC
13	IN	TP_SPI_CS1_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_CS1_L
13	IN	TP_SPI_CS2_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_CS2_L
19	IN	TP_SYSCLK_CLK24M_SSD	MAKE_BASE=TRUE	NO_TEST=1	NC_SYSCLK_CLK24M_SSD
15	IN	TP_USB3_03_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_D2RN
15	IN	TP_USB3_03_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_D2RP
15	IN	TP_USB3_03_R2DN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_R2DN
15	IN	TP_USB3_03_R2DP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_R2DP
15	IN	TP_USB3_04_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_D2RN
15	IN	TP_USB3_04_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_D2RP
15	IN	TP_USB3_04_R2DN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_R2DN
15	IN	TP_USB3_04_R2DP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_R2DP
14	IN	PCH_SOC_FORCE_DFU	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SOC_FORCE_DFU
13	OUT	PCH_SOC_WDOG	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SOC_WDOG
14	OUT	UPC_I2C_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_I2C_INT_L
30	IN	TP_UPC_XB_SWD_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XB_SWD_DATA
29	IN	TP_UPC_XA_SWD_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XA_SWD_DATA
29	IN	TP_UPC_XA_SWD_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XA_SWD_CLK
15	IN	TP_PCIE_CLK100M5P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M5P
15	IN	TP_PCIE_CLK100M5N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M5N
15	IN	TP_PCH_CLKREQ5_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLKREQ5_L
15	IN	TP_ITPXDP_CLK100MP	MAKE_BASE=TRUE	NO_TEST=1	NC_ITPXDP_CLK100MP
15	IN	TP_ITPXDP_CLK100MN	MAKE_BASE=TRUE	NO_TEST=1	NC_ITPXDP_CLK100MN
55	IN	TP_CPUVR_GH1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPUVR_GH1
6	IN	TP_CPU_RSVD_BB69	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BB69
6	IN	TP_CPU_RSVD_BB68	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BB68
6	IN	TP_CPU_RSVD_BA70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BA70
6	IN	TP_CPU_RSVD_BA68	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BA68
6	IN	TP_CPU_RSVD_AW71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AW71
6	IN	TP_CPU_RSVD_AW70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AW70
6	IN	TP_CPU_RSVD_AK12	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AK12
19	IN	TP_SPKR_ID0	MAKE_BASE=TRUE	NO_TEST=1	NC_SPKR_ID0
60	IN	TP_PGOOD_PVCCIO	MAKE_BASE=TRUE	NO_TEST=1	NC_PGOOD_PVCCIO
60	IN	TP_PGOOD_P1V00	MAKE_BASE=TRUE	NO_TEST=1	NC_PGOOD_P1V00
19	IN	TP_PCH_CLK32K_RTCX2	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLK32K_RTCX2
19	IN	TP_PCH_CLK24M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLK24M_XTALOUT
19	IN	TP_XDP_BPM_L<3>	MAKE_BASE=TRUE	NO_TEST=1	NC_XDP_BPM_L<3>
19	IN	TP_XDP_BPM_L<2>	MAKE_BASE=TRUE	NO_TEST=1	NC_XDP_BPM_L<2>
19	IN	TP_XDP_BPM_L<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_XDP_BPM_L<1>

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB_CATZ
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NC_ AND NO_TEST SIGNALS

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Memory Bit/Byte Swizzle

CPU	MAKE_BASE	DRAM
MEM_A_DQ<0>	TRUE	=MEM_A_DQ<16>
MEM_A_DQ<1>	TRUE	=MEM_A_DQ<17>
MEM_A_DQ<2>	TRUE	=MEM_A_DQ<23>
MEM_A_DQ<3>	TRUE	=MEM_A_DQ<19>
MEM_A_DQ<4>	TRUE	=MEM_A_DQ<20>
MEM_A_DQ<5>	TRUE	=MEM_A_DQ<21>
MEM_A_DQ<6>	TRUE	=MEM_A_DQ<22>
MEM_A_DQ<7>	TRUE	=MEM_A_DQ<18>
MEM_A_DQ<8>	TRUE	=MEM_A_DQ<2>
MEM_A_DQ<9>	TRUE	=MEM_A_DQ<7>
MEM_A_DQ<10>	TRUE	=MEM_A_DQ<6>
MEM_A_DQ<11>	TRUE	=MEM_A_DQ<4>
MEM_A_DQ<12>	TRUE	=MEM_A_DQ<0>
MEM_A_DQ<13>	TRUE	=MEM_A_DQ<3>
MEM_A_DQ<14>	TRUE	=MEM_A_DQ<1>
MEM_A_DQ<15>	TRUE	=MEM_A_DQ<5>
MEM_A_DQ<16>	TRUE	=MEM_A_DQ<46>
MEM_A_DQ<17>	TRUE	=MEM_A_DQ<47>
MEM_A_DQ<18>	TRUE	=MEM_A_DQ<42>
MEM_A_DQ<19>	TRUE	=MEM_A_DQ<43>
MEM_A_DQ<20>	TRUE	=MEM_A_DQ<44>
MEM_A_DQ<21>	TRUE	=MEM_A_DQ<45>
MEM_A_DQ<22>	TRUE	=MEM_A_DQ<40>
MEM_A_DQ<23>	TRUE	=MEM_A_DQ<41>
MEM_A_DQ<24>	TRUE	=MEM_A_DQ<63>
MEM_A_DQ<25>	TRUE	=MEM_A_DQ<59>
MEM_A_DQ<26>	TRUE	=MEM_A_DQ<61>
MEM_A_DQ<27>	TRUE	=MEM_A_DQ<56>
MEM_A_DQ<28>	TRUE	=MEM_A_DQ<62>
MEM_A_DQ<29>	TRUE	=MEM_A_DQ<58>
MEM_A_DQ<30>	TRUE	=MEM_A_DQ<60>
MEM_A_DQ<31>	TRUE	=MEM_A_DQ<57>
MEM_A_DQ<32>	TRUE	=MEM_A_DQ<8>
MEM_A_DQ<33>	TRUE	=MEM_A_DQ<11>
MEM_A_DQ<34>	TRUE	=MEM_A_DQ<10>
MEM_A_DQ<35>	TRUE	=MEM_A_DQ<13>
MEM_A_DQ<36>	TRUE	=MEM_A_DQ<12>
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MEM_A_DQ<38>	TRUE	=MEM_A_DQ<14>
MEM_A_DQ<39>	TRUE	=MEM_A_DQ<15>
MEM_A_DQ<40>	TRUE	=MEM_A_DQ<24>
MEM_A_DQ<41>	TRUE	=MEM_A_DQ<25>
MEM_A_DQ<42>	TRUE	=MEM_A_DQ<27>
MEM_A_DQ<43>	TRUE	=MEM_A_DQ<30>
MEM_A_DQ<44>	TRUE	=MEM_A_DQ<28>
MEM_A_DQ<45>	TRUE	=MEM_A_DQ<29>
MEM_A_DQ<46>	TRUE	=MEM_A_DQ<31>
MEM_A_DQ<47>	TRUE	=MEM_A_DQ<26>
MEM_A_DQ<48>	TRUE	=MEM_A_DQ<39>
MEM_A_DQ<49>	TRUE	=MEM_A_DQ<33>
MEM_A_DQ<50>	TRUE	=MEM_A_DQ<34>
MEM_A_DQ<51>	TRUE	=MEM_A_DQ<35>
MEM_A_DQ<52>	TRUE	=MEM_A_DQ<36>
MEM_A_DQ<53>	TRUE	=MEM_A_DQ<37>
MEM_A_DQ<54>	TRUE	=MEM_A_DQ<38>
MEM_A_DQ<55>	TRUE	=MEM_A_DQ<32>
MEM_A_DQ<56>	TRUE	=MEM_A_DQ<55>
MEM_A_DQ<57>	TRUE	=MEM_A_DQ<51>
MEM_A_DQ<58>	TRUE	=MEM_A_DQ<49>
MEM_A_DQ<59>	TRUE	=MEM_A_DQ<52>
MEM_A_DQ<60>	TRUE	=MEM_A_DQ<48>
MEM_A_DQ<61>	TRUE	=MEM_A_DQ<53>
MEM_A_DQ<62>	TRUE	=MEM_A_DQ<54>
MEM_A_DQ<63>	TRUE	=MEM_A_DQ<50>
MEM_A_DQS_P<0>	TRUE	=MEM_A_DQS_P<2>
MEM_A_DQS_N<0>	TRUE	=MEM_A_DQS_N<2>
MEM_A_DQS_P<1>	TRUE	=MEM_A_DQS_P<0>
MEM_A_DQS_N<1>	TRUE	=MEM_A_DQS_N<0>
MEM_A_DQS_P<2>	TRUE	=MEM_A_DQS_P<5>
MEM_A_DQS_N<2>	TRUE	=MEM_A_DQS_N<5>
MEM_A_DQS_P<3>	TRUE	=MEM_A_DQS_P<7>
MEM_A_DQS_N<3>	TRUE	=MEM_A_DQS_N<7>
MEM_A_DQS_P<4>	TRUE	=MEM_A_DQS_P<1>
MEM_A_DQS_N<4>	TRUE	=MEM_A_DQS_N<1>
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MEM_A_DQS_N<6>	TRUE	=MEM_A_DQS_N<4>
MEM_A_DQS_P<7>	TRUE	=MEM_A_DQS_P<6>
MEM_A_DQS_N<7>	TRUE	=MEM_A_DQS_N<6>

CPU	MAKE_BASE	DRAM
MEM_B_DQ<0>	TRUE	=MEM_B_DQ<6>
MEM_B_DQ<1>	TRUE	=MEM_B_DQ<7>
MEM_B_DQ<2>	TRUE	=MEM_B_DQ<1>
MEM_B_DQ<3>	TRUE	=MEM_B_DQ<3>
MEM_B_DQ<4>	TRUE	=MEM_B_DQ<4>
MEM_B_DQ<5>	TRUE	=MEM_B_DQ<5>
MEM_B_DQ<6>	TRUE	=MEM_B_DQ<2>
MEM_B_DQ<7>	TRUE	=MEM_B_DQ<0>
MEM_B_DQ<8>	TRUE	=MEM_B_DQ<16>
MEM_B_DQ<9>	TRUE	=MEM_B_DQ<20>
MEM_B_DQ<10>	TRUE	=MEM_B_DQ<19>
MEM_B_DQ<11>	TRUE	=MEM_B_DQ<23>
MEM_B_DQ<12>	TRUE	=MEM_B_DQ<21>
MEM_B_DQ<13>	TRUE	=MEM_B_DQ<17>
MEM_B_DQ<14>	TRUE	=MEM_B_DQ<22>
MEM_B_DQ<15>	TRUE	=MEM_B_DQ<18>
MEM_B_DQ<16>	TRUE	=MEM_B_DQ<40>
MEM_B_DQ<17>	TRUE	=MEM_B_DQ<41>
MEM_B_DQ<18>	TRUE	=MEM_B_DQ<45>
MEM_B_DQ<19>	TRUE	=MEM_B_DQ<46>
MEM_B_DQ<20>	TRUE	=MEM_B_DQ<42>
MEM_B_DQ<21>	TRUE	=MEM_B_DQ<43>
MEM_B_DQ<22>	TRUE	=MEM_B_DQ<44>
MEM_B_DQ<23>	TRUE	=MEM_B_DQ<47>
MEM_B_DQ<24>	TRUE	=MEM_B_DQ<63>
MEM_B_DQ<25>	TRUE	=MEM_B_DQ<59>
MEM_B_DQ<26>	TRUE	=MEM_B_DQ<57>
MEM_B_DQ<27>	TRUE	=MEM_B_DQ<61>
MEM_B_DQ<28>	TRUE	=MEM_B_DQ<58>
MEM_B_DQ<29>	TRUE	=MEM_B_DQ<62>
MEM_B_DQ<30>	TRUE	=MEM_B_DQ<60>
MEM_B_DQ<31>	TRUE	=MEM_B_DQ<56>
MEM_B_DQ<32>	TRUE	=MEM_B_DQ<10>
MEM_B_DQ<33>	TRUE	=MEM_B_DQ<9>
MEM_B_DQ<34>	TRUE	=MEM_B_DQ<12>
MEM_B_DQ<35>	TRUE	=MEM_B_DQ<13>
MEM_B_DQ<36>	TRUE	=MEM_B_DQ<11>
MEM_B_DQ<37>	TRUE	=MEM_B_DQ<15>
MEM_B_DQ<38>	TRUE	=MEM_B_DQ<14>
MEM_B_DQ<39>	TRUE	=MEM_B_DQ<8>
MEM_B_DQ<40>	TRUE	=MEM_B_DQ<24>
MEM_B_DQ<41>	TRUE	=MEM_B_DQ<31>
MEM_B_DQ<42>	TRUE	=MEM_B_DQ<26>
MEM_B_DQ<43>	TRUE	=MEM_B_DQ<27>
MEM_B_DQ<44>	TRUE	=MEM_B_DQ<25>
MEM_B_DQ<45>	TRUE	=MEM_B_DQ<28>
MEM_B_DQ<46>	TRUE	=MEM_B_DQ<30>
MEM_B_DQ<47>	TRUE	=MEM_B_DQ<29>
MEM_B_DQ<48>	TRUE	=MEM_B_DQ<32>
MEM_B_DQ<49>	TRUE	=MEM_B_DQ<33>
MEM_B_DQ<50>	TRUE	=MEM_B_DQ<34>
MEM_B_DQ<51>	TRUE	=MEM_B_DQ<38>
MEM_B_DQ<52>	TRUE	=MEM_B_DQ<36>
MEM_B_DQ<53>	TRUE	=MEM_B_DQ<37>
MEM_B_DQ<54>	TRUE	=MEM_B_DQ<35>
MEM_B_DQ<55>	TRUE	=MEM_B_DQ<39>
MEM_B_DQ<56>	TRUE	=MEM_B_DQ<55>
MEM_B_DQ<57>	TRUE	=MEM_B_DQ<54>
MEM_B_DQ<58>	TRUE	=MEM_B_DQ<50>
MEM_B_DQ<59>	TRUE	=MEM_B_DQ<51>
MEM_B_DQ<60>	TRUE	=MEM_B_DQ<52>
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MEM_B_DQS_P<0>	TRUE	=MEM_B_DQS_P<0>
MEM_B_DQS_N<0>	TRUE	=MEM_B_DQS_N<0>
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MEM_B_DQS_N<1>	TRUE	=MEM_B_DQS_N<2>
MEM_B_DQS_P<2>	TRUE	=MEM_B_DQS_P<5>
MEM_B_DQS_N<2>	TRUE	=MEM_B_DQS_N<5>
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MEM_B_DQS_P<4>	TRUE	=MEM_B_DQS_P<1>
MEM_B_DQS_N<4>	TRUE	=MEM_B_DQS_N<1>
MEM_B_DQS_P<5>	TRUE	=MEM_B_DQS_P<3>
MEM_B_DQS_N<5>	TRUE	=MEM_B_DQS_N<3>
MEM_B_DQS_P<6>	TRUE	=MEM_B_DQS_P<4>
MEM_B_DQS_N<6>	TRUE	=MEM_B_DQS_N<4>
MEM_B_DQS_P<7>	TRUE	=MEM_B_DQS_P<6>
MEM_B_DQS_N<7>	TRUE	=MEM_B_DQS_N<6>

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB_CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
Memory Signal Swaps

Apple Inc.

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XDP

17 6	CPU_CFG<3>	FUNC_TEST=TRUE
17 6	ITP_PMODE	FUNC_TEST=TRUE
17 15	XDP_CPU_PRDY_L	FUNC_TEST=TRUE
17 15	XDP_CPU_PREQ_L	FUNC_TEST=TRUE
17	XDP_CPU_PWRBTN_L	FUNC_TEST=TRUE
17 6	XDP_CPU_TCK	FUNC_TEST=TRUE
17 6	XDP_CPU_TDI	FUNC_TEST=TRUE
17 6	XDP_CPU_TDO	FUNC_TEST=TRUE
17 6	XDP_CPU_TMS	FUNC_TEST=TRUE
17 6	XDP_CPU_TRST_L	FUNC_TEST=TRUE
17	XDP_DBRESET_L	FUNC_TEST=TRUE
17 6	XDP_PCH_TCK	FUNC_TEST=TRUE
17 6	XDP_PCH_TDI	FUNC_TEST=TRUE
17 6	XDP_PCH_TDO	FUNC_TEST=TRUE
17 6	XDP_PCH_TMS	FUNC_TEST=TRUE
17 6	XDP_PCH_TRST_L	FUNC_TEST=TRUE
17	XDP_PM_RSMRST_L	FUNC_TEST=TRUE
17	XDP_PRESENT_CPU	FUNC_TEST=TRUE
60 17	XDP_PRESENT_L	FUNC_TEST=TRUE
69 64 63 62 19	PP1V_S5G	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

AUDIO FLEX

51	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE
51	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE
51	AUD_CONN_HP_SENSE_L	FUNC_TEST=TRUE
51	AUD_CONN_HP_SENSE_R	FUNC_TEST=TRUE
51	AUD_CONN_RING2	FUNC_TEST=TRUE
51	AUD_CONN_RING2_XW	FUNC_TEST=TRUE
51	AUD_CONN_SLEEVE	FUNC_TEST=TRUE
51	AUD_CONN_SLEEVE_XW	FUNC_TEST=TRUE
51	AUD_CONN_TIP_SENSE	FUNC_TEST=TRUE
51 48	DMIC1_CLK	FUNC_TEST=TRUE
51 48	DMIC1_DATA	FUNC_TEST=TRUE
51 41	HALL_SENSOR_RIGHT	FUNC_TEST=TRUE
69 67 64 63 60 51 50 48	PP1V8_S0	FUNC_TEST=TRUE
53 52 51 47 42 41 28 19 72 69 68 66	PP3V3_G3H	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

LEFT SPEAKERS

51 48	8409_SPKR_ID0	FUNC_TEST=TRUE
51 50	SPKRCONN_FL_OUT_N	FUNC_TEST=TRUE
51 50	SPKRCONN_FL_OUT_P	FUNC_TEST=TRUE
51 50	SPKRCONN_RL_OUT_N	FUNC_TEST=TRUE
51 50	SPKRCONN_RL_OUT_P	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

RIGHT SPEAKERS

51 48	8409_SPKR_ID1	FUNC_TEST=TRUE
51 50	SPKRCONN_FR_OUT_N	FUNC_TEST=TRUE
51 50	SPKRCONN_FR_OUT_P	FUNC_TEST=TRUE
51 50	SPKRCONN_RR_OUT_N	FUNC_TEST=TRUE
51 50	SPKRCONN_RR_OUT_P	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

BATTERY

52	SYS_DETECT_L	FUNC_TEST=TRUE
72 42	SMBUS_SMC_5_G3H_SCL	FUNC_TEST=TRUE
72 42	SMBUS_SMC_5_G3H_SCL	FUNC_TEST=TRUE

SMC

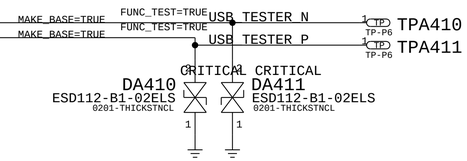
47 40 39 28	SMC_TCK	FUNC_TEST=TRUE
40 39	SMC_TDI	FUNC_TEST=TRUE
40 39	SMC_TDO	FUNC_TEST=TRUE
47 40 39 28	SMC_TMS	FUNC_TEST=TRUE
41	SMC_DEV_SUPPLY_L	FUNC_TEST=TRUE

BOOTROM

47 16	SPIROM_USE_MLB	FUNC_TEST=TRUE
47	SPI_MLBROM_CS_L	FUNC_TEST=TRUE
47	SPI_MLB_CLK	FUNC_TEST=TRUE
47	SPI_MLB_CS_L	FUNC_TEST=TRUE
47	SPI_MLB_IO<2>	FUNC_TEST=TRUE
47	SPI_MLB_IO<3>	FUNC_TEST=TRUE
47	SPI_MLB_MISO	FUNC_TEST=TRUE
47	SPI_MLB_MOSI	FUNC_TEST=TRUE

USB2 FIXTURE PORT

15	TP_USB_TESTERN	FUNC_TEST=TRUE
15	TP_USB_TESTERP	FUNC_TEST=TRUE
69 64 63 60 58 54	PP5V_S4	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE



CAP POWER DISCHARGE

69 68 63 60 58 53 50 43	PPBUS_G3H	FUNC_TEST=TRUE
69 68 63 53	PPDCIN_G3H	FUNC_TEST=TRUE
53 52	PPDCIN_G3H_CHGR	FUNC_TEST=TRUE
72 66 65	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE

SYSTEM STATE

68 60 19	PM_SLP_S0S3_L	FUNC_TEST=TRUE
60 39 14	PM_SLP_S0_L	FUNC_TEST=TRUE
66 60 59 39 26 14	PM_SLP_S3_L	FUNC_TEST=TRUE
68 60 39 14	PM_SLP_S4_L	FUNC_TEST=TRUE
60 39 14	PM_SLP_S5_L	FUNC_TEST=TRUE
60 14	PM_SLP_SUS_L	FUNC_TEST=TRUE
41 39 17	PM_PWRBTN_L	FUNC_TEST=TRUE
60 39	ALL_SYS_PWRGD	FUNC_TEST=TRUE

MOJO PORT

40 39 28	SMC_DEBUGPRT_TX_L	FUNC_TEST=TRUE
40 39 28	SMC_DEBUGPRT_RX_L	FUNC_TEST=TRUE

MISC

67	SSD_BOOT_CONN_L	FUNC_TEST=TRUE
14	TP_PCH_SLP_A_L	FUNC_TEST=TRUE

CAMERA

36	CAM_TEST_MODE	FUNC_TEST=TRUE
36	TP_CAM_LV_JTAG_TCK	FUNC_TEST=TRUE
36	TP_CAM_LV_JTAG_TDI	FUNC_TEST=TRUE
36	TP_CAM_LV_JTAG_TDO	FUNC_TEST=TRUE
36	TP_CAM_LV_JTAG_TMS	FUNC_TEST=TRUE
36	TP_CAM_LV_JTAG_TRSTN	FUNC_TEST=TRUE
36	TP_CAM_TEST_MODE0	FUNC_TEST=TRUE
36	TP_CAM_TEST_MODE1	FUNC_TEST=TRUE
36	TP_CAM_TEST_MODE2	FUNC_TEST=TRUE

DISPLAY

66 5	DP_INT_HPD	FUNC_TEST=TRUE
66 5	EDP_BKLT_PWM	FUNC_TEST=TRUE
66	EDP_INT_AUX_N	FUNC_TEST=TRUE
66	EDP_INT_AUX_P	FUNC_TEST=TRUE
66 5	EDP_PANEL_PWR_EN	FUNC_TEST=TRUE
66	I2C_ALS_SCL_CONN	FUNC_TEST=TRUE
66	I2C_ALS_SDA_CONN	FUNC_TEST=TRUE
70 66	I2C_BKLT_SCL	FUNC_TEST=TRUE
70 66	I2C_BKLT_SDA	FUNC_TEST=TRUE
66	I2C_CAM_SCL_CONN	FUNC_TEST=TRUE
66	I2C_CAM_SDA_CONN	FUNC_TEST=TRUE
66	I2C_TCON_SCL_CONN	FUNC_TEST=TRUE
66	I2C_TCON_SDA_CONN	FUNC_TEST=TRUE
66 16	LCD_IRQ_L	FUNC_TEST=TRUE
66 37	MIPI_CLK_CONN_N	FUNC_TEST=TRUE
66 37	MIPI_CLK_CONN_P	FUNC_TEST=TRUE
66 37	MIPI_DATA_CONN_N	FUNC_TEST=TRUE
66 37	MIPI_DATA_CONN_P	FUNC_TEST=TRUE
66 41	TCON_BKLT_PWM	FUNC_TEST=TRUE
66	PP3V3_S0SW_LCD	FUNC_TEST=TRUE
66	PP5V_S0SW_LCD	FUNC_TEST=TRUE
66 37	PP5V_S0_ALSCAM_F	FUNC_TEST=TRUE
72 66 65	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

USBC/TBT

28 26	JTAG_TBT_TCK	FUNC_TEST=TRUE
28 26	JTAG_TBT_TDI	FUNC_TEST=TRUE
28 26	JTAG_TBT_X_TMS	FUNC_TEST=TRUE
26	TBT_X_TEST_EN	FUNC_TEST=TRUE
31 28	PP20V_USBC_XA_VBUS	FUNC_TEST=TRUE
32 28	PP20V_USBC_XB_VBUS	FUNC_TEST=TRUE

POWER

69 67 64 61 59	PP1V8_S5G	FUNC_TEST=TRUE
59	PP1V_OPC_S0	FUNC_TEST=TRUE
69 63 44	PP3V3_S4_WLS	FUNC_TEST=TRUE
69 68 64 63 61 60 58 44	PP3V3_S5	FUNC_TEST=TRUE
69 64 60	PP3V3_S5G	FUNC_TEST=TRUE
69 63 55 45	PPVCCCPU_S0G	FUNC_TEST=TRUE
69 63 57 45	PPVCCGT_S0G	FUNC_TEST=TRUE
69 63 61	PPVCCIO_S0G	FUNC_TEST=TRUE
59	PPVCCOPC_S0G	FUNC_TEST=TRUE
69 63 61	PPVCCPCH_S5G	FUNC_TEST=TRUE
69 56	PPVCCSA_S0G	FUNC_TEST=TRUE
69 62	PPVTT_S0	FUNC_TEST=TRUE

WIRELESS

34	JTAG_WLAN_SEL	FUNC_TEST=TRUE
34	TP_JTAG_WLAN_TCK	FUNC_TEST=TRUE
34	JTAG_WLAN_TDI	FUNC_TEST=TRUE
34	TP_JTAG_WLAN_TDO	FUNC_TEST=TRUE
34	TP_JTAG_WLAN_TMS	FUNC_TEST=TRUE
34	TP_JTAG_WLAN_TRST	FUNC_TEST=TRUE

TRACKPAD AND KEYBOARD

39 38	ACT_THERM_TRIP_L	FUNC_TEST=TRUE
38	FAN_LT_PWM	FUNC_TEST=TRUE
38	FAN_LT_TACH	FUNC_TEST=TRUE
38	KBD_BLC_GSLAT	FUNC_TEST=TRUE
38	KBD_BLC_GSSCK	FUNC_TEST=TRUE
38	KBD_BLC_GSSIN	FUNC_TEST=TRUE
38	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
38	KBD_BLC_XBLANK	FUNC_TEST=TRUE
38	KBD_I2C_SCL	FUNC_TEST=TRUE
38	KBD_I2C_SDA	FUNC_TEST=TRUE
38	KBD_INT_L	FUNC_TEST=TRUE
38 16	TPAD_SPI_MOSI	FUNC_TEST=TRUE
38 16	TPAD_SPI_INT_L	FUNC_TEST=TRUE
38	TPAD_SPI_CS_CONN_L	FUNC_TEST=TRUE
38 16	TPAD_SPI_MISO	FUNC_TEST=TRUE
38 16	TPAD_SPI_IF_EN	FUNC_TEST=TRUE
38 16	TPAD_SPI_CLK	FUNC_TEST=TRUE
38	TPAD_VIBE_L	FUNC_TEST=TRUE
41 38	SMC_LSOC_RST	FUNC_TEST=TRUE
68 40 39 38	SMC_ONOFF_L	FUNC_TEST=TRUE
41 40 39	SMC_PME_S4_WAKE_L	FUNC_TEST=TRUE
68 60 53 52 51 47 42 41 28 19 72 69	PP3V3_G3H	FUNC_TEST=TRUE
69 67 64 63 45 44 43 41	PP3V3_S4	FUNC_TEST=TRUE
69 64 59 57 56 55 54	PP5V_S0	FUNC_TEST=TRUE
38	PP5V_S4_TPAD_CONN	FUNC_TEST=TRUE
38	PPVIN_S4_TPAD_FUSE	FUNC_TEST=TRUE
	GND	FUNC_TEST=TRUE

66 5	EDP_ML_C_N<0..3>	NO_TEST=1
66 5	EDP_ML_C_P<0..3>	NO_TEST=1
66	EDP_INT_ML_N<0..3>	NO_TEST=1
66	EDP_INT_ML_P<0..3>	NO_TEST=1
35 34	PCIE_AP_D2R_C_N	NO_TEST=1
35 34	PCIE_AP_D2R_C_P	NO_TEST=1
35 15	PCIE_AP_D2R_N	NO_TEST=1
35 15	PCIE_AP_D2R_P	NO_TEST=1
35 15	PCIE_AP_R2D_C_N	NO_TEST=1
35 15	PCIE_AP_R2D_C_P	NO_TEST=1
35 34	PCIE_AP_R2D_N	NO_TEST=1
35 34	PCIE_AP_R2D_P	NO_TEST=1
67 15	PCIE_SSD_D2R_N<0..3>	NO_TEST=1
67 15	PCIE_SSD_D2R_P<0..3>	NO_TEST=1
67 15	PCIE_SSD_R2D_C_N<0..3>	NO_TEST=1
67 15	PCIE_SSD_R2D_C_P<0..3>	NO_TEST=1
67	PCIE_SSD_R2D_N<0..3>	NO_TEST=1
67	PCIE_SSD_R2D_P<0..3>	NO_TEST=1
30	USB_UPC_XB_F_N	NO_TEST=1
30	USB_UPC_XB_F_P	NO_TEST=1
31 26	USBC_XA_D2R_N<1..2>	NO_TEST=1
31 26	USBC_XA_D2R_P<1..2>	NO_TEST=1
31 26	USBC_XA_R2D_C_N<1..2>	NO_TEST=1
31 26	USBC_XA_R2D_C_P<1..2>	NO_TEST=1
31	USBC_XA_R2D_N<1..2>	NO_TEST=1
31	USBC_XA_R2D_P<1..2>	NO_TEST=1
29 28	USBC_XA_USB_BOT_N	NO_TEST=1
29 28	USBC_XA_USB_BOT_P	NO_TEST=1
29 28	USBC_XA_USB_TOP_N	NO_TEST=1
29 28	USBC_XA_USB_TOP_P	NO_TEST=1
32 26	USBC_XB_D2R_N<1..2>	NO_TEST=1
32 26	USBC_XB_D2R_P<1..2>	NO_TEST=1
32 26	USBC_XB_R2D_C_N<1..2>	NO_TEST=1
32 26	USBC_XB_R2D_C_P<1..2>	NO_TEST=1
32	USBC_XB_R2D_N<1..2>	NO_TEST=1
32	USBC_XB_R2D_P<1..2>	NO_TEST=1
32 30	USBC_XB_USB_BOT_N	NO_TEST=1
32 30	USBC_XB_USB_BOT_P	NO_TEST=1
32 30	USBC_XB_USB_TOP_N	NO_TEST=1
32 30	USBC_XB_USB_TOP_P	NO_TEST=1
55	AGND_U7320	NO_TEST=1
	BANJO_VBSTVR1	NO_TEST=1
	BANJO_VBSTVR3	NO_TEST=1
62	BANJO_VBSTVR4	NO_TEST=1
61	BANJO_VBSTVR5	NO_TEST=1
55	CPUVR_BP2	NO_TEST=1
55	CPUVR_PHASE2	
55	CPUVR_SNB1	NO_TEST=1
55	CPUVR_SNB2	NO_TEST=1
59	PD_VSNS_CPU_VCCEOPIO_TN	NO_TEST=1
59	PD_VSNS_CPU_VCCOPC_TN	NO_TEST=1
55	PPVCCCPU_S0G_PH1	NO_TEST=1
55	PPVCCCPU_S0G_PH2	NO_TEST=1
56	PPVCCSA_S0G_R	NO_TEST=1
59	PU_VSNS_CPU_VCCEOPIO_TP	NO_TEST=1
59	PU_VSNS_CPU_VCCOPC_TP	NO_TEST=1
27	VR0V9_IND_TBT_X	NO_TEST=1
12	PP1V_SUS_PCH_VCCAPLL_F	NO_TEST=1
12	PP1V8_S0_PCH_VCCHDA_F	NO_TEST=1
25 21 7	MEM_A_CAA<0..9>	NO_TEST=1
25 22 7	MEM_A_CAB<0..9>	NO_TEST=1
25 22 21 7	MEM_A_CKE<0..3>	NO_TEST=1
25 22 21 7	MEM_A_CLK_N<0..1>	NO_TEST=1
25 22 21 7	MEM_A_CLK_P<0..1>	NO_TEST=1
25 22 21 7	MEM_A_CS_L<0..1>	NO_TEST=1
71 7	MEM_A_DQ<0..63>	NO_TEST=1
71 7	MEM_A_DQS_N<0..7>	NO_TEST=1
71 7	MEM_A_DQS_P<0..7>	NO_TEST=1
25 22 21 7	MEM_A_ODT<0>	NO_TEST=1
25 23 7	MEM_B_CAA<0..9>	NO_TEST=1
25 24 7	MEM_B_CAB<0..9>	NO_TEST=1
25 24 23 7	MEM_B_CKE<0..3>	NO_TEST=1
25 24 23 7	MEM_B_CLK_N<0..1>	NO_TEST=1
25 24 23 7	MEM_B_CLK_P<0..1>	NO_TEST=1
25 24 23 7	MEM_B_CS_L<0..1>	NO_TEST=1
71 7	MEM_B_DQ<0..63>	NO_TEST=1
71 7	MEM_B_DQS_N<0..7>	NO_TEST=1
71 7	MEM_B_DQS_P<0..7>	NO_TEST=1
25 24 23 7	MEM_B_ODT<0>	NO_TEST=1
37 36	MEM_CAM_A<0..14>	NO_TEST=1
37 36	MEM_CAM_BA<0..2>	NO_TEST=1
37 36	MEM_CAM_DM<0..1>	NO_TEST=1
37 36	MEM_CAM_DQ<0..15>	NO_TEST=1
37 36	MEM_CAM_DQS_N<0..1>	NO_TEST=1
37 36	MEM_CAM_DQS_P<0..1>	NO_TEST=1
34	RF_0_ANT	NO_TEST=1
34	RF_0_ANT_MATCH_T	NO_TEST=1
34	RF_1_ANT	NO_TEST=1
34	RF_1_ANT_MATCH_T	NO_TEST=1
34	RF_A_0_DIPLEXER	NO_TEST=1
34	RF_A_0_MATCH	NO_TEST=1
34	RF_A_1_DIPLEXER	NO_TEST=1
34	RF_A_1_MATCH	NO_TEST=1
34	RF_G_0_DIPLEXER	NO_TEST=1
34	RF_G_0_MATCH	NO_TEST=1
34	RF_G_1_DIPLEXER	NO_TEST=1
34	RF_G_1_MATCH	NO_TEST=1
55	AGND_U7310	NO_TEST=1
61	BANJO_FBVR2_N	NO_TEST=1
61	BANJO_FBVR2_RC	NO_TEST=1
61	BANJO_SWVR2	NO_TEST=1
61	BANJO_SWVR2_SNUB	NO_TEST=1
61	BANJO_SWVR3R	NO_TEST=1
61	BANJO_SWVR3_SNUB	NO_TEST=1
62	BANJO_VBSTVR1_R	NO_TEST=1
61	BANJO_VBSTVR3_R	NO_TEST=1
62	BANJO_VBSTVR4_R	NO_TEST=1
61	BANJO_VBSTVR5_R	NO_TEST=1
55	CPUVR_BOOT1	NO_TEST=1
55	CPUVR_BP1	NO_TEST=1
55 45	CPUVR_ISNS2_N	NO_TEST=1
55 45	CPUVR_ISNS2_P	NO_TEST=1
55	CPUVR_PHASE1	NO_TEST=1
55	CPUVR_SW1	NO_TEST=1
6	CPU_PROCHOT_R_L	NO_TEST=1
54 8	CPU_VCCGTSENSE_N	NO_TEST=1
14	CPU_VCCST_PWRGD_R	NO_TEST=1
57	GTVR_BP1	
57 45	GTVR_ISNS2_P	NO_TEST=1
57	GTVR_SNB1	NO_TEST=1
57	GTVR_SNB2	NO_TEST=1
57	GTVR_SNB3	NO_TEST=1
57	GTVR_SW1	NO_TEST=1
57	GTVR_SW2	NO_TEST=1
59	P1VOPC_BOOT_RC	NO_TEST=1
59	P1VOPC_DRVH_R	NO_TEST=1
59	P1VOPC_REFIN_R	NO_TEST=1
59	P1VOPC_SNS_R	NO_TEST=1
58	P3V3S5_DRVH_R	NO_TEST=1
58	P5VS4_DRVH_R	NO_TEST=1
56	SAVR_BP	NO_TEST=1
56	SAVR_SNB1	NO_TEST=1
56	SAVR_SW	NO_TEST=1
72 55	VCINP_P5V_U7310	NO_TEST=1
56	AGND_U7470	NO_TEST=1
72 55	VCINP_P5V_U7310	NO_TEST=1
59	VCINP_P5V_U7320	NO_TEST=1
53	TBA_PHASE1	NO_TEST=1
60	PMIC_ENH	NO_TEST=1

FOR DC/DC

53	TBA_HPWR_EN_L	FUNC_TEST=TRUE
53	PD_TBA_MPM_DET	FUNC_TEST=TRUE

FOR DEBUG

29	TP_UPC_XA_DBG_UART_TX	FUNC_TEST=TRUE
29	TP_UPC_XA_DBG_UART_RX	FUNC_TEST=TRUE
30	TP_UPC_XB_DBG_UART_TX	FUNC_TEST=TRUE
30	TP_UPC_XB_DBG_UART_RX	FUNC_TEST=TRUE

BOM_COST_GROUP=NO COST ITEMS

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

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