

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	APPD DATE
			2010-03-18

SCHM, MLB_LDO, K6
PVT, 3/18/10


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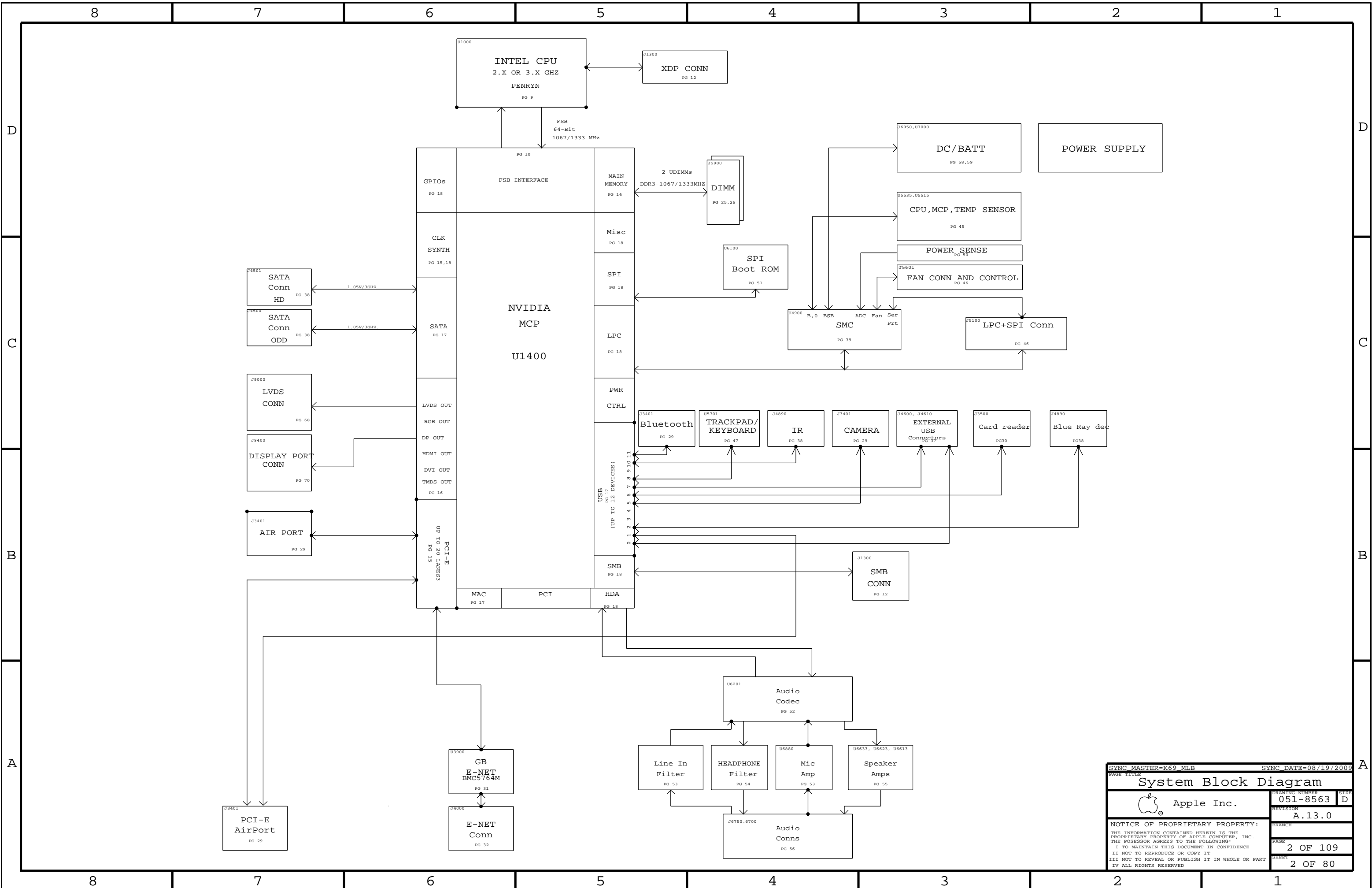
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Schematic / PCB #'s

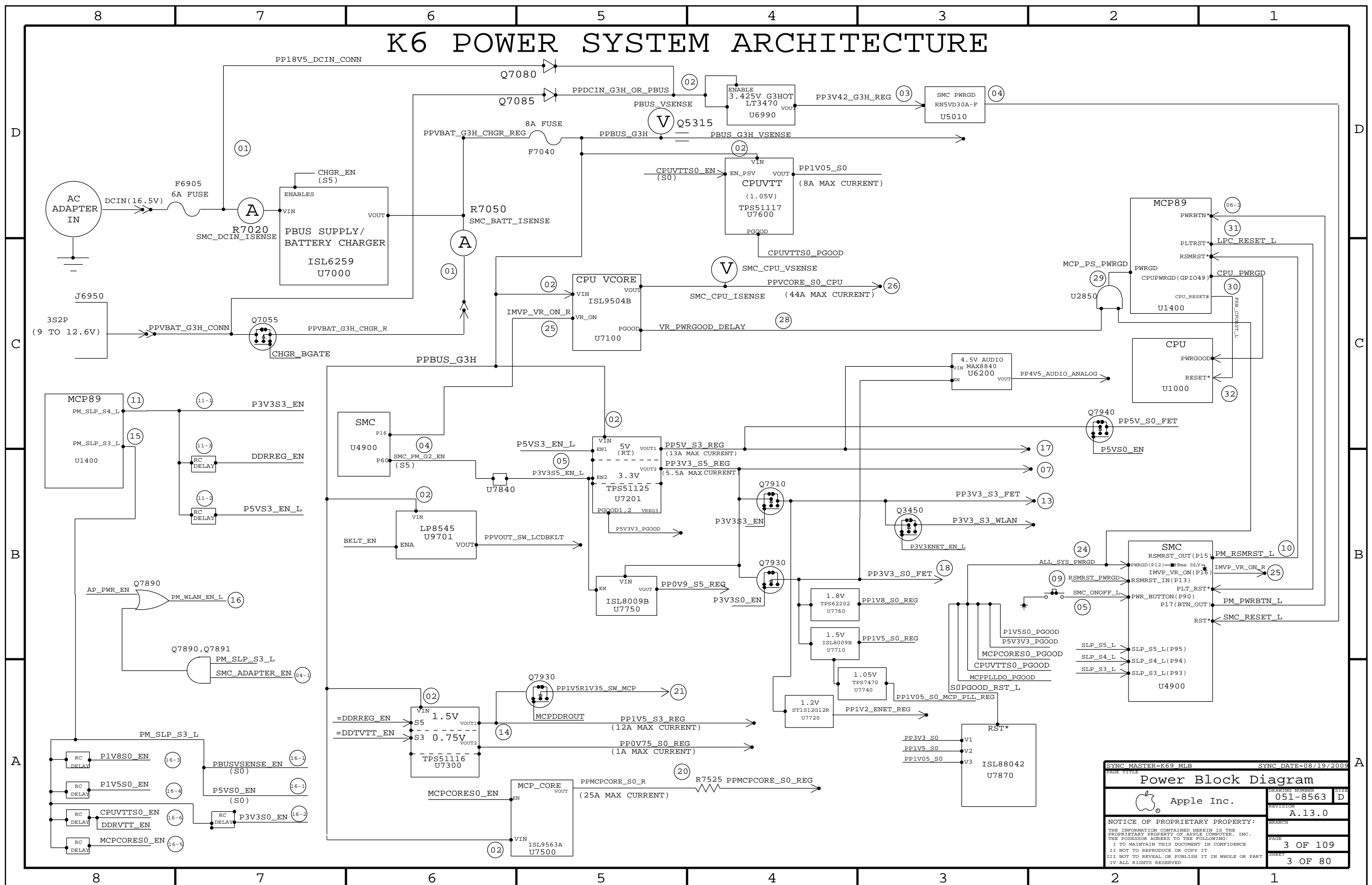
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8563	1	SCHEM,MLB_LDO,K6	SCH	CRITICAL	
820-2879	1	PCBP,MLB_LDO,K6	PCB	CRITICAL	

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DRAWING TITLE	
SCHEM, MLB_LDO, K6	
	Apple Inc.
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K6 POWER SYSTEM ARCHITECTURE



8		7		6		
BOM Variants						
BOM NUMBER	BOM NAME			BOM OPTIONS		
639-1120	PCBA,MLB_LDO,BETTER,K6			K6_COMMON,CPU:2.4GHZ,MCP89M:A02,EEEE:DD24		
639-1119	PCBA,MLB_LDO,BEST,K6			K6_COMMON,CPU:2.66GHZ,MCP89M:A02,EEEE:DD23		
085-1634	K6 MLB_LDO DEVELOPMENT BOM			K6_DEVEL:PVT		

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DD23]	CRITICAL	EEEE:DD23
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DD24]	CRITICAL	EEEE:DD24

BOM Groups	
BOM GROUP	BOM OPTIONS
K6_COMMON	COMMON,ALTERNATE,K6_MISC,K6_DEBUG:PROD,KB_BL,K6_PROGPARTS,RDRV:NO,SPI:25MHZ,CPU_CAP:15
K6_MISC	DP_ESD,MIKEY,BCM5764M,GLI37,ENET_ESD,VFRQ:SLP3,LVDDR3:YES,MCPLL_R:REG,SOPGOOD_BJT,BOOST_VOL:LOW,HDA:1.5V
K6_PROGPARTS	BOOTROM:UNLOCKED,SMC:PROG,IR:PROG,WELLSPRING:PROG
K6_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,LPCPLUS,VREFMRGN:YES,EFI_DEBUG,SOPGOOD_ISL,RDRV:IN_DEVEL
K6_DEVEL:PVT	LPCPLUS,XDP_CONN
K6_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG:YES,XDP
K6_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO
K6_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG:YES,XDP,VREFMRGN:NO,LPCPLUS,MCPHVD:P2V5,LDO:FIXED,HTOL_SENSE:YES

Module Parts						
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
337S3769	1	PDC, SLOVT, FRQ. 2.26, 25W, 1066, R0, 3M, BGA, P7550	U1000	CRITICAL	CPU: 2.26GHZ	
337S3680	1	PDC, L2DE, FRQ. 2.40, 25W, 1066, R0, 3M, BGA	U1000	CRITICAL	CPU: 2.43GHZ	
337S3756	1	PDC, SLOFO, FRQ. 2.53, 25W, 1066, R0, 3M, BGA	U1000	CRITICAL	CPU: 2.53GHZ	
337S3761	1	PDC, ELGLA, FRQ. 2.66, 25W, 1066, R0, 3M, BGA	U1000	CRITICAL	CPU: 2.66GHZ	
337S3797	1	IC, MCP89M-A01, 31X31MM, BGA1168	U1400	CRITICAL	MCP89M: A01	
337S3866	1	IC, MCP89M-A01, 31X31MM, BGA1168	U1400	CRITICAL	MCP89M: A02	
341S2731	1	IC, 1MBIT, SPI FLASH, K17/18	U3990	CRITICAL	BCM5764M	
343S0493	1	IC, ASIC, BCM5764M, ENET CONTROLLER, 8x8, 64QFN	U3900	CRITICAL	BCM5764M	
338S0753	1	IC, FW643-E2, 1394B PHY/ONCI LINK/PCI-E-1, 2	U4100	CRITICAL		
353S2896	1	IC, LP8545, LED BKLT CTRLR, LLP24	U9701	CRITICAL		


Programmable Parts						
338S0563	1	IC, SMC, HS8/2117, 9X9MM, TLP, HF	U4900	CRITICAL	SMC: BLANK	
341T0240	1	SMC EXTERNAL, K6	U4900	CRITICAL	SMC: PROG	
335S0610	1	IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP	U6100	CRITICAL	BOOTROM: BLANK	
341T0238	1	EFI UNLOCKED, K6/K69	U6100	CRITICAL	BOOTROM: UNLOCKED	
341S2589	1	IC, EFI, LOCKED, K6	U6100	CRITICAL	BOOTROM: LOCKED	
338S0633	1	IC, CYPRS, CY7C63803-LQXC, 4X4MM, USB, 24-PIN	U4800	CRITICAL	IR: BLANK	
341S2384	1	IC, ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	IR: PROG	
337S2983	1	IC, PSOC+ W/ USB, 56 PIN, MLF, CY8C24794	U5701	CRITICAL	WELLSPRING: BLANK	
341S2616	1	IC, TP PSOC, K17, K18	U5701	CRITICAL	WELLSPRING: PROG	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0693	152S0778		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE /VISHAY AS ALTERNATE
128S0093	128S0218		ALL	ESMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
152S1025	152S1024		ALL	TOKO AS ALTERNATE
337S3769	337S3704		ALL	INTEL P7550 CPU AS ALTERNATE
152S1135	152S0586		ALL	TOKO AS ALTERNATE
516-0213	516-0201		ALL	MOLEX AS ALTERNATE
516S0790	516S0706		ALL	MOLEX AS ALTERNATE
376S0699	376S0360		ALL	SM6P15PF AS ALTERNATE

DEVELOPMENT BOM					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1634	1	K6 MLB_LDO DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM

K6 BOARD STACK-UP

Top		SIGNAL
2		GROUND
3		SIGNAL(High Speed)
4		SIGNAL(High Speed)
5		GROUND
6		POWER
7		POWER
8		GROUND
9		SIGNAL(High Speed)
10		SIGNAL(High Speed)
11		GROUND
BOTTOM		SIGNAL

SYNC MASTER=K24 MLB			
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BOM Configuration			
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Functional Test Points

Fan Connectors

PP5V_S0	TRUE	PP5V_S0	(NEED 2 TP)
FAN_RT_PWM	TRUE	FAN_RT_PWM	46
FAN_RT_TACH	TRUE	FAN_RT_TACH	46
(NEED TO ADD 3 GND TP)			

MIC_FUNC_TEST

BI_MIC_LO	TRUE	BI_MIC_LO	55 56
BI_MIC_HI	TRUE	BI_MIC_HI	55 56
BI_MIC_SHIELD	TRUE	BI_MIC_SHIELD	55 56

SPEAKER_FUNC_TEST

SPKRAMP_L_N_OUT	TRUE	SPKRAMP_L_N_OUT	54 55
SPKRAMP_L_P_OUT	TRUE	SPKRAMP_L_P_OUT	54 55
SPKRAMP_R_N_OUT	TRUE	SPKRAMP_R_N_OUT	54 55
SPKRAMP_R_P_OUT	TRUE	SPKRAMP_R_P_OUT	54 55
SPKRAMP_SUB_N_OUT	TRUE	SPKRAMP_SUB_N_OUT	54 55
SPKRAMP_SUB_P_OUT	TRUE	SPKRAMP_SUB_P_OUT	54 55

LVDS_FUNC_TEST

PP3V3_LCDVDD_SW_F	TRUE	PP3V3_LCDVDD_SW_F	6 67
PP3V3_S0_LCD_F	TRUE	PP3V3_S0_LCD_F	6 67
PPVOUT_SW_LCDBKLT	TRUE	PPVOUT_SW_LCDBKLT	67 70
BKL_VSYNC	TRUE	BKL_VSYNC	67 70
LVDS_DDC_CLK	TRUE	LVDS_DDC_CLK	8 67
LVDS_DDC_DATA	TRUE	LVDS_DDC_DATA	8 67
LVDS_IG_A_DATA_N<0>	TRUE	LVDS_IG_A_DATA_N<0>	8 67 74
LVDS_IG_A_DATA_P<0>	TRUE	LVDS_IG_A_DATA_P<0>	8 67 74
LVDS_IG_A_DATA_N<1>	TRUE	LVDS_IG_A_DATA_N<1>	8 67 74
LVDS_IG_A_DATA_P<1>	TRUE	LVDS_IG_A_DATA_P<1>	8 67 74
LVDS_IG_A_DATA_N<2>	TRUE	LVDS_IG_A_DATA_N<2>	8 67 74
LVDS_IG_A_DATA_P<2>	TRUE	LVDS_IG_A_DATA_P<2>	8 67 74
LVDS_CONN_A_CLK_F_N	TRUE	LVDS_CONN_A_CLK_F_N	67 79
LVDS_CONN_A_CLK_F_P	TRUE	LVDS_CONN_A_CLK_F_P	67 79
LED_RETURN_1	TRUE	LED_RETURN_1	67 70
BKL_ISEN2	TRUE	BKL_ISEN2	70
BKL_ISEN3	TRUE	BKL_ISEN3	70
LED_RETURN_4	TRUE	LED_RETURN_4	67 70
LED_RETURN_5	TRUE	LED_RETURN_5	67 70
LED_RETURN_6	TRUE	LED_RETURN_6	67 70
(NEED TO ADD 5 GND TP)			

SATA_ODD_CONN

PP5V_SW_ODD	TRUE	PP5V_SW_ODD	(NEED 4 TP)
SMC_ODD_DETECT	TRUE	SMC_ODD_DETECT	36 39
SATA_ODD_D2R_UF_P	TRUE	SATA_ODD_D2R_UF_P	36 79
SATA_ODD_D2R_UF_N	TRUE	SATA_ODD_D2R_UF_N	36 79
SATA_ODD_R2D_P	TRUE	SATA_ODD_R2D_P	36 74
SATA_ODD_R2D_N	TRUE	SATA_ODD_R2D_N	36 74
(NEED TO ADD 4 GND TP)			

SATA_HDD/IR/SIL

PP5V_S0_HDD_FLT	TRUE	PP5V_S0_HDD_FLT	(NEED 3 TP)
SATA_HDD_R2D_P	TRUE	SATA_HDD_R2D_P	36 74
SATA_HDD_R2D_N	TRUE	SATA_HDD_R2D_N	36 74
SATA_HDD_D2R_C_P	TRUE	SATA_HDD_D2R_C_P	36 74
SATA_HDD_D2R_C_N	TRUE	SATA_HDD_D2R_C_N	36 74
SYS_LED_ANODE_R	TRUE	SYS_LED_ANODE_R	36
IR_RX_OUT	TRUE	IR_RX_OUT	36 38
PP5V_S3_IR_R	TRUE	PP5V_S3_IR_R	36
(NEED TO ADD 5 GND TP)			

BATT_POWER_CONN

SMBUS_SMC_BSA_SCL	TRUE	SMBUS_SMC_BSA_SCL	6 42 78
SMBUS_SMC_BSA_SDA	TRUE	SMBUS_SMC_BSA_SDA	6 42 78
SYS_DETECT_L	TRUE	SYS_DETECT_L	57
PPVBAT_G3H_CONN	TRUE	PPVBAT_G3H_CONN	57 58
(NEED 3 TP)			
(NEED TO ADD 4 GND TP)			

BIL_CONN

PP3V42_G3H	TRUE	PP3V42_G3H	6 7
SMBUS_SMC_BSA_SCL	TRUE	SMBUS_SMC_BSA_SCL	6 42 78
SMBUS_SMC_BSA_SDA	TRUE	SMBUS_SMC_BSA_SDA	6 42 78
SMC_BIL_BUTTON_L	TRUE	SMC_BIL_BUTTON_L	39 40 57
SMC_LID_R	TRUE	SMC_LID_R	57
(NEED TO ADD 4 GND TP)			

RIGHT_CLUTCH_CONN

PP5V_S3_BT_CAMERA_F	TRUE	PP5V_S3_BT_CAMERA_F	29
PCIE_AP_D2R_P	TRUE	PCIE_AP_D2R_P	15 29 74
PCIE_AP_D2R_N	TRUE	PCIE_AP_D2R_N	15 29 74
PCIE_AP_R2D_P	TRUE	PCIE_AP_R2D_P	29 74
PCIE_AP_R2D_N	TRUE	PCIE_AP_R2D_N	29 74
PCIE_CLK100M_AP_CONN_P	TRUE	PCIE_CLK100M_AP_CONN_P	29 79
PCIE_CLK100M_AP_CONN_N	TRUE	PCIE_CLK100M_AP_CONN_N	29 79
USB_CAMERA_CONN_P	TRUE	USB_CAMERA_CONN_P	29 79
USB_CAMERA_CONN_N	TRUE	USB_CAMERA_CONN_N	29 79
PP5V_WLAN	TRUE	PP5V_WLAN	6 29
PCIE_WAKE_L	TRUE	PCIE_WAKE_L	15 24 29
SMBUS_SMC_A_S3_SCL	TRUE	SMBUS_SMC_A_S3_SCL	6 42 78
SMBUS_SMC_A_S3_SDA	TRUE	SMBUS_SMC_A_S3_SDA	6 42 78
USB_BT_CONN_P	TRUE	USB_BT_CONN_P	29 79
USB_BT_CONN_N	TRUE	USB_BT_CONN_N	29 79
AP_CLKREQ_O_L	TRUE	AP_CLKREQ_O_L	29
AP_RESET_CONN_L	TRUE	AP_RESET_CONN_L	29
(NEED TO ADD 6 GND TP)			

IPD_FLEX_CONN

PP3V3_S3	TRUE	PP3V3_S3	6 7
PP18V5_S3	TRUE	PP18V5_S3	6 48
Z2_CS_L	TRUE	Z2_CS_L	47 48
Z2_DEBUG3	TRUE	Z2_DEBUG3	47 48
Z2_MOSI	TRUE	Z2_MOSI	47 48
Z2_SCLK	TRUE	Z2_SCLK	47 48
Z2_BOOST_EN	TRUE	Z2_BOOST_EN	48
Z2_HOST_INTN	TRUE	Z2_HOST_INTN	47 48
Z2_CLKIN	TRUE	Z2_CLKIN	47 48
Z2_KEY_ACT_L	TRUE	Z2_KEY_ACT_L	47 48
Z2_RESET	TRUE	Z2_RESET	47 48
PSOC_MISO	TRUE	PSOC_MISO	47 48
PSOC_MOSI	TRUE	PSOC_MOSI	47 48
PSOC_SCLK	TRUE	PSOC_SCLK	47 48
SMBUS_SMC_A_S3_SDA	TRUE	SMBUS_SMC_A_S3_SDA	6 42 78
SMBUS_SMC_A_S3_SCL	TRUE	SMBUS_SMC_A_S3_SCL	6 42 78
PSOC_F_CS_L	TRUE	PSOC_F_CS_L	47 48
PICKB_L	TRUE	PICKB_L	47 48
(NEED TO ADD 2 GND TP)			

KEYBOARD_CONN

PP3V3_S3	TRUE	PP3V3_S3	6 7
PP3V42_G3H	TRUE	PP3V42_G3H	6 7
WS_KBD1	TRUE	WS_KBD1	47
WS_KBD2	TRUE	WS_KBD2	47
WS_KBD3	TRUE	WS_KBD3	47
WS_KBD4	TRUE	WS_KBD4	47
WS_KBD5	TRUE	WS_KBD5	47
WS_KBD6	TRUE	WS_KBD6	47
WS_KBD7	TRUE	WS_KBD7	47
WS_KBD8	TRUE	WS_KBD8	47
WS_KBD9	TRUE	WS_KBD9	47
WS_KBD10	TRUE	WS_KBD10	47
WS_KBD11	TRUE	WS_KBD11	47
WS_KBD12	TRUE	WS_KBD12	47
WS_KBD13	TRUE	WS_KBD13	47
WS_KBD14	TRUE	WS_KBD14	47
WS_KBD15_CAP	TRUE	WS_KBD15_CAP	47
WS_KBD16_NUM	TRUE	WS_KBD16_NUM	47
WS_KBD17	TRUE	WS_KBD17	47
WS_KBD18	TRUE	WS_KBD18	47
WS_KBD19	TRUE	WS_KBD19	47
WS_KBD20	TRUE	WS_KBD20	47
WS_KBD21	TRUE	WS_KBD21	47
WS_KBD22	TRUE	WS_KBD22	47
WS_KBD23	TRUE	WS_KBD23	47
WS_KBD_ONOFF_L	TRUE	WS_KBD_ONOFF_L	47
WS_LEFT_SHIFT_KBD	TRUE	WS_LEFT_SHIFT_KBD	47
WS_LEFT_OPTION_KBD	TRUE	WS_LEFT_OPTION_KBD	47
WS_CONTROL_KBD	TRUE	WS_CONTROL_KBD	47
(NEED TO ADD 2 GND TP)			

KBD_BACKLIGHT_CONN

KBDLED_ANODE	TRUE	KBDLED_ANODE	48
SMC_KBDLED_PRESENT_L	TRUE	SMC_KBDLED_PRESENT_L	48
(NEED TO ADD 1 GND TP)			

T57_CONN

PP5V_S3	TRUE	PP5V_S3	6 7
PP3V3_S3	TRUE	PP3V3_S3	6 7
T57_PWR_EN	TRUE	T57_PWR_EN	18
T57_RESET	TRUE	T57_RESET	18
USB_T57_N	TRUE	USB_T57_N	38 75
USB_T57_P	TRUE	USB_T57_P	38 75
(NEED TO ADD 5 GND TP)			

DEBUG_VOLTAGE

PPVCORE_S0_CPU	TRUE	PPVCORE_S0_CPU	7 43
PPVCORE_S0_MCP	TRUE	PPVCORE_S0_MCP	7 43
PP1V2_ENET	TRUE	PP1V2_ENET	7
PP1V05_S0	TRUE	PP1V05_S0	7 65
PP1V5_S0	TRUE	PP1V5_S0	7 65 79
PP1V8_S0	TRUE	PP1V8_S0	7
PP3V3_S0	TRUE	PP3V3_S0	7 65 79
PP5V_S0	TRUE	PP5V_S0	6 7 65
PP3V3_S3	TRUE	PP3V3_S3	6 7
PP5V_S3	TRUE	PP5V_S3	6 7
PP0V9_S5	TRUE	PP0V9_S5	7
PP3V3_S5	TRUE	PP3V3_S5	7 65 79
PP3V42_G3H	TRUE	PP3V42_G3H	6 7
PPBUS_G3H	TRUE	PPBUS_G3H	7 43
PP3V3_ENET	TRUE	PP3V3_ENET	7
PP5V_WLAN	TRUE	PP5V_WLAN	6 29
PP5V_SW_ODD	TRUE	PP5V_SW_ODD	6 8
PP5V_S0_HDD_FLT	TRUE	PP5V_S0_HDD_FLT	6 36
PP18V5_S3	TRUE	PP18V5_S3	6 48
PP3V3_S0_LCD_F	TRUE	PP3V3_S0_LCD_F	6 67
PP3V3_LCDVDD_SW_F	TRUE	PP3V3_LCDVDD_SW_F	6 67
PP4V5_AUDIO_ANALOG	TRUE	PP4V5_AUDIO_ANALOG	51
PP1V5R1V35_S3	TRUE	PP1V5R1V35_S3	7 79
SMC_PM_G2_EN	TRUE	SMC_PM_G2_EN	39 65
PM_SLP_S4_L	TRUE	PM_SLP_S4_L	18 39 40 65
PM_SLP_S3_L	TRUE	PM_SLP_S3_L	18 39 65 69
(NEED TO ADD 6 GND TP)			

SPI_DEBUG_CONN


PP3V42_G3H	TRUE	PP3V42_G3H	6 7
SPI_CS0_L	TRUE	SPI_CS0_L	41 75
SPI_CLK	TRUE	SPI_CLK	41 75
SPI_MOSI	TRUE	SPI_MOSI	41 75
SPI_MISO	TRUE	SPI_MISO	18 41 75
SPIROM_USE_MLB	TRUE	SPIROM_USE_MLB	18 41 50

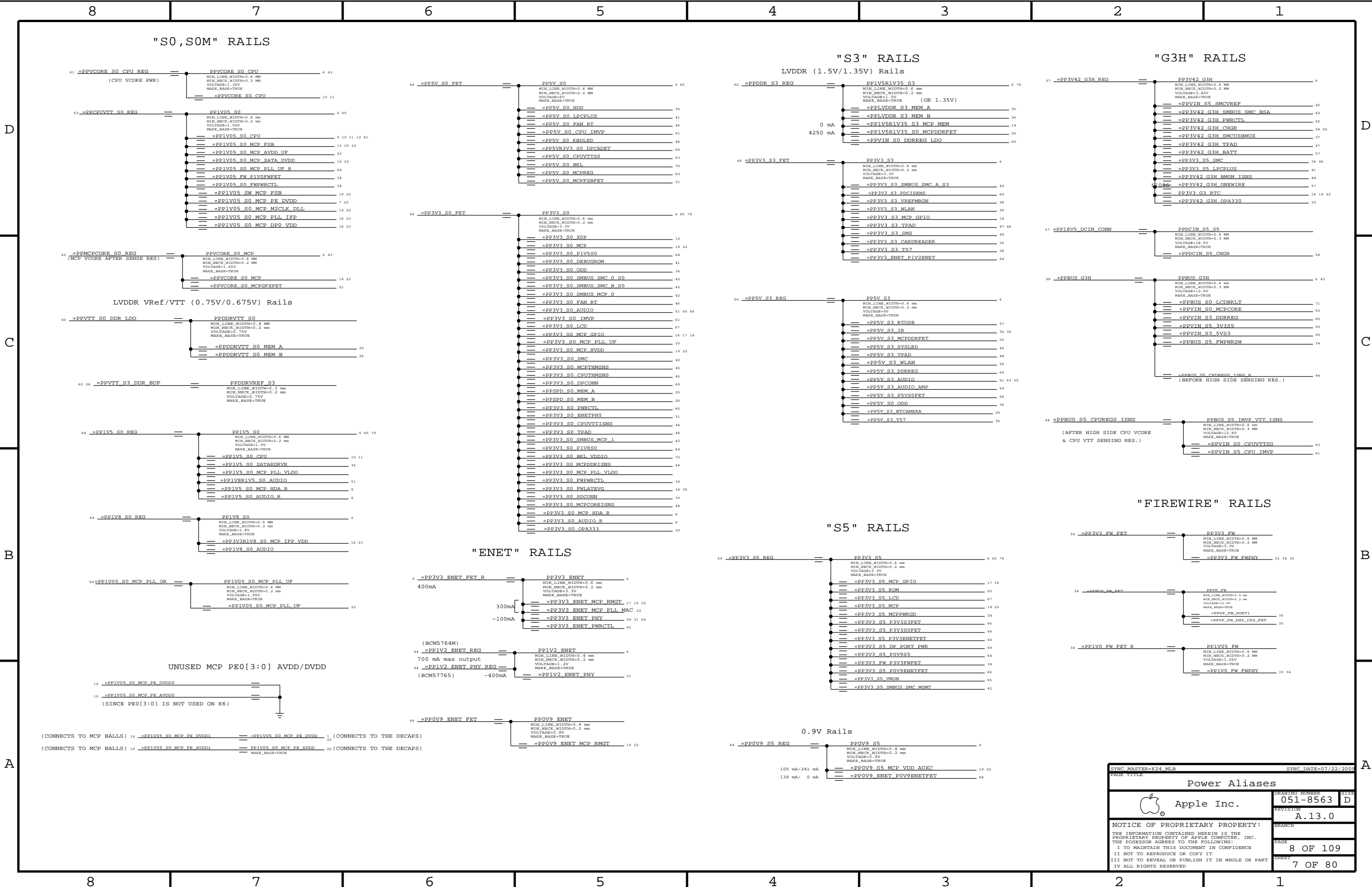
DC_POWER_CONN

PP18V5_DCIN_FUSE	TRUE	PP18V5_DCIN_FUSE	67
ADAPTER_SENSE	TRUE	ADAPTER_SENSE	67
(NEED TO ADD 4 GND TP)			

FSB_SIGNALS_WITH_NOTEST

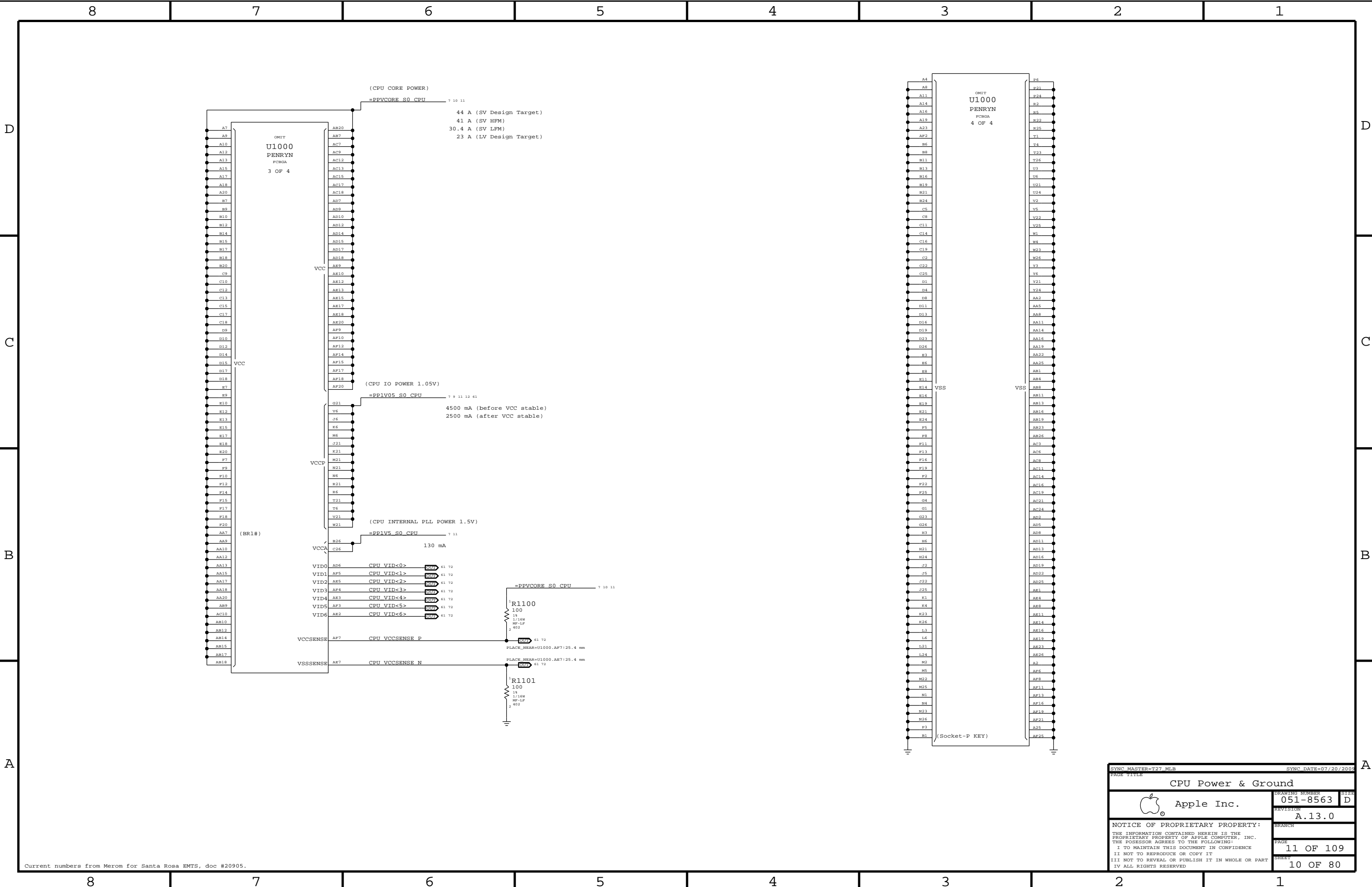
NO_TEST=TRUE	FSB_A_L<35..3>	9 13 72
NO_TEST=TRUE	FSB_ADS_L	9 13 72
NO_TEST=TRUE	FSB_ADSTB_L<1..0>	9 13 72
NO_TEST=TRUE	FSB_D_L<63..0>	9 13 72
NO_TEST=TRUE	FSB_DINV_L<3..0>	9 13 72
NO_TEST=TRUE	FSB_DSTB_L_N<3..0>	9 13 72
NO_TEST=TRUE	FSB_DSTB_L_P<3..0>	9 13 72
NO_TEST=TRUE	FSB_HIT_L	9 13 72
NO_TEST=TRUE	FSB_HITM_L	9 13 72
NO_TEST=TRUE	FSB_LOCK_L	9 13 72
NO_TEST=TRUE	FSB_REQ_L<4..0>	9 13 72


SYNC MASTER=K24_MLB			
PAGE TITLE			
FUNC TEST			
 Apple Inc.		DRAWING NUMBER	051-8563
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SYNC MASTER=K24 MLB		SYNC DATE=07/22/2009	
PAGE TITLE		PAGE	
Power Aliases		DRAWING NUMBER	051-8563
Apple Inc.		REVISION	A.13.0
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SYNC MASTER=T27 MLB		SYNC DATE=07/20/2005	
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CPU Power & Ground			
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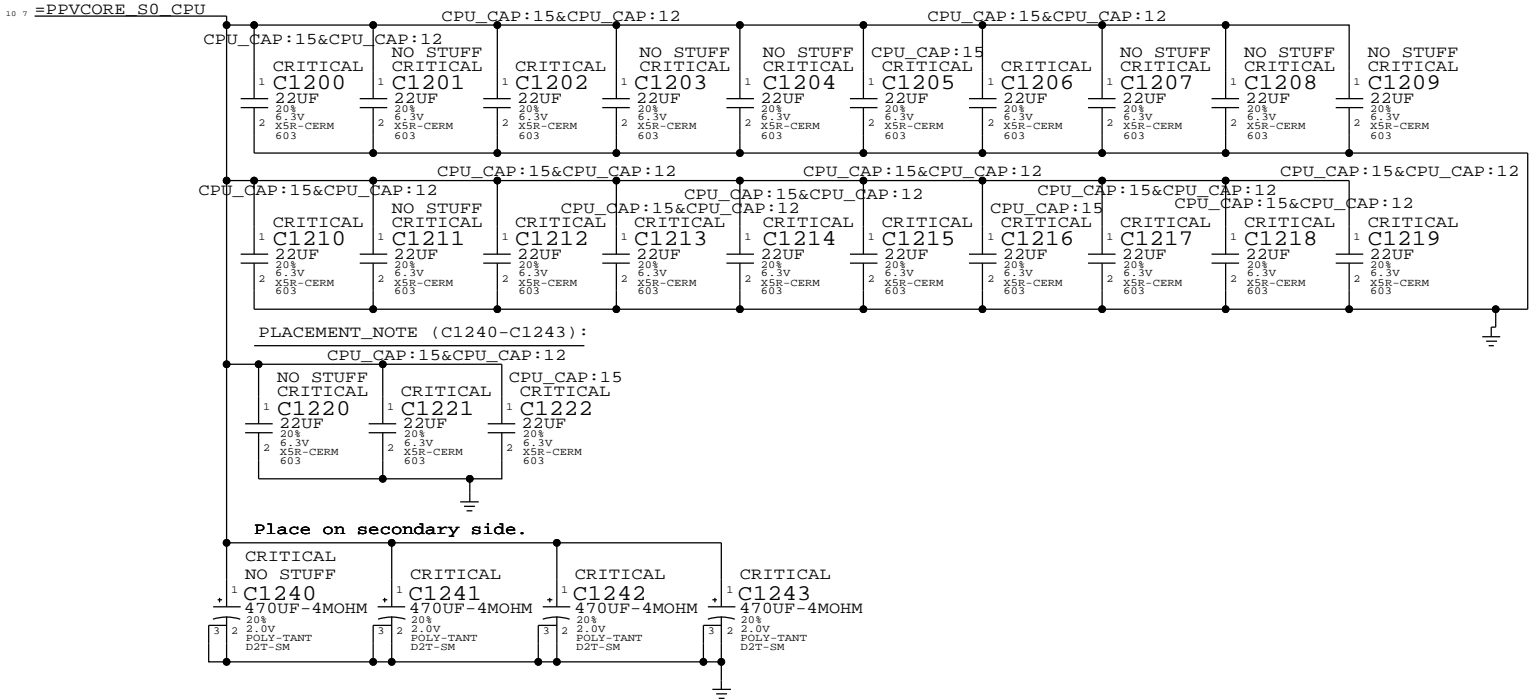
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CPU VCore HF and Bulk Decoupling

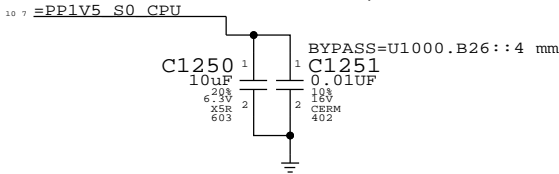
4X 330UF. 20X 22UF 0805

PLACEMENT_NOTE (C1200-C1219):
Place inside socket cavity on secondary side.



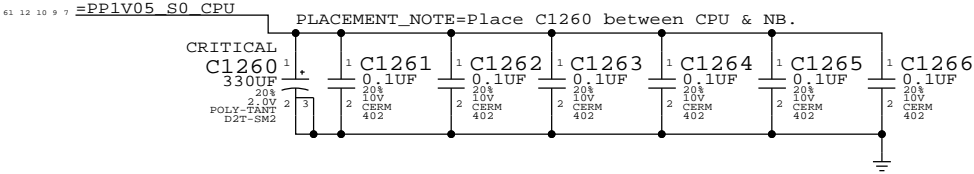
VCCA (CPU AVdd) DECOUPLING


1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC MASTER=T27 MLB		SYNC DATE=11/23/2009	
PAGE TITLE			
CPU Decoupling			
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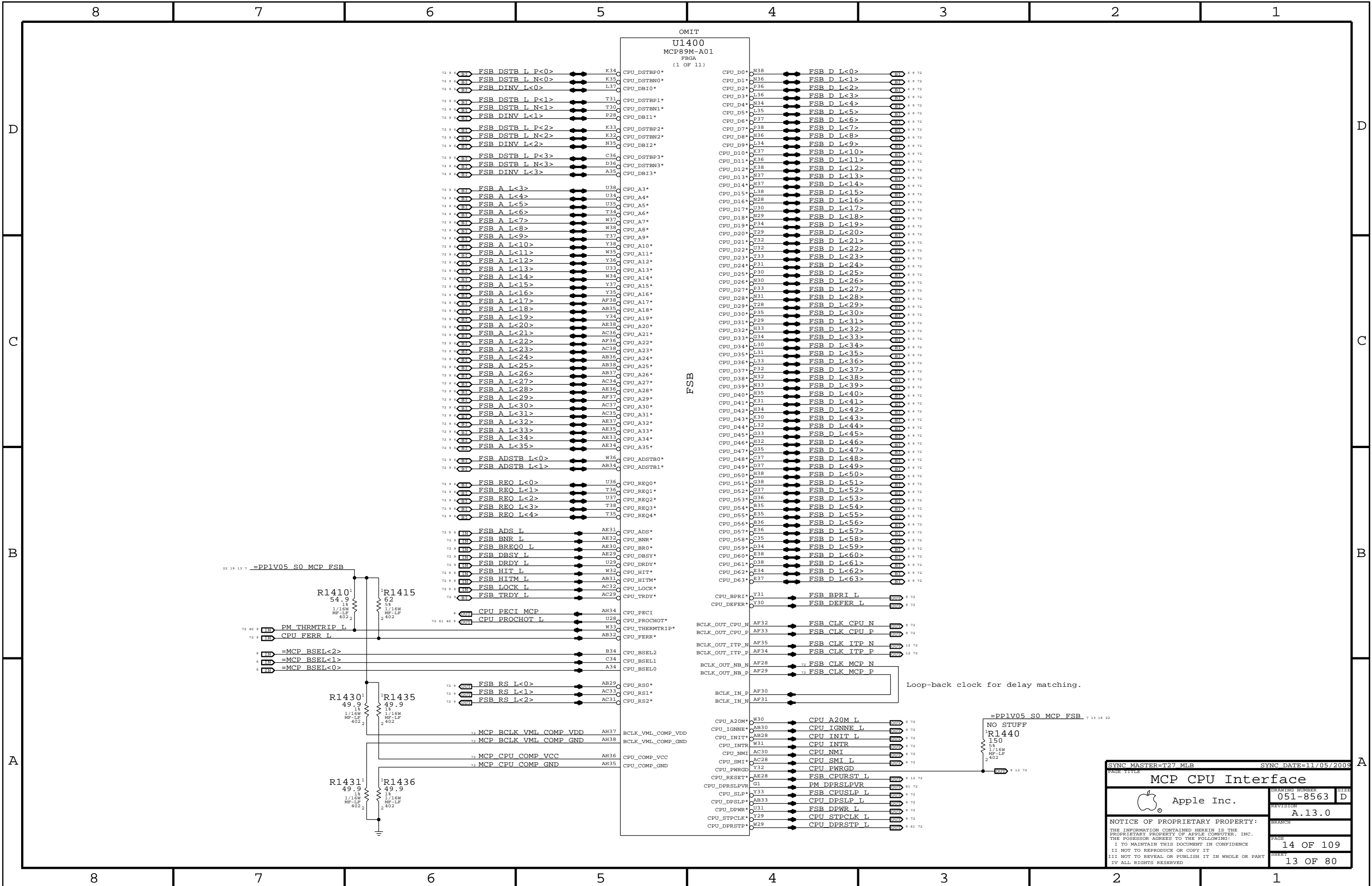
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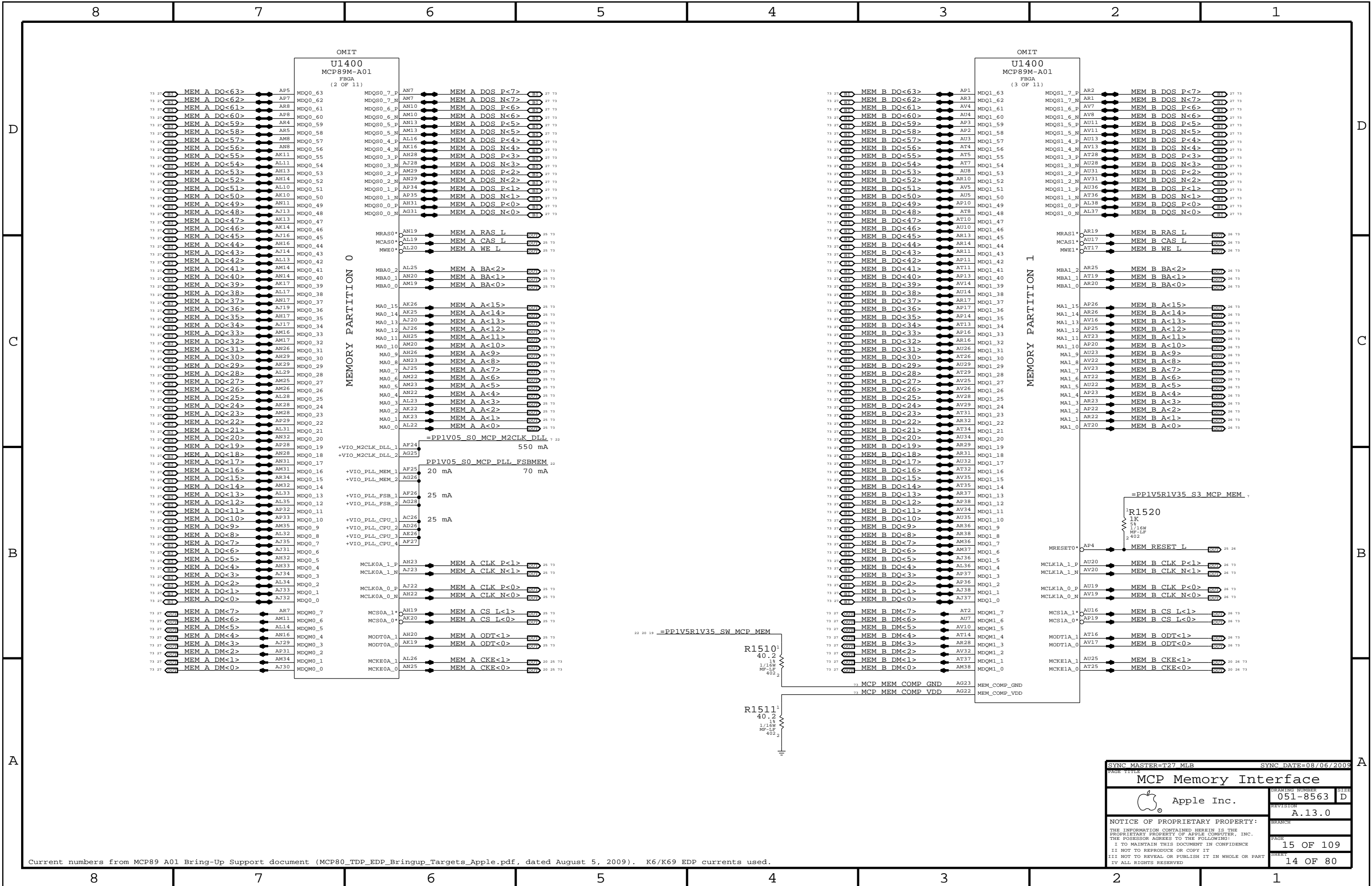
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B

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Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

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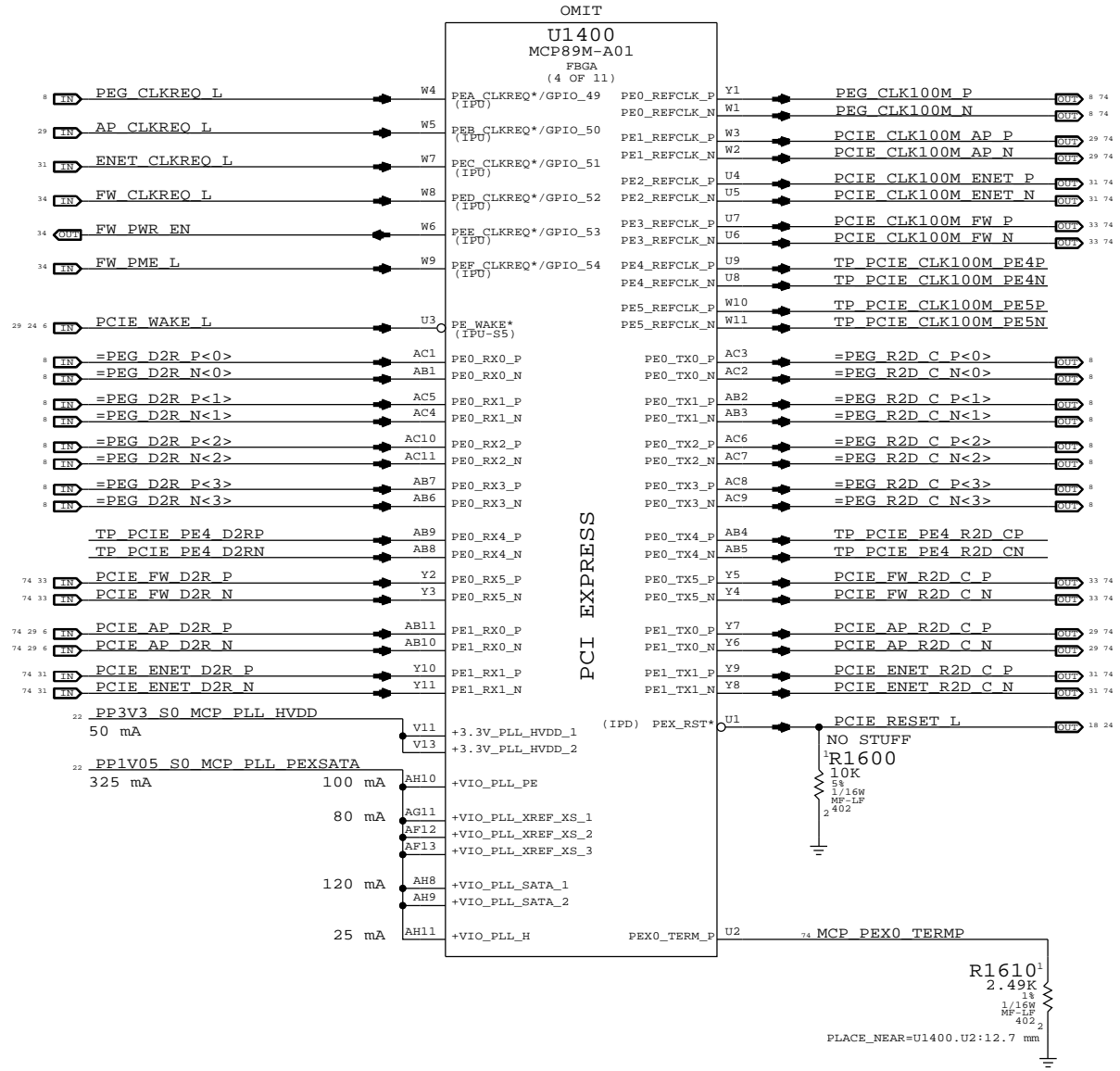
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PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
PE1 ports are Gen1-only. 2 RCs: x1, x1

If PE0[3:0] are not used,
+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PE0[4:5] and PE1[0:1] are not used,
+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND

D

C

B

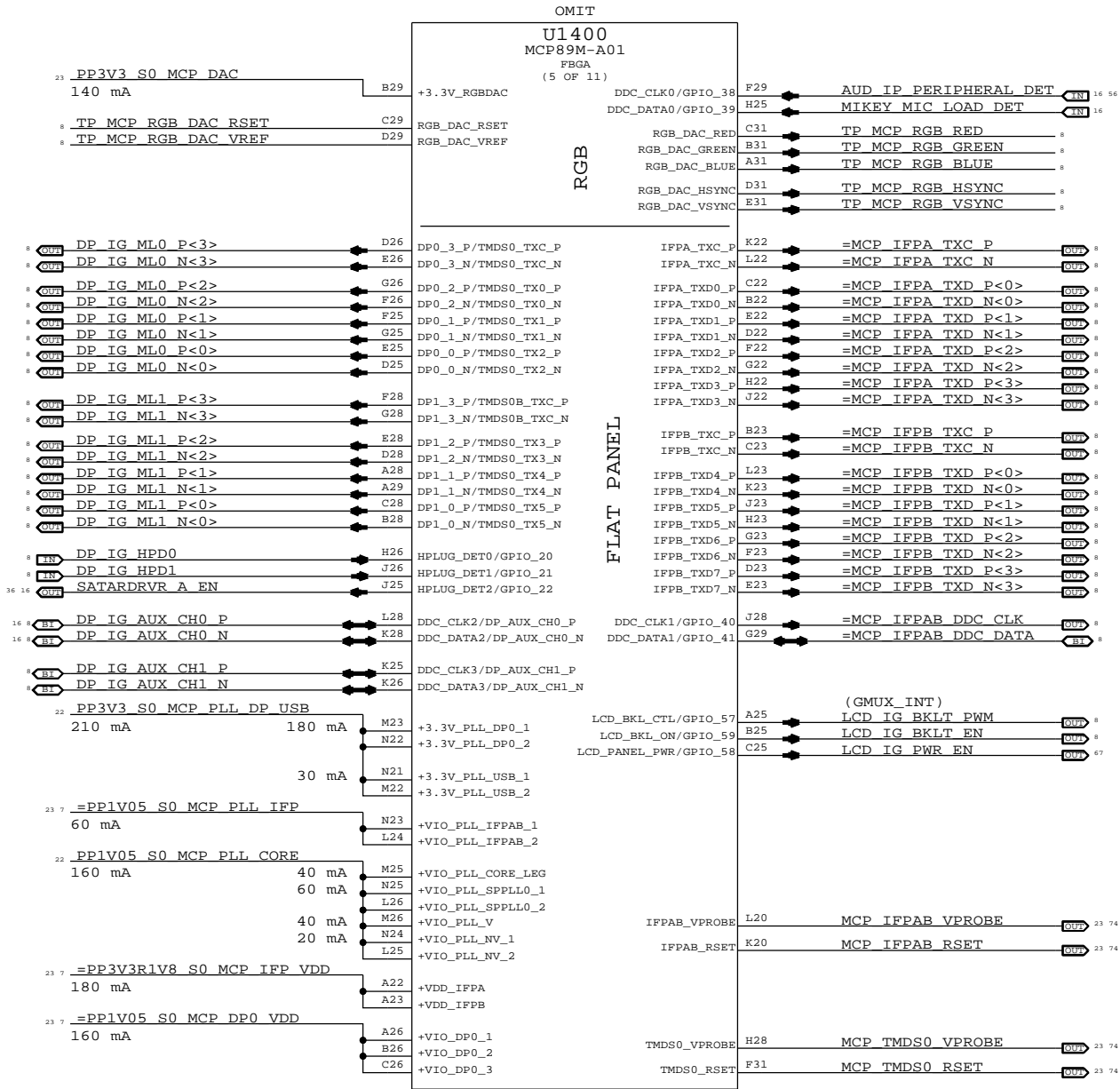
A

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NOTE: 100K pull-downs required if
HPLUG_DET0/HPLUG_DET1 are not used.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).
Connect +3.3V_RGBDAC pin to GND.

NOTE: No Composite/S-Video/Component Video support on MCP89

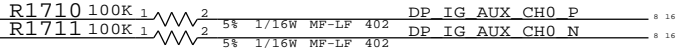
Interface Mode		
MCP Signal	TMDS/HDMI	LVDS
=MCP_IFPA_TXC_P/N	TMDS_IG_TXC_P/N	LVDS_IG_A_CLK_P/N
=MCP_IFPA_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	LVDS_IG_A_DATA_P/N<0>
=MCP_IFPA_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	LVDS_IG_A_DATA_P/N<1>
=MCP_IFPA_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	LVDS_IG_A_DATA_P/N<2>
=MCP_IFPA_TXD_P/N<3>	(UNUSED)	LVDS_IG_A_DATA_P/N<3>
=MCP_IFPB_TXC_P/N	(UNUSED)	LVDS_IG_B_CLK_P/N
=MCP_IFPB_TXD_P/N<0>	TMDS_IG_TXD_P/N<3>	LVDS_IG_B_DATA_P/N<0>
=MCP_IFPB_TXD_P/N<1>	TMDS_IG_TXD_P/N<4>	LVDS_IG_B_DATA_P/N<1>
=MCP_IFPB_TXD_P/N<2>	TMDS_IG_TXD_P/N<5>	LVDS_IG_B_DATA_P/N<2>
=MCP_IFPB_TXD_P/N<3>	(UNUSED)	LVDS_IG_B_DATA_P/N<3>
=MCP_IFPAB_DDC_CLK	TMDS_IG_DDC_CLK	LVDS_IG_DDC_CLK
=MCP_IFPAB_DDC_DATA	TMDS_IG_DDC_DATA	LVDS_IG_DDC_DATA

LVDS: Power +VDD_IFPx at 1.8V

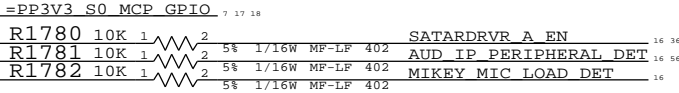
TMDS: Power +VDD_IFPx at 3.3V

DDC Mode Pull-downs


NOTE: DP_AUX_CH1 also requires pull-downs if used for dual-mode DisplayPort (DP++). If unused no pulls are necessary, if used for TMDS/HDMI only then only pull-ups are necessary.

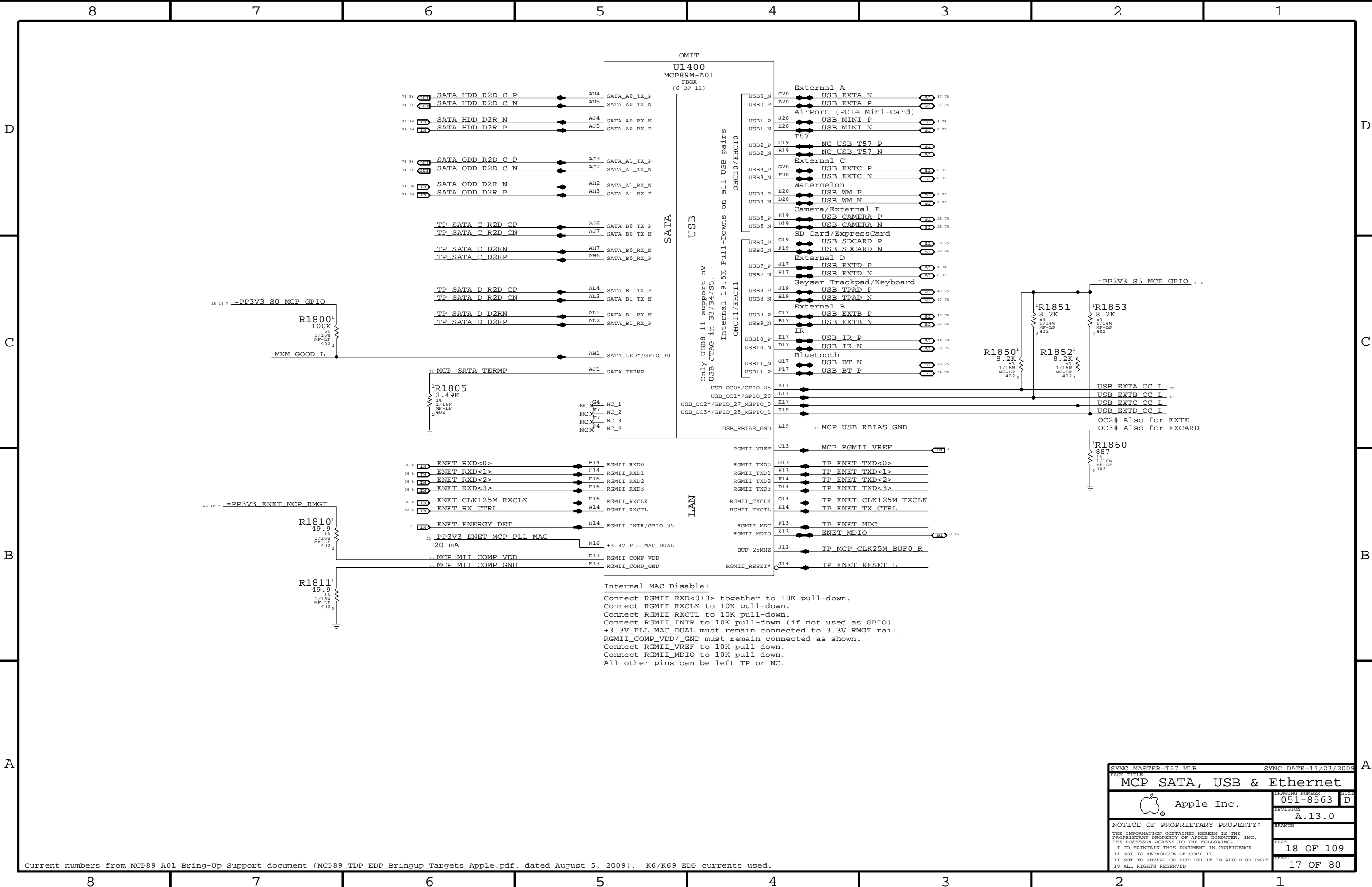


GPIO Pull-Ups



Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB		SYNC DATE=11/05/2009	
PAGE TITLE			
MCP Graphics			
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SYNC MASTER=T27 MLB

SYNC DATE=11/23/2009

MCP SATA, USB & Ethernet

Apple Inc.

051-8563

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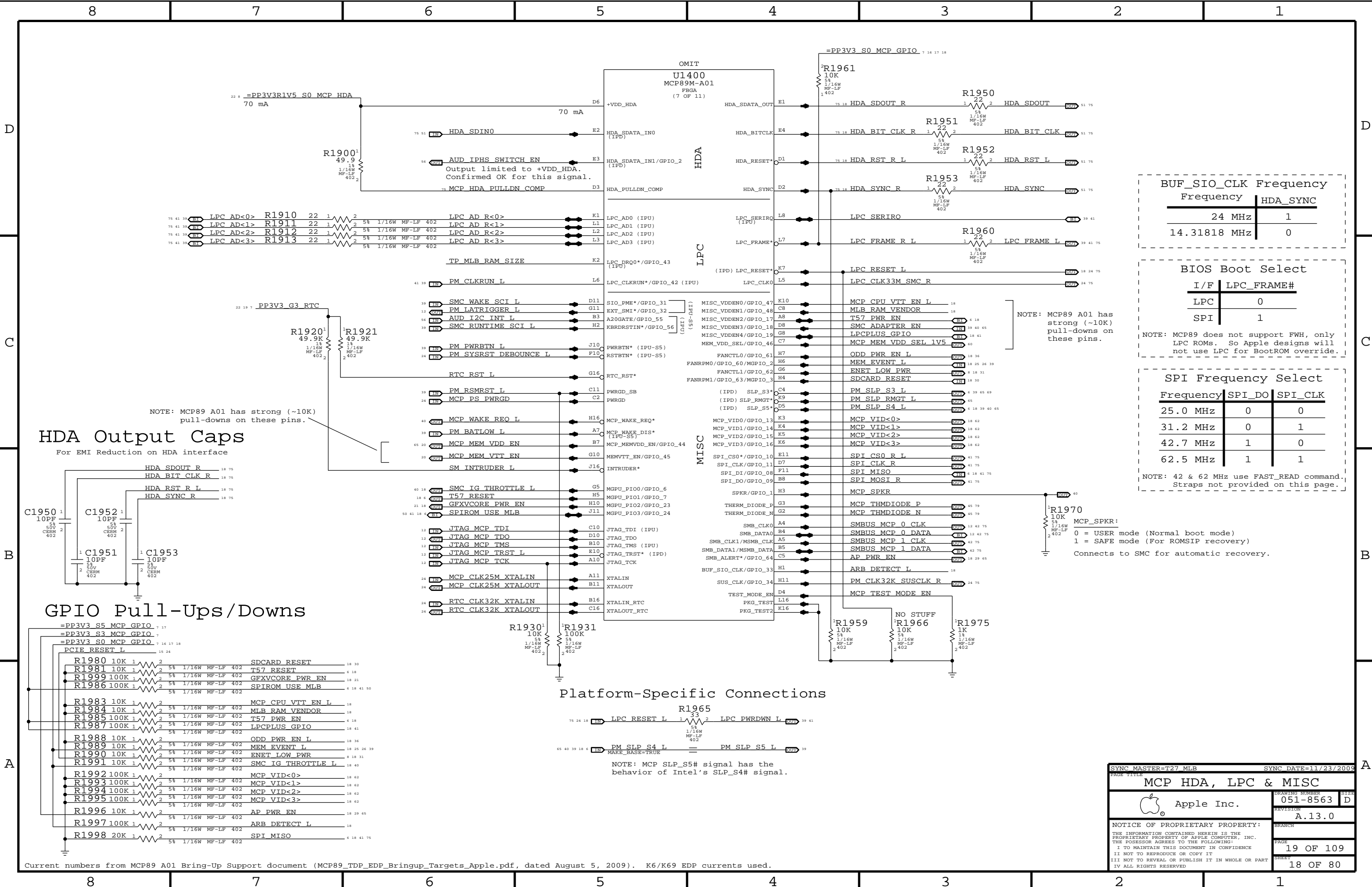
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BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select	
I/F	LPC_FRAME#
LPC	0
SPI	1

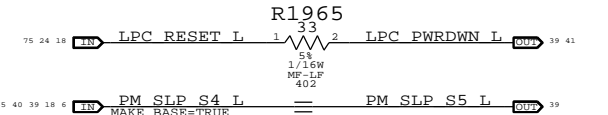
SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 Mhz use FAST_READ command. Straps not provided on this page.

NOTE: MCP89 A01 has strong (~10K) pull-downs on these pins.

MCP_SPKR:
0 = USER mode (Normal boot mode)
1 = SAFE mode (For ROMSIP recovery)
Connects to SMC for automatic recovery.

Platform-Specific Connections



NOTE: MCP SLP_S5# signal has the behavior of Intel's SLP_S4# signal.

SYNC MASTER=T27 MLB

SYNC DATE=11/23/2009

MCP HDA, LPC & MISC

Apple Inc.

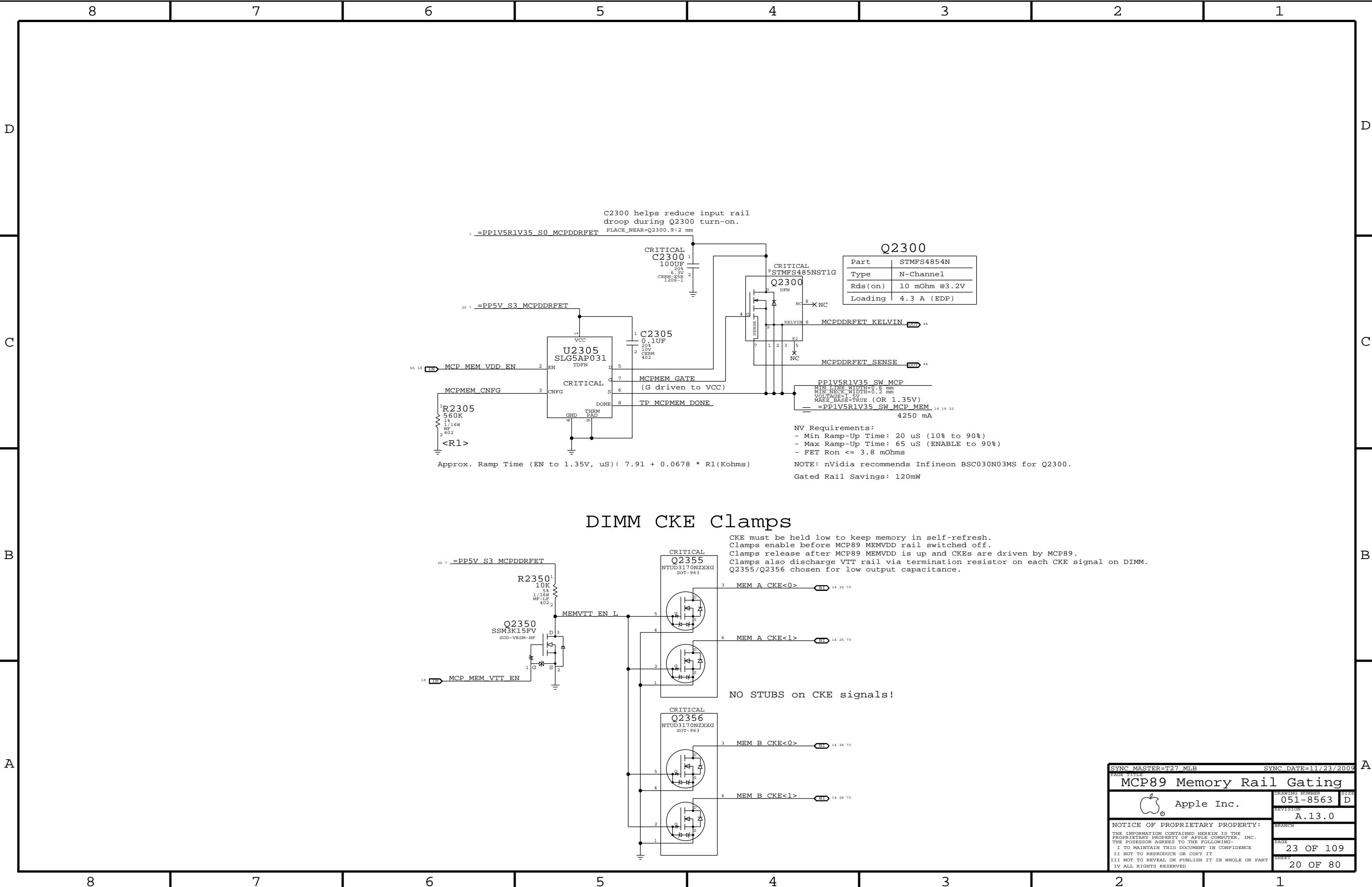
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Part	STMFS4854N
Type	N-Channel
Rds(on)	10 mOhm @3.2V
Loading	4.3 A (EDP)


NV Requirements:
- Min Ramp-Up Time: 20 uS (10% to 90%)
- Max Ramp-Up Time: 65 uS (ENABLE to 90%)
- FET Ron <= 3.8 mOhms

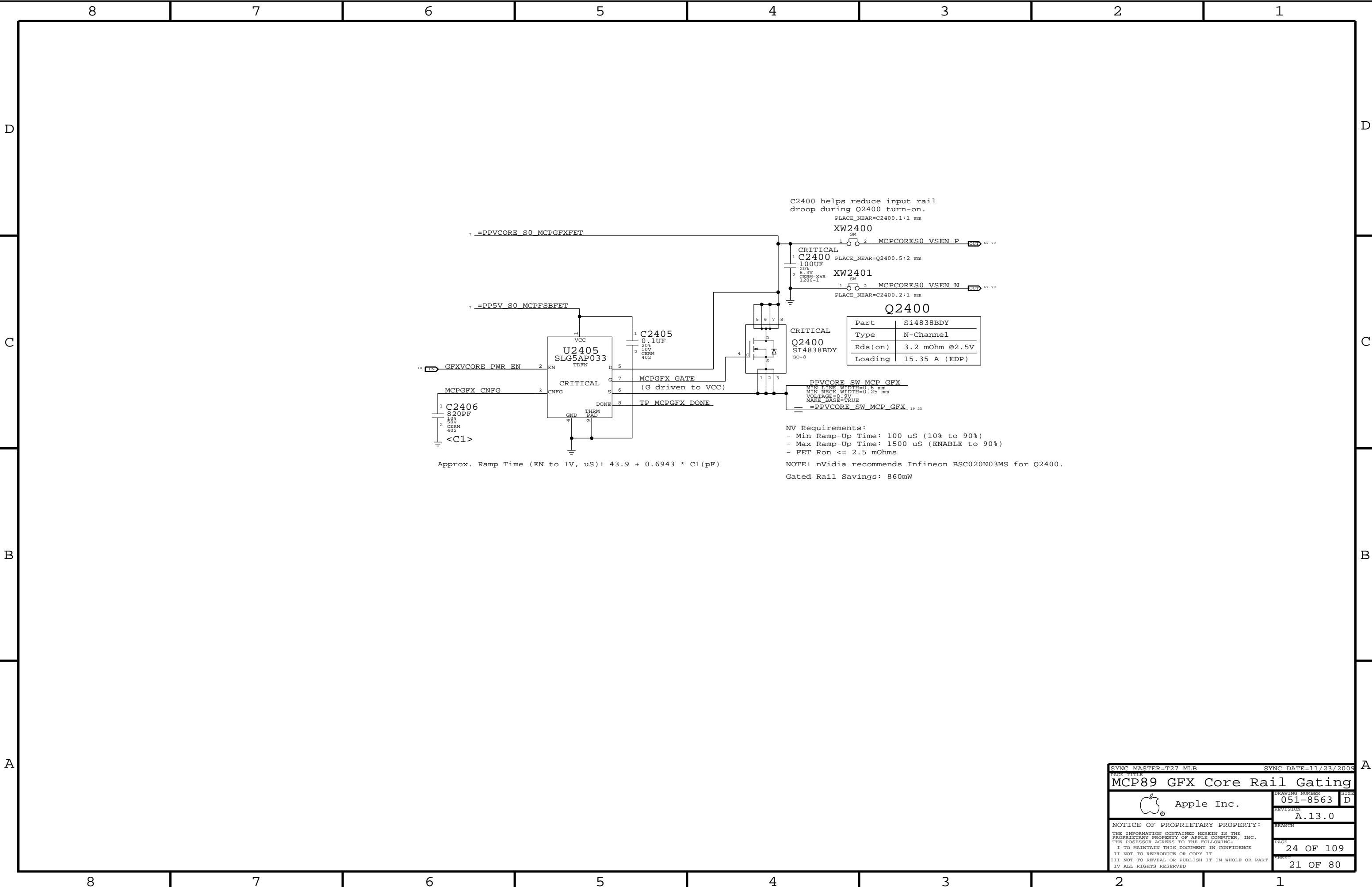
NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.
Gated Rail Savings: 120mW

DIMM CKE Clamps

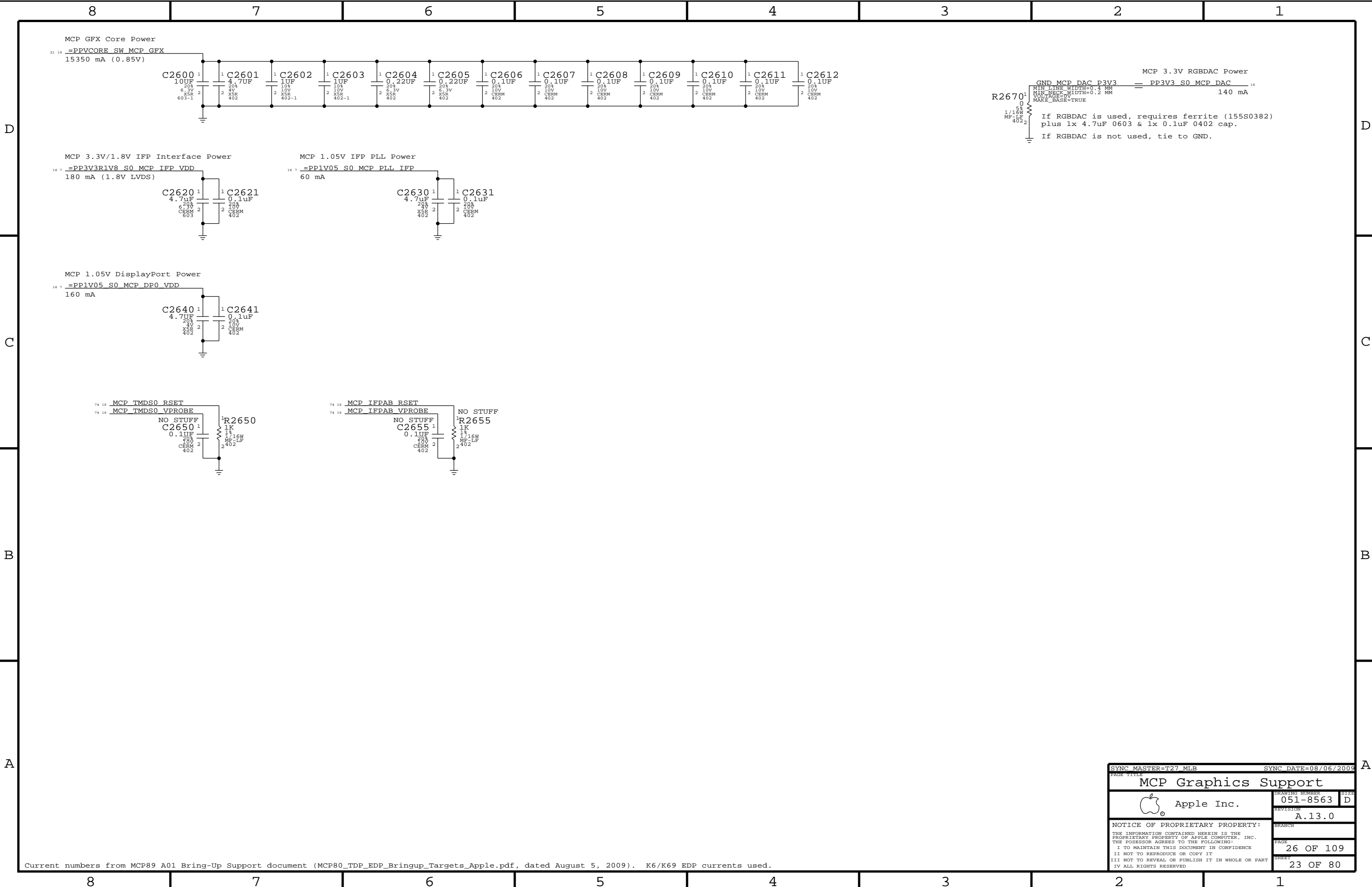
CKE must be held low to keep memory in self-refresh.
Clamps enable before MCP89 MEMVDD rail switched off.
Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
Q2355/Q2356 chosen for low output capacitance.

NO STUBS on CKE signals!


SYNC MASTER=T27 MLB		SYNC DATE=11/23/2009	
PAGE TITLE			
MCP89 Memory Rail Gating			
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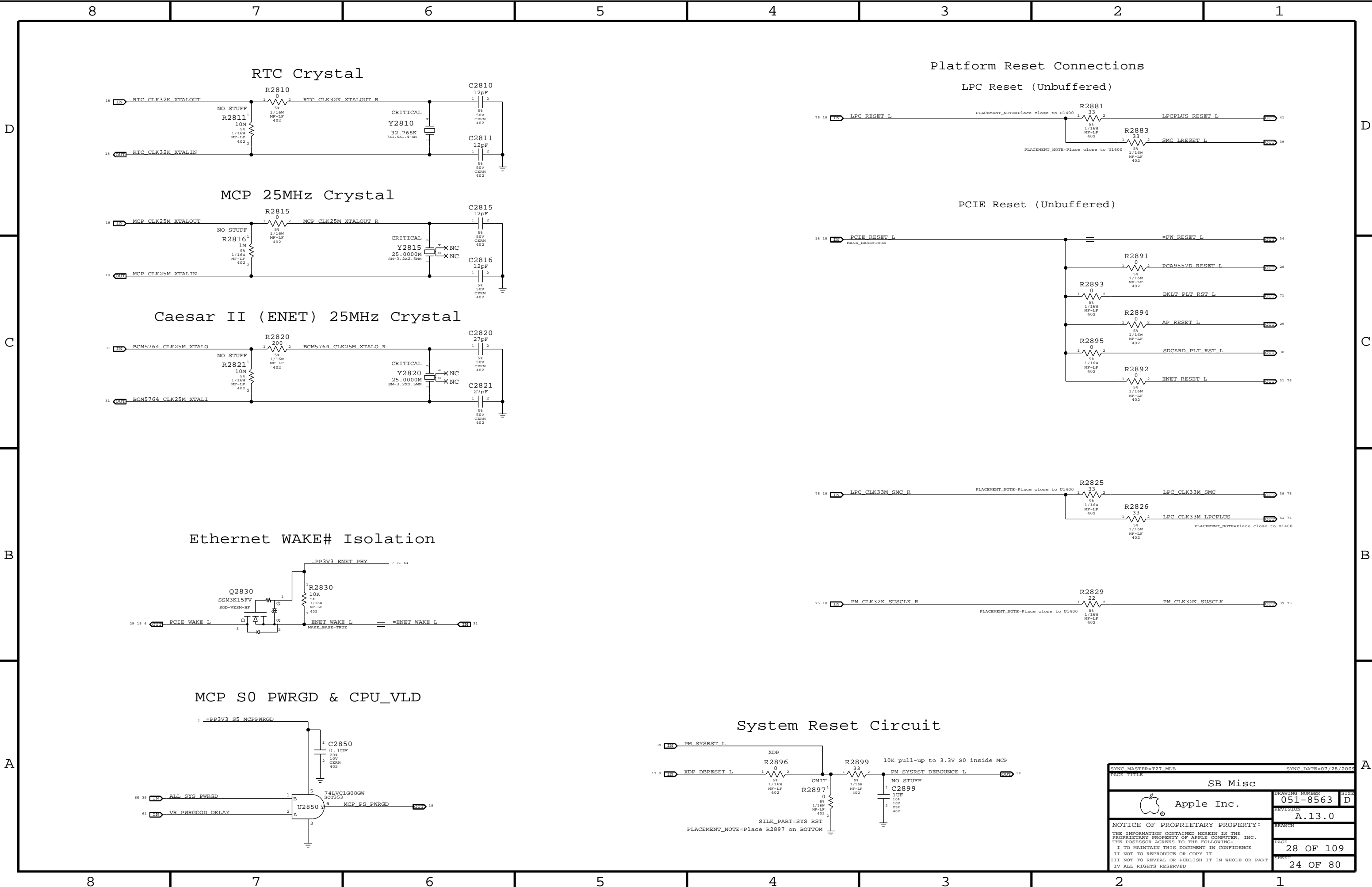




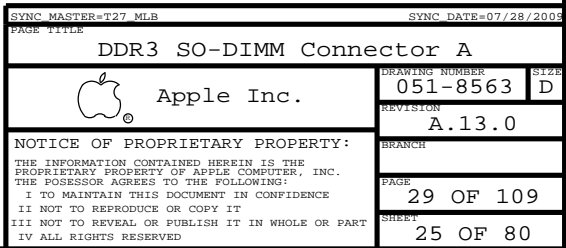


Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27_MLB		SYNC DATE=08/06/2009	
PAGE TITLE			
MCP Graphics Support		Drawing Number	
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		REVISION	
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SB Misc		051-8563		D	
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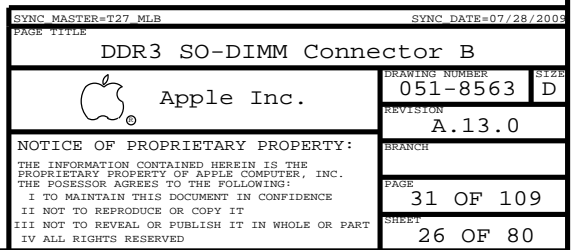
- =PPLVDDR_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

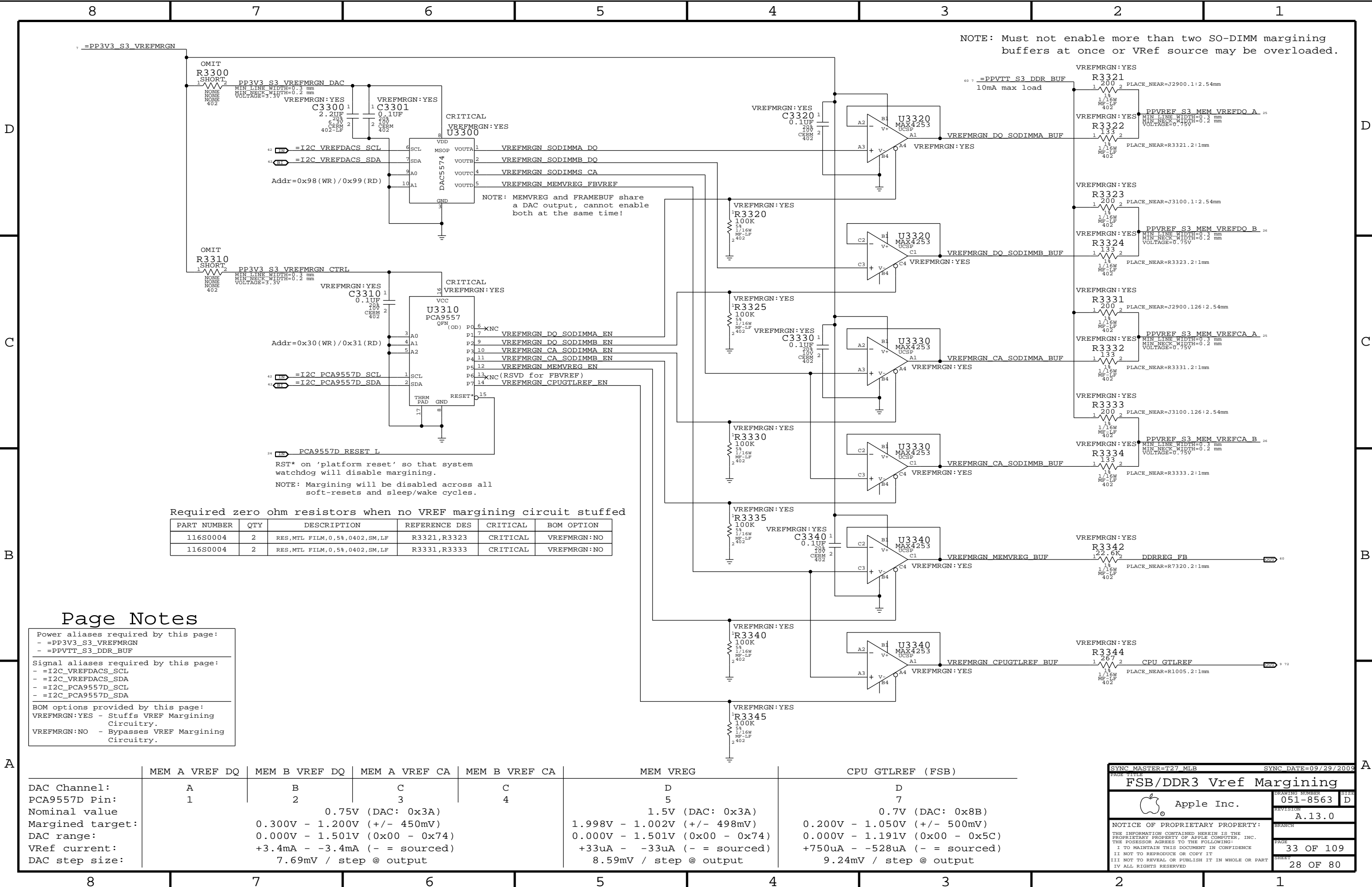
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

(NONE)



<



Page Notes

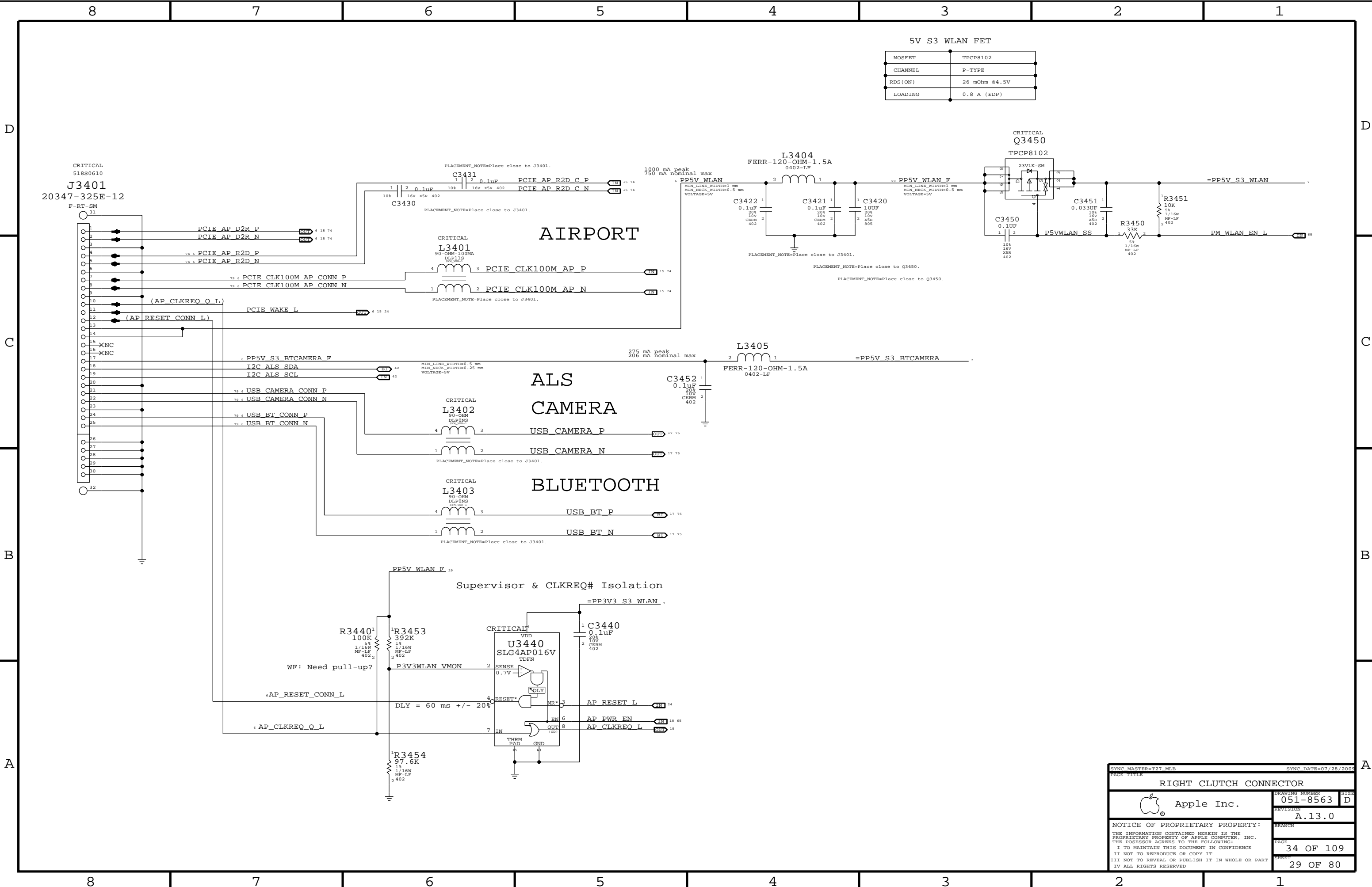
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA


BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	7
Nominal value			0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:			0.300V - 1.200V (+/- 450mV)		1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:			0.000V - 1.501V (0x00 - 0x74)		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:			+3.4mA - -3.4mA (- = sourced)		+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:			7.69mV / step @ output		8.59mV / step @ output	9.24mV / step @ output

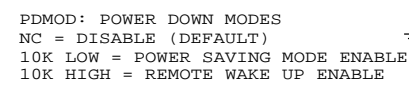
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FSB/DDR3 Vref Margining		051-8563		A.13.0	
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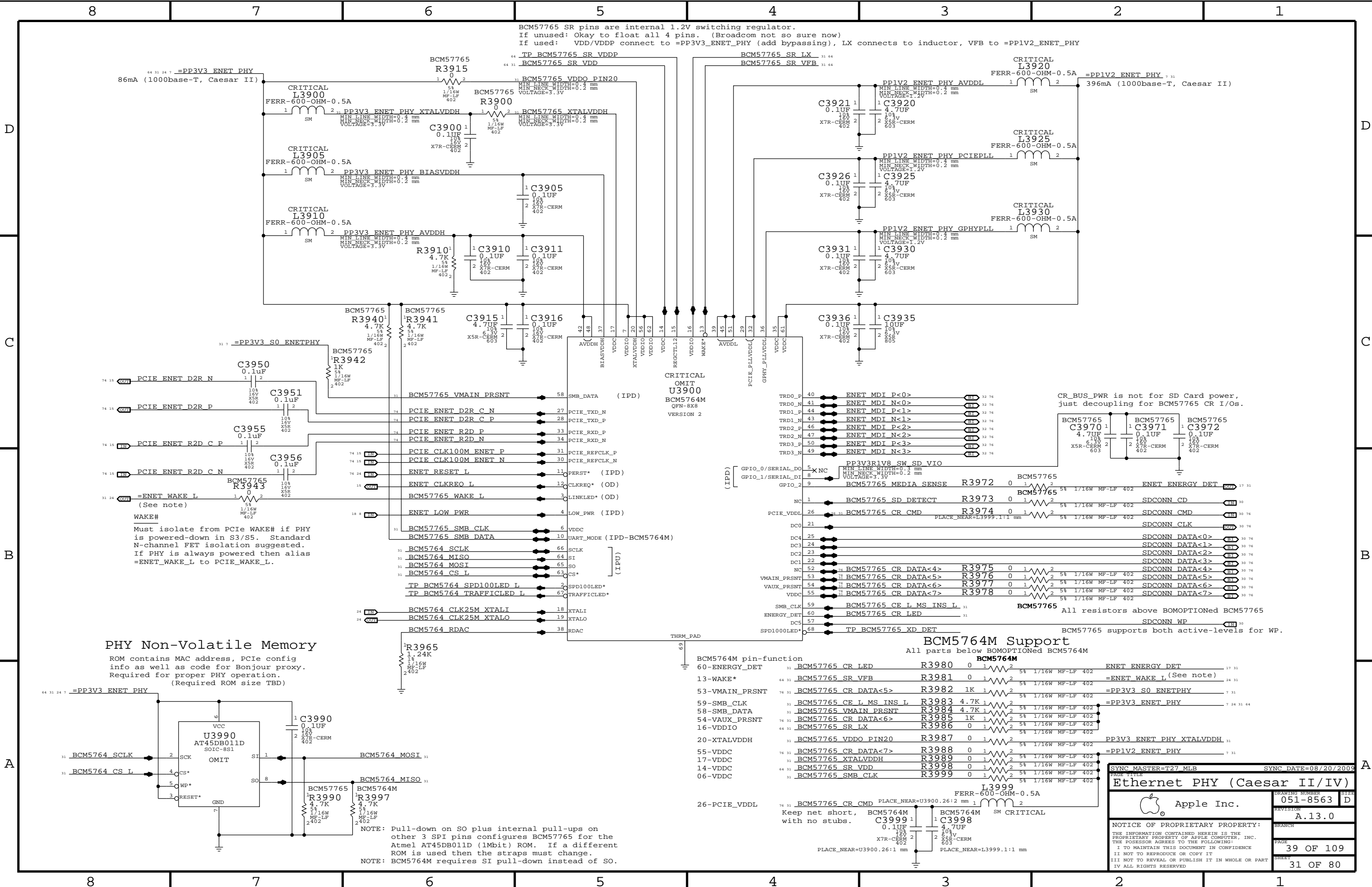
5V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

SYNC MASTER=T27 MLB		SYNC DATE=07/28/2005	
PAGE TITLE			
RIGHT CLUTCH CONNECTOR			
 Apple Inc.	DRAWING NUMBER	051-8563	SIZE
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Time	Signal	Value	Frequency	Period	Phase	Signal	Value
76.31	SDCONN DATA<0>	R3550	0	1/16W	MF-LF	402	SD D<0>
76.31	SDCONN DATA<1>	R3551	0	1/16W	MF-LF	402	SD D<1>
76.31	SDCONN DATA<2>	R3552	0	1/16W	MF-LF	402	SD D<2>
76.31	SDCONN DATA<3>	R3553	0	1/16W	MF-LF	402	SD D<3>
76.31	SDCONN DATA<4...7>						SD D<4...7>
76.31	SDCONN CLK	R3554	0	1/16W	MF-LF	402	SD CLK
76.31	SDCONN CMD	R3556	0	1/16W	MF-LF	402	SD CMD
76.31	SDCONN WP						SD WP
76.31	SDCONN CD						SD CD L



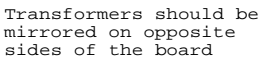
SYNC MASTER=T27 MLE		SYNC DATE=09/30/2009	
PAGE TITLE			
SecureDigital Card Reader			
 Apple Inc.		DRAWING NUMBER	SIZE
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PAGE		35 OF 109	
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Signal aliases required by this page:
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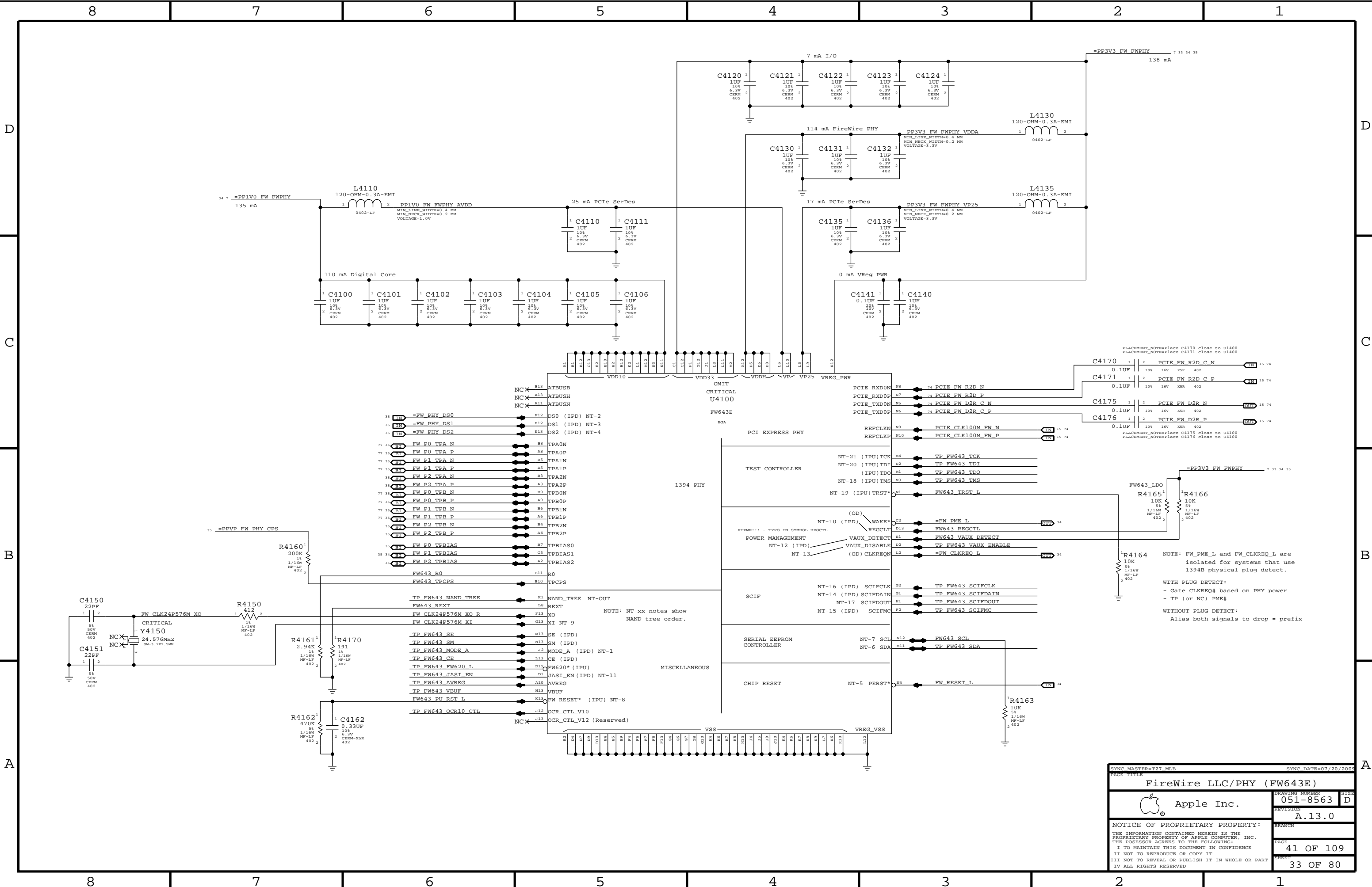
BOM options provided by this page:
(NONE)




```
D4000.1:    PLACE_NEAR=T4000.6:4 mm
D4000.5:    PLACE_NEAR=T4000.1:4 mm

D4001.1:    PLACE_NEAR=T4001.6:4 mm
D4001.5:    PLACE_NEAR=T4001.1:4 mm
```

SYNCH MASTER=T27 MLB		SYNCH DATE=07/28/2005	
PAGE TITLE			
Ethernet Connector			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-8563	D
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		A.13.0	
		BRANCH	
		PAGE	40 OF 109
		SHEET	32 OF 80



SYNC MASTER=T27 MLB		SYNC DATE=07/20/2005	
PAGE TITLE			
FireWire LLC/PHY		(FW643E)	
 Apple Inc.	DRAWING NUMBER	051-8563	SIZE D
	REVISION	A.13.0	
	BRANCH		
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PAGE	41	OF	109
SHEET	33	OF	80

Page Notes

Power aliases required by this page:

- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

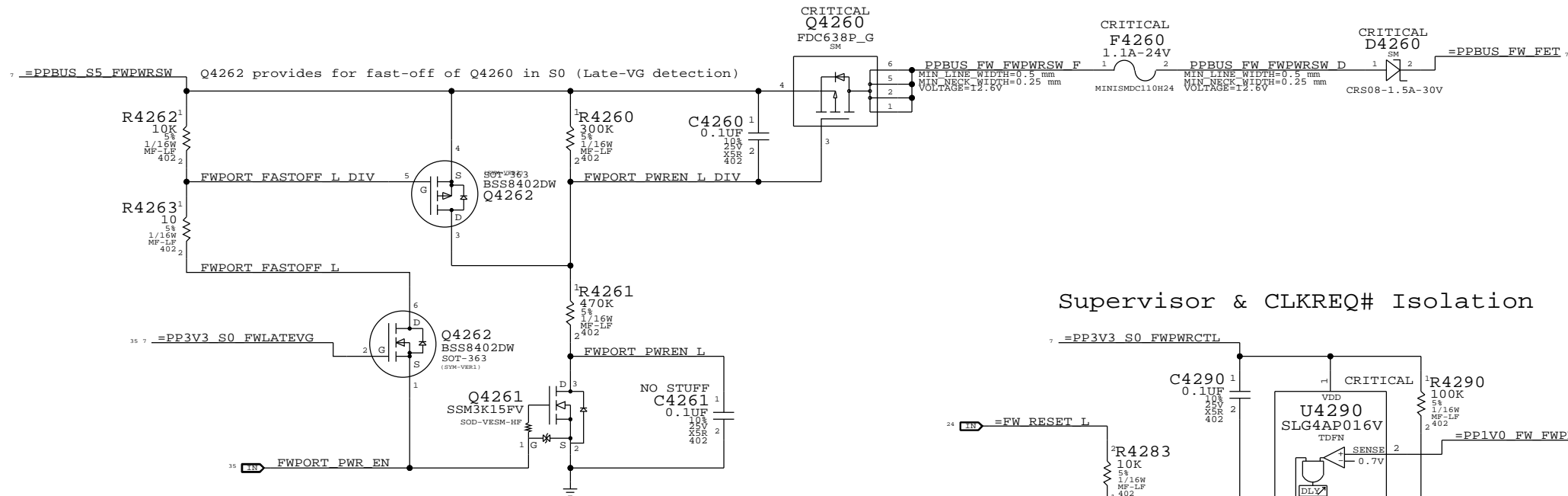
Signal aliases required by this page:

- =FW_CLKREQ_L
- =FW_PME_L

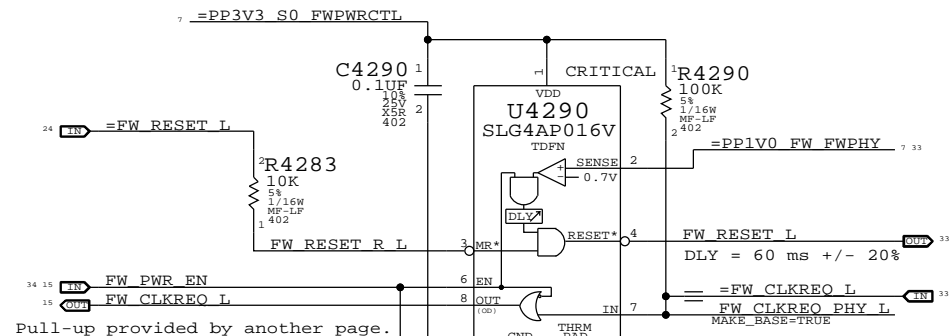
BOM options provided by this page:

(NONE)

FireWire Port Power Switch

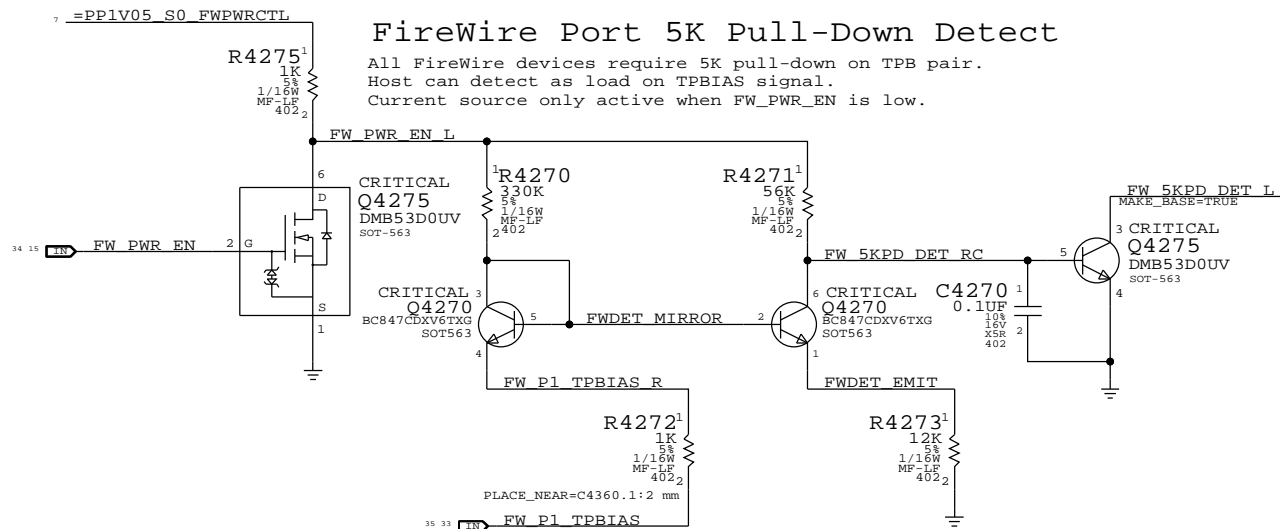


Supervisor & CLKREQ# Isolation



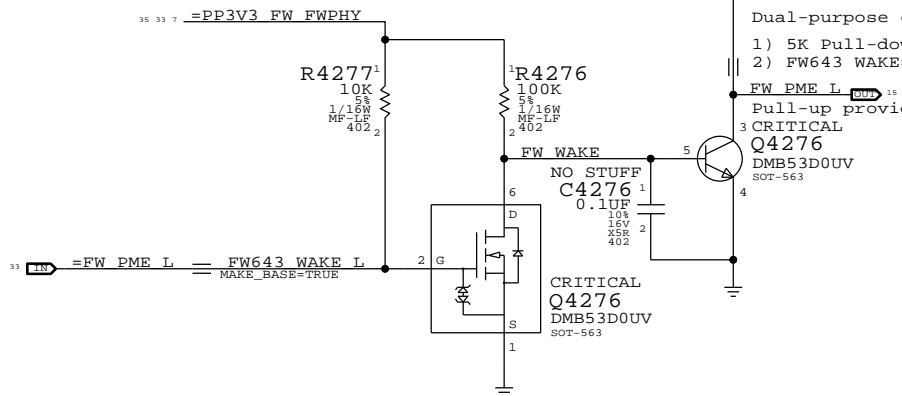
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.

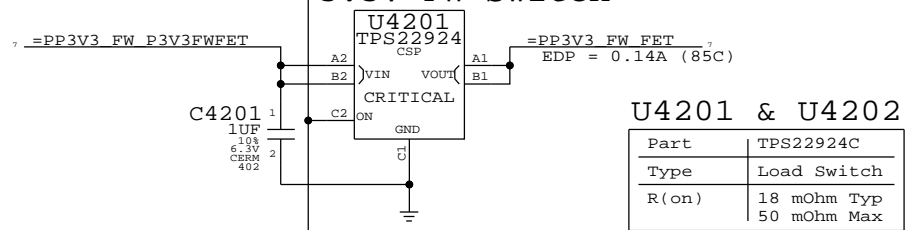


Dual-purpose output:

- 1) 5K Pull-down Detect when FW_PWR_EN is low.
- 2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

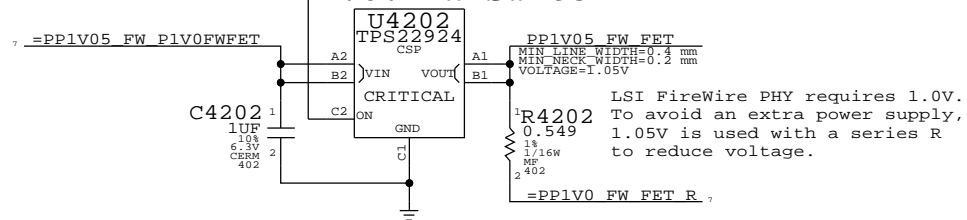
3.3V FW Switch




Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC MASTER=T27 MLB		SYNC DATE=12/15/2009	
PAGE TITLE			
FireWire Port & PHY Power			
 Apple Inc.		DRAWING NUMBER	051-8563
		SIZE	D
		REVISION	A.13.0
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		SHEET	34 OF 80

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:

- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

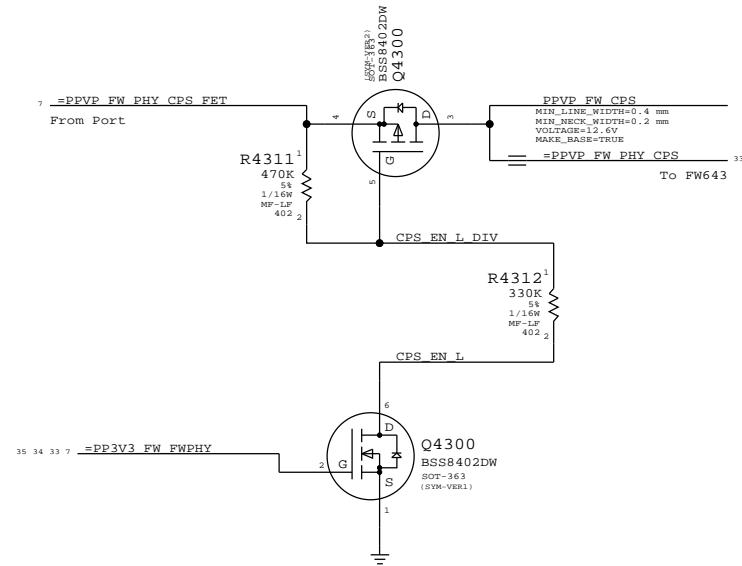
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

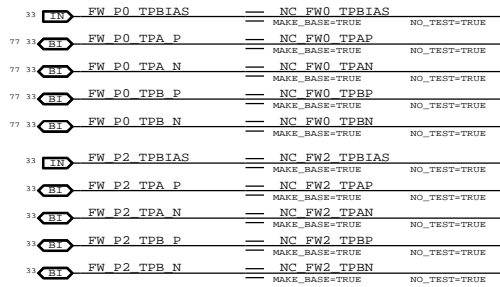
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



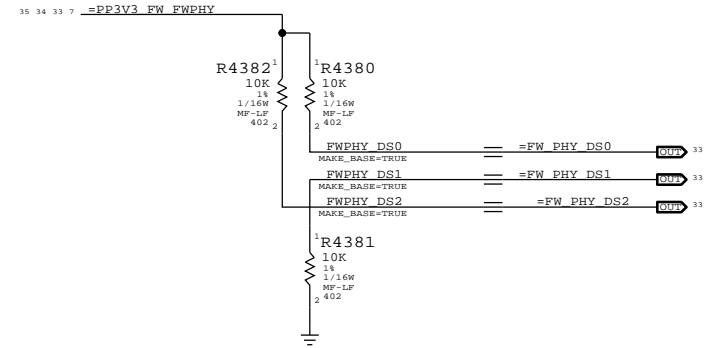
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



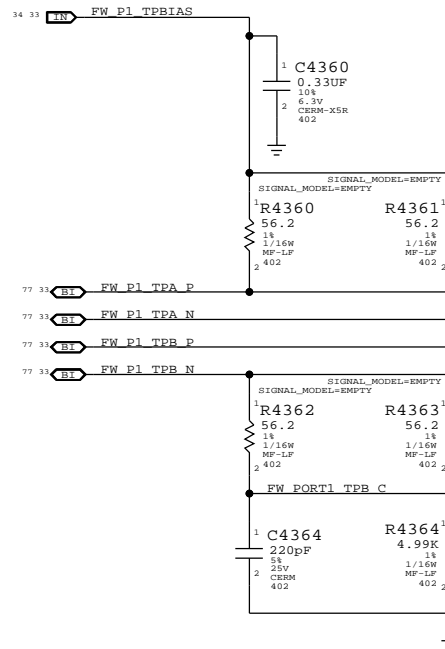
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)



Termination

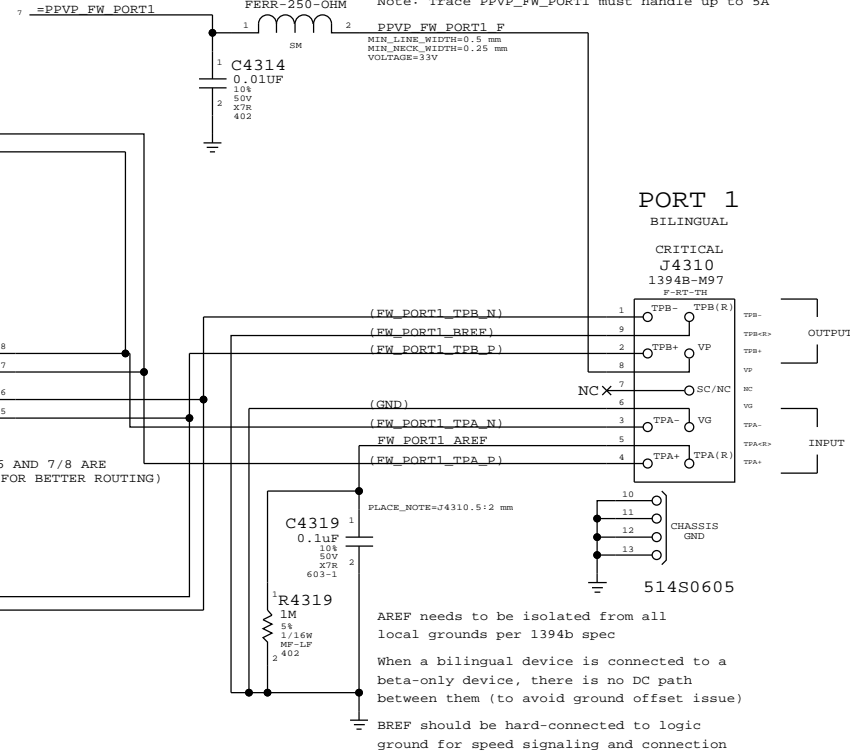
Place close to FireWire PHY



Cable Power

CRITICAL
L4310
FERR-250-OHM

Note: Trace PPVP_FW_PORT1 must handle up to 5A



"Snapback" & "Late VG" Protection

PLACE_NEAR=U4350.1:2 mm

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

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TP FWLATEVG VCLMP

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TP FWLATEVG VCLMP

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TP FWLATEVG VCLMP

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TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN


TP FWLATEVG VCLMP

FWPORT_FWR_EN

TP FWLATEVG VCLMP

FWPORT_FWR_EN

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

SYNC MASTER=T27_MLB		SYNC DATE=07/28/2005	
PAGE TITLE			
FireWire Connector			
 Apple Inc.		DRAWING NUMBER	051-8563
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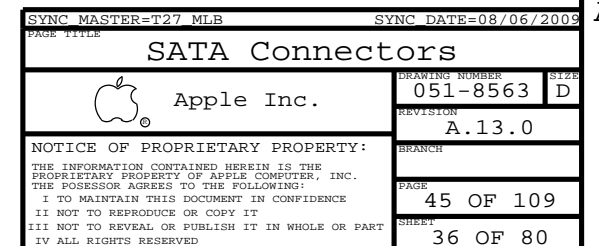
B

J5401 PINOUTS ARE DIFFERENT FOR K6, DO NOT SYNC THIS PAGE FROM T27 DIRECTLY

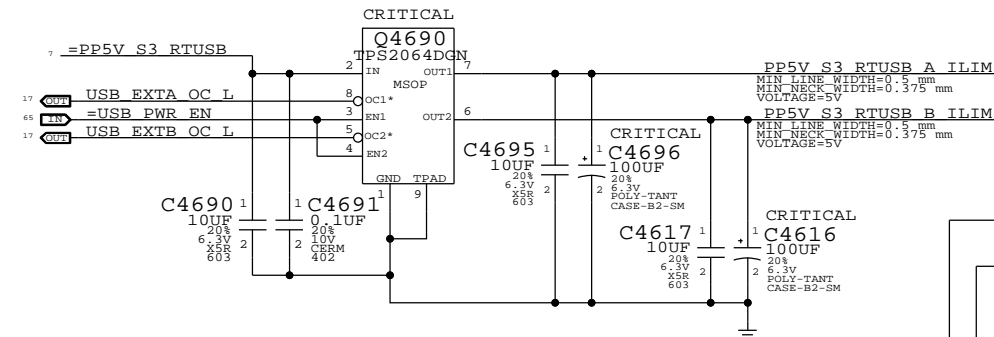
8 =PP5V SW ODD

PS8511A / PS8515A Straps

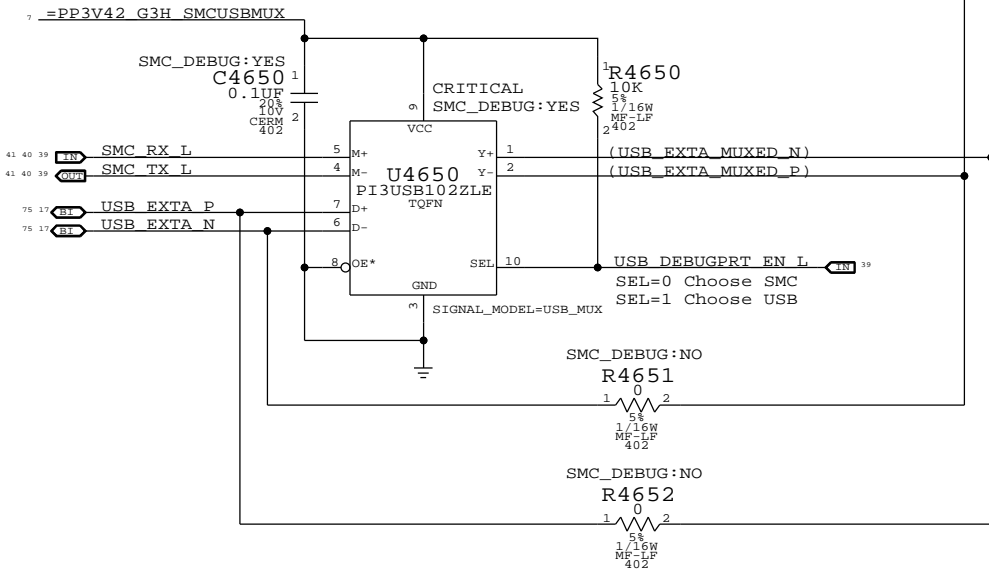
SATA Redriver



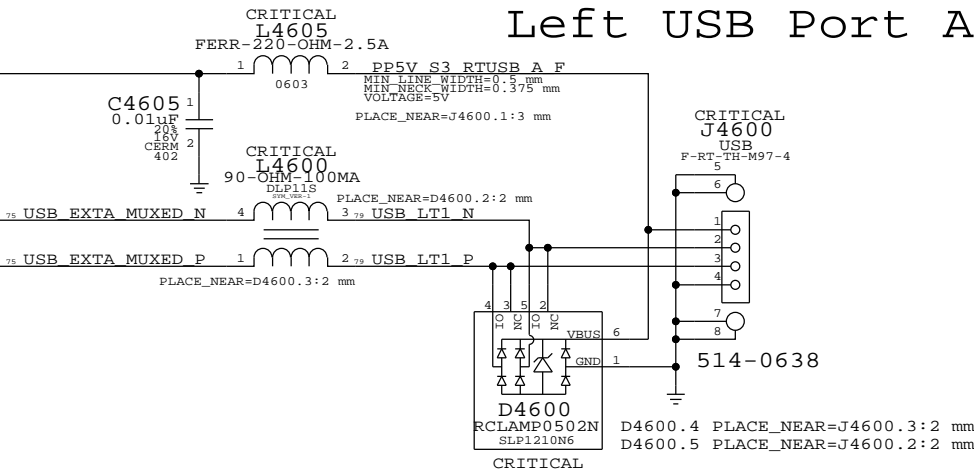
Port Power Switch



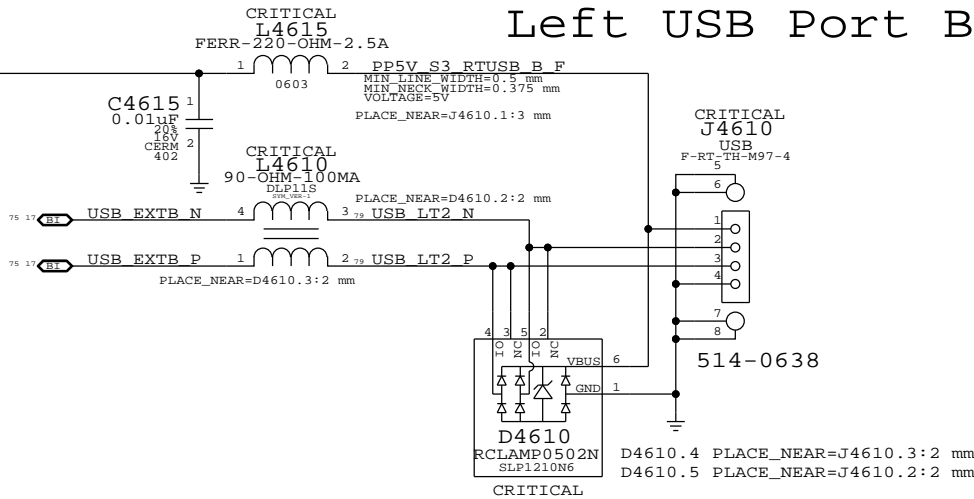
USB/SMC Debug Mux




Left USB Port A



Left USB Port B



SYNC MASTER=T27_MLB		SYNC DATE=08/27/2009	
PAGE TITLE			
External USB Connectors			
 Apple Inc.		DRAWING NUMBER	051-8563
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		PAGE	46 OF 109
		SHEET	37 OF 80

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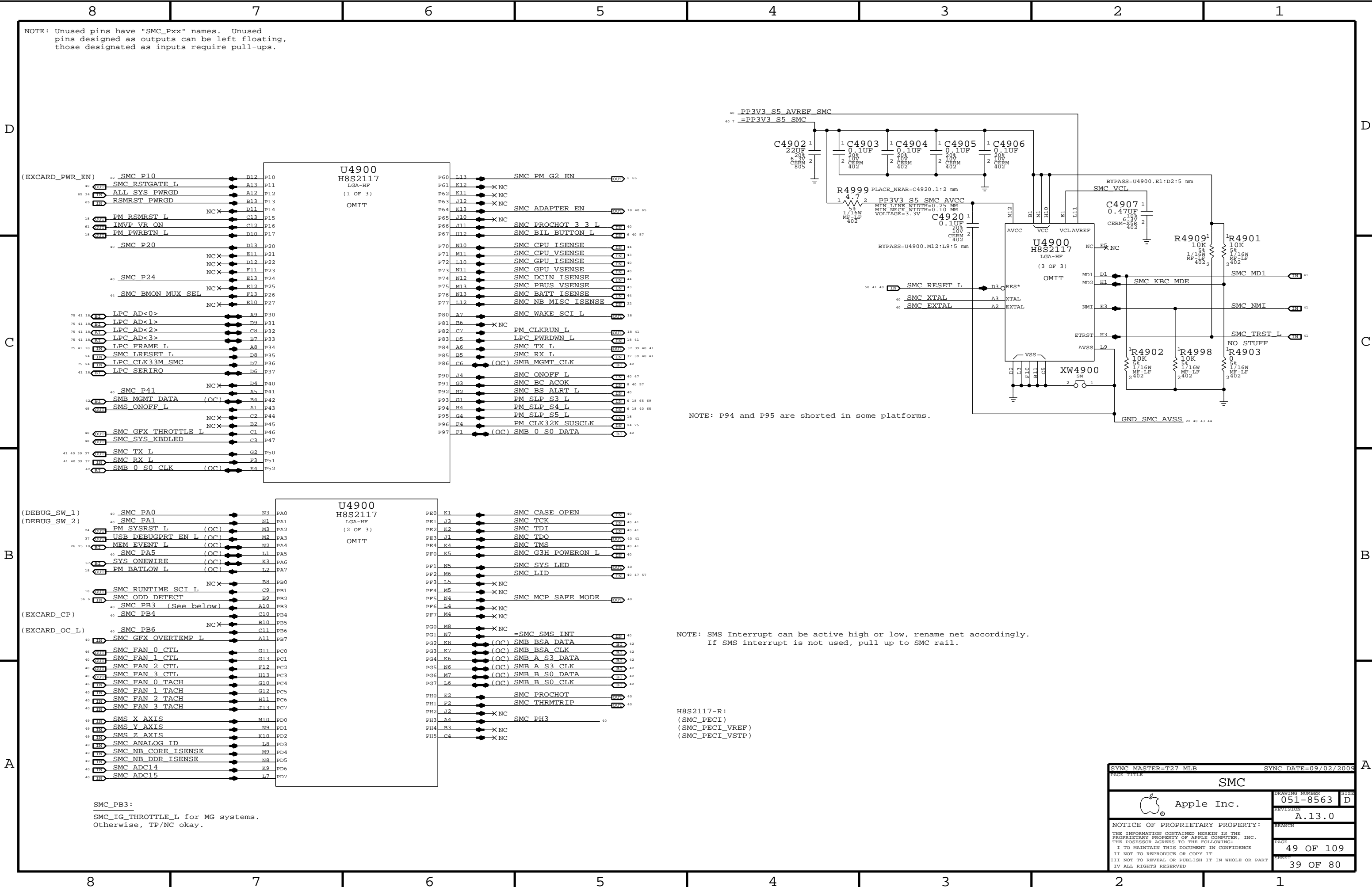


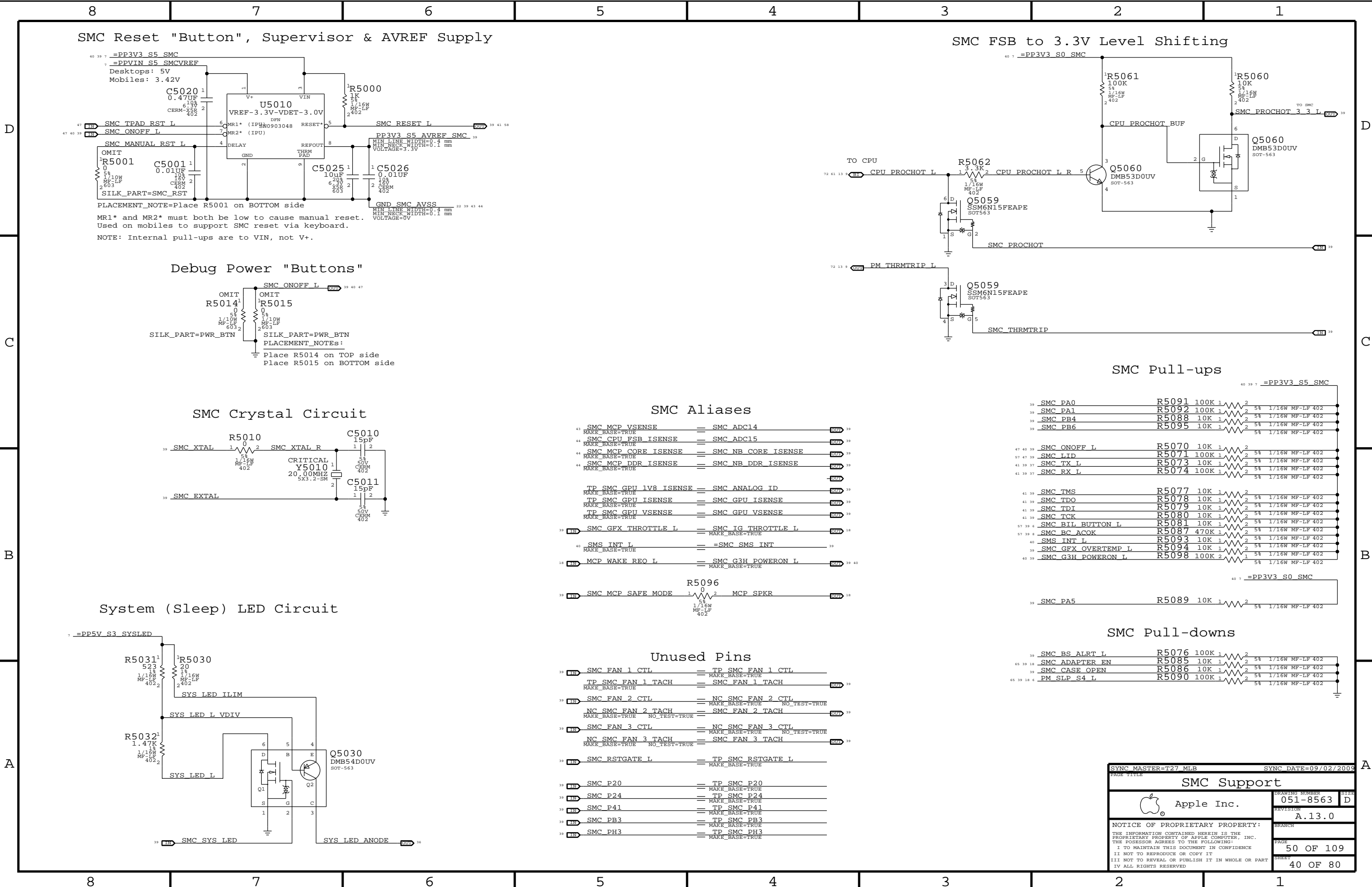
C



B

B





SMC Reset "Button", Supervisor & AVREF Supply

SMC FSB to 3.3V Level Shifting

Debug Power "Buttons"

SMC Crystal Circuit

System (Sleep) LED Circuit

SMC Aliases

SMC Pull-ups


SMC Pull-downs

Unused Pins

SYNC MASTER=T27 MLB

SYNC DATE=09/02/2009

SMC Support

 Apple Inc.

DRAWING NUMBER051-8563SIZE D

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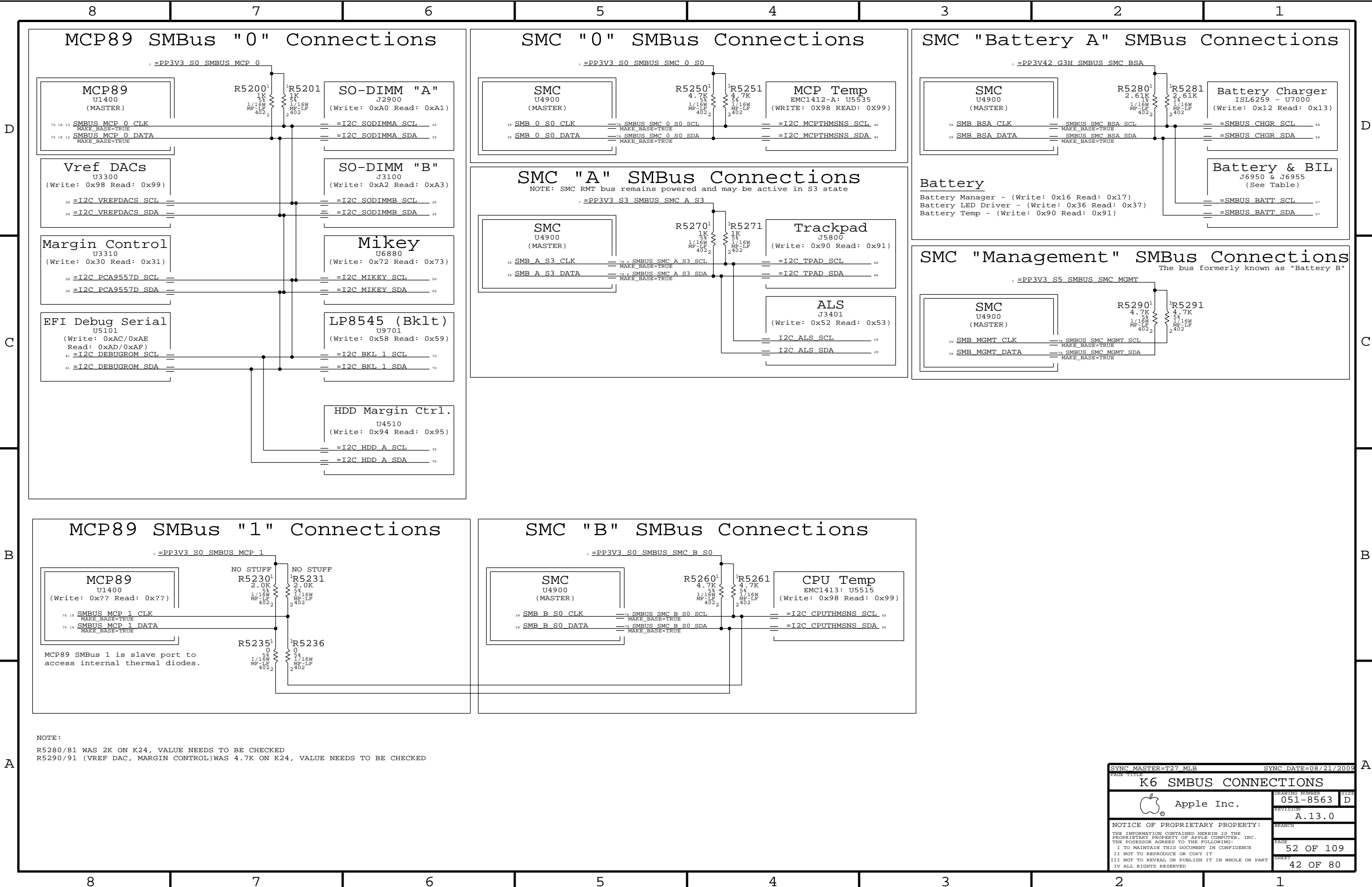


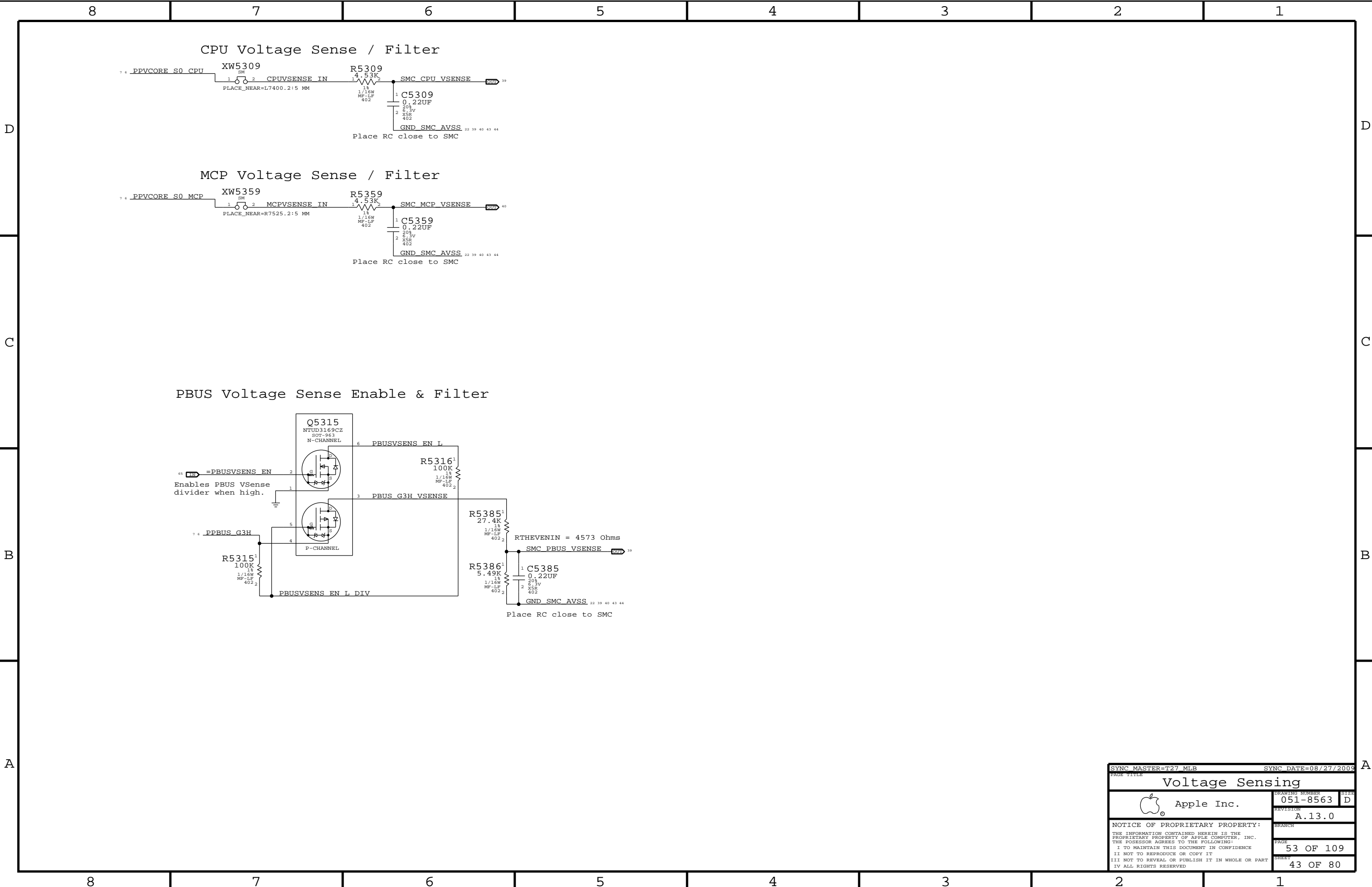
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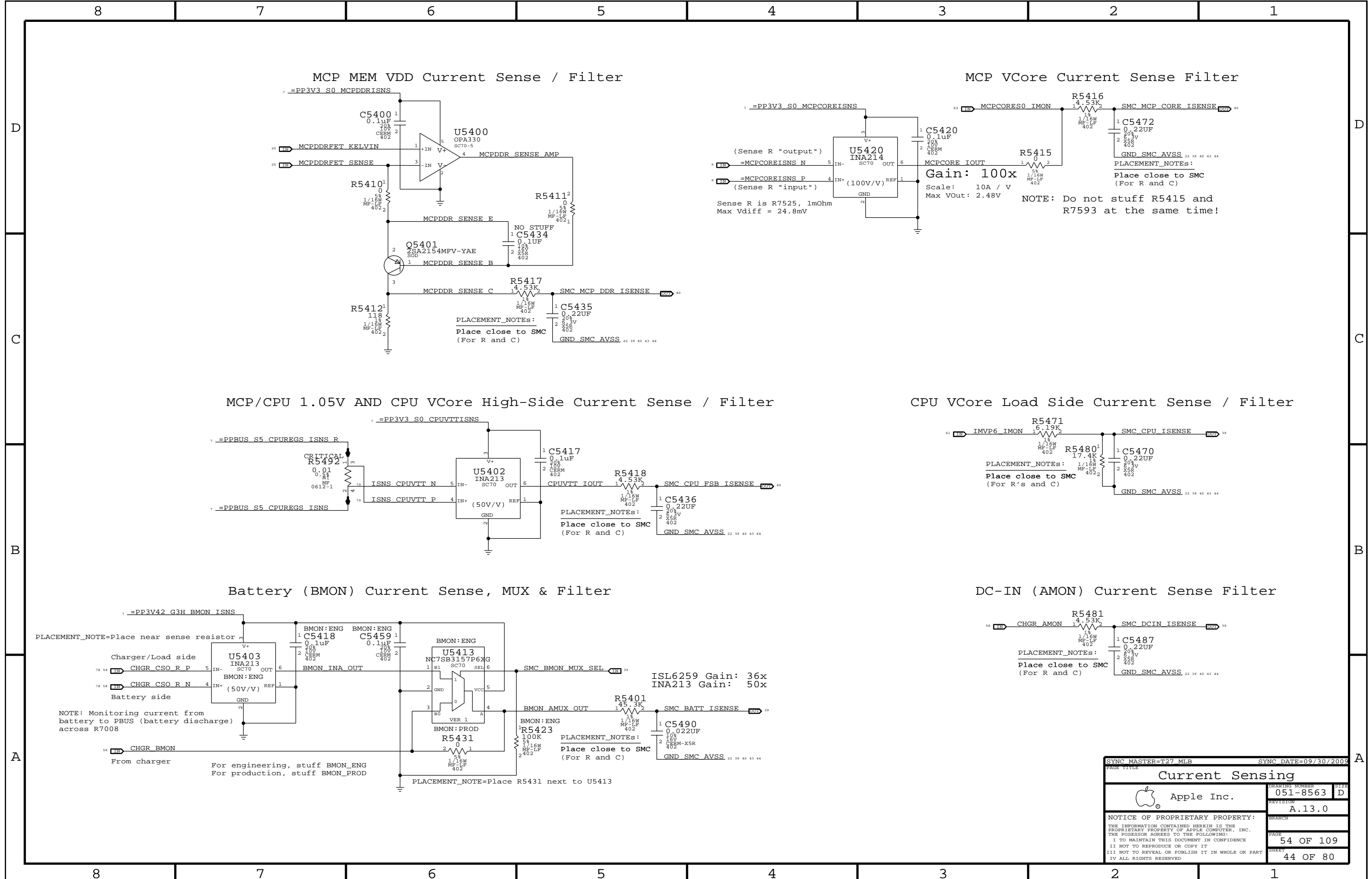
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SYNC MASTER=T27_MLB		SYNC DATE=08/27/2009	
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Voltage Sensing			
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SYNC MASTER=T27 MLB		SYNC DATE=09/30/2009	
PAGE TITLE			
Current Sensing			
 Apple Inc.		DRAWING NUMBER	051-8563
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		SHEET	44 OF 80

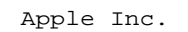
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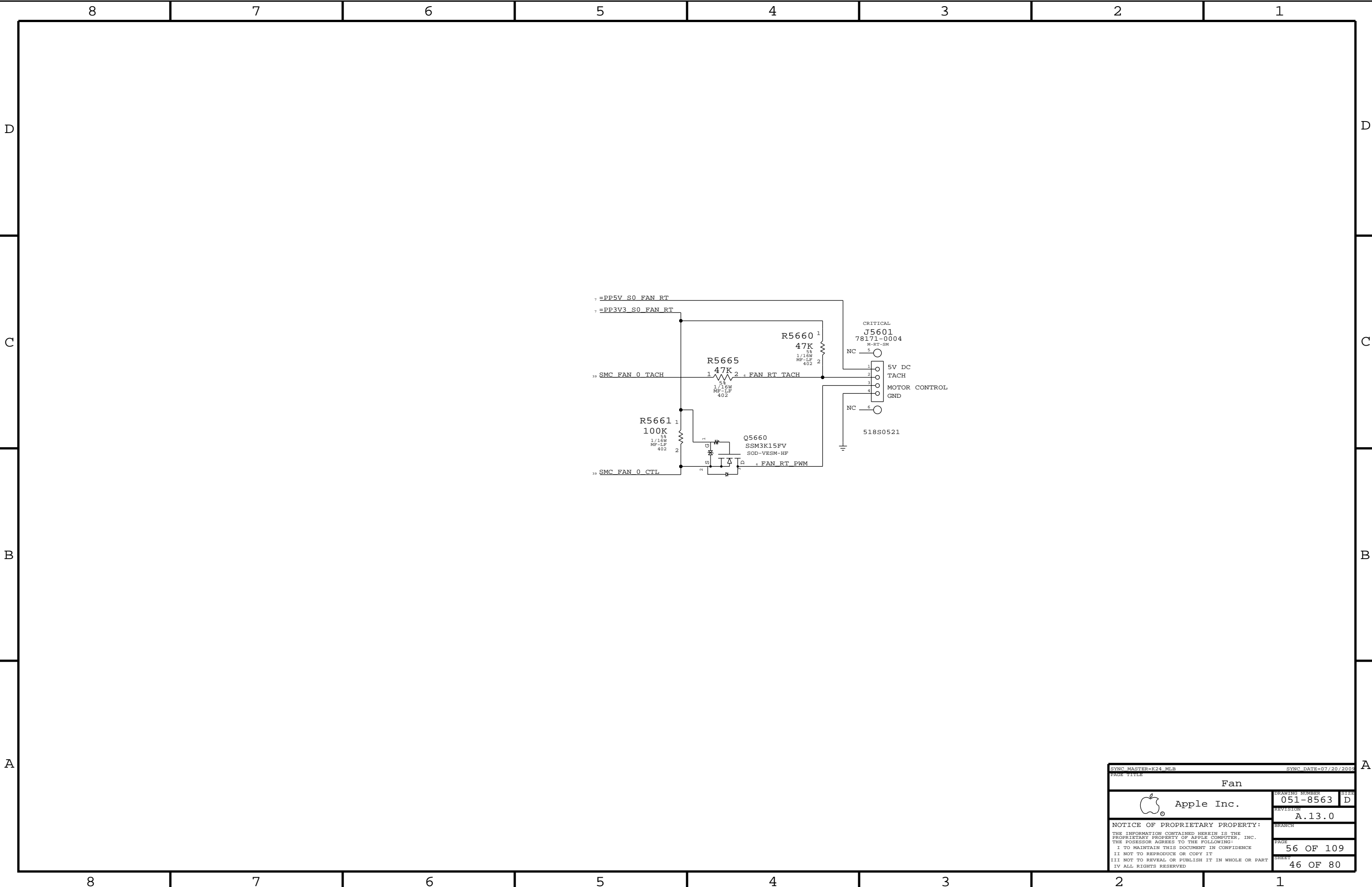
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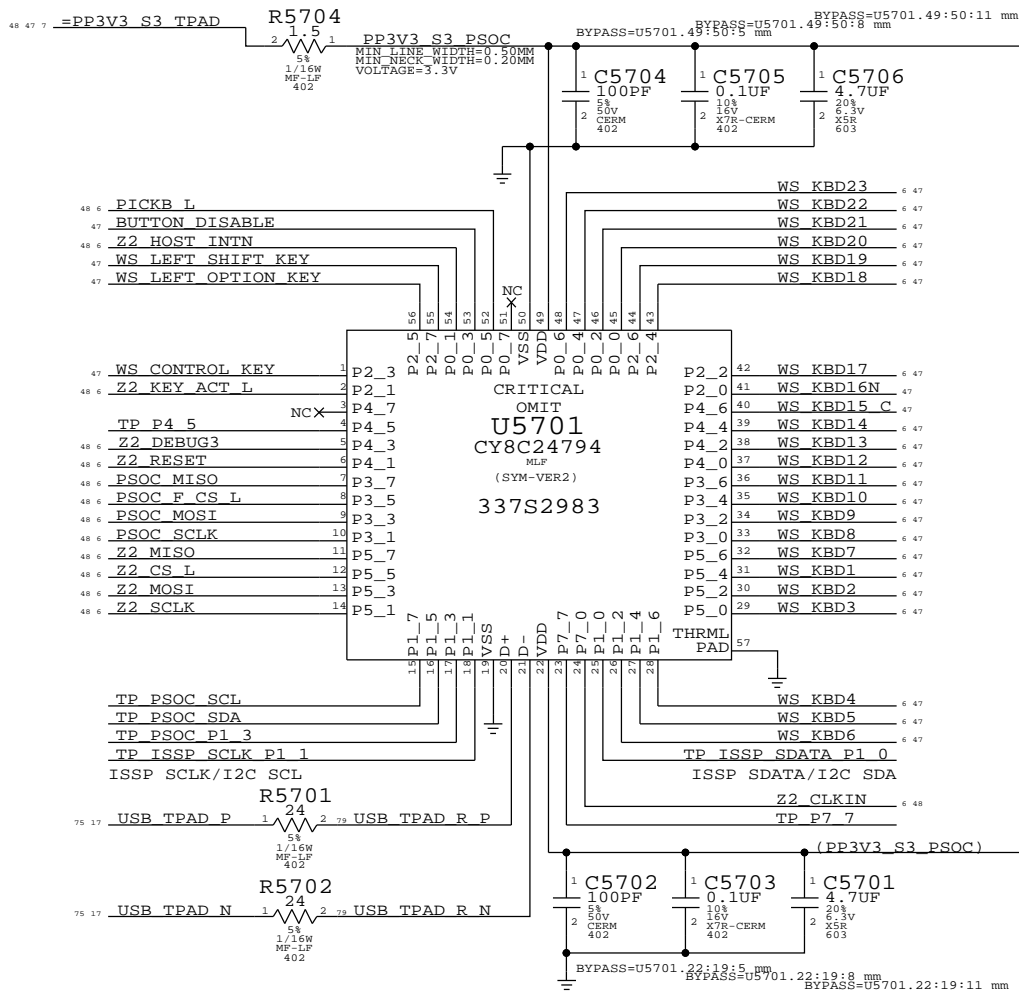


DRAWING NUMBER	051-8563	SIZE	D
REVISION			
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BRANCH			
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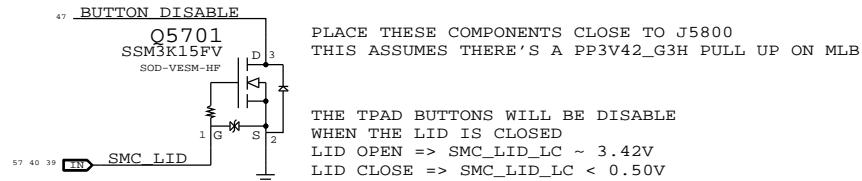


SYNC MASTER=K24 MLB		SYNC DATE=07/20/2009	
PAGE TITLE			
Fan			
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- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

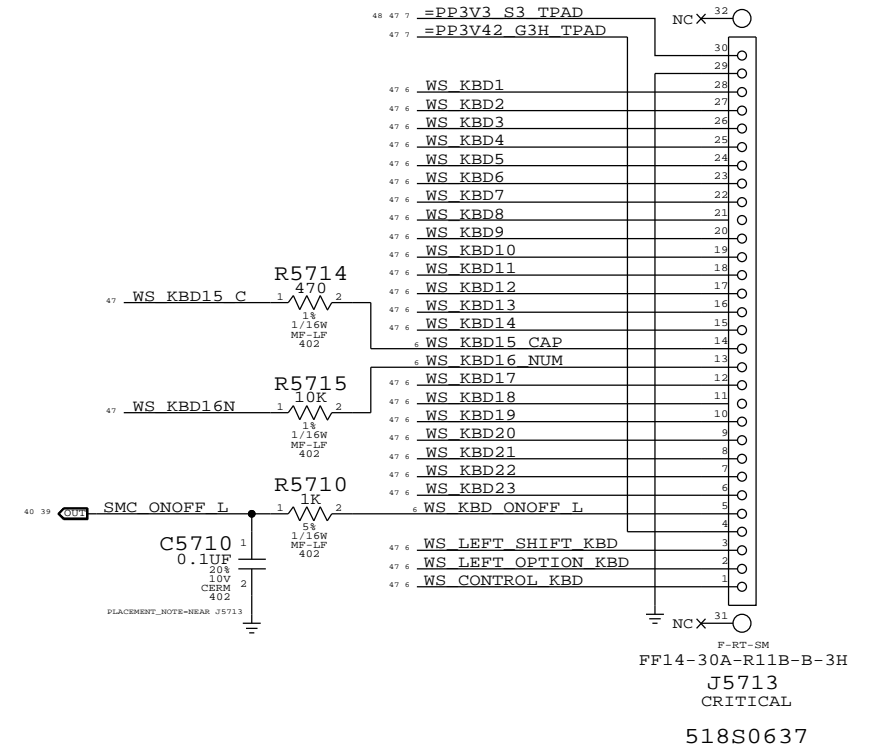


TPAD Buttons Disable



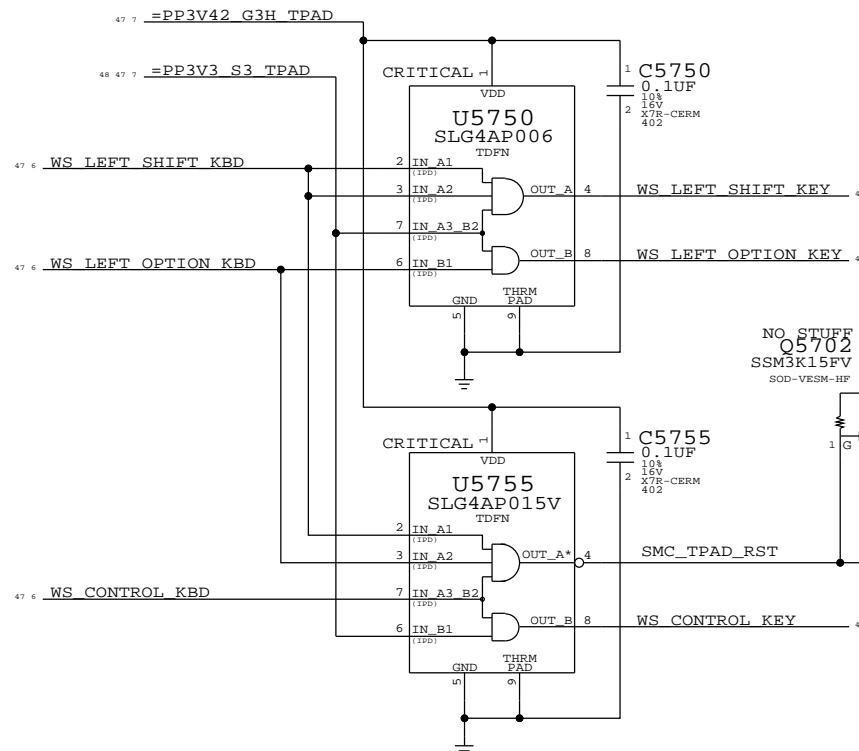
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	100A	2.55 KOHM	0.0255 V	0.255E-6 W
		800A		0.204 V	16.32E-6 W
3V3 LDO	VDD	60mA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60mA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8mA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14mA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4mA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W


Keyboard Connector



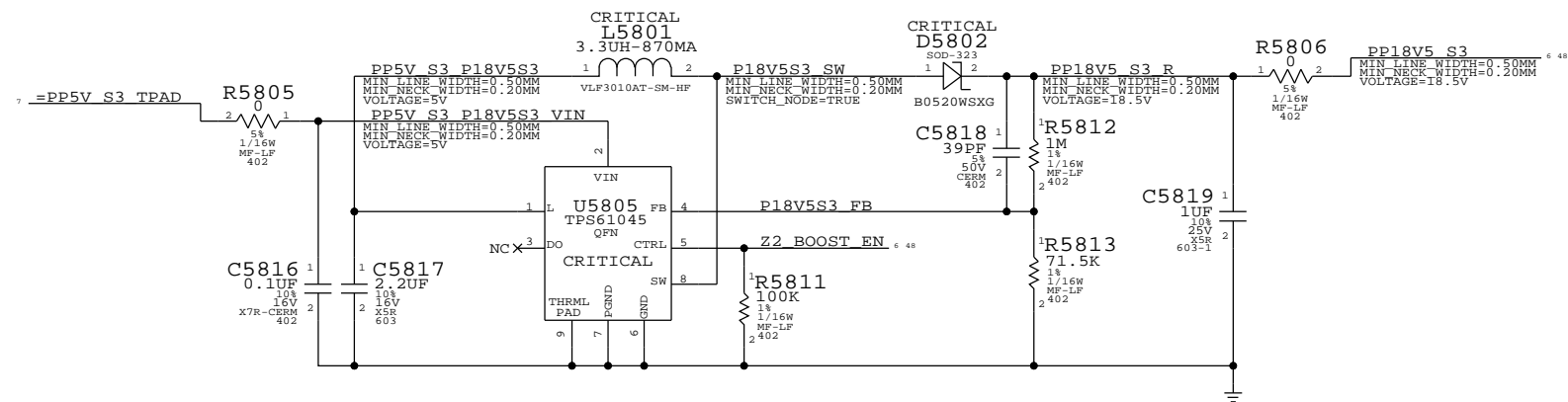
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



SYNC MASTER=T27 MLB		SYNC DATE=08/15/2009	
PAGE TITLE			
WELLSPRING 1			
	Apple Inc.		DRAWING NUMBER 051-8563
			SIZE D
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```
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED
```



CRITICAL
J5800
55560-0228
M-ST-SM

PP3V3V3 S3 TPAD

PP18V5 S3

Z2 CS L

Z2 DEBUG3

Z2 MOSI

Z2 MISO

Z2 SCLK

Z2 BOOST EN

Z2 HOST INTN

Z2 CLKIN

Z2 KEY ACT L

Z2 RESET

PSOC F CS L

PICKB L

PSOC MISO

PSOC MOSI

PSOC SCLK

=I2C TPAD SDA

=I2C TPAD SCL

516S0689

7 = PP5V S0 KBDLED
 BYPASS=U5850.1:2:2 MM
 7 = PP3V3 S0 TPAD
 R5853 470K 5% 1/16W MF-LP 402 2
 KB_BL C5850 1UF 10V X5R 402-1 1 2
 10UH-0.58A-0.35OHM 1 2 KBDLED SW
 109SAS-SM MIN_LINE_WIDTH=0.3 MM MIN_NECK_WIDTH=0.25 MM SWITCH_NODE=TRUE
 SMC_SYS KBDLED 30
 KB_BL R5854 4.7K 5% 1/16W MF-LP 402 2 1
 NO STUFF R5855 10K 5% 1/16W MF-LP 402 2 1
 KB_BL U5850 LT3491 1 2 3 4 5 6
 CTRL LED VIN GND THERM PAD
 KB_BL R5855 10 5% 1/16W MF-LP 402 2 1
 KBDLED CAP 1 2
 MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.25 MM
 KB_BL C5855 1UF 35V X5R 603 1 2
 (SMC KBDLED PRESENT I.)

To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:
 If LOW, keyboard backlight present
 If HIGH, keyboard backlight not present
 R5853 always stuffed, R5854 only grounded when KB BL flex connected.

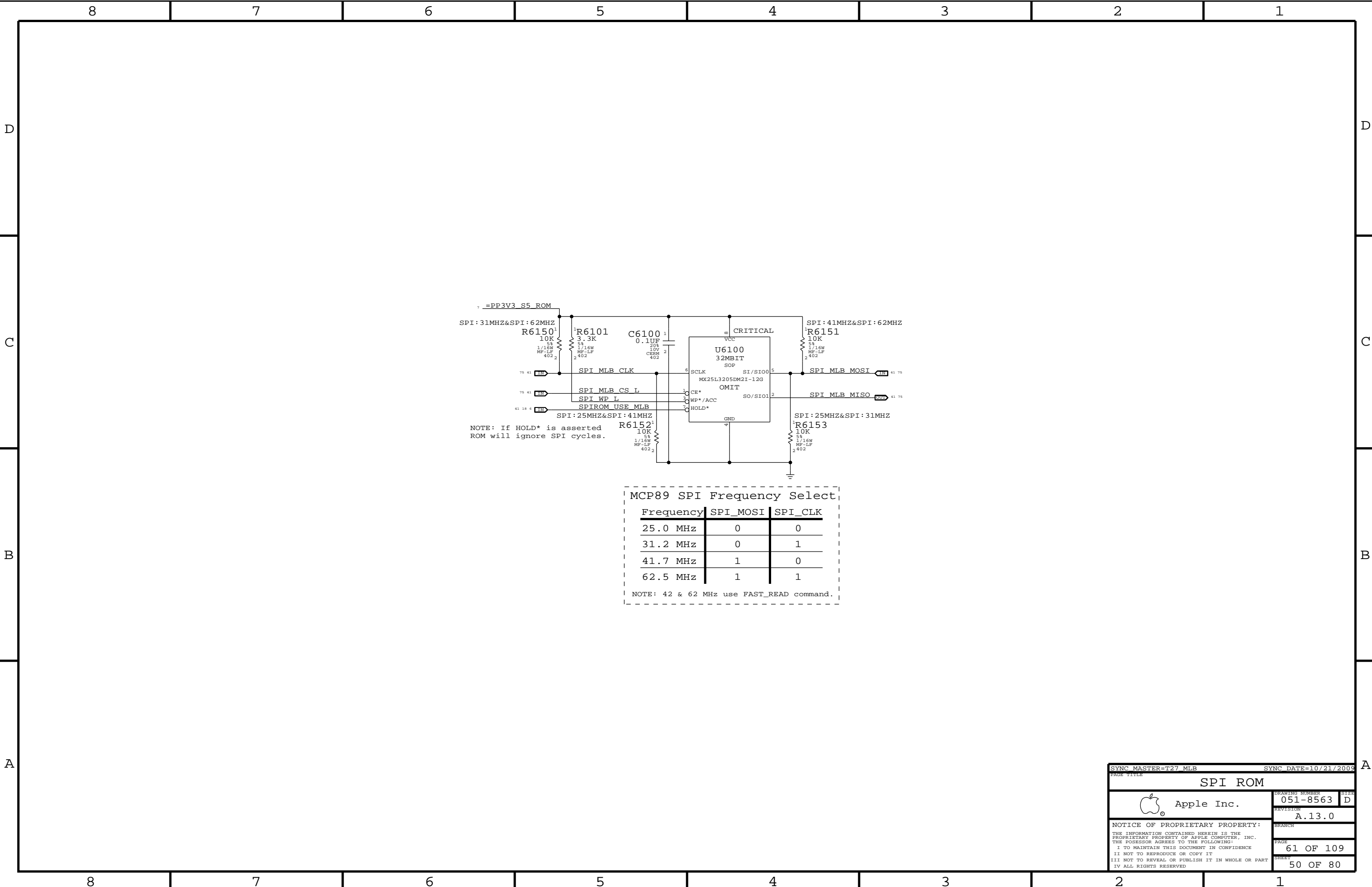
CRITICAL

KB BL
J5815
FF18-4A-R11AD-B-3H
FF18-04

SMC KDBLED PRESENT L

J5815 pin 1 is grounded
on keyboard backlight flex

518S0691




MCP89 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1
NOTE: 42 & 62 MHz use FAST_READ command.		

SYNC_MASTER=T27_MLB

SYNC_DATE=10/21/2009

SPI ROM

 Apple Inc.

DRAWING NUMBER

051-8563

REVISION

A.13.0

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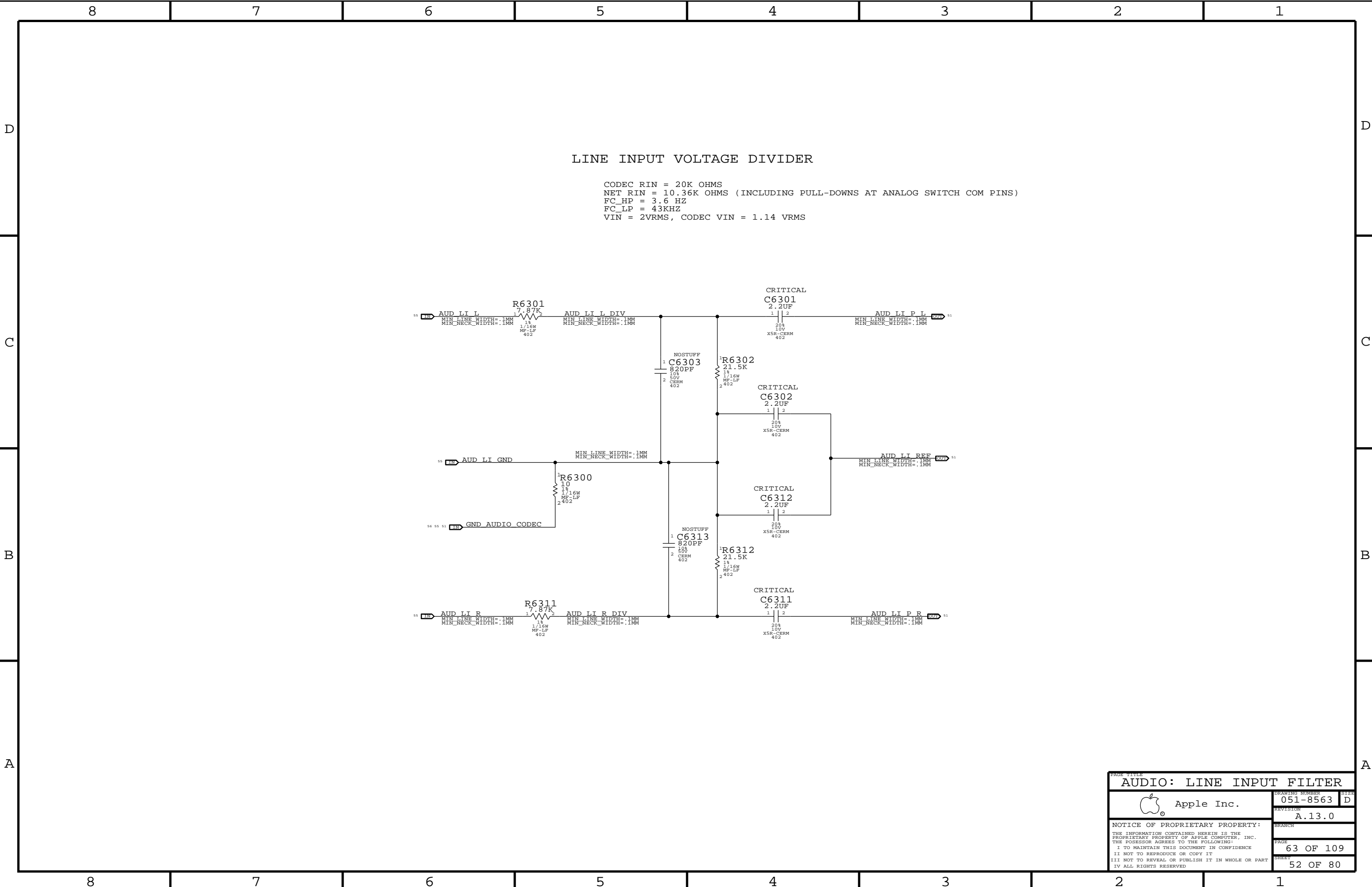
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SHEET

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PAGE TITLE AUDIO: LINE INPUT FILTER		
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D

D

C

C

B

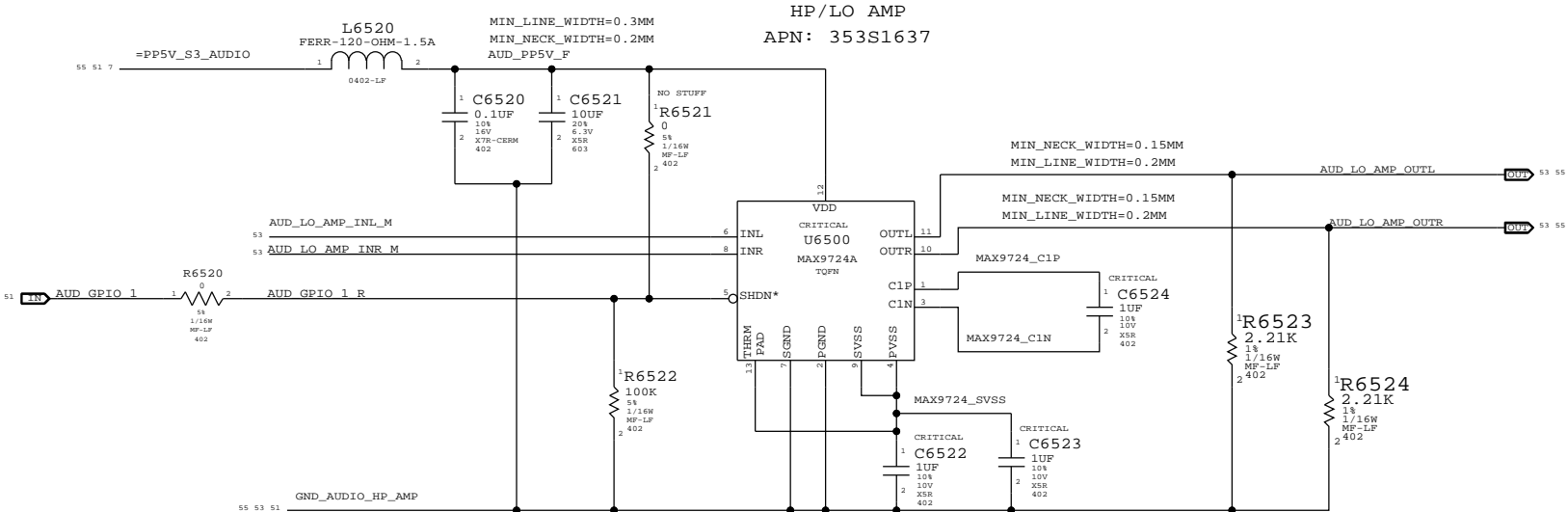
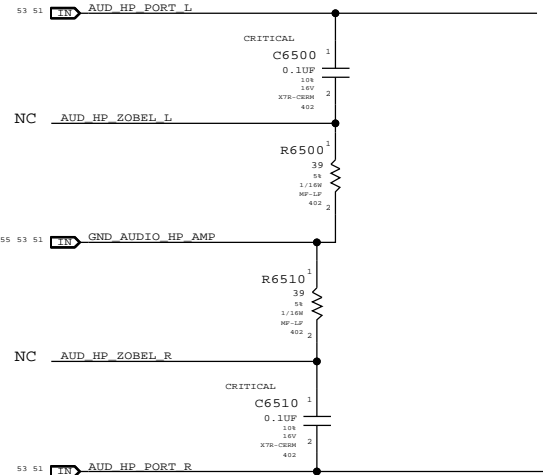
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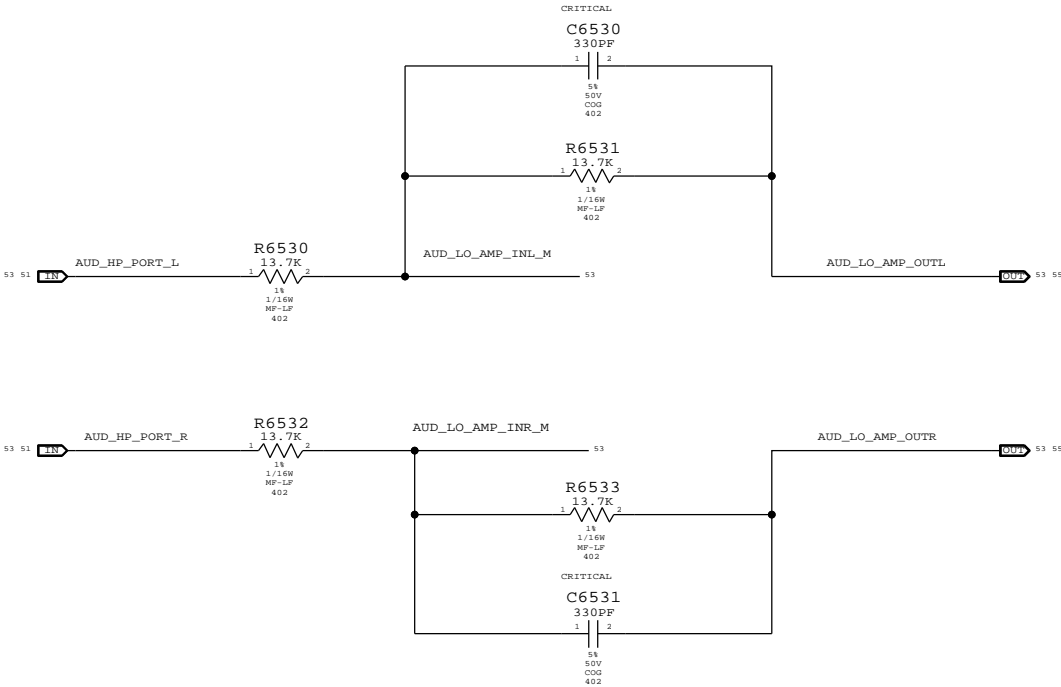
A


FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

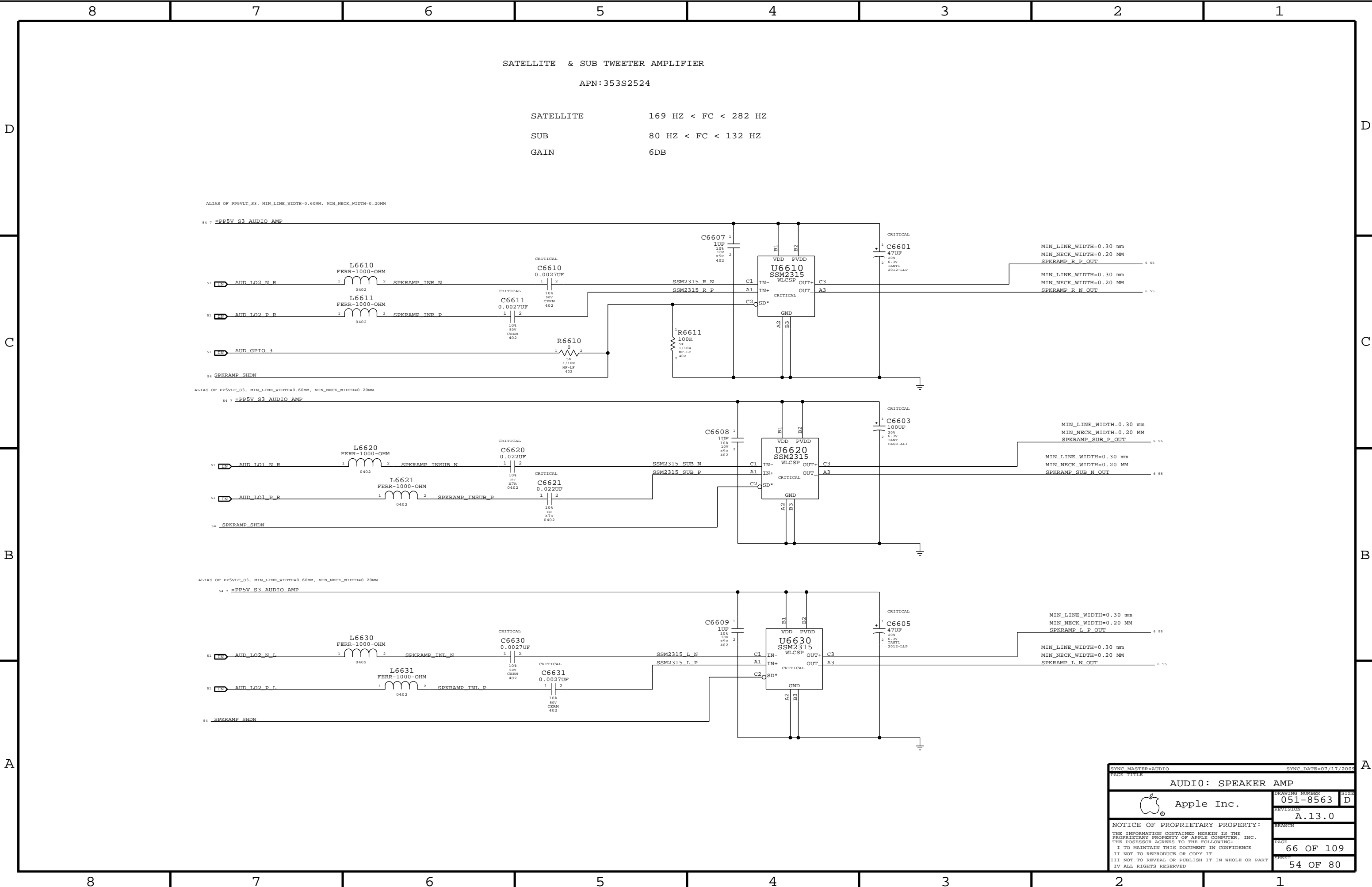
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER

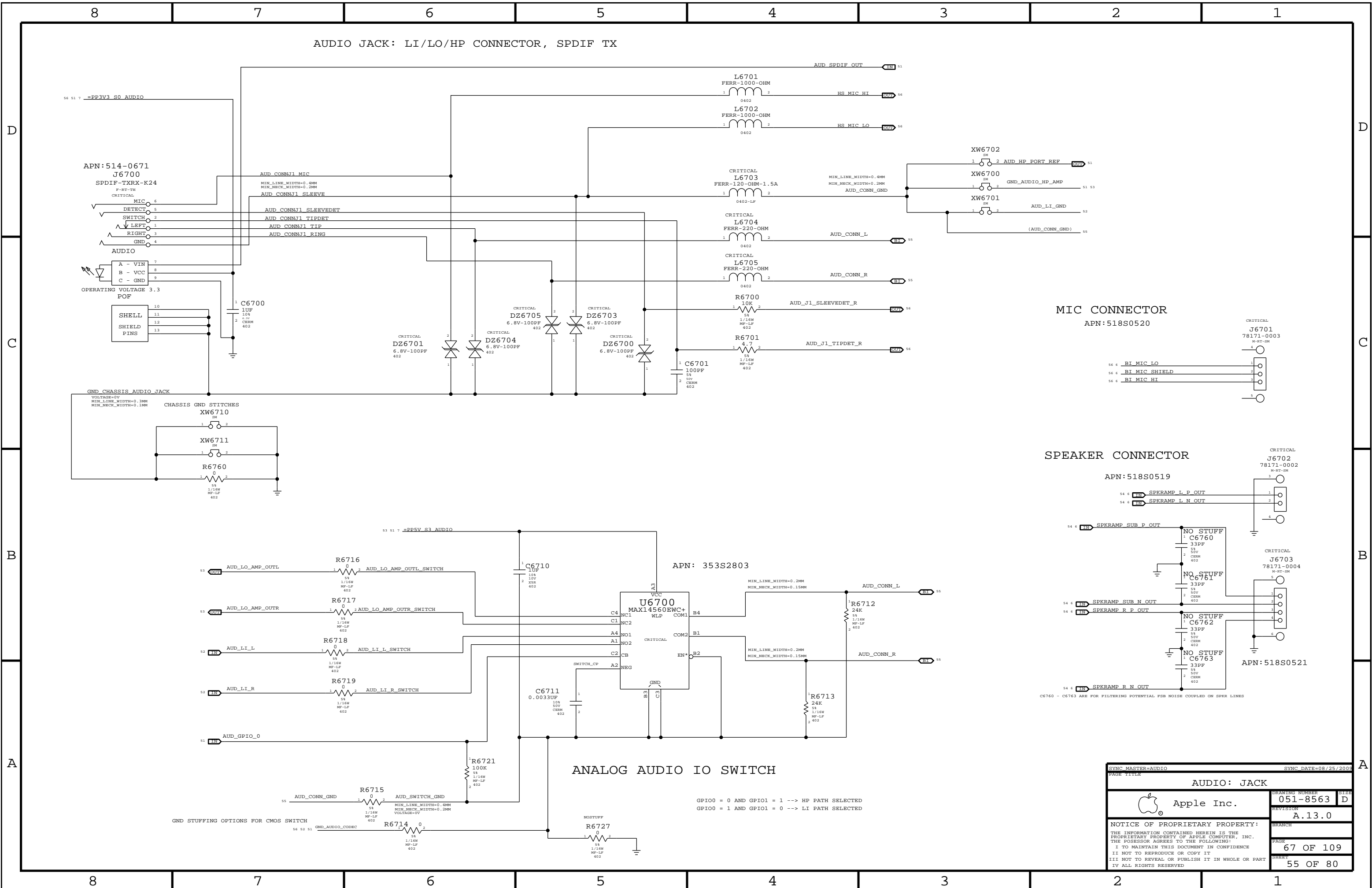


MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1V/V, FC_LPF = 35.2KHZ



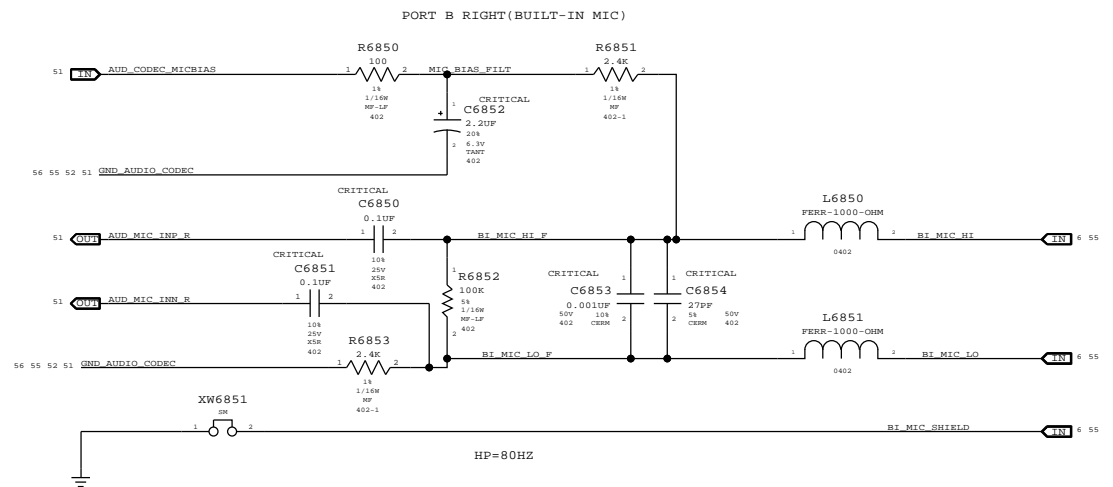
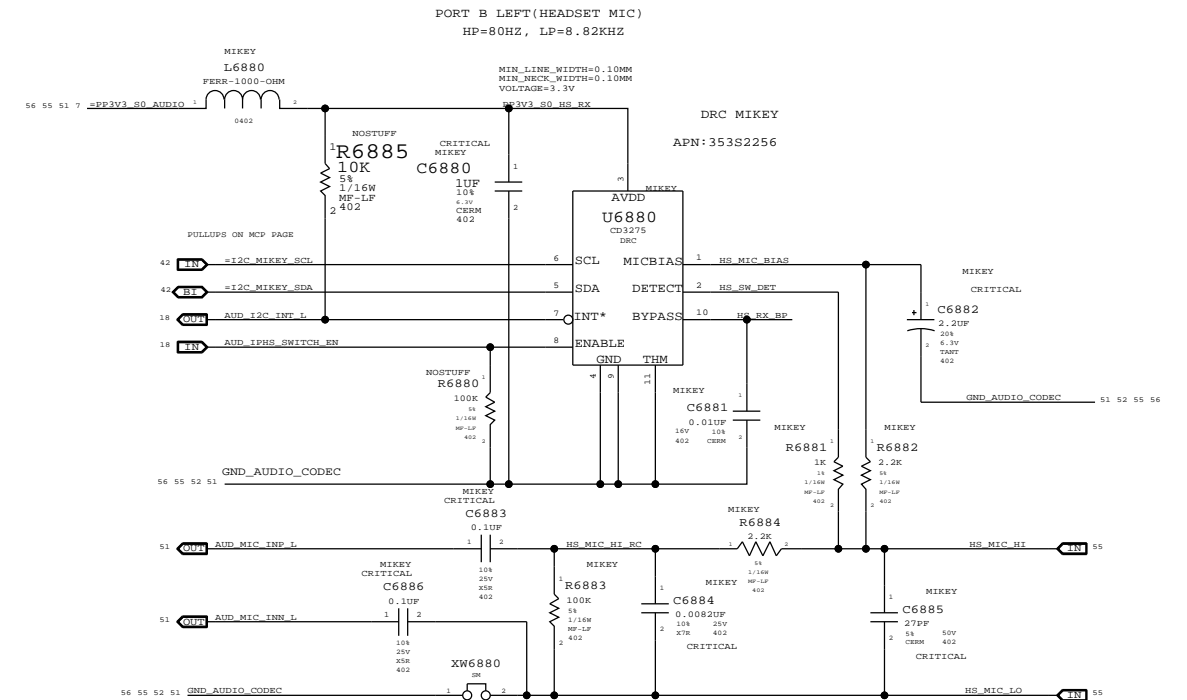
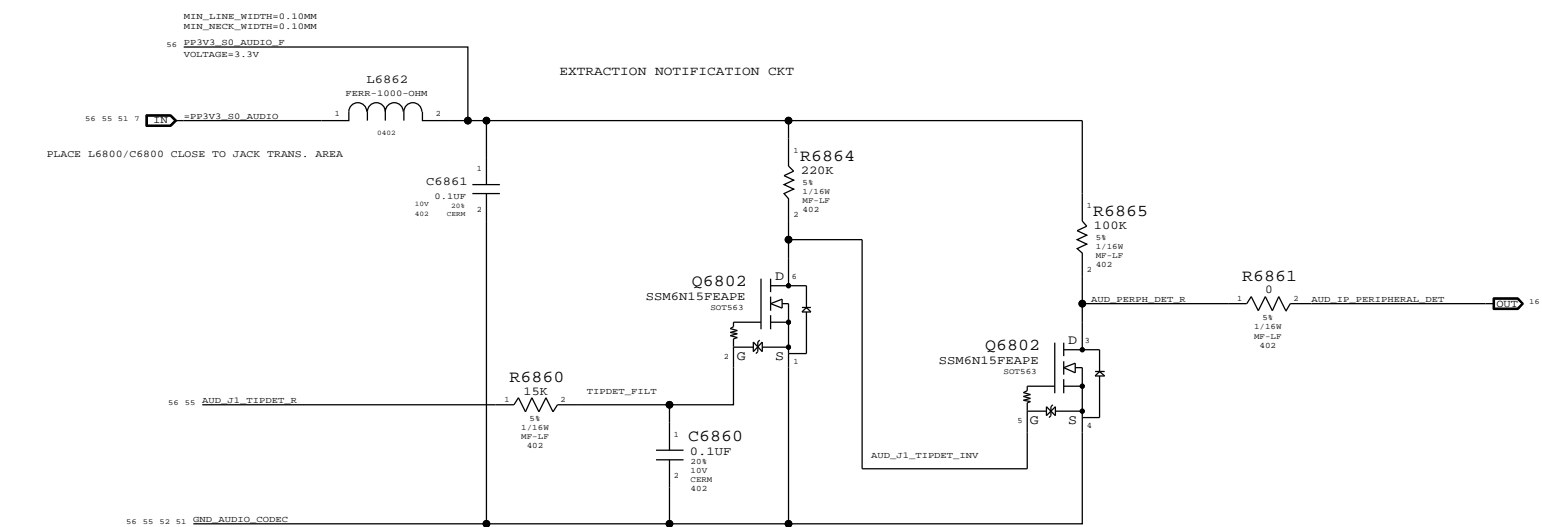
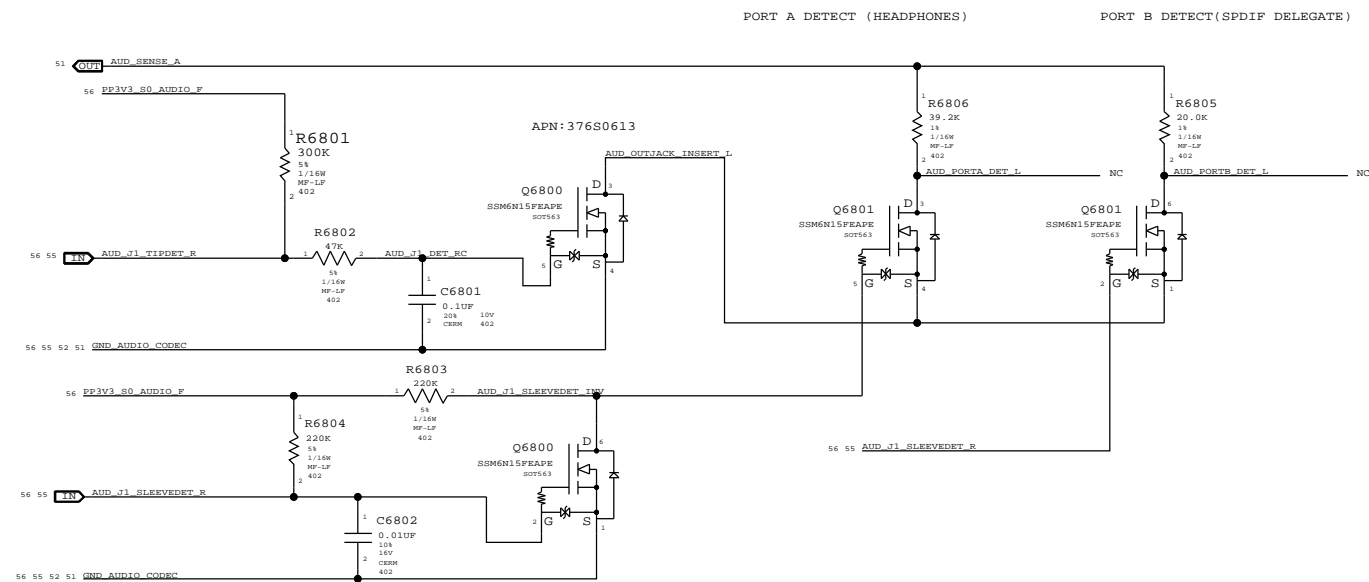
SYNC MASTER=AUDIO		SYNC DATE=07/17/2005	
PAGE TITLE			
AUDIO: HEADPHONE FILTER			
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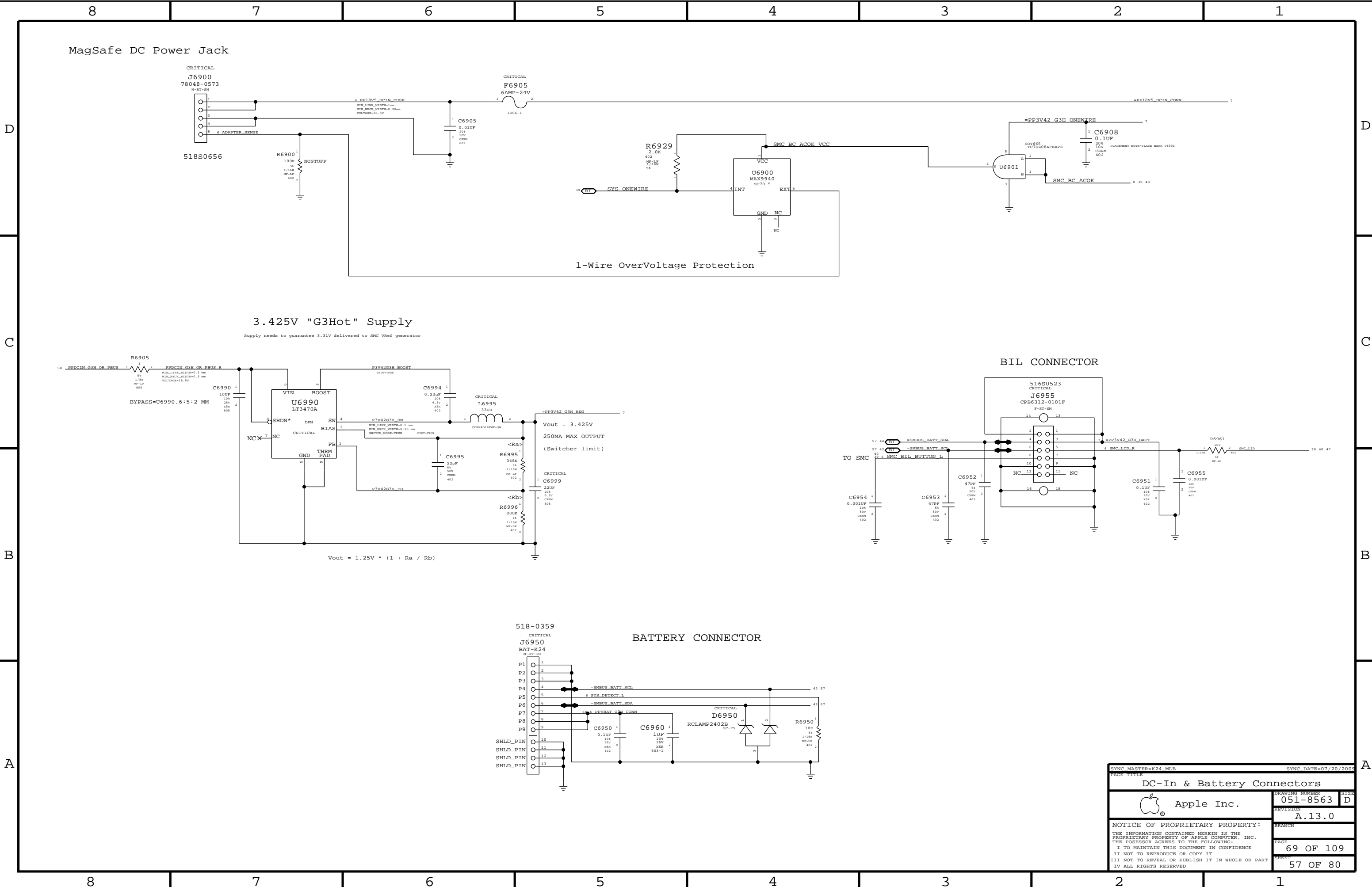



CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_0 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_0 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)



SYNC MASTER-AUDIO		SYNC DATE=08/27/2005	
PAGE TITLE			
AUDIO: JACK TRANSLATORS			
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			SIZE D
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SYNC MASTER=K24 MLB		SYNC DATE=07/20/2005	
PAGE TITLE			
DC-In & Battery Connectors			
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[illegible]

SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

SYNC MASTER=K24 MLB		SYNC DATE=07/20/2005	
PAGE TITLE			
5V/3.3V SUPPLY			
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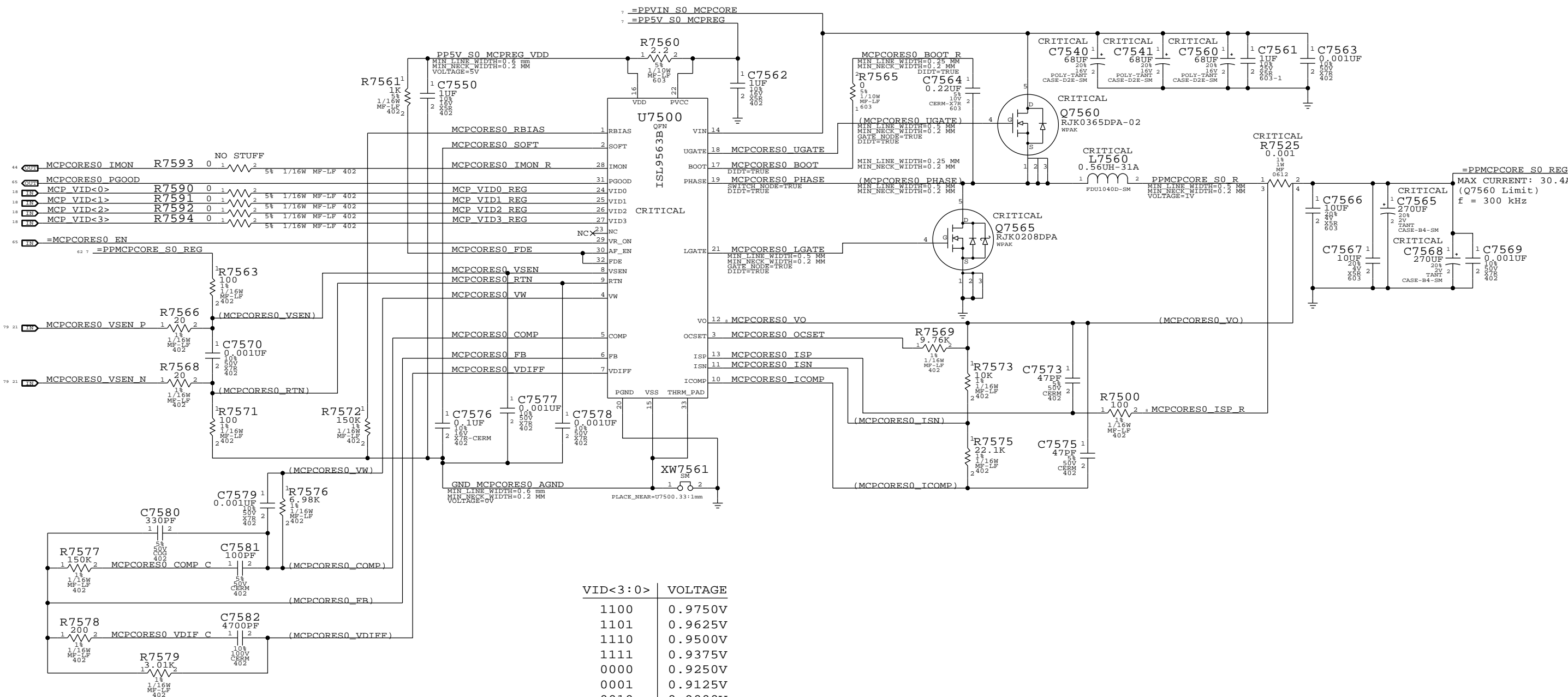
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A



K6 NOTES : XOR AND INVERTER IS REMOVED, CANNOT SYNC THIS PAGE FROM T27

SYNC MASTER=T27_MLB

SYNC DATE=08/18/2009

MCP VCore Regulator

Apple Inc.

051-8563

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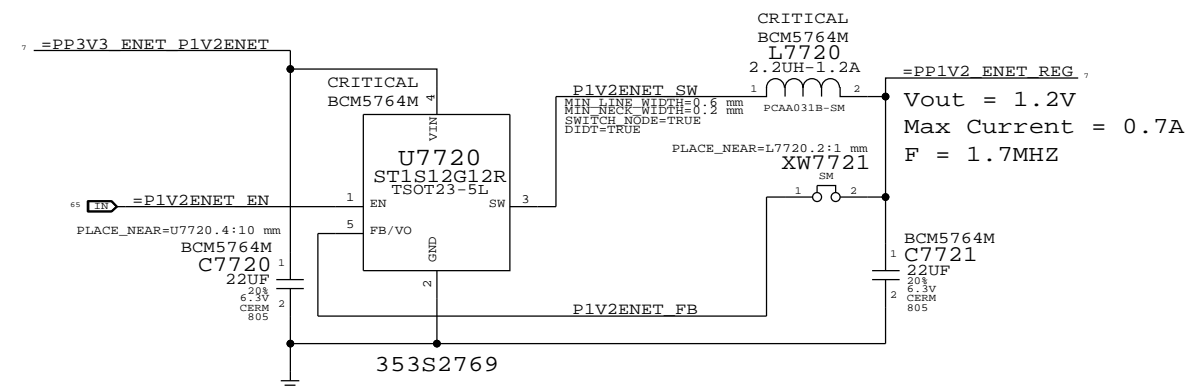
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B

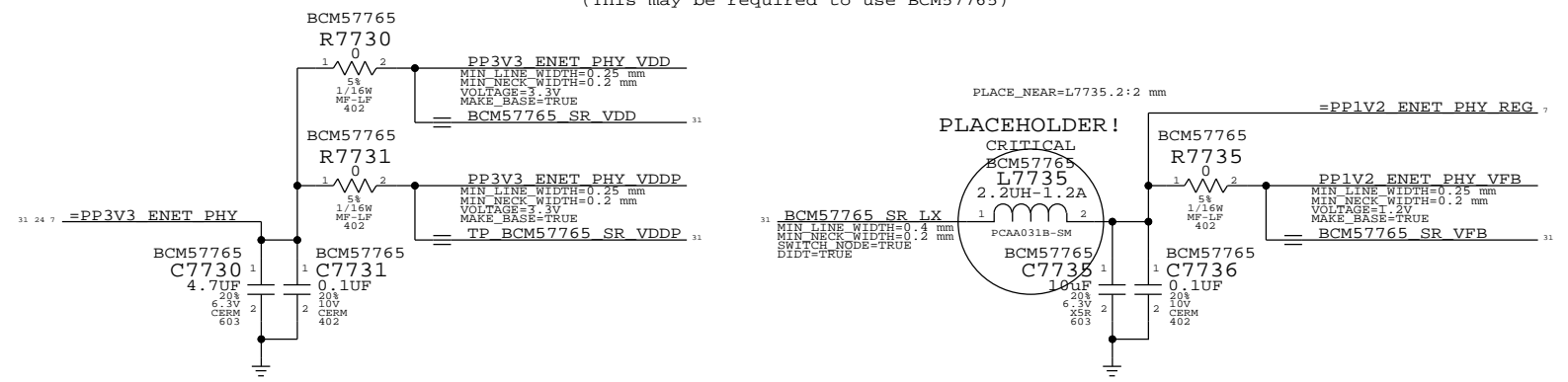
B

1.2V ENET Switcher

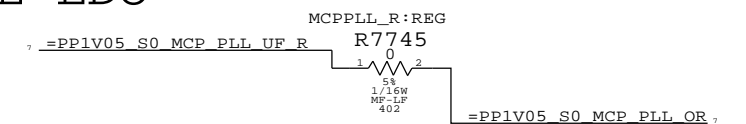


BCM57765 Internal Switcher Support

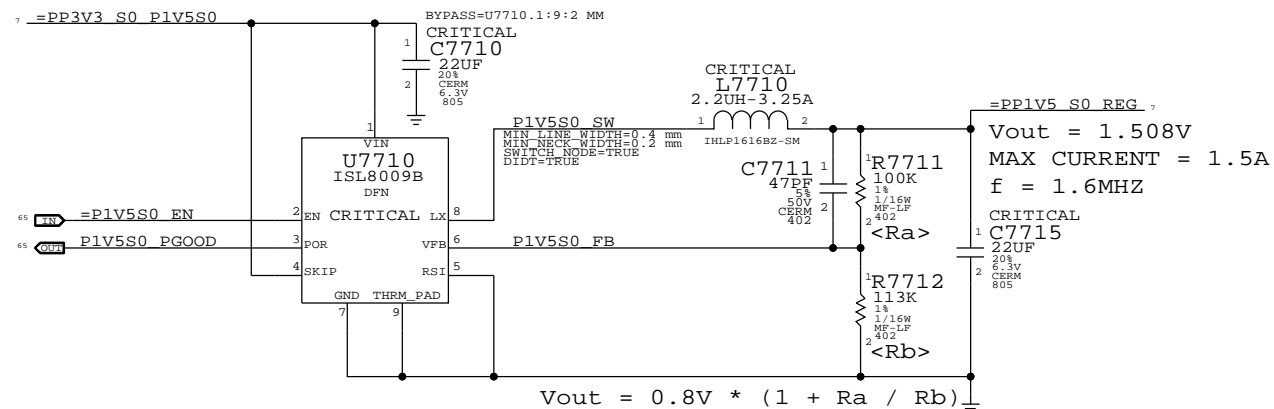
(This may be required to use BCM57765)



1.05V S0 MCP PLL LDO



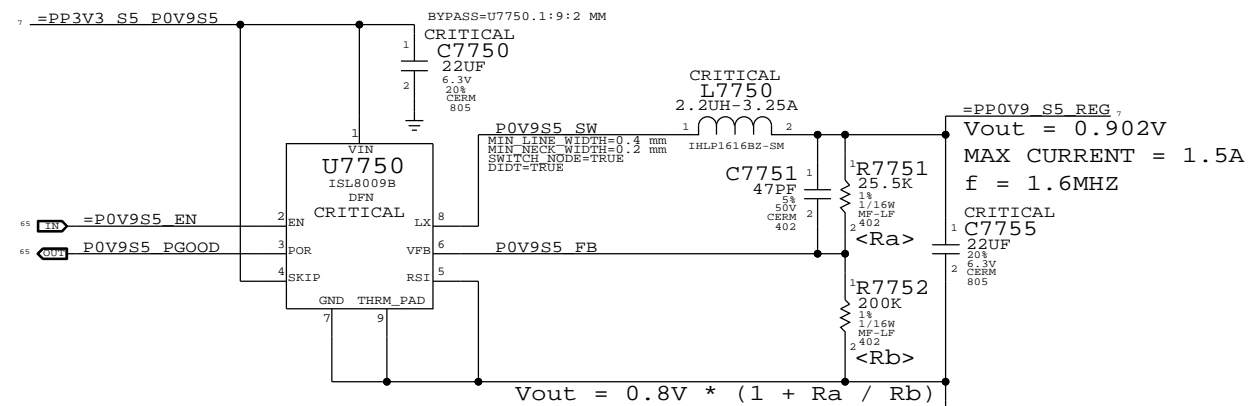
1.5V S0 Regulator



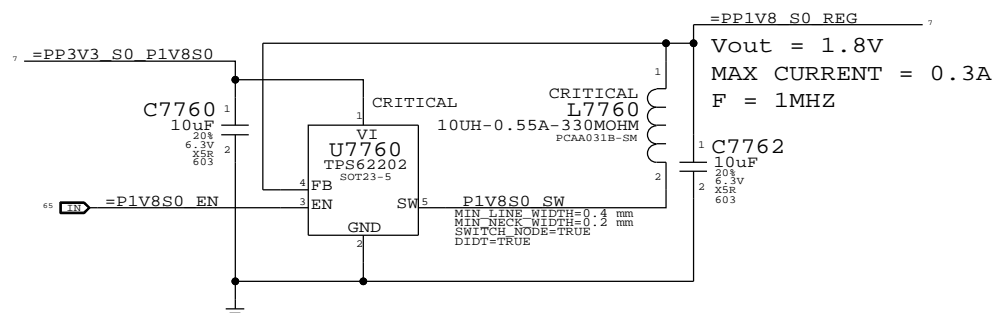
BOMOPTIONS:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.


MCP 0.9V S5 (AUXC) Switcher



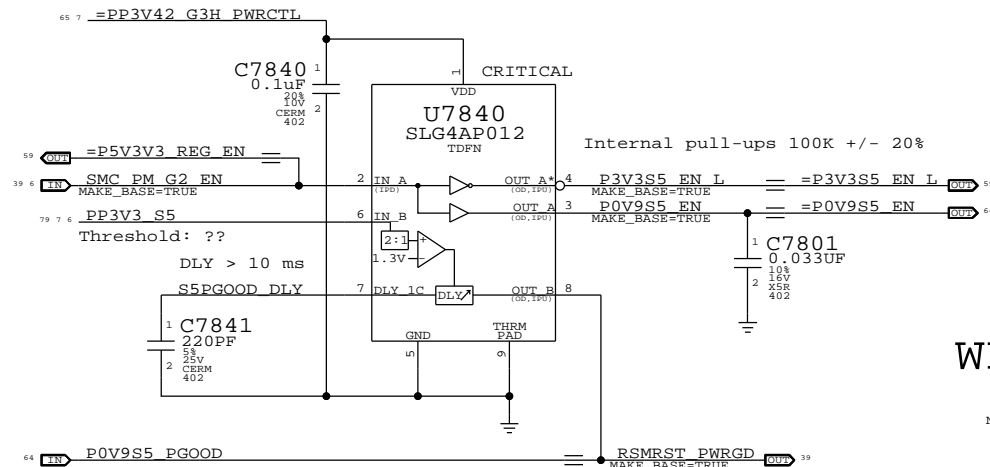
1.8V S0 Switcher



K6 NOTES : C7710 AND C7750 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC MASTER=T27 MLB		SYNC DATE=09/30/2009	
PAGE TITLE			
Misc Power Supplies			
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			SIZE D
		REVISION A.13.0	
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S5 Rail Enables & PGOOD



Power Control Signals

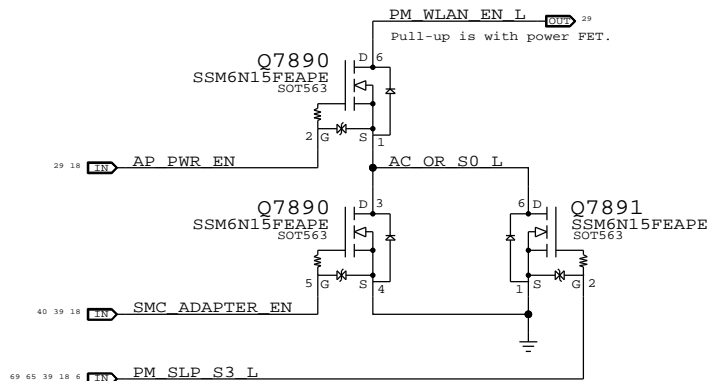
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

WLAN Enable Generation

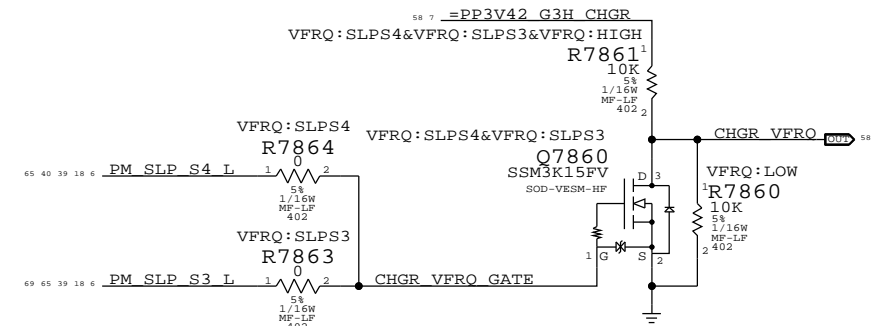
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

Pull-up is with power FET.

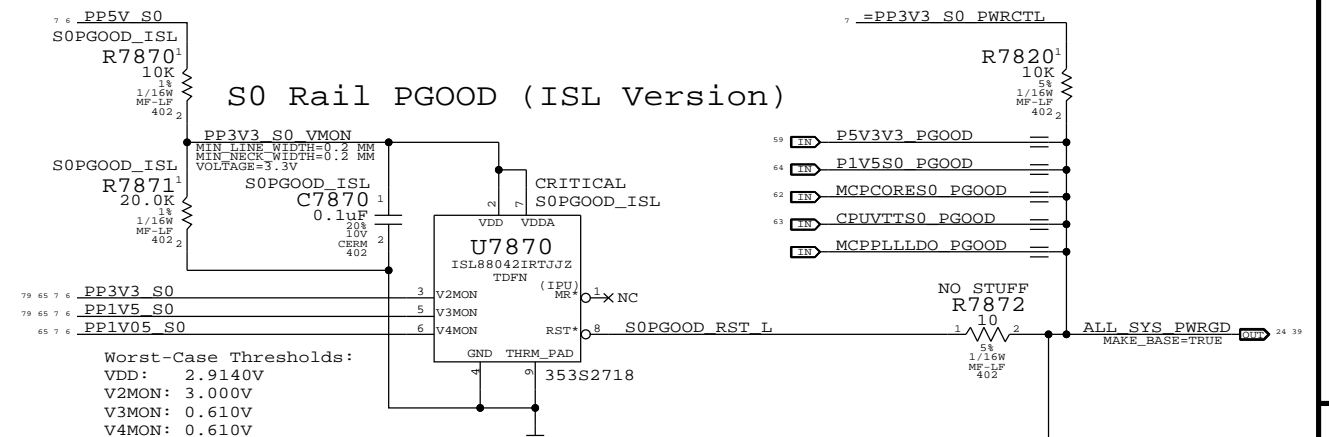


ISL6259 Frequency Select

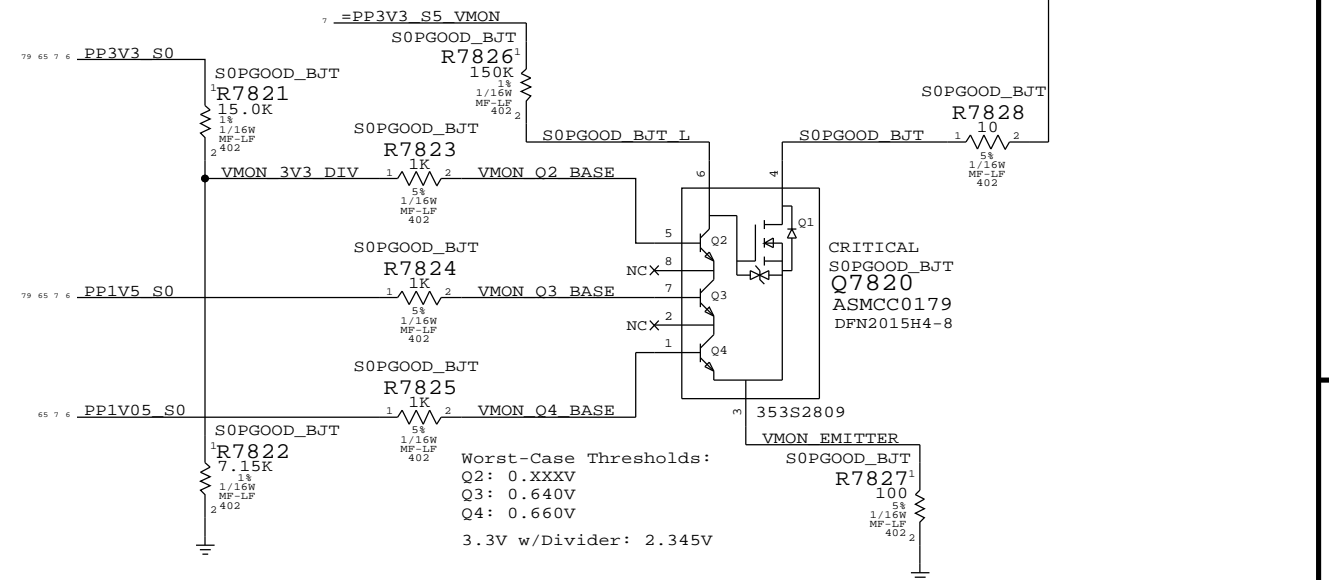


S0 Rail PGOOD Circuitry

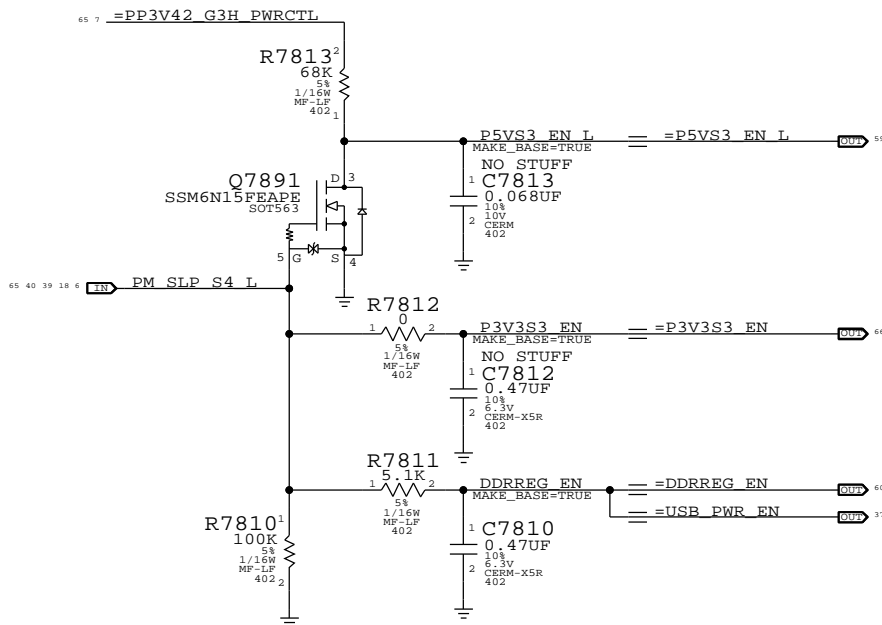
S0 Rail PGOOD (ISL Version)



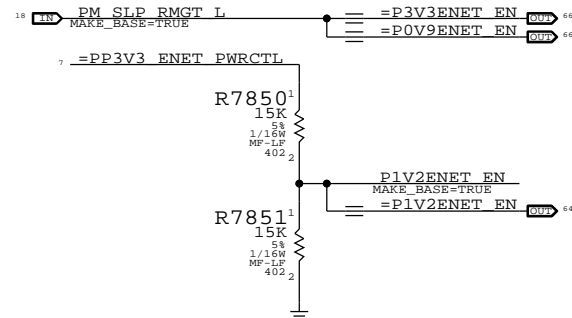
S0 Rail PGOOD (BJT Version)



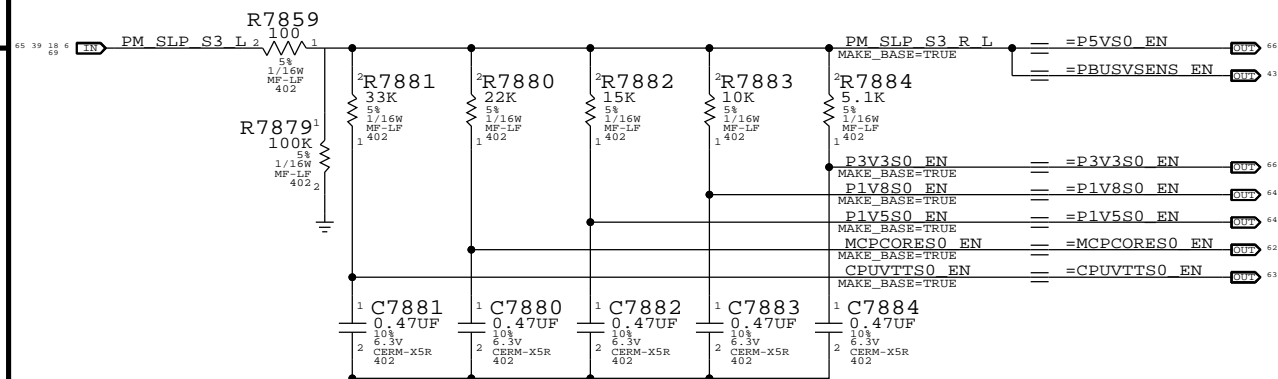
S3 Rail Enables



ENET Rail Enables



S0 Rail Enables



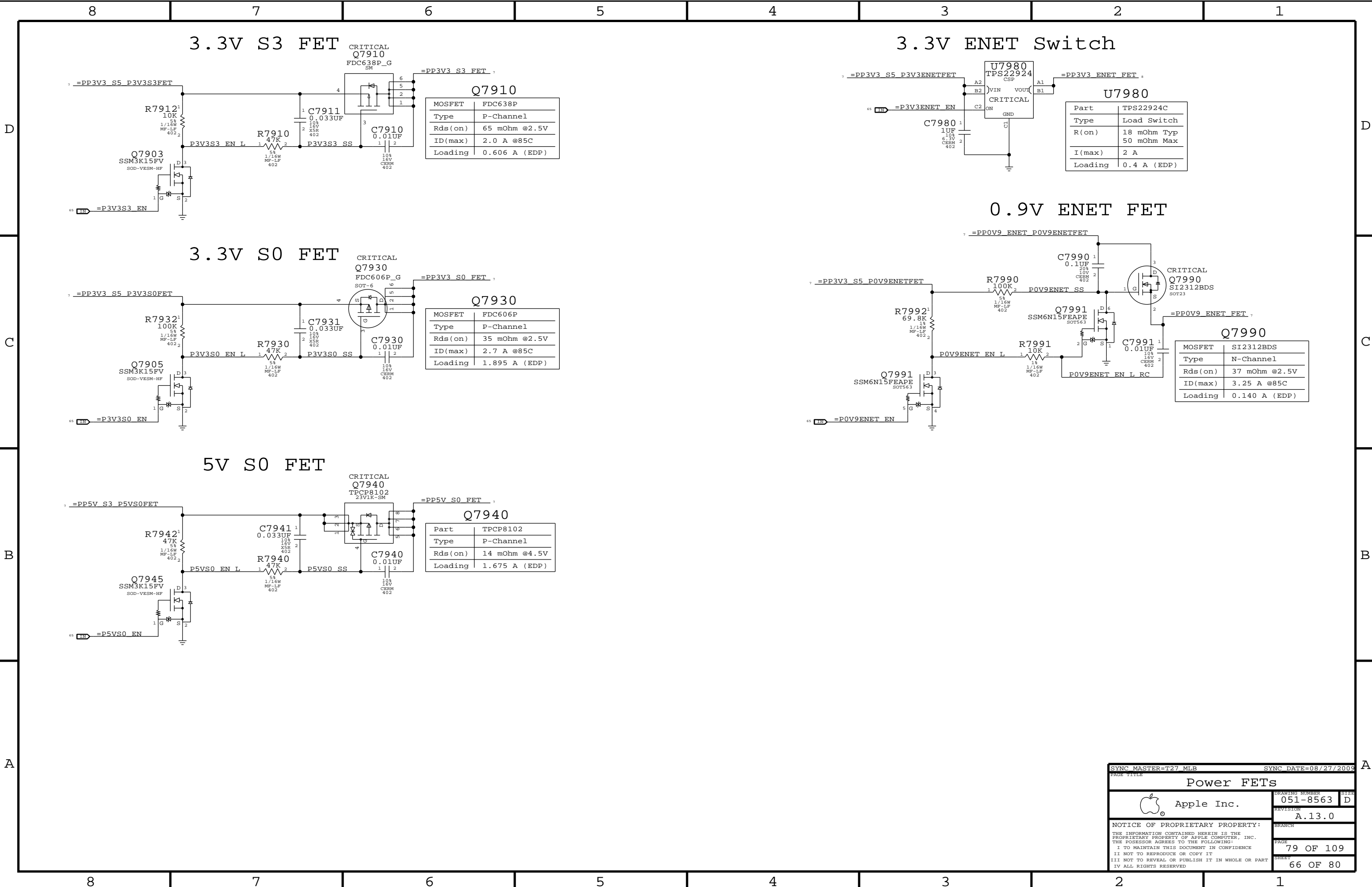
VTT Rail Enable

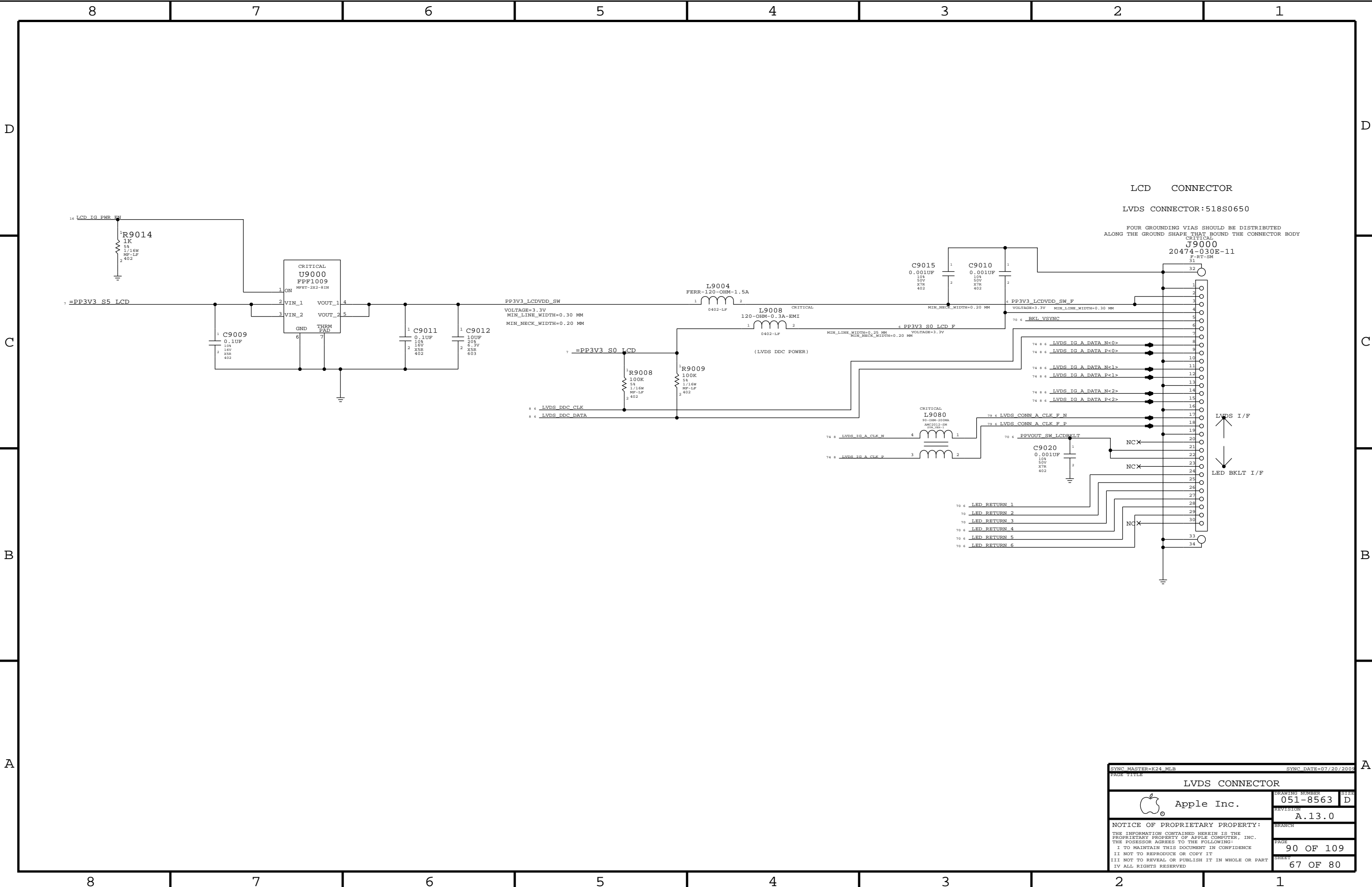
VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).




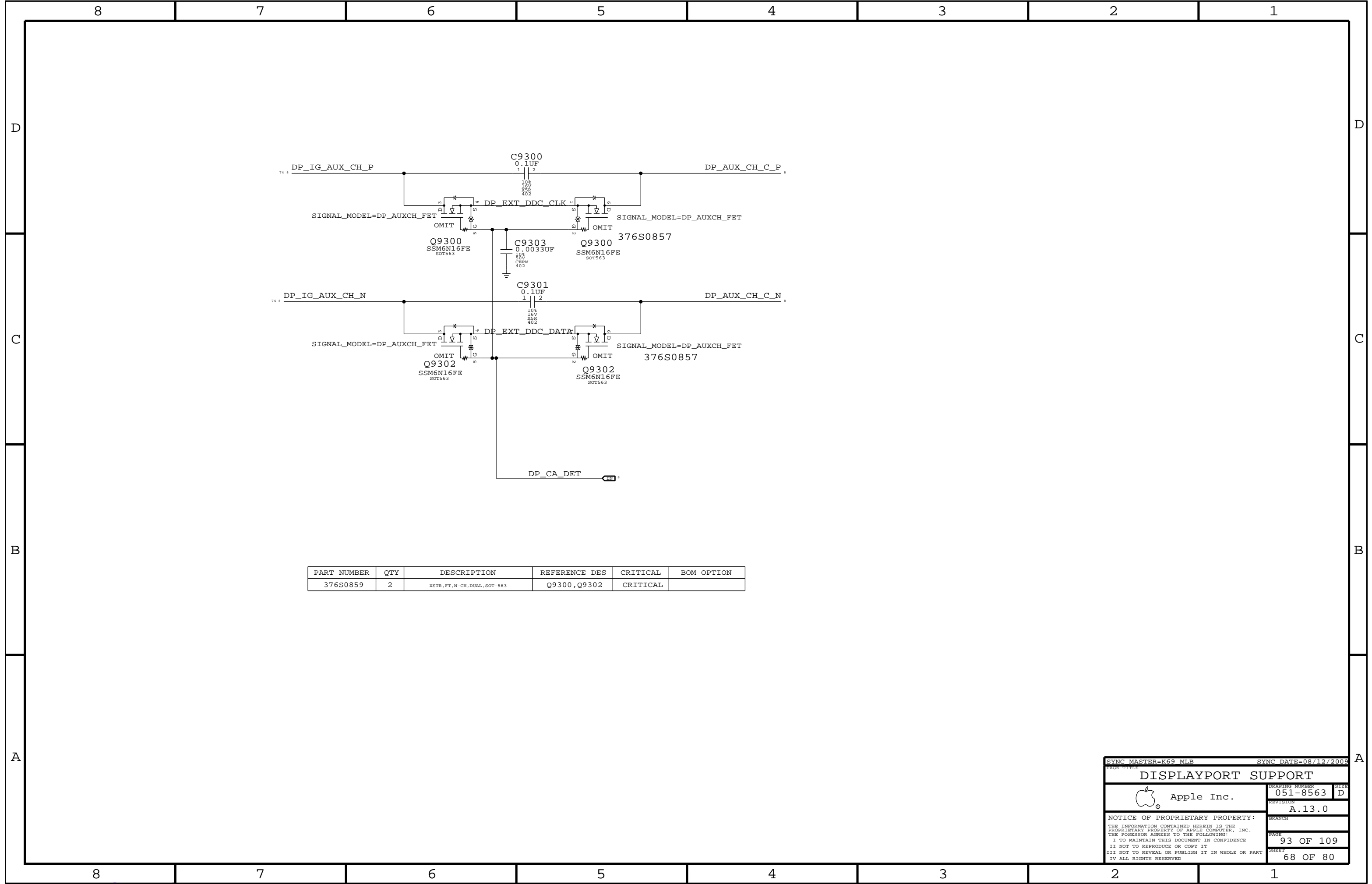
K6 HAS A PULL UP ON DDRREG_PGOOD. REMOVED ALIAS TO TP SIGNAL

SYNC MASTER=T27 MLB	SYNC DATE=11/24/2009
PAGE TITLE	Power Sequencing
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LVDS CONNECTOR			
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0859	2	XSTR,PT,N-CH,DUAL,SOT-563	Q9300,Q9302	CRITICAL	

SYNC MASTER=K69_MLB

SYNC DATE=08/12/2009

DISPLAYPORT SUPPORT

 Apple Inc.

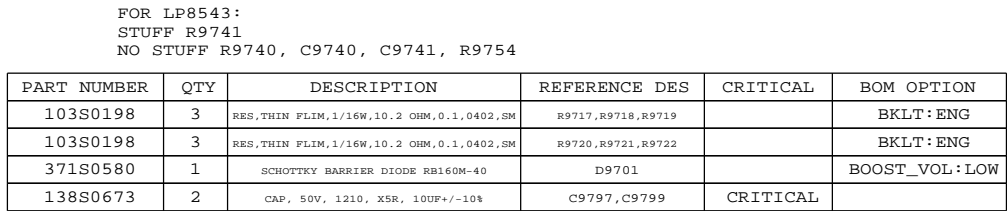
051-8563


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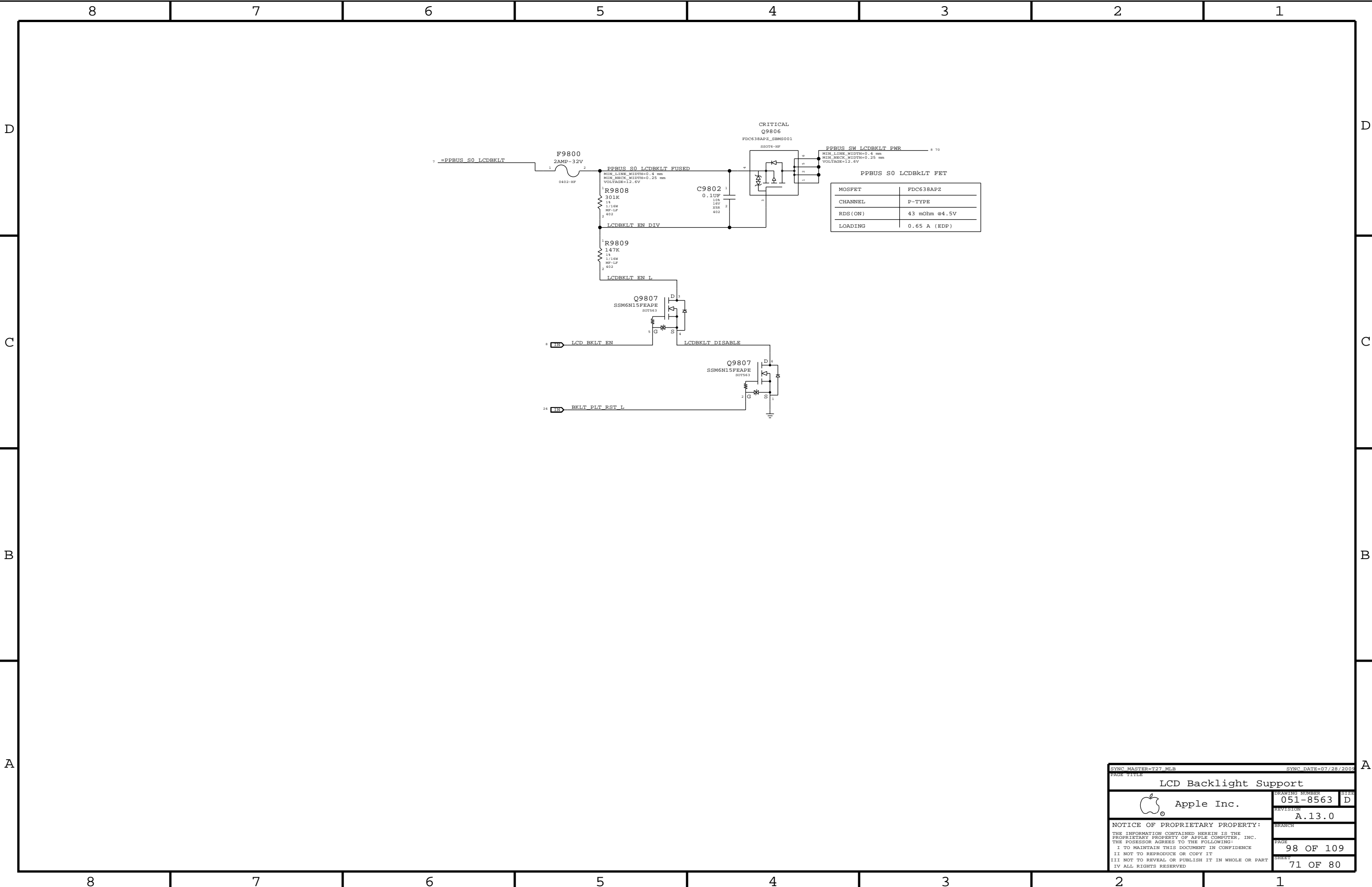
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SYNC MASTER=K69 MLB		SYNC DATE=08/27/2009	
PAGE TITLE			
LCD Backlight		Drawer	
 Apple Inc.		Drawing Number	Size
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		A.13.0	
		Branch	
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SYNC MASTER=T27_MLB

SYNC DATE=07/28/2009

LCD Backlight Support

 Apple Inc.

DRAWING NUMBER

051-8563

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87654321

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	9 13
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	9 13
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	9 13
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	9 13
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	9 13
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	9 13
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	9 13
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	9 13
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	9 13
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	9 13
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	9 13
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	9 13
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	9 13
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	9 13
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	9 13
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	9 13
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	9 13
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	9 13
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	9 13
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	9 13
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	9 13
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	9 13
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	9 13
FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 13 61
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	9 13
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	9 13
CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNE L	9 13
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	9 13
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	9 13
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	9 13
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	9 13 40 61
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	9 12 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	9 13
PM_THERMTRIP_L	CPU_50S	CPU_8MIL	PM_THERMTRIP_L	9 13 40
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	9 13
CPU_FROM_SR	CPU_50S	CPU_AGTL	CPU DPSLP L	9 13
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 13 61
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	9 13
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	9 13
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	9 13
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	12 13
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	12 13
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	13
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	13
CPU_IERR_L	CPU_50S		CPU_IERR L	9
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	13 61
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	61
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	13
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	13
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	9 28
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	9
CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	9
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	9
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	9 12
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	9 12
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	9 12
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	9 12
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	9 12
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>	9 12
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>	9 12
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	12
	CPU_50S	CPU_8MIL	CPU VID<6..0>	10 61
	CPU_50S	CPU_8MIL	IMVP6 VID<6..0>	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	10 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	10 61
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 270 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	9 13
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	9 13
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	9 13
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	9 13
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	9 13
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	9 13
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	9 13
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	9 13
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	9 13
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	9 13
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	9 13
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	9 13
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	9 13
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	9 13
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	9 13
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	9 13
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	9 13
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	9 13
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	9 13
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	9 13
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	9 13
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	9 13
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	9 13
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	9 13
FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 13 61
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	9 13
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	9 13
CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNE L	9 13
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	9 13
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	9 13
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	9 13
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	9 13 40 61
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	9 12 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	9 13
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	9 13
PM_THERMTRIP_L	CPU_50S	CPU_8MIL	PM_THERMTRIP_L	9 13 40
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	9 13
CPU_FROM_SR	CPU_50S	CPU_AGTL	CPU DPSLP L	9 13
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 13 61
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	9 13
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	9 13
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	

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1

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20OTHER	*	25 MIL	?

NV DG says 3x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 2x inner, 4x outer

NV DG says 4x inner, 5x outer

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20OTHER
MEM_CTRL	*	*	MEM_20OTHER
MEM_CMD	*	*	MEM_20OTHER
MEM_DATA	*	*	MEM_20OTHER
MEM_DQS	*	*	MEM_20OTHER

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

CMD/CTRL signals should be matched within 150 ps.

All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

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MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>	14 25
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>	14 25
MEM_A_CKE	MEM_40S	MEM_CTRL	MEM A CKE<3..0>	14 20 25
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM A CS L<3..0>	14 25
MEM_A_CNTL	MEM_40S	MEM_CTRL	MEM A ODT<3..0>	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	14 25
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	14 25
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	14 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	14 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	14 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	14 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	14 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	14 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	14 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	14 27
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	14 27
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	14 27
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	14 27
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	14 27
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	14 27
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	14 27
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	14 27
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	14 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	14 27
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	14 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	14 27
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	14 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	14 27
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	14 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	14 27
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	14 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	14 27
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	14 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	14 27
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	14 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	14 27
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	14 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	14 27
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	14 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>	14 26
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>	14 26
MEM_B_CKE	MEM_40S	MEM_CTRL	MEM B CKE<3..0>	14 20 26
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM B CS L<3..0>	14 26
MEM_B_CNTL	MEM_40S	MEM_CTRL	MEM B ODT<3..0>	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	14 26
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	14 26
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	14 27
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	14 27
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	14 27
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	14 27
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	14 27
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	14 27
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	14 27
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	14 27
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	14 27
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	14 27
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	14 27
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	14 27
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	14 27
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	14 27
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	14 27
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	14 27
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	14 27
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	14 27
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	14 27
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	14 27
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	14 27
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	14 27
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	14 27
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	14 27
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	14 27
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	14 27
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	14 27
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	14 27
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	14 27
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	14 27
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	14 27
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	14 27
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	14
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	14

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

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SYNC MASTER=T27 MLB

SYNC DATE=08/03/2009

Memory Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PEG R2D P<15..0>
	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
	PCIE_90D	PCIE	PEG D2R N<15..0>
	PCIE_90D	PCIE	PEG D2R C P<15..0>
	PCIE_90D	PCIE	PEG D2R C N<15..0>
	PCIE_90D	PCIE	PCIE AP R2D P
	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
	PCIE_90D	PCIE	PCIE AP D2R N
	PCIE_90D	PCIE	PCIE ENET R2D P
	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
	PCIE_90D	PCIE	PCIE ENET D2R N
	PCIE_90D	PCIE	PCIE ENET D2R C P
	PCIE_90D	PCIE	PCIE ENET D2R C N
	PCIE_90D	PCIE	PCIE FW R2D P
	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
	PCIE_90D	PCIE	PCIE FW D2R N
	PCIE_90D	PCIE	PCIE FW D2R C P
	PCIE_90D	PCIE	PCIE FW D2R C N
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PE1_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PE2_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PE3_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP PEX0 TERMP
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP TV_DAC RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP TV_DAC VREF
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS IG TXC P
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS IG TXC N
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS IG TXD P<5..0>
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS IG TXD N<5..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH N
MCP_TMDS0_RSET	MCP_DV_COMP		MCP TMDS0 RSET
MCP_TMDS0_VPROBE			MCP TMDS0 VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP IFPAB RSET
MCP_IFPAB_VPROBE			MCP IFPAB VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
	SATA_90D	SATA	SATA HDD R2D C N
	SATA_90D	SATA	SATA HDD R2D P
	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
	SATA_90D	SATA	SATA HDD D2R N
	SATA_90D	SATA	SATA HDD D2R C P
	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
	SATA_90D	SATA	SATA ODD R2D C N
	SATA_90D	SATA	SATA ODD R2D P
	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
	SATA_90D	SATA	SATA ODD D2R N
	SATA_90D	SATA	SATA ODD D2R C P
	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERM		SATA_TERM	MCP SATA TERMP

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIA5	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	= 1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	LPC_AD	LPC_55S	LPC	LPC AD<3..0>	18 39 41
	LPC_FRAME_L	LPC_55S	LPC	LPC FRAME_L	18 39 41
	LPC_RESET_L	LPC_55S	LPC	LPC RESET_L	18 24
	MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC_R	18 24
		CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	24 39
		CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	24 41
	USB_EXTN	USB_90D	USB	USB_EXTN_P	17 37
		USB_90D	USB	USB_EXTN_N	17 37
		USB_90D	USB	USB_EXTN_MUXED_P	37 79
		USB_90D	USB	USB_EXTN_MUXED_N	37 79
	USB_MINI	USB_90D	USB	USB_MINI_P	8 17
		USB_90D	USB	USB_MINI_N	8 17
	USB_EXTD	USB_90D	USB	USB_EXTD_P	8 17
		USB_90D	USB	USB_EXTD_N	8 17
	USB_CAMERA	USB_90D	USB	USB_CAMERA_P	17 29
		USB_90D	USB	USB_CAMERA_N	17 29
	USB_BT	USB_90D	USB	USB_BT_P	17 29
		USB_90D	USB	USB_BT_N	17 29
	USB_TPAD	USB_90D	USB	USB_TPAD_P	17 47
		USB_90D	USB	USB_TPAD_N	17 47
	USB_IR	USB_90D	USB	USB_IR_P	17 38
		USB_90D	USB	USB_IR_N	17 38
	USB_EXTR	USB_90D	USB	USB_EXTR_P	17 37
		USB_90D	USB	USB_EXTR_N	17 37
	USB_T57	USB_90D	USB	USB_T57_P	6 38
		USB_90D	USB	USB_T57_N	6 38
	USB_EXTC	USB_90D	USB	USB_EXTC_P	8 17
		USB_90D	USB	USB_EXTC_N	8 17
	USB_SDCARD	USB_90D	USB	USB_SDCARD_P	17 30
		USB_90D	USB	USB_SDCARD_N	17 30
	USB_WM	USB_90D	USB	USB_WM_P	8 17
		USB_90D	USB	USB_WM_N	8 17
	MCP_USB_RBIA5	MCP_USB_RBIA5		MCP_USB_RBIA5_GND	17
	SMBUS_MCP_0_CLK	SMR_55S	SMR	SMBUS_MCP_0_CLK	12 18 42
	SMBUS_MCP_0_DATA	SMR_55S	SMR	SMBUS_MCP_0_DATA	12 18 42
	(SMBUS_SMC_MGMT_SCL)	SMR_55S	SMR	SMBUS_MCP_1_CLK	18 42
	(SMBUS_SMC_MGMT_SDA)	SMR_55S	SMR	SMBUS_MCP_1_DATA	18 42
	HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	18 51
		HDA_55S	HDA	HDA_BIT_CLK_R	18
	HDA_SYNC	HDA_55S	HDA	HDA_SYNC	18 51
		HDA_55S	HDA	HDA_SYNC_R	18
	HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	18
		HDA_55S	HDA	HDA_RST_L	18 51
	HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	18 51
		HDA_55S	HDA	HDA_SDIN_CODEC	
	HDA_SDOU1T	HDA_55S	HDA	HDA_SDOU1T	18 51
		HDA_55S	HDA	HDA_SDOU1T_R	18
	MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	18
	MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	18 24
		CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	24 39
	SPI_CLK	SPT_55S	SPT	SPI_CLK_R	18 41
		SPT_55S	SPT	SPI_CLK	6 41
	SPI_MOSI	SPT_55S	SPT	SPI_MOSI_R	18 41
		SPT_55S	SPT	SPI_MOSI	6 41
	SPI_MISO	SPT_55S	SPT	SPI_MISO	6 18 41
	SPI_CS0	SPT_55S	SPT	SPI_CS0_R_L	18 41
		SPT_55S	SPT	SPI_CS0_L	6 41
		SPT_55S	SPT	SPI_MLB_CLK	41 50
		SPT_55S	SPT	SPI_MLB_MOSI	41 50
		SPT_55S	SPT	SPI_MLB_MISO	41 50
		SPT_55S	SPT	SPI_MLB_CS_L	41 50
		SPT_55S	SPT	SPI_ALT_CLK	41
		SPT_55S	SPT	SPI_ALT_MOSI	41
		SPT_55S	SPT	SPI_ALT_MISO	41
		SPT_55S	SPT	SPI_ALT_CS_L	41

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?




















SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

SD Card Interface Constraints



PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?















RGMII Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD	17
	MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND	17
	MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M_BUF0_R	
		ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	
	ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
	ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	8 17
	ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	
	ENET_PWDOWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDOWN_L	
	ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	
		ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	8 17
		ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	
	ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<0>	8 17
	ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	8 17
	ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	8 17
	ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	
	ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	
	ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	
	ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	
		ENET_MII_55S	ENET_MII	ENET_RESET_L	24 31

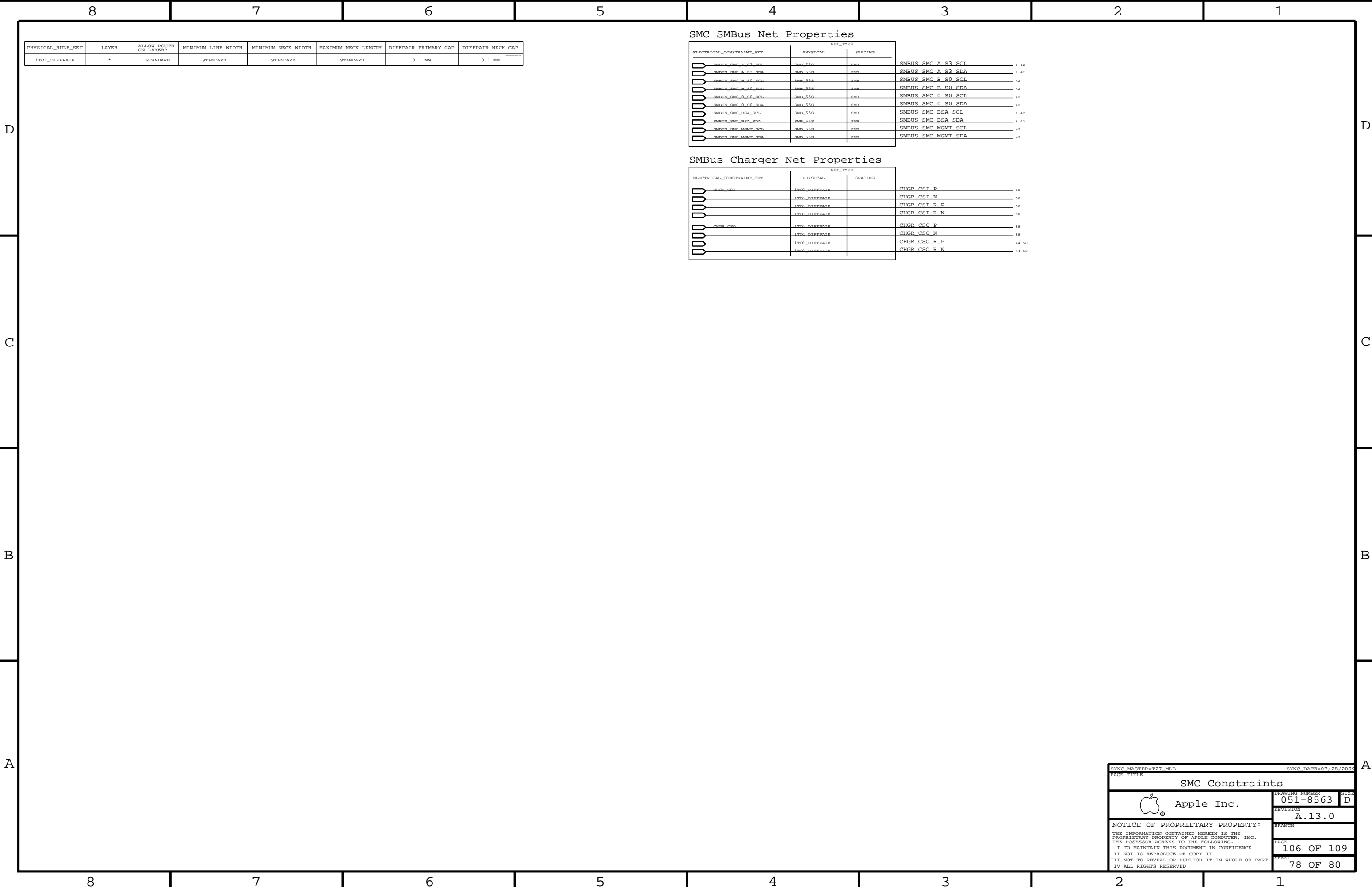
Ethernet Net Properties

		NET_TYPE		
ELECTRICAL_CONSTRAINT_SET		PHYSICAL	SPACING	
	ENET_MDI	ENET_MDI_100M	ENET_MDI	ENET MDI P<3..0> 31 32
		ENET_MDI_100M	ENET_MDI	ENET MDI N<3..0> 31 32

SD Card Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SD_DATA	SD_55S	SD_INTERFACE	SD D<4..0>
		SD_55S	SD_INTERFACE	SDCONN DATA<4..0>
		SD_55S	SD_INTERFACE	SDCONN DATA<4..0>
		SD_55S	SD_INTERFACE	SDCONN DATA<4..0>
	SD_DATA_R	SD_55S	SD_INTERFACE	SD D<7..5>
		SD_55S	SD_INTERFACE	SDCONN DATA<7..5>
		SD_55S	SD_INTERFACE	SDCONN DATA<7..5>
		SD_55S	SD_INTERFACE	SDCONN DATA<7..5>
	SD_CLK	SD_55S	SD_INTERFACE	SD CLK
		SD_55S	SD_INTERFACE	SD CLK R
		SD_55S	SD_INTERFACE	SDCONN CLK
	SD_CMD	SD_55S	SD_INTERFACE	SD CMD
		SD_55S	SD_INTERFACE	SDCONN CMD
		SD_55S	SD_INTERFACE	SDCONN CMD

NOTE: SD_D<7..5> are different to support BCM5764M/BCM57765 co-layout.



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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	(PCIE_AD)	CLK_PCIE 100D	CLK_PCIE	PCIE CLK100M AP CONN P	6 29
		CLK_PCIE 100D	CLK_PCIE	PCIE CLK100M AP CONN N	6 29
	(USB_EXT_A)	USB_90D	USB	USB_EXT_A MUXED P	37 75
	(USB_EXT_A)	USB_90D	USB	USB_EXT_A MUXED N	37 75
	(USB_EXT_A)	USB_90D	USB	USB LT1 P	37
	(USB_EXT_A)	USB_90D	USB	USB LT1 N	37
	(USB_TP_A)	USB_90D	USB	USB TP_A R P	47
	(USB_TP_A)	USB_90D	USB	USB TP_A R N	47
	(USB_CAMERA)	USB_90D	USB	USB CAMERA CONN P	6 29
	(USB_CAMERA)	USB_90D	USB	USB CAMERA CONN N	6 29
		USB_90D	USB	USB BT CONN P	6 29
		USB_90D	USB	USB BT CONN N	6 29
		USB_90D	USB	USB LT2 P	37
		USB_90D	USB	USB LT2 N	37
		ENET_MDI 100D	ENETCONN	ENETCONN P<3..0>	32
		ENET_MDI 100D	ENETCONN	ENETCONN N<3..0>	32
		SATA_90D	SATA	SATA ODD R2D UF P	36
		SATA_90D	SATA	SATA ODD R2D UF N	36
		SATA_90D	SATA	SATA ODD D2R UF P	6 36
		SATA_90D	SATA	SATA ODD D2R UF N	6 36
		SATA_90D	SATA	SATA HDD D2R UF P	36
		SATA_90D	SATA	SATA HDD D2R UF N	36
		SATA_90D	SATA	SATA HDD R2D UF P	36
		SATA_90D	SATA	SATA HDD R2D UF N	36
		SATA_90D	SATA	SATA HDD D2R RDRV IN P	36
		SATA_90D	SATA	SATA HDD D2R RDRV IN N	36
		SATA_90D	SATA	SATA HDD R2D RDRV IN P	36
		SATA_90D	SATA	SATA HDD R2D RDRV IN N	36
		SATA_90D	SATA	SATA HDD D2R RDRV OUT P	36
		SATA_90D	SATA	SATA HDD D2R RDRV OUT N	36
		SATA_90D	SATA	SATA HDD R2D RDRV OUT P	36
		SATA_90D	SATA	SATA HDD R2D RDRV OUT N	36
		SATA_90D	SATA	SATA HDD D2R NORDRV P	36
		SATA_90D	SATA	SATA HDD D2R NORDRV N	36
		SATA_90D	SATA	SATA HDD R2D NORDRV P	36
		SATA_90D	SATA	SATA HDD R2D NORDRV N	36

Graphics Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
		LVDS_100P	LVDS	LVDS_CONN A CLK P	
		LVDS_100P	LVDS	LVDS_CONN A CLK N	
		LVDS_100P	LVDS	LVDS_CONN A CLK F P	6 67
		LVDS_100P	LVDS	LVDS_CONN A CLK F N	6 67
		LVDS_100P	LVDS	LVDS_CONN A DATA P<2..0>	
		LVDS_100P	LVDS	LVDS_CONN A DATA N<2..0>	
		LVDS_100P	LVDS	LVDS_CONN B CLK P	
		LVDS_100P	LVDS	LVDS_CONN B CLK N	
		LVDS_100P	LVDS	LVDS_CONN B CLK F P	
		LVDS_100P	LVDS	LVDS_CONN B CLK F N	
		LVDS_100P	LVDS	LVDS_CONN B DATA P<2..0>	
		LVDS_100P	LVDS	LVDS_CONN B DATA N<2..0>	
	(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP_EXT_ML P<3..0>	8 69
		DP_90D	DISPLAYPORT	DP_EXT_ML N<3..0>	8 69
		DP_90D	DISPLAYPORT	DP_EXT_ML C P<3..0>	69
		DP_90D	DISPLAYPORT	DP_EXT_ML C N<3..0>	69
		DP_90D	DISPLAYPORT	DP_EXT_ML F P<3..0>	69
		DP_90D	DISPLAYPORT	DP_EXT_ML F N<3..0>	69
	(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP_EXT_AUX_CH C P	8 69
		DP_90D	DISPLAYPORT	DP_EXT_AUX_CH C N	8 69
		DP_90D	DISPLAYPORT	DP_AUX_CH_SW_P	
		DP_90D	DISPLAYPORT	DP_AUX_CH_SW_N	

Power Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	CPU1THMSNS_D2	THERM 1T01 55S	THERM	CPUTHMSNS D2 P 45
		THERM 1T01 55S	THERM	CPUTHMSNS D2 N
	CPU_THERMD	THERM 1T01 55S	THERM	CPU_THERMD P 9 45
		THERM 1T01 55S	THERM	CPU_THERMD N 9 45
	MCPTHMSNS_D2	THERM 1T01 55S	THERM	MCPTHMSNS D2 P
		THERM 1T01 55S	THERM	MCPTHMSNS D2 N
	MCP_THMDIODE	THERM 1T01 55S	THERM	MCP_THMDIODE P 18 45
		THERM 1T01 55S	THERM	MCP_THMDIODE N 18 45
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS 1V5 S3 P
		SENSE 1T01 55S	SENSE	ISNS 1V5 S3 N
		SENSE 1T01 55S	SENSE	ISNS 1V5 S3 R P
		SENSE 1T01 55S	SENSE	ISNS 1V5 S3 R N
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS AIRPORT P
		SENSE 1T01 55S	SENSE	ISNS AIRPORT N
		SENSE 1T01 55S	SENSE	ISNS AIRPORT R P
		SENSE 1T01 55S	SENSE	ISNS AIRPORT R N
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS HDD P
		SENSE 1T01 55S	SENSE	ISNS HDD N
		SENSE 1T01 55S	SENSE	ISNS HDD R P
		SENSE 1T01 55S	SENSE	ISNS HDD R N
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS LCDCLKLT P
		SENSE 1T01 55S	SENSE	ISNS LCDCLKLT N
		SENSE 1T01 55S	SENSE	ISNS LCDCLKLT R P
		SENSE 1T01 55S	SENSE	ISNS LCDCLKLT R N
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS ODD P
		SENSE 1T01 55S	SENSE	ISNS ODD N
		SENSE 1T01 55S	SENSE	ISNS ODD R P
		SENSE 1T01 55S	SENSE	ISNS ODD R N
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS CPUVTT P 44
		SENSE 1T01 55S	SENSE	ISNS CPUVTT N 44
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	MCPCORES0 VSEN P 21 62
		SENSE 1T01 55S	SENSE	MCPCORES0 VSEN N 21 62
MEM			MEM_POWER	PP1V5R1V35 S3 6 7
			SB_POWER	PP3V3 S5 6 7 6
			SB_POWER	PP3V3 S0 6 7 6
			SB_POWER	PP1V5 S0 6 7 6
			GND	GND

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		DIFFPAIR	AUDIO	AUD SPKRAMP LIN P
		DIFFPAIR	AUDIO	AUD SPKRAMP LIN N
		DIFFPAIR	AUDIO	AUD SPKRAMP SUBIN P
		DIFFPAIR	AUDIO	AUD SPKRAMP SUBIN N
		DIFFPAIR	AUDIO	AUD SPKRAMP RIN P
		DIFFPAIR	AUDIO	AUD SPKRAMP RIN N
		DIFFPAIR	AUDIO	SSM2315L P
		DIFFPAIR	AUDIO	SSM2315L N
		DIFFPAIR	AUDIO	SSM2315S P
		DIFFPAIR	AUDIO	SSM2315S N
		DIFFPAIR	AUDIO	SSM2315R P
		DIFFPAIR	AUDIO	SSM2315R N
	SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN L OUT P
		DIFFPAIR	AUDIO	SPKRCONN L OUT N
	SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN S OUT P
		DIFFPAIR	AUDIO	SPKRCONN S OUT N
	SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN R OUT P
		DIFFPAIR	AUDIO	SPKRCONN R OUT N
		DIFFPAIR	AUDIO	BI MIC P
		DIFFPAIR	AUDIO	BI MIC N
		DIFFPAIR	AUDIO	HS MIC P
		DIFFPAIR	AUDIO	HS MIC N

K6/K69 Board-Specific Physical & Spacing Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.080 MM	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.151 MM	0.109 MM	=STANDARD	0.224 MM	0.090 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	1SL3, 1SL4, 1SL9, 1SL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	1SL3, 1SL4, 1SL9, 1SL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	1SL3, 1SL4, 1SL9, 1SL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1_5X_DIELECTRIC	TOP,BOTTOM	0.105 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
1_5X_DIELECTRIC	*	0.095 MM	?
2X_DIELECTRIC	*	0.126 MM	?
3X_DIELECTRIC	*	0.189 MM	?
4X_DIELECTRIC	*	0.252 MM	?
5X_DIELECTRIC	*	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_LPC	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA	STANDARD

SYNCH MASTER=T27 MLB		SYNCH DATE=08/06/2009	
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