1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
C		681298	PRODUCTION RELEASED	03/11/09	?

M97A MLB SCHEMATIC

REFERENCED FROM T18
03/11/2009

POST-RAMP

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7918	1	SCHEM,MLB,M97A	SCH	CRITICAL	
820-2327	1	PCBF,MLB,M97	PCB	CRITICAL	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

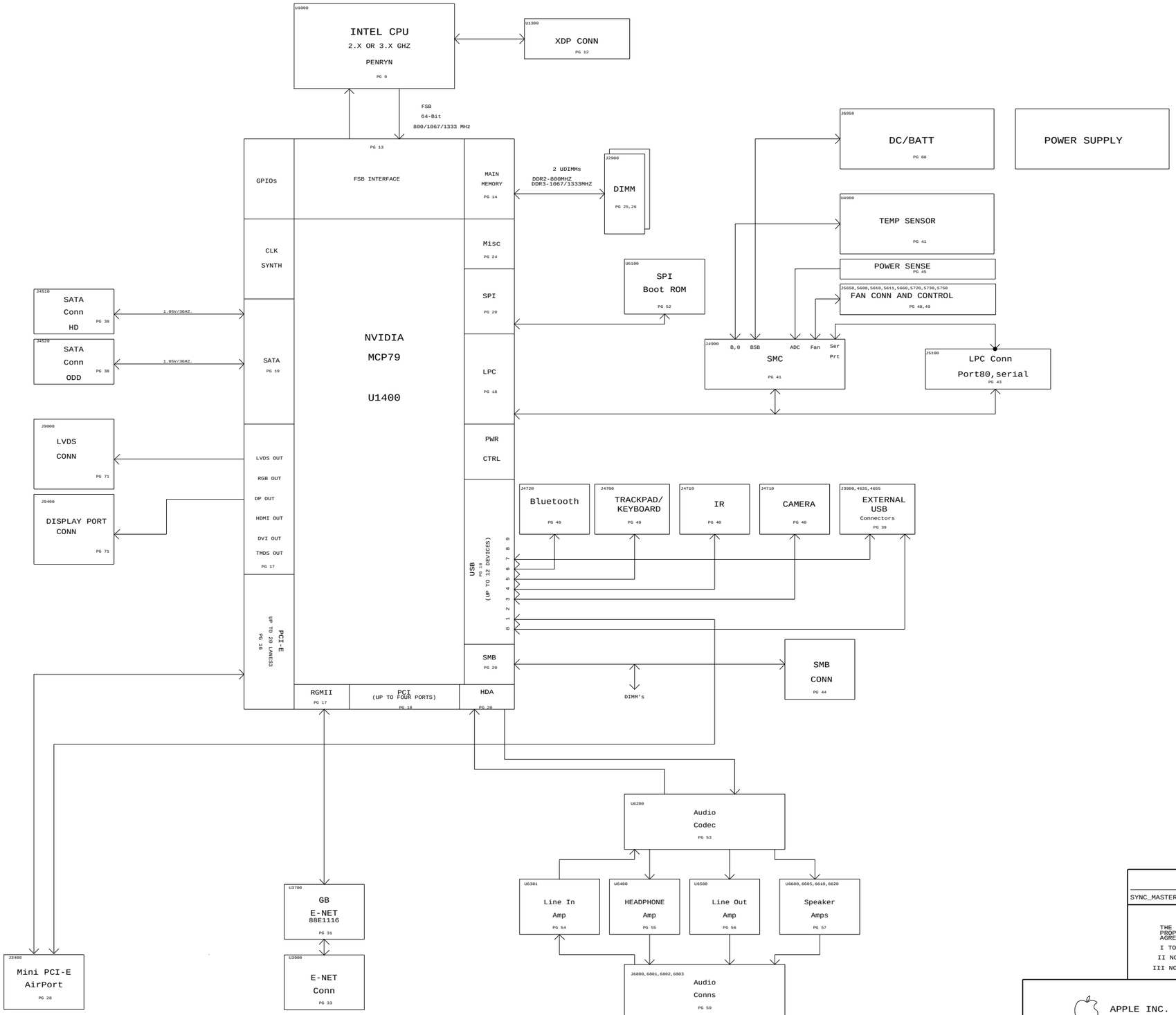
SIZE D

APPLE INC.

TITLE
SCHEM,MLB,M97A

DRAWING NUMBER 051-7918 REV. C

SHT 1 OF 109



System Block Diagram

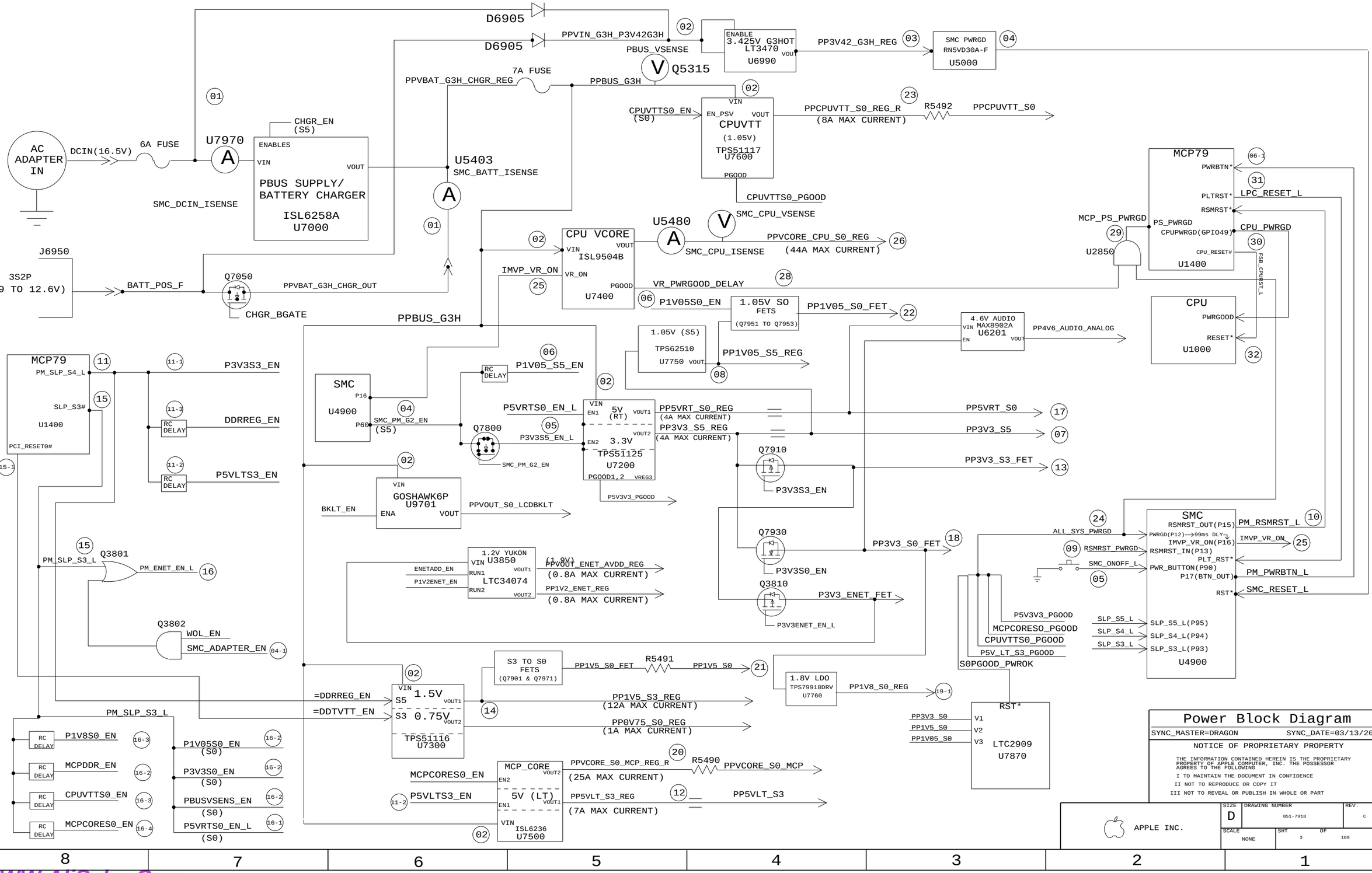
SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	2	109

M97 POWER SYSTEM ARCHITECTURE



BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9937	PCBA,MLB,BETTER,M97A	M97A_COMMON,CPU_2_0GHZ,EEE_6KM
630-9938	PCBA,MLB,BEST,M97A	M97A_COMMON,CPU_2_4GHZ,EEE_6KN,KB_BL

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6KM]	CRITICAL	EEE_6KM
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6KN]	CRITICAL	EEE_6KN

BOM Groups

BOM GROUP	BOM OPTIONS
M97A_COMMON	COMMON,ALTERNATE,M97A_MCP,M97A_MISC,M97A_DEBUG_PROD,M97A_PROGPARTS
M97A_MCP	MCP_B02,MCP_PROD,MEMRESET_HW,MEMRESET_MCP,BOOT_MODE_USER,MCPSEQ_SMC,MCP_CS1_NO
M97A_MISC	ONEWIRE_PU,BKLT_PLL_NOT,DP_ESD,PROD_BMON,MIKEY
M97A_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
M97A_DEBUG_ENG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS,VREFMRGN,TPAD_DEBUG
M97A_DEBUG_PVT	SMC_DEBUG_YES,XDP,LPCPLUS,NO_VREFMRGN
M97A_DEBUG_PROD	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3693	1	PDC,SLGBE,PRQ,2.0,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3680	1	PDC,SLB4N,PRQ,2.4,25W,1066,R0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0635	1	IC,GMCP,MCP79,35X35MM,BGA1437,B02	U1400	CRITICAL	MCP_B02

Programmable Parts

338S0563	1	IC,SMC,HS8/2117,9X9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341S2444	1	IC,SMC,M97A	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2440	1	IC,PRGRM,EFI BOOTROM,UNLOCK,M97A	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97A	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2348	1	IC,WELLSPRING CONTROLLER,M97A	U5701	CRITICAL	WELLSPRING_PROG

LOCKED M97A BOOTROM IS 341S2442

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
152S0694	152S0138		ALL	MAGLAYERS AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
353S1381	353S1912		ALL	INTERSIL ISL69002 AS ALTERNATE
337S3646	337S3693		ALL	M0 CPU AS ALTERNATE FOR R0 CPU
337S3639	337S3680		ALL	M0 CPU AS ALTERNATE FOR R0 CPU
341S2287	341S2444		ALL	M97 SMC AS ALTERNATE
341S2285	341S2440		ALL	M97 BOOTROM AS ALTERNATE

M97 BOARD STACK-UP

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

BOM Configuration

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	4	109

Revision History

BOM CHANGES FROM M97:

- REMOVE U5850, L5850, R5854, R5855, C5850, C5855, J5815 ON BETTER BOM.
- STUFF R5932.
- CHANGE R6382 FROM 10K(114S315) TO 1K(114S0218).
- STUFF L6300.
- NOSTUFF L6301.
- UPDATE CCU APNS TO B0 STEPPING.
- UPDATE M97A 630 NUMBERS AND EEE CODES, AND 051 NUMBER.
- UPDATE 341 NUMBERS FOR SMC AND BOOTROM.
- CHANGE U3700 FROM 338S0570 TO 338S0094, REALTEK PHY WITH ALDPS FIXED.
- ADD BOLEX SODIMM CONNECTORS AS ALTERNATE
- CHANGE R9717-R9722 FROM 10.2OHM(103S0198) TO 0OHM(116S0004).
- CHANGE R9730 FROM 0.1OHM(114S0538) TO 0OHM(116S0004).
- CHANGE J3900 FROM 514-0596 TO 514-0636.
- CHANGE J4600 AND J4610 FROM 514-0606 TO 514-0638.
- CHANGE J9400 FROM 514-0610 TO 514-0637.
- ADD INTERSIL ISL6000(353S1381) AS ALTERNATE FOR TI REF3333(353S1912).

C

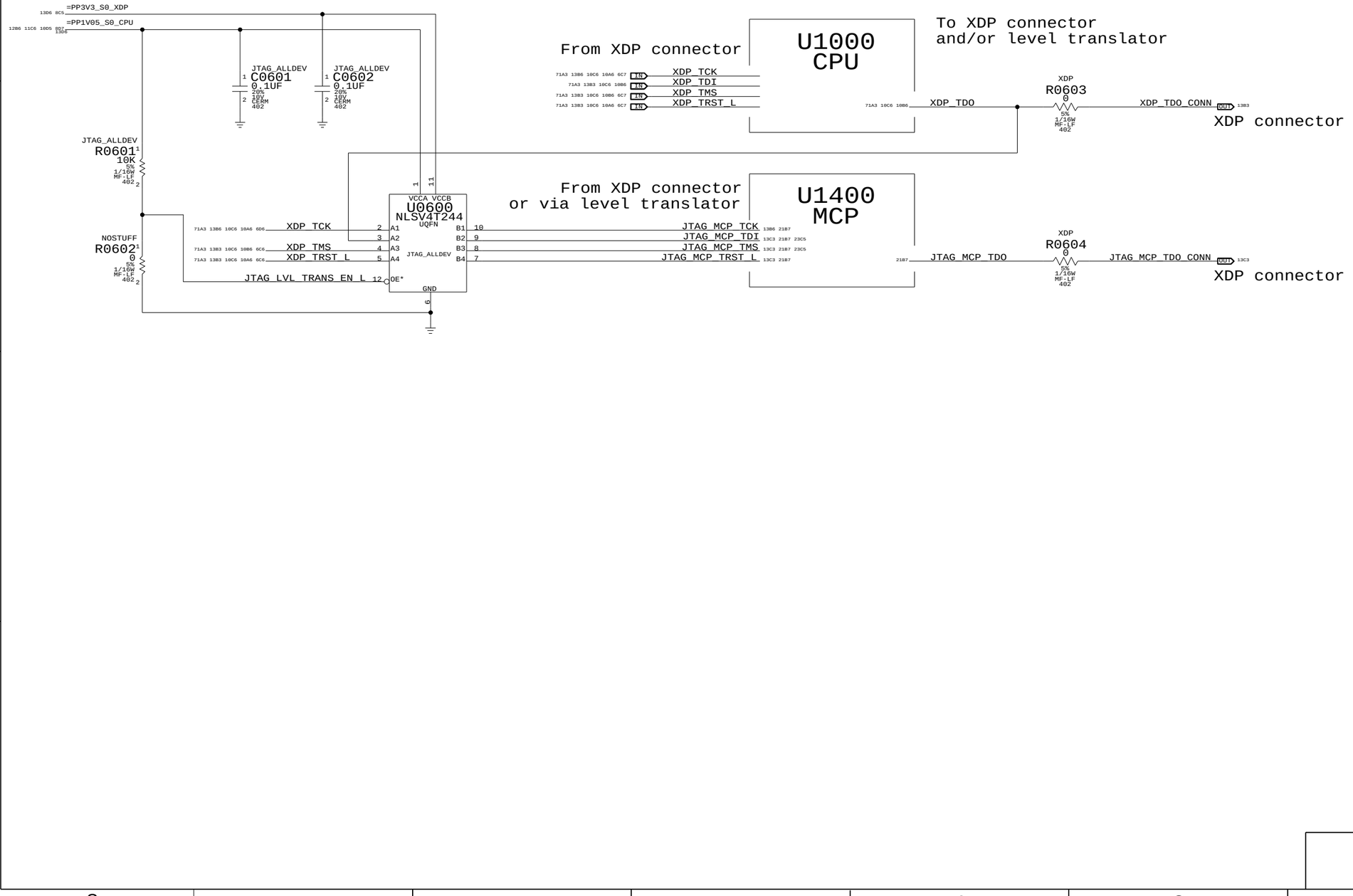
SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	5	109

NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

1.05V TO 3.3V LEVEL TRANSLATOR (M97: ON ICT FIXTURE)



JTAG Scan Chain

SYNC_MASTER=BEN SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	6	109

Functional Test Points

Fan Connectors

L14	TRUE	PP5VRT_S0	(NEED 3 TP) 7D3 8D5
L15	TRUE	FAN_RT_PWM	46B4
L16	TRUE	FAN_RT_TACH	46C4

(NEED TO ADD 3 GND TP)

MIC FUNC_TEST

F23D	TRUE	MIC_HI_CONN	54B1 54D2
F23F	TRUE	MIC_LO_CONN	54B1 54D2
F23G	TRUE	MIC_SHLD_CONN	54D2 55A6

SPEAKER FUNC_TEST

L22	TRUE	SPKRAMP_L_N_OUT	53B2 54D2
L23	TRUE	SPKRAMP_L_P_OUT	53B2 54D2
L24	TRUE	SPKRAMP_R_N_OUT	53C3 54C2
L25	TRUE	SPKRAMP_R_P_OUT	53C3 54C2
L26	TRUE	SPKRAMP_SUB_N_OUT	53B2 54C2
L27	TRUE	SPKRAMP_SUB_P_OUT	53C2 54C2

THERMAL FUNC_TEST

L28	TRUE	MCPTHMSNS_D2_P	45B5 77D3
L29	TRUE	MCPTHMSNS_D2_N	45B5 77D3

LVDS FUNC_TEST

F23C	TRUE	PP3V3_LCDVDD_SW_F	7C3 66C2
F23E	TRUE	PP3V3_S0_LCD_F	66C3
F23H	TRUE	PPVOUT_S0_LCDBKLT	7C3 66B2 69B3 69C1
L48	TRUE	LVDS_IG_DDC_CLK	18B3 66C5
L49	TRUE	LVDS_IG_DDC_DATA	18A3 66C5
L50	TRUE	LVDS_IG_A_DATA_N<0>	18B3 66C2 73B3
L51	TRUE	LVDS_IG_A_DATA_P<0>	18B3 66C2 73B3
L52	TRUE	LVDS_IG_A_DATA_N<1>	18B3 66C2 73B3
L53	TRUE	LVDS_IG_A_DATA_P<1>	18B3 66C2 73B3
L54	TRUE	LVDS_IG_A_DATA_N<2>	18B3 66C2 73B3
L55	TRUE	LVDS_IG_A_DATA_P<2>	18B3 66C2 73B3
L56	TRUE	LVDS_IG_A_CLK_F_N	66C2 73B3
L57	TRUE	LVDS_IG_A_CLK_F_P	66C2 73B3
L58	TRUE	LED_RETURN_1	66B3 69C1
L59	TRUE	LED_RETURN_2	66B3 69C1
L60	TRUE	LED_RETURN_3	66B3 69B1
L61	TRUE	LED_RETURN_4	66B3 69B1
L62	TRUE	LED_RETURN_5	66B3 69B1
L63	TRUE	LED_RETURN_6	66B3 69B1

(NEED TO ADD 5 GND TP)

SATA ODD CONN

F26A	TRUE	PP5V_SW_ODD	(NEED 4 TP) 7C3 36D3
F26B	TRUE	SMC_ODD_DETECT	36B7 39B8
F26D	TRUE	SATA_ODD_D2R_C_P	36B5 73A3
F26F	TRUE	SATA_ODD_D2R_C_N	36B5 73A3
F26H	TRUE	SATA_ODD_R2D_P	36C5 73A3
F26G	TRUE	SATA_ODD_R2D_N	7C5 36C5 73A3

(NEED TO ADD 4 GND TP)

DC POWER CONN

L81A	TRUE	PP18V5_DCIN_FUSE	(NEED 3 TP) 56D6
L80A	TRUE	ADAPTER_SENSE	56D7

(NEED TO ADD 4 GND TP)

BATT POWER CONN

L80C	TRUE	PPVBAT_G3H_CONN_F	(NEED 3 TP) 56A8
L80C	TRUE	GND_BATT_CONN	(NEED 3 TP) 56A8
L42C	TRUE	SMBUS_SMC_BSA_SCL	7A7 42C5 76D3
L42J	TRUE	SMBUS_SMC_BSA_SCL	7A7 7B7 42C5 76D3
L42D	TRUE	SMC_BS_ALRT_L	39C5 40B2 56A8

BATT SIGNAL CONN

L52C	TRUE	PP3V42_G3H	(NEED 3 TP) 7B5 7C3 8D1
L52D	TRUE	SMBUS_SMC_BSA_SCL	7A7 7B7 42C5 76D3
L52J	TRUE	SMBUS_SMC_BSA_SCL	7A7 7B7 42C5 76D3
L52G	TRUE	SMC_BIL_BUTTON_DB_L	56A5

(NEED TO ADD 3 GND TP)

FRONT FLEX CONN

L31C	TRUE	PP3V42_G3H_LIDSWITCH_R	38B6
L31J	TRUE	PP5V_S3_IR_R	38B6
L30C	TRUE	IR_RX_OUT	38B4 38C4
L30G	TRUE	SMC_LID_R	38B6
L30J	TRUE	SYS_LED_ANODE_R	38B6

(NEED TO ADD 2 GND TP)

RIGHT CLUTCH CONN

F30A	TRUE	PP5V_S3_BTCAMERA_F	31C7
F30C	TRUE	PCIE_MINI_D2R_P	17B6 31C7 73D3
F30E	TRUE	PCIE_MINI_D2R_N	17B6 31C7 73D3
F30G	TRUE	PCIE_MINI_R2D_P	31C7 73D3
F30J	TRUE	PCIE_MINI_R2D_N	31C7 73D3
F25C	TRUE	PCIE_CLK100M_MINI_CONN_P	31C7 73D3
F25E	TRUE	PCIE_CLK100M_MINI_CONN_N	31C7 73D3
F25G	TRUE	USB_CAMERA_CONN_P	31B7 74C3
F25J	TRUE	USB_CAMERA_CONN_N	31B7 74C3
F27A	TRUE	PP5V_WLAN	7C3 31C5
F27B	TRUE	PCIE_WAKE_L	17B6 23C5 31C7
F25C	TRUE	SMBUS_SMC_A_S3_SCL	7B5 42D2 76D3
F25E	TRUE	SMBUS_SMC_A_S3_SDA	7B5 42D2 76D3
F25A	TRUE	CONN_USB2_BT_P	31B7 74C3
F25G	TRUE	CONN_USB2_BT_N	31B7 74B3
F27J	TRUE	MINI_CLKREQ_O_L	31C7
F28B	TRUE	MINI_RESET_CONN_L	31A7

(NEED TO ADD 3 GND TP)

SATA HDD CONN

L81C	TRUE	PP5V_S0_HDD_FLT	(NEED 4 TP) 7C3 36B7
L81A	TRUE	SATA_HDD_R2D_P	36A7 73A3
L81E	TRUE	SATA_HDD_R2D_N	36A7 73A3
L81G	TRUE	SATA_HDD_D2R_C_P	36A7 73A3
L81J	TRUE	SATA_HDD_D2R_C_N	36A7 73A3
L81K	TRUE	SATA_ODD_R2D_N	7B7 36C5 73A3

(NEED TO ADD 4 GND TP)

IPD_FLEX_CONN

L37C	TRUE	PP3V3_S3_LDO	7C3 48B4 48C3
L37E	TRUE	PP18V5_S3	7C3 48C1 48D3
L37G	TRUE	TPAD_GND_F	48B4 48C3 48C4 48C7
L37J	TRUE	Z2_CS_L	47C8 48C3
L37D	TRUE	Z2_DEBUG3	47C8 48C3
L37A	TRUE	Z2_MOSI	47C8 48C3
L46C	TRUE	Z2_MISO	47C8 48C3
L46G	TRUE	Z2_SCLK	47C8 48C3
L46A	TRUE	Z2_BOOST_EN	48C3 48C5
L46E	TRUE	Z2_HOST_INTN	47D8 48C3
L46J	TRUE	Z2_BOOT_CFG1	47C8 48C3
L46D	TRUE	Z2_CLKIN	47C6 48C3
L36G	TRUE	Z2_KEY_ACT_L	47C8 48C1
L36A	TRUE	Z2_RESET	47C8 48C1
L36C	TRUE	PSOC_MISO	47C8 48C1
L36E	TRUE	PSOC_MOSI	47C8 48C1
L36J	TRUE	PSOC_SCLK	47C8 48C1
L35C	TRUE	SMBUS_SMC_A_S3_SDA	7D5 42D2 76D3
L35E	TRUE	SMBUS_SMC_A_S3_SCL	7D5 42D2 76D3
L35G	TRUE	PSOC_F_CS_L	47C8 48C1
L37J	TRUE	PICKB_L	47D8 48C1

KEYBOARD CONN

F35A	TRUE	PP3V3_S3	7D3 8D3
F35C	TRUE	PP3V42_G3H	7A7 7C3 8D1
L34A	TRUE	WS_KBD1	47C6 47D2
L34C	TRUE	WS_KBD2	47C6 47D2
L34E	TRUE	WS_KBD3	47C6 47D2
L34G	TRUE	WS_KBD4	47C6 47D2
L34J	TRUE	WS_KBD5	47C6 47D2
L33A	TRUE	WS_KBD6	47C6 47D2
L33C	TRUE	WS_KBD7	47C6 47D2
L33E	TRUE	WS_KBD8	47C6 47D2
L33G	TRUE	WS_KBD9	47C6 47D2
L33J	TRUE	WS_KBD10	47C6 47D2
L32A	TRUE	WS_KBD11	47C6 47D2
L32C	TRUE	WS_KBD12	47C6 47D2
L32E	TRUE	WS_KBD13	47C6 47D2
L32G	TRUE	WS_KBD14	47C6 47D2
L32J	TRUE	WS_KBD15_CAP	47C2 47C6
L44A	TRUE	WS_KBD16_NUM	47C2
L44C	TRUE	WS_KBD17	47C2
L44E	TRUE	WS_KBD18	47C2 47D6
L44G	TRUE	WS_KBD19	47C2 47D7
L44J	TRUE	WS_KBD20	47C2 47D7
L43A	TRUE	WS_KBD21	47C2 47D7
L43C	TRUE	WS_KBD22	47C2 47D7
L43E	TRUE	WS_KBD23	47C2 47D7
L43G	TRUE	WS_KBD_ONOFF_L	47C2
L43J	TRUE	WS_LEFT_SHIFT_KBD	47B3 47B5 47C2
L42A	TRUE	WS_LEFT_OPTION_KBD	47B3 47B5 47C2
L42C	TRUE	WS_CONTROL_KBD	47B3 47B5 47C2

(NEED TO ADD 1 GND TP)

KBD BACKLIGHT CONN

L35A	TRUE	KBDLED_ANODE	48A4

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

F23J	TRUE	PPVCORE_S0_CPU	8D7
F24A	TRUE	PPCPUVTT_S0	8D7
F23A	TRUE	PPVCORE_S0_MCP	8C7
F23C	TRUE	PP0V75_S0	8C7
L60A	TRUE	PP1V05_S0	8C7
F24J	TRUE	PP1V5_S0	8B7
F24C	TRUE	PP1V8_S0	8B7
L67A	TRUE	PP5VRT_S0	7D7 8D5
F23E	TRUE	PP3V3_S0	8C5
F24E	TRUE	PP1V5_S3	8D3
F24G	TRUE	PP3V3_S3	7B5 8D3
F27C	TRUE	PP5VLT_S3	8C3
F27G	TRUE	PP1V1R1V05_S5	8B3
L67C	TRUE	PP3V3_S5	8B3
F27J	TRUE	PP3V42_G3H	7A7 7B5 8D1
F27A	TRUE	PPBUS_G3H	8C1
F27E	TRUE	PP3V3_ENET_PHY	8B1
F27C	TRUE	PP1V2R1V05_ENET	8B1
F27J	TRUE	PP3V3_G3_RTC	21C8 22A5 26D4
L83A	TRUE	PP5V_WLAN	7D5 31C5
L83C	TRUE	PP5V_SW_ODD	7B7 36D3
L83E	TRUE	PP5V_S0_HDD_FLT	7C5 36B7
L83G	TRUE	PP3V3_S5_AVREF_SMC	39D4 40C6
L83J	TRUE	PP18V5_S3	7C5 48C1 48D3
L84A	TRUE	PP3V3_S3_LDO	7C5 48B4 48C3
L84C	TRUE	PP3V3_LCDVDD_SW_F	7C7 66C2
L84E	TRUE	PPVOUT_S0_LCDBKLT	7C7 66B2 69B3 69C1
L84G	TRUE	BKL_VREF_4V9	69B6 69B8 69C4 69C8
L84J	TRUE	PP4V6_AUDIO_ANALOG	51A3 51D3 52D6
L85A	TRUE	SMC_PM_G2_EN	39D5 64D8
L85C	TRUE	PM_SLP_S4_L	21C3 39C5 48A2 64C8
L85E	TRUE	PM_SLP_S3_L	21C3 34B7 39C5 41A5 64D5 68D8

(NEED TO ADD 4 GND TP)

FUNC TEST

SYNC_MASTER=M97_MLB

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II NOT TO REPRODUCE OR COPY IT

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 7 OF 109	

"S0,S0M" RAILS

60D1 =PPVCORE_S0_CPU_REG (CPU VCORE PWR)
- PPVCORE_S0_CPU — 7D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=1.25V
  MAKE_BASE=TRUE
  - =PPVCORE_S0_CPU — 11B5 11D6 12D6
  - =PPVCORE_S0_CPU_VSENSE — 43D8

65A6 62C7 =PPCPUVTT_S0_REG
- PPCPUVTT_S0 — 7D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_S0_CPU — 6D8 10D5 11C6 12B6 13D6
  - =PP1V05_S0_MCP_FSB — 9C2 14A2 14B7 22D3 24C8
  - =PP1V05_S0_SMC_LS — 48D3

61C1 =PPMCPCORE_S0_REG
44D8 =PPVCORE_S0_MCP_REG_R (MCP VCORE REG. OUTPUT)
- PPVCORE_S0_MCP_R — 7D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PPVCORE_S0_MCP_VSENSE — 43D8

44D7 24D8 61B1 =PPVCORE_S0_MCP (MCP VCORE AFTER SENSE RES)
- PPVCORE_S0_MCP — 7D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE

59C8 =PP0V75_S0_REG
- PP0V75_S0 — 7D3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=0.75V
  MAKE_BASE=TRUE
  - =PPVTT_S0_VTTCLAMP — 65B3
  - =PP0V75_S0_MEM_VTT_A — 28A4
  - =PP0V75_S0_MEM_VTT_B — 29A4

65A5 =PP1V05_S0_FET
- PP1V05_S0 — 7D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V05_S0_MCP_PEX_DVDD — 8A8 24D8
  - =PP1V05_S0_MCP_AVDD_UF — 24D4
  - =PP1V05_S0_MCP_PLL_UF — 24C4
  - =PP1V05_S0_MCP_SATA_DVDD — 8A8 24D6
  - =PP1V05_S0_MCP_HDMI_VDD — 18A6 25D7
  - =PP1V05_S0_VMON — 64A8

65D1 =PP1V5_S0_FET
44C8 =PP1V5_S0_FET_R (DDR PWR REG. OUTPUT)
- PP1V5_S0_R — 7D3
  MIN_LINE_WIDTH=0.5 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V5_S0_CPU — 11B6 12B6
  - =PP1V5_S0_VMON — 64A8
  - =PP1V5_FC_CON — 32C3

44C7 =PP1V5_S0 (DDR PWR AFTER SENSE RES.)
- PP1V5_S0 — 7D3
  MIN_LINE_WIDTH=0.5 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V8R1V5_S0_MCP_MEM — 16C3 16C7 24C8
  - =PP1V5_S0_MEM_MCP — 29B3

63C2 =PP1V8_S0_REG
- PP1V8_S0 — 7D3
  MIN_LINE_WIDTH=0.5 MM
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.8V
  MAKE_BASE=TRUE
  - =PP3V3R1V8_S0_MCP_IFP_VDD — 18B6 25D7

58B8 =PP5VRT_S0_REG
- PP5VRT_S0 — 7D3 7D7
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=5V
  MAKE_BASE=TRUE
  - =PP5V_S0_HDD — 36B5
  - =PP5V_S0_LPCPLUS — 41D5
  - =PP5V_S0_FAN_RT — 46C5
  - =PP5V_S0_CPU_IMVP — 60D8
  - =PP5V_S0_ODD — 36D5
  - =PP5V_S0_KBDLED — 48A5
  - =PP5V_S0_DP_AUX_MUX — 67B6
  - =PP5V_S0_CPUVTTS0 — 62C8

65C6 =PP3V3_S0_FET
- PP3V3_S0 — 7D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S0_XDP — 6D8 13D6
  - =PP3V3_S0_MCP — 21C2 22B3 24B8
  - =PP3V3_S0_MCP_DAC_UF — 25D4
  - =PP3V3_S0_MCP_VPLL_UF — 25C7
  - =PP3V3_S0_ODD — 36C7 36D5
  - =PP3V3_S0_LPCPLUS — 41C3
  - =PP3V3_S0_SMBUS_SMC_0_S0 — 42D5
  - =PP3V3_S0_SMBUS_SMC_B_S0 — 42C3
  - =PP3V3_S0_SMBUS_MCP_0 — 42D8
  - =PP3V3_S0_FAN_RT — 46C5
  - =PP3V3_S0_AUDIO — 51A7 51D8 52D6 54D8 55B5
  - =PP3V3_S0_IMVP — 60D8
  - =PP3V3_S0_LCD — 66C5
  - =PP3V3_S0_MCP_GPIO — 18C1 19D1 21A4
  - =PP3V3_S0_HDCPROM — 25B8
  - =PP3V3_S0_MCP_PLL_UF — 24B6
  - =PP3V3R1V5_S0_MCP_HDA — 21D3 21D8 24A8
  - =PP3V3_S0_SMC — 40A1 40D2
  - =PP3V3_S0_MCPTHMSNS — 45C6
  - =PP3V3_S0_CPUTHMSNS — 45D6
  - =PP5VR3V3_S0_MCPCOREISNS — 44D7
  - =PP3V3_S0_DPCONN — 68B8 68C8
  - =PPSPD_S0_MEM_A — 28A8
  - =PPSPD_S0_MEM_B — 29A8
  - =PP3V3_S0_PWRCTL — 64A5
  - =PP3V3_S0_VMON — 64B8
  - =PP3V3_S0_MCPDDRISNS — 44C7
  - =PP3V3_S0_CPUVTTISNS — 44C7
  - =PPVIN_S0_P1V8S0 — 63C5
  - =PP3V3_FC_CON — 32C3
  - =PP3V3_S0_TPAD — 48A6
  - =PP3V3_S0_SMBUS_MCP_1 — 42C8

PEX & SATA AVDD/DVDD aliases

24D1 PP1V05_S0_MCP_PEX_AVDD (MAKE_BASE=TRUE)
206 mA (A01)

24D8 8C7 =PP1V05_S0_MCP_PEX_DVDD
206 mA (A01)

24D2 PP1V05_S0_MCP_SATA_AVDD (MAKE_BASE=TRUE)
127 mA (A01)

24D6 8B7 =PP1V05_S0_MCP_SATA_DVDD
127 mA (A01)

- =PP1V05_S0_MCP_PEX_AVDD0 — 17B3
- =PP1V05_S0_MCP_PEX_AVDD1 — 17A3
  206 mA (A01)
- =PP1V05_S0_MCP_PEX_DVDD0 — 17B6
- =PP1V05_S0_MCP_PEX_DVDD1 — 17A6
  57 mA (A01)
- =PP1V05_S0_MCP_SATA_AVDD0 — 20B6
- =PP1V05_S0_MCP_SATA_AVDD1 — 20B6
  127 mA (A01)
- =PP1V05_S0_MCP_SATA_DVDD0 — 20B6
- =PP1V05_S0_MCP_SATA_DVDD1 — 20B6
  43 mA (A01)

"S3" RAILS

59C1 =PP1V5_S3_REG
- PP1V5_S3 — 7D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=1.5V
  MAKE_BASE=TRUE
  - =PP1V5_S3_P1V5S0FET — 65D3
  - =PP1V5_S3_MEM_A — 28D7
  - =PP1V5_S3_MEM_B — 29D7
  - =PP1V5_S3_MEMRESET — 30C6

65D6 =PP3V3_S3_FET
- PP3V3_S3 — 7B5 7D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S3_SMBUS_SMC_A_S3 — 42D3
  - =PP3V3_S3_PDCISENS — 59B3
  - =PP3V3_S3_SMBUS_SMC_MGMT — 42B5
  - =PP3V3_S3_VREFMRGN — 27D8
  - =PP3V3_S3_WLAN — 31A6
  - =PP3V3_S3_MCP_GPIO — 21A3
  - =PP3V3_S3_TPAD — 47A6 47B5 47C5 47D2
  - =PP3V3_S3_SMS — 49B7 49D5

61C8 =PP5VLT_S3_REG
- PP5VLT_S3 — 7D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=5V
  MAKE_BASE=TRUE
  - =PP5V_S3_EXTUSB — 37C7
  - =PP5V_S3_IR — 38B4 38D7
  - =PP5V_S3_BTCAMERA — 31C3
  - =PP5V_S3_VTTCLAMP — 65A3
  - =PP5V_S3_MCPDDRFET — 65D4
  - =PP5V_S3_SYSLED — 40B8
  - =PP5V_S3_TPAD — 48C8
  - =PP5V_S3_WLAN — 31C1
  - =PP5V_S3_1V5S30V75S0 — 59C5
  - =PP5V_S3_AUDIO — 51A7 55D4
  - =PP5V_S3_AUDIO_AMP — 53B8 53C8 53D8
  - =PP5V_S3_P1V05S0FET — 65B8

59D7 27D3 =PPVTT_S3_DDR_BUF
- PPVTT_S3_DDR_BUF
  MIN_LINE_WIDTH=0.3 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=0.75V
  MAKE_BASE=TRUE

"S5" RAILS

63B4 =PP1V05_S5_REG
- PP1V1R1V05_S5 — 7D3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_S5_MCP_VDD_AUXC — 22A3 24D8
  - =PP1V05_ENET_P1V05ENETFET — 34C4
  - =PP1V05_S5_P1V05S0FET — 65B6

58B1 =PP3V3_S5_REG
- PP3V3_S5 — 7D3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.2 mm
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_S5_MCP_GPIO — 18C7 20C1
  - =PP3V3_S5_ROM — 41B5 41C7 50C6
  - =PP3V3_S5_LCD — 66C8
  - =PP3V3_S5_MCP — 22B3 24B8
  - =PP3V3_S5_MCPPWRGD — 26B8
  - =PP3V3_S5_SMBUS_MCP_1 — 42C7
  - =PP3V3_S5_MCP_A01 — 23C4 41B4
  - =PP3V3_S5_PWRCTL — 64B3 64D4
  - =PP3V3_S5_P1V05ENETFET — 34C5
  - =PP3V3_S5_P3V3S3FET — 65D8
  - =PP3V3_S5_P3V3S0FET — 65C8
  - =PP3V3_S5_P1V05S5 — 63B7
  - =PP3V3_S5_P1V05FET — 65A8
  - =PP3V3_S5_MEMRESET — 30C6
  - =PP3V3_S5_P3V3ENETFET — 34D5
  - =PP3V3_S5_DP_PORT_PWR — 68D8

"G3H" RAILS

56B4 =PP3V42_G3H_REG
- PP3V42_G3H — 7A7 7B5 7C3
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=3.42V
  MAKE_BASE=TRUE
  - =PPVIN_S5_SMCVREF — 40C8
  - =PP3V42_G3H_SMBUS_SMC_BSA — 42C5
  - =PP3V42_G3H_PWRCTL — 64B3 64D3 64D8
  - =PP3V42_G3H_CHGR — 57A8 57C6 57D5
  - =PP3V42_G3H_SMCUSBMUX — 37B8
  - =PP3V42_G3H_LIDSWITCH — 38B4
  - =PP3V42_G3H_TPAD — 47B5 47C2 47C3 47C5
  - =PP3V42_G3H_BATT — 56A3 56B3
  - =PP3V3_S5_SMC — 39D4 40C1 40C7 40D8 49D7
  - =PP3V3_S5_LPCPLUS — 41C3 41C7 41D5
  - =PP3V42_G3H_RTC_D — 26D8
  - =PP3V42_G3H_BMON_ISNS — 44B8

56D1 56C8 =PP18V5_DCIN_CONN
- PP18V5_G3H
  MIN_LINE_WIDTH=0.6 MM
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=18.5V
  MAKE_BASE=TRUE
  - =PP18V5_G3H_CHGR — 57D8

57C1 =PPBUS_G3H
- PPBUS_G3H — 7C3
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=12.6V
  MAKE_BASE=TRUE
  - =PPBUS_S0_LCDBKLT — 70D8
  - =PPVIN_S0_MCPCORES0 — 61C3
  - =PPVIN_S0_MCPREG_VIN — 61C6
  - =PPVIN_S5_1V5S30V75S0 — 59C2
  - =PPVIN_S5_3V3S5 — 58C3
  - =PPVIN_S0_5VRTS0 — 58C6
  - =PPVIN_S3_5VLTS3 — 61D8
  - =PPBUS_G3HRS5 — 43B8
  - =PPCPUVCORE_VTT_ISNS_R — 44B8 (BEFORE HIGH SIDE SENSING RES.)

44B7 =PPCPUVCORE_VTT_ISNS (AFTER HIGH SIDE CPU VCORE & CPU VTT SENSING RES.)
- PPBUS_G3H_CPU_ISNS
  MIN_LINE_WIDTH=0.6 mm
  MIN_NECK_WIDTH=0.3 MM
  VOLTAGE=12.6V
  MAKE_BASE=TRUE
  - =PPVIN_S0_CPUVTTS0 — 62C6
  - =PPVIN_S5_CPU_IMVP — 60C2 60D4 60D8

"ENET" RAILS

34D2 =PP3V3_ENET_FET
- PP3V3_ENET_PHY — 7C3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=3.3V
  MAKE_BASE=TRUE
  - =PP3V3_ENET_MCP_RMGT — 18D3 18D7 24A5 24B6
  - =PP3V3_ENET_PHY — 33D7

34B2 =PP1V05_ENET_FET
- PP1V2R1V05_ENET — 7C3
  MIN_LINE_WIDTH=0.4 MM
  MIN_NECK_WIDTH=0.2 MM
  VOLTAGE=1.05V
  MAKE_BASE=TRUE
  - =PP1V05_ENET_MCP_PLL_MAC — 24A8
  - =PP1V05_ENET_MCP_RMGT — 18D3 24D6
  - =PP1V05_ENET_PHY — 33D2

Power Aliases

SYNC_MASTER=BEN

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 8 OF 109	

HEATSINK STANDOFFS

Z0902 STDOFF-4.50D.98H-1.1-3.48-TH — LEFT OF CPU

Z0901 STDOFF-4.50D.98H-1.1-3.48-TH — ABOVE CPU

Z0903 STDOFF-4.50D.98H-1.1-3.48-TH — BELOW MCP

Z0904 STDOFF-4.50D.98H-1.1-3.48-TH — BELOW CPU

FAN STANDOFF

Z0905 STDOFF-4.50D.98H-1.1-3.48-TH

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

AUDIO CHASSIS GND

GND_CHASSIS_AUDIO MAKE_BASE=TRUE — OMIT Z0906 TH SL-3.10X2.70

54C8 54A8 =GND_CHASSIS_AUDIO_JACK
55A4 54A3 =GND_CHASSIS_AUDIO_MIC

MLB MOUNTING SCREW HOLES

OMIT Z0908 3R2P5 — OMIT Z0909 3R2P5 — OMIT Z0910 3R2P5

OMIT Z0911 3R2P5 — OMIT Z0912 3R2P5 — OMIT Z0913 3R2P5

VENICE BOARD STANDOFFS

VENICE Z0914 STDOFF-4.0OD3.0H-TH — VENICE Z0915 STDOFF-4.0OD3.0H-TH — VENICE Z0916 STDOFF-4.0OD3.0H-TH

EMI IO POGO PINS

ZS0900 1.4DIA-SHORT-EMI-MLB-M97-M98 SM

ZS0901 1.4DIA-SHORT-EMI-MLB-M97-M98 SM

ZS0902 1.4DIA-SHORT-EMI-MLB-M97-M98 SM

ZS0903 1.4DIA-SHORT-EMI-MLB-M97-M98 SM

EMI POGO PINS

ZS0904 2.0DIA-TALL-EMI-MLB-M97-M98 SM

ZS0905 2.0DIA-TALL-EMI-MLB-M97-M98 SM

ZS0906 2.0DIA-TALL-EMI-MLB-M97-M98 SM

ZS0907 2.0DIA-TALL-EMI-MLB-M97-M98 SM

PCI-E ALIASES

UNUSED GPU LANES

17D6 17C6 =PEG_D2R_N<15:0> — NC_PEG_D2R_N<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
17D6 17C6 =PEG_D2R_P<15:0> — NC_PEG_D2R_P<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
17D3 17C3 =PEG_R2D_C_N<15:0> — NC_PEG_R2D_C_N<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
17D3 17C3 =PEG_R2D_C_P<15:0> — NC_PEG_R2D_C_P<15:0> NO_TEST=TRUE MAKE_BASE=TRUE
17C6 PEG_PRSNT_L — TP_PEG_PRSNT_L MAKE_BASE=TRUE
17C3 PEG_CLK100M_P — TP_PEG_CLK100M_P MAKE_BASE=TRUE
17C3 PEG_CLK100M_N — TP_PEG_CLK100M_N MAKE_BASE=TRUE

UNUSED FW LANE

17B6 PCIE_FW_D2R_P — TP_PCIE_FW_D2R_P MAKE_BASE=TRUE
17B6 PCIE_FW_D2R_N — TP_PCIE_FW_D2R_N MAKE_BASE=TRUE
17B3 PCIE_FW_R2D_C_P — TP_PCIE_FW_R2D_C_P MAKE_BASE=TRUE
17B3 PCIE_FW_R2D_C_N — TP_PCIE_FW_R2D_C_N MAKE_BASE=TRUE
17C6 PCIE_FW_PRSNT_L — TP_PCIE_FW_PRSNT_L MAKE_BASE=TRUE
17C6 FW_CLKREQ_L — TP_FW_CLKREQ_L MAKE_BASE=TRUE
17C3 PCIE_CLK100M_FW_P — TP_PCIE_CLK100M_FW_P MAKE_BASE=TRUE
17C3 PCIE_CLK100M_FW_N — TP_PCIE_CLK100M_FW_N MAKE_BASE=TRUE

UNUSED EXPRESS CARD LANE

17B6 PCIE_EXCARD_D2R_P — TP_PCIE_EXCARD_D2R_P MAKE_BASE=TRUE
17B6 PCIE_EXCARD_D2R_N — TP_PCIE_EXCARD_D2R_N MAKE_BASE=TRUE
17B3 PCIE_EXCARD_R2D_C_P — TP_PCIE_EXCARD_R2D_C_P MAKE_BASE=TRUE
17B3 PCIE_EXCARD_R2D_C_N — TP_PCIE_EXCARD_R2D_C_N MAKE_BASE=TRUE
17C6 PCIE_EXCARD_PRSNT_L — TP_PCIE_EXCARD_PRSNT_L MAKE_BASE=TRUE
17C6 EXCARD_CLKREQ_L — TP_EXCARD_CLKREQ_L MAKE_BASE=TRUE
17C3 PCIE_CLK100M_EXCARD_P — TP_PCIE_CLK100M_EXCARD_P MAKE_BASE=TRUE
17C3 PCIE_CLK100M_EXCARD_N — TP_PCIE_CLK100M_EXCARD_N MAKE_BASE=TRUE

AIRPORT CARD PRESENT SIGNAL (WRONG ALAIS, REMOVE AT NEXT BOARD SPIN)

31D7 17C6 PCIE_MINI_PRSNT_L — MAKE_BASE=TRUE

FOR VENICE CARD

17C6 TP_PE4_CLKREQ_L — FC_CLKREQ_L 32C5 MAKE_BASE=TRUE
17C6 TP_PE4_PRSNT_L — FC_PRSNT_L 32C3 MAKE_BASE=TRUE
17C3 TP_PCIE_CLK100M_PE4P — PCIE_CLK100M_FC_P 32C5 73D3 MAKE_BASE=TRUE
17C3 TP_PCIE_CLK100M_PE4N — PCIE_CLK100M_FC_N 32C5 73D3 MAKE_BASE=TRUE
17B6 TP_PCIE_PE4_D2RP — PCIE_FC_D2R_P 32C5 73D3 MAKE_BASE=TRUE
17B6 TP_PCIE_PE4_D2RN — PCIE_FC_D2R_N 32C5 73D3 MAKE_BASE=TRUE
17B3 TP_PCIE_PE4_R2D_CP — PCIE_FC_R2D_C_P 32C6 73D3 MAKE_BASE=TRUE
17B3 TP_PCIE_PE4_R2D_CN — PCIE_FC_R2D_C_N 32C6 73D3 MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

20C3 USB_EXTC_P — TP_USB_EXTC_P MAKE_BASE=TRUE
20C3 USB_EXTC_N — TP_USB_EXTC_N MAKE_BASE=TRUE
20D3 USB_EXTD_P — TP_USB_EXTD_P MAKE_BASE=TRUE
20D3 USB_EXTD_N — TP_USB_EXTD_N MAKE_BASE=TRUE
20C3 USB_EXCARD_P — TP_USB_EXCARD_P MAKE_BASE=TRUE
20C3 USB_EXCARD_N — TP_USB_EXCARD_N MAKE_BASE=TRUE
20D3 USB_MINI_P — TP_USB_MINI_P MAKE_BASE=TRUE
20D3 USB_MINI_N — TP_USB_MINI_N MAKE_BASE=TRUE

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

18C6 MCP_TV_DAC_RSET — NC_MCP_TV_DAC_RSET NO_TEST=TRUE MAKE_BASE=TRUE
18C6 MCP_TV_DAC_VREF — NC_MCP_TV_DAC_VREF NO_TEST=TRUE MAKE_BASE=TRUE
18C6 MCP_CLK27M_XTALIN — NC_MCP_CLK27M_XTALIN NO_TEST=TRUE MAKE_BASE=TRUE
18C6 MCP_CLK27M_XTALOUT — NC_MCP_CLK27M_XTALOUT NO_TEST=TRUE MAKE_BASE=TRUE
18C3 CRT_IG_R_C_PR — NC_CRT_IG_R_C_PR NO_TEST=TRUE MAKE_BASE=TRUE
18C3 CRT_IG_G_Y_Y — NC_CRT_IG_G_Y_Y NO_TEST=TRUE MAKE_BASE=TRUE
18C3 CRT_IG_B_COMP_PB — NC_CRT_IG_B_COMP_PB NO_TEST=TRUE MAKE_BASE=TRUE
18C3 CRT_IG_HSYNC — NC_CRT_IG_HSYNC NO_TEST=TRUE MAKE_BASE=TRUE
18C3 CRT_IG_VSYNC — NC_CRT_IG_VSYNC NO_TEST=TRUE MAKE_BASE=TRUE

LVDS ALIASES

UNUSED LVDS SIGNALS

18B3 LVDS_IG_A_DATA_P<3> — NC_LVDS_IG_A_DATA_P3 NO_TEST=TRUE MAKE_BASE=TRUE
18B3 LVDS_IG_A_DATA_N<3> — NC_LVDS_IG_A_DATA_N3 NO_TEST=TRUE MAKE_BASE=TRUE
18B3 LVDS_IG_B_CLK_P — NC_LVDS_IG_B_CLK_P NO_TEST=TRUE MAKE_BASE=TRUE
18B3 LVDS_IG_B_CLK_N — NC_LVDS_IG_B_CLK_N NO_TEST=TRUE MAKE_BASE=TRUE
18B3 LVDS_IG_B_DATA_P<3:0> — NC_LVDS_IG_B_DATA_P<3:0> NO_TEST=TRUE MAKE_BASE=TRUE
18B3 LVDS_IG_B_DATA_N<3:0> — NC_LVDS_IG_B_DATA_N<3:0> NO_TEST=TRUE MAKE_BASE=TRUE

MISC MCP79 ALIASES

14B6 CPU_PECI_MCP — TP_CPU_PECI_MCP MAKE_BASE=TRUE
19B7 FW_PME_L — TP_FW_PME_L MAKE_BASE=TRUE
17B6 GMUX_JTAG_TCK_L — TP_GMUX_JTAG_TCK_L MAKE_BASE=TRUE
17B6 GMUX_JTAG_TDO — TP_GMUX_JTAG_TDO MAKE_BASE=TRUE
19D4 GMUX_JTAG_TDI — TP_GMUX_JTAG_TDI MAKE_BASE=TRUE
19D4 GMUX_JTAG_TMS — TP_GMUX_JTAG_TMS MAKE_BASE=TRUE

LAN ALIASES

18D6 =MCP_MII_RXER — MCP_MII_PD MAKE_BASE=TRUE
18D6 =MCP_MII_COL
18D6 =MCP_MII_CRS

R0930 4.7K 5% 1/16W MF-LF 402

DP HOTPLUG PULL-DOWN

18B6 =DVI_HPD_GMUX_INT — HPLUG_DET2 MAKE_BASE=TRUE

R0940 20K 5% 1/16W MF-LF 402

SO-DIMM ALIASES

UNUSED ADDRESS PINS

28D5 MEM_A_A<15> — TP_MEM_A_A15 MAKE_BASE=TRUE
29D5 MEM_B_A<15> — TP_MEM_B_A15 MAKE_BASE=TRUE

ETHERNET ALIASES

34C5 =P3V3ENET_EN — PM_SLP_RMGT_L 21C3 MAKE_BASE=TRUE
34B5 =P1V05ENET_EN
33C2 =P3V3_ENET_PHY_VDDREG — TP_PP3V3_ENET_PHY_VDDREG
33C2 =RTL8211_REGOUT — NC_RTL8211_REGOUT MAKE_BASE=TRUE
33C6 =RTL8211_ENSWREG MAKE_BASE=TRUE

CPU FSB FREQUENCY STRAPS

71C3 10B4 IN CPU_BSEL<0:2> — =MCP_BSEL<0:2> OUT 14A7 MAKE_BASE=TRUE

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

24C8 22D3 14B7 14A2 8D7 =PP1V05_S0_MCP_FSB

MCP_A01&MCP_A01P&MCP_A01Q

R0950 220 5% 1/16W MF-LF 402 — NO STUFF R0970 200 5% 1/16W MF-LF 402 — NO STUFF R0990 150 5% 1/16W MF-LF 402

NO STUFF R0960 62 5% 1/16W MF-LF 402 — NO STUFF R0980 150 5% 1/16W MF-LF 402

71B3 60C7 14A3 10B2 OUT CPU_DPRSTP_L
71C3 14B6 10D6 OUT FSB_BREQ0_L
71C3 14A3 13C2 10D6 OUT FSB_CPURST_L
71C3 14A3 10C8 OUT CPU_INTR
71C3 14A3 10B8 OUT CPU_NMI

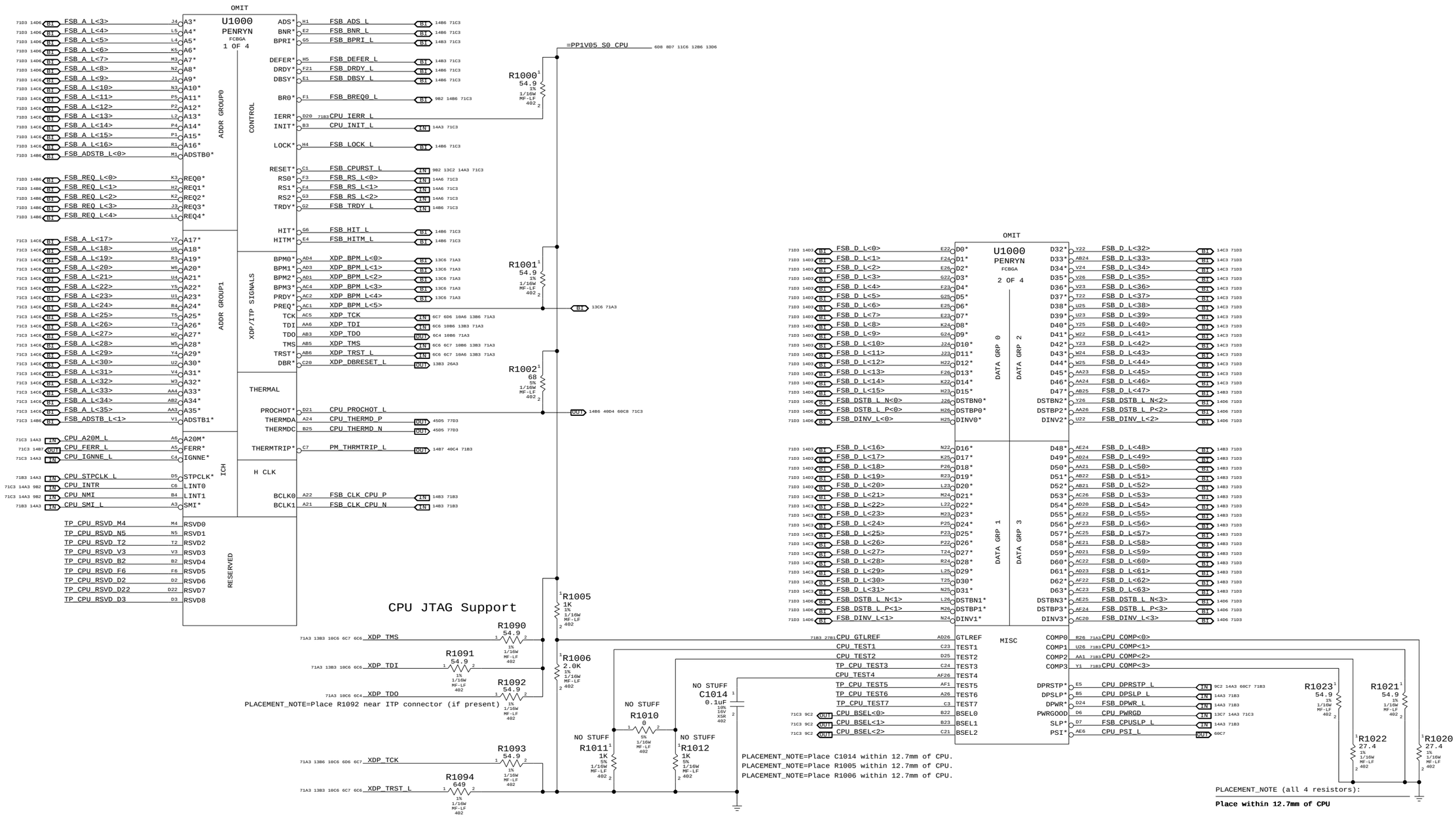
SIGNAL ALIAS

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE D | DRAWING NUMBER 051-7918 | REV. C

SCALE NONE | SHT 9 OF 109



SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

CPU FSB

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

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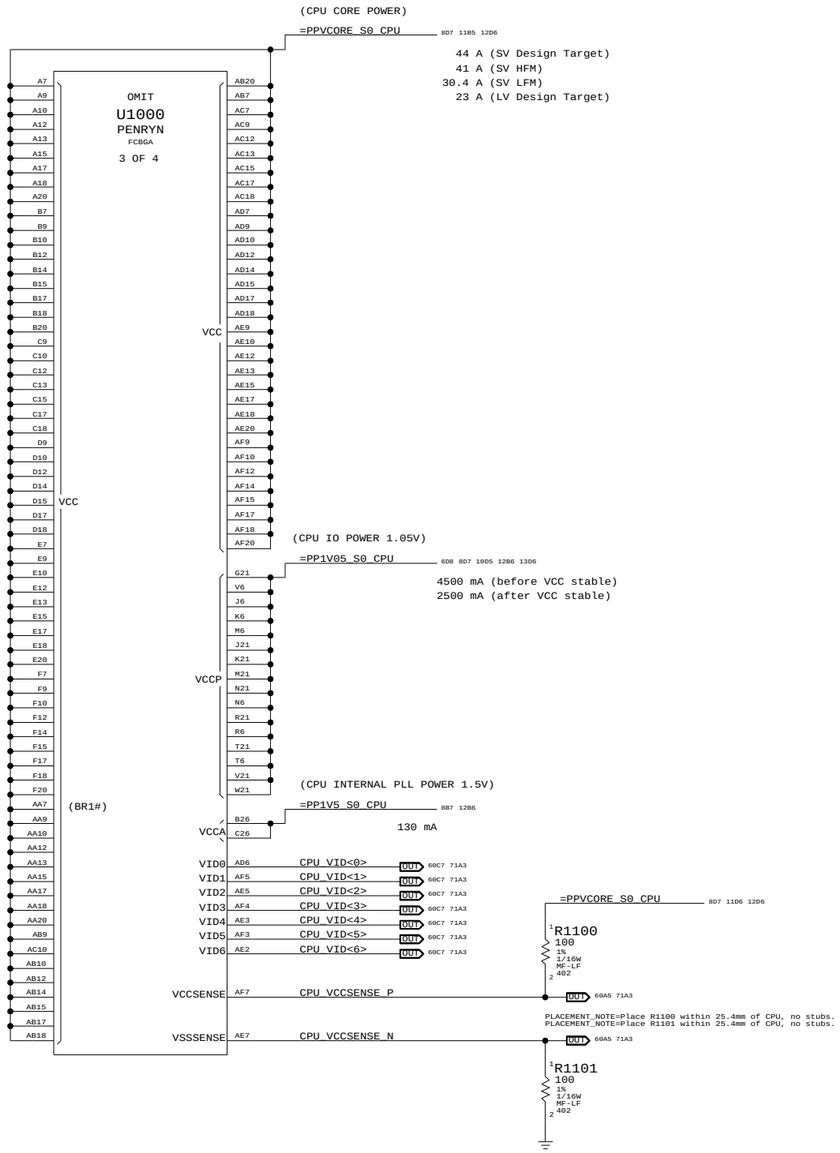
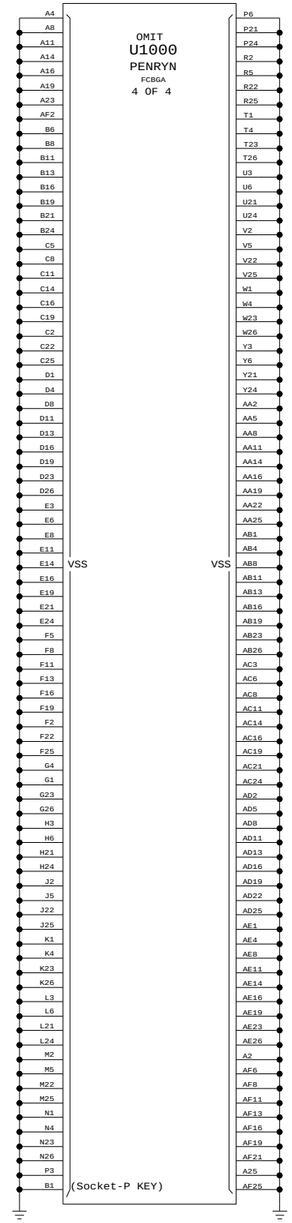
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 10 OF 109	





SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU Power & Ground

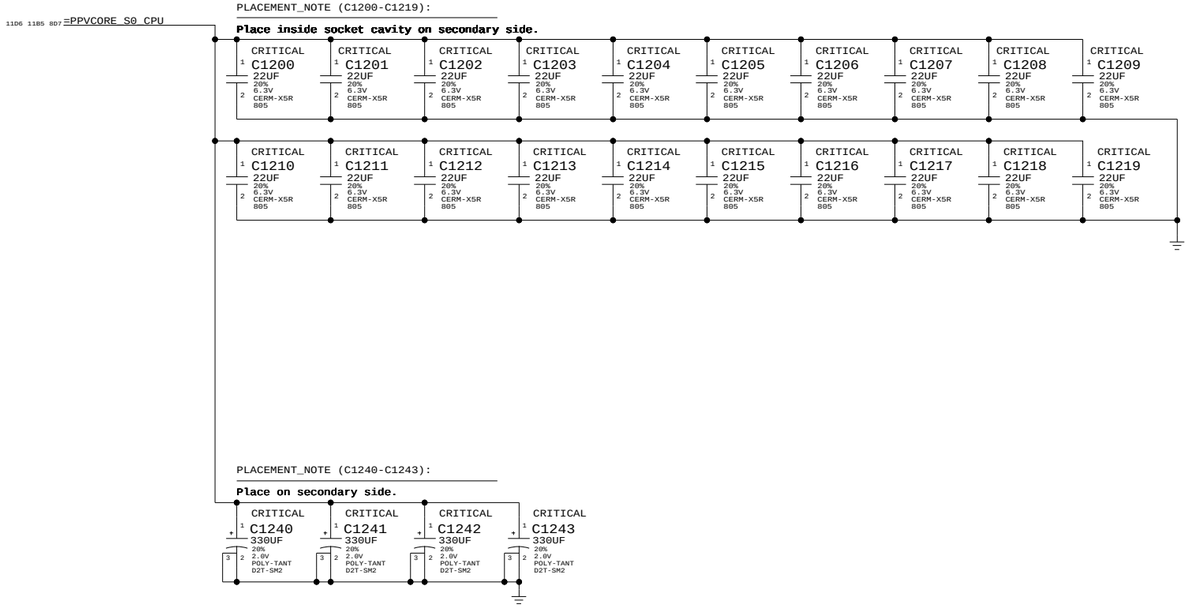
SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 11 OF 109	

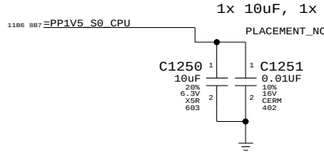
CPU VCore HF and Bulk Decoupling

4X 330UF. 20X 22UF 0805



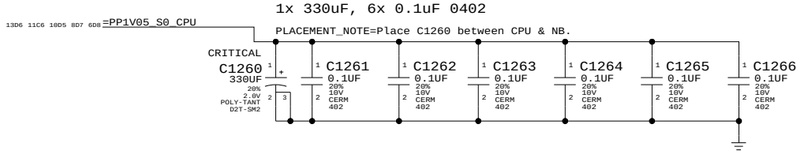
VCCA (CPU AVdd) DECOUPLING

1x 10uF, 1x 0.01uF



VCCP (CPU I/O) DECOUPLING

1x 330uF, 6x 0.1uF 0402



SYNC FROM T18
REMOVE NO STUFF CAPS C1220 TO C1231
REMOVE C1244 & C1245
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

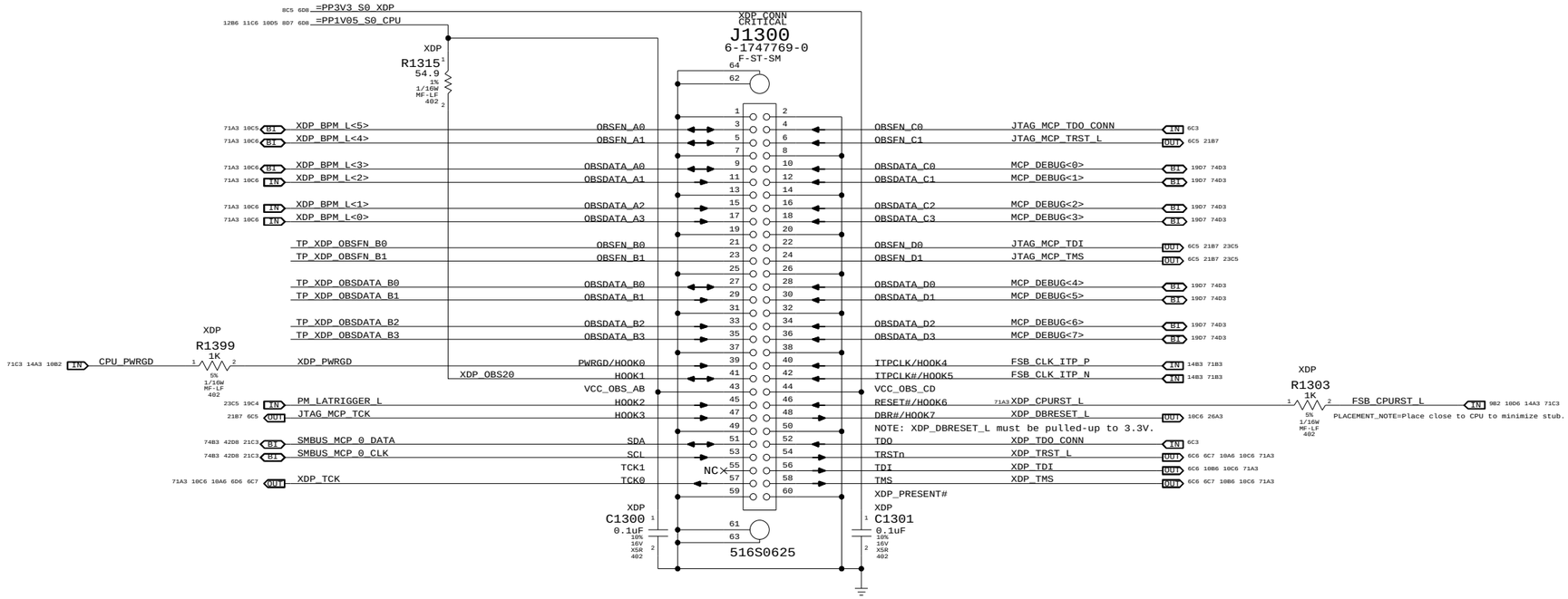
CPU Decoupling

SYNC_MASTER=RAYMOND SYNC_DATE=03/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 12 OF 109	

MCP79-specific pinout



SYNC FROM T18
CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625
RENAME JTAG_MCP_TDO TO JTAG_MCP_TDO_CONN
RENAME XDP_TDO TO XDP_TDO_CONN

eXtended Debug Port (XDP)

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 13 OF 109	

OMIT

U1400
MCP79-TOPO-B
BGA
(1 OF 11)

FSB

71D3 10C4	BI	FSB_DSTB_L_P<0>	T40	CPU_DSTBP0#			
71D3 10C4	BI	FSB_DSTB_L_N<0>	U40	CPU_DSTBN0#			
71D3 10C4	BI	FSB_DINV_L<0>	V41	CPU_DBI0#			
71D3 10B4	BI	FSB_DSTB_L_P<1>	W39	CPU_DSTBP1#			
71D3 10B4	BI	FSB_DSTB_L_N<1>	W37	CPU_DSTBN1#			
71D3 10B4	BI	FSB_DINV_L<1>	V35	CPU_DBI1#			
71D3 10C2	BI	FSB_DSTB_L_P<2>	N37	CPU_DSTBP2#			
71D3 10C2	BI	FSB_DSTB_L_N<2>	L36	CPU_DSTBN2#			
71D3 10C2	BI	FSB_DINV_L<2>	N35	CPU_DBI2#			
71D3 10B2	BI	FSB_DSTB_L_P<3>	M39	CPU_DSTBP3#			
71D3 10B2	BI	FSB_DSTB_L_N<3>	M41	CPU_DSTBN3#			
71D3 10B2	BI	FSB_DINV_L<3>	J41	CPU_DBI3#			
71D3 10D8	BI	FSB_A_L<3>	AC34	CPU_A3#			
71D3 10D8	BI	FSB_A_L<4>	AE38	CPU_A4#			
71D3 10D8	BI	FSB_A_L<5>	AE34	CPU_A5#			
71D3 10D8	BI	FSB_A_L<6>	AC37	CPU_A6#			
71D3 10D8	BI	FSB_A_L<7>	AE37	CPU_A7#			
71D3 10D8	BI	FSB_A_L<8>	AE35	CPU_A8#			
71D3 10D8	BI	FSB_A_L<9>	AB35	CPU_A9#			
71D3 10D8	BI	FSB_A_L<10>	AF35	CPU_A10#			
71D3 10D8	BI	FSB_A_L<11>	AG35	CPU_A11#			
71D3 10D8	BI	FSB_A_L<12>	AG39	CPU_A12#			
71D3 10D8	BI	FSB_A_L<13>	AE33	CPU_A13#			
71D3 10D8	BI	FSB_A_L<14>	AG37	CPU_A14#			
71D3 10D8	BI	FSB_A_L<15>	AG38	CPU_A15#			
71D3 10D8	BI	FSB_A_L<16>	AG34	CPU_A16#			
71C3 10D8	BI	FSB_A_L<17>	AN38	CPU_A17#			
71C3 10C8	BI	FSB_A_L<18>	AL39	CPU_A18#			
71C3 10C8	BI	FSB_A_L<19>	AG33	CPU_A19#			
71C3 10C8	BI	FSB_A_L<20>	AL33	CPU_A20#			
71C3 10C8	BI	FSB_A_L<21>	AJ33	CPU_A21#			
71C3 10C8	BI	FSB_A_L<22>	AN36	CPU_A22#			
71C3 10C8	BI	FSB_A_L<23>	AJ35	CPU_A23#			
71C3 10C8	BI	FSB_A_L<24>	AJ37	CPU_A24#			
71C3 10C8	BI	FSB_A_L<25>	AJ36	CPU_A25#			
71C3 10C8	BI	FSB_A_L<26>	AJ38	CPU_A26#			
71C3 10C8	BI	FSB_A_L<27>	AL37	CPU_A27#			
71C3 10C8	BI	FSB_A_L<28>	AL34	CPU_A28#			
71C3 10C8	BI	FSB_A_L<29>	AN37	CPU_A29#			
71C3 10C8	BI	FSB_A_L<30>	AJ34	CPU_A30#			
71C3 10C8	BI	FSB_A_L<31>	AL38	CPU_A31#			
71C3 10C8	BI	FSB_A_L<32>	AL35	CPU_A32#			
71C3 10C8	BI	FSB_A_L<33>	AN34	CPU_A33#			
71C3 10C8	BI	FSB_A_L<34>	AR39	CPU_A34#			
71C3 10C8	BI	FSB_A_L<35>	AN35	CPU_A35#			
71D3 10D8	BI	FSB_ADSTB_L<0>	AE36	CPU_ADSTB0#			
71C3 10C8	BI	FSB_ADSTB_L<1>	AK35	CPU_ADSTB1#			
71D3 10D8	BI	FSB_REQ_L<0>	AC38	CPU_REQ0#			
71D3 10D8	BI	FSB_REQ_L<1>	AA33	CPU_REQ1#			
71D3 10D8	BI	FSB_REQ_L<2>	AC39	CPU_REQ2#			
71D3 10D8	BI	FSB_REQ_L<3>	AC33	CPU_REQ3#			
71D3 10D8	BI	FSB_REQ_L<4>	AC35	CPU_REQ4#			
71C3 10D6	BI	FSB_ADS_L	AD42	CPU_ADS#			
71C3 10D6	BI	FSB_BNR_L	AD43	CPU_BNR#			
71C3 10D6 982	BI	FSB_BREQ0_L	AE40	CPU_BR0#			
71C3		FSB_BREQ1_L	AL32	CPU_BR1#			
71C3 10D6	BI	FSB_DBSY_L	AD39	CPU_DBSY#			
71C3 10D6	BI	FSB_DRDY_L	AD41	CPU_DRDY#			
71C3 10D6	BI	FSB_HIT_L	AB42	CPU_HIT#			
71C3 10D6	BI	FSB_HITM_L	AD40	CPU_HITM#			
71C3 10D6	IN	FSB_LOCK_L	AC43	CPU_LOCK#			
71C3 10D6	OUT	FSB_TRDY_L	AE41	CPU_TRDY#			
9C4	OUT	CPU_PECI_MCP	E41	CPU_PECI			
71C3 60C8 40D4 10C5	OUT	CPU_PROCHOT_L	AJ41	CPU_PROCHOT#			
			AG43	CPU_THERMTRIP#			
			AH40	CPU_FERR#			
9C1	IN	=MCP_BSEL<2>	(MCP_BSEL<2>)	F42	CPU_BSEL2		
9C1	IN	=MCP_BSEL<1>	(MCP_BSEL<1>)	D42	CPU_BSEL1		
9C1	IN	=MCP_BSEL<0>	(MCP_BSEL<0>)	F41	CPU_BSEL0		
71C3 10D6	OUT	FSB_RS_L<0>	AC41	CPU_RS0#			
71C3 10D6	OUT	FSB_RS_L<1>	AB41	CPU_RS1#			
71C3 10D6	OUT	FSB_RS_L<2>	AC42	CPU_RS2#			
24C2	PP1V05_S0_MCP_PLL_FSB	270 mA (A01)	206 mA	AG27	+V_DLL_DLCELL_AVDD		
			20 mA	AH27	+V_PLL_MCLK		
			29 mA	AG28	+V_PLL_FSB		
			15 mA	AH28	+V_PLL_CPU		
71B3	MCP_BCLK_VML_COMP_VDD		AM39	BCLK_VML_COMP_VDD			
71B3	MCP_BCLK_VML_COMP_GND		AM40	BCLK_VML_COMP_GND			
71B3	MCP_CPU_COMP_VCC		AM43	CPU_COMP_VCC			
71B3	MCP_CPU_COMP_GND		AM42	CPU_COMP_GND			

CPU_D0#	Y43	FSB_D_L<0>	BI	10C4 71D3
CPU_D1#	W42	FSB_D_L<1>	BI	10C4 71D3
CPU_D2#	Y40	FSB_D_L<2>	BI	10C4 71D3
CPU_D3#	W41	FSB_D_L<3>	BI	10C4 71D3
CPU_D4#	Y39	FSB_D_L<4>	BI	10C4 71D3
CPU_D5#	V42	FSB_D_L<5>	BI	10C4 71D3
CPU_D6#	Y41	FSB_D_L<6>	BI	10C4 71D3
CPU_D7#	Y42	FSB_D_L<7>	BI	10C4 71D3
CPU_D8#	P42	FSB_D_L<8>	BI	10C4 71D3
CPU_D9#	U41	FSB_D_L<9>	BI	10C4 71D3
CPU_D10#	R42	FSB_D_L<10>	BI	10C4 71D3
CPU_D11#	T39	FSB_D_L<11>	BI	10C4 71D3
CPU_D12#	T42	FSB_D_L<12>	BI	10C4 71D3
CPU_D13#	T41	FSB_D_L<13>	BI	10C4 71D3
CPU_D14#	R41	FSB_D_L<14>	BI	10C4 71D3
CPU_D15#	T43	FSB_D_L<15>	BI	10C4 71D3
CPU_D16#	W35	FSB_D_L<16>	BI	10C4 71D3
CPU_D17#	AA37	FSB_D_L<17>	BI	10C4 71D3
CPU_D18#	W33	FSB_D_L<18>	BI	10C4 71D3
CPU_D19#	W34	FSB_D_L<19>	BI	10C4 71D3
CPU_D20#	AA36	FSB_D_L<20>	BI	10C4 71D3
CPU_D21#	AA34	FSB_D_L<21>	BI	10B4 71D3
CPU_D22#	AA38	FSB_D_L<22>	BI	10B4 71D3
CPU_D23#	AA35	FSB_D_L<23>	BI	10B4 71D3
CPU_D24#	U38	FSB_D_L<24>	BI	10B4 71D3
CPU_D25#	U36	FSB_D_L<25>	BI	10B4 71D3
CPU_D26#	U35	FSB_D_L<26>	BI	10B4 71D3
CPU_D27#	U33	FSB_D_L<27>	BI	10B4 71D3
CPU_D28#	U34	FSB_D_L<28>	BI	10B4 71D3
CPU_D29#	W38	FSB_D_L<29>	BI	10B4 71D3
CPU_D30#	R33	FSB_D_L<30>	BI	10B4 71D3
CPU_D31#	U37	FSB_D_L<31>	BI	10B4 71D3
CPU_D32#	N34	FSB_D_L<32>	BI	10C2 71D3
CPU_D33#	N33	FSB_D_L<33>	BI	10C2 71D3
CPU_D34#	R34	FSB_D_L<34>	BI	10C2 71D3
CPU_D35#	R35	FSB_D_L<35>	BI	10C2 71D3
CPU_D36#	P35	FSB_D_L<36>	BI	10C2 71D3
CPU_D37#	R39	FSB_D_L<37>	BI	10C2 71D3
CPU_D38#	R37	FSB_D_L<38>	BI	10C2 71D3
CPU_D39#	R38	FSB_D_L<39>	BI	10C2 71D3
CPU_D40#	L37	FSB_D_L<40>	BI	10C2 71D3
CPU_D41#	L39	FSB_D_L<41>	BI	10C2 71D3
CPU_D42#	L38	FSB_D_L<42>	BI	10C2 71D3
CPU_D43#	N36	FSB_D_L<43>	BI	10C2 71D3
CPU_D44#	N38	FSB_D_L<44>	BI	10C2 71D3
CPU_D45#	J39	FSB_D_L<45>	BI	10C2 71D3
CPU_D46#	J38	FSB_D_L<46>	BI	10C2 71D3
CPU_D47#	J37	FSB_D_L<47>	BI	10C2 71D3
CPU_D48#	L42	FSB_D_L<48>	BI	10C2 71D3
CPU_D49#	M42	FSB_D_L<49>	BI	10C2 71D3
CPU_D50#	P41	FSB_D_L<50>	BI	10C2 71D3
CPU_D51#	N41	FSB_D_L<51>	BI	10C2 71D3
CPU_D52#	N40	FSB_D_L<52>	BI	10C2 71D3
CPU_D53#	M40	FSB_D_L<53>	BI	10B2 71D3
CPU_D54#	H40	FSB_D_L<54>	BI	10B2 71D3
CPU_D55#	K42	FSB_D_L<55>	BI	10B2 71D3
CPU_D56#	H41	FSB_D_L<56>	BI	10B2 71D3
CPU_D57#	L41	FSB_D_L<57>	BI	10B2 71D3
CPU_D58#	H43	FSB_D_L<58>	BI	10B2 71D3
CPU_D59#	H42	FSB_D_L<59>	BI	10B2 71D3
CPU_D60#	K41	FSB_D_L<60>	BI	10B2 71D3
CPU_D61#	J40	FSB_D_L<61>	BI	10B2 71D3
CPU_D62#	H39	FSB_D_L<62>	BI	10B2 71D3
CPU_D63#	M43	FSB_D_L<63>	BI	10B2 71D3
CPU_BPRI#	AA41	FSB_BPRI_L	OUT	10D6 71C3
CPU_DEFER#	AA40	FSB_DEFER_L	OUT	10D6 71C3
BCLK_OUT_CPU_P	G42	FSB_CLK_CPU_P	OUT	10B6 71B3
BCLK_OUT_CPU_N	G41	FSB_CLK_CPU_N	OUT	10B6 71B3
BCLK_OUT_ITP_P	AL43	FSB_CLK_ITP_P	OUT	13C3 71B3
BCLK_OUT_ITP_N	AL42	FSB_CLK_ITP_N	OUT	13C3 71B3
BCLK_OUT_NB_P	AL41	71B3 FSB_CLK_MCP_P		
BCLK_OUT_NB_N	AK42	71B3 FSB_CLK_MCP_N		
BCLK_IN_N	AK41			
BCLK_IN_P	AJ40			
CPU_A20M#	AF41	CPU_A20M_L	OUT	10C8 71C3
CPU_IGNNE#	AH39	CPU_IGNNE_L	OUT	10C8 71C3
CPU_INIT#	AH42	CPU_INIT_L	OUT	10D6 71C3
CPU_INTR	AF42	CPU_INTR	OUT	9B2 10C8 71C3
CPU_NMI	AG41	CPU_NMI	OUT	9B2 10B8 71C3
CPU_SMI#	AH41	CPU_SMI_L	OUT	10B8 71B3
CPU_PWRGD	AH43	CPU_PWRGD		
CPU_RESET#	H38	FSB_CPURST_L	OUT	9B2 10D6 13C2 71C3
CPU_SLP#	AM33	FSB_CPUSLP_L	OUT	10B2 71B3
CPU_DPSLP#	AN33	CPU_DPSLP_L	OUT	10B2 71B3
CPU_DPWR#	AM32	FSB_DPWR_L	OUT	10B2 71B3
CPU_STPCLK#	AG42	CPU_STPCLK_L	OUT	10C8 71B3
CPU_DPRSTP#	AN32	CPU_DPRSTP_L	OUT	9C2 10B2 60C7 71B3

Loop-back clock for delay matching.

24C8 22D3 14A2 9C2 8D7 =PP1V05_S0_MCP_FSB

R1410 54.9 1% 1/16W MF-LF 402
R1415 62 5% 1/16W MF-LF 402
R1416 62 5% 1/16W MF-LF 402

71B3 40C4 10C6 IN PM_THRMTRIP_L
71C3 10C8 IN CPU_FERR_L

NO STUFF
R1420 1K 5% 1/16W MF-LF 402
NO STUFF
R1421 1K 5% 1/16W MF-LF 402
NO STUFF
R1422 1K 5% 1/16W MF-LF 402

R1430 49.9 1% 1/16W MF-LF 402
R1435 49.9 1% 1/16W MF-LF 402
R1431 49.9 1% 1/16W MF-LF 402
R1436 49.9 1% 1/16W MF-LF 402

=PP1V05_S0_MCP_FSB 8D7 9C2 14B7 22D3 24C8
NO STUFF
R1440 150 5% 1/16W MF-LF 402
OUT 10B2 13C7 71C3

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP CPU Interface

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

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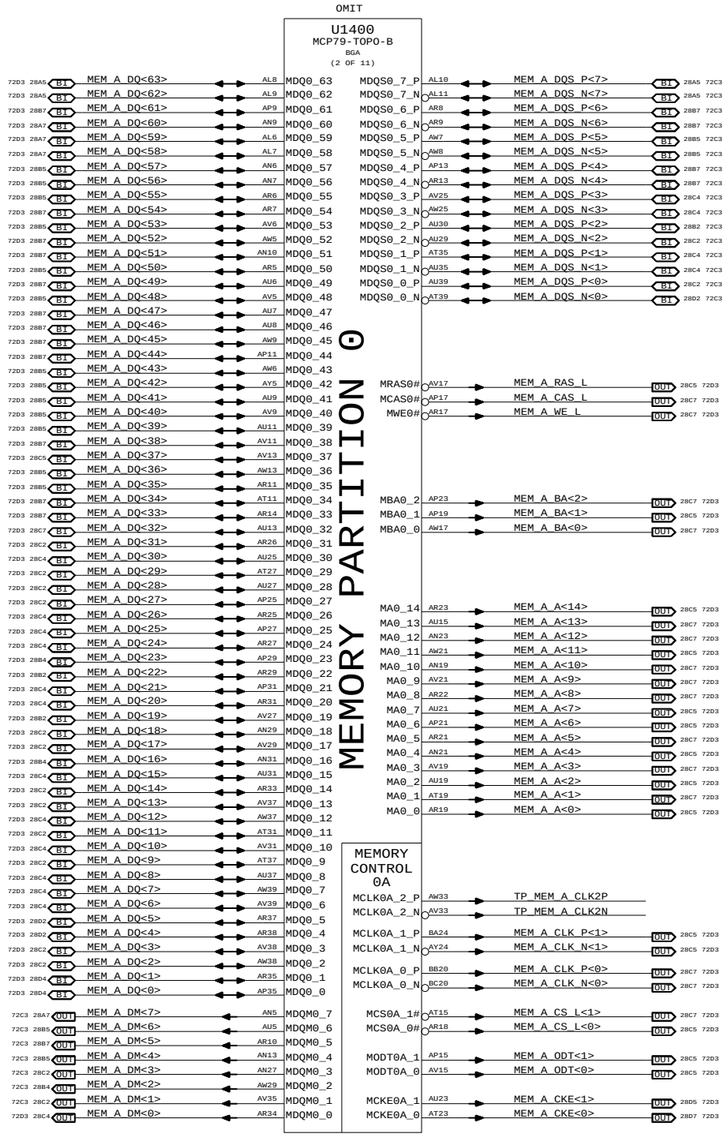
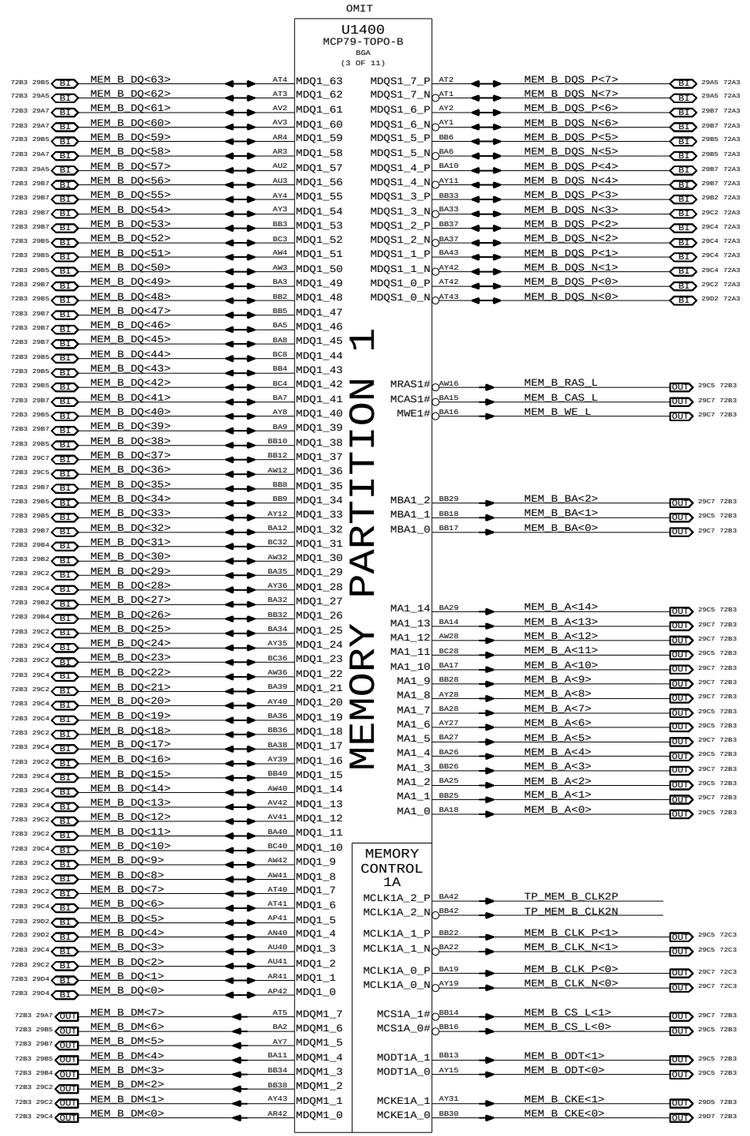
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	14	109





MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 15 OF 109	

OMIT

U1400
MCP79-TOPO-B
BGA
(4 OF 11)

MEMORY CONTROL 0B

TP_MEM_A_CLK5P	AU33	MCLK0B_2_P
TP_MEM_A_CLK5N	AU34	MCLK0B_2_N
TP_MEM_A_CLK4P	BB24	MCLK0B_1_P
TP_MEM_A_CLK4N	BC24	MCLK0B_1_N
TP_MEM_A_CLK3P	BA21	MCLK0B_0_P
TP_MEM_A_CLK3N	BB21	MCLK0B_0_N
TP_MEM_A_CS_L<2>	AU17	MCS0B_0#
TP_MEM_A_CS_L<3>	AR15	MCS0B_1#
TP_MEM_A_ODT<2>	AN17	MODT0B_0
TP_MEM_A_ODT<3>	AN15	MODT0B_1
TP_MEM_A_CKE<2>	AV23	MCKE0B_0
TP_MEM_A_CKE<3>	AN25	MCKE0B_1

MEMORY CONTROL 1B

MCLK1B_2_P	BA41	TP_MEM_B_CLK5P
MCLK1B_2_N	BB41	TP_MEM_B_CLK5N
MCLK1B_1_P	AY23	TP_MEM_B_CLK4P
MCLK1B_1_N	BA23	TP_MEM_B_CLK4N
MCLK1B_0_P	BA20	TP_MEM_B_CLK3P
MCLK1B_0_N	AY20	TP_MEM_B_CLK3N
MCS1B_0#	BC16	TP_MEM_B_CS_L<2>
MCS1B_1#	BA13	TP_MEM_B_CS_L<3>
MODT1B_0	AY16	TP_MEM_B_ODT<2>
MODT1B_1	BC13	TP_MEM_B_ODT<3>
MCKE1B_0	BA30	TP_MEM_B_CKE<2>
MCKE1B_1	BA31	TP_MEM_B_CKE<3>

24C8 16C3 8B7 =PP1V8R1V5_S0_MCP_MEM

R1610 1
40.2
1%
1/16W
MF-LF
402
2

R1611 1
40.2
1%
1/16W
MF-LF
402
2

72A3 MCP_MEM_COMP_VDD — AN41 MEM_COMP_VDD
72A3 MCP_MEM_COMP_GND — AM41 MEM_COMP_GND

24B2 PP1V05_S0_MCP_PLL_CORE
87 mA (A01)

17 mA	T27	+V_PLL_XREF_XS
12 mA	U28	+V_PLL_DP
19 mA	U27	+V_PLL_CORE
39 mA	T28	+V_VPLL

MRESET0# AY32 — MCP_MEM_RESET_L (OUT) 30B6
TP or NC for DDR2.

=PP1V8R1V5_S0_MCP_MEM 8B7 16C7 24C8
4771 mA (A01, DDR3)

+VDD_MEM1	AM17	GND1 AA22
+VDD_MEM2	AM19	GND2 AP12
+VDD_MEM3	AM21	GND3 G30
+VDD_MEM4	AM23	GND4 P10
+VDD_MEM5	AM25	GND5 T10
+VDD_MEM6	AM27	GND6 T6
+VDD_MEM7	AM29	GND7 V10
+VDD_MEM8	AN16	GND8 V34
+VDD_MEM9	BC29	GND9 W5
+VDD_MEM10	AN20	GND10 AA39
+VDD_MEM11	AN24	GND11 AB22
+VDD_MEM12	AT17	GND12 AB7
+VDD_MEM13	AP16	GND13 AD22
+VDD_MEM14	AN22	GND14 AE20
+VDD_MEM15	AP20	GND15 AF24
+VDD_MEM16	AP24	GND16 AG24
+VDD_MEM17	AV16	GND17 AH35
+VDD_MEM18	AR16	GND18 AK7
+VDD_MEM19	AR20	GND19 AM28
+VDD_MEM20	AR24	GND20 AT25
+VDD_MEM21	AW15	GND21 AP30
+VDD_MEM22	AP22	GND22 AR36
+VDD_MEM23	AP18	GND23 AU10
+VDD_MEM24	AU16	GND24 F28
+VDD_MEM25	AN18	GND25 BC21
+VDD_MEM26	AU24	GND26 AY9
+VDD_MEM27	AT21	GND27 BC9
+VDD_MEM28	AY29	GND28 D34
+VDD_MEM29	AV24	GND29 F24
+VDD_MEM30	AU20	GND30 G32
+VDD_MEM31	AU22	GND31 H31
+VDD_MEM32	AW27	GND32 K7
+VDD_MEM33	BC17	GND33 M38
+VDD_MEM34	AV20	GND34 M5
+VDD_MEM35	AY17	GND35 M6
+VDD_MEM36	AY18	GND36 M7
+VDD_MEM37	AM15	GND37 M9
+VDD_MEM38	AU18	GND38 N39
+VDD_MEM39	AY25	GND39 N8
+VDD_MEM40	AY26	GND40 P33
+VDD_MEM41	AW19	GND41 P34
+VDD_MEM42	AW24	GND42 P37
+VDD_MEM43	BC25	GND43 P4
+VDD_MEM44	AL30	GND44 P40
+VDD_MEM45	AM31	GND45 P7
		GND46 R36
		GND47 R40
		GND48 R43
		GND49 R5
		GND50 T18
		GND51 T20
		GND52 AK11
		GND53 T24
		GND54 T26

GND55	T33	
GND56	T34	
GND57	T35	
GND58	T37	
GND59	T38	
GND60	T7	
GND61	T9	
GND62	U18	
GND63	U20	
GND64	U22	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Memory Misc

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 16 OF 109	

OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS

9D6	IN	=PEG_D2R_P<0>	F7	PE0_RX0_P	C5	PE0_TX0_P	=PEG_R2D_C_P<0>
9D6	IN	=PEG_D2R_N<0>	E7	PE0_RX0_N	D4	PE0_TX0_N	=PEG_R2D_C_N<0>
9D6	IN	=PEG_D2R_P<1>	D7	PE0_RX1_P	C4	PE0_TX1_P	=PEG_R2D_C_P<1>
9D6	IN	=PEG_D2R_N<1>	C7	PE0_RX1_N	B4	PE0_TX1_N	=PEG_R2D_C_N<1>
9D6	IN	=PEG_D2R_P<2>	E6	PE0_RX2_P	A4	PE0_TX2_P	=PEG_R2D_C_P<2>
9D6	IN	=PEG_D2R_N<2>	F6	PE0_RX2_N	A3	PE0_TX2_N	=PEG_R2D_C_N<2>
9D6	IN	=PEG_D2R_P<3>	E5	PE0_RX3_P	B3	PE0_TX3_P	=PEG_R2D_C_P<3>
9D6	IN	=PEG_D2R_N<3>	F5	PE0_RX3_N	B2	PE0_TX3_N	=PEG_R2D_C_N<3>
9D6	IN	=PEG_D2R_P<4>	E4	PE0_RX4_P	C1	PE0_TX4_P	=PEG_R2D_C_P<4>
9D6	IN	=PEG_D2R_N<4>	E3	PE0_RX4_N	D1	PE0_TX4_N	=PEG_R2D_C_N<4>
9D6	IN	=PEG_D2R_P<5>	C3	PE0_RX5_P	D2	PE0_TX5_P	=PEG_R2D_C_P<5>
9D6	IN	=PEG_D2R_N<5>	D3	PE0_RX5_N	E1	PE0_TX5_N	=PEG_R2D_C_N<5>
9D6	IN	=PEG_D2R_P<6>	G5	PE0_RX6_P	E2	PE0_TX6_P	=PEG_R2D_C_P<6>
9D6	IN	=PEG_D2R_N<6>	H5	PE0_RX6_N	F2	PE0_TX6_N	=PEG_R2D_C_N<6>
9D6	IN	=PEG_D2R_P<7>	J7	PE0_RX7_P	F3	PE0_TX7_P	=PEG_R2D_C_P<7>
9D6	IN	=PEG_D2R_N<7>	J6	PE0_RX7_N	F4	PE0_TX7_N	=PEG_R2D_C_N<7>
9D6	IN	=PEG_D2R_P<8>	J5	PE0_RX8_P	G3	PE0_TX8_P	=PEG_R2D_C_P<8>
9D6	IN	=PEG_D2R_N<8>	J4	PE0_RX8_N	H4	PE0_TX8_N	=PEG_R2D_C_N<8>
9D6	IN	=PEG_D2R_P<9>	L11	PE0_RX9_P	H3	PE0_TX9_P	=PEG_R2D_C_P<9>
9D6	IN	=PEG_D2R_N<9>	L10	PE0_RX9_N	H2	PE0_TX9_N	=PEG_R2D_C_N<9>
9D6	IN	=PEG_D2R_P<10>	L9	PE0_RX10_P	H1	PE0_TX10_P	=PEG_R2D_C_P<10>
9D6	IN	=PEG_D2R_N<10>	L8	PE0_RX10_N	J1	PE0_TX10_N	=PEG_R2D_C_N<10>
9D6	IN	=PEG_D2R_P<11>	L7	PE0_RX11_P	J2	PE0_TX11_P	=PEG_R2D_C_P<11>
9D6	IN	=PEG_D2R_N<11>	L6	PE0_RX11_N	J3	PE0_TX11_N	=PEG_R2D_C_N<11>
9D6	IN	=PEG_D2R_P<12>	N11	PE0_RX12_P	K2	PE0_TX12_P	=PEG_R2D_C_P<12>
9D6	IN	=PEG_D2R_N<12>	N10	PE0_RX12_N	K3	PE0_TX12_N	=PEG_R2D_C_N<12>
9D6	IN	=PEG_D2R_P<13>	N9	PE0_RX13_P	L4	PE0_TX13_P	=PEG_R2D_C_P<13>
9D6	IN	=PEG_D2R_N<13>	P8	PE0_RX13_N	L3	PE0_TX13_N	=PEG_R2D_C_N<13>
9D6	IN	=PEG_D2R_P<14>	N7	PE0_RX14_P	M4	PE0_TX14_P	=PEG_R2D_C_P<14>
9D6	IN	=PEG_D2R_N<14>	N6	PE0_RX14_N	M3	PE0_TX14_N	=PEG_R2D_C_N<14>
9D6	IN	=PEG_D2R_P<15>	N5	PE0_RX15_P	M2	PE0_TX15_P	=PEG_R2D_C_P<15>
9D6	IN	=PEG_D2R_N<15>	N4	PE0_RX15_N	M1	PE0_TX15_N	=PEG_R2D_C_N<15>

9D6	IN	PEG_PRSNT_L	C9	PE0_PRSNT_16# Int PU	E11	PE0_REFCLK_P	PEG_CLK100M_P 9D6
					D11	PE0_REFCLK_N	PEG_CLK100M_N 9D6
31D7	IN	MINI_CLKREQ_L	D5	PEB_CLKREQ#/GPIO_49 Int PU	G11	PE1_REFCLK_P	PCIE_CLK100M_MINI_P 31C5 73D3
31D7 9C6	IN	PCIE_MINI_PRSNT_L	D9	PEB_PRSNT# Int PU	F11	PE1_REFCLK_N	PCIE_CLK100M_MINI_N 31C5 73D3
9D6	IN	FW_CLKREQ_L	E8	PEC_CLKREQ#/GPIO_50 Int PU	J11	PE2_REFCLK_P	PCIE_CLK100M_FW_P 9D6
9D6	IN	PCIE_FW_PRSNT_L	C10	PEC_PRSNT# Int PU	J10	PE2_REFCLK_N	PCIE_CLK100M_FW_N 9C6
9C6	IN	EXCARD_CLKREQ_L	M15	PED_CLKREQ#/GPIO_51 Int PU	G13	PE3_REFCLK_P	PCIE_CLK100M_EXCARD_P 9C6
9C6	IN	PCIE_EXCARD_PRSNT_L	B10	PED_PRSNT# Int PU	F13	PE3_REFCLK_N	PCIE_CLK100M_EXCARD_N 9C6
9C6		TP_PE4_CLKREQ_L	L16	PEE_CLKREQ#/GPIO_16 Int PU	J13	PE4_REFCLK_P	TP_PCIE_CLK100M_PE4P 9C6
9C6		TP_PE4_PRSNT_L	L18	PEE_PRSNT#/GPIO_46 Int PU	H13	PE4_REFCLK_N	TP_PCIE_CLK100M_PE4N 9C6
		TP_MCP_GPIO_17	M16	PEF_CLKREQ#/GPIO_17 Int PU	L14	PE5_REFCLK_P	TP_PCIE_CLK100M_PE5P
9C4	OUT	GMUX_JTAG_TCK_L	M18	PEF_PRSNT#/GPIO_47 Int PU	K14	PE5_REFCLK_N	TP_PCIE_CLK100M_PE5N
		TP_MCP_GPIO_18	M17	PEG_CLKREQ#/GPIO_18 Int PU	N14	PE6_REFCLK_P	TP_PCIE_CLK100M_PE6P
9C4	IN	GMUX_JTAG_TDO	M19	PEG_PRSNT#/GPIO_48 Int PU	M14	PE6_REFCLK_N	TP_PCIE_CLK100M_PE6N
31C7 23C5 7D5	IN	PCIE_WAKE_L	F17	PE_WAKE# Int PU (S5)	K11	PEX_RST0#	PCIE_RESET_L 26C4
73D3 31C7 7D5	IN	PCIE_MINI_D2R_P	K9	PE1_RX0_P	D8	PE1_TX0_P	PCIE_MINI_R2D_C_P 31C5 73D3
73D3 31C7 7D5	IN	PCIE_MINI_D2R_N	J9	PE1_RX0_N	C8	PE1_TX0_N	PCIE_MINI_R2D_C_N 31C5 73D3
9D6	IN	PCIE_FW_D2R_P	H9	PE1_RX1_P	B8	PE1_TX1_P	PCIE_FW_R2D_C_P 9D6
9D6	IN	PCIE_FW_D2R_N	G9	PE1_RX1_N	A8	PE1_TX1_N	PCIE_FW_R2D_C_N 9D6
9C6	IN	PCIE_EXCARD_D2R_P	F9	PE1_RX2_P	A7	PE1_TX2_P	PCIE_EXCARD_R2D_C_P 9C6
9C6	IN	PCIE_EXCARD_D2R_N	E9	PE1_RX2_N	B7	PE1_TX2_N	PCIE_EXCARD_R2D_C_N 9C6
9B6		TP_PCIE_PE4_D2RP	H7	PE1_RX3_P	B6	PE1_TX3_P	TP_PCIE_PE4_R2D_CP 9B6
9B6		TP_PCIE_PE4_D2RN	G7	PE1_RX3_N	C6	PE1_TX3_N	TP_PCIE_PE4_R2D_CN 9B6

8A6	=PP1V05_S0_MCP_PEX_DVDD0	T17	+DVDD0_PEX1	Y12	+AVDD0_PEX1	=PP1V05_S0_MCP_PEX_AVDD0 8A6	
	57 mA (A01, DVDD0 & 1)	W19	+DVDD0_PEX2	AA12	+AVDD0_PEX2	206 mA (A01, AVDD0 & 1)	
		U17	+DVDD0_PEX3	AB12	+AVDD0_PEX3		
		V19	+DVDD0_PEX4	M12	+AVDD0_PEX4		
		W16	+DVDD0_PEX5	P12	+AVDD0_PEX5		
		W17	+DVDD0_PEX6	R12	+AVDD0_PEX6		
		W18	+DVDD0_PEX7	N12	+AVDD0_PEX7		
		U16	+DVDD0_PEX8	T12	+AVDD0_PEX8		
				U12	+AVDD0_PEX9		
8A6	=PP1V05_S0_MCP_PEX_DVDD1	T19	+DVDD1_PEX1	AC12	+AVDD0_PEX10		
		U19	+DVDD1_PEX2	AD12	+AVDD0_PEX11		
				V12	+AVDD0_PEX12		
				W12	+AVDD0_PEX13		
24C2	PP1V05_S0_MCP_PLL_PEX	T16	+V_PLL_PEX			=PP1V05_S0_MCP_PEX_AVDD1 8A6	
	84 mA (A01)				+AVDD1_PEX1		
				M13			
				N13	+AVDD1_PEX2		
73C3	MCP_PEX_CLK_COMP	A11	PEX_CLK_COMP	P13	+AVDD1_PEX3		

NO STUFF
R1710
2.37K
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 12.7mm of U1400

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	17	109

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

OMIT

U1400
MCP79-TOPO-B
BGA
(6 OF 11)

LAN

75D3 33C1 IN ENET_RXD<0>	C23	RGMII_RXD0	
75D3 33C1 IN ENET_RXD<1>	B23	RGMII_RXD1	
75D3 33C1 IN ENET_RXD<2>	E24	RGMII_RXD2	
75D3 33C1 IN ENET_RXD<3>	A24	RGMII_RXD3	
75D3 33C1 IN ENET_CLK125M_RXCLK	A23	RGMII_RXC/MII_RXCLK	
75D3 33B1 IN ENET_RX_CTRL	C22	RGMII_RXCTL/MII_RXDV	
9C4 IN =MCP_MII_RXER	F23	MII_RXER/GPIO_36	
9C4 IN =MCP_MII_COL	B26	MII_COL/GPIO_20/MSMB_DATA	
9C4 IN =MCP_MII_CRS	B22	MII_CRS/GPIO_21/MSMB_CLK	
TP_ENET_INTR_L	J22	RGMII_INTR/GPIO_35	
24A6 PP1V05_ENET_MCP_PLL_MAC 5 mA (A01)	T23	+V_DUAL_MACPLL	
75D3 MCP_MII_COMP_VDD	C27	MII_COMP_VDD	
75D3 MCP_MII_COMP_GND	B27	MII_COMP_GND	
TP_MCP_RGB_DAC_RSET	C39	RGB_DAC_RSET	
TP_MCP_RGB_DAC_VREF	B38	RGB_DAC_VREF	
9D4 OUT MCP_TV_DAC_RSET	E36	TV_DAC_RSET	
9D4 OUT MCP_TV_DAC_VREF	A35	TV_DAC_VREF	
9D4 IN MCP_CLK27M_XTALIN	C38	XTALIN_TV	
9D4 OUT MCP_CLK27M_XTALOUT	D38	XTALOUT_TV	
41C3 B1 LPCPLUS_GPIO	E16	GPIO_6/FERR*/IGPU_GPIO_6	
67A5 IN DP_IG_CA_DET	B15	GPIO_7/NFERR*/IGPU_GPIO_7	
70B7 69A8 OUT LVDS_IG_BKL_PWM (See below)	G39	LCD_BKL_CTL/GPIO_57	
70C8 70B7 OUT LVDS_IG_BKL_ON	E37	LCD_BKL_ON/GPIO_59	
66B8 OUT LVDS_IG_PANEL_PWR	F40	LCD_PANEL_PWR/GPIO_58	
67D3 OUT =MCP_HDMI_TXC_P	D35	HDMI_TXC_P/ML0_LANE3_P	
67D3 OUT =MCP_HDMI_TXC_N	E35	HDMI_TXC_N/ML0_LANE3_N	
67D3 OUT =MCP_HDMI_TXD_P<0>	G35	HDMI_TXD0_P/ML0_LANE2_P	
67D3 OUT =MCP_HDMI_TXD_N<0>	F35	HDMI_TXD0_N/ML0_LANE2_N	
67D3 OUT =MCP_HDMI_TXD_P<1>	F33	HDMI_TXD1_P/ML0_LANE1_P	
67D3 OUT =MCP_HDMI_TXD_N<1>	G33	HDMI_TXD1_N/ML0_LANE1_N	
67D3 OUT =MCP_HDMI_TXD_P<2>	J33	HDMI_TXD2_P/ML0_LANE0_P	
67D3 OUT =MCP_HDMI_TXD_N<2>	H33	HDMI_TXD2_N/ML0_LANE0_N	
73B3 67C7 OUT DP_IG_AUX_CH_P	D43	DP_AUX_CH0_P	
73B3 67C7 OUT DP_IG_AUX_CH_N	C43	DP_AUX_CH0_N	
9B4 IN =DVI_HPD_GMUX_INT (See below)	C31	HPLUG_DET2/GPIO_22	
67D3 IN =MCP_HDMI_HPD	F31	HPLUG_DET3	
25D7 8A7 =PP3V3R1V8_S0_MCP_IFP_VDD 190 mA (A01, 1.8V)	M27	+VDD_IFPA	
	M26	+VDD_IFPB	
25C5 PP3V3_S0_MCP_VPLL 16 mA (A01)	M28	+V_PLL_IFPAB (8 mA)	
	M29	+V_PLL_HDMI (8 mA)	
25D7 8B7 =PP1V05_S0_MCP_HDMI_VDD 95 mA (A01)	T25	+VDD_HDMI	
73B3 25C7 OUT MCP_HDMI_RSET	J31	HDMI_RSET	
73B3 25C7 OUT MCP_HDMI_VPROBE	J30	HDMI_VPROBE	

DACS

RGB ONLY

TV / Component
C / Pr
Y / Y
Comp / Pb

+3.3V_DUAL_RMGT1 J24	=PP3V3_ENET_MCP_RMGT	8B1 18D7 24A5 24B6	83 mA (A01)
+3.3V_DUAL_RMGT2 K24			
+V_DUAL_RMGT1 U23	=PP1V05_ENET_MCP_RMGT	8B1 24D6	131 mA (A01)
+V_DUAL_RMGT2 V23			
MII_VREF E28	MCP_MII_VREF	IN 24A4	
RGMII_TXD0 B24	ENET_TXD<0>	OUT 33C6 75D3	
RGMII_TXD1 C24	ENET_TXD<1>	OUT 33C6 75D3	
RGMII_TXD2 C25	ENET_TXD<2>	OUT 33C6 75D3	
RGMII_TXD3 D25	ENET_TXD<3>	OUT 33C6 75D3	
RGMII_TXC/MII_TXCLK D24	ENET_CLK125M_TXCLK	OUT 33C8 75D3	
RGMII_TXCTL/MII_TXEN C26	ENET_TX_CTRL	OUT 33B6 75C3	
RGMII_MDC D21	ENET_MDC	OUT 33B6 75D3	
RGMII_MDIO C21	ENET_MDIO	B1 33B6 75D3	
RGMII_PWRDWN/GPIO_37 G23	TP_ENET_PWRDWN_L		
BUF_25MHZ E23	MCP_CLK25M_BUF0_R	OUT 34A5 75D3	
MII_RESET# J23	ENET_RESET_L	OUT 33B7 75C3	
+V_RGB_DAC J32	PP3V3_S0_MCP_DAC 103 mA	25D2 206 mA (A01)	
+V_TV_DAC K32	103 mA		
DDC_CLK0 B31	MCP_DDC_CLK0		
DDC_DATA0 A31	MCP_DDC_DATA0		
RGB_DAC_RED B39	TP_MCP_RGB_RED		
RGB_DAC_GREEN A39	TP_MCP_RGB_GREEN		
RGB_DAC_BLUE B40	TP_MCP_RGB_BLUE		
RGB_DAC_HSYNC A40	TP_MCP_RGB_HSYNC		
RGB_DAC_VSYNC A41	TP_MCP_RGB_VSYNC		
TV_DAC_RED A36	CRT_IG_R_C_PR	OUT 9D4	
TV_DAC_GREEN B36	CRT_IG_G_Y_Y	OUT 9D4	
TV_DAC_BLUE C36	CRT_IG_B_COMP_PB	OUT 9D4	
TV_DAC_HSYNC/GPIO_44 D36	CRT_IG_HSYNC	OUT 9D4	
TV_DAC_VSYNC/GPIO_45 C37	CRT_IG_VSYNC	OUT 9D4	

FLAT PANEL

IFPA_TXC_P B35	LVDS_IG_A_CLK_P	OUT 66B3 73B3	
IFPA_TXC_N C35	LVDS_IG_A_CLK_N	OUT 66B3 73B3	
IFPA_TXD0_P B32	LVDS_IG_A_DATA_P<0>	OUT 7C7 66C2 73B3	
IFPA_TXD0_N A32	LVDS_IG_A_DATA_N<0>	OUT 7C7 66C2 73B3	
IFPA_TXD1_P D32	LVDS_IG_A_DATA_P<1>	OUT 7C7 66C2 73B3	
IFPA_TXD1_N C32	LVDS_IG_A_DATA_N<1>	OUT 7C7 66C2 73B3	
IFPA_TXD2_P D33	LVDS_IG_A_DATA_P<2>	OUT 7C7 66C2 73B3	
IFPA_TXD2_N C33	LVDS_IG_A_DATA_N<2>	OUT 7C7 66C2 73B3	
IFPA_TXD3_P B34	LVDS_IG_A_DATA_P<3>	OUT 9D4	
IFPA_TXD3_N C34	LVDS_IG_A_DATA_N<3>	OUT 9D4	
IFPB_TXC_P L31	LVDS_IG_B_CLK_P	OUT 9D4	
IFPB_TXC_N K31	LVDS_IG_B_CLK_N	OUT 9D4	
IFPB_TXD4_P J29	LVDS_IG_B_DATA_P<0>	OUT 9C4	
IFPB_TXD4_N H29	LVDS_IG_B_DATA_N<0>	OUT 9C4	
IFPB_TXD5_P L29	LVDS_IG_B_DATA_P<1>	OUT 9C4	
IFPB_TXD5_N K29	LVDS_IG_B_DATA_N<1>	OUT 9C4	
IFPB_TXD6_P L30	LVDS_IG_B_DATA_P<2>	OUT 9C4	
IFPB_TXD6_N K30	LVDS_IG_B_DATA_N<2>	OUT 9C4	
IFPB_TXD7_P N30	LVDS_IG_B_DATA_P<3>	OUT 9C4	
IFPB_TXD7_N M30	LVDS_IG_B_DATA_N<3>	OUT 9C4	
DDC_CLK2/GPIO_23 C30	LVDS_IG_DDC_CLK	OUT 7C7 66C5	
DDC_DATA2/GPIO_24 B30	LVDS_IG_DDC_DATA	B1 7C7 66C5	
DDC_CLK3 D31	=MCP_HDMI_DDC_CLK	OUT 67D3	
DDC_DATA3 E31	=MCP_HDMI_DDC_DATA	B1 67D3	
IFPAB_RSET E32	MCP_IFPAB_RSET	OUT 25C6 73B3	
IFPAB_VPROBE G31	MCP_IFPAB_VPROBE	OUT 25C6 73B3	

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

R1850 10K 5% 1/16W MF-LF 402

R1810 49.9 1% 1/16W MF-LF 402 — 24B6 24A5 18D3 8B1 =PP3V3_ENET_MCP_RMGT

R1811 49.9 1% 1/16W MF-LF 402

R1820 47K 5% 1/16W MF-LF 402 — 20C1 8A3 =PP3V3_S5_MCP_GPIO

R1860 100K 5% 1/16W MF-LF 402 — =PP3V3_S0_MCP_GPIO 8C5 19D1 21A4

R1861 100K 5% 1/16W MF-LF 402

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

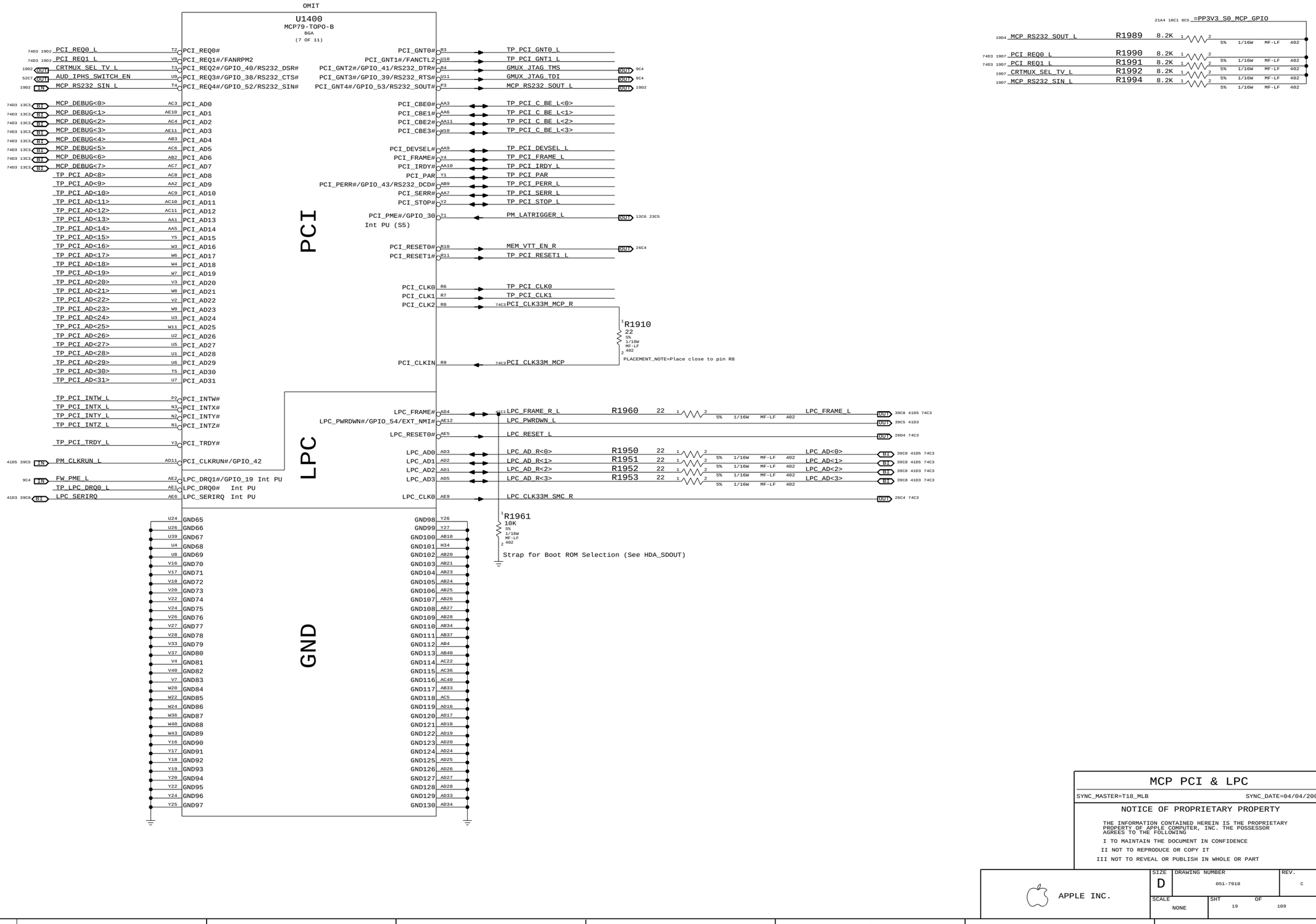
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

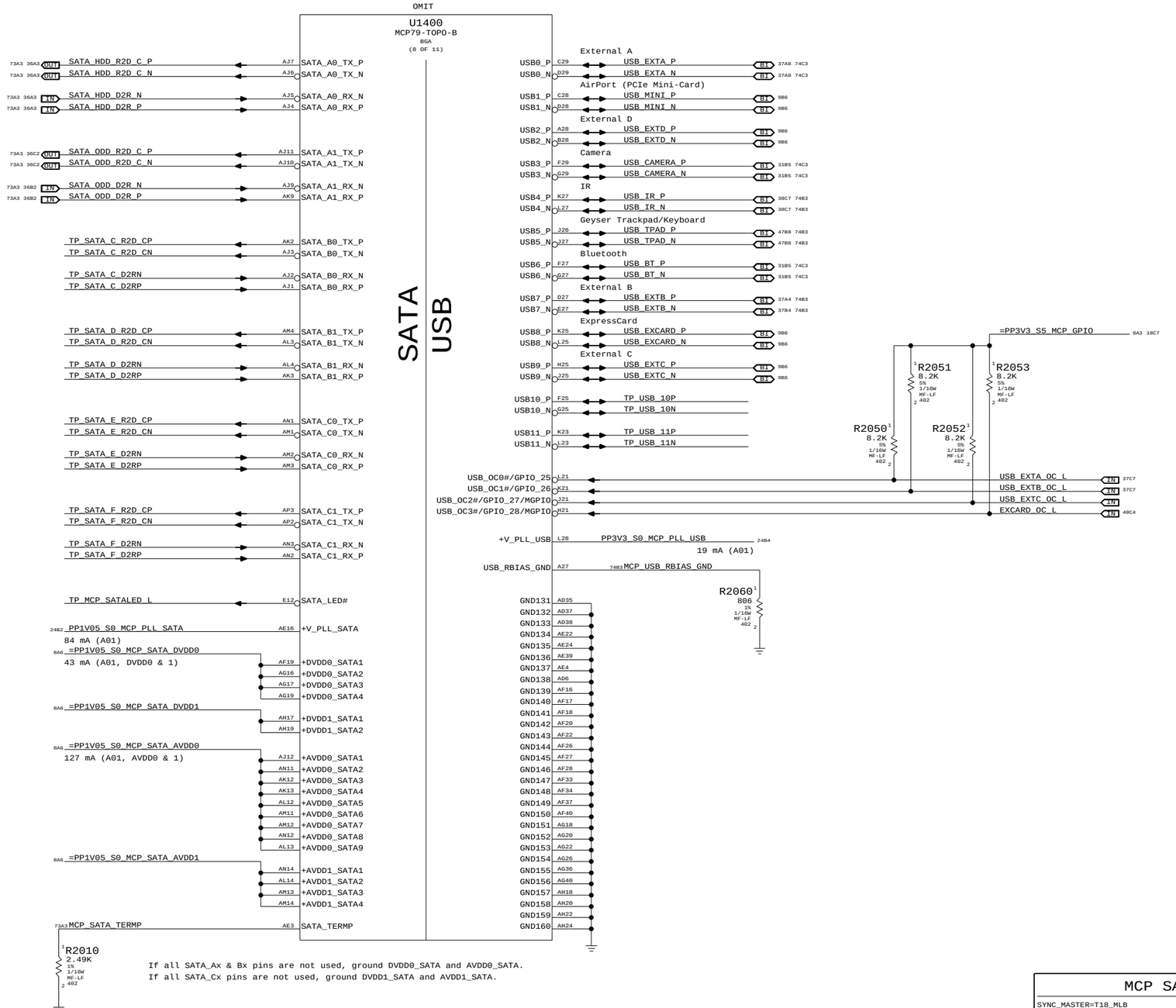
MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 18 OF 109	





MCP SATA & USB

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 20 OF 109	

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OMIT

U1400
MCP79-TOPO-B
BGA
(9 OF 11)

HDA

74A3 51C7 IN	HDA_SDIN0	G15	HDA_SDATA_IN0 Int PD
	TP_MLB_RAM_SIZE	J14	HDA_SDATA_IN1_GPIO_2/PS2_KB_CLK Int PD
	TP_MLB_RAM_VENDOR (MXM_OK for MXM systems)	J15	HDA_SDATA_IN2_GPIO_3/PS2_KB_DATA Int PD
24A8 21D3 8B5 =PP3V3R1V5_S0_MCP_HDA	R2110 49.9 1% 1/16W MF-LF 402		
74A3 MCP_HDA_PULLDN_COMP		A15	HDA_PULLDN_COMP
24A2 PP1V05_S0_MCP_PLL_NV	37 mA (A01)		
	20 mA	AE18	+V_PLL_NV_H
	17 mA	AE17	+V_PLL_SP_SPREF

26D4 22A5 7C3 PP3V3_G3_RTC	R2120 49.9K 1% 1/16W MF-LF 402		
	R2121 49.9K 1% 1/16W MF-LF 402		
41B1 OUT	=SPI_CS1_R_L_USE_MLB	L24	GPIO_1/PWRDN_OK/SPI_CS1
40B2 39D5 34B7 IN	SMC_ADAPTER_EN	L26	GPIO_12_SUS_STAT_ACCLMTR_EXT_TRIG_L
	TP_SB_A20GATE	K13	A20GATE Int PU
	TP_MCP_KBDRSTIN_L	L13	KBRDRSTIN* Int PU
39C5 23C5 IN	SMC_WAKE_SCI_L	C19	SIO_PME* Int PU (S5)
39B8 23C5 IN	SMC_RUNTIME_SCI_L	C18	EXT_SMI/GPIO_32* Int PU (S5)
	SM_INTRUDER_L	B20	INTRUDER*
23C5	TP_MCP_LID_L	M25	LID* Int PU (S5)
39B8 23C5 IN	PM_BATLOW_L	M24	LLB* Int PU (S5)
71B3 60D8 IN	PM_DPRSLPVR	M22	CPU_DPRSLPVR
39C8 23C5 IN	PM_PWRBTN_L	C16	PWRBTN* Int PU (S5)
26A1 23C5 IN	PM_SYSRST_DEBOUNCE_L	D16	RSTBTN* Int PU
	RTC_RST_L	C20	RTC_RST*
39D8 IN	PM_RSMRST_L	D20	PWRGD_SB
26A5 IN	MCP_PS_PWRGD	E20	PS_PWRGD
26A5 IN	MCP_CPU_VLD	C17	CPU_VLD
23C5 13C3 6C5 IN	JTAG_MCP_TDI	E19	JTAG_TDI Int PU
6C4 OUT	JTAG_MCP_TDO	F19	JTAG_TDO
23C5 13C3 6C5 IN	JTAG_MCP_TMS	J19	JTAG_TMS Int PU
13C3 6C5 IN	JTAG_MCP_TRST_L	J18	JTAG_TRST*
13B6 6C5 IN	JTAG_MCP_TCK	G19	JTAG_TCK
26B7 IN	MCP_CLK25M_XTALIN	A16	XTALIN
26C7 OUT	MCP_CLK25M_XTALOUT	B16	XTALOUT
26C7 IN	RTC_CLK32K_XTALIN	A19	XTALIN_RTC
26C7 OUT	RTC_CLK32K_XTALOUT	B19	XTALOUT_RTC

R2150 10K 5% 1/16W MF-LF 402
R2151 100K 5% 1/16W MF-LF 402

MISC

	=PP3V3R1V5_S0_MCP_HDA		8B5 21D8 24A8
			7 mA (A01)
	+V_DUAL_HDA1	J16	
	+V_DUAL_HDA2	K16	
	R2160 8.2K 5% 1/16W MF-LF 402		
74A3 21A7	HDA_SDATA_OUT	F15	HDA_SDOUT_R → R2170 22 5% 1/16W MF-LF 402 → HDA_SDOUT OUT 51C7 74A3
74B3 21A7	HDA_BITCLK	E15	HDA_BIT_CLK_R → R2171 22 5% 1/16W MF-LF 402 → HDA_BIT_CLK OUT 51D7 74B3
74A3 21A7	HDA_RESET*	K15	HDA_RST_R_L → R2172 22 5% 1/16W MF-LF 402 → HDA_RST_L OUT 51C7 74A3
74B3 21A7	HDA_SYNC	L15	HDA_SYNC_R → R2173 22 5% 1/16W MF-LF 402 → HDA_SYNC OUT 51C7 74B3
	HDA_DOCK_EN*_GPIO_4/PS2_MS_CLK	K17	MCP_GPIO_4 21A4
	HDA_DOCK_RST*_GPIO_5/PS2_MS_DATA	L17	AUD_I2C_INT_L IN 21A4 52C7
	SLP_S3*	G17	PM_SLP_S3_L OUT 7C3 34B7 39C5 41A5 64D5 68D8
	SLP_RMGT*	J17	PM_SLP_RMGT_L OUT 9D1
	SLP_S5*	M17	PM_SLP_S4_L OUT 7C3 39C5 40A2 64C8
	THERM_DIODE_P	B11	MCP_THMDIODE_P OUT 45C5 77D3
	THERM_DIODE_N	C11	MCP_THMDIODE_N OUT 45C5 77D3
	MCP_VID0/GPIO_13	L20	MCP_VID<0> OUT 21A3 61B8
	MCP_VID1/GPIO_14	M20	MCP_VID<1> OUT 21A3 61A8
	MCP_VID2/GPIO_15	M21	MCP_VID<2> OUT 21A3 61A8
	SPKR	C13	MCP_SPKR
	SMB_CLK0	L19	SMBUS_MCP_0_CLK OUT 13B6 42D8 74B3
	SMB_DATA0	K19	SMBUS_MCP_0_DATA BI 13B6 42D8 74B3
	SMB_CLK1/MSMB_CLK	G21	SMBUS_MCP_1_CLK OUT 42C8 74B3
	SMB_DATA1/MSMB_DATA	F21	SMBUS_MCP_1_DATA BI 42C8 74B3
	SMB_ALERT*/GPIO_64	M23	AP_PWR_EN OUT 21A3 31D5 34C7
(MGPIO2)	FANRPM0/GPIO_60	B12	MEM_EVENT_L IN 21A4 28A5 29A5 39B8
	FANCTL0/GPIO_61	A12	ODD_PWR_EN_L OUT 36C6
(MGPIO3)	FANRPM1/GPIO_63	D12	SMC_IG_THROTTLE_L IN 21A4 40D4
	FANCTL1/GPIO_62	C12	ARB_DETECT 21A4
	CPUVDD_EN	D17	MCP_CPUVDD_EN OUT 26A8
	SPI_CS0/GPIO_10	C14	SPI_CS0_R_L OUT 41B7 74A3
	SPI_CLK/GPIO_11	D13	SPI_CLK_R OUT 41A5 41C8 74A3
	SPI_DI/GPIO_8	C15	SPI_MISO IN 41A5 41B7 74A3
	SPI_DO/GPIO_9	B14	SPI_MOSI_R OUT 41A5 41C7 74A3
	SUS_CLK/GPIO_34	B18	PM_CLK32K_SUSCLK_R OUT 26B4 74A3
	BUF_SIO_CLK	AE7	TP_MCP_BUF_SIO_CLK
	TEST_MODE_EN	K22	MCP_TEST_MODE_EN
	PKG_TEST	L22	

R2163 10K 5% 1/16W MF-LF 402
R2190 1K 1% 1/16W MF-LF 402

=PP3V3_S0_MCP 8C5 22B3 24B8
R2180 10K 5% 1/16W MF-LF 402 → OUT 23B5 BOOT_MODE_USER
R2181 10K 5% 1/16W MF-LF 402

USER mode: Normal
SAFE mode: For ROMSIP recovery

Connects to SMC for automatic recovery.

BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface

HDA_SDOUT_R 21D4 74A3
HDA_BIT_CLK_R 21D4 74B3
HDA_RST_R_L 21D4 74A3
HDA_SYNC_R 21D4 74B3

C2170 10PF 5% 50V CERM 402
C2172 10PF 5% 50V CERM 402
C2171 10PF 5% 50V CERM 402
C2173 10PF 5% 50V CERM 402

=PP3V3_S0_MCP_GPIO 8C5 18C1 19D1
R2140 10K 5% 1/16W MF-LF 402
R2141 10K 5% 1/16W MF-LF 402
R2142 10K 5% 1/16W MF-LF 402
R2143 10K 5% 1/16W MF-LF 402
MCP_GPIO_4 21C3
AUD_I2C_INT_L 21C3 52C7
MEM_EVENT_L 21B3 28A5 29A5 39B8
SMC_IG_THROTTLE_L 21B3 40D4

ARB_DETECT 21B3
R2147 100K 5% 1/16W MF-LF 402

=PP3V3_S3_MCP_GPIO 8D3
R2154 100K 5% 1/16W MF-LF 402
AP_PWR_EN 21C3 31D5 34C7

MCP_VID<0> 21C3 61B8
MCP_VID<1> 21C3 61A8
MCP_VID<2> 21C3 61A8
R2155 22K 5% 1/16W MF-LF 402
R2156 22K 5% 1/16W MF-LF 402
R2157 22K 5% 1/16W MF-LF 402

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MCP HDA & MISC

SYNC_MASTER=T18_MLB SYNC_DATE=06/26/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 21 OF 109	

OMIT

U1400
MCP79-TOPO-B
BGA
(11 OF 11)

GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

61B1 44D7 24D8 8C8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25	+VDD_CORE1	+VTT_CPU1	R32
AC23	+VDD_CORE2	+VTT_CPU2	AC32
U25	+VDD_CORE3	+VTT_CPU3	E40
AH12	+VDD_CORE4	+VTT_CPU4	J36
AG10	+VDD_CORE5	+VTT_CPU5	N32
AG5	+VDD_CORE6	+VTT_CPU6	T32
Y21	+VDD_CORE7	+VTT_CPU7	U32
Y23	+VDD_CORE8	+VTT_CPU8	V32
AA16	+VDD_CORE9	+VTT_CPU9	W32
AA26	+VDD_CORE10	+VTT_CPU10	P31
AA27	+VDD_CORE11	+VTT_CPU11	AF32
AA28	+VDD_CORE12	+VTT_CPU12	AE32
AC16	+VDD_CORE13	+VTT_CPU13	AH32
AC17	+VDD_CORE14	+VTT_CPU14	AJ32
AC18	+VDD_CORE15	+VTT_CPU15	AK31
AC19	+VDD_CORE16	+VTT_CPU16	AK32
AC20	+VDD_CORE17	+VTT_CPU17	AD32
AC21	+VDD_CORE18	+VTT_CPU18	AL31
AA17	+VDD_CORE19	+VTT_CPU19	AB32
AC24	+VDD_CORE20	+VTT_CPU20	B41
AC25	+VDD_CORE21	+VTT_CPU21	B42
AC26	+VDD_CORE22	+VTT_CPU22	C40
AC27	+VDD_CORE23	+VTT_CPU23	C41
AC28	+VDD_CORE24	+VTT_CPU24	C42
AD21	+VDD_CORE25	+VTT_CPU25	D39
AD23	+VDD_CORE26	+VTT_CPU26	D40
W27	+VDD_CORE27	+VTT_CPU27	D41
V25	+VDD_CORE28	+VTT_CPU28	E38
AA18	+VDD_CORE29	+VTT_CPU29	E39
AE19	+VDD_CORE30	+VTT_CPU30	F37
AE21	+VDD_CORE31	+VTT_CPU31	F38
AE23	+VDD_CORE32	+VTT_CPU32	F39
AE25	+VDD_CORE33	+VTT_CPU33	G36
AE26	+VDD_CORE34	+VTT_CPU34	G37
AE27	+VDD_CORE35	+VTT_CPU35	G38
AE28	+VDD_CORE36	+VTT_CPU36	H35
AF10	+VDD_CORE37	+VTT_CPU37	H37
AF11	+VDD_CORE38	+VTT_CPU38	J34
AA19	+VDD_CORE39	+VTT_CPU39	J35
AF2	+VDD_CORE40	+VTT_CPU40	K33
AF21	+VDD_CORE41	+VTT_CPU41	K34
AF23	+VDD_CORE42	+VTT_CPU42	K35
AF25	+VDD_CORE43	+VTT_CPU43	L32
AF3	+VDD_CORE44	+VTT_CPU44	L33
AF4	+VDD_CORE45	+VTT_CPU45	L34
AF7	+VDD_CORE46	+VTT_CPU46	M31
AH23	+VDD_CORE47	+VTT_CPU47	M32
AF9	+VDD_CORE48	+VTT_CPU48	M33
AA20	+VDD_CORE49	+VTT_CPU49	N31
AG11	+VDD_CORE50	+VTT_CPU50	P32
AG12	+VDD_CORE51	+VTT_CPU51	Y32
AG21	+VDD_CORE52	+VTT_CPU52	AA32
AG23	+VDD_CORE53		
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32
AG3	+VDD_CORE55		
AG4	+VDD_CORE56		
AA21	+VDD_CORE57		
AG6	+VDD_CORE58		
AG7	+VDD_CORE59		
AG8	+VDD_CORE60		
AG9	+VDD_CORE61		
AH1	+VDD_CORE62		
AH10	+VDD_CORE63		
AH11	+VDD_CORE64		
W26	+VDD_CORE65		
AH2	+VDD_CORE66		
AA23	+VDD_CORE67		
W28	+VDD_CORE68		
AH25	+VDD_CORE69		
AH21	+VDD_CORE70	+3.3V_DUAL1	G18
AH3	+VDD_CORE71	+3.3V_DUAL2	H19
AH4	+VDD_CORE72	+3.3V_DUAL3	J20
AH5	+VDD_CORE73	+3.3V_DUAL4	K20
AH6	+VDD_CORE74		
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28
W23	+VDD_CORE79		
W25	+VDD_CORE80		
AF12	+VDD_CORE81		
		+VDD_AUXC1	T21
		+VDD_AUXC2	U21
A20	+VBAT	+VDD_AUXC3	V21

=PP1V05_S0_MCP_FSB
1139 mA
BD7 9C2 14A2 14B7 24C8
1182 mA (A01)

+VTT_CPUCLK: 43 mA

=PP3V3_S0_MCP
8C5 21C2 24B8
450 mA (A01)

+3.3V_1 AD10
+3.3V_2 AE8
+3.3V_3 AB10
+3.3V_4 AD9
+3.3V_5 Y10
+3.3V_6 AB11
+3.3V_7 AA8
+3.3V_8 Y9

=PP3V3_S5_MCP
8A3 24B8
16 mA
266 mA (A01)

+3.3V_DUAL1 G18
+3.3V_DUAL2 H19
+3.3V_DUAL3 J20
+3.3V_DUAL4 K20

+3.3V_DUAL_USB1 G26: 250 mA

=PP1V05_S5_MCP_VDD_AUXC
8B3 24D8
105 mA (A01)

+VDD_AUXC1 T21
+VDD_AUXC2 U21
+VDD_AUXC3 V21

26D4 21C8 7C3 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

+VBAT A20

MCP Power & Ground

SYNC_MASTER=T18_MLB
SYNC_DATE=04/04/2008

APPLE INC.

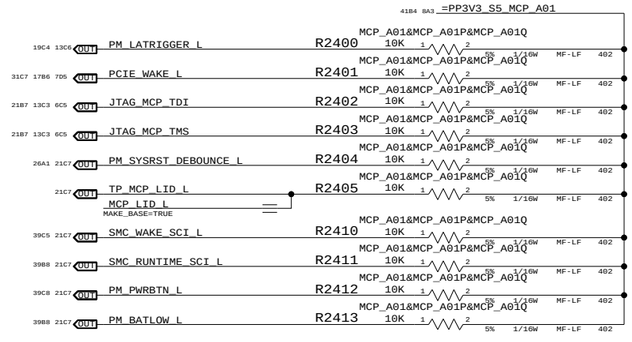
SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE: NONE
SHT 22 OF 109

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.



MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

RADAR 5925345

MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/08/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	24	109

MCP Core Power

NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)

61B1 44D7 22D5 8C8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

(No IG vs. EG data)

C2500 4.7UF 20% 4V X5R 402
C2501 4.7UF 20% 4V X5R 402
C2502 4.7UF 20% 4V X5R 402
C2503 4.7UF 20% 4V X5R 402
C2504 1UF 10% 10V X5R 402-1
C2505 1UF 10% 10V X5R 402-1
C2506 1UF 10% 10V X5R 402-1
C2507 1UF 10% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power

8C7 8A9 =PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)

C2515 4.7UF 20% 4V X5R 402
C2516 1UF 10% 10V X5R 402-1
C2517 1UF 10% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power

8B7 8A9 =PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)

C2520 4.7UF 20% 4V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power

22A3 8B3 =PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)

C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power

18D3 8B1 =PP1V05_ENET_MCP_RMGT
131 mA (A01)

C2528 4.7UF 20% 4V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)

14B7 14A2 9C2 8B7 22G3 =PP1V05_S0_MCP_FSB
1182 mA (A01)

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power

16C7 16C3 8B7 =PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)

C2540 4.7UF 20% 4V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power

NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)

22B3 21C2 8C5 =PP3V3_S0_MCP
450 mA (A01)

C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

22B3 8A3 =PP3V3_S5_MCP
266 mA (A01)

C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

21D8 21D3 8B5 =PP3V3R1V5_S0_MCP_HDA
7 mA (A01)

C2562 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V PLL Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

8C5 =PP3V3_S0_MCP_PLL_UF
19 mA (A01)

L2555 30-OHM-1.7A 0402

PP3V3_S0_MCP_PLL_USB 20C3
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)

C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

24A5 18D7 18D3 8B1 =PP3V3_ENET_MCP_RMGT
83 mA (A01)

C2564 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef

24B6 18D7 18D3 8B1 =PP3V3_ENET_MCP_RMGT

R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402

MCP_MII_VREF OUT 18D3

C2591 0.1UF 20% 10V CERM 402

MCP 1.5V PLL Power

8B7 =PP1V05_S0_MCP_PLL_UF
562 mA (A01)

L2580 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_FSB 14A6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)

C2580 4.7UF 20% 4V X5R 402
C2581 0.1UF 20% 10V CERM 402

L2582 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_PEX 17A6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2582 4.7UF 20% 4V X5R 402
C2583 0.1UF 20% 10V CERM 402

L2584 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_SATA 20B6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)

C2584 4.7UF 20% 4V X5R 402
C2585 0.1UF 20% 10V CERM 402

L2586 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_CORE 16C6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)

C2586 4.7UF 20% 4V X5R 402
C2587 0.1UF 20% 10V CERM 402

L2588 30-OHM-1.7A 0402

PP1V05_S0_MCP_PLL_NV 21C7
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)

C2588 4.7UF 20% 4V X5R 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

MCP 1.5V PLL Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)

8B7 =PP1V05_S0_MCP_AVDD_UF
333 mA (A01)

L2570 30-OHM-5A 0603

PP1V05_S0_MCP_PEX_AVDD 8A8
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)

C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

MCP 1.5V SATA Power

NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

L2575 30-OHM-5A 0603

PP1V05_S0_MCP_SATA_AVDD 8A8
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)

C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

MCP 1.8V PLL Power

8B1 =PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)

L2595 30-OHM-1.7A 0402

PP1V05_ENET_MCP_PLL_MAC 18C6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)

C2595 4.7UF 20% 4V X5R 402
C2596 0.1UF 20% 10V CERM 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	25	109

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

18B6 8A7 =PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)

C2610 2.2UF 20% 6.3V CERM 402-LF

18A6 8B7 =PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)

C2615 4.7UF 20% 4V X5R 402
C2616 0.1UF 20% 10V CERM 402

73B3 18A6 MCP_HDMI_RSET
73B3 18A6 MCP_HDMI_VPROBE

NO STUFF
C2620 0.1UF 20% 10V CERM 402
R2620 1K 1% 1/16W MF-LF 402

73B3 18A3 MCP_IFPAB_RSET
73B3 18A3 MCP_IFPAB_VPROBE

NO STUFF
C2630 0.1UF 20% 10V CERM 402
NO STUFF
R2630 1K 1% 1/16W MF-LF 402

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

8C5 =PP3V3_S0_MCP_VPLL_UF
16 mA (A01)

L2640 30-OHM-1.7A 0402

PP3V3_S0_MCP_VPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
18B6
16 mA (A01)

C2640 4.7UF 20% 6.3V CERM 603
C2641 0.1uF 20% 10V CERM 402

8C5 =PP3V3_S0_MCP_DAC_UF
206 mA (A01)

NO STUFF
L2650 30-OHM-1.7A 0402

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
18C3
206 mA (A01)

NO STUFF
C2650 2.2UF 20% 6.3V CERM 402-LF
R2651 0 5% 1/16W MF-LF 402

HDCP ROM

WF: Open question on which packge option(s) nVidia can support.

8C6 =PP3V3_S0_HDCPROM

C2690 0.1UF 20% 10V CERM 402

NOSTUFF
U2695 AT24C08 SOIC
A0 A1 A2 SDA SCL WP GND
=I2C_HDCPROM_SDA
=I2C_HDCPROM_SCL
HDCPROM_WP

R2690 10K 5% 1/16W MF-LF 402

42C6 IO
42C6 IN

25A8 HDCPROM_WP

NOSTUFF
U2690 AT24C01B SOT23
25A7 HDCPROM_WP
WP SDA SCL GND

SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

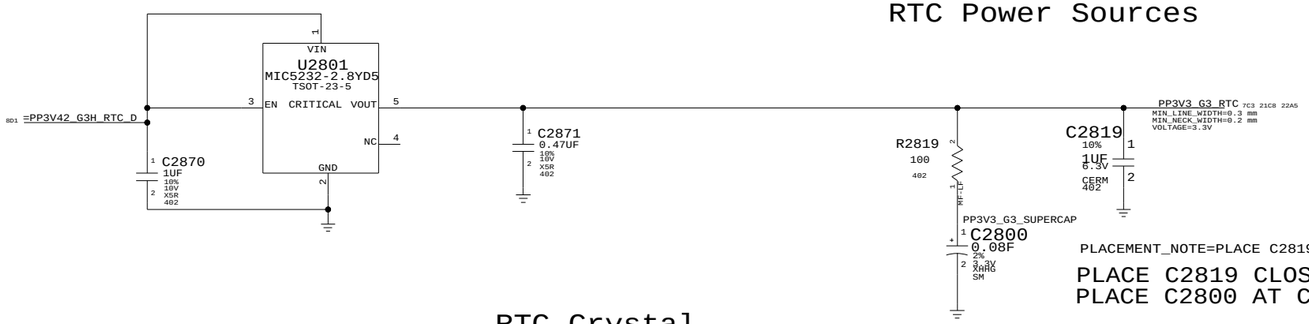
MCP Graphics Support

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 26 OF 109	

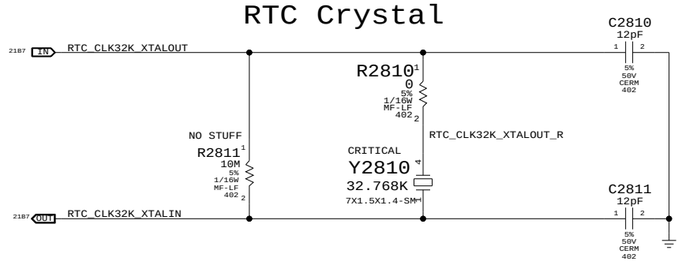
RTC Power Sources



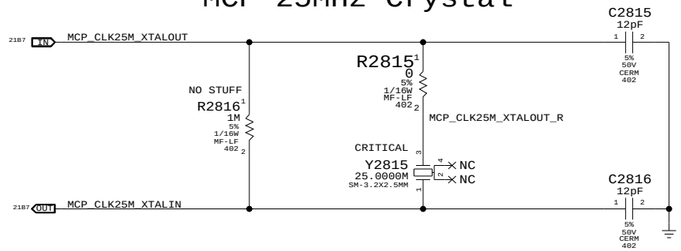
PLACEMENT_NOTE=PLACE C2819 CLOSE TO MCP79

PLACE C2819 CLOSE TO MCP79
PLACE C2800 AT COOLEST SPOT ON MLB

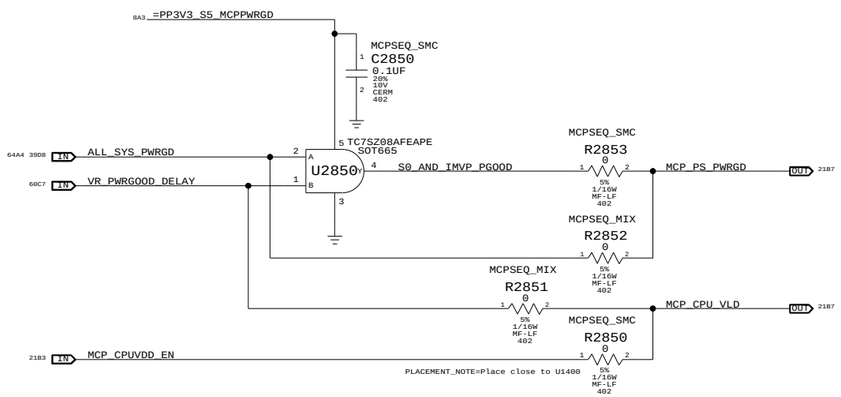
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

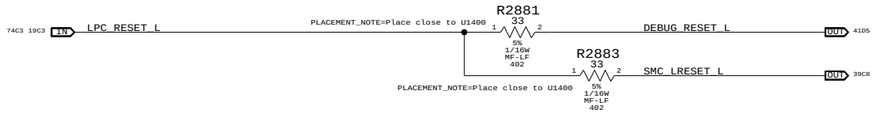
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

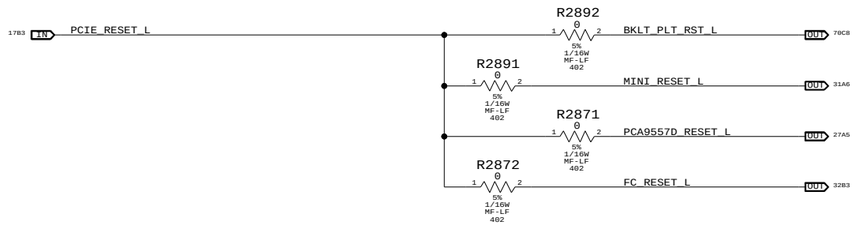
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

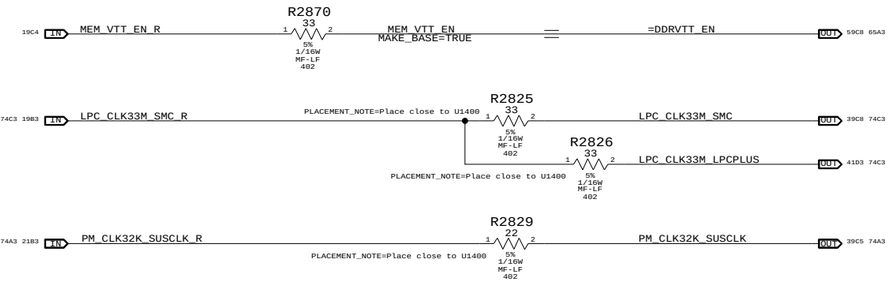
Platform Reset Connections

LPC Reset (Unbuffered)

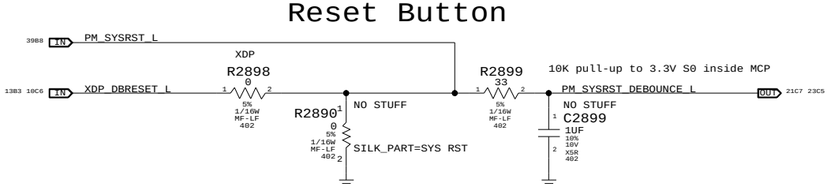


PCIE Reset (Unbuffered)





Reset Button



SYNC FROM T18
CHANGE RESET BUTTOM TO RESET PADS
REMOVE UNUSED PCIE RESET SIGNALS
REMOVE R2824 AND NET PCI_CLK33M_SLOT_A
CHANGE RTC COIN CELL TO LDO & SUPERCAP
ALIAS MEM_VTT_EN TO =DDRVTT_EN
CHANGE Y2810 AND U2850 TO SMALLER PARTS

SB Misc

SYNC_MASTER=RAYMOND SYNC_DATE=04/05/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 28 OF 109	

Page Notes

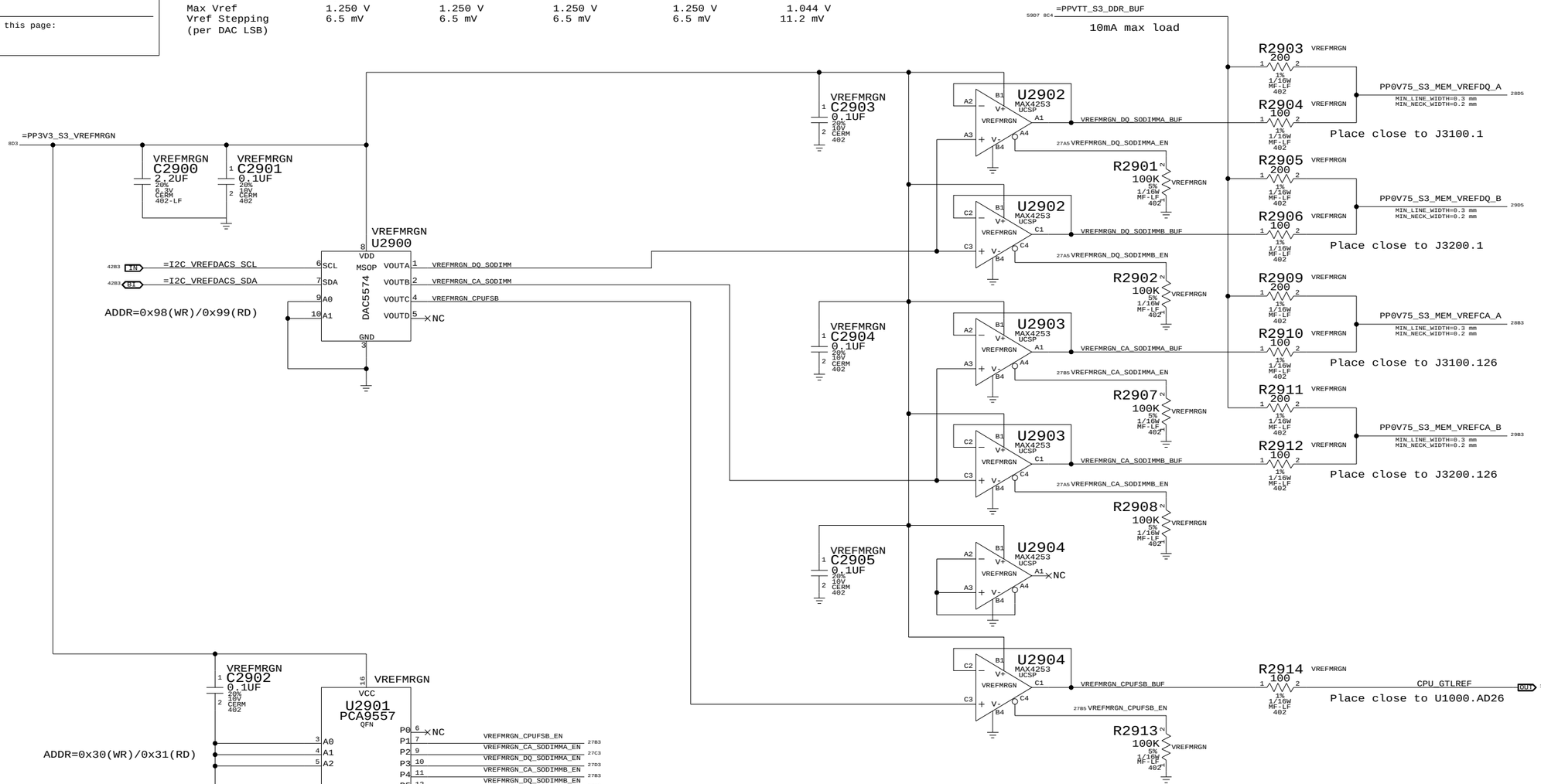
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining

SYNC_MASTER=BEN SYNC_DATE=03/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 29 OF 109	

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PP5PD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

8D3 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 6.3V X5S-CERM 0204-1
C3111 0.1UF 20% 6.3V X5S-CERM 0204-1
C3112 0.1UF 20% 6.3V X5S-CERM 0204-1
C3113 0.1UF 20% 6.3V X5S-CERM 0204-1
C3114 0.1UF 20% 6.3V X5S-CERM 0204-1
C3115 0.1UF 20% 6.3V X5S-CERM 0204-1
C3116 0.1UF 20% 6.3V X5S-CERM 0204-1
C3117 0.1UF 20% 6.3V X5S-CERM 0204-1

27D1 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 2 OF 2)
KEY

72D3 15A5	IN	MEM_A_CKE<0>	73	CKE0	
			75	VDD	
		NC	77	NC	
72D3 15C5	IN	MEM_A_BA<2>	79	BA2	
			81	VDD	
72D3 15C5	IN	MEM_A_A<12>	83	A12/BC*	
72D3 15C5	IN	MEM_A_A<9>	85	A9	
			87	VDD	
72D3 15C5	IN	MEM_A_A<8>	89	A8	
72D3 15B5	IN	MEM_A_A<5>	91	A5	
			93	VDD	
72D3 15B5	IN	MEM_A_A<3>	95	A3	
72D3 15B5	IN	MEM_A_A<1>	97	A1	
			99	VDD	
72D3 15B5	IN	MEM_A_CLK_P<0>	101	CK0	
72D3 15B5	IN	MEM_A_CLK_N<0>	103	CK0*	
			105	VDD	
72D3 15C5	IN	MEM_A_A<10>	107	A10/AP	
72D3 15C5	IN	MEM_A_BA<0>	109	BA0	
			111	VDD	
72D3 15C5	IN	MEM_A_WE_L	113	WE*	
72D3 15C5	IN	MEM_A_CAS_L	115	CAS*	
			117	VDD	
72D3 15C5	IN	MEM_A_A<13>	119	A13	
72D3 15B5	IN	MEM_A_CS_L<1>	121	S1*	
			123	VDD	
			125	TEST	
			127	VSS	
72D3 15C7	BI	MEM_A_DQ<32>	129	DQ32	
72D3 15C7	BI	MEM_A_DQ<33>	131	DQ33	
			133	VSS	
72C3 15D5	BI	MEM_A_DQS_N<4>	135	DQS4*	
72C3 15D5	BI	MEM_A_DQS_P<4>	137	DQS4	
			139	VSS	
72D3 15C7	BI	MEM_A_DQ<34>	141	DQ34	
72D3 15C7	BI	MEM_A_DQ<38>	143	DQ35	
			145	VSS	
72D3 15C7	BI	MEM_A_DQ<44>	147	DQ40	
72D3 15C7	BI	MEM_A_DQ<45>	149	DQ41	
			151	VSS	
72C3 15B7	IN	MEM_A_DM<5>	153	DM5	
			155	VSS	
72D3 15D7	BI	MEM_A_DQ<47>	157	DQ42	
72D3 15D7	BI	MEM_A_DQ<46>	159	DQ43	
			161	VSS	
72D3 15D7	BI	MEM_A_DQ<49>	163	DQ48	
72D3 15D7	BI	MEM_A_DQ<52>	165	DQ49	
			167	VSS	
72C3 15D5	BI	MEM_A_DQS_N<6>	169	DQS6*	
72C3 15D5	BI	MEM_A_DQS_P<6>	171	DQS6	
			173	VSS	
72D3 15D7	BI	MEM_A_DQ<54>	175	DQ50	
72D3 15D7	BI	MEM_A_DQ<51>	177	DQ51	
			179	VSS	
72D3 15D7	BI	MEM_A_DQ<61>	181	DQ56	
72D3 15D7	BI	MEM_A_DQ<60>	183	DQ57	
			185	VSS	
72C3 15B7	IN	MEM_A_DM<7>	187	DM7	
			189	VSS	
72D3 15D7	BI	MEM_A_DQ<58>	191	DQ58	
72D3 15D7	BI	MEM_A_DQ<59>	193	DQ59	
			195	VSS	
		MEM_A_SA<0>	197	SA0	
			199	VDDSPD	
		MEM_A_SA<1>	201	SA1	
			203	VTT	

NC

		MEM_A_CKE<1>	74	CKE1	
			76	VDD	
		MEM_A_A<15>	78	A15	9D2
		MEM_A_A<14>	80	A14	15C5 72D3
			82	VDD	
		MEM_A_A<11>	84	A11	15C5 72D3
		MEM_A_A<7>	86	A7	15C5 72D3
			88	VDD	
		MEM_A_A<6>	90	A6	15B5 72D3
		MEM_A_A<4>	92	A4	15B5 72D3
			94	VDD	
		MEM_A_A<2>	96	A2	15B5 72D3
		MEM_A_A<0>	98	A0	15B5 72D3
			100	VDD	
		MEM_A_CLK_P<1>	102	CK1	15B5 72D3
		MEM_A_CLK_N<1>	104	CK1*	15B5 72D3
			106	VDD	
		MEM_A_BA<1>	108	BA1	15C5 72D3
		MEM_A_RAS_L	110	RAS*	15C5 72D3
			112	VDD	
		MEM_A_CS_L<0>	114	S0*	15B5 72D3
		MEM_A_ODT<0>	116	ODT0	15B5 72D3
			118	VDD	
		MEM_A_ODT<1>	120	ODT1	15B5 72D3
			122	NC	
			124	VDD	
			126	VREFCA	
			128	VSS	
		MEM_A_DQ<37>	130	DQ36	15C7 72D3
		MEM_A_DQ<36>	132	DQ37	15C7 72D3
			134	VSS	
		MEM_A_DM<4>	136	DM4	15B7 72C3
			138	VSS	
		MEM_A_DQ<35>	140	DQ38	15C7 72D3
		MEM_A_DQ<39>	142	DQ39	15C7 72D3
			144	VSS	
		MEM_A_DQ<40>	146	DQ44	15C7 72D3
		MEM_A_DQ<41>	148	DQ45	15C7 72D3
			150	VSS	
		MEM_A_DQS_N<5>	152	DQS5*	15D5 72C3
		MEM_A_DQS_P<5>	154	DQS5	15D5 72C3
			156	VSS	
		MEM_A_DQ<43>	158	DQ46	15C7 72D3
		MEM_A_DQ<42>	160	DQ47	15C7 72D3
			162	VSS	
		MEM_A_DQ<53>	164	DQ52	15D7 72D3
		MEM_A_DQ<48>	166	DQ53	15D7 72D3
			168	VSS	
		MEM_A_DM<6>	170	DM6	15B7 72C3
			172	VSS	
		MEM_A_DQ<55>	174	DQ54	15D7 72D3
		MEM_A_DQ<50>	176	DQ55	15D7 72D3
			178	VSS	
		MEM_A_DQ<57>	180	DQ60	15D7 72D3
		MEM_A_DQ<56>	182	DQ61	15D7 72D3
			184	VSS	
		MEM_A_DQS_N<7>	186	DQS7*	15D5 72C3
		MEM_A_DQS_P<7>	188	DQS7	15D5 72C3
			190	VSS	
		MEM_A_DQ<62>	192	DQ62	15D7 72D3
		MEM_A_DQ<63>	194	DQ63	15D7 72D3
			196	VSS	
		MEM_EVENT_L	198	EVENT*	OUT 21A4 21B3 29A5 39B8
		=I2C_SODIMMA_SDA	200	SDA	BI 42D6
		=I2C_SODIMMA_SCL	202	SCL	IN 42D6
			204	VTT	

NC

8B5 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

C3150 2.2UF 20% 6.3V CERM 402-LF
C3151 2.2UF 20% 6.3V CERM 402-LF

=PP0V75_S0_MEM_VTT_A 8C7

516-0201
SPD ADDR=0xA0(WR)/0xA1(RD)

J3100 F-RT-THB
DDR3-SODIMM-DUAL-M97-3 (SYMBOL 1 OF 2)
CRITICAL
KEY

72D3 15B7	BI	MEM_A_DQ<0>	1	VREFDQ	
			3	VSS	
72D3 15B7	BI	MEM_A_DQ<1>	5	DQ0	
			7	DQ1	
72D3 15A7	IN	MEM_A_DM<0>	9	VSS	
			11	DM0	
			13	VSS	
72D3 15B7	BI	MEM_A_DQ<6>	15	DQ2	
72D3 15B7	BI	MEM_A_DQ<7>	17	DQ3	
			19	VSS	
72D3 15B7	BI	MEM_A_DQ<8>	21	DQ8	
72D3 15B7	BI	MEM_A_DQ<12>	23	DQ9	
			25	VSS	
72C3 15D5	BI	MEM_A_DQS_N<1>	27	DQS1*	
72C3 15D5	BI	MEM_A_DQS_P<1>	29	DQS1	
			31	VSS	
72D3 15B7	BI	MEM_A_DQ<10>	33	DQ10	
72D3 15B7	BI	MEM_A_DQ<15>	35	DQ11	
			37	VSS	
72D3 15C7	BI	MEM_A_DQ<25>	39	DQ16	
72D3 15C7	BI	MEM_A_DQ<24>	41	DQ17	
			43	VSS	
72C3 15D5	BI	MEM_A_DQS_N<3>	45	DQS2*	
72C3 15D5	BI	MEM_A_DQS_P<3>	47	DQS2	
			49	VSS	
72D3 15C7	BI	MEM_A_DQ<26>	51	DQ18	
72D3 15C7	BI	MEM_A_DQ<30>	53	DQ19	
			55	VSS	
72D3 15C7	BI	MEM_A_DQ<20>	57	DQ24	
72D3 15C7	BI	MEM_A_DQ<21>	59	DQ25	
			61	VSS	
72C3 15B7	IN	MEM_A_DM<2>	63	DM3	
			65	VSS	
72D3 15C7	BI	MEM_A_DQ<23>	67	DQ26	
72D3 15B7	BI	MEM_A_DQ<16>	69	DQ27	
			71	VSS	

			2	VSS	
		MEM_A_DQ<4>	4	DQ4	BI 15B7 72D3
		MEM_A_DQ<5>	6	DQ5	BI 15B7 72D3
			8	VSS	
		MEM_A_DQS_N<0>	10	DQS0*	BI 15D5 72C3
		MEM_A_DQS_P<0>	12	DQS0	BI 15D5 72C3
			14	VSS	
		MEM_A_DQ<3>	16	DQ6	BI 15B7 72D3
		MEM_A_DQ<2>	18	DQ7	BI 15B7 72D3
			20	VSS	
		MEM_A_DQ<9>	22	DQ12	BI 15B7 72D3
		MEM_A_DQ<13>	24	DQ13	BI 15B7 72D3
			26	VSS	
		MEM_A_DM<1>	28	DM1	IN 15A7 72C3
		MEM_RESET_L	30	RESET*	IN 29C2 30C3
			32	VSS	
		MEM_A_DQ<11>	34	DQ14	BI 15B7 72D3
		MEM_A_DQ<14>	36	DQ15	BI 15B7 72D3
			38	VSS	
		MEM_A_DQ<29>	40	DQ20	BI 15C7 72D3
		MEM_A_DQ<28>	42	DQ21	BI 15C7 72D3
			44	VSS	
		MEM_A_DM<3>	46	DM2	IN 15B7 72C3
			48	VSS	
		MEM_A_DQ<27>	50	DQ22	BI 15C7 72D3
		MEM_A_DQ<31>	52	DQ23	BI 15C7 72D3
			54	VSS	
		MEM_A_DQ<18>	56	DQ28	BI 15B7 72D3
		MEM_A_DQ<17>	58	DQ29	BI 15B7 72D3
			60	VSS	
		MEM_A_DQS_N<2>	62	DQS3*	BI 15D5 72C3
		MEM_A_DQS_P<2>	64	DQS3	BI 15D5 72C3
			66	VSS	
		MEM_A_DQ<19>	68	DQ30	BI 15B7 72D3
		MEM_A_DQ<22>	70	DQ31	BI 15C7 72D3
			72	VSS	

516-0201

PP0V75_S3_MEM_VREFCA_A 27C1

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BEN SYNC_DATE=06/30/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 31 OF 109	

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

8D3 =PP1V5_S3_MEM_B

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3210 0.1UF 20% 6.3V X6S-CERM 0204-1
C3211 0.1UF 20% 6.3V X6S-CERM 0204-1
C3212 0.1UF 20% 6.3V X6S-CERM 0204-1
C3213 0.1UF 20% 6.3V X6S-CERM 0204-1
C3214 0.1UF 20% 6.3V X6S-CERM 0204-1
C3215 0.1UF 20% 6.3V X6S-CERM 0204-1
C3216 0.1UF 20% 6.3V X6S-CERM 0204-1
C3217 0.1UF 20% 6.3V X6S-CERM 0204-1

27C1 PP0V75_S3_MEM_VREFDQ_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 F-RT-BGA3 DDR3-SODIMM (2 OF 2)

72B3 15A1 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 15A1 72B3
		75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 9D2
72B3 15C1 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 15C1 72B3
		81	VDD	VDD	82		
72B3 15C1 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 15C1 72B3
72B3 15C1 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 15C1 72B3
		87	VDD	VDD	88		
72B3 15C1 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 15B1 72B3
72B3 15B1 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 15B1 72B3
		93	VDD	VDD	94		
72B3 15B1 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 15B1 72B3
72B3 15B1 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 15B1 72B3
		99	VDD	VDD	100		
72C3 15B1 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 15B1 72C3
72C3 15B1 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 15B1 72C3
		105	VDD	VDD	106		
72B3 15C1 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 15C1 72B3
72B3 15C1 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 15C1 72B3
		111	VDD	VDD	112		
72B3 15C1 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 15B1 72B3
72B3 15C1 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 15B1 72B3
		117	VDD	VDD	118		
72B3 15C1 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 15B1 72B3
72B3 15B1 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
72B3 15C3 BI	MEM_B_DQ<37>	129	DQ32	DQ36	130	MEM_B_DQ<36>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<32>	131	DQ33	DQ37	132	MEM_B_DQ<33>	BI 15C3 72B3
		133	VSS	VSS	134		
72A3 15D1 BI	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	IN 15B3 72B3
72A3 15D1 BI	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<38>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<35>	141	DQ34	DQ39	142	MEM_B_DQ<34>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<39>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<40>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<45>	147	DQ40	DQ45	148	MEM_B_DQ<44>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	BI 15D1 72A3
72B3 15B3 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	BI 15D1 72A3
		155	VSS	VSS	156		
72B3 15D3 BI	MEM_B_DQ<46>	157	DQ42	DQ46	158	MEM_B_DQ<42>	BI 15C3 72B3
72B3 15D3 BI	MEM_B_DQ<47>	159	DQ43	DQ47	160	MEM_B_DQ<43>	BI 15C3 72B3
		161	VSS	VSS	162		
72B3 15D3 BI	MEM_B_DQ<53>	163	DQ48	DQ52	164	MEM_B_DQ<52>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<48>	BI 15D3 72B3
		167	VSS	VSS	168		
72A3 15D1 BI	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 15B3 72B3
72A3 15D1 BI	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<51>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<55>	175	DQ50	DQ55	176	MEM_B_DQ<50>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<54>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<63>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<59>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<58>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	BI 15D1 72A3
72B3 15B3 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	BI 15D1 72A3
		189	VSS	VSS	190		
72B3 15D3 BI	MEM_B_DQ<61>	191	DQ58	DQ62	192	MEM_B_DQ<62>	BI 15D3 72B3
72B3 15D3 BI	MEM_B_DQ<60>	193	DQ59	DQ63	194	MEM_B_DQ<57>	BI 15D3 72B3
		195	VSS	VSS	196		
MEM_B_SA<0>		197	SA0	EVENT*	198	MEM_EVENT_L	OUT 21A4 21B3 28A5 39B8
8B5 =PPSPD_S0_MEM_B		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	BI 42D6
MEM_B_SA<1>		201	SA1	SCL	202	=I2C_SODIMMB_SCL	IN 42D6
		203	VTT	VTT	204	=PP0V75_S3_MEM_VTT_B	8C7
		MTG PINS					
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

J3200 F-RT-BGA3 DDR3-SODIMM (1 OF 2) CRITICAL

		1	VREFDQ	VSS	2		
72B3 15B3 BI	MEM_B_DQ<1>	3	VSS	DQ4	4	MEM_B_DQ<4>	BI 15B3 72B3
72B3 15B3 BI	MEM_B_DQ<0>	5	DQ0	DQ5	6	MEM_B_DQ<5>	BI 15B3 72B3
		7	DQ1	VSS	8		
72B3 15A3 IN	MEM_B_DM<0>	9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 15D1 72A3
		11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 15D1 72A3
		13	VSS	VSS	14		
72B3 15B3 BI	MEM_B_DQ<3>	15	DQ2	DQ6	16	MEM_B_DQ<7>	BI 15B3 72B3
72B3 15B3 BI	MEM_B_DQ<6>	17	DQ3	DQ7	18	MEM_B_DQ<2>	BI 15B3 72B3
		19	VSS	VSS	20		
72B3 15B3 BI	MEM_B_DQ<13>	21	DQ8	DQ12	22	MEM_B_DQ<12>	BI 15B3 72B3
72B3 15B3 BI	MEM_B_DQ<14>	23	DQ9	DQ13	24	MEM_B_DQ<9>	BI 15B3 72B3
		25	VSS	VSS	26		
72A3 15D1 BI	MEM_B_DQS_N<1>	27	DQS1*	DM1	28	MEM_B_DM<1>	IN 15A3 72B3
72A3 15D1 BI	MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 28C2 30C3
		31	VSS	VSS	32		
72B3 15B3 BI	MEM_B_DQ<15>	33	DQ10	DQ14	34	MEM_B_DQ<8>	BI 15B3 72B3
72B3 15B3 BI	MEM_B_DQ<10>	35	DQ11	DQ15	36	MEM_B_DQ<11>	BI 15B3 72B3
		37	VSS	VSS	38		
72B3 15C3 BI	MEM_B_DQ<20>	39	DQ16	DQ20	40	MEM_B_DQ<16>	BI 15B3 72B3
72B3 15B3 BI	MEM_B_DQ<17>	41	DQ17	DQ21	42	MEM_B_DQ<21>	BI 15C3 72B3
		43	VSS	VSS	44		
72A3 15D1 BI	MEM_B_DQS_N<2>	45	DQS2*	DM2	46	MEM_B_DM<2>	IN 15B3 72B3
72A3 15D1 BI	MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<18>	BI 15B3 72B3
72B3 15C3 BI	MEM_B_DQ<22>	51	DQ18	DQ23	52	MEM_B_DQ<23>	BI 15C3 72B3
72B3 15B3 BI	MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<29>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<24>	57	DQ24	DQ29	58	MEM_B_DQ<25>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<28>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<3>	BI 15D1 72A3
72B3 15B3 IN	MEM_B_DM<3>	63	DM3	DQS3	64	MEM_B_DQS_P<3>	BI 15D1 72A3
		65	VSS	VSS	66		
72B3 15C3 BI	MEM_B_DQ<26>	67	DQ26	DQ30	68	MEM_B_DQ<30>	BI 15C3 72B3
72B3 15C3 BI	MEM_B_DQ<31>	69	DQ27	DQ31	70	MEM_B_DQ<27>	BI 15C3 72B3
		71	VSS	VSS	72		

KEY

516S0706

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFCA_B 27C1

R3240 10K 5% 1/16W MF-LF 402
R3241 10K 5% 1/16W MF-LF 402

C3240 2.2UF 20% 6.3V CERM 402-LF
C3250 2.2UF 20% 6.3V CERM 402-LF
C3251 2.2UF 20% 6.3V CERM 402-LF

516S0706
SPD ADDR=0xA2(WR)/0xA3(RD)

DDR3 GROUND RETURN CAPS (MCP SIDE)

8B7 =PP1V5_S0_MEM_MCP

C3222 0.1UF 20% 6.3V X6S-CERM 0204-1
C3223 0.1UF 20% 6.3V X6S-CERM 0204-1
C3224 0.1UF 20% 6.3V X6S-CERM 0204-1
C3225 0.1UF 20% 6.3V X6S-CERM 0204-1
C3226 0.1UF 20% 6.3V X6S-CERM 0204-1
C3227 0.1UF 20% 6.3V X6S-CERM 0204-1
C3228 0.1UF 20% 6.3V X6S-CERM 0204-1
C3229 0.1UF 20% 6.3V X6S-CERM 0204-1

"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

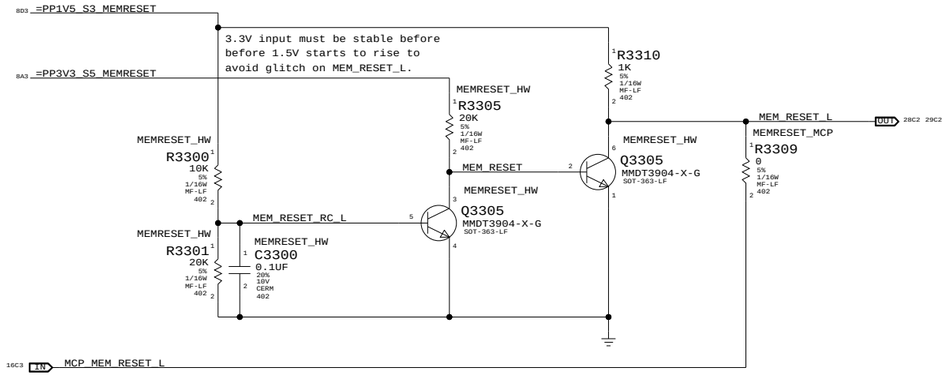
SYNC_MASTER=BEN SYNC_DATE=05/09/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 32 OF 109	

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support		
SYNC_MASTER=T18_MLB	SYNC_DATE=04/04/2008	

APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7918	REV.: C
	SCALE: NONE	SHT: 33	OF: 109

AIRPORT

PCIE_MINI_PRSNT_L
Q3401 SSM6N15FEAPE SOT563
AP_PWR_EN
MINI_CLKREQ_L
Q3401 SSM6N15FEAPE SOT563

CRITICAL
518S0610
J3401
20347-325E-12
F-RT-SM

PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_P
PCIE_MINI_R2D_N
PCIE_CLK100M_MINI_CONN_P
PCIE_CLK100M_MINI_CONN_N
MINI_CLKREQ_O_L
PCIE_WAKE_L
NC
NC

PLACEMENT_NOTE=Place close to J3401.
C3431 0.1uF 10% 16V X5R 402
PCIE_MINI_R2D_C_P
PCIE_MINI_R2D_C_N
C3430 0.1uF 10% 16V X5R 402
PLACEMENT_NOTE=Place close to J3401.

CRITICAL
L3401 90-OHM-100MA DLP11S
PCIE_CLK100M_MINI_P
PCIE_CLK100M_MINI_N
PLACEMENT_NOTE=Place close to J3401.

1000 mA peak
750 mA nominal max
PP5V_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V
L3404 FERR-120-OHM-1.5A 0402-LF
C3422 0.1uF 20% 10V CERM 402
C3421 0.1uF 20% 10V CERM 402
C3420 10UF 20% 10V X5R 805
PLACEMENT_NOTE=Place close to J3401.
PP5V_WLAN_F
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

5V S3 WLAN FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

Q3450 FDC606P_G SOT-6
PLACEMENT_NOTE=Place close to Q3450.
C3450 0.1UF 10% 16V X5R 402
C3451 0.033UF 10% 16V X5R 402
R3450 100K 5% 1/16W MF-LF 402
R3451 10K 5% 1/16W MF-LF 402
P5VWLAN_SS
PM_WLAN_EN_L
=PP5V_S3_WLAN
MIN_LINE_WIDTH=1 mm
MIN_NECK_WIDTH=0.5 mm
VOLTAGE=5V

ALS CAMERA

PP5V_S3_BTCAMERA_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
I2C_ALS_SDA
I2C_ALS_SCL
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
CONN_USB2_BT_P
CONN_USB2_BT_N

275 mA peak
206 mA nominal max
L3405 FERR-120-OHM-1.5A 0402-LF
C3452 0.1uF 20% 10V CERM 402
=PP5V_S3_BTCAMERA
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

CRITICAL
L3402 90-OHM DLP0NS
USB_CAMERA_P
USB_CAMERA_N
PLACEMENT_NOTE=Place close to J3401.

BLUETOOTH

CRITICAL
L3403 90-OHM DLP0NS
USB_BT_P
USB_BT_N
PLACEMENT_NOTE=Place close to J3401.

=PP3V3_S3_WLAN
PP5V_WLAN_F
U3402 74LVC1G17DRL SOT-553
TC7SZ08AFEAPE SOT665
U3401
MINI_RESET_CONN_L
WLAN_SMIT_BUF
WLAN_SMIT_RC
MINI_RESET_L
R3453 33K 5% 1/16W MF-LF 402
R3454 62K 5% 1/16W MF-LF 402
C3453 1UF 10% 6.3V CERM 402
NC

Right Clutch Connector
SYNC_MASTER=YITE
SYNC_DATE=04/22/2008

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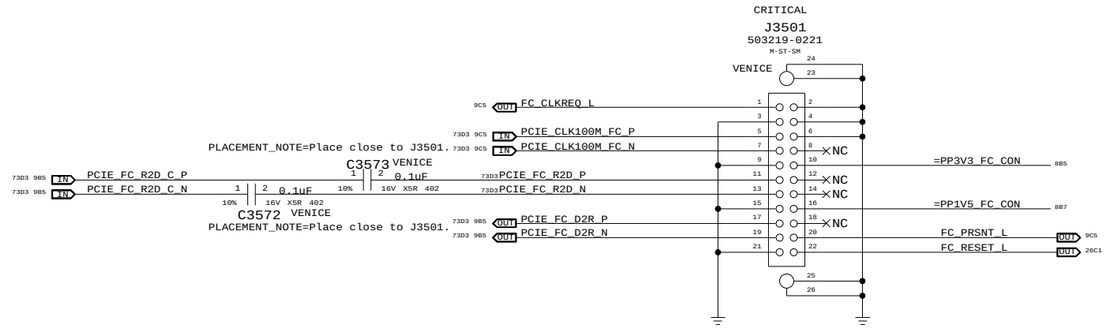
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 34 OF 109	



Venice Connector

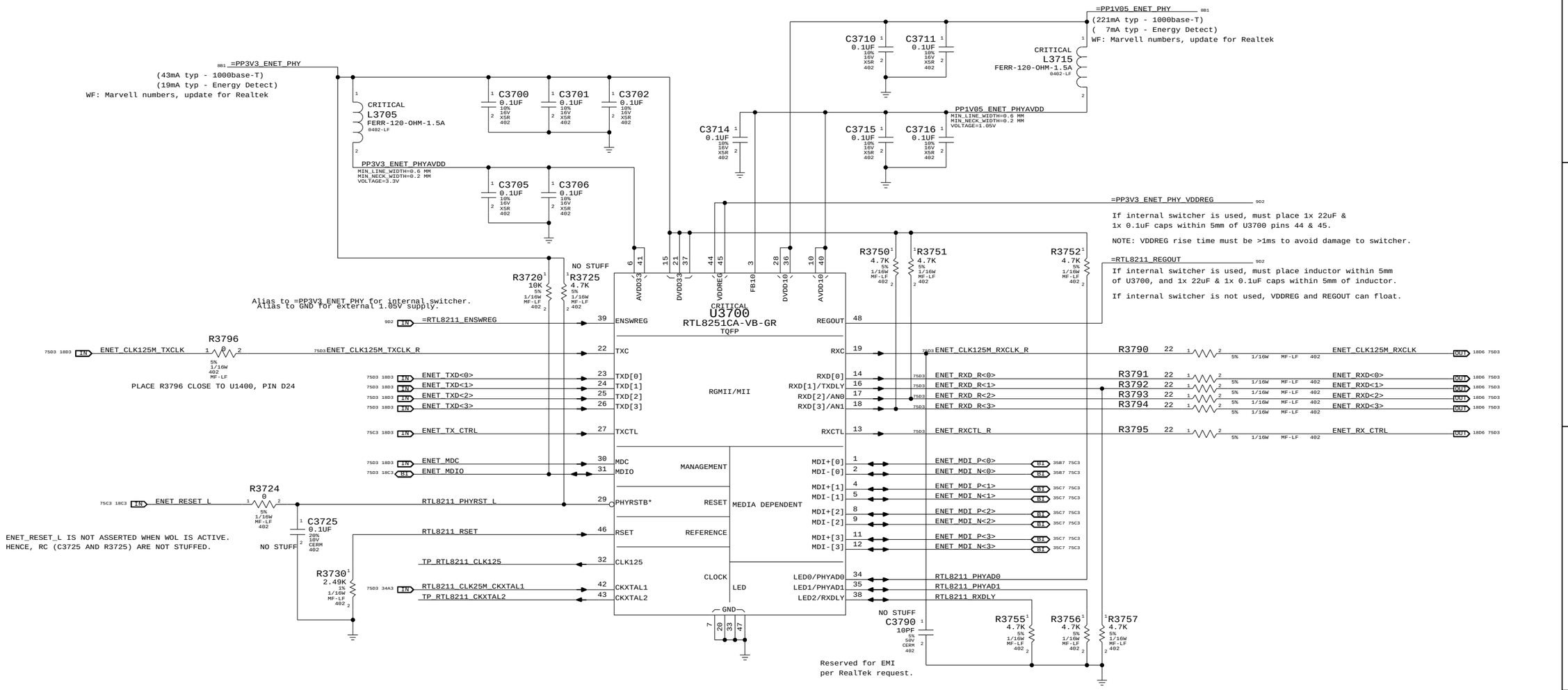
VENICE CONNECTOR

SYNC_MASTER=YITE SYNC_DATE=03/13/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	35	109



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA SYNC_DATE=05/23/2008

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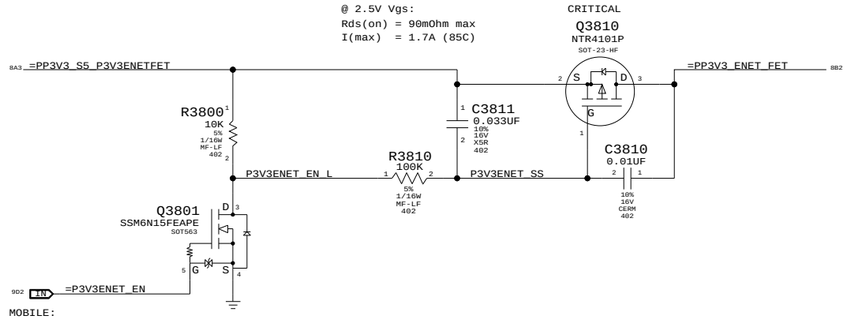
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 37 OF 109	

3.3V ENET FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL



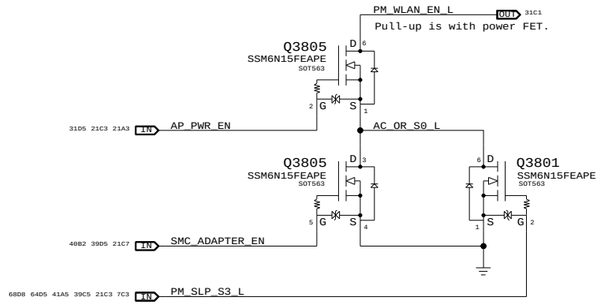
MOBILE:

Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

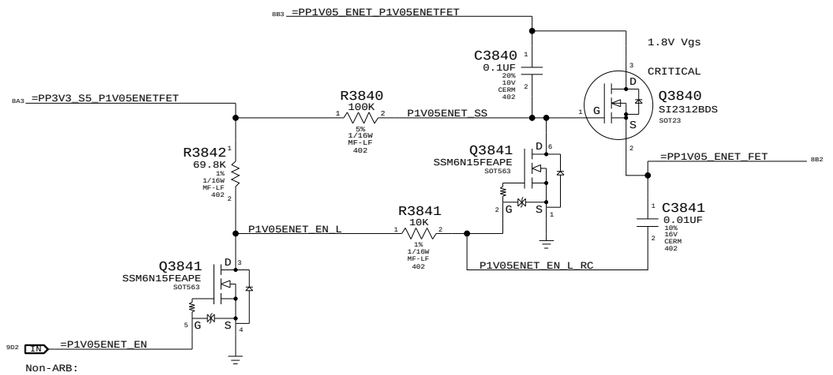
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET



Non-ARB:

Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

Ethernet & AirPort Support

SYNC_MASTER=SUMA SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 38 OF 109	

- COPY THIS PAGE FROM K36 CSA.39

PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902

ENET_CONN_CTAP

C3900 0.1UF 10% 16V X5R 402
C3901 0.1UF 10% 16V X5R 402
C3902 0.1UF 10% 16V X5R 402
C3903 0.1UF 10% 16V X5R 402

CRITICAL
T3901
SM
TLA-6T213HF
TX
RX

CRITICAL
T3902
SM
TLA-6T213HF
TX
RX

ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<3>
ENET_MDI_N<3>
ENET_MDI_N<2>
ENET_MDI_P<2>
ENET_MDI_N<0>
ENET_MDI_P<0>

R3903 75 1% 1/16W MF-LF 402
R3902 75 1% 1/16W MF-LF 402
R3901 75 1% 1/16W MF-LF 402
R3900 75 1% 1/16W MF-LF 402

ENET_CENTER_TAP<1>
ENET_CENTER_TAP<3>
ENET_CENTER_TAP<2>
ENET_CENTER_TAP<0>

ENET_MDI_TRAN_P<1>
ENET_MDI_TRAN_N<1>
ENET_MDI_TRAN_P<3>
ENET_MDI_TRAN_N<3>
ENET_MDI_TRAN_N<2>
ENET_MDI_TRAN_P<2>
ENET_MDI_TRAN_N<0>
ENET_MDI_TRAN_P<0>

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM

CRITICAL
C3910 1000PF 10% 2KV CERM 1206

ETHERNET CONNECTOR

CRITICAL
J3900
RJ45-M97-3
F-RT-TH
514-0636

ETHERNET CONNECTOR

SYNC_MASTER=SUMA SYNC_DATE=04/04/2008

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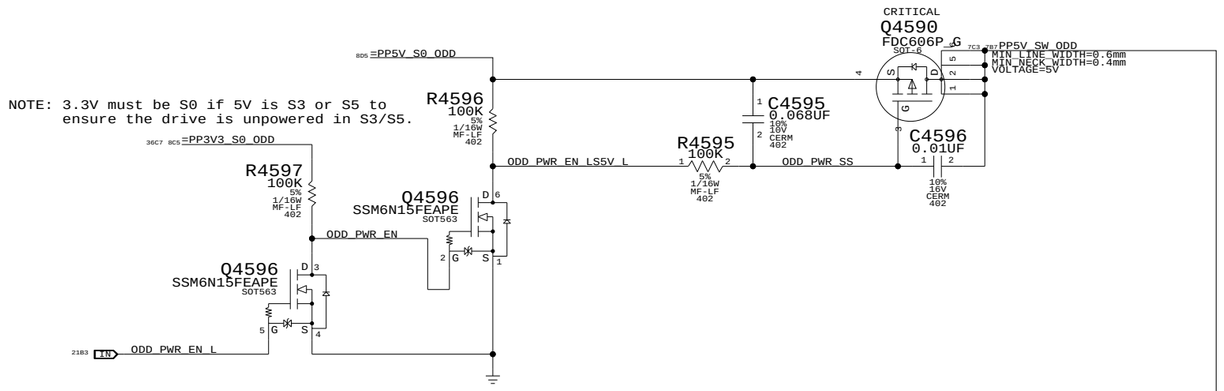
APPLE INC.

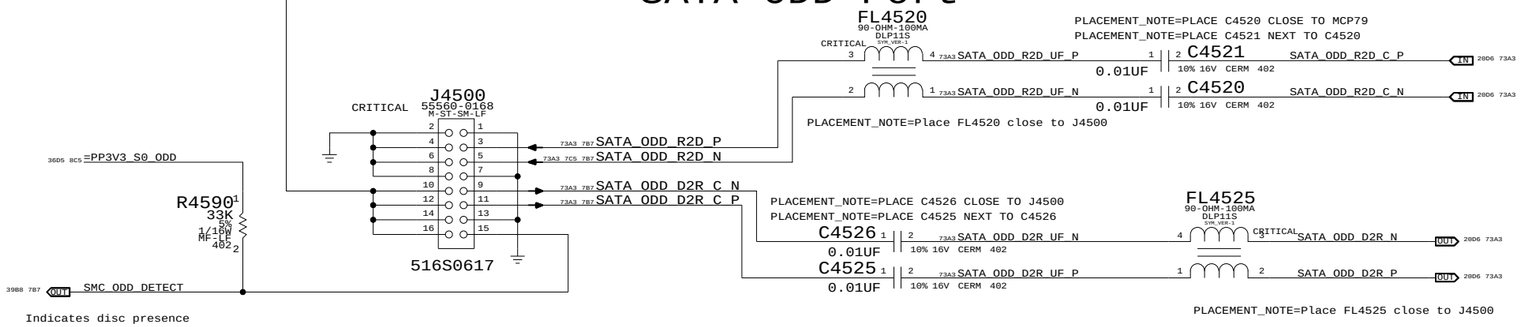
SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	39	109

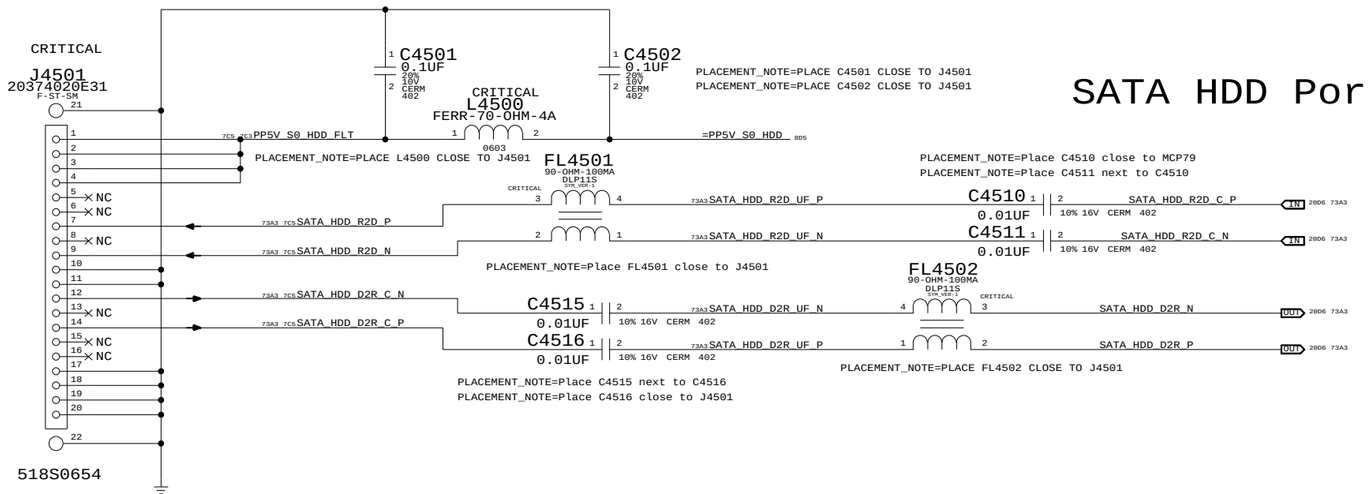
ODD Power Control



SATA ODD Port



SATA HDD Port



SATA Connectors

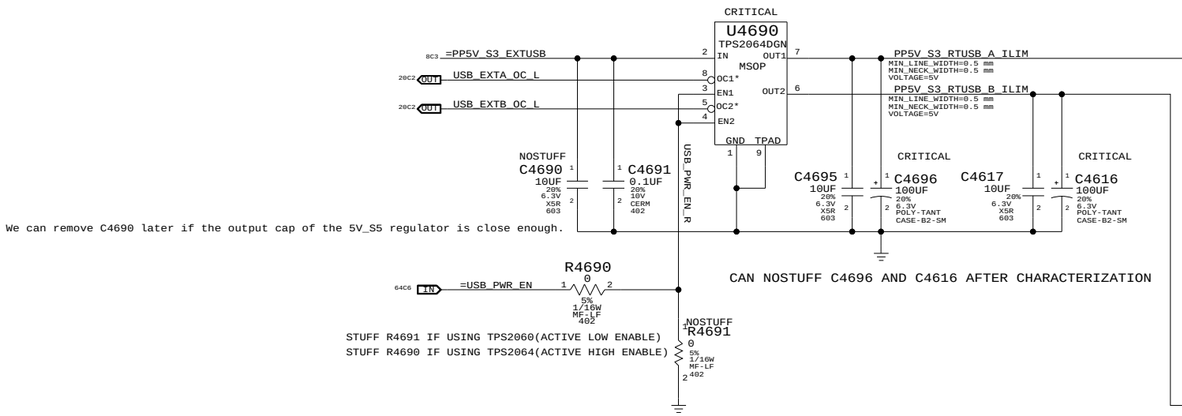
SYNC_MASTER=CHANGZHANG SYNC_DATE=04/14/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

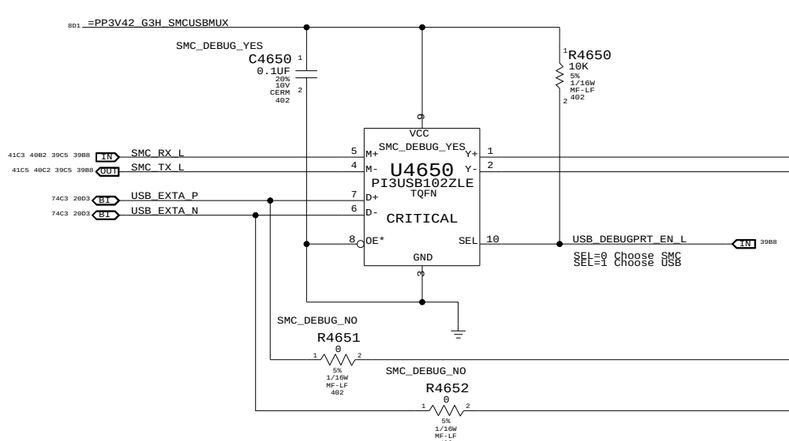
SCALE: NONE SHT 45 OF 109

Port Power Switch

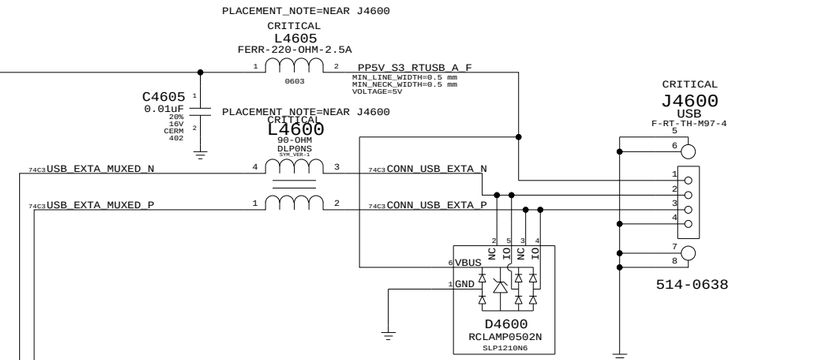


We can remove C4690 later if the output cap of the 5V_S5 regulator is close enough.

USB/SMC Debug Mux



USB PORT A (FRONT PORT)



PLACEMENT_NOTE=NEAR J4610

CRITICAL

L4615

FERR-220-OHM-2.5A

0603

PP5V_S3_RTUSB_B_F

MIN_LINE_WIDTH=0.5 mm

MIN_NECK_WIDTH=0.5 mm

VOLTAGE=5V

C4615

0.01uF

20%

16V

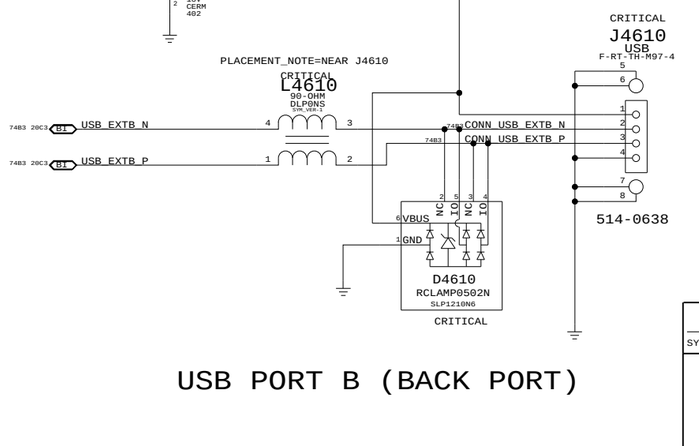
CERM

402

We can add protection to 5V if we want, but leaving NC for now

Place L4600 and L4605 at connector pin

USB PORT B (BACK PORT)



External USB Connectors			
SYNC_MASTER=YUAN.MA		SYNC_DATE=01/18/2008	
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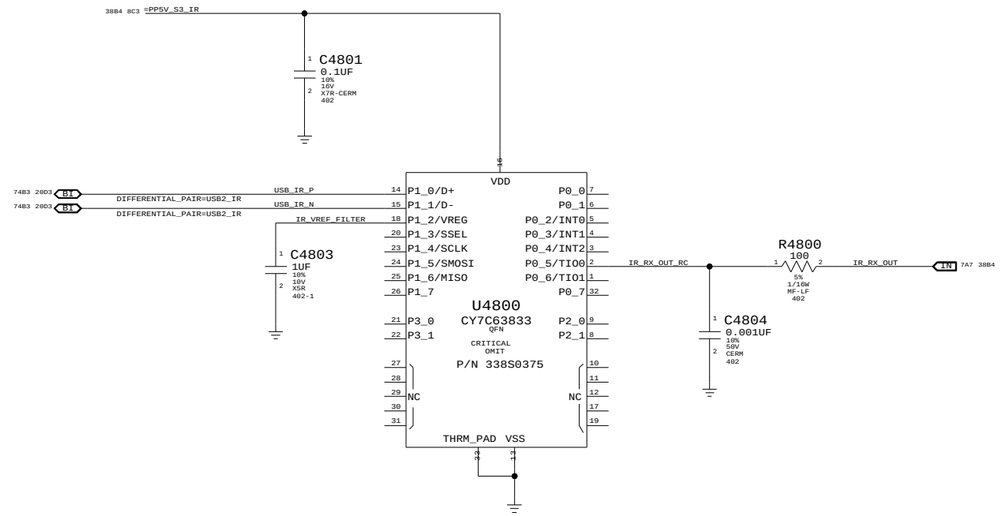
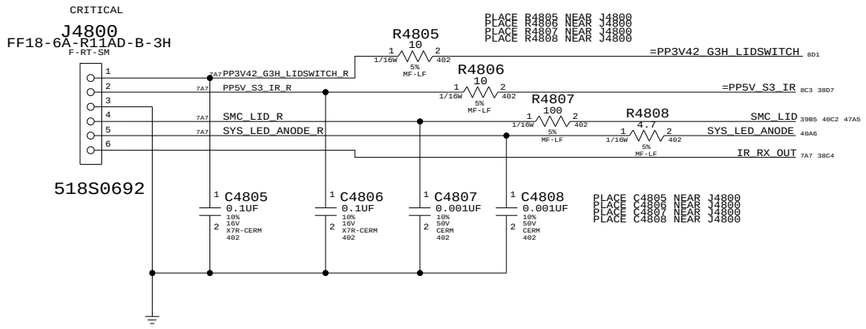
APPLE INC.	SIZE D	DRAWING NUMBER 051-7918	REV. C
	SCALE NONE	SHT 46 OF 109	



CYPRESS 'ENCORE II' USB CONTROLLER



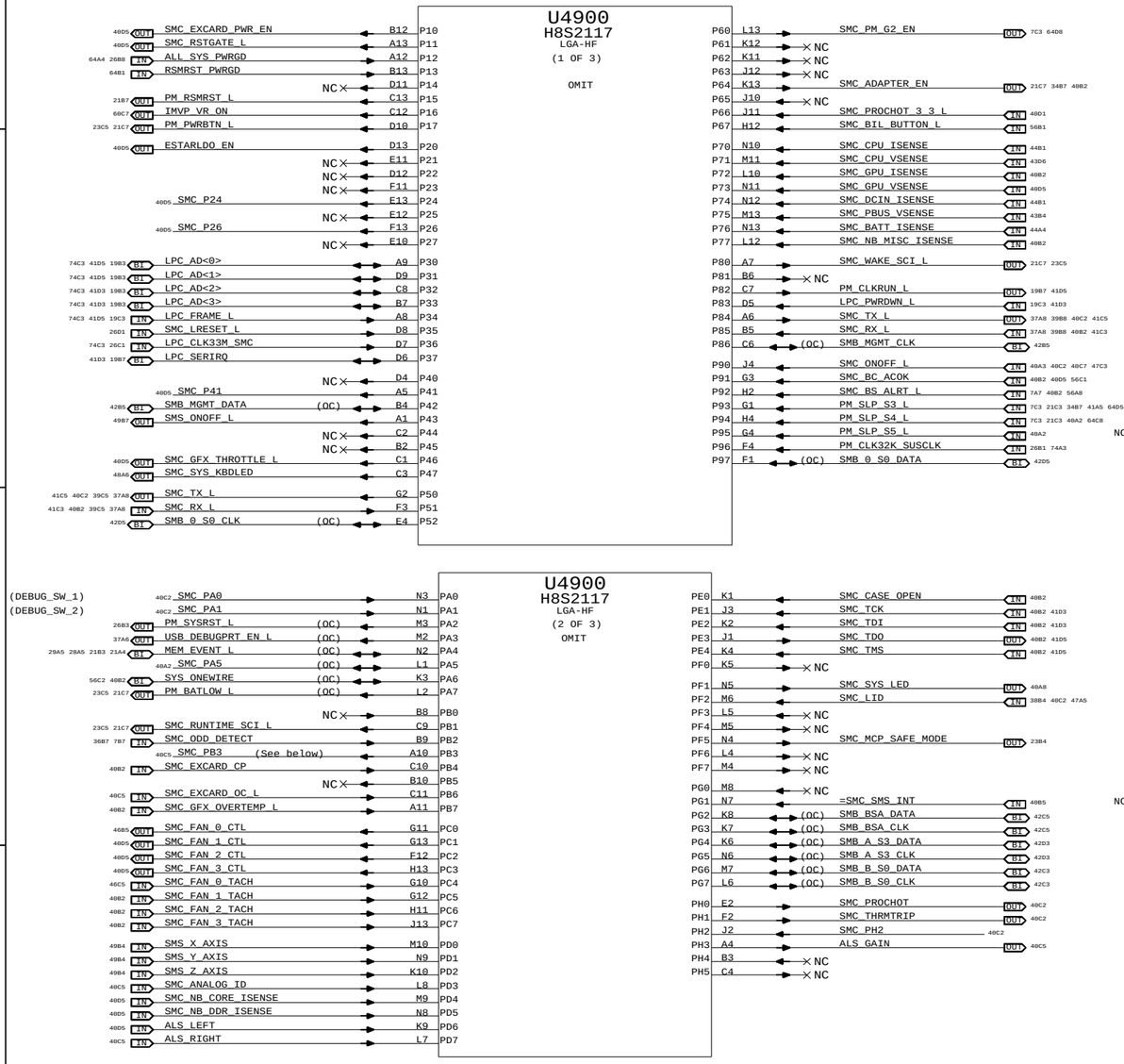
Front Flex Support

SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

APPLE INC.

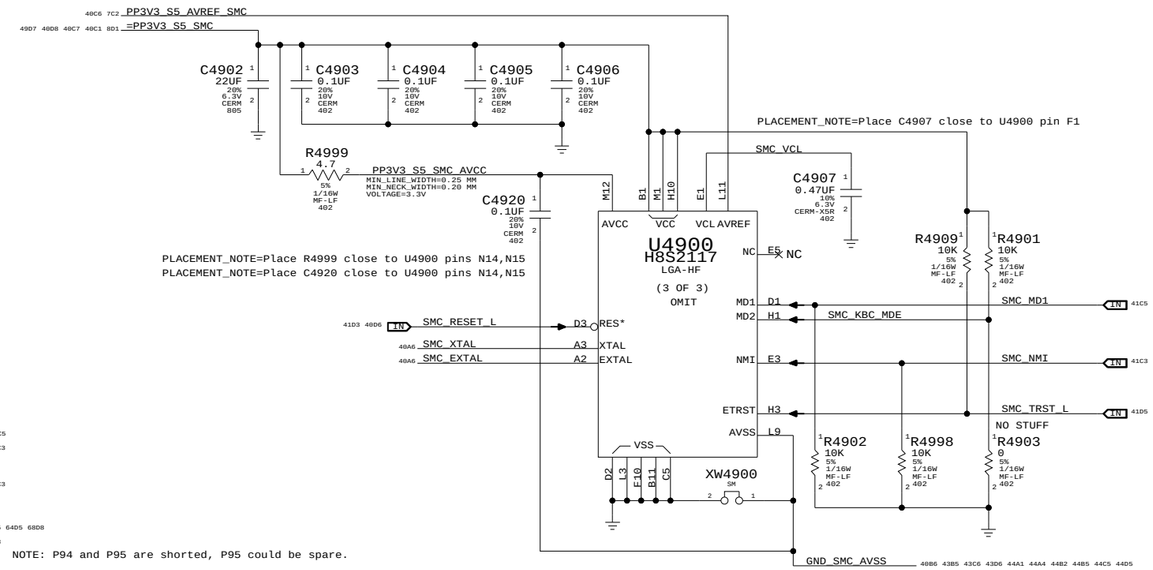
SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	48	109

NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SMC			
SYNC_MASTER=T18_MLB		SYNC_DATE=06/26/2008	
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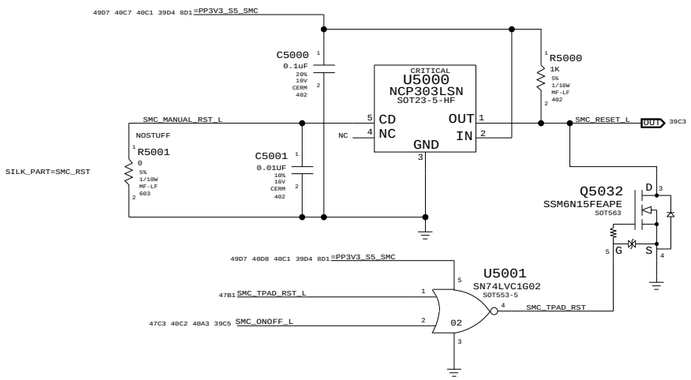
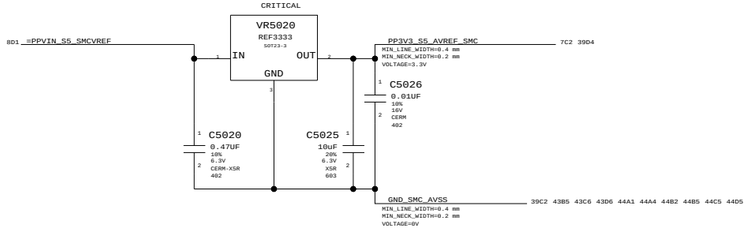
APPLE INC.	SIZE D	DRAWING NUMBER 051-7918	REV. C
	SCALE NONE	SHT 49 OF 109	

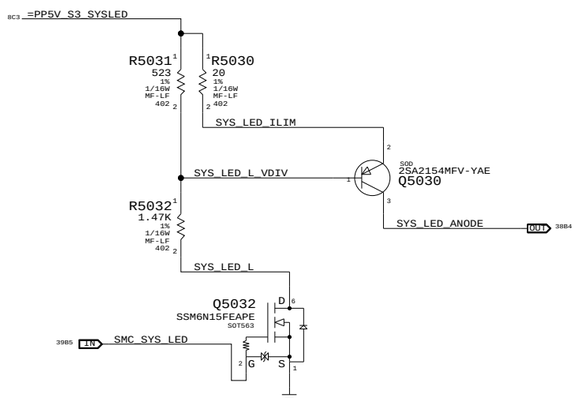
SMC Reset "Button" / Brownout Detect

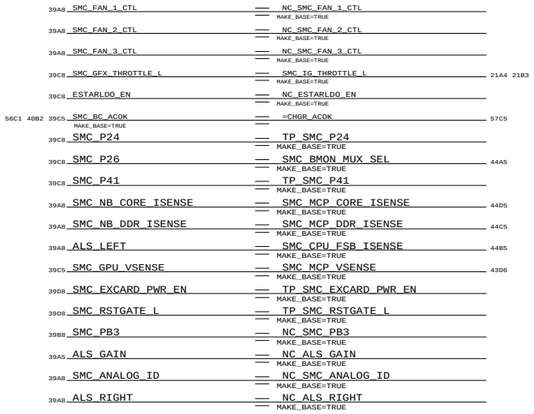


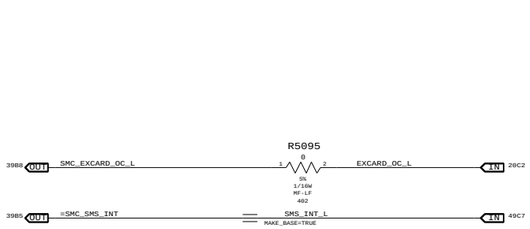
SMC AVREF Supply



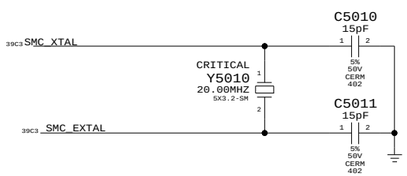
System (Sleep) LED Circuit



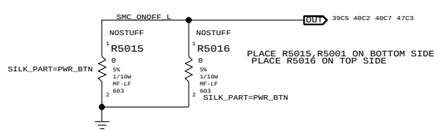




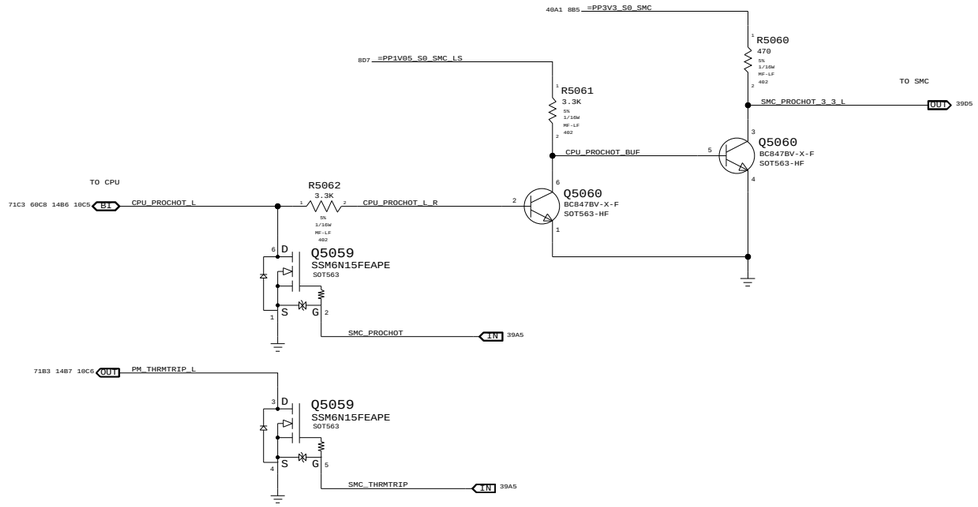
SMC Crystal Circuit

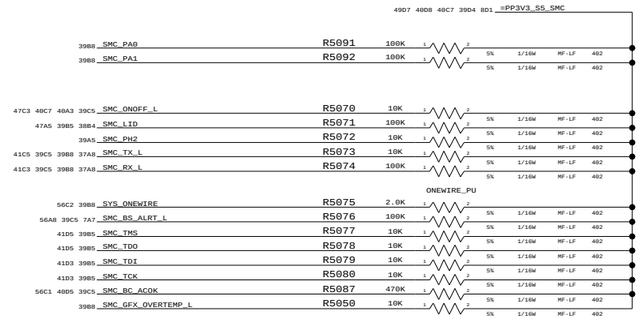


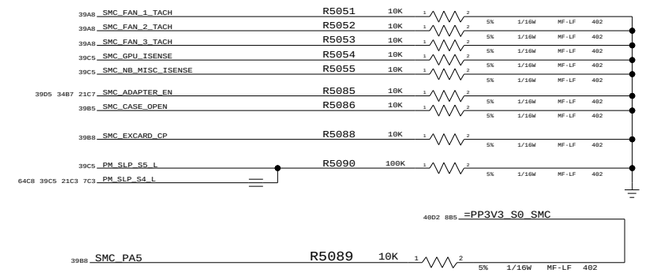
Debug Power "Button"



SMC FSB to 3.3V Level Shifting







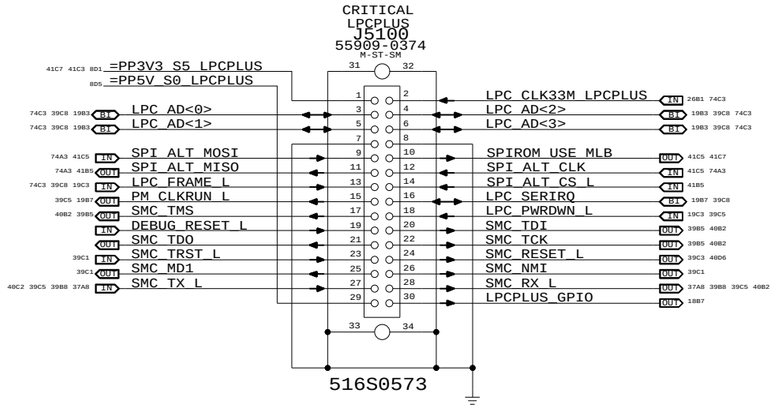
SMC Support

SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008

APPLE INC.

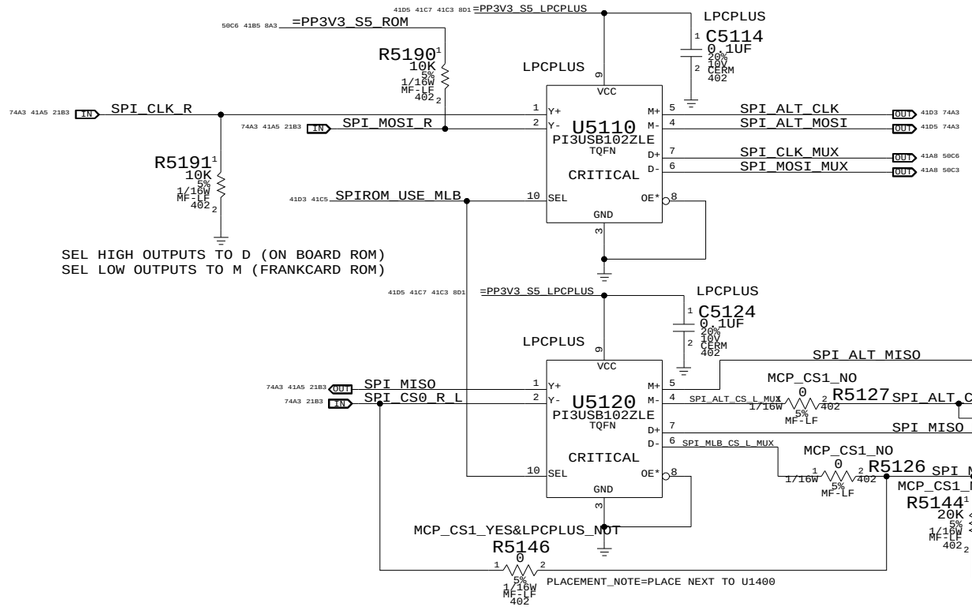
SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 50 OF 109	

LPC+SPI Connector



Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

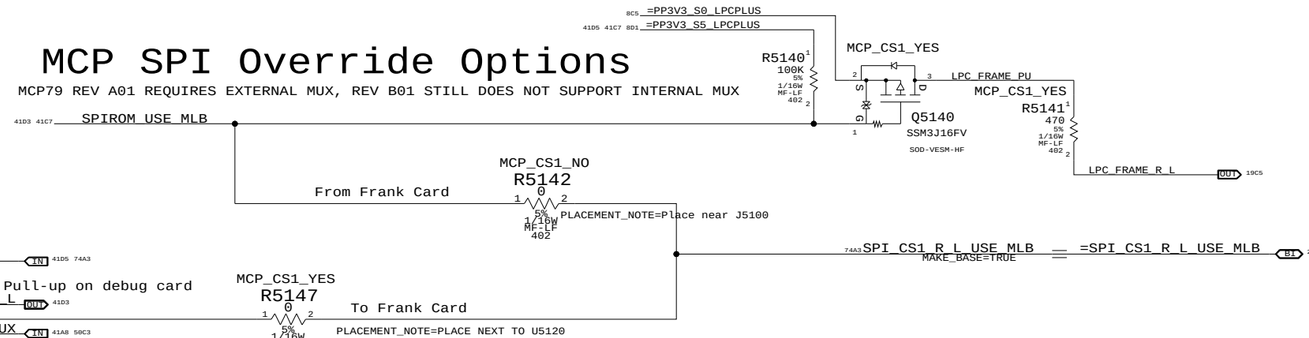


MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

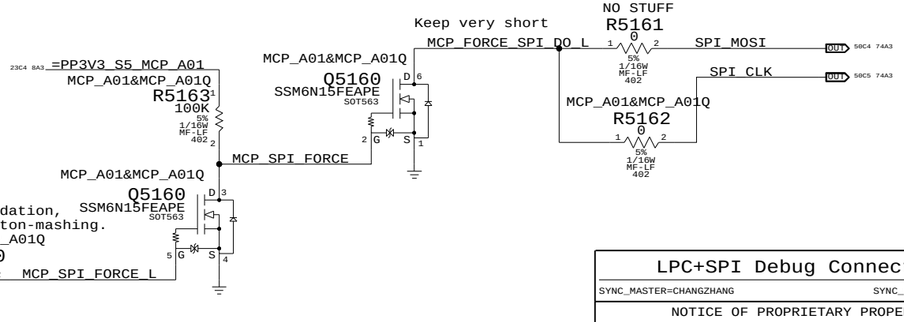
MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

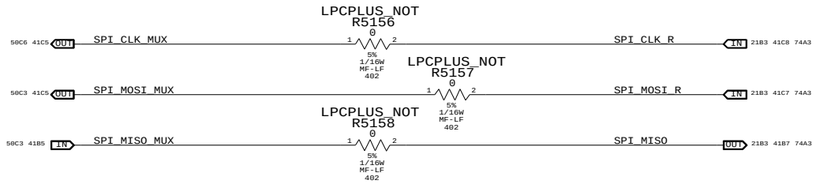


SPI Frequency Clamp

ENSURES MCP79 SPI_DO OR SPI_CLK INPUT IS LOW WHEN STRAP IS LATCHED.NOT NEEDED FOR B01 OR LATER.



SPI MUX BYPASS



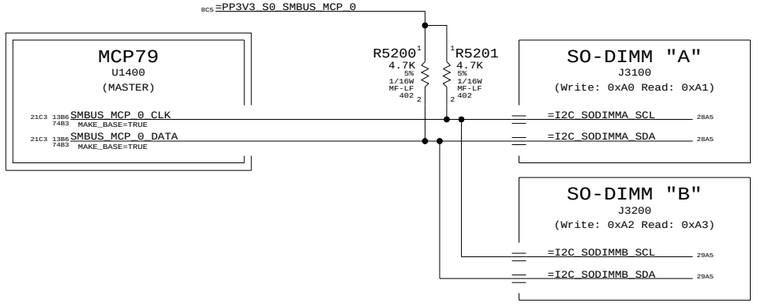
LPC+SPI Debug Connector

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

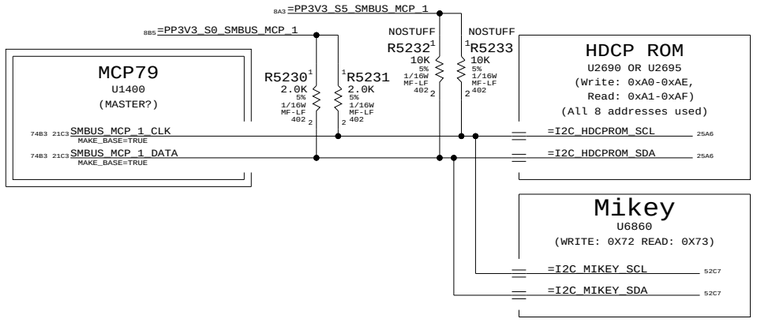
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 51 OF 109	

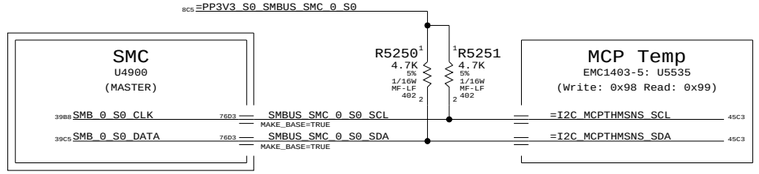
MCP79 SMBUS "0" CONNECTIONS



MCP79 SMBUS "1" CONNECTIONS

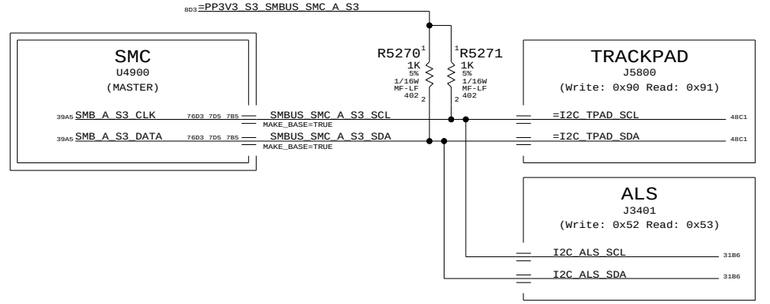


SMC "0" SMBus Connections

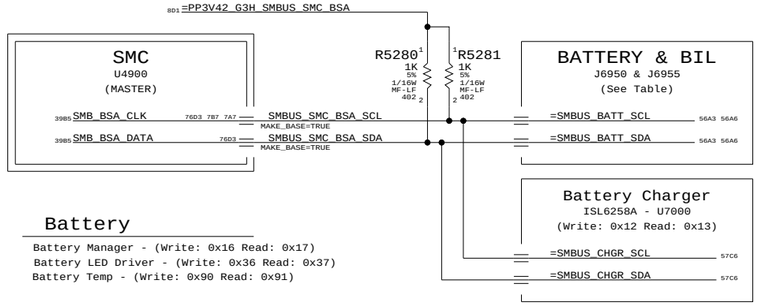


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



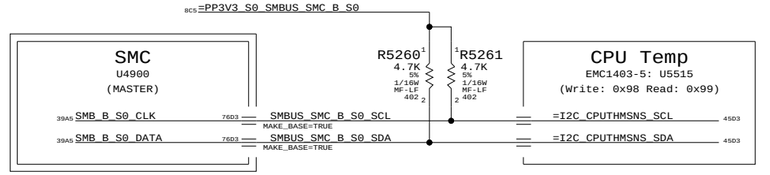
SMC "Battery A" SMBus Connections



Battery

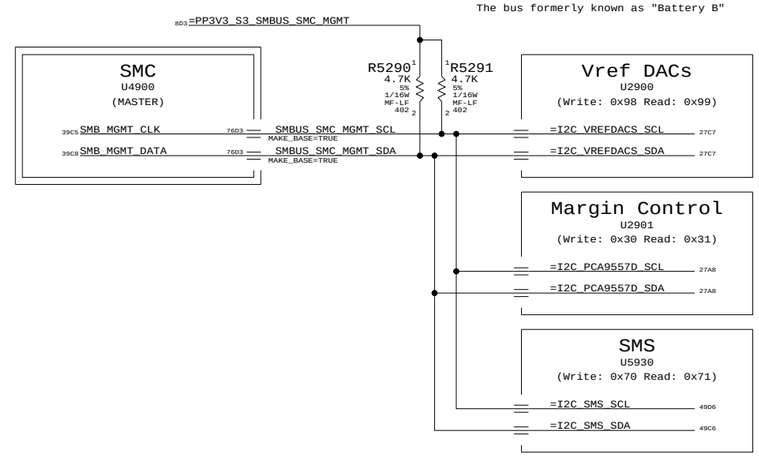
Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "B" SMBus Connections



SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



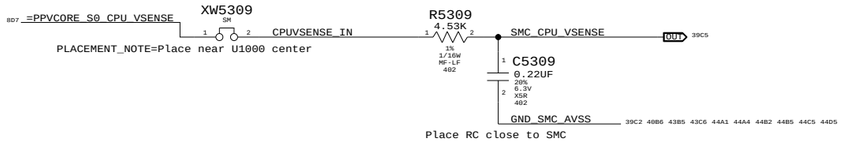
M97 SMBUS CONNECTIONS

SYNC_MASTER=BEN SYNC_DATE=04/21/2008

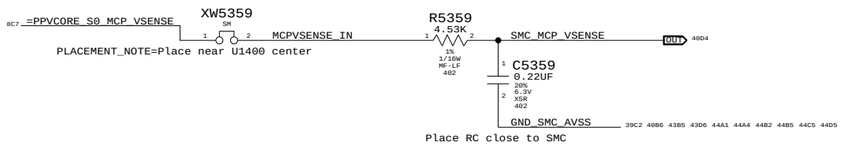
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	52	109

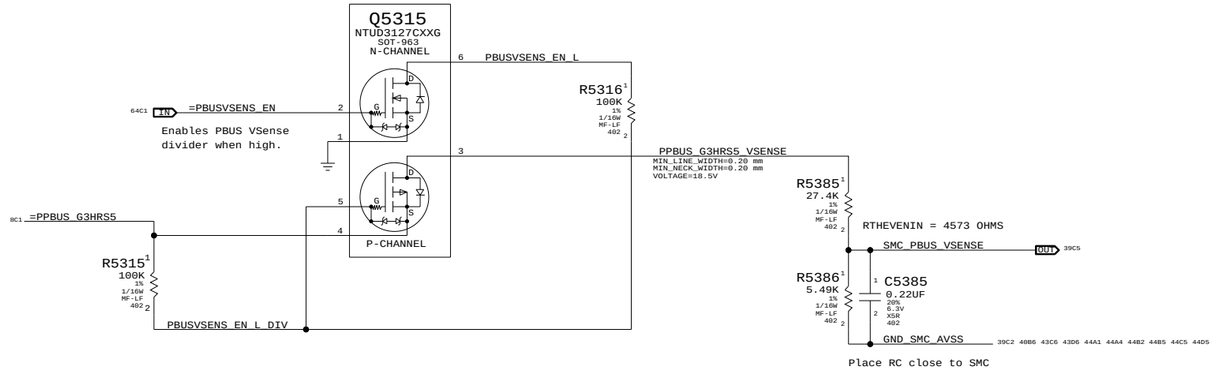
CPU Voltage Sense / Filter



MCP Voltage Sense / Filter



PBUS VOLTAGE SENSE ENABLE & FILTER



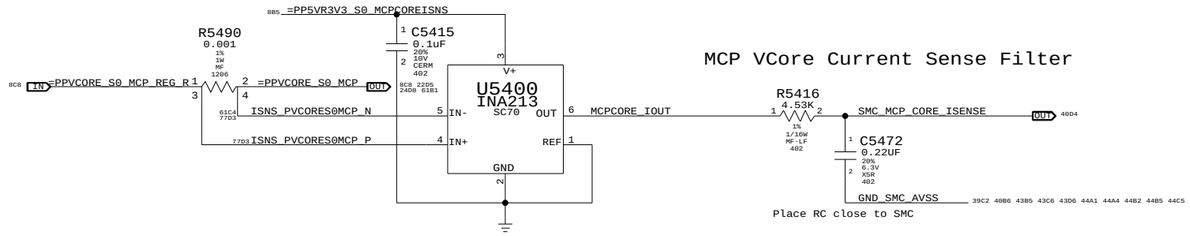
VOLTAGE SENSING

SYNC_MASTER=YUNWU SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 53 OF 109	

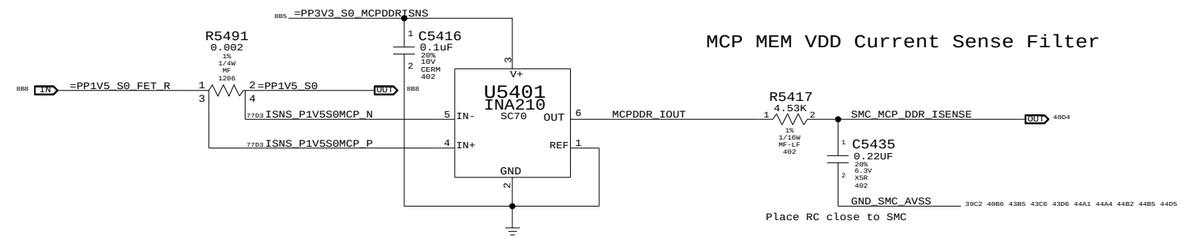
MCP VCore Current Sense



MCP VCore Current Sense Filter

Place RC close to SMC

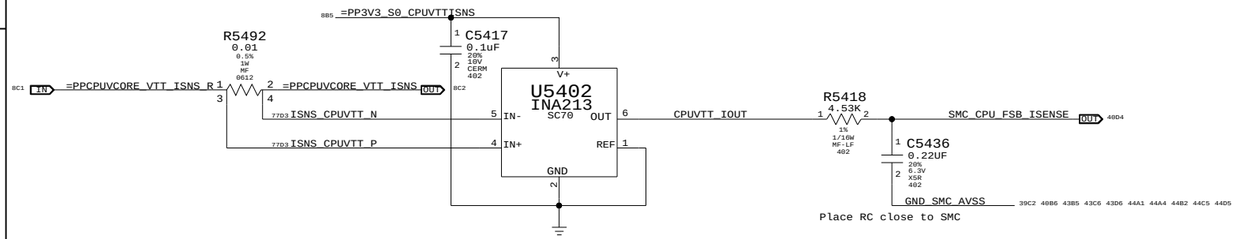
MCP MEM VDD Current Sense



MCP MEM VDD Current Sense Filter

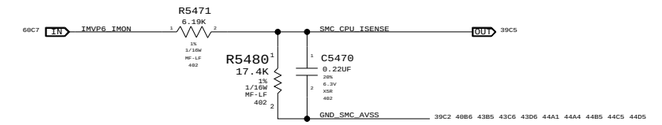
Place RC close to SMC

CPU 1.05V AND CPU VCORE HIGH SIDE CURRENT SENSE

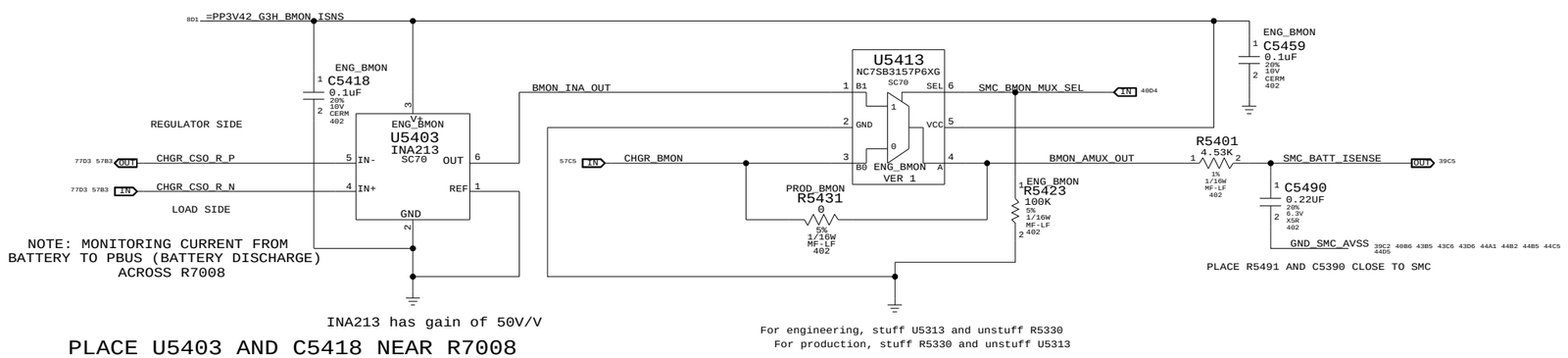


CPU VCore Load Side Current Sense / Filter

Place RC close to SMC



BMON CURRENT SENSE



NOTE: MONITORING CURRENT FROM BATTERY TO PBUS (BATTERY DISCHARGE) ACROSS R7008

INA213 has gain of 50V/V

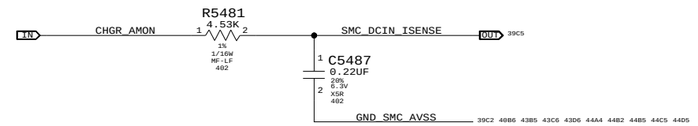
PLACE U5403 AND C5418 NEAR R7008

PLACE U5413, R5423, R5431, C5459 NEAR SMC (U4900)

For engineering, stuff U5313 and unstuff R5330
For production, stuff R5330 and unstuff U5313

PLACE R5491 AND C5390 CLOSE TO SMC

DC-IN (AMON) CURRENT SENSE



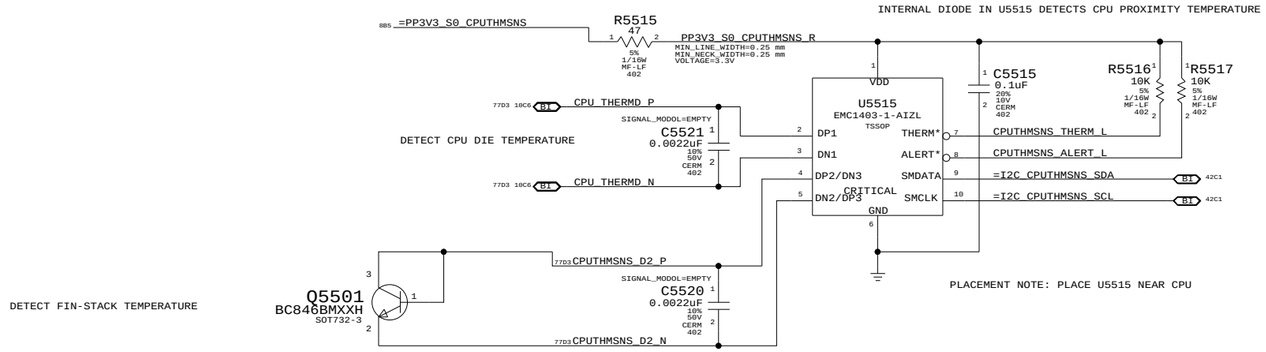
Current Sensing

SYNC_MASTER=YUNWU SYNC_DATE=04/07/2008

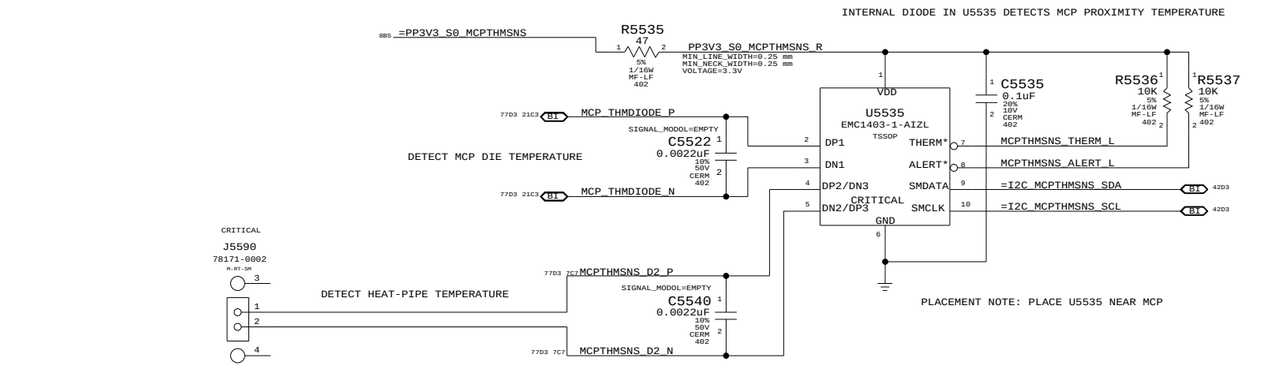
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 54 OF 109	

CPU T-Diode Thermal Sensor



MCP T-Diode Thermal Sensor



REPLACED 518S0521 WITH 518S0519

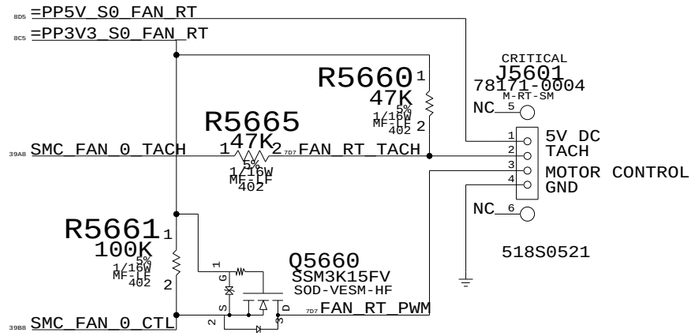
Thermal Sensors

SYNC_MASTER=YUNWU SYNC_DATE=03/20/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	55	109



Fan

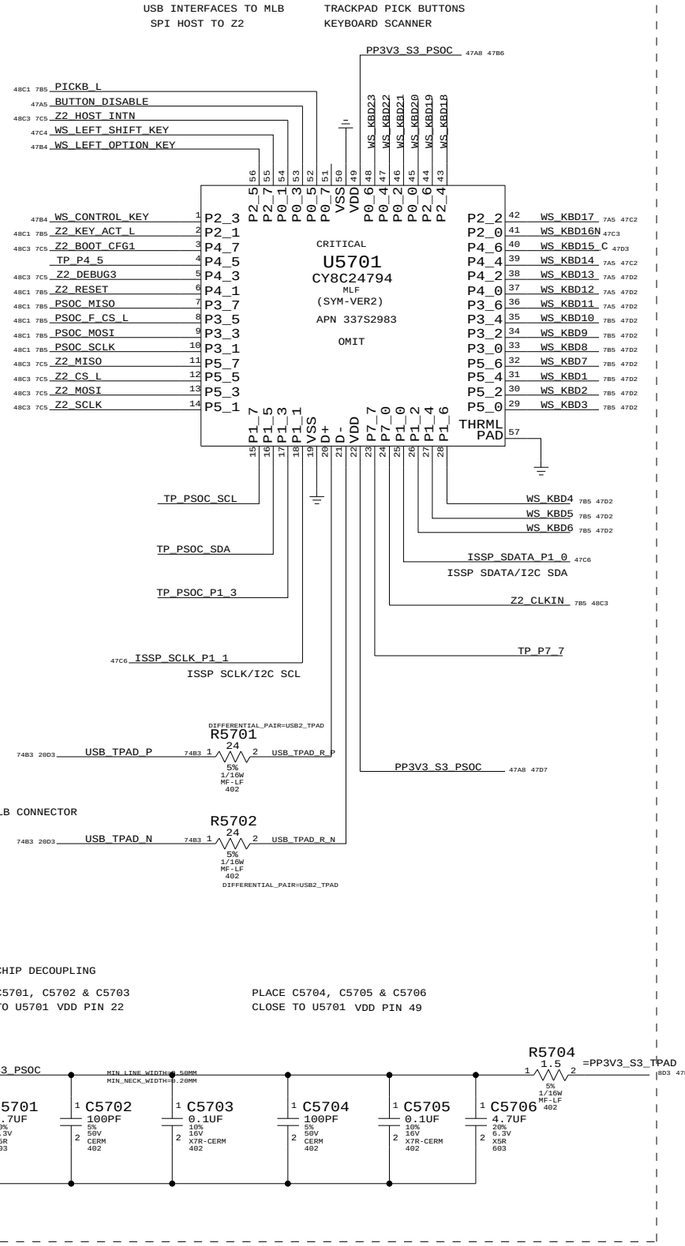
SYNC_MASTER=CHANGZHANG SYNC_DATE=01/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	56	109

PSOC USB CONTROLLER



U5701 CHIP DECOUPLING

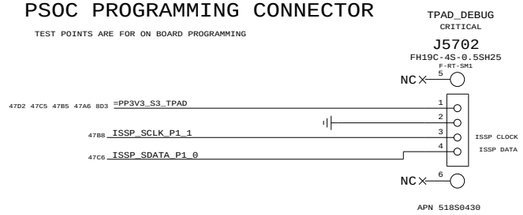
PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

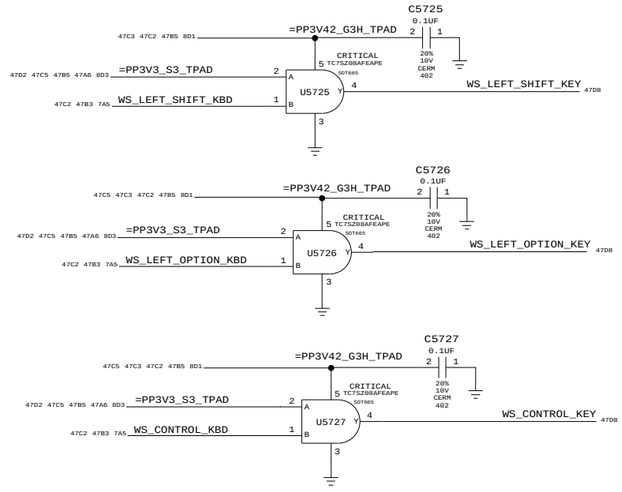
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA MAX	10 OHM	0.6 V	36E-3 W
	VOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

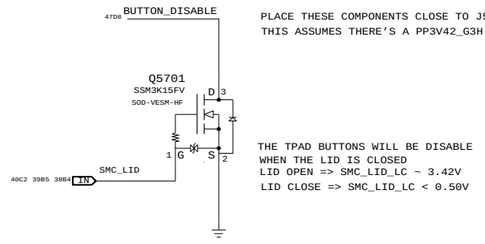
TEST POINTS ARE FOR ON BOARD PROGRAMMING



ISOLATION CIRCUIT



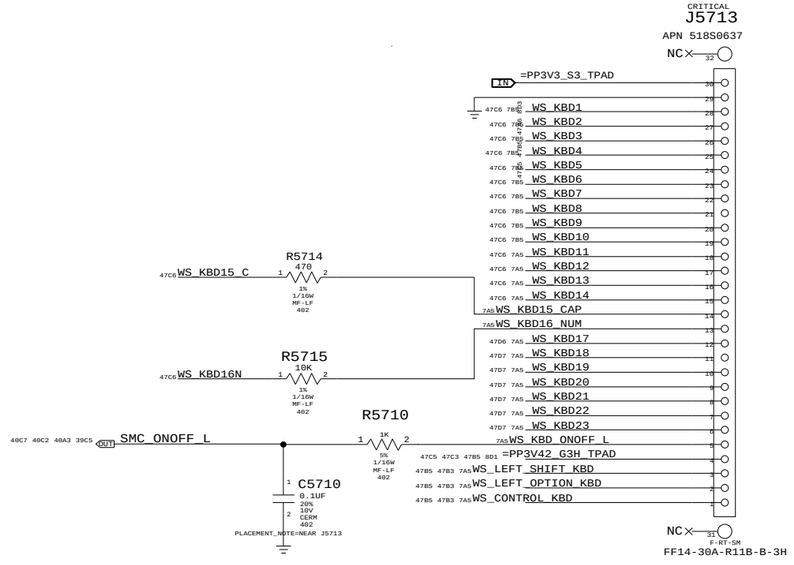
TPAD BUTTONS DISABLE



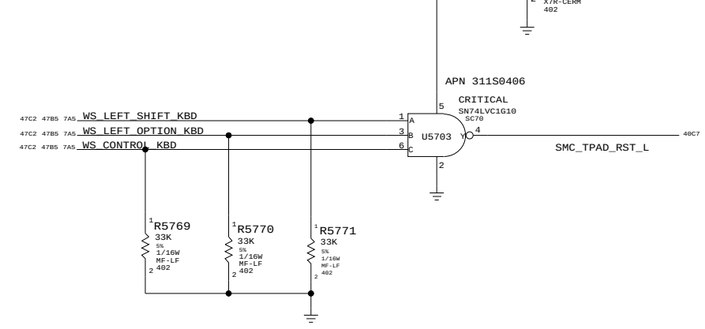
PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



WELLSPRING 1

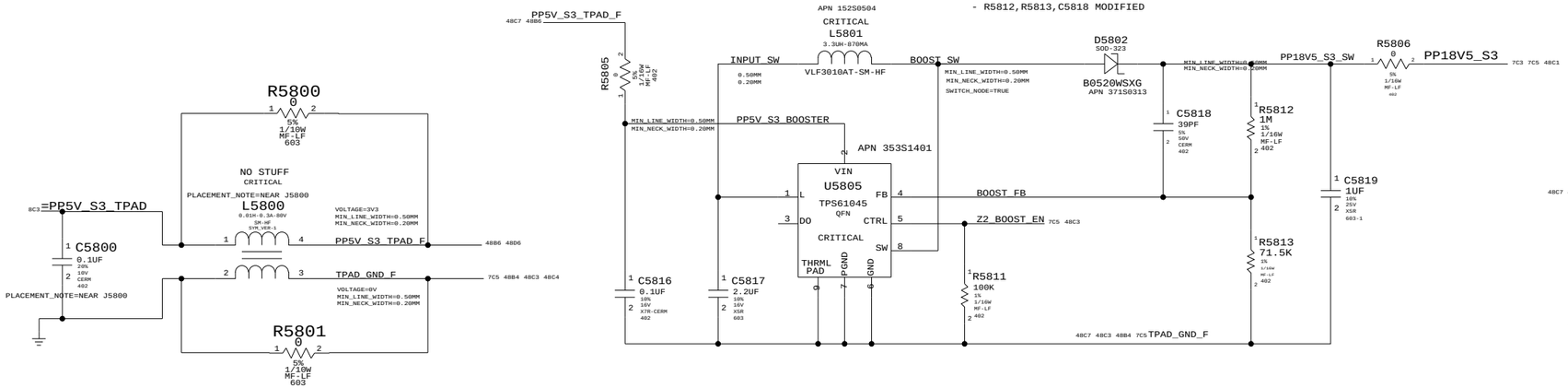
SYNC_MASTER=YUAN.MA SYNC_DATE=04/22/2008

APPLE INC.

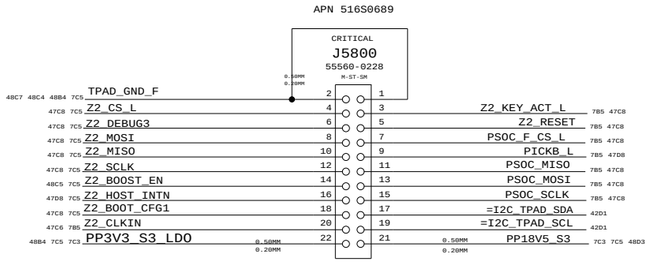
SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 57 OF 109	

BOOSTER +18.5VDC FOR SENSORS

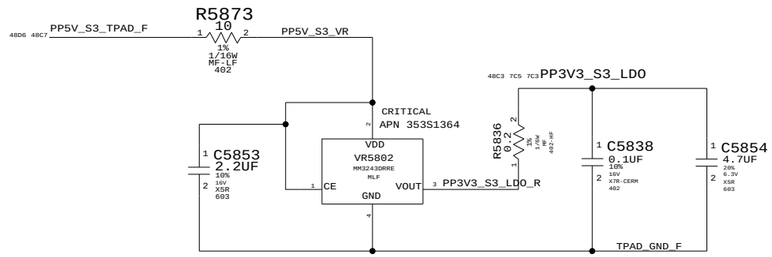
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD



KEYBOARD BACKLIGHT DRIVNG AND DETECTION

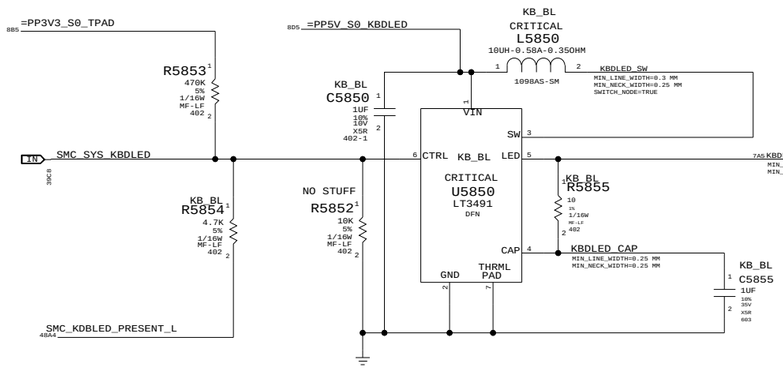
To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:

LOW = keyboard backlight present

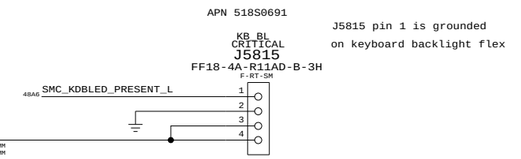
HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES
TURNED ON FOR BEST MLB CONFIG

R5853 ALWAYS PRESENT



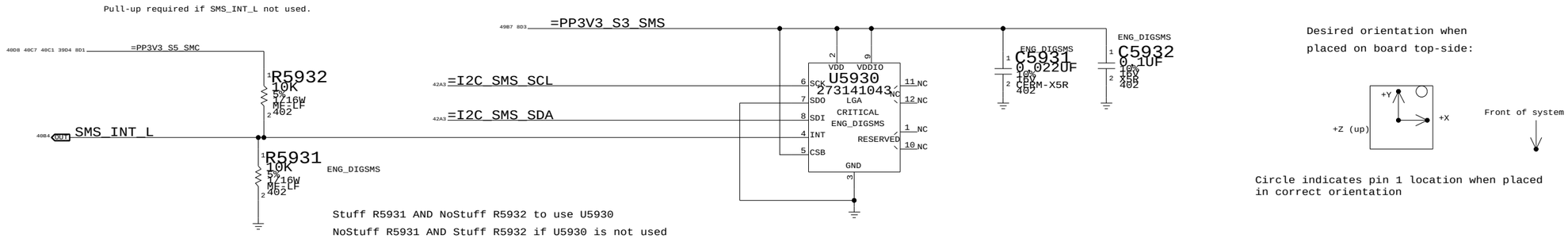
KBD BACKLIGHT CONNECTOR



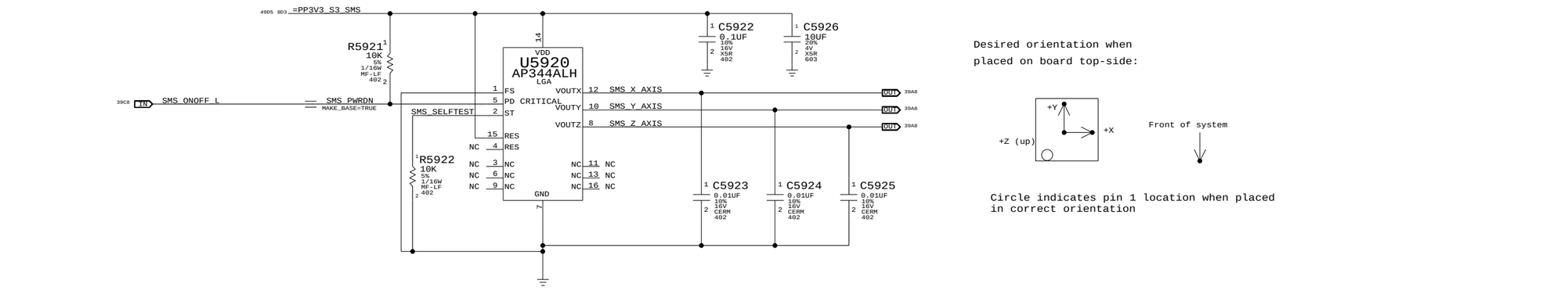
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 58 OF 109	

Digital SMS



Analog SMS

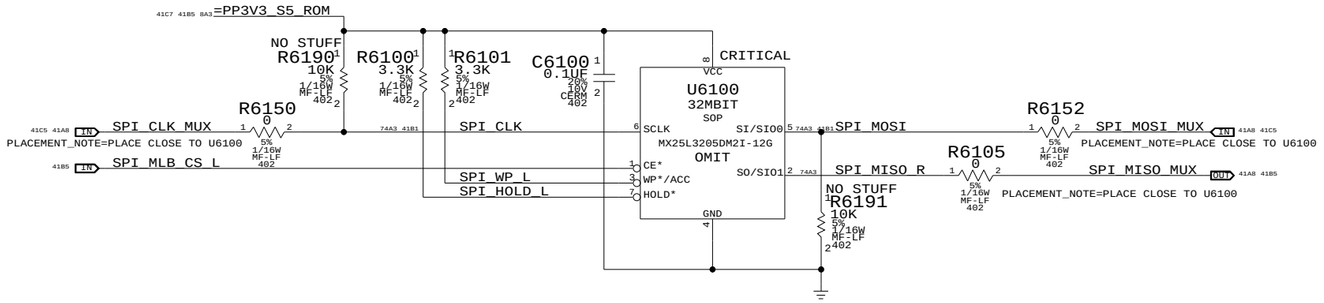


SMS

SYNC_MASTER=YUNWU SYNC_DATE=06/26/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 59 OF 109	



MCP79 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

SPI ROM

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/02/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 61 OF 109	

AUDIO CODEC

APPLE P/N 353S1538

ALIAS OF PP3V3_SO, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM

VOLTAGE=3.3V
=PP3V3_S0_AUDIO

CRITICAL
L6201
FERR-220-OHM
0402

MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.28MM
VOLTAGE=3.3V
CODEC_DVDD

CRITICAL
C6200 1UF 10% 6.3V CERM 402
C6201 0.01UF 10% 25V X7R 402
C6203 0.01UF 10% 25V X7R 402

R6270 100K 5% 1/16W MF-LF 402

CRITICAL
L6202
FERR-220-OHM
0402

MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=4.6V
PP4V6_AUDIO_ANALOG 7C2 51A3 52D6

MIN_LINE_WIDTH=0.20MM
MIN_NECK_WIDTH=0.28MM
AVDD_ADC_DAC

CRITICAL
C6204 100UF 20% 6.3V TANT CASE-AL1
C6206 0.01UF 10% 25V X7R 402
CRITICAL
C6205 100UF 20% 6.3V TANT CASE-AL1
C6207 0.01UF 10% 25V X7R 402

GND_AUDIO_CODEC 51A7 51B7 52B6 52C3 52C6 53A8 53B8 53C8 54B3 55A4 55A8 55B2 55B4 55B5 55B8 55C8 55D4

HDA_BIT_CLK 74B3 21D2 IN
HDA_SYNC 74B3 21D2 IN
HDA_SDOUT 74A3 21D2 IN
HDA_SDIN0 74A3 21D7 OUT

R6204 22 5% 1/16W MF-LF 402

HP AMP. SHDN CONTROL
AUD_GPIO_0 55D3 OUT

PORT C RT=SUB. SPKR SIGNAL SOURCE
AUD_BI_PORT_C_R 53B8 OUT
AUD_BI_PORT_D_L 55C4 OUT
AUD_BI_PORT_D_R 55B4 OUT
PORT D=HP SIGNAL SOURCE

HDA_RST_L 74A3 21D2 IN

R6203 100K 5% 1/16W MF-LF 402
CRITICAL
C6208 0.1UF 10% 10V X5R 402

NO STUFF
R6201 0 5% 1/16W MF-LF 402

GND_AUDIO_CODEC 55A4 54B3 53C8 53B8 53A8 52C6 52C3 52B6 51D3 51B7 55D4 55C8 55B8 55B5 55B4 55B2 55A8
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

CRITICAL
U6200
ALC885Q-VB3-GR
QFN
REV B3

DVDD	1		
DVDD_IO	9		
AVDD1	25		
AVDD2	38		
BCLK	6		
SYNC	10		
SDATA_OUT	5		
SDATA_IN	8		
GPIO0/DMIC-CLK	2		
GPIO1/DMIC-L	3		
PORT-C-L	23	NO_TEST	NC_AUD_BI_PORT_C_L
PORT-C-R	24		
PORT-D-L	35		
PORT-D-R	36		
CD-L	18	NO_TEST	NC_BAL_IN_L
CD-GND	19	NO_TEST	NC_BAL_IN_COM
CD-R	20	NO_TEST	NC_BAL_IN_R
BEEP	12		
RESET*	11		
THRM_PAD	49		
DVSS	4		
	7		
AVSS1	26		
AVSS2	42		
SPDIFO	48		AUD_SPDIF_O
SPDIFI/EAPD/MIDI-I/DMIC-R	47		
SENSE_A	13		
SENSE_B	34		
PORT-A-L	39		
PORT-A-R	41		
PORT-F-L	16		
PORT-F-R	17		
PORT-F-VREFO	30		
PORT-A-VREFO/DCVOL	33	NO_TEST	NC_AUD_VREF_PORT_A
PORT-E-L	14		
PORT-E-R	15		
PORT-E-VREFO	31	NO_TEST	NC_AUD_VREF_PORT_E
PORT-B-VREFO	28		
PORT-B-L	21		
PORT-B-R	22		
PORT-C-VREFO	29	NO_TEST	NC_AUD_VREF_PORT_C
PORT-B-VREFO2	32	NO_TEST	NC_AUD_VREF_PORT_D
PORT-G-L	43	NO_TEST	NC_AUD_BI_PORT_G_L
PORT-G-R	44	NO_TEST	NC_AUD_BI_PORT_G_R
PORT-H-L	45	NO_TEST	NC_AUD_BI_PORT_H_L
PORT-H-R	46	NO_TEST	NC_AUD_BI_PORT_H_R
VREF	27		AUD_CODEC_VREF
JDREF	40		AUD_CODEC_JDREF
NC	37	NO_TEST	NC_VRP

R6205 20.0K 1% 1/16W MF-LF 402
CRITICAL
C6210 3.3UF 10% 16V TANT SMA-HF
C6212 0.001UF 10% 50V CERM 402

R6206 22 5% 1/16W MF-LF 402

AUD_SPDIF_OUT 54D3 OUT
AUD_SPDIF_I 54B3 IN
AUD_SENSE_A 55C8 55B8 IN
AUD_SENSE_B 55C8 IN

PORT A = LINE INPUT
AUD_BI_PORT_A_L 55B1 IN
AUD_BI_PORT_A_R 55A1 IN

AUD_BI_PORT_F_L 55B4 IN
AUD_BI_PORT_F_R 55A4 IN
PORT F= MIC INPUT
AUD_VREF_PORT_F 55B4 OUT
PORT F VREF=MIC BIAS

AUD_BI_PORT_E_L 52B4 IN
PORT E = MIKEY MIC INPUT

SPKR. AMP. SHDN CONTROL
AUD_VREF_PORT_B 53C8 53B8 53A8 OUT
AUD_BI_PORT_B_L 53B8 OUT
AUD_BI_PORT_B_R 53C8 OUT
PORT B=L AND R SPKR AMP. SIGNAL SOURCE

R6209 100K 5% 1/16W MF-LF 402

AUDIO 4.6V REGULATOR

APPLE P/N 353S1897

ALIAS OF PP5VLT_S3, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

VOLTAGE=5V
=PP5V_S3_AUDIO 55D4 8C5

CRITICAL
L6200
FERR-220-OHM
0402

MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.30MM
PP5V_S3_AUDIO_F

CRITICAL
U6201
MAX8902A
TDFN

R6202 1K 5% 1/16W MF-LF 402

=PP3V3_S0_AUDIO 55B5 54D8 52D6 51D8 8C5

PP4V6_ENABLE

EN	3		
IN	1		
BP	7		
GND	2		
THRML PAD	9		
SELA	4		
SELB	5		
OUT	8		
OUTS	6		

MAX8902_BP

C6220 0.1UF 10% 16V X5R 402
R6210 10K 5% 1/16W MF-LF 402
C6223 0.01UF 10% 25V X7R 402
CRITICAL
C6221 10UF 20% 6.3V X5R 603
C6224 0.01UF 10% 50V X7R 603-1
CRITICAL
C6222 10UF 20% 6.3V X5R 603
C6225 0.01UF 10% 25V X7R 402

PP4V6_AUDIO_ANALOG 7C2 51D3 52D6

GND_AUDIO_CODEC 55A4 54B3 53C8 53B8 53A8 52C6 52C3 52B6 51D3 51B7 55D4 55C8 55B8 55B5 55B4 55B2 55A8

XW6200 SM
PLACE XW6200 AND XW6201 NEAR U6200
XW6201 SM
STAR GND PT. FOR AUDIO SYSTEM
GND_SPKR_AMP 53C4 53B3 53A4

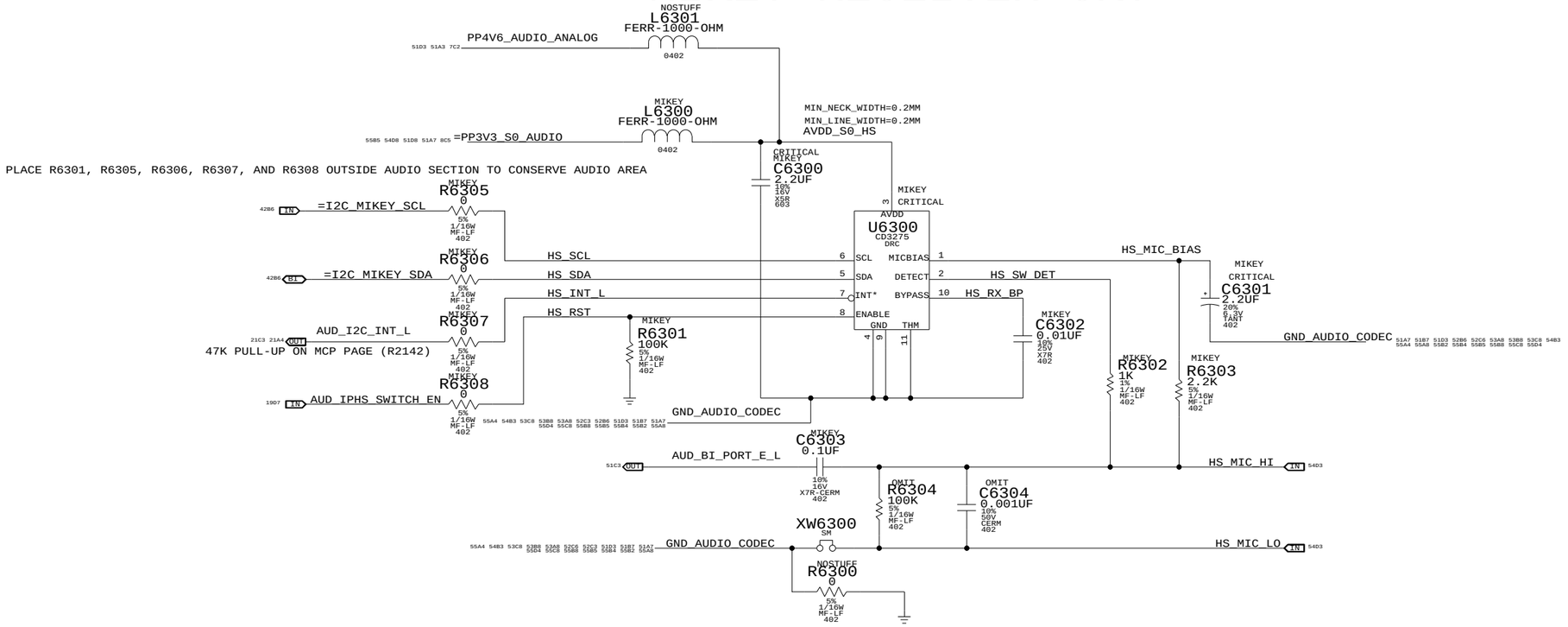
AUDIO: CODEC

SYNC_MASTER=AUDIO
SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 62 OF 109	

MIKEY RECEIVER CKT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6304	?	NOMIKEY
132S0045	1	0.001UF 50V 10% 0402 CAP	C6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6304	?	NOMIKEY

AUDIO: MIKEY

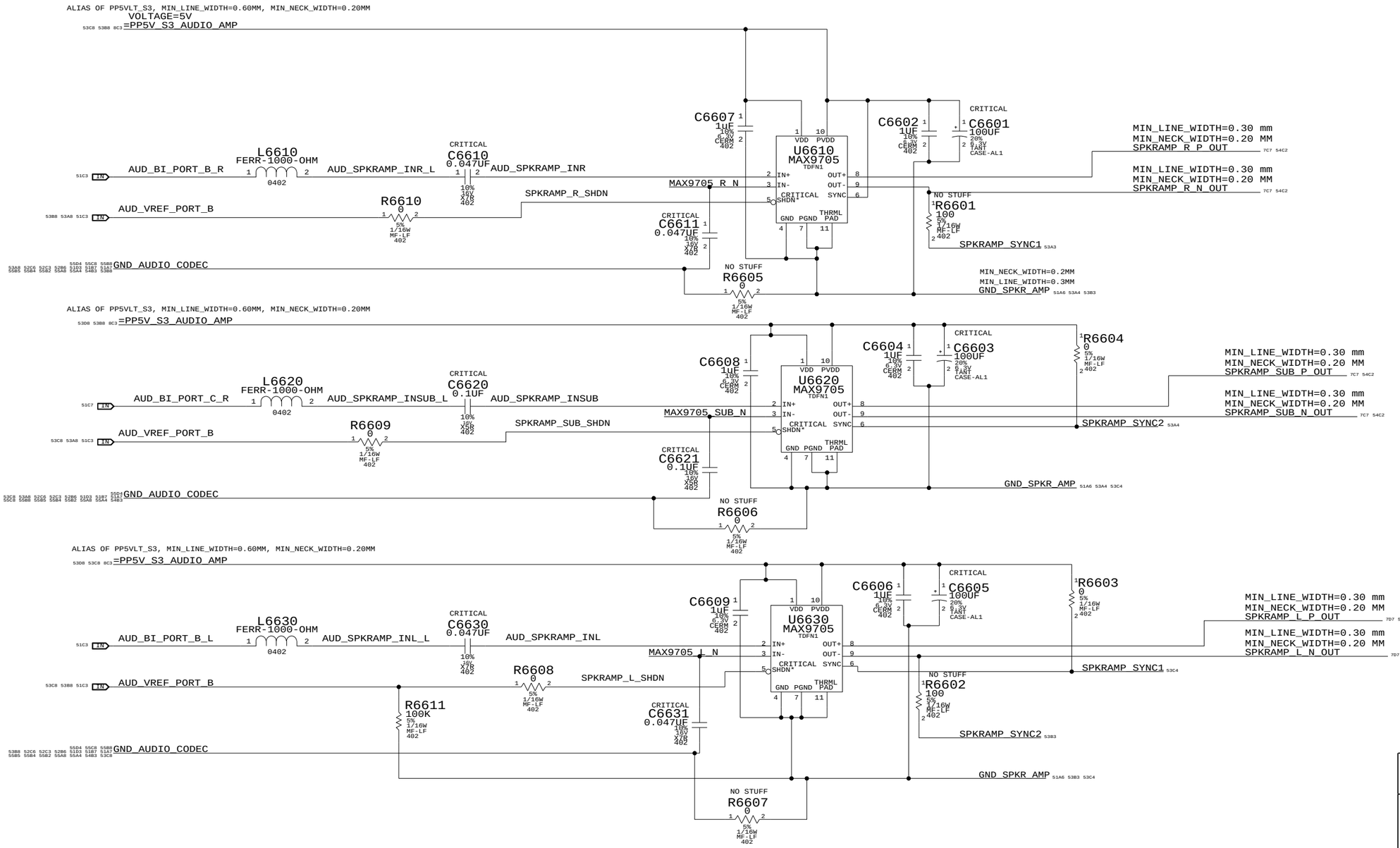
SYNC_MASTER=AUDIO SYNC_DATE=07/03/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 63 OF 109	

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	12DB



AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 66 OF 109	

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

=PP3V3_S0_AUDIO
PP3V3_S0_AUDIO_SPDIF
=GND_CHASSIS_AUDIO_JACK
AUD_SPDIF_OUT
AUD_CONNJ1_MIC_F
HS_MIC_HI
HS_MIC_LO
AUD_CONNJ1_MIC
AUD_CONNJ1_SLEEVE
AUD_CONNJ1_SLEEVE_F
AUD_CONNJ1_TIPDET
AUD_CONNJ1_TIPDET_F
AUD_CONNJ1_TIP
AUD_CONNJ1_TIP_F
AUD_CONNJ1_RING
AUD_CONNJ1_RING_F
AUD_CONNJ1_SLEEVEDET
AUD_CONNJ1_SLEEVEDET_F
AUD_LO_AMP_OUTR
AUD_LO_AMP_OUTL
AUD_J1_SLEEVEDET_R
AUD_J1_TIPDET_R
AUD_J1_COM
AUD_LO_GND
CHASSIS GND BAND AID

R6790 0 5% 1/16W MF-LF 402
R6702 0 5% 1/16W MF-LF 402
R6703 0 5% 1/16W MF-LF 402
R6704 0 5% 1/16W MF-LF 402
R6705 0 5% 1/16W MF-LF 402
R6706 0 5% 1/16W MF-LF 402
R6707 0 5% 1/16W MF-LF 402
R6700 10K 5% 1/16W MF-LF 402
R6701 4.7 5% 1/16W MF-LF 402
NOSTUFF R6760 0 5% 1/16W MF-LF 402

L6709 FERR-1000-OHM 0402
L6710 FERR-1000-OHM 0402
CRITICAL L6701 FERR-120-OHM-1.5A 0402-LF
L6704 FERR-1000-OHM 0402
L6706 FERR-1000-OHM 0402

CRITICAL J6700 AUDIO-JACK-TRANS-M97 F-RT-TH5
AUDIO
A - VIN
B - VCC
C - GND
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
APN:514-0634

C6700 1UF 10% 10V CERM 402
C6705 100PF 5% 50V CERM 402

CRITICAL DZ6706 6.8V-100PF 402
CRITICAL DZ6702 6.8V-100PF 402
CRITICAL DZ6703 6.8V-100PF 402
CRITICAL DZ6704 6.8V-100PF 402
CRITICAL DZ6705 6.8V-100PF 402

XW6700 SM
XW6701 SM

MIC CONNECTOR

APN:518S0520

CRITICAL J6701 78171-0003 M-RT-SM
MIC_LO_CONN
MIC_HI_CONN
MIC_SHLD_CONN

SPEAKER CONNECTOR

APN:518S0519

CRITICAL J6702 78171-0002 M-RT-SM
SPKRAMP_L_P_OUT
SPKRAMP_L_N_OUT
SPKRAMP_SUB_P_OUT
SPKRAMP_SUB_N_OUT
SPKRAMP_R_P_OUT
SPKRAMP_R_N_OUT

C6760 100PF 5% 50V CERM 402
C6761 100PF 5% 50V CERM 402
C6762 100PF 5% 50V CERM 402
C6763 100PF 5% 50V CERM 402

CRITICAL J6703 78171-0004 M-RT-SM
APN:518S0521

C6760 - C6763 ARE FOR FILTERING POTENTIAL FSB NOISE COUPLED ON SPKR LINES

MIC EMI FILTER

MIC_LO
MIC_HI
MIC_LO_CONN_F
MIC_HI_CONN_F
MIC_LO_CONN
MIC_HI_CONN
=GND_CHASSIS_AUDIO_MIC

L6770 FERR-1000-OHM 0402
L6771 FERR-1000-OHM 0402
L6772 FERR-1000-OHM 0402
L6773 FERR-1000-OHM 0402

CRITICAL DZ6770 6.8V-100PF 402
CRITICAL DZ6771 6.8V-100PF 402

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

=PP3V3_S0_AUDIO_SPDIF
=GND_CHASSIS_AUDIO_JACK
AUD_J2_OPT_OUT
AUD_SPDIF_I
AUD_J2_COM
GND_AUDIO_CODEC
AUD_CONNJ2_SLEEVE
AUD_CONNJ2_SLEEVE_F
AUD_CONNJ2_TIPDET
AUD_CONNJ2_TIPDET_F
AUD_CONNJ2_TIP
AUD_CONNJ2_RING
AUD_CONNJ2_RING_F
AUD_CONNJ2_TIP_F
AUD_CONNJ2_SLEEVEDET
AUD_CONNJ2_SLEEVEDET_F
AUD_PORTA_R
AUD_PORTA_L
AUD_J2_TIPDET_R

R6749 22 5% 1/16W MF-LF 402
R6752 0 5% 1/16W MF-LF 402
R6753 0 5% 1/16W MF-LF 402
R6754 0 5% 1/16W MF-LF 402
R6755 0 5% 1/16W MF-LF 402
R6756 0 5% 1/16W MF-LF 402
R6750 10K 5% 1/16W MF-LF 402
R6751 4.7 5% 1/16W MF-LF 402

CRITICAL L6751 FERR-120-OHM-1.5A 0402-LF
L6754 FERR-1000-OHM 0402
L6756 FERR-1000-OHM 0402

CRITICAL J6750 AUDIO-RCVR-M97 F-RT-TH5
DETECT FOR PLUG TYPE
SWITCH
LEFT
RIGHT
GROUND
AUDIO
A - VDD
B - GND
C - VOUT
OPERATING VOLTAGE 3.3
POF
SHELL
SHIELD PINS
APN:514-0635

C6750 1UF 10% 10V CERM 402
C6756 100PF 5% 50V CERM 402

CRITICAL DZ6752 6.8V-100PF 402
CRITICAL DZ6753 6.8V-100PF 402
CRITICAL DZ6754 6.8V-100PF 402
CRITICAL DZ6755 6.8V-100PF 402

APPLE INC.
SIZE D
DRAWING NUMBER 051-7918
REV. C
SCALE NONE
SHT 67 OF 109

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0C (12)	0X02 (2)	0X14 (20,PORTD)	GPIO 0	0X14 (20,PORTD)
SAT SPKRS	0X0D (13)	0X03 (3)	0X18 (24,PORTB)	VREF_B(100%)	N/A
SUB SPKR	0X0F (15)	0X05 (5)	0X1A (26,PORTC)	VREF_B(100%)	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X16 (22, PORTG)

CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X15 (21,PORTA)	N/A	0X15 (21,PORTA)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X19 (25,PORTF)	VREF_F (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A

HP/LO AMP
APN:353S1637
PORT D HP/LO

ALIAS OF PP5VLT_S3, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

L6880 FERR-120-OHM-1.5A 0402-LF

=PP5V_S3_AUDIO → AUD_PP5V_F

MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.3MM

C6880 0.1UF 10% 16V X7R-CERM 402

C6881 10UF 20% 6.3V X5R 603

U6801 MAX9724A TQFN CRITICAL

VDD, INL ← AUD_LO_AMP_INL_M, INR ← AUD_LO_AMP_INR_M, SHDN* ← AUD_GPIO_0, THRM PAD, SGND, PGND, SVSS, PVSS

OUTL → AUD_LO_AMP_OUTL, OUTR → AUD_LO_AMP_OUTR

MIN_NECK_WIDTH=0.15MM MIN_LINE_WIDTH=0.2MM

MAX9724 C1P: C1P → C6882 1UF 10% 16V X5R 402-1 → MAX9724 C1N

R6880 2.21K 1% 1/16W MF-LF 402

R6881 2.21K 1% 1/16W MF-LF 402

R6885 10K 5% 1/16W MF-LF 402

MAX9724 SVSS: C6884 1UF 10% 16V X5R 402-1, C6885 1UF 10% 16V X5R 402-1 CRITICAL

GND_AUDIO_CODEC → XW6880 SM PLACE CLOSE TO U6801

MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.4MM

AUD_LO_GND

NO STUFF R6882 0 5% 1/16W MF-LF 402

PORT D DETECT

AUD_SENSE_B, AUD_SENSE_A

PP3V3_S0_AUDIO_F → R6801 270K 5% 1/16W MF-LF 402

AUD_J1_TIPDET_R → R6802 47K 5% 1/16W MF-LF 402 → AUD_J1_DET_RC

C6801 0.1UF 10% 16V X5R 402

Q6800 SSM6N15FEAPE SOT563

AUD_OUTJACK_INSERT_L

R6806 5.11K 1% 1/16W MF-LF 402 → AUD_PORTD_DET_L NC

Q6801 SSM6N15FEAPE SOT563

PORT G DETECT(SPDIF DELEGATE)

R6805 10K 1% 1/16W MF-LF 402 → AUD_PORTG_DET_L NC

Q6801 SSM6N15FEAPE SOT563

R6803 100K 5% 1/16W MF-LF 402

PP3V3_S0_AUDIO_F → R6861 270K 5% 1/16W MF-LF 402 → AUD_J1_SLEEVEDET_INV

AUD_J1_SLEEVEDET_R

Q6800 SSM6N15FEAPE SOT563

C6802 0.01UF 10% 16V CERM 402

GND_AUDIO_CODEC

PLACE L6800/C6800 CLOSE TO Q6800

AUD_J1_SLEEVEDET_R

L6800 FERR-1000-OHM 0402

=PP3V3_S0_AUDIO → PP3V3_S0_AUDIO_F

C6800 0.1UF 10% 16V X5R 402

GND_AUDIO_CODEC

MIC INPUT CIRCUITRY

R6850 6.81K 1% 1/16W MF-LF 402 → VREF_PORT_F_R

R6855 2.2K 5% 1/16W MF-LF 402 → AUD_VREF_PORT_F

C6853 10UF 20% 6.3V X5R 603 CRITICAL

GND_AUDIO_CODEC

MIC_HI → R6851 330 5% 1/16W MF-LF 402 → MIC_IN

C6850 0.1UF 10% 16V X5R 402 → AUD_BI_PORT_F_L MAKE_BASE=TRUE

C6851 680PF 10% 50V CERM 402 CRITICAL

R6852 100K 5% 1/16W MF-LF 402

C6852 100PF 5% 50V CERM 402 CRITICAL

AUD_BI_PORT_F_R

NO STUFF PLACE C6852 NEAR U6200

MIC_LO → XW6800 SM NO STUFF → GND_AUDIO_CODEC

MIC_SHLD_CONN → R6853 0 5% 1/16W MF-LF 402

R6854 0 5% 1/16W MF-LF 402 → =GND_CHASSIS_AUDIO_MIC

NO STUFF R6856 0 5% 1/16W MF-LF 402

LINE-IN (PORT A) DETECT

AUD_SENSE_A

PP3V3_S0_AUDIO_F → R6811 270K 5% 1/16W MF-LF 402

R6813 39.2K 1% 1/16W MF-LF 402 → AUD_INJACK_INSERT_L NC

AUD_J2_TIPDET_R → R6812 47K 5% 1/16W MF-LF 402 → AUD_J2_DET_RC

C6811 0.1UF 10% 16V X5R 402

Q6802 SSM3K15FV SOD-VESM-HF

GND_AUDIO_CODEC

MAX9724 GAIN/FILTER COMPONENTS
AV_PB = -1 V/V, FC_HPF=5.28HZ, FC_LPF=34.45KHZ

C6888 220PF 5% 25V CERM 402 CRITICAL

R6884 21K 1% 1/16W MF-LF 402

AUD_BI_PORT_D_L → C6886 2.2UF 20% 6.3V TANT 402 CRITICAL → AUD_LO_AMP_INL_C

R6883 13.7K 1% 1/16W MF-LF 402 → AUD_LO_AMP_INL_M → AUD_LO_AMP_OUTL

AUD_BI_PORT_D_R → C6889 2.2UF 20% 6.3V TANT 402 CRITICAL → AUD_LO_AMP_INR_C

R6886 13.7K 1% 1/16W MF-LF 402 → AUD_LO_AMP_INR_M → AUD_LO_AMP_OUTR

R6888 21K 1% 1/16W MF-LF 402

C6891 220PF 5% 25V CERM 402 CRITICAL

PORT A LI

AUD_PORTA_L → C6832 2.2UF 20% 6.3V TANT 402 CRITICAL → AUD_BI_PORT_A_L

R6836 27.4K 1% 1/16W MF-LF 402

GND_AUDIO_CODEC

R6837 27.4K 1% 1/16W MF-LF 402

AUD_PORTA_R → C6833 2.2UF 20% 6.3V TANT 402 CRITICAL → AUD_BI_PORT_A_R

AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO SYNC_DATE=07/01/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE: NONE SHT 68 OF 109

MagSafe DC Power Jack

CRITICAL
J6900
78048-0573
M-RT-SM
518S0656

787 PP18V5_DCIN_FUSE
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V

CRITICAL
F6905
6AMP-24V
1206-1

C6905 0.01UF 20% 50V CERM 603

R6928 0 5% 1/16W MF-LF 402

787 ADAPTER_SENSE

ADAPTER_SENSE_R

=PP18V5_DCIN_CONN 8D2 56C8

Q6910 restricts system load to 10K-70K window until adapter detects system and enables 16.5V output.

1-Wire OverVoltage Protection

CRITICAL
Q6910
NTUD3127CXXG
SOT-963
P-CHN
Vgs(max) = 8V

PP18V5_DCIN_ONEWIRE
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.20mm
VOLTAGE=18.5V

R6917 270K 5% 1/16W MF-LF 402
R6911 180K 5% 1/16W MF-LF 402

ONEWIRE_PWR_EN_L_DIV

Vgs = 7.30V @ 20V DCIN
Vgs = 4.74V @ 13V DCIN

R6912 470K 5% 1/16W MF-LF 402

C6915 0.1UF 10% 25V X5R 402

<Ra>
R6913 100K 5% 1/16W MF-LF 402

<Rb>
R6914 100K 5% 1/16W MF-LF 402

ONEWIRE_DCIN_DIV
<Vth>
ONEWIRE_ESD

If ADAPTER_SENSE > Vth
then turn off FET

CRITICAL
U6915
LM397
SOT23-5-HF

ONEWIRE_OVERVOLT

R6915 270K 5% 1/16W MF-LF 402
R6916 270K 5% 1/16W MF-LF 402

CRITICAL
Q6915
SSM3K15FV
SOD-VESM-HF

ONEWIRE_EN

R6918 270K 5% 1/16W MF-LF 402

C6917 0.001UF 10% 50V CERM 402

ONEWIRE_PWR_EN_L

CRITICAL
Q6910
N-CHN
NTUD3127CXXG
SOT-963

SMC_BC_ACOK_RC
R6910 1K 5% 1/16W MF-LF 402
SMC_BC_ACOK
IN 39C5 40B2 40D5

C6910 0.001UF 10% 50V CERM 402

Vth = Vdcin * (Rb / (Ra + Rb))
Vth = Vdcin / 2

R6920 24.3K 1% 1/16W MF-LF 402

VOLTAGE DIVIDER FROM DCIN ENSURES Q6910
Vgs is met when SYS_ONEWIRE is high or low.
Q6920 used as bilateral switch to ensure
SYS_ONEWIRE doesn't drive unpowered U6990

CRITICAL
Q6920
SSM6N15FEAPE
SOT563

SYS_ONEWIRE_BILAT
SYS_ONEWIRE
BI 39B8 40B2

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

56D1 8D2 =PP18V5_DCIN_CONN

R6905 47 5% 1/8W MF-LF 805

PPDCIN_S5_P3V42G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=18.5V

D6905
HN2D01JEAPE
SOT665
NC

57A2 56A7 BATT_POS_F
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=12.6V

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V

P3V42G3H_BOOST

C6990 10UF 10% 25V X5R 805

U6990
LT3479ETS8
TSOT23-8
VIN
BOOST
SHDN*
NC
SW
BIAS
FB
GND
CRITICAL

C6994 0.22uF 20% 6.3V X5R 402

CRITICAL
L6995
33UH
CDPH4D19FHF-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

=PP3V42_G3H_REG 8D2

Vout = 3.425V
200mA max output
(Switcher limit)

C6995 22pF 5% 50V CERM 402

<Ra>
R6995 348K 1% 1/16W MF-LF 402

CRITICAL
C6999 22UF 20% 6.3V CERM 805

<Rb>
R6996 200K 1% 1/16W MF-LF 402

P3V42G3H_FB

Vout = 1.25V * (1 + Ra / Rb)

BIL BUTTON DEBOUNCE CIRCUIT

56A3 8D1 =PP3V42_G3H_BATT

C6960 0.1UF 10% 16V X5R 402

R6960 10K 1/10W 402 MF-LF 5%

U6960
74LVC1G17DRL
SOT-553
NC

(SMC_BIL_BUTTON_L)
SMC_BIL_BUTTON_L
OUT 39C5
TO SMC

C6961 0.01UF 10% 16V X7R 402

BATTERY POWER CONNECTOR

CRITICAL
J6950
BAT-M98
F-RT-SM
516S0698

L6950
FERR-50-OHM
SM-LF

7B7 PPVBAT_G3H_CONN_F
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=12.6V

57A2 56B8 BATT_POS_F

=SMBUS_BATT_SCL 42C3 56A3
=SMBUS_BATT_SDA 42C3 56A3
SMC_BS_ALRT_L

CRITICAL
D6950
RCLAMP2402B
SC-75

C6956 47PF 5% 50V CERM 402

C6950 0.1UF 10% 25V X5R 402

L6951
FERR-50-OHM
SM-LF

7B7 GND_BATT_CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=0V

BATTERY SIGNAL CONNECTOR

CRITICAL
J6955
78171-0005
M-RT-SM
518S0588

=PP3V42_G3H_BATT
=SMBUS_BATT_SDA
=SMBUS_BATT_SCL
7A7 SMC_BIL_BUTTON_DB_L

OUT 8D1 56B3
BI 42C3 56A6
BI 42C3 56A6

C6954 0.001UF 10% 50V CERM 402
C6952 47PF 5% 50V CERM 402
C6951 0.1UF 10% 25V X5R 402
C6953 47PF 5% 50V CERM 402

DC-In & Battery Connectors

SYNC_MASTER=JACK SYNC_DATE=03/13/2008

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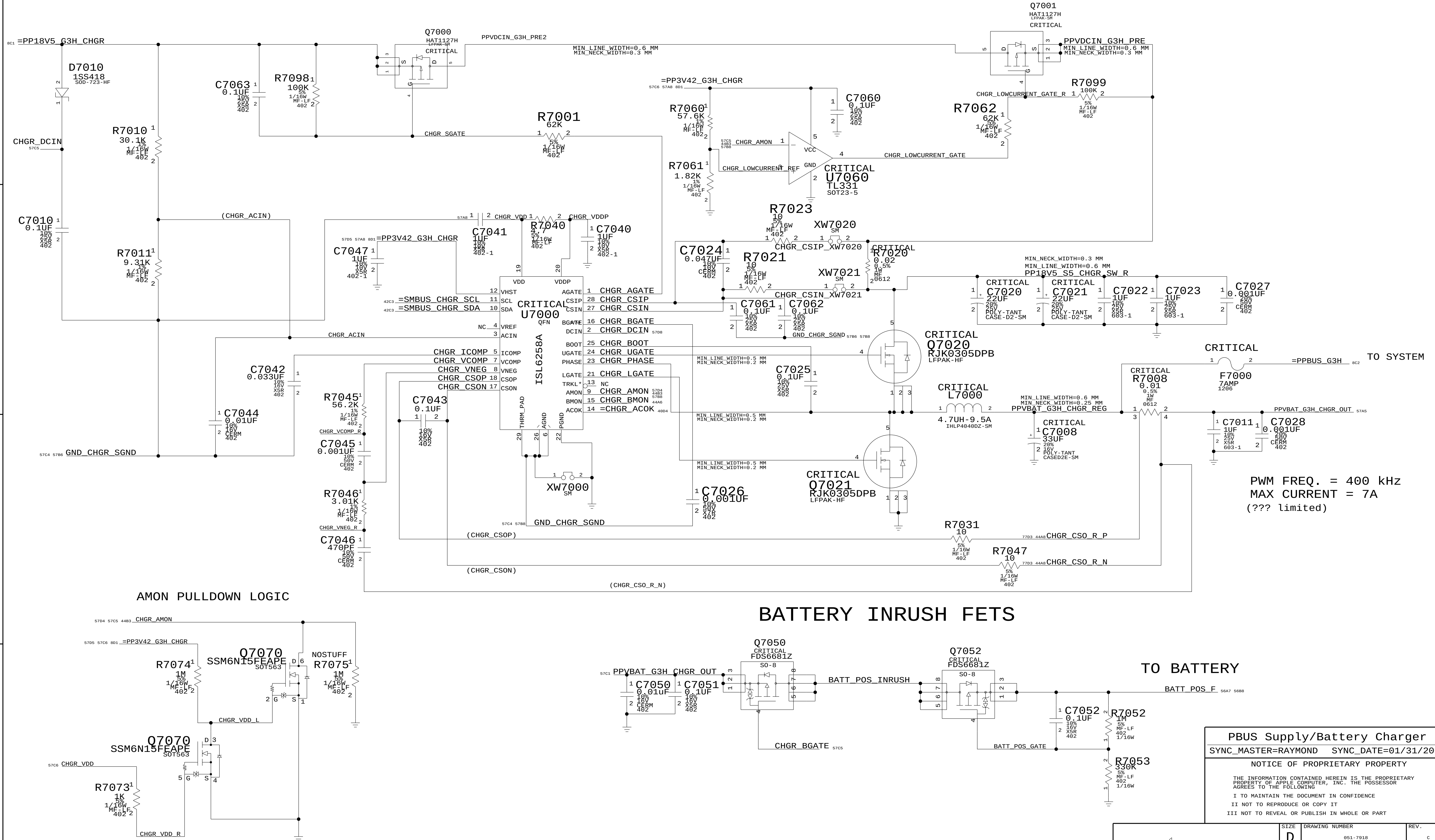
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE: NONE SHT 69 OF 109

PBUS SUPPLY / BATTERY CHARGER



=PP18V5_G3H_CHGR
D7010
1SS418
CHGR_DCIN
R7010
30.1K
C7010
0.1UF
R7011
9.31K
GND_CHGR_SGND
C7063
0.1UF
R7098
100K
Q7000
HAT1127H
CRITICAL
PPVDCIN_G3H_PRE2
CHGR_SGATE
R7001
62K
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.3 MM
Q7001
HAT1127H
CRITICAL
PPVDCIN_G3H_PRE
=PP3V42_G3H_CHGR
R7060
57.6K
C7060
0.1UF
R7061
1.82K
CHGR_AMON
CHGR_LOWCURRENT_REF
CRITICAL
U7060
TL331
CHGR_LOWCURRENT_GATE
R7062
62K
R7099
100K
CHGR_LOWCURRENT_GATE_R
(CHGR_ACIN)
CHGR_VDD
CHGR_VDDP
C7041
1UF
R7040
4.7
C7040
1UF
C7047
1UF
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
CRITICAL
U7000
ISL6258A
CHGR_AGATE
CHGR_CSIP
CHGR_CSIN
CHGR_BGATE
CHGR_DCIN
CHGR_BOOT
CHGR_UGATE
CHGR_PHASE
CHGR_LGATE
CHGR_AMON
CHGR_BMON
=CHGR_ACOK
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSOP
CHGR_CSON
CHGR_ACIN
C7042
0.033UF
C7044
0.01UF
R7045
56.2K
C7045
0.001UF
R7046
3.01K
C7046
470PF
C7043
0.1UF
XW7000
C7024
0.047UF
R7023
10
XW7020
R7021
10
XW7021
CHGR_CSIP_XW7020
CHGR_CSIN_XW7021
CRITICAL
R7020
0.02
C7061
0.1UF
C7062
0.1UF
GND_CHGR_SGND
CRITICAL
C7020
22UF
CRITICAL
C7021
22UF
C7022
1UF
C7023
1UF
C7027
0.001UF
PP18V5_S5_CHGR_SW_R
CRITICAL
Q7020
RJK0305DPB
C7025
0.1UF
CRITICAL
L7000
4.7UH-9.5A
PPVBAT_G3H_CHGR_REG
CRITICAL
C7008
33UF
CRITICAL
R7008
0.01
CRITICAL
F7000
7AMP
=PPBUS_G3H
TO SYSTEM
PPVBAT_G3H_CHGR_OUT
C7011
1UF
C7028
0.001UF
CRITICAL
Q7021
RJK0305DPB
C7026
0.001UF
R7031
10
CHGR_CSO_R_P
R7047
10
CHGR_CSO_R_N
(CHGR_CSOP)
(CHGR_CSON)
(CHGR_CSO_R_N)
PWM FREQ. = 400 kHz
MAX CURRENT = 7A
(??? limited)
AMON PULLDOWN LOGIC
CHGR_AMON
=PP3V42_G3H_CHGR
R7074
1M
Q7070
SSM6N15FEAPE
NOSTUFF
R7075
1M
CHGR_VDD_L
Q7070
SSM6N15FEAPE
CHGR_VDD
R7073
1K
CHGR_VDD_R
BATTERY INRUSH FETS
PPVBAT_G3H_CHGR_OUT
C7050
0.01uF
C7051
0.1UF
Q7050
CRITICAL
FDS6681Z
BATT_POS_INRUSH
Q7052
CRITICAL
FDS6681Z
CHGR_BGATE
TO BATTERY
BATT_POS_F
C7052
0.1UF
R7052
1M
BATT_POS_GATE
R7053
330K

PBUS Supply/Battery Charger

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

NOTICE OF PROPRIETARY PROPERTY

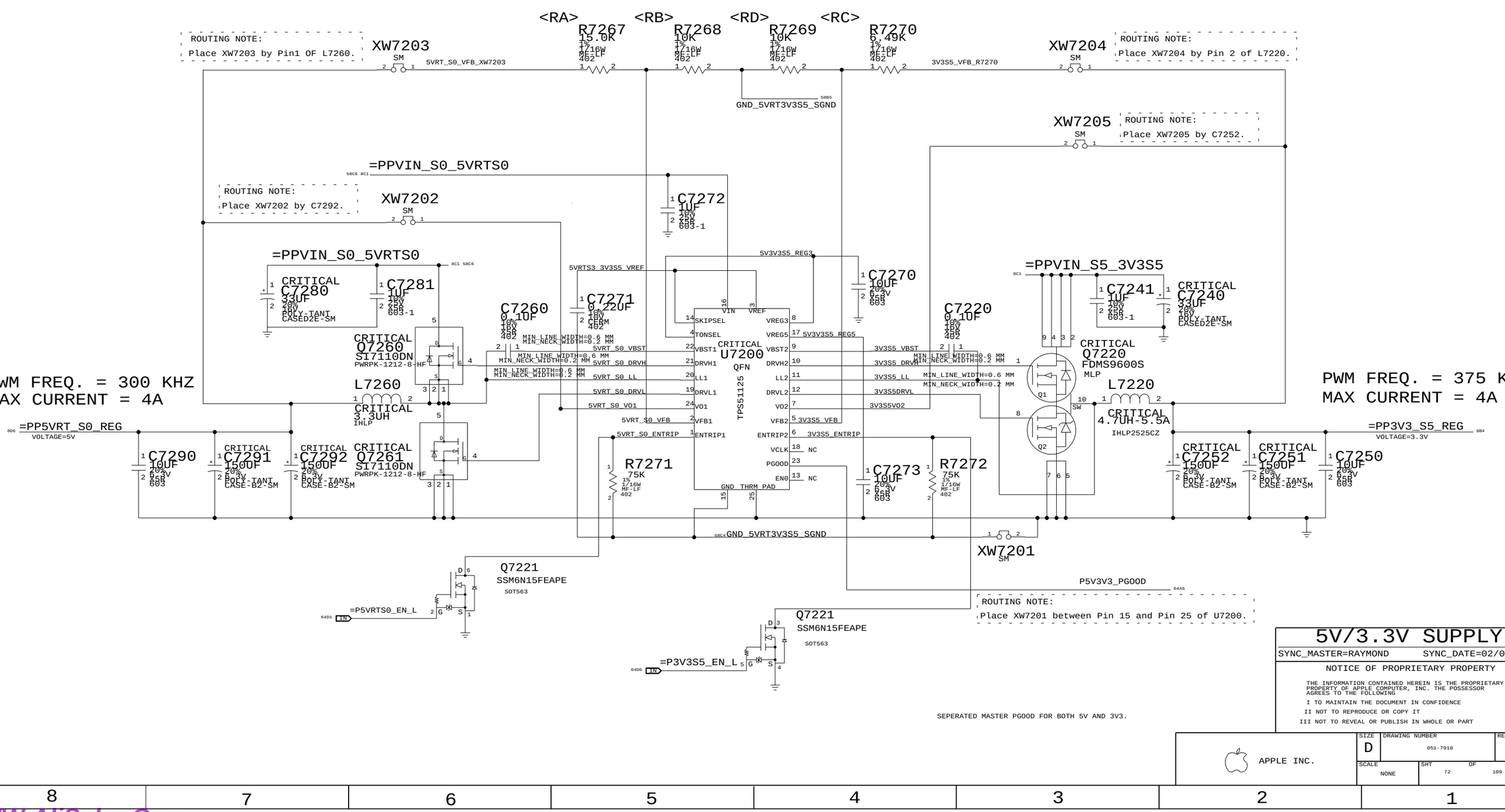
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE NONE	SHT 70	OF 109

5V_RT/3.3V POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



5V/3.3V SUPPLY

SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	72	109

1.5V/0.75V(DDR3) POWER SUPPLY

VOUT = 0.75V * (1 + RA / RB)

<RB> R7322 20K 0.1% 1/16W MF 402

<RA> R7321 20K 0.1% 1/16W MF 402

NO STUFF C7303 100PF 5% 50V CERM 402

=PPVTT_S3_DDR_BUF

C7340 0.033UF 10% 16V X5R 402

C7301 10UF 20% 6.3V X5R 603

1V5S3_V5FILT

C7300 1UF 10% 10V X5R 402-1

=PP5V_S3_1V5S30V75S0

R7307 4.7 5% 1/16W MF-LF 402

C7302 10UF 20% 6.3V X5R 603

=PP0V75_S0_REG

1V5S3_VTTSNS

1V5S3_VDDQSNS

XW7301 SM

ROUTING NOTE: Place XW7301 by L7320.

1V5S3_VBST

R7300 0 5% 1/16W MF-LF 402

=PPVIN_S5_1V5S30V75S0

R7310 10.7K 1% 1/16W MF-LF 402

VDDQSET VTTREF VLDOIN VTT V5FILT VBST V5IN VDDQSNS VTTSNS

=DDRVTT_EN

=DDRREG_EN

CRITICAL U7300 SYM (1 OF 2) TPS51116 QFN

PGOOD DRVH LL DRVL MODE NC0 NC1

1V5S3_VBST_RC

C7309 0.1UF 10% 10V X5R 402

CRITICAL Q7320 SI7110DN PWRPK-1212-8-HF

CRITICAL C7330 33UF 20% 16V POLY-TANT CASED2E-SM

CRITICAL C7331 33UF 20% 16V POLY-TANT CASED2E-SM

C7332 1UF 10% 25V X5R 603-1

C7333 0.001UF 10% 50V CERM 402

CRITICAL L7320 1.0UH-13A-5.6M-OHM SM-IHLP-1

MIN_LINE_WIDTH=1 mm MIN_NECK_WIDTH=0.25 mm

VOLTAGE=1.5V

CRITICAL Q7321 SI7108DN PWRPK-1212-8-HF

CRITICAL C7342 330UF 20% 2.5V POLY-TANT CASE-D2E-SM

C7341 10UF 20% 6.3V X5R 603

MAX CURRENT = 12A

PWM FREQ. = 400 KHZ

PUT ONE BULK CAP NEXT TO THE LOAD

=PP1V5_S3_REG

CRITICAL C7343 330UF 20% 2.5V POLY-TANT CASE-C2-SM1

C7344 0.001UF 10% 50V CERM 402

XW7303 SM

1V5S3_CS

ROUTING NOTE: Place XW7303 by C7308.

ROUTING NOTE: CONNECT CS GND TO Q7321 PIN1,2,3 USING KEVIN CONNECTION.

CRITICAL C7307 22UF 20% 6.3V X5R-CERM 603

CRITICAL C7308 22UF 20% 6.3V X5R-CERM 603

THRM_PAD CS_GND GND PGND VTTGND

ROUTING NOTE: PUT 6 VIAS UNDER THE THERMAL PAD

GND_1V5S3_SGND

XW7300 SM

ROUTING NOTE: Place XW7300 between Pin 9 and Pin 25 of U7300.

GND_1V5S3_CSGND

XW7302 SM

ROUTING NOTE: Place XW7302 by Q7321.

DDRREG_PGOOD

R7399 100K 5% 1/16W MF-LF 402

=PP3V3_S3_PDCISENS

STATE	PM_SLP_S4_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3HOT	LOW	LOW	0.0V	0.0V

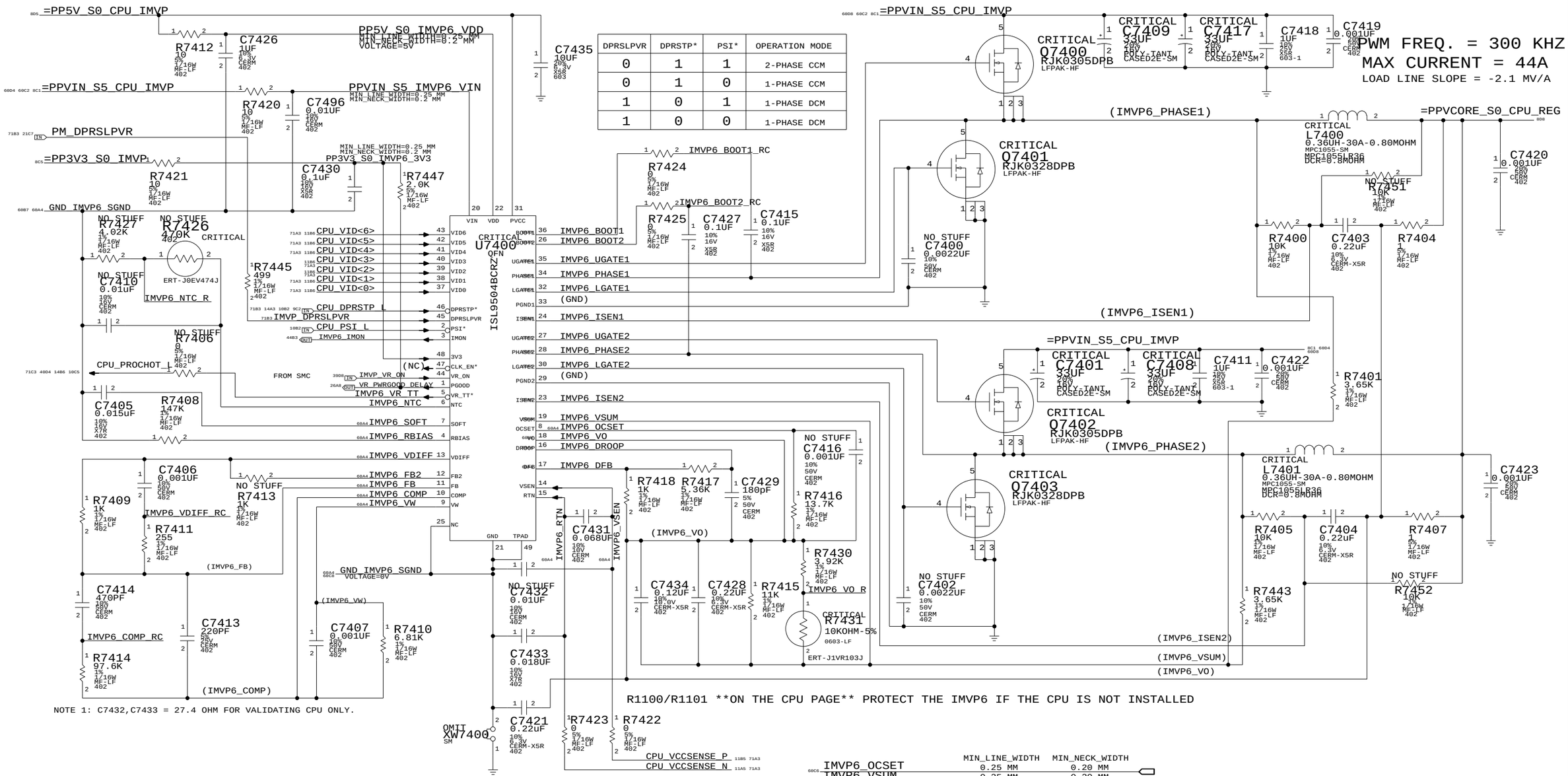
1.5V/0.75V DDR3 SUPPLY

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE NONE SHT 73 OF 109



IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

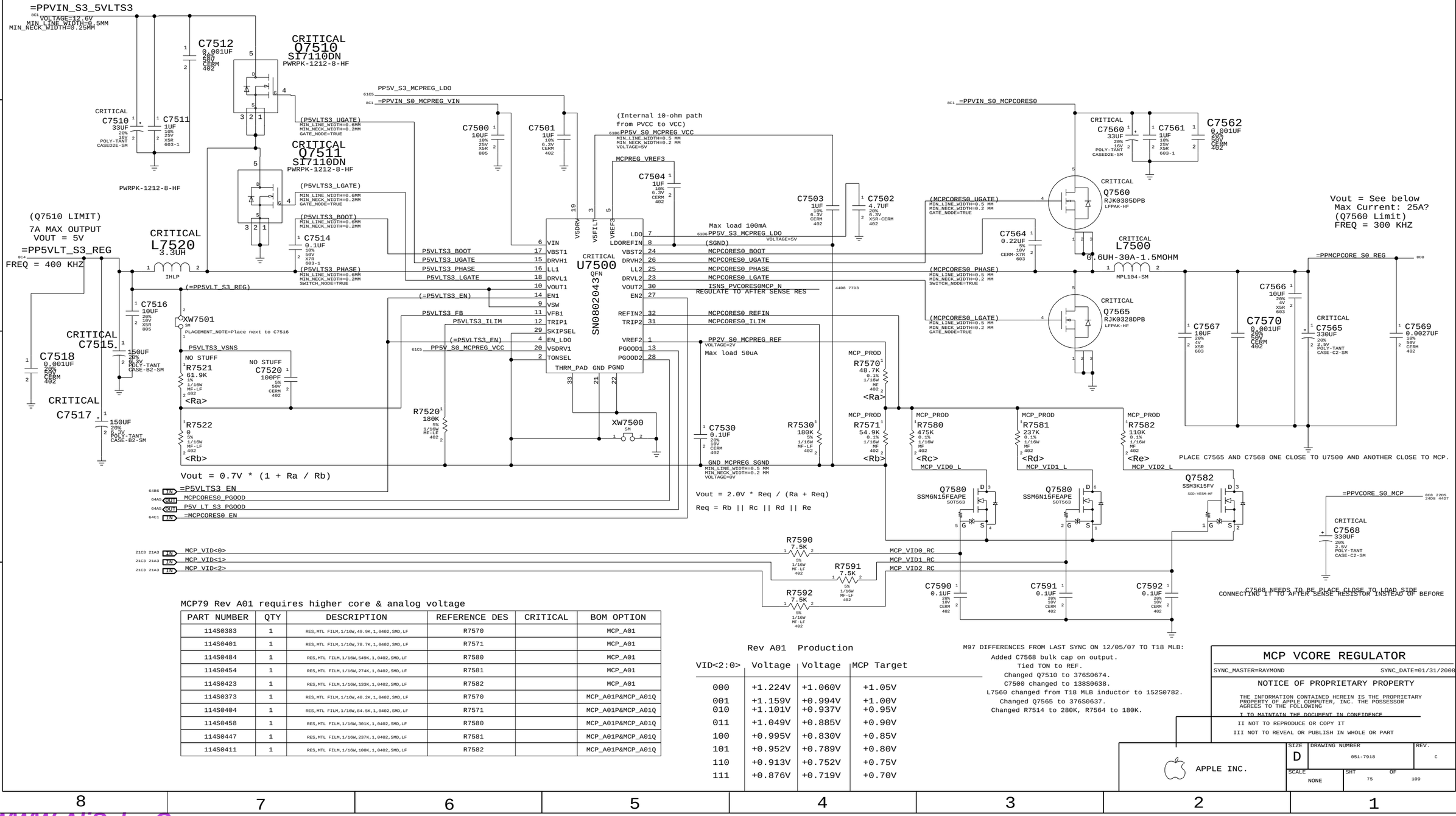
SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	74	109

MCP VCORE/5V_S3 LEFT REGULATOR



MCP79 Rev A01 requires higher core & analog voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0383	1	RES,MTL FILM,1/16W,49.9K,1,0402,SMD,LF	R7570		MCP_A01
114S0401	1	RES,MTL FILM,1/16W,78.7K,1,0402,SMD,LF	R7571		MCP_A01
114S0484	1	RES,MTL FILM,1/16W,549K,1,0402,SMD,LF	R7580		MCP_A01
114S0454	1	RES,MTL FILM,1/16W,274K,1,0402,SMD,LF	R7581		MCP_A01
114S0423	1	RES,MTL FILM,1/16W,133K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES,MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01P&MCP_A01Q
114S0404	1	RES,MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01P&MCP_A01Q
114S0458	1	RES,MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01P&MCP_A01Q
114S0447	1	RES,MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01P&MCP_A01Q
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01P&MCP_A01Q

Rev A01 Production

VID<2:0>	Voltage	Voltage	MCP Target
000	+1.224V	+1.060V	+1.05V
001	+1.159V	+0.994V	+1.00V
010	+1.101V	+0.937V	+0.95V
011	+1.049V	+0.885V	+0.90V
100	+0.995V	+0.830V	+0.85V
101	+0.952V	+0.789V	+0.80V
110	+0.913V	+0.752V	+0.75V
111	+0.876V	+0.719V	+0.70V

M97 DIFFERENCES FROM LAST SYNC ON 12/05/07 TO T18 MLB:
Added C7568 bulk cap on output.
Tied TON to REF.
Changed Q7510 to 376S0674.
C7500 changed to 138S0638.
L7560 changed from T18 MLB inductor to 152S0782.
Changed Q7565 to 376S0637.
Changed R7514 to 280K, R7564 to 180K.

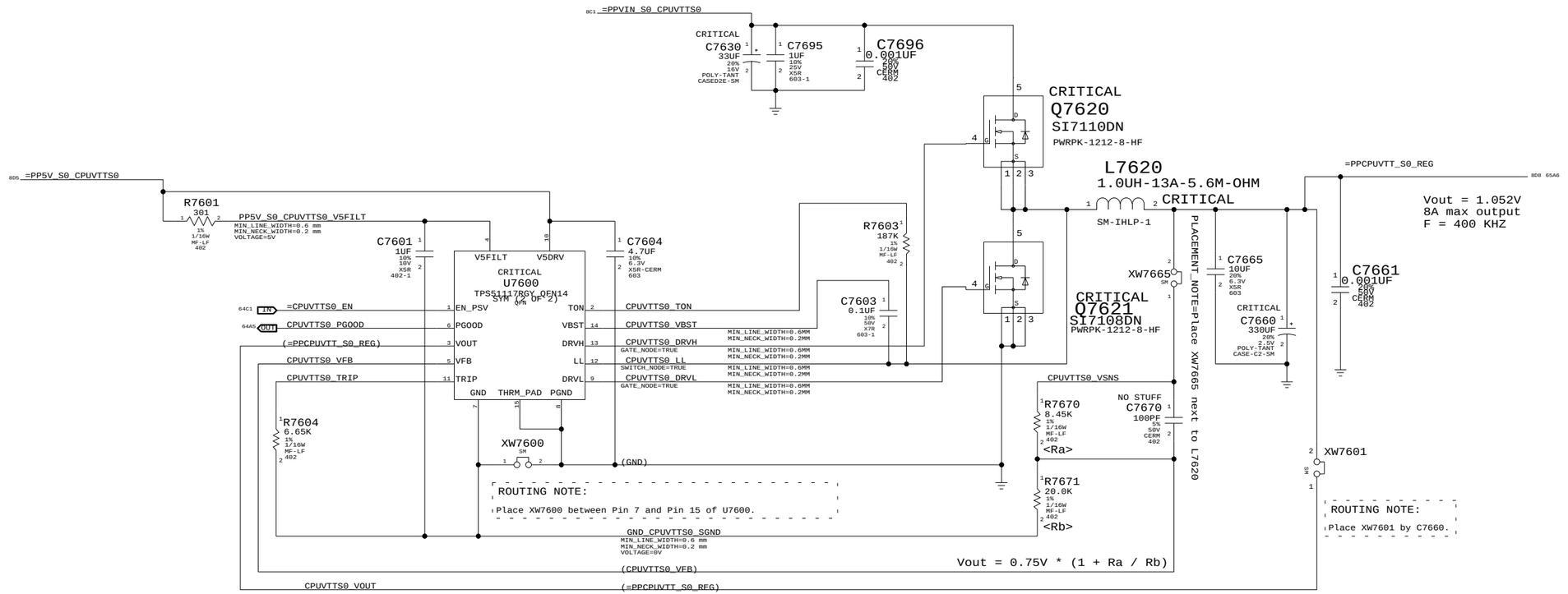
MCP VCORE REGULATOR

SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 75 OF 109	

CPUVTT POWER SUPPLY



CPU VTT(1.05V) SUPPLY

SYNC_MASTER=RAYMOND SYNC_DATE=02/08/2008

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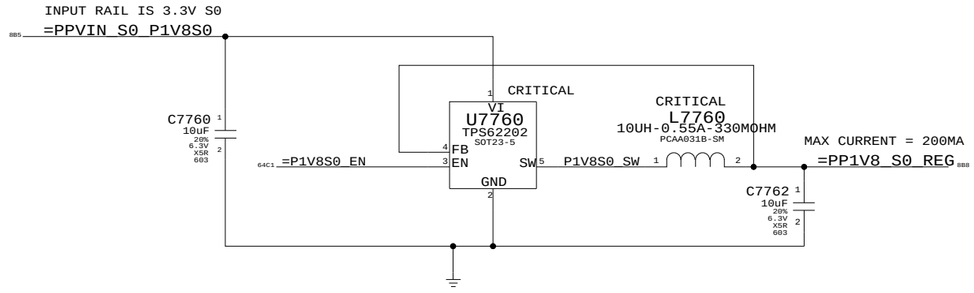
APPLE INC.

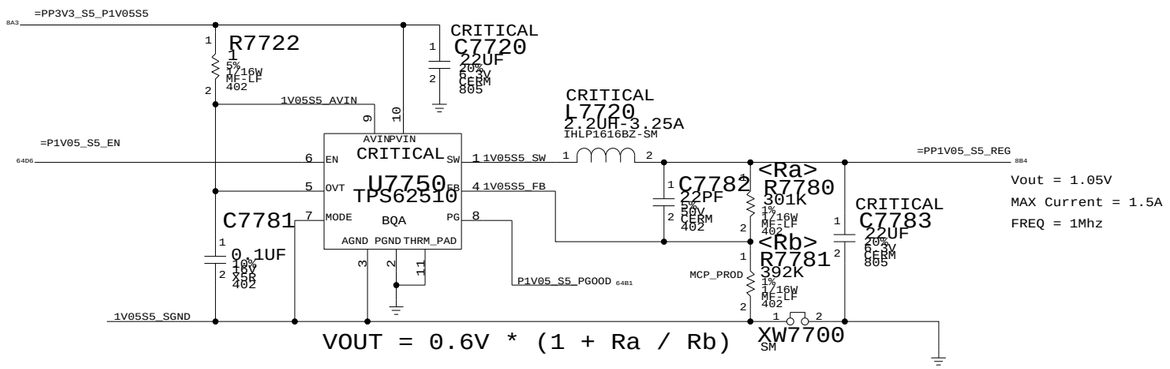
SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	76	109

1.8V S0 SWITCHER



MCP 1.05V_S5 AUXC SUPPLY



MCP79 Rev A01 requires higher voltage

	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
VOUT = 1.102V	114S0464	1	RES,MTL FILM,1/16W,348K,1%,0402,SMD,LF	R7781	MCP_A01&MCP_A01P&MCP_A01Q	

MISC POWER SUPPLIES

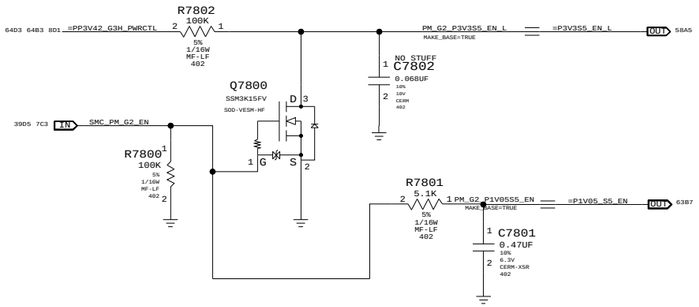
SYNC_MASTER=RAYMOND SYNC_DATE=01/23/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	77	109

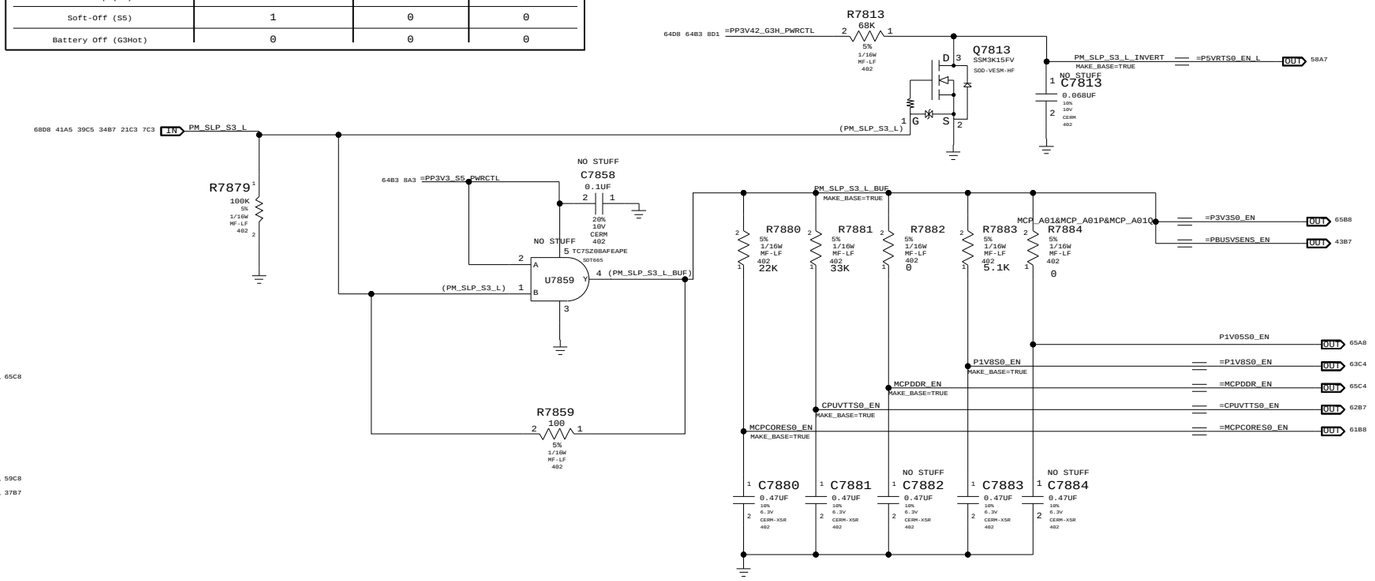
3.3V 1.05V S5 ENABLE



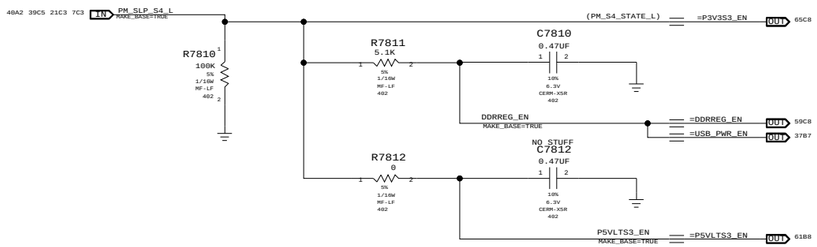
Power Control Signals

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

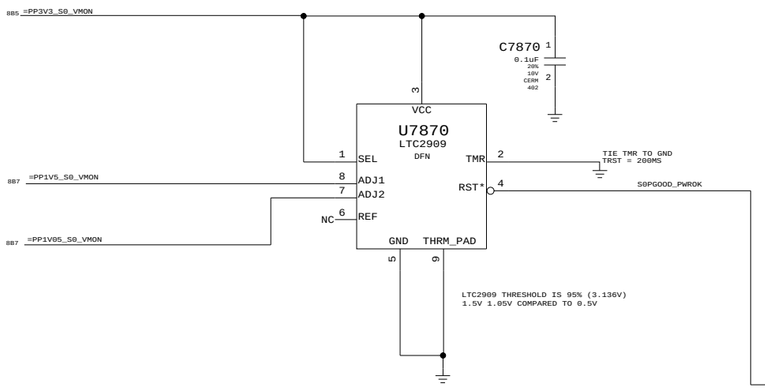
3.3V_S0, 1.8V_S0 ENABLE
MCPDDR, CPUVTT,MCPCORES0 ENABLE
1.5V S0 AND 1.05V S0 ENABLE



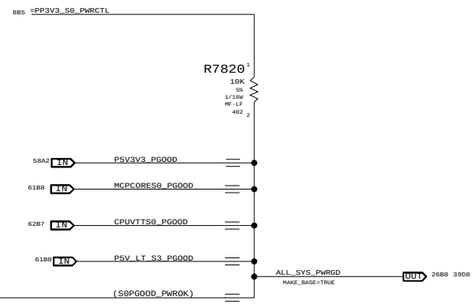
S3 ENABLE



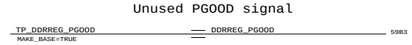
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT



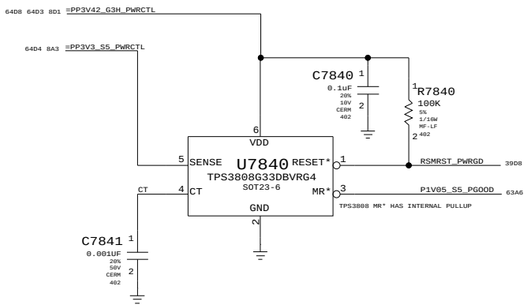
OTHER S0 RAILS PGOOD



Unused PGOOD signal



VOLTAGE MONITOR



POWER SEQUENCING

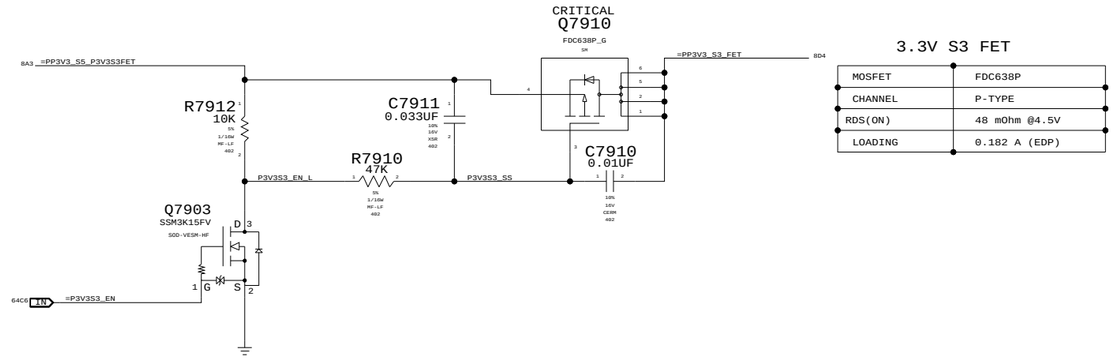
SYNC_MASTER=YUAN.MA SYNC_DATE=04/22/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE: NONE SHT 78 OF 109

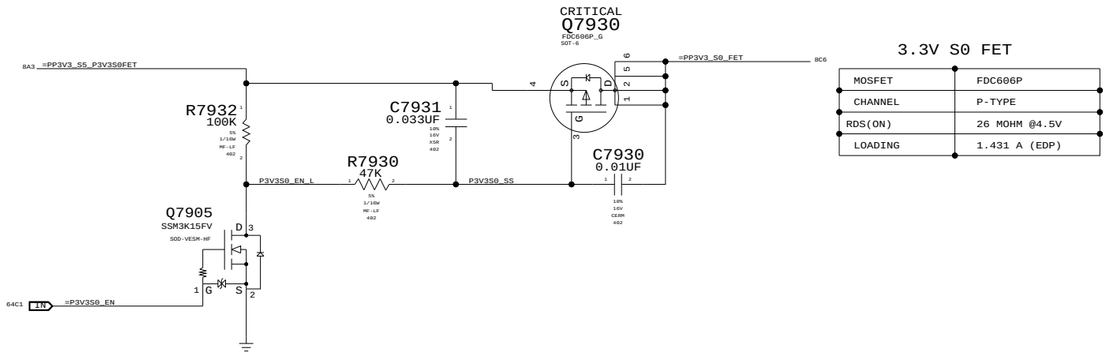
3.3V S3 FET



3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

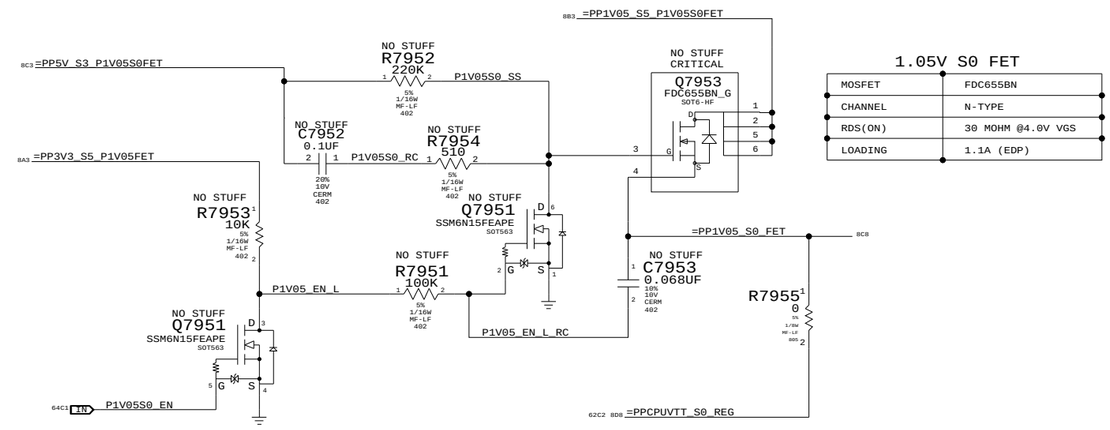
3.3V S0 FET



3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

1.05V S0 FET

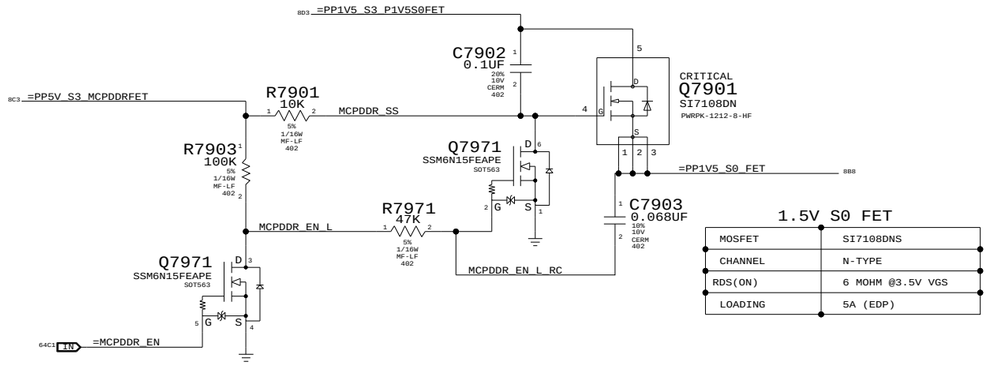


1.05V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	30 MOHM @4.0V VGS
LOADING	1.1A (EDP)

1.5V S0 FET

(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)

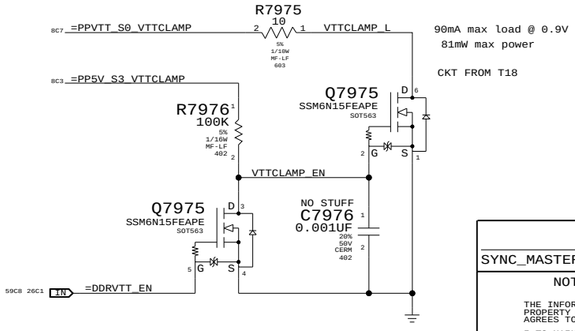


1.5V S0 FET

MOSFET	SI7108DNS
CHANNEL	N-TYPE
RDS(ON)	6 MOHM @3.5V VGS
LOADING	5A (EDP)

MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



POWER FETS

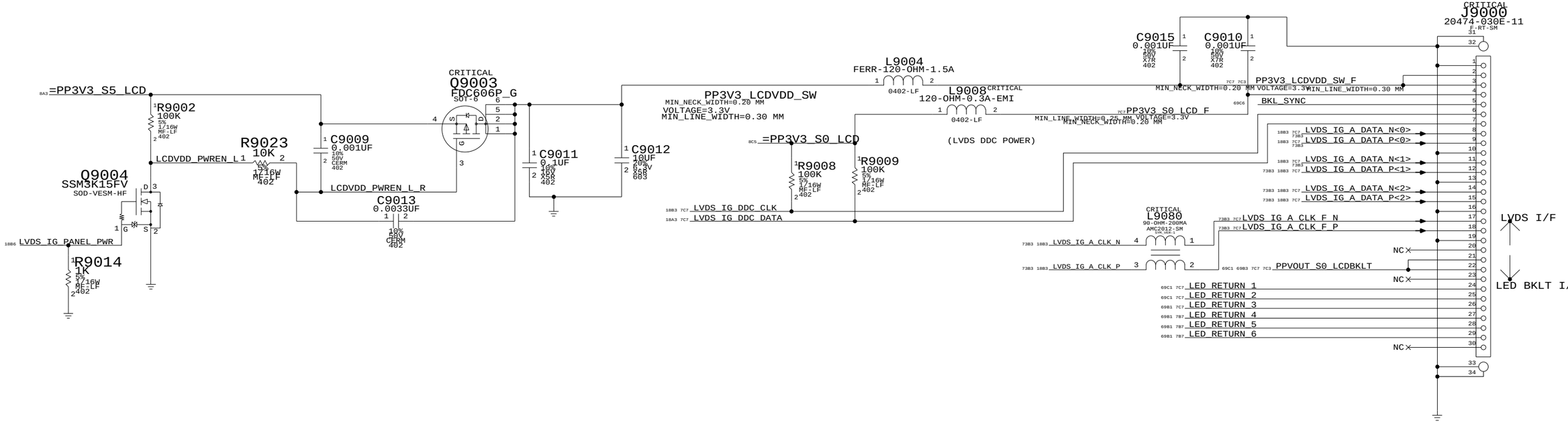
SYNC_MASTER=YUAN.MA SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE	SHT	OF
NONE	79	109

LCD CONNECTOR

LVDS CONNECTOR:518S0650

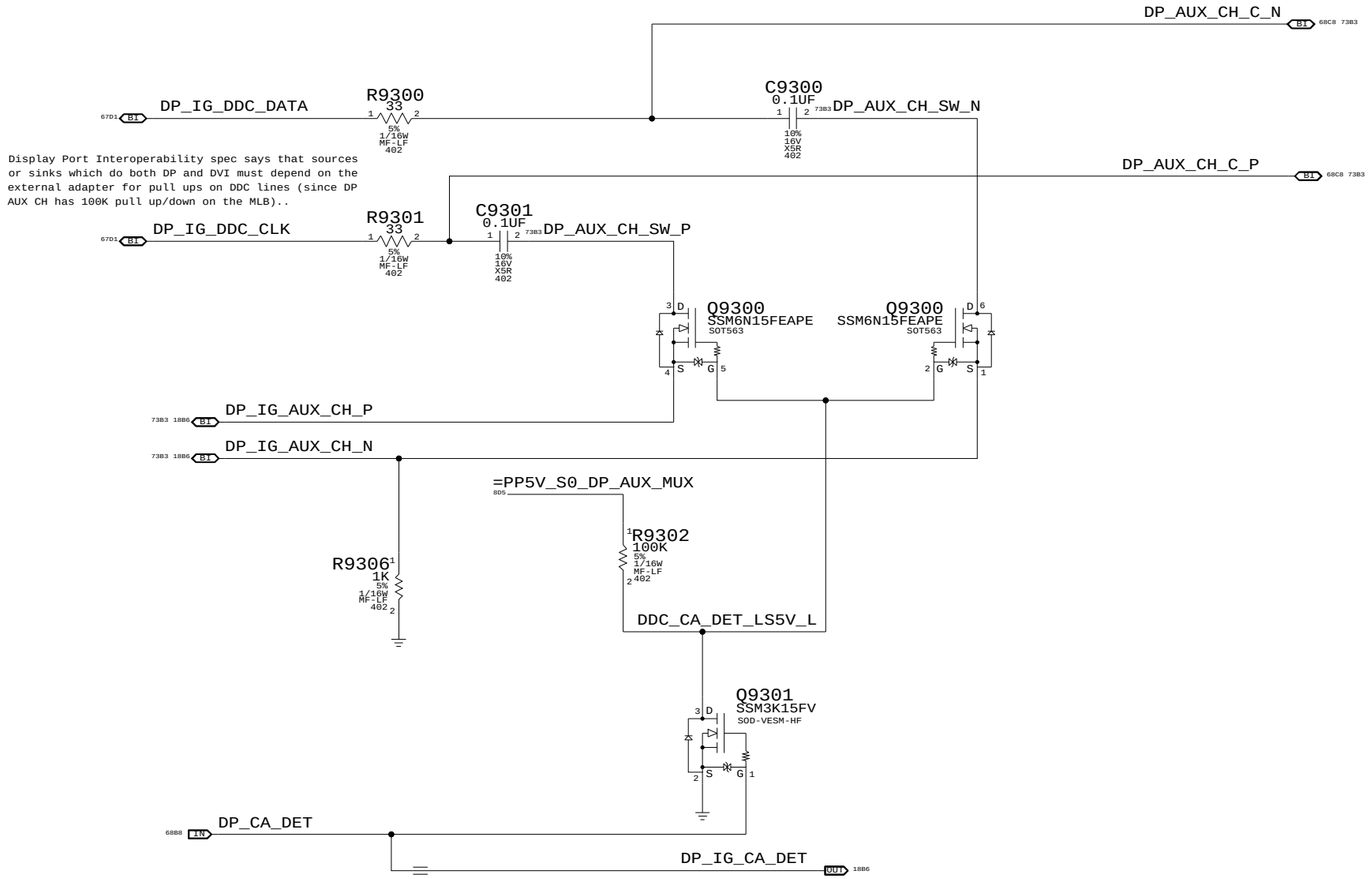


LVDS CONNECTOR

SYNC_MASTER=NMARSTON SYNC_DATE=04/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 90 OF 109	



=MCP_HDMI_TXC_P — DP_ML_P<3> — MAKE_BASE=TRUE
=MCP_HDMI_TXC_N — DP_ML_N<3> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_P<0> — DP_ML_P<2> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_N<0> — DP_ML_N<2> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_P<1> — DP_ML_P<1> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_N<1> — DP_ML_N<1> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_P<2> — DP_ML_P<0> — MAKE_BASE=TRUE
=MCP_HDMI_TXD_N<2> — DP_ML_N<0> — MAKE_BASE=TRUE
=MCP_HDMI_HPD — DP_HPD — MAKE_BASE=TRUE
=MCP_HDMI_DDC_CLK — DP_IG_DDC_CLK — MAKE_BASE=TRUE
=MCP_HDMI_DDC_DATA — DP_IG_DDC_DATA — MAKE_BASE=TRUE

DISPLAYPORT SUPPORT

SYNC_MASTER=AMASON SYNC_DATE=04/18/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	93	109

Port Power Switch

CRITICAL
U9480
TPS2051B
SOT23
=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
IN
OUT
OC*
EN
GND
TP_DPPWR_OC_L
PP3V3_S0_DPILIM
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
L9400
FERR-120-OHM-3A
0603
PP3V3_S0_DPPWR
C9400
0.01UF
C9480
10UF
C9481
0.1UF
NO STUFF
C9485
10UF
CRITICAL
C9486
22UF
R9420
100K
HDMI_CEC
R9425
1M
R9403
R9413
FL9403
12-OHM-100MA
TCM1210-4SM
DP_ML_P<3>
DP_ML_N<3>
C9414
C9415
0.1UF
DP_AUX_CH_C_P
DP_AUX_CH_C_N
=PP3V3_S0_DPCONN
R9443
R9442
100K
DP_CA_DET
Q9440
2N7002DW-X-G
SOT-363
DP_CA_DET_L_Q
Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm
R9422
1M
DP to DVI/HDMI
Cable Adapter
(CA) has 100k
pull-up to DP_PWR.
R9445
R9444
10K
DP_HPD
R9446
100K
MCP79 requires pull
down HPD input with
100K if DP_HPD is used.
Q9441
DP_HPD_L_Q
DP_HPD_Q
R9423
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).
CRITICAL
J9400
DSPLYPRT-M97-1
F-RT-THSM
BOT ROW
TH PINS
TOP ROW
SM PINS
HOT_PLUG_DETECT
CONFIG1
CONFIG2
GND
ML_LANE3P
ML_LANE3N
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
ML_LANE1P
ML_LANE1N
ML_LANE2P
ML_LANE2N
RETURN
SHIELD PINS
514-0637
DP_ESD
CRITICAL
D9411
RCLAMP0524P
SLP2510P8
D9421
D9400
RCLAMP0504F
SC70-6-1
DP_ESD
CRITICAL
D9410
RCLAMP0524P
SLP2510P8
R9401
R9431
R9400
R9430
FL9400
FL9401
FL9402
DP_ML_C_P<0>
DP_ML_C_N<0>
DP_ML_C_P<1>
DP_ML_C_N<1>
DP_ML_C_P<2>
DP_ML_C_N<2>
C9410
C9411
C9412
C9413
C9416
C9417
R9402
R9432
NO STUFF
5% 1/16W MF-LF 402
0.1UF
10% 16V X5R 402

DisplayPort Connector

SYNC_MASTER=AMASON
SYNC_DATE=06/30/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 94 OF 109	

*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
*BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.

PPBUS_S0_LCDBKLT_PWR
R9730 0 5% 1/16W MF-LF 402
PPVIN_S0_LCDBKLT_BUF
CRITICAL L9701 22UH-2.5A IHLP2525CZ-SM
PPVOUT_S0_LCDBKLT_SW
R9701 100 1% 1/16W MF-LF 402
CRITICAL C9701 10UF 10% 25V X5R 805
PLACEMENT_NOTE=Place near L9701
PLACEMENT_NOTE=Place near Q9701
PLACEMENT_NOTE=Place near PPVOUT_S0_LCDBKLT_SW
BKL_VIN
C9702 0.1UF 10% 25V X5R 402
XW9701 SM
GND_BKL_PWRGND
PLACEMENT_NOTE=Place near C9701
MIN_NECK_WIDTH=0.20MM MIN_LINE_WIDTH=0.5MM
D9701 PDWER01-123 DFLS1100 CRITICAL
PLACEMENT_NOTE=Place near Q9701
PLACEMENT_NOTE=Place near C9710
PLACEMENT_NOTE=Place near J9000
Q9701 FDC5612 SSOT6
BOOST_FET_CNTL
MIN_NECK_WIDTH=0.20MM MIN_LINE_WIDTH=0.6MM
CRITICAL C9709 4.7UF 10% 50V X7R-CERM 1206
CRITICAL C9710 4.7UF 10% 50V X7R-CERM 1206
PLACEMENT_NOTE=Place near C9709
MIN_NECK_WIDTH=0.20MM MIN_LINE_WIDTH=0.5MM
BOOST_SINK
GND_BKL_PWRGND
PLACEMENT_NOTE=Place near C9709 and Q9701
R9704 100 1% 1/16W MF-LF 402
R9702 0.4 1% 1/16W MF 402
R9715 0.4 1% 1/16W MF 402
XW9702 SM
GND_BKL_PWRGND_X
MIN_NECK_WIDTH=0.20MM MIN_LINE_WIDTH=0.5MM
PLACEMENT_NOTE=Place near C9709 and Q9701
*R9702 AND R9715 PIN 1 SHOULD BE PLACED NEAR C9709 PIN 2
C9712 47PF 5% 50V CERM 402 NOSTUFF
PPVOUT_S0_LCDBKLT
VOLTAGE=30V MIN_NECK_WIDTH=0.20 mm MIN_LINE_WIDTH=0.5 mm

BKL_VREF_4V9
R9731 187K 1% 1/16W MF-LF 402
PPBUS_S0_LCDBKLT_PWR
BKLT_EN
BKL_SYNC
BKLT_PLL
R9734 0 5% 1/16W MF-LF 402
BKL_VSYNC
R9707 3.01K 1% 1/16W MF-LF 402
C9703 1UF 10% 10V X5R 402-1
C9713 0.1UF 10% 25V X5R 402
R9705 100K 1% 1/16W MF-LF 402
R9706 10K 5% 1/16W MF-LF 402
PLACEMENT_NOTE=Away from Q9701
U9701 APP001A QFN
VIN
VREF ENA VSYNC ISET RT SSTCMP DIM LPF LRT GNDA THRM_PAD
DRV ISWSEN ISEN1 ISEN2 ISEN3 ISEN4 ISEN5 ISEN6 VSEN
BKL_ISET
BKL_RT
BKL_SSTCMP
BKL_DIM
BKL_LPF
BKL_LRT
CRITICAL
BKL_ISEN1 BKL_ISEN2 BKL_ISEN3 BKL_ISEN4 BKL_ISEN5 BKL_ISEN6
R9717 0 5% 1/16W MF-LF 402
LED_RETURN_1
R9718 0 5% 1/16W MF-LF 402
LED_RETURN_2
R9719 0 5% 1/16W MF-LF 402
LED_RETURN_3
R9720 0 5% 1/16W MF-LF 402
LED_RETURN_4
R9721 0 5% 1/16W MF-LF 402
LED_RETURN_5
R9722 0 5% 1/16W MF-LF 402
LED_RETURN_6
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.20 mm

PLACEMENT_NOTE=Away from Q9701
R9708 100K 1% 1/16W MF-LF 402
R9709 1K 1% 1/16W MF-LF 402
R9703 2.0M 5% 1/16W MF-LF 402 NOSTUFF
BKL_SSTCMP_RC
C9705 0.1UF 20% 10V CERM 402
BKLT_PWM_RC
R9733 0 5% 1/16W MF-LF 402
C9706 0.0022UF 10% 50V CERM 402 NOSTUFF
C9714 1UF 10% 10V X5R 402 NOSTUFF
BKL_VREF_4V9
R9713 0 5% 1/16W MF-LF 402
PLACEMENT_NOTE=Away from Q9701
BKLT_PLL_NOT
BKLT_PLL
R9714 10K 5% 1/16W MF-LF 402
C9707 2.2UF 20% 6.3V CERM 402-LF
BKLT_PLL
BKL_LRT_RC
C9708 0.1UF 10% 25V X5R 402
R9727 15.0K 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Away from Q9701
GND_BKL_PWRGND
PPVOUT_S0_LCDBKLT
R9723 1.2M 1% 1/16W MF-LF 603
R9724 71.5K 1% 1/16W MF-LF 402
BKL_VSEN

CRITICAL Q9702 NTUD3127CXXG SOT-963 P-CHN
BKL_VREF_4V9
BKL_VREF_IN_4V9
R9700 100K 1% 1/16W MF-LF 402
R9710 10K 1% 1/16W MF-LF 402
BKL_PWR_EN_L
CRITICAL Q9702 NTUD3127CXXG SOT-963 N-CHN
LVDS_IG_BKL_PWM
R9711 30.1K 1% 1/16W MF-LF 402

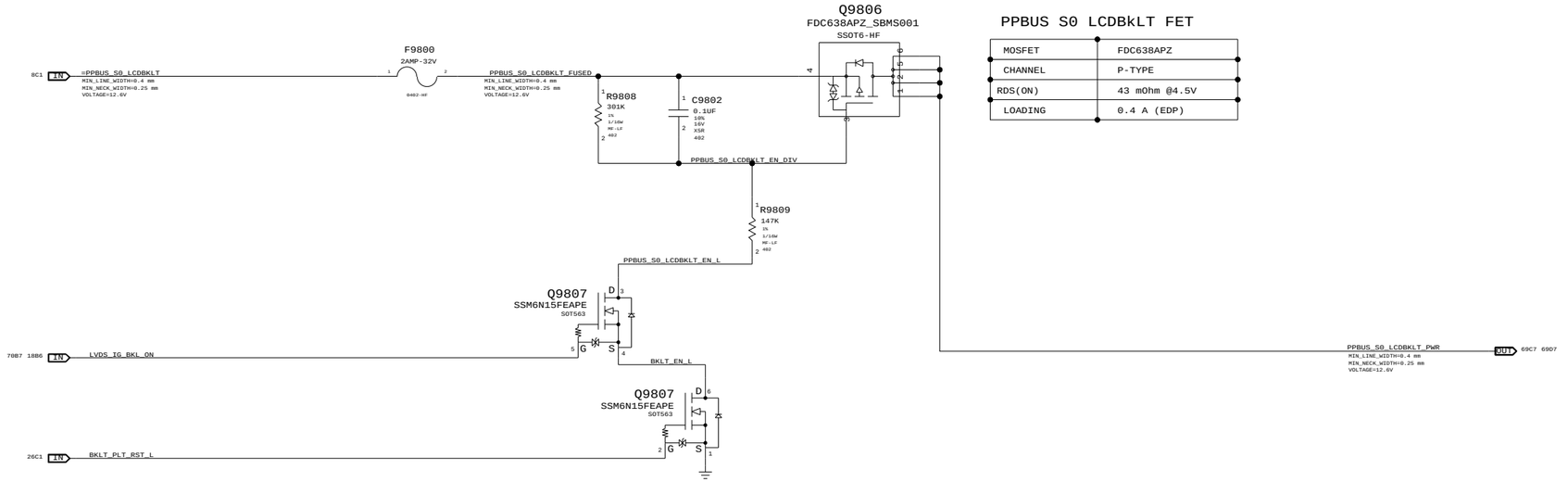
*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

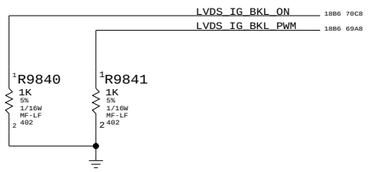
LCD BACKLIGHT DRIVER

SYNC_MASTER=YITE
SYNC_DATE=08/12/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 97 OF 109	





LCD Backlight Support

SYNC_MASTER=YITE SYNC_DATE=06/30/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 98 OF 109	

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SR DG recommends at least 25 mils, >50 mils preferred

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	10C4 14D3
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	10C4 14D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	10C4 14D6
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	10C4 14D6
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	10B4 10C4 14C3 14D3
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	10B4 14D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	10B4 14D6
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	10B4 14D6
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	10C2 14B3 14C3
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	10C2 14D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	10C2 14D6
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	10C2 14D6
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	10B2 10C2 14B3
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	10B2 14D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	10B2 14D6
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	10B2 14D6
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	10D8 14C6 14D6
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10D8 14B6
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	10D8 14B6
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	10C8 10D8 14C6
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	10C8 14B6
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	10D6 14B6
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9B2 10D6 14B6
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10D6 14B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10D6 14B3
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	10D6 14B6
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	10D6 14B6
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9B2 10D6 13C2 14A3
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10D6 14A6
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10D6 14B6
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10C8 14A3
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9C2 10B4
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10C8 14B7
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10C8 14A3
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10D6 14A3
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9B2 10C8 14A3
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9B2 10B8 14A3
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10C5 14B6 40D4 60C8
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10B2 13C7 14A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10B8 14A3
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10C8 14A3
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10C6 14B7 40C4
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10B2 14A3
	CPU_EFOM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10B2 14A3
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9C2 10B2 14A3 60C7
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10B2 14A3
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14A6
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14A6
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10B6 14B3
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10B6 14B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13C3 14B3
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13C3 14B3
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14A4
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14A4
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10D6
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21C7 60D8
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	60C7
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10B4 27B1
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10B3
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10B3
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10B3
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6C6 10B6 10C6 13B3
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6C4 10B6 10C6
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6C6 6C7 10B6 10C6 13B3
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6C7 6D6 10A6 10C6 13B6
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6C6 6C7 10A6 10C6 13B3
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10C6 13C6
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10C5 13C6
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13C4
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	11B6 60C7
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11B5 60A5
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11A5 60A5
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

CPU/FSB Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 100 OF 109	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15B5 28C5 28C7
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15B5 28C5 28C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15A5 28D5 28D7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15B5 28C5 28C7
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15B5 28C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15B5 15C5 28C5 28C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15C5 28C5 28C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15C5 28C5
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15C5 28C7
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15C5 28C7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15B7 28C2 28C4 28D2 28D4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15B7 28C2 28C4
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15B7 15C7 28B2 28B4 28C2 28C4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15C7 28C2 28C4
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15C7 28B5 28B7 28C5 28C7
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15C7 15D7 28B5 28B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15D7 28B5 28B7
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15D7 28A5 28A7 28B5 28B7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15A7 28C4
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15A7 28C2
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15B7 28B4
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15B7 28C2
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15B7 28B5
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15B7 28B7
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15B7 28B5
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15B7 28A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15D5 28C2
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15D5 28D2
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15D5 28C4
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15D5 28C4
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15D5 28B2
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15D5 28C2
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15D5 28C4
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15D5 28C4
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15D5 28B7
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15D5 28B7
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15D5 28B5
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15D5 28B5
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15D5 28B7
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15D5 28B7
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15D5 28A5
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15D5 28A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15B1 29C5 29C7
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15B1 29C5 29C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15A1 29D5 29D7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15B1 29C5 29C7
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15B1 29C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15B1 15C1 29C5 29C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15C1 29C5 29C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15C1 29C5
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15C1 29C7
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15C1 29C7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15B3 29C2 29C4 29D2 29D4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15B3 29C2 29C4
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15B3 15C3 29C2 29C4
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15C3 29B2 29B4 29C2 29C4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15C3 29B5 29B7 29C5 29C7
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15C3 15D3 29B5 29B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15D3 29B5 29B7
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15D3 29A5 29A7 29B5 29B7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15A3 29C4
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15A3 29C2
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15B3 29C2
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15B3 29B4
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15B3 29B5
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15B3 29B7
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15B3 29B5
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15B3 29A7
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15D1 29C2
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15D1 29D2
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15D1 29C4
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15D1 29C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15D1 29C4
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15D1 29C4
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15D1 29B2
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15D1 29C2
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15D1 29B7
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15D1 29B7
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15D1 29B5
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15D1 29B5
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15D1 29B7
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15D1 29B7
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15D1 29A5
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15D1 29A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16C6
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16C6

Memory Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE: NONE SHT: 101 OF 109

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7D5 31C7
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7D5 31C7
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17B3 31C5
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17B3 31C5
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7D5 17B6 31C7
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7D5 17B6 31C7
	PCIE_90D	PCIE	PCIE_FC_R2D_P	32C5
	PCIE_90D	PCIE	PCIE_FC_R2D_N	32C5
PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	9B5 32C6
	PCIE_90D	PCIE	PCIE_FC_R2D_C_N	9B5 32C6
PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	9B5 32C5
	PCIE_90D	PCIE	PCIE_FC_D2R_N	9B5 32C5
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17C3 31C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17C3 31C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7D5 31C7
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7D5 31C7
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	9C5 32C5
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	9C5 32C5
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17A6
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	67D1 68C1 68C8
	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	68C2 68C7
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	67D1 68C1 68C8
	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	68C2 68C7
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18B6 67C7
	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18B6 67C7
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	67C6
	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	67C5
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	67C4 68C8
	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	67D4 68C8
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18A6 25C7
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18A6 25C7
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18B3 66B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	7C7 66C2
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18B3 66B3
	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	7C7 66C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	7C7 18B3 66C2
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	7C7 18B3 66C2
I102 DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	68C3 68C4 68C5
I102	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	68C3 68C4 68C5
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18A3 25C6
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18A3 25C6
SATA_HDD_R2D	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_P	20D6 36A3
	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_N	20D6 36A3
	SATA_100D_HDD	SATA	SATA_HDD_R2D_P	7C5 36A7
	SATA_100D_HDD	SATA	SATA_HDD_R2D_N	7C5 36A7
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_P	36A5
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_N	36A5
SATA_HDD_D2R	SATA_100D_HDD	SATA	SATA_HDD_D2R_P	20D6 36A3
	SATA_100D_HDD	SATA	SATA_HDD_D2R_N	20D6 36A3
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_P	7C5 36A7
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_N	7C5 36A7
	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_P	36A5
	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_N	36A5
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20D6 36C2
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20D6 36C2
	SATA_100D	SATA	SATA_ODD_R2D_P	7B7 36C5
	SATA_100D	SATA	SATA_ODD_R2D_N	7B7 7C5 36C5
	SATA_100D	SATA	SATA_ODD_R2D_UF_P	36C4
	SATA_100D	SATA	SATA_ODD_R2D_UF_N	36C4
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20D6 36B2
	SATA_100D	SATA	SATA_ODD_D2R_N	20D6 36B2
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7B7 36B5
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7B7 36B5
	SATA_100D	SATA	SATA_ODD_D2R_UF_P	36B4
	SATA_100D	SATA	SATA_ODD_D2R_UF_N	36B4
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20A6

MCP Constraints 1

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE NONE SHT 102 OF 109

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0> 13C3 19D7
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI	PCI_AD<24>
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>
PCI_AD	PCI_55S	PCI	PCI_PAR
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L 19D2 19D7
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 19D2 19D7
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R 19C5
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP 19C5
LPC_AD	LPC_55S	LPC	LPC_AD<3..0> 19B3 39C8 41D3 41D5
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L 19C3 39C8 41D5
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L 19C3 26D4
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 19B3 26C4
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 26C1 39C8
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 26B1 41D3
USB_EXTA	USB_90D	USB	USB_EXTA_P 20D3 37A8
	USB_90D	USB	USB_EXTA_N 20D3 37A8
	USB_90D	USB	USB_EXTA_MUXED_P 37C4
	USB_90D	USB	USB_EXTA_MUXED_N 37C4
	USB_90D	USB	CONN_USB_EXTA_P 37C3
	USB_90D	USB	CONN_USB_EXTA_N 37C3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 20D3 31B5
	USB_90D	USB	USB_CAMERA_N 20D3 31B5
	USB_90D	USB	USB_CAMERA_CONN_P 7D5 31B7
	USB_90D	USB	USB_CAMERA_CONN_N 7D5 31B7
USB_BT	USB_90D	USB	USB_BT_P 20D3 31B5
	USB_90D	USB	USB_BT_N 20C3 31B5
	USB_90D	USB	CONN_USB2_BT_P 7D5 31B7
	USB_90D	USB	CONN_USB2_BT_N 7D5 31B7
USB_TPAD	USB_90D	USB	USB_TPAD_P 20D3 47B8
	USB_90D	USB	USB_TPAD_N 20D3 47B8
	USB_90D	USB	USB_TPAD_R_P 47B7
	USB_90D	USB	USB_TPAD_R_N 47B7
USB_IR	USB_90D	USB	USB_IR_P 20D3 38C7
	USB_90D	USB	USB_IR_N 20D3 38C7
USB_EXTB	USB_90D	USB	USB_EXTB_P 20C3 37A4
	USB_90D	USB	USB_EXTB_N 20C3 37B4
	USB_90D	USB	CONN_USB_EXTB_P 37B3
	USB_90D	USB	CONN_USB_EXTB_N 37B3
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 20C4
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK 13B6 21C3 42D8
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA 13B6 21C3 42D8
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK 21C3 42C8
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA 21C3 42C8
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 21D2 51D7
	HDA_55S	HDA	HDA_BIT_CLK_R 21A7 21D4
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 21D2 51C7
	HDA_55S	HDA	HDA_SYNC_R 21A7 21D4
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L 21A7 21D4
	HDA_55S	HDA	HDA_RST_L 21D2 51C7
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 21D7 51C7
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 21D2 51C7
	HDA_55S	HDA	HDA_SDOUT_R 21A7 21D4
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 21C7
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R 21B3 26B4
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK 26B1 39C5
SPI_CLK	SPI_55S	SPI	SPI_CLK_R 21B3 41A5 41C8
	SPI_55S	SPI	SPI_CLK 41B1 50C5
	SPI_55S	SPI	SPI_ALT_CLK 41C5 41D3
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R 21B3 41A5 41C7
	SPI_55S	SPI	SPI_MOSI 41B1 50C4
	SPI_55S	SPI	SPI_ALT_MOSI 41C5 41D5
SPI_MISO	SPI_55S	SPI	SPI_MISO 21B3 41A5 41B7
	SPI_55S	SPI	SPI_MISO_R 50C4
	SPI_55S	SPI	SPI_ALT_MISO 41B5 41D5
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L 21B3 41B7
	SPI_55S	SPI	SPI_CS0_L
	SPI_55S	SPI	SPI_CS1_R_L
	SPI_55S	SPI	SPI_CS1_R_L_USE_MLB 41B2

MCP Constraints 2

SYNC_MASTER=T18_MLB SYNC_DATE=12/14/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE: NONE	SHT 103 OF 109	

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD 18C6
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND 18C6
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R 18C3 34A5
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1 33B6 34A3
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO 18C3 33B6
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC 18D3 33B6
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R 33C4
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK 18D6 33C1
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0> 33C4
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0> 18D6 33C1
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1> 18D6 33C1
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL 18D6 33B1
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R 33B4
	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK_R 33C6
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK 18D3 33C8
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0> 18D3 33C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1> 18D3 33C6
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL 18D3 33B6
	ENET_MII_55S	ENET_MII	ENET_RESET_L 18C3 33B7
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0> 33B3 35B7 35C7
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0> 33B3 35B7 35C7
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_P<3..0> 35B4 35C4 35C5
	ENET_MDI_100D	ENET_MDI	ENET_MDI_TRAN_N<3..0> 35B4 35C4 35C5

Ethernet Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=03/19/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE NONE SHT 104 OF 109

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5S5	SMB	SMBUS_SMC_A_S3_SCL	7B5 7D5 42D2
SMBUS_SMC_A_S3_SDA	SMB_5S5	SMB	SMBUS_SMC_A_S3_SDA	7B5 7D5 42D2
SMBUS_SMC_B_S0_SCL	SMB_5S5	SMB	SMBUS_SMC_B_S0_SCL	42C2
SMBUS_SMC_B_S0_SDA	SMB_5S5	SMB	SMBUS_SMC_B_S0_SDA	42C2
SMBUS_SMC_0_S0_SCL	SMB_5S5	SMB	SMBUS_SMC_0_S0_SCL	42D5
SMBUS_SMC_0_S0_SDA	SMB_5S5	SMB	SMBUS_SMC_0_S0_SDA	42D5
SMBUS_SMC_BSA_SCL	SMB_5S5	SMB	SMBUS_SMC_BSA_SCL	7A7 7B7 42C5
SMBUS_SMC_BSA_SDA	SMB_5S5	SMB	SMBUS_SMC_BSA_SDA	42C5
SMBUS_SMC_MGMT_SCL	SMB_5S5	SMB	SMBUS_SMC_MGMT_SCL	42B5
SMBUS_SMC_MGMT_SDA	SMB_5S5	SMB	SMBUS_SMC_MGMT_SDA	42B5

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

SMC Constraints

SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C
SCALE NONE	SHT 106 OF 109	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

M97 SENSOR NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DIFFPAIR		CHGR_CSO_R_P	44A8 57B3
	DIFFPAIR		CHGR_CSO_R_N	44A8 57B3
	DIFFPAIR		CPUTHMSNS_D2_P	45C5
	DIFFPAIR		CPUTHMSNS_D2_N	45C5
	DIFFPAIR		CPU_THERMD_P	10C6 45D5
	DIFFPAIR		CPU_THERMD_N	10C6 45D5
	DIFFPAIR		ISNS_CPUVTT_P	44B7
	DIFFPAIR		ISNS_CPUVTT_N	44B7
	DIFFPAIR		ISNS_P1V5S0MCP_P	44C7
	DIFFPAIR		ISNS_P1V5S0MCP_N	44C7
	DIFFPAIR		ISNS_PVCORES0MCP_P	44D8
	DIFFPAIR		ISNS_PVCORES0MCP_N	44D8 61C4
	DIFFPAIR		MCPTHMSNS_D2_P	7C7 45B5
	DIFFPAIR		MCPTHMSNS_D2_N	7C7 45B5
	DIFFPAIR		MCP_THMDIODE_P	21C3 45C5
	DIFFPAIR		MCP_THMDIODE_N	21C3 45C5

M97 SPECIAL CONSTRAINTS

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	107	109

M97 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3,ISL4,ISL9,ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
2X_DIELECTRIC	-	0.126 MM	?
3X_DIELECTRIC	-	0.189 MM	?
4X_DIELECTRIC	-	0.252 MM	?
5X_DIELECTRIC	-	0.315 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA_P1MM	STANDARD
MEM_40S_VDD	BGA_P1MM	STANDARD

M97 RULE DEFINITIONS

SYNC_MASTER=M97_MLB

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7918	C

SCALE	SHT	OF
NONE	109	109