

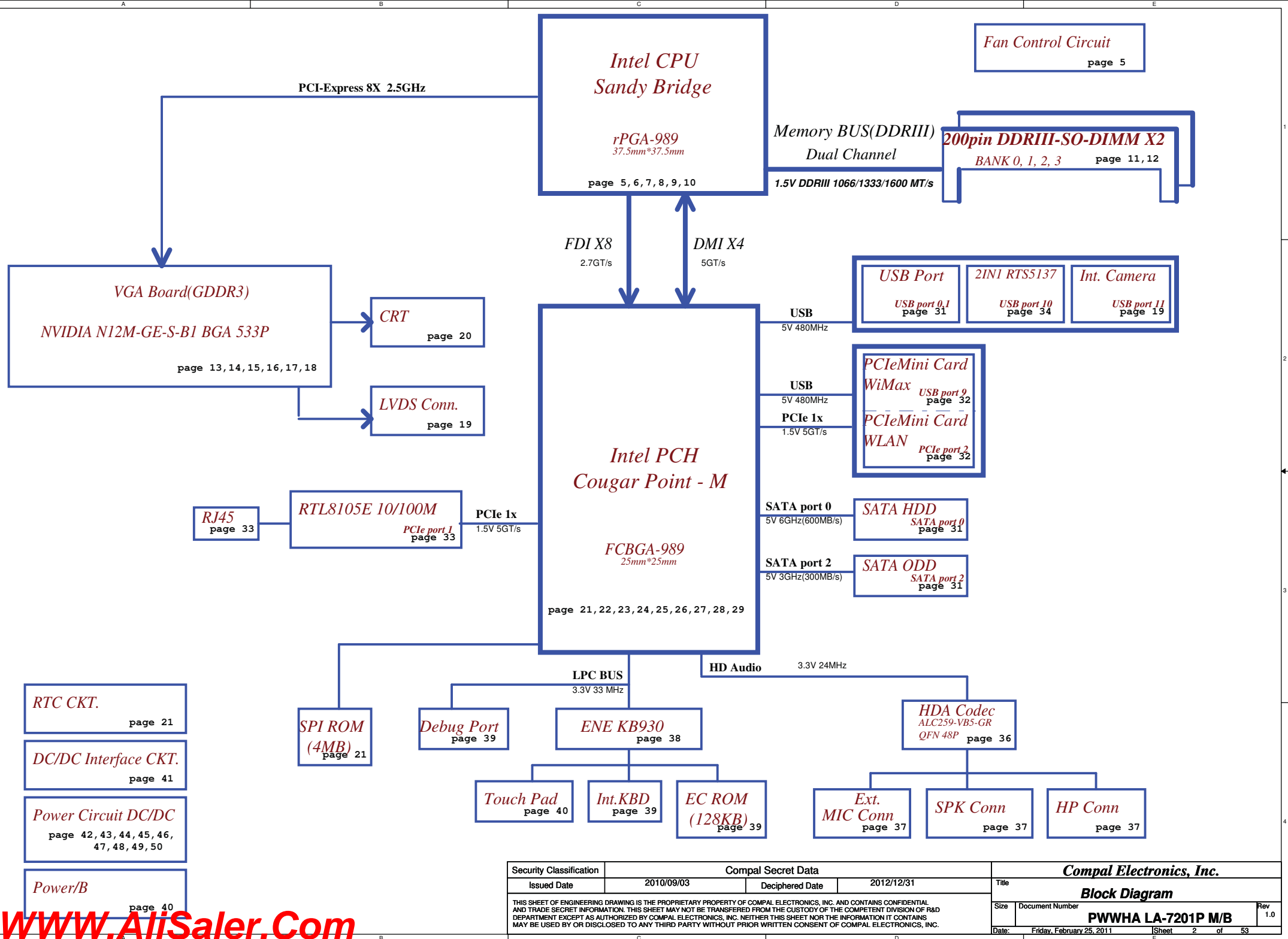
PWWHA

Delhi 10RG

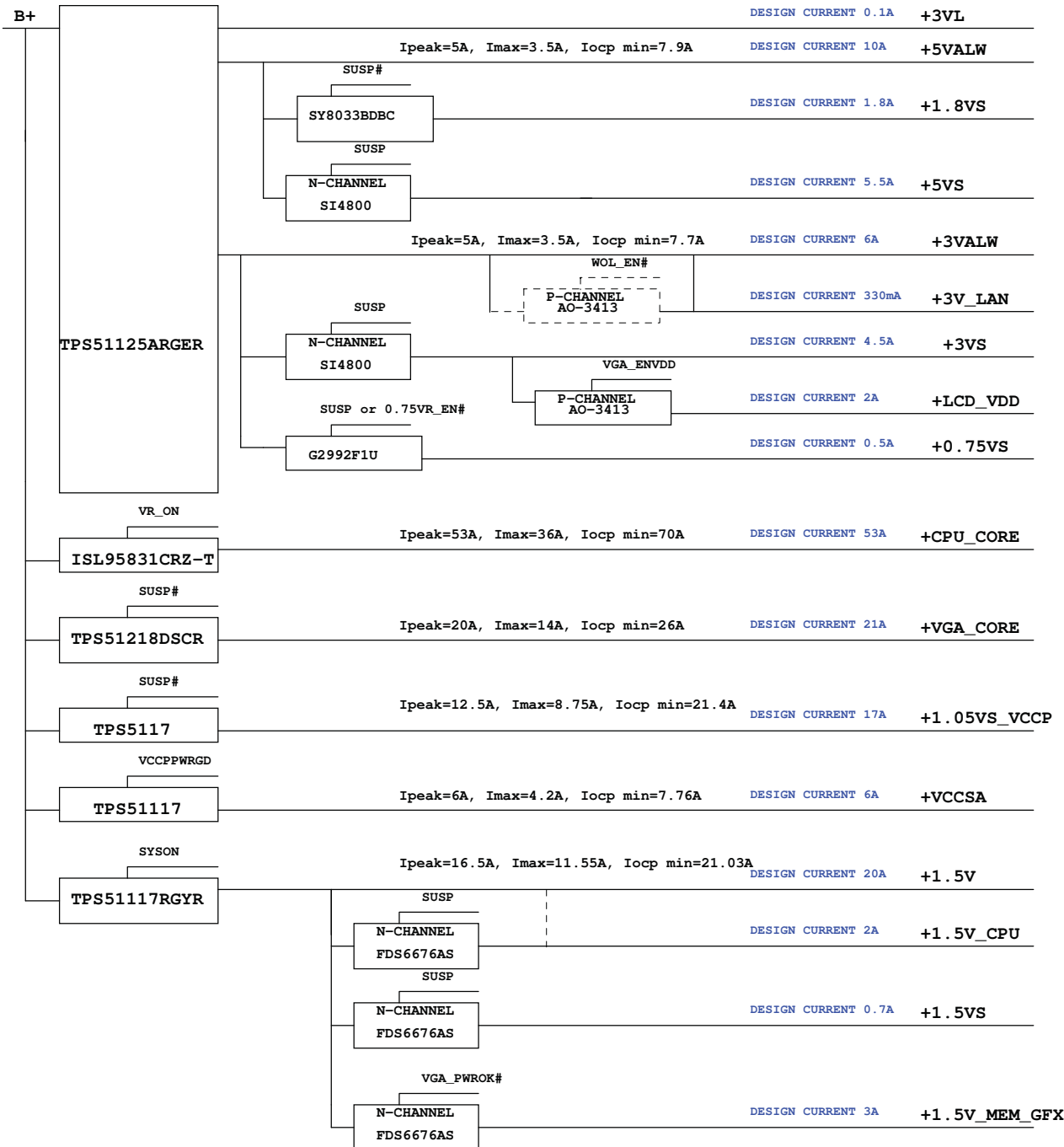
LA-7201P REV 1.0 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2011-01-31 Rev 1.0

| | | | | | |
|---|------------|--------------------|------------|-----------------------------------|---------------------------------------|
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| Issued Date | 2010/09/03 | Deciphered Date | 2012/12/31 | Title | |
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| | | | | Date Friday, February 25, 2011 | Rev 1.0 |
| | | | | Cover Page | |
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| | | | | | |
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Voltage Rails

(O MEANS ON X MEANS OFF)

| power plane State | +RTCVCC | B+ | +3VL | +5VALW +3VALW +VSB | +1.5V | +5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE |
|--------------------------------|---------|----|------|--------------------------|-------|--|
| S0 | O | O | O | O | O | O |
| S1 | O | O | O | O | O | O |
| S3 | O | O | O | O | O | X |
| S5 S4/AC | O | O | O | O | X | X |
| S5 S4/ Battery only | O | O | O | X | X | X |
| S5 S4/AC & Battery don't exist | O | X | X | X | X | X |

PCH SM Bus Address

| Power | Device | HEX | Address |
|-------|---------------|------|-------------|
| +3VS | DDR SO-DIMM 0 | A0 H | 1010 0000 b |
| +3VS | DDR SO-DIMM 1 | A4 H | 1010 0100 b |
| +3VS | WLAN/WIMAX | | |

EC SM Bus1 Address

EC SM Bus2 Address

| Power | Device | HEX | Address | Power | Device | HEX | Address |
|-------|---------------|------|-------------|-------|--------|------|-------------|
| +3VL | Smart Battery | 16 H | 0001 0110 b | +3VS | PCH | 96 H | 1001 0110 b |

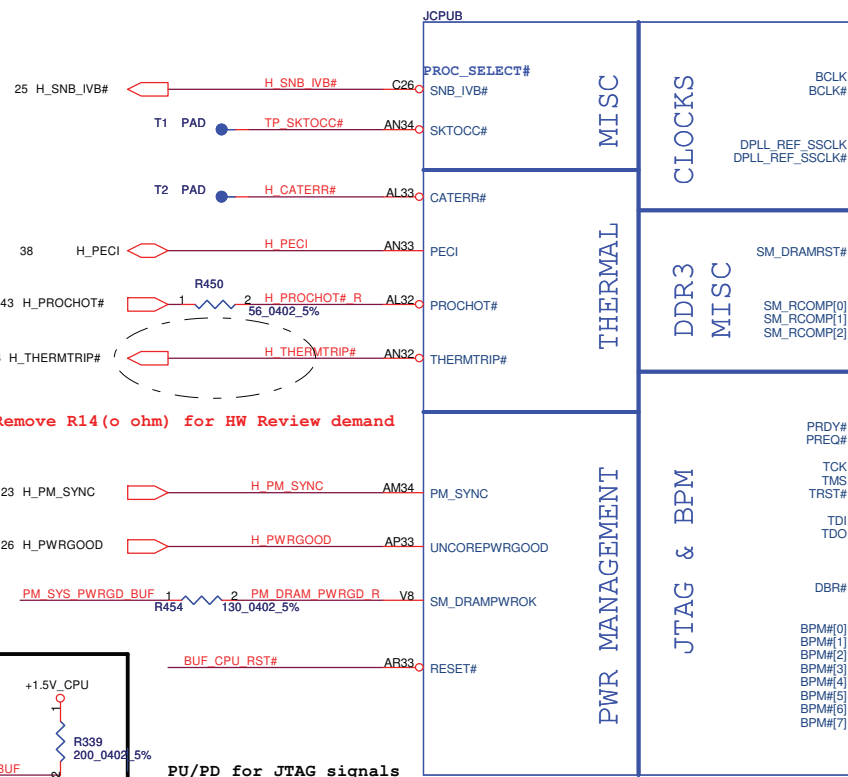
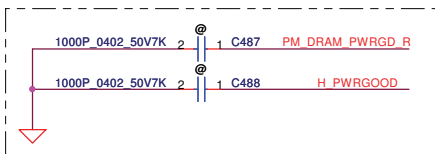
BTO Option Table

| Function | DIS only | MINI PCI-E SLOT | LAN | | | Camera & Mic |
|-------------|----------|-----------------|-----------|-----------|--------|--------------|
| description | | SLOT1 | LAN | | | Camera & Mic |
| explain | | WIMAX | 10/100M | Giga | | Camera & Mic |
| BTO | DIS@ | WIMAX@ | 8105ELDO@ | 8105ESWR@ | 8111E@ | CAM@ |

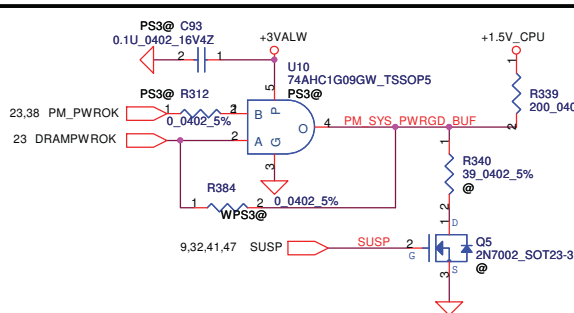
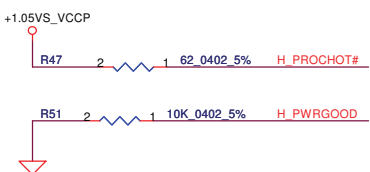
| Function | PCH | HDMI/Non-HDMI | EC Chip | | | Zero ODD |
|-------------|--------|---------------|-------------|----------|--------|----------|
| description | | | 930 or 9012 | | | |
| explain | | | 930 | Complete | Simple | |
| BTO | Q65R3@ | HDMI@/NHDMI@ | 930@ | 9012@ | S9012@ | ZODD@ |

| STATE | SIGNAL | SLP_S3# | SLP_S4# | SLP_S5# |
|-----------------------|--------|---------|---------|---------|
| Full ON | | HIGH | HIGH | HIGH |
| S1 (Power On Suspend) | | HIGH | HIGH | HIGH |
| S3 (Suspend to RAM) | | LOW | HIGH | HIGH |
| S4 (Suspend to Disk) | | LOW | LOW | HIGH |
| S5 (Soft OFF) | | LOW | LOW | LOW |
| G3 | | LOW | LOW | LOW |

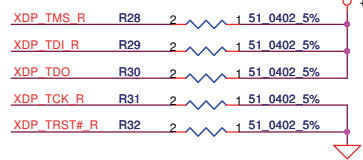
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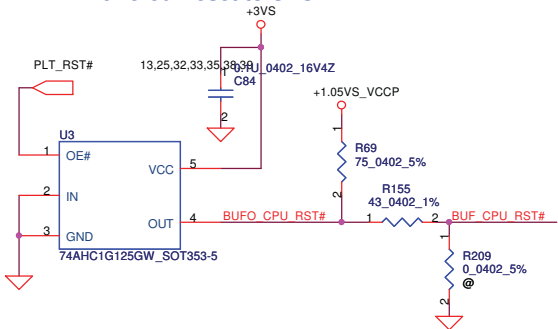
Remove R14(0 ohm) for HW Review demand



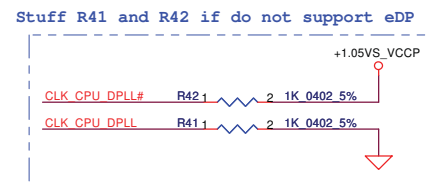
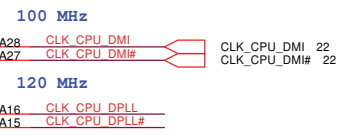
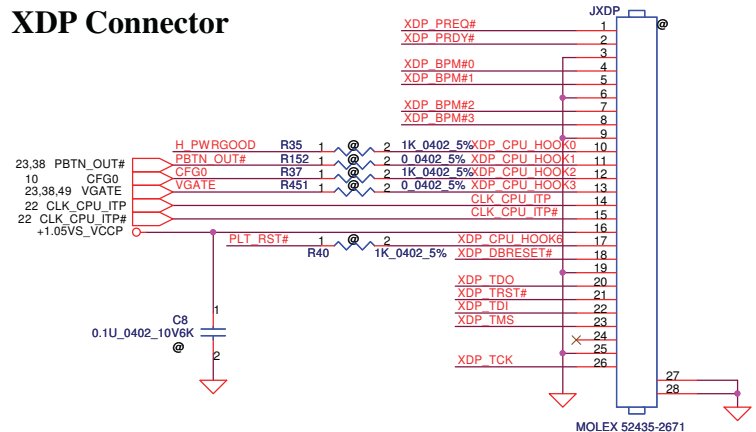
PU/PD for JTAG signals



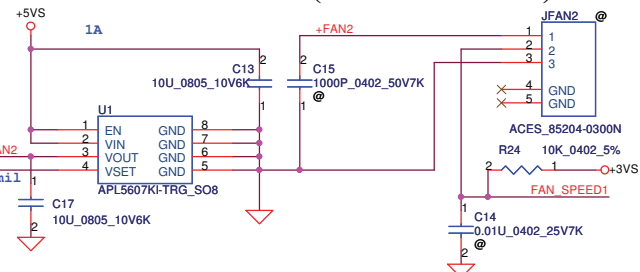
Buffered Reset to CPU



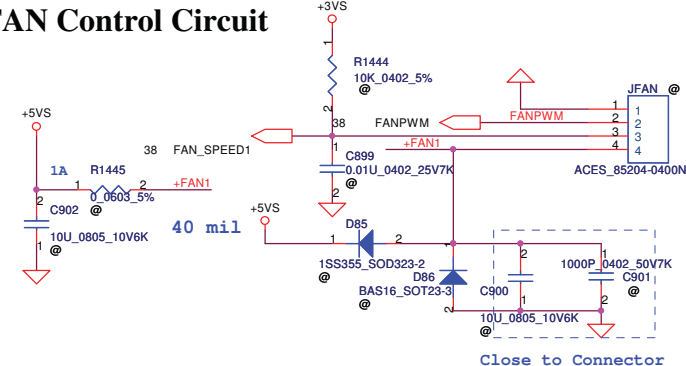
XDP Connector



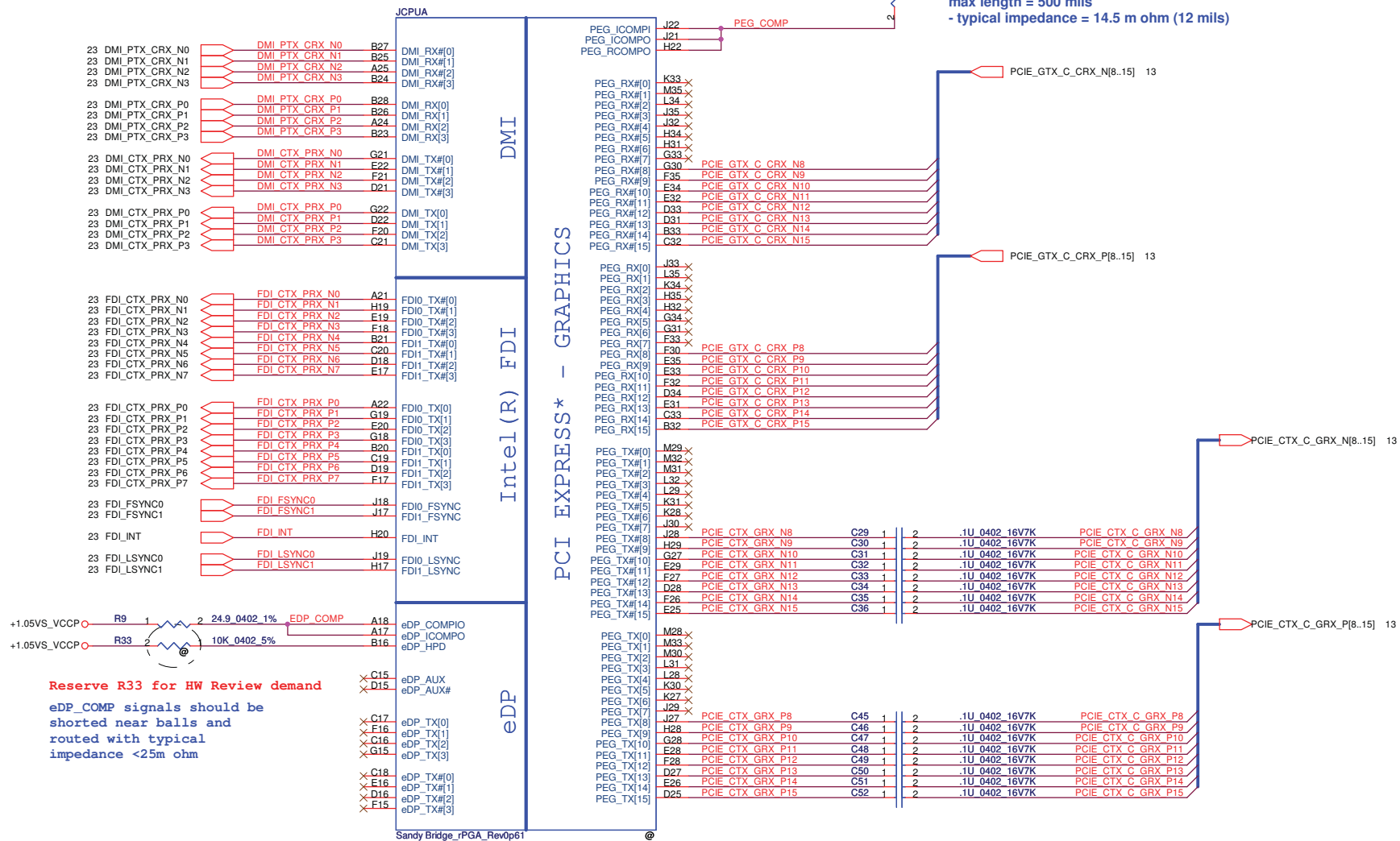
FAN Control Circuit (RPM and PWM)



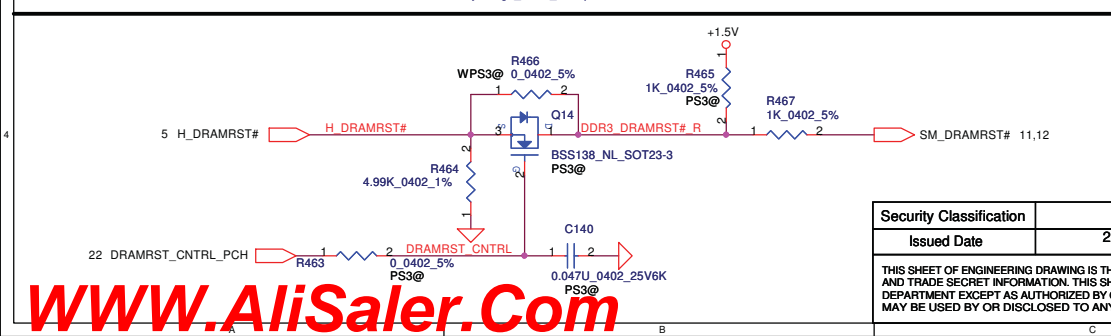
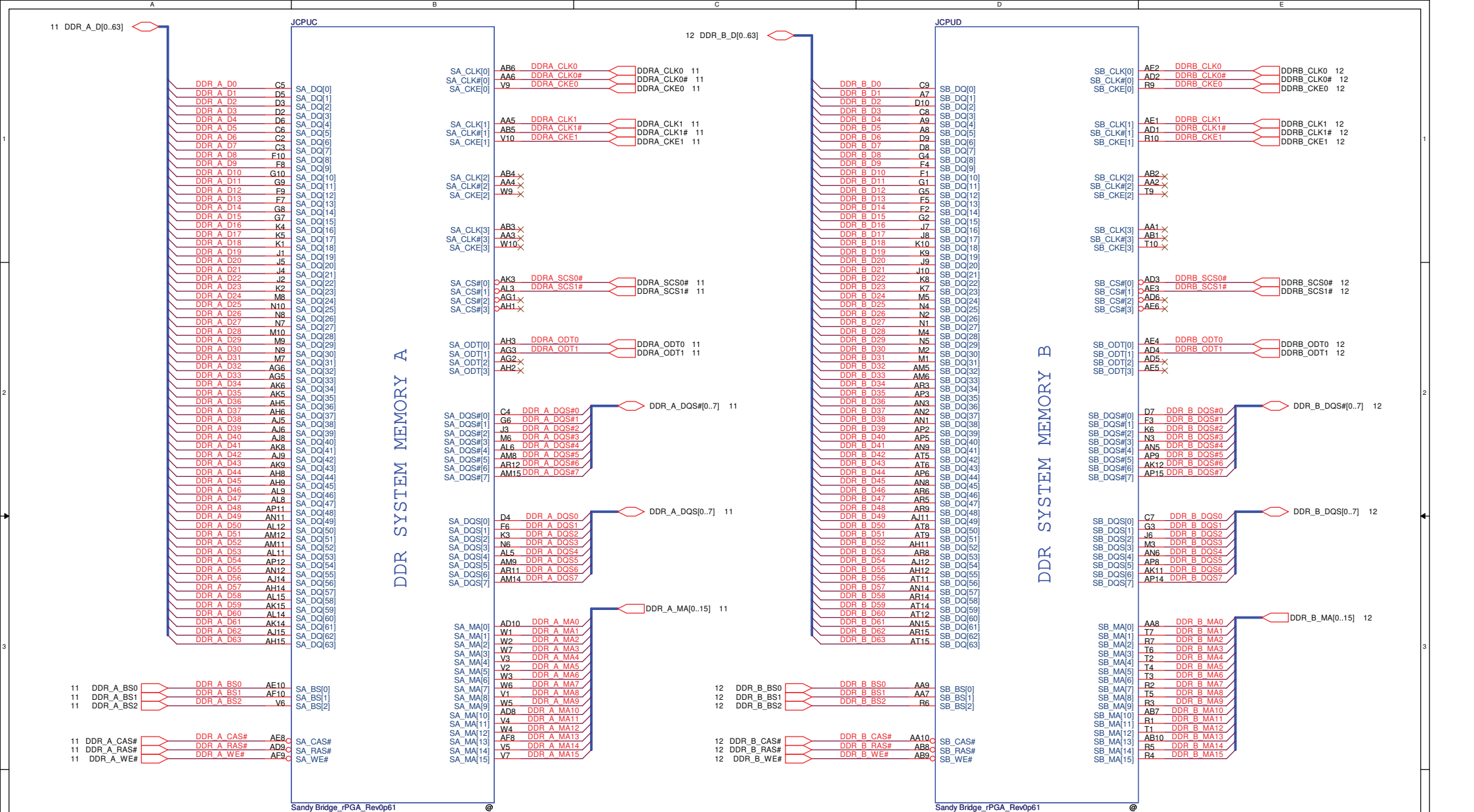
FAN Control Circuit



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+CPU_CORE
 JCPUF
53A (SV 35W)
 AG35 VCC1
 AG34 VCC2
 AG33 VCC3
 AG32 VCC4
 AG31 VCC5
 AG30 VCC6
 AG29 VCC7
 AG28 VCC8
 AG27 VCC9
 AG26 VCC10
 AF35 VCC11
 AF34 VCC12
 AF33 VCC13
 AF32 VCC14
 AF31 VCC15
 AF30 VCC16
 AF29 VCC17
 AF28 VCC18
 AF27 VCC19
 AF26 VCC20
 AD35 VCC21
 AD34 VCC22
 AD33 VCC23
 AD32 VCC24
 AD31 VCC25
 AD29 VCC26
 AD28 VCC27
 AD27 VCC28
 AD26 VCC29
 AC34 VCC30
 AC33 VCC31
 AC32 VCC32
 AC31 VCC33
 AC30 VCC34
 AC29 VCC35
 AC28 VCC36
 AC27 VCC37
 AC26 VCC38
 AC25 VCC39
 AC24 VCC40
 AC23 VCC41
 AC22 VCC42
 AC21 VCC43
 AC20 VCC44
 AC19 VCC45
 AC18 VCC46
 AC17 VCC47
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 AC15 VCC49
 AC14 VCC50
 AC13 VCC51
 AC12 VCC52
 AC11 VCC53
 AC10 VCC54
 AC9 VCC55
 AC8 VCC56
 AC7 VCC57
 AC6 VCC58
 AC5 VCC59
 AC4 VCC60
 AC3 VCC61
 AC2 VCC62
 AC1 VCC63
 AC0 VCC64
 AC-1 VCC65
 AC-2 VCC66
 AC-3 VCC67
 AC-4 VCC68
 AC-5 VCC69
 AC-6 VCC70
 AC-7 VCC71
 AC-8 VCC72
 AC-9 VCC73
 AC-10 VCC74
 AC-11 VCC75
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 AC-13 VCC77
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 AC-16 VCC80
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 AC-19 VCC83
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 AC-21 VCC85
 AC-22 VCC86
 AC-23 VCC87
 AC-24 VCC88
 AC-25 VCC89
 AC-26 VCC90
 AC-27 VCC91
 AC-28 VCC92
 AC-29 VCC93
 AC-30 VCC94
 AC-31 VCC95
 AC-32 VCC96
 AC-33 VCC97
 AC-34 VCC98
 AC-35 VCC99
 AC-36 VCC100

POWER

CORE SUPPLY

SENSE LINES

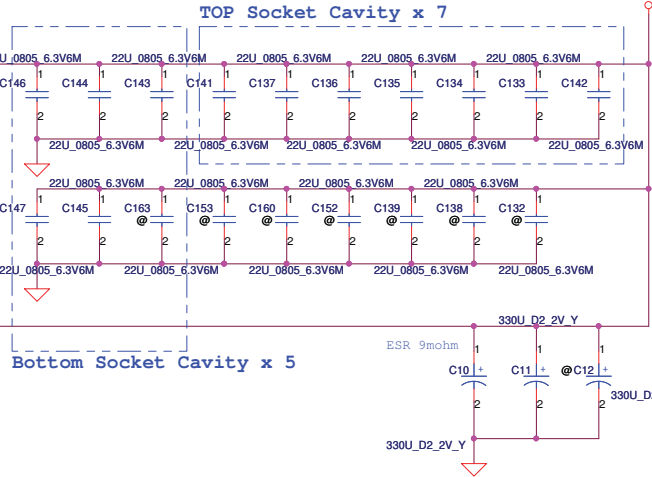
PEG AND DDR

SVID

SENSE LINES

8.5A

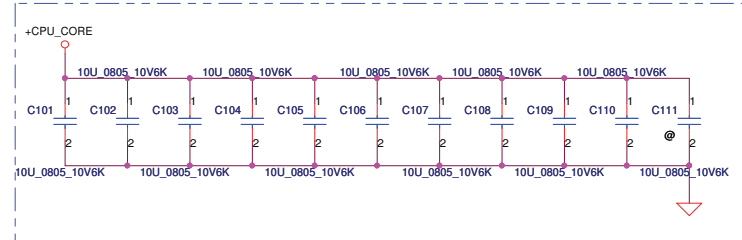
VCCIO1 AH13
 VCCIO2 AH10
 VCCIO3 AG30
 VCCIO4 Y10
 VCCIO5 L10
 VCCIO6 J14
 VCCIO7 J13
 VCCIO8 J12
 VCCIO9 J11
 VCCIO10 J10
 VCCIO11 J09
 VCCIO12 J08
 VCCIO13 J07
 VCCIO14 J06
 VCCIO15 J05
 VCCIO16 J04
 VCCIO17 J03
 VCCIO18 J02
 VCCIO19 J01
 VCCIO20 J00
 VCCIO21 J-01
 VCCIO22 J-02
 VCCIO23 J-03
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 VCCIO26 J-06
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 VCCIO98 J-78
 VCCIO99 J-79
 VCCIO100 J-80



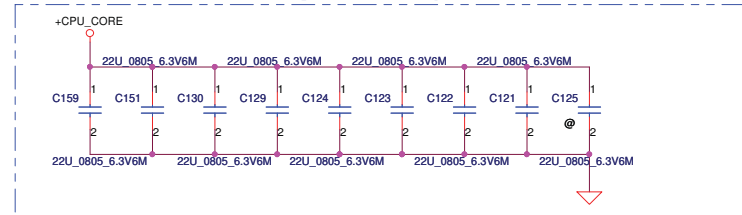
+1.05VS_VCCP
 +1.05VS_VCCP Decoupling:
 2X 330U (6m ohm), 12X 22U

+CPU_CORE Decoupling:
 4X 470U (4m ohm), 16X 22U, 10X 10U

Bottom Socket Cavity

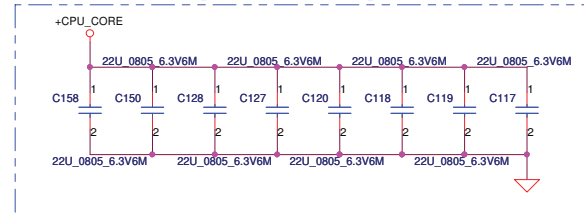


Top Socket Edge

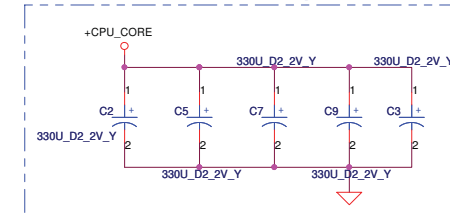


9/02 Remove C126, C131 by Power Demand

Top Socket Cavity



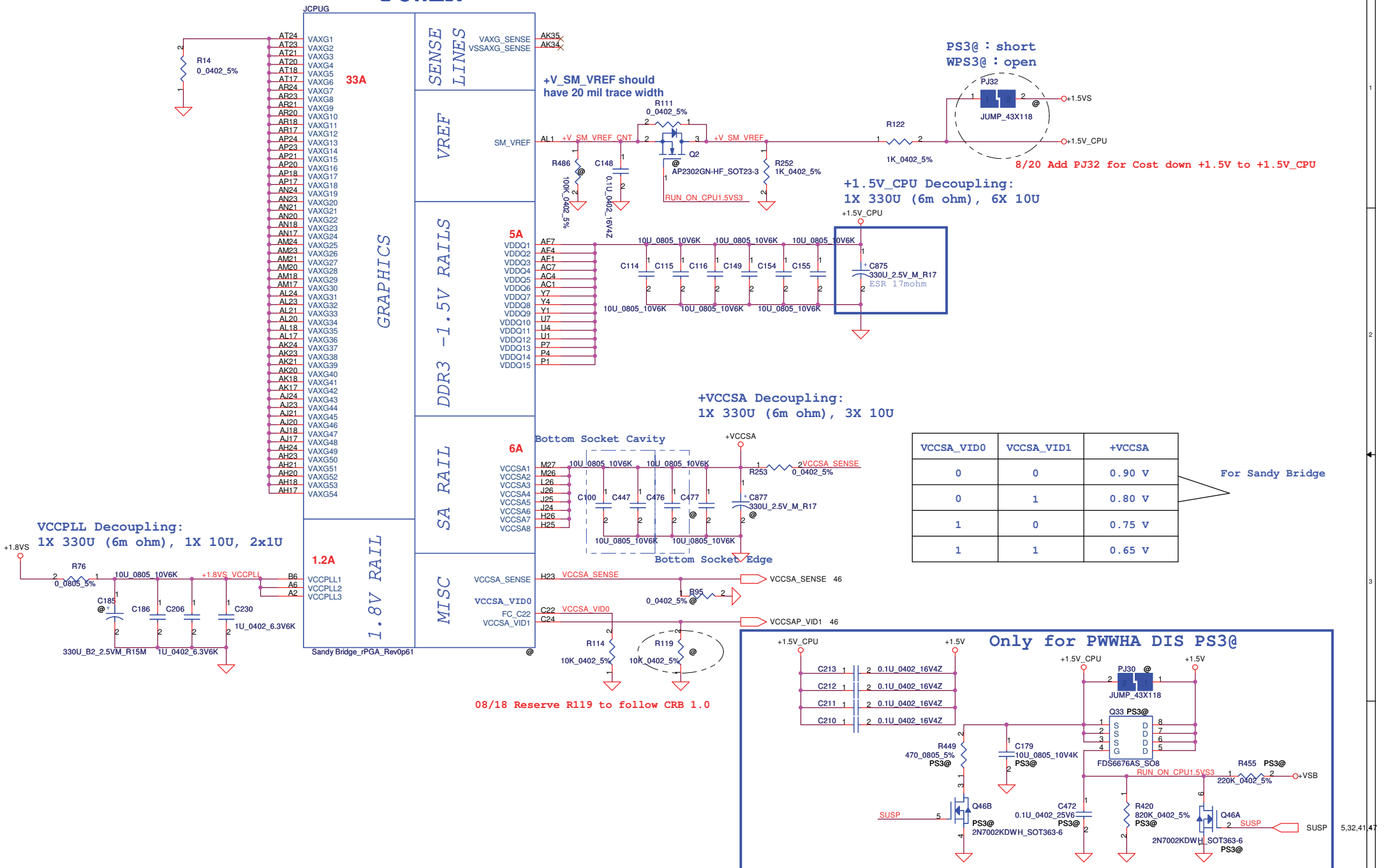
Bottom Socket Edge



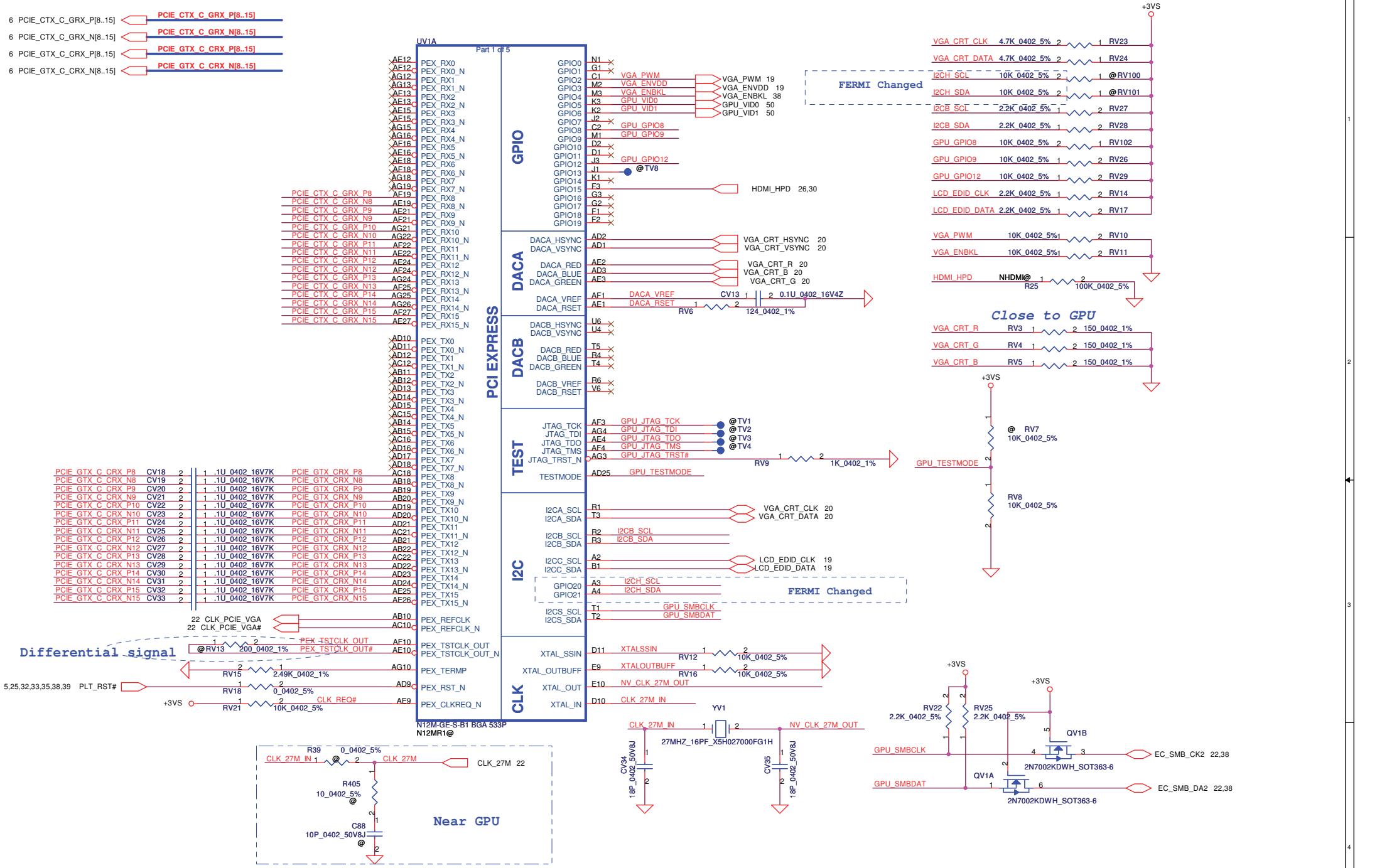
9/02 Add C898 3Pin Bulk Cap by Power Demand
 9/02 Change C890, C891, C894 from SGA00005R00 to SGA00004X80 for Power demand

| | | | | | |
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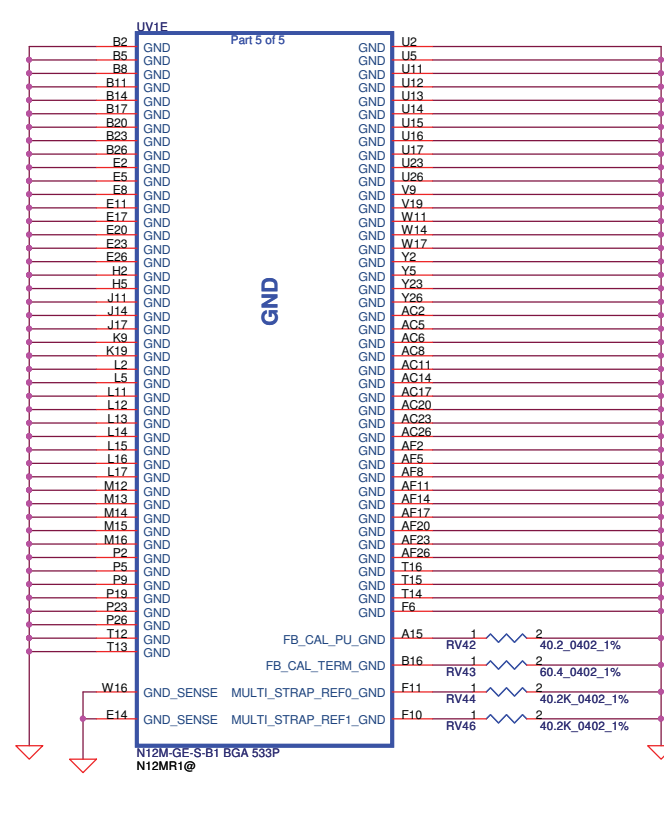
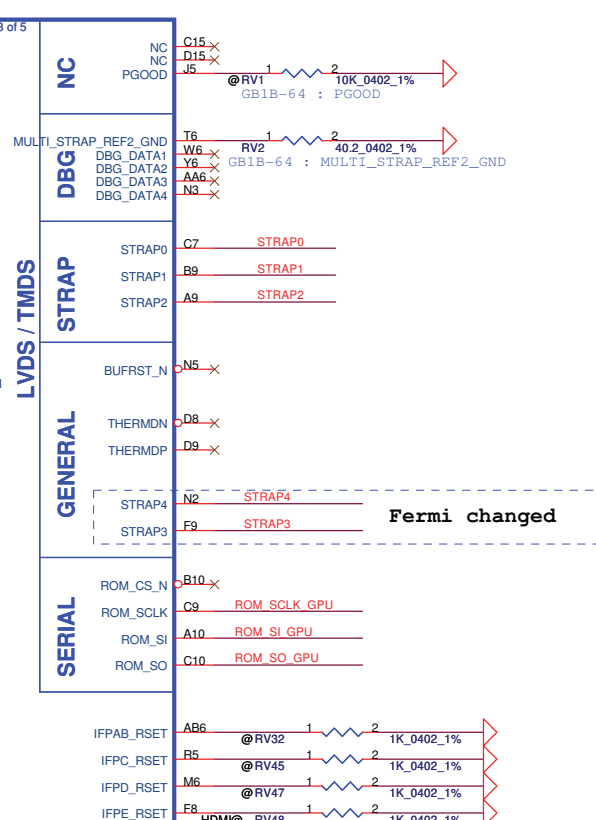
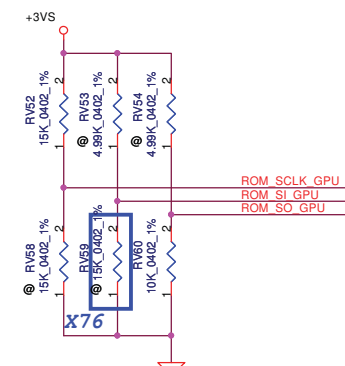
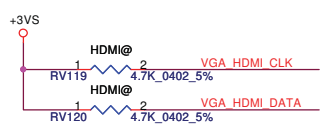
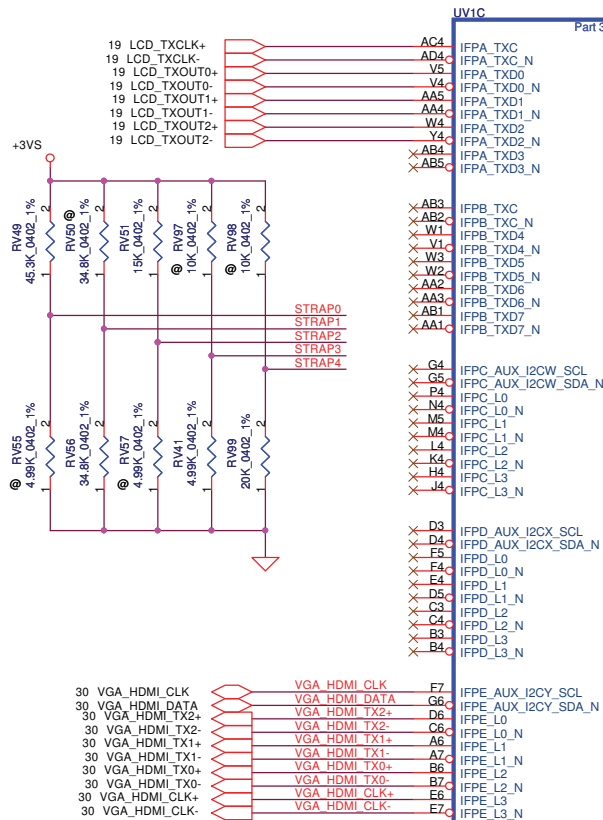
POWER



| | | | | | |
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| | | | | Rev | 1.0 |



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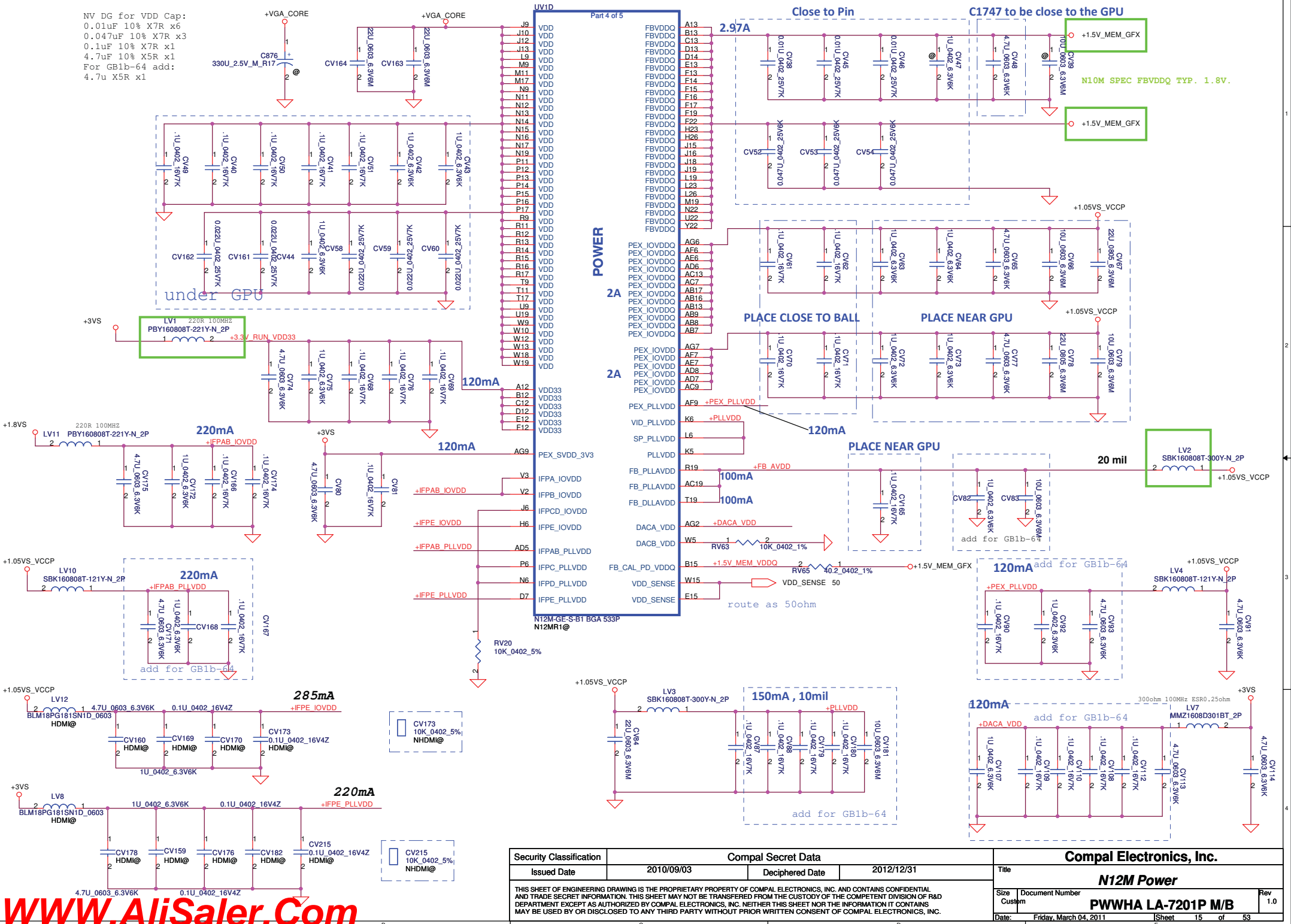
| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|------------------------|------------|------------------------|------------------------|------------------------|------------------------|
| ROM_SO | +3VS | XCLK_417 | FB_0_BAR_SIZE | SMB_ALT_ADDR | VGA_DEVICE |
| ROM_SCLK | +3VS | PCI_DEVID[4] | SUB_VENDOR | SLOT_CLK_CFG | PEX_PLLEN_TERM |
| ROM_SI | +3VS | RAMCFG[3] | RAMCFG[2] | RAMCFG[1] | RAMCFG[0] |
| STRAP2 | +3VS | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] |
| STRAP1 | +3VS | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] |
| STRAP0 | +3VS | USER[3] | USER[2] | USER[1] | USER[0] |

| Resistor Values | Pull-up to +3VS | Pull-down to Gnd |
|-----------------|-----------------|------------------|
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |

| | | | |
|--|-------|------|-----------------------------|
| Hynix (800MHZ) 64MX16 H5TQ1G63DFR-12C SA0000324C0 | 512MB | 0010 | RV59 PD 15K (SD034150280) |
| Hynix (900MHZ) 128MX16 H5TQ2G63BFR-11C SA00003Y000 | 1GB | 0110 | RV59 PD 34.8K (SD034348280) |
| Samsung (800MHZ) 64MX16 K4W1G1646G-BC12 SA00004HS00 | 512MB | 0011 | RV59 PD 20K (SD034200280) |
| Samsung (900MHZ) 128MX16 K4W2G1646C-HC11 SA000047Q00 | 1GB | 0111 | RV59 PD 45.3K (SD034453280) |

| | | | | | | |
|---|--------------------|-----------------|------------|--------------------------|------------------------|----------------|
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| | | | | Custom | PWWHA LA-7201P M/B | 1.0 |
| | | | | Date: | Friday, March 04, 2011 | Sheet 14 of 53 |

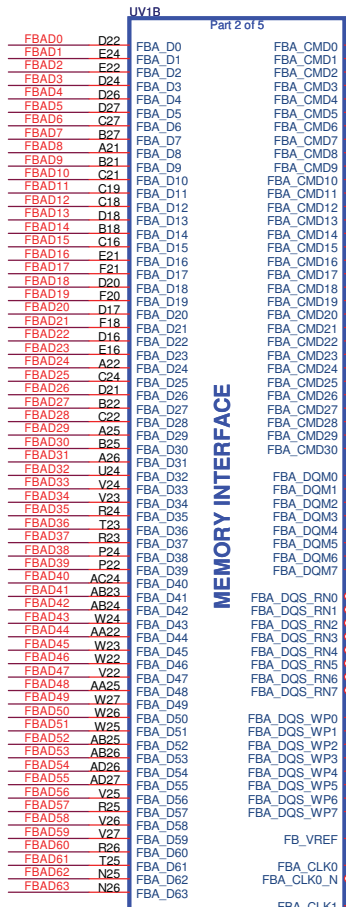
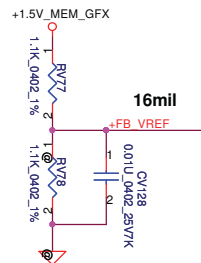
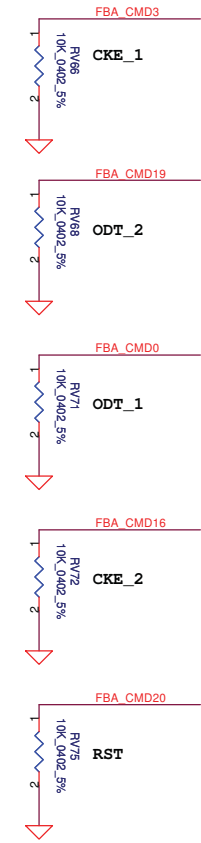
NV DG for VDD Cap:
 0.01uF 10% X7R x6
 0.047uF 10% X7R x3
 0.1uF 10% X7R x1
 4.7uF 10% X5R x1
 For GB1b-64 add:
 4.7u X5R x1



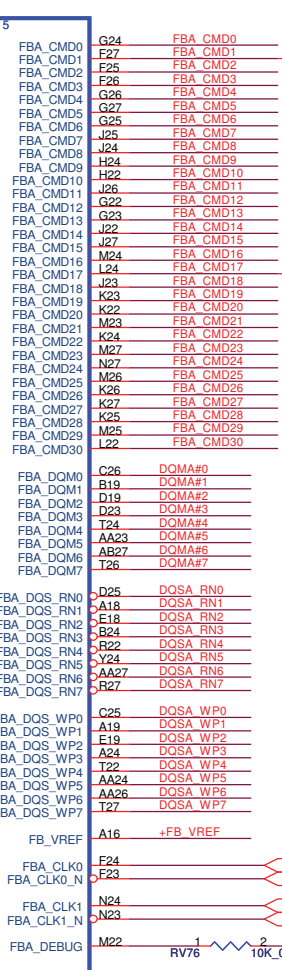
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|---|--|--------------------|--|-----------------|--|--------------------------|--|------------------------|--|----------------|--|
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| | | | | | | Size | | Document Number | | Rev | |
| | | | | | | Custom | | PWWHA LA-7201P M/B | | 1.0 | |
| | | | | | | Date: | | Friday, March 04, 2011 | | Sheet 15 of 53 | |

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FBAD[0..63] 17,18
FBA_CMD[0..30] 17,18
DQMA#[0..7] 17,18
DQSA_RN[0..7] 17,18
DQSA_WP[0..7] 17,18



N12M-GE-S-B1 BGA 533P
N12MR1@

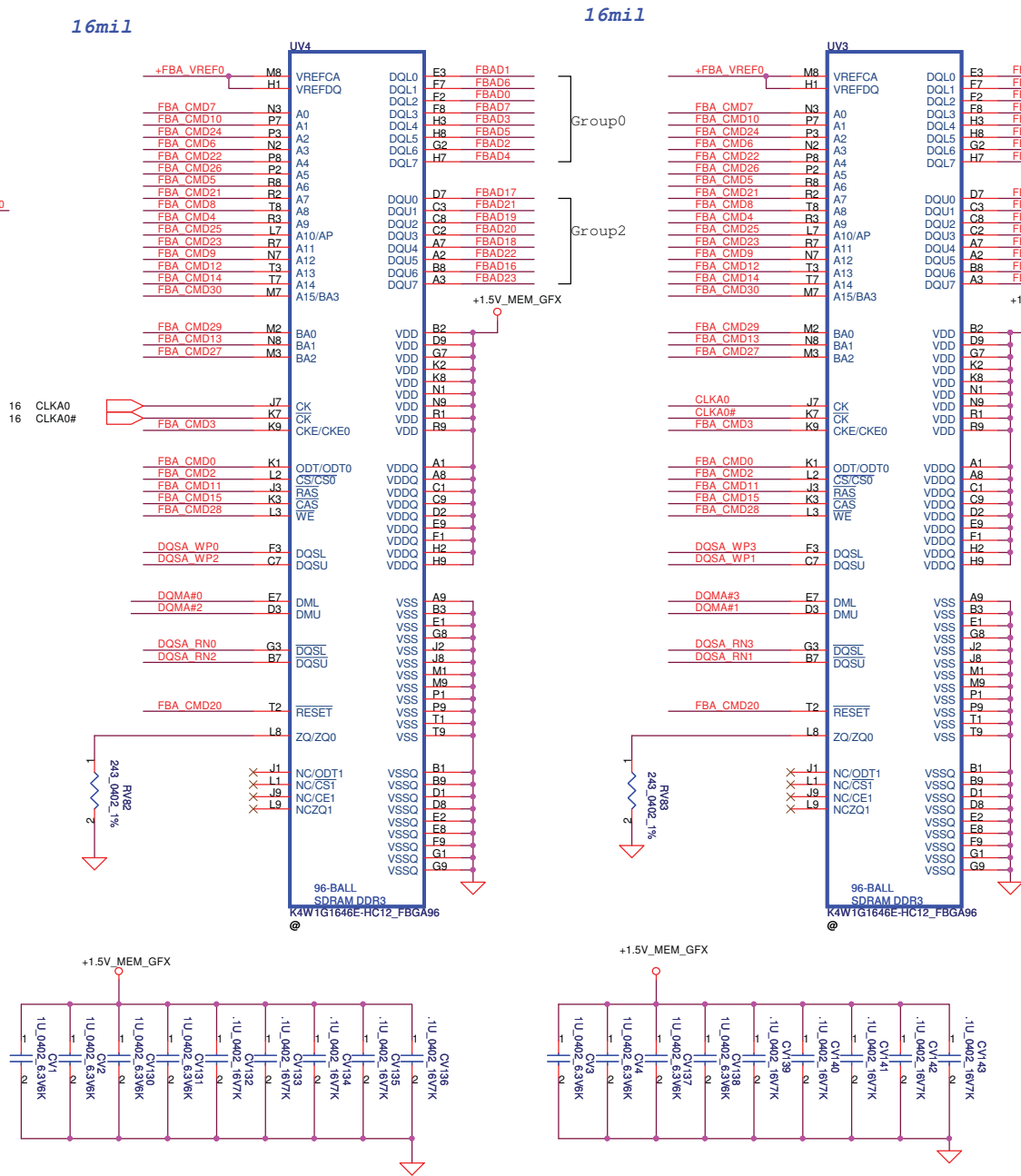


Mode E - Mirror Mode Mapping

| DATA Bus | | |
|----------|--------|--------|
| Address | 0..31 | 32..63 |
| CMD0 | ODT_L | |
| CMD1 | CS1#_L | |
| CMD2 | CS0#_L | |
| CMD3 | CKE_L | |
| CMD4 | A9 | A11 |
| CMD5 | A6 | A7 |
| CMD6 | A3 | BA1 |
| CMD7 | A0 | A12 |
| CMD8 | A8 | A8 |
| CMD9 | A12 | A0 |
| CMD10 | A1 | A2 |
| CMD11 | RAS# | RAS# |
| CMD12 | A13 | A14 |
| CMD13 | BA1 | A3 |
| CMD14 | A14 | A13 |
| CMD15 | CAS# | CAS# |
| CMD16 | | CKE_H |
| CMD17 | | CS1#_H |
| CMD18 | | CS0#_H |
| CMD19 | | ODT_H |
| CMD20 | RST | RST |
| CMD21 | A7 | A6 |
| CMD22 | A4 | A5 |
| CMD23 | A11 | A9 |
| CMD24 | A2 | A1 |
| CMD25 | A10 | WE# |
| CMD26 | A5 | A4 |
| CMD27 | BA2 | A15 |
| CMD28 | WE# | A10 |
| CMD29 | BA0 | BA0 |
| CMD30 | A15 | BA2 |

| | | | | | | | | | | |
|---|--|--------------------|--|------------------------|--|--------------------------|--|----------|--|-----|
| Security Classification | | Compal Secret Data | | | | Compal Electronics, Inc. | | | | |
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| | | Size | | Document Number | | PWWHA LA-7201P M/B | | | | Rev |
| | | Custom | | | | | | | | 1.0 |
| | | Date: | | Friday, March 04, 2011 | | Sheet | | 16 of 53 | | |

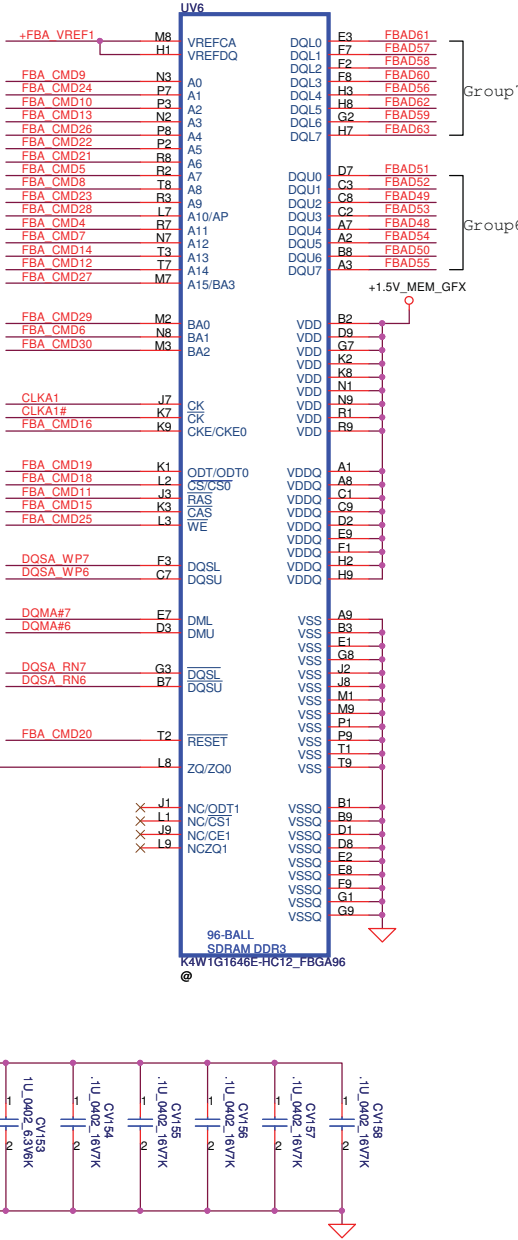
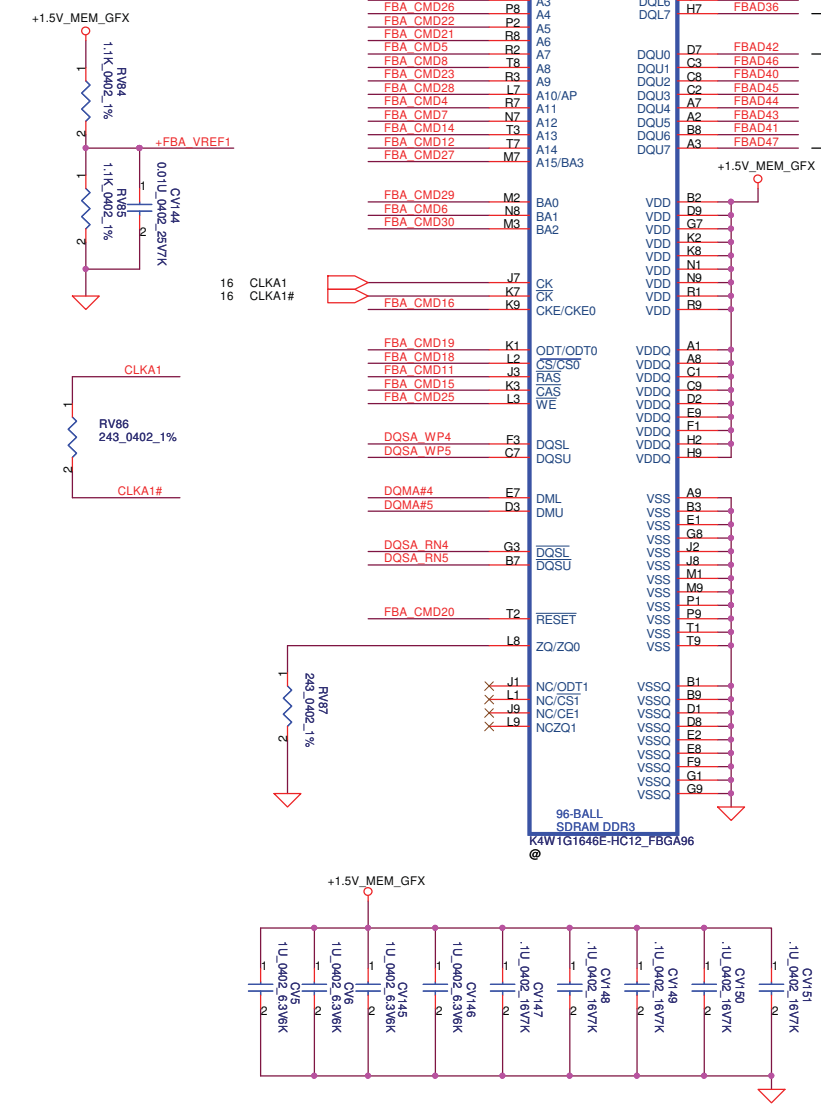
Memory Partition A - Lower 32 bits



Memory Partition A - Upper 32 bits

16mi1

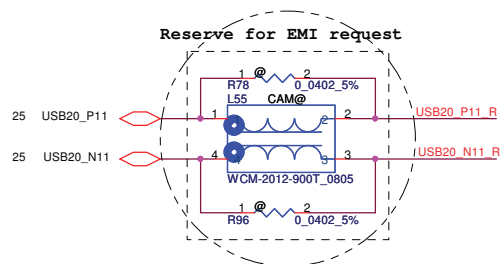
16mi1



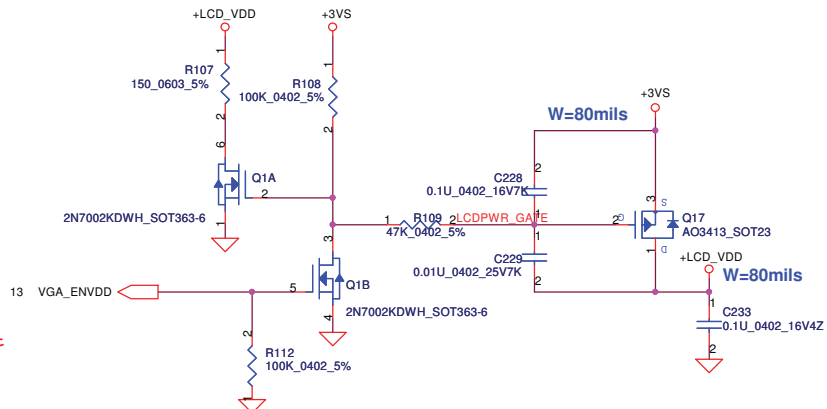
- FBA[0..63] FBAD[0..63] 16,17
- FBA_CMD[0..30] FBA_CMD[0..30] 16,17
- DQMA#[0..7] DQMA#[0..7] 16,17
- DQSA_RN[0..7] DQSA_RN[0..7] 16,17
- DQSA_WP[0..7] DQSA_WP[0..7] 16,17

Mode E - Mirror Mode Mapping

| DATA Bus | |
|----------|--------------|
| Address | 0..31 32..63 |
| CMD0 | ODT_L |
| CMD1 | CS1#_L |
| CMD2 | CS0#_L |
| CMD3 | CKE_L |
| CMD4 | A9 |
| CMD5 | A6 |
| CMD6 | A3 |
| CMD7 | A0 |
| CMD8 | A8 |
| CMD9 | A12 |
| CMD10 | A1 |
| CMD11 | RAS# |
| CMD12 | A13 |
| CMD13 | BA1 |
| CMD14 | A14 |
| CMD15 | CAS# |
| CMD16 | CKE_H |
| CMD17 | CS1#_H |
| CMD18 | CS0#_H |
| CMD19 | ODT_H |
| CMD20 | RST |
| CMD21 | A7 |
| CMD22 | A4 |
| CMD23 | A11 |
| CMD24 | A2 |
| CMD25 | A10 |
| CMD26 | A5 |
| CMD27 | BA2 |
| CMD28 | WE# |
| CMD29 | BA0 |
| CMD30 | A15 |

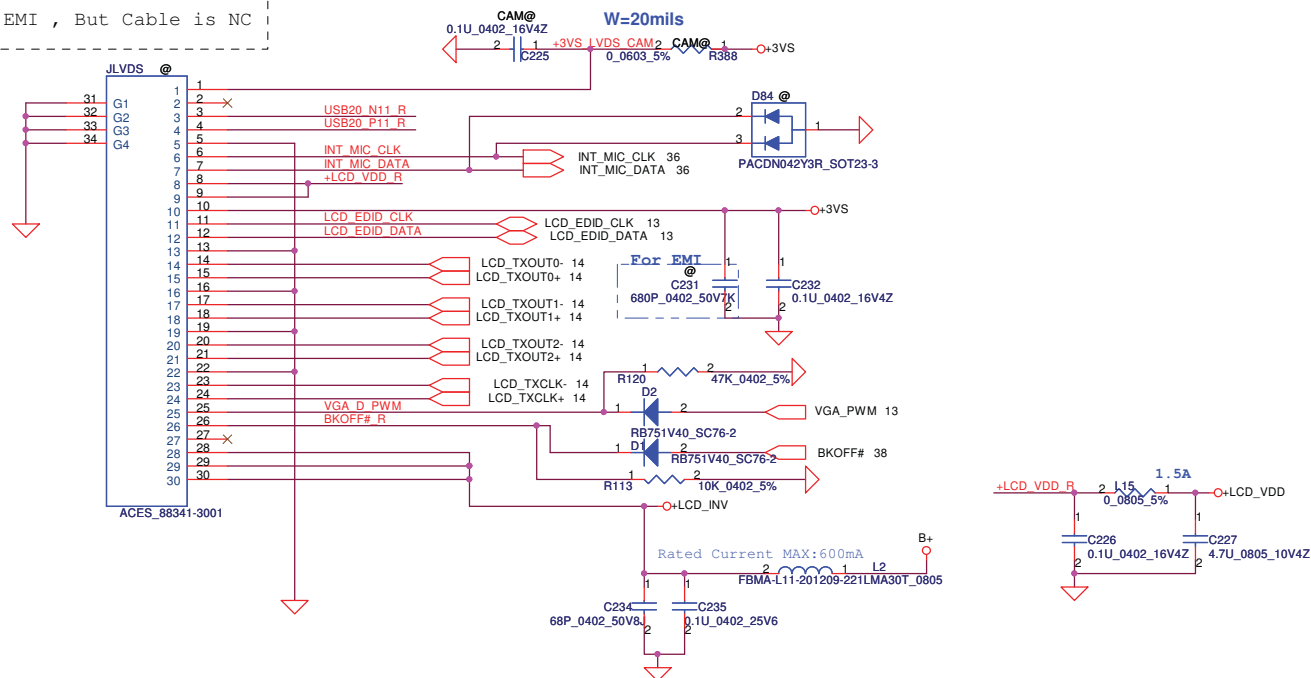


8/20 Swap USB20_P11 and USB20_N11 for layout request



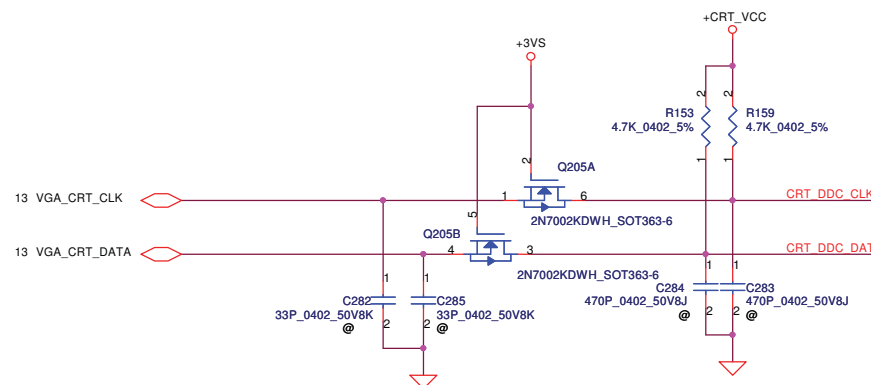
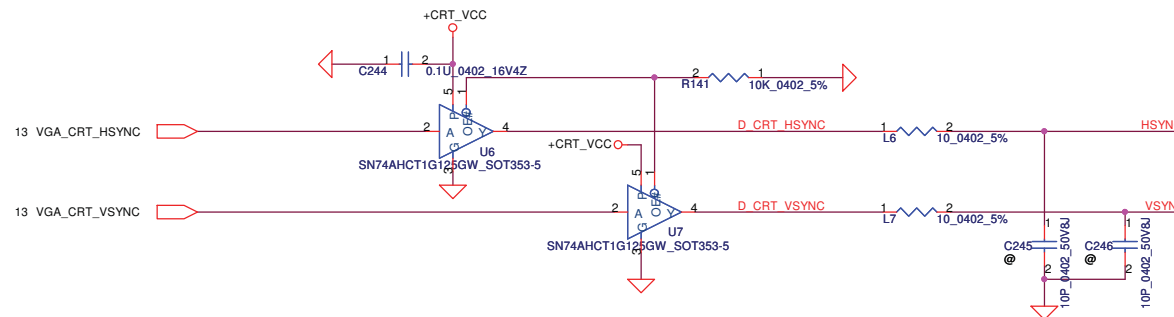
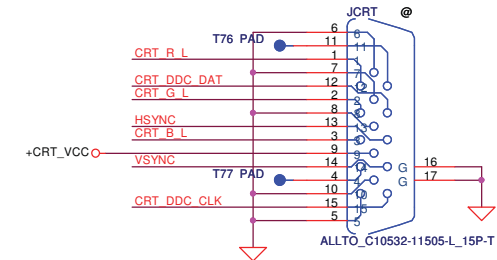
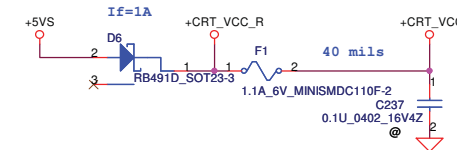
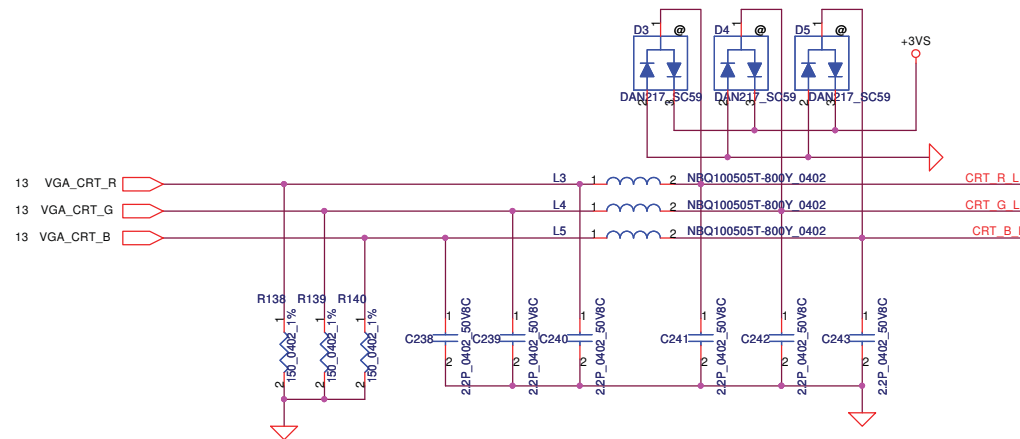
LCD/PANEL BD. Conn.

Pin13 GND for EMI , But Cable is NC

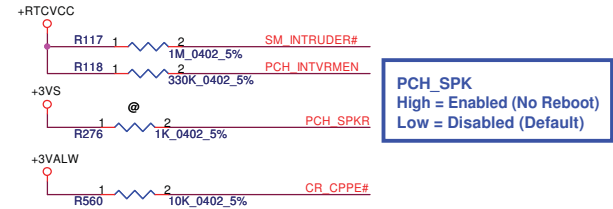
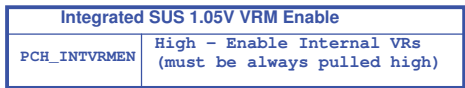
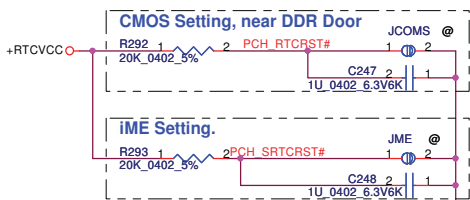


| | | | | | |
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| | | | | Date | Rev |
| | | | | Friday, March 04, 2011 | 1.0 |
| | | | | Sheet | 19 of 53 |

CRT CONNECTOR

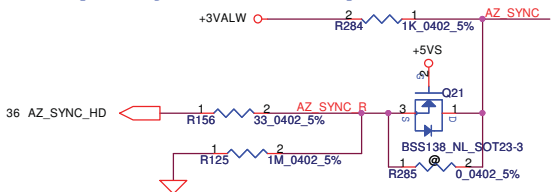


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|---|------------|------------------------|------------|--------------------------|--|
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| | | PWWHA LA-7201P M/B | | 1.0 | |
| Date | | Friday, March 04, 2011 | | Sheet | |
| | | 20 | | of | |
| | | 53 | | | |

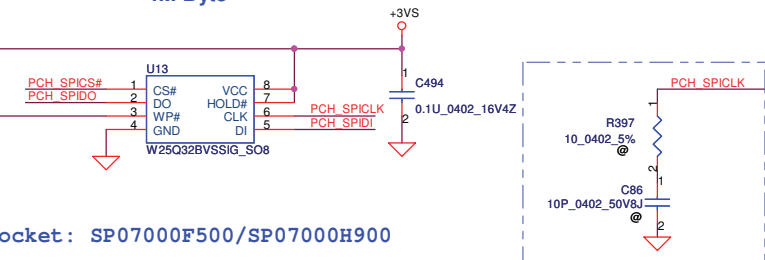


HDA_SDO
ME debug mode,
this signal has a weak internal pull down
★Low = Disable (default)
High = Enable (flash descriptor security override)

HDA_SYNC
★This signal has a weak internal pull down
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V
Need to pull high for Huron River platform



4M Byte

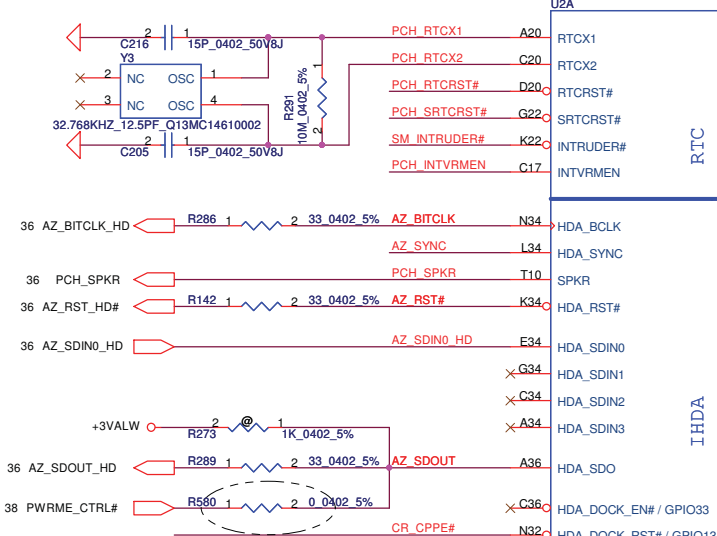


Socket: SP07000F500/SP07000H900

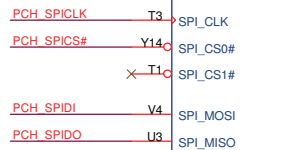
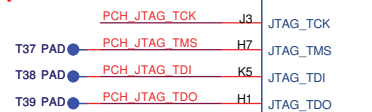
Please close to U2 PCH

8/30 Change U13 from SA000021A00 to SA000031N00 due to EOL of SA000021A00

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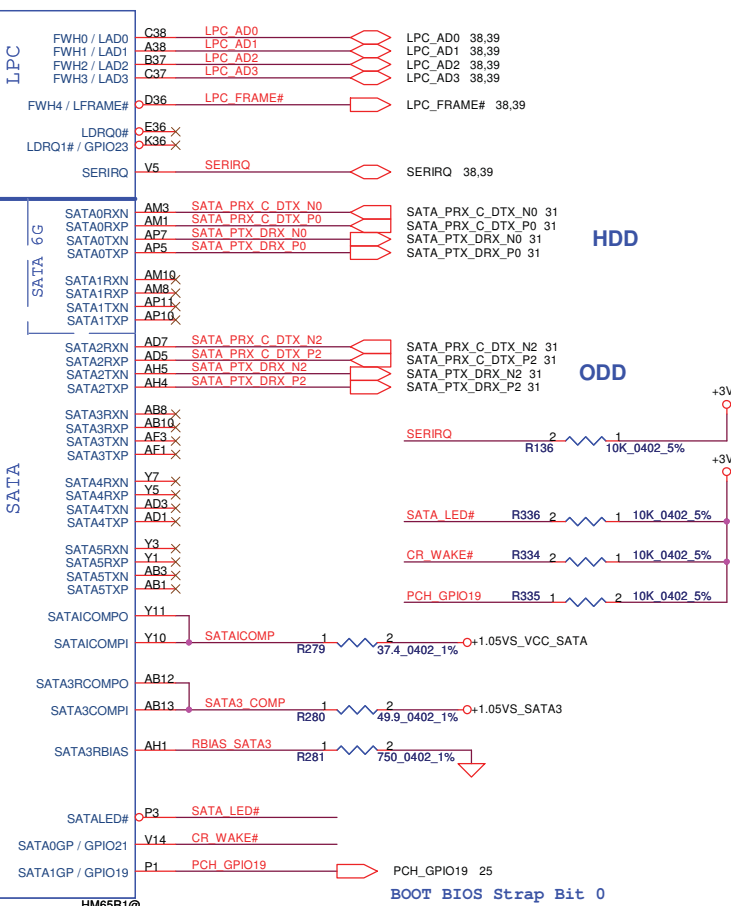
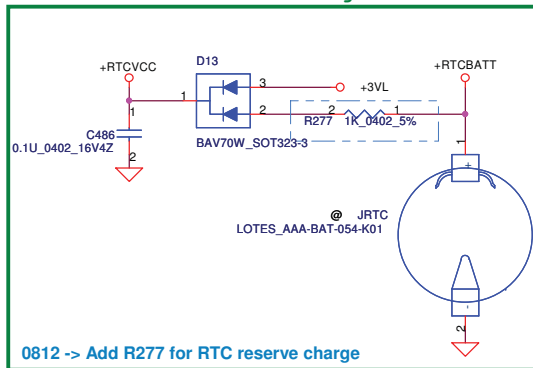


8/30 Change PWRME_CTRL# to HDA_SDO by PCH EDS

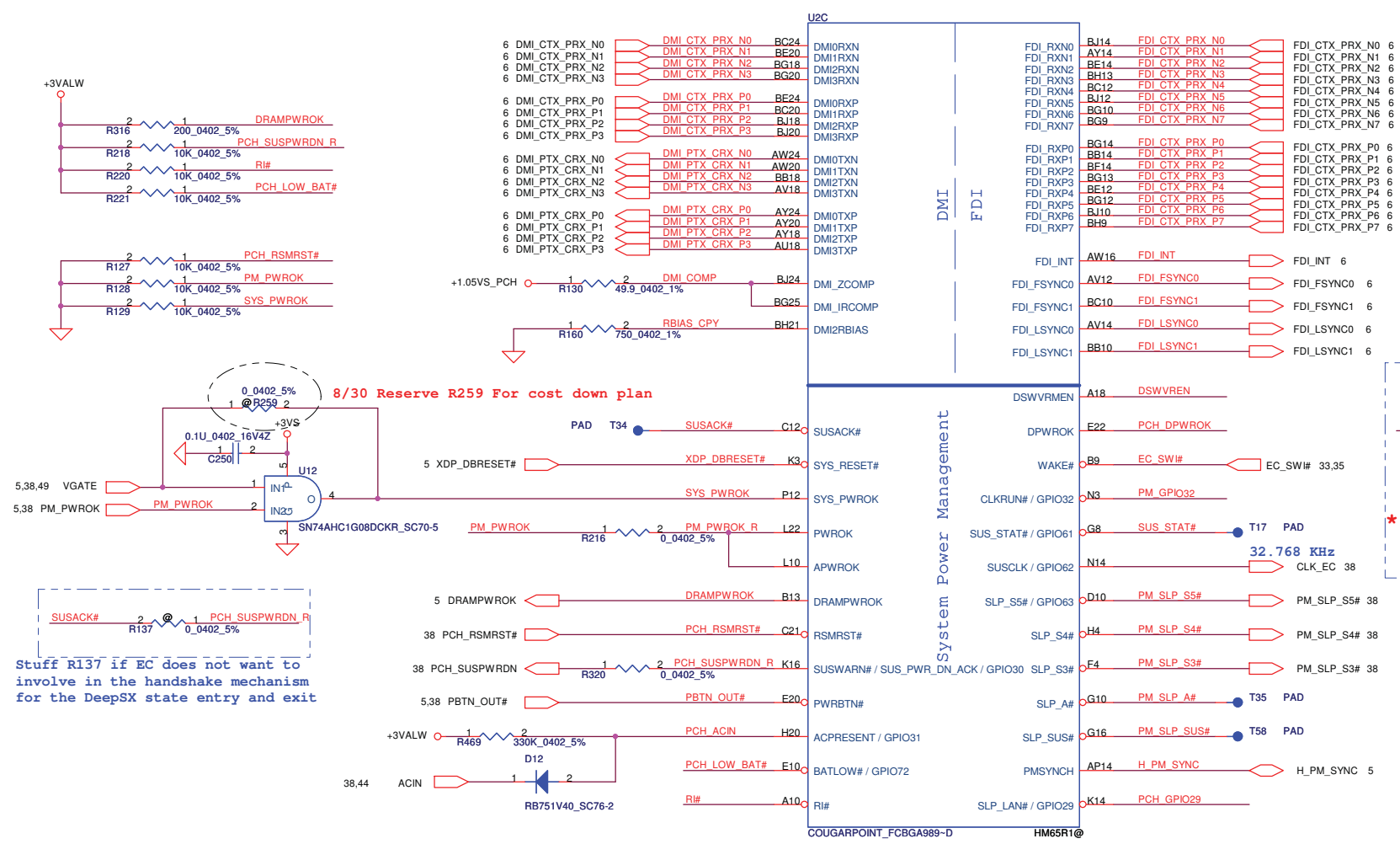


for EMI

RTC schematic for non-chargeable

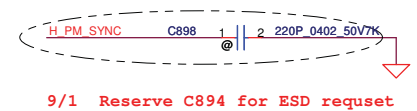
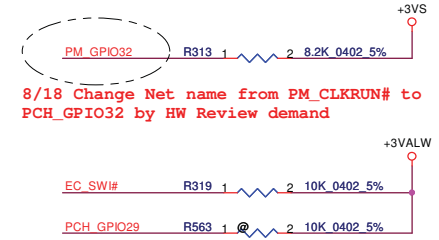


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| Issued Date | | 2010/09/03 | | Deciphered Date | | 2012/12/31 | | Title | | | | | | | |
| | | | | | | | | PCH_HDA/JTAG/SATA/SPI/LPC | | | | | | | |
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| Size | | | | | | | | Document Number | Rev | | | | | | |
| Custom | | | | | | | | PWWHA LA-7201P M/B | 1.0 | | | | | | |
| | | | | Date: | | Friday, March 04, 2011 | | Sheet | 21 of 53 | | | | | | |

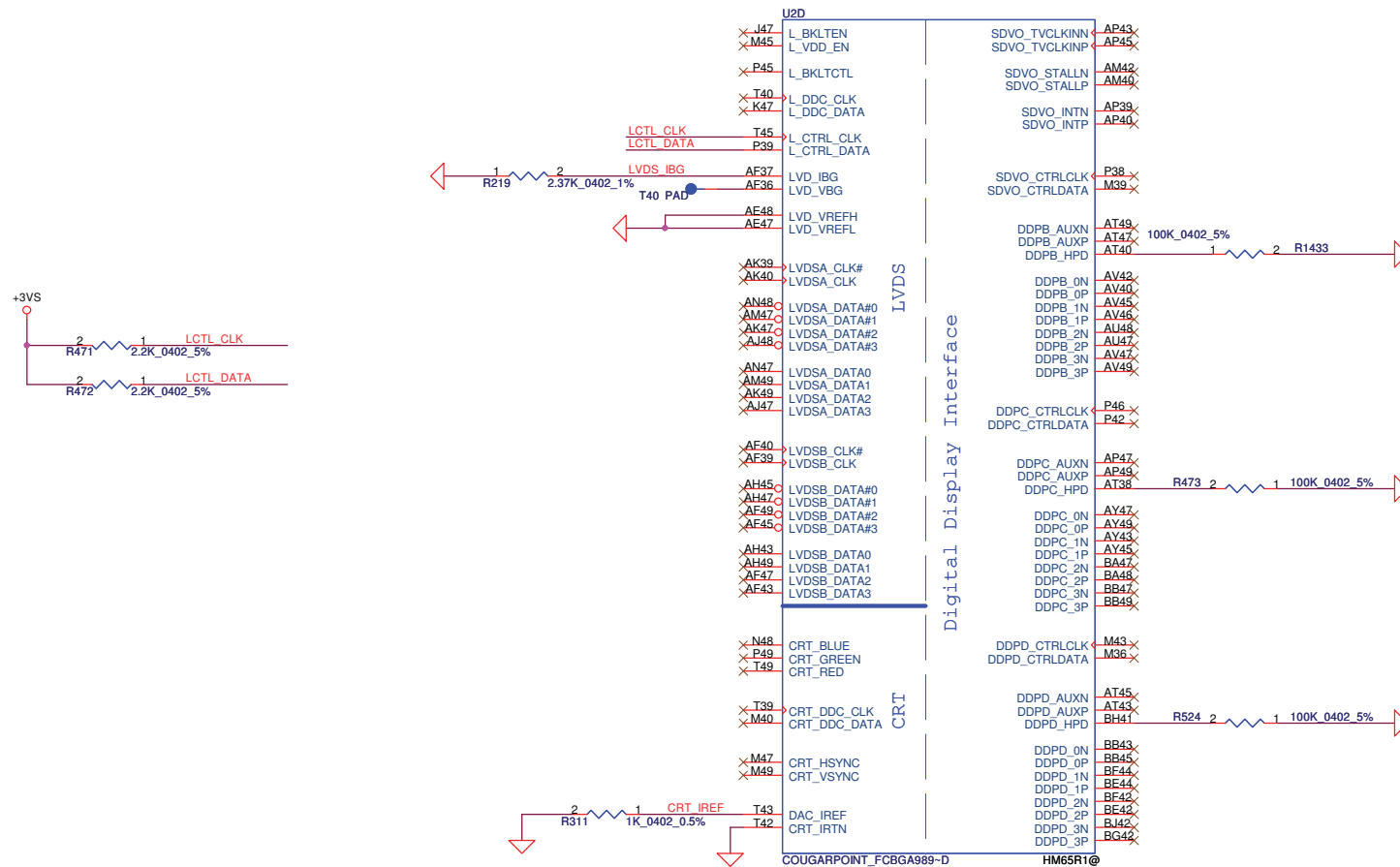


Stuff R222 if do not support DeepSX state

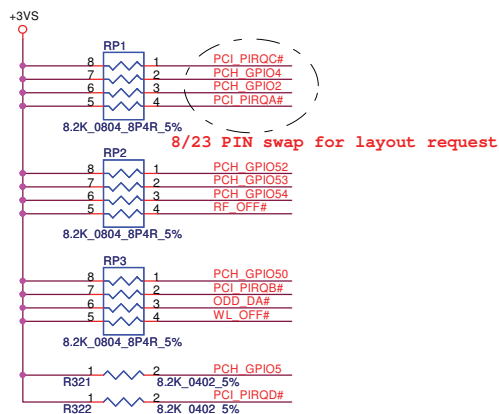
DSWVREN must be always pulled high to +RTCVCC
 ★ DSWVREN - Internal Deep Sleep 1.05V regulator
 H : Enable
 L : Disable



| | | | | | |
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| | | | | PCH_DMI/FDI/PM | |
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| | | | | Custom | 1.0 |
| | | | | Date | Friday, March 04, 2011 |
| | | | | Sheet | 23 of 53 |



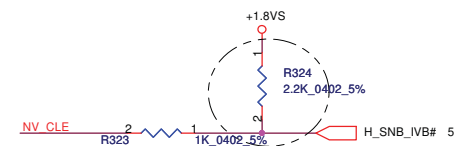
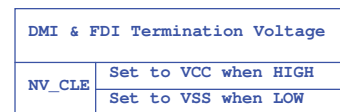
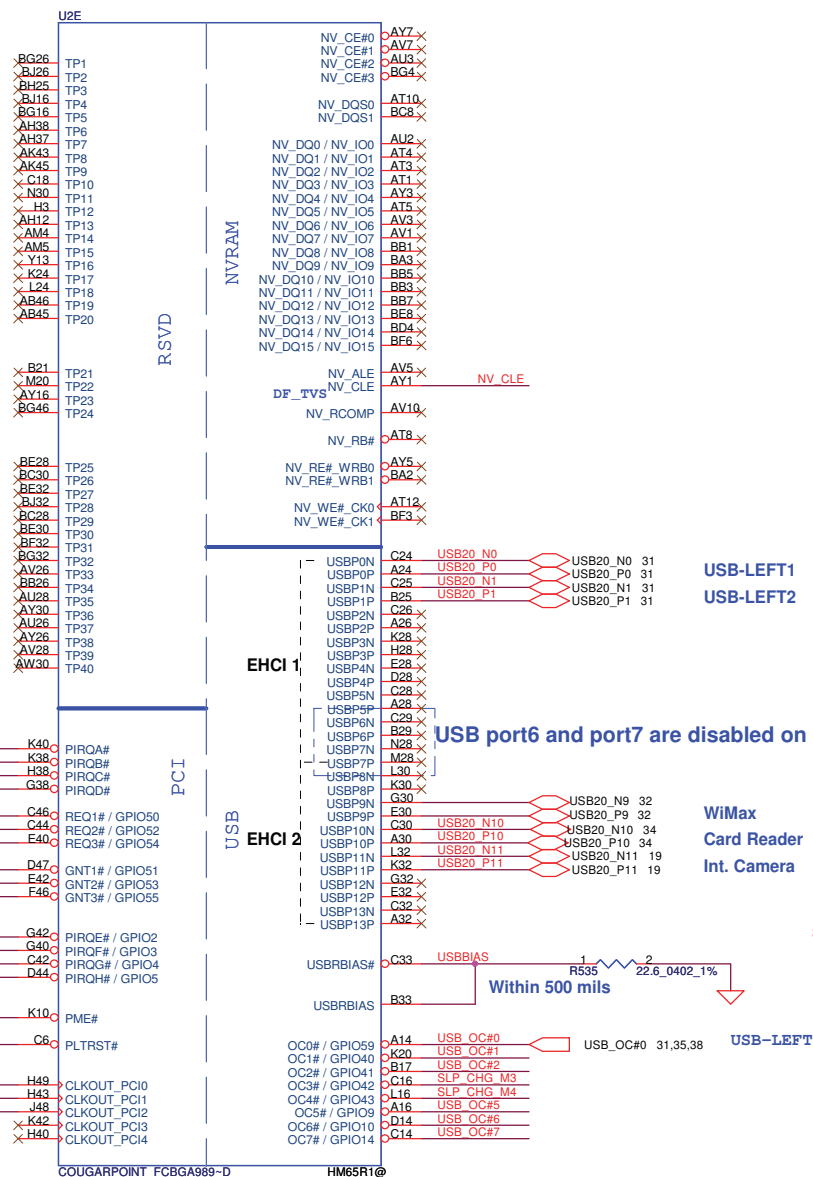
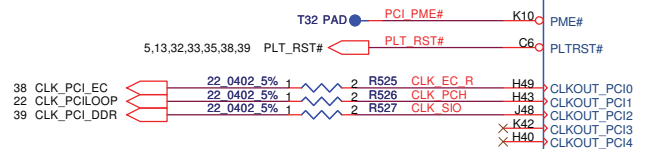
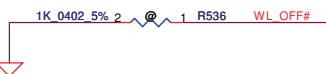
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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/09/03 | Deciphered Date | 2012/12/31 | Title | |
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| Size | Custom | Document Number | PWWHA LA-7201P M/B | Rev | 1.0 |
| Date: | Friday, February 25, 2011 | Sheet | 24 | of | 53 |



| Boot BIOS Strap | | |
|-----------------|------------|--------------------|
| RF_OFF# | PCH_GPIO19 | Boot BIOS Loaction |
| 0 | 0 | LPC |
| 0 | 1 | Reserved |
| 1 | 0 | PCI |
| 1 | 1 | SPI ★ |



| A16 Swap Override Strap | |
|-------------------------|--|
| WL_OFF# | * Low= A16 swap override Enable High= A16 swap override Disable |



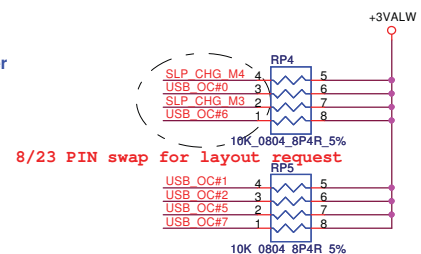
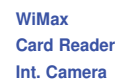
8/18 Change R324 From 1K to 2.2K by
Intel check list demand



9/1 Reserve C895 for ESD request

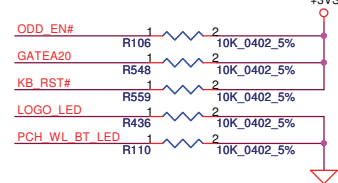
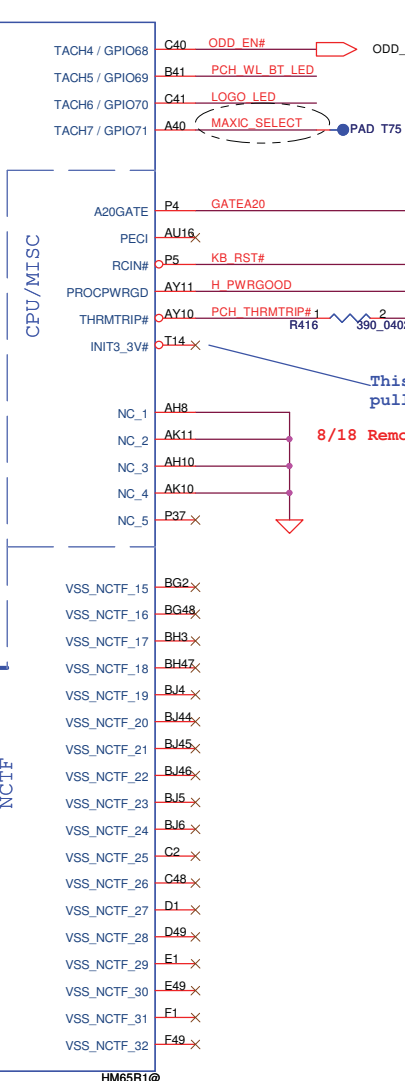
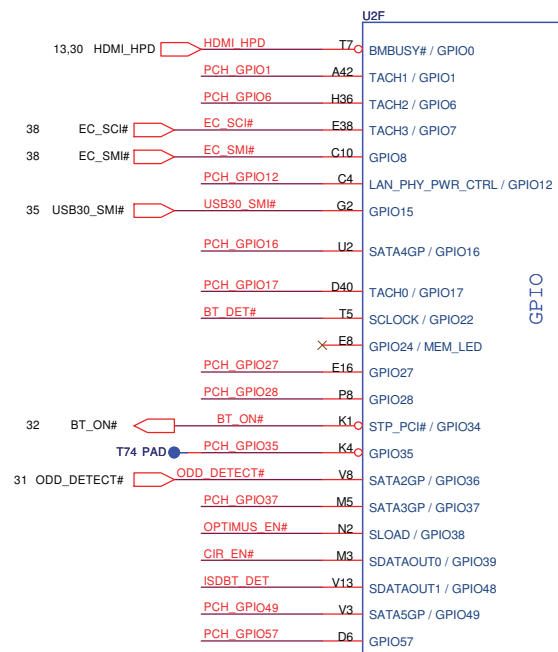
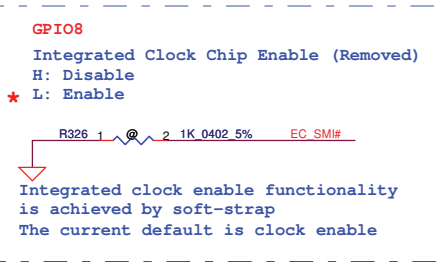
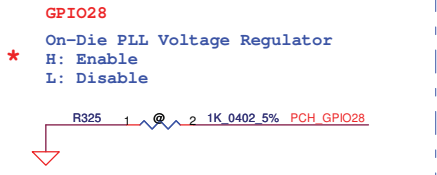
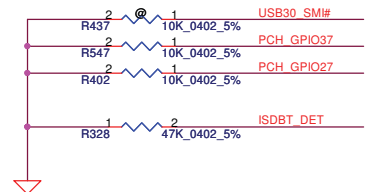
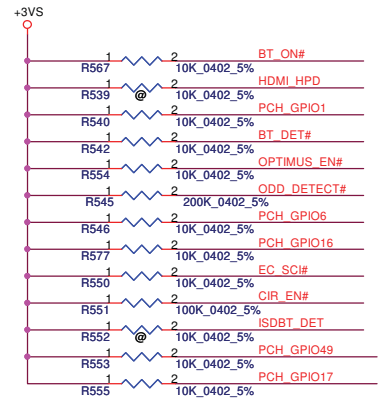
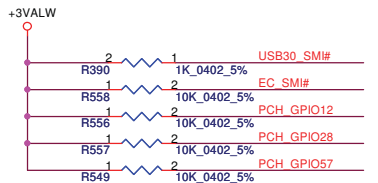


✖ USB port6 and port7 are disabled on HM65



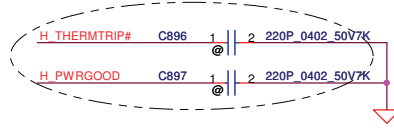
8/23 PIN swap for layout request

| | | | | | |
|---|------------|--------------------|------------|---------------------------|-------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/09/03 | Deciphered Date | 2012/12/31 | Title | PCH_PCI/USB/NAND |
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| | | | | Document Number Custom | |
| | | | | PWWHA LA-7201P M/B | |
| Date: Friday, March 04, 2011 | | [Sheet 25 of 53] | | | |



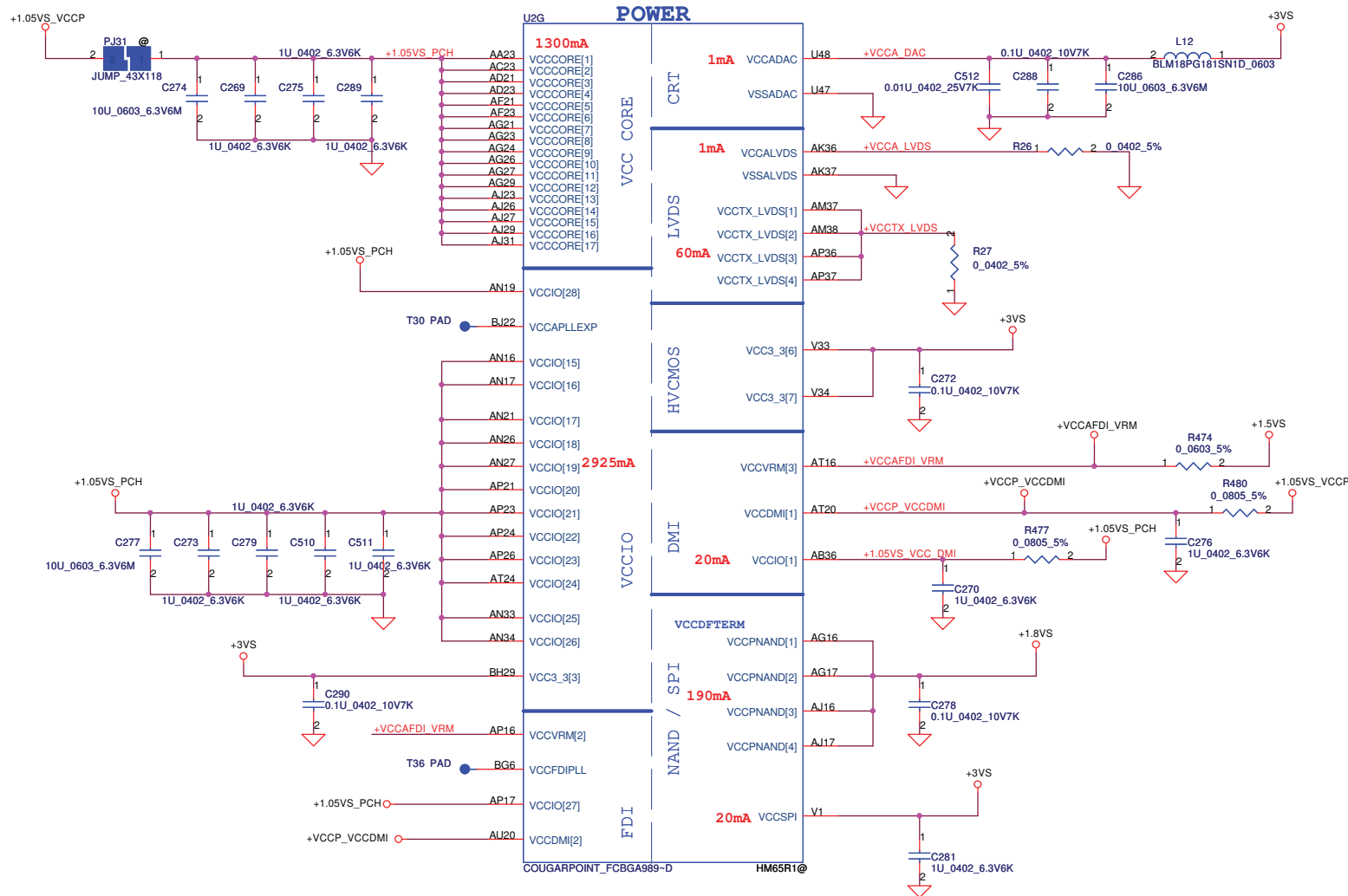
This signal has weak internal pull-up, can't be pulled low

8/18 Remove PCH PECL by HW Review demand



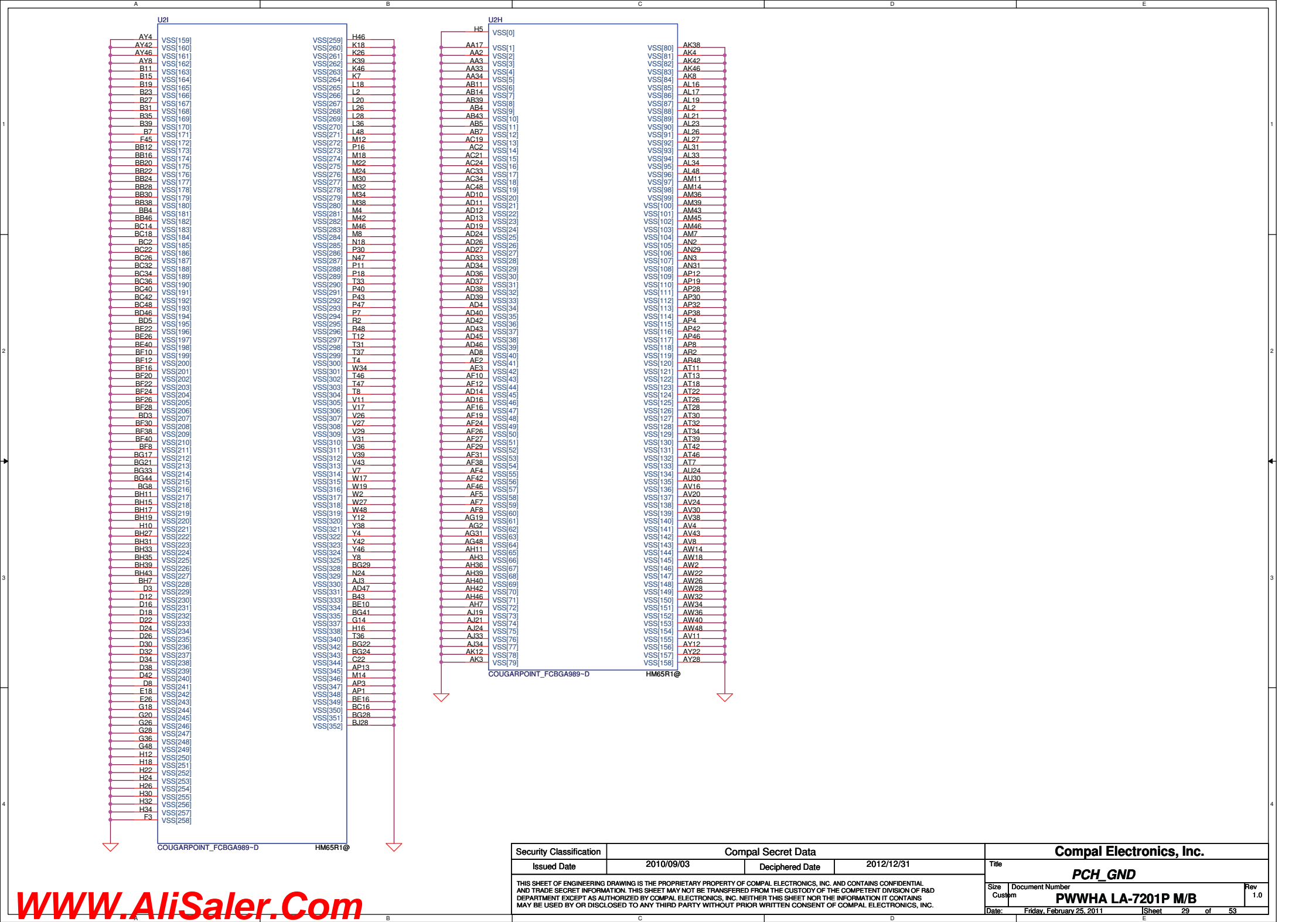
9/1 Reserve C896, C897 for ESD request

| | | | | | | | | | |
|--|--|---------------------|--|---------------------------|--|--------------------------|--|----------|--|
| Security Classification | | Compal Secret Data | | | | Compal Electronics, Inc. | | | |
| Issued Date | | 2010/09/03 | | Deciphered Date | | 2012/12/31 | | Title | |
| <div>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</div> | | PCH_CPU/GPIO | | | | | | | |
| | | Size | | Document Number | | | | Rev | |
| | | Custom | | PWWHA LA-7201P M/B | | | | 1.0 | |
| | | Date: | | Friday, March 04, 2011 | | Sheet | | 26 of 53 | |



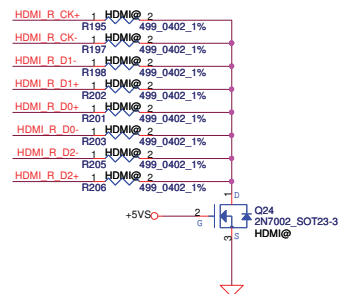
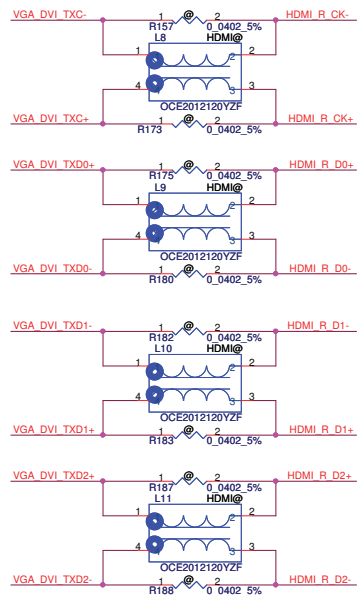
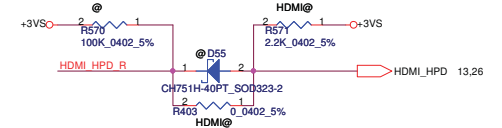
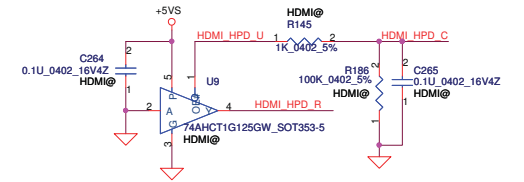
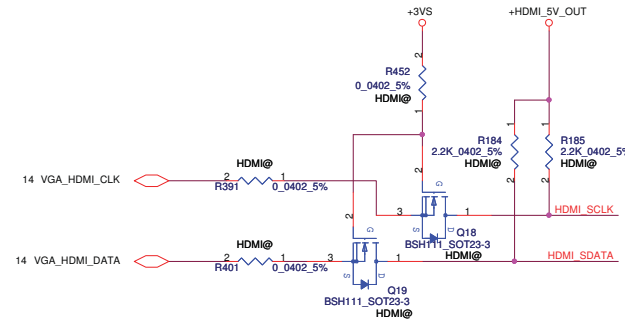
| PCH Power Rail Table | | |
|----------------------|-----------|-----------------------|
| Voltage Rail | Voltage | 50 Iccmax Current (A) |
| V_PROC_IO | 1.05 | 0.001 |
| V5REF | 5 | 0.001 |
| V5REF_SUS | 5 | 0.001 |
| VCC3_3 | 3.3 | 0.266 |
| VCCADAC | 3.3 | 0.001 |
| VCCADPLLA | 1.05 | 0.08 |
| VCCADPLLB | 1.05 | 0.08 |
| VCCCORE | 1.05 | 1.3 |
| VCCDMI | 1.05 | 0.042 |
| VCCIO | 1.05 | 2.925 |
| VCCASW | 1.05 | 1.01 |
| VCCSPI | 3.3 | 0.02 |
| VCCDSW | 3.3 | 0.002 |
| VCCDFTERM | 1.8 | 0.19 |
| VCCRTC | 3.3 | 6 uA |
| VCCSUS3_3 | 3.3 | 0.97 |
| VCCSUSHDA | 3.3 / 1.5 | 0.01 |
| VCCVRM | 1.5 | 0.16 |
| VCCCLKDMI | 1.05 | 0.02 |
| VCCSSC | 1.05 | 0.095 |
| VCCDIFFCLKN | 1.05 | 0.055 |
| VCCALVDS | 3.3 | 0.001 |
| VCCTX_LVDS | 1.8 | 0.06 |

| | | | | | | | | | | | |
|---|--|--------------------|--|-----------------|--|--------------------------|--|---------------------------|--|----------------|--|
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| Issued Date | | 2010/09/03 | | Deciphered Date | | 2012/12/31 | | Title | | | |
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| | | | | | | Size | | Document Number | | Rev | |
| | | | | | | Custom | | PWWHA LA-7201P M/B | | 1.0 | |
| | | | | | | Date | | Friday, February 25, 2011 | | Sheet 27 of 53 | |

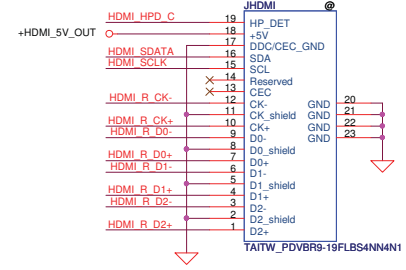


For DISCRETE

| | | | | | | | |
|----|---------------|-------|---|---|-----------------|-------|---------------|
| 14 | VGA_HDMI_CLK+ | CV296 | 1 | 2 | 0.1U_0402_16V7K | HDMI@ | VGA_DVI_TXC+ |
| 14 | VGA_HDMI_CLK- | CV293 | 1 | 2 | 0.1U_0402_16V7K | HDMI@ | VGA_DVI_TXC- |
| 14 | VGA_HDMI_TX0+ | CV294 | 1 | 2 | 0.1U_0402_16V7K | HDMI@ | VGA_DVI_TXD0+ |
| 14 | VGA_HDMI_TX0- | CV297 | 1 | 2 | 0.1U_0402_16V7K | HDMI@ | VGA_DVI_TXD0- |
| 14 | VGA_HDMI_TX1+ | CV299 | 1 | 2 | 0.1U_0402_16V7K | HDMI@ | VGA_DVI_TXD1+ |
| 14 | VGA_HDMI_TX1- | CV298 | 1 | 2 | 0.1U_0402_16V7K | HDMI@ | VGA_DVI_TXD1- |
| 14 | VGA_HDMI_TX2+ | CV295 | 1 | 2 | 0.1U_0402_16V7K | HDMI@ | VGA_DVI_TXD2+ |
| 14 | VGA_HDMI_TX2- | CV300 | 1 | 2 | 0.1U_0402_16V7K | HDMI@ | VGA_DVI_TXD2- |

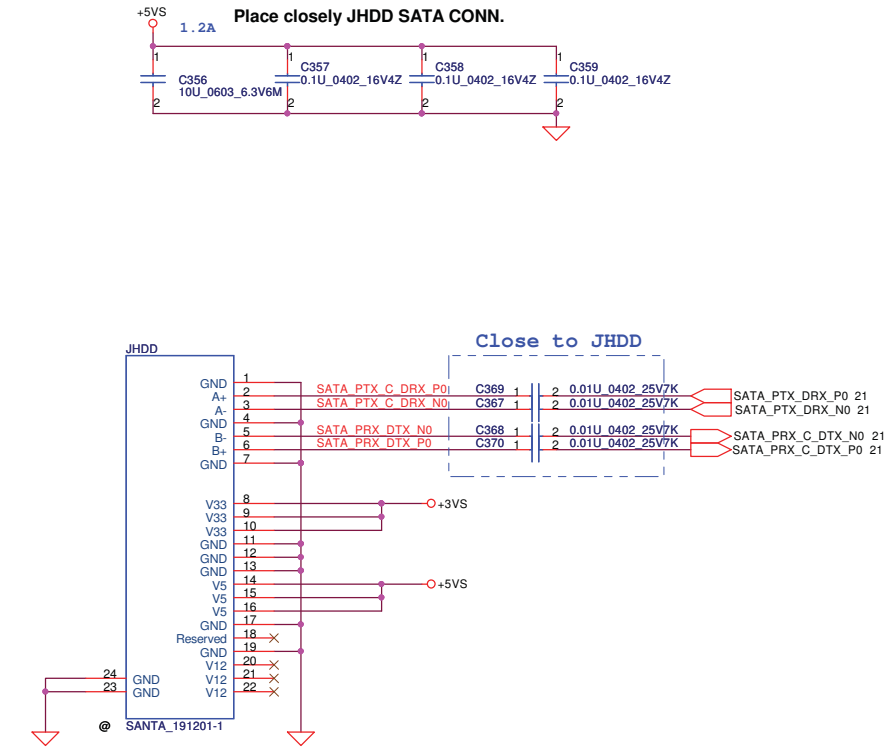


HDMI Connector

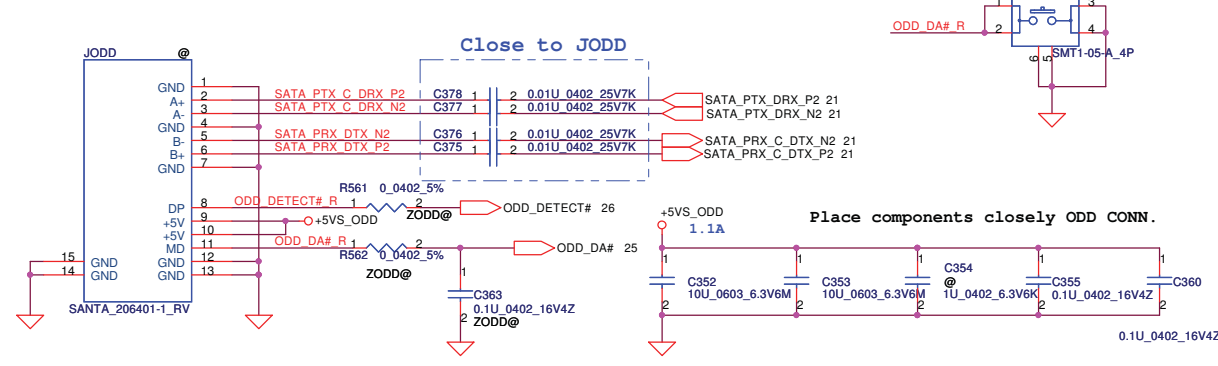


| | | | | | |
|---|------------|--------------------|------------|--------------------------|------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/09/03 | Deciphered Date | 2012/12/31 | Title | HDMI Conn. |
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| | | | | | PWWHA LA-7201P M/B |
| | | | | Date: | Friday, March 04, 2011 |
| | | | | Sheet | 30 of 53 |

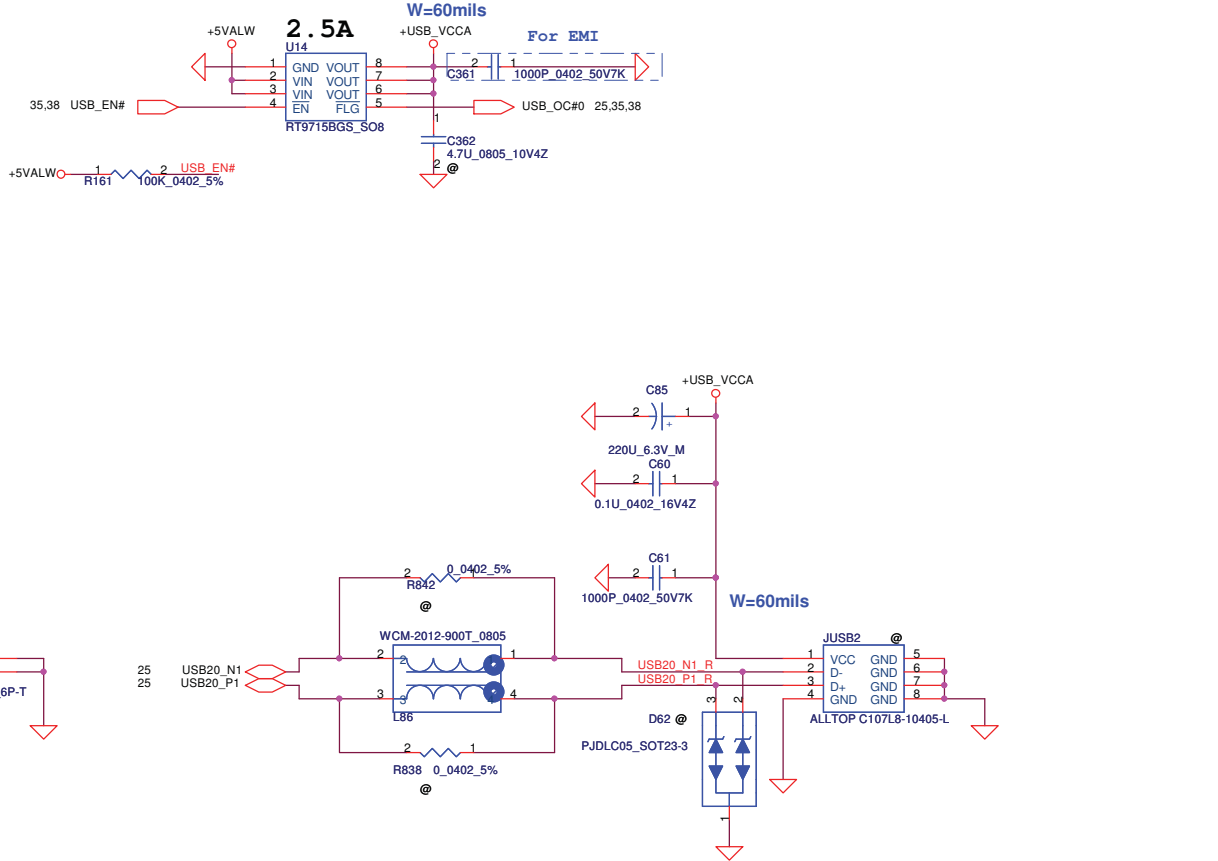
SATA HDD Conn



SATA ODD Conn

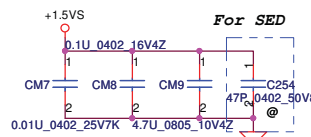
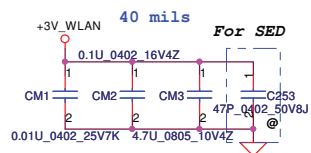
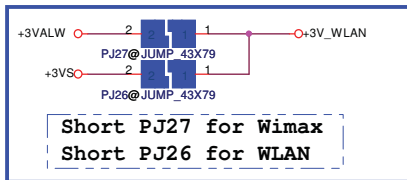


USB Conn



| | | | | | |
|---|------------|--------------------|------------|--------------------------|------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/09/03 | Deciphered Date | 2012/12/31 | Title | |
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| | | | | PWWHA LA-7201P M/B | |
| | | | | Date | Friday, March 04, 2011 |
| | | | | Sheet | 31 of 53 |
| | | | | Rev | 1.0 |

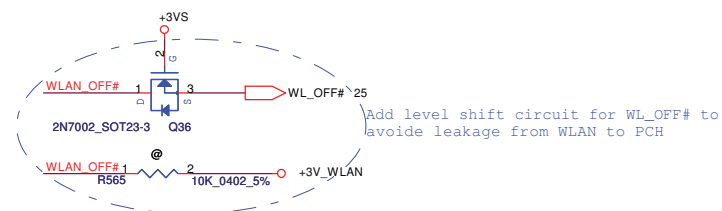
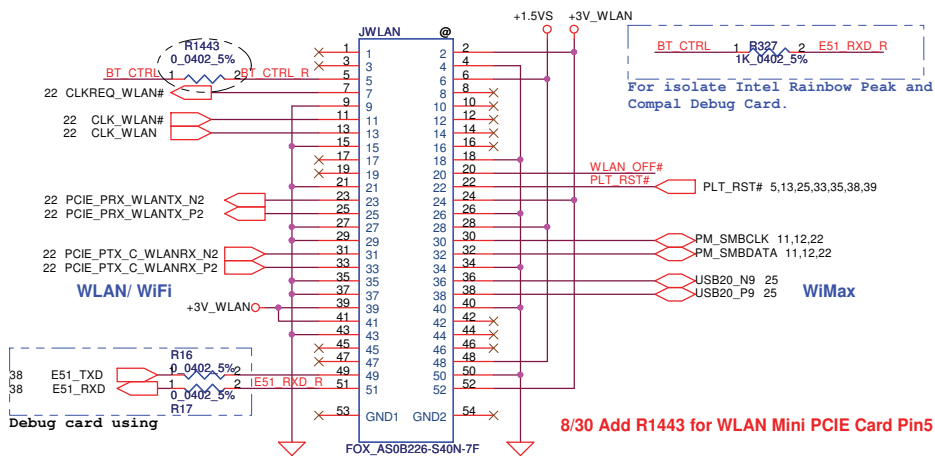
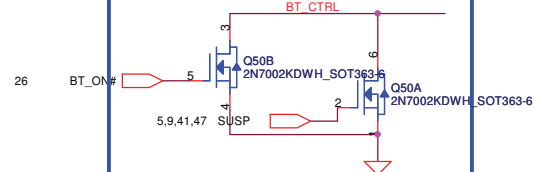
Half PCIe Mini Card-WLAN/ WiMax



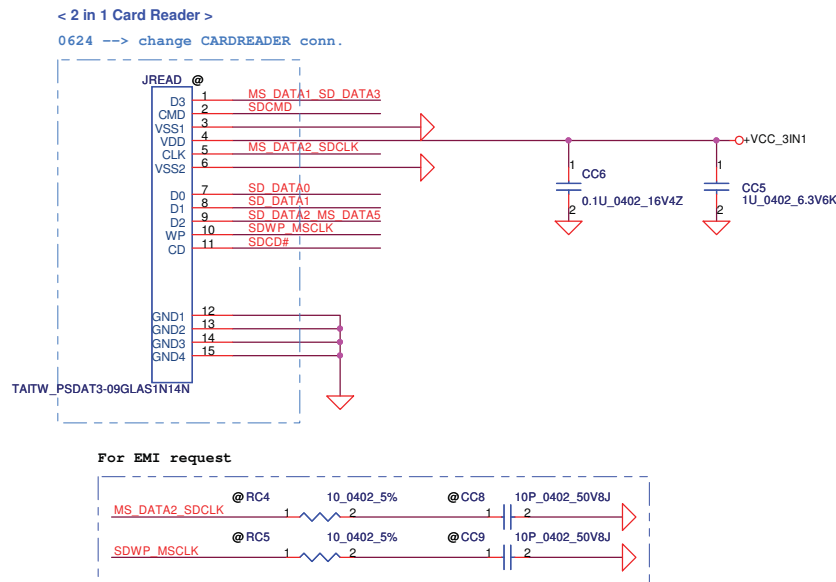
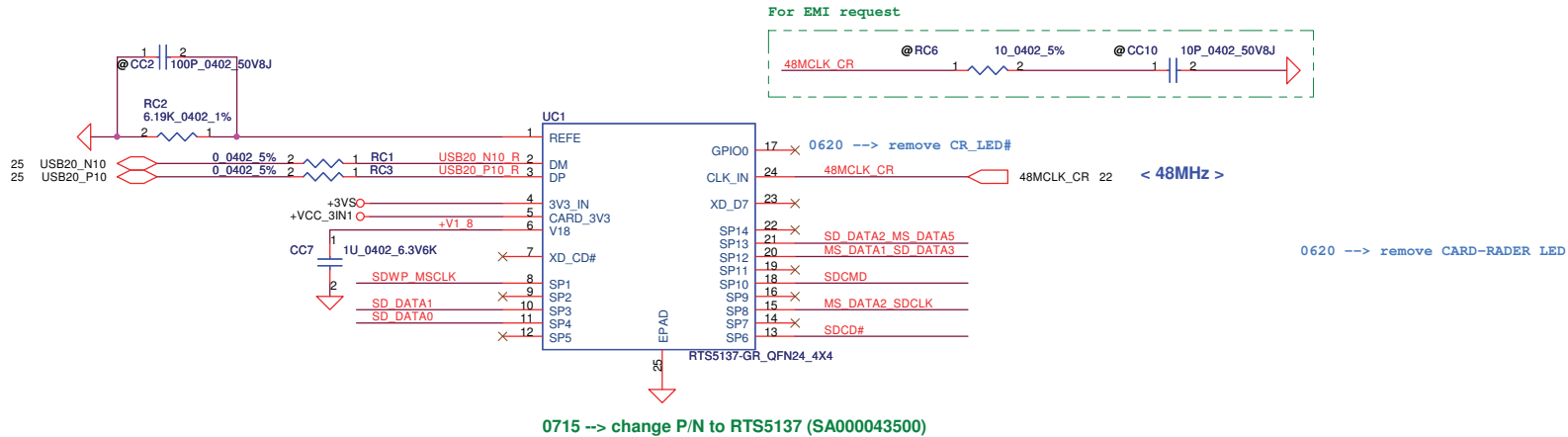
WLAN&BT Combo module circuits

| | BT on module Enable | BT on module Disable |
|---------|---------------------|----------------------|
| BT_CTRL | H | L |
| BT_ON# | L | H |

**If +3V_WLAN is +3VS, please remove D24

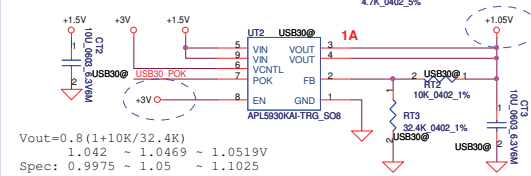


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|---|------------|--------------------|------------|--------------------------|------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/09/03 | Deciphered Date | 2012/12/31 | Title | PCle-WLAN |
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| | | | | Date | Friday, March 04, 2011 |
| | | | | Sheet | 32 of 53 |
| | | | | Rev | 1.0 |

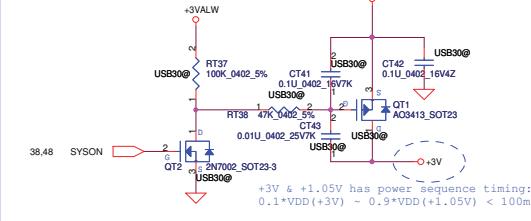


| | | | | | |
|---|------------------------|--------------------|--------------------|--------------------------|-----|
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| Issued Date | 2010/09/03 | Deciphered Date | 2012/12/31 | Title | |
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| Size | Custom | Document Number | PWWHA LA-7201P M/B | Rev | 1.0 |
| Date: | Friday, March 04, 2011 | Sheet | 34 | of | 53 |

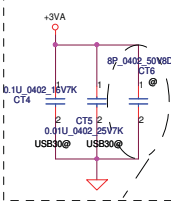
+1.5V to +1.05V Transfer



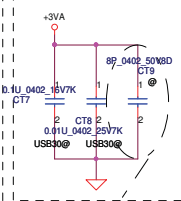
+3VALW to +3V Transfer



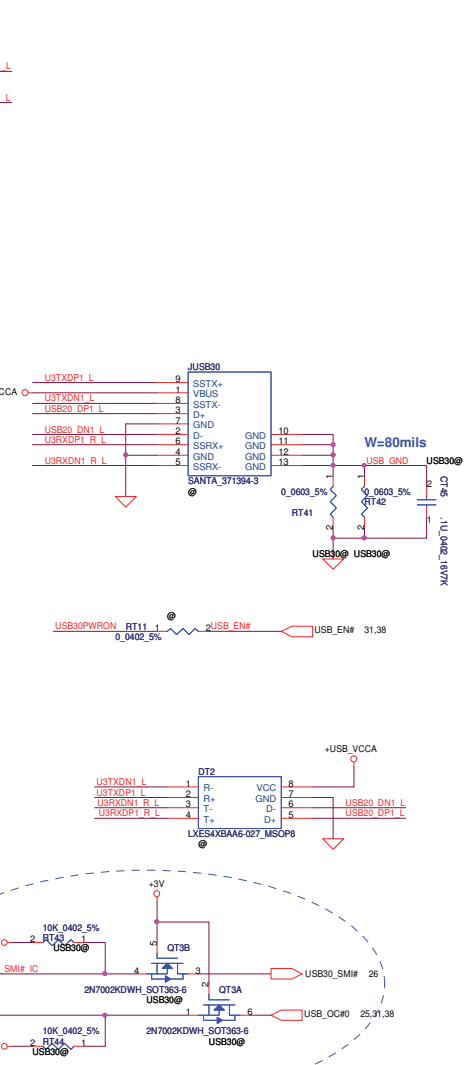
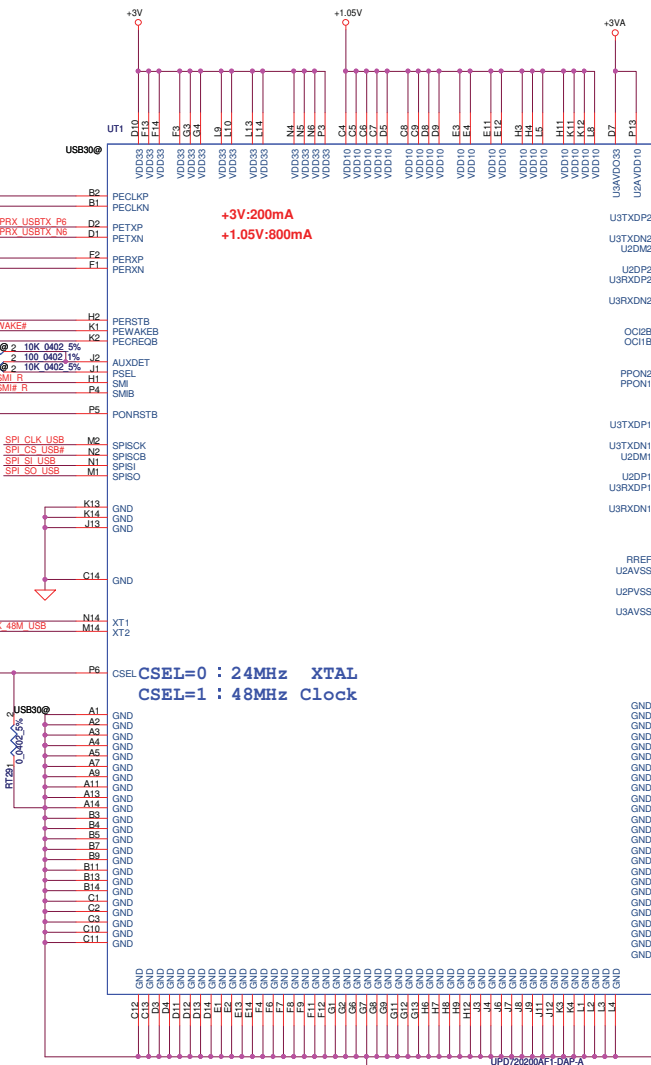
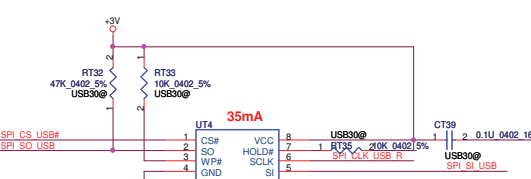
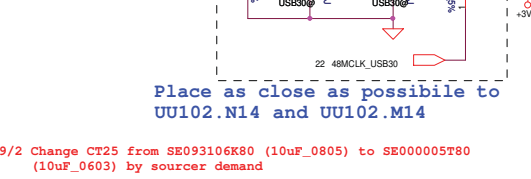
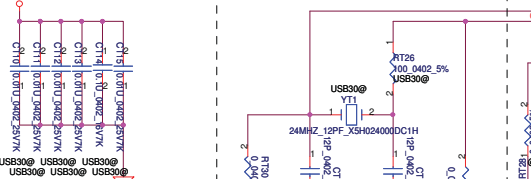
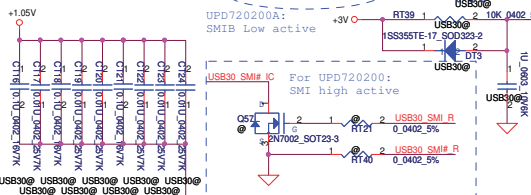
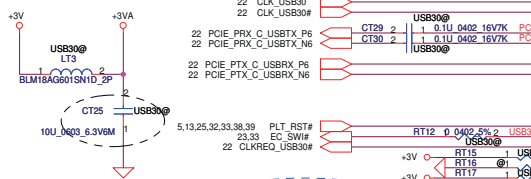
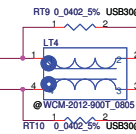
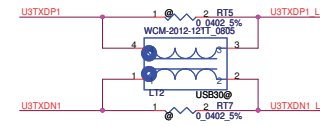
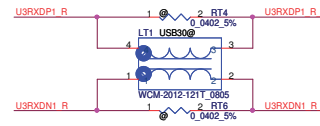
Close to U102.D7



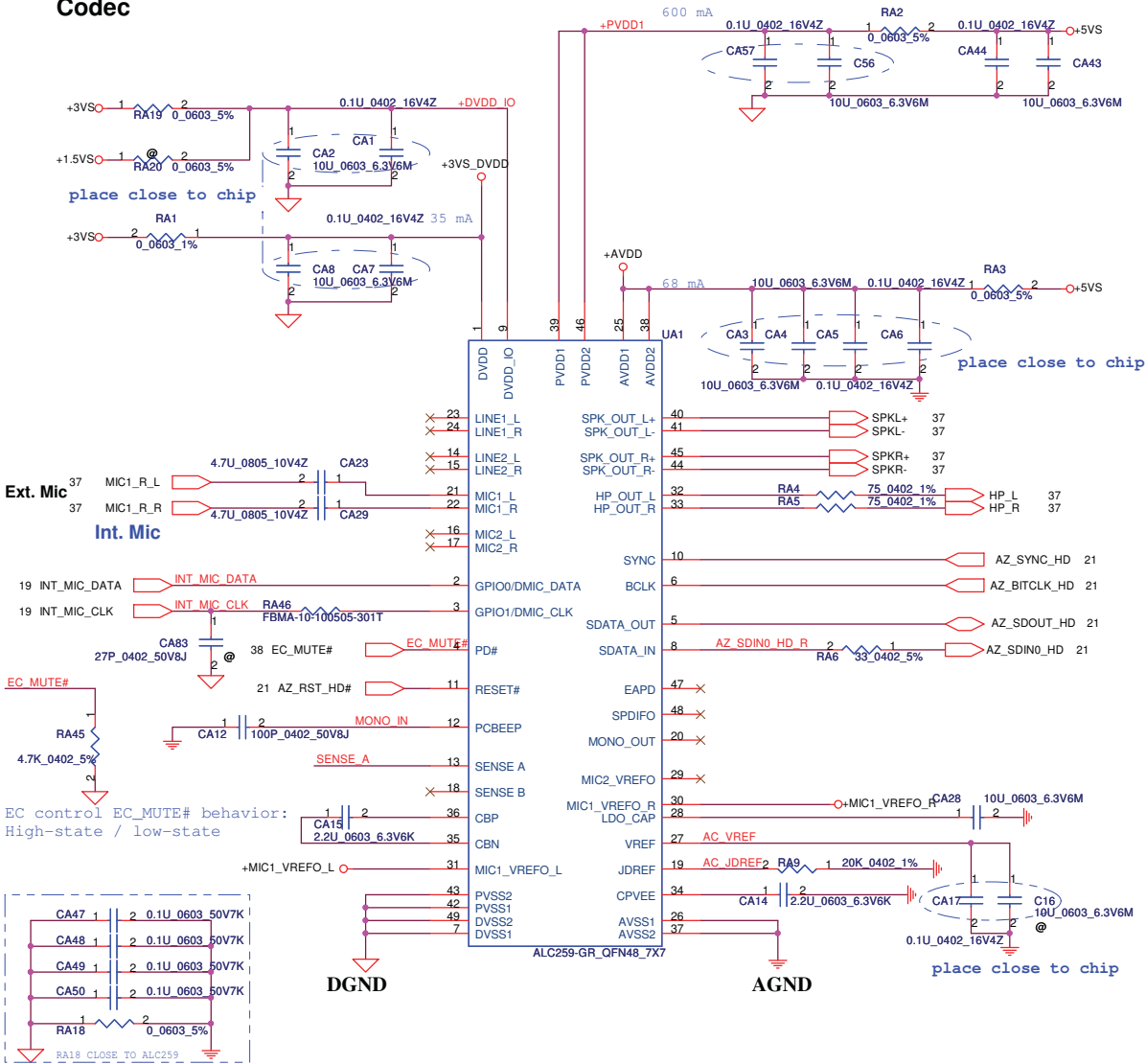
Close to U102.P13



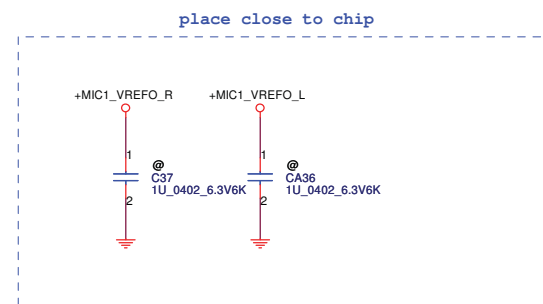
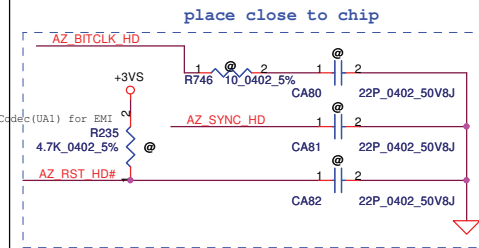
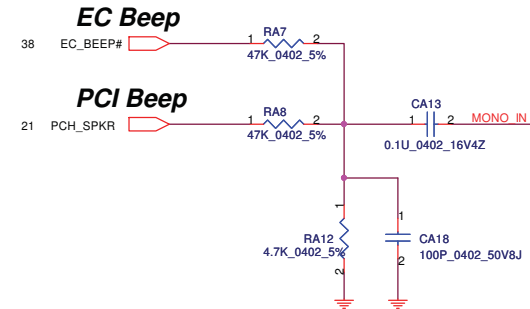
Follow Vendor recommend.



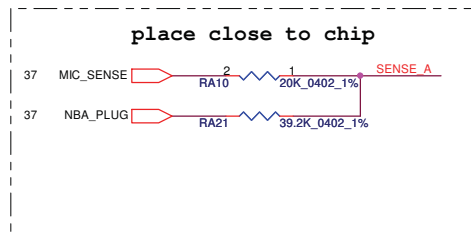
Codec



Beep sound



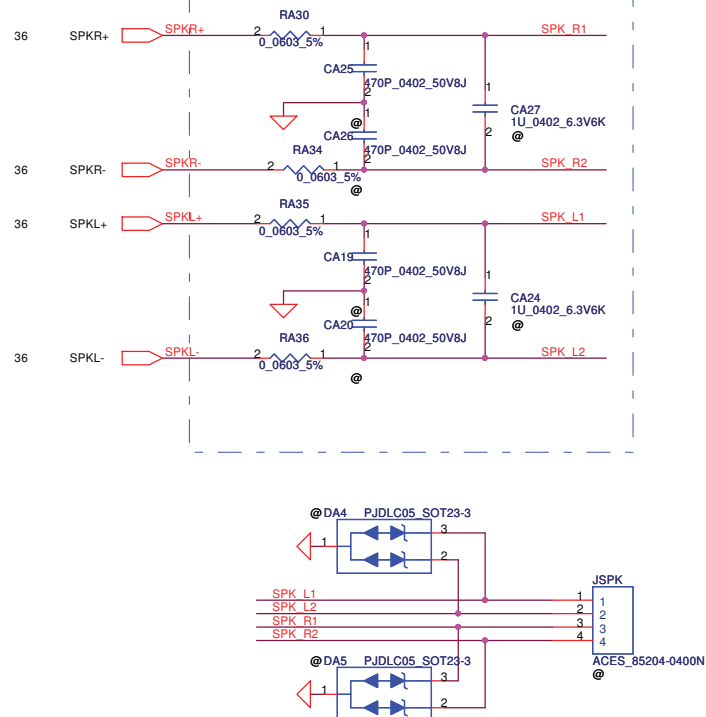
| Sense Pin | Impedance | Codec Signals | Function |
|-----------|-----------|---------------------|---------------|
| SENSE A | 39.2K | PORT-I (PIN 32, 33) | Headphone out |
| | 20K | PORT-B (PIN 21, 22) | Ext. MIC |
| | 10K | PORT-C (PIN 23, 24) | |
| | 5.1K | (PIN 48) | |
| SENSE B | 39.2K | PORT-E (PIN 14, 15) | |
| | 20K | PORT-F (PIN 16, 17) | Int. MIC |
| | 10K | PORT-H (PIN 20) | |



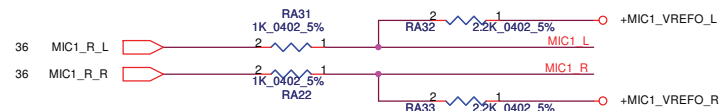
| Security Classification | | | | Compal Secret Data | | | | Compal Electronics, Inc. | | | |
|-------------------------|--|------------------------|--|--------------------|--|------------|--|--------------------------|--|--|--|
| Issued Date | | 2010/09/03 | | Deciphered Date | | 2012/12/31 | | Title | | | |
| | | | | | | | | HD CODEC ALC259 | | | |
| Size | | Document Number | | | | | | PWWHA LA-7201P M/B | | | |
| Date: | | Friday, March 04, 2011 | | Sheet | | 36 | | Rev 1.0 | | | |
| | | | | | | | | of 53 | | | |

Speaker Connector

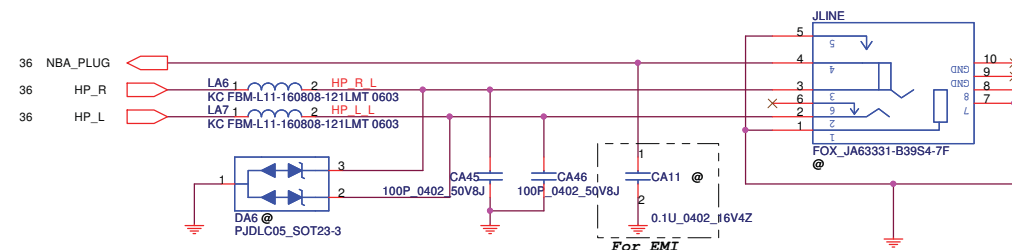
placement near Audio Codec UA1



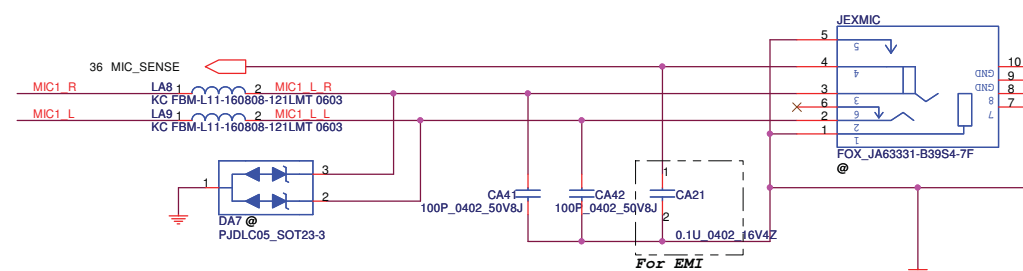
Ext. Mic



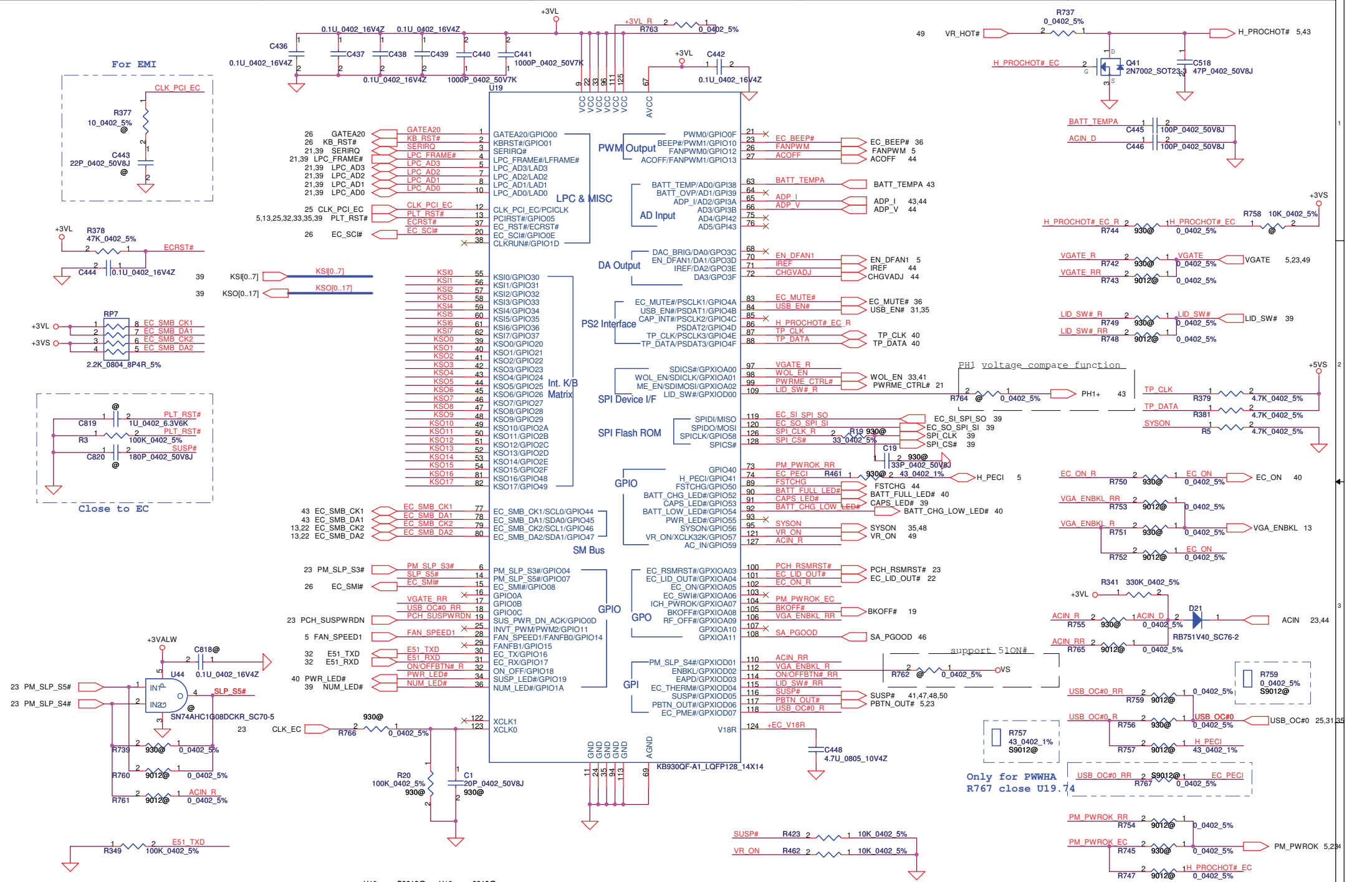
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

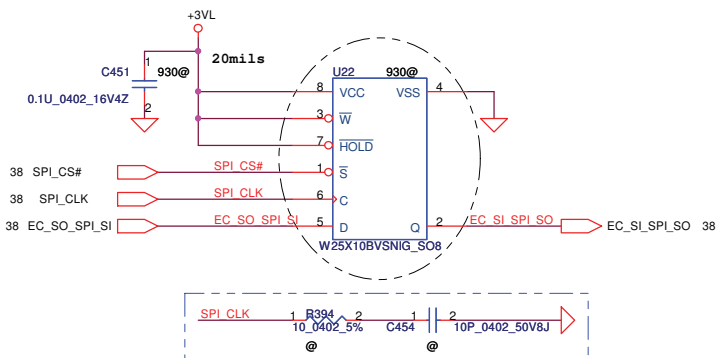


| | | | | | |
|---|------------|------------------------|------------|--------------------------|--|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2010/09/03 | Deciphered Date | 2012/12/31 | Title | |
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| Size | | Document Number | | Rev | |
| Date | | Friday, March 04, 2011 | | Sheet 37 of 53 | |
| PWWHA LA-7201P M/B | | Rev 1.0 | | | |



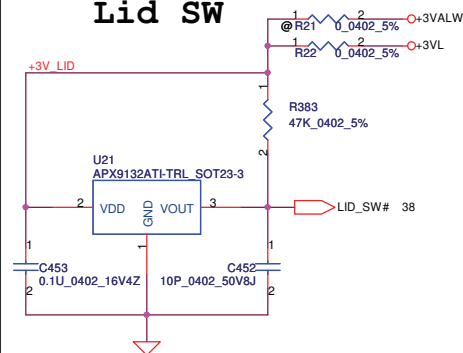
| Security Classification | | | | Compal Secret Data | | | | Compal Electronics, Inc. | | | |
|---|--|------------|--|--------------------|--|------------|--|--------------------------|--|------------------------|--|
| Issued Date | | 2010/09/03 | | Deciphered Date | | 2012/12/31 | | Title | | LPC-EC-KB930 | |
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| | | | | | | | | | | PWWHA LA-7201P M/B | |
| | | | | | | | | | | Rev 1.0 | |
| | | | | | | | | Date | | Friday, March 04, 2011 | |
| | | | | | | | | | | Sheet 38 of 53 | |

SPI Flash (256KB)



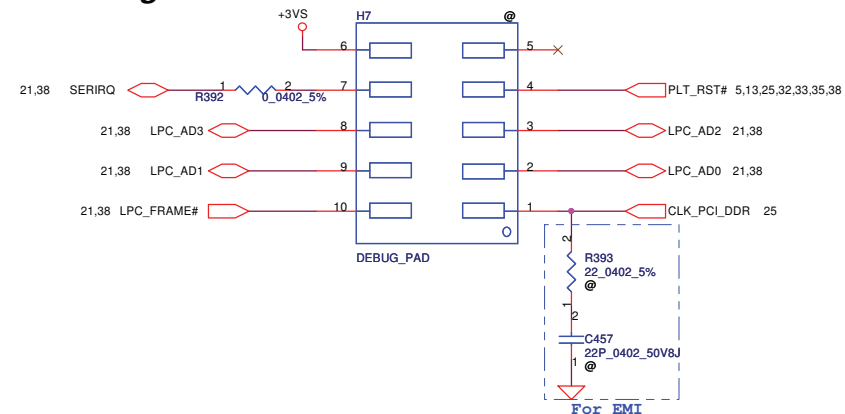
8/30 Change U22 From SA00003GK00 to SA00003GM10 due to EOL of SA00003GK00
9/03 Change U22 change to SA00003FL10

Lid SW



LPC Debug Port

Place the PAD under DDR DIMM.



KEYBOARD CONN.

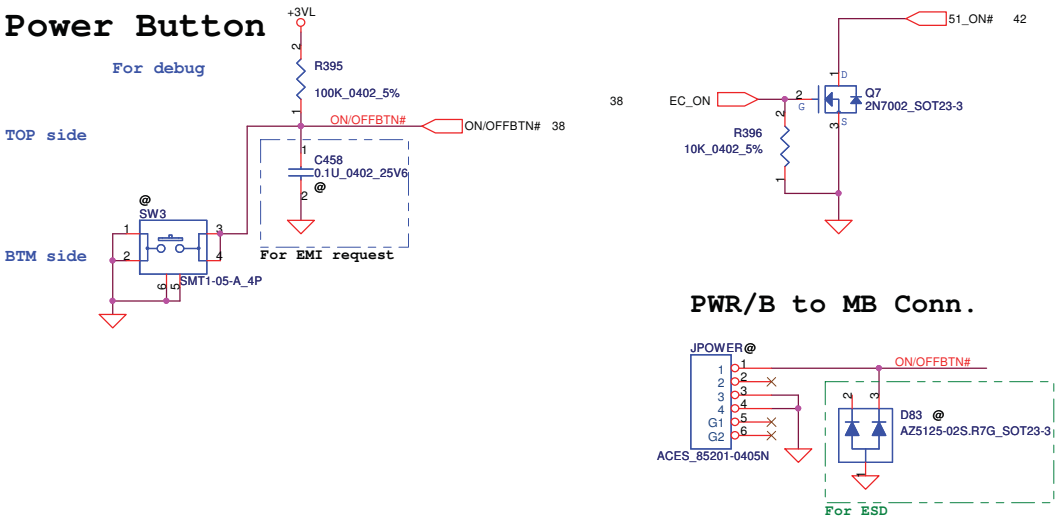
Noticed: KB Connector Pin Definition
Reversed with KB Membrane Pin Definition



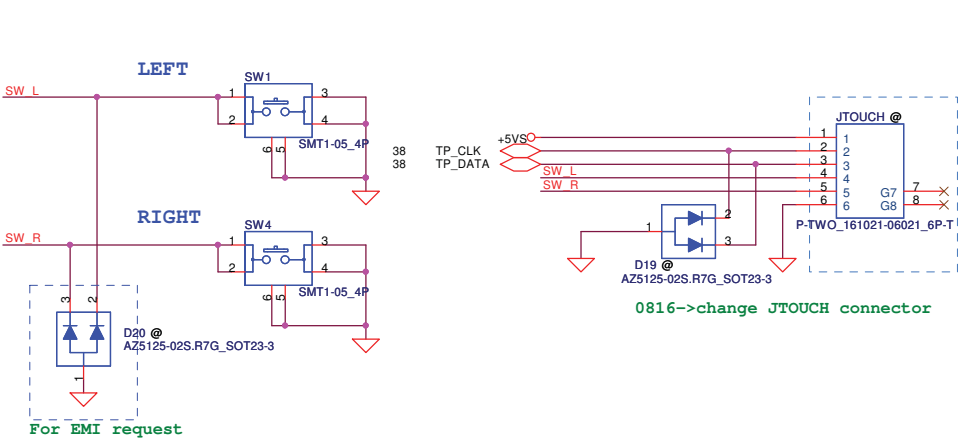
| Security Classification | | | | Compal Secret Data | | | | Compal Electronics, Inc. | | | |
|-------------------------|--|--|--|--------------------|--|-----------------|--|--------------------------|--|------------------------------|--|
| Issued Date | | | | 2010/09/03 | | Deciphered Date | | 2012/12/31 | | Title | |
| | | | | | | | | | | SPI ROM/LID/Debug/KB | |
| | | | | | | | | | | PWWHA LA-7201P M/B | |
| | | | | | | | | | | Rev 1.0 | |
| | | | | | | | | | | Date: Friday, March 04, 2011 | |
| | | | | | | | | | | Sheet 39 of 53 | |

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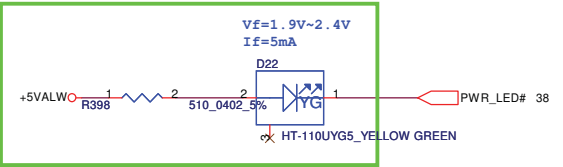
Power Button



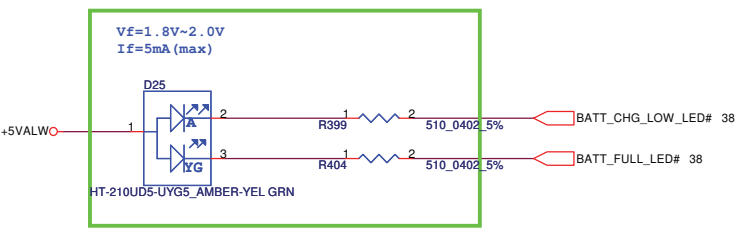
TP Button/Conn.



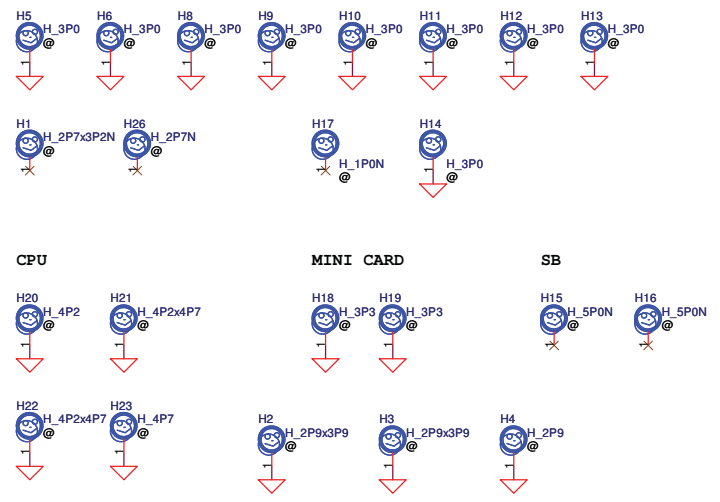
POWER/SUSPEND LED



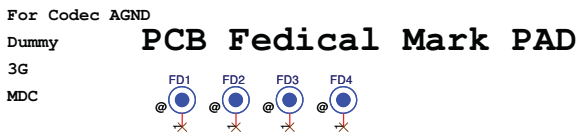
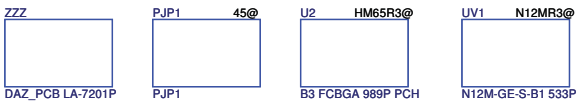
BATT CHARGE/FULL LED



Screw Hole



ISPD



+3VALW TO +3VS

for EMI

0.1U_0402_10V6K

+3VALW

+3VS

Vgs=10V, Id=9A, Rds=18.5mohm

4.7U_0805_10V4Z

1U_0402_6.3V6K

47K_0402_5%

47K_0402_5%

47K_0402_5%

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+5VALW TO +5VS

Vgs=10V, Id=9A, Rds=18.5mohm

4.7U_0805_10V4Z

1U_0402_6.3V6K

47K_0402_5%

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+1.5V to +1.5VS

Only for PWWHA DIS unmount

Vgs=10V, Id=9A, Rds=18.5mohm

4.7U_0805_10V4Z

1U_0402_6.3V6K

47K_0402_5%

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For S3 CPU Power Saving

0.75V_R EN#

46,47 VCCPPWRGD

PS3@

100K_0402_5%

100K_0402_5%

100K_0402_5%

100K_0402_5%

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Each 250pF on CAP_MOS1 (2) will make Slew Rate(uS/V) increase of 100uS/V

38,47,48,50

SUSP#

NLS@

4.7U_0805_10V4Z

1U_0402_6.3V6K

47K_0402_5%

47K_0402_5%

47K_0402_5%

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+5VS TO +5VS_ODD

0.75V_R EN#

46,47 VCCPPWRGD

PS3@

100K_0402_5%

100K_0402_5%

100K_0402_5%

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+3VALW TO +3V_LAN

0.75V_R EN#

46,47 VCCPPWRGD

PS3@

100K_0402_5%

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100K_0402_5%

+1.5V to +1.5V_MEM GFX

0.75V_R EN#

46,47 VCCPPWRGD

PS3@

100K_0402_5%

100K_0402_5%

100K_0402_5%

100K_0402_5%

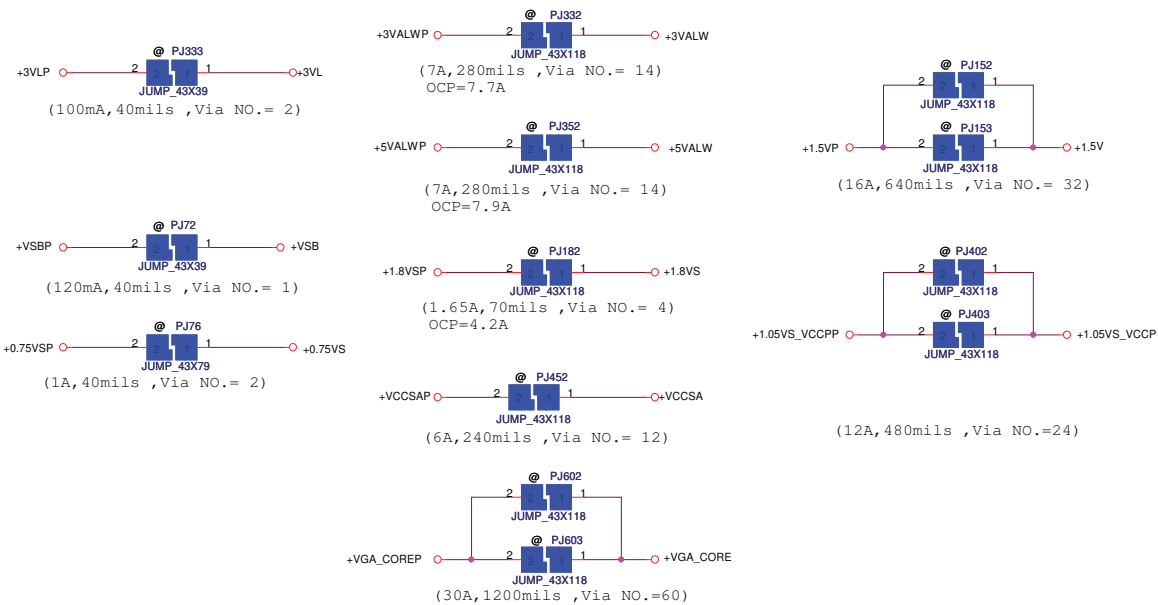
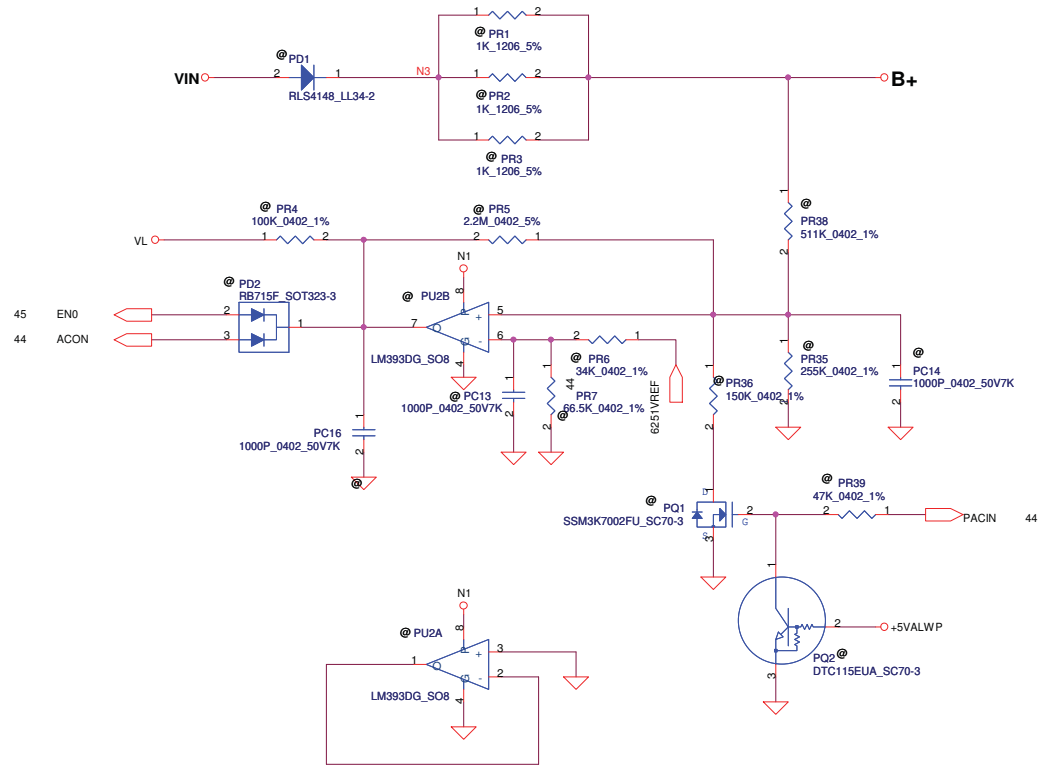
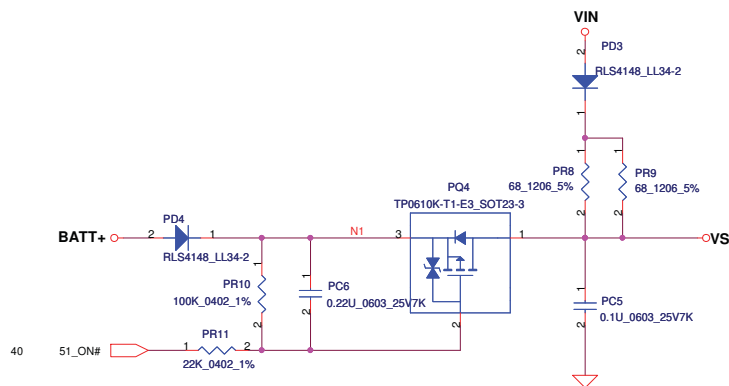
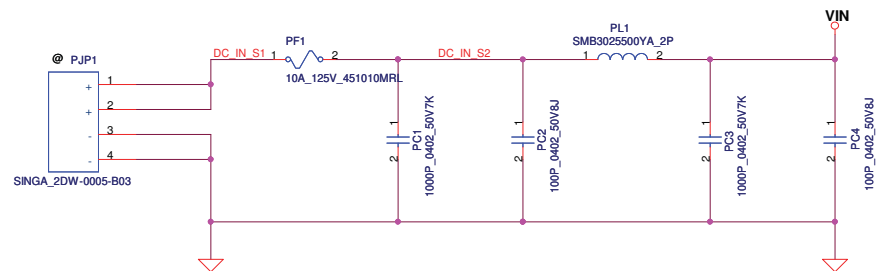
100K_0402_5%

100K_0402_5%

100K_0402_5%

100K_0402_5%

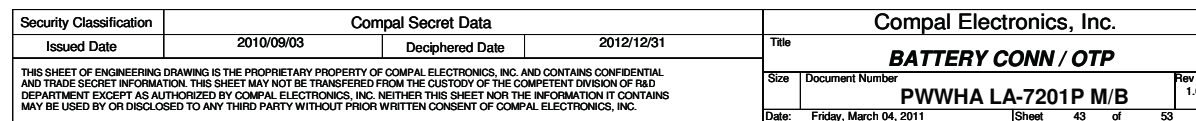
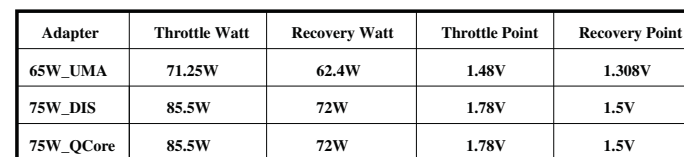
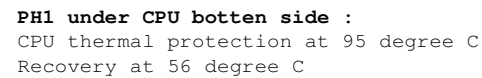
100K_0402_5%



| ACIN | | | |
|--------------------|--------|--------|--------|
| Precharge detector | | | |
| | Min. | typ. | Max. |
| H-->L | 14.42V | 14.74V | 15.23V |
| L-->H | 15.39V | 15.88V | 16.39V |

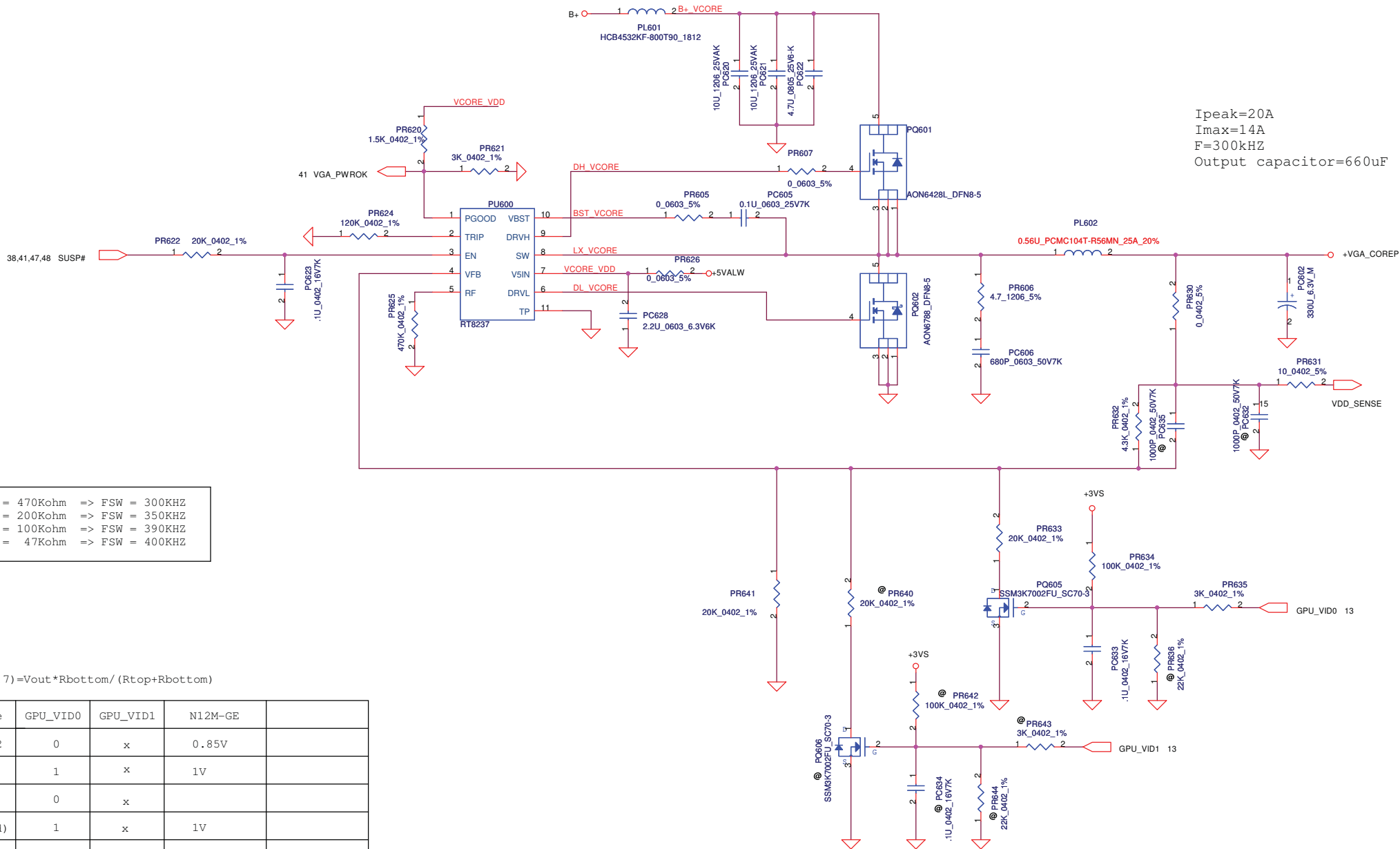
| | | | | | | | | | | | | | |
|---|--|--------------------|--|-----------------|--|------------------------------|--|-----------------|--|--------------------|--|------------|--|
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| | | | | | | Size | | Document Number | | PWWHA LA-7201P M/B | | Rev 1.0 | |
| | | | | | | Date: Friday, March 04, 2011 | | Sheet 42 of 53 | | | | | |

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| Issued Date | | | | 2010/09/03 | | Deciphered Date | | 2012/12/31 | | Title | |
| | | | | | | | | | | VGA_CORE | |
| | | | | | | | | | | Size | |
| | | | | | | | | | | Document Number | |
| | | | | | | | | | | PWWHA LA-7201P M/B | |
| | | | | | | | | | | Rev | |
| | | | | | | | | | | 1.0 | |
| | | | | | | | | | | Date | |
| | | | | | | | | | | Friday, March 04, 2011 | |
| | | | | | | | | | | Sheet | |
| | | | | | | | | | | 50 of 53 | |

| | | | | | |
|------------------|--|---------------------------|--|-----------------|--------------------------|
| | 5 | 4 | 3 | 2 | 1 |
| | DATE | PAGE | MODIFICATION LIST | | PURPOSE |
| D | 2010/12/31 (PVT) | P36 Charger | add snubber PR206,PC206 | | EMI command |
| | 2010/12/31 (PVT) | P36 Charger | change boost to 2.2 ohm PR205 | | EMI command |
| | 2010/12/31 (PVT) | P35 +3VALW/+5VALW | add snubber PR336,PC336,PR356,PC336 | | EMI command |
| | 2010/12/31 (PVT) | P37 +1.5VP/+1.8VSP | Change PR155,PR165 to 0 ohm | | EMI command |
| C | 2010/12/31 (PVT) | P37 +1.5VP/+1.8VSP | Change PQ151 to POK 5*6 | | EMI command |
| | 2010/12/31 (PVT) | P37 +1.5VP/+1.8VSP | Reserve snubber PR156,PC156 | | EMI command |
| | 2010/12/31 (PVT) | P37 +1.5VP/+1.8VSP | add PC165 for MEI | | EMI command |
| | 2010/12/31 (PVT) | P37 +VCCSA | add snubber PR456,PC456 | | EMI command |
| B | 2010/12/31 (PVT) | P38 +1.05VS/+0.75 | change PRQ401 to POK 5x6 | | EMI command |
| | 2010/12/31 (PVT) | P38 +1.05VS/+0.75 | change PR405,PR510 to 0 ohm | | EMI command |
| | 2010/12/31 (PVT) | P38 +1.05VS/+0.75 | change 0.75V enable PR279 tp PR282 | | HW command |
| | 2010/12/31 (PVT) | P39 +CPU_CORE | change PC549,PC515,PC525 to correct rating | | design change |
| A | 2010/12/31 (PVT) | P39 +CPU_CORE | change PL503,PL504 to DCR 5% | | design change |
| | 2010/12/31 (PVT) | P39 +CPU_CORE | change PC568 PC 566 to 5.8mmm capacitor | | design change |
| | 2010/12/31 (PVT) | P39 +CPU_CORE | change PC551 for load line adjust | | design change |
| | 2010/12/31 (PVT) | P39 +CPU_CORE | change PR560 for program temperture | | design change |
| | 2010/12/31 (PVT) | P39 +CPU_CORE | change PC505,PQ503 change to POK5X6 | | design change |
| | 2010/12/31 (PVT) | P40+VGA_CORE | change PU600 to RT8237 | | design change |
| | 2010/12/31 (PVT) | P40+VGA_CORE | change PR605,PR607 to 0ohm | | design change |
| | 2010/12/31 (PVT) | P40+VGA_CORE | change PR601 to POK 5X6 | | EMI command |
| | 2010/12/31 (PVT) | P40+VGA_CORE | change VID0 and VID1 compont chage | | design change |
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| | Issued Date | | 2010/09/03 | Deciphered Date | 2012/12/31 |
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| WWW.AllSaler.Com | Size | | Document Number | | Rev |
| | | | PWWHA LA-7201P M/B | | 1.0 |
| Date: | | Friday, February 25, 2011 | | Sheet | 51 of 53 |

HW PIR (Product Improve Record)

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2010/10/29

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|----|-------|------|------------------------------|-------------------------------------|
| 1 | 10/29 | 17 | SWAP FBA_CMD2 and FBA_CMD11 | Schematic error |
| 2 | 10/29 | 18 | SWAP FBA_CMD18 and FBA_CMD11 | Schematic error |
| 3 | 10/29 | 21 | Chane +3V_SPI to +3VS | Schematic error |
| 4 | 10/29 | 22 | Add R23 for CLK_REQ_VGA# | Reserve pull down for clock request |

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2010/11/11

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|----|-------|-------|----------------------------------|----------------------|
| 1 | 11/03 | 25,31 | Add USB20_N9 & USB20_P9 | Support Wimax |
| 2 | 11/03 | 32 | Co-Lay Giga LAN | Giga LAN support |
| 3 | 11/22 | 22 | Add R584 & R564 for Panel select | For HW common design |
| 4 | 11/22 | 5 | change D86 (SC100001M00) | For HW common design |
| 5 | 11/22 | 5 | cancel D85 @ | For HW common design |
| 6 | 11/24 | 32 | LAN 8105E-VC update to 8105E-VL | For HW common design |

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.4 TO 0.6

GERBER-OUT DATE: 2011/01/18

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|----|-------|-------|---|----------------------------|
| 1 | 01/15 | 14 | Change RV48 BOM structure from @ to HDMI@. | For HDMI function |
| 2 | 01/15 | 15 | Add net name +IFPE_IOVDD & +IFPE_PLLVDD | For HDMI function |
| 3 | 01/15 | 15 | Add LV12,CV160,CV169,CV170,CV173,LV8,CV178,CV159,CV176,CV182,CV215 | For HDMI function |
| 4 | 01/15 | 38 | Add U19 BOM symbol for 9012 | For EC 9012 |
| 5 | 01/15 | 19 | Change R120 from 10Kohm to 47Kohm. | For backlight PWM issue |
| 6 | 01/15 | 35 | Change UT2.6 & RT1 connector from +5VALW to +3V and del CT1. | For LDO leakage issue |
| 7 | 01/15 | 41 | Add Q31 BOM symbol and add BOM structure PS3@. | For power saving function |
| 8 | 01/16 | 13 | Change R25 BOM structure from @ to NHDMI@. | For HDMI function |
| 9 | 01/16 | 38 | Delete U19.123 CLK_EC_R net name | Due to duplicate net name |
| 10 | 01/16 | 38 | Change U19.104 & R745.2 & R747.2 net name from PM_PWROK_R to PM_PWROK_EC. | Due to duplicate net name |
| 11 | 01/18 | 38 | Add R757 & R759 & U19 BOM symbol and add BOM structure S9012@ | For EC9012 solution |
| 12 | 01/18 | 38 | Add R767 and BOM structure S9012@ | For EC9012 solution |
| 13 | 01/19 | 21~29 | Change U2 P/N from SA00003P440 to SA00004EE80. | For PCH P/N update |
| 14 | 01/19 | 21~29 | Change U2 BOM structure from Q65R3@ to HM65R1@. | For BOM structure update |
| 15 | 01/19 | 40 | Add U2 BOM symbol and BOM structure HM65R3@. | For BOM structure update |
| 16 | 01/19 | 33 | Change UL3 to SP050006E00 | For EMI |
| 17 | 01/20 | 5,7,9 | Change C93,R312,U10,Q14,R465,R463,C140 BOM structure to PS3@ | For BOM structure update |
| 18 | 01/20 | 41 | Change Q31 BOM symbol structure from PS3@ to @ | Only for PWWHA DIS unmount |
| 19 | 01/20 | 9 | Change Q46,R449,C179,C472,R420,R455,Q33 BOM structure from @ to PS3@ | Only for PWWHA DIS PS3@ |

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.6 TO 0.7

GERBER-OUT DATE: 2011/02/18

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|----|-------|------|--|---------------------------------|
| 1 | 01/31 | 5 | Change JFAN2.2 connect FAN_SPEED1, JFAN2.3 connect GND | For FAN pin define modification |
| 2 | 02/09 | 5,38 | Change Q5,Q41 from SB570020110 to SB570020020 | For common material |

| | | | | | |
|---|------------|--------------------|------------|--------------------------|--|
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| | | | | Size | |
| | | | | Document Number | |
| | | | | PWWHA LA-7201P M/B | |
| | | | | Rev | |
| | | | | 1.0 | |
| Date: Friday, February 25, 2011 | | | | Sheet 52 of 53 | |

HW PIR (Product Improve Record)

PWWHA LA-7201P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.6 TO 1.0

GERBER-OUT DATE: 2011/02/18

| NO | DATE | PAGE | MODIFICATION LIST |
|----|------|------|-------------------|
|----|------|------|-------------------|

| PURPOSE |
|---------|
|---------|

| | | | | |
|----|-------|----------|---|---------------------------------|
| 1 | 01/31 | 5 | Change JFAN2.2 connect FAN_SPEED1, JFAN2.3 connect GND | For FAN pin define modification |
| 2 | 02/09 | 5,38 | Change Q5,Q41 from SB570020110 to SB570020020 | For common material |
| 3 | 02/17 | 5 | Change C902,R1445,D85,D86,C900,C901,R1444 from mount to @. | For unused PWM FAN |
| 4 | 02/17 | 5 | Change R24 from @ to mount. | For use RPM FAN |
| 5 | 02/17 | 40 | Change R396,Q7 from 930@ to mount. | For EC9012 function |
| 6 | 02/17 | 31 | Add C363 | For solving ODD issue |
| 7 | 02/17 | 31 | Change SW3 from mount to @ | For MP phase |
| 8 | 02/17 | 41 | Change C496,C499,C236,C249,C255 from NLS@ to @ | For low cost power switch |
| 9 | 02/17 | 41 | Change R415,R419 from 47Kohm to 0ohm | For low cost power switch |
| 10 | 02/17 | 40 | Change ZZZ P/N from DA60000L700 to DAZ0II00101 | For MP phase |
| 11 | 02/17 | 41 | Change C252 from SE070104Z80 to SE071121J80 | For low cost power switch |
| 12 | 02/17 | 31 | Change R561,R562,R457,Q53,R441,R440,C471,C217,Q45 from mount to ZODD@ | For zero ODD function |
| 13 | 02/18 | 21~29 | Change U2 P/N from SA00004EE80 to SA00004EES0 | For PCH B3 version |
| 14 | 02/18 | 40 | Change U2 P/N from SA00004EEA0 to SA00004EET0 | For PCH B3 version |
| 15 | 02/22 | 40 | ADD UV1 BOM symbol and BOM structure N12MR3@. | For N12M R3 P/N |
| 16 | 02/22 | 13~16 | ADD UV1 BOM structure N12MR1@. | For N12M R1 P/N |
| 17 | 02/23 | 32,35,41 | Change Q50,Q53,QT3 from SB00000EO00 to SB00000EO10 | For common material |
| 18 | 02/23 | 41 | Change C465,C467 BOM structure from OLS@ to always mount | For low cost power switch |

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