

Thurman Discrete VGA nVidia G86 Schematics Document

uFCPGA Mobile Merom

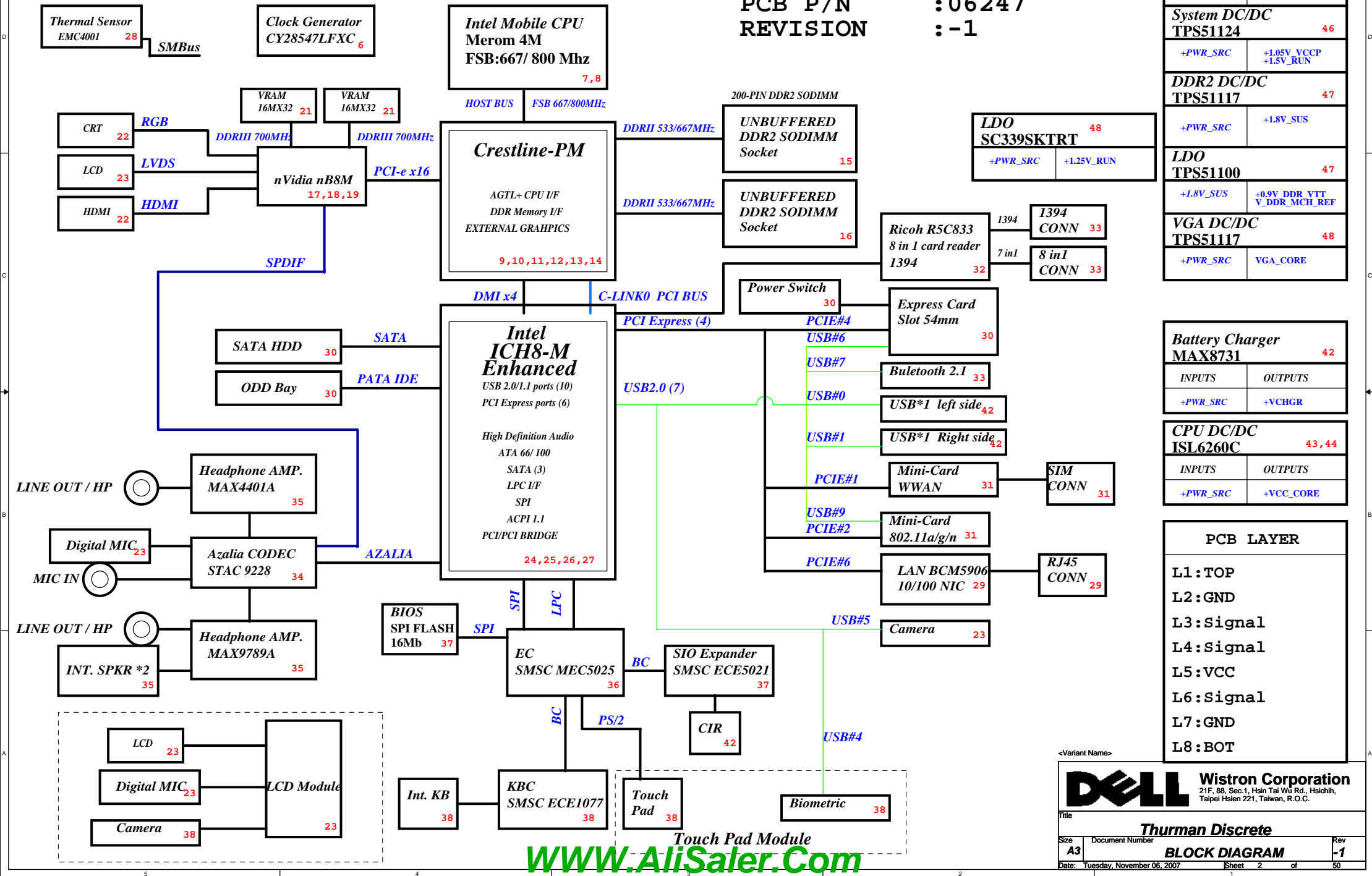
Intel Crestline-PM + ICH8M

2007-11-06

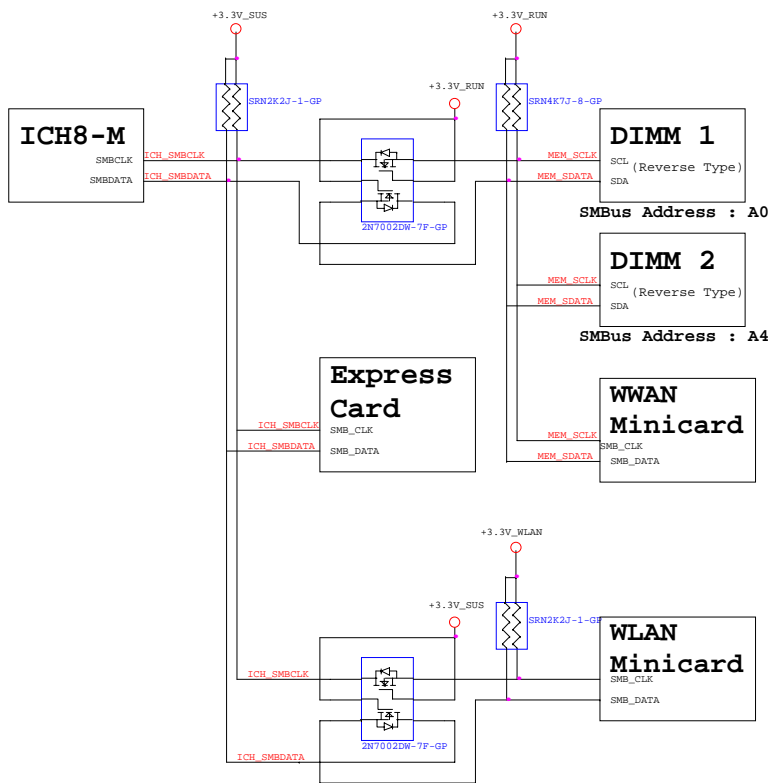
REV : -1(DELL:A00)

Thurman Discrete Block Diagram

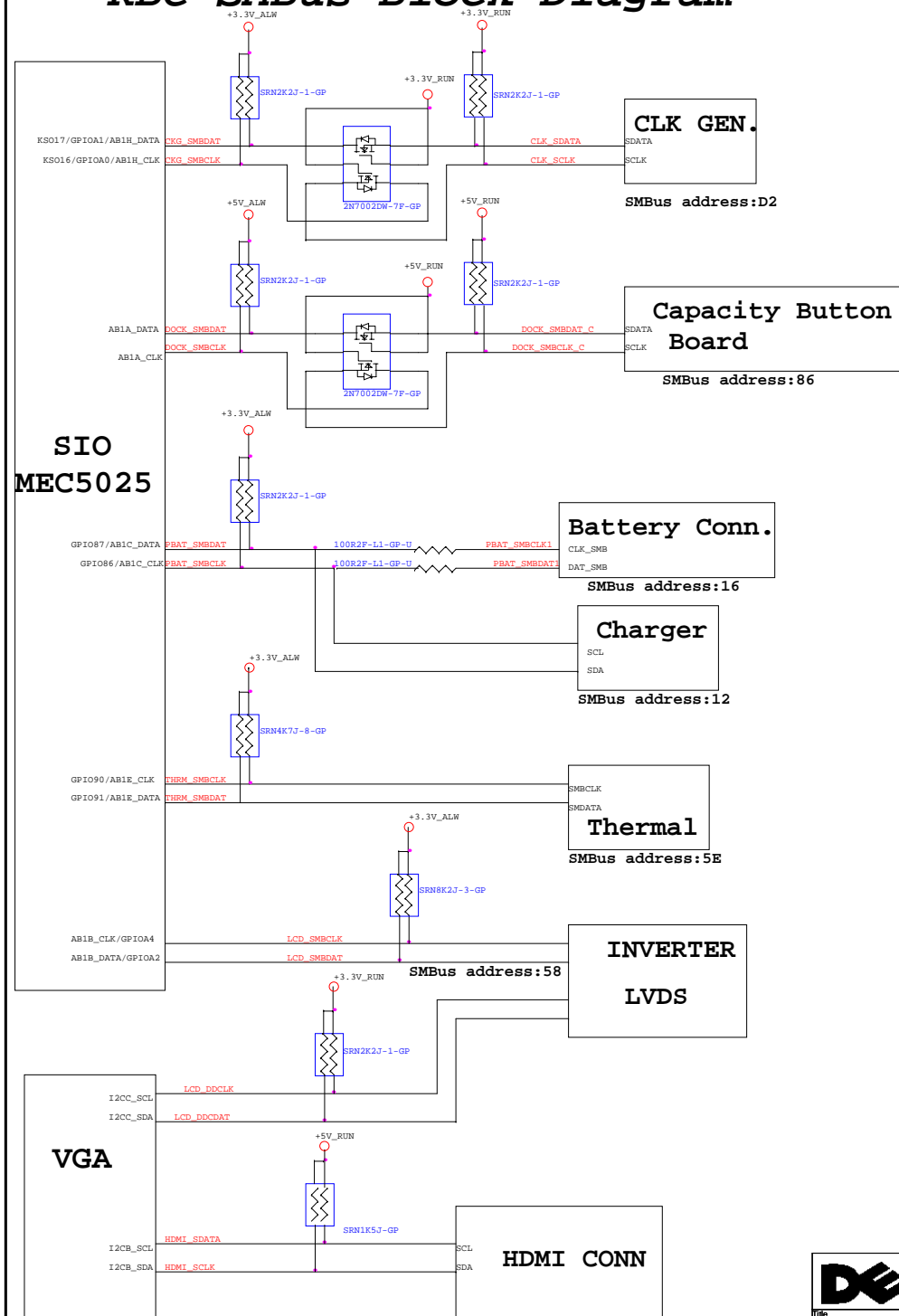
Project code:91.4C301.001
PCB P/N :06247
REVISION :-1



ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



WWW.AliSaler.Com

CLOCK GEN_CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 15
IO_VOUT[2,1,0]

BYTE 10

bits S1	bits S0	Spread Spectrum S(110)
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

bits2	bits1	bits0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

PIN34	0 UMA	1 DISC.
FCTSEL1		
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi1_05 VccSusi1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSusi1_05,VccSusi1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

INTEL CRESTLINE STRAP PIN

* is Default setting

CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16		
FSB Dynamic ODT	Disabled	Enabled *
CFG 18 VCC Select	1.05V *	1.5V
CFG 19 DMI Lane Reserved	Normal Operation*	Reserved Lane
CFG 20 PCIE/SDVO Select	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

	CFG[13:12]
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation*

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	10/100 LOM

ICH USB TABLE

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

PCI ROUTING

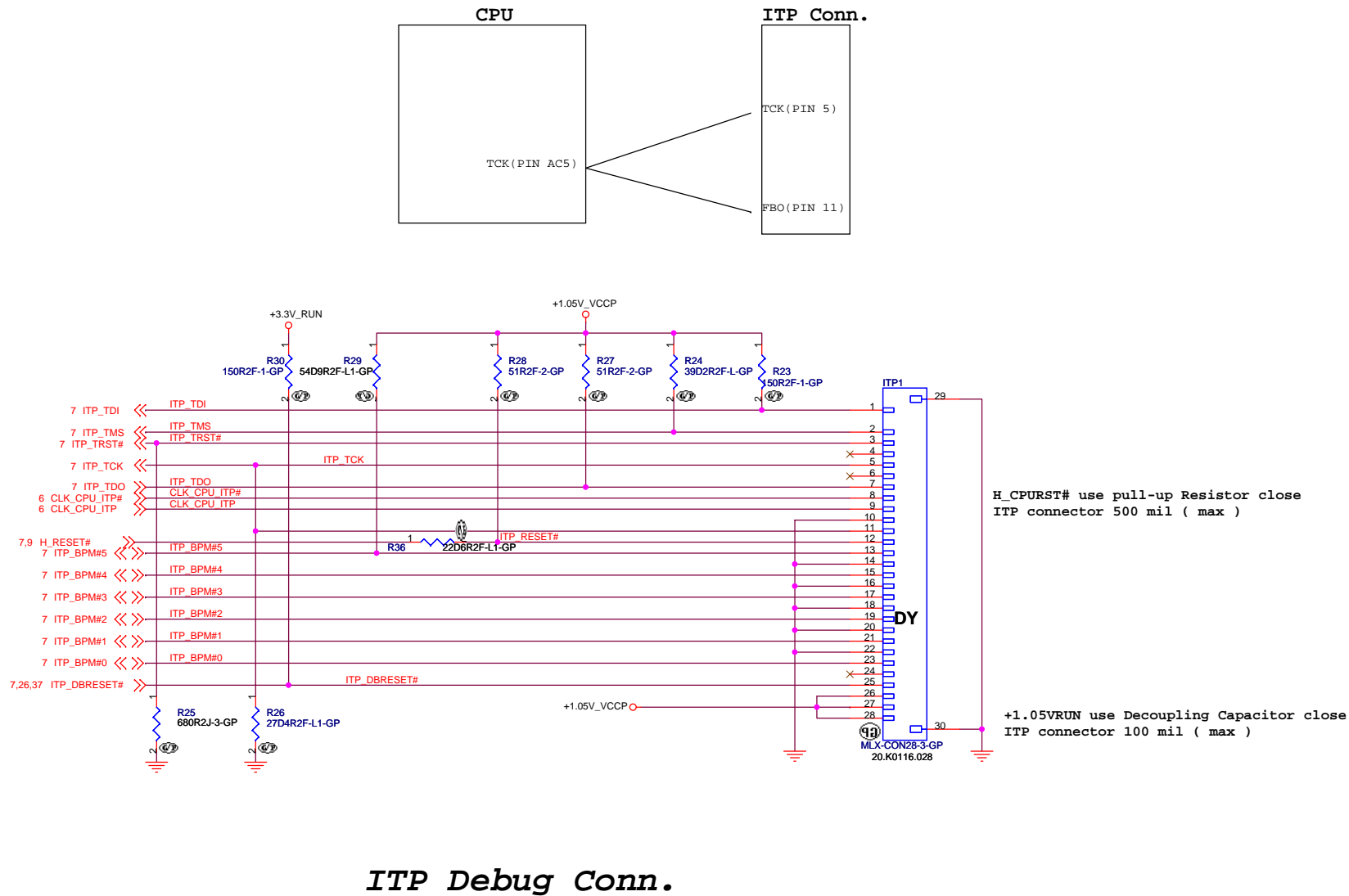
	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

INTEL ICH8-M INTEGRATED
PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

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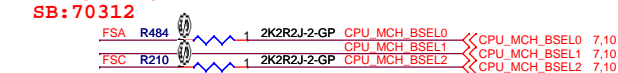
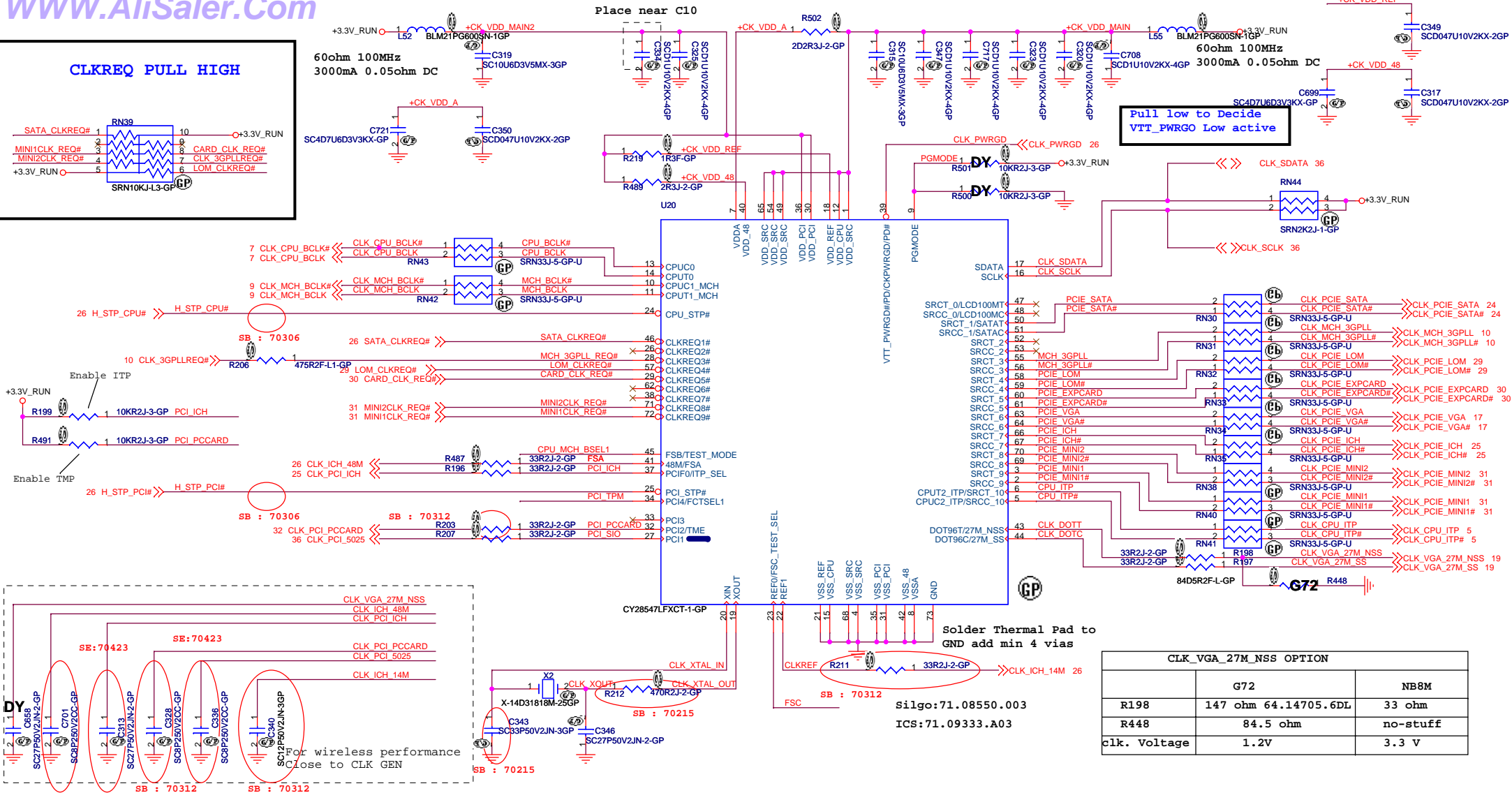
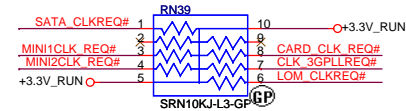
Title		Thurman Discrete	
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A3			Rev -1
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H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max)

+1.05V_RUN use Decoupling Capacitor close
ITP connector 100 mil (max)

CLKREQ PULL HIGH



SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

SB:70412

PIN34	0 UMA	1 DISC.
FCTSEL1		
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

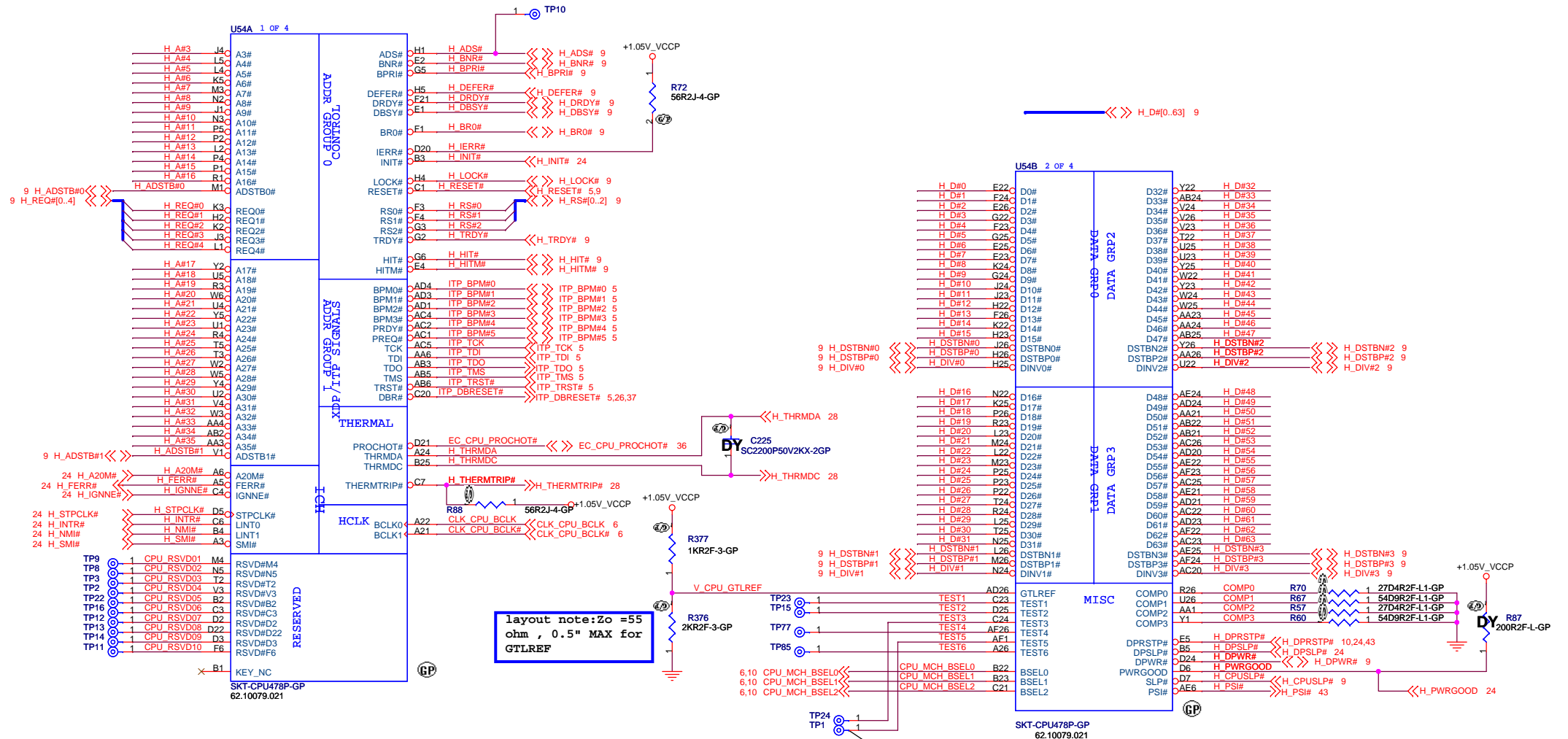
CLK_VGA_27M_NSS OPTION		
	G72	NB8M
R198	147 ohm 64.14705.6DL	33 ohm
R448	84.5 ohm	no-stuff
clk. Voltage	1.2V	3.3 V

PIN9	PIN39
PGMODE	DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD# (DEFAULT)

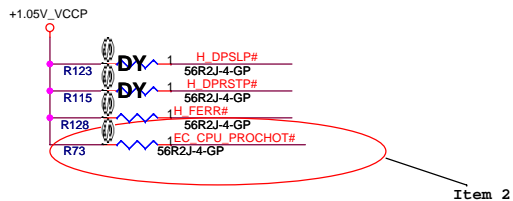
<Variant Name>

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Title Thurman Discrete		
Size A3	Document Number CLK_GEN CY28547	Rev -1
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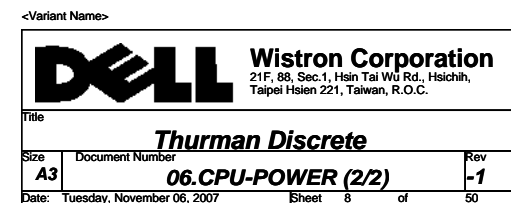
Use old Symbol replace New P/N
original value: SKT-CPU478P-GP



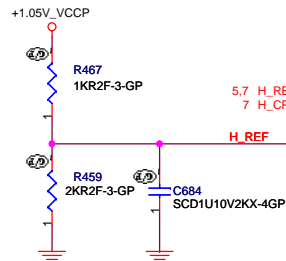
<Variant Name>



Title			Thurman Discrete		
Size	Document Number	CPU-FSB (1/2)			Rev
A3					-1
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H_REF Decoupling Crestline
close Crestline 100 mil



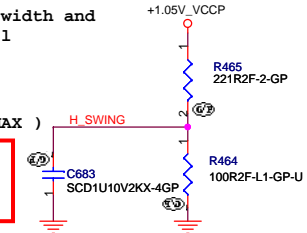
Change to 71.CREEST.M03

CRESTLINE-GP-U-NF

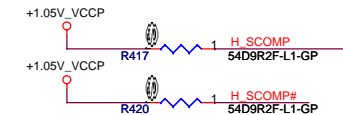
H_SWING routing Trace width and
Spacing use 10 / 20 mil

H_SWING Resistors and
Capacitors close
Caliistoga 500 mil (MAX)

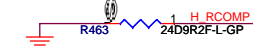
From Schematic Design
Checklit v.1201
221 1% pull high 100
1% pull low



H_SCOMP and H_SCOMP# Resistors
and Capacitors close Caliistoga
500 mil (MAX)
Zo=55ohms



H_RCOMP routing Trace width and
Spacing use 10 / 20 mil



<Variant Name>



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Title

Thurman Discrete

Size

Document Number

A3

GMCH-FSB LIBC (1/6)

Rev

-1

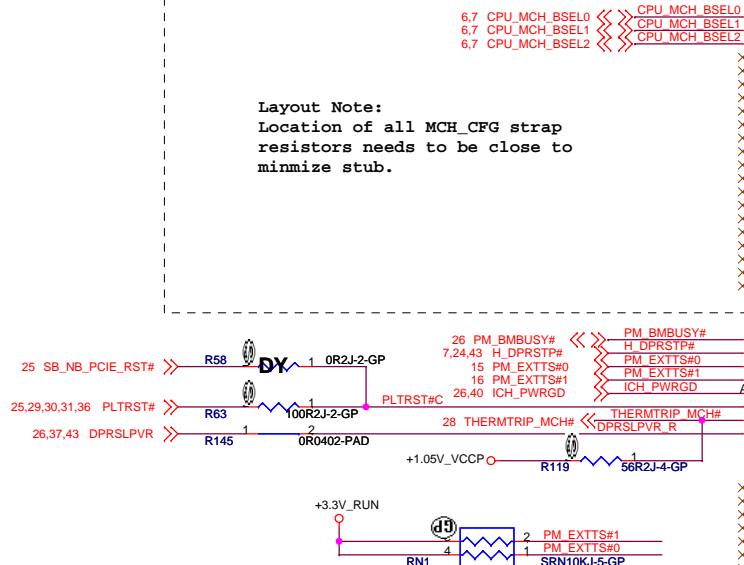
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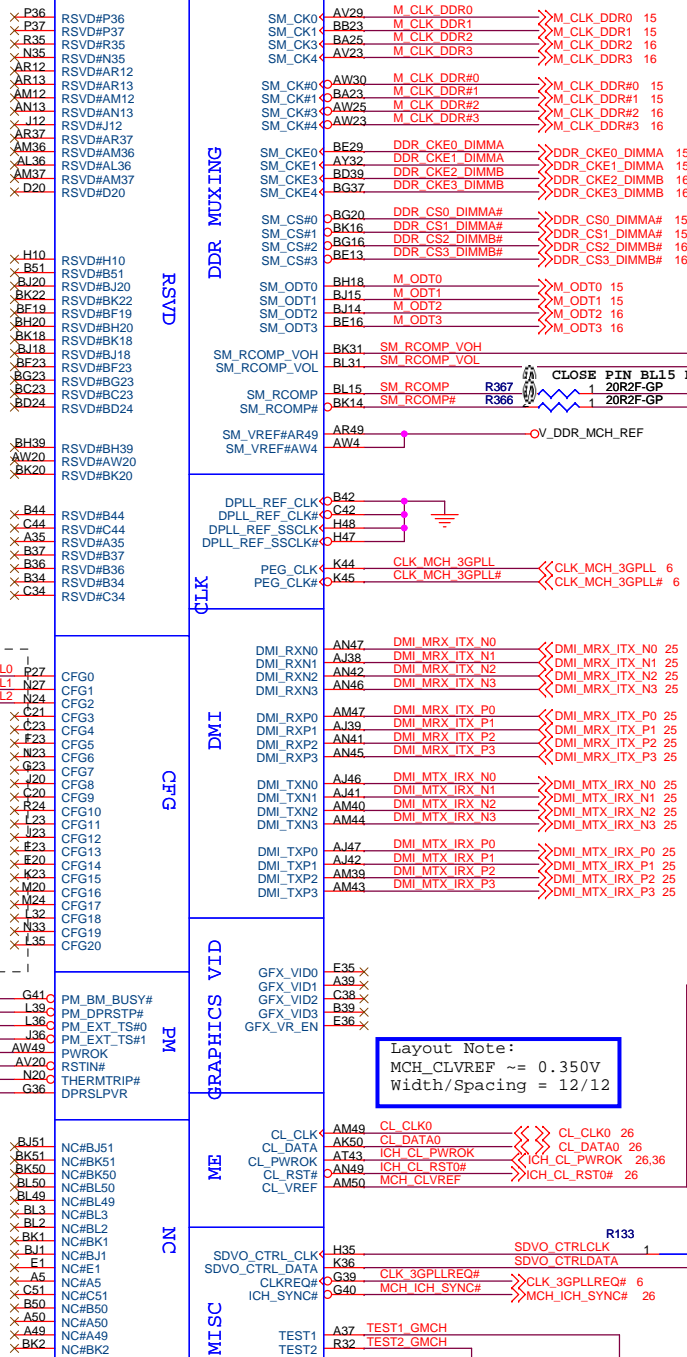
CFG Strap	Low	High
CFG 5	DMI X 2	DMI X 4 *
CFG 6	Moby Dick	Calistoga *
CFG 7	DT/Transportable CPU	Mobile CPU *
CFG 9	Reserved Lane	Normal Operation *
CFG 10	Reserved	Mobility *
CFG 11	Calistoga *	Reserved
CFG 16	Disabled	Enabled *
CFG 18		
VCC Select	1.05V *	1.5V
CFG 19		
DMI Lane Reserved	Normal Operation *	Reserved Lane
CFG 20	Only PCIE or SDVO is operation *	PCIE and SDVO are operation simu
PCIE/SDVO Select		
SDVO_CTRLDATA	No SDVO Device present *	SDVO Device present

CFG[13:12]	
LL	Reserved
LH	XOR Mode Enabled
HL	All Z Mode Enabled
HH	Normal Operation *
CFG[2..0] FSB Select	
LHL	FSB 800
LHH	FSB 667
Other	Reserved

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minimize stub.



U56B 2 OF 10

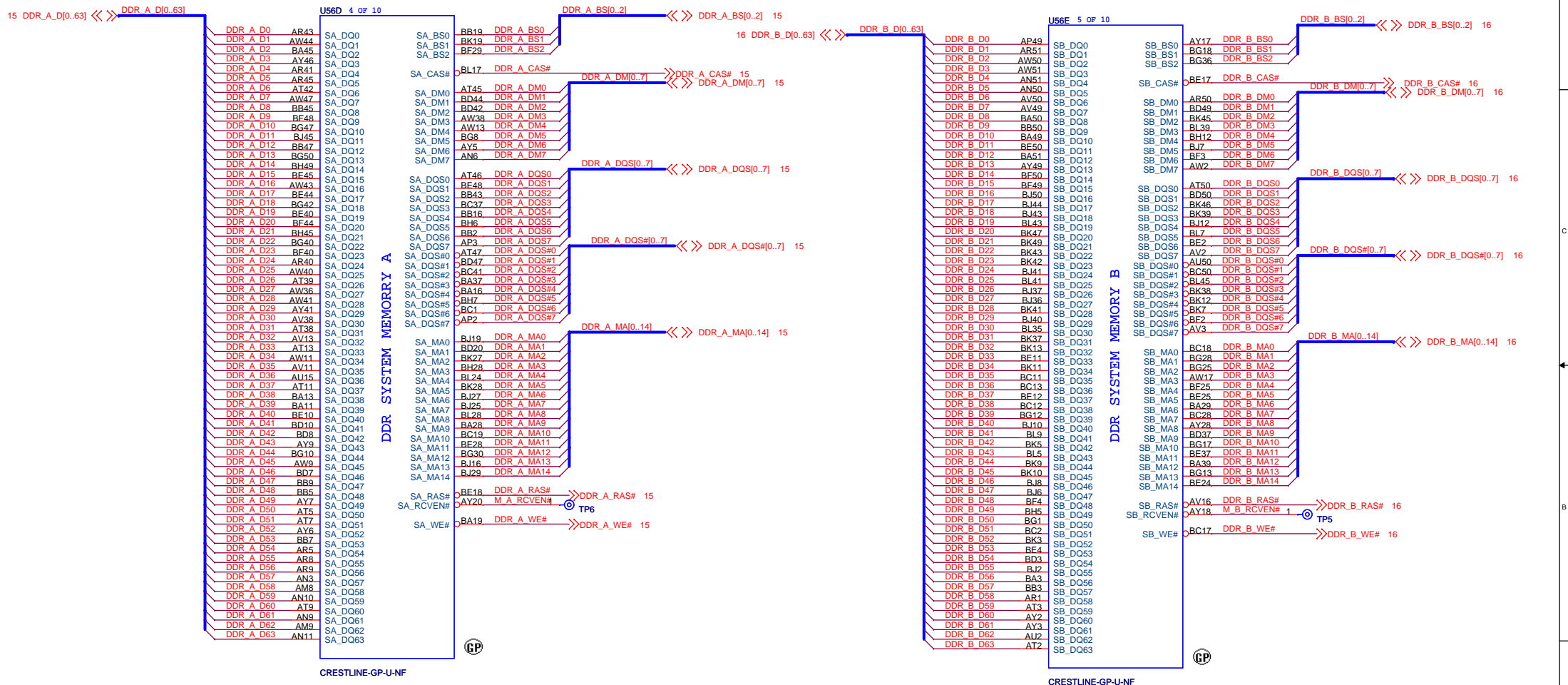


Layout Note:
MCH_CLVREF ~ 0.350V
Width/Spacing = 12/12

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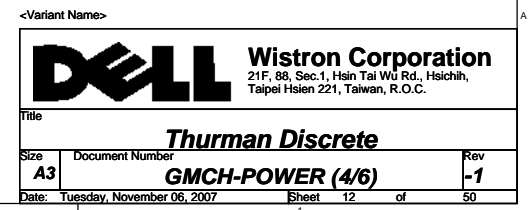
Thurman Discrete
GMCH-DM/DDR (2/6)

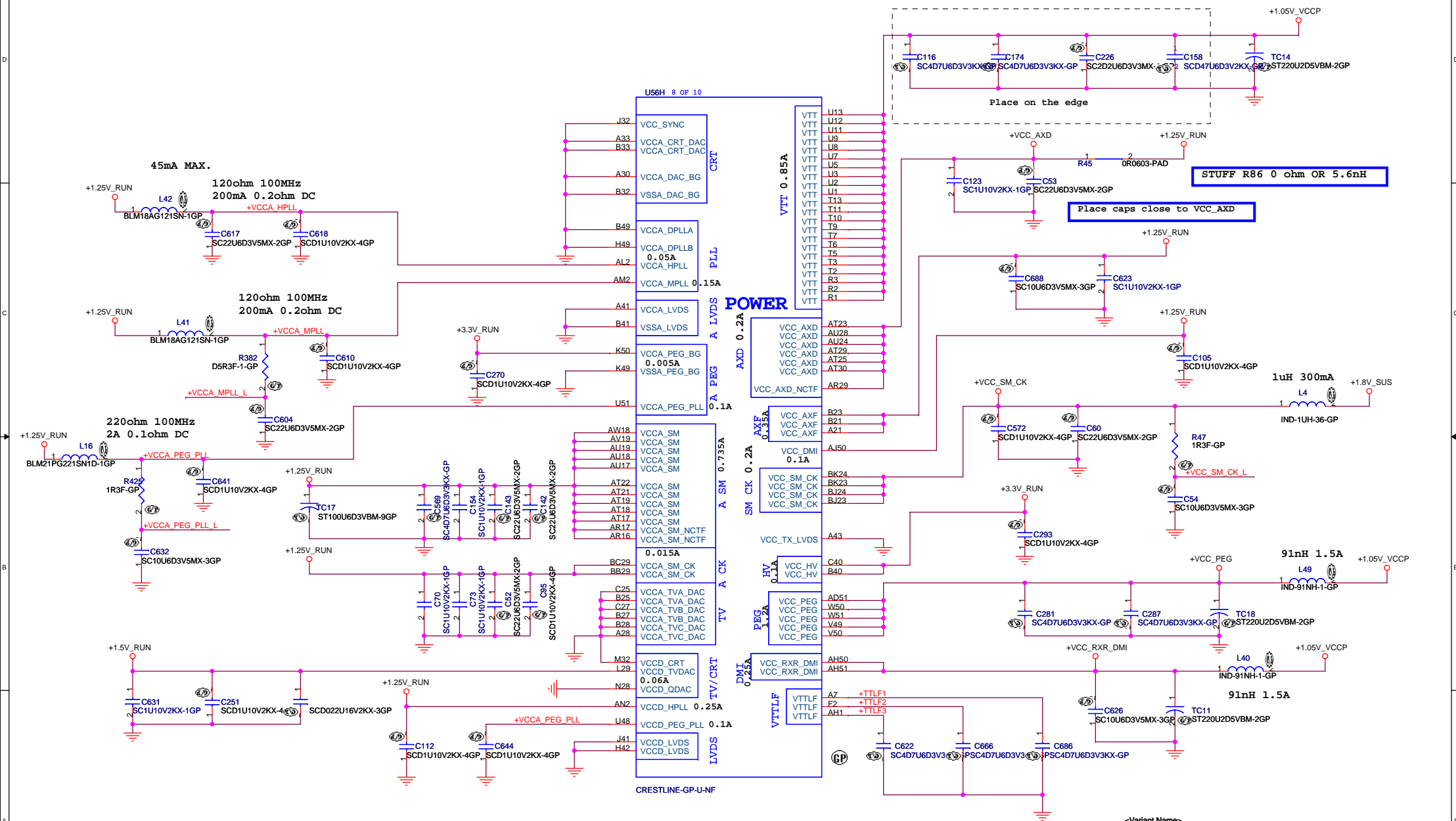
Size A3 Document Number Rev -1
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<Variant Name>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Thurman Discrete GMCH-DDR (3/6)	
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<Variant Name>



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Title

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Size
A3

Document Number

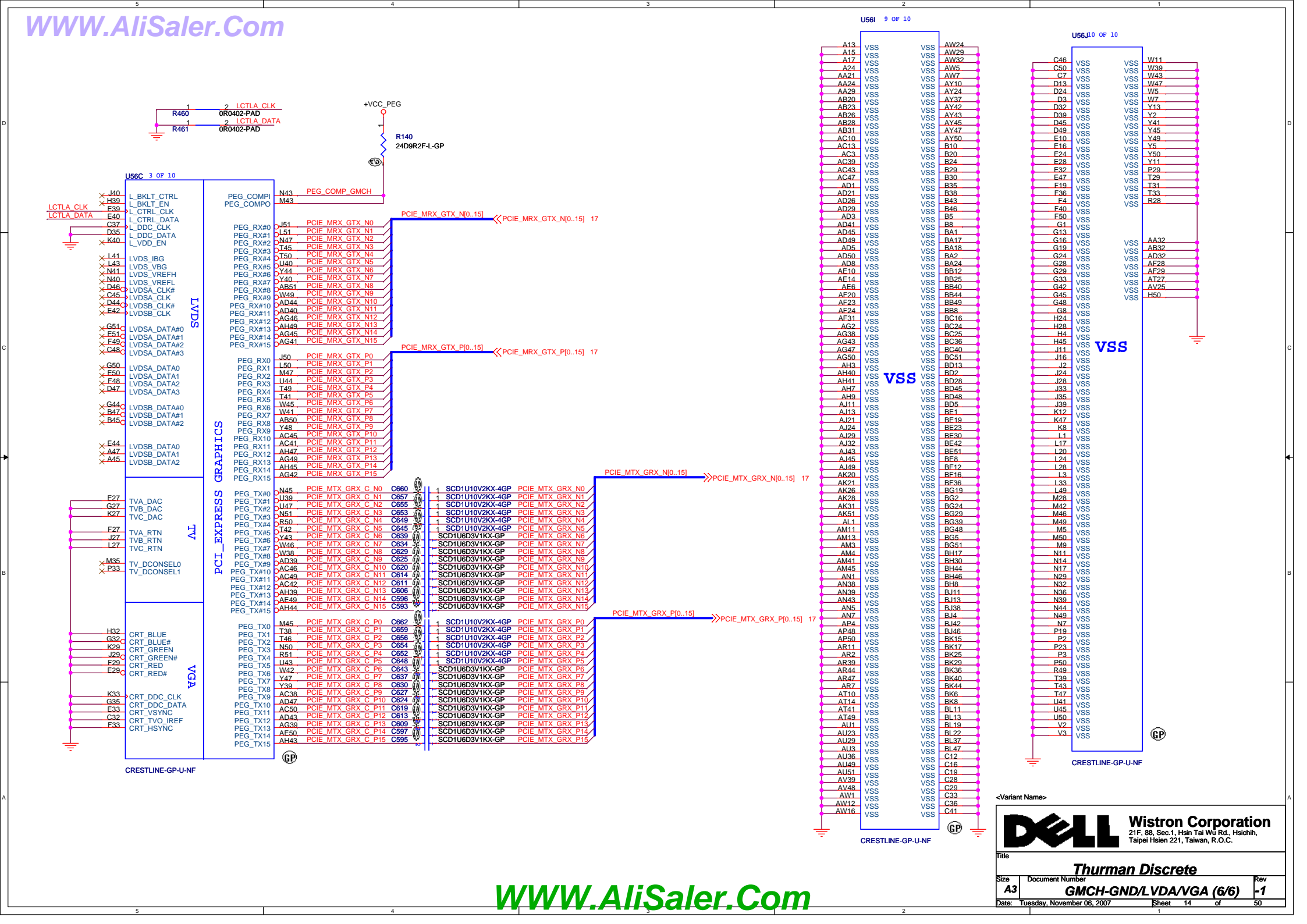
A3

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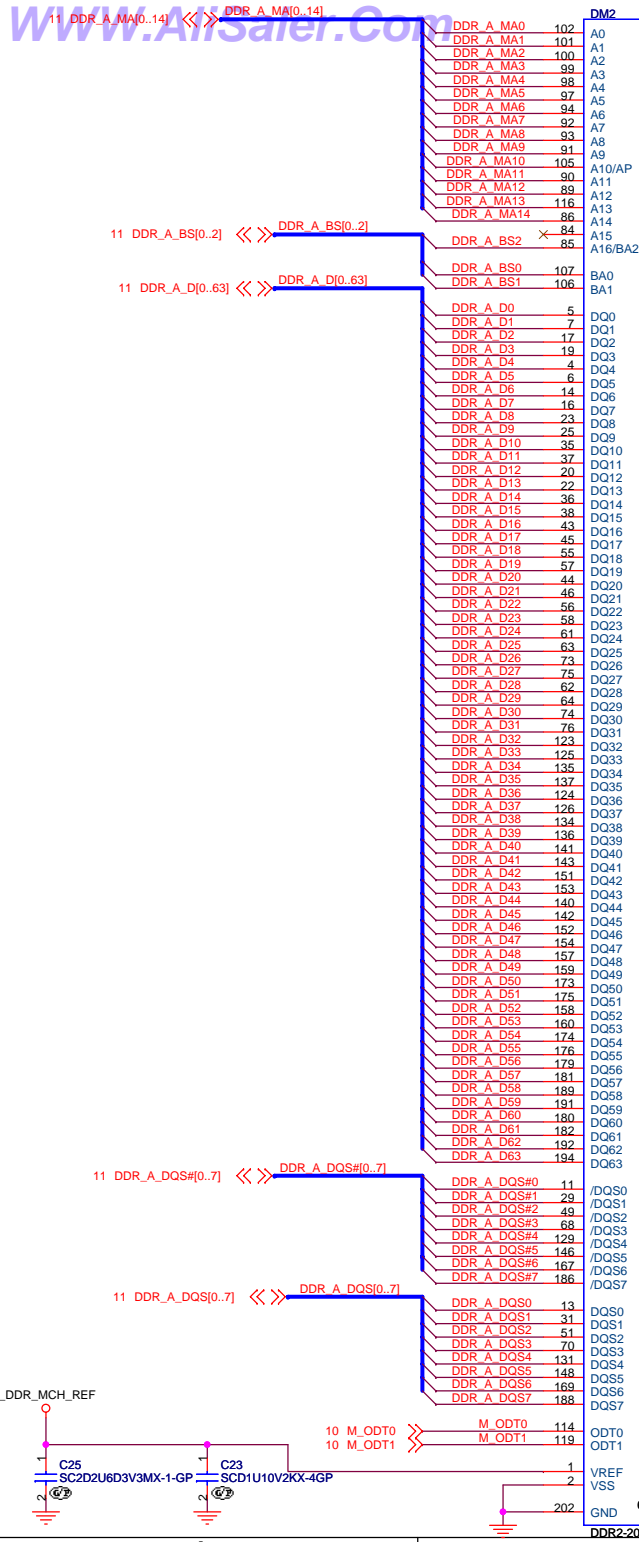


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 Taipei Hsien 221, Taiwan, R.O.C.

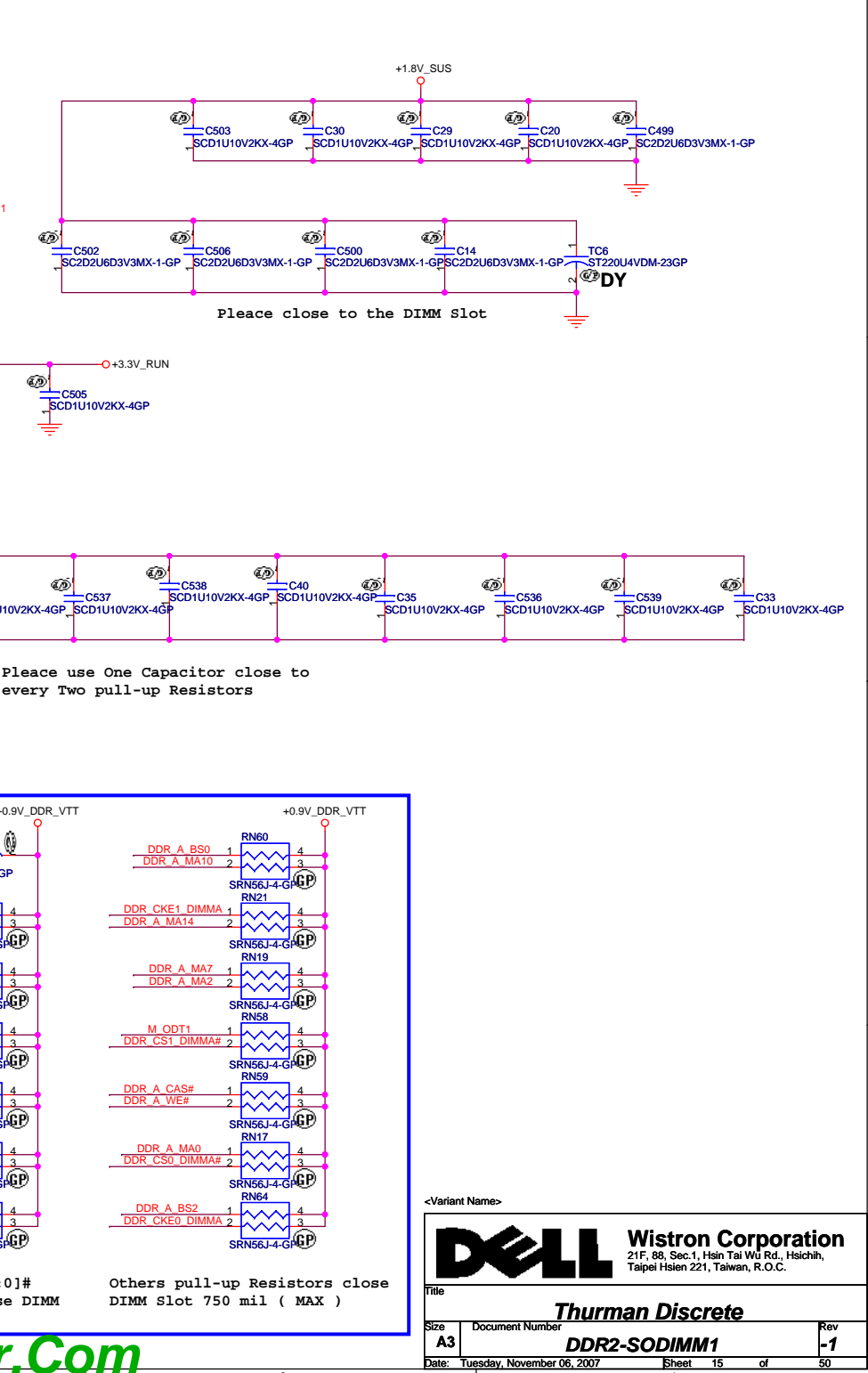
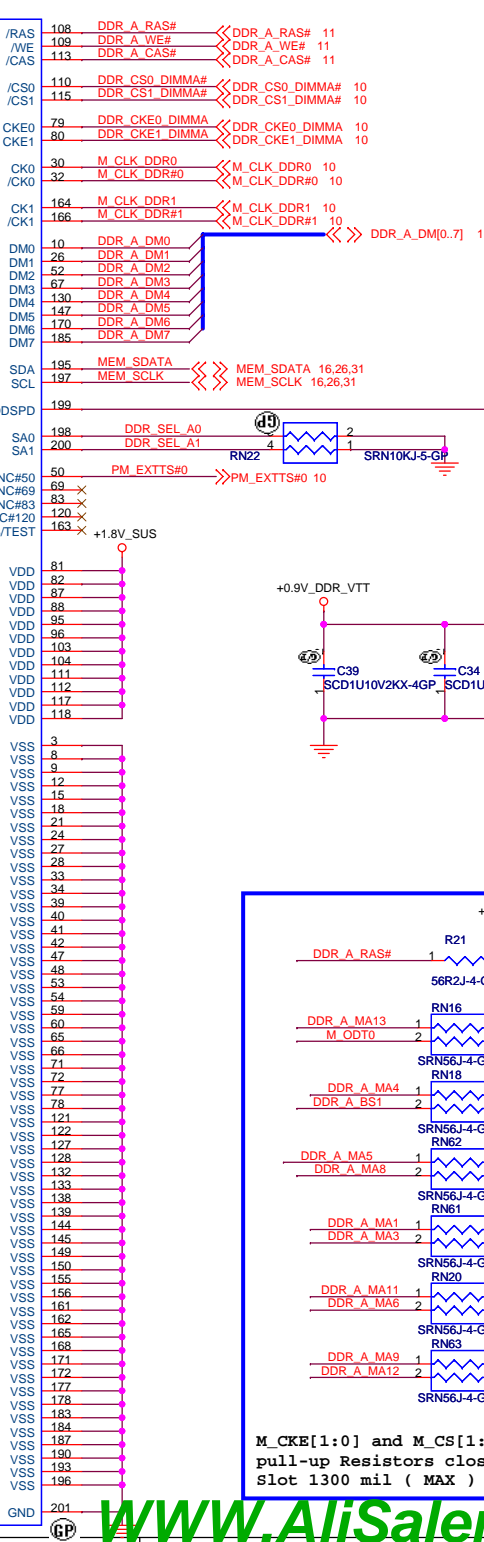
Thurman Discrete

Size A3 Document Number GMCH-GND/LVDA/VGA (6/6) Rev -1

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REVERSE TYPE
High 5.2 mm



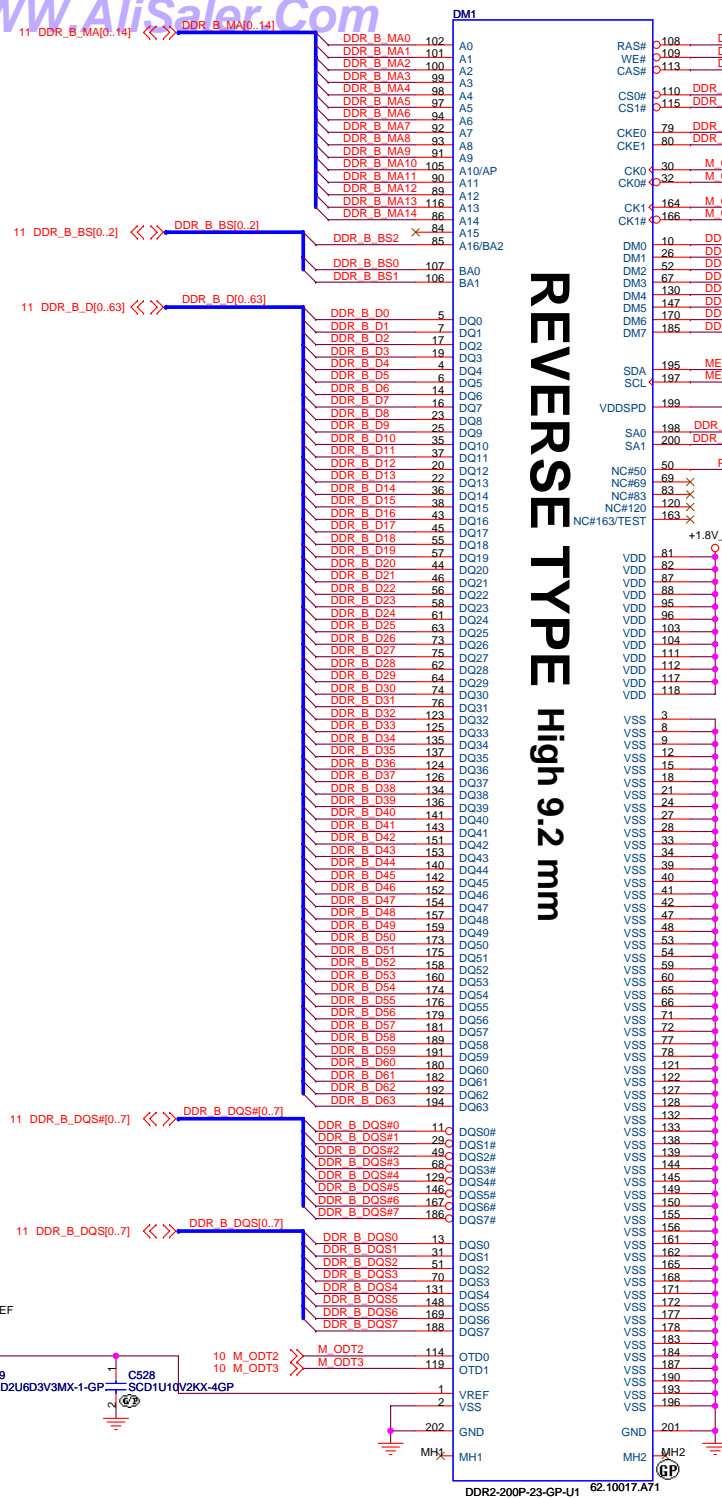
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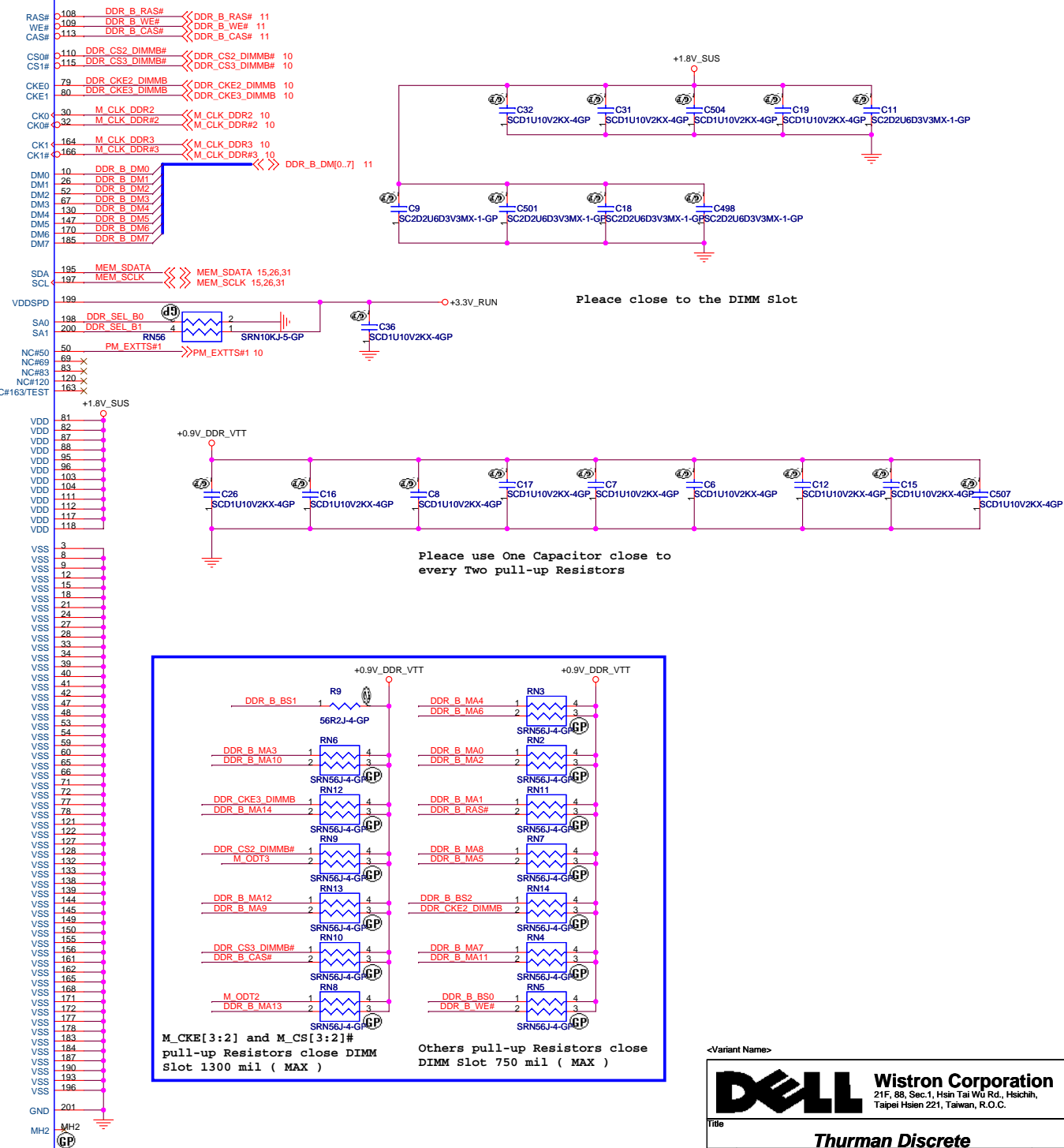
DDR2-SODIMM1

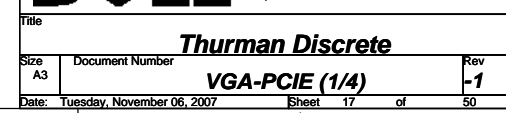
Rev -1

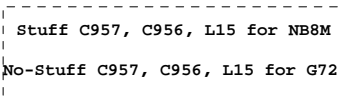
Date: Tuesday, November 06, 2007 Sheet 15 of 50

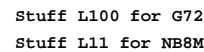


REVERSE TYPE High 9.2 mm

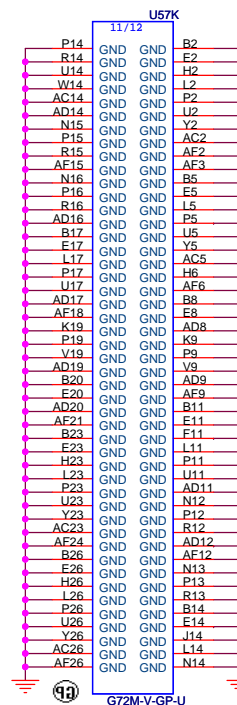
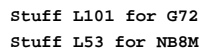
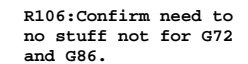
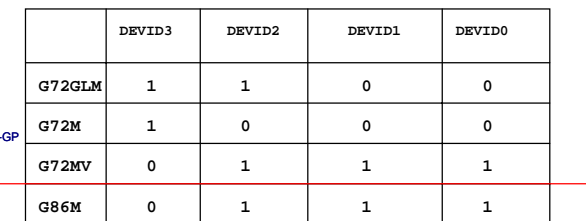








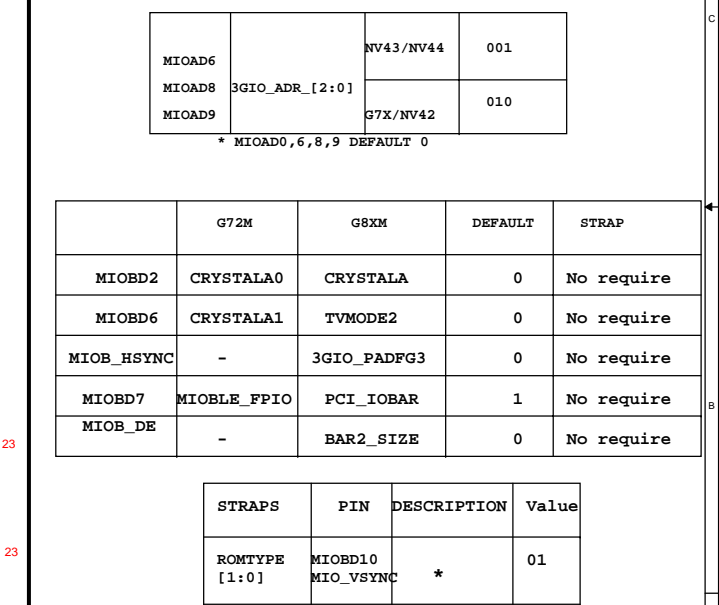
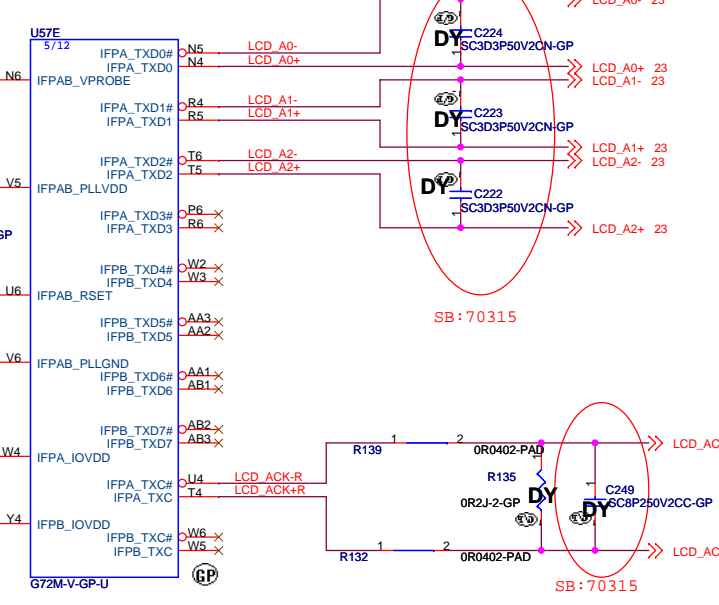
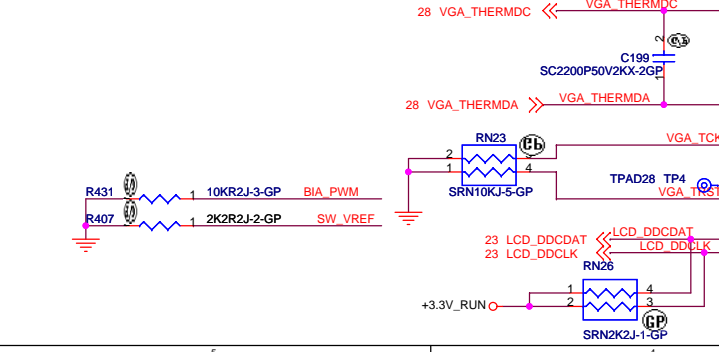
The schematic diagram illustrates the connection between the U57G, U55, and AT88SC0808C-SU-1-GP components. The U57G is connected to the U55 via a 72M-V-GP-U1 capacitor. The U55 is connected to the AT88SC0808C-SU-1-GP. The circuit includes a +3.3V_RUN supply, resistors R380 (10KR2J-3-GP), R386 (10KR2J-3-GP), and R111 (10KR2J-3-GP), and capacitors C63 and C64. The U57G is connected to the U55 via a 72M-V-GP-U1 capacitor.



G7XM	G8XM	G3-64 ball
GND	12SC_SDA	F11




Title			
<i>Thurman Discrete</i>			
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A3	VGA-HDMI	-1	
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PEX_PLL_TERM MIOAD0		0

* Parallel=00, SERIAL AT25F=01
 DEFAULT,Serial SST45VF=10,
 JPC=11
 <Variant Name>



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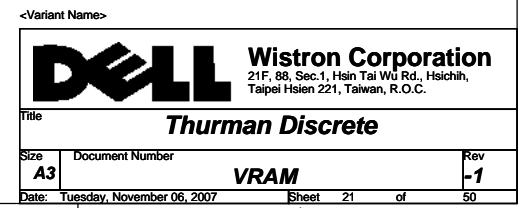
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

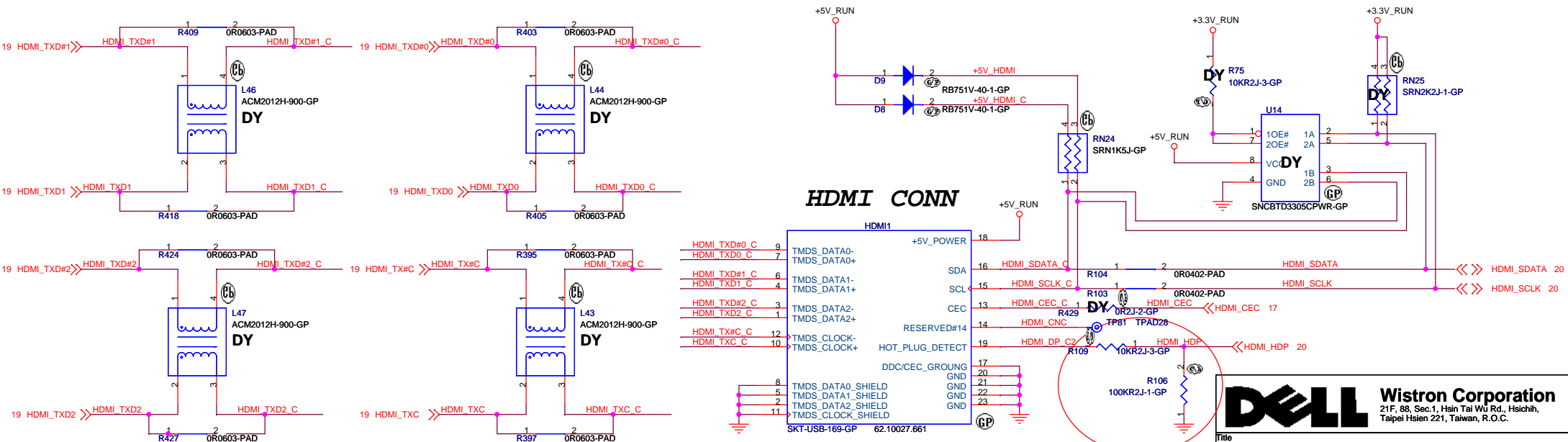
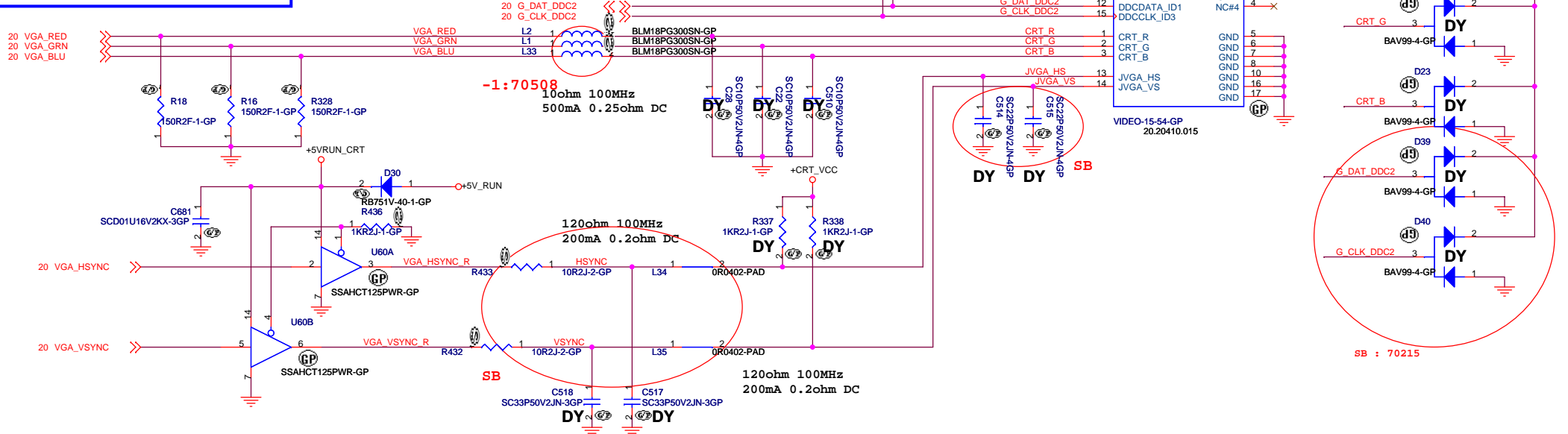
Thurman Discrete

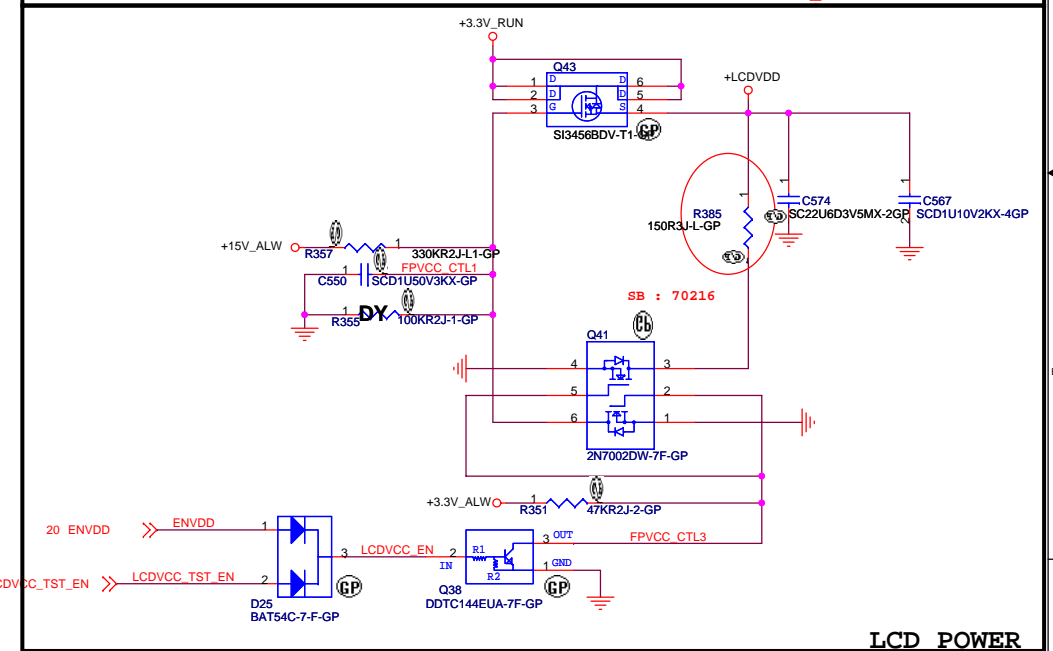
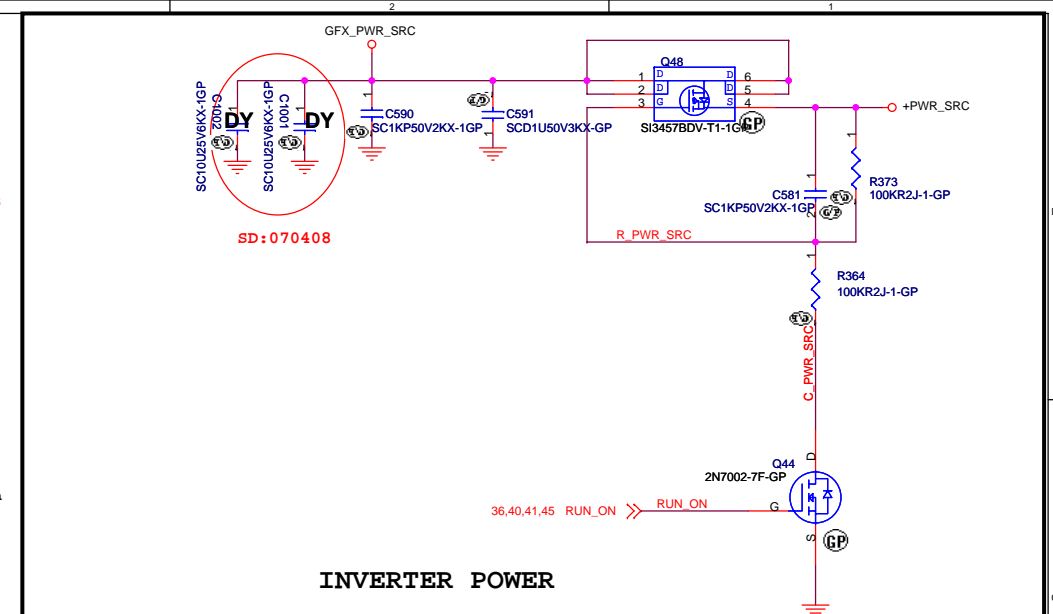
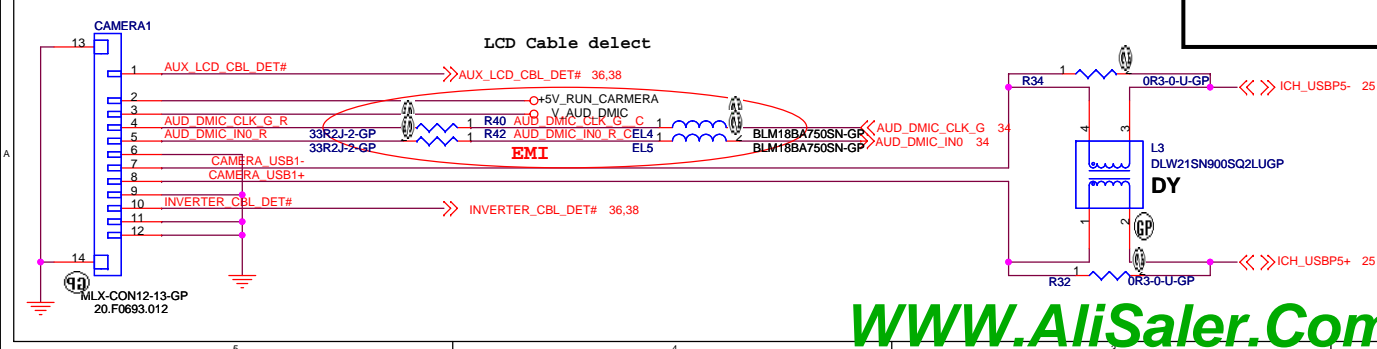
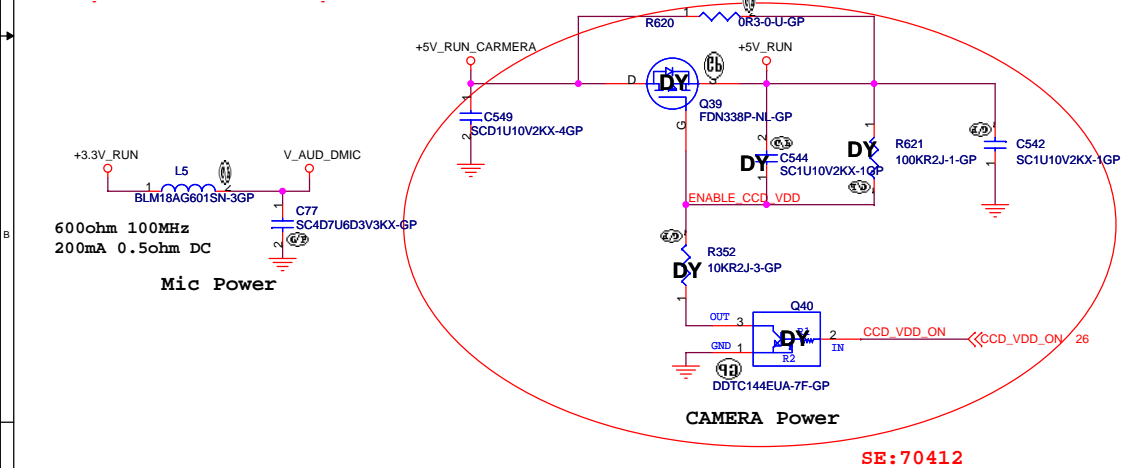
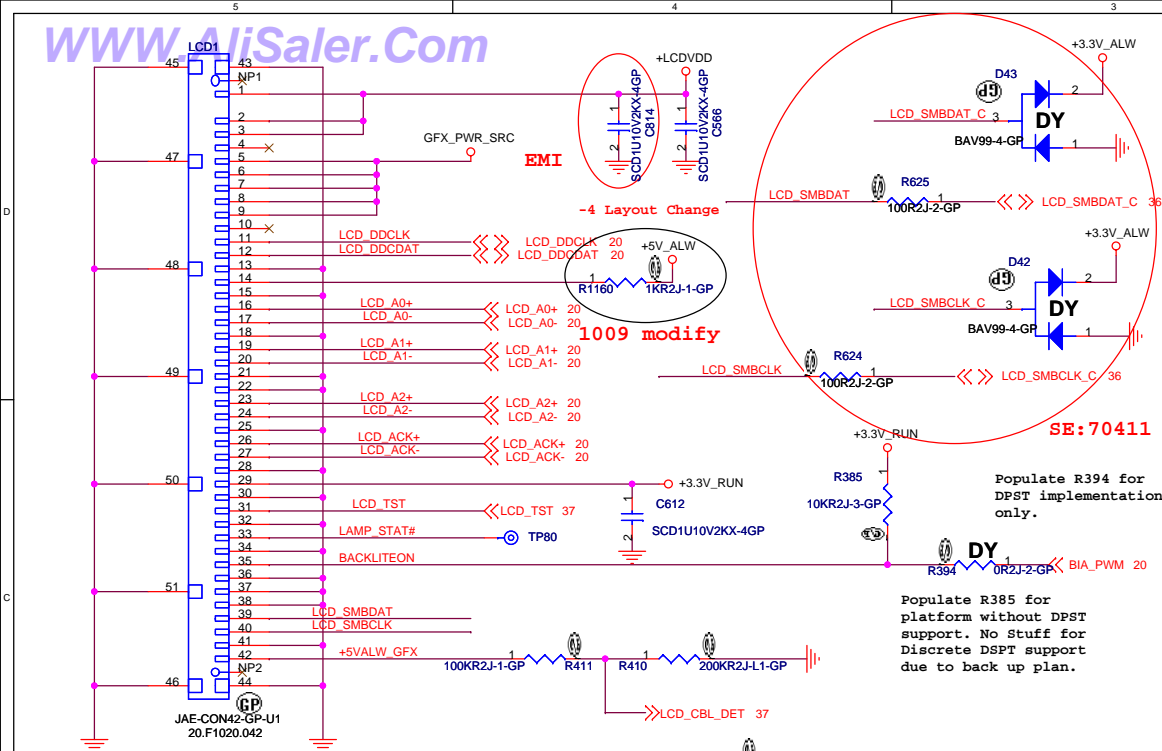
Size	Document Number	Rev
A3	VGA-LVDS/TV/CRT/STRAP (3/3)-1	

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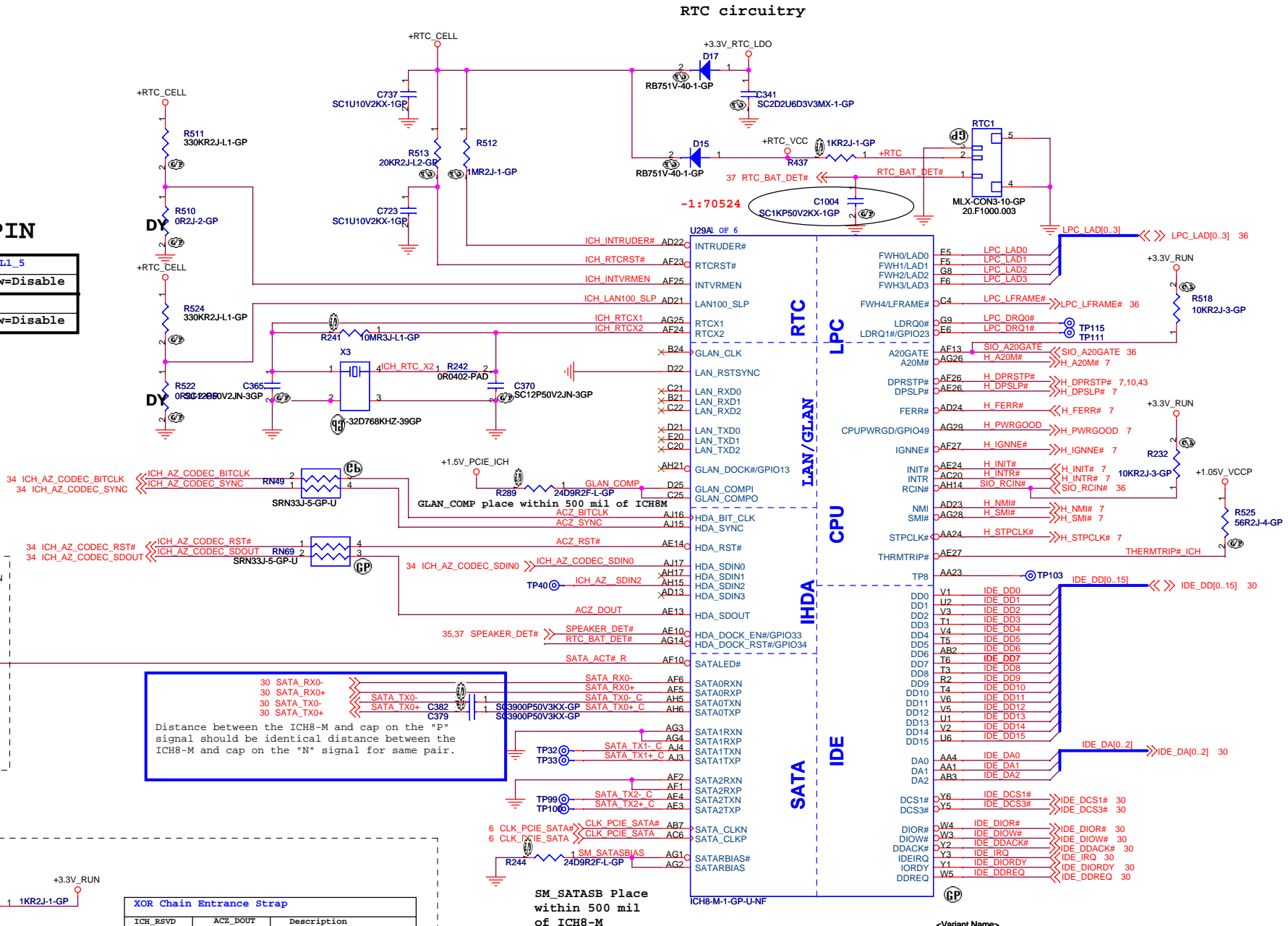


Setting R,G,B trace impedance to 50 ohm.

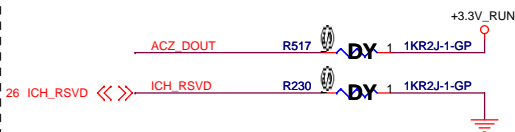




integrated VccSus1_05,VccSus1_5,VccCL1_5		
ICH_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
ICH_LAN100_SLP	High=Enable	Low=Disable



ICH8-Strap PIN



XOR Chain Entrance Strap		
ICH_RSVD	ACZ_DOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIe port cofig bit1

SM_SATASB Place
within 500 mil
of ICH8-M

Change to 71.0 ICH8.M08

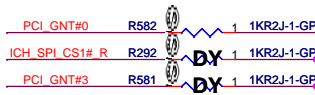
<Variant Name>



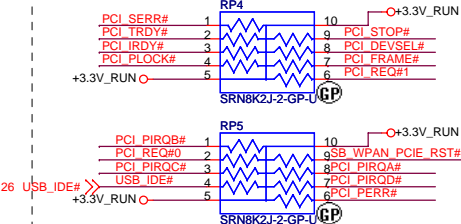
Title			
Thurman Discrete			
Size	Document Number		Rev
A3	ICH8M-RTC/IDE/LPC/DHI (1/4)		-1
Date:	Thursday, November 22, 2007	Sheet 24 of	50

BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

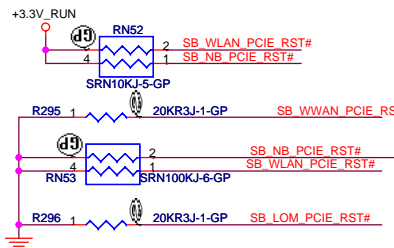
Al6 swap override strap	
PCI_GNT#3 (R168)	
low	= Al6 swap override enable
high	= default



PCI I/F PULL HIGH

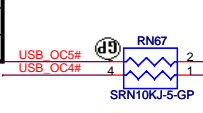


BIOS should not enable the internal GPIO pull up

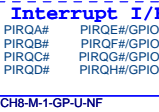
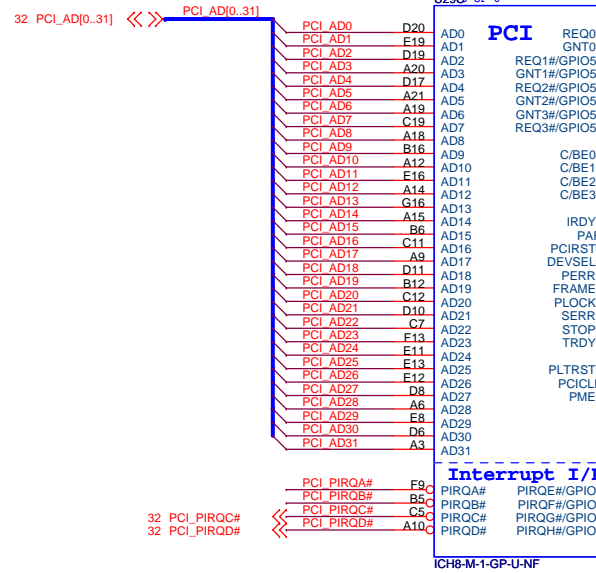
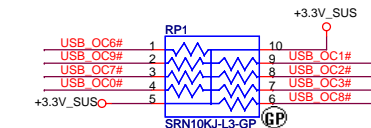


PCIE Interface Routing

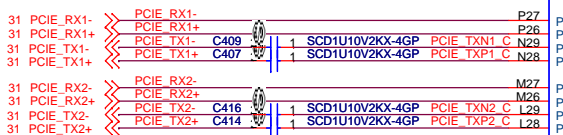
LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	No use
LANE4	Express Card
LANE5	No use
LANE6	LAN



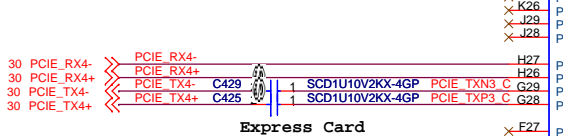
Layout Note:
Place R235, R237 and R234 within 500 mils from ICH.



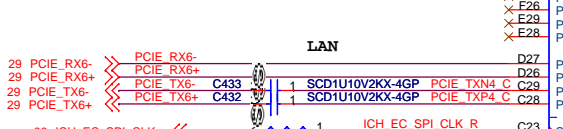
MiniCard WWAN



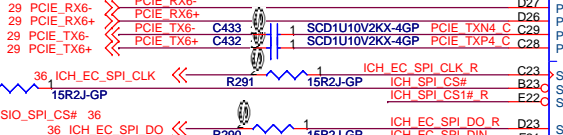
MiniCard WLAN



Express Card



LAN



U29B 2 OF 6



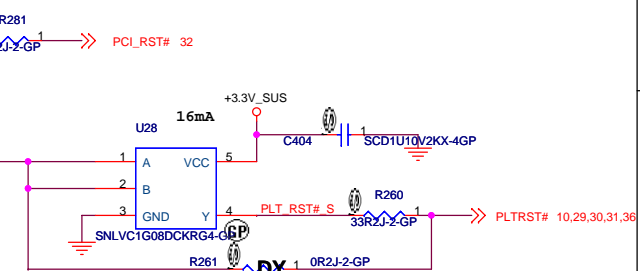
USB

ICH8-M-1-GP-U-NF

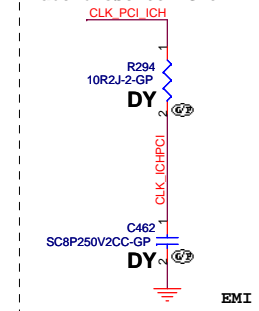
	IDSEL	INT	REQ	GNT
1394/MediaCard	AD17	C D	1	1

PCI Interface Routing

Add Buffers as need for Loading and Fanout concerns



CLK_ICH_14M EMI Mode



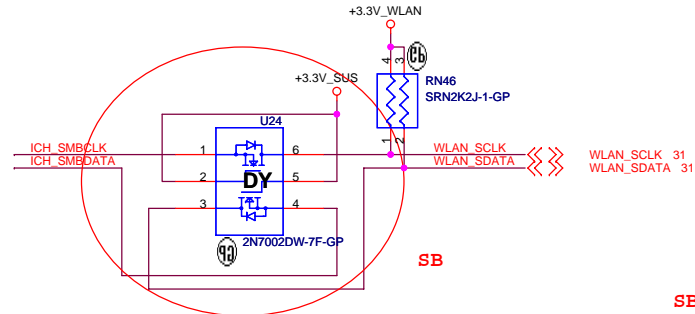
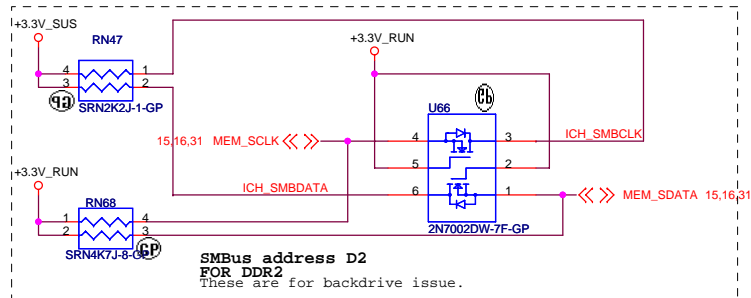
DMI_COMP R158 place within 500 mil of ICH8M

USB0	USB1
USB1	USB2
USB2	
USB3	
USB4	Biometric
USB5	Camera
USB6	Express Card
USB7	BT
USB8	
USB9	MINI Card WWAN

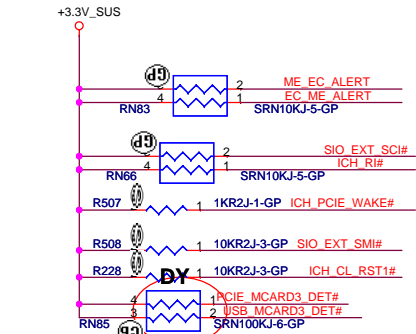
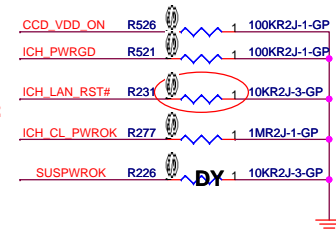
<Variant Name>



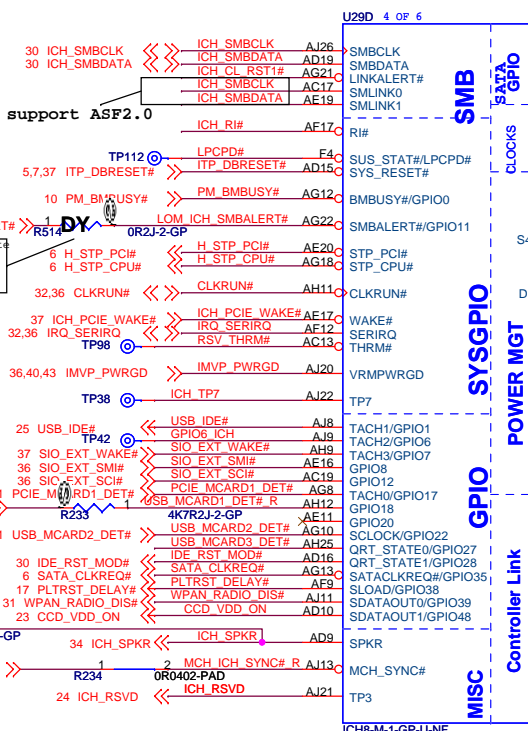
Thurman Discrete		
Size	Document Number	Rev
A3	ICH8M-PCIE/USB/SPI/DMI (2/4)	-1
Date:	Thursday, November 22, 2007	Sheet 25 of 50



SB:70302

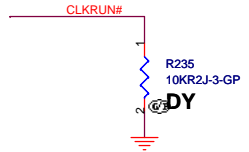


Note: Do not Populate this 0 ohm resistor for now.



ICH8-Strap PIN

No Reboot Strap	
ICH_SPKR	LOW = Defaule
	High=No Reboot



<Variant Name>

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Title: **Thurman Discrete**

Size: A3 Document Number: **ICH8M-CL/PM/GPIO (3/4)** Rev: -1

Date: Tuesday, November 06, 2007 Sheet 26 of 50



SSID = THERMAL

REM_DIODE1_N and REM_DIODE1_P
routing Trace width and Spacing
use 10 / 10 mil

Place inside CPU socket

C455 Please close to Guardian

Close to Pin5, Pin6

Close to Pin9

H_THERMDA and H_THERMDC
routing Trace width and
Spacing use 10 / 10 mil

C456 Please close to Guardian

REM_DIODE4_N and REM_DIODE4_P
routing Trace width and Spacing
use 10 / 10 mil

Thermal sensor for Mini Card
should be placed TOP Side under WWAN CARD

C459 Please Close to Guardian

Thermal sensor for VGA

C453 Please Close to Guardian

Note :

$VSET = (T_p - 70) / 21$
 $3.3 * (R411 / R406 + R411) = (T_p - 70) / 21$
Where $T_p = 70$ to 101 degrees C
 T_p set at 88 degrees C
Guardian temp tolerance = +/- 3 degrees C

Version B: 74.04001.A73

VGA THERMALTRIP

CPU THERMALTRIP

MCH THERMALTRIP

C916, C459, C472 Please Close to Guardian

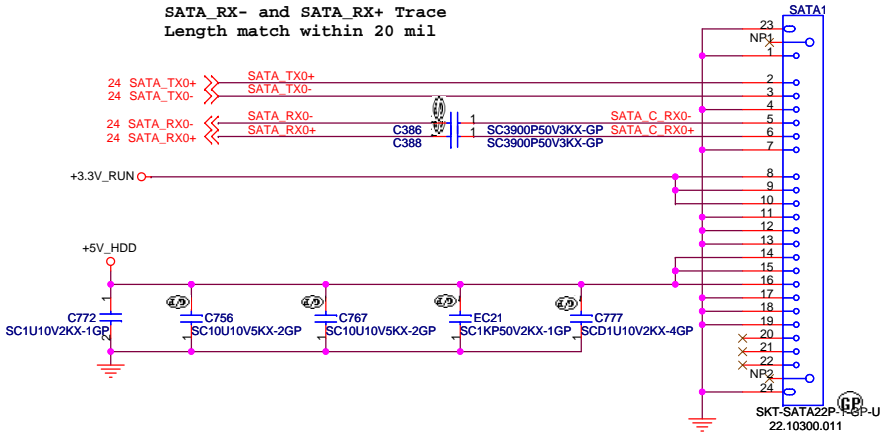
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

File
Thurman Discrete
Size A3 Document Number
FAN/EMC4001
Date: Tuesday, November 06, 2007 Sheet 28 of 50
Rev -1

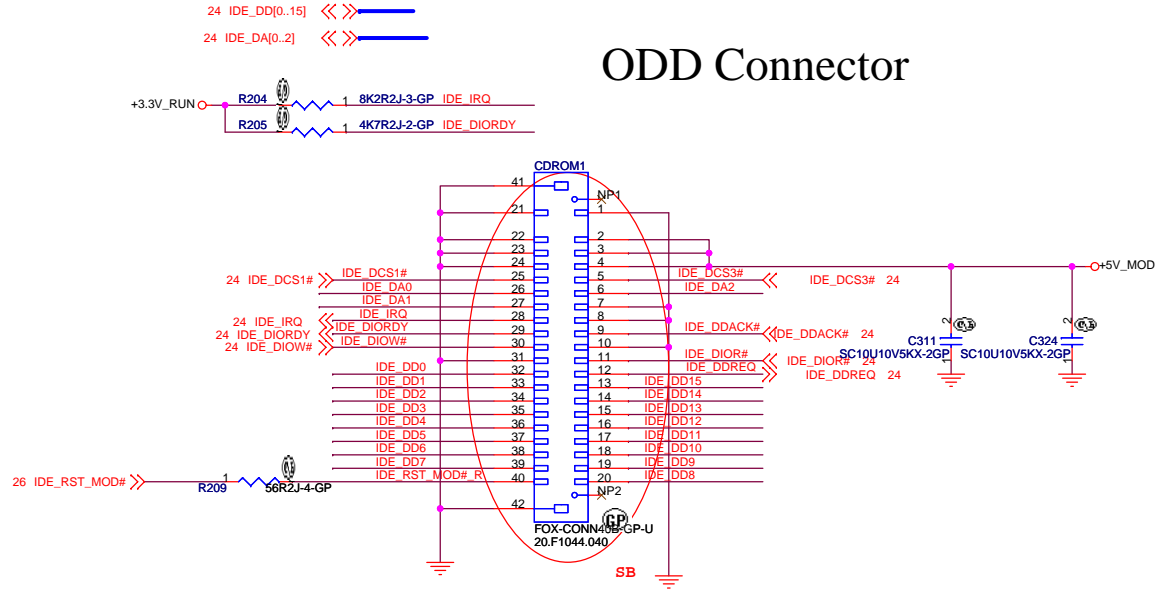


SATA HDD Connector

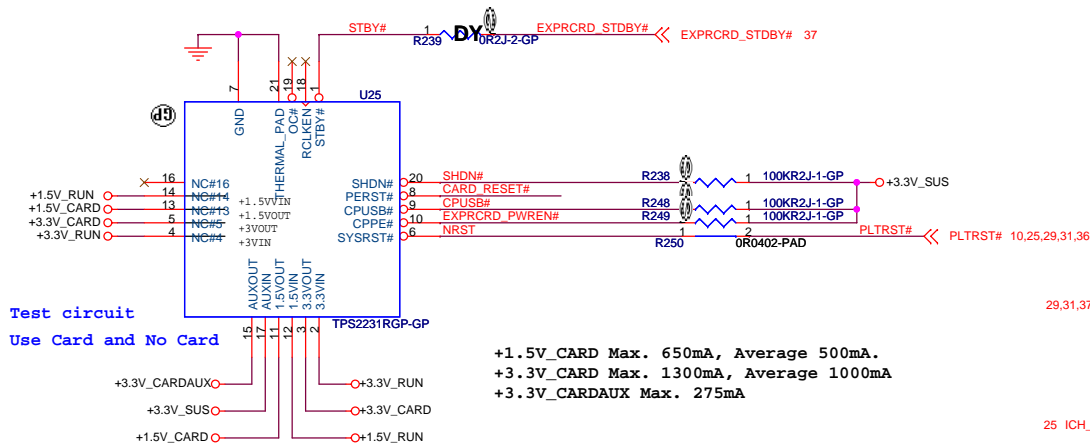
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil



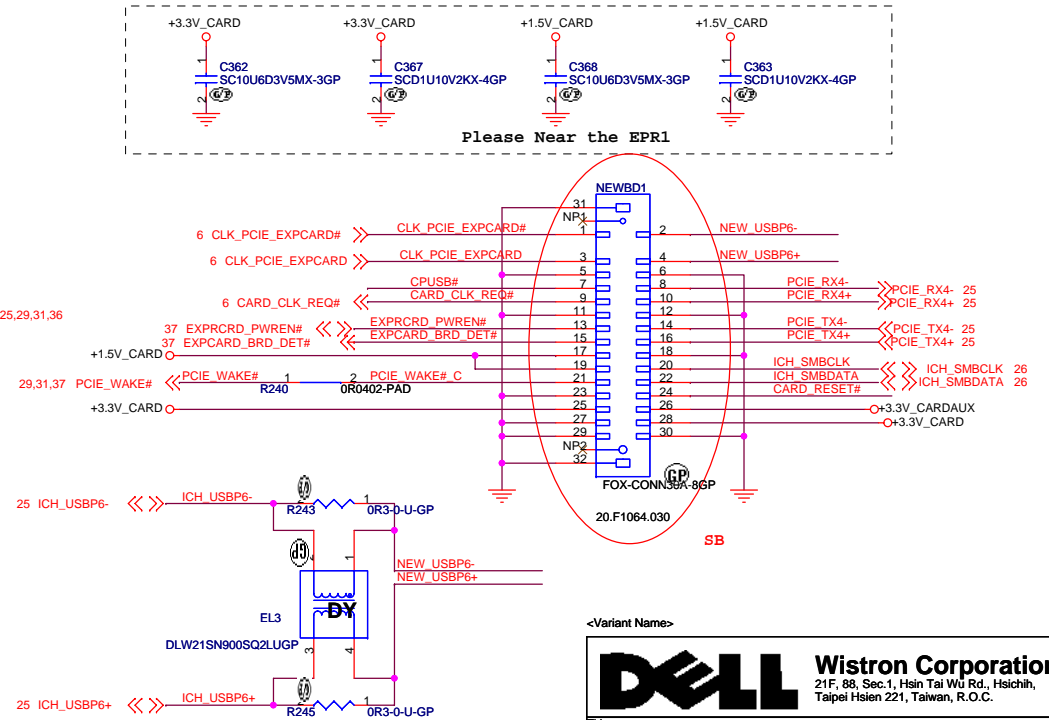
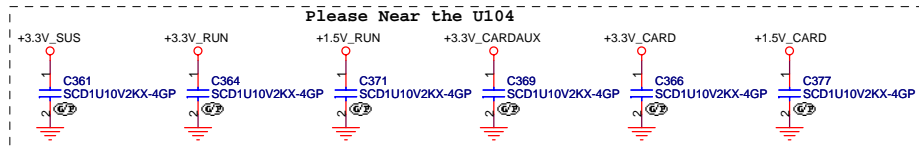
ODD Connector



Express Card



+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



<Variant Name>

DELL **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Thurman Discrete

Size

Document Number

HDD/ODD/TO EXPRESS BD CONN-1

Date _____

Tuesday, November 06, 2007

Sheet 30 of 50

Date: Tuesday, November 06, 2001	

1

DEBUG PINS



SSID = 1394

600ohm 100MHz
200mA 0.5ohm DC

+3.3V_RUN +3.3VRUN_PHY

BLM18AG601SN-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

SC10U16V2KX-3GP

U31A 1 OF 2

AVCC_PHY3V

AVCC_PHY3V

AVCC_PHY3V

AVCC_PHY3V

TPBIAS0

TPBIAS0

TPB0N

TPB0N

TPB0P

TPB0P

TPA0N

TPA0N

TPA0P

TPA0P

FIL0

REXT

VREF

MDIO17

MDIO16

MDIO15

MDIO14

MDIO13

MDIO12

MDIO11

MDIO10

MDIO05

MDIO08

MDIO19

MDIO18

MDIO02

MDIO03

MDIO00

MDIO01

MDIO09

MDIO04

MDIO06

MDIO07

RSV

RSV

RSV

RSV

TPBIAS0

TPBIAS0

TPB0N

TPB0N

TPB0P

TPB0P

TPA0N

TPA0N

TPA0P

TPA0P

FIL0

REXT

VREF

MDIO17

MDIO16

MDIO15

MDIO14

MDIO13

MDIO12

MDIO11

MDIO10

MDIO05

MDIO08

MDIO19

MDIO18

MDIO02

MDIO03

MDIO00

MDIO01

MDIO09

MDIO04

MDIO06

MDIO07

RSV

RSV

RSV

RSV

RSV

RSV

RSV

RSV

RSV

TPBIAS0

TPBIAS0

TPB0N

TPB0N

TPB0P

TPB0P

TPA0N

TPA0N

TPA0P

TPA0P

FIL0

REXT

VREF

MDIO17

MDIO16

MDIO15

MDIO14

MDIO13

MDIO12

MDIO11

MDIO10

MDIO05

MDIO08

MDIO19

MDIO18

MDIO02

MDIO03

MDIO00

MDIO01

MDIO09

MDIO04

MDIO06

MDIO07

RSV

RSV

RSV

RSV

RSV

RSV

RSV

RSV

RSV

TPBIAS0

TPBIAS0

TPB0N

TPB0N

TPB0P

TPB0P

TPA0N

TPA0N

TPA0P

TPA0P

FIL0

REXT

VREF

MDIO17

MDIO16

MDIO15

MDIO14

MDIO13

MDIO12

MDIO11

MDIO10

MDIO05

MDIO08

MDIO19

MDIO18

MDIO02

MDIO03

MDIO00

MDIO01

MDIO09

MDIO04

MDIO06

MDIO07

RSV

RSV

RSV

RSV

RSV

RSV

RSV

RSV

RSV

TPBIAS0

TPBIAS0

TPB0N

TPB0N

TPB0P

TPB0P

TPA0N

TPA0N

TPA0P

TPA0P

FIL0

REXT

VREF

MDIO17

MDIO16

MDIO15

MDIO14

MDIO13

MDIO12

MDIO11

MDIO10

MDIO05

MDIO08

MDIO19

MDIO18

MDIO02

MDIO03

MDIO00

MDIO01

MDIO09

MDIO04

MDIO06

MDIO07

RSV

RSV

RSV

RSV

RSV

RSV

RSV

RSV

RSV

TPBIAS0

TPBIAS0

TPB0N

TPB0N

TPB0P

TPB0P

TPA0N

TPA0N

TPA0P

TPA0P

FIL0

REXT

VREF

MDIO17

MDIO16

MDIO15

MDIO14

MDIO13

MDIO12

MDIO11

MDIO10

MDIO05

MDIO08

MDIO19

MDIO18

MDIO02

MDIO03

MDIO00

MDIO01

MDIO09

MDIO04

MDIO06

MDIO07

RSV

RSV

RSV

RSV

RSV

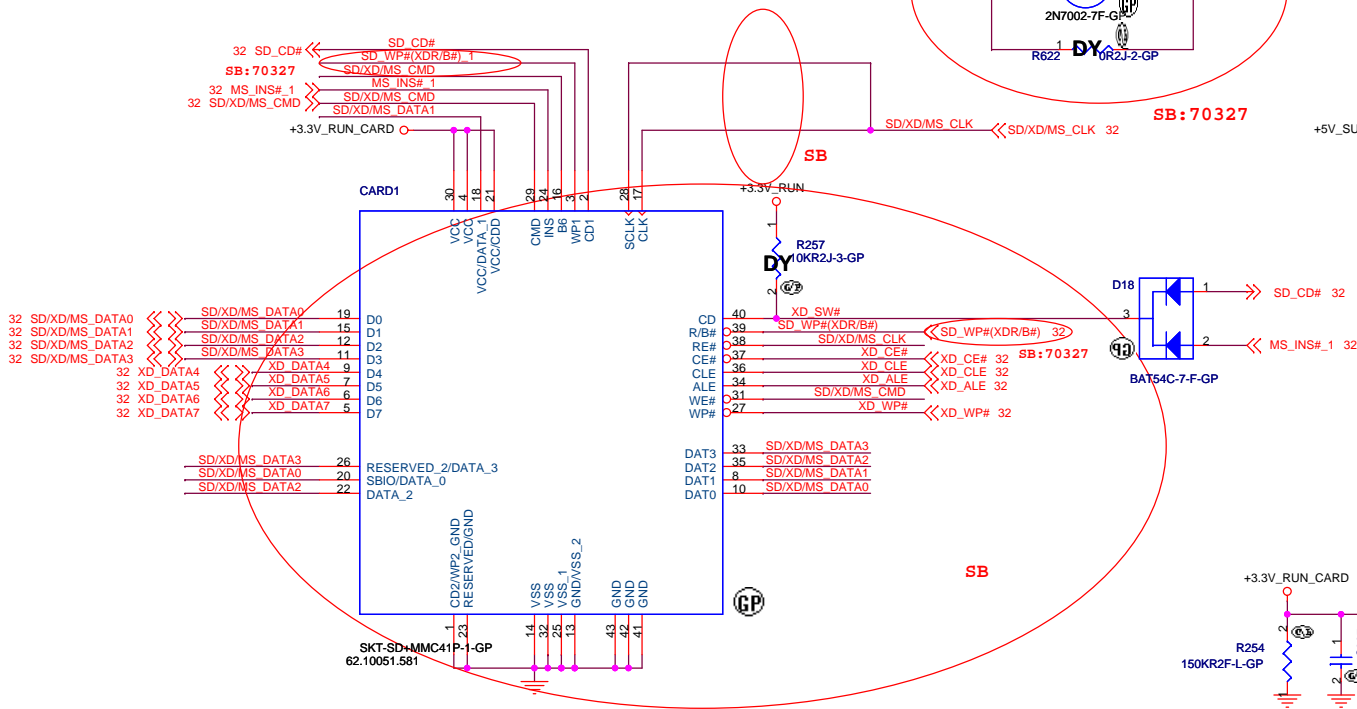
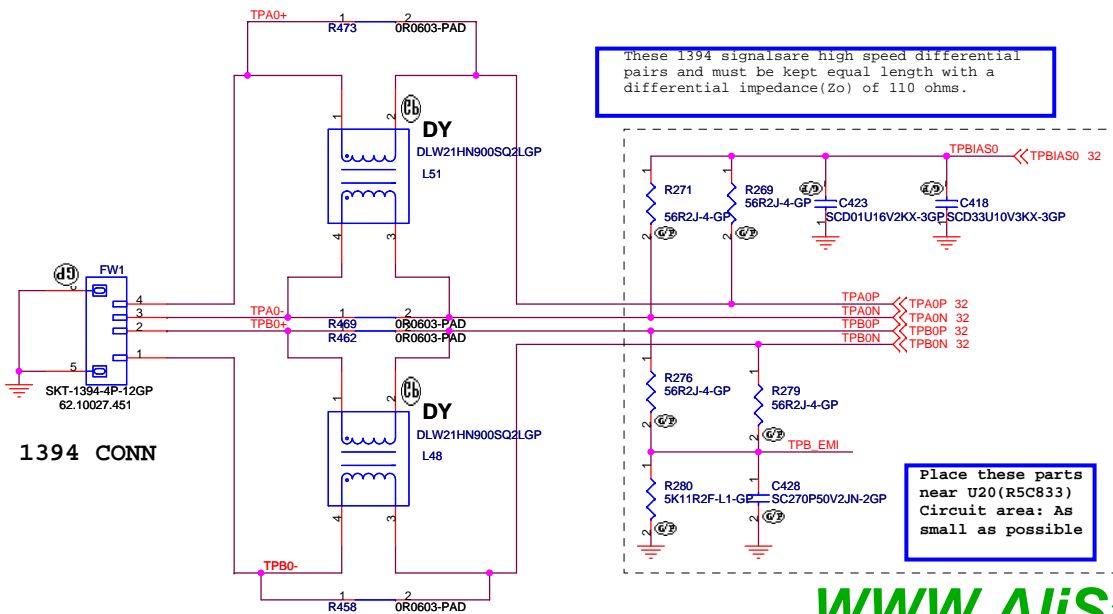
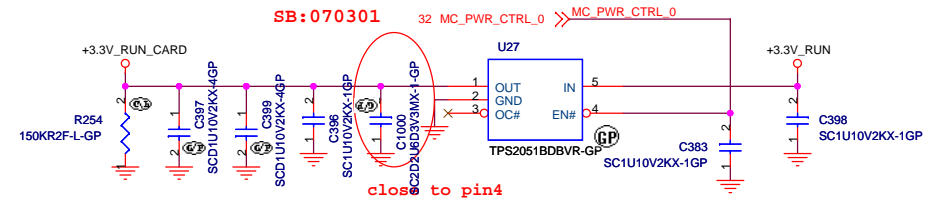
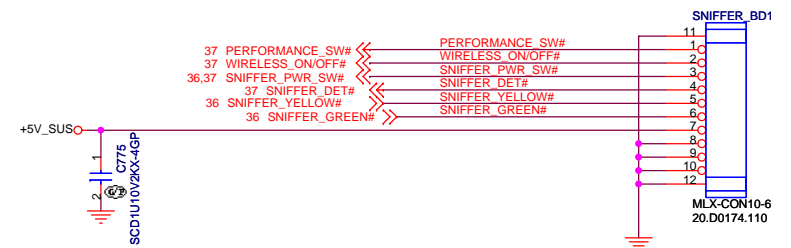
RSV

RSV

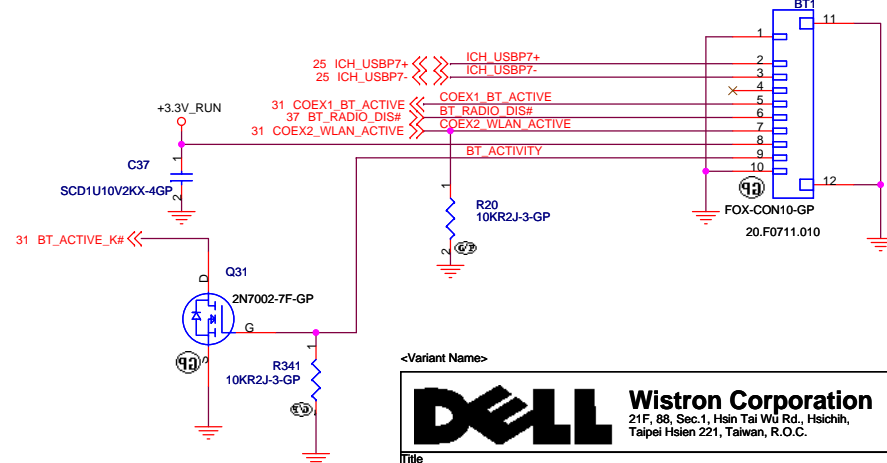
RSV

RSV

Card Reader CONN

**SNIFFER BOARD CONN**

Bluetooth Module conn.



<Variant Name>

DELL

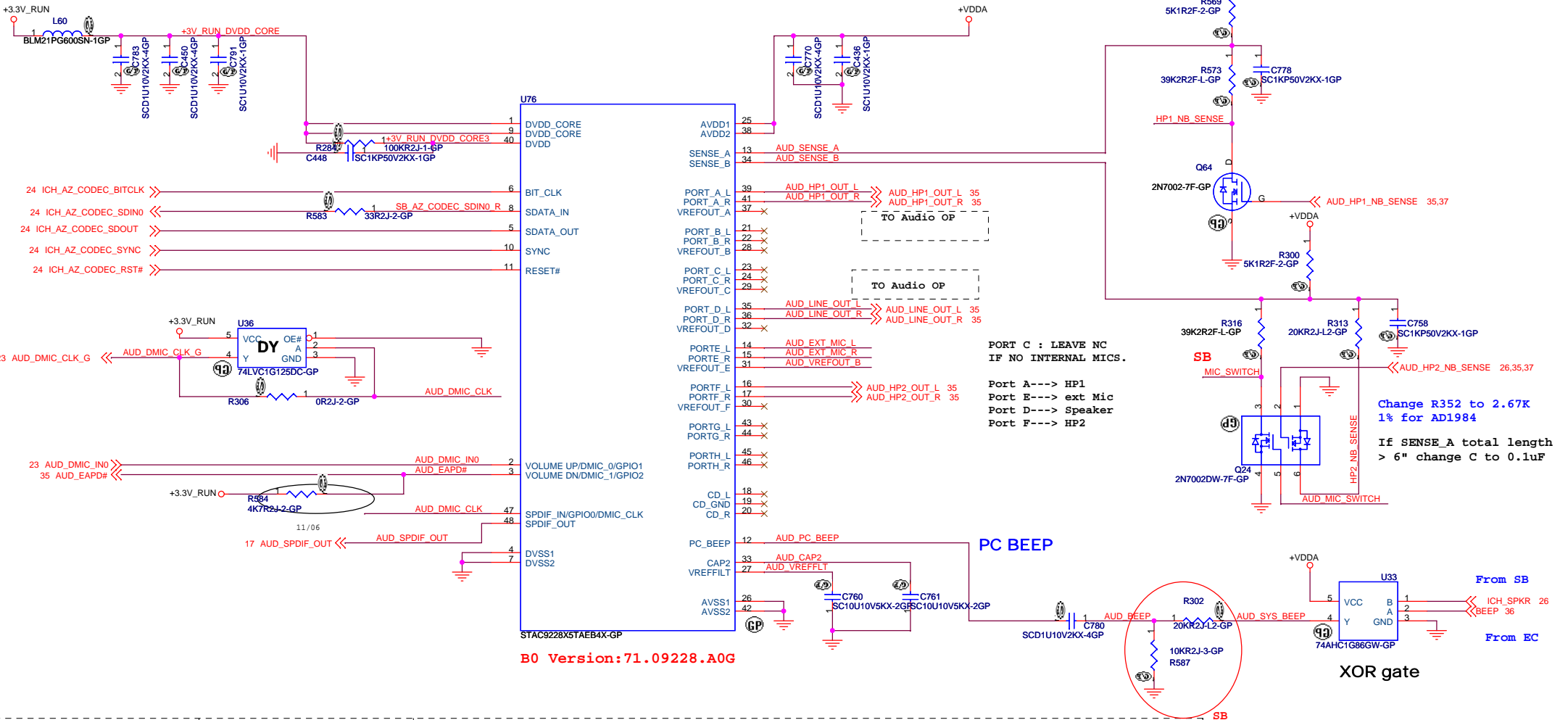
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Thurman Discrete

Size	Document Number
A3	8in1 /1394/SNIFFER BD CON/BT

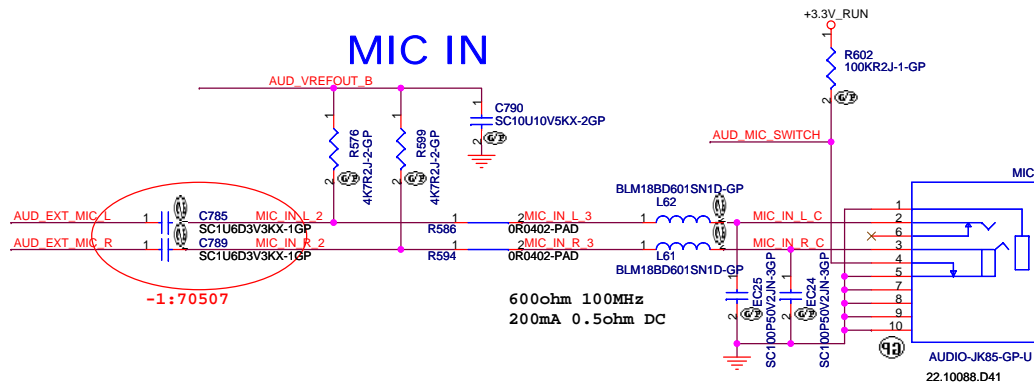
Date: Tuesday, November 06, 2007 Sheet 33 of 50



Azalia I/F EMI

Azalia I/F EMI

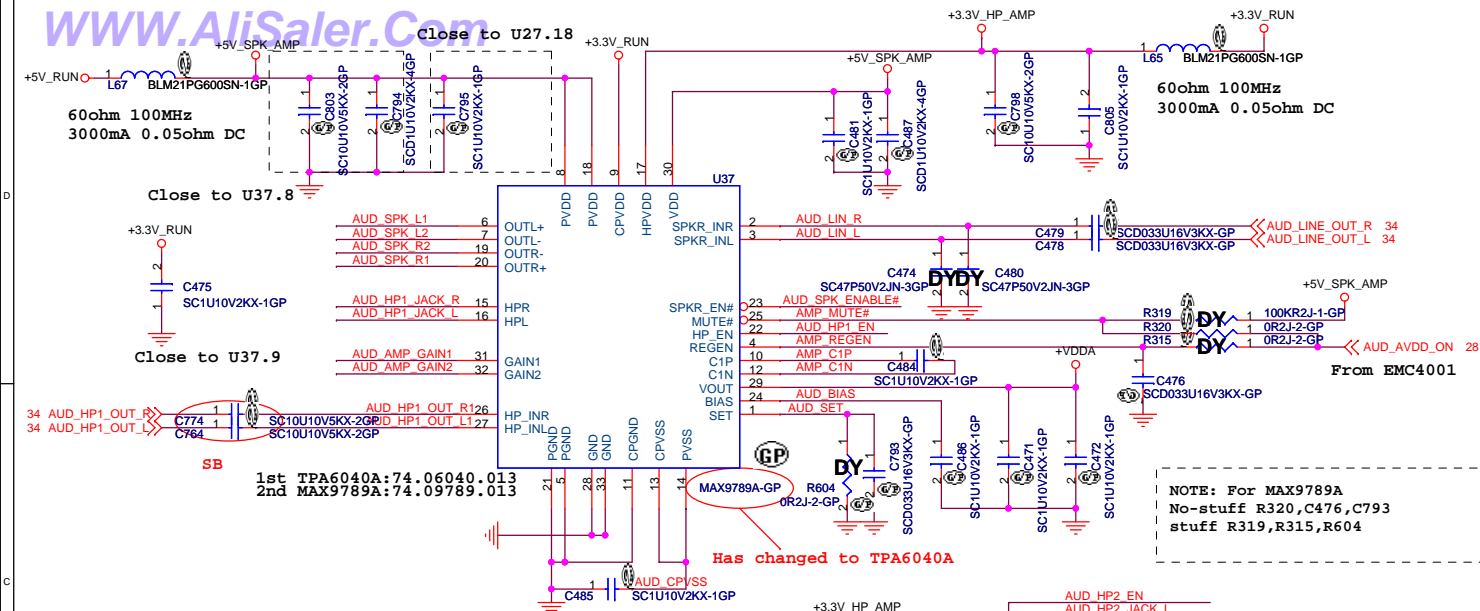
MIC IN



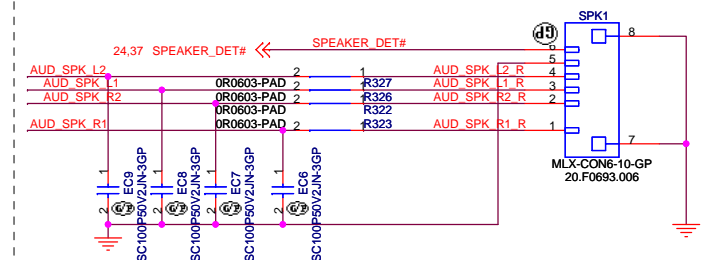
<Variant Name>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

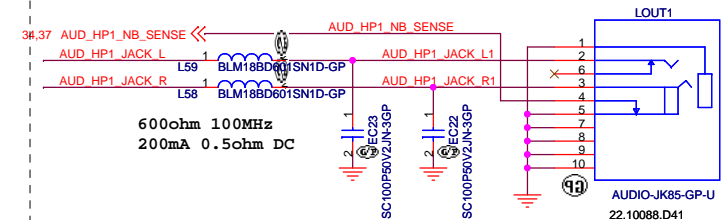
File
Size A3 Document Number
Date Thursday, November 22, 2007 Sheet 34 of 50
Rev -1
Thurman Discrete
CODEC STAC9228



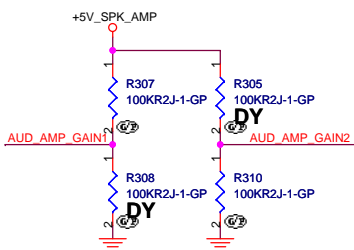
Speaker



LINE1 OUT

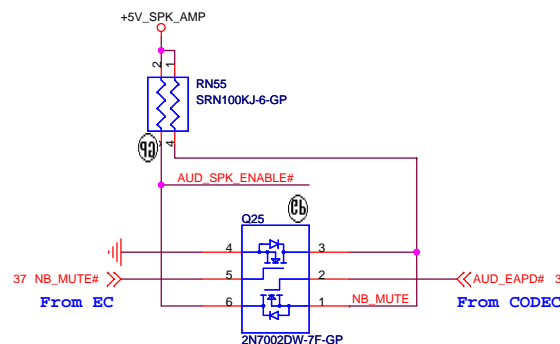


GAIN SETTING

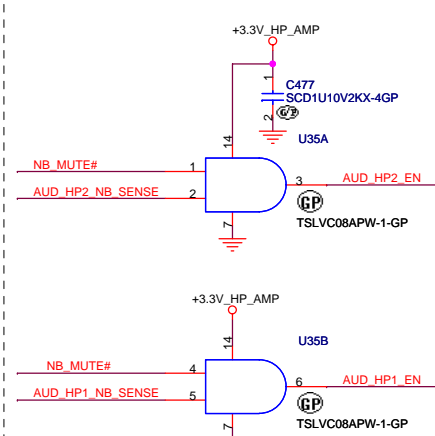


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

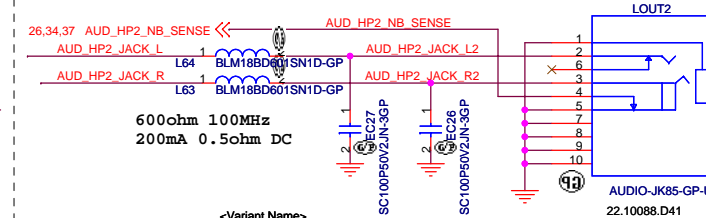
Signal inverter for speaker shutdown



AND Gate for HP Mute Function



LINE2 OUT



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size A3 Document Number

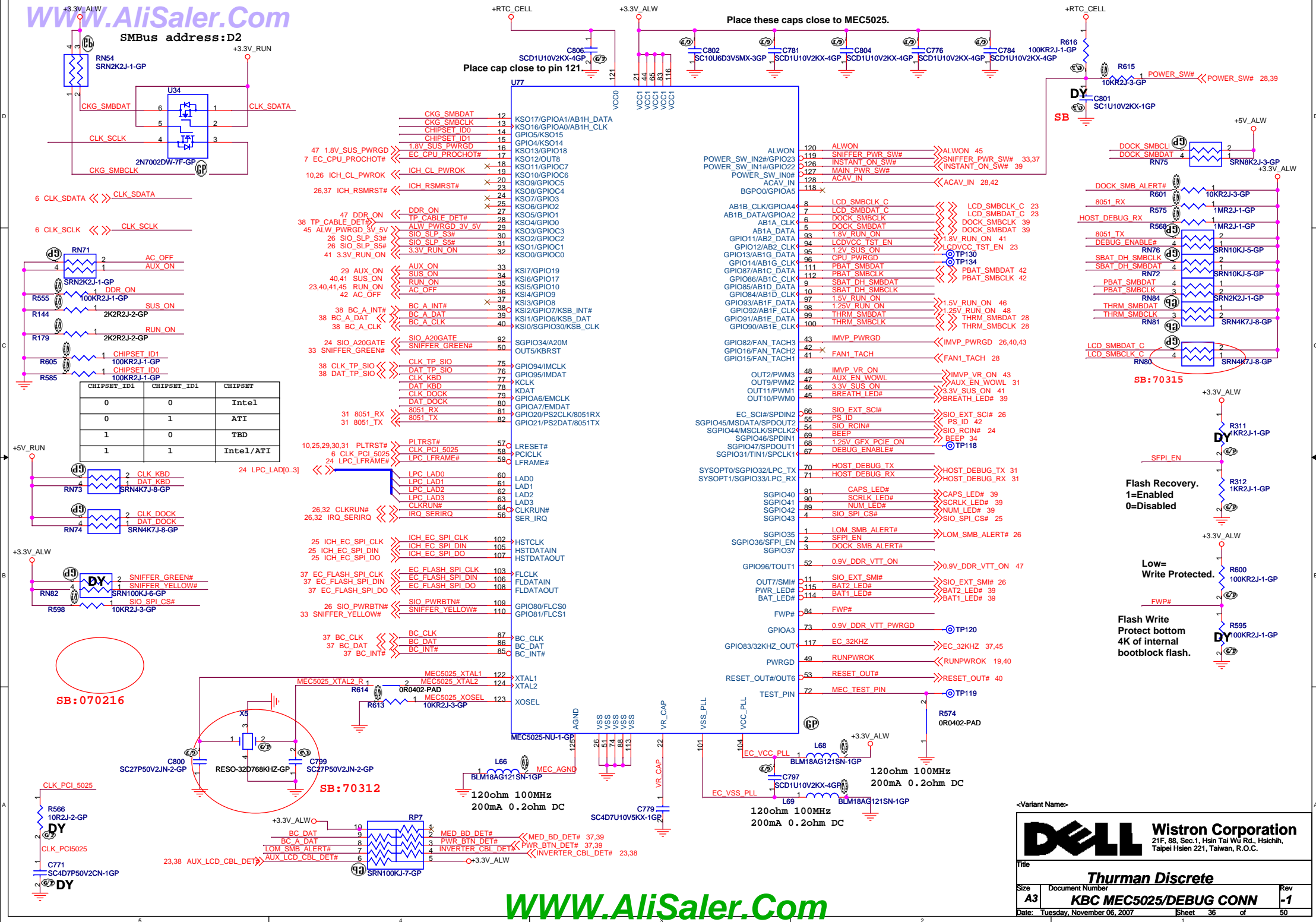
Thurman Discrete

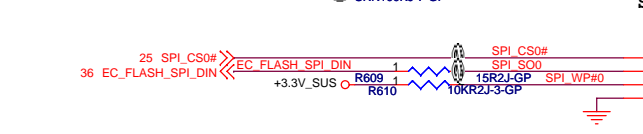
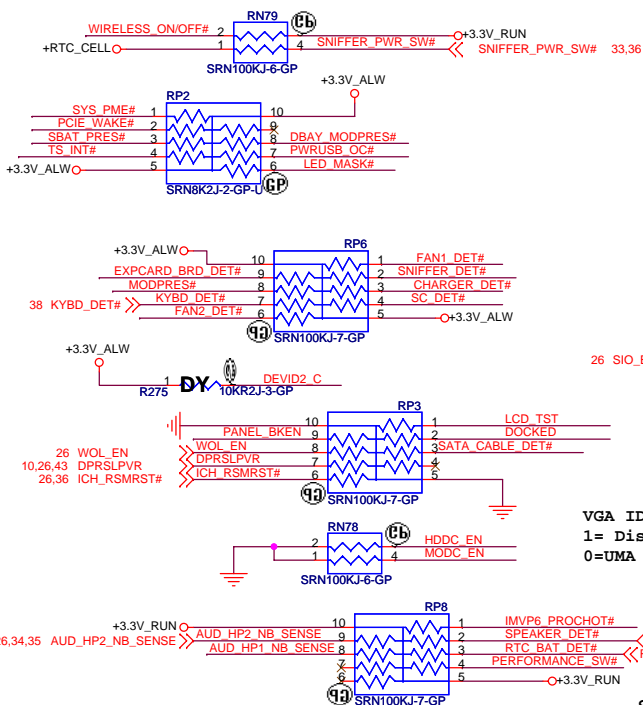
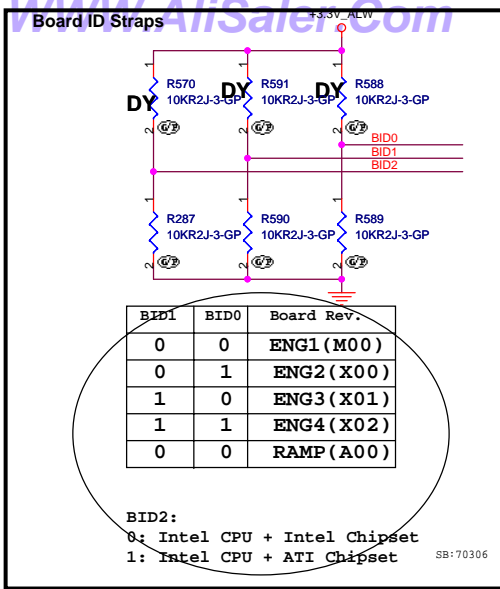
AUDIO AMP

Date: Tuesday, November 06, 2007

Rev -1

1 of 50

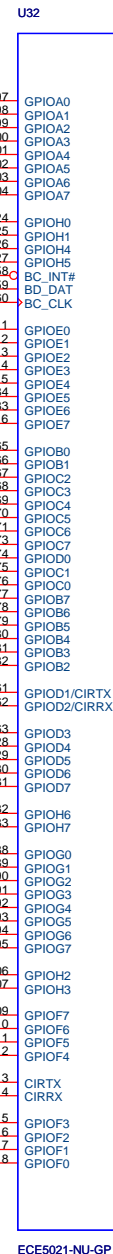
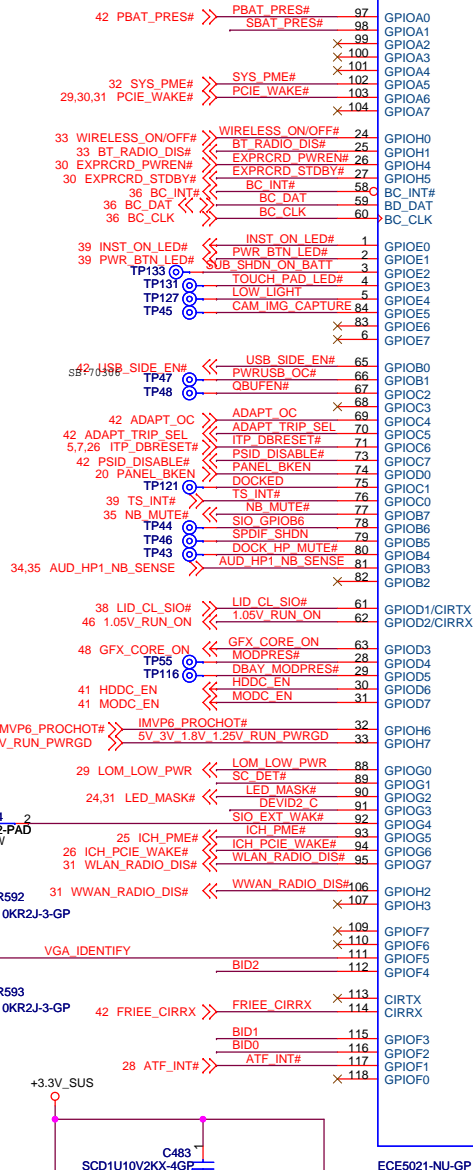




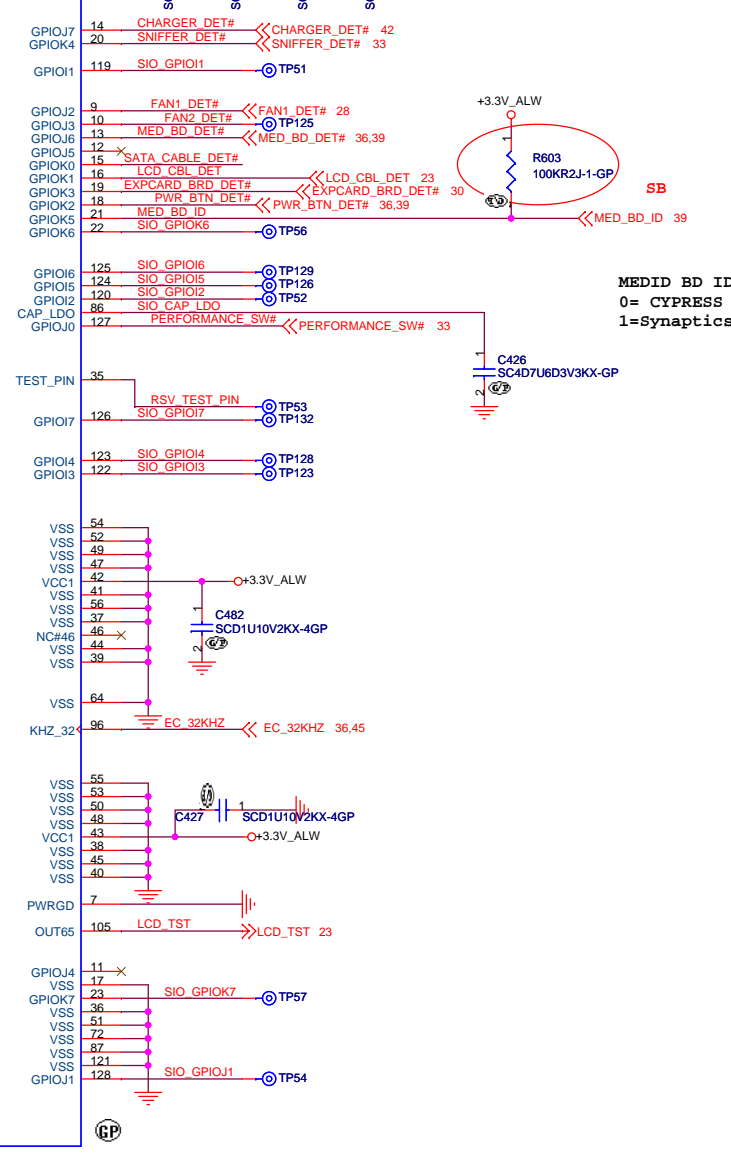
VGA IDENTITY
 1= Discrete GFX
 0=UMA

SPI

WWW.AliSaler.Com



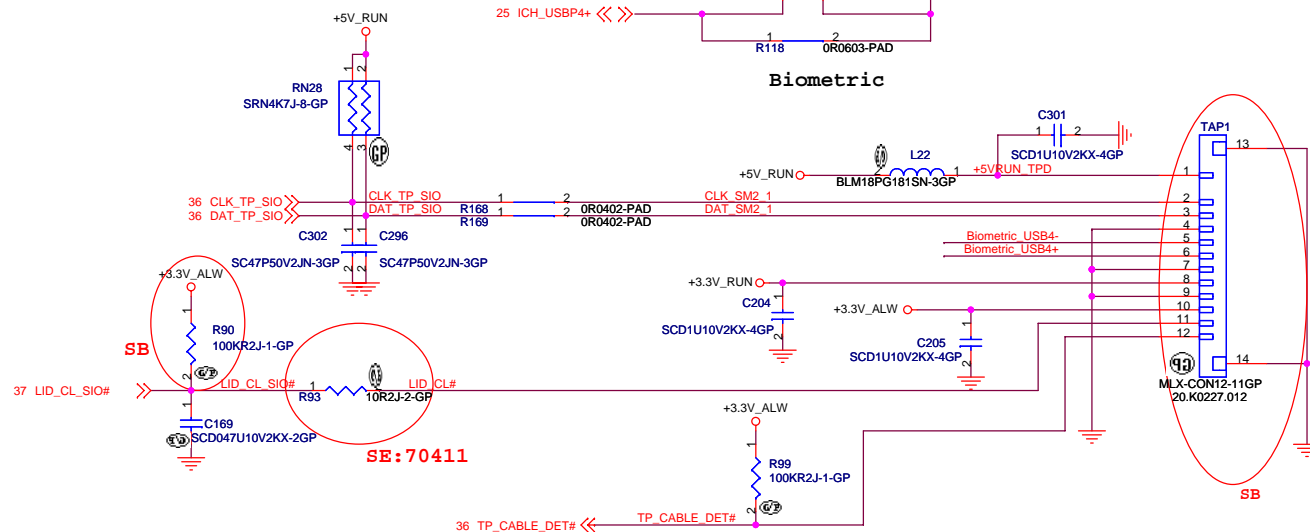
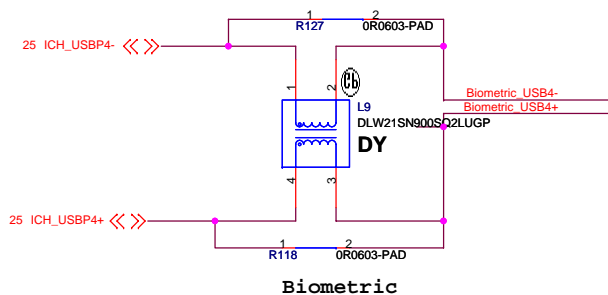
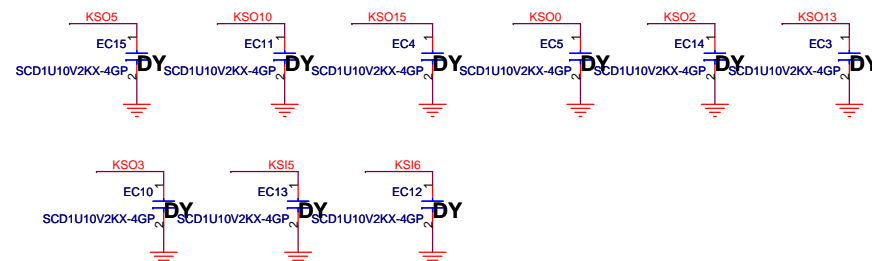
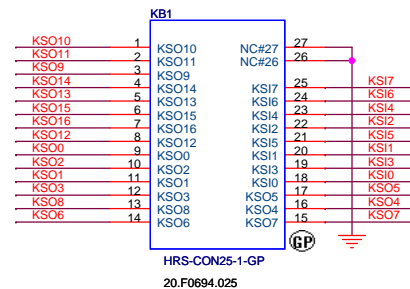
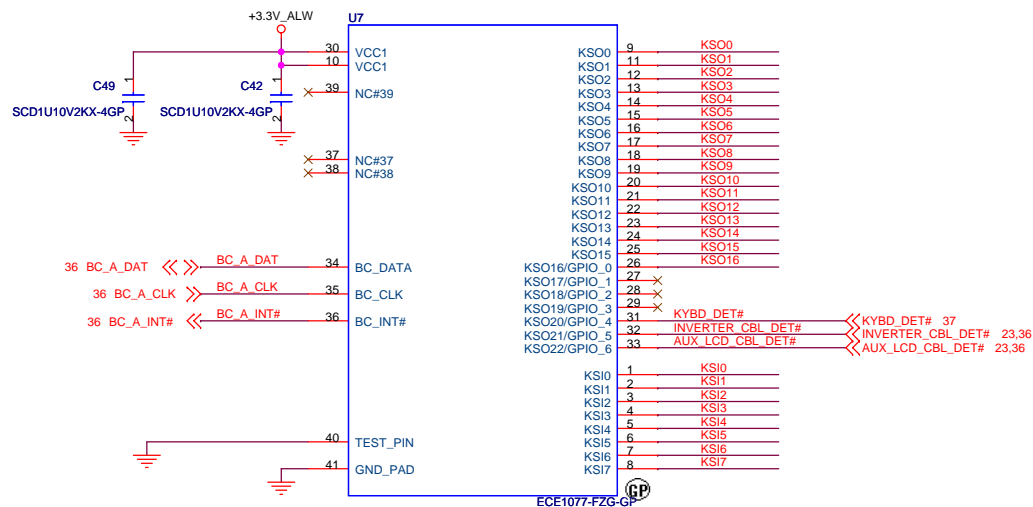
ECE5021-NU-GP



<Variant Name>

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
 Taipei Hsien 221, Taiwan, R.O.C.

Title			Thurman Discrete		
Size	Document Number		SIO ECE5011/SPI ROM		Rev
A3					-1
Date:	Tuesday, November 06, 2007		Sheet	37	of 50





CAPS LED

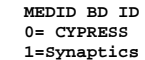
SCRLK LED

NUM LED

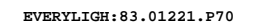
INSTANT POWER BUTTON LED

POWER / BUTTON LED

CONNECT TO THE LED Board



Power & Suspend LED

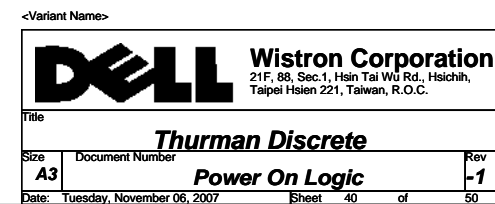


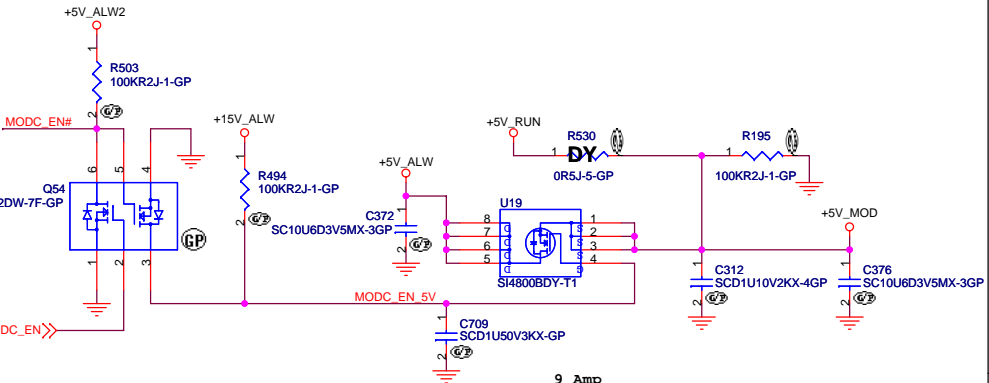
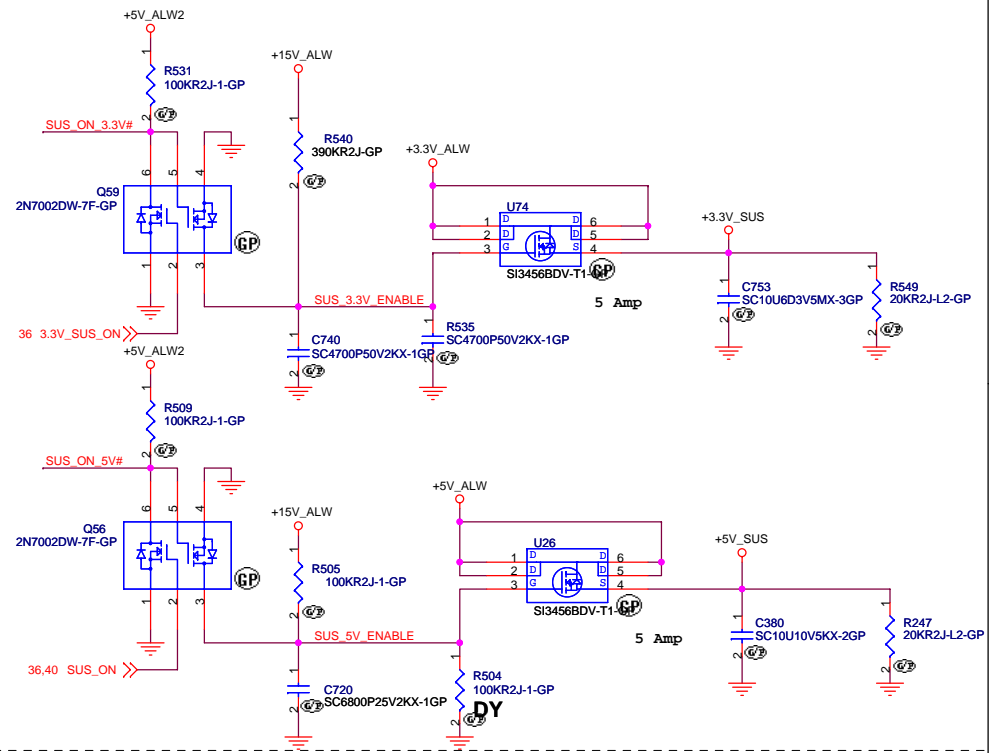
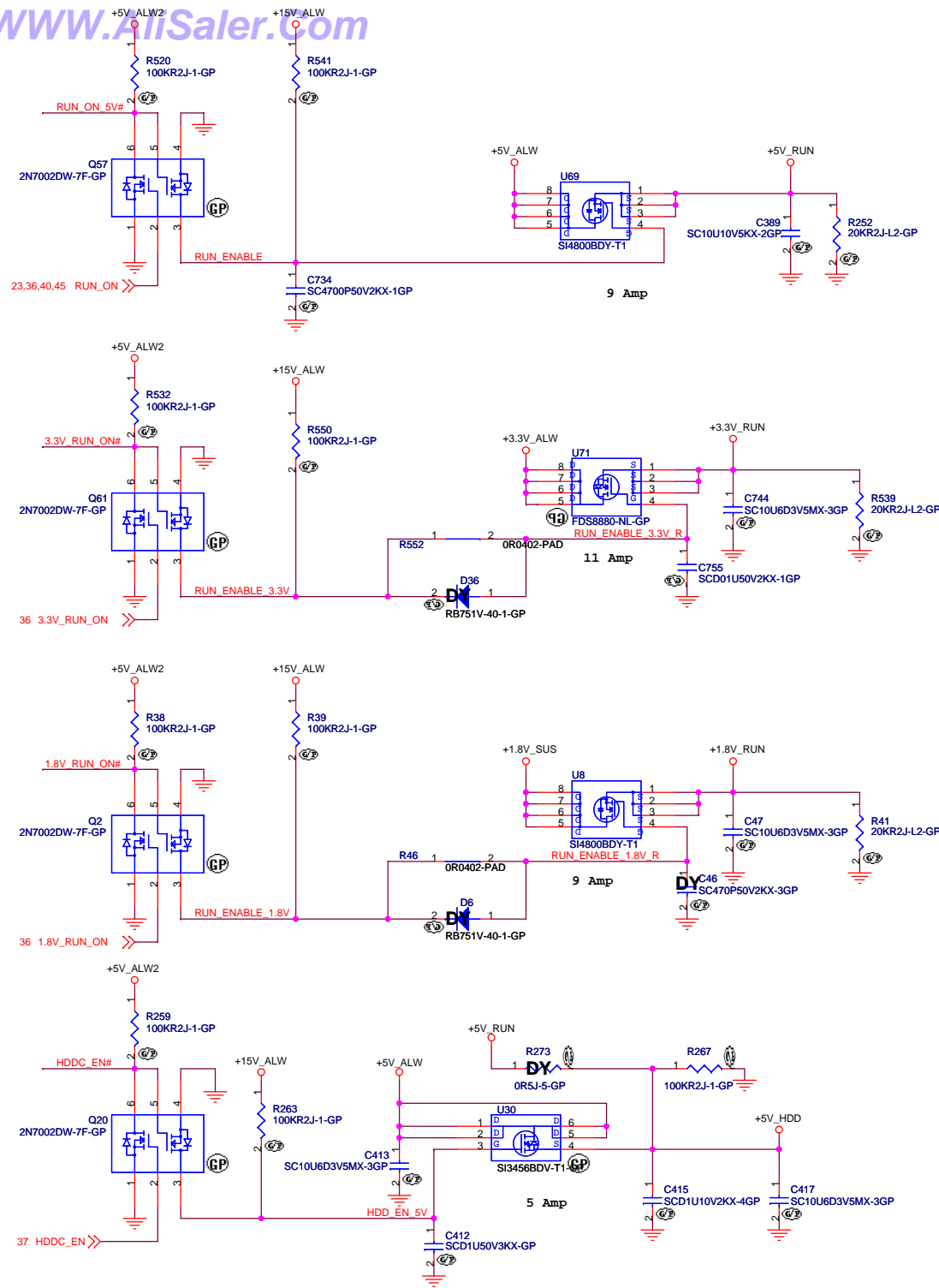
~~Battery LED~~



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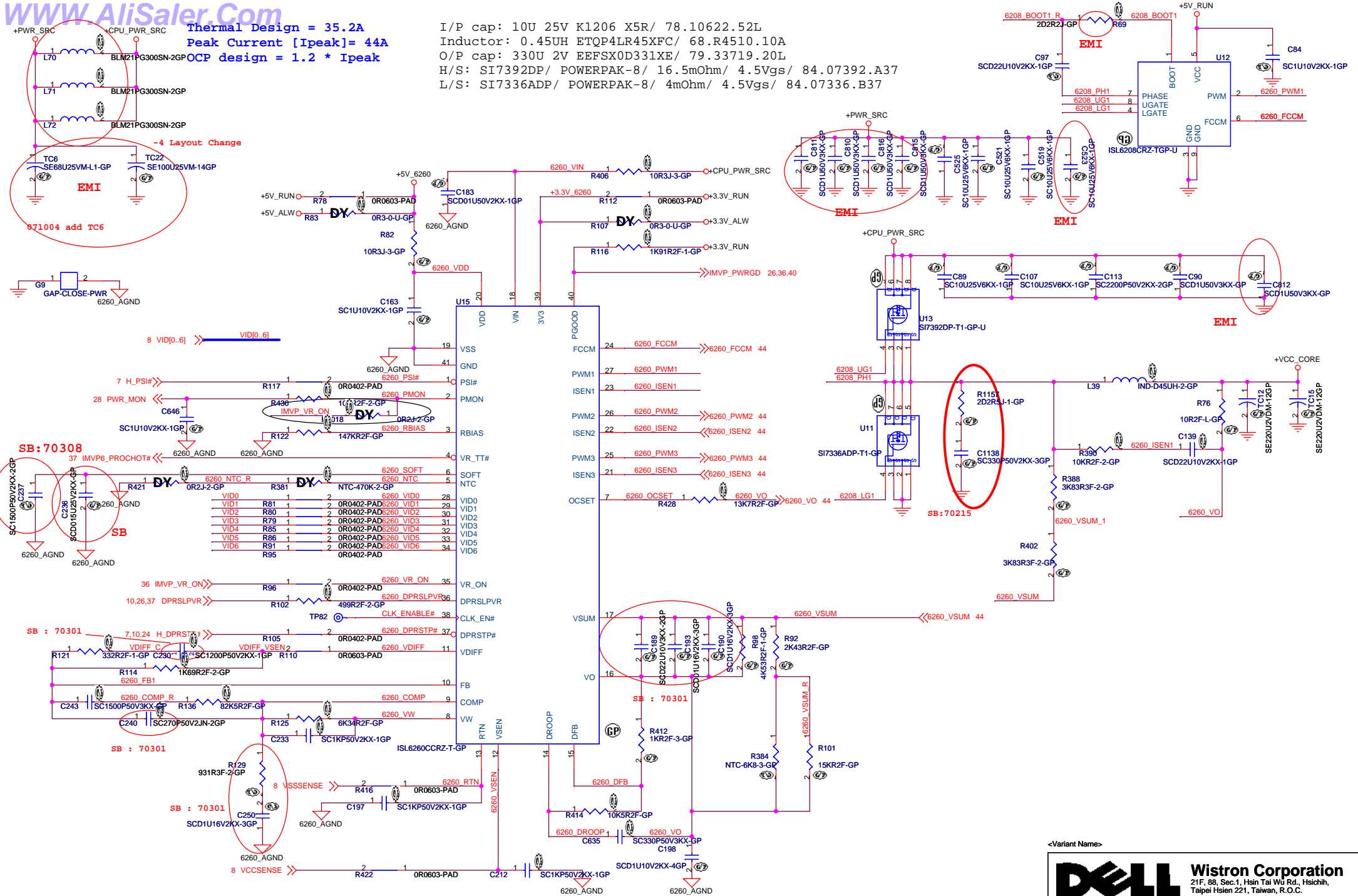






Thermal Design = 35.2A
Peak Current [Ipeak] = 44A
OCP design = 1.2 * Ipeak

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.45UH ETQP4LR45XFC/ 68.R4510.10A
O/P cap: 330U 2V EEF5X0D331XE/ 79.33719.20L
H/S: SI7392DP/ POWERPAK-8/ 16.5mOhm/ 4.5Vgs/ 84.07392.A37
L/S: SI7336ADP/ POWERPAK-8/ 4mOhm/ 4.5Vgs/ 84.07336.B37



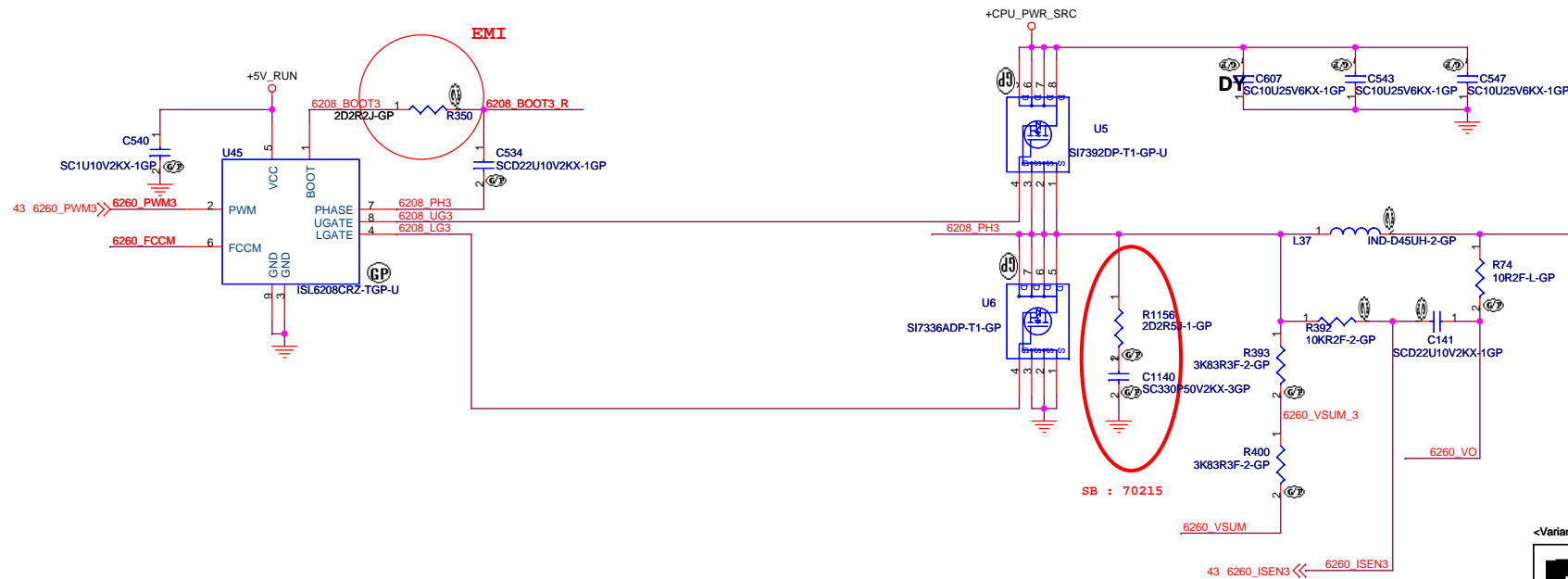
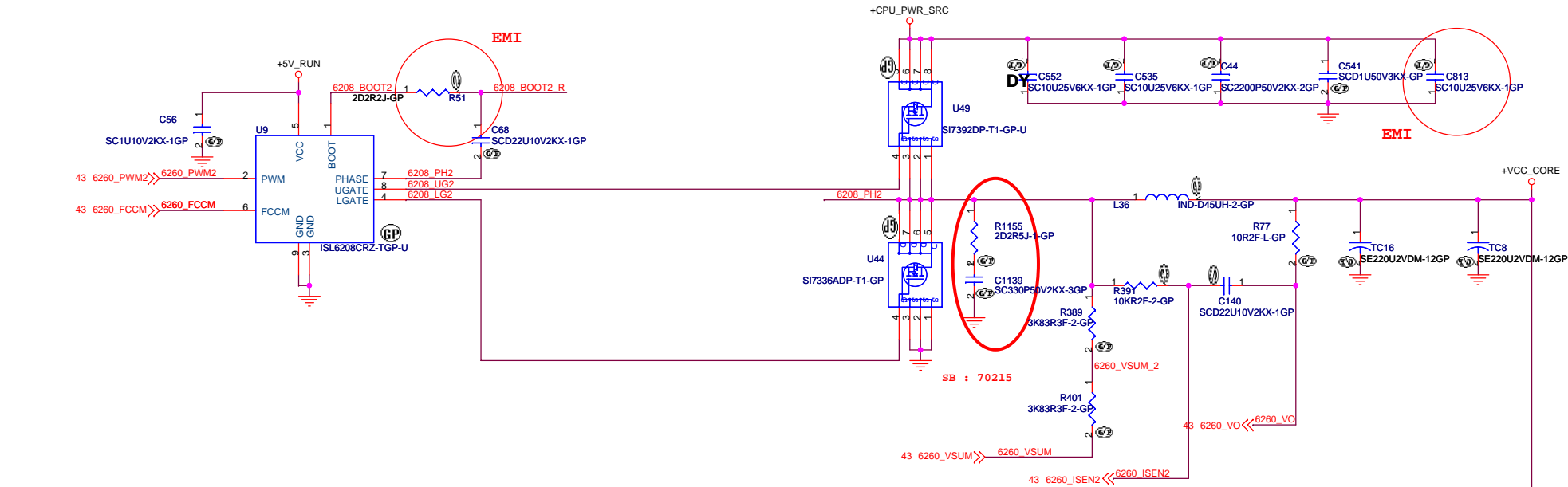
<Variant Name>

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Title: **Thurman Discrete**

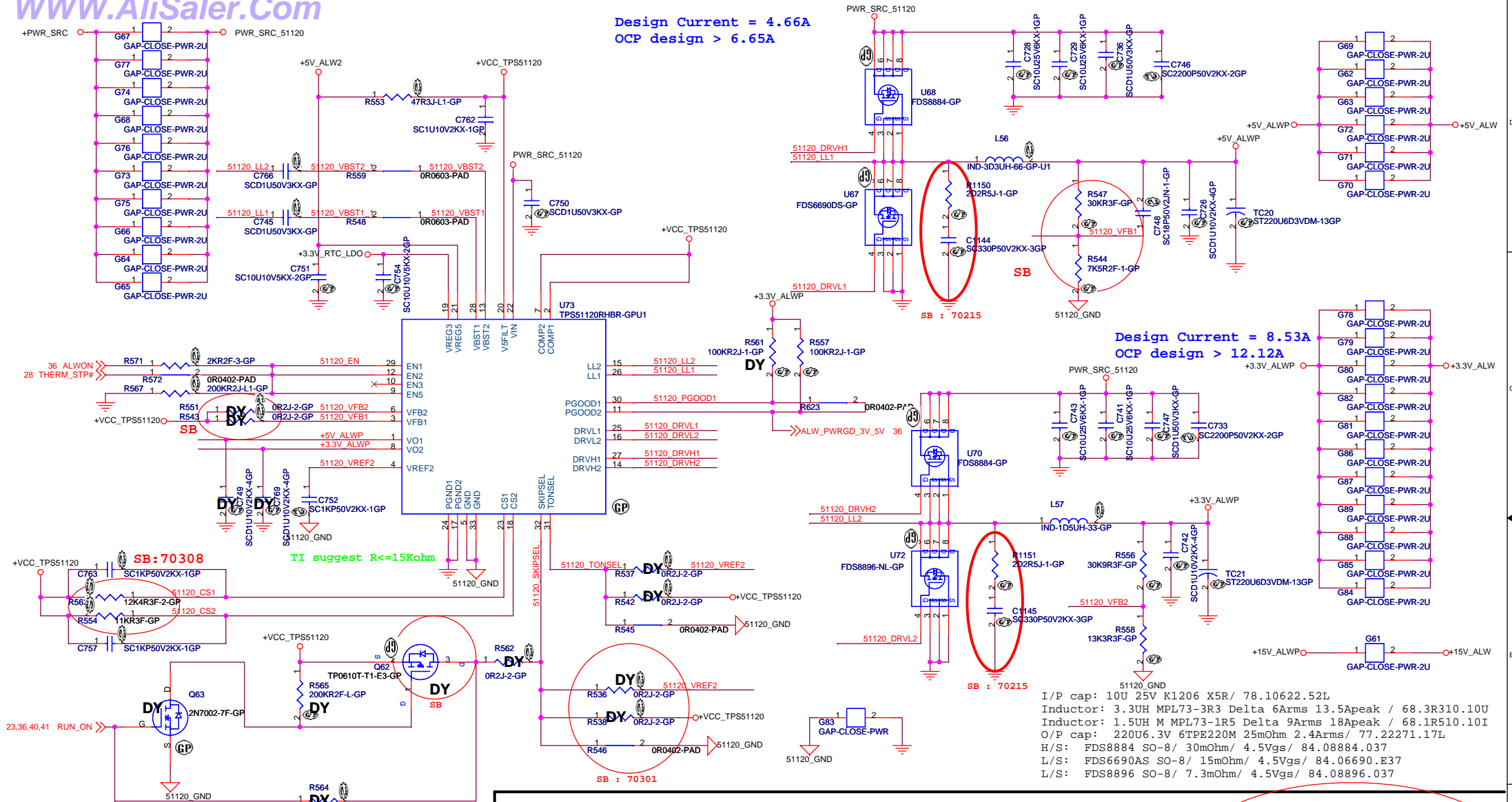
Size: **A3** Document Number: **CPU Core-01** Rev: **-1**

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Design Current = 4.66A
OCP design > 6.65A

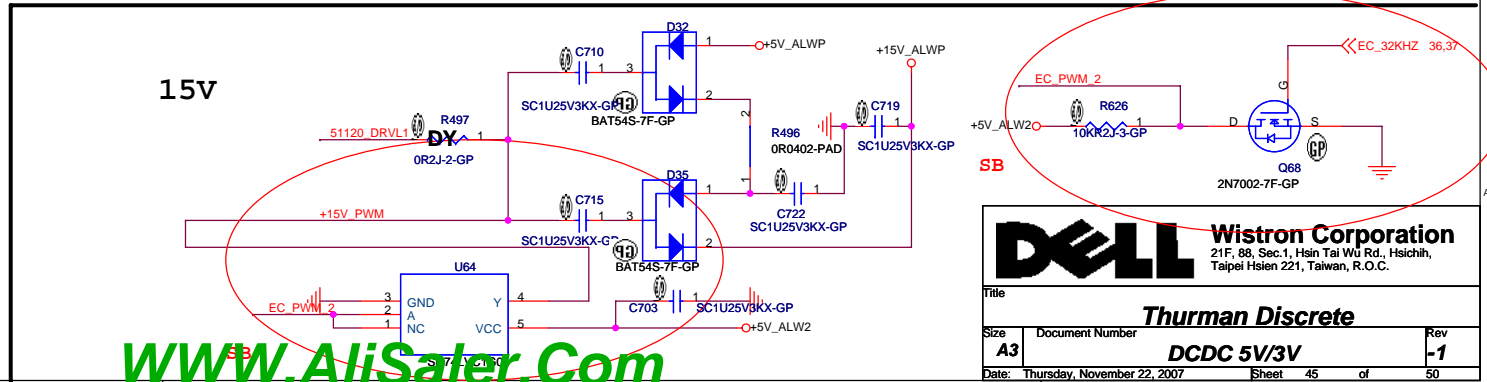
Design Current = 8.53A
OCP design > 12.12A



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH MPL73-3R3 Delta 6Arms 13.5Apeak / 68.3R310.10U
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U6.3V 6TPE220M 25mOhm 2.4Arms/ 77.22271.17L
H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37
L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037

$$V_{out} = 1V * (R1 + R2) / R2$$

	SKIPSEL	AUTOSKIP	VREF2	PWM	VSFILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM	
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE	
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2	
VFB1	N/A	not use	ADJ.	5V Fixed Output	
VFB2	N/A	not use	ADJ.	3.3V Fixed Output	
EN1,EN2	Switcher OFF	not use	Switcher ON	Switcher ON	
EN3,EN5	LDO OFF	not use	LDO ON	VR303 ON	

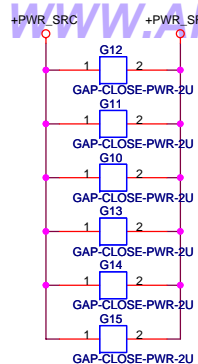


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Title: **Thurman Discrete**

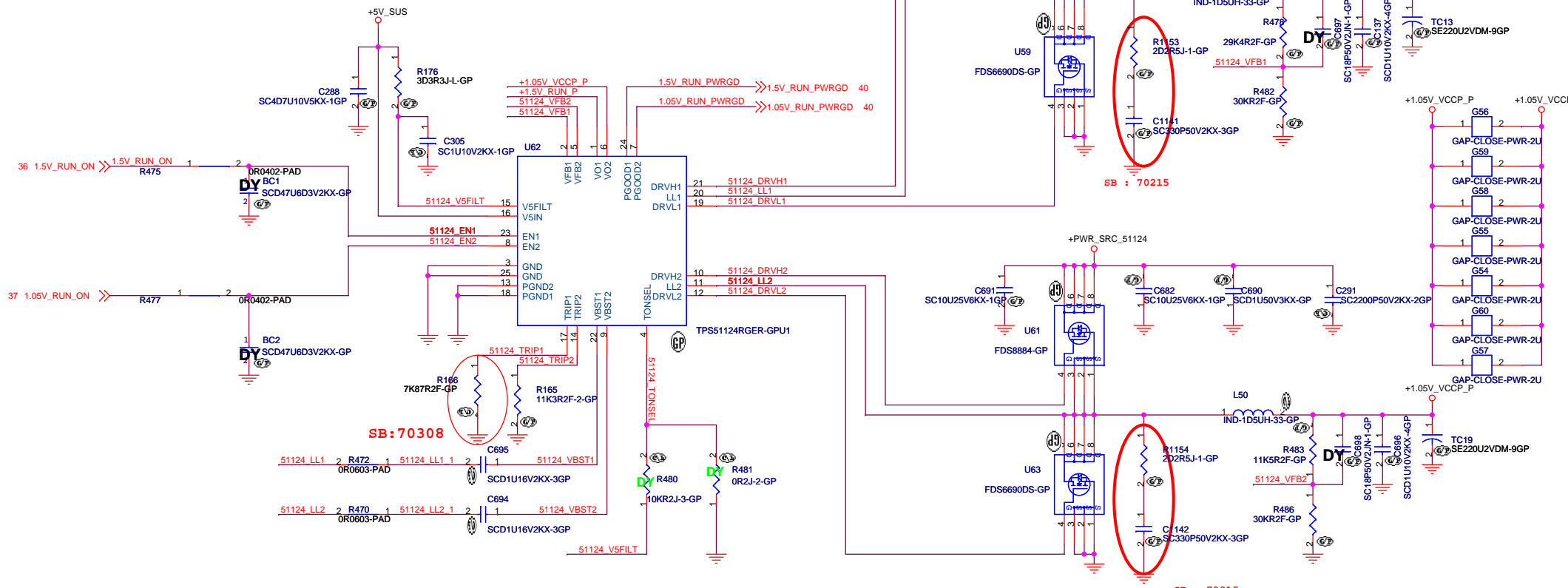
Size: **A3** Document Number: **DCDC 5V/3V** Rev: **-1**

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$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out})/V_{in}))$
 I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
 O/P cap: 220U 2V EEFSX0D221ER 9mOhm 3Arms Panasonic/ 79.22719.2PL
 H/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
 L/S: FDS6690AS SO-8/ 15mOhm/ 4.5Vgs/ 84.06690.E37

Design Current = 6.0A
 OCP design > 6.8A
 Included 1.25V LDO(3.02A)



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2)/R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2)/R2$ --> Skip Mode

Design Current= 5.9A
 OCP design > 7.3A

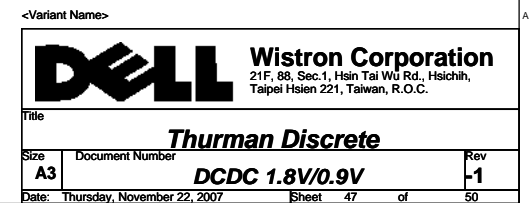
<Variant Name>

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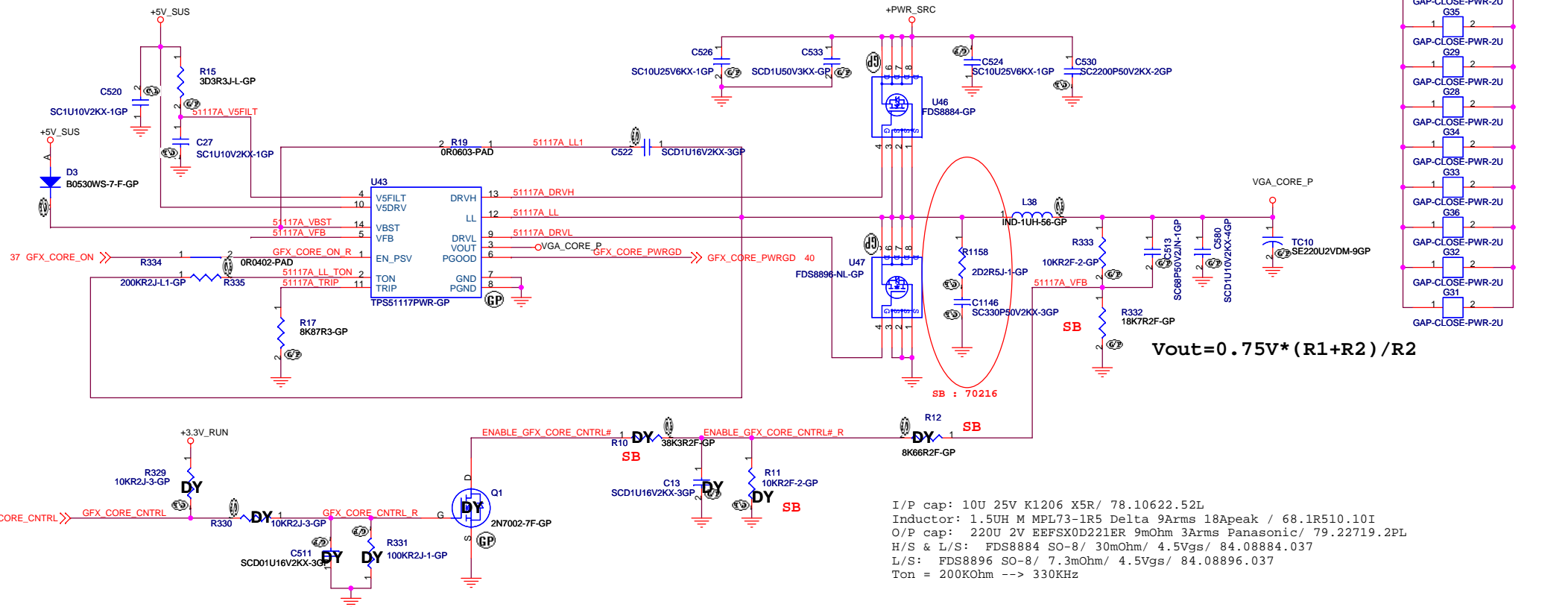
Title: **Thurman Discrete**

Size: **A3** Document Number: **DCDC 1.5V/1.05V** Rev: **-1**

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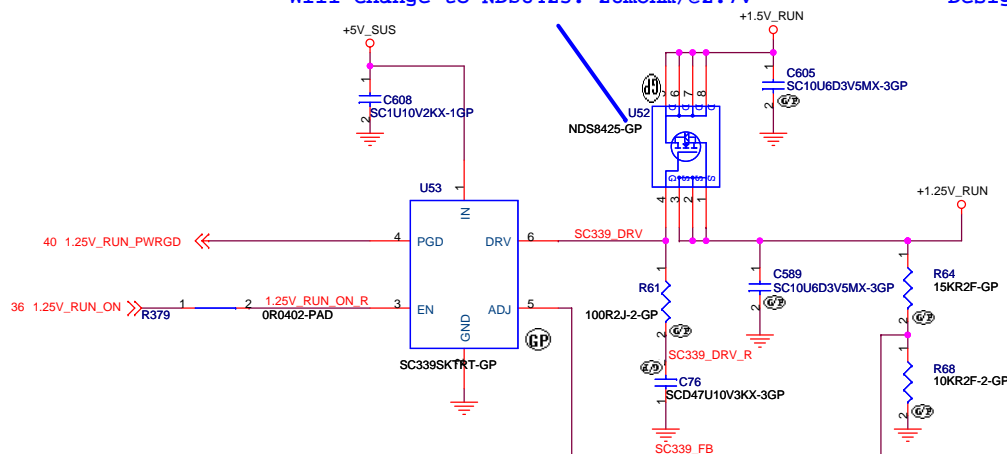


Design Current = 11A
 OCP design = 15A
 VGA_CORE = 1.0V



Will Change to NDS8425. 28mOhm/@2.7V

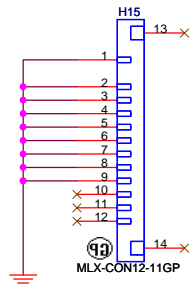
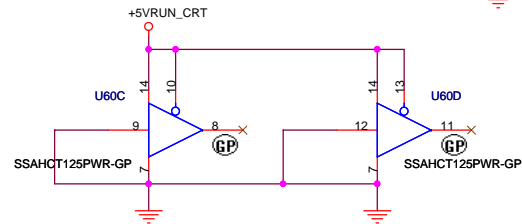
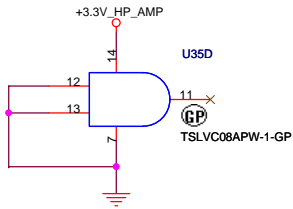
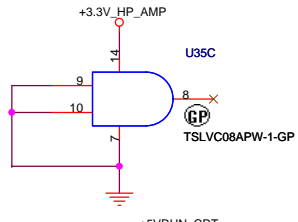
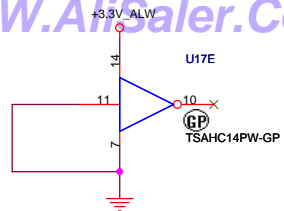
Design Current = 3.0A



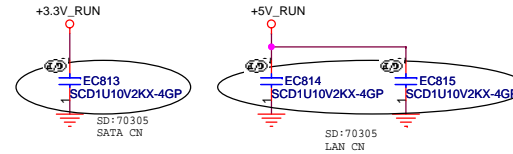
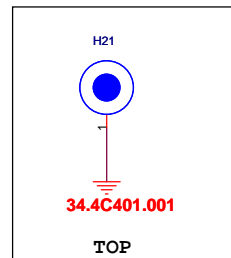
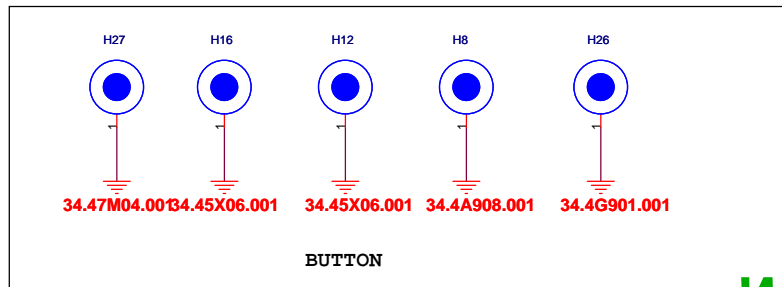
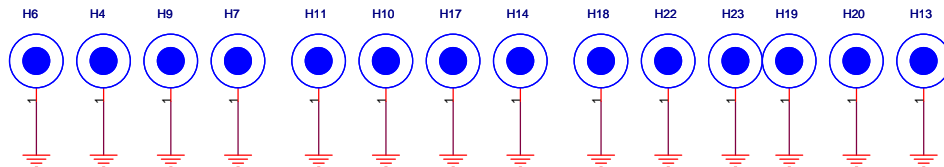
<Variant Name>

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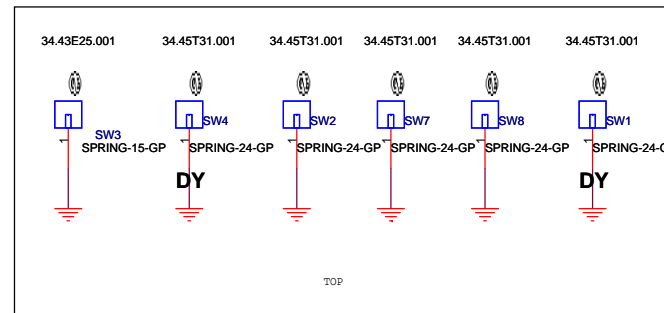
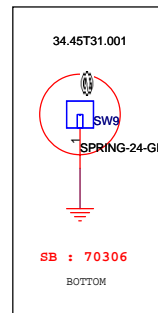
Title
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DCDC VGA_Core/1.25V
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34.4C309.001



SW3 - 34.43E25.001
SW9 - 34.49Q02.001
SW5 - 34.34T31.001 (Only for UMA)
others-34.45T31.001



<Variant Name>



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Title

Thurman Discrete

Size

Document Number

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<Variant Name>					
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsiehchih, Taipei Hsien 221, Taiwan, R.O.C.			
Title <i>Thurman Discrete</i>					
Size A3	Document Number HISTORY				Rev -1
Date:	Tuesday, November 06, 2007	Sheet	50	of	50