


Main Power Rails

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+0.75V_DDR_VTT	+0.75V	DDR3 reference voltage	RUN_ON	
+0.85V	+0.9V	Intel new power rail	1.05V_VTT_PWRGD	
+1.05V_LAN_M	+1.05V	LAN M power for iAMT	SLP_LAN#	
+1.05V_M	+1.05V	ME power for iAMT	SLP_A#	
+1.05V_PCH	+1.05V	PCH core power	RUN_ON	
+1.05V_SUS	+1.05V	USB3.0 chip power	SUSD	
+1.05V_VTT	+1.05V	CPU core logic power	RUN_ON	
+1.5V	+1.5V	I/O module power	RUN_ON	
+1.5V_CPU	+1.5V	CPU DDR3 controller power	RUN_ON_D	
+1.5V_GPU	+1.5V	GPU DDR3 controller power	PG_1.5V_EN	
+1.5V_SUS	+1.5V	DDR3 SODIMM power	SUS_ON	
+1.8V	+1.8V	CPU/PCH/LVDS power	RUN_ON	
+1.8_GPU	+1.8V	GPU power	+1.5V_GPU	
+1V_GPU	+1V	GPU PCIE VDDC power	PG_1V_EN	
+3V	+3.3V	I/O power	RUN_ON	
+3V_GPU	+3.3V	GPU power	DGPU_PWR_EN#	
+3V_M	+3.3V	PCH/SPI power for iAMT	SLP_A#	
+3V_S5	+3.3V	3V power sequence	S5_ON	
+3V_SUS	+3.3V	USB3.0 chip power	SUSD	
+3VPCU	+3.3V	Always power	SYS_SHDN#	
+5V	+5V	I/O power	RUN_ON	
+5V_S5	+5V	5V power sequence	S5_ON	
+5V_SUS	+5V	USB2.0 power	SUSD	
+5VPCU	+5V	Always power	SYS_SHDN#	
+15V_ALW	+15V	Power sequence		
+SMDDDR_VREF	+0.75V	DDR3 reference power	RUN_ON	
+VCC_CORE	+1.1V	CPU Core power	VRON	
+VCC_GFX	+1.52V	Internal GPU Core power	VRON	
+VGPU_CORE	+1V	GPU Core power	DGPU_VRON	
+VGPU_IO	+1V	GPU I/O controller power	PG_GPUUIO_EN	
+VIN	+19V	AC power input		

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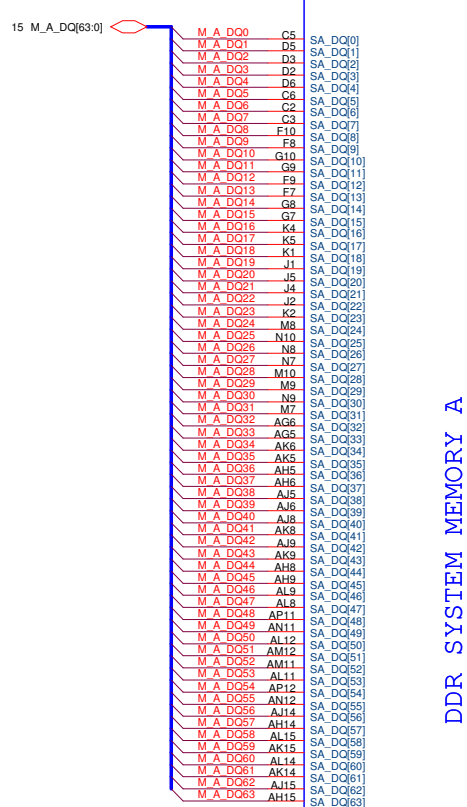
Quanta Computer Inc.

Project Name: GM7C

Title		
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Size	Document Number	Rev
	GM7C_MB	C
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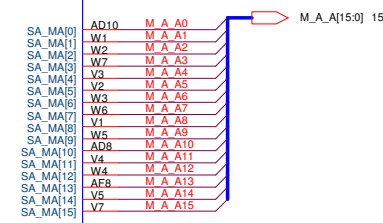
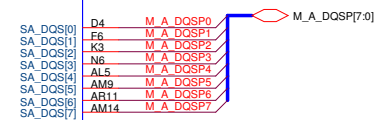
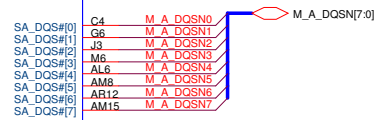
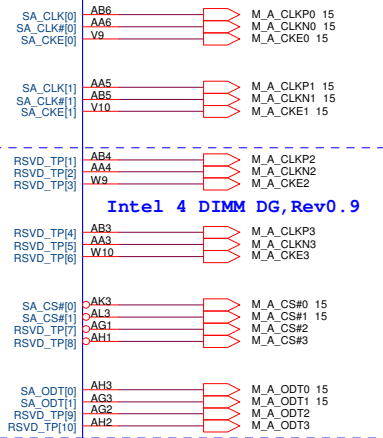


U28C

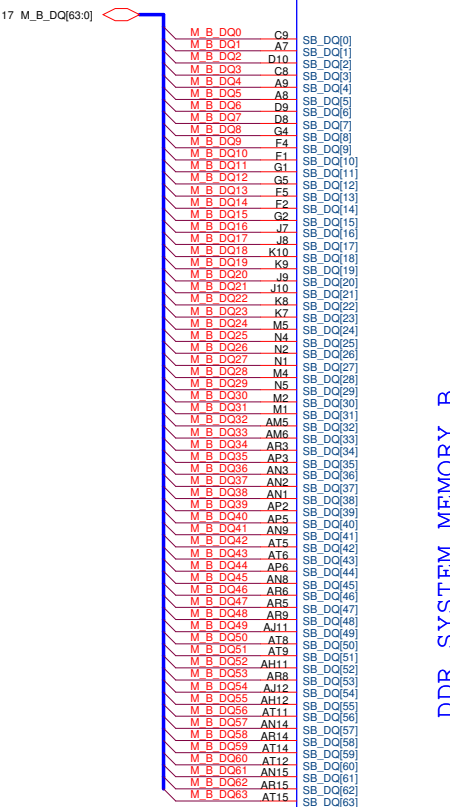


CPU-989P-rPGA

DDR SYSTEM MEMORY A

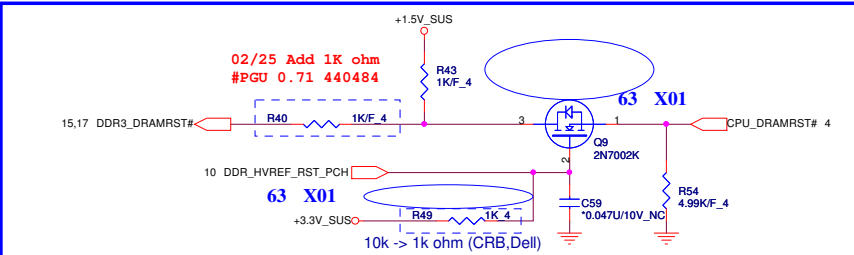
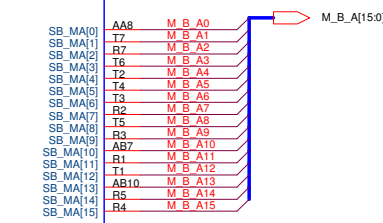
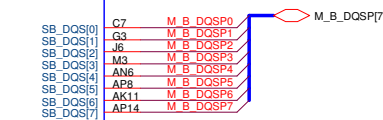
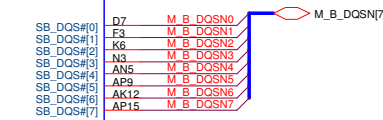
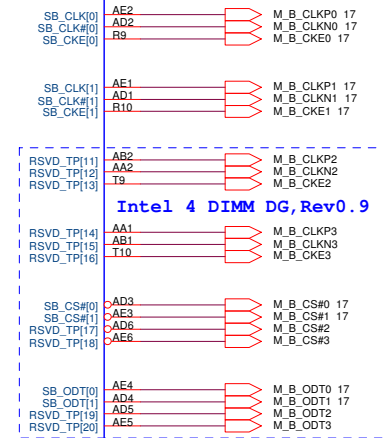


U28D



CPU-989P-rPGA

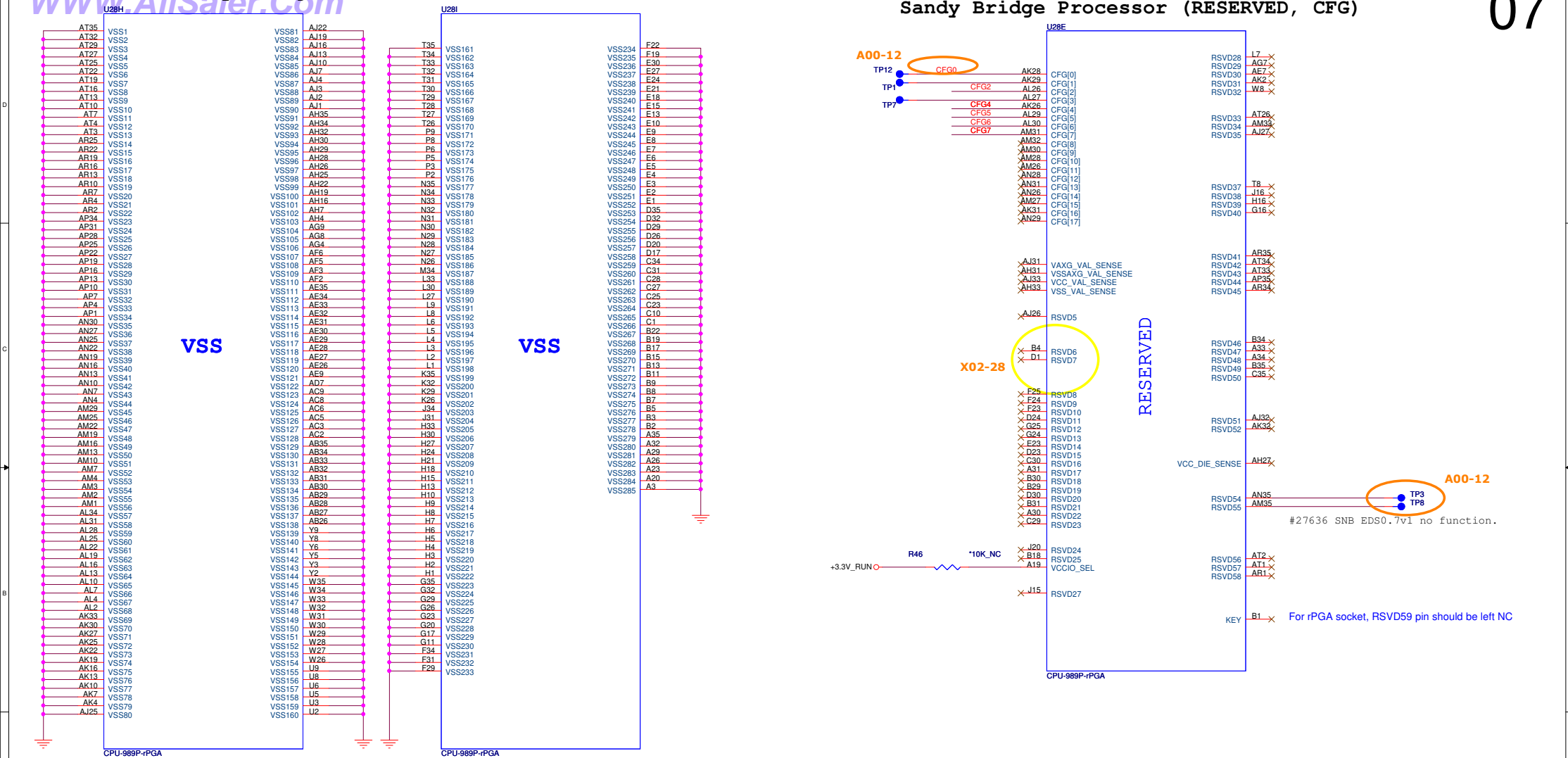
DDR SYSTEM MEMORY B



Quanta Computer Inc.
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Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)

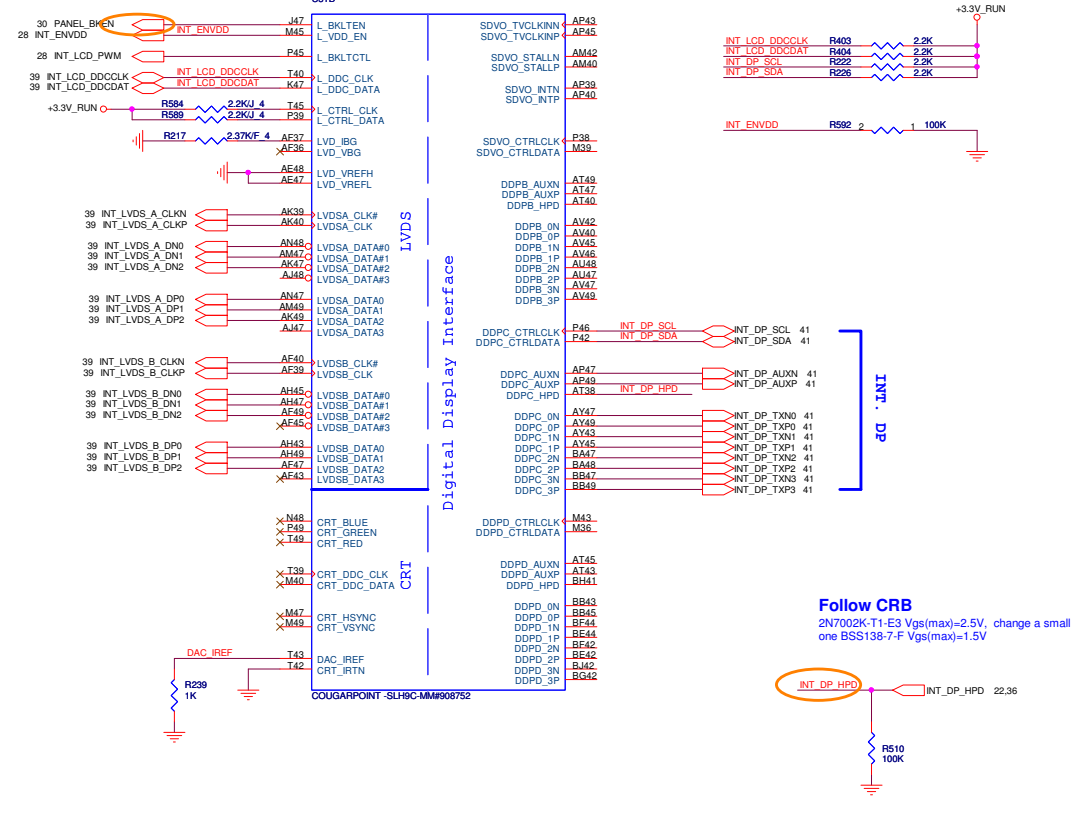
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



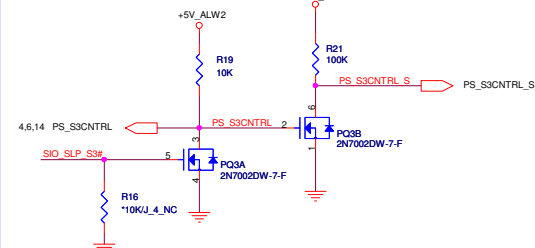
Quanta Computer Inc.
Project Name: **GM7C**

Title	SNB 4/4_GND		
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U31D



S3 Power Reduce



WWW.AliSaler.Com

36 ACZ_BITCLK \leftarrow R283 33U 4 ACZ_BITCLK R
 C592 50 22P/50V NC X02-11
 36 ACZ_SYNC \leftarrow R322 33U 4 ACZ_SYNC L
 30,36 ACZ_RST# \leftarrow R298 33U 4 ACZ_RST# R
 36 ACZ_SDOUT \leftarrow R316 33U 4 ACZ_SDOUT R

A00-12

+3.3V_SUS

R285 210F_4

R282 210F

R274 210F_4

R266 51U_4

R288 100F_4

R286 100F

R276 100F_4

PCH_JTAG_TMS_R




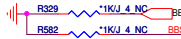





PCH_JTAG_T00_R

PCH_JTAG_TDI_R

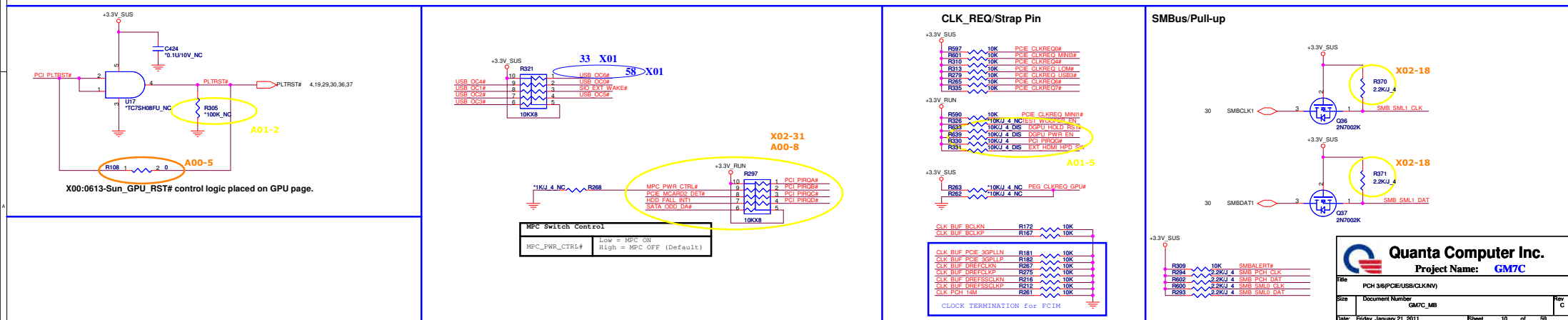
PCH_JTAG_TCK_R

Diagram illustrating the connection for the WWAN_HADIO_BIST# pin (MODC_EN) using a voltage divider circuit. The circuit consists of a 10K resistor (R377) in series with a 10K resistor (R227) connected to a +3.3V_RUN supply. The output of the divider is connected to the WWAN_HADIO_BIST# pin, which is also labeled as MODC_EN.

[illegible]

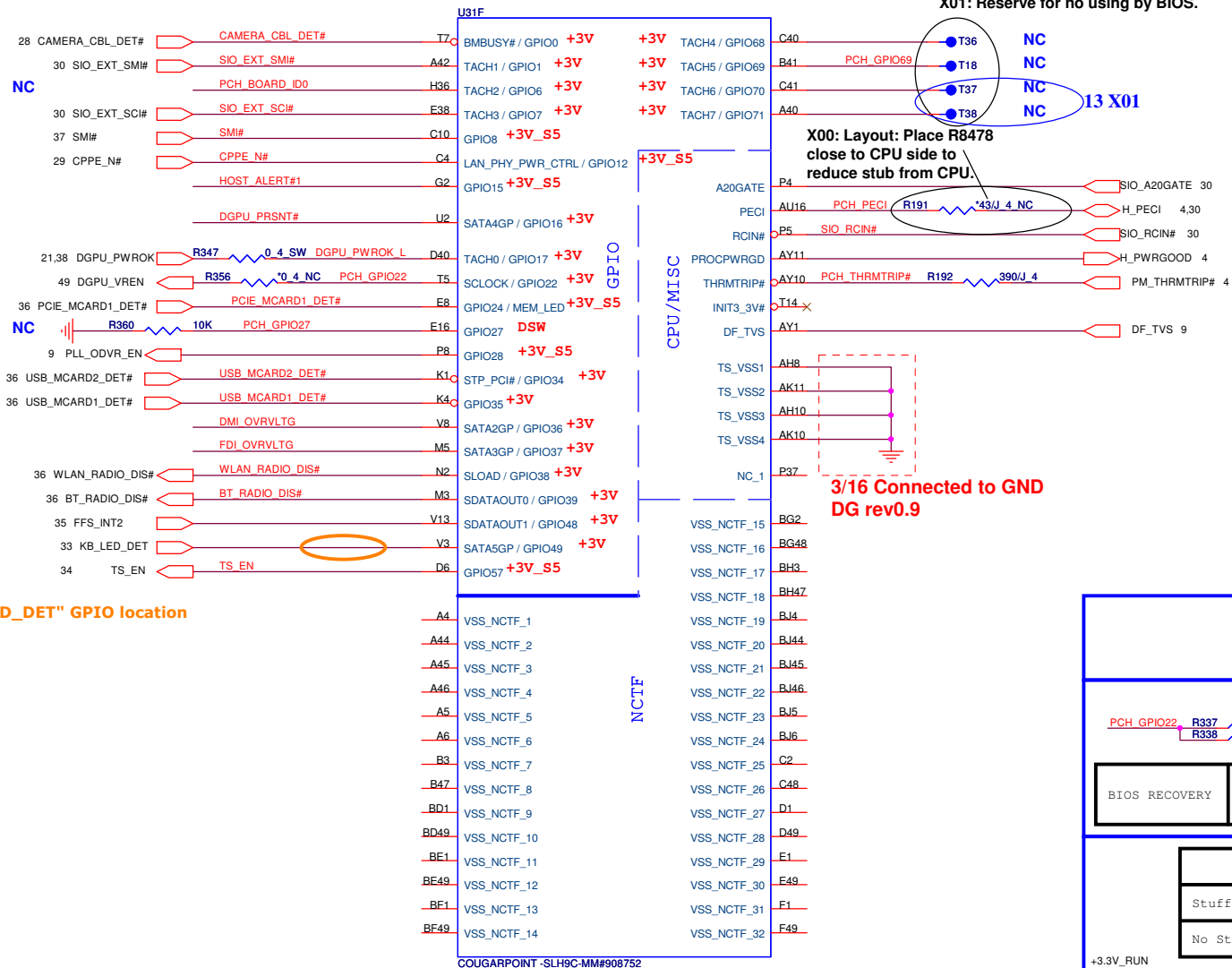
Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN  4 NC SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	 4 NC PCI_GNT3# 10									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL  4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>SPI *</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]  4 NC BBS_BIT1 10  4 NC BBS_BIT0
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3.3V_RUN  4 NC ACZ_SDOOUT_R									
DF_TVS	DMI/FDI Termination voltage	PWROK	For Sandy Bridge processor only: DF_TVS needs to be pulled up to VccdFTErm powerall through 2.2 K ohm resistor.	+1.8V_RUN  IDF_TVS									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	 4 NC PLL_OVDV_R									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3.3V_SUS  4 ACZ_SYNC_R									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	Need check schematic									
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)										

3/16 Remove based on CPT EDS rev1.0



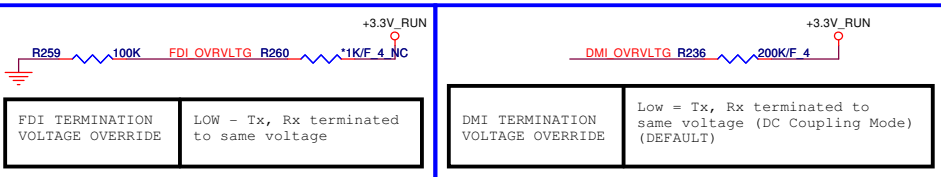
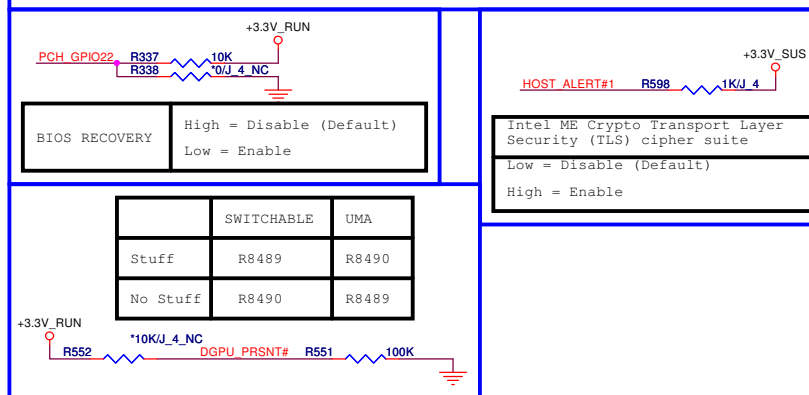
X01: Reserve for no using by BIOS.

11



X02-03
Change "KB_LED_DET" GPIO location

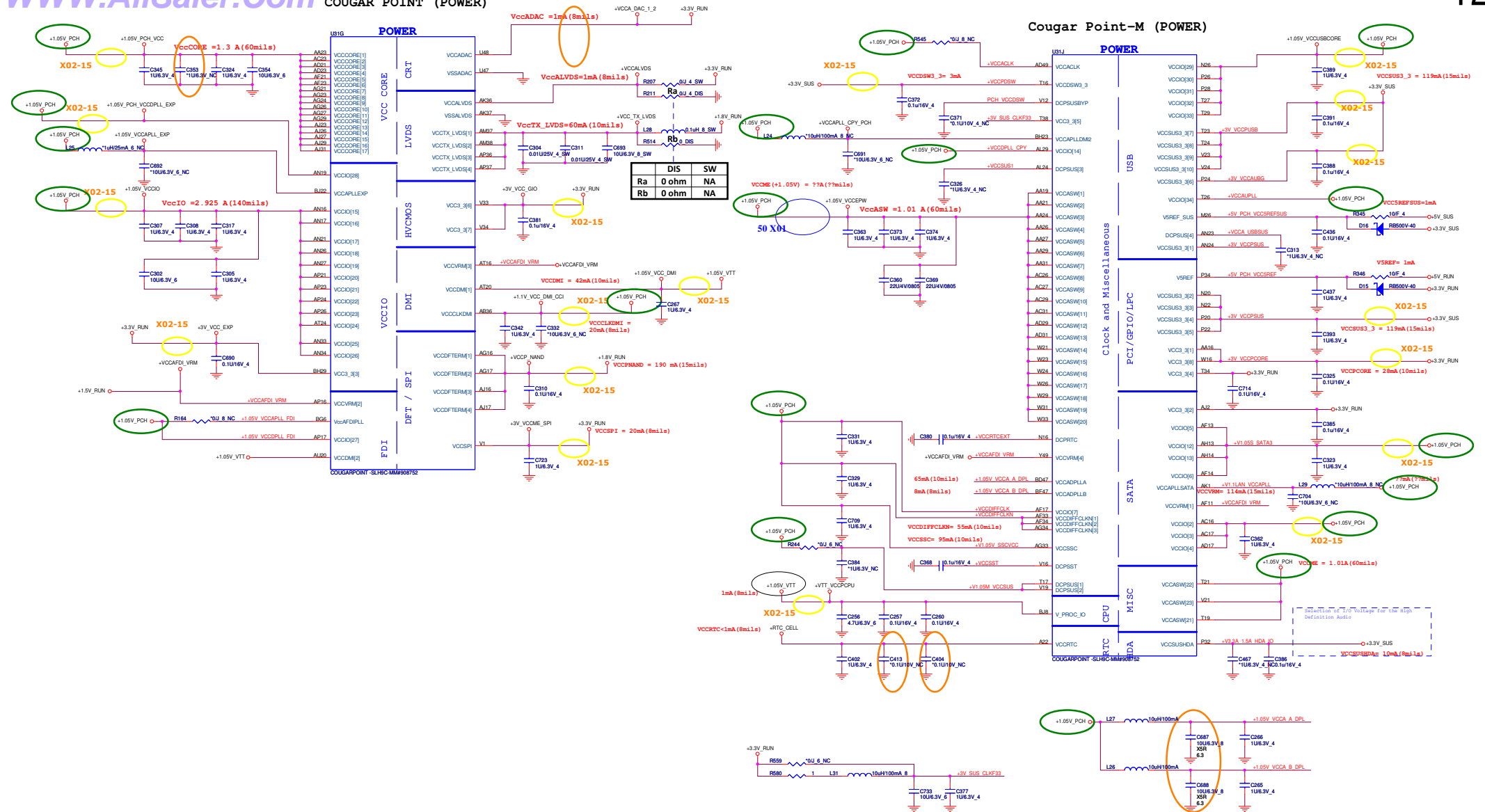
02/20 DEL for Pre-ES1



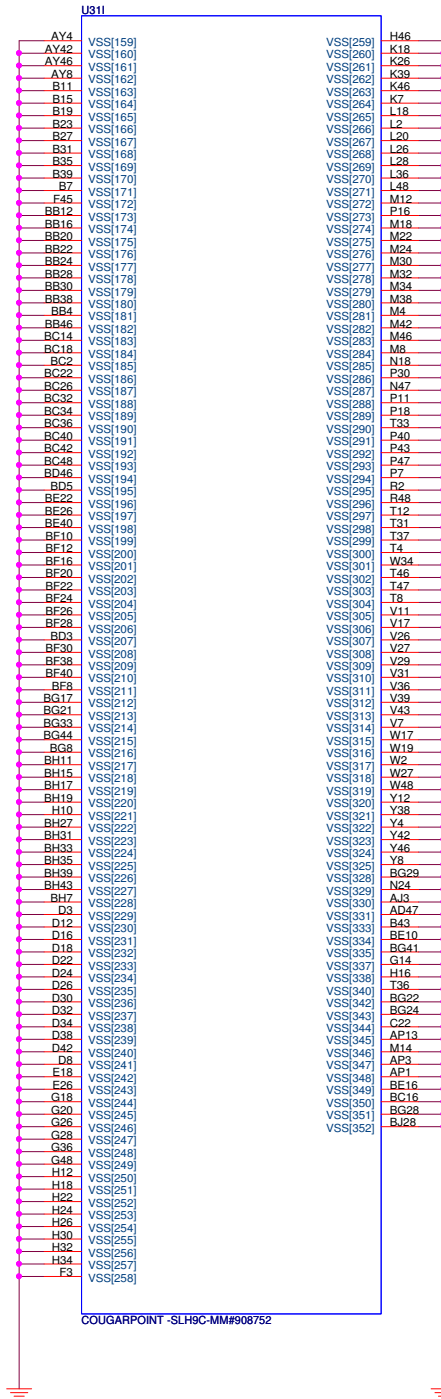
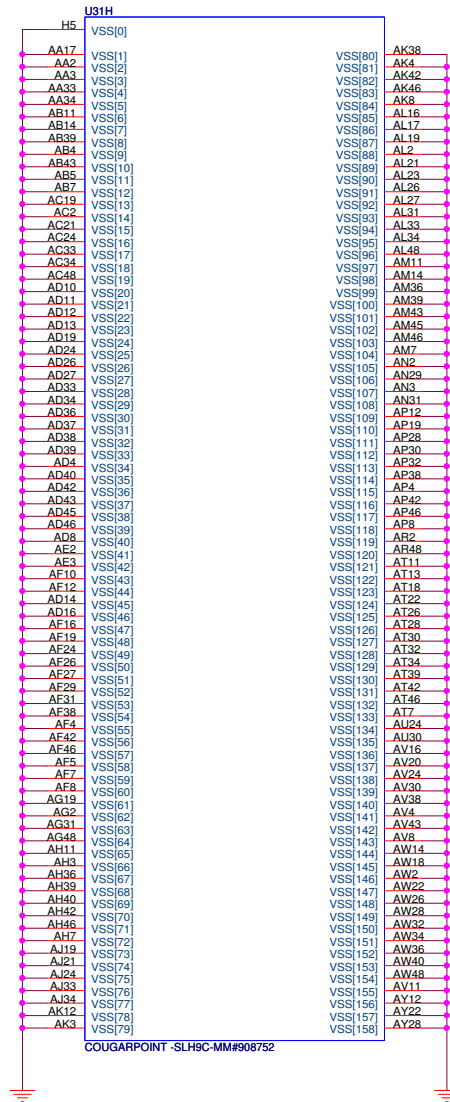
Quanta Computer Inc.

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Title	PCH 4/6(GPIO/CPU)		
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IBEX PEAK-M (GND)



Quanta Computer Inc.
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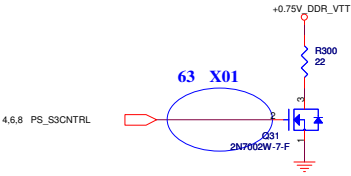
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Size: Document Number GM7C_MB Rev C

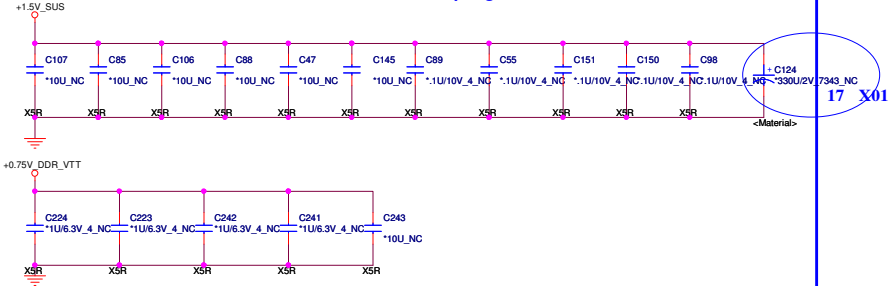
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67 X01

S3 Power Reduce (Discharge)



SODIMM# A0 Decoupling



Quanta Computer Inc.

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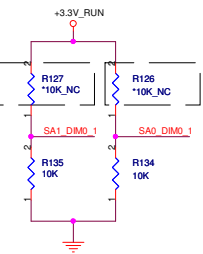
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Size Document Number GM7C_MB

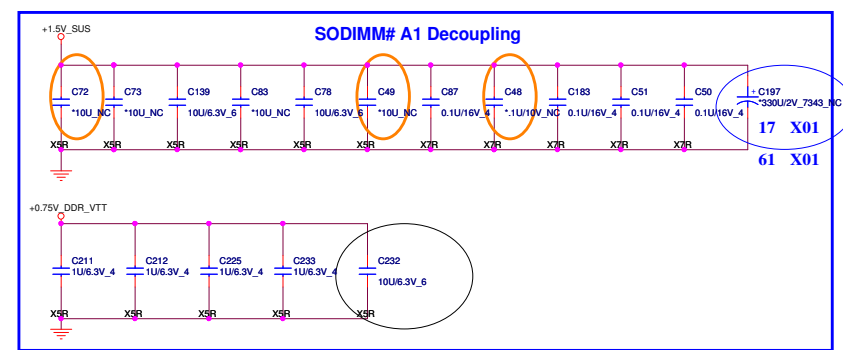
Rev B

Date: Friday, January 21, 2011

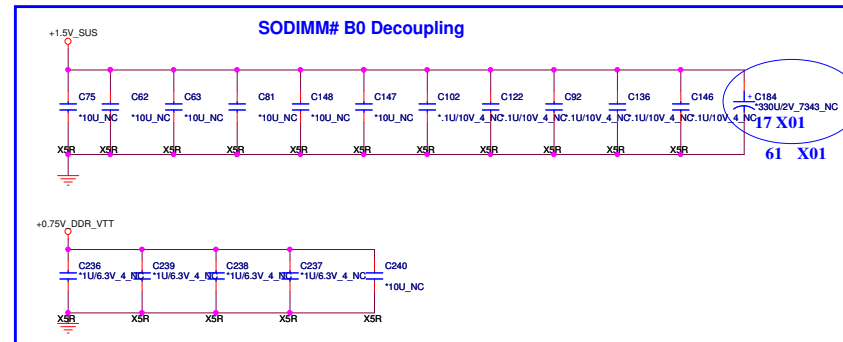
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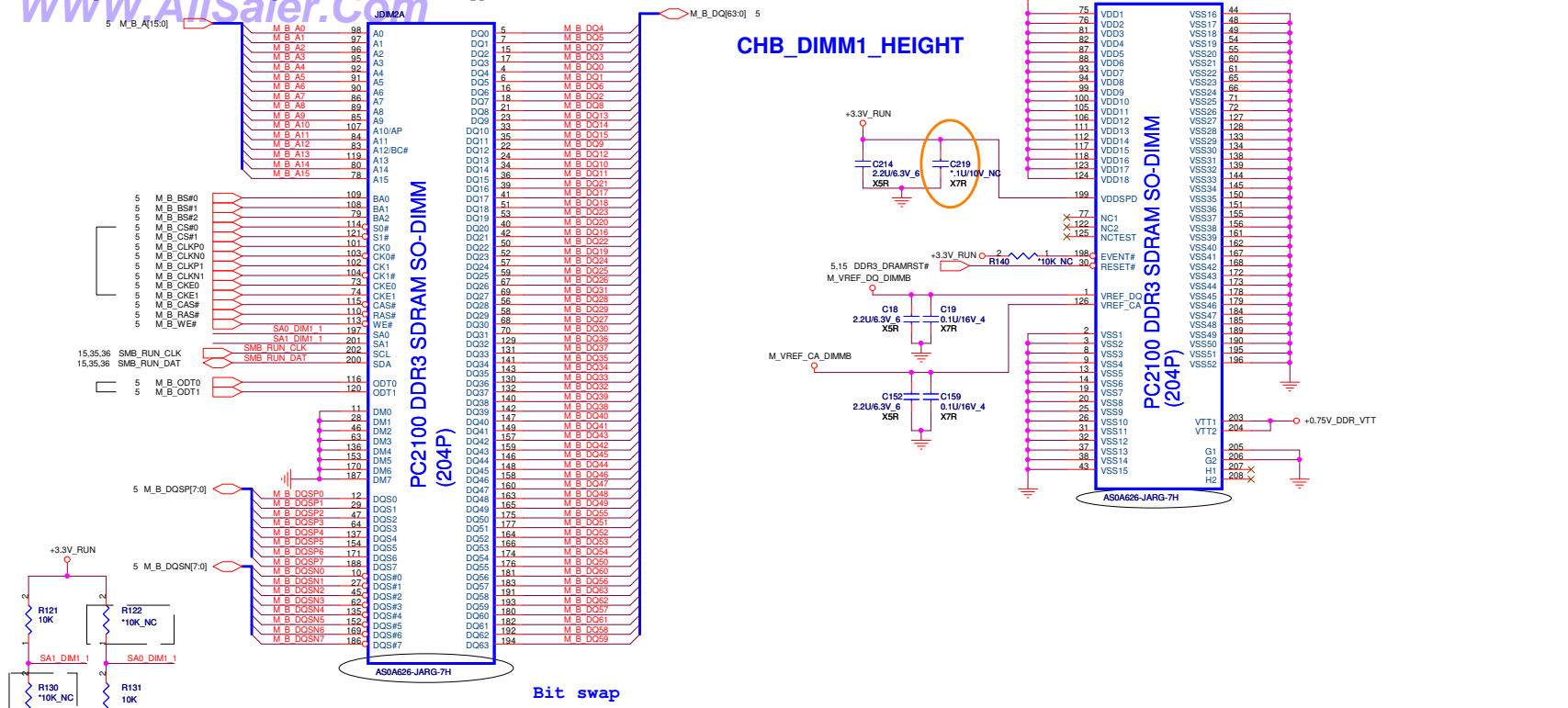


Note:
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



67 X01

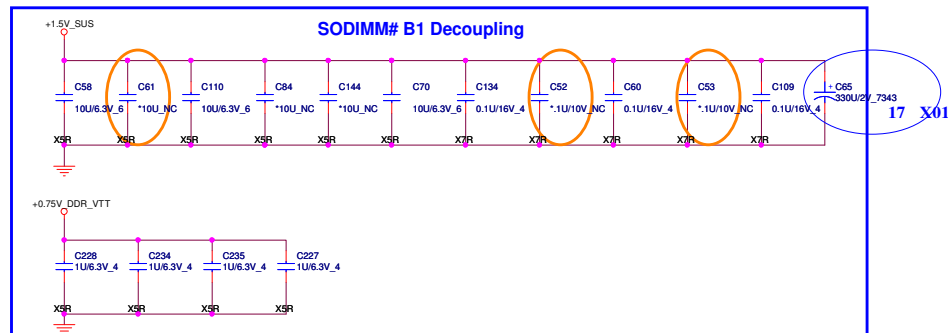




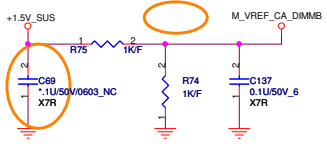
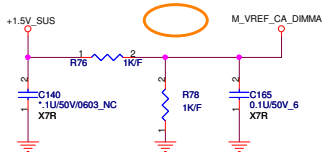
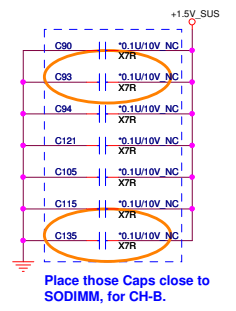
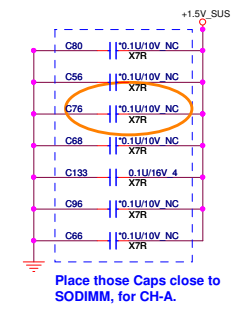
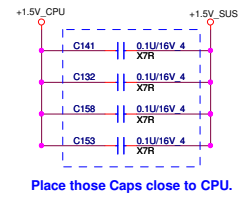
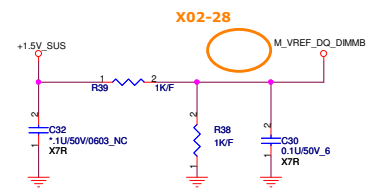
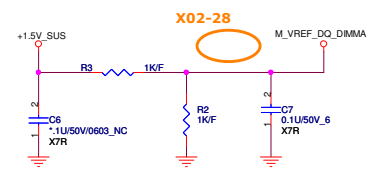
8 X01
0413>Add_DIS for SODIMM

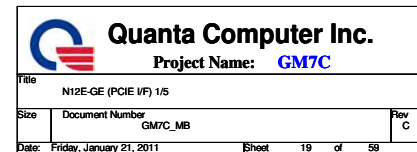
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

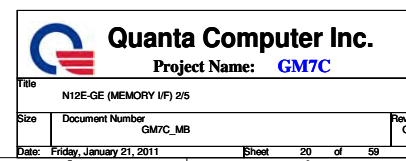
Note:
SO-DIMMA SPD Address is 0xA6
SO-DIMMA TS Address is 0x36



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Title	DDR3 DIMM-B1	
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27 FBC_D[63..0]
27 FBC_DOM[7..0]
27 FBC_DOSP[7..0]
27 FBC_DOSN[7..0]

U34D
lcbn1328-nvidia-n11e
COMMON

420 FBC
FBC_D0 M6 FBC_D0
FBC_D1 M4 FBC_D1
FBC_D2 M7 FBC_D2
FBC_D3 M5 FBC_D3
FBC_D4 K5 FBC_D4
FBC_D5 L6 FBC_D5
FBC_D6 L7 FBC_D6
FBC_D7 K7 FBC_D7
FBC_D8 P4 FBC_D8
FBC_D9 FBC_D9
FBC_D10 R4 FBC_D10
FBC_D11 R5 FBC_D11
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FBC_D14 U4 FBC_D14
FBC_D15 T6 FBC_D15
FBC_D16 U3 FBC_D16
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FBC_D19 T2 FBC_D19
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FBC_D58 C9 FBC_D58
FBC_D59 A9 FBC_D59
FBC_D60 C12 FBC_D60
FBC_D61 B12 FBC_D61
FBC_D62 C13 FBC_D62
FBC_D63 A12 FBC_D63

COMMAND BUS
REFERENCE

GND_REF
GND_REF

FBC_CMD0 H5 FBC_CMD0
FBC_CMD1 G1N FBC_CMD1
FBC_CMD2 G5 FBC_CMD2
FBC_CMD3 F4 FBC_CMD3
FBC_CMD4 G2 FBC_CMD4
FBC_CMD5 G1 FBC_CMD5
FBC_CMD6 G3 FBC_CMD6
FBC_CMD7 E1 FBC_CMD7
FBC_CMD8 J5 FBC_CMD8
FBC_CMD9 E3 FBC_CMD9
FBC_CMD10 H6 FBC_CMD10
FBC_CMD11 C2 FBC_CMD11
FBC_CMD12 F3 FBC_CMD12
FBC_CMD13 E2 FBC_CMD13
FBC_CMD14 D1 FBC_CMD14
FBC_CMD15 D2 FBC_CMD15
FBC_CMD16 E8 FBC_CMD16
FBC_CMD17 D2N FBC_CMD17
FBC_CMD18 E7 FBC_CMD18
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FBC_CMD22 C7 FBC_CMD22
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FBC_CMD24 E9 FBC_CMD24
FBC_CMD25 C5 FBC_CMD25
FBC_CMD26 F8 FBC_CMD26
FBC_CMD27 B3 FBC_CMD27
FBC_CMD28 C6 FBC_CMD28
FBC_CMD29 B5 FBC_CMD29
FBC_CMD30 A4 FBC_CMD30
FBC_CMD31 S4 FBC_CMD31

FBC_CMD0
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FBC_CMD2
FBC_CMD3
FBC_CMD4
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FBC_CMD29
FBC_CMD30
FBC_CMD31

FBC_DOM0 K4 FBC_DOM0
FBC_DOM1 R7 FBC_DOM1
FBC_DOM2 T3 FBC_DOM2
FBC_DOM3 L3 FBC_DOM3
FBC_DOM4 D10 FBC_DOM4
FBC_DOM5 G15 FBC_DOM5
FBC_DOM6 C16 FBC_DOM6
FBC_DOM7 C11 FBC_DOM7

FBC_DOSP0 L4 FBC_DOSP0
FBC_DOSP1 U7 FBC_DOSP1
FBC_DOSP2 R1 FBC_DOSP2
FBC_DOSP3 K1 FBC_DOSP3
FBC_DOSP4 D11 FBC_DOSP4
FBC_DOSP5 G17 FBC_DOSP5
FBC_DOSP6 A15 FBC_DOSP6
FBC_DOSP7 B10 FBC_DOSP7

FBC_DOSN0 M4 FBC_DOSN0
FBC_DOSN1 T7 FBC_DOSN1
FBC_DOSN2 R2 FBC_DOSN2
FBC_DOSN3 K2 FBC_DOSN3
FBC_DOSN4 D12 FBC_DOSN4
FBC_DOSN5 G16 FBC_DOSN5
FBC_DOSN6 B15 FBC_DOSN6
FBC_DOSN7 A10 FBC_DOSN7

FBC_DEBUG0 J6 R252 60.4 1%
FBC_DEBUG1 F9 R247 60.4 1%

FBC_CLK0 H3 FBC_CLK0 27
FBC_CLK0 H4 FBC_CLK0 27
FBC_CLK1 C8 FBC_CLK1 27
FBC_CLK1 D8 FBC_CLK1# 27

FBC_WCK01 P7 FBC_WCK01
FBC_WCK01 N7 FBC_WCK01
FBC_WCK23 N5 FBC_WCK23
FBC_WCK23 N6 FBC_WCK23
FBC_WCK45 G14 FBC_WCK45
FBC_WCK45 G13 FBC_WCK45
FBC_WCK87 E13 FBC_WCK87
FBC_WCK87 F13 FBC_WCK87

FBC_PLL_AVDD H8 FBA_PLLAVDD 20

Remove test pad for
VRAM power shape.

C420 0.1u/16V_4

+1.5V_GFX

U34E
lcbn1328-nvidia-n11e
COMMON

1600 FBVDDQ
A2 FBVDDQ H22
A3 FBVDDQ H24
AA38 FBVDDQ H25
AB35 FBVDDQ H26
AC38 FBVDDQ H27
AD35 FBVDDQ H28
AD41 FBVDDQ H29
AE35 FBVDDQ H31
AE35 FBVDDQ H32
AE35 FBVDDQ H33
AE38 FBVDDQ H34
AG35 FBVDDQ H7
AG38 FBVDDQ H9
AK35 FBVDDQ H35
AL35 FBVDDQ J4
B1 FBVDDQ J7
B2 FBVDDQ J8
B2 FBVDDQ J35
B29 FBVDDQ K8
B33 FBVDDQ M35
B6 FBVDDQ M8
C1 FBVDDQ N35
C4 FBVDDQ N8
D26 FBVDDQ R35
D33 FBVDDQ R8
D4 FBVDDQ T35
D5 FBVDDQ T8
D9 FBVDDQ U35
E32 FBVDDQ V35
E4 FBVDDQ V38
E8 FBVDDQ W35
E2 FBVDDQ Y35
F5 FBVDDQ H21
F7 FBVDDQ Y41
G19 FBVDDQ
G30 FBVDDQ
G6 FBVDDQ
G8 FBVDDQ
G9 FBVDDQ
H10 FBVDDQ
H12 FBVDDQ
H13 FBVDDQ
H15 FBVDDQ
H16 FBVDDQ
H18 FBVDDQ
H19 FBVDDQ

FBVDDQ_PROBE V8

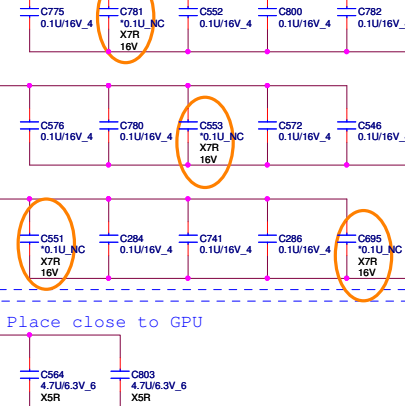
FB_CAL_PD_VDDQ V6

FB_CAL_PU_GND V7

FB_CALTERM_GND V4

GPU FBVDDQ Decoupling

Place close to GPU balls



Place close to GPU

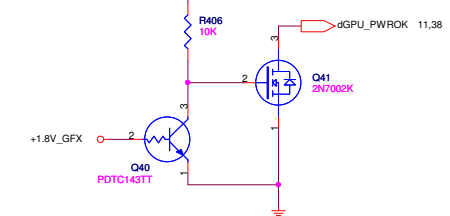
+1.5V_GFX

FB_CAL_PD_VDDQ R257 40.2 1%

FB_CAL_PU_GND R242 40.2 1%

FB_CALTERM_GND R258 60.4 1%

GPU all PWROK

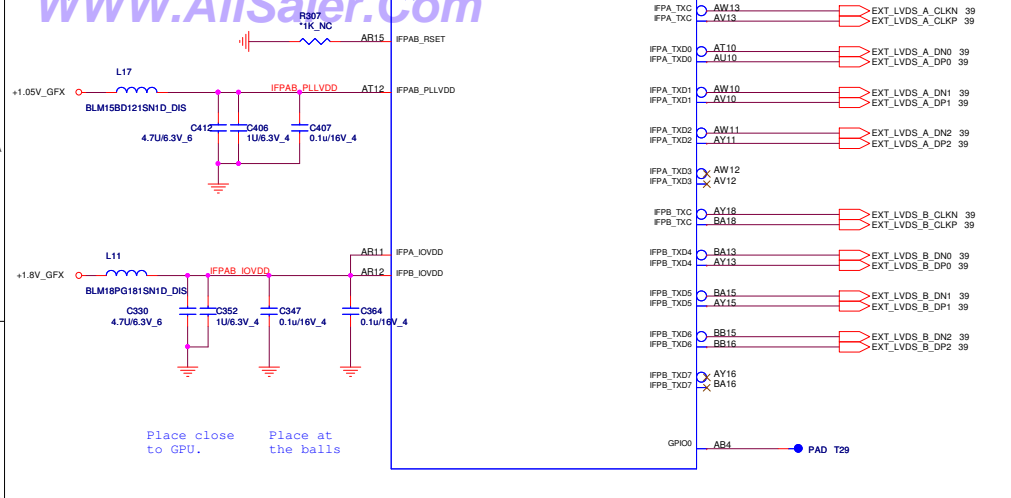


Quanta Computer Inc.

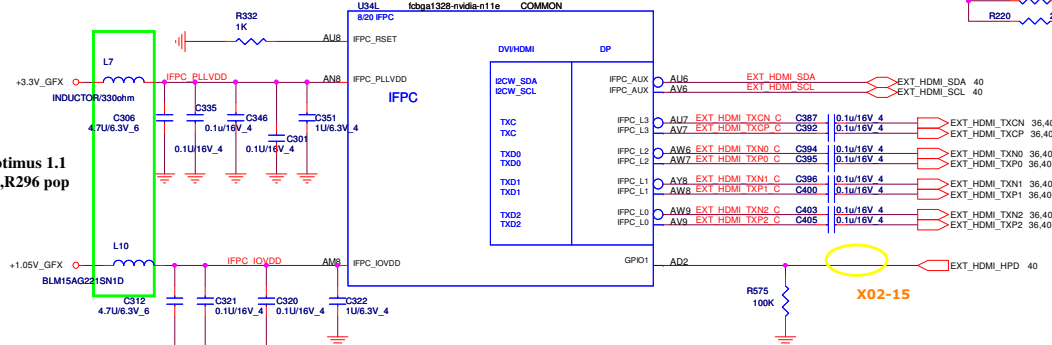
Project Name: GM7C

Title	N12E-GE (MEMORY I/F) 3/5		
Size	Document Number	GM7C_MB	Rev C
Date	Friday, January 21, 2011	Sheet 21 of 59	

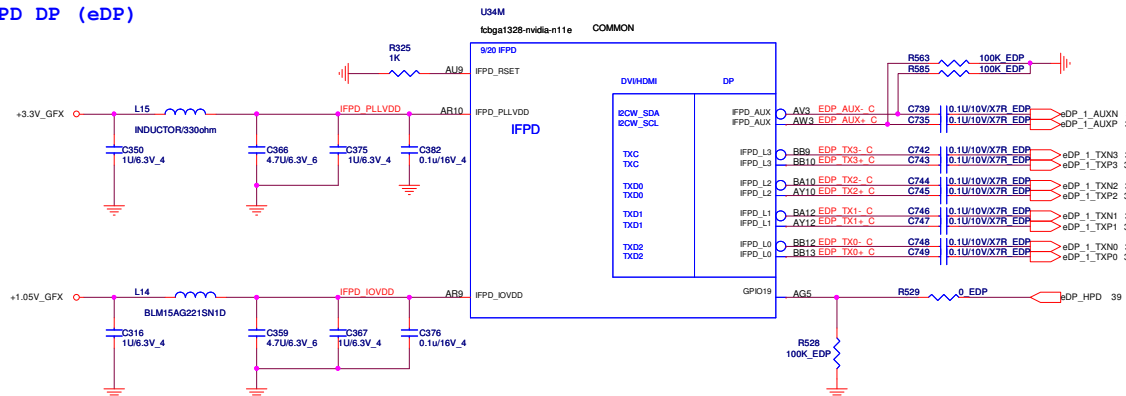
IFPA/B LVDS Dual Link



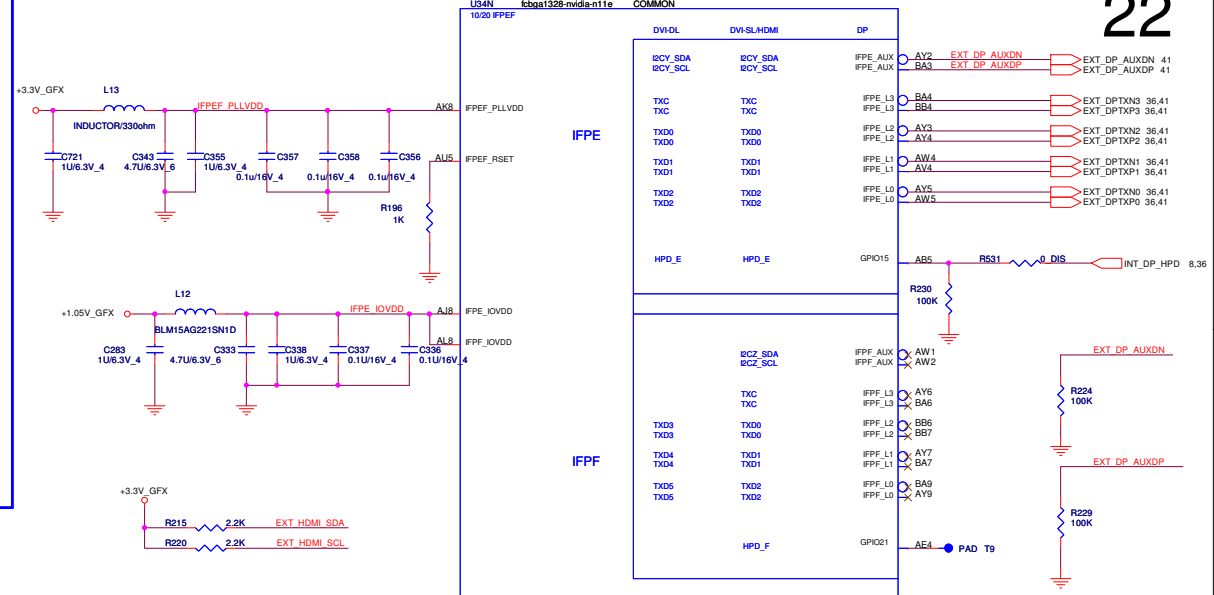
IFPC HDMI

For Optimus I.1
L9,L12,R296 pop

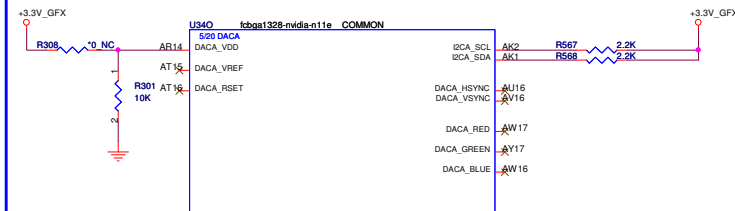
IFPD DP (eDP)



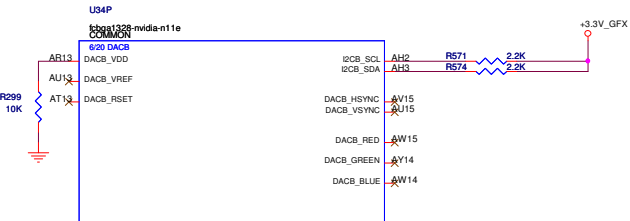
IFPE/F TMDs DVI-I

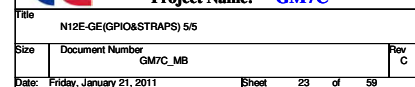


DAC_A VGA



DAC_B Header







Project Name: GM7C

Size	Document Number
------	-----------------

GM7C_ME

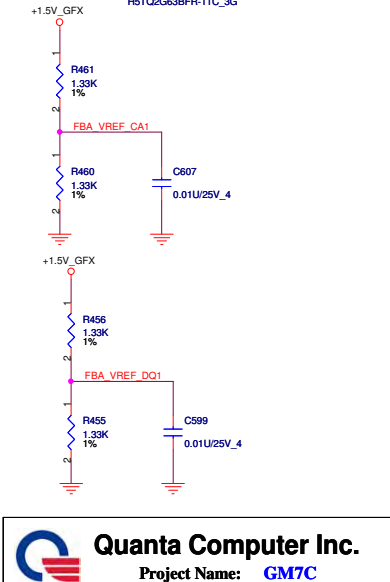
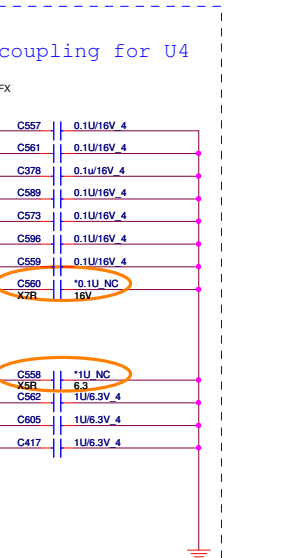
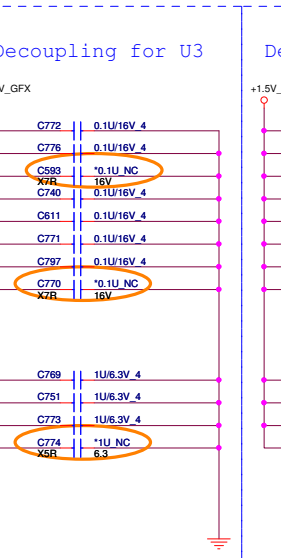
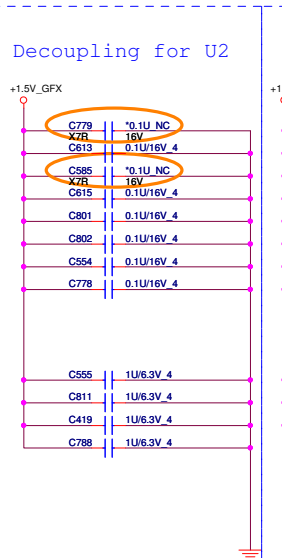
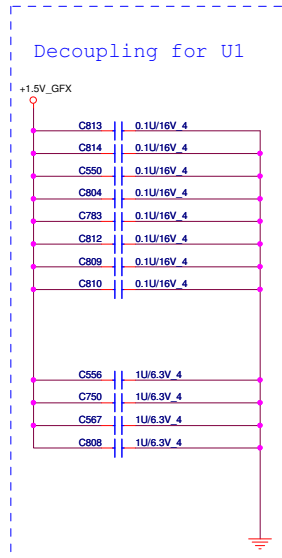
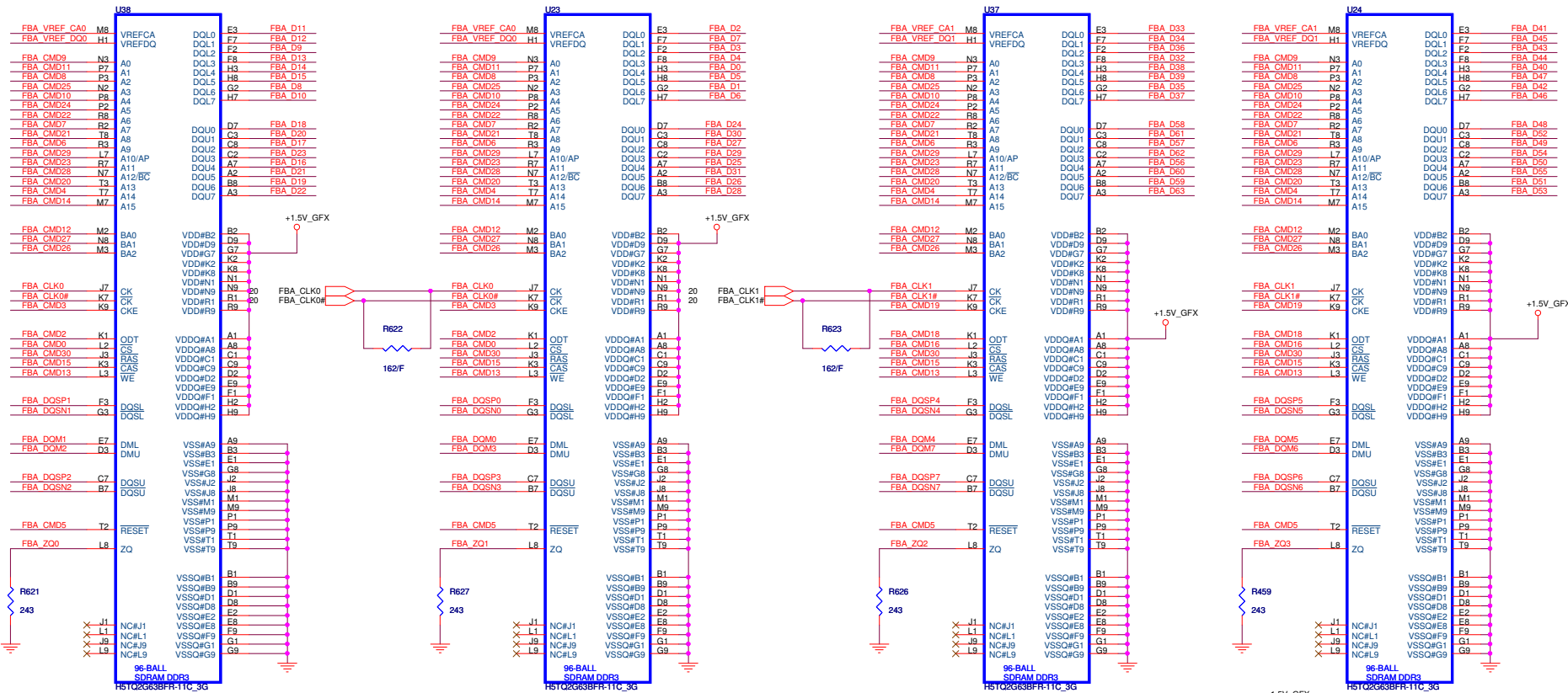
Date: Friday, January 21, 2011

Sheet 24 of 59

Memory Lower Partition A

Memory Upper Partition A

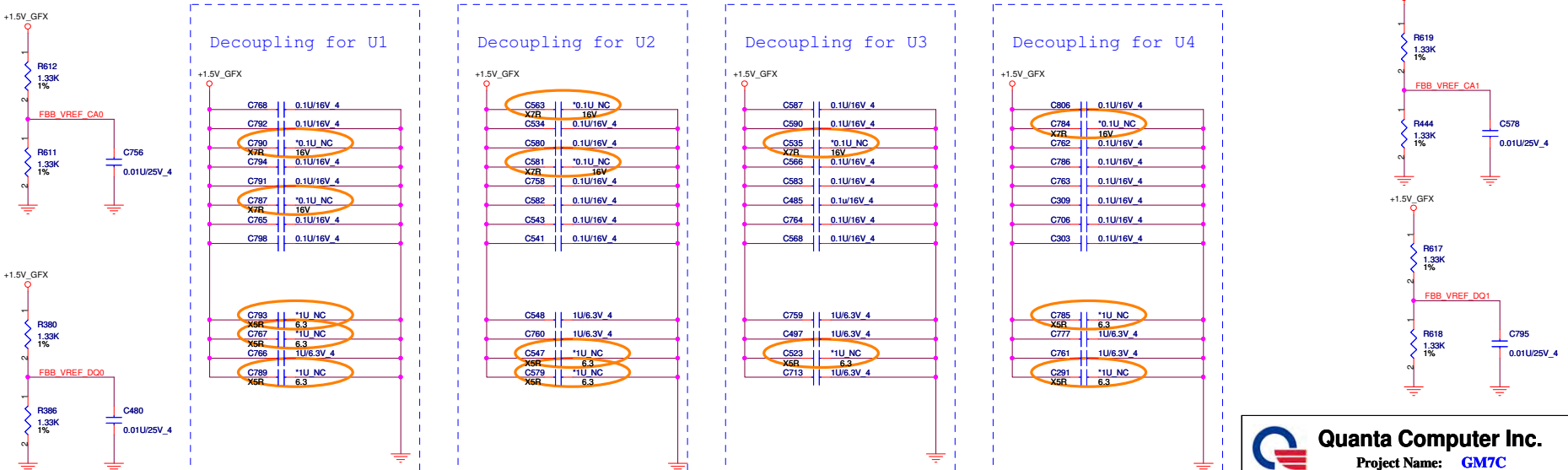
25

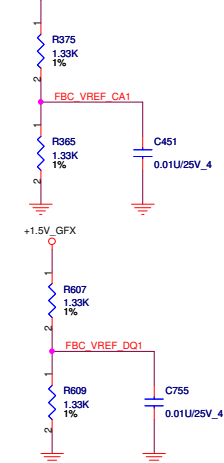
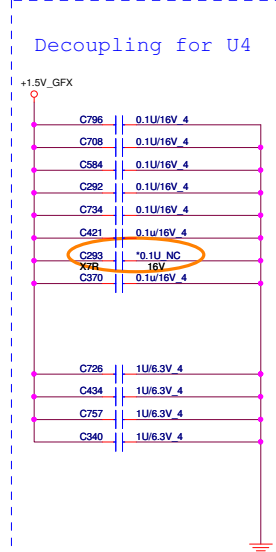
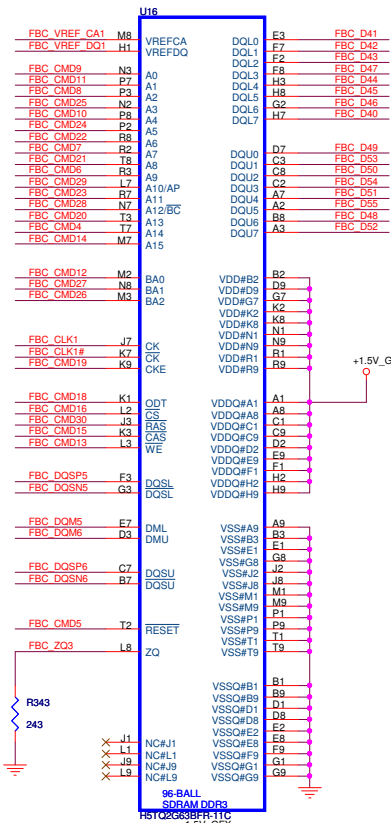


For 128 bit, Partition A don't need to mount

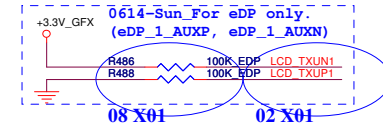
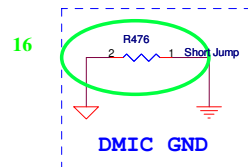
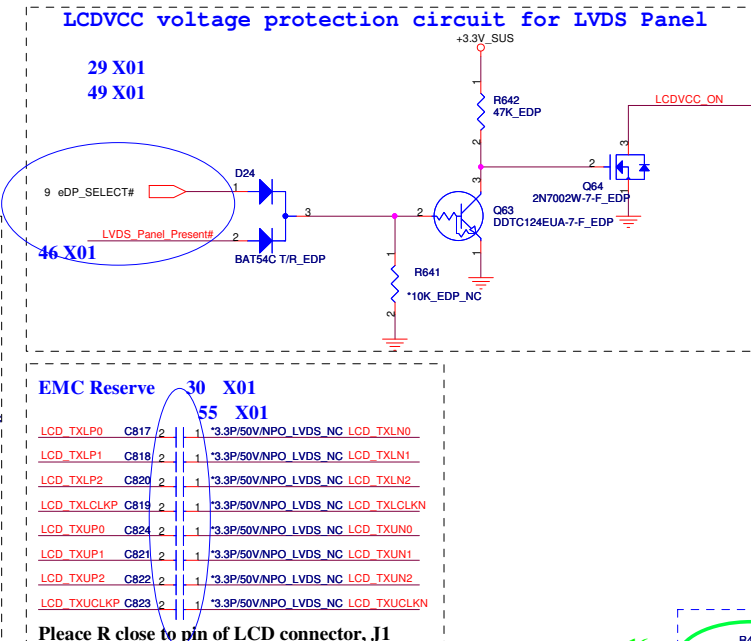
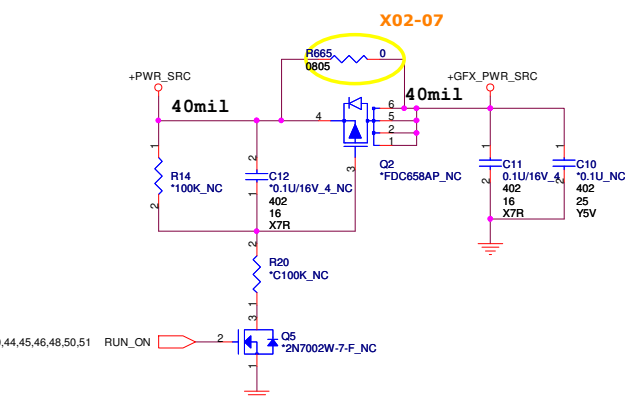
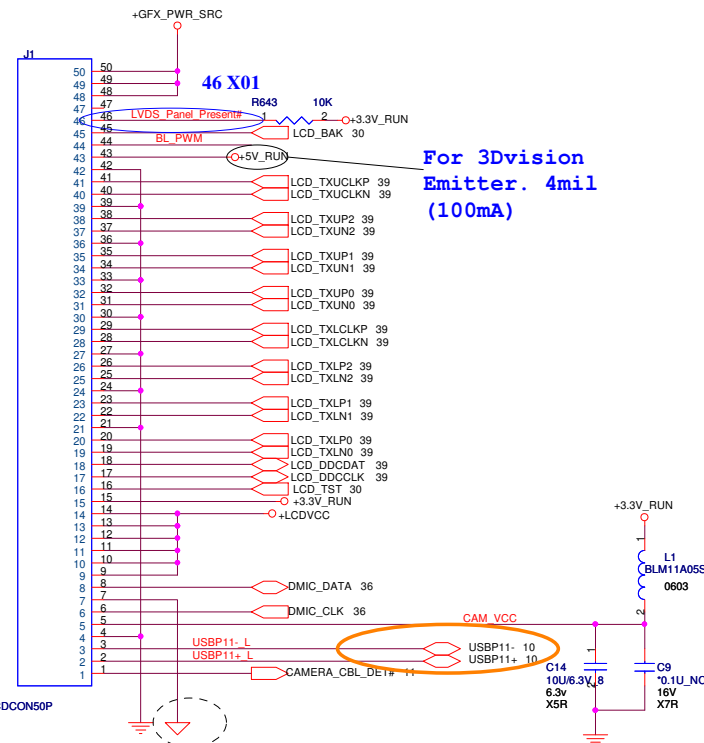
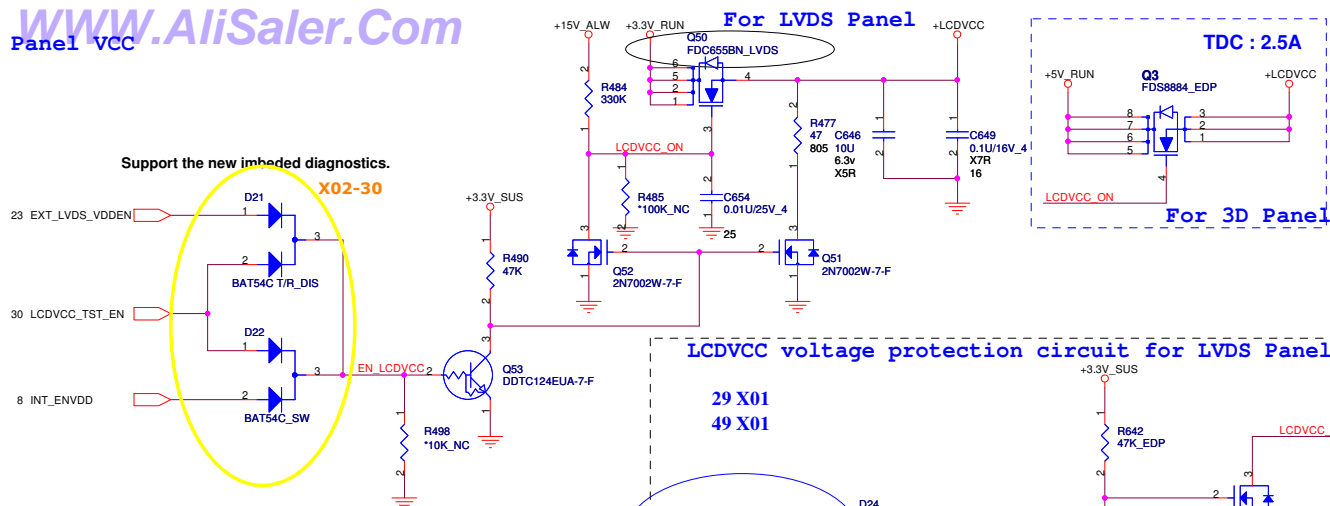
WWW.AliSaler.Com

Decoupling for U4

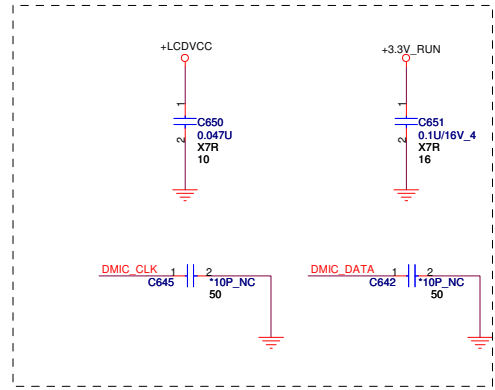
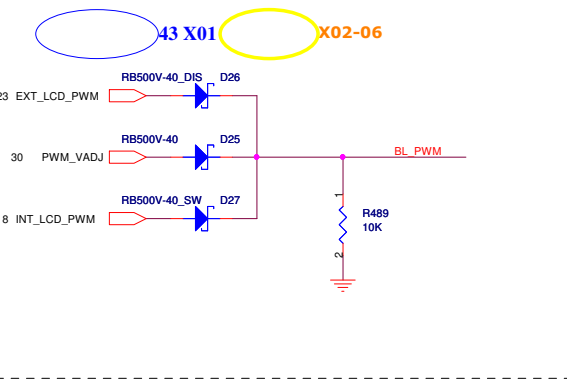





50Pin LVDS & Array Microphone & Camera Connector

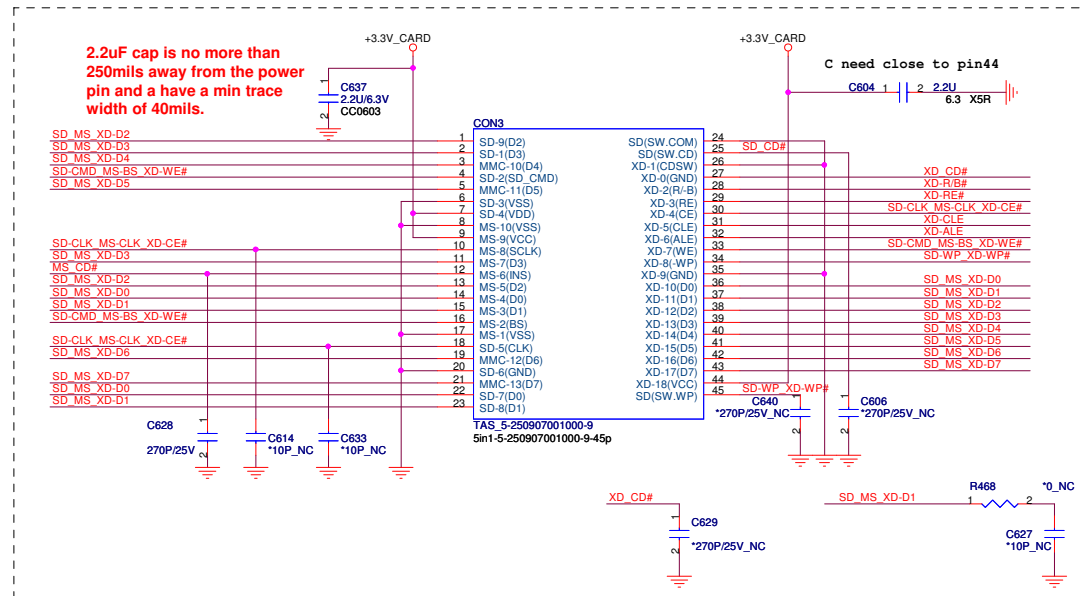
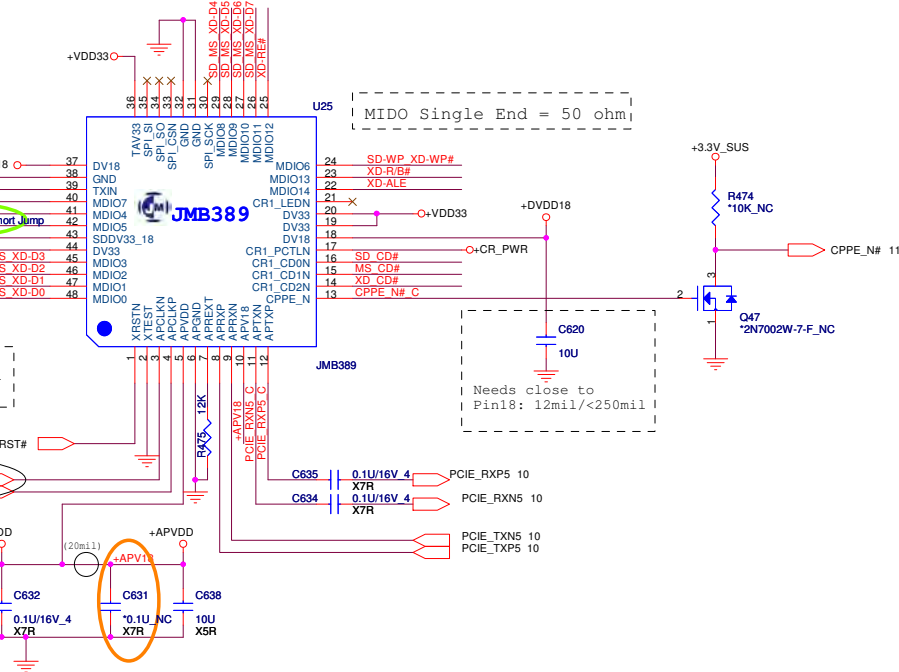
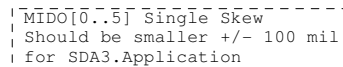
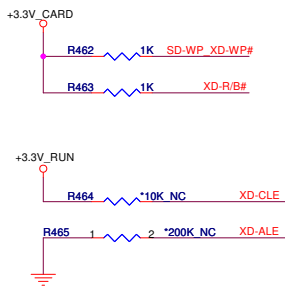
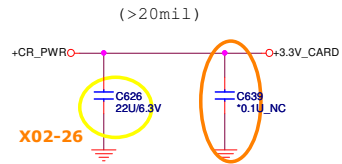
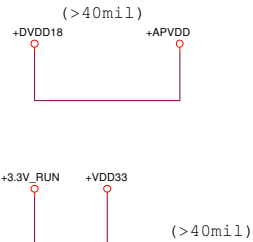


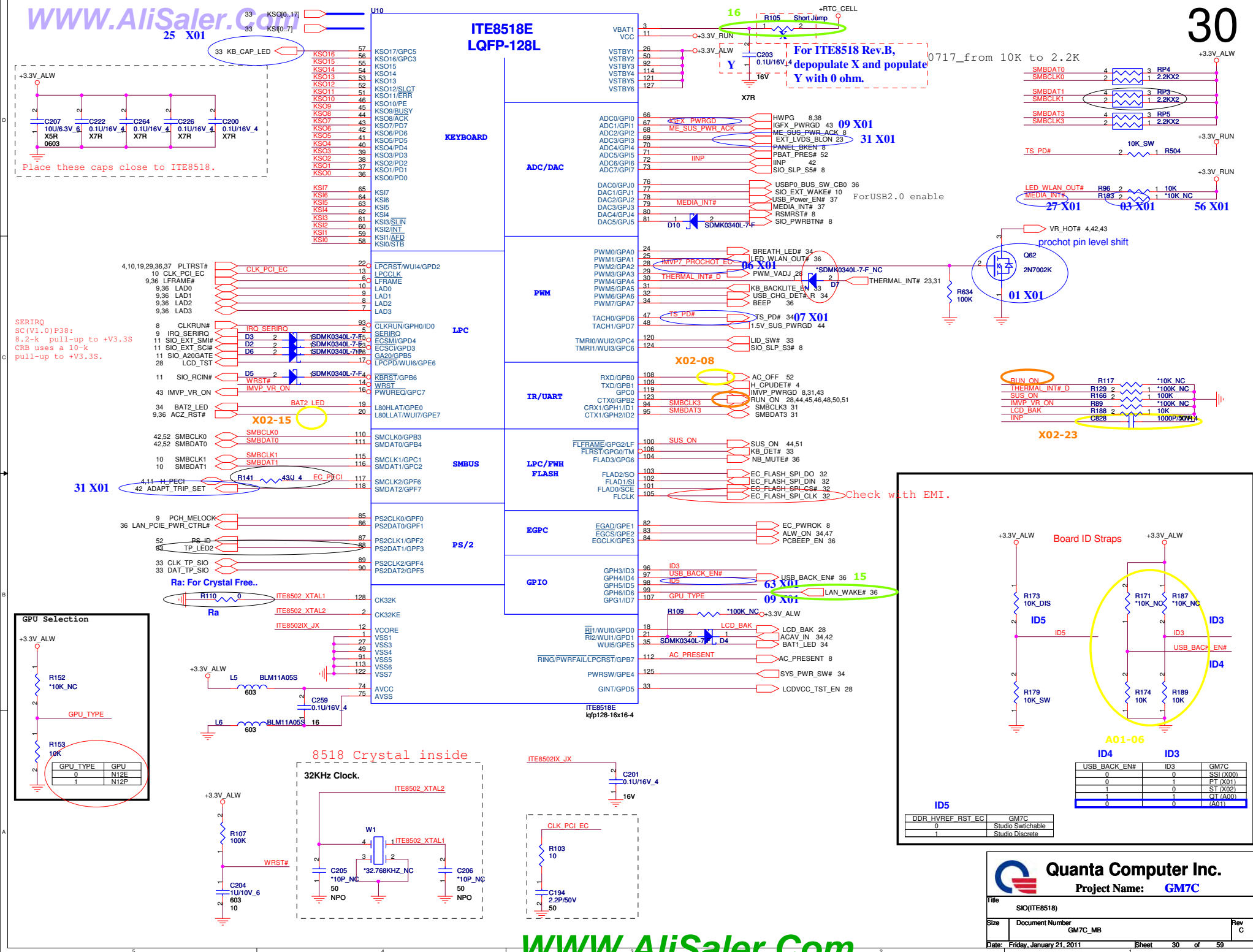
Backlight Control



 Quanta Computer Inc. Project Name: GM7C	
Title: LCD CONN	
Size: Document Number	GM7C_MB
Date: Friday, January 21, 2011	Sheet 28 of 59

Pin	Default	SD	M0C	MS	XD
M01000	SD/MC/MS/SD	SD	MS	MS_D0	XD_D0
M01001	SD_D1	MS_D1	MS	D1	XD_D1
M01002	SD_D2	MS_D2	MS	D2	XD_D2
M01003	SD_D3	MS_D3	MS	D3	XD_D3
M01004	SD_CMD	MS_B5	MS	XD_WE#	
M01005	SD_CLK	MS_CLK	MS	XD_CE#	
M01006	SD_WF	MS_WF	MS	XD_WF	
M01007				XD_CLE	
M01008	M0C_D4	MS_D4	MS	XD_D4	
M01009	M0C_D5	MS_D5	MS	XD_D5	
M01010	M0C_D6	MS_D6	MS	XD_D6	
M01011	M0C_D7	MS_D7	MS	XD_D7	
M01012				XD_RE#	
M01013				XD_R/B	
M01014				XD_ALE	
CR1_LEDN	SD_LED#	MS_LED#	MS	XD_LED#	
CR1_PCTLN	SD_PWR#	MS_PWR#	MS	XD_PWR#	
CR1_CD	SD_CD#				
CR1_C2D		MS_CD#			
CR1_C02				XD_CD#	

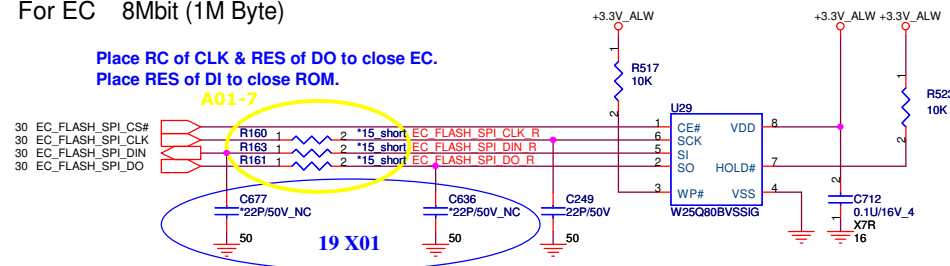






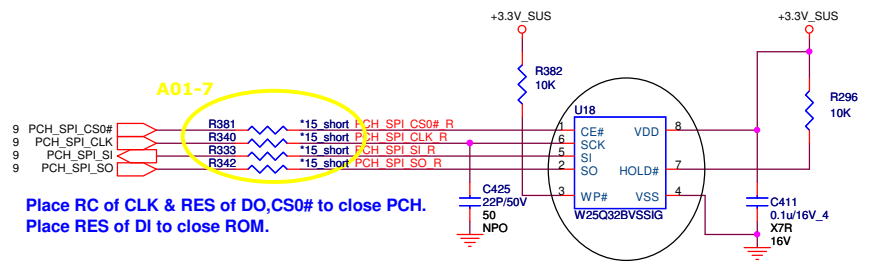
For EC 8Mbit (1M Byte)

Place RC of CLK & RES of DO to close EC.
Place RES of DI to close ROM.



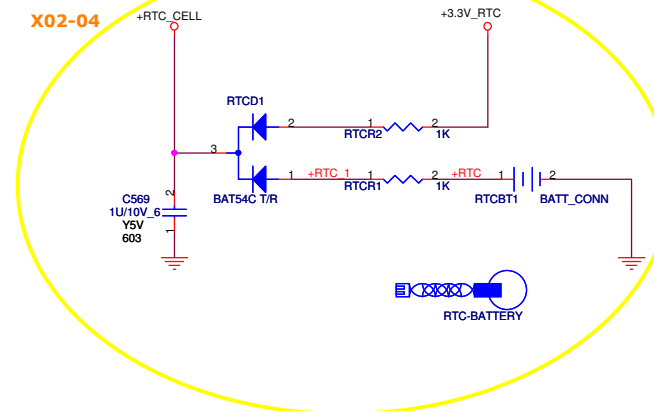
For PCH 32Mbit (4M Byte)

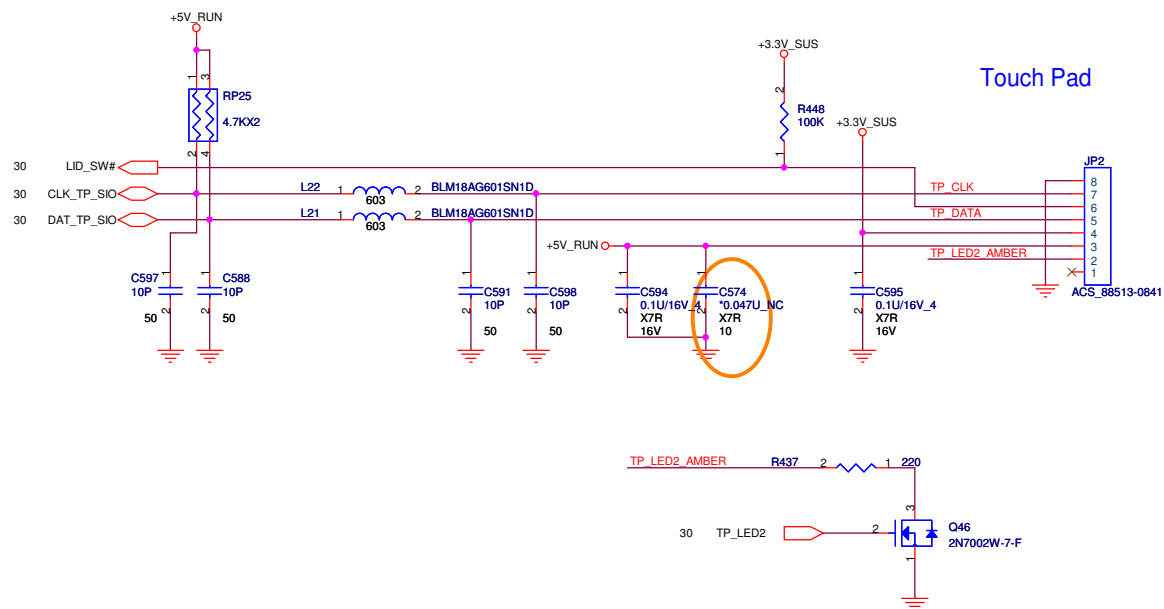
Place RC of CLK & RES of DO,CS0# to close PCH.
Place RES of DI to close ROM.



RTC BATTERY

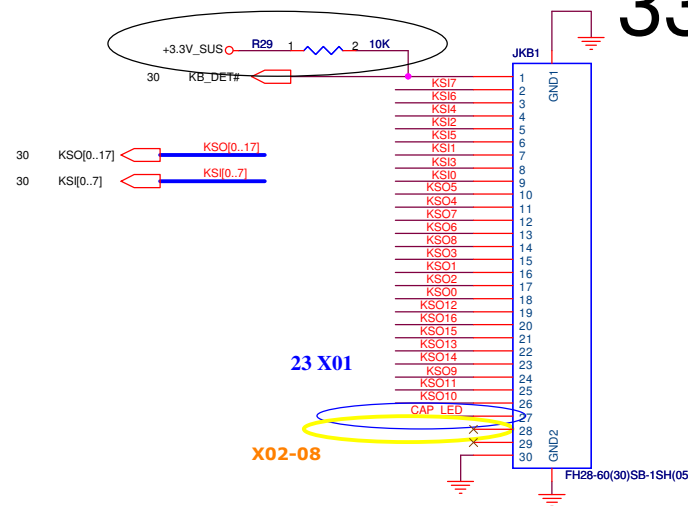
X02-04





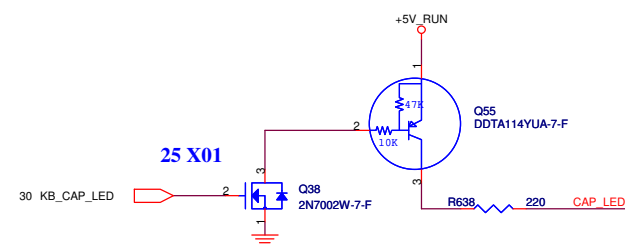
KEYBOARD CONNECTOR

33



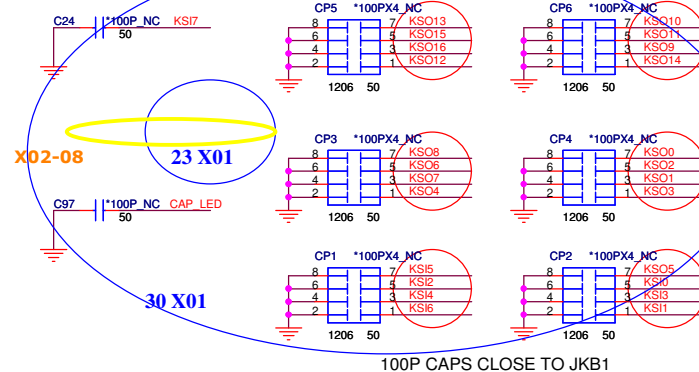
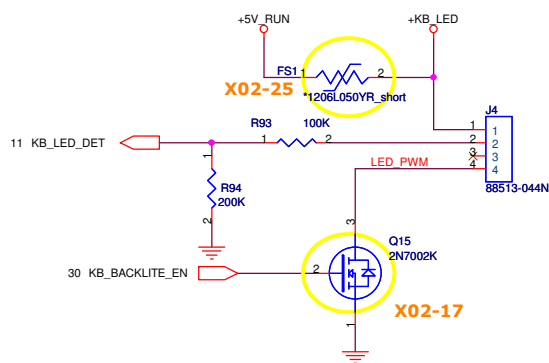
Cap_Lock WLED for GM7C.

23 X01

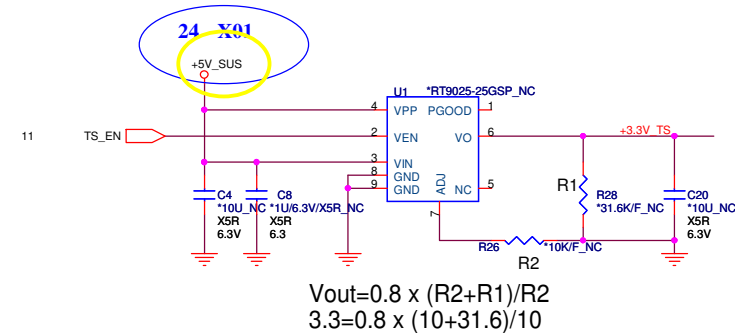
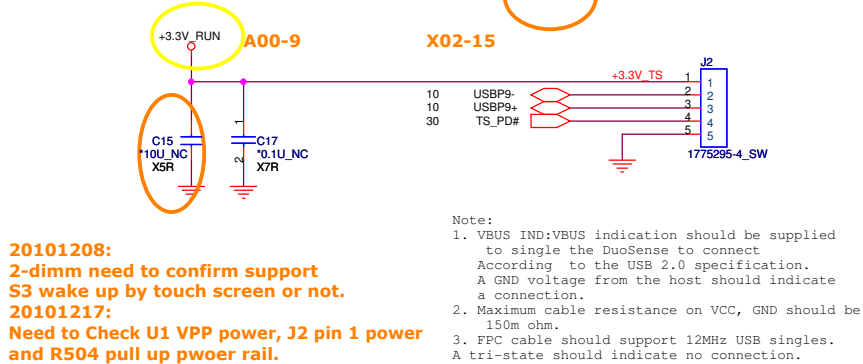


Key board illumination

+KB_LED power trace width >10 mil

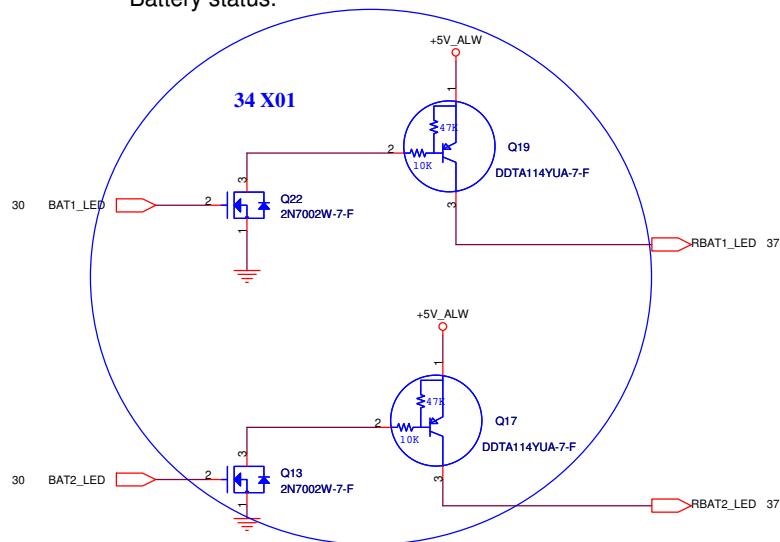


Quanta Computer Inc. Project Name: GM7C		
Title	TP / KB	
Size	Document Number GM7C_MB	Rev C
Date:	Friday, January 21, 2011	Sheet 33 of 59

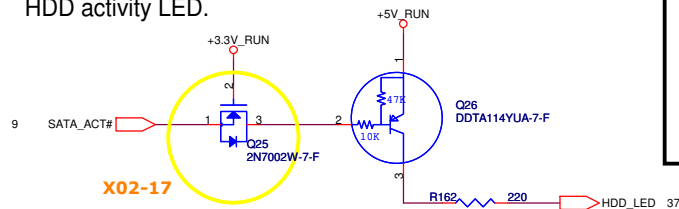


LED

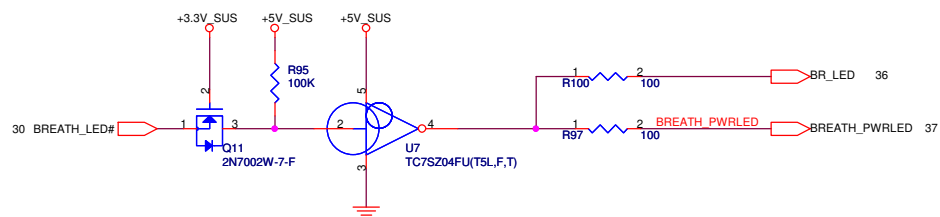
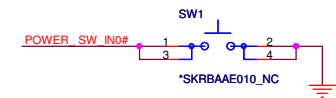
Battery status.



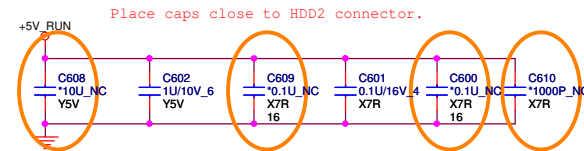
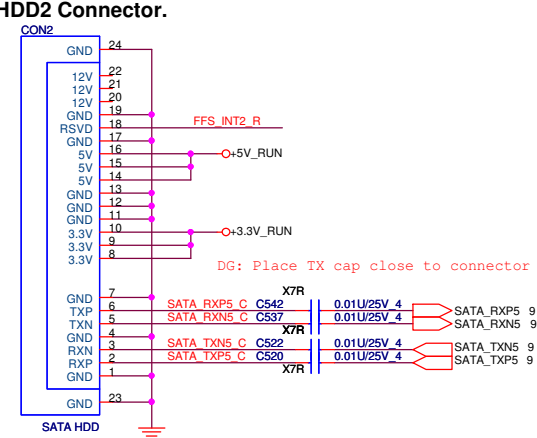
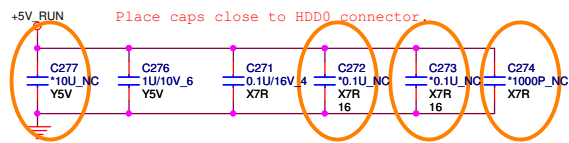
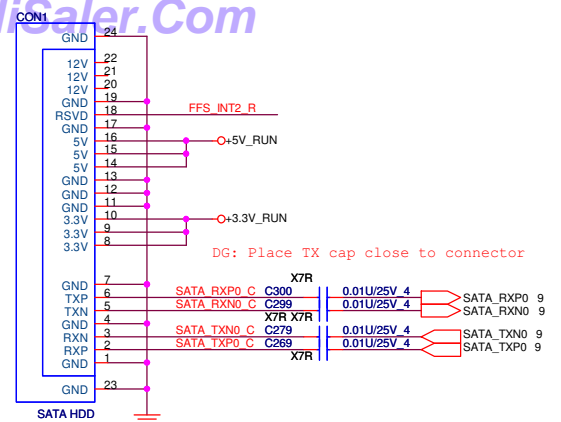
HDD activity LED.



Power button for Engineer



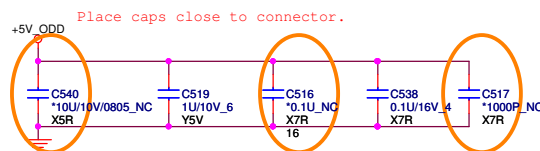
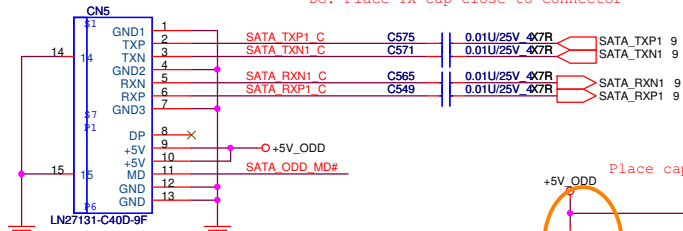
Quanta Computer Inc. Project Name: GM7C		
Title	SWITCH/LED/T-Screen	
Size	Document Number: GM7C_MB	Rev: C
Date: Friday, January 21, 2011	Sheet: 34	of 59



ODD Connector

X02-05

DG: Place TX cap close to connector



Backwards Compatibility

MODC_EN

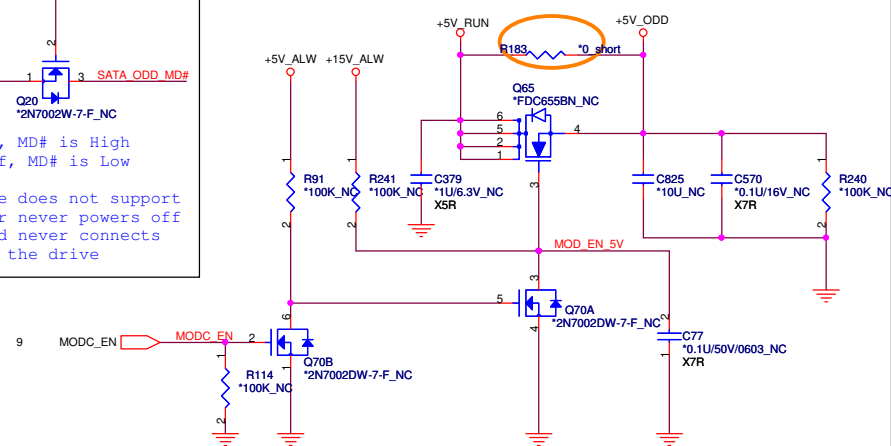
10 SATA_ODD_DA#

Q20 2N7002W-7-F_NC

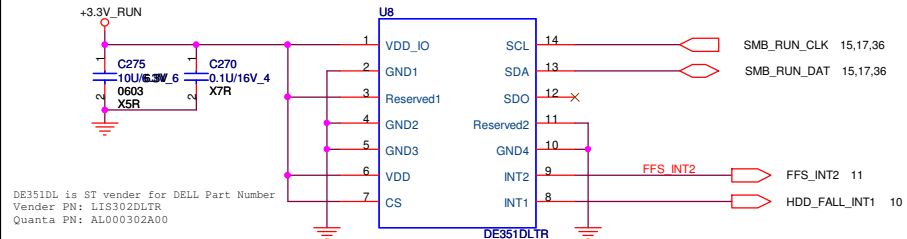
Drive powered on, MD# is High

Drive powered off, MD# is Low

Because the drive does not support 2PODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive



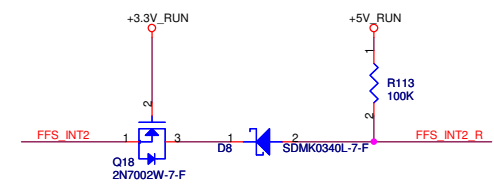
3-axis Fall Sensor (HDD data protector)



DE351DL is ST vender for DELL Part Number

Vender PN: LIS302DLTR

Quanta PN: AL000302A00



Quanta Computer Inc.

Project Name: **GM7C**

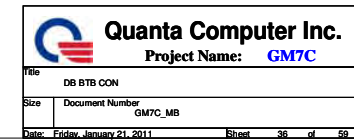
Title: SATA (HDD&ODD)

Size: Document Number: GM7C_MB

Date: Friday, January 21, 2011

Sheet: 35 of 59

Rev: C



R314 R115	POP	NC
R112	NC	POP



A00-10 13

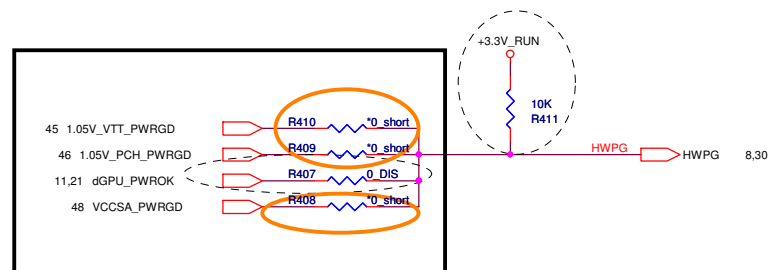
33 X01


X02-31 Remove Dell BT375 module

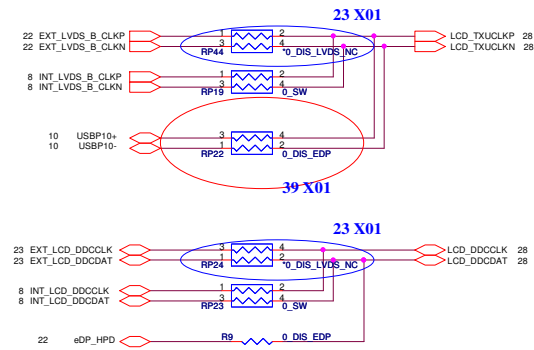



33 X01

58 X01



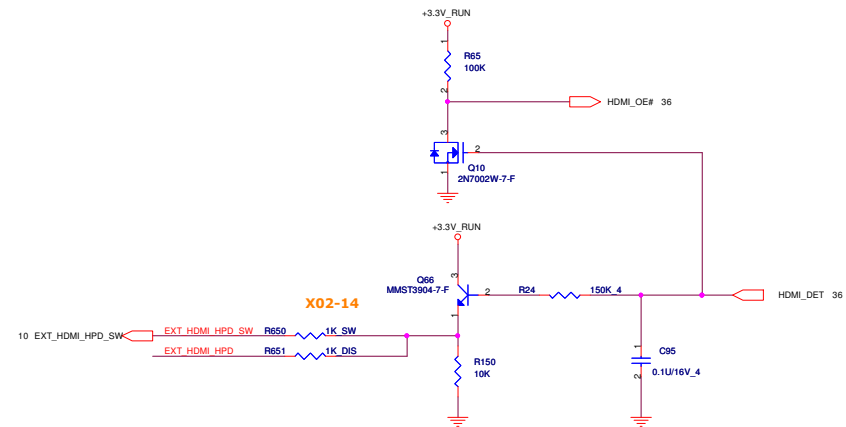
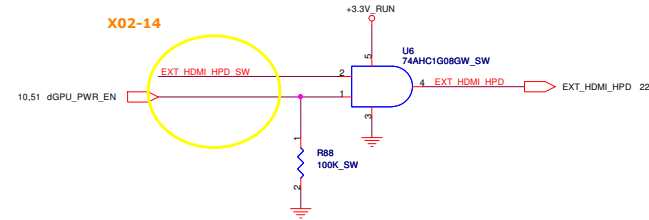
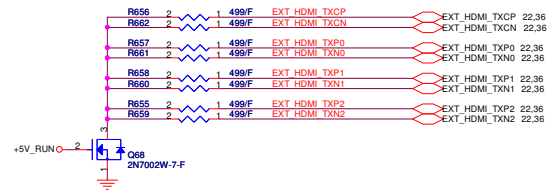
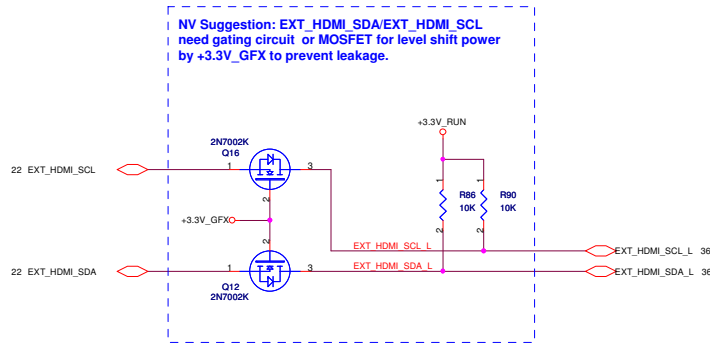
		Quanta Computer Inc.	
		Project Name: GM7C	
Title: System Reset Circuit			
Size	Document Number: GM7C_MB		Rev: C
Date: Friday, January 21, 2011		Sheet: 38	of 59




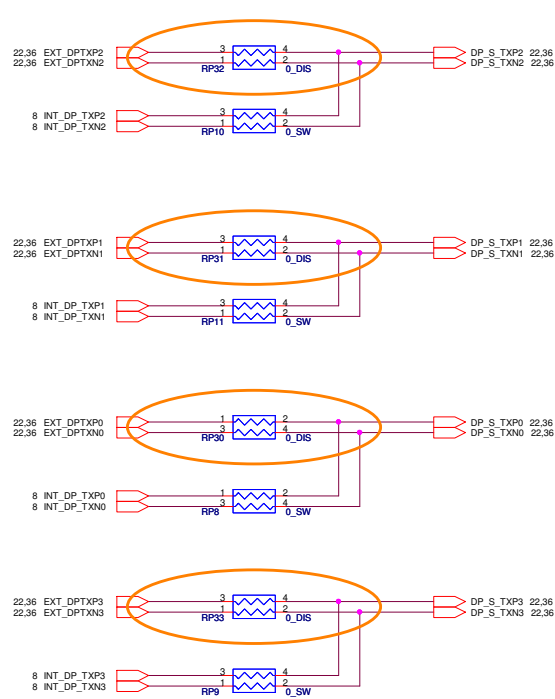
 Quanta Computer Inc. Project Name: GM7C			
Title LVDS Option			
Size	Document Number GM7C_MB	Rev C	
Date: Friday, January 21, 2011	Sheet 39	of 59	

Optimus 1.1

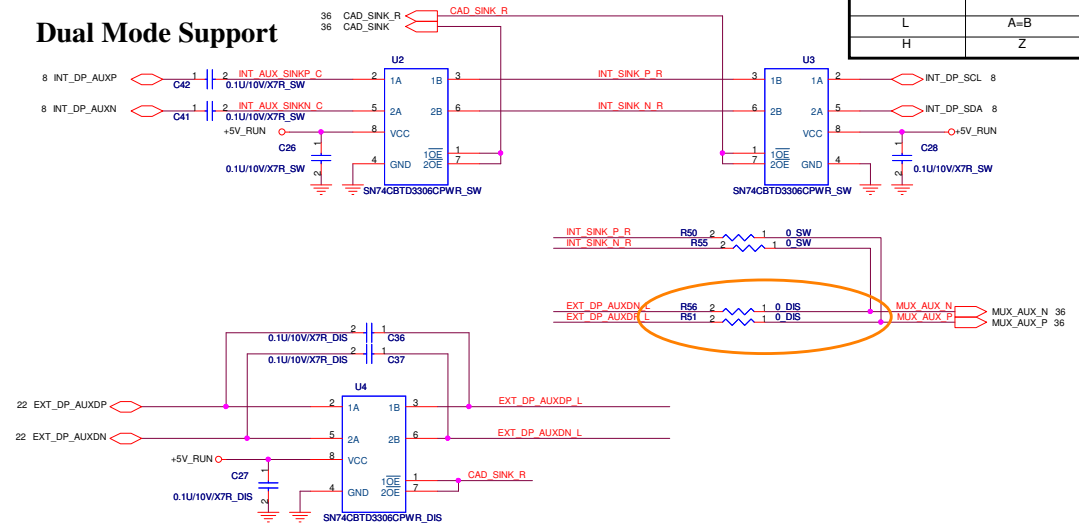
X02-01 Remove DP139 level shift



 Quanta Computer Inc. Project Name: GM7C		
File	HDMI Option	
Size	Document Number	Rev
	GM7C_MB	C
Date: Friday, January 21, 2011	Sheet	40 of 59



Dual Mode Support



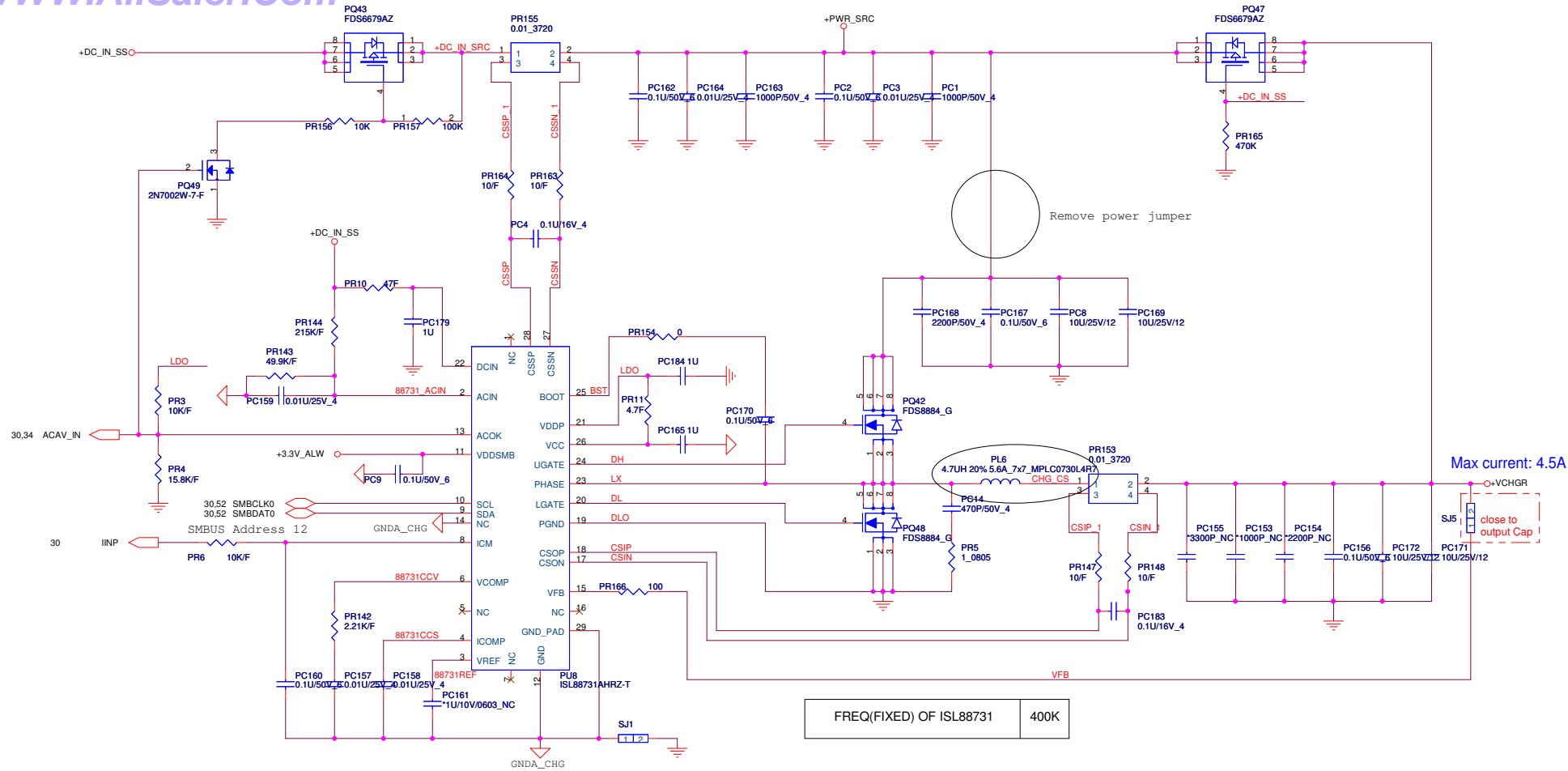
SN74CBTD3306 truth table

OE	Output
L	A=B
H	Z

Quanta Computer Inc.

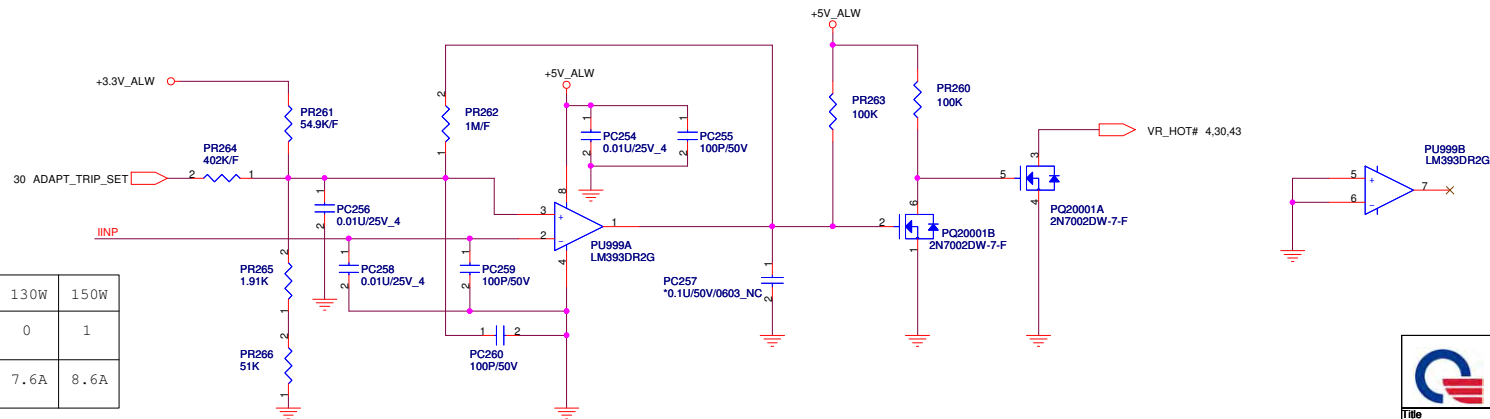
Project Name: GM7C

Title	DP Option
Size	Document Number
	GM7C_MB
Date: Friday, January 21, 2011	Sheet 41 of 59

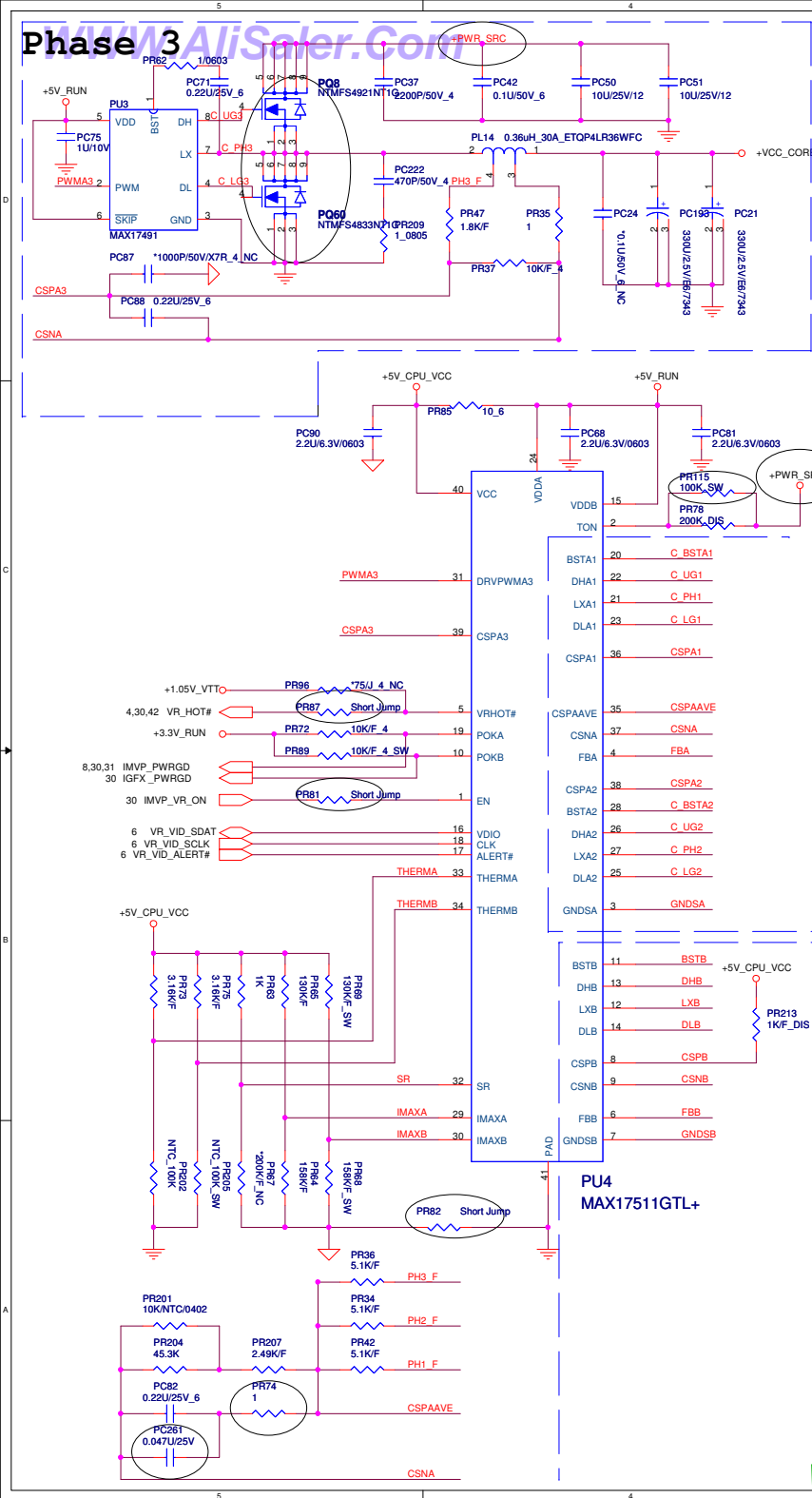


FREQ(FIXED) OF ISL88731 400K

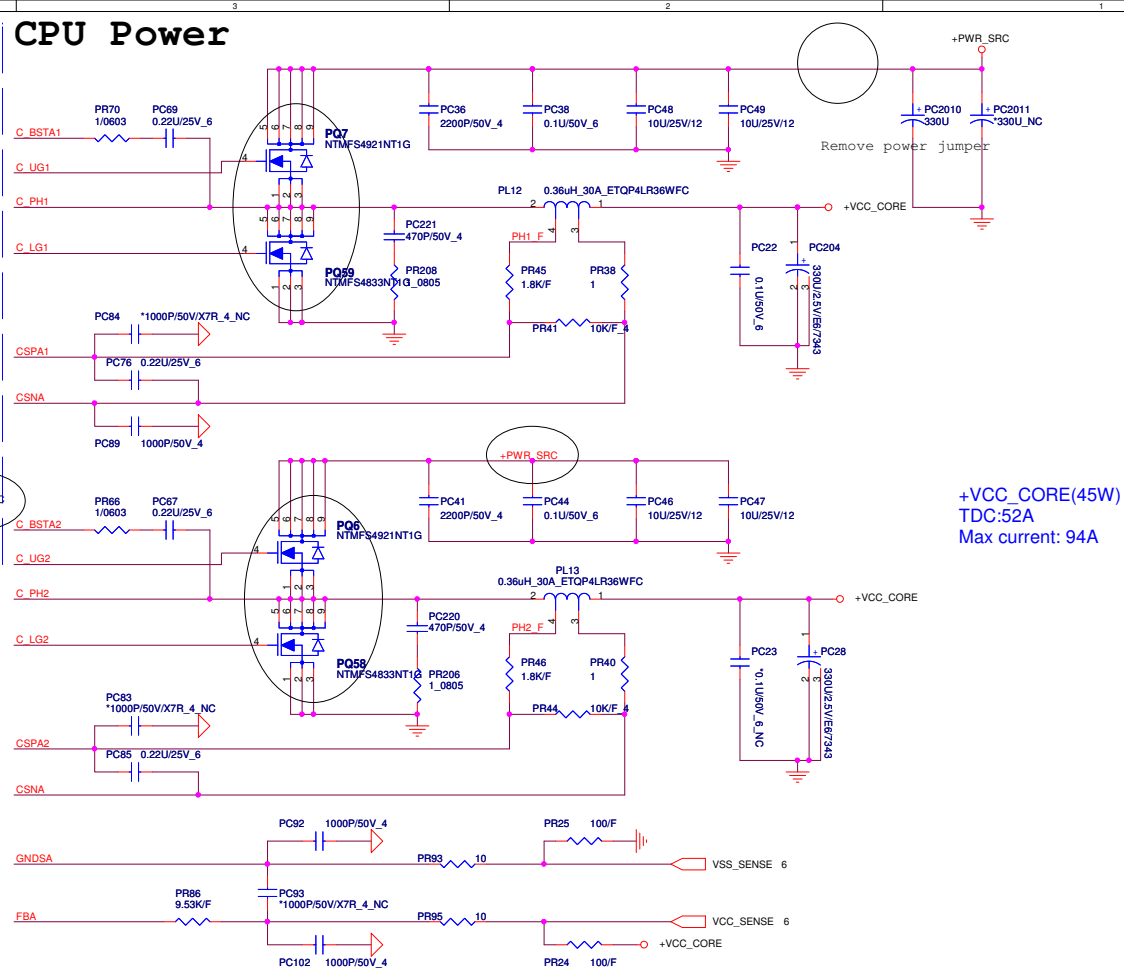
Max current: 4.5A



Phase 3

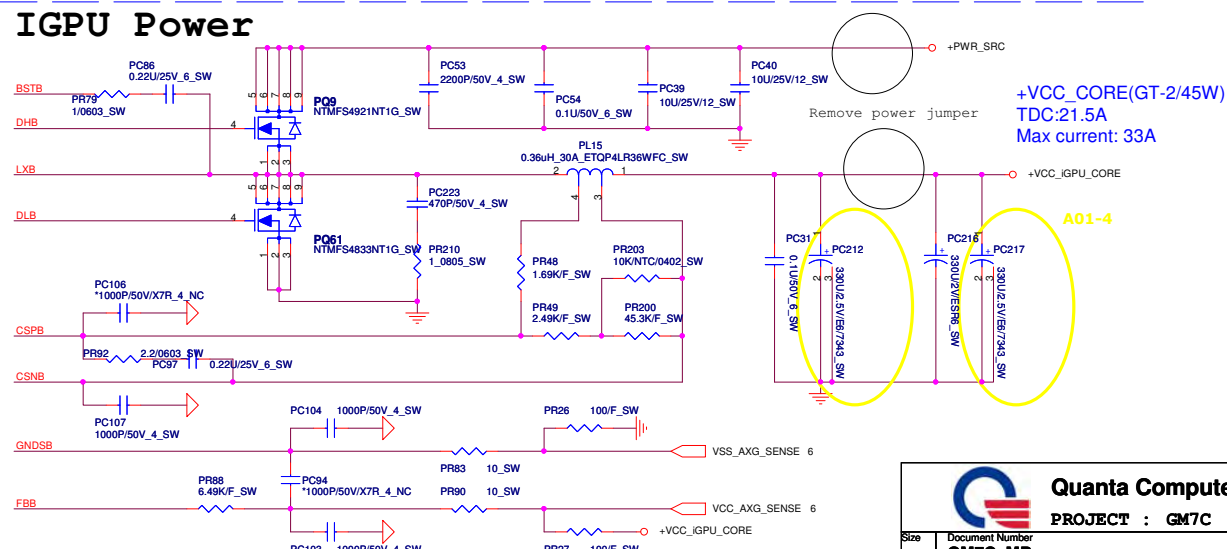


CPU Power

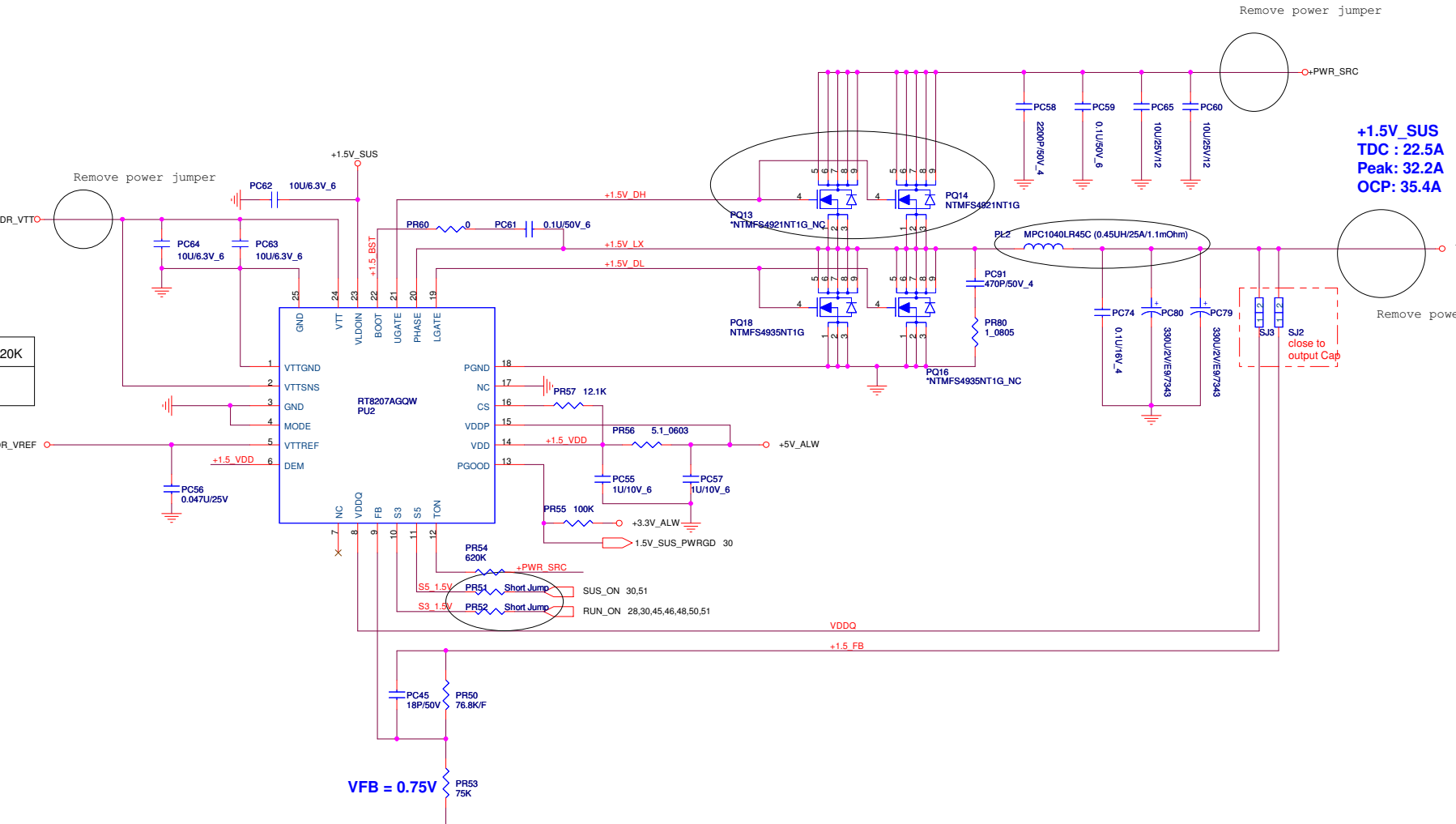


+VCC_CORE(45W)
TDC:52A
Max current: 94A

IGPU Power



+VCC_CORE(GT-2/45W)
TDC:21.5A
Max current: 33A



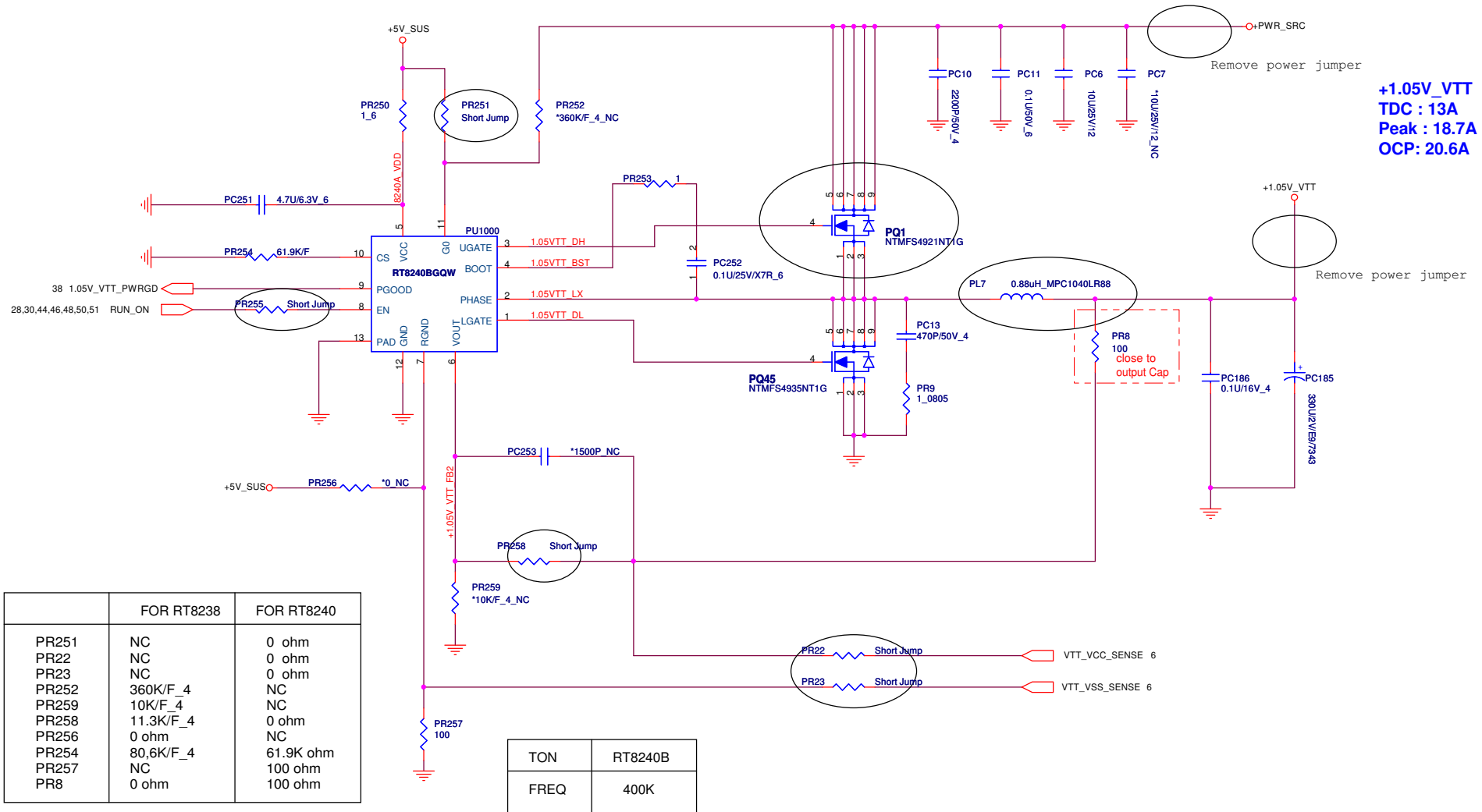
TON	PR54 = 620K
FREQ	400K

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

FB	VDDQ (V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	0.75V < VDDQ < 3.3V

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

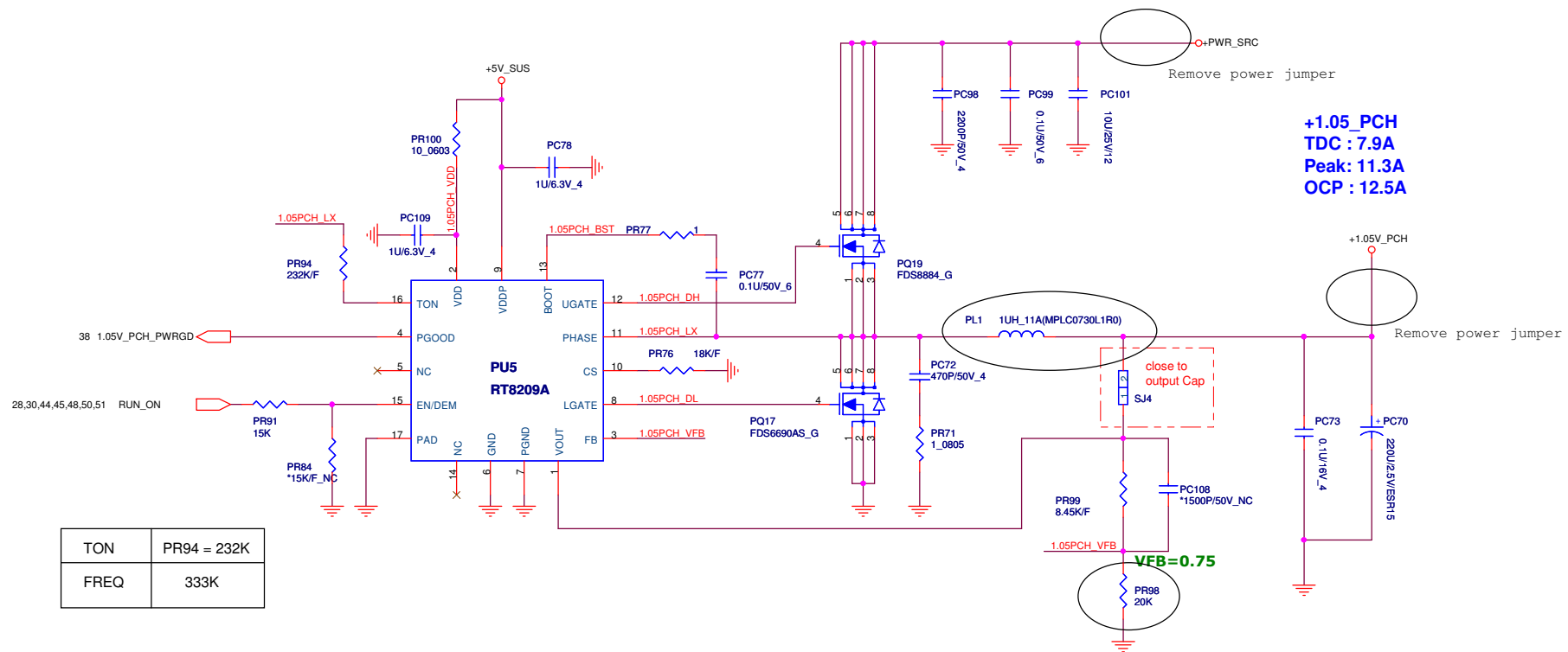
+1.05V_ VTT (RT8240B)

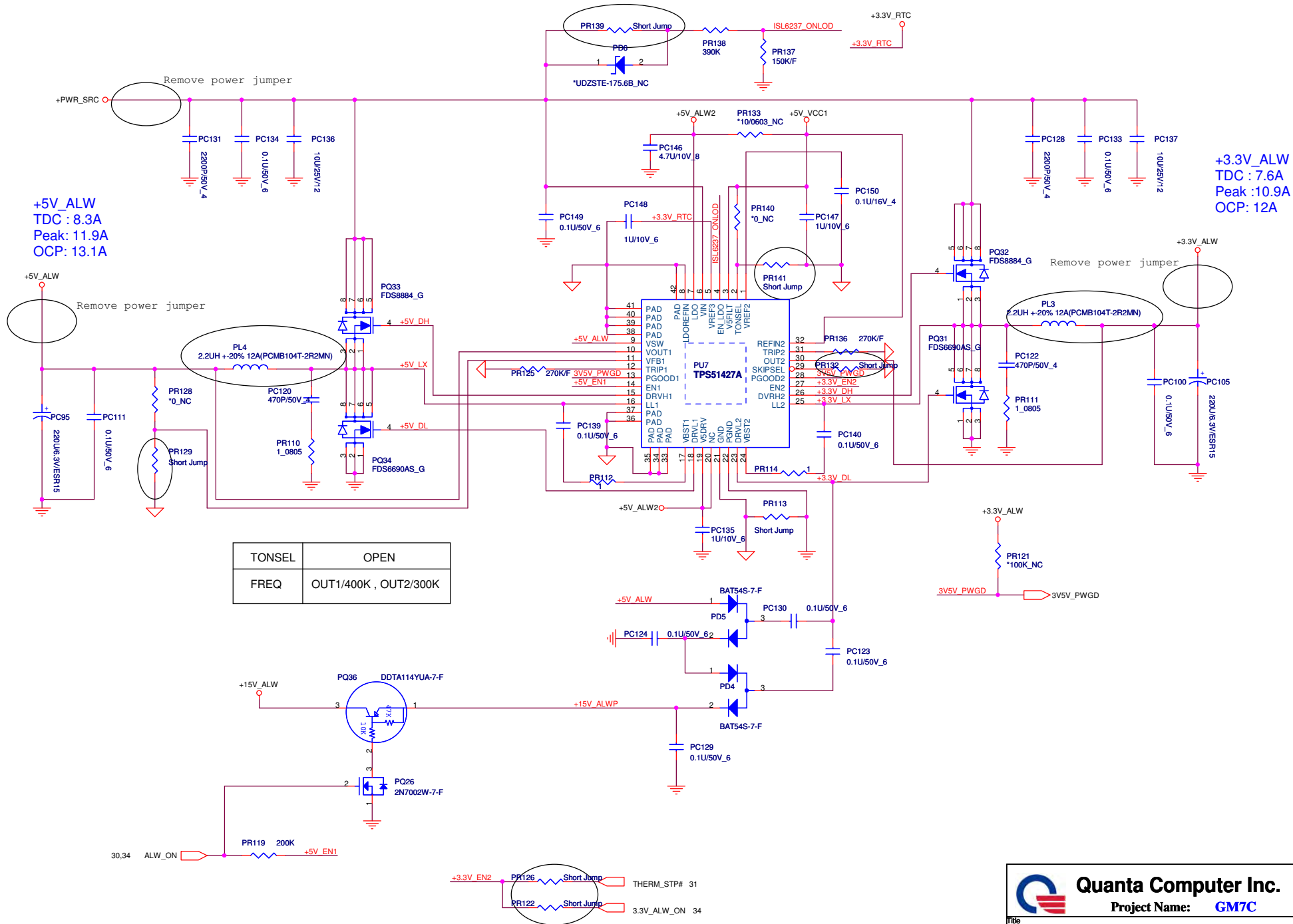


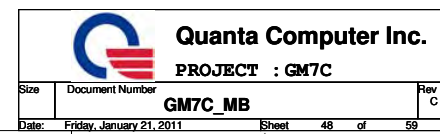
+1.05V_ VTT
TDC : 13A
Peak : 18.7A
OCP: 20.6A




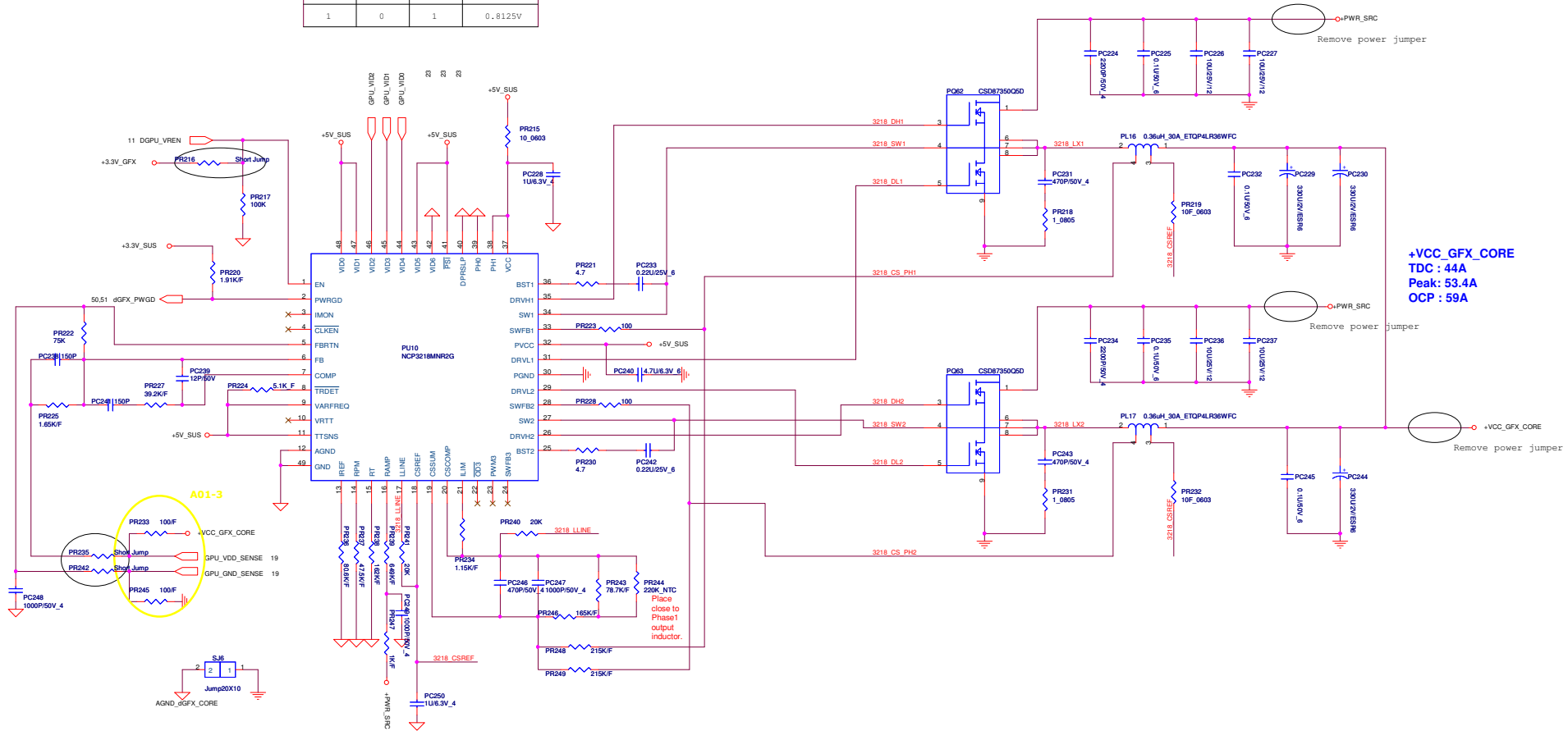
Quanta Computer Inc.
PROJECT : GM7C

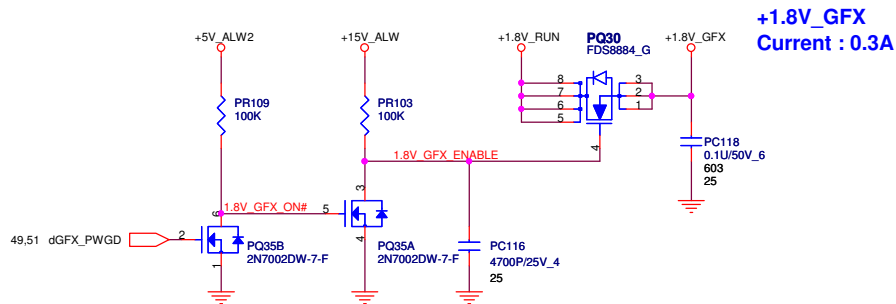
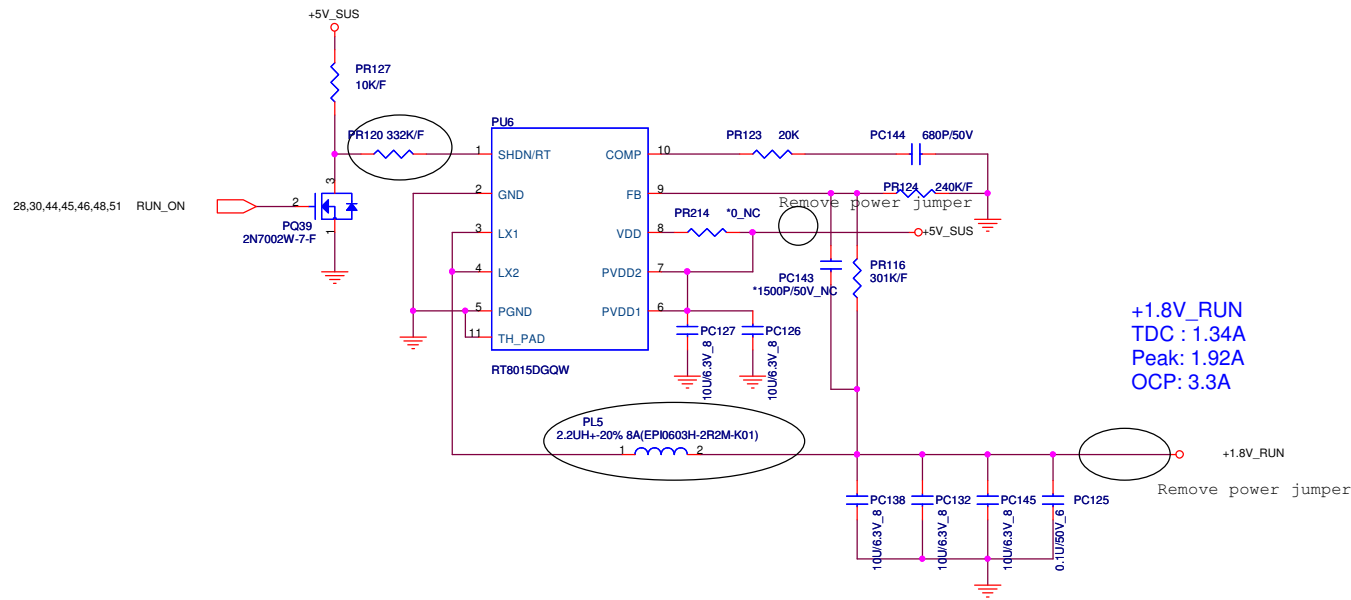


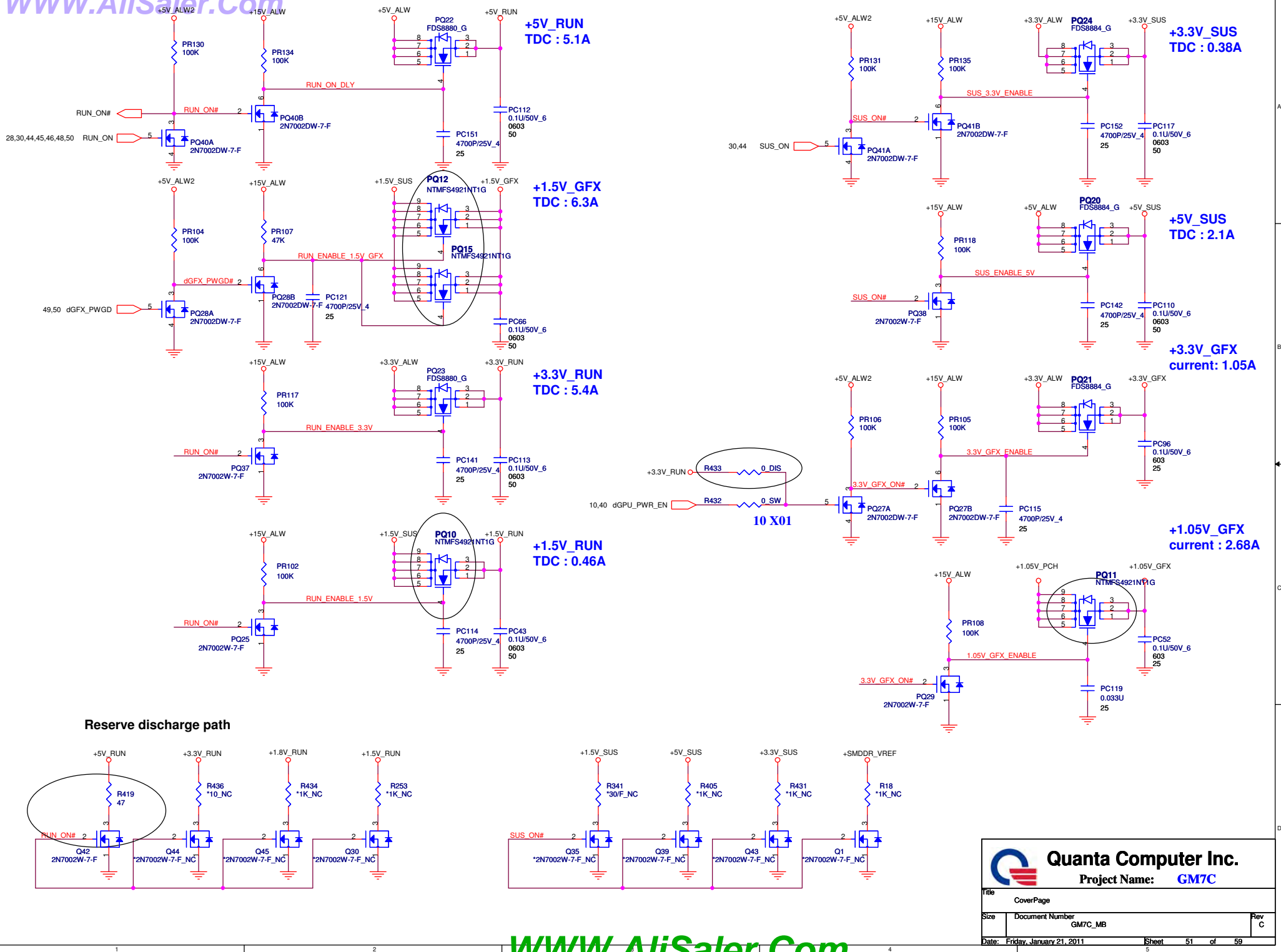


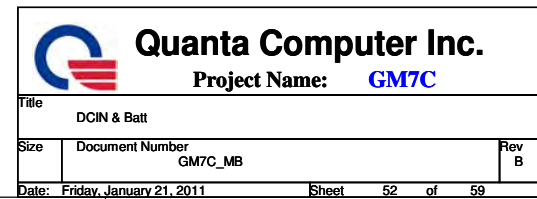


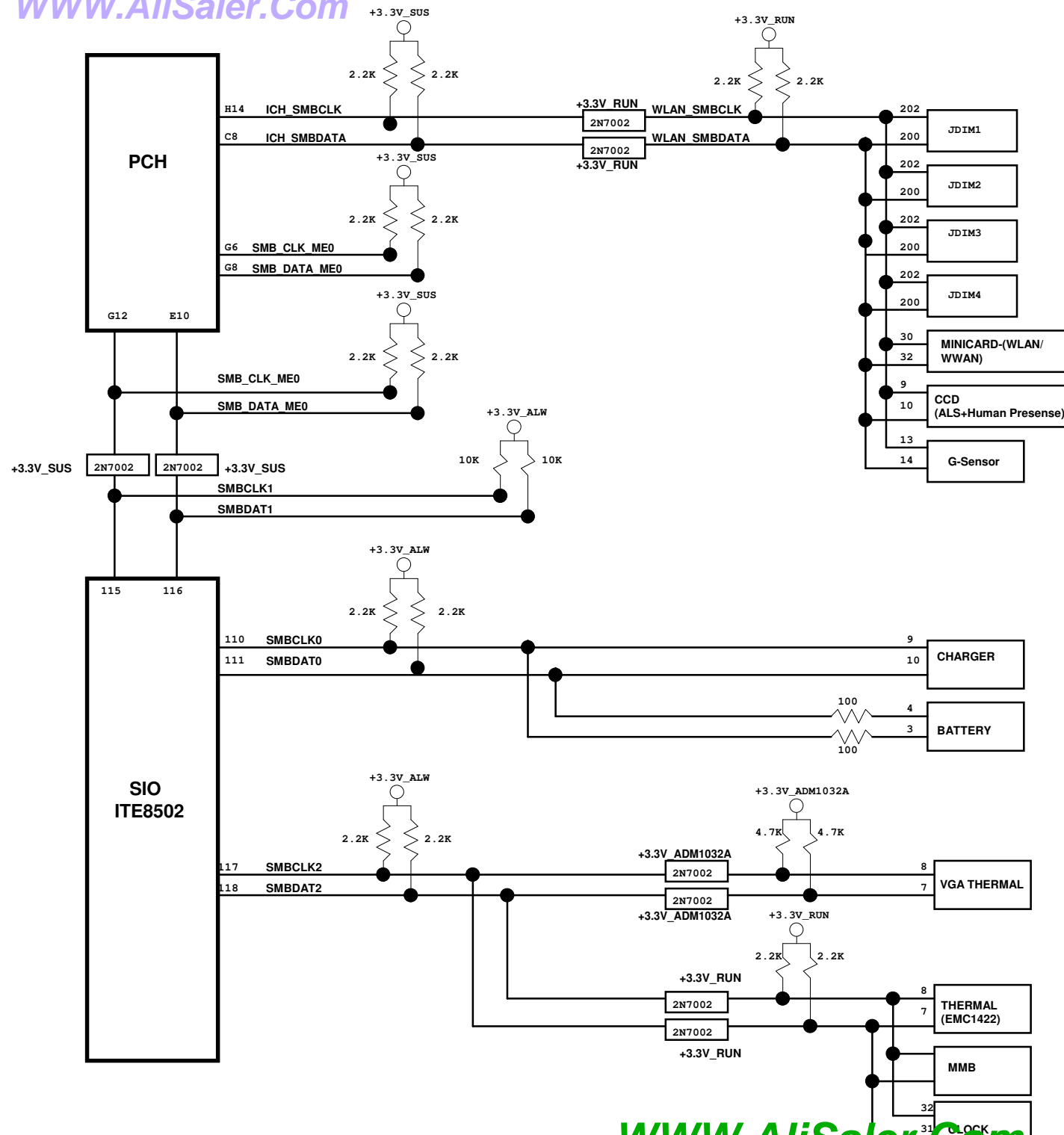
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	GM7C_MB		C
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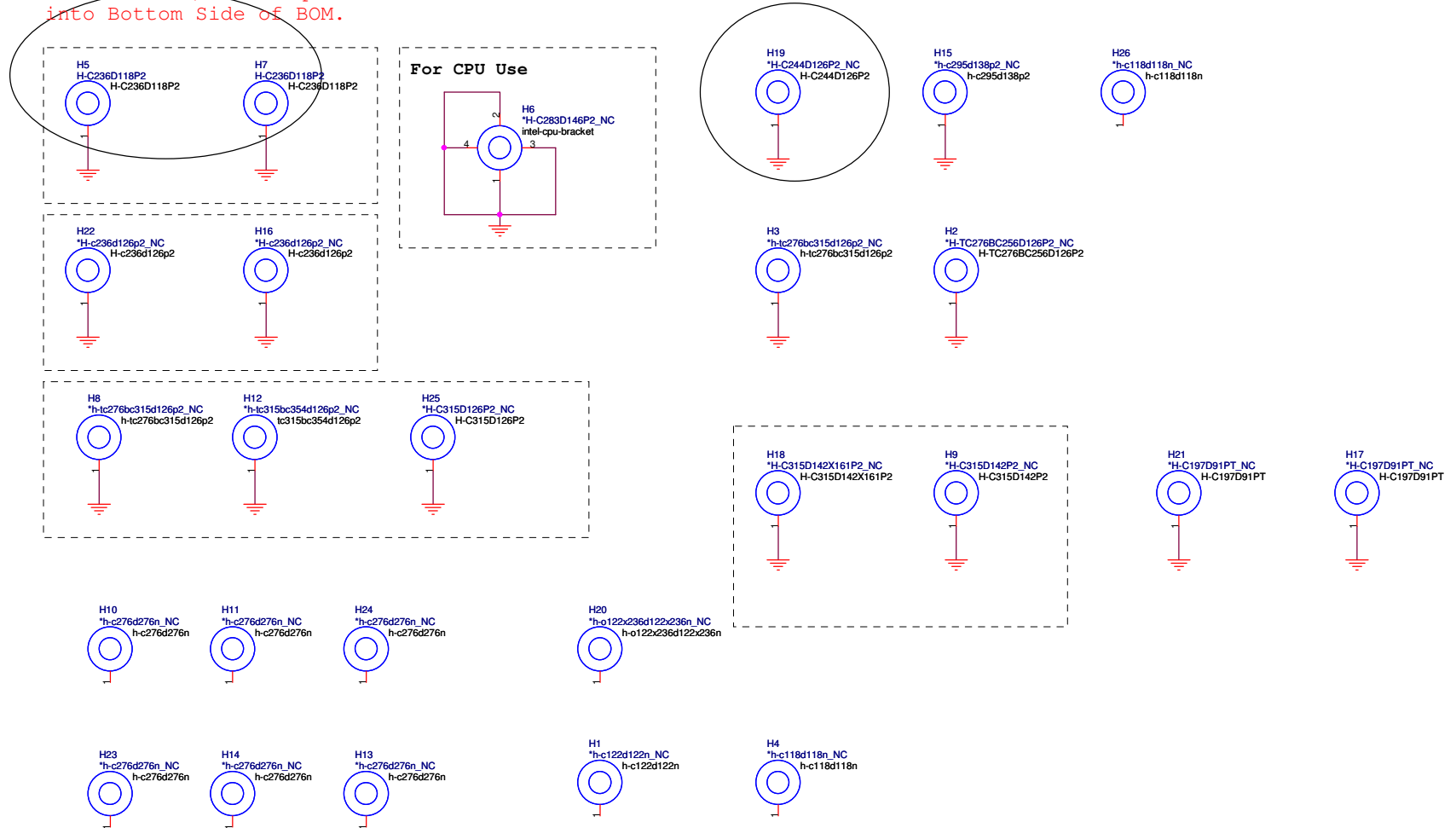







HCJM5004013
GM7C label on 31 header PN_3M

Add NUT on H5, H7 and put it into Bottom Side of BOM.



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