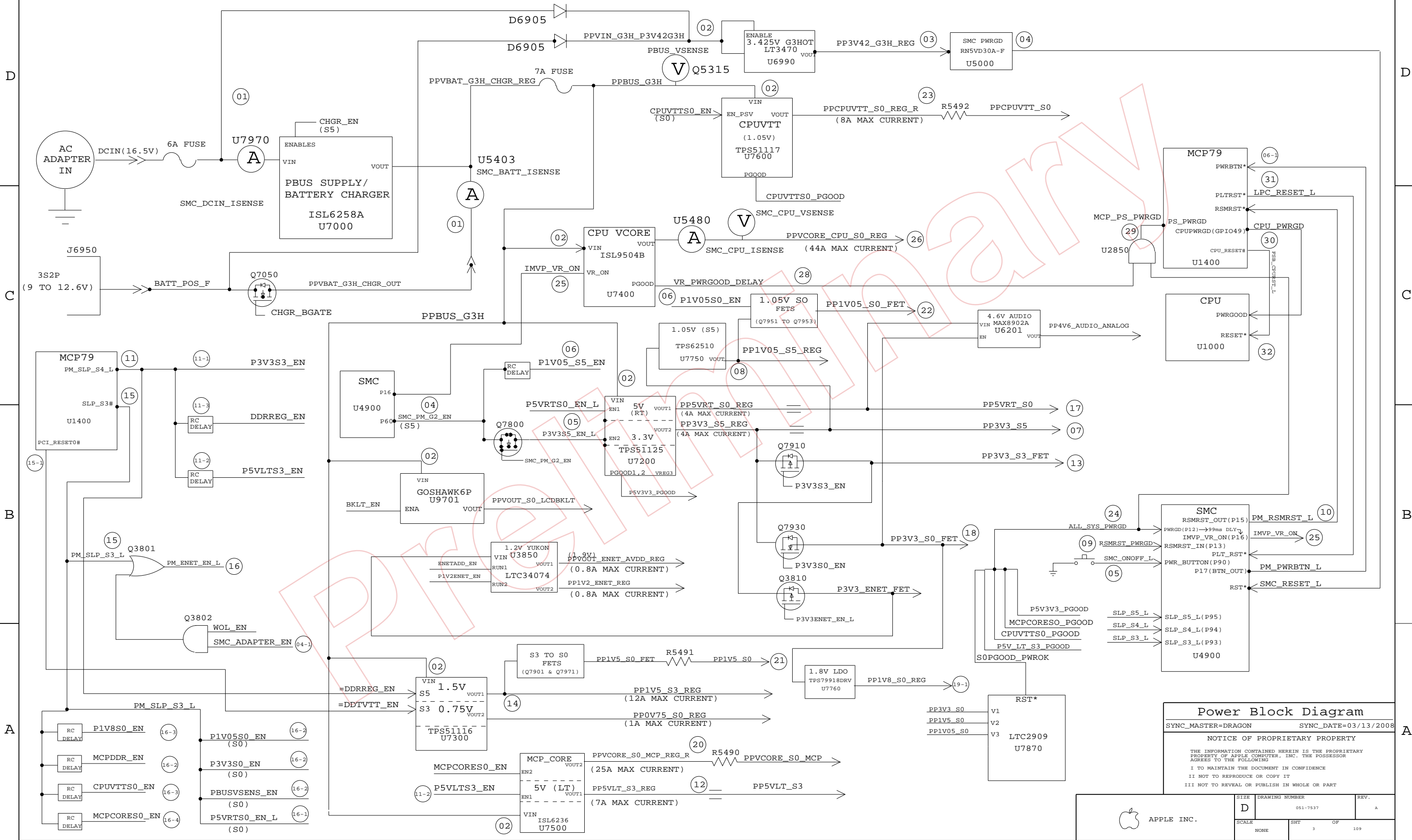


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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.												REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.												A		625211	PRODUCTION RELEASED	08/29/08	?
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.																	
M97 MLB SCHEMATIC																	
REFERENCED FROM T18																	
08/27/2008																	
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M97 POWER SYSTEM ARCHITECTURE



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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9554	PCBA,MLB,BETTER,M97	M97_COMMON,CPU_2_0GHZ,EEE_2KA
630-9314	PCBA,MLB,BEST,M97	M97_COMMON,CPU_2_4GHZ,EEE_1DJ

BOM Groups

BOM GROUP	BOM OPTIONS
M97_COMMON	COMMON,ALTERNATE,M97_MCP,M97_MISC,M97_DEBUG_PVT,M97_PROGPARTS
M97_MCP	MCP_B02,MCP_PROD,MEMRESET_HW,MEMRESET_MCP,BOOT_MODE_USER,MCPSEQ_SMC,MCP_CS1_NO
M97_MISC	ONEWIRE_PU,BKLT_PLL_NOT,DP_ESD,ENG_BMON,MIKEY
M97_PROGPARTS	BOOTROM_PROG,SMC_PROG,IR_PROG,WELLSPRING_PROG
M97_DEBUG_ENG	SMC_DEBUG_YES,XDP,XDP_CONN,LPCPLUS,VREFMRGN,TFAD_DEBUG
M97_DEBUG_PVT	SMC_DEBUG_YES,XDP,LPCPLUS,NO_VREFMRGN
M97_DEBUG_PROD	SMC_DEBUG_YES,XDP,LPCPLUS_NOT,NO_VREFMRGN

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3622	1	PDC,QDQL,QS,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ_QS
337S3624	1	PDC,QDYD,QS,2.26,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ_QS
337S3625	1	PDC,QDVJ,QS,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ_QS
337S3646	1	PDC,SLGRK,PRQ,2.0,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_0GHZ
337S3653	1	PDC,SL3BU,PRQ,2.26,25W,1066,C0,3M,BGA	U1000	CRITICAL	CPU_2_26GHZ
337S3639	1	PDC,SLB4N,PRQ,2.4,25W,1066,M0,3M,BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0540	1	IC,GMCP,MCP79,35X35MM,BGA1437,A01	U1400	CRITICAL	MCP_A01
338S0591	1	IC,GMCP,MCP79,35X35MM,BGA1437,A01P	U1400	CRITICAL	MCP_A01P
338S0603	1	IC,GMCP,MCP79,35X35MM,BGA1437,A01Q	U1400	CRITICAL	MCP_A01Q
338S0600	1	IC,GMCP,MCP79,35X35MM,BGA1437,B01	U1400	CRITICAL	MCP_B01
338S0635	1	IC,GMCP,MCP79,35X35MM,BGA1437,B02	U1400	CRITICAL	MCP_B02
338S0570	1	IC,RTL8211CL,GIGE TRANSCEIVER,48P,TQFP	U3700	CRITICAL	

Programmable Parts

338S0563	1	IC,SMC,H58/2117,9X9MM,TLP,HP	U4900	CRITICAL	SMC_BLANK
341S2287	1	IC,SMC,M97	U4900	CRITICAL	SMC_PROG
335S0610	1	IC,FLASH,SP1,32MBIT,3.3V,86MHZ,8-SOP	U6100	CRITICAL	BOOTROM_BLANK
341S2285	1	IC,PRGRM,EPI BOOTROM,UNLOCK,M97	U6100	CRITICAL	BOOTROM_PROG
338S0375	1	IC,CY7C63833,ENCORE II,USB CONTROLLER	U4800	CRITICAL	IR_BLANK
341S2093	1	IC,IR CONTROLLER,M97	U4800	CRITICAL	IR_PROG
337S2983	1	IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794	U5701	CRITICAL	WELLSPRING_BLANK
341S2348	1	IC,WELLSPRING CONTROLLER,M97	U5701	CRITICAL	WELLSPRING_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	CYNTEC AS ALTERNATE
152S0796	152S0685		ALL	CYNTEC AS ALTERNATE
152S0694	152S0138		ALL	MAGLAYERS AS ALTERNATE
157S0058	157S0055		ALL	DELTA AS ALTERNATE
104S0018	104S0023		ALL	DALE/VISHAY AS ALTERNATE
128S0093	128S0218		ALL	KEMET AS ALTERNATE
152S0874	152S0516		ALL	MAGLAYERS AS ALTERNATE
152S0847	152S0586		ALL	MAGLAYERS AS ALTERNATE
514-0612	514-0607		ALL	FOXLINK AS ALTERNATE
514-0613	514-0608		ALL	FOXLINK AS ALTERNATE

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2K9]	CRITICAL	EEE_2K9
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:2KA]	CRITICAL	EEE_2KA
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:1DJ]	CRITICAL	EEE_1DJ

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BOTTOM

SIGNAL

GROUND

SIGNAL(High Speed)

SIGNAL(High Speed)

GROUND

POWER

POWER

GROUND

SIGNAL(High Speed)

SIGNAL(High Speed)

GROUND

SIGNAL

BOM Configuration

SYNC_MASTER=M97_MLB

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APPLE INC.

SIZE D

SCALE NONE

DRAWING NUMBER 051-7537

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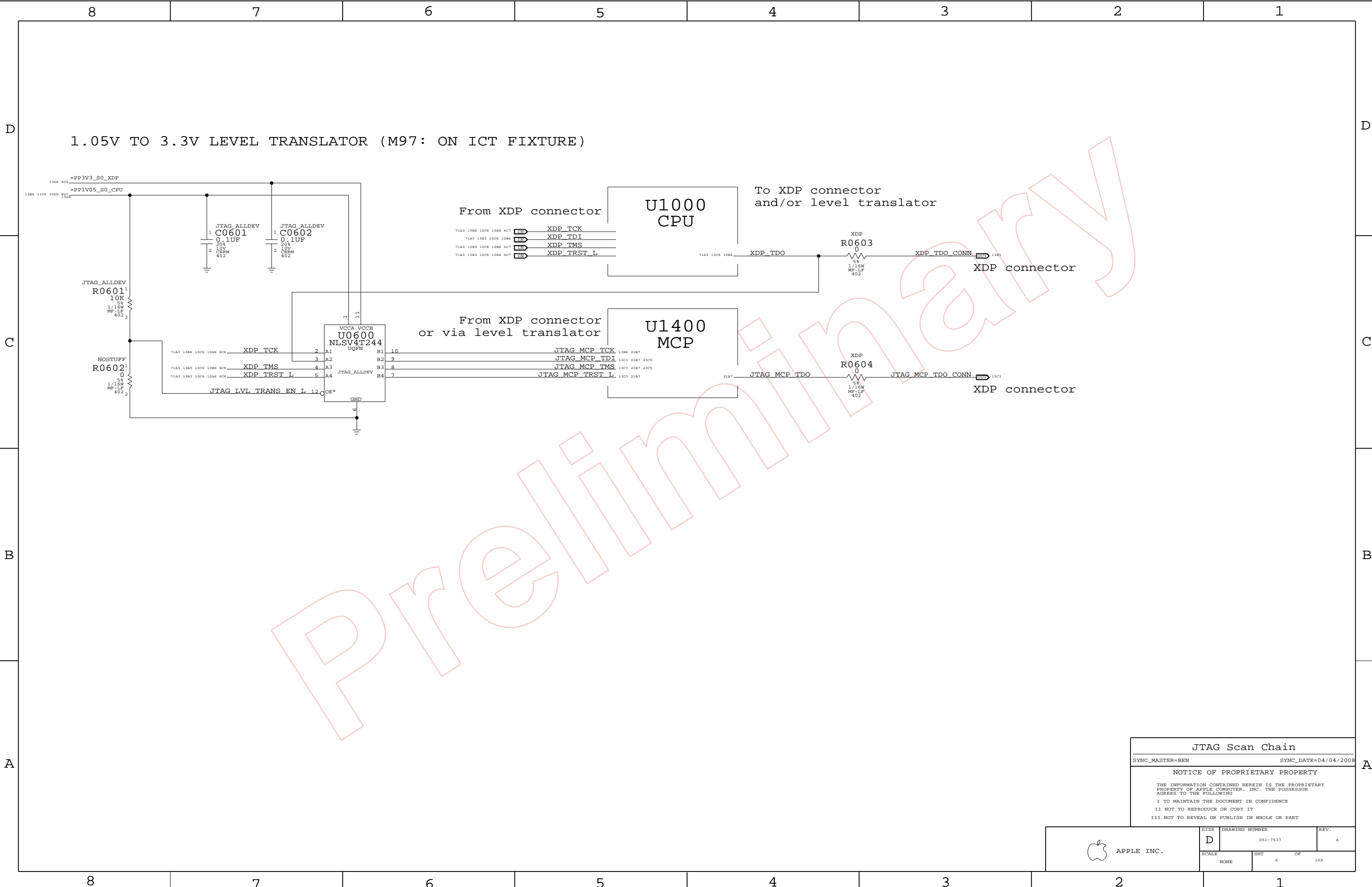
Preliminary

Revision History

A		
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SIZE D	DRAWING NUMBER 051-7537	REV. A
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	APPLE INC.
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NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.



JTAG Scan Chain

SYNC_MASTER=BEN

SYNC_DATE=04/04/2008


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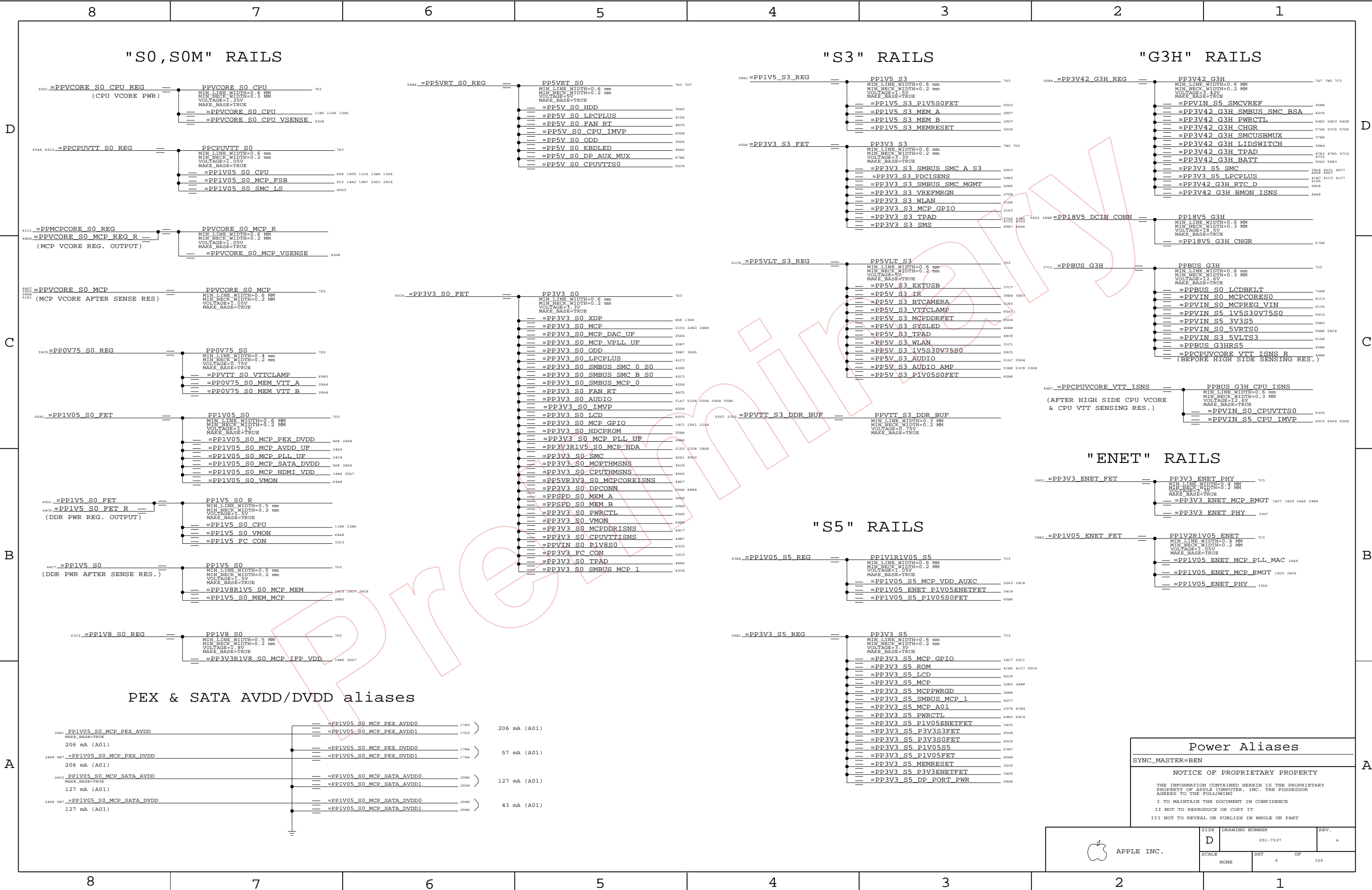
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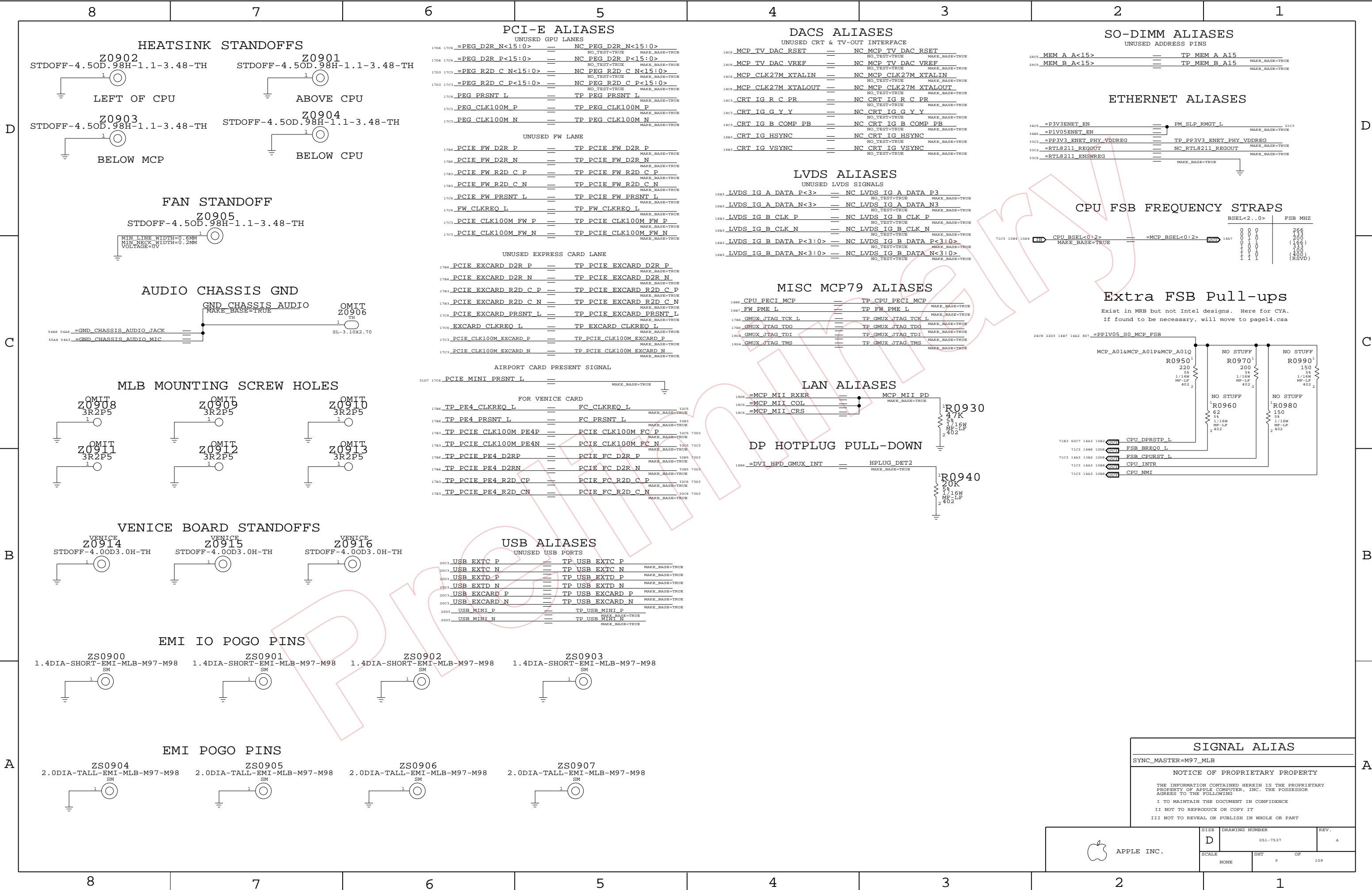
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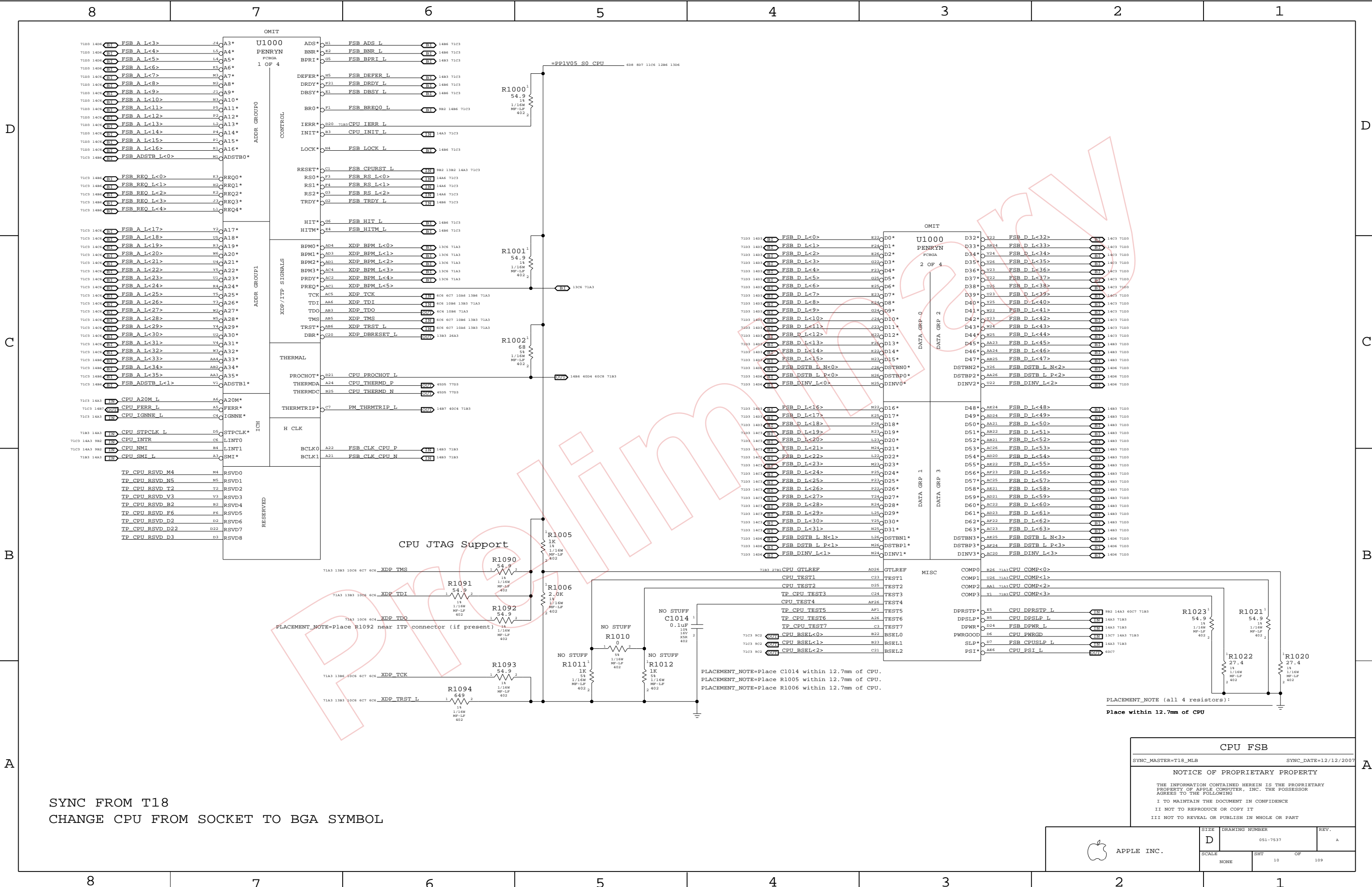
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Functional Test Points								
D	Fan Connectors		RIGHT CLUTCH CONN		DEBUG VOLTAGE			
	188P	TRUE PP5VRT S0 (NEED 3 TP) 703 805	188B	TRUE PP5V S3 BTCAMERA F 3187	188P	TRUE PPVCORE S0 CPU 807	D	
	188S	TRUE FAN RT PWM 4684	188B	TRUE PCIE MINI D2R P 1786 3107 7303	188P	TRUE PPCPUVTT S0 807		
	188C	TRUE FAN RT TACH 46C4	188B	TRUE PCIE MINI D2R N 1786 3107 7303	188P	TRUE PPVCORE S0 MCP 807		
	(NEED TO ADD 3 GND TP)		188B	TRUE PCIE MINI R2D P 3107 7303	188P	TRUE PP0V75 S0 807		
	MIC FUNC_TEST		188B	TRUE PCIE MINI R2D N 3107 7303	188P	TRUE PP1V05 S0 807		
	189T	TRUE MIC HI CONN 5481 54D2	188B	TRUE PCIE CLK100M MINI CONN P 3108 7303	188P	TRUE PP1V5 S0 887		
	189S	TRUE MIC LO CONN 5481 54D2	188B	TRUE PCIE CLK100M MINI CONN N 3108 7303	188P	TRUE PP1V8 S0 887		
	189C	TRUE MIC SHLD CONN 54D2 55A6	188B	TRUE USB CAMERA CONN P 3187 7403	188P	TRUE PP5VRT S0 707 8D5		
	SPEAKER FUNC_TEST		188B	TRUE USB CAMERA CONN N 3187 7403	188P	TRUE PP3V3 S0 8C5		
	189P	TRUE SPKRAMP L N OUT 53A2 54C2	188B	TRUE PP5V WLAN 703 31C5	188P	TRUE PP1V5 S3 8D3		
C	189S	TRUE SPKRAMP L P OUT 53B2 54C2	188B	TRUE TRUE SMBUS SMC A S3 SCL 1786 23C5 31C7	188P	TRUE PP3V3 S3 785 8D3	C	
	189C	TRUE SPKRAMP R N OUT 53C3 54C2	188B	TRUE TRUE SMBUS SMC A S3 SDA 785 42D2 76D3	188P	TRUE PP5VLT S3 8C3		
	189S	TRUE SPKRAMP R P OUT 53C3 54C2	188B	TRUE CONN USB2 BT P 3187 7483	188P	TRUE PP1V1R1V05 S5 8B3		
	189P	TRUE SPKRAMP R P OUT 53C3 54C2	188B	TRUE CONN USB2 BT N 3187 7483	188P	TRUE PP3V3 S5 8B3		
	189P	TRUE SPKRAMP SUB N OUT 53B2 54C2	188B	TRUE MINI CLKREQ O L 31C7	188P	TRUE PP3V42 G3H 7A7 785 8D1		
	189C	TRUE SPKRAMP SUB P OUT 53B2 54C2	188B	TRUE MINI RESET CONN L 31A7	188P	TRUE PPBUS G3H 8C1		
	THERMAL FUNC_TEST		188B	(NEED TO ADD 3 GND TP)	188P	TRUE PP3V3 ENET PHY 8B1		
	189P	TRUE MCPTHMSNS D2 P 45B5 77D3	188B	SATA HDD CONN (NEED 4 TP)	188P	TRUE PP1V2R1V05 ENET 8B1		
	189S	TRUE MCPTHMSNS D2 N 45B5 77D3	188B	189B	188P	TRUE PP3V3 G3 RTC 21C8 22A5 26D4		
	LVDS FUNC_TEST		188B	189B	188P	TRUE PP5V WLAN 7D5 31C5		
B	189C	TRUE PP3V3 LCDVDD SW F 7C3 66C2	188B	189B	188P	TRUE PP5V SW ODD 787 36D3	B	
	189B	TRUE PP3V3 S0 LCD F 66C3	188B	189B	188P	TRUE PP5V S0 HDD FLT 7C5 36A7		
	189C	TRUE PPVOUT S0 LCDBKLT 7C3 66B2 69B3 69C1	188B	189B	188P	TRUE PP3V3 S5 AVREF SMC 39D4 40B6		
	189B	TRUE LVDS IG DDC CLK 18A3 66C5	188B	189B	188P	TRUE PP18V5 S3 7C5 48C1 48D3		
	189C	TRUE LVDS IG A DATA N<0> 18B3 66C2 73B3	188B	189B	188P	TRUE PP3V3 S3 LDO 7C5 48B4 48C3		
	189S	TRUE LVDS IG A DATA P<0> 18B3 66C2 73B3	188B	189B	188P	TRUE PP3V3 LCDVDD SW F 7C7 66C2		
	189C	TRUE LVDS IG A DATA N<1> 18B3 66C2 73B3	188B	189B	188P	TRUE PPVOUT S0 LCDBKLT 7C7 66B2 69B3 69C1		
	189S	TRUE LVDS IG A DATA P<1> 18B3 66C2 73B3	188B	189B	188P	TRUE BKL VREF 4V9 49A8 49B6 49C4 49C8		
	189C	TRUE LVDS IG A DATA N<2> 18B3 66C2 73B3	188B	189B	188P	TRUE PP4V6 AUDIO ANALOG 51A3 51D3 52D6		
	189S	TRUE LVDS IG A DATA P<2> 18B3 66C2 73B3	188B	189B	188P	TRUE SMC PM G2 EN 39D5 64D8		
A	189C	TRUE LVDS IG A CLK F N 66B2 73B3	188B	189B	188P	TRUE PM SLP S4 L 21C3 39C5 40A2 64C8	A	
	189B	TRUE LVDS IG A CLK F P 66B2 73B3	188B	189B	188P	TRUE PM SLP S3 L 21C3 34B7 39C5 41A5 64D5 68D8		
	189C	TRUE LED RETURN 1 66B3 69C1	188B	189B	(NEED TO ADD 4 GND TP)			
	189S	TRUE LED RETURN 2 66B3 69B1	188B	189B	FUNC TEST			
	189C	TRUE LED RETURN 3 66B3 69B1	188B	189B	SYNC_MASTER=M97_MLB			
	189S	TRUE LED RETURN 4 66B3 69B1	188B	189B	NOTICE OF PROPRIETARY PROPERTY			
	189C	TRUE LED RETURN 5 66B3 69B1	188B	189B	THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING			
	189S	TRUE LED RETURN 6 66B3 69B1	188B	189B	I TO MAINTAIN THE DOCUMENT IN CONFIDENCE			
	(NEED TO ADD 5 GND TP)		188B	189B	II NOT TO REPRODUCE OR COPY IT			
	SATA ODD CONN		188B	189B	III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
A	189C	TRUE PP5V SW ODD (NEED 4 TP) 7C3 36D3	188B	189B	SIZE D		A	
	189B	TRUE SMC ODD DETECT 36B7 39B8	188B	189B	DRAWING NUMBER 051-7537			
	189C	TRUE SATA ODD D2R C P 36B5 73A3	188B	189B	SCALE NONE			
	189S	TRUE SATA ODD D2R C N 36B5 73A3	188B	189B	SHT 7			
	189P	TRUE SATA ODD R2D P 36B5 73A3	188B	189B	OF 109			
	189C	TRUE SATA ODD R2D N 7C5 36B5 73A3	188B	189B	APPLE INC.			
	(NEED TO ADD 4 GND TP)		188B	189B	REV. A			
	DC POWER CONN		188B	189B	KBD BACKLIGHT CONN			
	189B	TRUE PP18V5 DCIN FUSE (NEED 3 TP) 56D6	188B	189B	TRUE KBDLED ANODE 48A4			
	189C	TRUE ADAPTER SENSE 56D7	188B	189B	(NEED TO ADD 2 GND TP)			
A	BATT POWER CONN		188B	189B	KBD BACKLIGHT CONN		A	
	189B	TRUE PPVBAT G3H CONN F (NEED 3 TP) 56A8	188B	189B	TRUE KBDLED ANODE 48A4			
	189C	TRUE GND BATT CONN (NEED 3 TP) 56A8	188B	189B	(NEED TO ADD 2 GND TP)			
	189S	TRUE SMBUS SMC BSA SCL 7A7 42C5 76D3	188B	189B	KBD BACKLIGHT CONN			
	189C	TRUE SMBUS SMC BSA SCL 7A7 42C5 76D3	188B	189B	TRUE KBDLED ANODE 48A4			
	189B	TRUE SMC BS ALRT L 39C5 40B2 56A8	188B	189B	(NEED TO ADD 2 GND TP)			
	BATT SIGNAL CONN		188B	189B	KBD BACKLIGHT CONN			
	189B	TRUE PP3V42 G3H (NEED 3 TP) 785 7C3 8D1	188B	189B	TRUE KBDLED ANODE 48A4			
	189C	TRUE SMBUS SMC BSA SCL 7A7 42C5 76D3	188B	189B	(NEED TO ADD 2 GND TP)			
	189S	TRUE SMBUS SMC BSA SCL 7A7 42C5 76D3	188B	189B	KBD BACKLIGHT CONN			
A	189C	TRUE SMC BIL BUTTON DB L 56A5	188B	189B	TRUE KBDLED ANODE 48A4		A	
	(NEED TO ADD 3 GND TP)		188B	189B	(NEED TO ADD 2 GND TP)			
	FRONT FLEX CONN		188B	189B	KBD BACKLIGHT CONN			
	189B	TRUE PP3V42 G3H LIDSWITCH R 38B6	188B	189B	TRUE KBDLED ANODE 48A4			
	189C	TRUE PP5V S3 IR R 38B6	188B	189B	(NEED TO ADD 2 GND TP)			
	189S	TRUE IR RX OUT 38A4 38C4	188B	189B	KBD BACKLIGHT CONN			
	189C	TRUE SMC LID R 38B6	188B	189B	TRUE KBDLED ANODE 48A4			
	189B	TRUE SYS LED ANODE R 38B6	188B	189B	(NEED TO ADD 2 GND TP)			
	(NEED TO ADD 2 GND TP)		188B	189B	KBD BACKLIGHT CONN			
	FRONT FLEX CONN		188B	189B	TRUE KBDLED ANODE 48A4			







SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

CPU FSB
SYNC_MASTER=T18_MLB
SYNC_DATE=12/12/2007
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7537	REV. A
	SCALE NONE	SHT 10	OF 109

D

C

B

A

D

C

B

A

SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL

Current numbers from Merom for Santa Rosa EMTS, doc #20905.

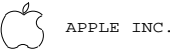


CPU Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	11	109



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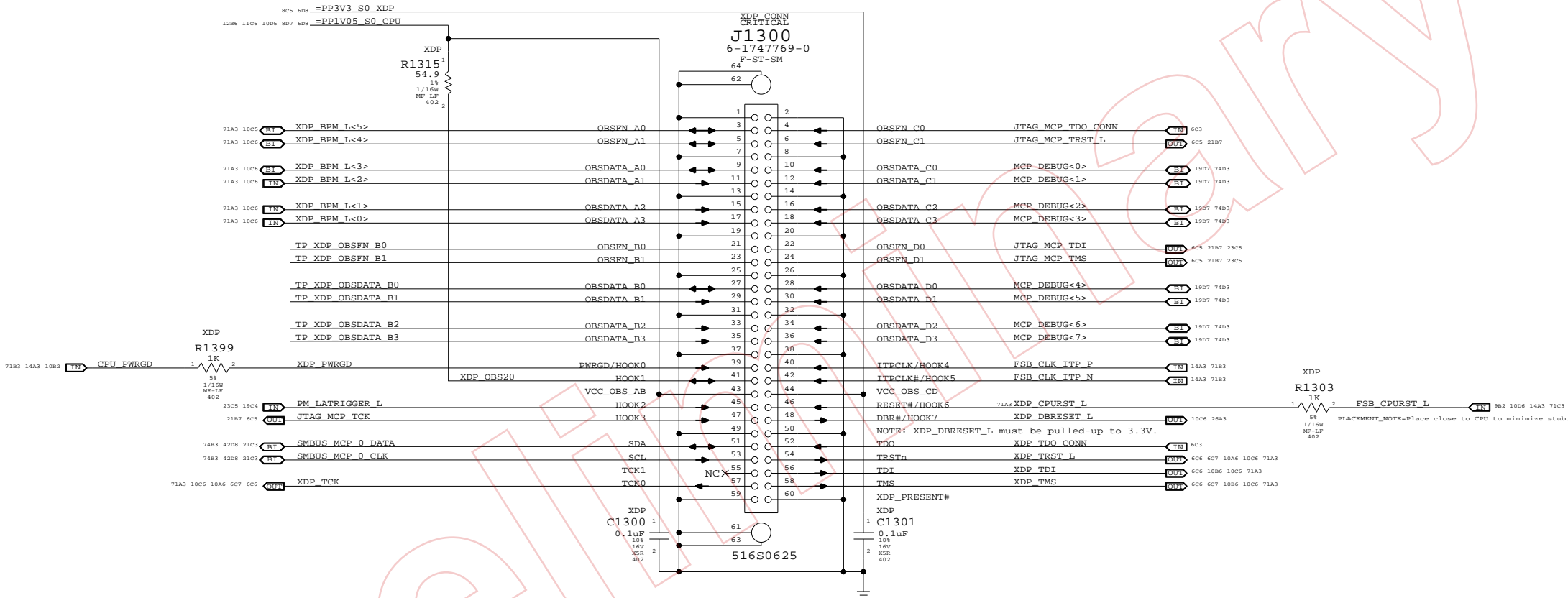
D

C

B

A

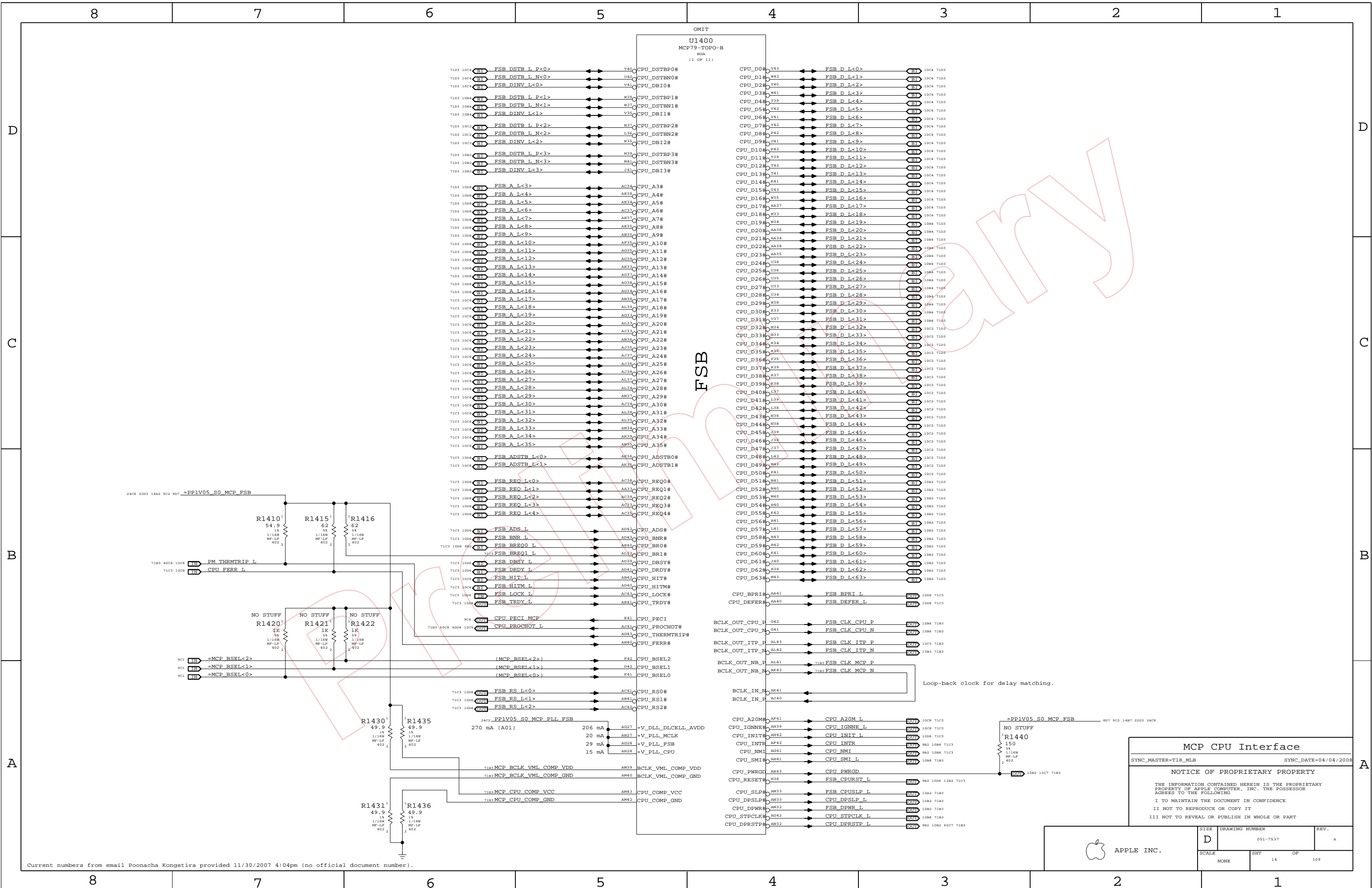
MCP79-specific pinout

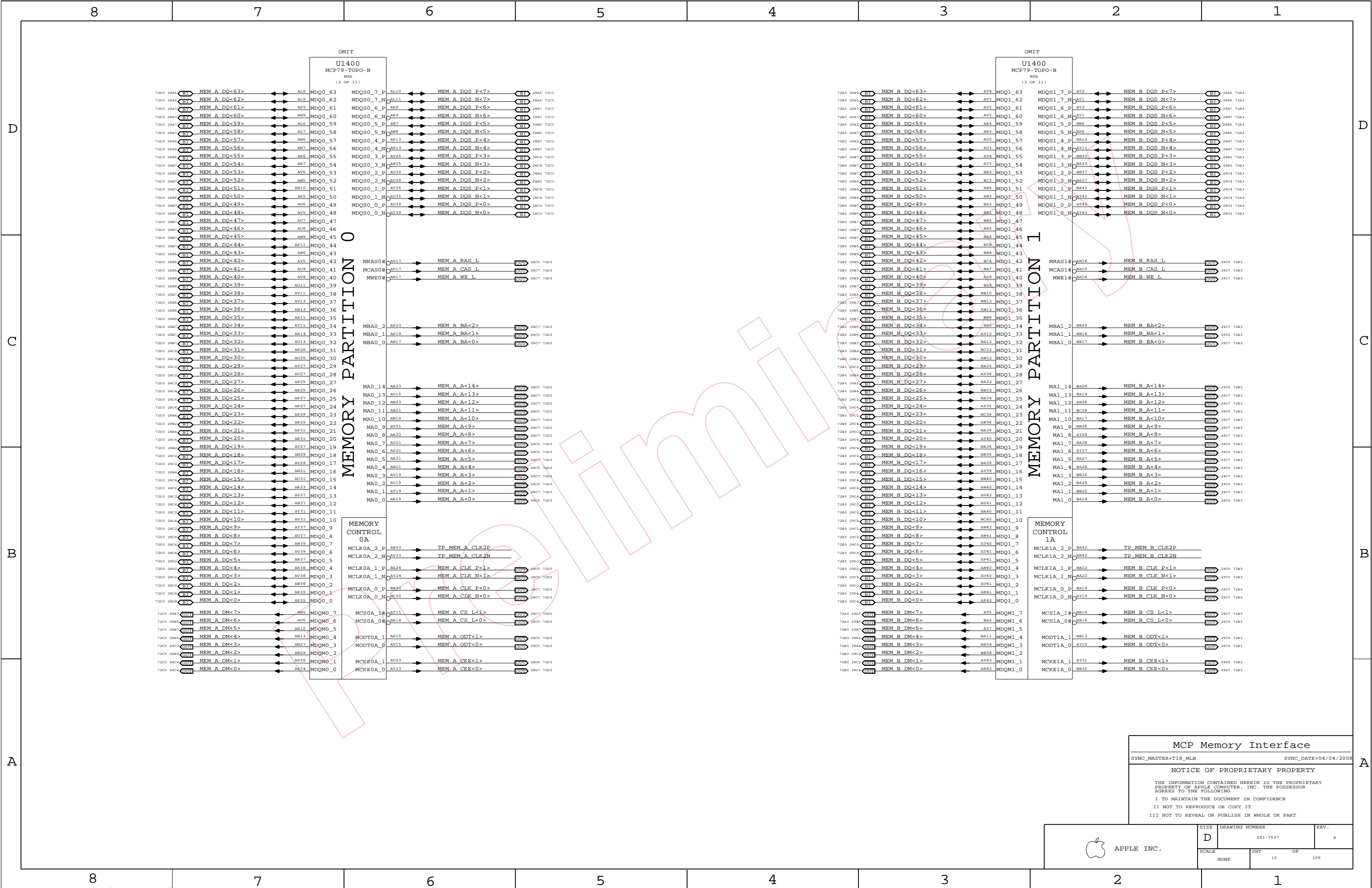


SYNC FROM T18
CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625
RENAME JTAG_MCP_TDO TO JTAG_MCP_TDO_CONN
RENAME XDP_TDO TO XDP_TDO_CONN

eXtended Debug Port (XDP)	
SYNC_MASTER=T18_MLB	SYNC_DATE=12/12/2007
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SCALE		SHT	OF
NONE		13	109





MCP Memory Interface

SYNC_MASTER=T18_MLB

SYNC_DATE=04/04/2008

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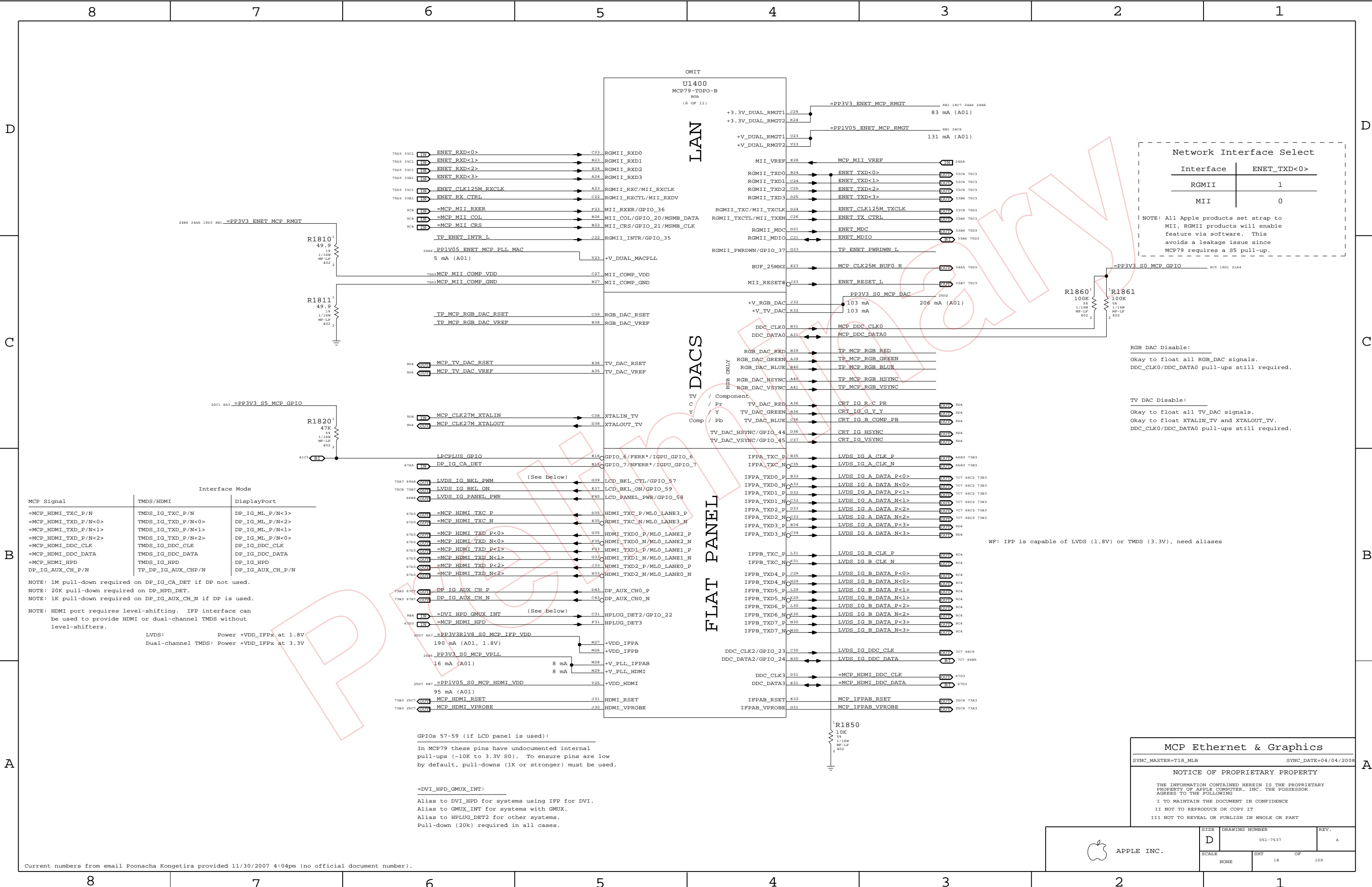
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SCALE		SHT	OF
NONE		15	109



Network Interface Select	
Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: _____
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable: _____
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

Interface Mode		
MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

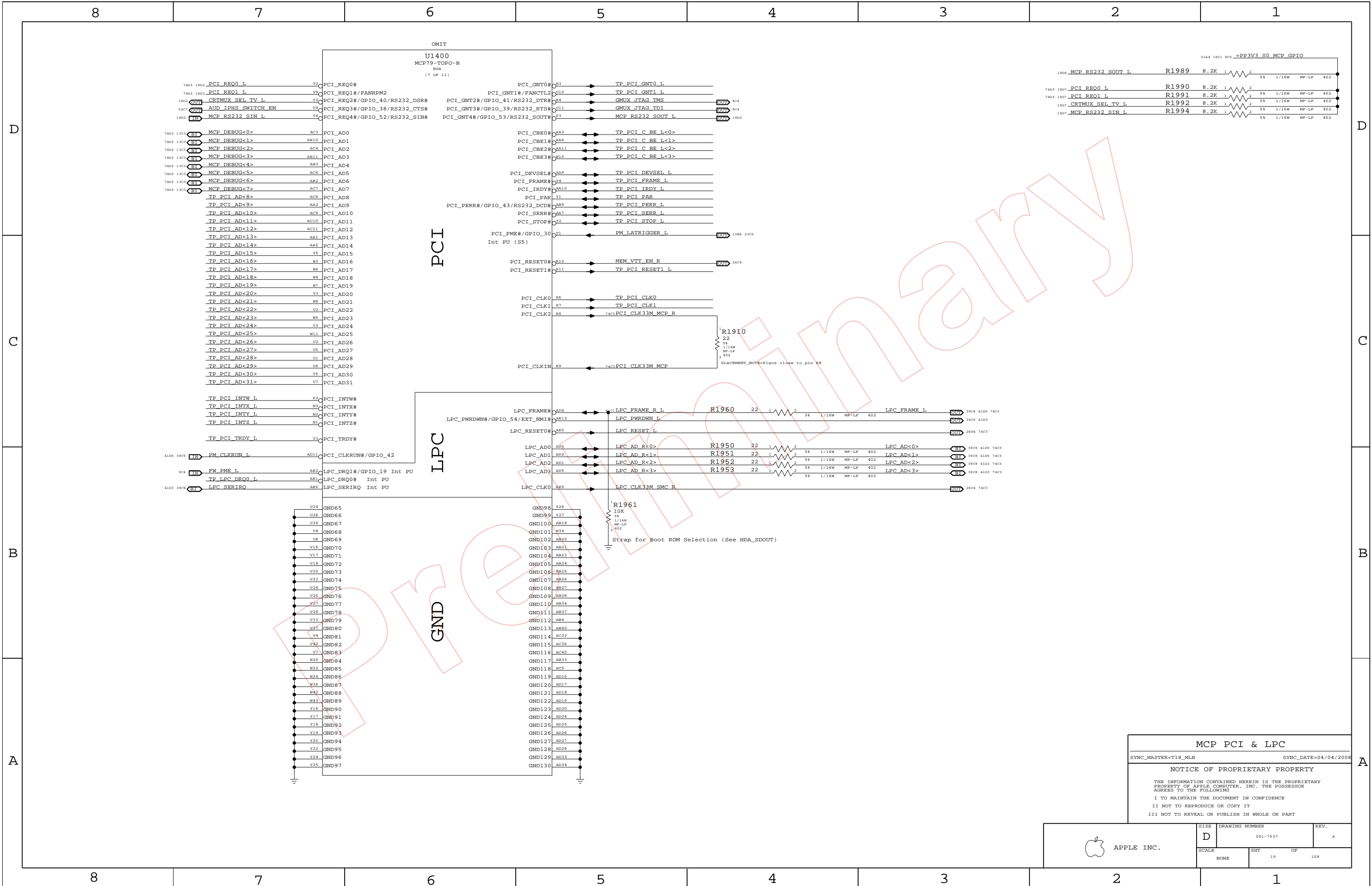
LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):
In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:
Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

MCP Ethernet & Graphics	
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MCP PCI & LPC

SYNC_MASTER=T18_MLB

SYNC_DATE=04/04/2008


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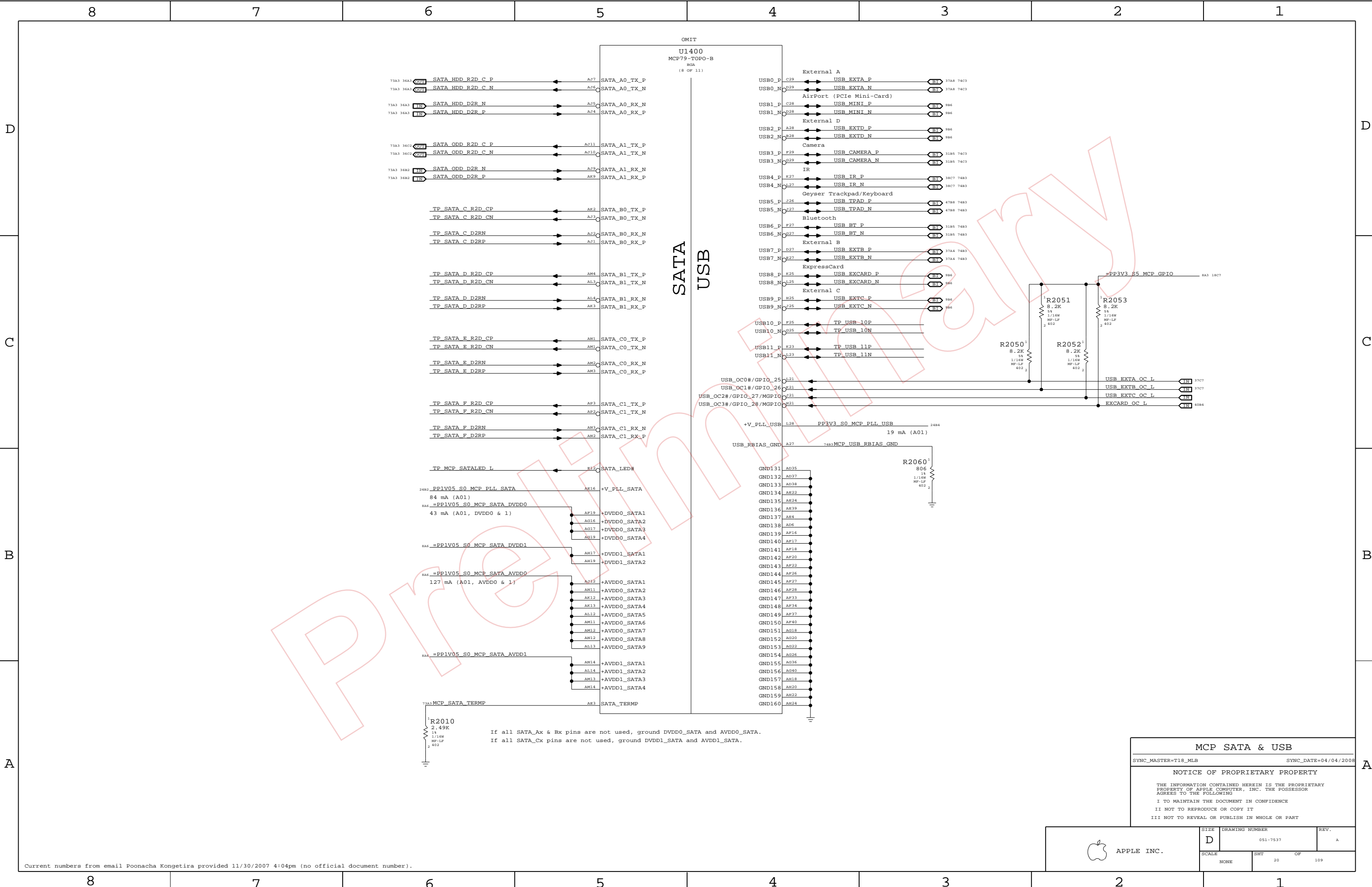
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NONE		19	109

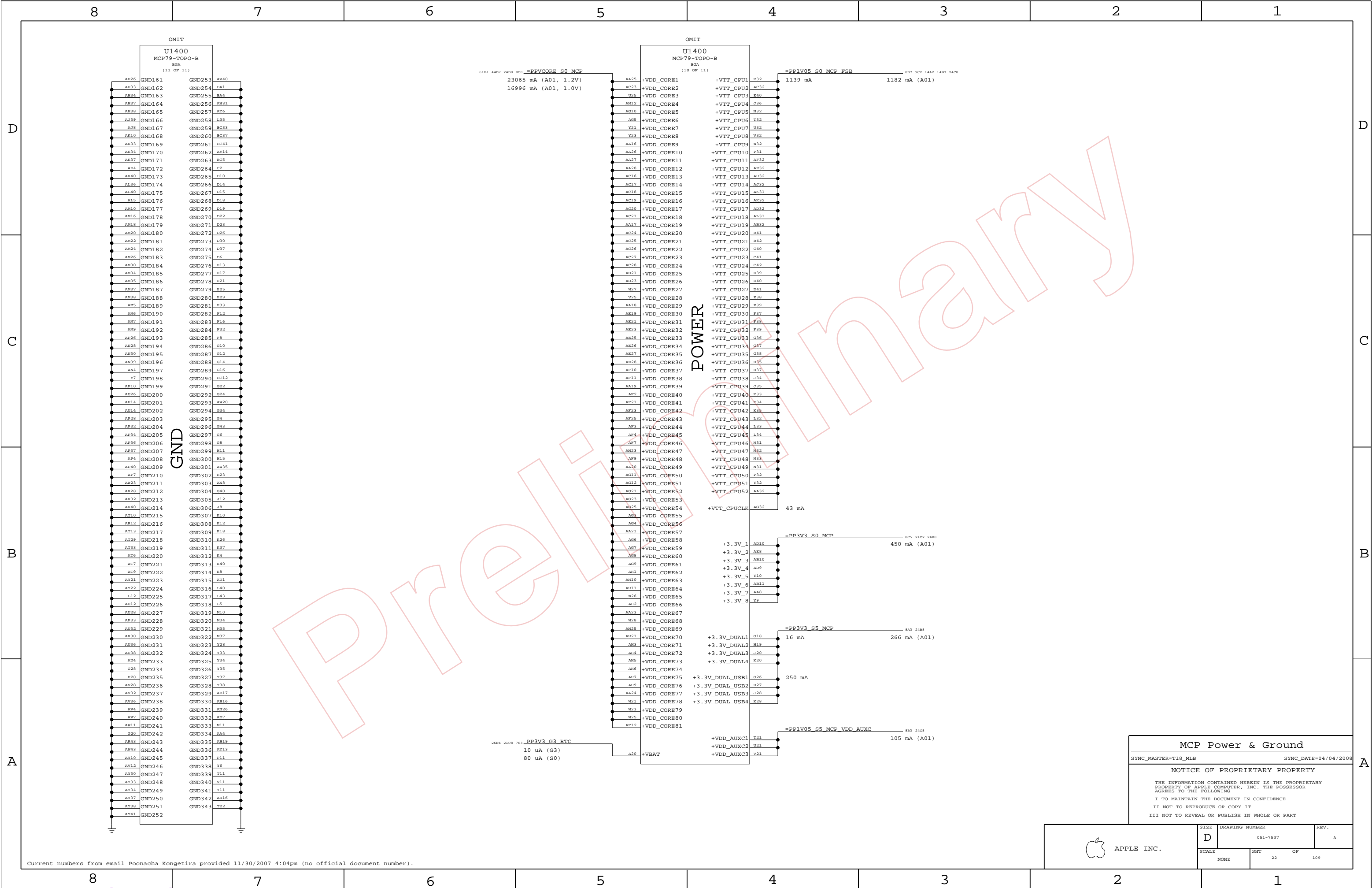


If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

MCP SATA & USB		
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MCP Power & Ground

SYNC_MASTER=T18_MLB

SYNC_DATE=04/04/2008


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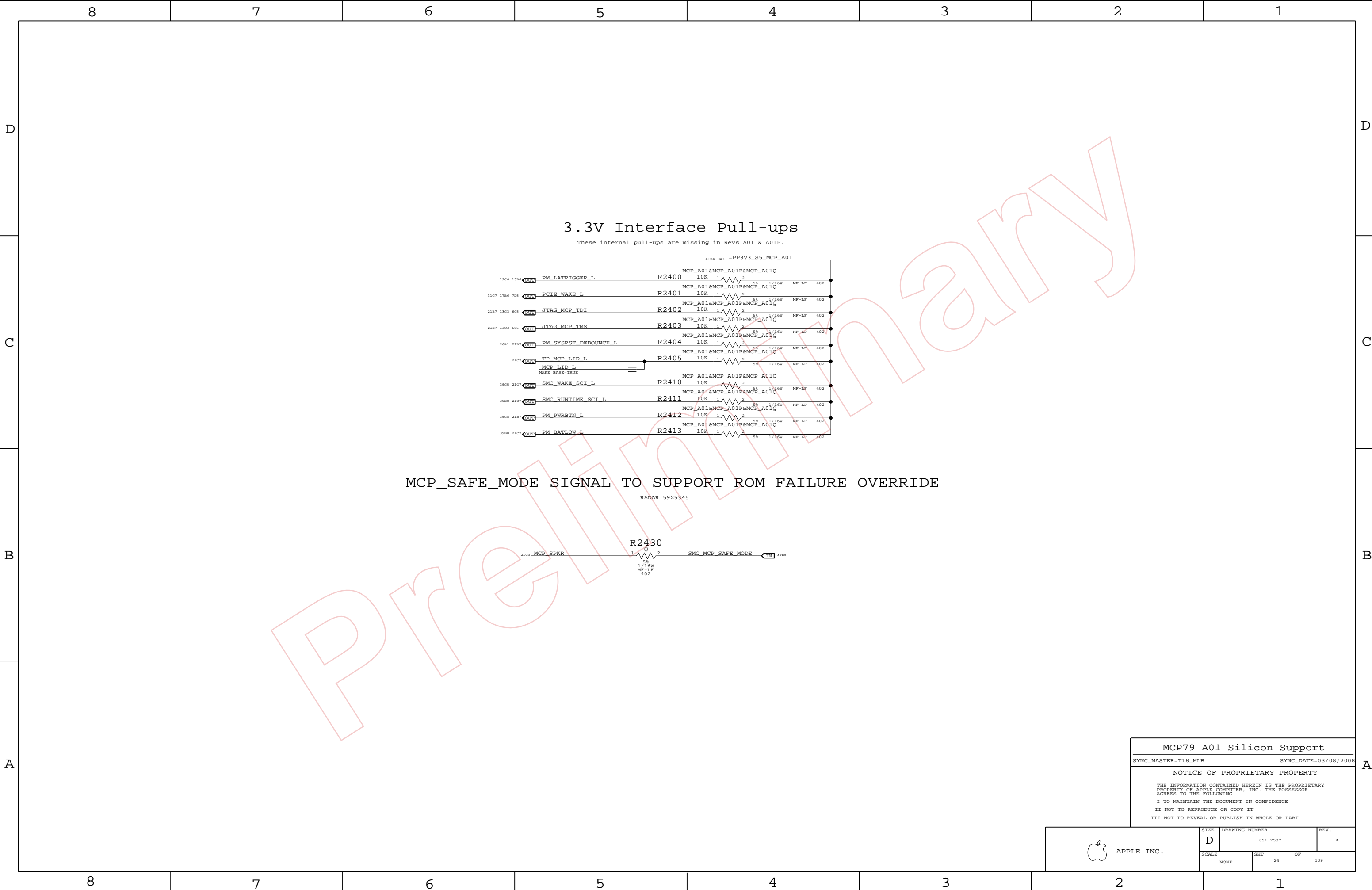
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MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB

SYNC_DATE=03/08/2008


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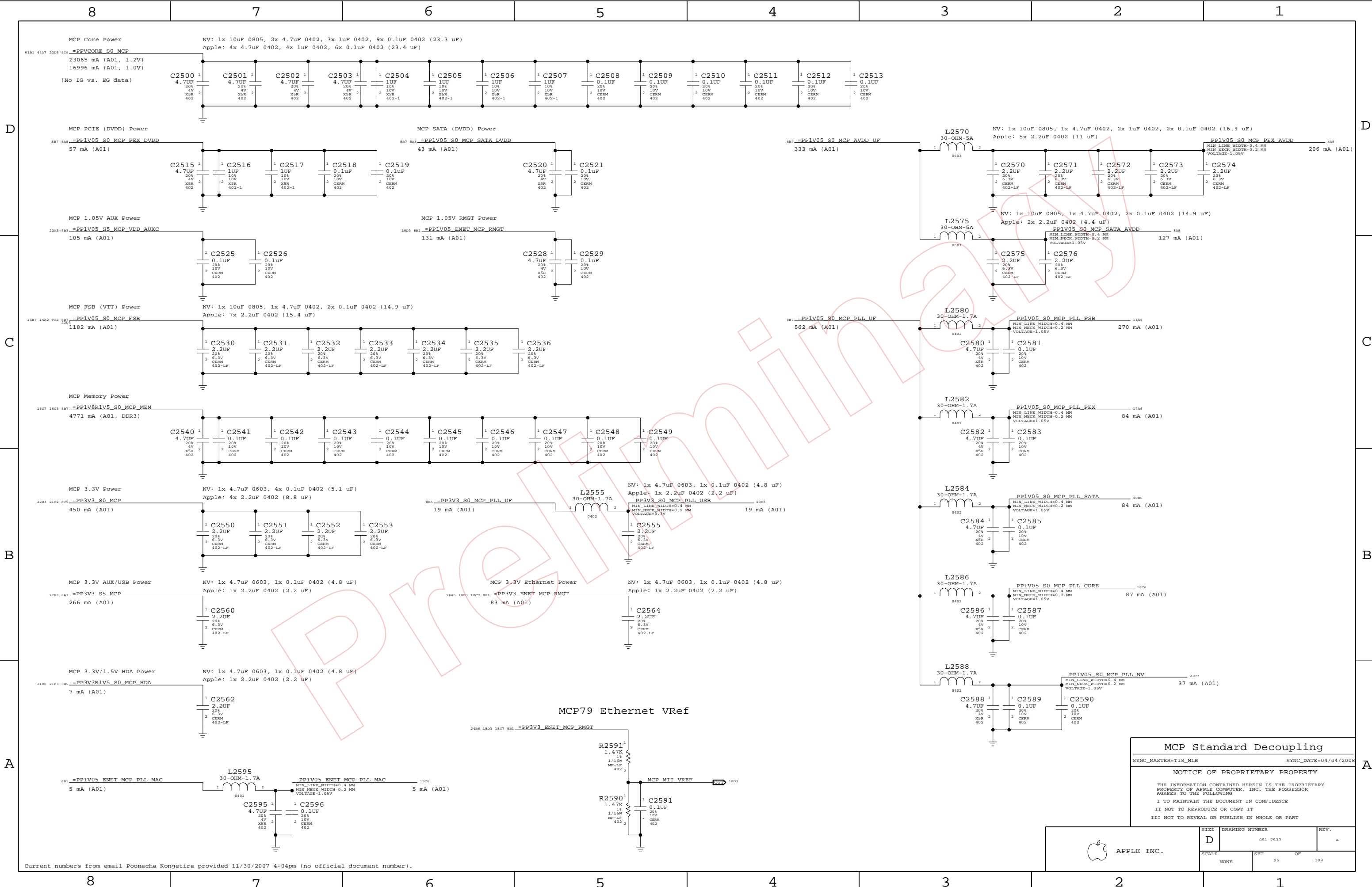
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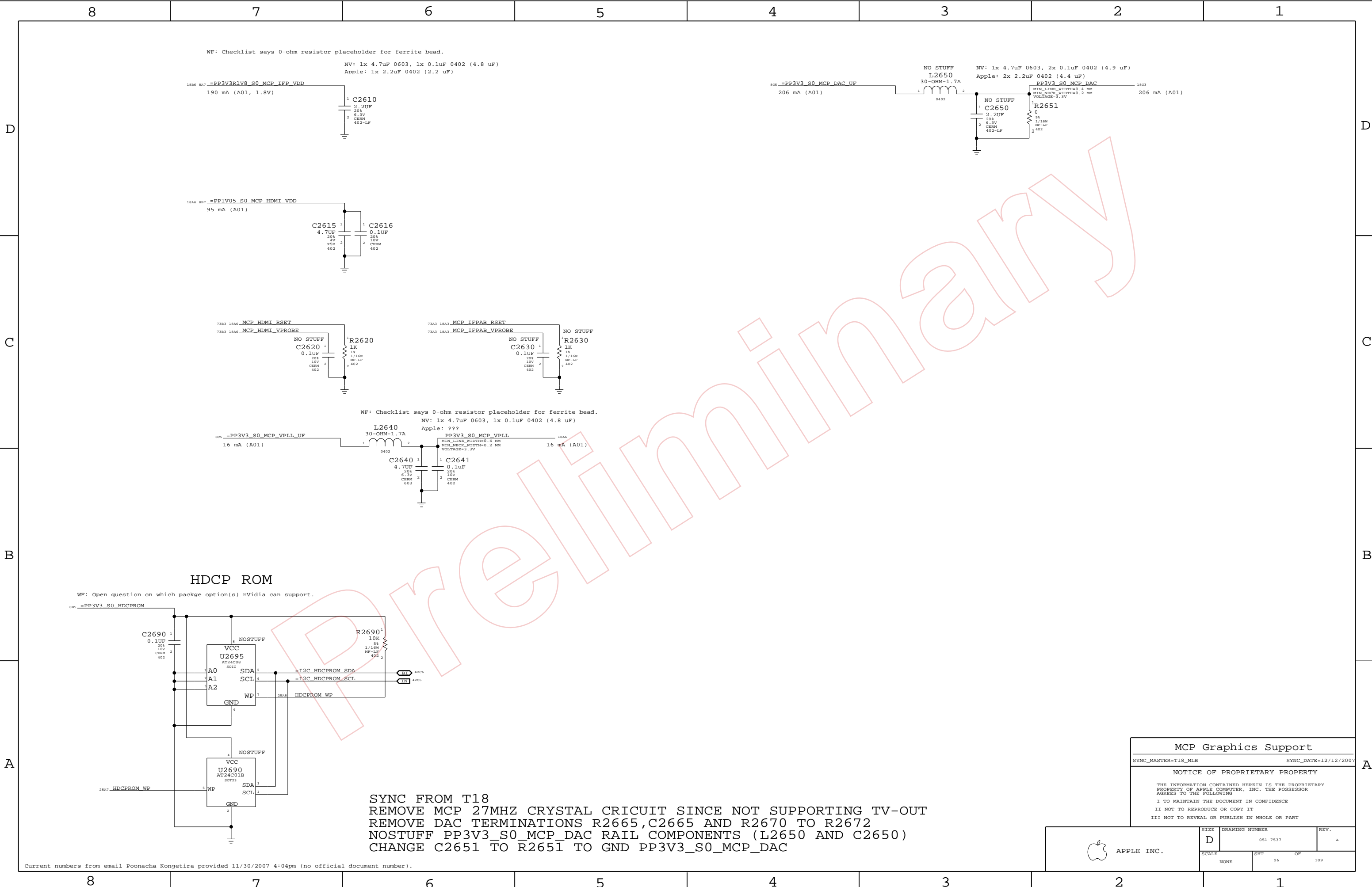
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	D	051-7537	A
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NONE	24 109		





SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CRICUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665,C2665 AND R2670 TO R2672
NOSTUFF PP3V3_S0_MCP_DAC RAIL COMPONENTS (L2650 AND C2650)
CHANGE C2651 TO R2651 TO GND PP3V3_S0_MCP_DAC

MCP Graphics Support		
SYNC_MASTER=T18_MLB		SYNC_DATE=12/12/2007
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		26	109

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

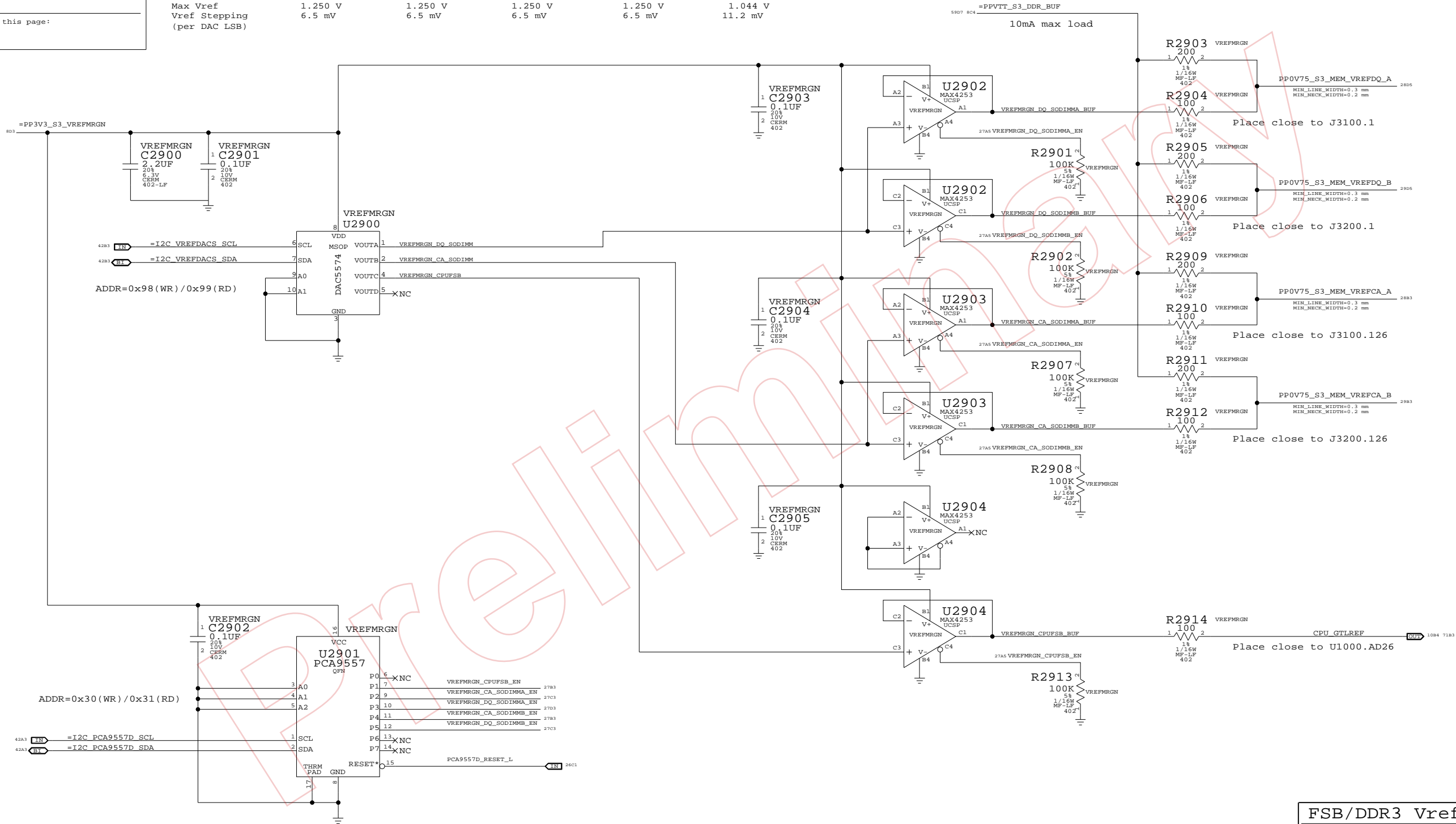
Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel
Min DAC code
Max DAC code
Max sink I
Max source I
Nominal Vref
Min Vref
Max Vref
Vref Stepping
(per DAC LSB)

MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
A	B	A	B	C
0x00	0x00	0x00	0x00	0x00
0x87	0x87	0x87	0x87	0x55
-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
5 mA	5 mA	5 mA	5 mA	0.52 mA
0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining

SYNC_MASTER=BEN SYNC_DATE=03/31/2008

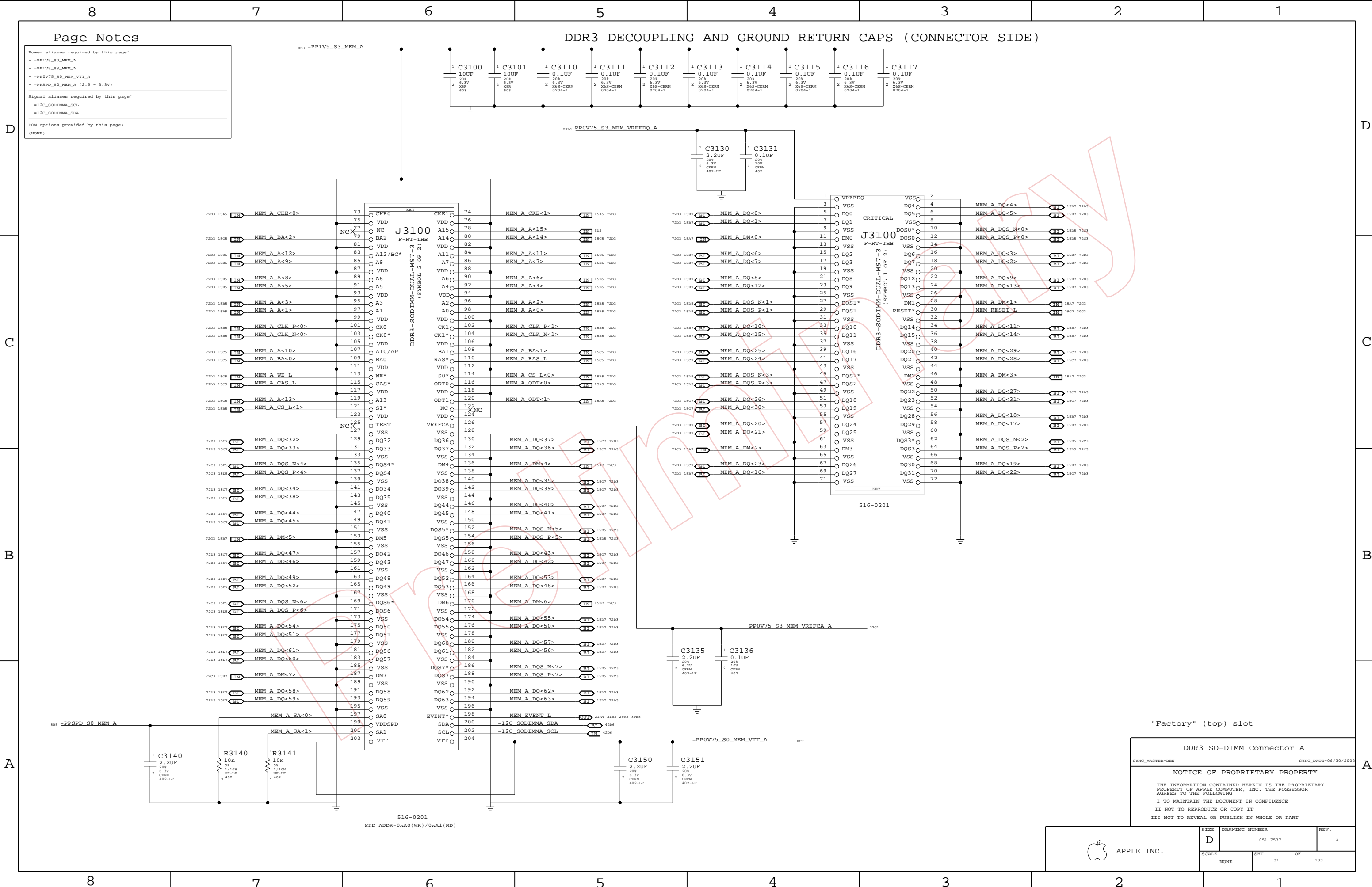
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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	29	109



Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=BIN SYNC_DATE=06/30/2008

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Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

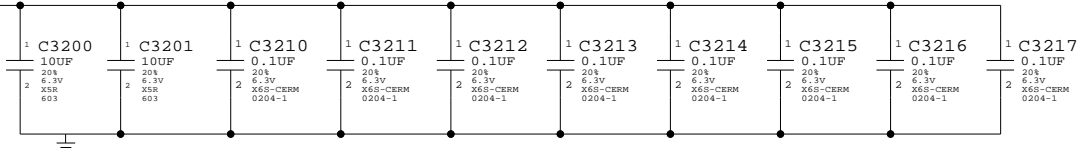
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:

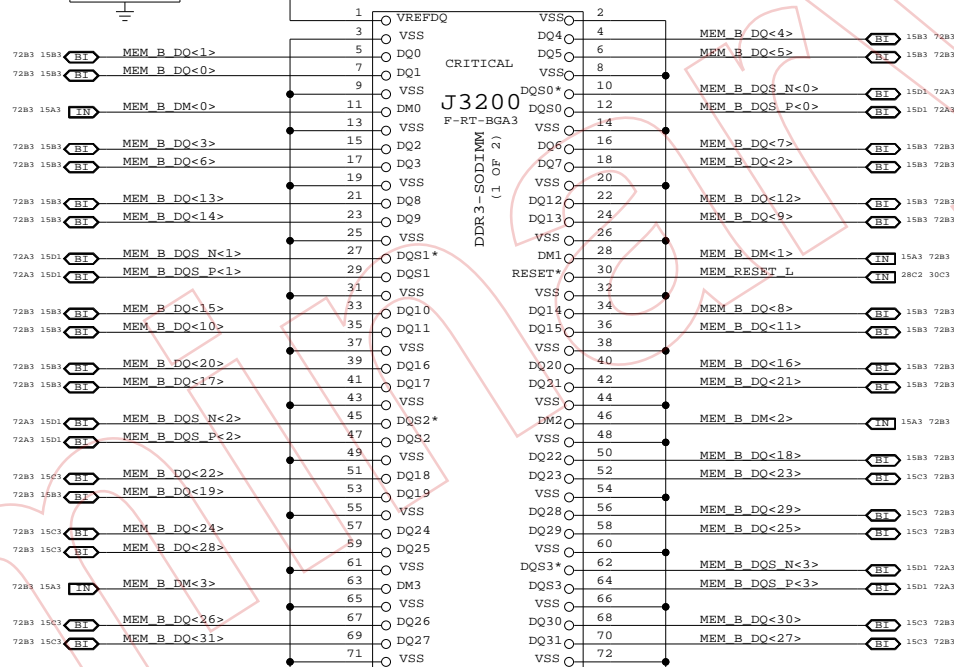
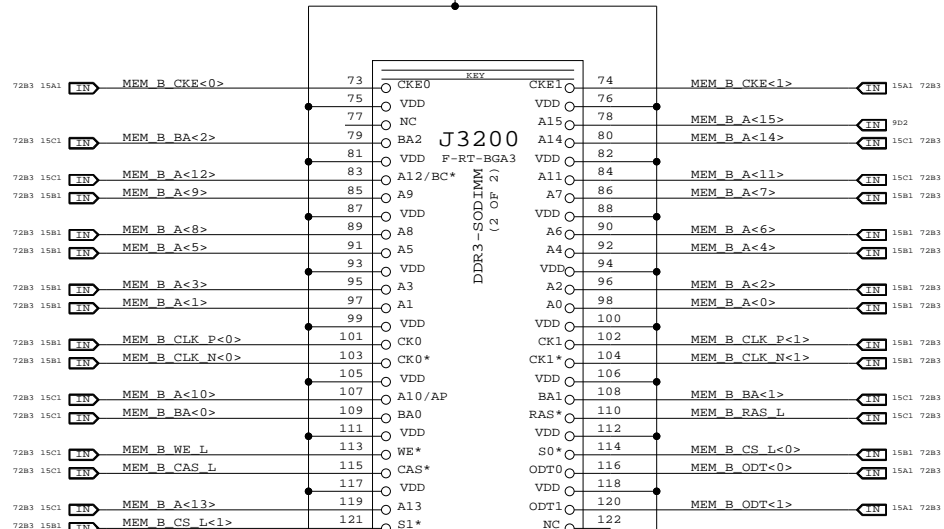
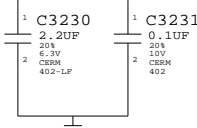
(NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)

803 =PP1V5_S3_MEM_B



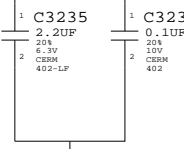
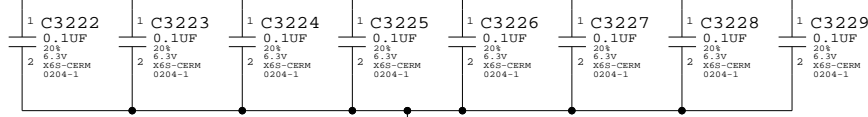
2701 PP0V75_S3_MEM_VREFDQ_B



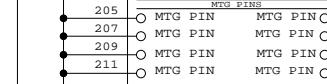
516S0706

DDR3 GROUND RETURN CAPS (MCP SIDE)

887 =PP1V5_S0_MEM_MCP



885 =PPSPD_S0_MEM_B



"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B

SYNC_MASTER=BBN SYNC_DATE=05/09/2008

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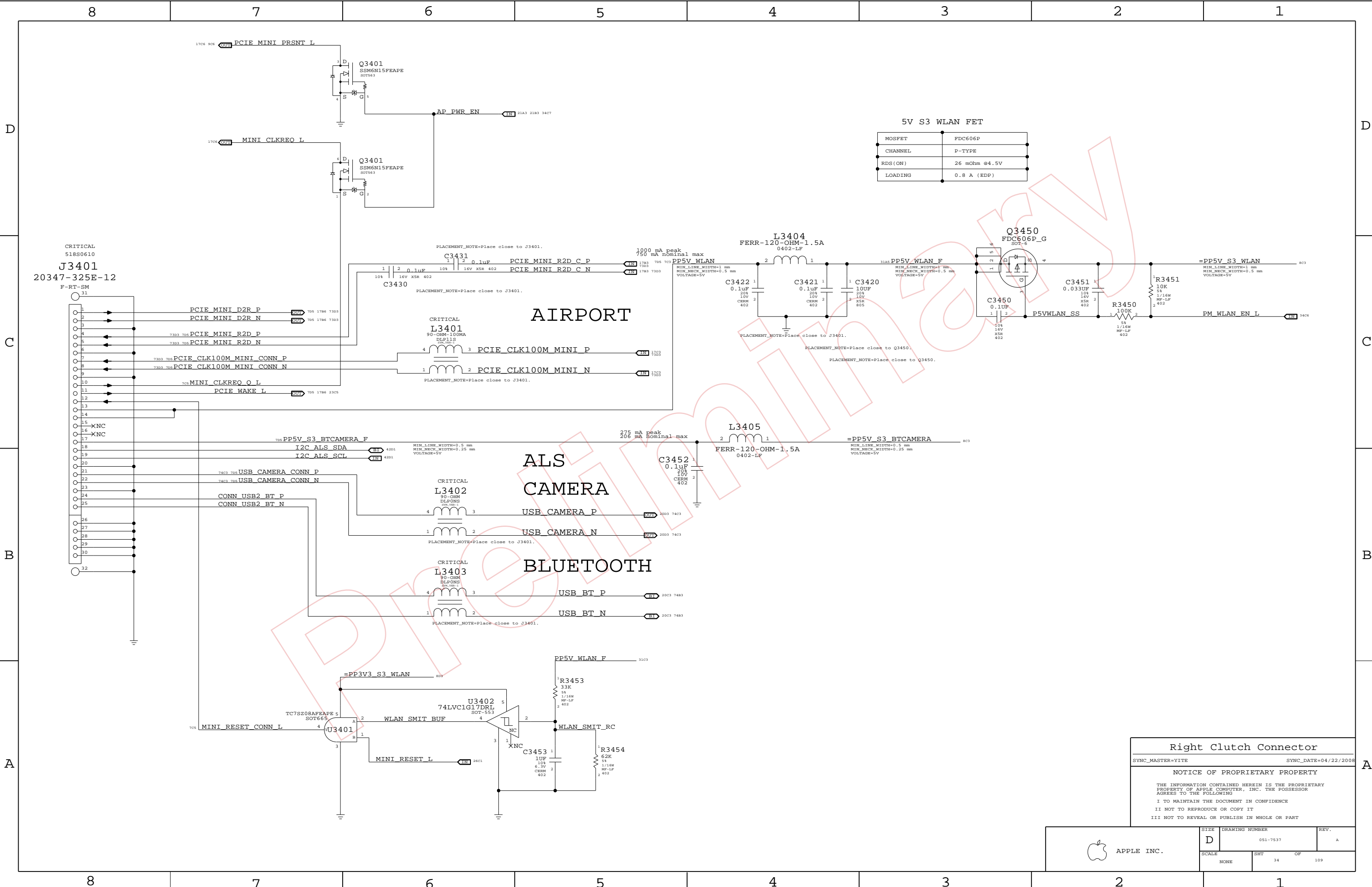
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APPLE INC.

SIZE D DRAWING NUMBER 051-7537 REV. A

SCALE NONE SHT 32 OF 109



5V S3 WLAN FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

Right Clutch Connector

SYNC_MASTER=YITE SYNC_DATE=04/22/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		34	109

D

C

B

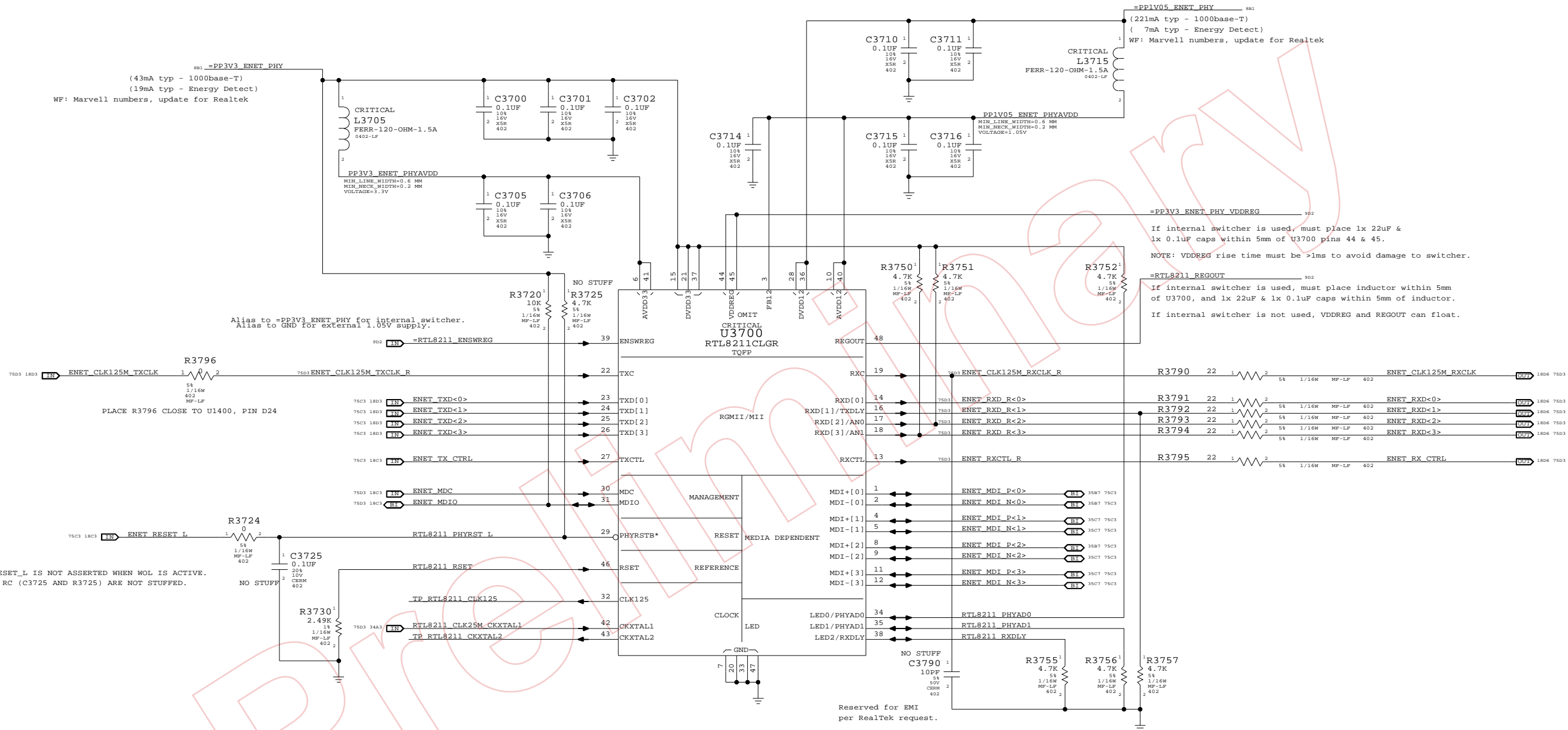
A

D

C

B

A



Configuration Settings:
PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)

SYNC_MASTER=SUMA

SYNC_DATE=05/23/2008

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APPLE INC.

SIZE
D

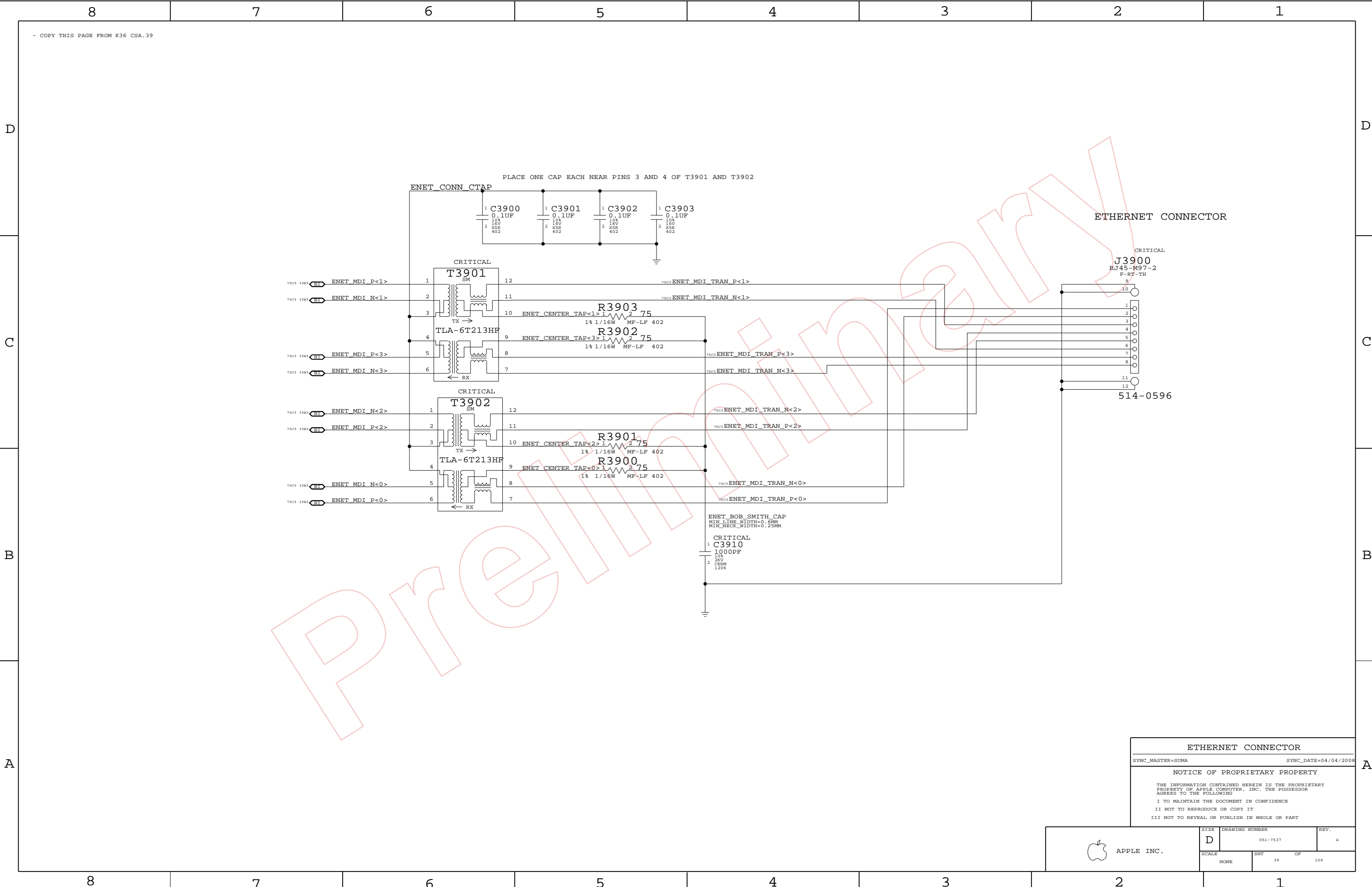
DRAWING NUMBER
051-7537

REV.
A


SCALE
NONE

SHT
37

OF
109



ETHERNET CONNECTOR		
SYNC_MASTER=SUMA		SYNC_DATE=04/04/2008
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 APPLE INC.	SIZE D	DRAWING NUMBER 051-7537	REV. A
	SCALE NONE	SHT 39	OF 109

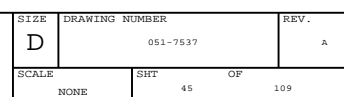
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C

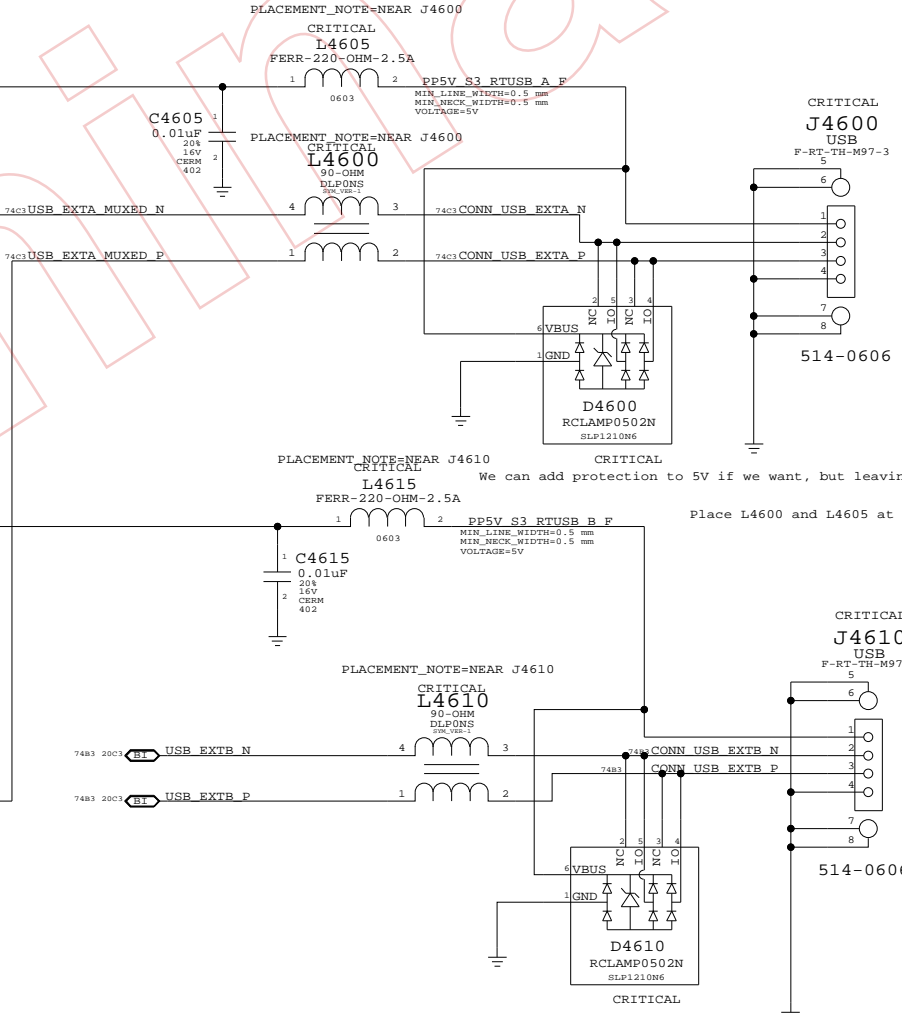
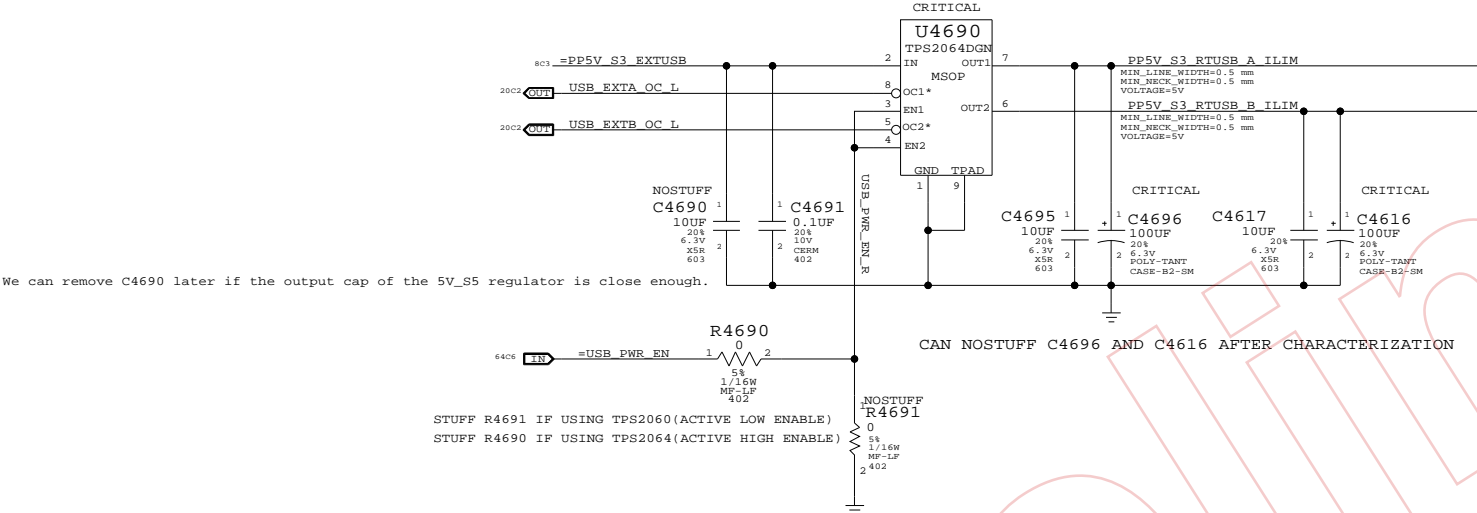


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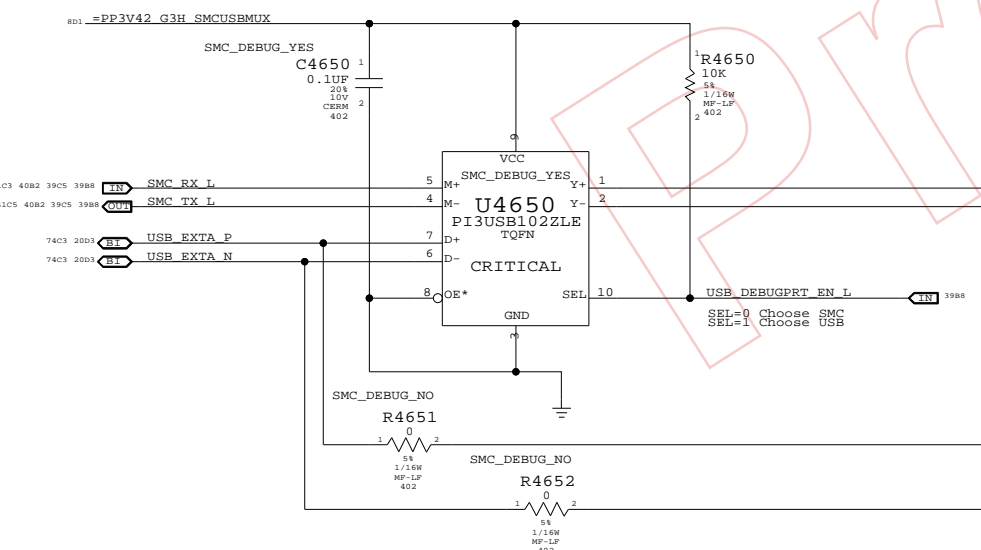
A

Port Power Switch

USB PORT A (FRONT PORT)



USB/SMC Debug Mux



USB PORT B (BACK PORT)

External USB Connectors

SYNC_MASTER=YUAN.MA SYNC_DATE=01/18/2008

NOTICE OF PROPRIETARY PROPERTY

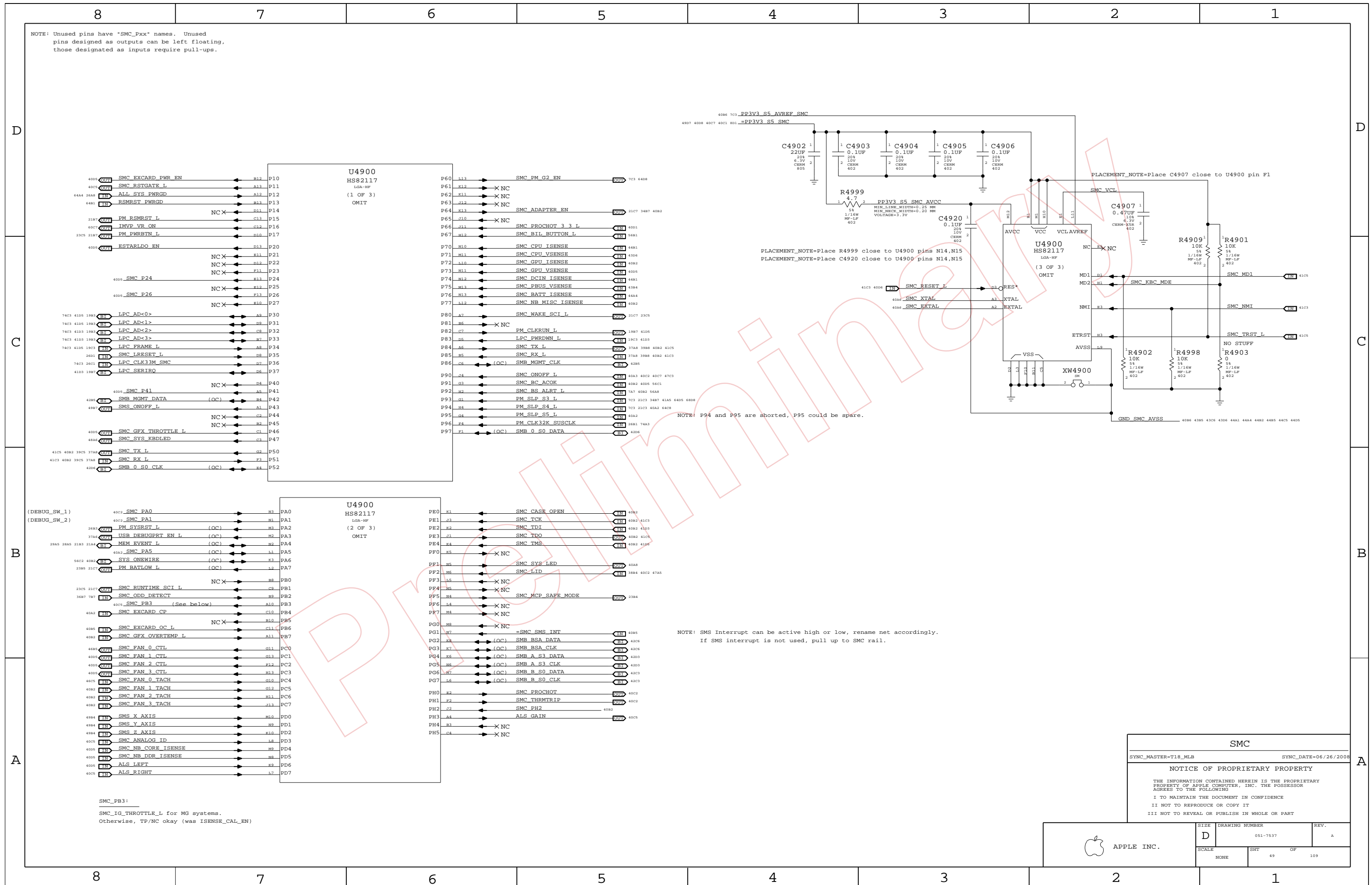
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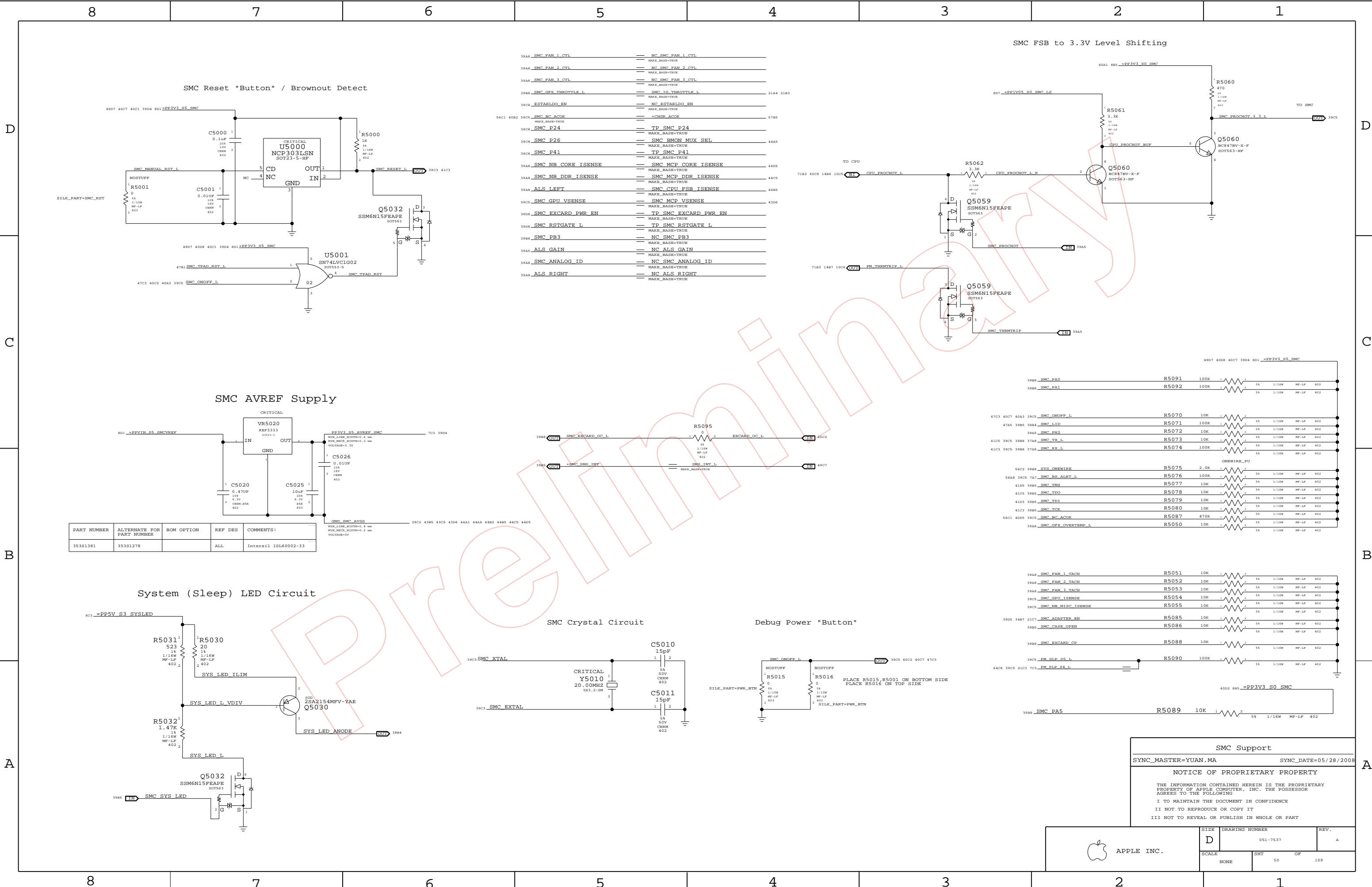
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II NOT TO REPRODUCE OR COPY IT

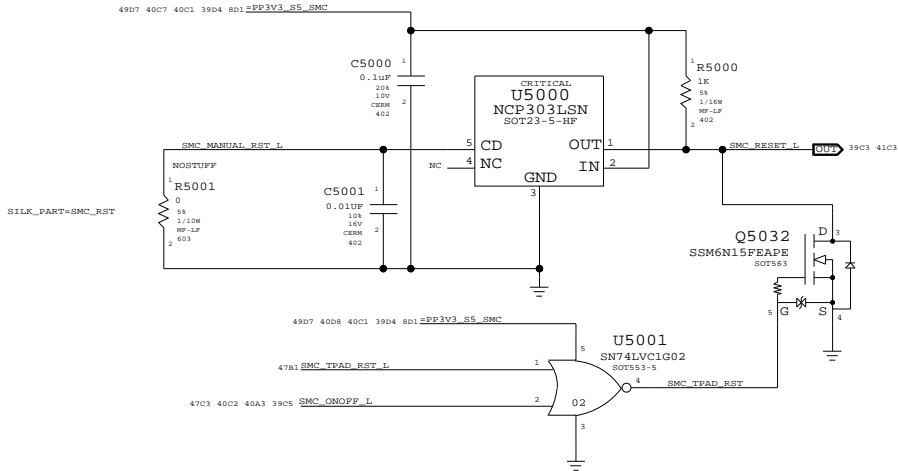
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		46	109

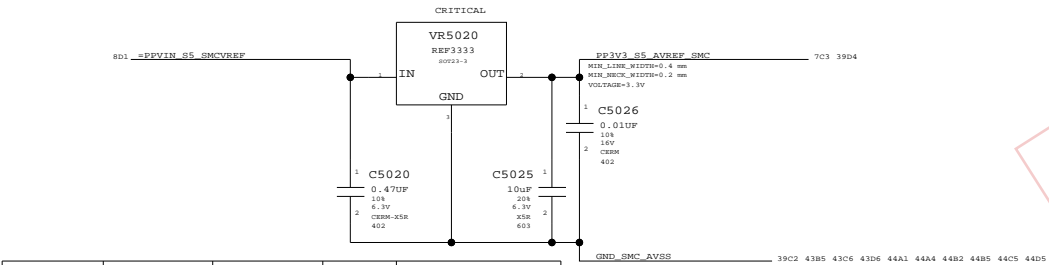




SMC Reset "Button" / Brownout Detect

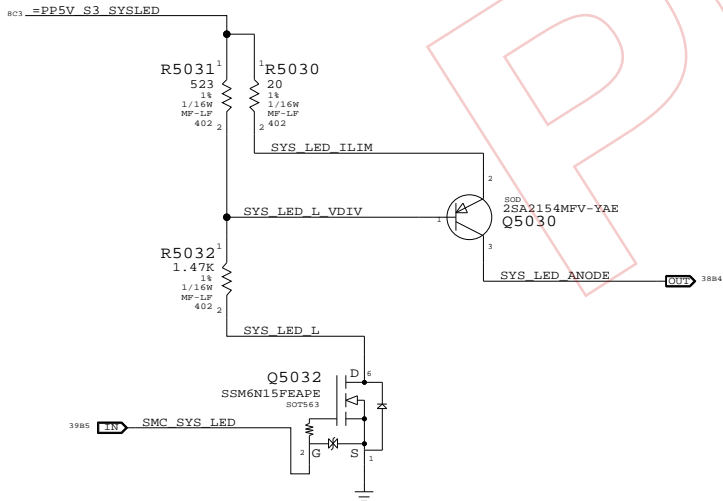


SMC AVREF Supply

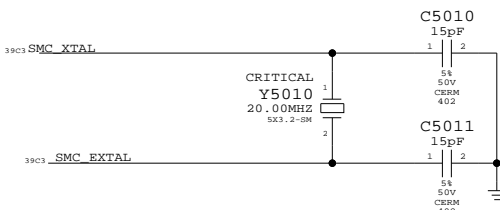


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Intersil ISL60002-33

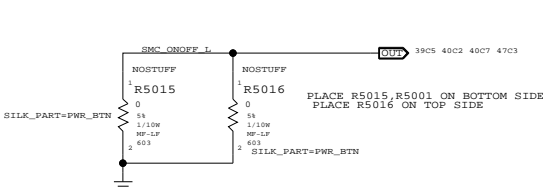
System (Sleep) LED Circuit



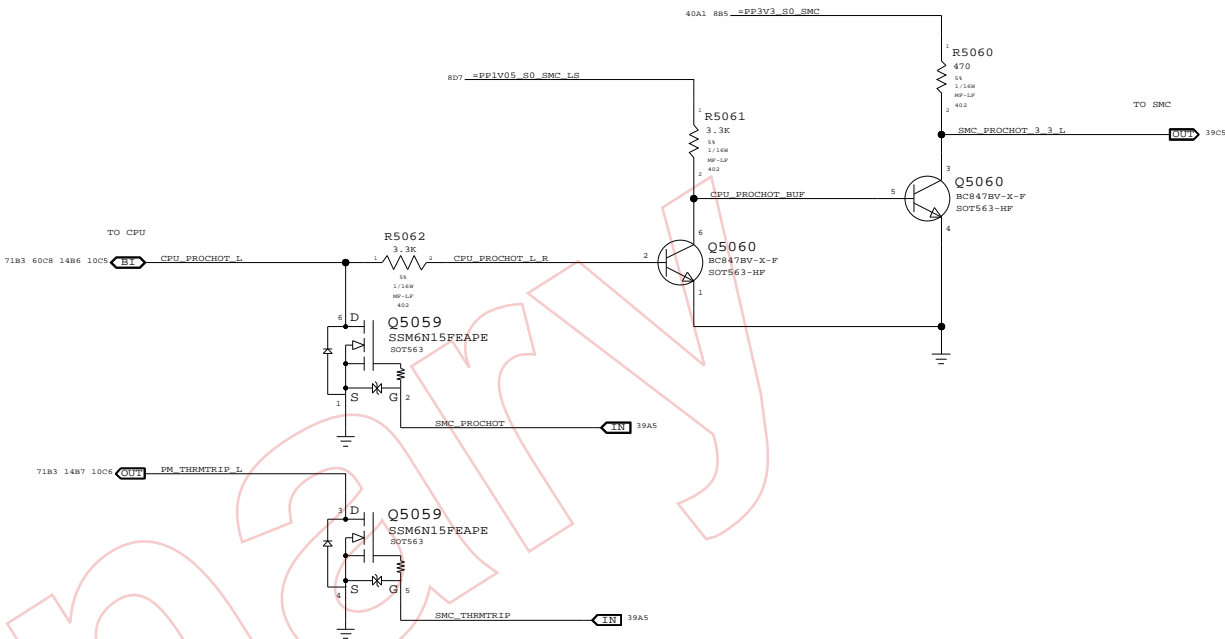
SMC Crystal Circuit



Debug Power "Button"



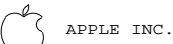
SMC FSB to 3.3V Level Shifting



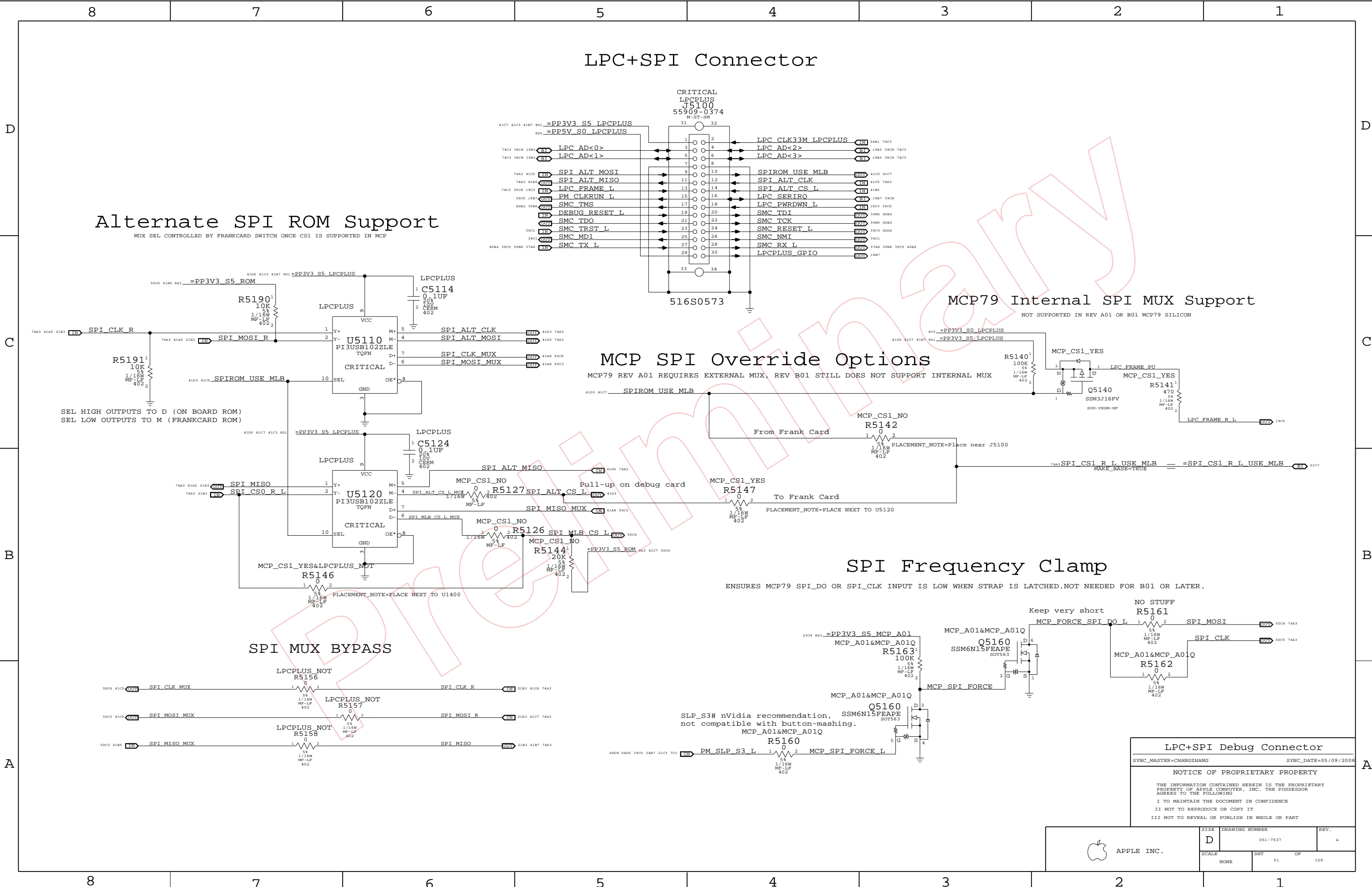
4907 4008 4001 3904 801=PP3V3_S5_SMC	R5091	100K	1	5	5	1/16W	NP-LF	402
3988 SMC_PA0	R5092	100K	1	5	5	1/16W	NP-LF	402
4703 4007 40A3 39C5 SMC_ONOFF_L	R5070	10K	1	5	5	1/16W	NP-LF	402
47A5 3985 3884 SMC_LID	R5071	100K	1	5	5	1/16W	NP-LF	402
39A5 SMC_PH2	R5072	10K	1	5	5	1/16W	NP-LF	402
41C5 39C5 3988 37A8 SMC_TX_L	R5073	10K	1	5	5	1/16W	NP-LF	402
41C3 39C5 3988 37A8 SMC_RX_L	R5074	100K	1	5	5	1/16W	NP-LF	402
56C2 3988 SYS_ONWIRE_RU	R5075	2.0K	1	5	5	1/16W	NP-LF	402
56A8 39C5 7A7 SMC_BS_ALERT_L	R5076	100K	1	5	5	1/16W	NP-LF	402
41D5 3985 SMC_TMS	R5077	10K	1	5	5	1/16W	NP-LF	402
41C5 3985 SMC_TDO	R5078	10K	1	5	5	1/16W	NP-LF	402
41D3 3985 SMC_TDI	R5079	10K	1	5	5	1/16W	NP-LF	402
41C3 3985 SMC_TCK	R5080	10K	1	5	5	1/16W	NP-LF	402
56C1 40D5 39C5 SMC_BC_ACLK	R5087	470K	1	5	5	1/16W	NP-LF	402
39A8 SMC_GFX_OVERTEMP_L	R5050	10K	1	5	5	1/16W	NP-LF	402

39A8 SMC_FAN_1_TACH	R5051	10K	1	5	5	1/16W	NP-LF	402
39A8 SMC_FAN_2_TACH	R5052	10K	1	5	5	1/16W	NP-LF	402
39A8 SMC_FAN_3_TACH	R5053	10K	1	5	5	1/16W	NP-LF	402
39C5 SMC_GPU_ISENSE	R5054	10K	1	5	5	1/16W	NP-LF	402
39C5 SMC_NB_MISC_ISENSE	R5055	10K	1	5	5	1/16W	NP-LF	402
39D5 3487 21C7 SMC_ADAPTER_EN	R5085	10K	1	5	5	1/16W	NP-LF	402
3985 SMC_CASE_OPEN	R5086	10K	1	5	5	1/16W	NP-LF	402
3988 SMC_EXCARD_CP	R5088	10K	1	5	5	1/16W	NP-LF	402
39C5 PM_SLP_S5_L	R5090	100K	1	5	5	1/16W	NP-LF	402
64C8 39C5 21C3 7C3 PM_SLP_S4_L	R5089	10K	1	5	5	1/16W	NP-LF	402

SMC Support
SYNC_MASTER=YUAN.MA SYNC_DATE=05/28/2008
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SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	50	109



LPC+SPI Connector

Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP

MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

SPI Frequency Clamp

ENSURES MCP79 SPI_DO OR SPI_CLK INPUT IS LOW WHEN STRAP IS LATCHED. NOT NEEDED FOR B01 OR LATER.

SPI MUX BYPASS

LPC+SPI Debug Connector

SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

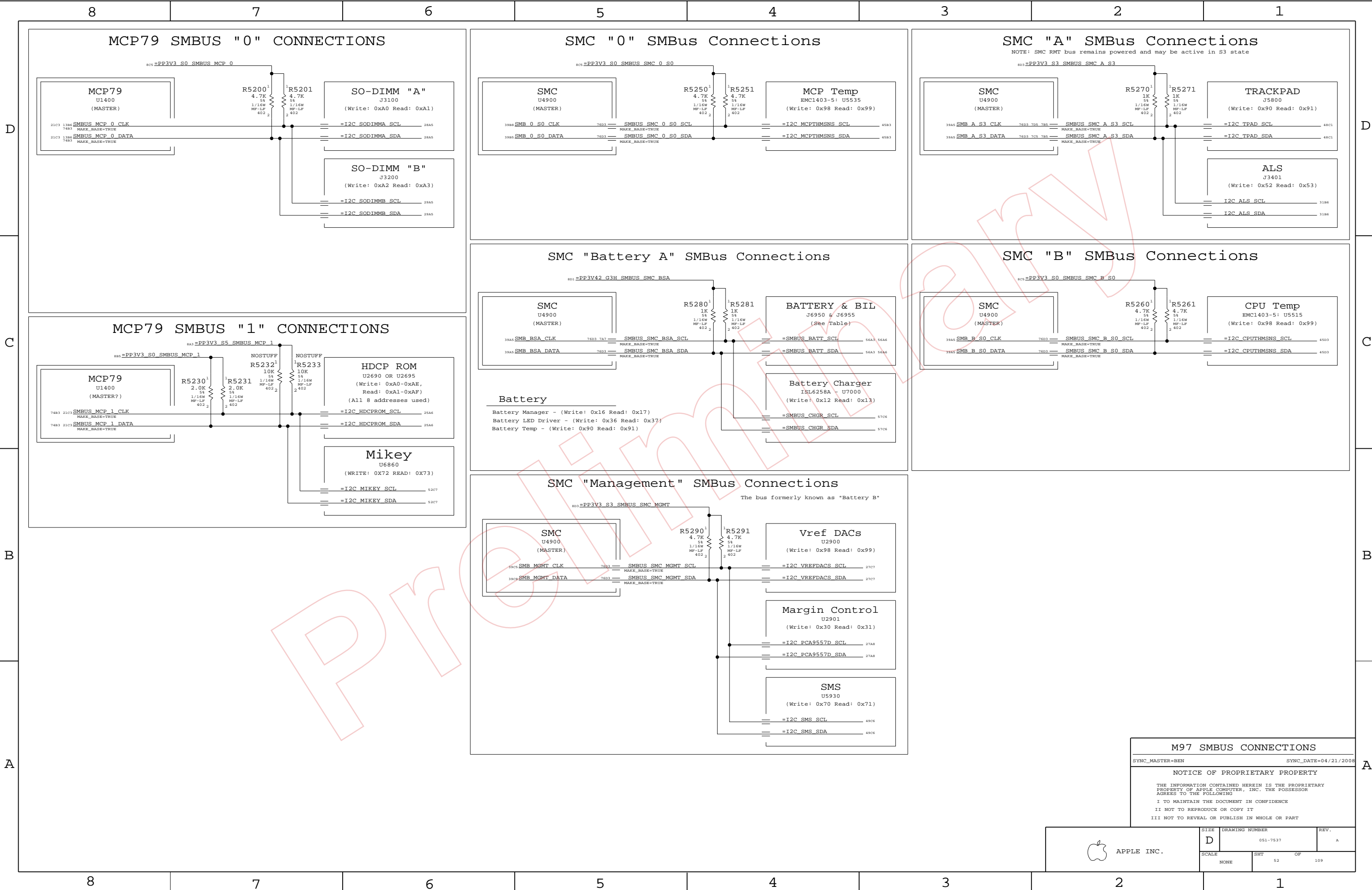
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APPLE INC.

SIZE	D	DRAWING NUMBER	051-7537	REV.	A
SCALE	NONE	SHT	51	OF	109



M97 SMBUS CONNECTIONS

SYNC_MASTER=BEN SYNC_DATE=04/21/2008

NOTICE OF PROPRIETARY PROPERTY

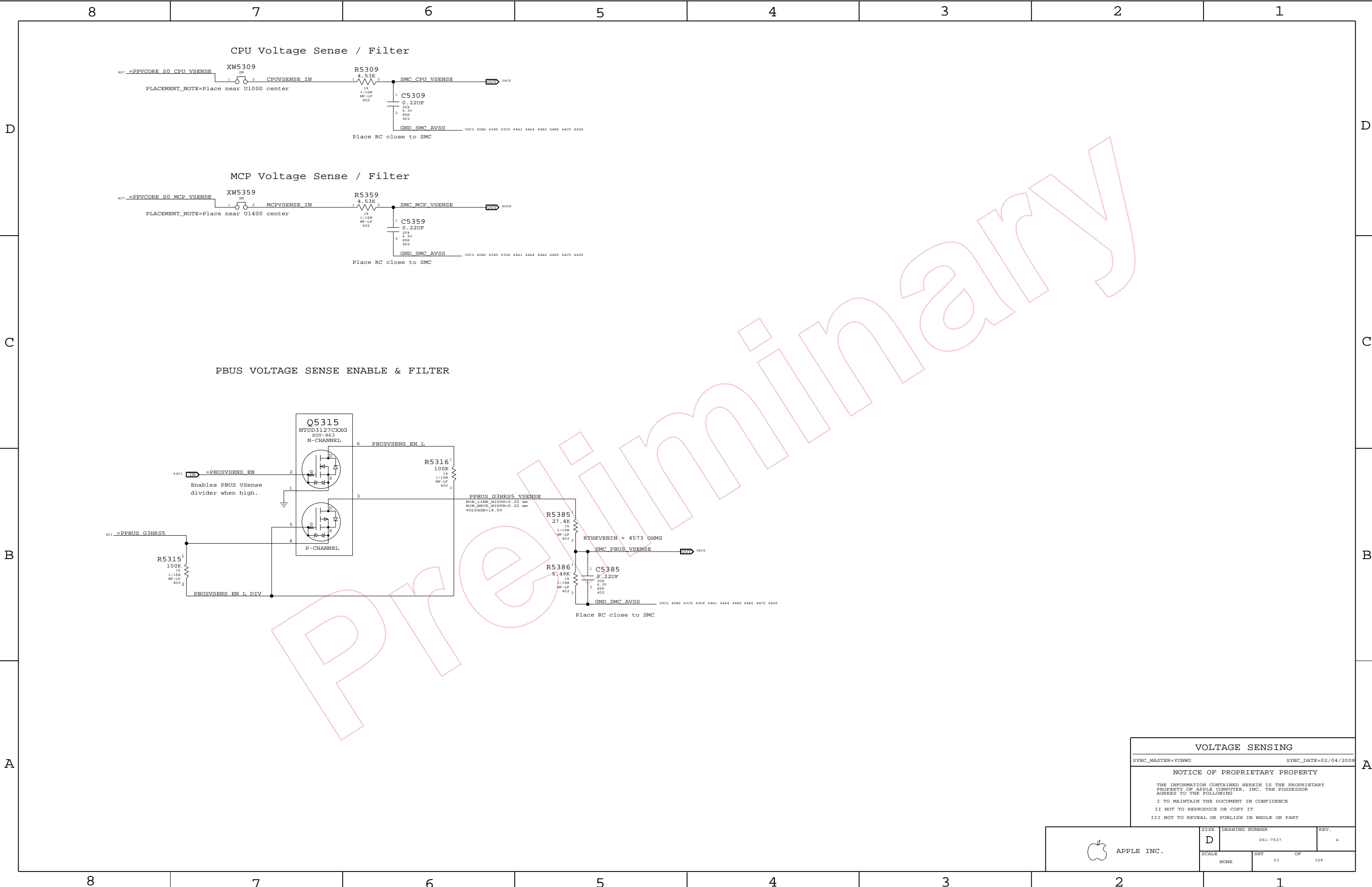
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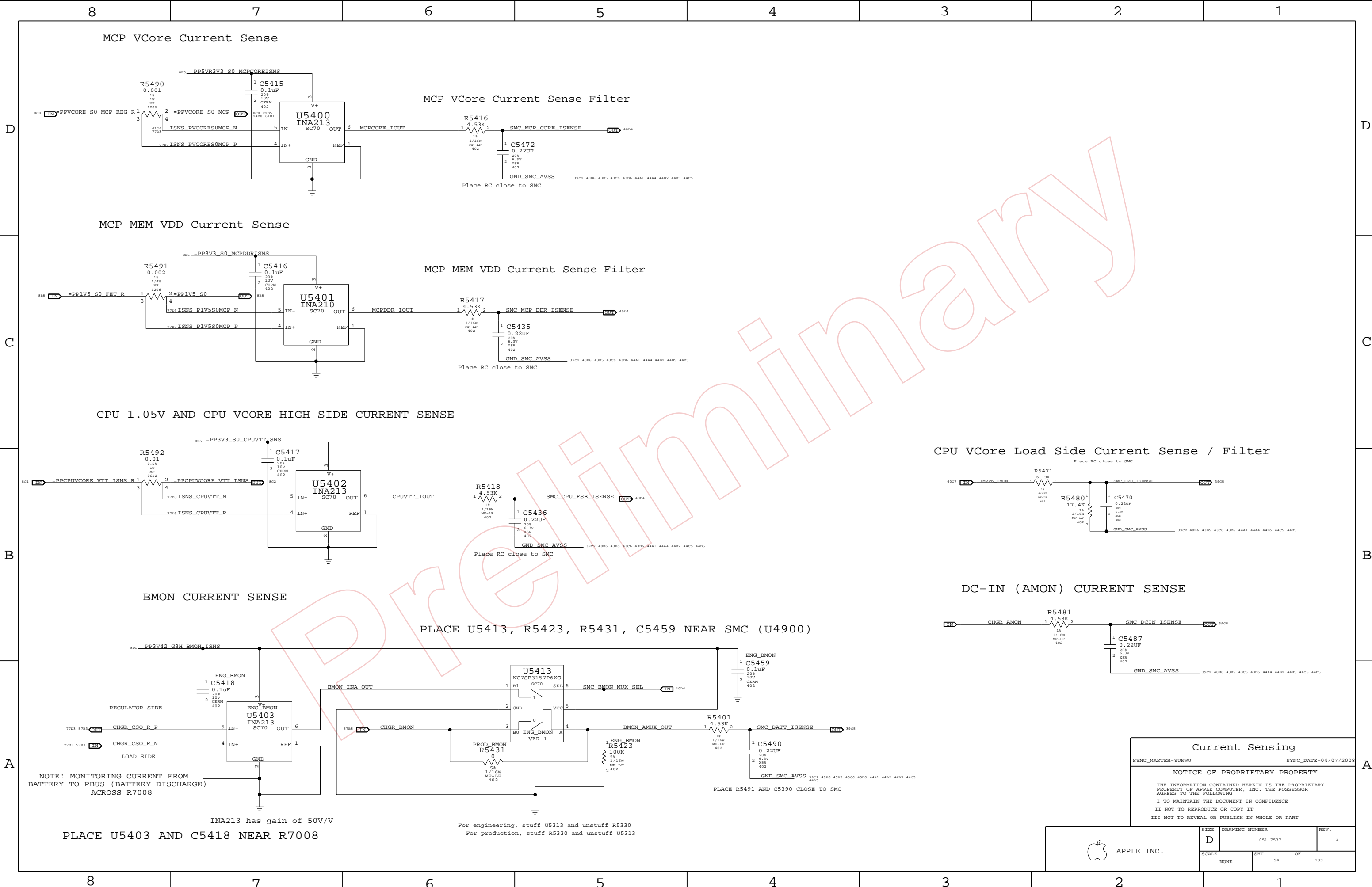
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		52	109



VOLTAGE SENSING		
SYNC_MASTER=YUNWU		SYNC_DATE=02/04/2008
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	D	051-7537	A
SCALE		SHT	OF
NONE		53	109



Current Sensing

SYNC_MASTER=YUNWU SYNC_DATE=04/07/2008

NOTICE OF PROPRIETARY PROPERTY

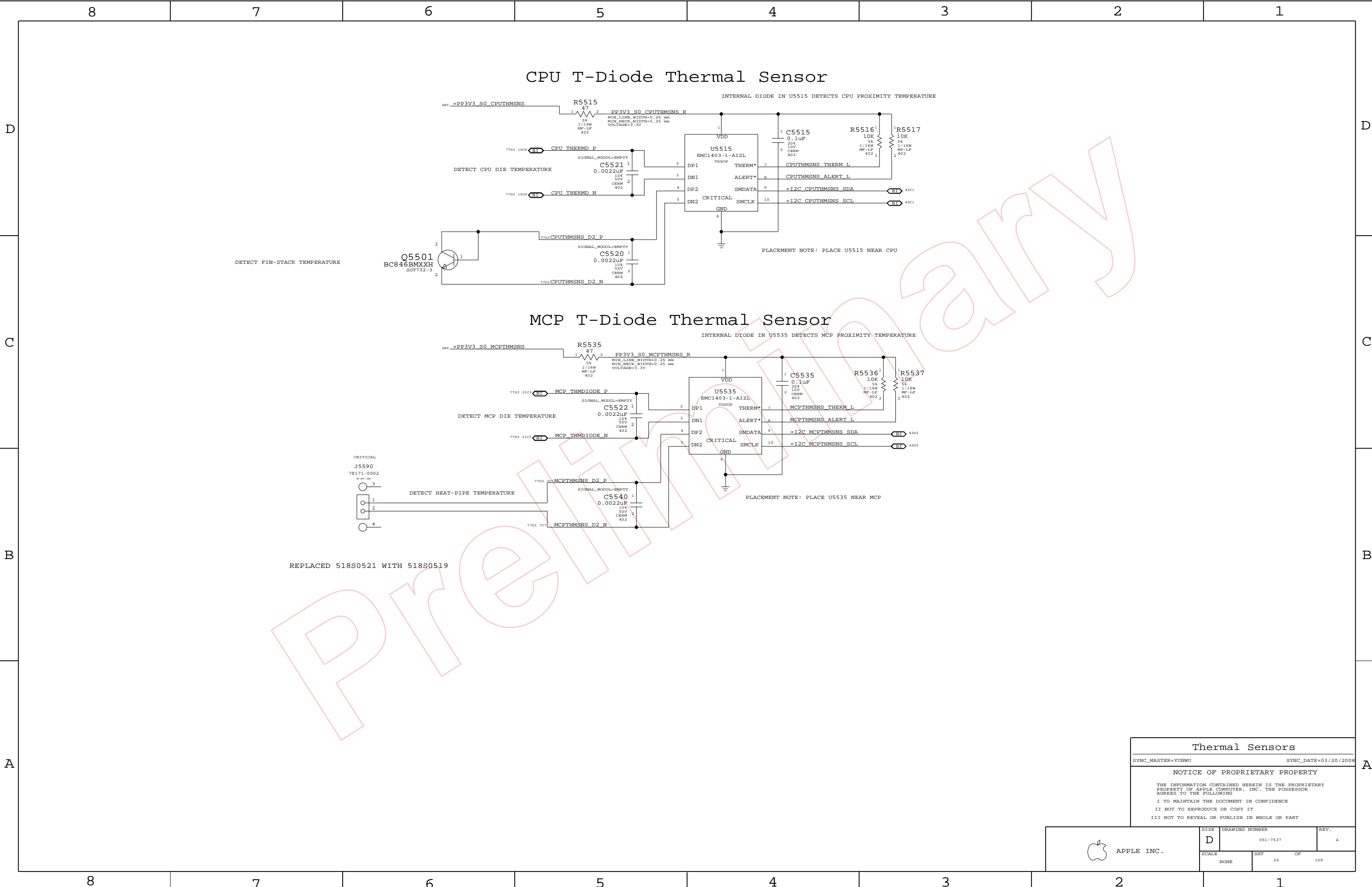
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SCALE		SHT	OF
NONE		54	109



Thermal Sensors

SYNC_MASTER=YUNWU SYNC_DATE=03/20/2008


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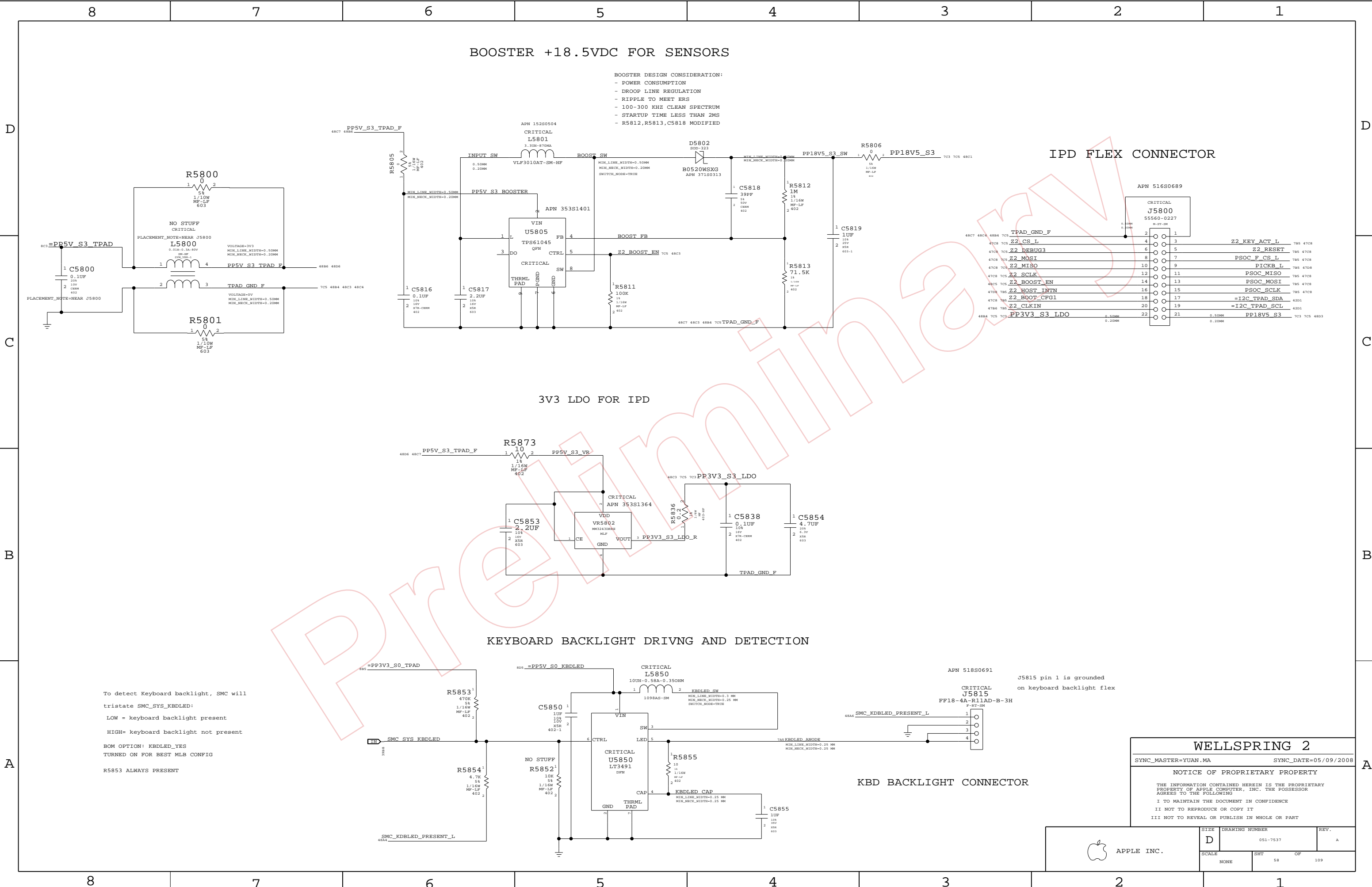
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 APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	55	109





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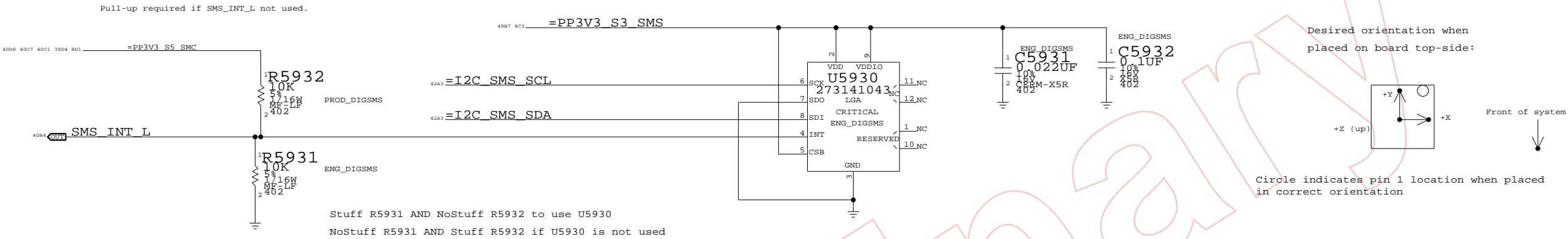
D

C

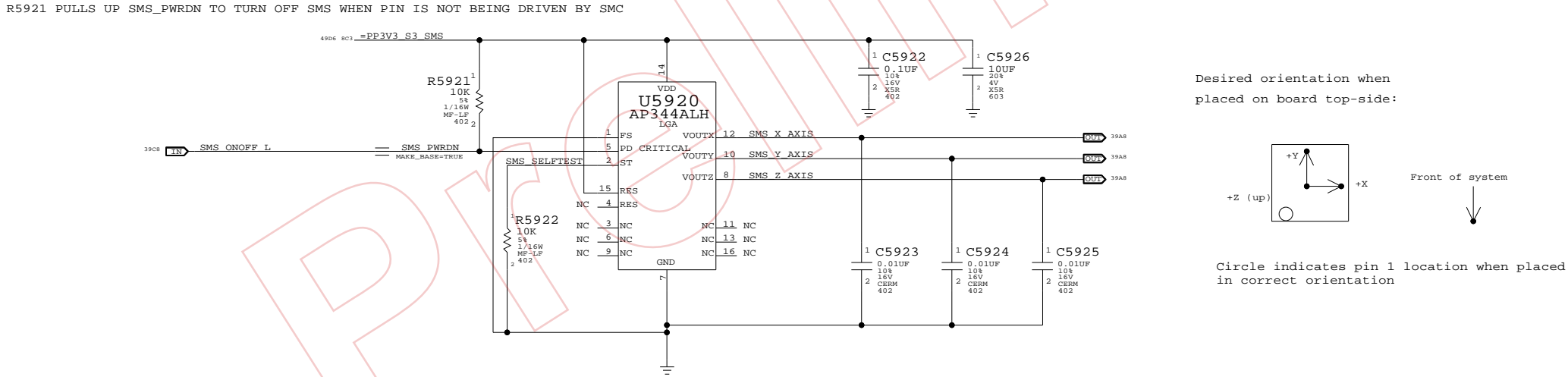
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A

Digital SMS



Analog SMS



SMS

SYNC_MASTER=YUNWU SYNC_DATE=06/26/2008

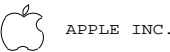
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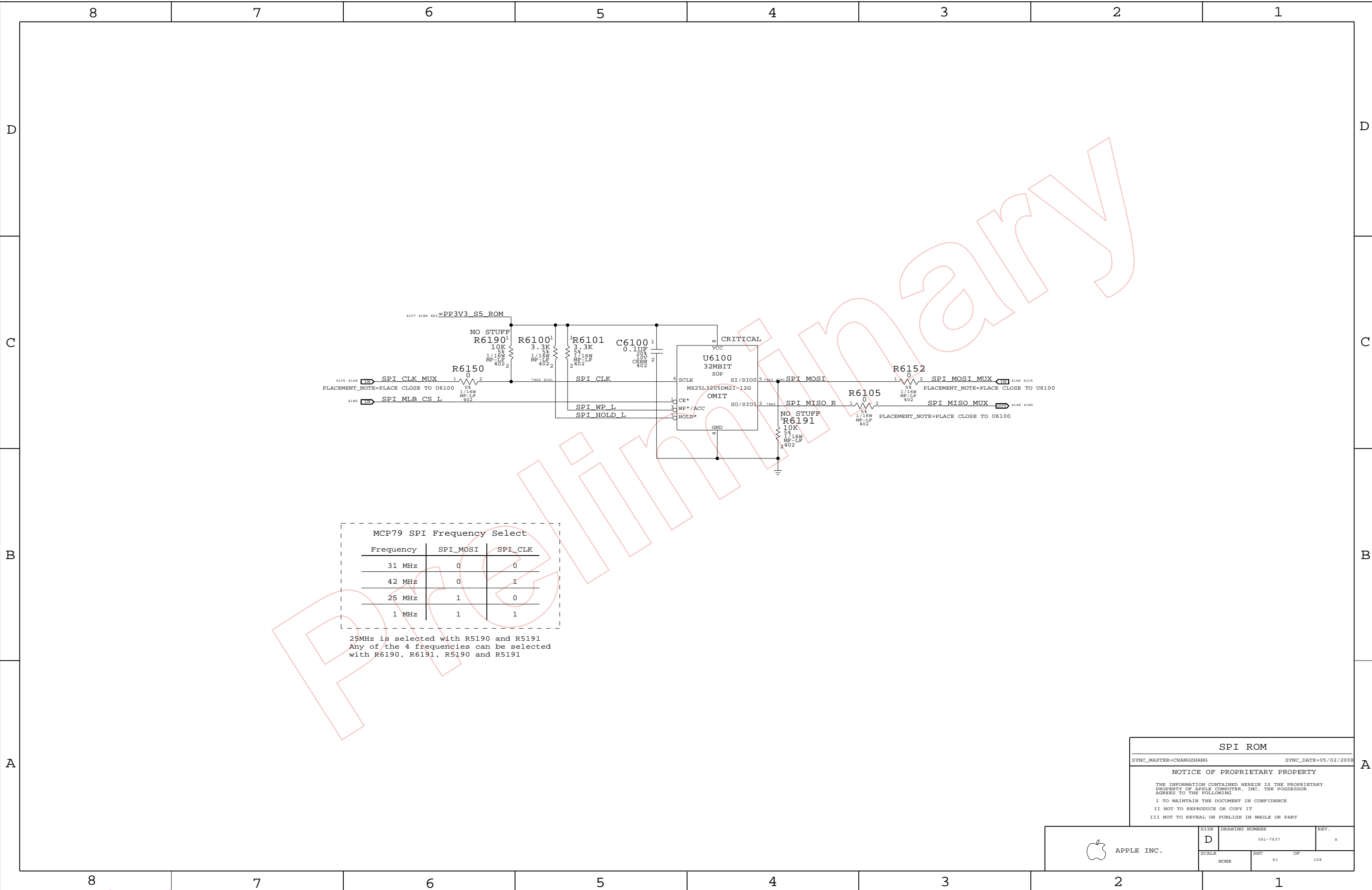
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	59	109



D

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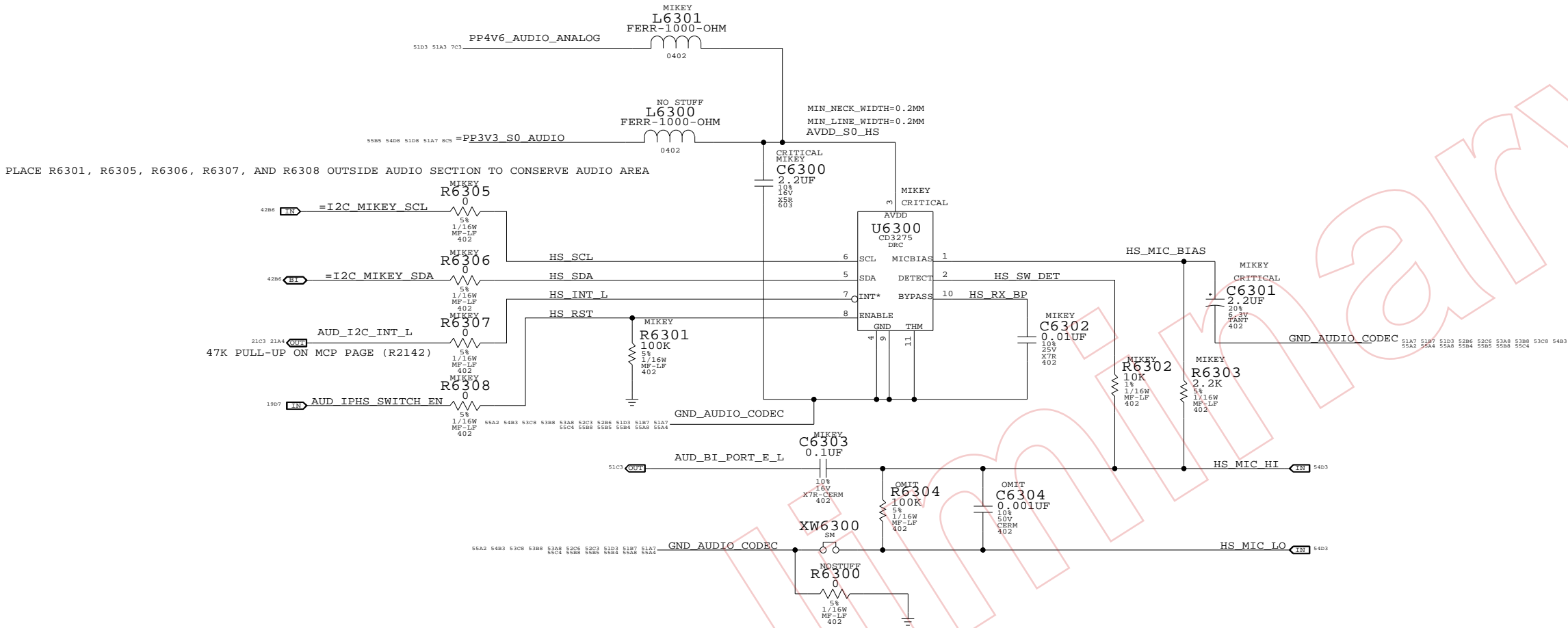
D

C

B

A

MIKEY RECEIVER CKT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6304	?	NOMIKEY
132S0045	1	100PF 50V 10% 0402 CAPACITOR	C6304	?	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6304	?	NOMIKEY

AUDIO: MIKEY

SYNC_MASTER=AUDIO SYNC_DATE=07/03/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7537

REV.

A

SCALE

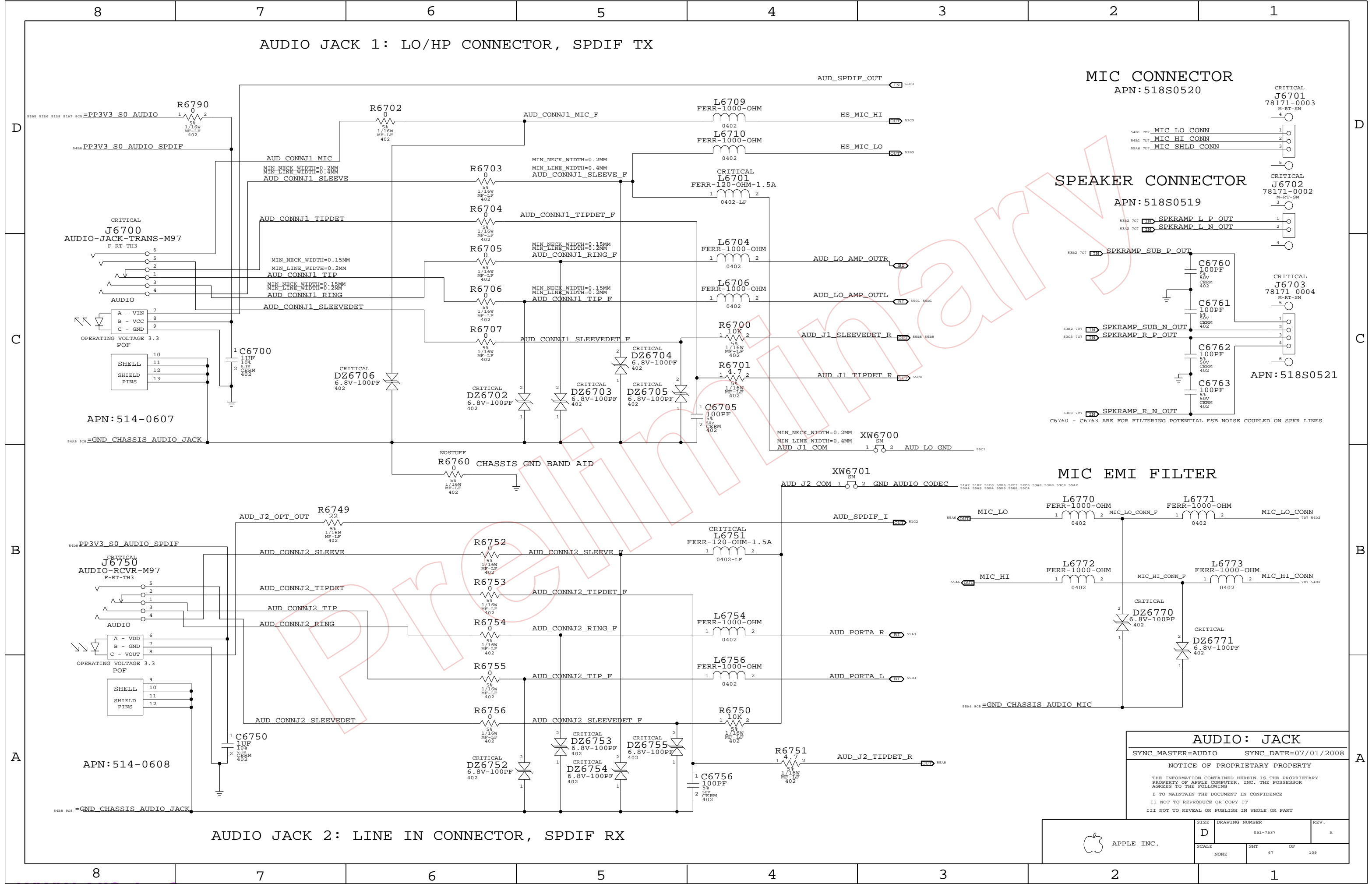
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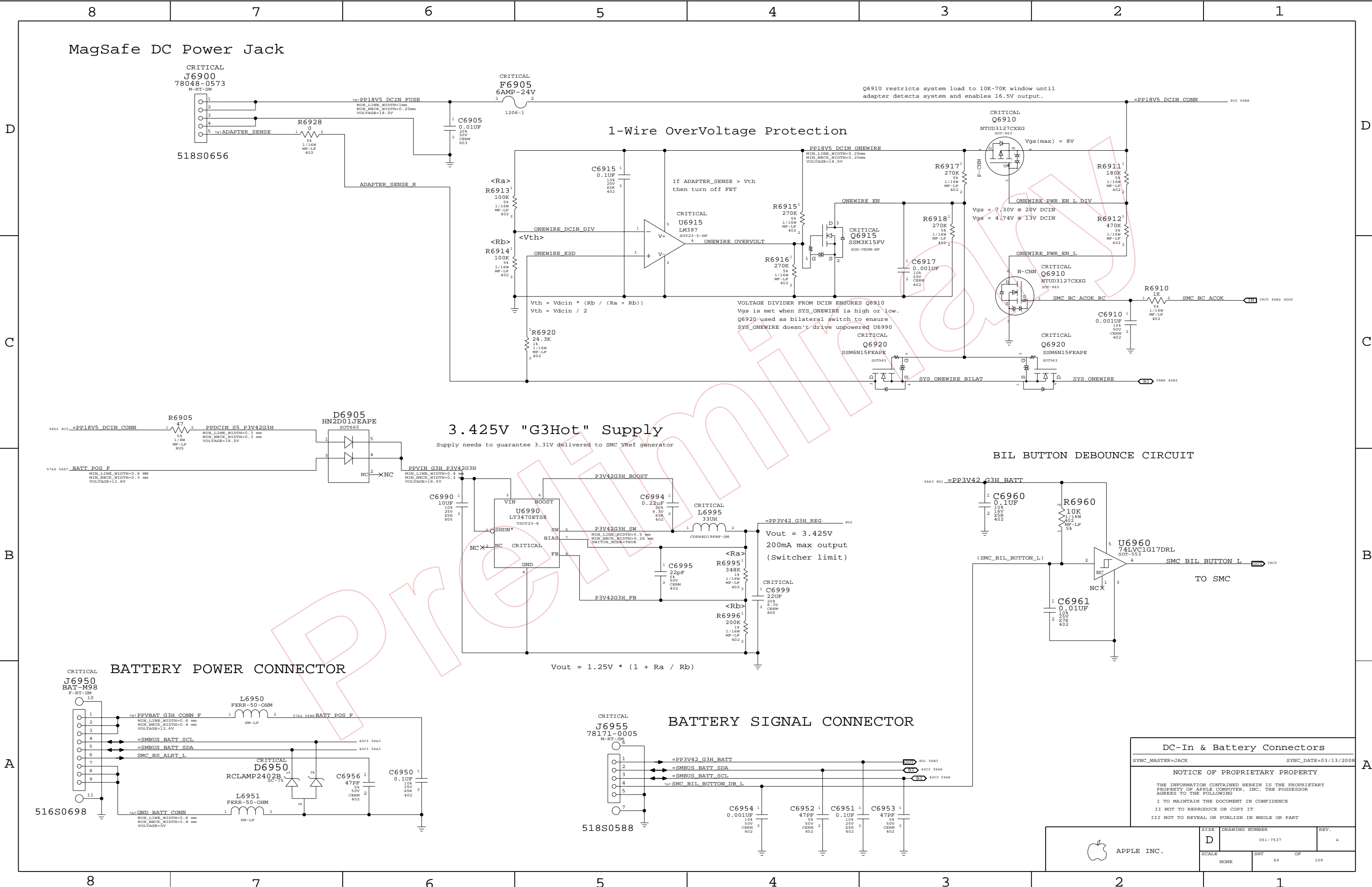
SHT

63

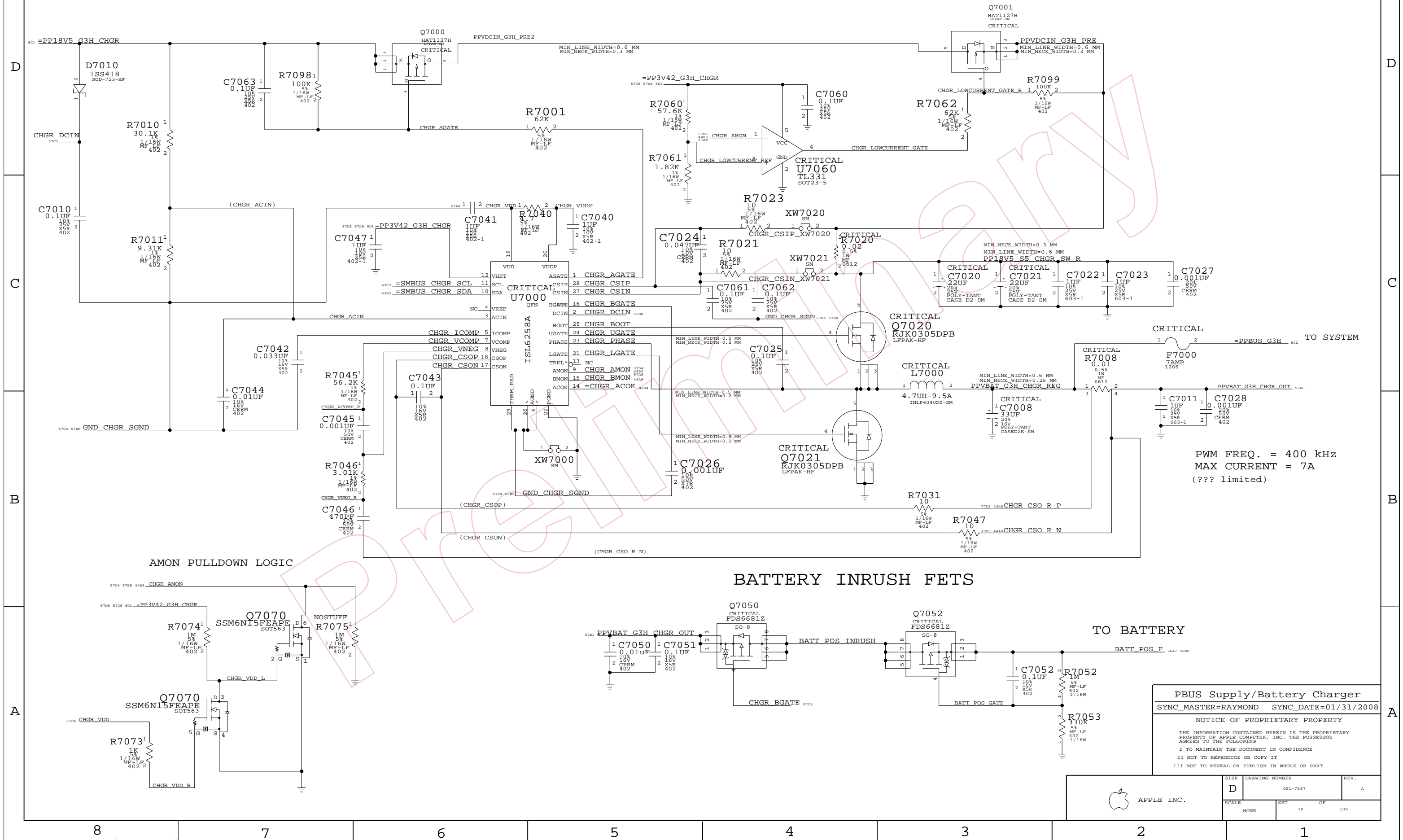
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109





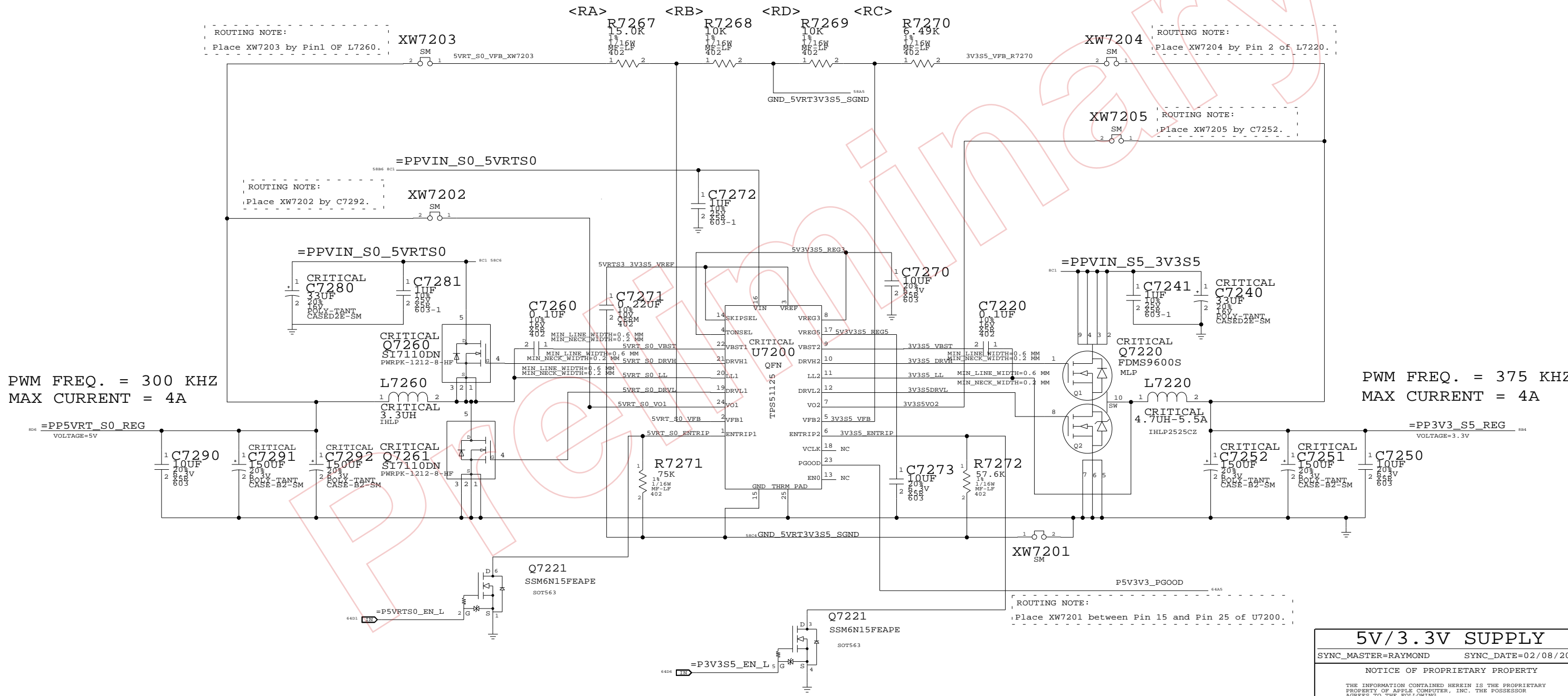
PBUS SUPPLY / BATTERY CHARGER



5V_RT/3.3V POWER SUPPLY

$VOUT = (2 * RA / RB) + 2$

$VOUT = (2 * RC / RD) + 2$



PWM FREQ. = 300 KHZ
MAX CURRENT = 4A

PWM FREQ. = 375 KHZ
MAX CURRENT = 4A

SEPARATED MASTER PGGOOD FOR BOTH 5V AND 3V3.

5V/3.3V SUPPLY

SYNC_MASTER=RAYMOND

SYNC_DATE=02/08/2008

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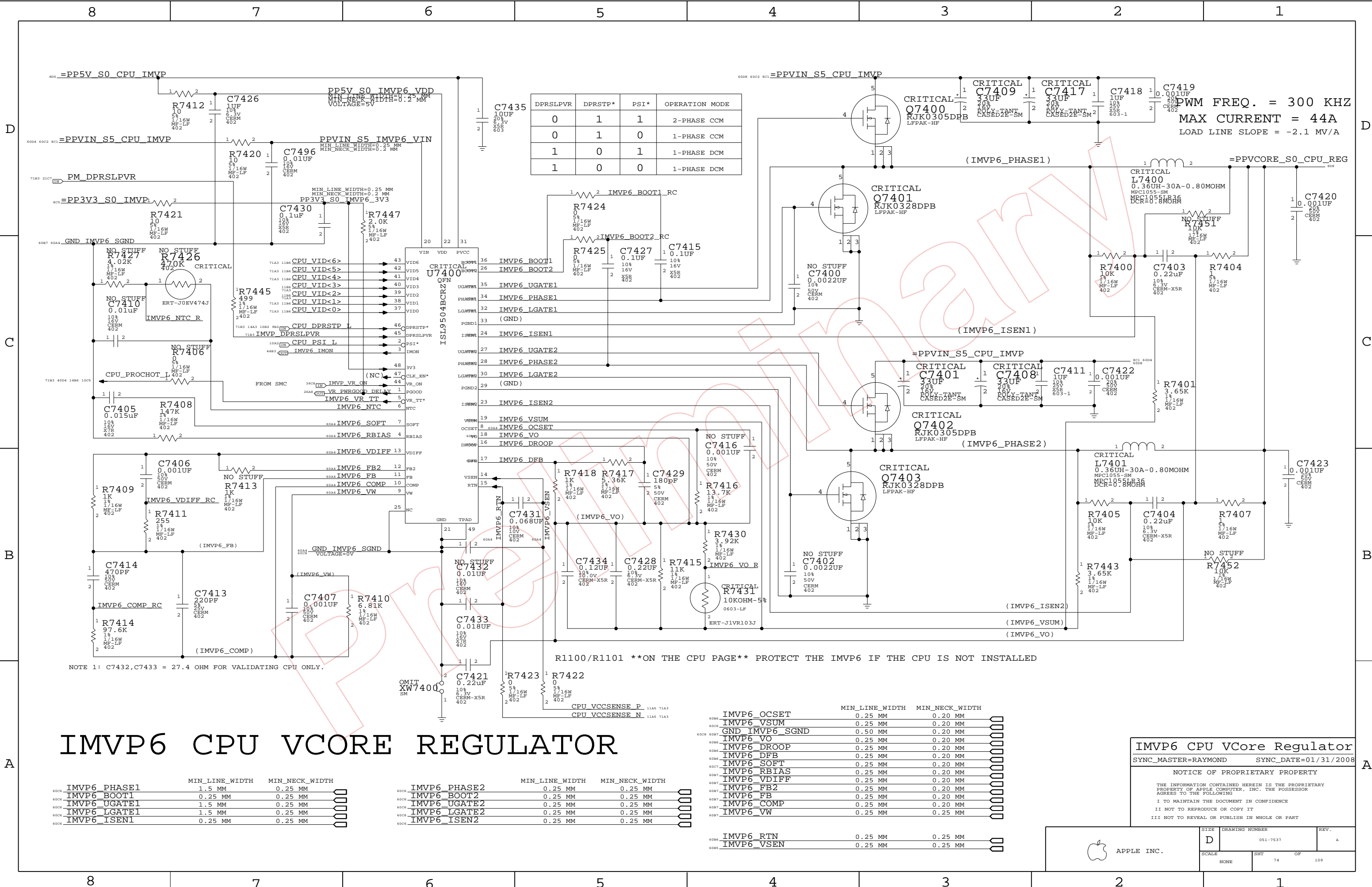
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		72	109

D

BA



IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

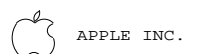
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM

IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
SYNC_MASTER=RAYMOND SYNC_DATE=01/31/2008

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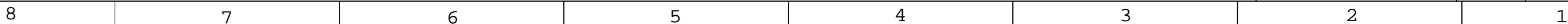
SIZE	DRAWING NUMBER	REV.
D	051-7537	A
SCALE	SHT	OF
NONE	74	109

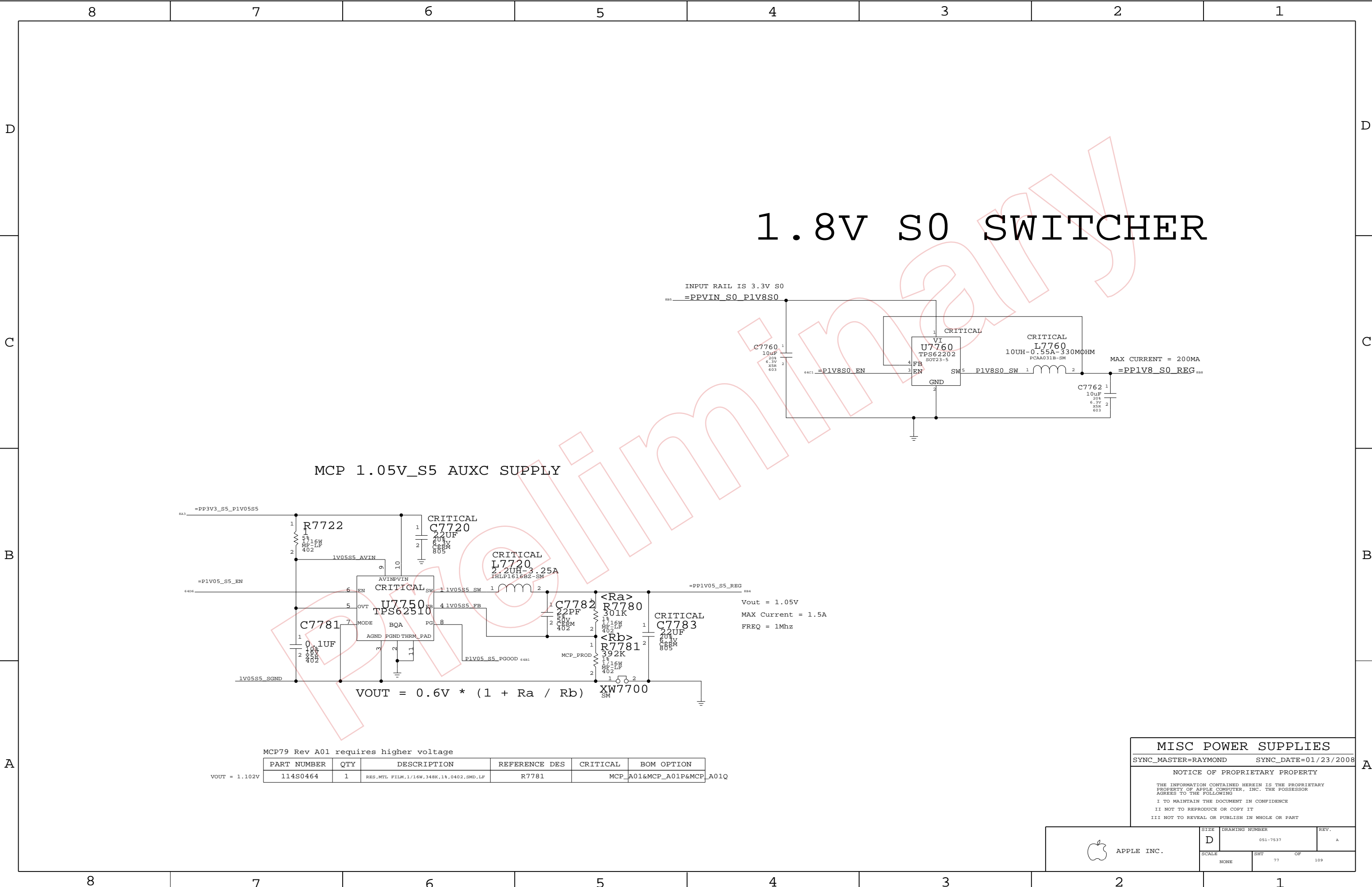
D

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MCP VCORE REGULATOR			
SYNC_MASTER=RAYMOND		SYNC_DATE=01/31/2008	
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D	051-7537	A	
SCALE	SHT	OF	109
NONE			

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1.8V S0 SWITCHER

MCP 1.05V_S5 AUXC SUPPLY

Vout = 1.05V
MAX Current = 1.5A
FREQ = 1Mhz

MCP79 Rev A01 requires higher voltage

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0464	1	RES,MTL FILM,1/16W,348K,1%,0402,SMD,LF	R7781	MCP_A01&MCP_A01P&MCP_A01Q	

MISC POWER SUPPLIES

SYNC_MASTER=RAYMOND

SYNC_DATE=01/23/2008

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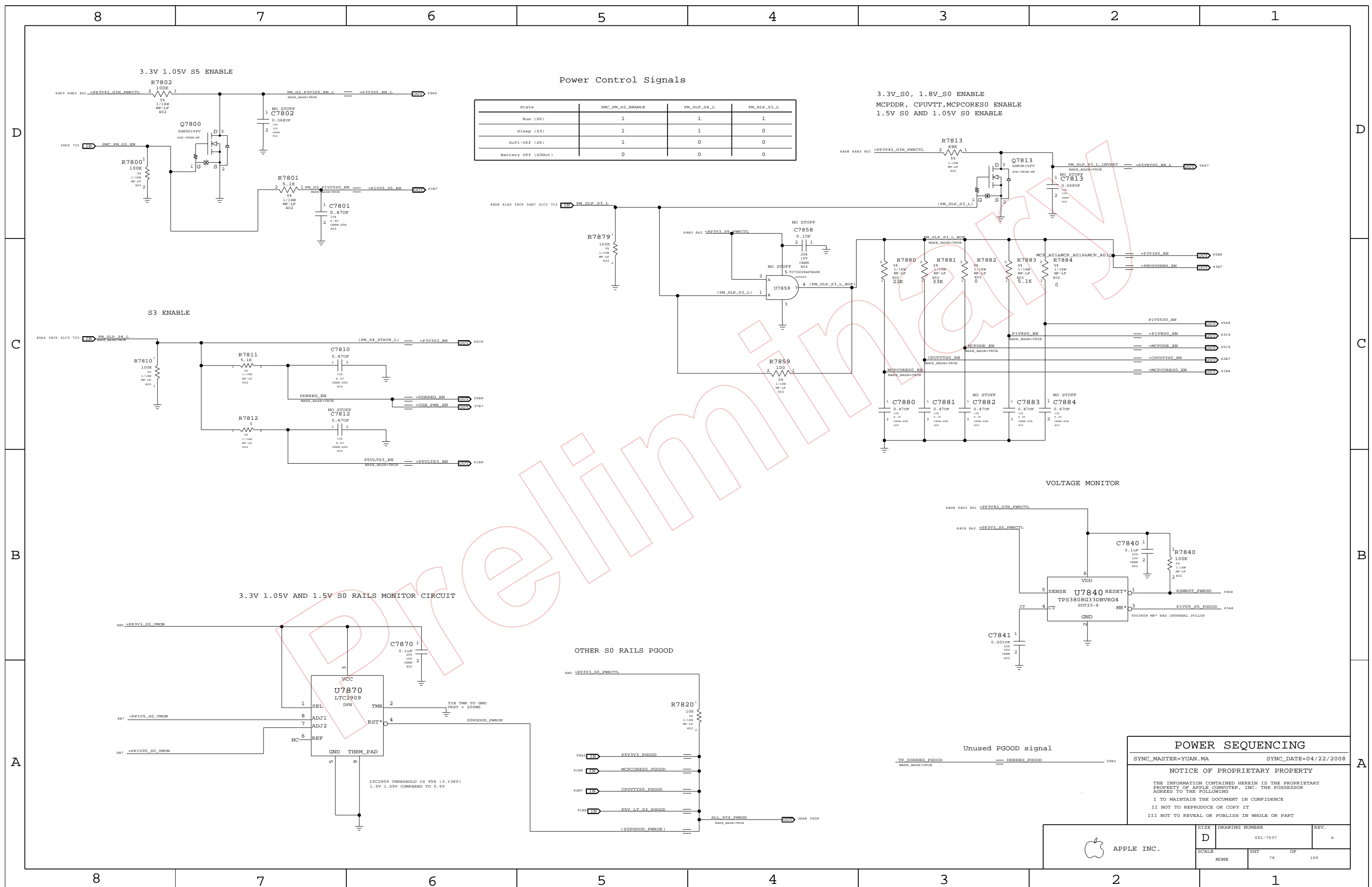
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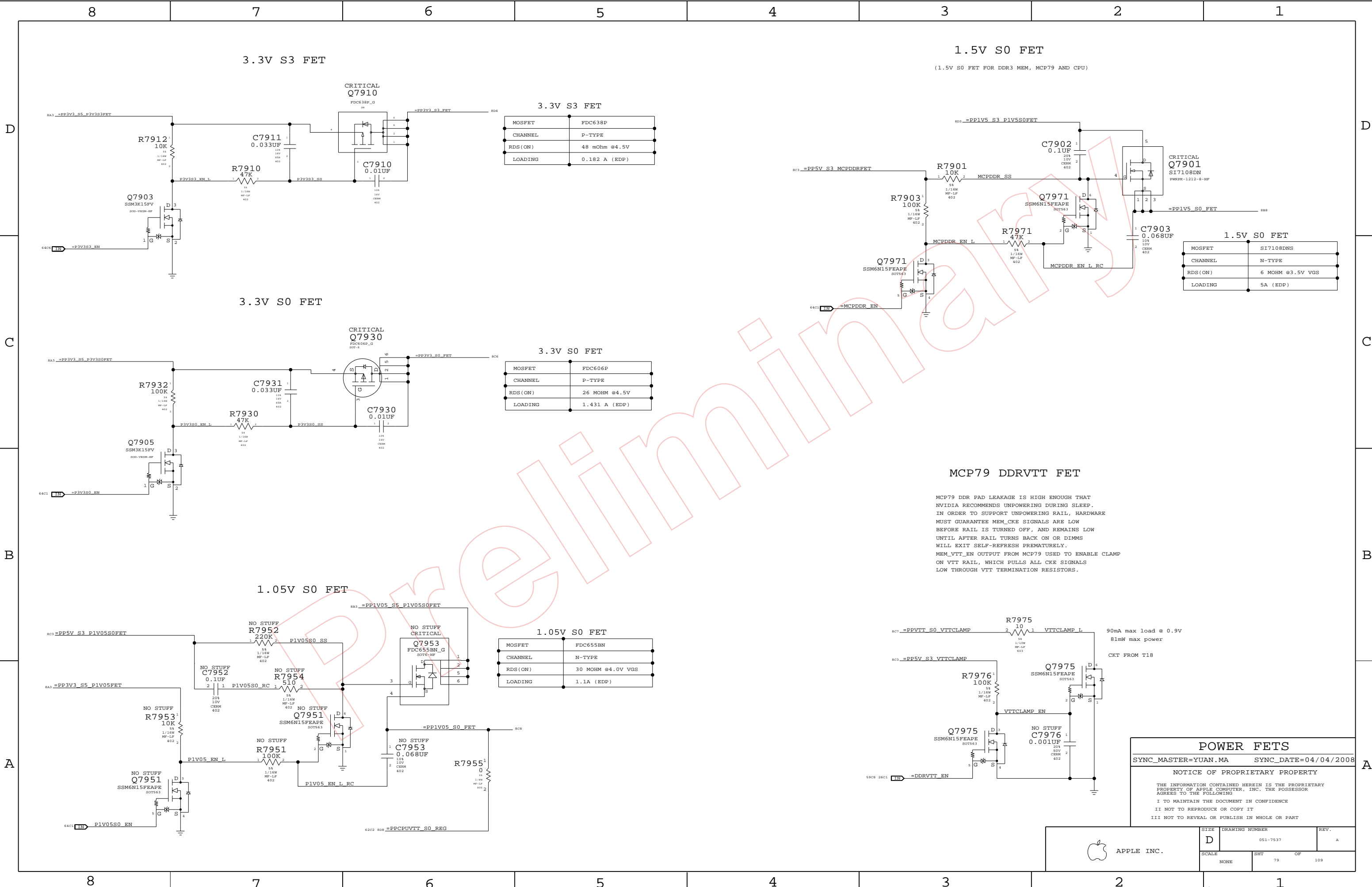
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SCALE		SHT	OF
NONE		77	109





3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.182 A (EDP)

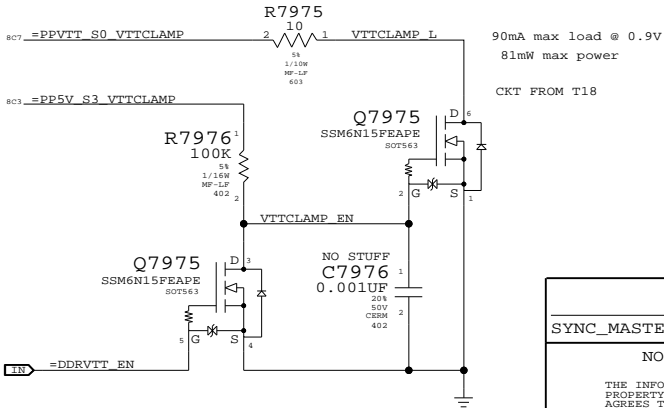
3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.431 A (EDP)

1.05V S0 FET	
MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	30 MOHM @4.0V VGS
LOADING	1.1A (EDP)

1.5V S0 FET	
MOSFET	SI7108DNS
CHANNEL	N-TYPE
RDS(ON)	6 MOHM @3.5V VGS
LOADING	5A (EDP)

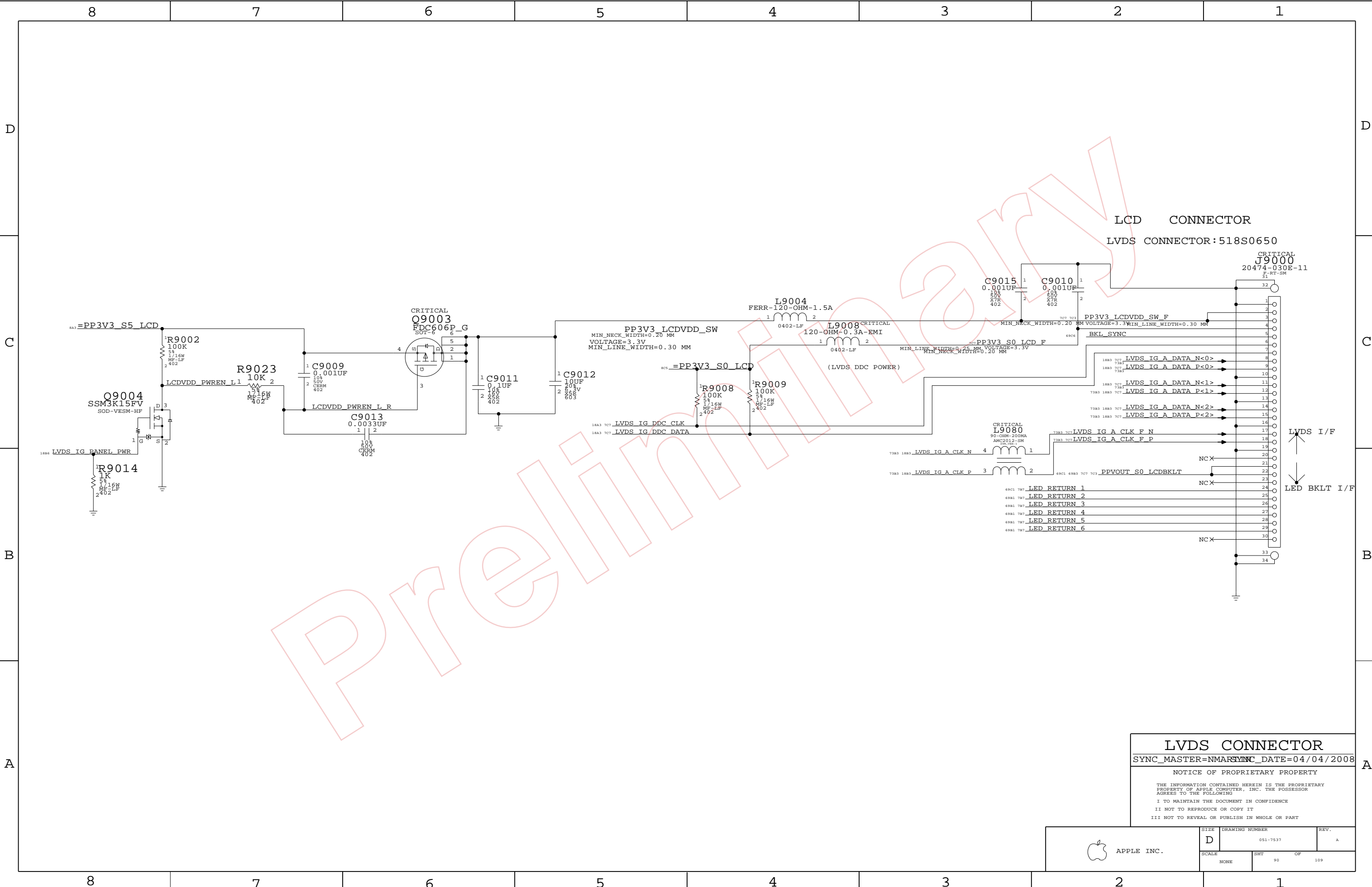
MCP79 DDRVT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



POWER FETS		
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SCALE		SHT	OF
NONE		79	109



LCD CONNECTOR
LVDS CONNECTOR:518S0650

LVDS CONNECTOR

SYNC_MASTER=NMASSYNC_DATE=04/04/2008


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	D	051-7537	A
SCALE		SHT	OF
NONE		90	109

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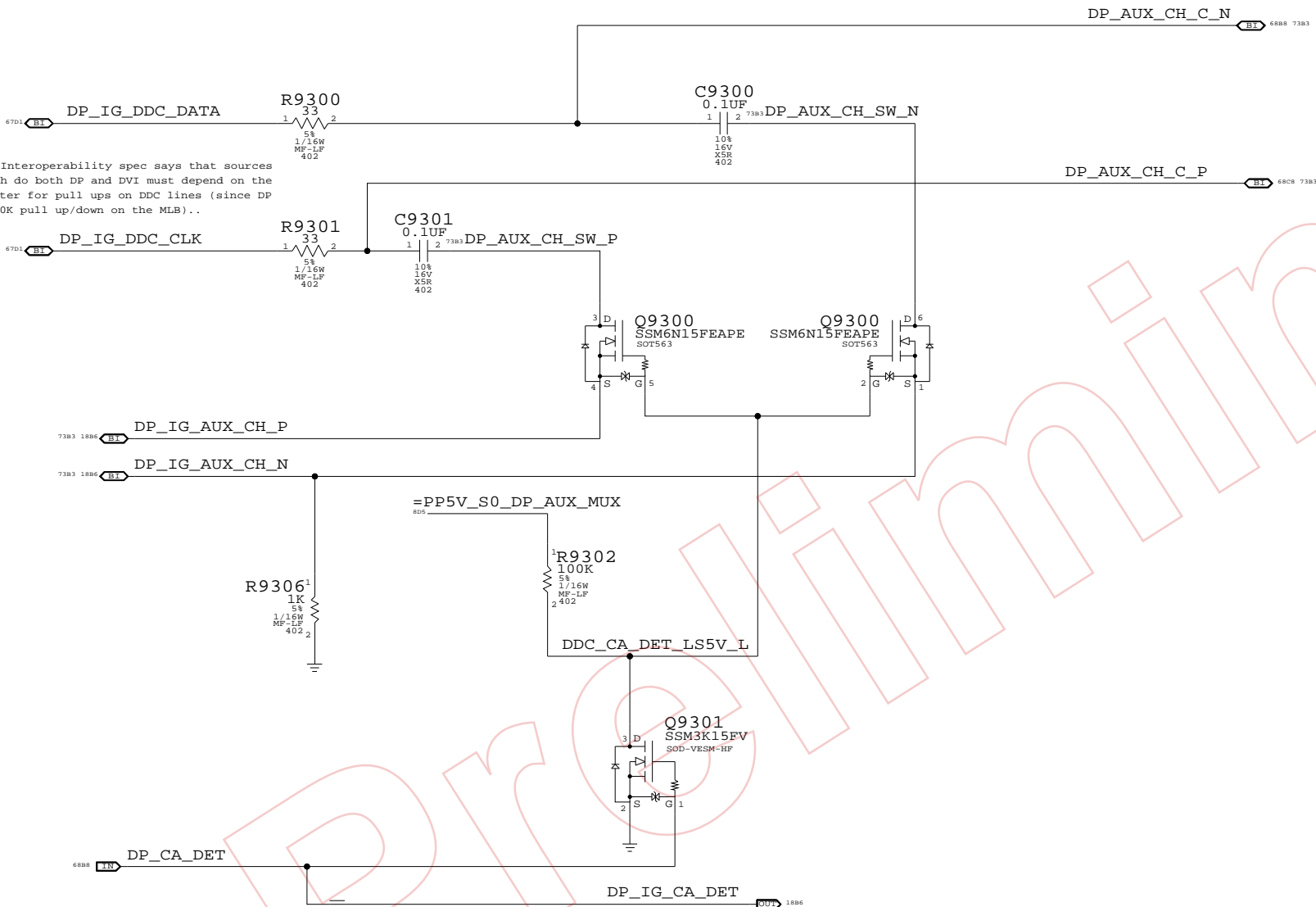
3

2

1

1886	=MCP_HDMI_TXC_P	DP_ML_P<3>	68C8 73C3
1886	=MCP_HDMI_TXC_N	DP_ML_N<3>	MAKE_BASE=TRUE 68C8 73B3
1886	=MCP_HDMI_TXD_P<0>	DP_ML_P<2>	MAKE_BASE=TRUE 68C1 73C3
1886	=MCP_HDMI_TXD_N<0>	DP_ML_N<2>	MAKE_BASE=TRUE 68B1 73B3
1886	=MCP_HDMI_TXD_P<1>	DP_ML_P<1>	MAKE_BASE=TRUE 68C1 73C3
1886	=MCP_HDMI_TXD_N<1>	DP_ML_N<1>	MAKE_BASE=TRUE 68C1 73B3
1886	=MCP_HDMI_TXD_P<2>	DP_ML_P<0>	MAKE_BASE=TRUE 68C1 73C3
1886	=MCP_HDMI_TXD_N<2>	DP_ML_N<0>	MAKE_BASE=TRUE 68C1 73B3
1886	=MCP_HDMI_HPD	DP_HPD	MAKE_BASE=TRUE 68A8
18A3	=MCP_HDMI_DDC_CLK	DP_IG_DDC_CLK	67C8
18A3	=MCP_HDMI_DDC_DATA	DP_IG_DDC_DATA	MAKE_BASE=TRUE 67C8

Display Port Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP AUX CH has 100K pull up/down on the MLB)..



DISPLAYPORT SUPPORT

SYNC_MASTER=AMASON SYNC_DATE=04/18/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7537

REV.

A

SCALE

NONE

SHT

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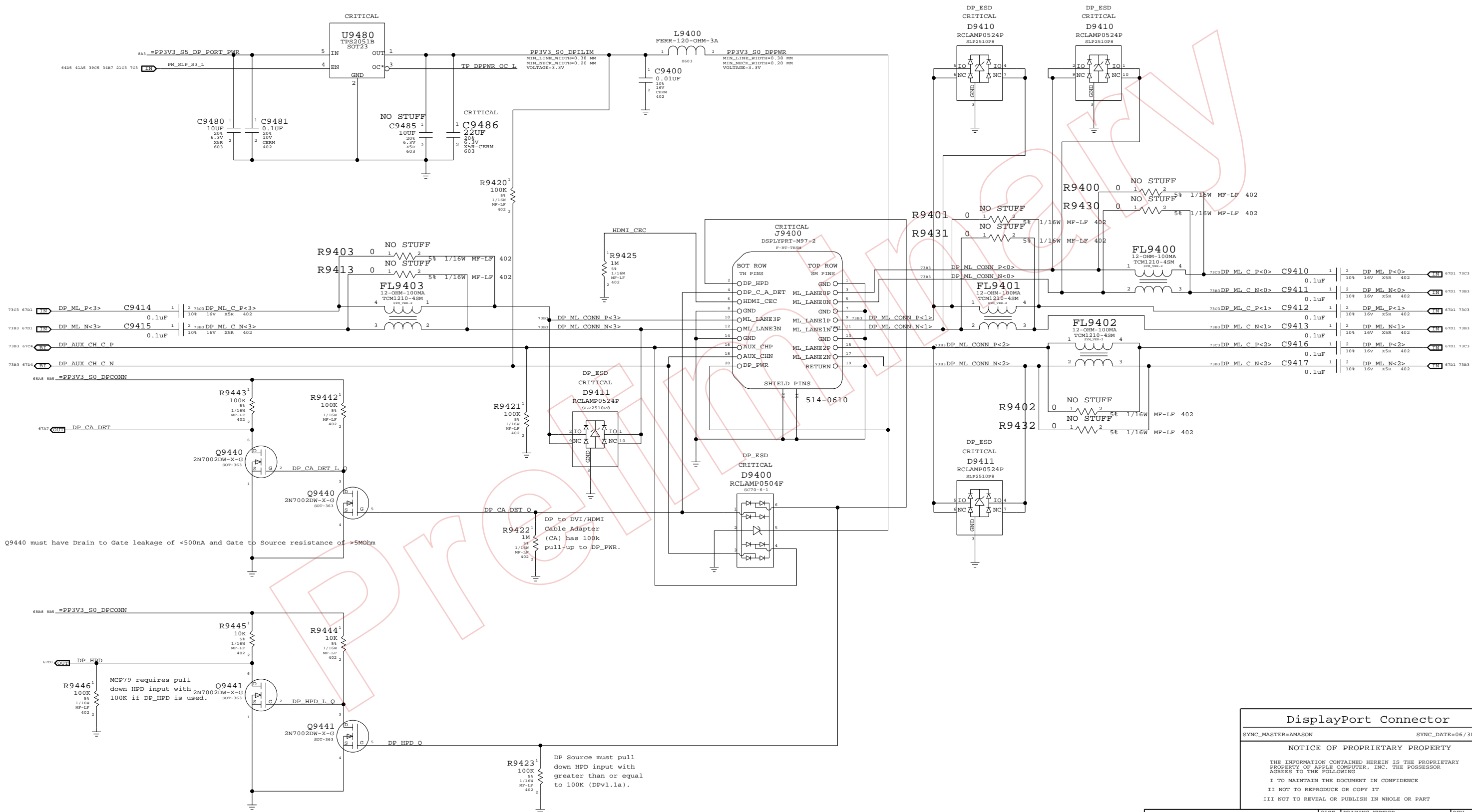
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1

Port Power Switch



DisplayPort Connector

SYNC_MASTER=AMASON SYNC_DATE=06/30/2008

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APPLE INC.

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051-7537

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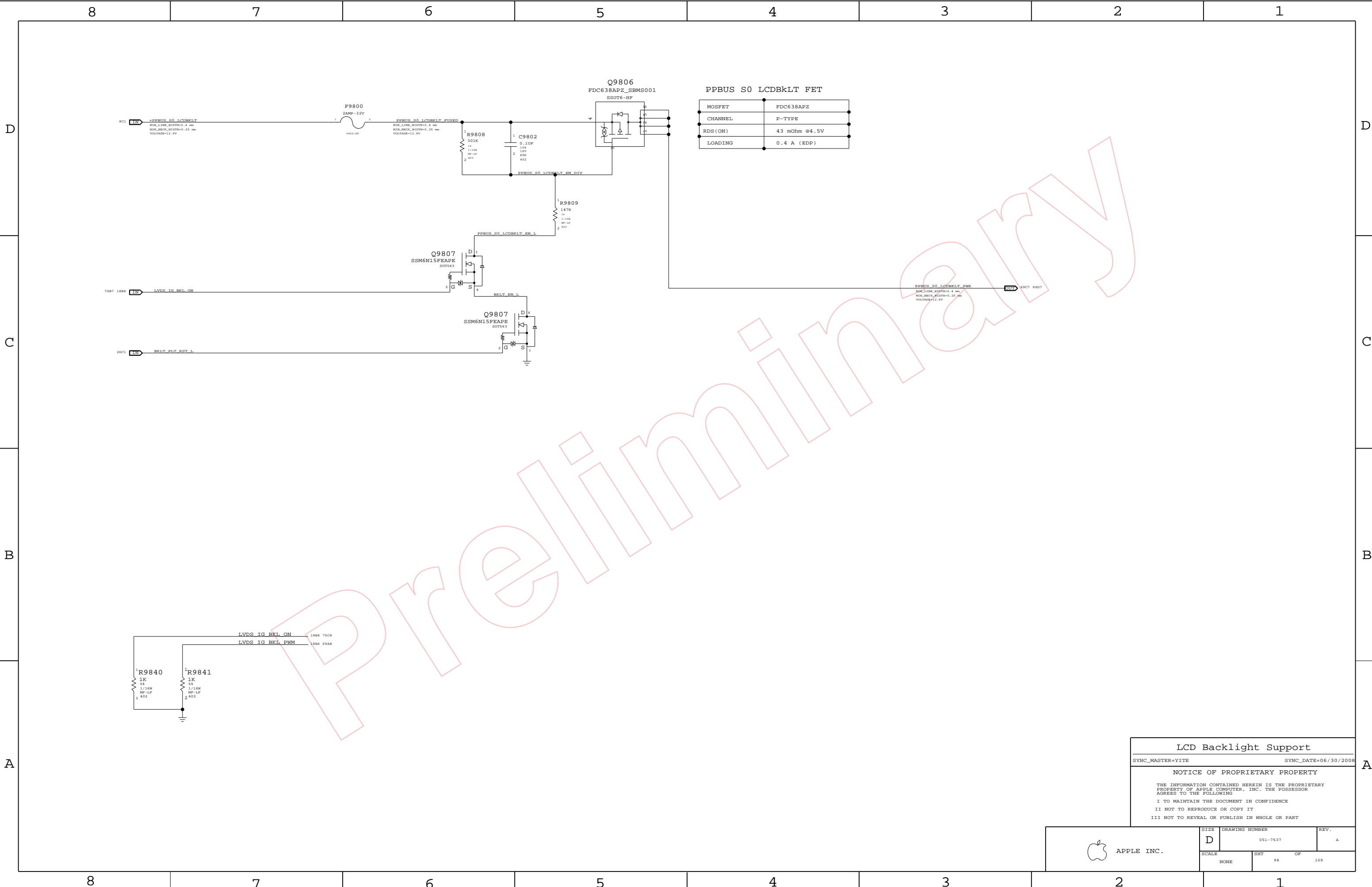
NONE

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OF

109





LCD Backlight Support

SYNC_MASTER=YITE SYNC_DATE=06/30/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7537	A
SCALE		SHT	OF
NONE		98	109

	8	7	6	5	4	3	2	1							
D	FSB (Front-Side Bus) Constraints								D						
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
	FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD							
	FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR							
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT							
	FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?							
	FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?							
	FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?							
	FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?							
	FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?							
All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.															
FSB 4X signals / groups shown in signal table on right. Signals within each 4x group should be matched within 5 ps of strobe. DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps. Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s. DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.															
FSB 2X signals / groups shown in signal table on right. Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps. Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.															
FSB 1X signals shown in signal table on right. Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.															
Design Guide recommends each strobe/signal group is routed on the same layer. Intel Design Guide recommends FSB signals be routed only on internal layers.															
NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.															
SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2															
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3															
C	CPU Signal Constraints								C						
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
	CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD							
	CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL							
	NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.														
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT							
	CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?							
	CPU_8MIL	*	8 MIL	?	SR DG recommends at least 25 mils, >50 mils preferred										
	CPU_COMP	*	25 MIL	?											
	CPU_GTLREF	*	25 MIL	?											
CPU_ITP	*	=2:1_SPACING	?												
CPU_VCCSENSE	*	25 MIL	?												
Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.															
SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2															
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4															
B	MCP FSB COMP Signal Constraints								B						
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
	MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD							
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SR DG recommends at least 25 mils, >50 mils preferred										
	MCP_FSB_COMP	*	8 MIL	?											
	SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4														
	FSB Clock Constraints														
	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP							
	CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF							
	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT							
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?								
SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5															
A	CPU / FSB Net Properties								A						
	FSB 4X Signal Groups	ELECTRICAL_CONSTRAINT_SET	NET_TYPE												
		PHYSICAL	SPACING												
		FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	10C4	14D3								
		FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	10C4	14D6								
		FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	10C4	14D6								
		FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	10C4	14D6								
		FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	10B4	10C4 14C3 14D3								
		FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	10B4	14D6								
		FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	10B4	14D6								
FSB_DSTB1		FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	10B4	14D6									
FSB 2X Signals		FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	10C2	14B3 14C3								
		FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	10C2	14D6								
		FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	10C2	14D6								
		FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	10C2	14D6								
		FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	10B2	10C2 14B3								
		FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	10B2	14D6								
		FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	10B2	14D6								
		FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	10B2	14D6								
		FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	10D8	14C6 14D6								
		FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	10D8	14B6								
FSB 1X Signals		FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	10D8	14B6								
		FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	10C8	14B6 14C6								
		FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	10C8	14B6								
		FSB_1X	FSB_50S	FSB_1X	FSB ADS L	10D6	14B6								
		FSB_BREQ0_1	FSB_50S	FSB_1X	FSB BREQ0 L	9B2	10D6 14B6								
		FSB_BREQ1_1	FSB_50S	FSB_1X	FSB BREQ1 L	14B6									
		FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10D6	14B6								
		FSB_1X	FSB_50S	FSB_1X	FSB BPR1 L	10D6	14B3								
		FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	10D6	14B6								
		FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	10D6	14B3								
		FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	10D6	14B6								
		FSB_1X	FSB_50S	FSB_1X	FSB HIT L	10C6	14B6								
		FSB_1X	FSB_50S	FSB_1X	FSB HITM L	10C6	14B6								
		FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	10D6	14B6								
		FSB_CPURST_1	FSB_50S	FSB_1X	FSB CPURST L	9B2	10D6 13B2 14A3								
		FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	10D6	14A6								
		FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10D6	14B6								
		CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	10C8	14A3								
		CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9C2	10A4 10B4								
		CPU_FERR_1	CPU_50S	CPU_BMT	CPU FERR L	10C8	14B7								
		CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNNR L	10C8	14A3								
		CPU_INIT_1	CPU_50S	CPU_AGTL	CPU INIT L	10D6	14A3								
		CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	9B2	10B8 14A3								
		CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	9B2	10B8 14A3								
		CPU_PROCHOT_1	CPU_50S	CPU_AGTL	CPU PROCHOT L	10C5	14B6 40D4 60C8								
		CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	10B2	13C7 14A3								
		CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	10B8	14A3								
		CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	10B8	14A3								
		PM THERMTRIP_1	CPU_50S	CPU_BMT	PM THERMTRIP L	10C6	14B7 40C4								
		FSB_CPUSLP_1	CPU_50S	CPU_AGTL	FSB CPUSLP L	10A2	14A3								
		CPU_FERR_SR	CPU_50S	CPU_AGTL	CPU DPSLP L	10B2	14A3								
		CPU_DPRSTP_1	CPU_50S	CPU_AGTL	CPU DPRSTP L	9B2	10B2 14A3 60C7								
		CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	10B2	14A3								
		MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14A6									
		MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14A6									
		MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14A6									
		MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14A6									
		FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10B6	14B3								
		FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10B6	14B3								
		FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13C3	14A3								
		FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13B3	14A3								
		FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14A4									
		FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14A4									
		CPU_FERR_1	CPU_50S		CPU IERR L	10D6									
		PM DPRSLPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	21C7	60D8								
		(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	60C7									
		CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10B4	27B1								
		CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10B3									
		CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10B3									
		CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10B3									
		CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10B3									
		XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	6C6	10B6 10C6 13B3								
		XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	6C4	10B6 10C6								
		XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	6C6	6C7 10B6 10C6 13B3								
		XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	6C6	6C7 10A6 10C6 13B6								
		XDP_TRST_1	CPU_50S	CPU_ITP	XDP TRST L	6C6	6C7 10A6 10C6 13B3								
		XDP_BPM_1	CPU_50S	CPU_ITP	XDP BPM L<4..0>	10C6	13C6								
		XDP_BPM_1_5	CPU_50S	CPU_ITP	XDP BPM L<5>	10C5	13C6								
		(FSB_CPURST_1)	CPU_50S	CPU_ITP	XDP CPURST L	13B4									
			CPU_50S	CPU_BMT	CPU VID<6..0>	11B6	60C7								
		CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	IMVP6 VID<6..0>	11A5	60A5								
		CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11A5	60A5								
		(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11A5	60A5								
		(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P										
		(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N										
		CPU/FSB Constraints													
		SYNC_MASTER=T18_MLB				SYNC_DATE=01/04/2008									
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 APPLE INC.						SIZE	DRAWING NUMBER	REV.							
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

All DQS pairs should be matched within 100 ps of clocks.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

A/BA/cmd signals should be matched within 5 ps of CLK pairs.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0>	1585 2805 2807
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0>	1585 2805 2807
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0>	15A5 2805 2807
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM A CS L<3..0>	1585 2805 2807
MEM_A_CTRL	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0>	15A5 2805
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0>	1585 1505 2805 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0>	1505 2805 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS L	1505 2805
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS L	1505 2807
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE L	1505 2807
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	1587 2802 2804 2802 2804
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	1587 2802 2804
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	1587 1507 2882 2884 2802 2804
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	1507 2802 2804
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	1507 2885 2887
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	1507 2885 2887
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	1507 2885 2887
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	1507 28A5 28A7
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15A7 2804
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15A7 2802
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15A7 2884
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15A7 2802
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15A7 2885
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	1587 2887
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	1587 2885
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	1587 28A7
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	1505 2802
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	1505 2802
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	1505 2804
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	1505 2804
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	1505 2882
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	1505 2882
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	1505 2804
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	1505 2804
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	1505 2887
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	1505 2887
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	1505 2885
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	1505 2885
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	1505 2887
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	1505 2887
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	1505 28A5
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	1505 28A5
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0>	1581 2905 2907
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0>	1581 2905 2907
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0>	15A1 2905 2907
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM B CS L<3..0>	1581 2905 2907
MEM_B_CTRL	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0>	15A1 2905
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0>	1581 1501 2905 2907
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0>	1501 2905 2907
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS L	1501 2905
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS L	1501 2907
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE L	1501 2907
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	1583 2902 2904 2902 2904
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	1583 2902 2904
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	1583 1501 2902 2904
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	1503 2982 2984 2902 2904
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	1503 2985 2987
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	1503 2985 2987
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	1503 2985 2987
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	1503 29A5 29A7
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15A3 2904
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15A3 2902
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15A3 2902
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15A3 2984
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15A3 2985
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	1583 2987
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	1583 2985
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	1583 29A7
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	1501 2902
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	1501 2902
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	1501 2904
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	1501 2904
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	1501 2904
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	1501 2904
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	1501 2982
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3>	1501 2982
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	1501 2987
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	1501 2987
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	1501 2985
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	1501 2985
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	1501 2987
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	1501 2987
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	1501 29A5
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	1501 29A5
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	1606
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	1606

Memory Constraints

SYNC_MASTER=T18_MLB

SYNC_DATE=01/04/2008

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PCI-Express				<table><tr><th rowspan="2">ELECTRICAL_CONSTRAINT_SET</th><th colspan="2">NET_TYPE</th><th rowspan="2"></th><th rowspan="2"></th></tr><tr><th>PHYSICAL</th><th>SPACING</th></tr><tr><td rowspan="6"></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI R2D P</td><td>705 3107</td></tr><tr><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI R2D N</td><td>705 3107</td></tr><tr><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI R2D C P</td><td>1783 3105</td></tr><tr><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI R2D C N</td><td>1783 3105</td></tr><tr><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI D2R P</td><td>705 1786 3107</td></tr><tr><td>PCIE_90D</td><td>PCIE</td><td>PCIE MINI D2R N</td><td>705 1786 3107</td></tr><tr><td rowspan="6"></td><td>PCIE_90D</td><td>PCIE</td><td>PCIE FC R2D P</td><td>3205</td></tr><tr><td>PCIE_90D</td><td>PCIE</td><td>PCIE FC R2D N</td><td>3205</td></tr><tr><td>PCIE_90D</td><td>PCIE</td><td>PCIE FC R2D C P</td><td>985 3205</td></tr><tr><td>PCIE_90D</td><td>PCIE</td><td>PCIE FC R2D C N</td><td>985 3205</td></tr><tr><td>PCIE_90D</td><td>PCIE</td><td>PCIE FC D2R P</td><td>985 3285</td></tr><tr><td>PCIE_90D</td><td>PCIE</td><td>PCIE FC D2R N</td><td>985 3285</td></tr><tr><td rowspan="4"></td><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M MINI P</td><td>1703 3105</td></tr><tr><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M MINI N</td><td>1703 3105</td></tr><tr><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M MINI CONN P</td><td>705 3105</td></tr><tr><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M MINI CONN N</td><td>705 3105</td></tr><tr><td rowspan="2"></td><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M FC P</td><td>985 3205</td></tr><tr><td>CLK_PCIE_100D</td><td>CLK_PCIE</td><td>PCIE CLK100M FC N</td><td>985 3205</td></tr><tr><td></td><td></td><td>MCP_PEX_COMP</td><td>MCP_PEX_CLK_COMP</td><td>17A6</td></tr></table>				ELECTRICAL_CONSTRAINT_SET	NET_TYPE				PHYSICAL	SPACING		PCIE_90D	PCIE	PCIE MINI R2D P	705 3107	PCIE_90D	PCIE	PCIE MINI R2D N	705 3107	PCIE_90D	PCIE	PCIE MINI R2D C P	1783 3105	PCIE_90D	PCIE	PCIE MINI R2D C N	1783 3105	PCIE_90D	PCIE	PCIE MINI D2R P	705 1786 3107	PCIE_90D	PCIE	PCIE MINI D2R N	705 1786 3107		PCIE_90D	PCIE	PCIE FC R2D P	3205	PCIE_90D	PCIE	PCIE FC R2D N	3205	PCIE_90D	PCIE	PCIE FC R2D C P	985 3205	PCIE_90D	PCIE	PCIE FC R2D C N	985 3205	PCIE_90D	PCIE	PCIE FC D2R P	985 3285	PCIE_90D	PCIE	PCIE FC D2R N	985 3285		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P	1703 3105	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N	1703 3105	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CONN P	705 3105	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI CONN N	705 3105		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FC P	985 3205	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FC N	985 3205			MCP_PEX_COMP	MCP_PEX_CLK_COMP	17A6																																																																																																																																																																																																																																																																																																																						
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Digital Video Signal Constraints				<table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>DP_100D</td><td>*</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td></tr><tr><td>LVDS_100D</td><td>*</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td></tr><tr><td>MCP_DV_COMP</td><td>*</td><td>?</td><td>20 MIL</td><td>20 MIL</td><td>=STANDARD</td><td>=STANDARD</td><td>=STANDARD</td></tr></table> <table><tr><th>SPACING_RULE_SET</th><th>LAYER</th><th>LINE-TO-LINE SPACING</th><th>WEIGHT</th></tr><tr><td>DISPLAYPORT</td><td>*</td><td>=3X_DIELECTRIC</td><td>?</td></tr><tr><td>LVDS</td><td>*</td><td>=3X_DIELECTRIC</td><td>?</td></tr></table> <p>LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches. SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.</p> <div>SATA Interface Constraints</div> <table><tr><th>PHYSICAL_RULE_SET</th><th>LAYER</th><th>ALLOW ROUTE ON LAYER?</th><th>MINIMUM LINE WIDTH</th><th>MINIMUM NECK WIDTH</th><th>MAXIMUM NECK LENGTH</th><th>DIFFPAIR PRIMARY GAP</th><th>DIFFPAIR NECK GAP</th></tr><tr><td>SATA_100D</td><td>*</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td><td>=100_OHM_DIFF</td></tr><tr><td>SATA_100D_HDD</td><td>*</td><td>=100_OHM_DIFF_HDD</td><td>=100_OHM_DIFF_HDD</td><td>=100_OHM_DIFF_HDD</td><td>=100_OHM_DIFF_HDD</td><td>=100_OHM_DIFF_HDD</td><td>=100_OHM_DIFF_HDD</td></tr></table> <table><tr><th>SPACING_RULE_SET</th><th>LAYER</th><th>LINE-TO-LINE SPACING</th><th>WEIGHT</th></tr><tr><td>SATA</td><td>*</td><td>=4X_DIELECTRIC</td><td>?</td></tr><tr><td>SATA_TERMP</td><td>*</td><td>8 MIL</td><td>?</td></tr></table> <table><tr><th>SPACING_RULE_SET</th><th>LAYER</th><th>LINE-TO-LINE SPACING</th><th>WEIGHT</th></tr><tr><td>SATA</td><td>TOP,BOTTOM</td><td>=3X_DIELECTRIC</td><td>?</td></tr></table> <div>SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.</div>				PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	MCP_DV_COMP	*	?	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	DISPLAYPORT	*	=3X_DIELECTRIC	?	LVDS	*	=3X_DIELECTRIC	?	PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SATA	*	=4X_DIELECTRIC	?	SATA_TERMP	*	8 MIL	?	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SATA	TOP,BOTTOM	=3X_DIELECTRIC	?	<table><tr><td></td><td>TMDS_IG_TXC</td><td>DP_100D</td><td>DISPLAYPORT</td><td>TMDS IG TXC P</td><td></td></tr><tr><td></td><td>TMDS_IG_TXC</td><td>DP_100D</td><td>DISPLAYPORT</td><td>TMDS IG TXC N</td><td></td></tr><tr><td></td><td>TMDS_IG_TXD</td><td>DP_100D</td><td>DISPLAYPORT</td><td>TMDS IG TXD P<2..0></td><td></td></tr><tr><td></td><td>TMDS_IG_TXD</td><td>DP_100D</td><td>DISPLAYPORT</td><td>TMDS IG TXD N<2..0></td><td></td></tr><tr><td></td><td>DP_ML</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP ML P<3..0></td><td>67D1 68C1 68C8</td></tr><tr><td></td><td>DP_ML</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP ML C P<3..0></td><td>68C2 68C7</td></tr><tr><td></td><td>DP_ML</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP ML N<3..0></td><td>67D1 68B1 68C1 68C8</td></tr><tr><td></td><td>DP_ML</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP ML C N<3..0></td><td>68B2 68C2 68C7</td></tr><tr><td></td><td>DP_AUX_CH</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP IG AUX CH P</td><td>1886 67C7</td></tr><tr><td></td><td>DP_AUX_CH</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP IG AUX CH N</td><td>1886 67B7</td></tr><tr><td></td><td>DP_AUX_CH</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP AUX CH SW P</td><td>67C6</td></tr><tr><td></td><td>DP_AUX_CH</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP AUX CH SW N</td><td>67C5</td></tr><tr><td></td><td>DP_AUX_CH</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP_AUX_CH_C_P</td><td>67C4 68C8</td></tr><tr><td></td><td>DP_AUX_CH</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP_AUX_CH_C_N</td><td>67D4 68B8</td></tr><tr><td></td><td>MCP_HDMI_RSET</td><td>MCP_DV_COMP</td><td></td><td>MCP HDMI RSET</td><td>18A6 25C7</td></tr><tr><td></td><td>MCP_HDMI_VPROBE</td><td>MCP_DV_COMP</td><td></td><td>MCP HDMI VPROBE</td><td>18A6 25C7</td></tr><tr><td></td><td>LVDS_IG_A_CLK</td><td>LVDS_100D</td><td>LVDS</td><td>LVDS IG A CLK P</td><td>18B3 66B3</td></tr><tr><td></td><td>LVDS_IG_A_CLK</td><td>LVDS_100D</td><td>LVDS</td><td>LVDS IG A CLK F P</td><td>7C7 66B2</td></tr><tr><td></td><td>LVDS_IG_A_CLK</td><td>LVDS_100D</td><td>LVDS</td><td>LVDS IG A CLK N</td><td>18B3 66B3</td></tr><tr><td></td><td>LVDS_IG_A_CLK</td><td>LVDS_100D</td><td>LVDS</td><td>LVDS IG A CLK F N</td><td>7C7 66B2</td></tr><tr><td></td><td>LVDS_IG_A_DATA</td><td>LVDS_100D</td><td>LVDS</td><td>LVDS IG A DATA P<2..0></td><td>7C7 18B3 66C2</td></tr><tr><td></td><td>LVDS_IG_A_DATA</td><td>LVDS_100D</td><td>LVDS</td><td>LVDS IG A DATA N<2..0></td><td>7C7 18B3 66C2</td></tr><tr><td></td><td>DP_ML</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP ML CONN P<3..0></td><td>68C3 68C4 68C5</td></tr><tr><td></td><td>DP_ML</td><td>DP_100D</td><td>DISPLAYPORT</td><td>DP ML CONN N<3..0></td><td>68B3 68C3 68C4 68C5</td></tr><tr><td></td><td>MCP_IFPAB_RSET</td><td>MCP_DV_COMP</td><td></td><td>MCP IFPAB RSET</td><td>18A3 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P	20D6 36A3		SATA_HDD_D2R	SATA_100D_HDD	SATA	SATA HDD D2R N	20D6 36A3		SATA_HDD_D2R	SATA_100D_HDD	SATA	SATA HDD D2R C P	7C5 36A7		SATA_HDD_D2R	SATA_100D_HDD	SATA	SATA HDD D2R C N	7C5 36A7		SATA_HDD_D2R	SATA_100D_HDD	SATA	SATA HDD D2R UF P	36A5		SATA_HDD_D2R	SATA_100D_HDD	SATA	SATA HDD D2R UF N	36A5		SATA_ODD_R2D	SATA_100D	SATA	SATA ODD R2D C P	20D6 36C2		SATA_ODD_R2D	SATA_100D	SATA	SATA ODD R2D C N	20D6 36C2		SATA_ODD_R2D	SATA_100D	SATA	SATA ODD R2D P	7B7 36B5		SATA_ODD_R2D	SATA_100D	SATA	SATA ODD R2D N	7B7 7C5 36B5		SATA_ODD_R2D	SATA_100D	SATA	SATA ODD R2D UF P	36C4		SATA_ODD_R2D	SATA_100D	SATA	SATA ODD R2D UF N	36C4		SATA_ODD_D2R	SATA_100D	SATA	SATA ODD D2R P	20D6 36B2		SATA_ODD_D2R	SATA_100D	SATA	SATA ODD D2R N	20D6 36B2		SATA_ODD_D2R	SATA_100D	SATA	SATA ODD D2R C P	7B7 36B5		SATA_ODD_D2R	SATA_100D	SATA	SATA ODD D2R C N	7B7 36B5		SATA_ODD_D2R	SATA_100D	SATA	SATA ODD D2R UF P	36B4		SATA_ODD_D2R	SATA_100D	SATA	SATA ODD D2R UF N	36B4		MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20A6
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP																																																																																																																																																																																																																																																																																																																																																																																																														
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	DP_ML	DP_100D	DISPLAYPORT	DP ML P<3..0>	67D1 68C1 68C8																																																																																																																																																																																																																																																																																																																																																																																																																
	DP_ML	DP_100D	DISPLAYPORT	DP ML C P<3..0>	68C2 68C7																																																																																																																																																																																																																																																																																																																																																																																																																
	DP_ML	DP_100D	DISPLAYPORT	DP ML N<3..0>	67D1 68B1 68C1 68C8																																																																																																																																																																																																																																																																																																																																																																																																																
	DP_ML	DP_100D	DISPLAYPORT	DP ML C N<3..0>	68B2 68C2 68C7																																																																																																																																																																																																																																																																																																																																																																																																																
	DP_AUX_CH	DP_100D	DISPLAYPORT	DP IG AUX CH P	1886 67C7																																																																																																																																																																																																																																																																																																																																																																																																																
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	DP_AUX_CH	DP_100D	DISPLAYPORT	DP AUX CH SW P	67C6																																																																																																																																																																																																																																																																																																																																																																																																																
	DP_AUX_CH	DP_100D	DISPLAYPORT	DP AUX CH SW N	67C5																																																																																																																																																																																																																																																																																																																																																																																																																
	DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	67C4 68C8																																																																																																																																																																																																																																																																																																																																																																																																																
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	MCP_HDMI_RSET	MCP_DV_COMP		MCP HDMI RSET	18A6 25C7																																																																																																																																																																																																																																																																																																																																																																																																																
	MCP_HDMI_VPROBE	MCP_DV_COMP		MCP HDMI VPROBE	18A6 25C7																																																																																																																																																																																																																																																																																																																																																																																																																
	LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P	18B3 66B3																																																																																																																																																																																																																																																																																																																																																																																																																
	LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK F P	7C7 66B2																																																																																																																																																																																																																																																																																																																																																																																																																
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	LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>	7C7 18B3 66C2																																																																																																																																																																																																																																																																																																																																																																																																																
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	MCP_IFPAB_RSET	MCP_DV_COMP		MCP IFPAB RSET	18A3 25C6																																																																																																																																																																																																																																																																																																																																																																																																																
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	SATA_HDD_R2D	SATA_100D_HDD	SATA	SATA HDD R2D P	7C5 36A7																																																																																																																																																																																																																																																																																																																																																																																																																
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				<div>MCP Constraints 1</div> <div>SYNC_MASTER=T18_MLB SYNC_DATE=01/04/2008</div> <div>NOTICE OF PROPRIETARY PROPERTY</div> <div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</div> <div>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</div> <div>II NOT TO REPRODUCE OR COPY IT</div> <div>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</div> <div> APPLE INC.</div> <div><table><tr><td>SIZE</td><td>DRAWING NUMBER</td><td>REV.</td></tr><tr><td>D</td><td>051-7537</td><td>A</td></tr><tr><td>SCALE</td><td>SHT</td><td>OF</td></tr><tr><td>NONE</td><td>102</td><td>109</td></tr></table></div>				SIZE	DRAWING NUMBER	REV.	D	051-7537	A	SCALE	SHT	OF	NONE	102	109																																																																																																																																																																																																																																																																																																																																																																																																		
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8	7	6	5	4	3	2	1				
PCI Bus Constraints											
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP				
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD				
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
PCI	*	=STANDARD	?								
CLK_PCI	*	8 MIL	?								
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.											
LPC Bus Constraints											
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP				
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD				
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
LPC	*	6 MIL	?								
CLK_LPC	*	8 MIL	?								
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.											
USB 2.0 Interface Constraints											
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP				
MCP_USB_RBBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD				
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT		SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT			
USB	*	=2x_DIELECTRIC	?		USB	TOP,BOTTOM	=4x_DIELECTRIC	?			
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.											
SMBus Interface Constraints											
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP				
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
SMB	*	=2x_DIELECTRIC	?								
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.											
HD Audio Interface Constraints											
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP				
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
HDA	*	=2x_DIELECTRIC	?								
MCP_HDA_COMP	*	8 MIL	?								
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.											
SIO Signal Constraints											
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP				
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
CLK_SLOW	*	8 MIL	?								
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.											
SPI Interface Constraints											
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP				
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD				
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT								
SPI	*	8 MIL	?								
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.											
ELECTRICAL_CONSTRAINT_SET											
NET_TYPE											
PHYSICAL											
SPACING											
MCP_DEBUG	PC1_55S	PC1	MCP_DEBUG<7..0>							1303	1907
PC1_AD	PC1_55S	PC1	PC1_AD<23..8>								
PC1_AD24	PC1_55S	PC1	PC1_AD<24>								
PC1_AD	PC1_55S	PC1	PC1_AD<31..25>								
PC1_AD	PC1_55S	PC1	PC1_PAR								
PC1_C_BE_L	PC1_55S	PC1	PC1_C_BE_L<3..0>								
PC1_CNTRL	PC1_55S	PC1	PC1_IRDY_L								
PC1_CNTRL	PC1_55S	PC1	PC1_DEVSEL_L								
PC1_CNTRL	PC1_55S	PC1	PC1_PERR_L								
PC1_CNTRL	PC1_55S	PC1	PC1_SERR_L								
PC1_CNTRL	PC1_55S	PC1	PC1_STOP_L								
PC1_CNTRL	PC1_55S	PC1	PC1_TRDY_L								
PC1_CNTRL	PC1_55S	PC1	PC1_FRAME_L								
PC1_BEQ0_L	PC1_55S	PC1	PC1_BEQ0_L							1902	1907
PC1_GNT0_L	PC1_55S	PC1	PC1_GNT0_L								
PC1_BEQ1_L	PC1_55S	PC1	PC1_BEQ1_L							1902	1907
PC1_GNT1_L	PC1_55S	PC1	PC1_GNT1_L								
PC1_INTW_L	PC1_55S	PC1	PC1_INTW_L								
PC1_INTX_L	PC1_55S	PC1	PC1_INTX_L								
PC1_INTY_L	PC1_55S	PC1	PC1_INTY_L								
PC1_INTZ_L	PC1_55S	PC1	PC1_INTZ_L								
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PC1_CLK33M MCP_R							1905	
CLK_PCI_55S	CLK_PCI	PC1	PC1_CLK33M MCP							1905	
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>							1983	1908 41D3 41D5
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L							1903	1908 41D5
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L							1983	2604
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC_R							1983	2604
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC							2601	1908
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M LPCPLUS							2681	41D3
USB_EXTN	USB_90D	USB	USB_EXTN_P							2603	37A8
	USB_90D	USB	USB_EXTN_N							2603	37A8
	USB_90D	USB	USB_EXTN_MUXED_P							3704	
	USB_90D	USB	USB_EXTN_MUXED_N							3704	
	USB_90D	USB	CONN_USB_EXTN_P							3703	
	USB_90D	USB	CONN_USB_EXTN_N							3703	
USB_CAMERA	USB_90D	USB	USB_CAMERA_P							2603	31B5
	USB_90D	USB	USB_CAMERA_N							2603	31B5
	USB_90D	USB	USB_CAMERA_CONN_P							705	31B7
	USB_90D	USB	USB_CAMERA_CONN_N							705	31B7
USB_BT	USB_90D	USB	USB_BT_P							2603	31B5
	USB_90D	USB	USB_BT_N							2603	31B5
	USB_90D	USB	CONN_USB2_BT_P							705	31B7
	USB_90D	USB	CONN_USB2_BT_N							705	31B7
USB_TP4D	USB_90D	USB	USB_TP4D_P							2603	47B8
	USB_90D	USB	USB_TP4D_N							2603	47B8
	USB_90D	USB	USB_TP4D_R_P							47B7	
	USB_90D	USB	USB_TP4D_R_N							47B7	
USB_IR	USB_90D	USB	USB_IR_P							2603	38C7
	USB_90D	USB	USB_IR_N							2603	38C7
USB_EXTB	USB_90D	USB	USB_EXTB_P							2603	37A4
	USB_90D	USB	USB_EXTB_N							2603	37A4
	USB_90D	USB	CONN_USB_EXTB_P							37A3	
	USB_90D	USB	CONN_USB_EXTB_N							37A3	
MCP_USB_RBBIAS	MCP_USB_RBBIAS		MCP_USB_RBBIAS_GND							20B4	
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK							1386	21C3 42D8
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA							1386	21C3 42D8
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK							21C3	42C8
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA							21C3	42C8
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK							21D2	51C7
HDA_BIT_CLK_R	HDA_55S	HDA	HDA_BIT_CLK_R							21A7	21D4
HDA_SYNC	HDA_55S	HDA	HDA_SYNC							21C2	51C7
HDA_SYNC_R	HDA_55S	HDA	HDA_SYNC_R							21A7	21D4
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L							21A7	21D4
HDA_RST_L	HDA_55S	HDA	HDA_RST_L							21D2	51B7
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0							21D7	51C7
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0_CODEC								
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT							21D2	51C7
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT_R							21A7	21D4
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP		MCP_HDA_PULLDN_COMP							21C7	
MCP_SMC_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R							21B3	26B4
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK							26B1	39C5
SPI_CLK	SPI_55S	SPI	SPI_CLK_R							21B3	41A5 41C8
	SPI_55S	SPI	SPI_CLK							41A1	50C5
	SPI_55S	SPI	SPI_ALT_CLK							41C5	41D3
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R							21B3	41A5 41C7
	SPI_55S	SPI	SPI_MOSI							41B1	50C4
	SPI_55S	SPI	SPI_ALT_MOSI							41C5	41D5
SPI_MISO	SPI_55S	SPI	SPI_MISO							21B3	41A5 41B7
	SPI_55S	SPI	SPI_MISO_R							50C4	
	SPI_55S	SPI	SPI_ALT_MISO							41B5	41D5
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L							21B3	41B7
	SPI_55S	SPI	SPI_CS0_L								
	SPI_55S	SPI	SPI_CS1_R_L								
	SPI_55S	SPI	SPI_CS1_R_L_USE_MLB							41B2	

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MCP RGMII (Ethernet) Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
MCP_BUF0_CLK	*	=3:1_SPACING	?				
ENET_MII	*	12 MIL	?				
SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4							
88E1116R (Ethernet PHY) Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT				
ENET_MDI	*	25 MIL	?				
SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4							

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

M97 SENSOR NET PROPERTIES

		NET_TYPE		
ELECTRICAL_CONSTRAINT_SET		PHYSICAL	SPACING	
		DIFFPAIR	CHGR CSO R P	444R 5783
		DIFFPAIR	CHGR CSO R N	444R 5783
		DIFFPAIR	CP1UTHMSNS D2 P	45C5
		DIFFPAIR	CP1UTHMSNS D2 N	45C5
		DIFFPAIR	CPU THERMO P	100C 45D5
		DIFFPAIR	CPU THERMD N	100C 45D5
		DIFFPAIR	ISNS CPUVTT P	4487
		DIFFPAIR	ISNS CPUVTT N	4487
		DIFFPAIR	ISNS P1V5S0MCP P	44C7
		DIFFPAIR	ISNS P1V5S0MCP N	44C7
		DIFFPAIR	ISNS P1VCORES0MCP P	44D8
		DIFFPAIR	ISNS P1VCORES0MCP N	44D8 61C4
		DIFFPAIR	MCPTHMSNS D2 P	7C7 45B5
		DIFFPAIR	MCPTHMSNS D2 N	7C7 45B5
		DIFFPAIR	MCP THMDIODE P	21C1 45C5
		DIFFPAIR	MCP THMDIODE N	21C1 45B5

M97 SPECIAL CONSTRAINTS

SYNC_MASTER=M97_MLB

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M97 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA_P1MM		MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	=STANDARD	=STANDARD	=STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.151 MM	0.100 MM	=STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL3, ISL4, ISL9, ISL10	Y	0.083 MM	0.083 MM		0.400 MM	0.400 MM
100_OHM_DIFF_HDD	TOP, BOTTOM	Y	0.095 MM	0.095 MM		0.400 MM	0.400 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4, ISL9, ISL10	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
SPACING_RULE_SET LAYER LINE-TO-LINE SPACING WEIGHT							
DEFAULT	*		0.1 MM	?			
STANDARD	*		=DEFAULT	?			
BGA_P1MM	*		=DEFAULT	?			
BGA_P2MM	*		=DEFAULT	?			
BGA_P3MM	*		=DEFAULT	?			
SPACING_RULE_SET LAYER LINE-TO-LINE SPACING WEIGHT							
1.5:1_SPACING	*		0.15 MM	?			
2:1_SPACING	*		0.2 MM	?			
2.5:1_SPACING	*		0.25 MM	?			
3:1_SPACING	*		0.3 MM	?			
4:1_SPACING	*		0.4 MM	?			
SPACING_RULE_SET LAYER LINE-TO-LINE SPACING WEIGHT							
2X_DIELECTRIC	TOP, BOTTOM		0.140 MM	?			
3X_DIELECTRIC	TOP, BOTTOM		0.210 MM	?			
4X_DIELECTRIC	TOP, BOTTOM		0.280 MM	?			
5X_DIELECTRIC	TOP, BOTTOM		0.350 MM	?			
2X_DIELECTRIC	*		0.126 MM	?			
3X_DIELECTRIC	*		0.189 MM	?			
4X_DIELECTRIC	*		0.252 MM	?			
5X_DIELECTRIC	*		0.315 MM	?			
NET_SPACING_TYPE1 NET_SPACING_TYPE2 AREA_TYPE SPACING_RULE_SET				NET_PHYSICAL_TYPE AREA_TYPE PHYSICAL_RULE_SET			
*	*	BGA_P1MM	BGA_P1MM	MEM_40S	BGA_P1MM	STANDARD	
MEM_CLK	*	BGA_P1MM	BGA_P2MM	MEM_40S_VDD	BGA_P1MM	STANDARD	
CLK_FSB	*	BGA_P1MM	BGA_P2MM				
CLK_LPC	*	BGA_P1MM	BGA_P2MM				
CLK_PCI	*	BGA_P1MM	BGA_P2MM				
CLK_PCIE	*	BGA_P1MM	BGA_P2MM				
CLK_SLOW	*	BGA_P1MM	BGA_P2MM				
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM				
M97 RULE DEFINITIONS							
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