1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,BLACK_PEARL,MLB,K92

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2009-05-19

pre-evt 11/22/10 rev3.11.3

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23	25	CPU & PCH XDP	K91_MLB	10/17/2010
24	26	USB HUBS	K92_BEN	06/29/2010
25	28	Chipset Support	K91_MLB	06/29/2010
26	29	DDR3 SO-DIMM Connector A	K92_YUN	06/14/2010
27	30	DDR3 Byte/Bit Swaps	K92_YUN	05/14/2010
28	31	DDR3 SO-DIMM Connector B	K92_YUN	06/14/2010
29	32	CPU Memory S3 Support	K17_MLB	04/26/2010
30	33	FSB/DDR3/FRAMEBUF Vref Margining	K91_YUN	08/26/2010
31	34	X19/ALS/CAMERA CONNECTOR	K91_MLB	10/21/2010
32	35	ExpressCard Connector	K92_ERIC	07/27/2010
33	36	T29 Host (1 of 2)	T29_REF	11/09/2010
34	37	T29 Host (2 of 2)	T29_REF	11/09/2010
35	38	T29 Power Support	T29_REF	11/09/2010
36	39	ETHERNET PHY (CAESAR IV)	K92_ERIC	10/19/2010
37	40	Ethernet Connector	K92_ERIC	08/24/2010
38	41	FireWire LLC/PHY (FW643)	K91_MLB	10/20/2010
39	42	FireWire Port & PHY Power	K91_MLB	10/20/2010
40	43	FireWire Connector	K91_MLB	07/22/2010
41	45	SATA Connectors	K92_ERIC	11/08/2010
42	46	External USB Connectors	K92_ERIC	08/24/2010
43	47	PROJECT SPECIFIC CONNS	K92_ERIC	07/22/2010
44	48	Front Flex Support	K17_MLB	04/26/2010
45	49	SMC	K91_BEN	07/12/2010
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55	59	Digital Accelerometer	K92_DINESH	06/02/2010
56	61	SPI ROM	K92_BEN	05/27/2010
57	62	AUDIO:CODEC	K92_KAVITHA	07/30/2010
58	63	AUDIO: LINE IN	K92_AUDIO	06/16/2010
59	65	AUDIO: HEADPHONE OUT	K92_KAVITHA	10/22/2010
60	66	AUDIO:SPEAKER AMP	K92_KAVITHA	10/22/2010
61	67	AUDIO: JACKS	K92_KAVITHA	11/02/2010
62	68	AUDIO: JACK TRANSLATORS	K92_KAVITHA	11/22/2010
63	69	DC-In & Battery Connectors	K92_CHANG	06/28/2010
64	70	PBus Supply & Battery Charger	K91_CHANG	07/21/2010
65	71	System Agent Supply	K91_CHANG	07/21/2010
66	72	5V / 3.3V Power Supply	K92_ERIC	08/30/2010
67	73	1.5V DDR3 Supply	K91_CHANG	07/21/2010
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69	75	CPU IMVP7 & AXG VCore Output	K92_ERIC	09/27/2010
70	76	CPU VCCIO (1.05V) Power Supply	K92_ERIC	09/23/2010
71	77	Misc Power Supplies	K91_CHANG	07/21/2010
72	78	Power FETs	K91_MLB	10/18/2010
73	79	Power Control 1/ENABLE	K92_YUAN	07/22/2010
74	80	Whistler PCI-E	K91_MLB	10/19/2010
75	81	Whistler CORE/FB POWER	K92_BEN	06/03/2010
76	82	Whistler FRAME BUFFER I/F	K18_MLB	04/27/2010
77	84	GDDR5 Frame Buffer A	K91_YUN	08/23/2010
78	85	GDDR5 Frame Buffer B	K91_YUN	08/23/2010
79	86	Whistler LVDS/DP/GPIO	K92_SUMA	10/21/2010
80	87	Whistler GPIOs & STRAPs	K91_MLB	07/17/2010
81	88	Whistler DP PWR/GNDs	K92_BEN	06/01/2010
82	89	GPU (Whistler) CORE SUPPLY	K91_CHANG	07/21/2010
83	90	LVDS Display Connector	K17_MLB	04/26/2010
84	92	Muxed Graphics Support	K92_YUN	06/25/2010
85	93	DisplayPort/T29 A MUXing	K91_MLB	10/22/2010
86	94	DisplayPort/T29 A Connector	K91_MLB	10/22/2010
87	95	1V0 GPU / 1V5 FB Power Supply	K91_CHANG	07/21/2010
88	96	Graphics MUX (GMUX)	K92_YUAN	07/28/2010
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102	121	PCH Power Aliases	K17_MLB	04/27/2010
103	130	DEBUG SENSORS AND ADC	K92_DINESH	09/07/2010
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105	132	Power Supplies BIST	K92_DINESH	08/23/2010

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8618	1	SCHEM,BLACK_PEARL,MLB,K92	SCH	CRITICAL	
820-2914	1	PCBF,BLACK_PEARL,MLB,K92	PCB	CRITICAL	

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TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Nov 23 20:44:38 2010

DRAWING TITLE: SCHEM,MLB,K92

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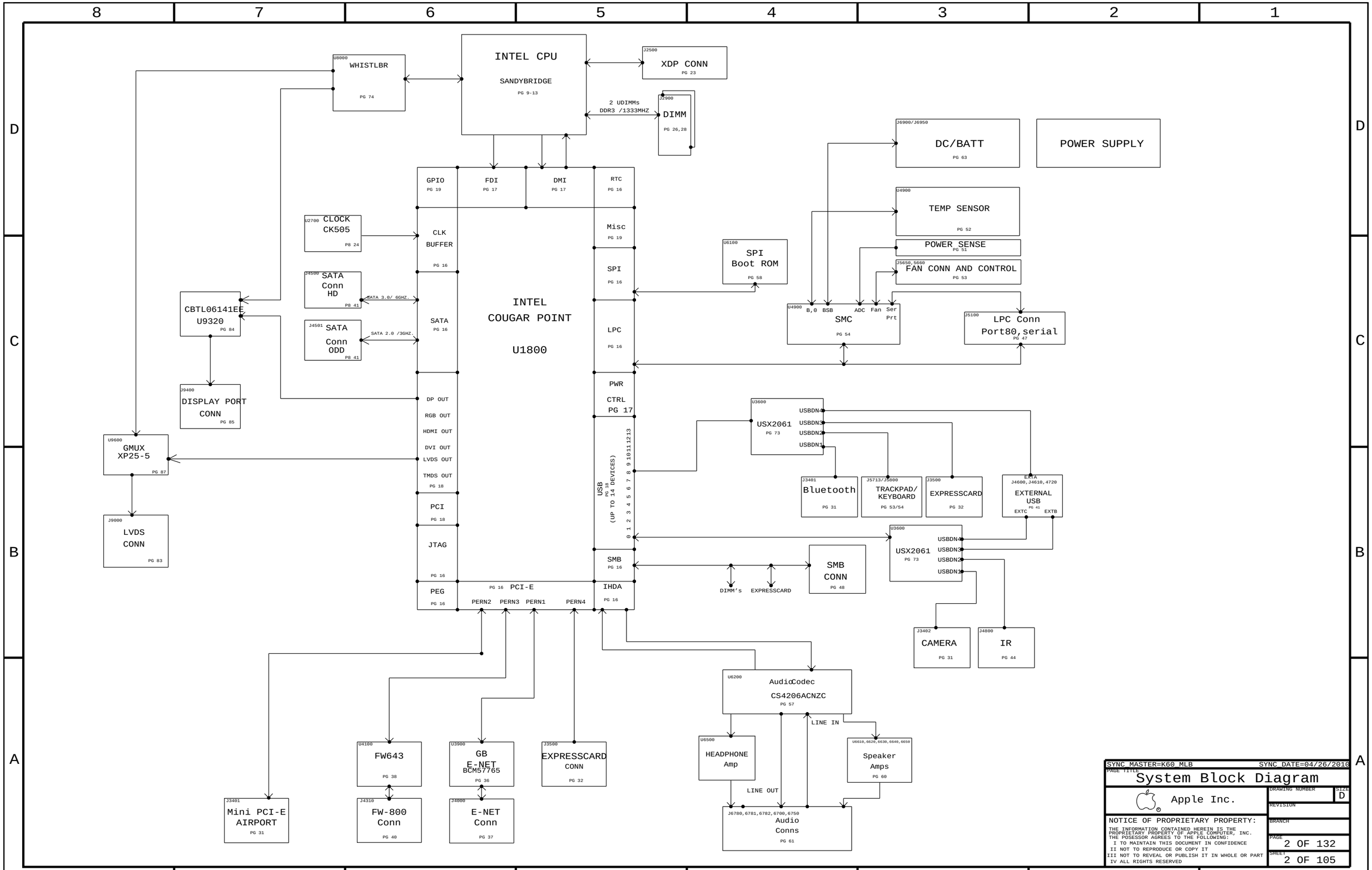

SYNC MASTER=K60 MLB SYNC DATE=04/26/2010

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System Block Diagram

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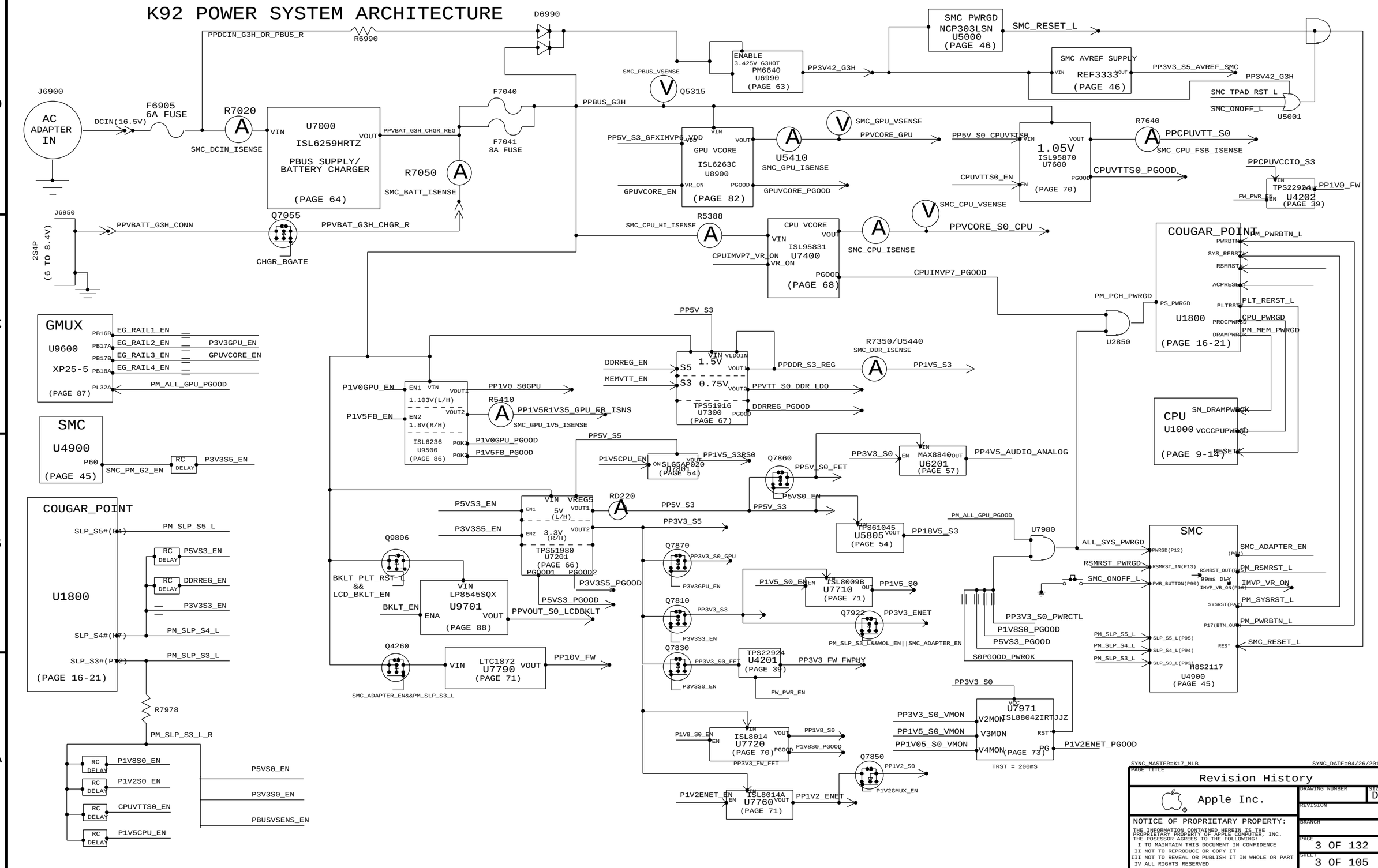
K92 POWER SYSTEM ARCHITECTURE



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PROTO2/EVT 11/11/10 rev3.0 for board 820-2914-05.brd release
PROTO2/EVT 11/15/10 rev3.6 for board 820-2914-06.brd release
PROTO2/EVT 11/19/10 rev3.7 for board 820-2914-07.brd release
EVT 11/22/10 rev3.9 for board 820-2914-07.brd release

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1303	PCBA,MLB,K92	K92_COMMON,CPU:2_2GHZ,FB_1G_SAMSUNG,EEEE_DG5Y
639-1464	PCBA,MLB,CFG2,K92	K92_COMMON,CPU:2_2GHZ,FB_1G_HYNIX,VRAM_HYNIX,EEEE_DG60
639-1466	PCBA,MLB,CFG3,K92	K92_COMMON,CPU:2_3GHZ,FB_1G_SAMSUNG,EEEE_DG62
639-1465	PCBA,MLB,CFG4,K92	K92_COMMON,CPU:2_3GHZ,FB_1G_HYNIX,VRAM_HYNIX,EEEE_DG61
085-1898	K92 MLB DEVELOPMENT BOM	K92_DEVEL:ENG

K92 BOM GROUPS

BOM GROUP	BOM OPTIONS
K92_COMMON	ALTERNATE,COMMON,K92_COMMON1,K92_COMMON2,K92_PROGPARTS
K92_COMMON1	CPUMEM_S0,EXT_HP_AMP,SMC_DEBUG_YES,USBHUB_2514B
K92_COMMON2	GPUVID_1P11V,HUB1_2NONREM,HUB2_2NONREM,KB_BL,ENET:B0,T29BST:Y,T29:YES,T29_DP_HPD:ALL_OR
K92_DEVEL:ENG	SNB_CPT_XDP,DEBUG_ADC,LPCPLUS:YES,VREFMRGN,GMUX_JTAG_CONN,S0PGOOD_ISL,BMON:ENG,CPURIPPLE_ENG,IMVPISNS_ENG,SDRVI2C:MCU
K92_DEVEL:PVT	SNB_CPT_XDP,LPCPLUS:YES,VREFMRGN_NOT
K92_PROGPARTS	SMC_PROG:EVT,BOOTROM_PROG:EVT,ENETROM_PROG:B0_NOSD,TPAD_PROG:EVT,T29ROM:PROG,GMUX_PROG,T29MCU:PROG
K92_PVT	VREFMRGN_NOT,XDP,XDP_CPU_BPM,BMON:PROD
SNB_CPT_XDP	XDP,XDP_CONN,XDP_CPU_BPM,XDP_PCH

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5Y]	CRITICAL	EEEE_DG5Y
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG60]	CRITICAL	EEEE_DG60
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG61]	CRITICAL	EEEE_DG61
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG62]	CRITICAL	EEEE_DG62

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4032	1	IC,CPU,SNB,SR00W,PRQ,D2,2.2,45W,4+2,1.30,6M,BGA	U1000	CRITICAL	CPU:2_2GHZ
337S4033	1	IC,CPU,SNB,SR00U,PRQ.D2,2.3,45W,4+2,1.30,8M,BGA	U1000	CRITICAL	CPU:2_3GHZ
337S4029	1	IC,PCH,COUGARPOINT SLH9D,PRQ,BD82HM63	U1800	CRITICAL	
343S0534	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN 8X8	U3900	CRITICAL	ENET:B0
343S0494	1	IC,ASIC,GBIT ETHNET&SD CTRLR,686 QFN 8X8	U3900	CRITICAL	ENET:A0
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
333S0543	4	IC,SGRAM,GDDR5,32MX32.1.25GHz,E-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_512_SAMSUNG
333S0564	4	IC,SDRAM,GDDR5,32MX32,1.25GHz,A-DIE1.35V	U8400,U8450,U8500,U8550	CRITICAL	FB_512_HYNIX
333S0571	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,C-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_SAMSUNG
333S0572	4	IC,SGRAM,GDDR5,64MX32,3.6GBPS,M-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB_1G_HYNIX
337S3936	1	IC,GPU,AMD,WHISTLER,962FCBGA,40NM,ES	U8000	CRITICAL	
338S0945	1	Light Ridge,S LHAJ,FCBGA,15x15mmm	U3600	CRITICAL	T29:YES
353S3055	1	IC, P13VEDP212,x2 DISPLAYPORT 2:1 MUX, QFN	U9390	CRITICAL	

Programmed Parts-All Builds

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0777	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	T29ROM:BLANK
341S2899	1	IC,T29 EEPROM,K92	U3690	CRITICAL	T29ROM:PROG
341S2384	1	IR,ENCORE II, CY7C63833-LFXC	U4800	CRITICAL	
335S0724	1	IC,GPU ROM,K91/F,K92	U8701	CRITICAL	GPUROM:BLANK
341S2957	1	IC,GPU ROM,K91/F,K92	U8701	CRITICAL	GPUROM:PROG
336S0042	1	IC,PLD,LATTICE,LFXP2-5E-5,132 BALL CSBGA	U9600	CRITICAL	GMUX_BLANK
341S2996	1	IC,GMUX,K92	U9600	CRITICAL	GMUX_PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2939	1	IC,PROGRAMMED MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:PROG

GPUROM will NOSUFFED @EVT

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
157S0058	157S0055		ALL	Delta alt to TDK Magnetics	
152S0896	152S0518		ALL	MAG LAYERS ALT TO CYNTEC	
152S0915	152S0796		ALL	MAG LAYERS ALT TO CYNTEC	
155S0457	155S0329		ALL	MAG LAYERS ALT TO MURATA	
516S0805	516S0806		ALL	FOXCONN ALT TO MOLEX	
353S2805	353S2603		ALL	Fairchild 8' alt to 6'wafer	
127S0111	127S0060		ALL	Rohm alt to Kemet	
353S3085	353S1658		ALL	ST Micro alt to LT	(U5850)
152S0905	152S1307		ALL	Cyntec (used on K90i) as alt	(L7630)
353S3055	353S3151		ALL	Pericom alt to NXP DP Mux	(U9390)
376S0855	376S0613		ALL	radar8515240 Toshiba FET	(Q3200, etc)
870-1939	870-1698		ALL	Silver alt to Gold tall pogo pins	
870-2015	870-1699		ALL	Silver alt to Gold short pogo pins	
376S0972	376S0612		ALL	add ROHM part as 2nd source	
138S0676	138S0691		ALL	add Murata part as 2nd source	
128S0327	128S0264		ALL	add NEC part as 2nd source	
376S0977	376S0859		ALL	add new part as 2nd source	
138S0681	138S0638		ALL	add new part as 2nd source	(Q3888,Q9430)

SMC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0895	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2855	1	IC,SMC,DEVELOPMENT-PROTO,K92	U4900	CRITICAL	SMC_PROG:PROTO0
341S2855	1	IC,SMC,DEVELOPMENT-PROTO1,K92	U4900	CRITICAL	SMC_PROG:PROTO1
341S2995	1	IC,SMC,DEVELOPMENT-PROTO2,K92	U4900	CRITICAL	SMC_PROG:PROTO2
341S2862	1	IC,SMC,DEVELOPMENT-EVT,K92	U4900	CRITICAL	SMC_PROG:EVT
341S2865	1	IC,SMC,DEVELOPMENT-DVT,K92	U4900	CRITICAL	SMC_PROG:DVT
341S2868	1	IC,SMC,DEVELOPMENT-PVT,K92	U4900	CRITICAL	SMC_PROG:PVT

EFI

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0740	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341S2893	1	IC,EFI,ROM,PROTO, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO0
341S2934	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S2991	1	IC,EFI,ROM,PROTO1, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PROTO2
341S2894	1	IC,EFI,ROM,EVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:EVT
341S2895	1	IC,EFI,ROM,DVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:DVT
341S2896	1	IC,EFI,ROM,PVT, K90/K90I/K91/K91F/K92	U6100	CRITICAL	BOOTROM_PROG:PVT

Ethernet

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0539	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENETROM_BLANK
341S2685	1	IC,ENET ROM,PROTO1,K92	U3990	CRITICAL	ENETROM_PROG:A0_SD
341S3027	1	IC,ENET ROM, PROTO2, EVT,DVT,PVT,K92	U3990	CRITICAL	ENETROM_PROG:B0_NOSD

PSOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S2902	1	IC,TP PSOC,PROTO,K90,K90i,K91,K91F,K92	U5701	CRITICAL	TPAD_PROG:PROTO1
341S3024	1	IC,TP PSOC,proto2,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:PROTO2
341S3024	1	IC,TP PSOC,proto1,EVT,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:EVT
341S3024	1	IC,TP PSOC,proto1,DVT,pVT,K90,K90i,K91,K91F,K92T	U5701	CRITICAL	TPAD_PROG:DVTPVT

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

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BOM Configuration

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Functional Test Points

FUNC_TEST

J5650 (LEFT FAN CONN)
- TRUE FAN_LT_PWM 52
- TRUE FAN_LT_TACH 52
- TRUE PP5V_S0 47 6,7,8 52 — 2 TPs
- TRUE GND 54 60 68 73 87 104 105 — 2 TPs

J5660 (RIGHT FAN CONN)
- TRUE FAN_RT_PWM 52
- TRUE FAN_RT_TACH 54 65 68 69 70 73 87 104 105
- 1148 PP5V_S0 47 6,7,8 52 41 — 2 TPs
- TRUE GND — 2 TPs

J6780 (MIC FR CONN)
- 1082 TRUE AUD_DMIC_CLK_FR
- 1082 TRUE AUD_DMIC_SDA_FR
- 1082 TRUE AUD_DMIC_PWR_FR
- TRUE GND — 2 TPs

J6783 (MIC BK CONN)
- 1146 TRUE AUD_DMIC_CLK_BK 61
- 1146 TRUE AUD_DMIC_SDA_BK 61
- 1146 TRUE AUD_DMIC_PWR_BK 61
- TRUE GND — 2 TPs

J6781 (LEFT SPEAKER)
- 1098 TRUE SPKRAMP_FL_OUT_P 60 61
- 1098 TRUE SPKRAMP_FL_OUT_N 60 61
- 1098 TRUE SPKRAMP_BL_OUT_P 60 61
- 1098 TRUE SPKRAMP_BL_OUT_N 60 61

J6782 (RIGHT & SUB SPEAKER)
- 1098 TRUE SPKRAMP_LFE_OUT_P 60 61
- 1098 TRUE SPKRAMP_LFE_OUT_N 60 61
- 1098 TRUE SPKRAMP_FR_OUT_P 60 61
- 1098 TRUE SPKRAMP_FR_OUT_N 60 61
- 1098 TRUE SPKRAMP_BR_OUT_P 60 61
- 1098 TRUE SPKRAMP_BR_OUT_N 60 61

J9000 (LVDS CONN)
- 1098 TRUE PP3V3_SW_LCD 83 84 85 86 87 88 — 2 TPs
- 1098 TRUE PP3V3_S0 6,7,32 33 35 36 — 2 TPs
- 1097 TRUE PPVOUT_S0_LCDBKLT 23 25 26 38 39 40 41 — 2 TPs
- 1098 TRUE LVDS_DDC_CLK 62 72 73 88 89 91 100 102
- 1098 TRUE LVDS_DDC_DATA 83 84
- 1098 TRUE LVDS_CONN_A_DATA_P<0> 83 84 99
- 1098 TRUE LVDS_CONN_A_DATA_N<0> 83 84 99
- 1098 TRUE LVDS_CONN_A_DATA_P<1> 83 84 99
- 1098 TRUE LVDS_CONN_A_DATA_N<1> 83 84 99
- 1098 TRUE LVDS_CONN_A_DATA_P<2> 83 84 99
- 1098 TRUE LVDS_CONN_A_DATA_N<2> 83 84 99
- 1098 TRUE LVDS_CONN_A_CLK_F_P 83 99
- 1098 TRUE LVDS_CONN_A_CLK_F_N 83 99
- 1098 TRUE LVDS_CONN_B_DATA_P<0> 83 84 99
- 1098 TRUE LVDS_CONN_B_DATA_N<0> 83 84 99
- 1098 TRUE LVDS_CONN_B_DATA_P<1> 83 84 99
- 1098 TRUE LVDS_CONN_B_DATA_N<1> 83 84 99
- 1098 TRUE LVDS_CONN_B_DATA_P<2> 83 84 99
- 1098 TRUE LVDS_CONN_B_DATA_N<2> 83 84 99
- 1098 TRUE LVDS_CONN_B_CLK_F_P 83 99
- 1098 TRUE LVDS_CONN_B_CLK_F_N 83 99
- 1098 TRUE LED_RETURN_1 83 89
- 1098 TRUE LED_RETURN_2 83 89
- 1098 TRUE LED_RETURN_3 83 89
- 1098 TRUE LED_RETURN_4 83 89
- 1098 TRUE LED_RETURN_5 83 89
- 1098 TRUE LED_RETURN_6 83 89
- TRUE GND — 5 TPs

J4500 (SATA ODD CONN)
- 1102 TRUE PP5V_SW_ODD 41 104 — 3 TPs
- 1102 TRUE SMC_ODD_DETECT 41 45
- 1102 TRUE SATA_ODD_D2R_UF_P 41 94
- 1102 TRUE SATA_ODD_D2R_UF_N 41 94
- 1102 TRUE SATA_ODD_R2D_P 41 94
- 1102 TRUE SATA_ODD_R2D_N 41 94
- TRUE GND — 4 TPs

J4501 (SATA HDD CONN)
- 1118 TRUE PP5V_S0_HDD_FLT 41 — 3 TPs
- 1118 TRUE SATA_HDD_R2D_P 41 94
- 1118 TRUE SATA_HDD_R2D_N 41 94
- 1118 TRUE SATA_HDD_D2R_C_P 6 41 94
- 1118 TRUE SATA_HDD_D2R_C_N 6 41 94
- 1118 TRUE PP5V_S3_IR_R 6 44
- 1118 TRUE IR_RX_OUT 6 44
- 1118 TRUE SYS_LED_ANODE_R 6 44
- TRUE GND — 4 TPs

J5815 (KBD BACKLIGHT CONN)
- 1116 TRUE KBDLED_ANODE 54
- 1116 TRUE SMC_KDBLED_PRESENT_L 54
- TRUE GND

J6995 (BAT LED CONN)
- 1116 TRUE PP3V42_G3H 6 7 25 42 44 45 46 47 48 53 63 64 73 104
- 1116 TRUE SMBUS_SMC_BSA_SDA 6 45 48 63 64 98
- 1116 TRUE SMBUS_SMC_BSA_SCL 6 45 48 63 64 98
- 1116 TRUE SMC_BIL_BUTTON_L 45 46 63
- 1116 TRUE SMC_LID_R 6 44
- TRUE GND

J6900 (DC POWER CONN)
- 1116 TRUE ADAPTER_SENSE 63
- 1116 TRUE PP18V5_DCIN_FUSE 63 — 3 TPs
- TRUE GND — 4 TPs

J3401(AIRPORT/BT CONN)
- 1160 TRUE WIFI_EVENT_L 31 45 46
- 1160 TRUE PCIE_AP_R2D_P 31 95
- 1160 TRUE PCIE_AP_R2D_N 31 95
- 1160 TRUE PCIE_AP_D2R_P 16 31 95
- 1160 TRUE PCIE_AP_D2R_N 16 31 95
- 1160 TRUE PCIE_CLK100M_AP_CONN_P 31 100
- 1160 TRUE PCIE_CLK100M_AP_CONN_N 31 100
- 1160 TRUE AP_CLKREQ_O_L 31
- 1160 TRUE PCIE_WAKE_L 6 17 25 31 32 85
- 1160 TRUE AP_RESET_CONN_L 31
- 1160 TRUE PP3V3_WLAN 31 46 — 3 TP needed
- 1160 TRUE PP3V3_S3_BT_F 31
- 1160 TRUE SMBUS_SMC_0_S0_SDA 31 45 48 51 80 98
- 1160 TRUE SMBUS_SMC_0_S0_SCL 31 45 48 51 80 98
- 1160 TRUE USB_BT_P 24 31 94
- 1160 TRUE USB_BT_N 24 31 94
- TRUE GND — 6 TP needed

J3402 (CAMERA/ALS CONN)
- 1160 TRUE USB_CAMERA_CONN_P 31 94
- 1160 TRUE USB_CAMERA_CONN_N 31 94
- 1163 TRUE PP5V_S3_ALSCAMERA_F 31
- 1147 TRUE SMBUS_SMC_A_S3_SDA 6 31 45 48 54 55 98
- 1147 TRUE SMBUS_SMC_A_S3_SCL 6 31 45 48 54 55 98
- TRUE GND — 2 TP needed

J3500 (EXPRESS CARD CONN)
- 1160 TRUE PP1V5_S0_EXCARD_SWITCH 32
- 1160 TRUE PCIE_WAKE_L 6 17 25 31 32 85
- 1160 TRUE SMBUS_PCH_CLK 16 23 26 28 30 32 41 48 62 89 95
- 1160 TRUE SMBUS_PCH_DATA 16 23 26 28 30 32 41 48 62 89 95
- 1160 TRUE PP3V3_S0_EXCARD_SWITCH 32
- 1160 TRUE PP3V3_S3_EXCARD_SWITCH 32
- 1160 TRUE USB2_EXCARD_CONN_N 32 100
- 1160 TRUE USB2_EXCARD_CONN_P 32 100
- 1160 TRUE EXCARD_CPUSB_L 32
- 1160 TRUE EXCARD_CLKREQ_CONN_L 32
- 1160 TRUE EXCARD_CPPE_L 32
- 1160 TRUE PLT_RESET_SWITCH_L 32
- 1160 TRUE PCIE_EXCARD_D2R_P 16 32 100
- 1160 TRUE PCIE_EXCARD_D2R_N 16 32 100
- 1160 TRUE PCIE_EXCARD_R2D_P 32 100
- 1160 TRUE PCIE_EXCARD_R2D_N 32 100
- 1160 TRUE PCIE_CLK100M_EXCARD_CONN_P 32 100
- 1160 TRUE PCIE_CLK100M_EXCARD_CONN_N 32 100

J5800 (IPD FLEX CONN)
- 1160 TRUE PP3V3_S3 6,7,8 18 24 25 29 30 31 32 48 49 50 54 55 73 88 104
- 1160 TRUE PP18V5_S4 6 54
- 1160 TRUE PP3V3_S4 6 7 46 53 54 72
- 1162 TRUE Z2_CS_L 53 54
- 1160 TRUE Z2_DEBUG3 53 54
- 1160 TRUE Z2_MISO 53 54
- 1160 TRUE Z2_BOOST_EN 54
- 1160 TRUE Z2_MOSI 53 54
- 1160 TRUE Z2_CLKIN 53 54
- 1160 TRUE Z2_KEY_ACT_L 53 54
- 1160 TRUE Z2_RESET 53 54
- 1160 TRUE Z2_HOST_INTN 53 54
- 1160 TRUE Z2_SCLK 53 54
- 1160 TRUE PSOC_F_CS_L 53 54
- 1160 TRUE PICKB_L 53 54
- 1160 TRUE PSOC_MISO 53 54
- 1160 TRUE PSOC_MOSI 53 54
- 1160 TRUE PSOC_SCLK 53 54
- 1160 TRUE SMBUS_SMC_A_S3_SCL 6 31 45 48 54 55 98
- 1160 TRUE SMBUS_SMC_A_S3_SDA 6 31 45 48 54 55 98
- TRUE GND — 2 TPS

J6950 (MAIN BATT CONN)
- 1116 TRUE PPVBAT_G3H_CONN 63 64 — 5 TPs
- 1116 TRUE SMBUS_SMC_BSA_SCL 6 45 48 63 64 98
- 1116 TRUE SMBUS_SMC_BSA_SDA 6 45 48 63 64 98
- 1116 TRUE SYS_DETECT_L 63
- TRUE GND — 5 TPs

J4800 (FRONT CABLE CONN)
- 1116 TRUE PP3V42_G3H_LIDSWITCH_R 44
- 1116 TRUE PP5V_S3_IR_R 6 44
- 1116 TRUE SMC_LID_R 6 44
- 1116 TRUE IR_RX_OUT 6 44
- 1116 TRUE SYS_LED_ANODE 44 46
- TRUE GND

J5713 (KEY BOARD CONN)
- 1110 TRUE PP3V3_S4 6 7 46 53 54 72
- 1110 TRUE PP3V42_G3H 28 53 63 64 6 7 25 42 44 45 46 47 73 104 53
- 1110 TRUE WS_KBD1
- 1110 TRUE WS_KBD2 53
- 1110 TRUE WS_KBD3 53
- 1110 TRUE WS_KBD4 53
- 1110 TRUE WS_KBD5 53
- 1110 TRUE WS_KBD6 53
- 1110 TRUE WS_KBD7 53
- 1110 TRUE WS_KBD8 53
- 1110 TRUE WS_KBD9 53
- 1110 TRUE WS_KBD10 53
- 1110 TRUE WS_KBD11 53
- 1110 TRUE WS_KBD12 53
- 1110 TRUE WS_KBD13 53
- 1110 TRUE WS_KBD14 53
- 1110 TRUE WS_KBD15_CAP 53
- 1110 TRUE WS_KBD16_NUM 53
- 1110 TRUE WS_KBD17 53
- 1110 TRUE WS_KBD18 53
- 1110 TRUE WS_KBD19 53
- 1110 TRUE WS_KBD20 53
- 1110 TRUE WS_KBD21 53
- 1110 TRUE WS_KBD22 53
- 1110 TRUE WS_KBD23 53
- 1110 TRUE WS_KBD_ONOFF_L 53
- 1110 TRUE WS_LEFT_SHIFT_KBD 53
- 1110 TRUE WS_LEFT_OPTION_KBD 53
- 1110 TRUE WS_CONTROL_KBD 53
- TRUE GND — 2 TP needed

POWER RAILS

FUNC_TEST
- TRUE PM_SLP_S3_L 17 29 45 73
- TRUE PPBUS_G3H 7 8 35 39 49 50 63 64 98
- TRUE PP3V42_G3H 104 6 7 25 42 44 45 46 47 48 53 63 64 73
- TRUE PP5V_S3
- TRUE PP5V_S0 87 104 105 6 7 8 23 41 47 52 54 65 68 69 70 73
- TRUE PPVCORE_S0_CPU 7 12 14 49 69 105
- TRUE PP3V3_S5 — 2 TPs
- TRUE PP3V3_S3 54 55 6 7 8 18 24 25 29 30 31 32 48 49 50
- TRUE PP3V3_S0 73 88 104 7 12 23 25 26 28 39 40 41 46 48 49 50 51 52 54 62 69 73 80 83 84 85 88 89 91 100 102
- TRUE PP1V2_S0 7 14 29 25 71 72 88 102
- TRUE PP1V8_S0 7 30 67
- TRUE PPVTTDDR_S3
- TRUE PPVP_FW 7 39 40
- TRUE PP3V3_S0GPU 7 72 75 79 80 82 84
- TRUE PP1V8_S0GPU 7 75 79 81 103
- TRUE PPVCORE_GPU 7 49 75 82
- TRUE PP1V8_S0GPU_ISNS_R 7 72 103
- TRUE PP3V3_S5_AVREF_SMC 45 46
- TRUE PP18V5_S4 6 54
- TRUE PPDCIN_G3H 7 49 63 64

FUNC_TEST
- TRUE SYS_LED_ANODE_R 6 44
- TRUE LPC_CLK33M_LPCPLUS 25 47 95
- TRUE LPC_AD<0..3> 16 45 47 88 95
- TRUE SPI_ALT_MOSI 47
- TRUE SPI_ALT_MISO 47
- TRUE LPC_FRAME_L 16 45 47 88 95
- TRUE PM_CLKRUN_L 17 45 47
- TRUE SMC_TMS 45 46 47
- TRUE LPCPLUS_RESET_L 25 47 88 95
- TRUE SMC_TDO 45 46 47
- TRUE SMC_TRST_L 45 47
- TRUE SMC_MD1 45 47
- TRUE SMC_TX_L 42 45 46 47
- TRUE SPIROM_USE_MLB 19 47 56
- TRUE SPI_ALT_CLK 47
- TRUE SPI_ALT_CS_L 47
- TRUE LPC_SERIRQ 16 45 47
- TRUE LPC_PWRDWN_L 17 45 47
- TRUE SMC_TDI 45 46 47
- TRUE SMC_TCK 45 46 47
- TRUE SMC_RESET_L 45 46 47 64
- TRUE SMC_NMI 45 47
- TRUE SMC_RX_L 42 45 46 47
- TRUE LPCPLUS_GPIO 19 47
- TRUE ISSP_SCLK_P1_1
- TRUE ISSP_SDATA_P1_0
- TRUE SMC_ONOFF_L 45 46 53
- TRUE PM_SYSRST_L 17 25 45
- TRUE LCD_BKLT_PWM 88 89

NO_TEST=TRUE

- TRUE T29_D2R_P<1..0> 33 85 97
- TRUE T29_D2R_N<1..0> 33 85 97
- TRUE T29_D2R_C_P<1..0> 85 86 97
- TRUE T29_D2R_C_N<1..0> 85 86 97
- TRUE T29_R2D_C_P<1..0> 33 85 97
- TRUE T29_R2D_C_N<1..0> 33 85 97
- TRUE T29_R2D_P<1..0> 85 97
- TRUE T29_R2D_N<1..0> 85 97
- TRUE T29DPA_ML_P<3..0> 85 86 97
- TRUE T29DPA_ML_N<3..0> 85 86 97
- TRUE DP_T29SNK0_AUXCH_C_P 33 79 97
- TRUE DP_T29SNK0_AUXCH_C_N 33 79 97
- TRUE DP_T29SNK0_AUXCH_P 33 97
- TRUE DP_T29SNK0_AUXCH_N 33 97
- TRUE DP_T29SNK0_ML_C_P<3..0> 33 79 97
- TRUE DP_T29SNK0_ML_C_N<3..0> 33 79 97
- TRUE DP_T29SNK0_ML_P<3..0> 33 97
- TRUE DP_T29SNK0_ML_N<3..0> 33 97
- TRUE DP_T29SNK1_AUXCH_C_P 33 79 97
- TRUE DP_T29SNK1_AUXCH_C_N 33 79 97
- TRUE DP_T29SNK1_AUXCH_P 33 97
- TRUE DP_T29SNK1_AUXCH_N 33 97
- TRUE DP_T29SNK1_ML_C_P<3..0> 33 79 97
- TRUE DP_T29SNK1_ML_C_N<3..0> 33 79 97
- TRUE DP_T29SNK1_ML_P<3..0> 33 97
- TRUE DP_T29SNK1_ML_N<3..0> 33 97
- TRUE TP_DP_T29SRC_AUXCH_CN 33
- TRUE TP_DP_T29SRC_AUXCH_CP 33
- TRUE TP_DP_T29SRC_ML_CP<3..0> 33
- TRUE TP_DP_T29SRC_ML_CN<3..0> 33
- TRUE DP_SDRVA_ML_C_P<0> 85 97
- TRUE DP_SDRVA_ML_C_N<0> 85 97
- TRUE DP_SDRVA_ML_C_P<2> 85 97
- TRUE DP_SDRVA_ML_C_N<2> 85 97
- TRUE DP_SDRVA_ML_P<0> 85 97
- TRUE DP_SDRVA_ML_N<0> 85 97
- TRUE DP_SDRVA_ML_P<2> 85 97
- TRUE DP_SDRVA_ML_N<2> 85 97
- TRUE TP_T29_PCIE_RESET0_L 33
- TRUE TP_T29_PCIE_RESET1_L 33
- TRUE TP_T29_PCIE_RESET2_L 33
- TRUE TP_T29_PCIE_RESET3_L 33
- TRUE T29DPA_D2R1_AUXCH_N 86 97
- TRUE T29DPA_D2R1_AUXCH_P 86 97
- TRUE T29_D2R1_BIAS
- TRUE DP_EXTA_ML_P<3..0> 85
- TRUE DP_A_BIAS_N_0 8 85
- TRUE DP_A_BIAS_P_0 8 85
- TRUE DP_A_BIAS_N_2 8 85
- TRUE DP_A_BIAS_P_2 8 85
- TRUE DP_A_BIAS 85
- TRUE DP_SDRVA_ML_R_N<0> 85 97
- TRUE DP_SDRVA_ML_R_P<0> 85 97
- TRUE DP_SDRVA_ML_R_N<2> 85 97
- TRUE DP_SDRVA_ML_R_P<2> 85 97
- TRUE T29_A_BIAS_R2D_N0 8 85
- TRUE T29_A_BIAS_R2D_P0 8 85
- TRUE T29_A_BIAS_R2D_N1 8 85
- TRUE T29_A_BIAS_R2D_P1 8 85
- TRUE SATA_HDD_R2D_UF_N 6 41 94
- TRUE SATA_HDD_R2D_UF_P 6 41 94
- TRUE SATA_HDD_R2D_RC_UF_N 41 94
- TRUE SATA_HDD_R2D_RC_UF_P 41 94
- TRUE SATA_HDD_R2D_RDRVR_OUT_N 41 94
- TRUE SATA_HDD_R2D_RDRVR_OUT_P 41 94
- TRUE SATA_HDD_R2D_RDRVR_IN_N 41 94
- TRUE SATA_HDD_R2D_RDRVR_IN_P 41 94
- TRUE SATA_HDD_R2D_C_N 16 41 94
- TRUE SATA_HDD_R2D_C_P 16 41 94
- TRUE SATA_HDD_R2D_UF_N 6 41 94
- TRUE SATA_HDD_R2D_UF_P 6 41 94
- TRUE SATA_HDD_D2R_N 16 41 94
- TRUE SATA_HDD_D2R_P 16 41 94
- TRUE SATA_HDD_D2R_RDRVR_OUT_N 41 94
- TRUE SATA_HDD_D2R_RDRVR_OUT_P 41 94
- TRUE SATA_HDD_D2R_RDRVR_IN_N 41 94
- TRUE SATA_HDD_D2R_RDRVR_IN_P 41 94
- TRUE SATA_HDD_D2R_C_N 6 41 94
- TRUE SATA_HDD_D2R_C_P 6 41 94

NO_TEST=TRUE

- TRUE TP_DVPCLK 79
- TRUE TP_DVPCNTL<2..0> 79
- TRUE TP_DVPCNTL_M<1..0> 79
- TRUE TP_DVPDATA<23..0> 79
- TRUE TP_GPU_JTAG_TRST_L 79 80
- TRUE TP_DC_TEST_A4 12
- TRUE TP_DC_TEST_D1 12
- TRUE TP_EDP_TX_P<3..0> 9
- TRUE TP_T29_SENSOR_ALERT 51
- TRUE DMI_S2N_P<1..0> 9 17 92
- TRUE DMI_S2N_N<1..0> 9 17 92
- 1160 TRUE DMI_N2S_P<1> 9 17 92
- 1160 TRUE DMI_N2S_N<1> 9 17 92
- 1160 TRUE DMI_N2S_P<3> 9 17 92
- 1160 TRUE DMI_N2S_N<3> 9 17 92

NC NO_TESTs

NO_TEST
- 17 6 NC_CRT_IG_BLUE — TRUE MAKE_BASE=TRUE — NC_CRT_IG_BLUE 6 17
- 17 6 NC_CRT_IG_GREEN — TRUE MAKE_BASE=TRUE — NC_CRT_IG_GREEN 6 17
- 17 6 NC_CRT_IG_RED — TRUE MAKE_BASE=TRUE — NC_CRT_IG_RED 6 17
- 17 6 NC_CRT_IG_DDC_CLK — TRUE MAKE_BASE=TRUE — NC_CRT_IG_DDC_CLK 6 17
- 17 6 NC_CRT_IG_DDC_DATA — TRUE MAKE_BASE=TRUE — NC_CRT_IG_DDC_DATA 6 17
- 17 6 NC_CRT_IG_HSYNC — TRUE MAKE_BASE=TRUE — NC_CRT_IG_HSYNC 6 17
- 17 6 NC_CRT_IG_VSYNC — TRUE MAKE_BASE=TRUE — NC_CRT_IG_VSYNC 6 17
- 18 6 NC_LVDS_IG_CTRL_CLK — TRUE MAKE_BASE=TRUE — NC_LVDS_IG_CTRL_CLK 6 18
- 18 6 NC_LVDS_IG_CTRL_DATA — TRUE MAKE_BASE=TRUE — NC_LVDS_IG_CTRL_DATA 6 18
- 18 6 NC_PCH_LVDS_VBG — TRUE MAKE_BASE=TRUE — NC_PCH_LVDS_VBG 6 18
- 16 6 NC_HDA_SDIN1 — TRUE MAKE_BASE=TRUE — NC_HDA_SDIN1 6 16
- 16 6 NC_HDA_SDIN2 — TRUE MAKE_BASE=TRUE — NC_HDA_SDIN2 6 16
- 16 6 NC_HDA_SDIN3 — TRUE MAKE_BASE=TRUE — NC_HDA_SDIN3 6 16

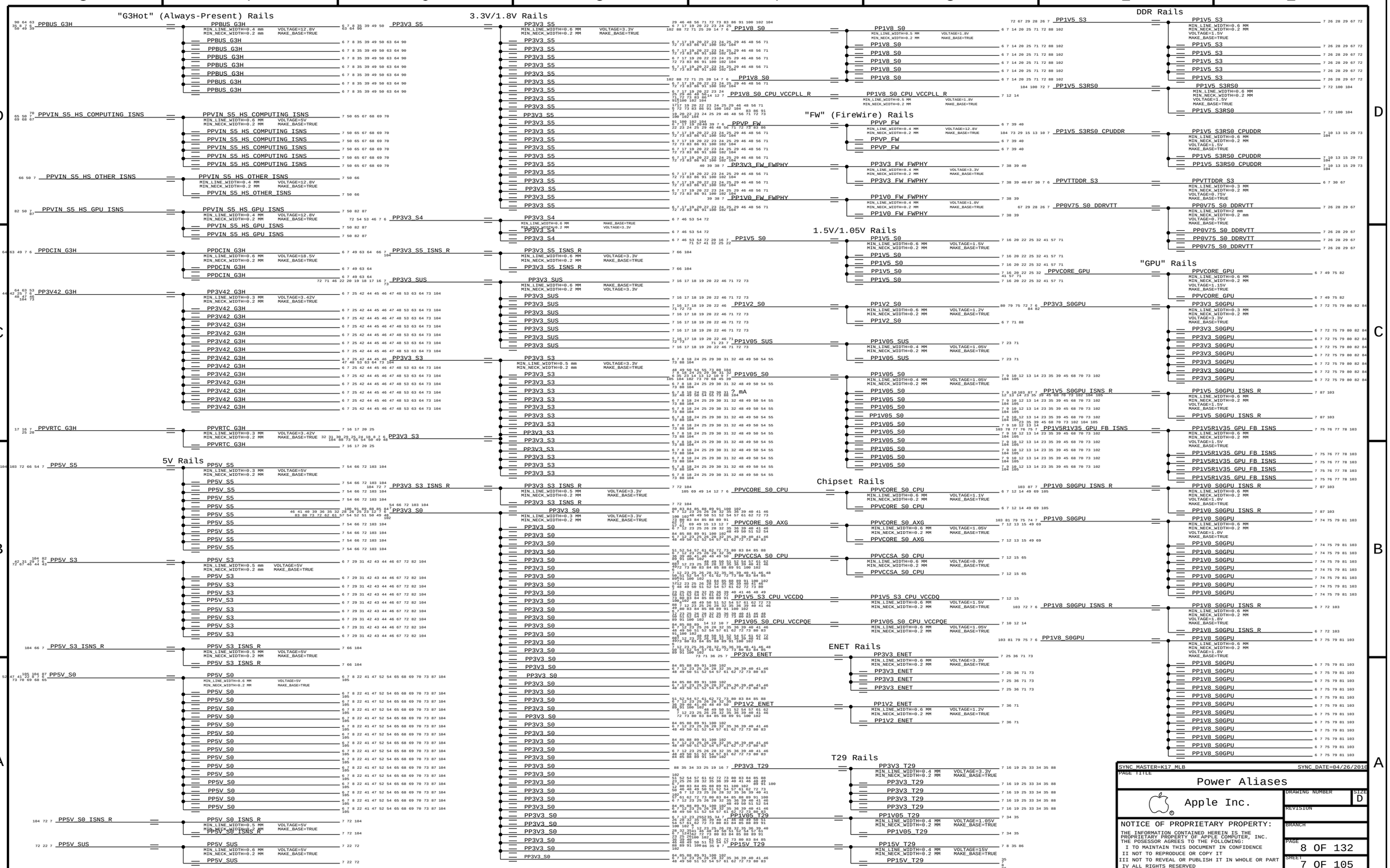
NC NO_TESTs

NO_TEST
- TP_PCI_AD<31..0> — TRUE MAKE_BASE=TRUE — NC_PCI_AD<31..0>
- TP_PCI_C_BE_L<3..0> — TRUE MAKE_BASE=TRUE — NC_PCI_C_BE_L<3..0>
- 6 NC_PCI_GNT3_L — TRUE MAKE_BASE=TRUE — NC_PCI_GNT3_L 6
- 6 NC_PCI_GNT2_L — TRUE MAKE_BASE=TRUE — NC_PCI_GNT2_L 6
- 6 NC_PCI_GNT1_L — TRUE MAKE_BASE=TRUE — NC_PCI_GNT1_L 6
- 6 NC_PCI_GNT0_L — TRUE MAKE_BASE=TRUE — NC_PCI_GNT0_L 6
- 6 NC_PCI_PAR — TRUE MAKE_BASE=TRUE — NC_PCI_PAR 6
- 6 NC_PCI_RESET_L — TRUE MAKE_BASE=TRUE — NC_PCI_RESET_L 6
- 18 6 NC_PCI_PME_L — TRUE MAKE_BASE=TRUE — NC_PCI_PME_L 6 18
- 18 6 NC_PCI_CLK33M_OUT3 — TRUE MAKE_BASE=TRUE — NC_PCI_CLK33M_OUT3 6 18
- TP_NV_DQ<15..0> — TRUE MAKE_BASE=TRUE — NC_NV_DQ<15..0>
- TP_NV_DQS<1..0> — TRUE MAKE_BASE=TRUE — NC_NV_DQS<1..0>
- TP_NV_CE_L<3..0> — TRUE MAKE_BASE=TRUE — NC_NV_CE_L<3..0>
- 6 NC_NV_ALE — TRUE MAKE_BASE=TRUE — NC_NV_ALE 6
- 6 NC_NV_CLE — TRUE MAKE_BASE=TRUE — NC_NV_CLE 6
- 6 NC_NV_RB_L — TRUE MAKE_BASE=TRUE — NC_NV_RB_L 6
- TP_NV_WR_RE_L<1..0> — TRUE MAKE_BASE=TRUE — NC_NV_WR_RE_L<1..0>
- TP_NV_WE_CK_L<1..0> — TRUE MAKE_BASE=TRUE — NC_NV_WE_CK_L<1..0>
- 6 NC_PCIE_CLK100M_PE4N — TRUE MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE4N 6
- 6 NC_PCIE_CLK100M_PE4P — TRUE MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE4P 6
- 16 6 NC_PCIE_CLK100M_PE5N — TRUE MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE5N 6 16
- 16 6 NC_PCIE_CLK100M_PE5P — TRUE MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE5P 6 16
- 19 6 NC_PCIE_CLK100M_PE6N — TRUE MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE6N 6 19
- 19 6 NC_PCIE_CLK100M_PE6P — TRUE MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE6P 6 19
- 19 6 NC_PCIE_CLK100M_PE7N — TRUE MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE7N 6 19
- 19 6 NC_PCIE_CLK100M_PE7P — TRUE MAKE_BASE=TRUE — NC_PCIE_CLK100M_PE7P 6 19
- 53 6 NC_PSOC_P1_3 — TRUE MAKE_BASE=TRUE — NC_PSOC_P1_3 6 53
- 6 NC_SATA_C_D2RN — TRUE MAKE_BASE=TRUE — NC_SATA_C_D2RN 6
- 6 NC_SATA_C_D2RP — TRUE MAKE_BASE=TRUE — NC_SATA_C_D2RP 6
- 6 NC_SATA_C_R2D_CN — TRUE MAKE_BASE=TRUE — NC_SATA_C_R2D_CN 6
- 6 NC_SATA_C_R2D_CP — TRUE MAKE_BASE=TRUE — NC_SATA_C_R2D_CP 6
- 16 6 NC_SATA_D_D2RN — TRUE MAKE_BASE=TRUE — NC_SATA_D_D2RN 6 16
- 16 6 NC_SATA_D_D2RP — TRUE MAKE_BASE=TRUE — NC_SATA_D_D2RP 6 16
- 16 6 NC_SATA_D_R2D_CN — TRUE MAKE_BASE=TRUE — NC_SATA_D_R2D_CN 6 16
- 16 6 NC_SATA_D_R2D_CP — TRUE MAKE_BASE=TRUE — NC_SATA_D_R2D_CP 6 16
- 6 NC_SATA_SSD2_D2RN — TRUE MAKE_BASE=TRUE — NC_SATA_SSD2_D2RN 6
- 6 NC_SATA_SSD2_D2RP — TRUE MAKE_BASE=TRUE — NC_SATA_SSD2_D2RP 6
- 6 NC_SATA_SSD2_R2D_CN — TRUE MAKE_BASE=TRUE — NC_SATA_SSD2_R2D_CN 6
- 6 NC_SATA_SSD2_R2D_CP — TRUE MAKE_BASE=TRUE — NC_SATA_SSD2_R2D_CP 6
- 36 6 NC_BCM57765_SPD100LED_L — MAKE_BASE=TRUE TRUE — NC_BCM57765_SPD100LED_L 6 36
- 36 6 NC_BCM57765_TRAFFICLED_L — MAKE_BASE=TRUE TRUE — NC_BCM57765_TRAFFICLED_L 6 36
- 36 6 NC_CE_L_MS_INS_L — MAKE_BASE=TRUE TRUE — NC_CE_L_MS_INS_L 6 36

NC NO_TESTs

NO_TEST
- 1154 TRUE NC_SMC_FAN_3_TACH 45 46
- 1154 TRUE NC_SMC_FAN_3_CTL 45 46
- 1154 TRUE NC_SMC_FAN_2_TACH 45 46
- 1154 TRUE NC_SMC_FAN_2_CTL 45 46
- 1154 NC_FW2_TPBP 38 40
- 1154 NC_FW2_TPBN 38 40
- 1154 NC_FW2_TPBIAS 38 40 — has TP
- 1154 NC_FW2_TPAP 38 40
- 1154 NC_FW2_TPAN 38 40
- 1154 NC_FW0_TPBP 38 40
- 1154 NC_FW0_TPBN 38 40
- 1154 NC_FW0_TPAP 38 40

NBC
- 38 TP_FW643_AVREG — NC_FW643_AVREG
- 38 6 NC_FW643_TDI — MAKE_BASE=TRUE — NC_FW643_TDI 6 38 — has TP
- 17 6 NC_DP_IG_C_HPD — TRUE MAKE_BASE=TRUE — NC_DP_IG_C_HPD 6 17
- 17 6 NC_DP_IG_C_CTRL_CLK — TRUE MAKE_BASE=TRUE — NC_DP_IG_C_CTRL_CLK 6 17
- 17 6 NC_DP_IG_C_CTRL_DATA — TRUE MAKE_BASE=TRUE — NC_DP_IG_C_CTRL_DATA 6 17
- TP_DP_IG_C_MLP<3..0> — TRUE MAKE_BASE=TRUE — NC_DP_IG_C_MLP<3..0> 17
- TP_DP_IG_C_MLN<3..0> — TRUE MAKE_BASE=TRUE — NC_DP_IG_C_MLN<3..0> 17
- 17 6 NC_DP_IG_C_AUXP — TRUE MAKE_BASE=TRUE — NC_DP_IG_C_AUXP 6 17
- 17 6 NC_DP_IG_C_AUXN — TRUE MAKE_BASE=TRUE — NC_DP_IG_C_AUXN 6 17
- 17 6 NC_DP_IG_D_HPD — TRUE MAKE_BASE=TRUE — NC_DP_IG_D_HPD 6 17
- 17 6 NC_DP_IG_D_CTRL_CLK — TRUE MAKE_BASE=TRUE — NC_DP_IG_D_CTRL_CLK 6 17
- 17 6 NC_DP_IG_D_CTRL_DATA — TRUE MAKE_BASE=TRUE — NC_DP_IG_D_CTRL_DATA 6 17
- TP_DP_IG_D_MLP<3..0> — TRUE MAKE_BASE=TRUE — NC_DP_IG_D_MLP<3..0> 17
- TP_DP_IG_D_MLN<3..0> — TRUE MAKE_BASE=TRUE — NC_DP_IG_D_MLN<3..0> 17
- 17 6 NC_DP_IG_D_AUXP — TRUE MAKE_BASE=TRUE — NC_DP_IG_D_AUXP 6 17
- 17 6 NC_DP_IG_D_AUXN — TRUE MAKE_BASE=TRUE — NC_DP_IG_D_AUXN 6 17
- 17 6 NC_SDVO_TVCLKINN — TRUE MAKE_BASE=TRUE — NC_SDVO_TVCLKINN 6 17
- 17 6 NC_SDVO_TVCLKINP — TRUE MAKE_BASE=TRUE — NC_SDVO_TVCLKINP 6 17
- 17 6 NC_SDVO_STALLN — TRUE MAKE_BASE=TRUE — NC_SDVO_STALLN 6 17
- 17 6 NC_SDVO_STALLP — TRUE MAKE_BASE=TRUE — NC_SDVO_STALLP 6 17
- 17 6 NC_SDVO_INTN — TRUE MAKE_BASE=TRUE — NC_SDVO_INTN 6 17
- 17 6 NC_SDVO_INTP — TRUE MAKE_BASE=TRUE — NC_SDVO_INTP 6 17
- 6 NC_GPU_BUFRST_L — TRUE MAKE_BASE=TRUE — NC_GPU_BUFRST_L 6
- 6 NC_GPU_GSTATE<0> — TRUE MAKE_BASE=TRUE — NC_GPU_GSTATE<0> 6
- TP_GPU_GSTATE<1> — TRUE MAKE_BASE=TRUE — NC_GPU_GSTATE<1>
- TP_GPU_MIOA_D<9..0> — TRUE MAKE_BASE=TRUE — NC_GPU_MIOA_D<9..0>
- 6 NC_GPU_MIOA_DE — TRUE MAKE_BASE=TRUE — NC_GPU_MIOA_DE 6
- 6 NC_LVDS_EG_B_CLKN — TRUE MAKE_BASE=TRUE — NC_LVDS_EG_B_CLKN 6
- 6 NC_LVDS_EG_B_CLKP — TRUE MAKE_BASE=TRUE — NC_LVDS_EG_B_CLKP 6
- 6 NC_LVDS_EG_BKL_PWM — TRUE MAKE_BASE=TRUE — NC_LVDS_EG_BKL_PWM 6
- 18 8 TP_LVDS_IG_B_CLKN — TRUE MAKE_BASE=TRUE — NC_LVDS_IG_B_CLKN 8
- 18 8 TP_LVDS_IG_B_CLKP — TRUE MAKE_BASE=TRUE — NC_LVDS_IG_B_CLKP 8
- 18 8 TP_LVDS_IG_BKL_PWM — TRUE MAKE_BASE=TRUE — NC_LVDS_IG_BKL_PWM 8
- 6 NC_PCH_SST — TRUE MAKE_BASE=TRUE — NC_PCH_SST 6
- 6 NC_PCH_NC1 — TRUE MAKE_BASE=TRUE — NC_PCH_NC1 6
- 6 NC_PCH_NC2 — TRUE MAKE_BASE=TRUE — NC_PCH_NC2 6
- 6 NC_PCH_NC3 — TRUE MAKE_BASE=TRUE — NC_PCH_NC3 6
- 6 NC_PCH_NC4 — TRUE MAKE_BASE=TRUE — NC_PCH_NC4 6
- 6 NC_PCH_NC5 — TRUE MAKE_BASE=TRUE — NC_PCH_NC5 6
- 6 NC_PCH_TP19 — TRUE MAKE_BASE=TRUE — NC_PCH_TP19 6
- 6 NC_PCH_TP18 — TRUE MAKE_BASE=TRUE — NC_PCH_TP18 6
- 6 NC_PCH_TP17 — TRUE MAKE_BASE=TRUE — NC_PCH_TP17 6
- 6 NC_PCH_TP16 — TRUE MAKE_BASE=TRUE — NC_PCH_TP16 6
- 6 NC_PCH_TP15 — TRUE MAKE_BASE=TRUE — NC_PCH_TP15 6
- 6 NC_PCH_TP14 — TRUE MAKE_BASE=TRUE — NC_PCH_TP14 6
- 6 NC_PCH_TP13 — TRUE MAKE_BASE=TRUE — NC_PCH_TP13 6
- 6 NC_PCH_TP12 — TRUE MAKE_BASE=TRUE — NC_PCH_TP12 6
- 6 NC_PCH_TP11 — TRUE MAKE_BASE=TRUE — NC_PCH_TP11 6
- 6 NC_PCH_TP10 — TRUE MAKE_BASE=TRUE — NC_PCH_TP10 6
- 6 NC_PCH_TP9 — TRUE MAKE_BASE=TRUE — NC_PCH_TP9 6
- 6 NC_PCH_TP8 — TRUE MAKE_BASE=TRUE — NC_PCH_TP8 6
- 6 NC_PCH_TP7 — TRUE MAKE_BASE=TRUE — NC_PCH_TP7 6
- 6 NC_PCH_TP6 — TRUE MAKE_BASE=TRUE — NC_PCH_TP6 6
- 6 NC_PCH_TP5 — TRUE MAKE_BASE=TRUE — NC_PCH_TP5 6
- 6 NC_PCH_TP4 — TRUE MAKE_BASE=TRUE — NC_PCH_TP4 6
- 6 NC_PCH_TP3 — TRUE MAKE_BASE=TRUE — NC_PCH_TP3 6
- 6 NC_PCH_TP2 — TRUE MAKE_BASE=TRUE — NC_PCH_TP2 6
- 6 NC_PCH_TP1 — TRUE MAKE_BASE=TRUE — NC_PCH_TP1 6
- 1140 TRUE PCH_VSS_NCTF<1>
- 1140 TRUE PCH_VSS_NCTF<2>
- 1140 TRUE PCH_VSS_NCTF<5>
- 1140 TRUE PCH_VSS_NCTF<7>
- 1140 TRUE PCH_VSS_NCTF<9>
- 1140 TRUE PCH_VSS_NCTF<11>
- 1140 TRUE PC



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Thermal Module Holes

Bottom GPU Right TM Hole — ZT0982 STDOFF-4.50D.98H-1.1-3.48-TH

Right CPU TM Hole — ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH

ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH

Top GPU Center TM Hole — ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH

ZT0983 STDOFF-4.50D.98H-1.1-3.48-TH

Left CPU TM Hole

ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH

Bottom CPU Left TM Hole

ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH

Bottom GPU Left TM Hole

Frame Holes

ZT0915 3R2P5 — GND

ZT0932 3R2P5

ZT0960 3R2P5

ZT0971 3R2P5

ZT0940 3R2P5

ZT0970 3R2P5

ZT0934 STDOFF-4.0OD3.35H-TH

ZT0931 STDOFF-4.0OD3.35H-TH

ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH

ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH

ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH

Bosses for Flex Protector Bracket

ZT0957 4.0OD1.65H-M1.6X0.35

ZT0958 4.0OD1.65H-M1.6X0.35

SH0920 1.4DIA-SHORT-EMI-MLB-M97-M98

SH0936 1.4DIA-SHORT-EMI-MLB-M97-M98 — GND_CHASSIS_AUDIO_JACK

SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98

SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98

SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98

SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98

SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98

SH0923 1.4DIA-SHORT-EMI-MLB-M97-M98

SH0924 2.0DIA-TALL-EMI-MLB-M97-M98

SH0916 2.0DIA-TALL-EMI-MLB-M97-M98

SH0917 2.0DIA-TALL-EMI-MLB-M97-M98

SH0918 2.0DIA-TALL-EMI-MLB-M97-M98

SH0919 2.0DIA-TALL-EMI-MLB-M97-M98

SH0930 2.0DIA-TALL-EMI-MLB-M97-M98

SH0921 2.0DIA-TALL-EMI-MLB-M97-M98

SH0931 2.0DIA-TALL-EMI-MLB-M97-M98

SH0922 2.0DIA-TALL-EMI-MLB-M97-M98

SH0932 2.0DIA-TALL-EMI-MLB-M97-M98

SH0902 2.0DIA-TALL-EMI-MLB-M97-M98

SH0900 2.0DIA-TALL-EMI-MLB-M97-M98

SH0934 2.0DIA-TALL-EMI-MLB-M97-M98

SH0933 2.0DIA-TALL-EMI-MLB-M97-M98

SH0903 2.0DIA-TALL-EMI-MLB-M97-M98

SH0901 2.0DIA-TALL-EMI-MLB-M97-M98

SH0935 2.0DIA-TALL-EMI-MLB-M97-M98

GMUX ALIASES

PM_ALL_GPU_PGOOD (MAKE_BASE=TRUE)	PM_ALL_GPU_PGOOD	8 74 82 87 88 91	
TP_LVDS_MUX_SEL_EG (MAKE_BASE=TRUE)	TP_LVDS_MUX_SEL_EG	8 88	
EG_RESET_L (MAKE_BASE=TRUE)	EG_RESET_L	8 74 88	
LVDS_IG_BKL_ON (MAKE_BASE=TRUE)	LVDS_IG_BKL_ON	8 18 88	
LVDS_IG_PANEL_PWR (MAKE_BASE=TRUE)	LVDS_IG_PANEL_PWR	8 18 88	
LCD_BKLT_EN (MAKE_BASE=TRUE)	LCD_BKLT_EN	8 88 90	
PEX_CLKREQ_L (MAKE_BASE=TRUE)	PEX_CLKREQ_L	8 80 88	
PEG_CLKREQ_L (MAKE_BASE=TRUE)	PEG_CLKREQ_L	8 16 88	
GND	GND		
GND	GND		
GND	GND		
GND	GND		
GND	GND (MAKE_BASE=TRUE)		
FW_PLUG_DET_L (MAKE_BASE=TRUE)	FW_PLUG_DET_L	8 19 39	
FW643_WAKE_L (MAKE_BASE=TRUE)	FW643_WAKE_L	8 38 39	

Unused SD card signals

TP_SDCONN_DATA<0..7> (MAKE_BASE=TRUE)	SDCONN_DATA<0..7>	
TP_SDCONN_CLK (MAKE_BASE=TRUE)	TP_SDCONN_CLK	8 36
TP_SDCONN_CMD (MAKE_BASE=TRUE)	TP_SDCONN_CMD	8 36
TP_SDCONN_DETECT_L (MAKE_BASE=TRUE)	TP_SDCONN_DETECT_L	8 36
TP_SDCONN_WP (MAKE_BASE=TRUE)	TP_SDCONN_WP	8 36
TP_ENET_CR_PWREN (MAKE_BASE=TRUE)	TP_ENET_CR_PWREN	8 36

AUDIO ALIASES

PP5V_S0 → XW0900 → PP5V_S0_AUDIO (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V)

XW0901 → PP5V_S0_AUDIO_AMP_R (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V)

XW0902 → PP5V_S0_AUDIO_AMP_L (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V)

Digital Ground

GND (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.11MM, VOLTAGE=0V)

LVDS_IG_PANEL_PWR (88 18 8) — R0902 100K 5% 1/16W MF-LF 402

Unused USB ports

PP3V3_S3 (6 7 18 24 25 29 30 31 32 48 49 50 54 55 73 88 104)

R0915 10K 5% 1/16W MF-LF 402 — USB_T29A_N (24 94)

R0916 10K 5% 1/16W MF-LF 402 — USB_T29A_P (24 94)

Heat spreader mounting boss for T29 router

SH0940 STDOFF-4.0OD1.85H-SM

SH0941 STDOFF-4.0OD1.85H-SM

Heat spreader mounting boss for PCH

SH0942 STDOFF-4.0OD2.23H-SM

SH0943 STDOFF-4.0OD2.23H-SM

CPU signals

CPU_VID<0..6> (MAKE_BASE=TRUE)	CPUIMVP_VID<0..6>	
GFX_VID<0..6> (MAKE_BASE=TRUE)	GFXIMVP_VID<0..6>	
MEMVTT_EN (MAKE_BASE=TRUE)	MEMVTT_EN	8 29 67

Unused PEG lanes

NC_PEG_D2R_P<15..12> (MAKE_BASE=TRUE)	=PEG_D2R_P<15..12>	
NC_PEG_D2R_N<15..12> (MAKE_BASE=TRUE)	=PEG_D2R_N<15..12>	
NC_PEG_R2D_C_P<15..12> (MAKE_BASE=TRUE)	=PEG_R2D_C_P<15..12>	
NC_PEG_R2D_C_N<15..12> (MAKE_BASE=TRUE)	=PEG_R2D_C_N<15..12>	

GPU signals

PEG_D2R_P<7..0> (MAKE_BASE=TRUE)	=PEG_D2R_P<7..0>	9
PEG_D2R_N<7..0> (MAKE_BASE=TRUE)	=PEG_D2R_N<7..0>	9
PEG_R2D_C_P<7..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_P<7..0>	9
PEG_R2D_C_N<7..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_N<7..0>	9
DP_IG_AUX_CH_P (MAKE_BASE=TRUE)	DP_IG_AUX_CH_P	8 17 84 94
DP_IG_AUX_CH_N (MAKE_BASE=TRUE)	DP_IG_AUX_CH_N	8 17 84 94
DP_IG_DDC_CLK (MAKE_BASE=TRUE)	DP_IG_DDC_CLK	8 17 80 84
DP_IG_DDC_DATA (MAKE_BASE=TRUE)	DP_IG_DDC_DATA	8 17 80 84
DP_IG_HPD (MAKE_BASE=TRUE)	DP_IG_HPD	8 17 84

T29 Signals

PCIE_T29_D2R_P<3..0> (MAKE_BASE=TRUE)	=PEG_D2R_P<11..8>	9
PCIE_T29_D2R_N<3..0> (MAKE_BASE=TRUE)	=PEG_D2R_N<11..8>	9
PCIE_T29_R2D_C_P<3..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_P<11..8>	9
PCIE_T29_R2D_C_N<3..0> (MAKE_BASE=TRUE)	=PEG_R2D_C_N<11..8>	9

Unused T29 Ports

T29_D2R_P<2..3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_T29_D2RP<2..3>	33
T29_D2R_N<2..3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_T29_D2RN<2..3>	33
T29_R2D_C_P<2..3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_T29_R2D_CP<2..3>	33
T29_R2D_C_N<2..3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_T29_R2D_CN<2..3>	33
33 8 T29_LSEO_LSOE3 (MAKE_BASE=TRUE NO_TEST=TRUE)	T29_LSEO_LSOE3	8 33
33 8 T29_LSEO_LSOE2 (MAKE_BASE=TRUE NO_TEST=TRUE)	T29_LSEO_LSOE2	8 33

T29 / GMUX JTAG Signals

JTAG_ISP_TCK	JTAG_ISP_TCK	8 19 23 33 88
88 33 23 19 8 JTAG_ISP_TCK (MAKE_BASE=TRUE)	JTAG_ISP_TCK	8 19 23 33 88
88 33 19 8 JTAG_ISP_TDI (MAKE_BASE=TRUE)	JTAG_ISP_TDI	8 19 33 88
88 33 19 8 JTAG_ISP_TDO (MAKE_BASE=TRUE)	JTAG_ISP_TDO	8 19 33 88

T29_A_BIAS caps

86 8 T29_A_BIAS_R — R0926 51 5% 1/20W MF 201 — T29_A_BIAS_D2R_P1 86 — C0906 0.01UF 10% 10V X5R 201 (SIGNAL_MODEL=EMPTY)

86 8 T29_A_BIAS_R — R0927 51 5% 1/20W MF 201 — T29_A_BIAS_D2R_N1 86 — C0907 0.01UF 10% 10V X5R 201 (SIGNAL_MODEL=EMPTY)

DP_A_BIAS caps

85 6 DP_A_BIAS_P_2 — C0910 0.01UF 10% 10V X5R 201 (SIGNAL_MODEL=EMPTY)

85 6 DP_A_BIAS_P_0 — C0911 0.01UF 10% 10V X5R 201 (SIGNAL_MODEL=EMPTY)

T29BST:N — R0950 0 5% 1/8W MF-LF 805 — 90 64 63 50 49 39 35 7 6 PPBUS_G3H — PP15V_T29 7 35 86

TP_CPU_VTT_SELECT (MAKE_BASE=TRUE)	TP_CPU_VTT_SELECT	8 92
NC_GPU_XTALOUT (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_GPU_XTALOUT	8
94 18 8 NC_LVDS_IG_A_DATAP<3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_IG_A_DATAP<3>	8 18 94
94 18 8 NC_LVDS_IG_A_DATAN<3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_IG_A_DATAN<3>	8 18 94
18 8 NC_LVDS_IG_B_DATAP<3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_IG_B_DATAP<3>	8 18
18 8 NC_LVDS_IG_B_DATAN<3> (MAKE_BASE=TRUE NO_TEST=TRUE)	NC_LVDS_IG_B_DATAN<3>	8 18
18 8 6 TP_LVDS_IG_B_CLKP (MAKE_BASE=TRUE)	TP_LVDS_IG_B_CLKP	6 8 18
18 8 6 TP_LVDS_IG_B_CLKN (MAKE_BASE=TRUE)	TP_LVDS_IG_B_CLKN	6 8 18
18 8 6 TP_LVDS_IG_BKL_PWM (MAKE_BASE=TRUE)	TP_LVDS_IG_BKL_PWM	6 8 18

USB Hub Aliases

32 24 8 EXCARD_OC_L (MAKE_BASE=TRUE)	EXCARD_OC_L	8 24 32
43 24 8 USB_EXTC_OC_L (MAKE_BASE=TRUE)	USB_EXTC_OC_L	8 24 43
100 32 24 8 USB_EXCARD_N (MAKE_BASE=TRUE)	USB_EXCARD_N	8 24 32 100
100 32 24 8 USB_EXCARD_P (MAKE_BASE=TRUE)	USB_EXCARD_P	8 24 32 100

Rev. A NCs

8 NC_ISNS_P1V05S0PCH_N (MAKE_BASE=TRUE)	NC_ISNS_P1V05S0PCH_N	8
8 NC_ISNS_P1V05S0PCH_P (MAKE_BASE=TRUE)	NC_ISNS_P1V05S0PCH_P	8
8 NC_ISNS_P3V3S0MPCH_N (MAKE_BASE=TRUE)	NC_ISNS_P3V3S0MPCH_N	8
8 NC_ISNS_P3V3S0MPCH_P (MAKE_BASE=TRUE)	NC_ISNS_P3V3S0MPCH_P	8
8 NC_ISNS_PVTTS0PCH_N (MAKE_BASE=TRUE)	NC_ISNS_PVTTS0PCH_N	8
8 NC_ISNS_PVTTS0PCH_P (MAKE_BASE=TRUE)	NC_ISNS_PVTTS0PCH_P	8

T29_A_BIAS caps

86 8 T29_A_BIAS_R — R0921 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_P0 6 85 — C0901 0.01UF 10% 10V X5R 201 (SIGNAL_MODEL=EMPTY)

86 8 T29_A_BIAS_R — R0922 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_N0 6 85 — C0902 0.01UF 10% 10V X5R 201 (SIGNAL_MODEL=EMPTY)

86 8 T29_A_BIAS_R — R0923 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_P1 6 85 — C0903 0.01UF 10% 10V X5R 201 (SIGNAL_MODEL=EMPTY)

86 8 T29_A_BIAS_R — R0924 51 5% 1/20W MF 201 — T29_A_BIAS_R2D_N1 6 85 — C0904 0.01UF 10% 10V X5R 201 (SIGNAL_MODEL=EMPTY)

DP_A_BIAS caps

85 6 DP_A_BIAS_N_2 — C0905 0.01UF 10% 10V X5R 201 (SIGNAL_MODEL=EMPTY)

85 6 DP_A_BIAS_N_0 — C0908 0.01UF 10% 10V X5R 201 (SIGNAL_MODEL=EMPTY)

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PAGE TITLE: Signal Aliases

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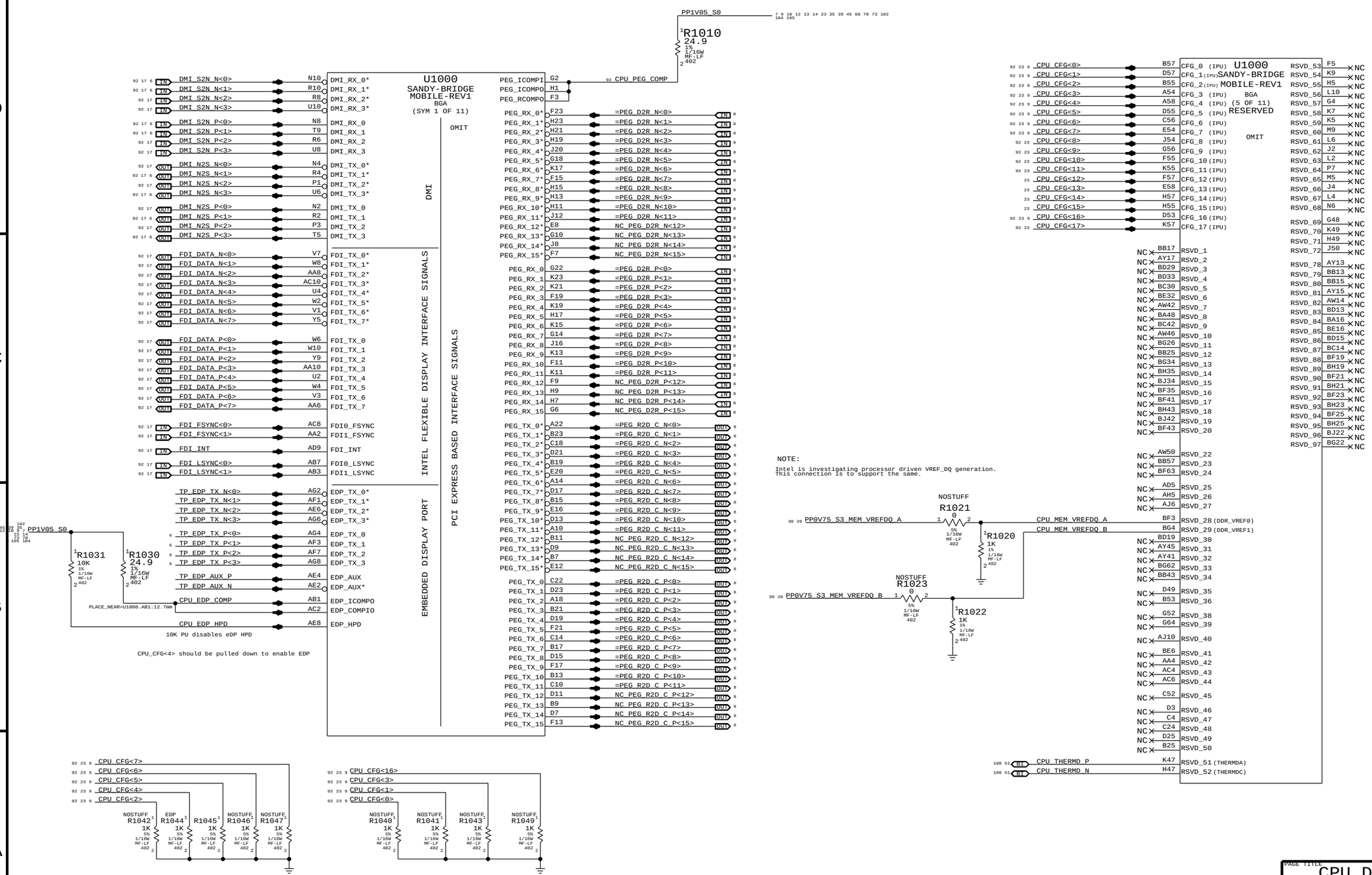

FOR SANDYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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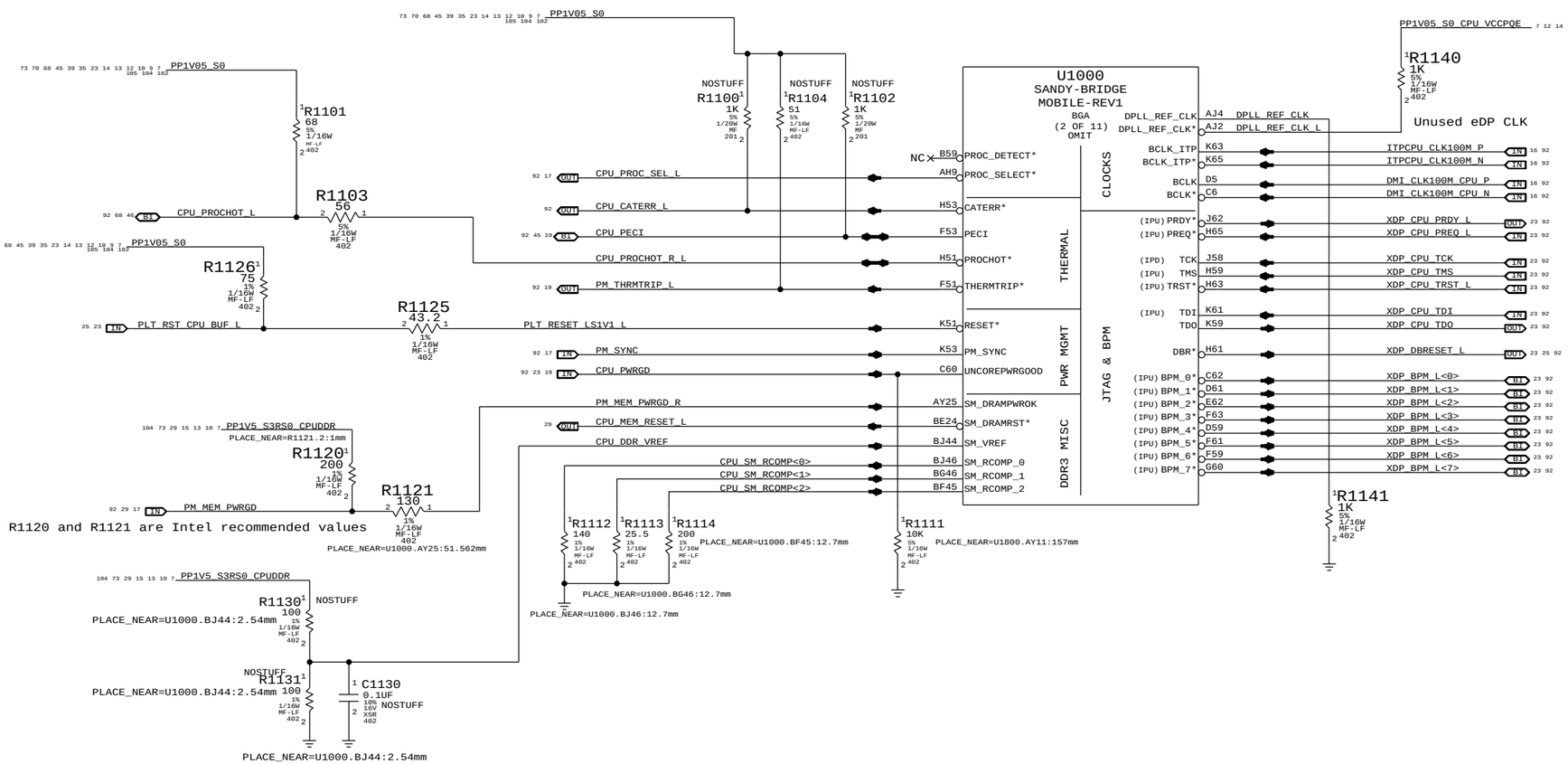

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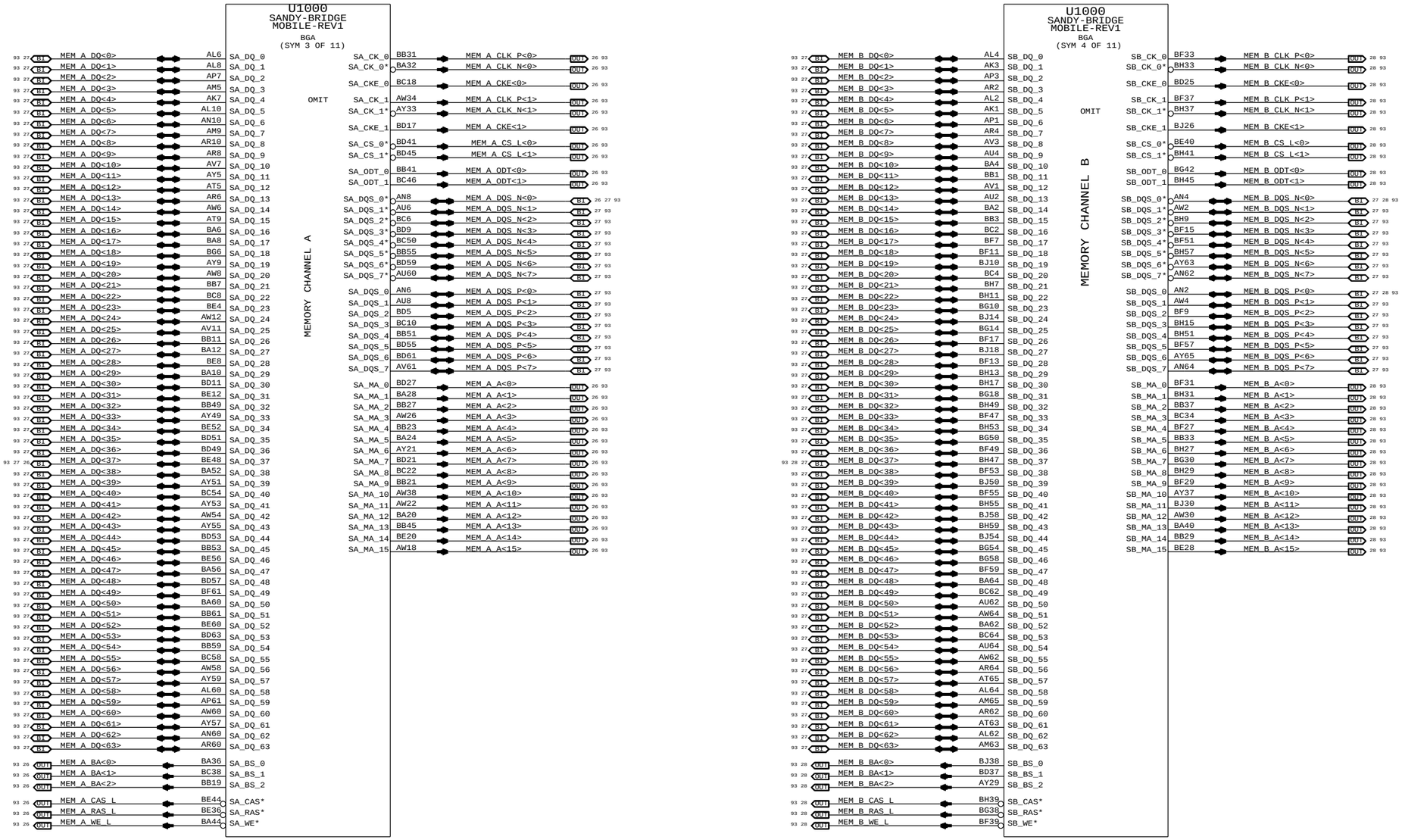

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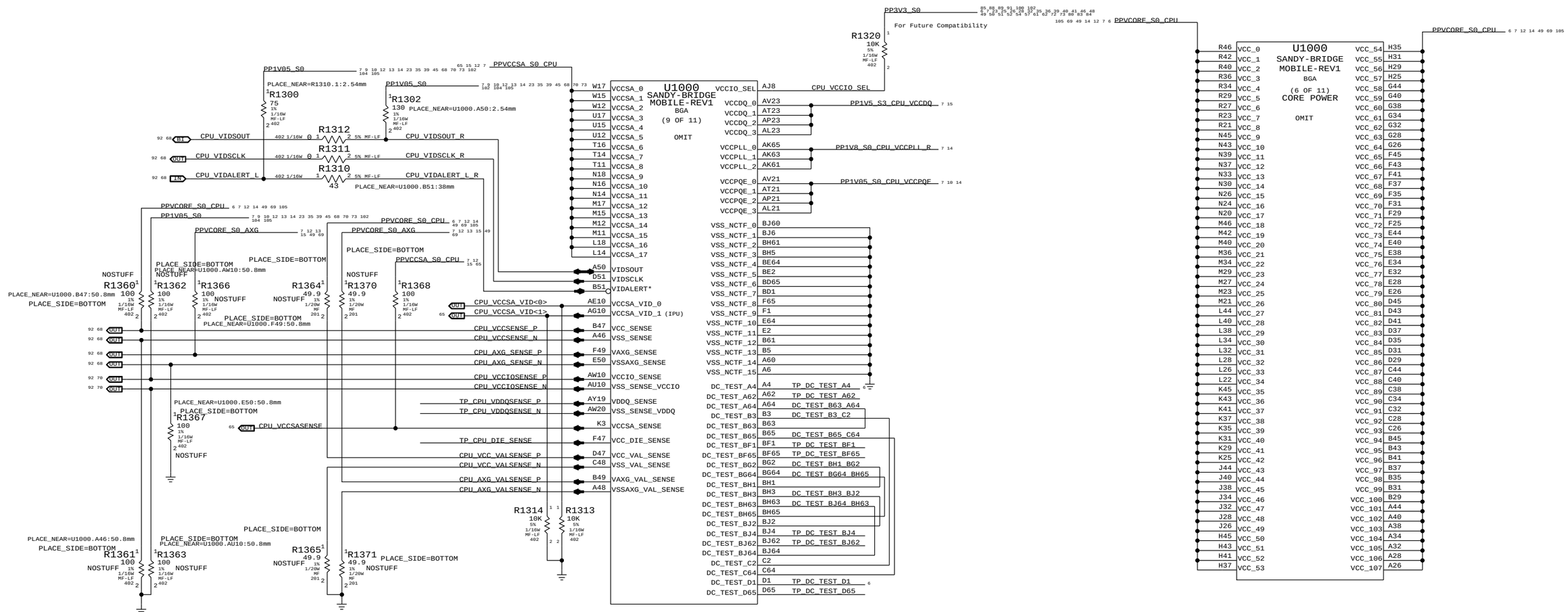

PLACEMENT NOTE: Please place all sense line resistors on BOTTOM side.
NOTE: Intel validation sense lines per doc 439028 rev1.0
HR_PPDG sections 6.2.1 and 6.3.1.

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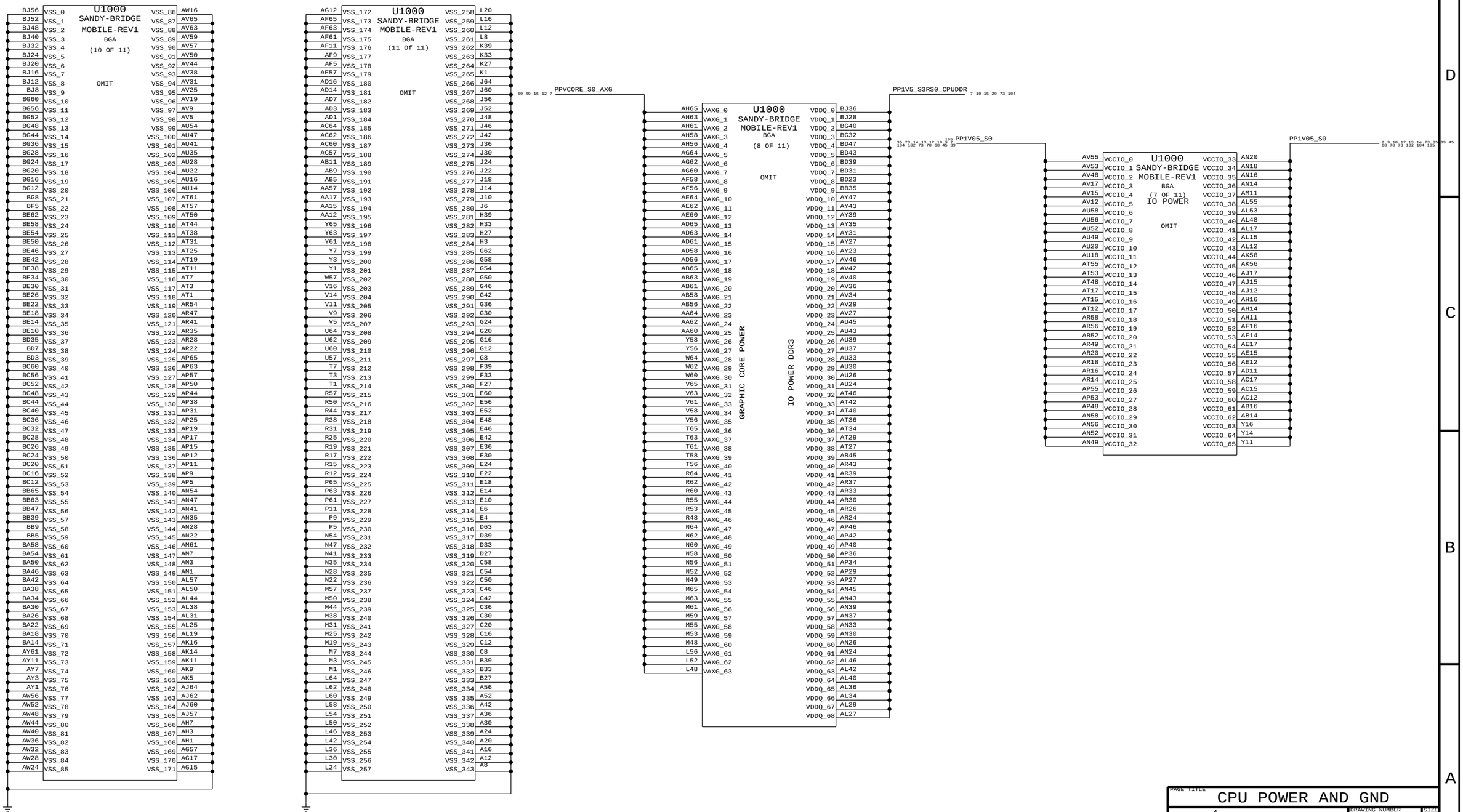

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CPU VCORE DECOUPLING

Intel recommendation: 4x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 16x 22uF 0805, 4x 10uF 0603, 20x 1uF 0402, 28x 1uF 0402 (NOSTUFF)
Apple Implementation: 4x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 16x 22uF 0603, 4x 10uF 0402, 20x 1uF 0402, 28x 1uF 0201 (NOSTUFF), 4x 22uF 0603 (NOSTUFF)

105 69 49 12 7 6 PPVCORE_S0_CPU

PLACEMENT_NOTE (C1600-C16C7):
Place on bottom side of U1000

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609 C1610 C1611 C1612 C1613 C1614 C1615 C1616 C1617 C1618 C1619
1UF 10% 10V X5R 402

NOSTUFF C16A0 C16A1 C16A2 C16A3 C16A4 C16A5 C16A6 C16A7 C16A8 C16A9 C16B0 C16B1 C16B2 C16B3 C16B4 C16B5 C16B6 C16B7 C16B8 C16B9
1UF 20% 6.3V X5R 0201

NOSTUFF C16C0 C16C1 C16C2 C16C3 C16C4 C16C5 C16C6 C16C7
1UF 20% 6.3V X5R 0201

PLACEMENT_NOTE (C1620-C1623):
Place near U1000 on bottom side

C1620 C1621 C1622 C1623
10UF 20% 6.3V CERM-X5R 0402-1 CRITICAL

PLACEMENT_NOTE (C1624-C16D5):
Place near inductors on bottom side.

CRITICAL C1624 C1625 C1626 C1627 C1628 C1629 C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
22UF 20% 6.3V X5R-CERM1 0603

NOSTUFF C16D0 C16D1 C16D2 C16D3
22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

CRITICAL C1640 C1641 C1642 C1643 C1644
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402
Apple Implementation: 2x 330uF, 10x 10uF 0603, 26x 1uF 0402

PLACEMENT_NOTE (C1646-C1671):
Place on bottom side of U1000

13 73 70 68, 13 18 37, 45 39 37 73, 105 101 102 PP1V05_S0

C1646 C1647 C1648 C1649 C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657 C1658
1UF 10% 10V X5R 402

C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666 C1667 C1668 C1669 C1670 C1671
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679 C1680 C1681
10UF 20% 6.3V X5R 603 CRITICAL

Place near inductors on bottom side

C1682 C1683
330UF-0.0060HM 20% 2V POLY CASE-D2-SM CRITICAL

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601
0.010
1% 1/4W 0603

PP1V05_S0_CPU_VCCPQE 7 10 12

C1684
1UF 10% 10V X5R 402

CPU VCCPLL DECOUPLING

102 88 72 71 25 20 7 6 PP1V8_S0

R1600
0
5% 1/16W MF-LF 402

PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA

C1685 C1686
1UF 10% 10V X5R 402

PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

PP1V8_S0_CPU_VCCPLL_R 7 12

CRITICAL C1687
330UF-0.0060HM 20% 2V POLY CASE-D2-SM
PLACE_NEAR=U1000.AK61:5 mm

CPU VCCPLL Low pass filter

SYNC_MASTER=K91_MLB SYNC_DATE=07/21/2010

PAGE TITLE
CPU DECOUPLING-I

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VAXG DECOUPLING

Intel recommendation: 2x 470uF 4mOhm, 2x 470uF 4mOhm (NOSTUFF), 6x 22uF 0805, 2x 22uF 0805 (NOSTUFF), 6x 10uF 0603, 2x 10uF 0603 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)
Apple Implementation: 2x 470uF 4mOhm, 1x 470uF 4mOhm (NOSTUFF), 6x 22uF 0603, 2x 22uF 0603 (NOSTUFF), 6x 10uF 0402, 2x 10uF 0402 (NOSTUFF), 9x 1uF 0402, 9x 1uF 0402 (NOSTUFF)

69 49 13 12 7 PPVCORE_S0_AXG

PLACEMENT_NOTE (C1700-C1708):
Place on bottom side of U1000

C1700 1UF 10% 10V X5R 402
C1701 1UF 10% 10V X5R 402
C1702 1UF 10% 10V X5R 402
C1703 1UF 10% 10V X5R 402
C1704 1UF 10% 10V X5R 402
C1705 1UF 10% 10V X5R 402
C1706 1UF 10% 10V X5R 402
C1707 1UF 10% 10V X5R 402
C1708 1UF 10% 10V X5R 402
NOSTUFF C1709 1UF 10% 10V X5R 402
NOSTUFF C1710 1UF 10% 10V X5R 402
NOSTUFF C1711 1UF 10% 10V X5R 402
NOSTUFF C1712 1UF 10% 10V X5R 402
NOSTUFF C1713 1UF 10% 10V X5R 402
NOSTUFF C1714 1UF 10% 10V X5R 402
NOSTUFF C1715 1UF 10% 10V X5R 402
NOSTUFF C1716 1UF 10% 10V X5R 402
NOSTUFF C1717 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1718-C1723):
Place close to U1000 on bottom side

C1718 10UF 20% 6.3V CERM-X5R 0402-1
C1719 10UF 20% 6.3V CERM-X5R 0402-1
C1720 10UF 20% 6.3V CERM-X5R 0402-1
C1721 10UF 20% 6.3V CERM-X5R 0402-1
C1722 10UF 20% 6.3V CERM-X5R 0402-1
C1723 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1724 10UF 20% 6.3V CERM-X5R 0402-1
NOSTUFF C1725 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1726-C1731):
Place near inductors on bottom side.

C1726 22UF 20% 6.3V X5R-CERM1 0603
C1727 22UF 20% 6.3V X5R-CERM1 0603
C1728 22UF 20% 6.3V X5R-CERM1 0603
C1729 22UF 20% 6.3V X5R-CERM1 0603
C1730 22UF 20% 6.3V X5R-CERM1 0603
C1731 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1732 22UF 20% 6.3V X5R-CERM1 0603
NOSTUFF C1733 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1734-C1735):
Place near inductors on bottom side.

C1734 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1735 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
NOSTUFF C1737 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 1x 330uF, 8x 10uF 0603, 10x 1uF 0402

104 73 29 13 10 7 PP1V5_S3RS0_CPUDDR

PLACEMENT_NOTE (C1738-C1747):
Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V X5R 603
C1749 10UF 20% 6.3V X5R 603
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V X5R 603
C1752 10UF 20% 6.3V X5R 603
C1753 10UF 20% 6.3V X5R 603
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V X5R 603

Place near inductors on bottom side

CRITICAL
C1756 330UF-0.0060HM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1700 0.010 1% 1/4W MF 0603

PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402
Apple Implementation: 1x 330uF, 5x 10uF 0603, 5x 1uF 0402

PLACEMENT_NOTE (C1758-C1762):

65 12 7 PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V X5R 603
C1764 10UF 20% 6.3V X5R 603
C1765 10UF 20% 6.3V X5R 603
C1766 10UF 20% 6.3V X5R 603
C1767 10UF 20% 6.3V X5R 603

C1768 270UF 20% 2V TANT CASE-B4-SM

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PAGE TITLE	CPU DECOUPLING-II
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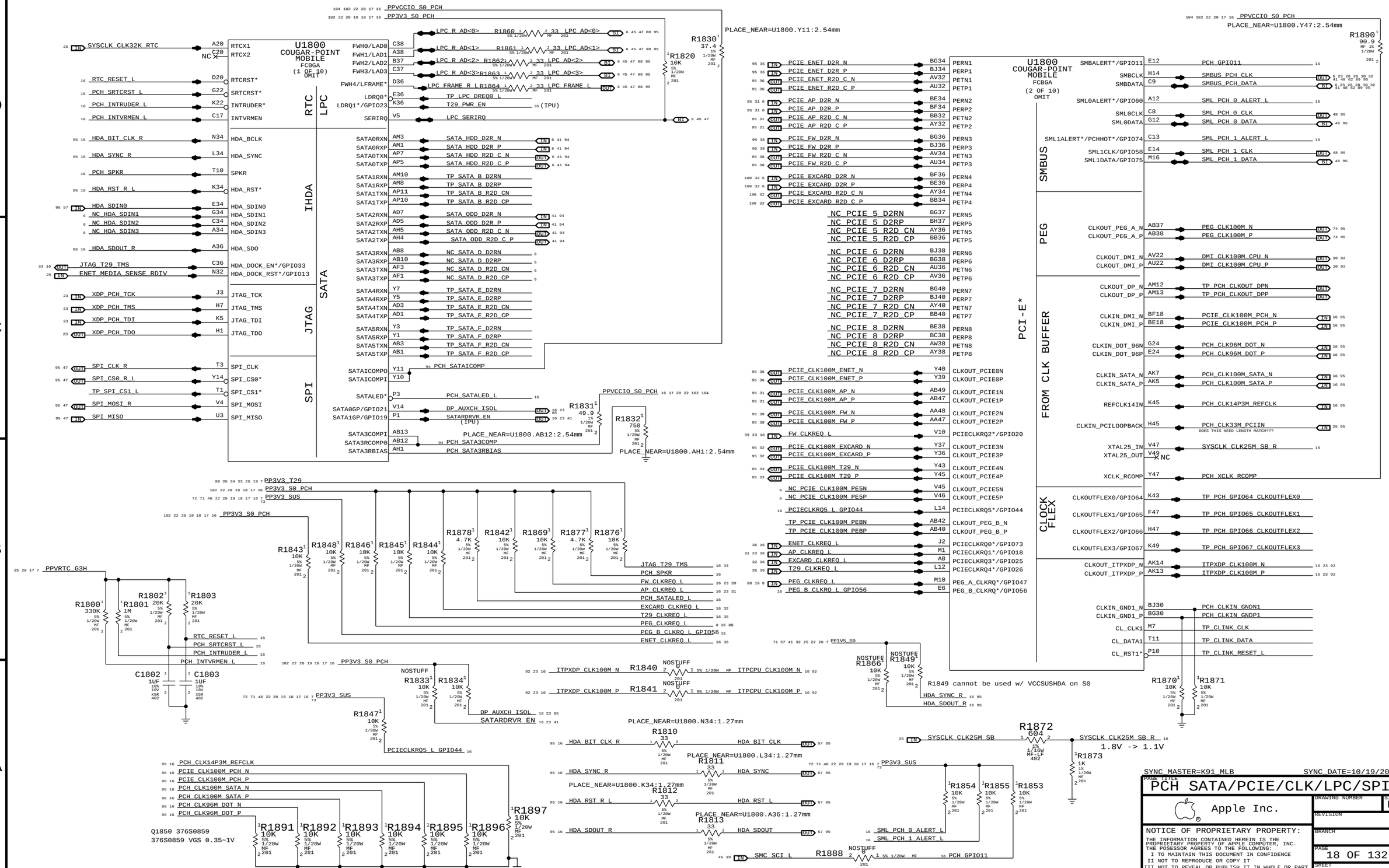

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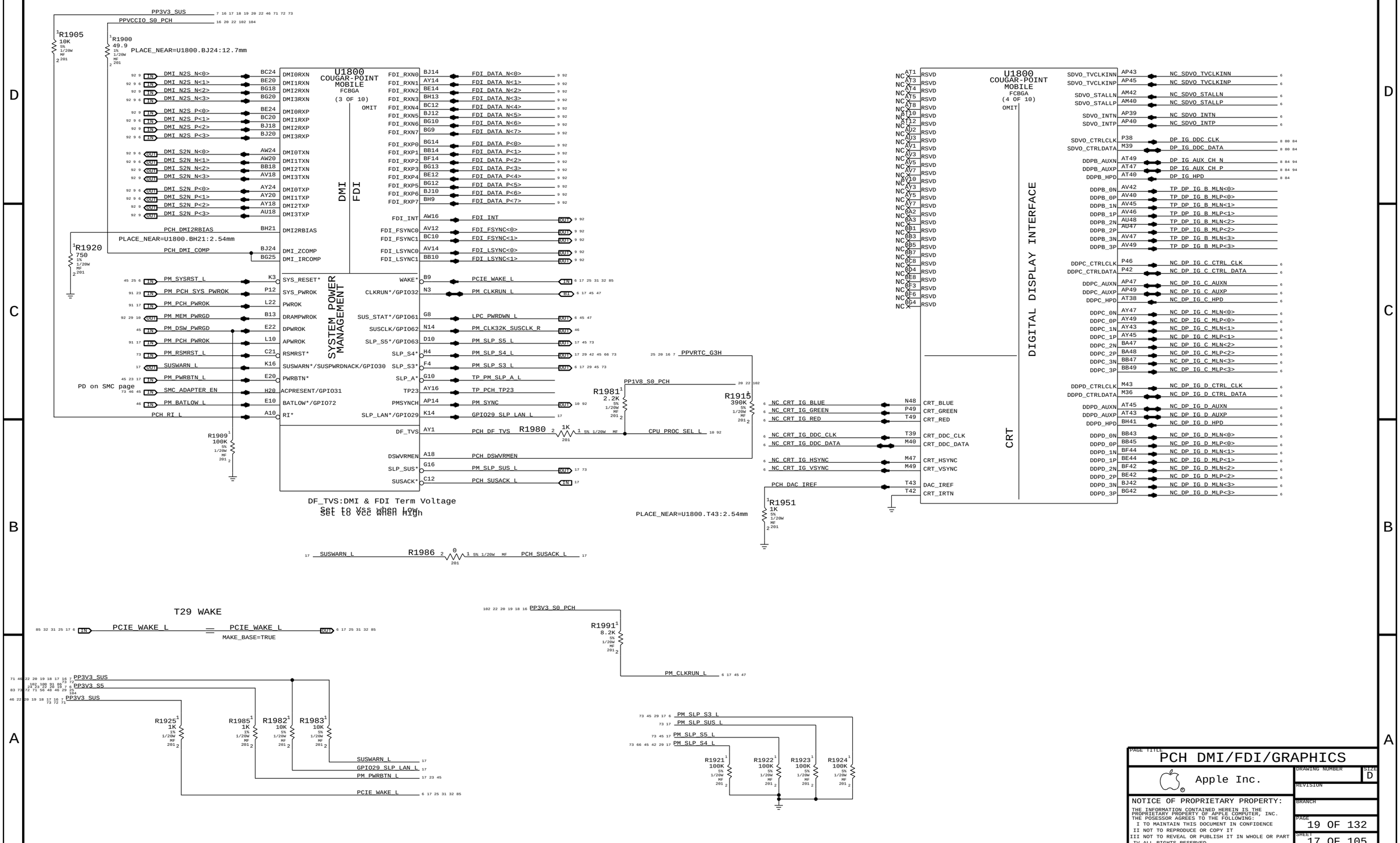

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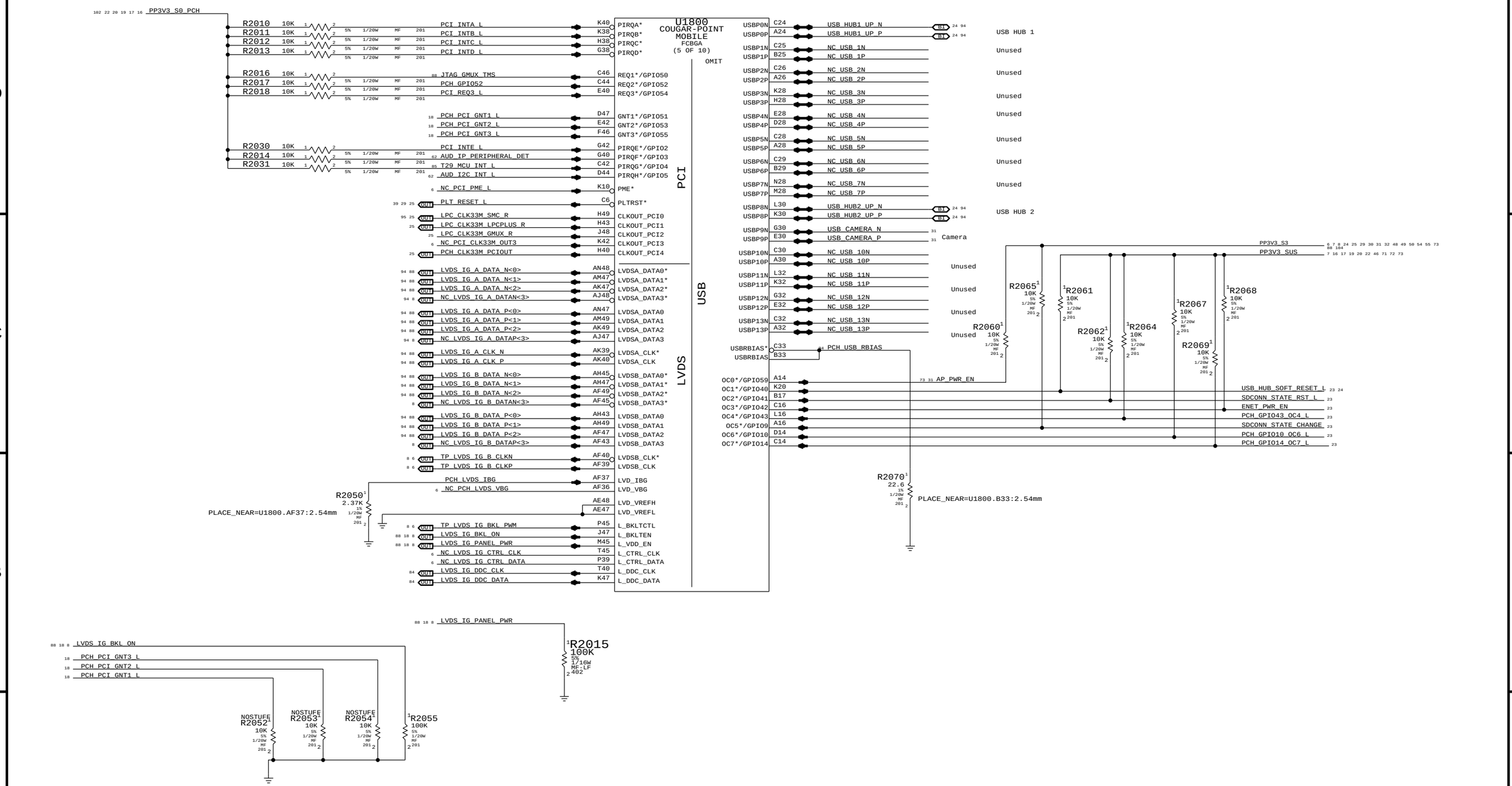

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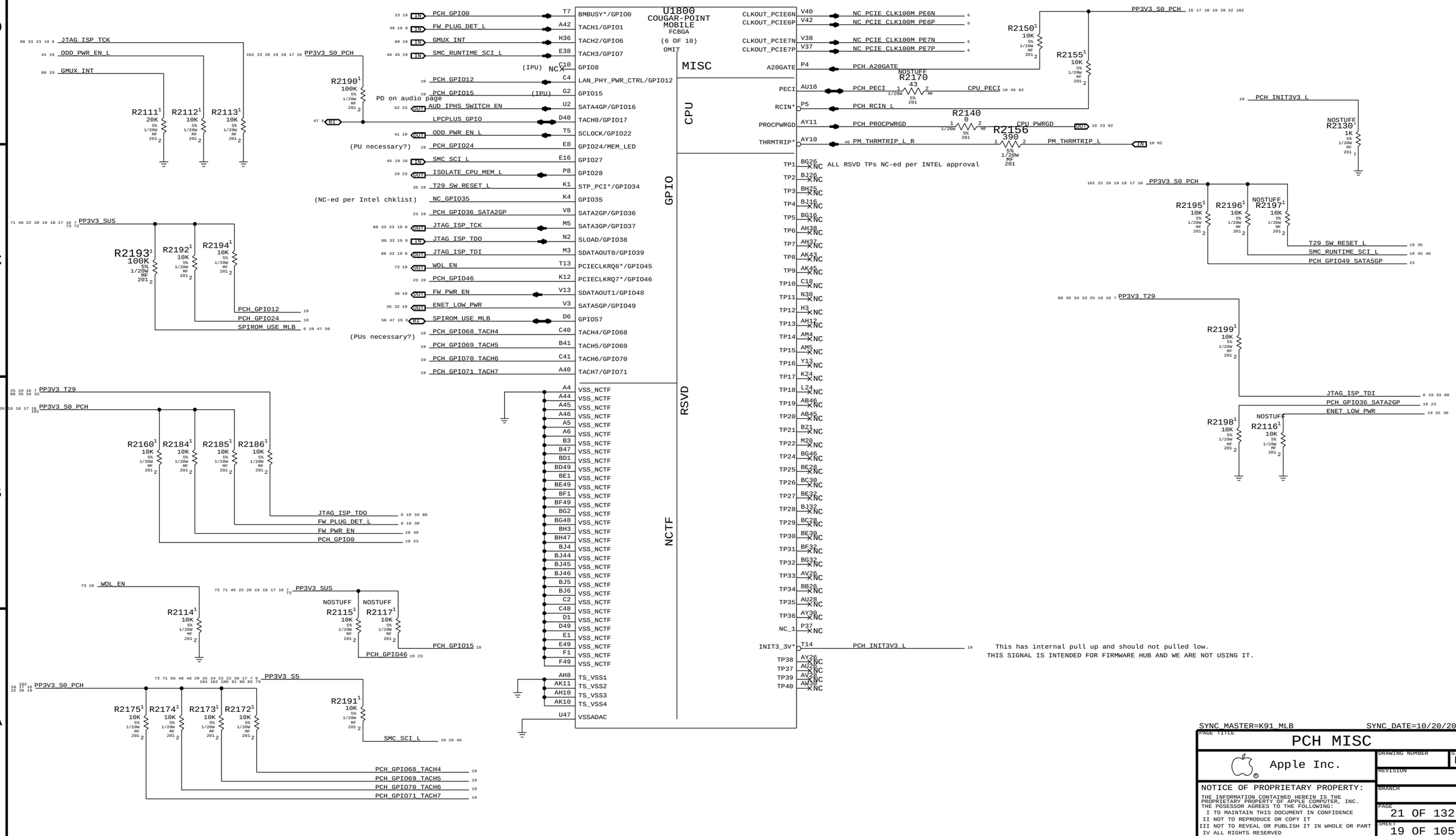

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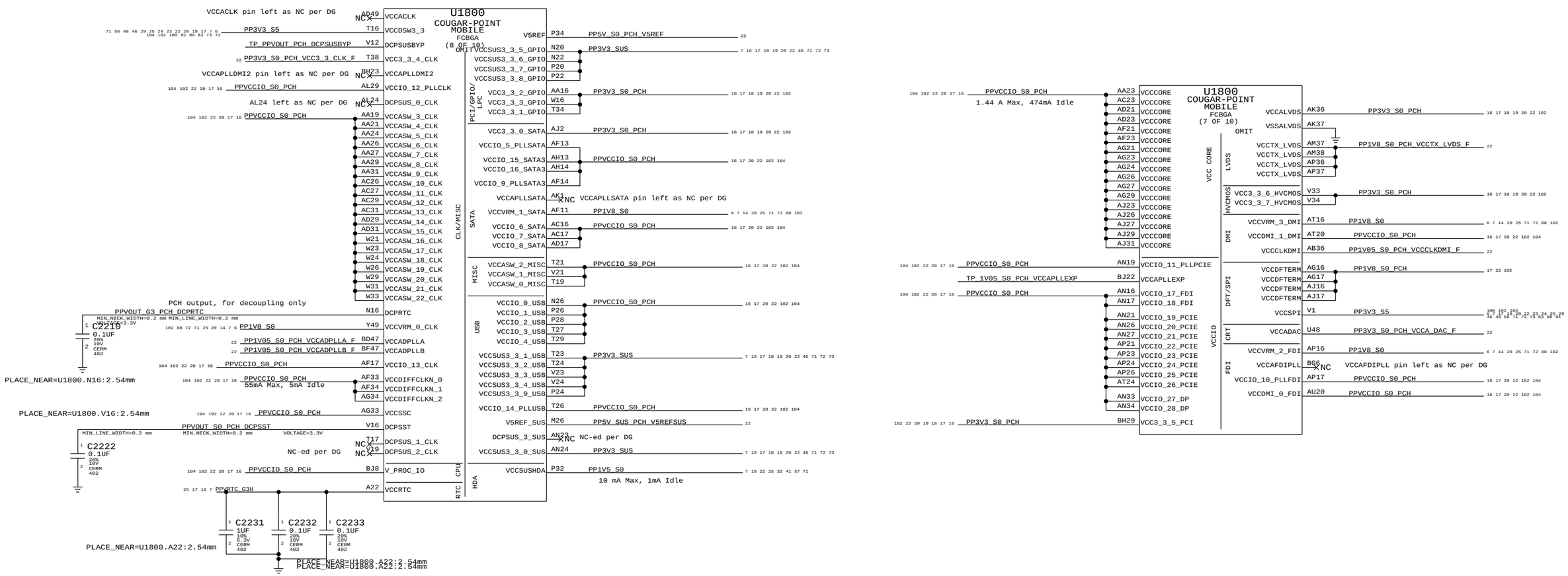

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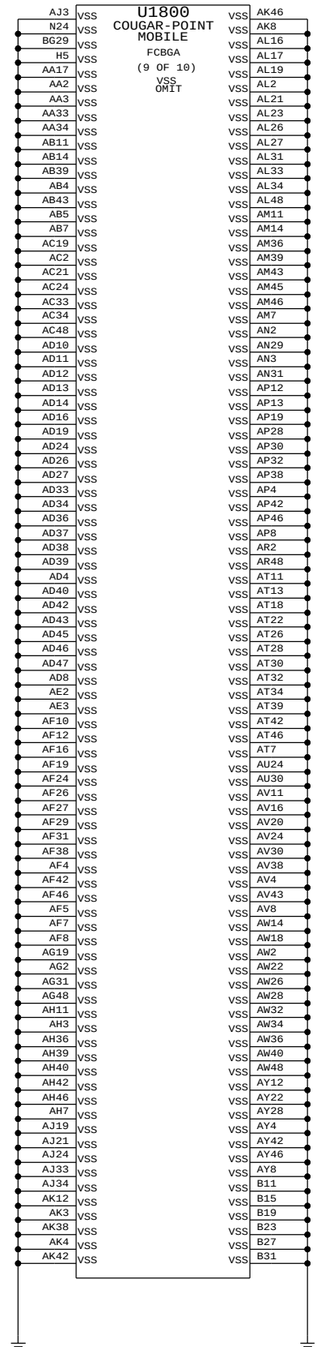

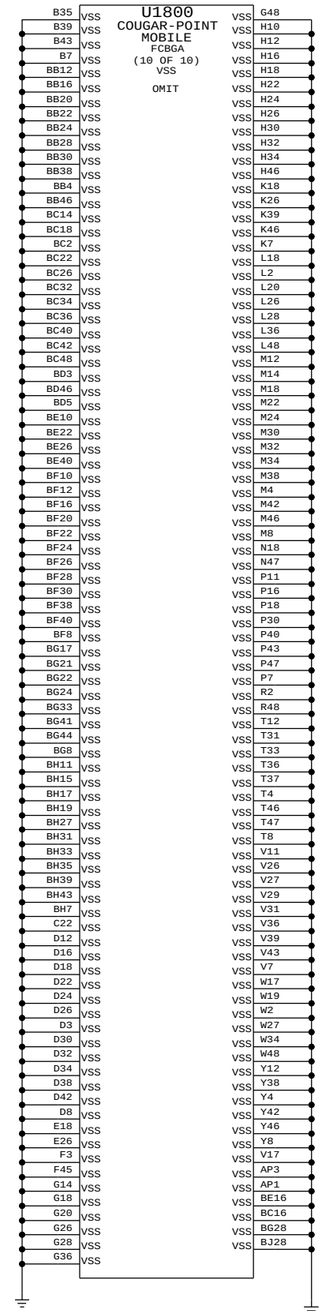

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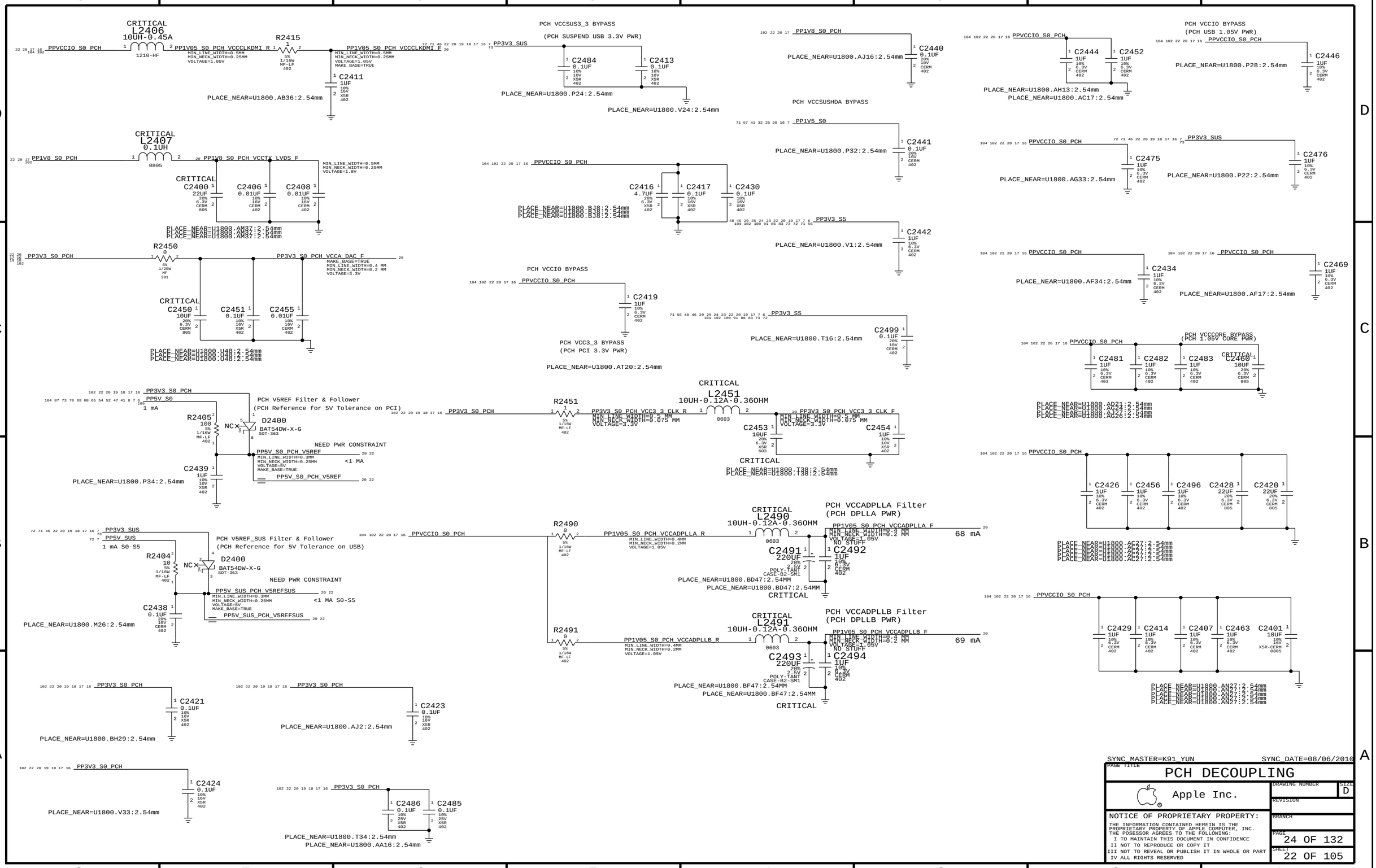

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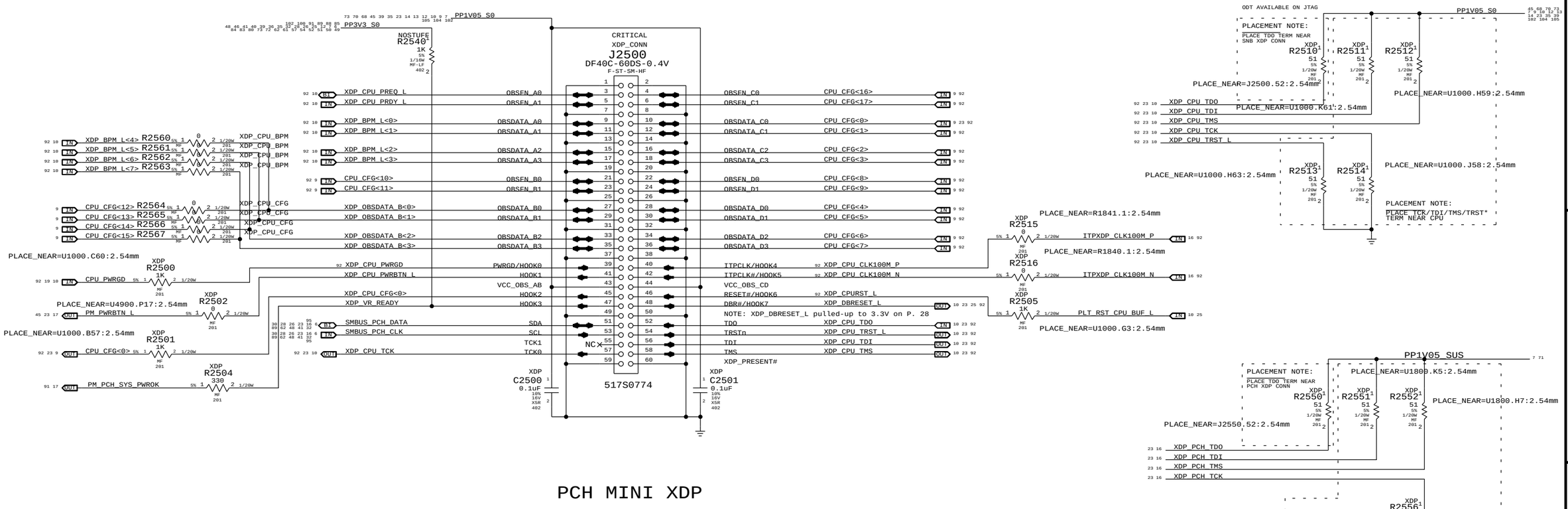
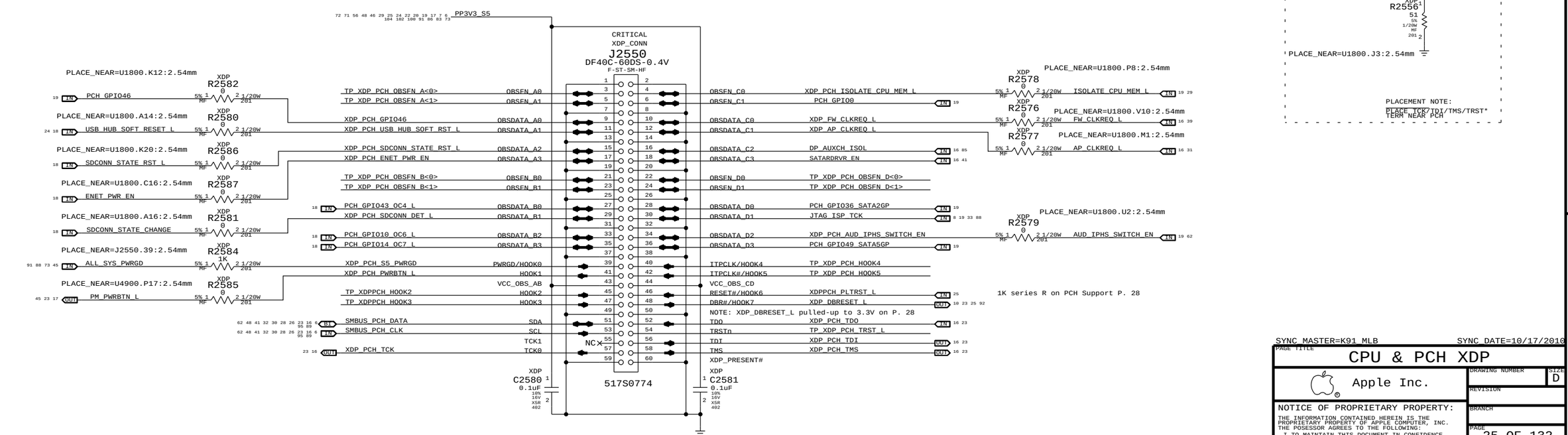
PROCESSOR MINI XDP



PCH MINI XDP



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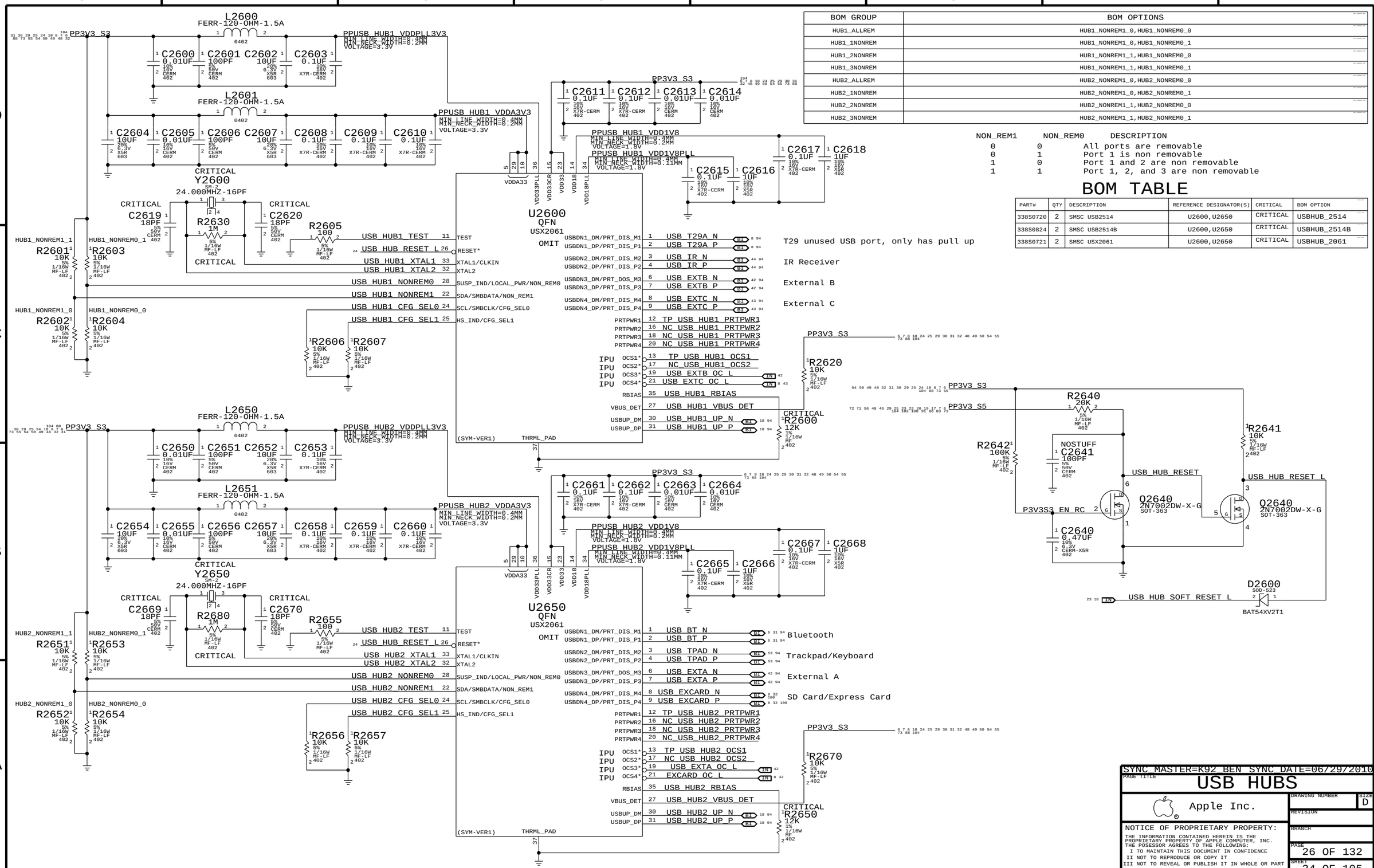

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0721	2	SMSC USX2061	U2600,U2650	CRITICAL	USBHUB_2061

SYNC MASTER=K92 BEN SYNC DATE=06/29/2010

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USB HUBS

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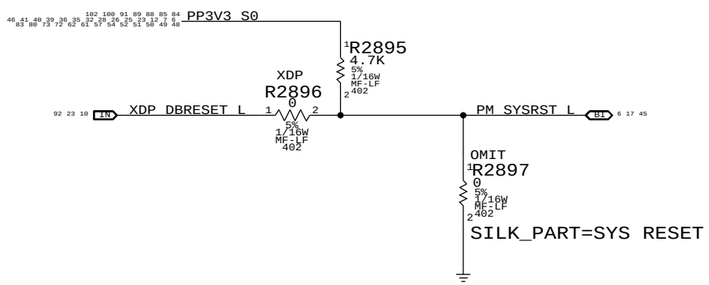
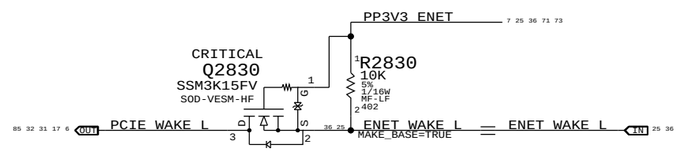
PCH Reset Button

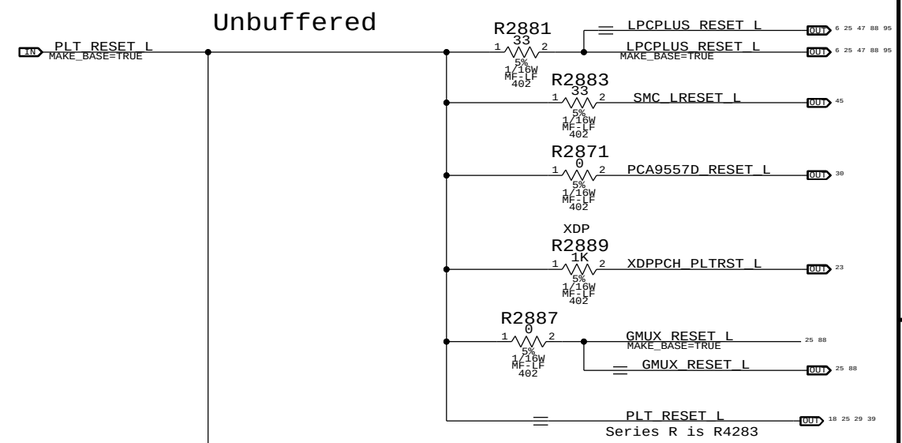


Ethernet WAKE# Isolation

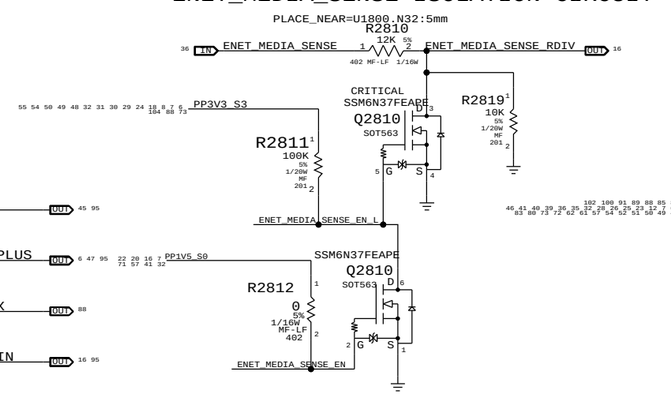


Platform Reset Connections

Unbuffered

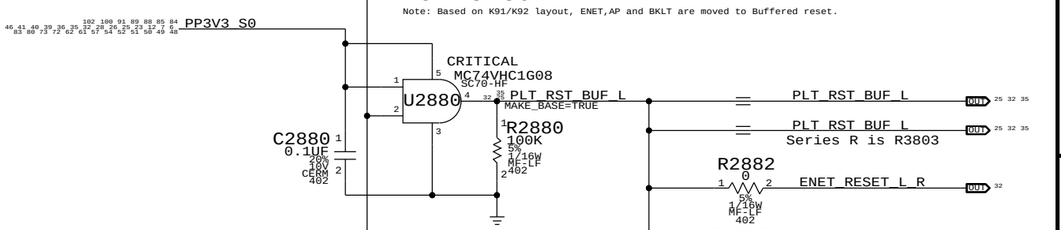


ENET_MEDIA_SENSE ISOLATION CIRCUIT



Buffered

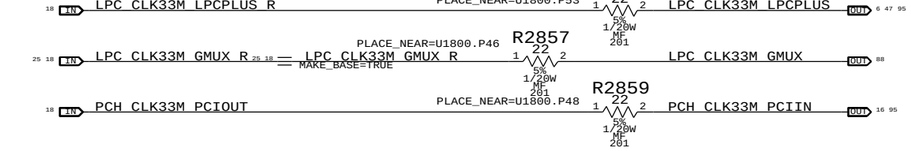
Note: Based on K91/K92 layout, ENET,AP and BKLT are moved to Buffered reset.

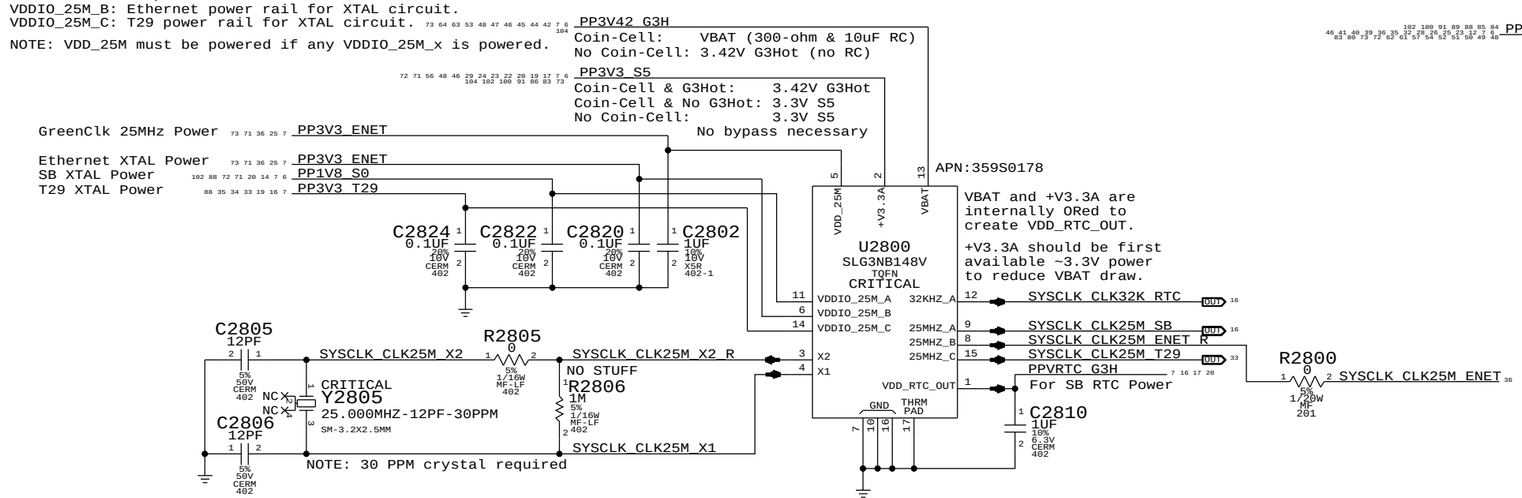


System RTC Power Source & 32kHz / 25MHz Clock Generator

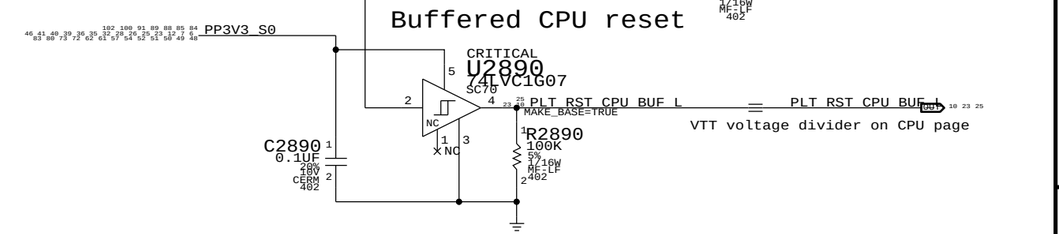
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.





Buffered CPU reset



SYNC MASTER=K91_MLB	SYNC DATE=06/29/2010
PAGE TITLE: Chipset Support	
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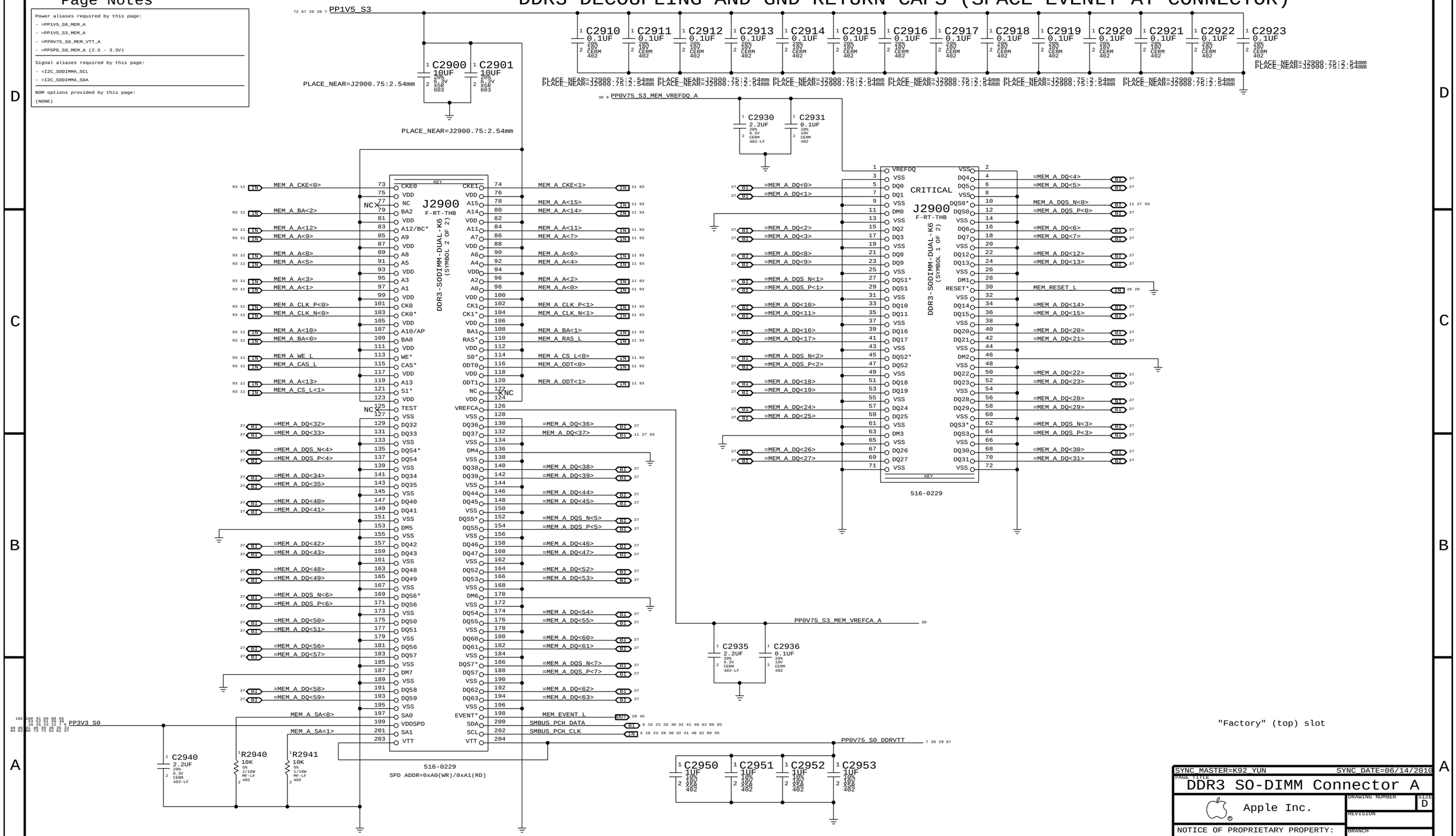
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)



SYNC MASTER=K92_YUN SYNC DATE=06/14/2010

PAGE TITLE
DDR3 SO-DIMM Connector A

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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

93 27 26 11	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	MEM_A_DQS_N<0>	11 26 27 93 93 28 27 11
93 11	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	26
93 11	MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	26
93 11	MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	26
93 11	MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	26
93 11	MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	26
93 11	MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	26
93 11	MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	26
93 11	MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	26
93 11	MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	26

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

93 11	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	26
93 11	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	26
93 11	MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	26
93 11	MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	26
93 11	MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	26
93 11	MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	26
93 11	MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	26
93 11	MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	26
93 11	MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	26
93 11	MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	26

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

93 11	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	26
93 11	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	26
93 11	MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	26
93 11	MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	26
93 11	MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	26
93 11	MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	26
93 11	MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	26
93 11	MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	26
93 11	MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	26
93 11	MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	26

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

93 11	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	26
93 11	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	26
93 11	MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	26
93 11	MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	26
93 11	MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	26
93 11	MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	26
93 11	MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	26
93 11	MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	26
93 11	MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	26
93 11	MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	26

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

93 11	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	26
93 11	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	26
93 11	MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	26
93 11	MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	26
93 27 26 11	MEM_A_DQ<37>	MAKE_BASE=TRUE	MEM_A_DQ<37>	11 26 27 93 93 28 27 11
93 11	MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	26
93 11	MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	26
93 11	MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	26
93 11	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	26
93 11	MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	26

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

93 11	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	26
93 11	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	26
93 11	MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	26
93 11	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	26
93 11	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	26
93 11	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	26
93 11	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	26
93 11	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	26
93 11	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	26
93 11	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	26

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

93 11	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	26
93 11	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	26
93 11	MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	26
93 11	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	26
93 11	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	26
93 11	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	26
93 11	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	26
93 11	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	26
93 11	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	26
93 11	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	26

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

93 11	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	26
93 11	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	26
93 11	MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	26
93 11	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	26
93 11	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	26
93 11	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	26
93 11	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	26
93 11	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	26
93 11	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	26
93 11	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	26

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

93 28 27 11	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	MEM_B_DQS_N<0>	11 27 28 93
93 28 27 11	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	MEM_B_DQS_P<0>	11 27 28 93
93 11	MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	28
93 11	MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	28
93 11	MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	28
93 11	MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	28
93 11	MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	28
93 11	MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	28
93 11	MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	28
93 11	MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	28

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

93 11	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	28
93 11	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	28
93 11	MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	28
93 11	MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	28
93 11	MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	28
93 11	MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	28
93 11	MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	28
93 11	MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	28
93 11	MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	28
93 11	MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	28

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

93 11	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	28
93 11	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	28
93 11	MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	28
93 11	MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	28
93 11	MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	28
93 11	MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	28
93 11	MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	28
93 11	MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	28
93 11	MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	28
93 11	MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	28

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

93 11	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	28
93 11	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	28
93 11	MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	28
93 11	MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	28
93 11	MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	28
93 11	MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	28
93 11	MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	28
93 11	MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	28
93 11	MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	28
93 11	MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	28

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

93 11	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	28
93 11	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	28
93 11	MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	28
93 11	MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	28
93 28 27 11	MEM_B_DQ<37>	MAKE_BASE=TRUE	MEM_B_DQ<37>	11 27 28 93
93 11	MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	28
93 11	MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	28
93 11	MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	28
93 11	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	28
93 11	MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	28

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

93 11	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	28
93 11	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	28
93 11	MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	28
93 11	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	28
93 11	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	28
93 11	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	28
93 11	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	28
93 11	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	28
93 11	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	28
93 11	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	28

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

93 11	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	28
93 11	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	28
93 11	MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	28
93 11	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	28
93 11	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	28
93 11	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	28
93 11	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	28
93 11	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	28
93 11	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	28
93 11	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	28

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

93 11	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	28
93 11	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	28
93 11	MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	28
93 11	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	28
93 11	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	28
93 11	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	28
93 11	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	28
93 11	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	28
93 11	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	28
93 11	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	28

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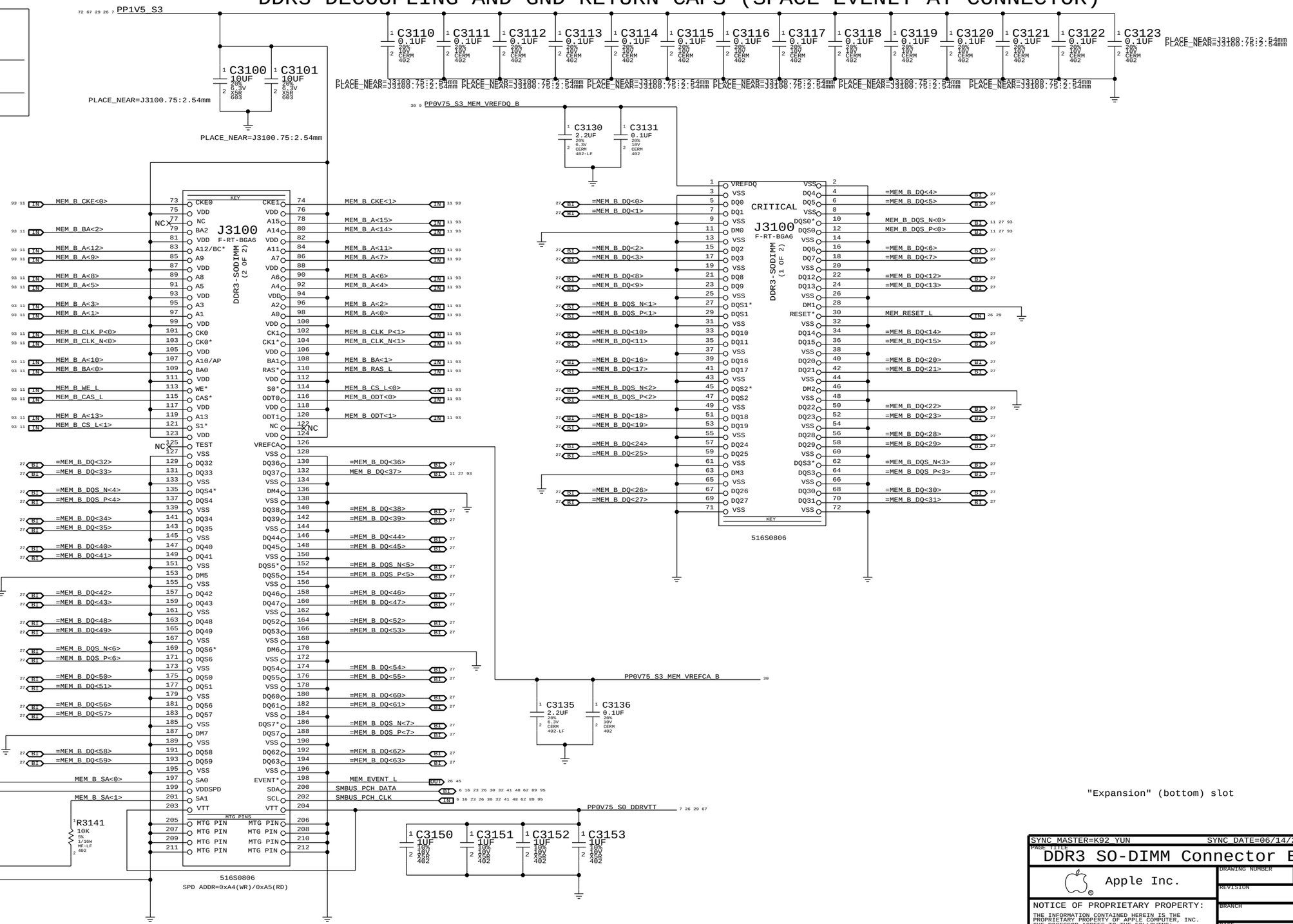
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)



"Expansion" (bottom) slot

SYNC MASTER=K92_YUN SYNC DATE=06/14/2010

PAGE TITLE
DDR3 SO-DIMM Connector B

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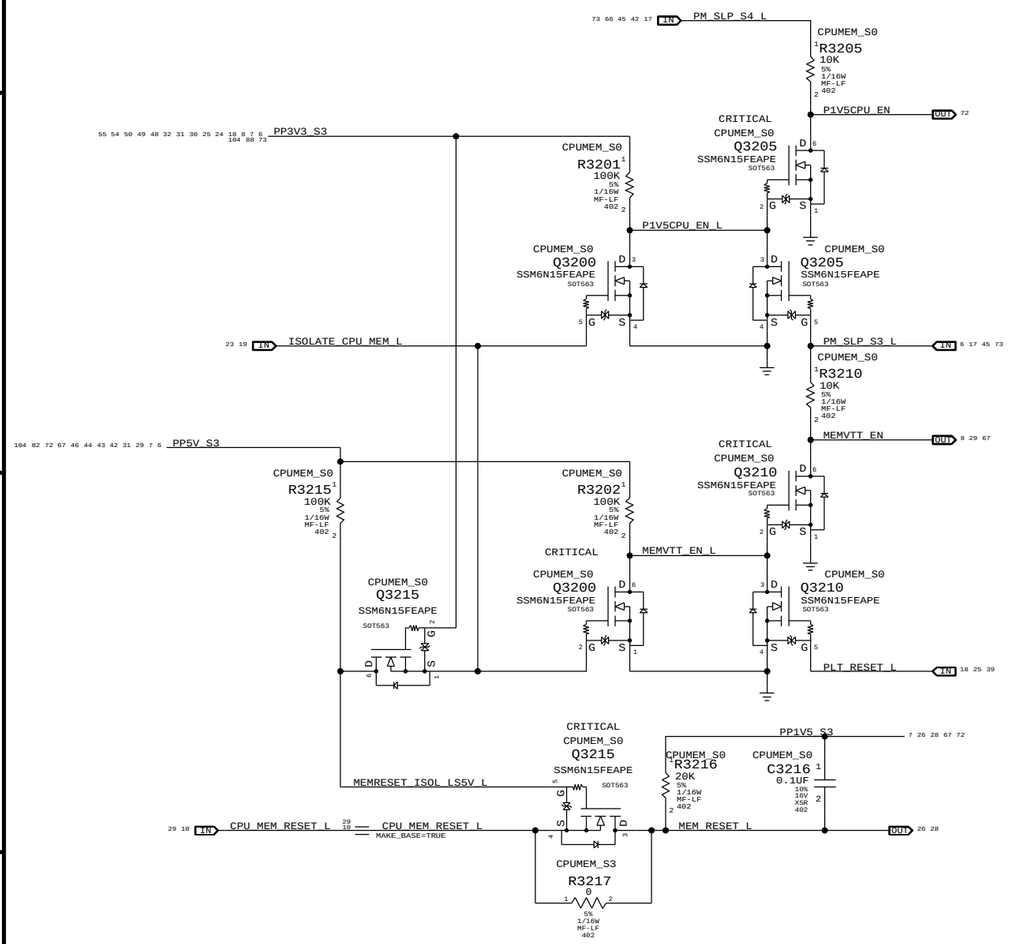
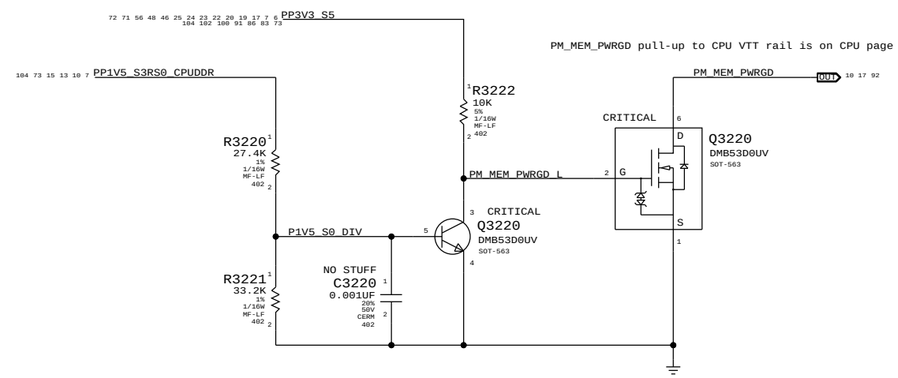
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

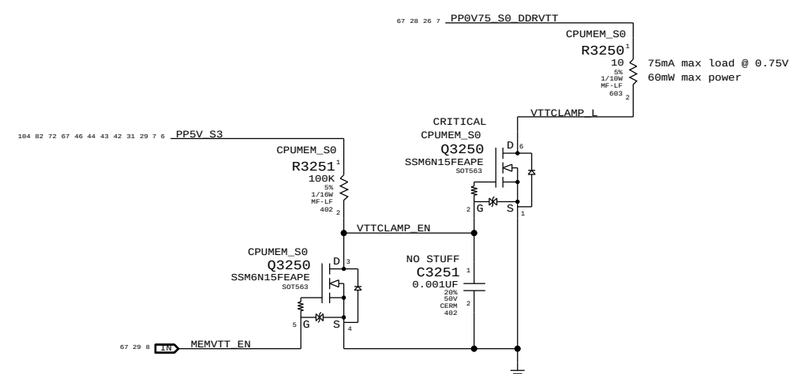


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
S3	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K17_MLB SYNC DATE=04/26/2010

PAGE TITLE
CPU Memory S3 Support

Apple Inc.

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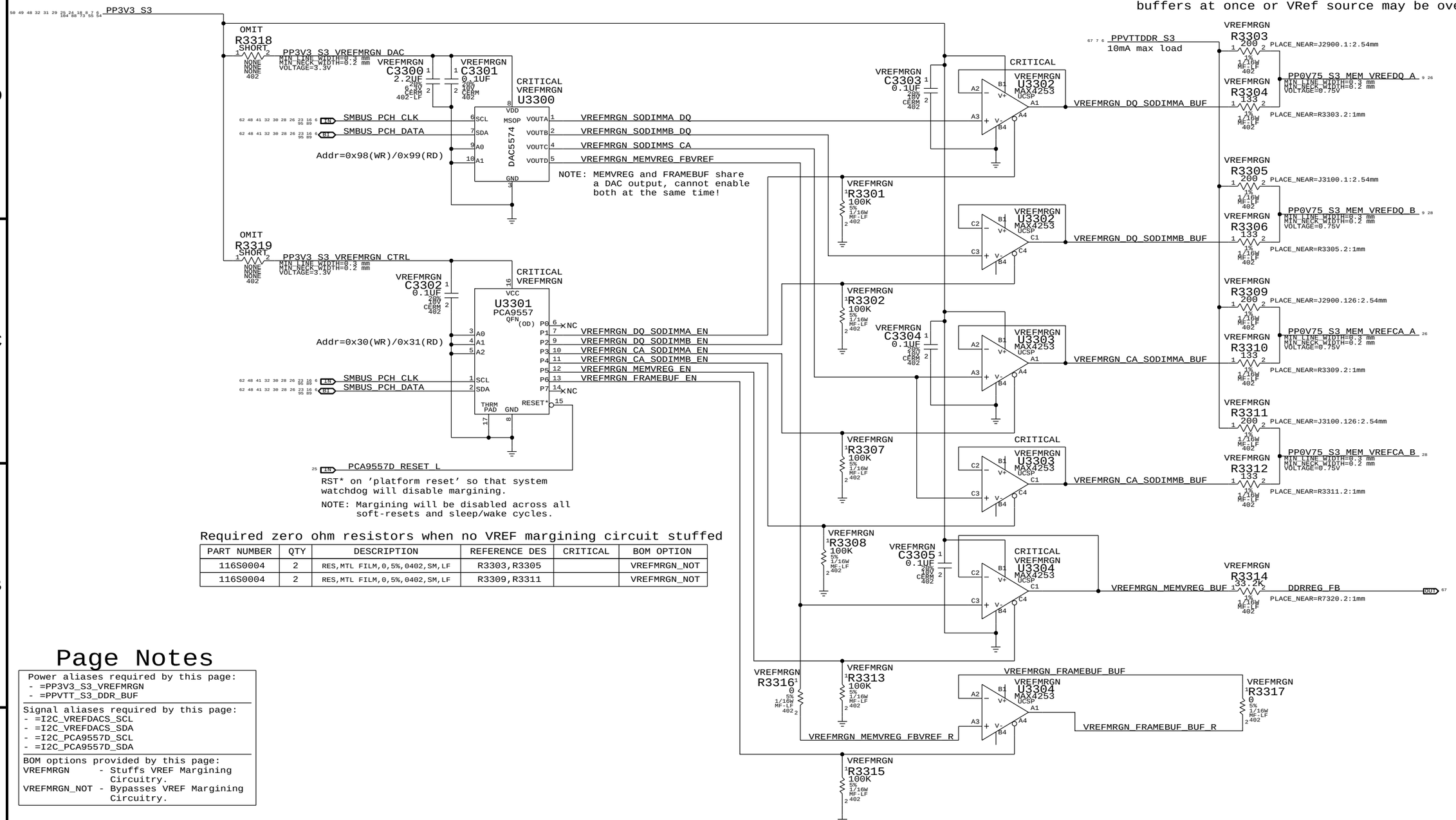
NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K91_YUN SYNC_DATE=08/26/2010

PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining

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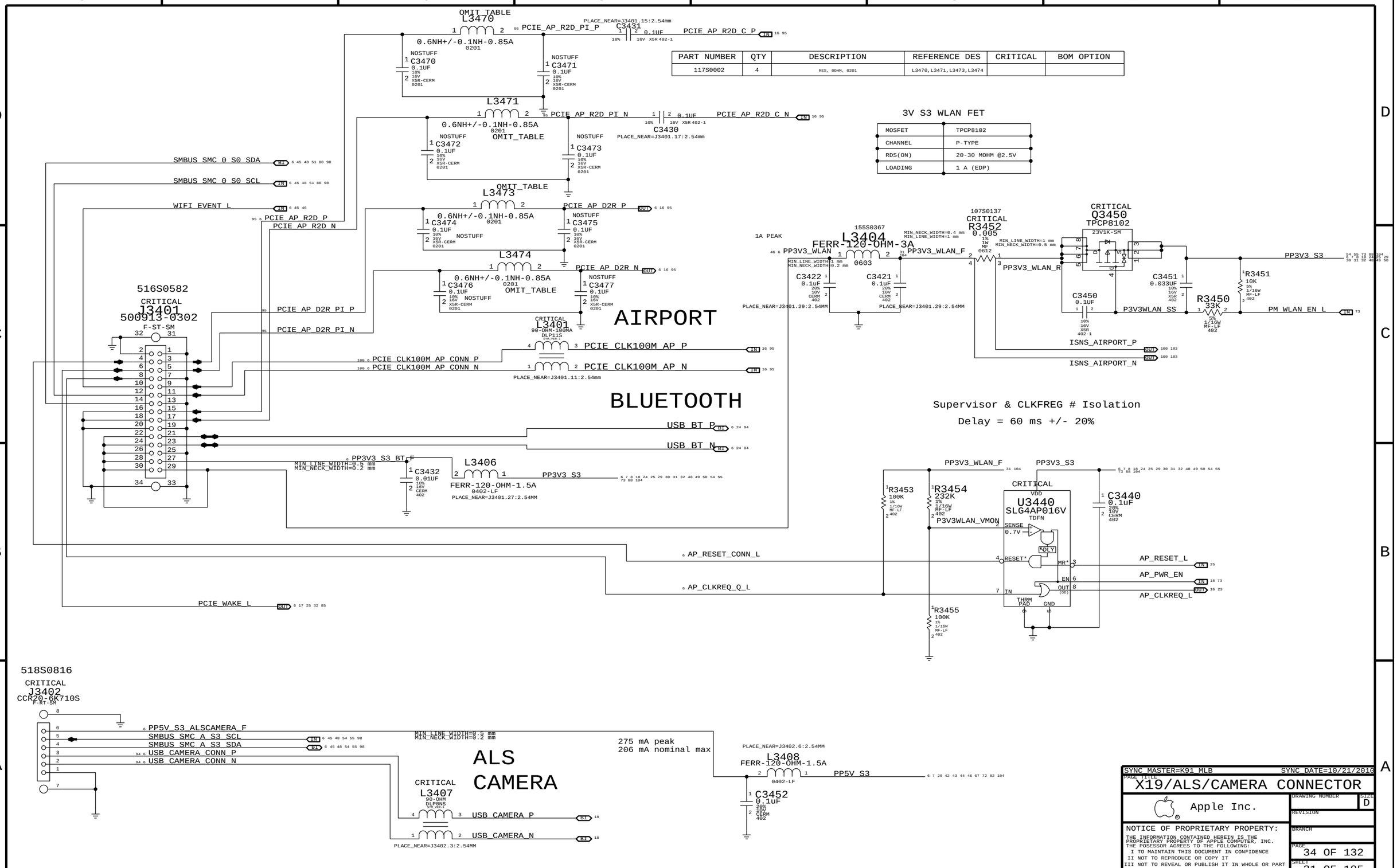

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L3470,L3471,L3473,L3474		

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	1 A (EDP)

SYNC_MASTER=K91_MLB SYNC_DATE=10/21/2016

PAGE TITLE: X19/ALS/CAMERA CONNECTOR

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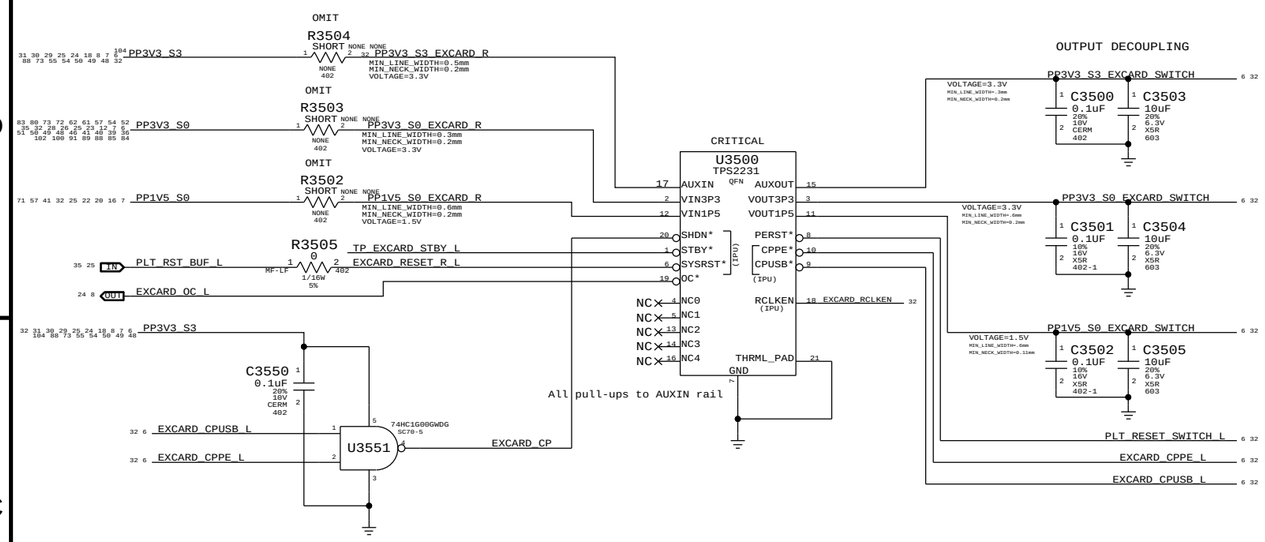
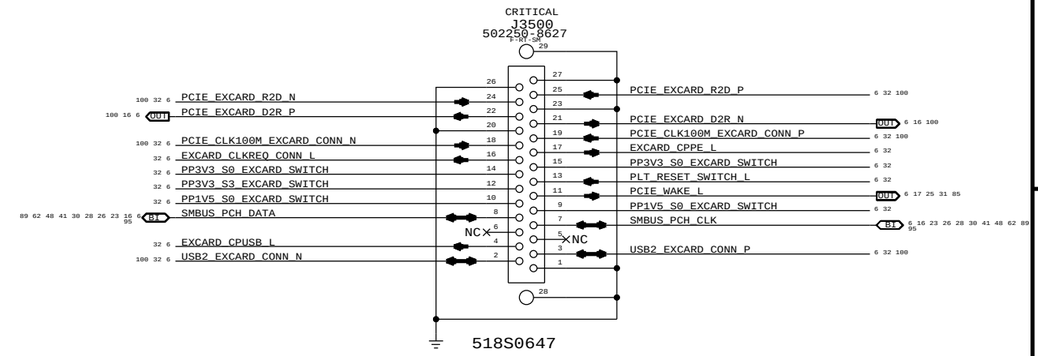
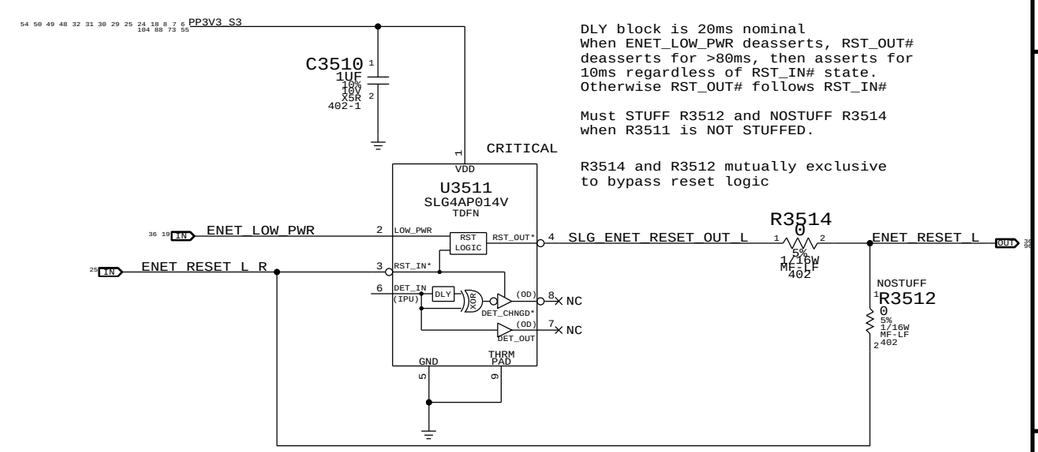


EXPRESSCARD/34 FLEX CONNECTOR



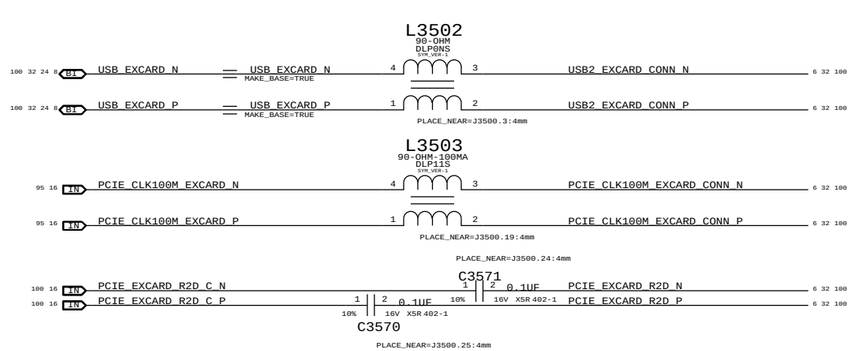
DETECT-CHANGED PCH GPIO LATCH CIRCUIT



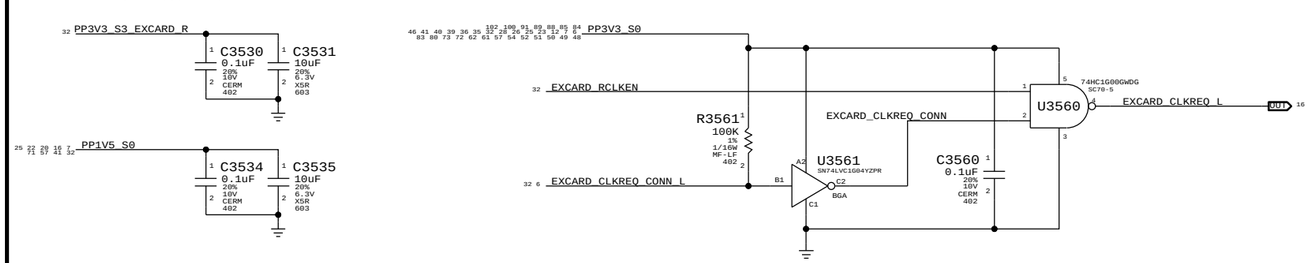
DLY block is 20ms nominal
When ENET_LOW_PWR deasserts, RST_OUT# deasserts for >80ms, then asserts for 10ms regardless of RST_IN# state.
Otherwise RST_OUT# follows RST_IN#

Must STUFF R3512 and NOSTUFF R3514 when R3511 is NOT STUFFED.

R3514 and R3512 mutually exclusive to bypass reset logic



INPUT DECOUPLING



SYNC_MASTER=K92_ERIC	SYNC_DATE=07/27/2010
PAGE TITLE: ExpressCard Connector	
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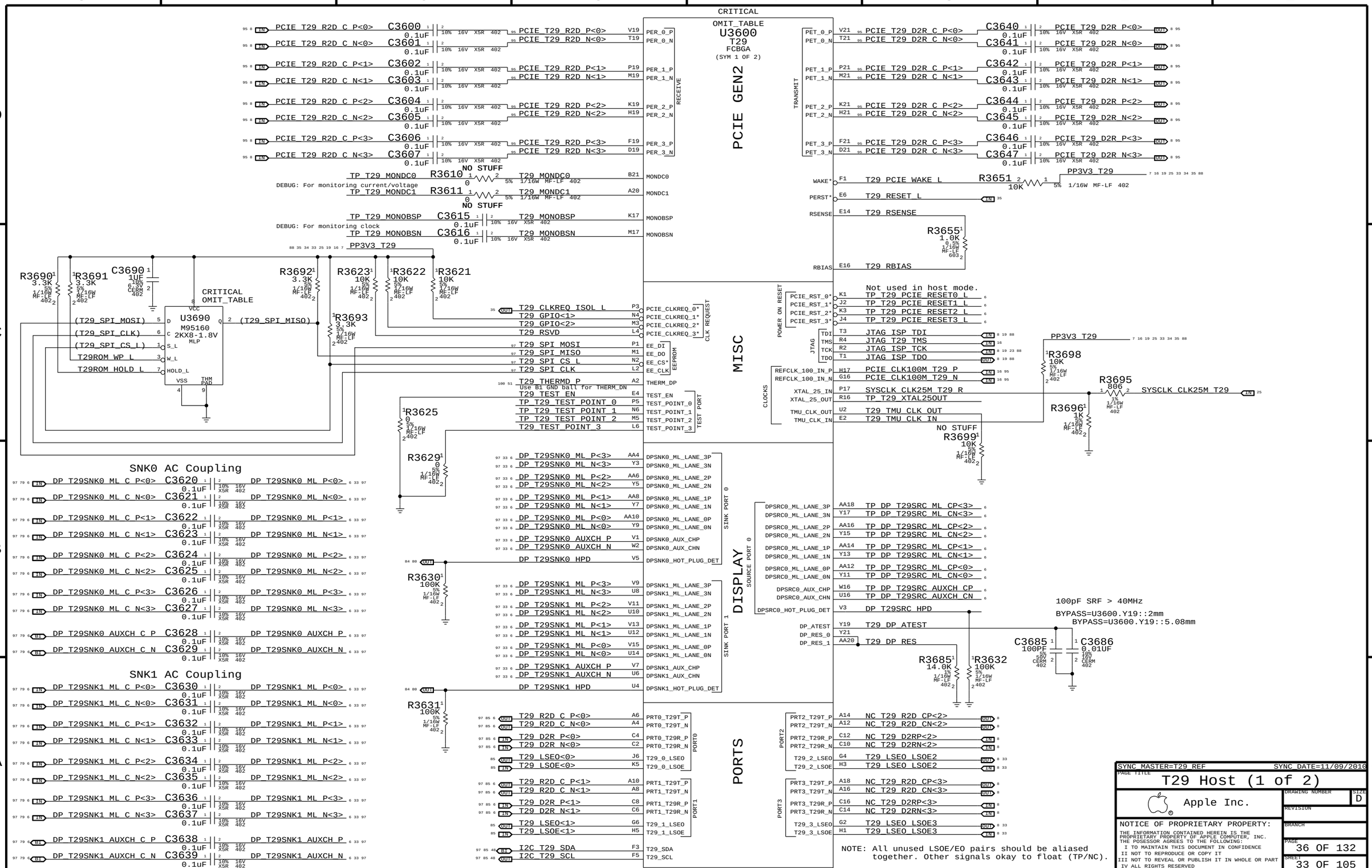

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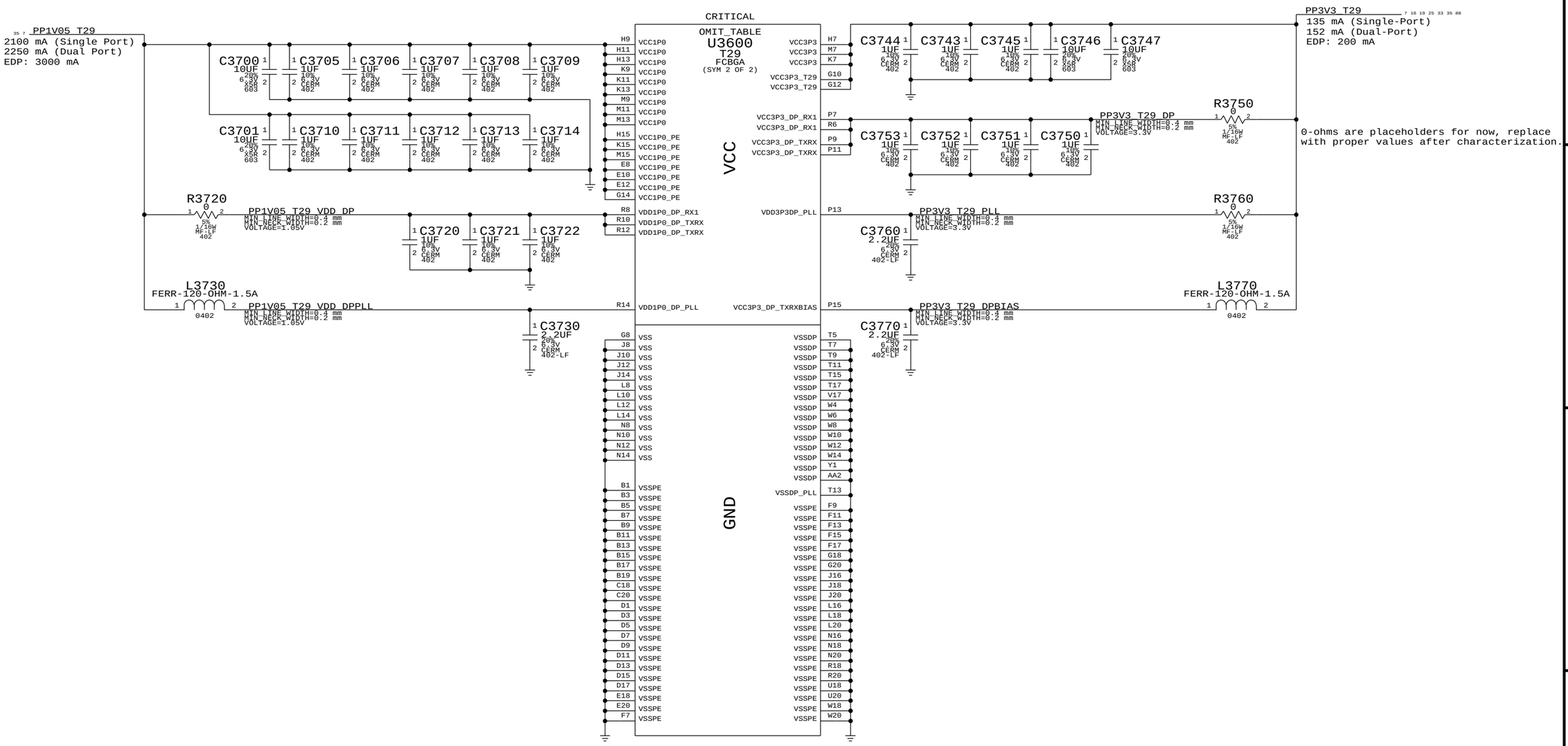

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_REF SYNC_DATE=11/09/2010

PAGE TITLE: T29 Host (2 of 2)

Apple Inc.

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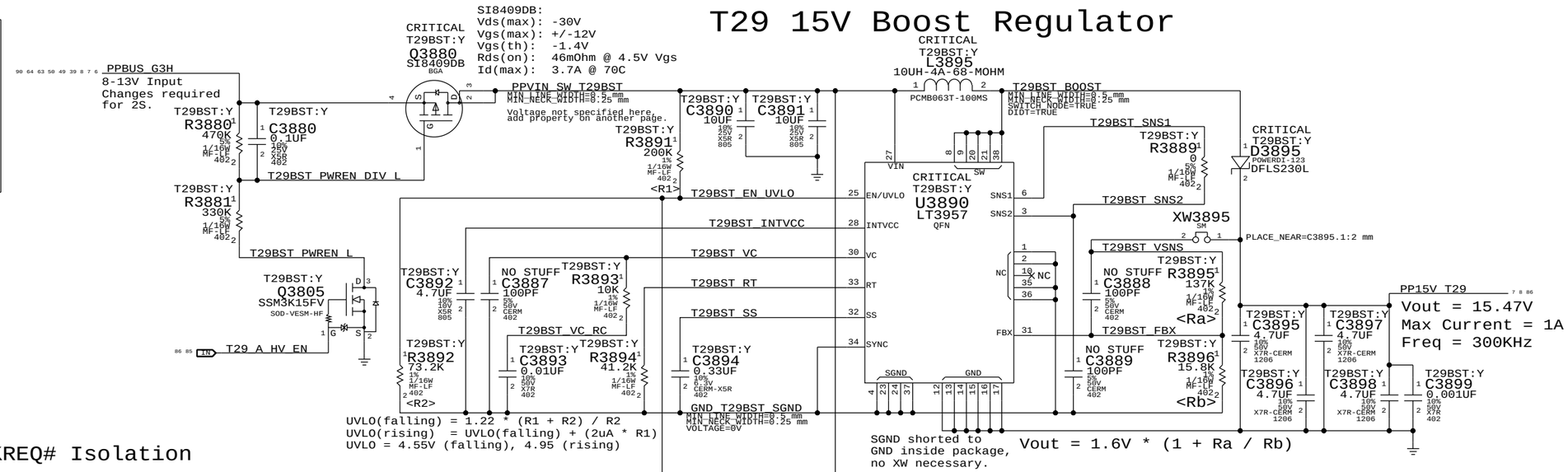
Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

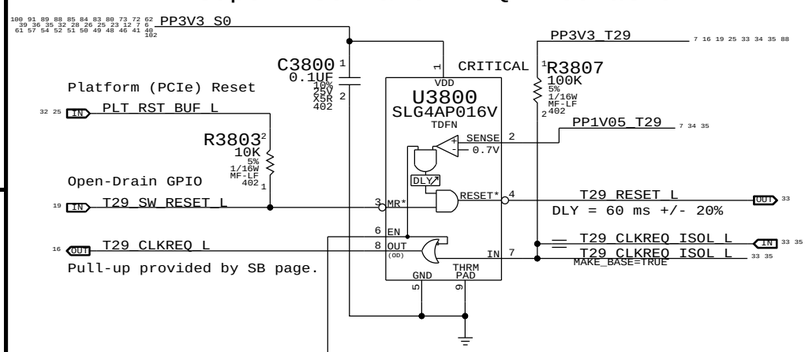
Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

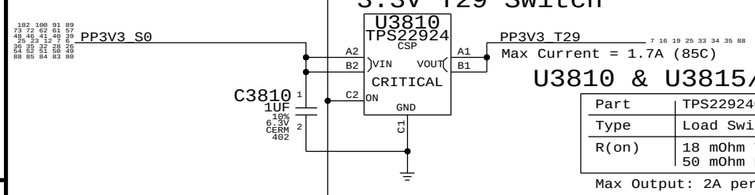
T29 15V Boost Regulator



Supervisor & CLKREQ# Isolation



3.3V T29 Switch

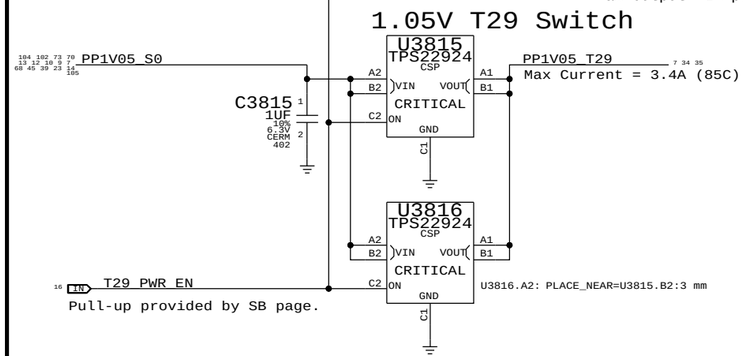


U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch



SYNC_MASTER=T29_REF SYNC_DATE=11/09/2010

PAGE TITLE: T29 Power Support

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

CRITICAL L3900 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_XTALVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V) — C3900 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3905 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_BIASVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V) — C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3910 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_AVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V) — R3910 4.7K 5% 1/16W MF-LF 402; C3910 0.1UF 10% 16V X7R-CERM 402; C3911 0.1UF 10% 16V X7R-CERM 402

VDD for Card Reader I/O
PP3V3R1V8_ENET_LR_OUT_REG

ENET_SR_LX
PP1V2_ENET

Internal 1.2V Switching Regulator pins.

PP1V2_ENET
???mA (1000base-T, Caesar V)

CRITICAL L3920 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_AVDDL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V) — C3921 0.1UF 10% 16V X7R-CERM 402; C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_PCIEPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V) — C3926 0.1UF 10% 16V X7R-CERM 402; C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_GPHYPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V) — C3931 0.1UF 10% 16V X7R-CERM 402; C3930 4.7UF 10% 6.3V X5R-CERM 603

R3940 4.7K 5% 1/16W MF-LF 402; R3941 4.7K 5% 1/16W MF-LF 402; C3915 4.7UF 10% 6.3V X5R-CERM 603; C3916 0.1UF 10% 16V X7R-CERM 402; C3936 0.1UF 10% 16V X7R-CERM 402; CRITICAL C3935 10UF 10% 6.3V X5R 805

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PP3V3_S0 — R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402; C3951 0.1uF 10% 16V X5R 402; C3955 0.1uF 10% 16V X5R 402; C3956 0.1uF 10% 16V X5R 402

PCIE_ENET_D2R_N — PCIE_ENET_D2R_P — PCIE_ENET_R2D_C_P — PCIE_ENET_R2D_C_N

ENET_WAKE_L (See note) — R3943 0 5% 1/16W MF-LF 402

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

OMIT
U3900
BCM57765B0
QFN-8X8
CRITICAL

Signal	Pin	Notes
ENET_VMAIN_PRSNT	58	VMAIN_PRSNT(IPD)
PCIE_ENET_D2R_C_N	27	PCIE_TXD_N
PCIE_ENET_D2R_C_P	28	PCIE_TXD_P
PCIE_ENET_R2D_P	33	PCIE_RXD_P
PCIE_ENET_R2D_N	34	PCIE_RXD_N
PCIE_CLK100M_ENET_P	31	PCIE_REFCLK_P
PCIE_CLK100M_ENET_N	30	PCIE_REFCLK_N
ENET_RESET_L	11	PERST* (IPD)
ENET_CLKREQ_L	12	CLKREQ* (OD)
ENET_WAKE_R_L	3	WAKE* (OD)
ENET_LOW_PWR	4	LOW_PWR (IPD)
BCM57765_SMB_CLK	6	SMB_CLK
BCM57765_SMB_DATA	10	SMD_DATA (IPD)
BCM57765_SCLK	66	SCLK
BCM57765_MISO	64	SI/LINKLED*
BCM57765_MOSI	65	SO
BCM57765_CS_L	63	CS*
NC BCM57765_SPD100LED_L	2	SPD100LED*/SERIAL_DO (OD)
NC BCM57765_TRAFFICLED_L	67	TRAFFICLED*/SERIAL_DI (OD)
SYSCLK_CLK25M_ENET	18	XTALI
NC	19	XTALO
BCM57765_RDAC	38	RDAC
	69	THRM_PAD

(IPU)

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

Signal	Pin	Notes
TRD0_P	40	ENET_MDI_P<0>
TRD0_N	41	ENET_MDI_N<0>
TRD1_P	44	ENET_MDI_P<1>
TRD1_N	43	ENET_MDI_N<1>
TRD2_P	46	ENET_MDI_P<2>
TRD2_N	47	ENET_MDI_N<2>
TRD3_P	50	ENET_MDI_P<3>
TRD3_N	49	ENET_MDI_N<3>
GPIO_0	5	NC
GPIO_1/CR_BUS_PWR	8	
RE*/GPIO_2	9	ENET_MEDIA_SENSE
SD_DETECT/WE*	1	TP_SDCONN_DETECT_L
CR_CMD/CLE	26	TP_SDCONN_CMD
CR_CLK/RY_BY*	21	TP_SDCONN_CLK
CR_DATA0	25	TP_SDCONN_DATA<0>
CR_DATA1	24	TP_SDCONN_DATA<1>
CR_DATA2	23	TP_SDCONN_DATA<2>
CR_DATA3	22	TP_SDCONN_DATA<3>
CR_DATA4	52	TP_SDCONN_DATA<4>
CR_DATA5	53	TP_SDCONN_DATA<5>
CR_DATA6	54	TP_SDCONN_DATA<6>
CR_DATA7	55	TP_SDCONN_DATA<7>
CE*/MS_INS*	59	NC_CE_L_MS_INS_L
CR_LED/ALE	60	TP_ENET_CR_PWREN
CR_WP*/XD_WP*	57	TP_SDCONN_WP
XD_DETECT	68	BDM57765_SR_DISABLE

(IPU)

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

R3980 1K 5% 1/16W MF-LF 402

BCM57765 supports both active-levels for WP.

SR_DISABLE must be pulled down to use internal SR. IPD has a race condition.

PP3V3R1V8_ENET_LR_OUT_REG
PP3V3R1V8_ENET_LR_OUT_REG (MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V)

C3970 4.7UF 10% 6.3V X5R-CERM 603; C3971 0.1UF 10% 16V X7R-CERM 402; C3972 0.1UF 10% 16V X7R-CERM 402

R3965 1.24K 1% 1/16W MF-LF 402

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Required for proper PHY operation.
(Required ROM size TBD)

PP3V3_ENET — C3990 0.1UF 10% 16V X7R-CERM 402

U3990
AT45DB011D
SOIC-8S1
OMIT

Pin	Signal
6	VCC
2	SCK
4	CS*
5	WP*
3	RESET*
1	SI
8	SO
7	GND

BCM57765_SCLK — BCM57765_CS_L — BCM57765_MOSI — BCM57765_MISO

NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402; R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC MASTER=K92_ERIC SYNC DATE=10/19/2010

ETHERNET PHY (CAESAR IV)

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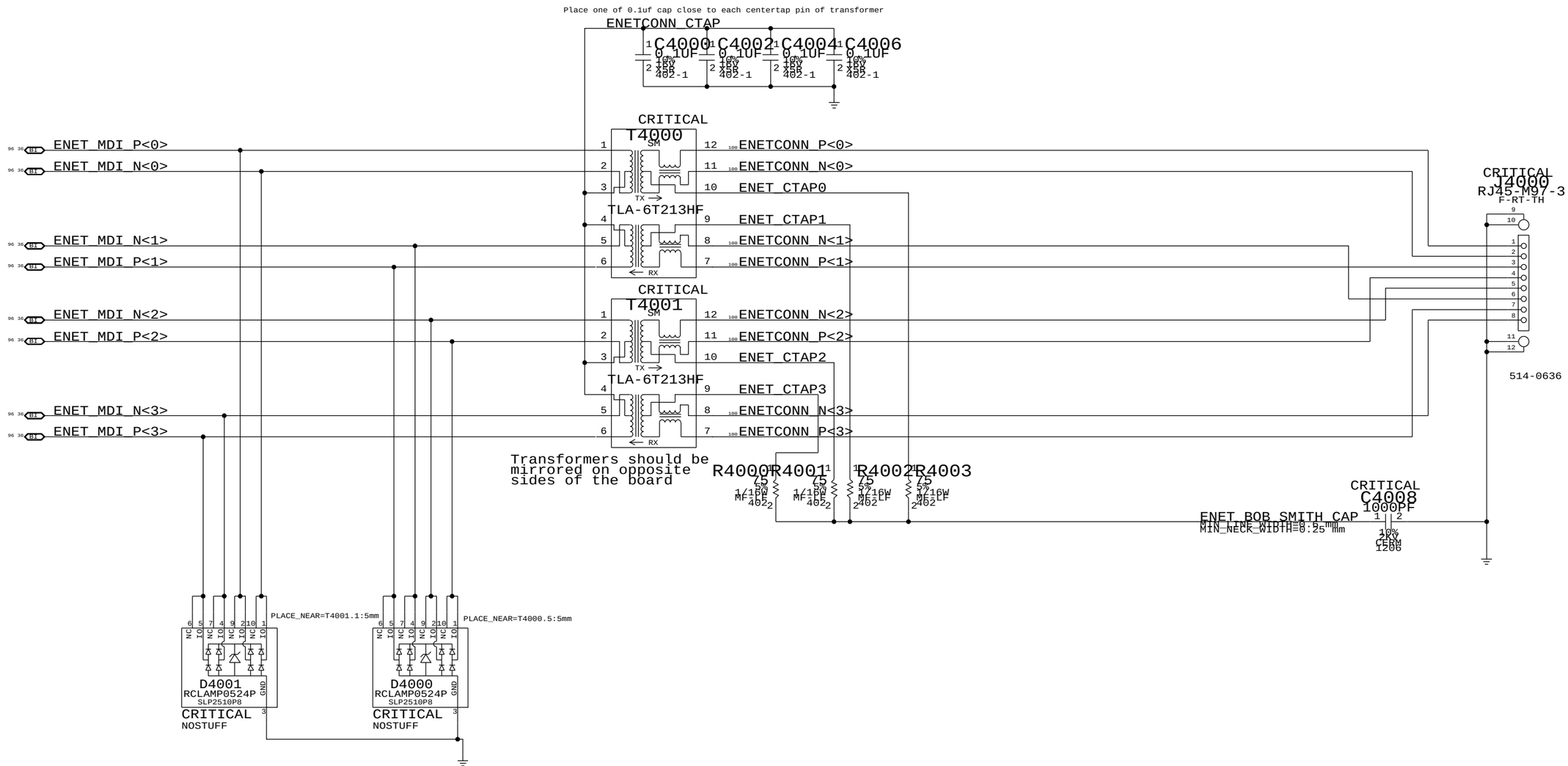
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K92_ERIC SYNC_DATE=08/24/2010

PAGE TITLE
Ethernet Connector

Apple Inc.

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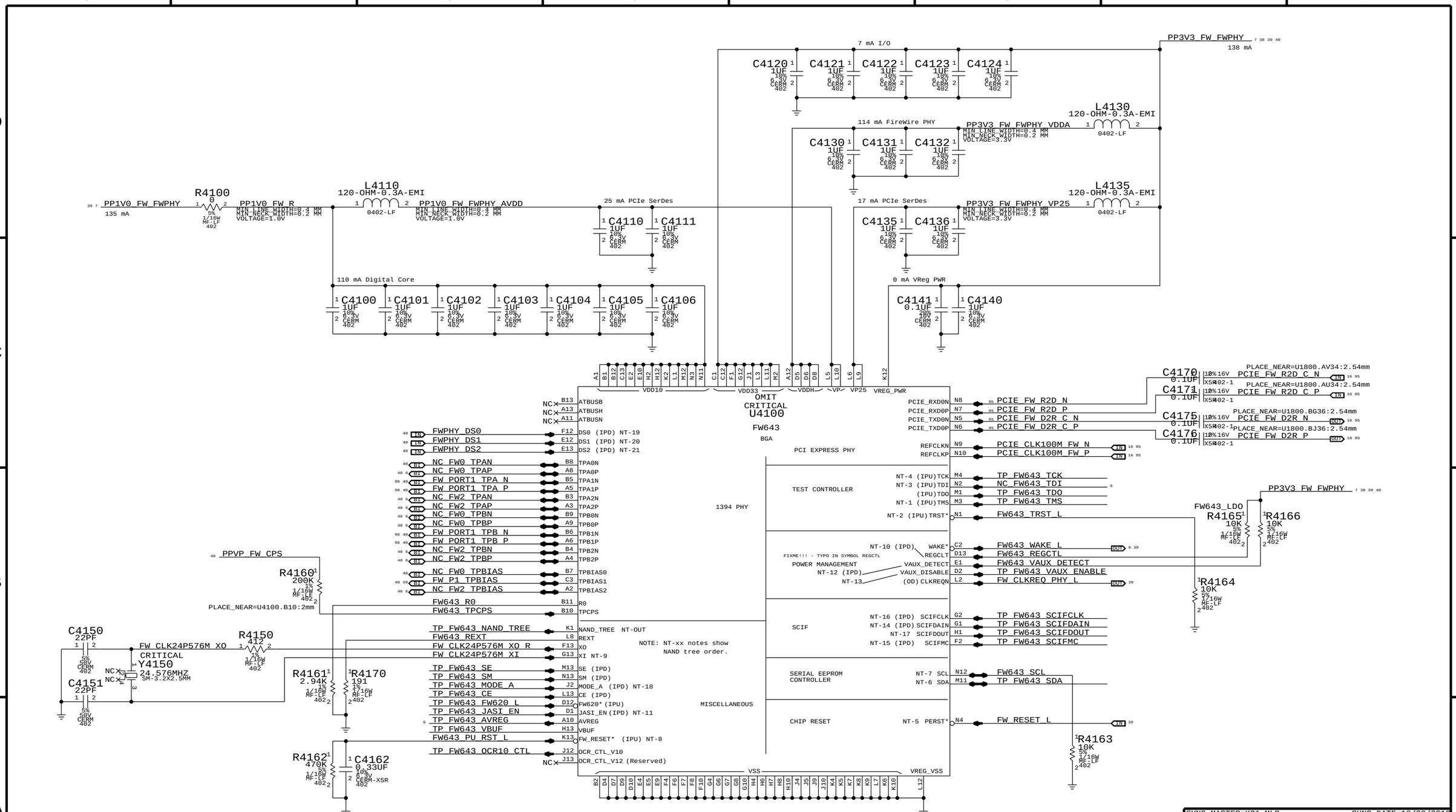

SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE

FireWire LLC/PHY (FW643)

Apple Inc.

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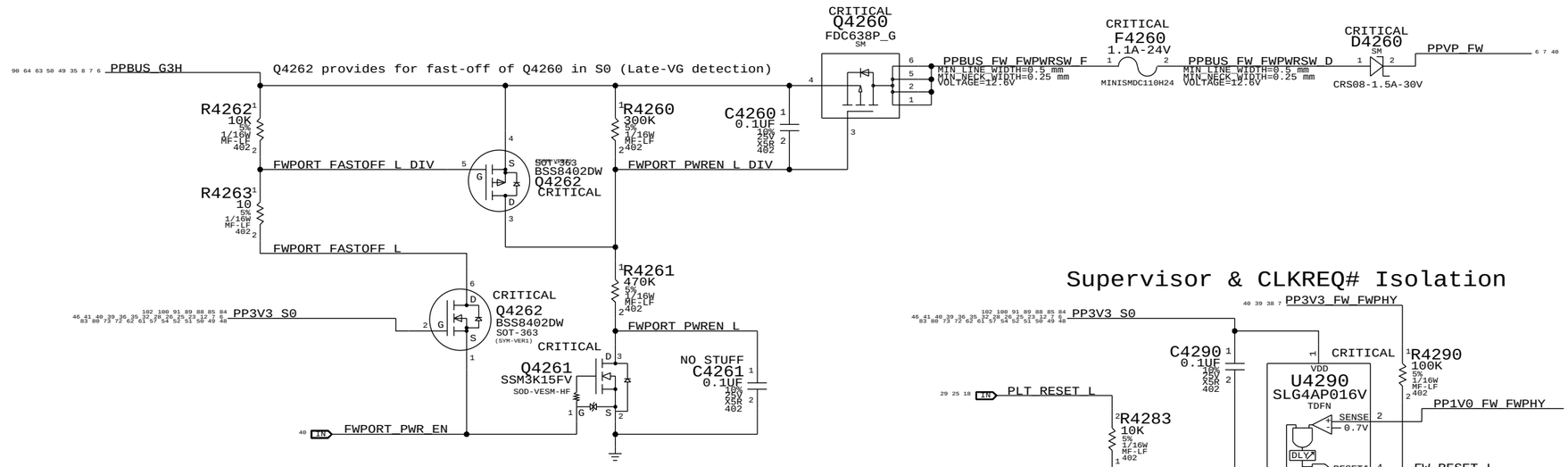
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

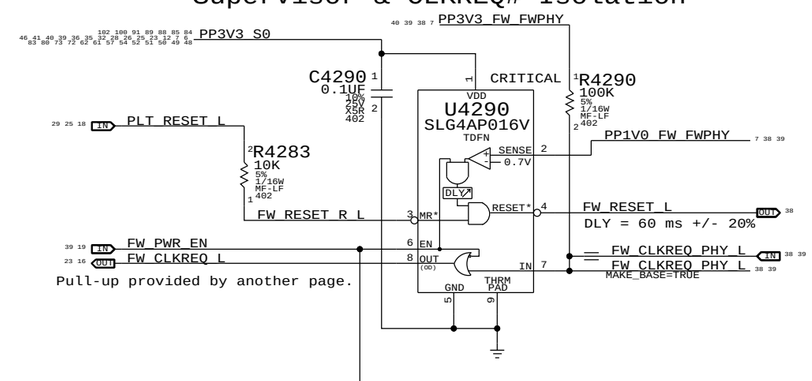
Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

FireWire Port Power Switch

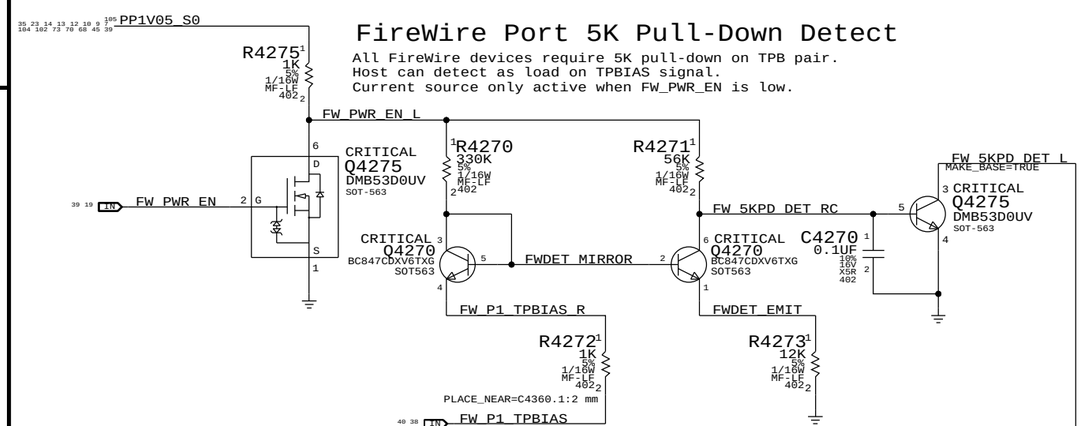


Supervisor & CLKREQ# Isolation



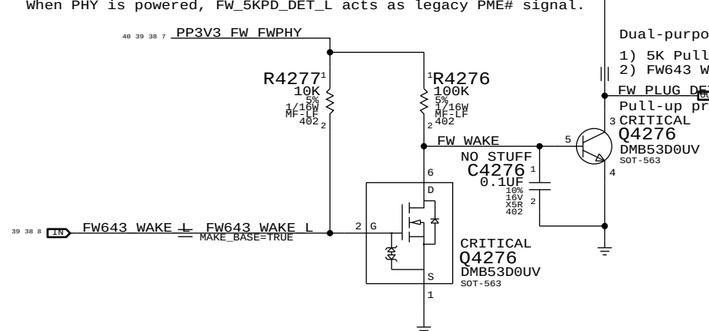
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



FireWire PHY WAKE# Support

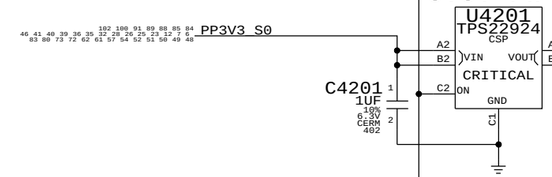
When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.



Dual-purpose output:
1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.

FW_PLUG_DET_L
Pull-up provided on another page.

3.3V FW Switch

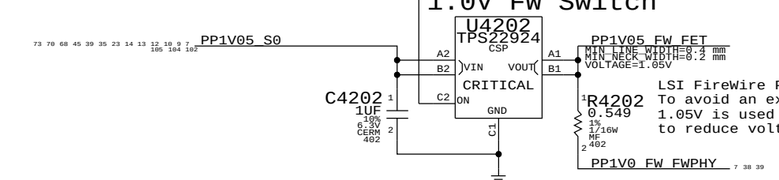


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

SYNC_MASTER=K91_MLB SYNC_DATE=10/20/2010

PAGE TITLE
FireWire Port & PHY Power

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

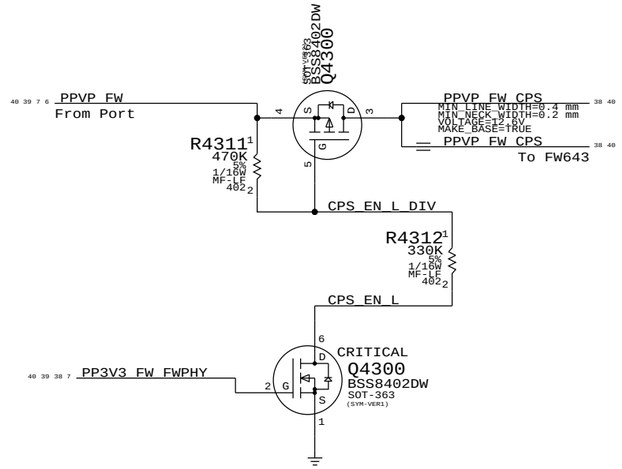
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

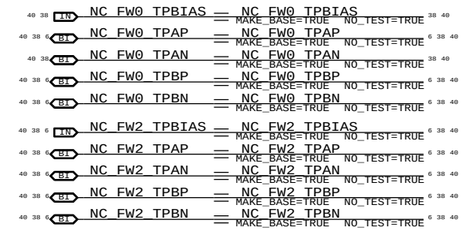
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



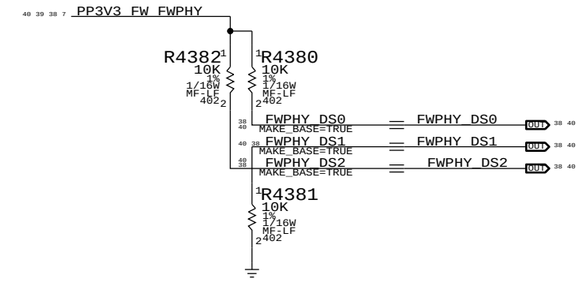
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



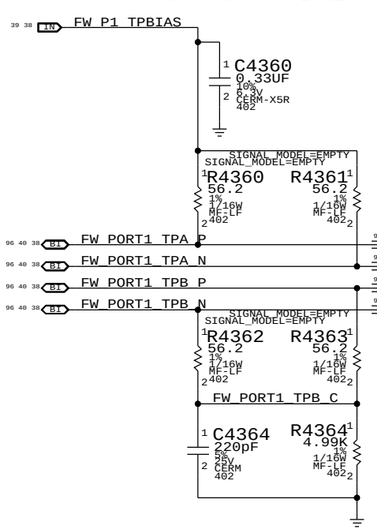
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

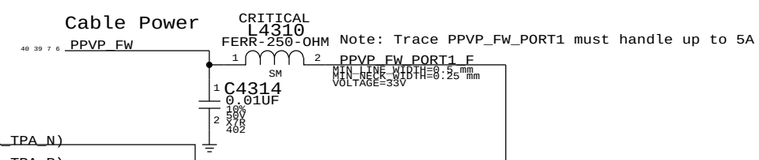


Termination

Place close to FireWire PHY

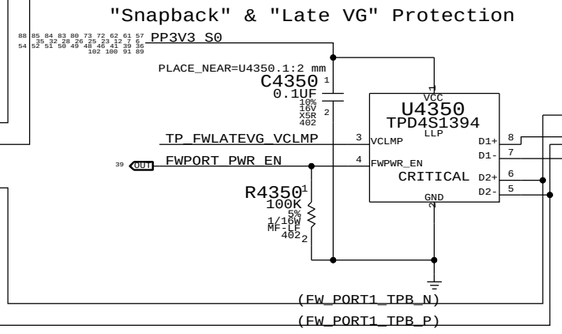


Cable Power



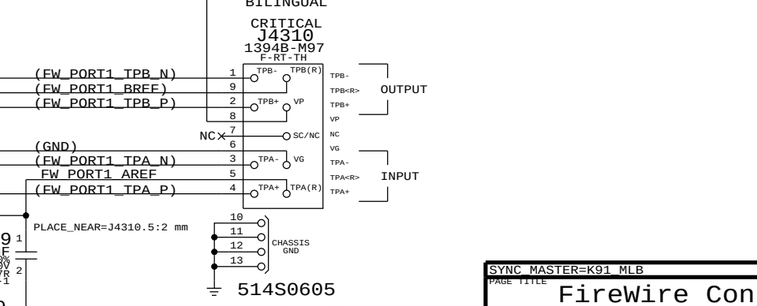
Note: Trace PPVP_FW_PORT1 must handle up to 5A

"Snapback" & "Late VG" Protection



PORT 1

BILINGUAL



AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

SYNC_MASTER=K91_MLB SYNC_DATE=07/22/2010

PAGE TITLE: FireWire Connector

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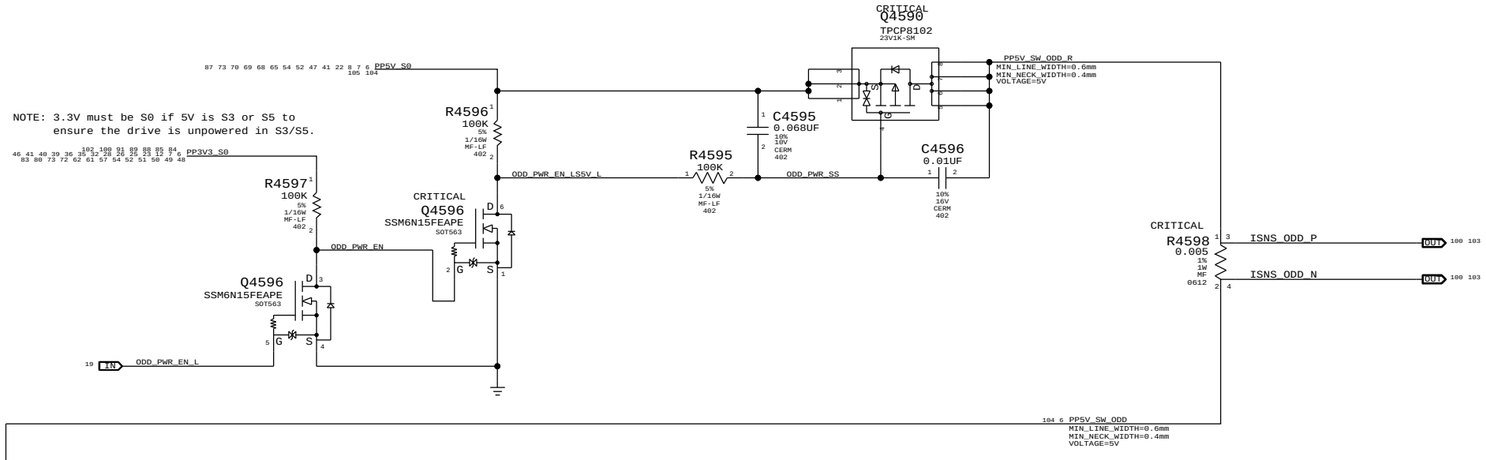
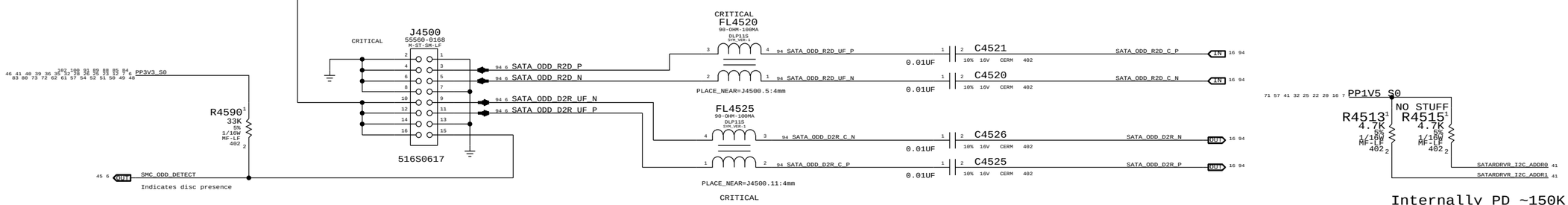
ODD Power Control



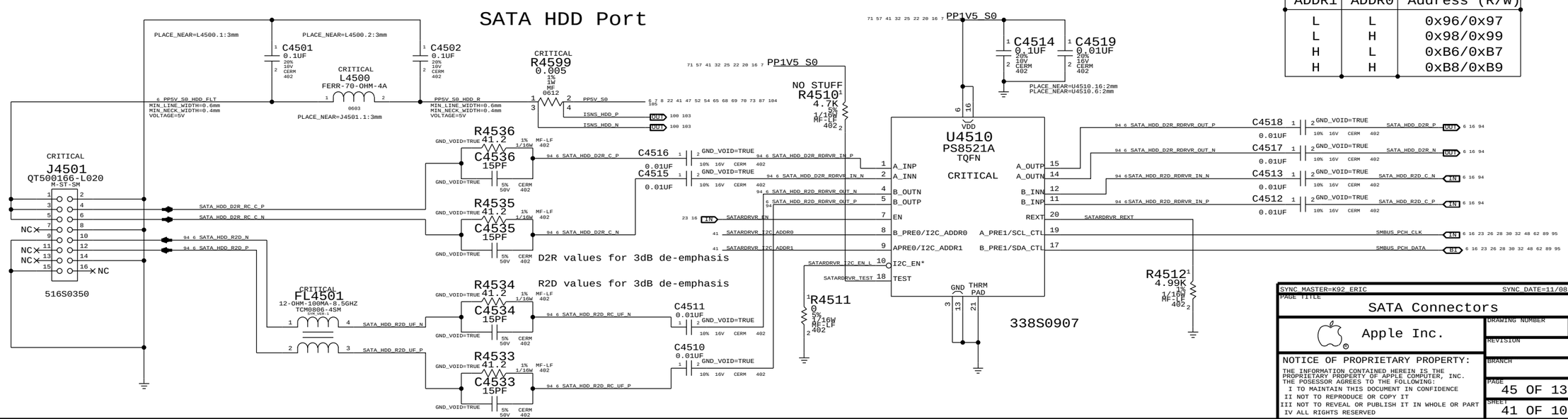
SATA ODD Port



Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADDR0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9

SATA HDD Port



SYNC_MASTER=K92_ERIC SYNC_DATE=11/08/2016

PAGE TITLE

SATA Connectors

Apple Inc.

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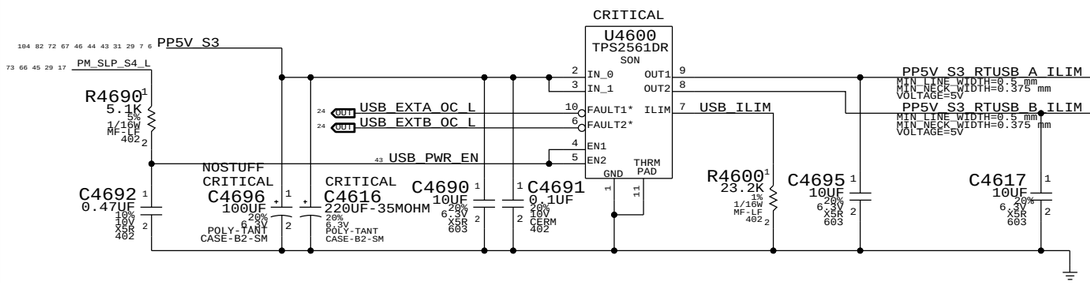
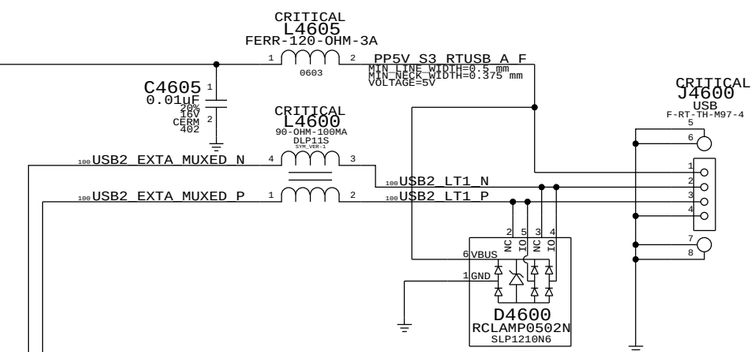
USB Port Power Switch



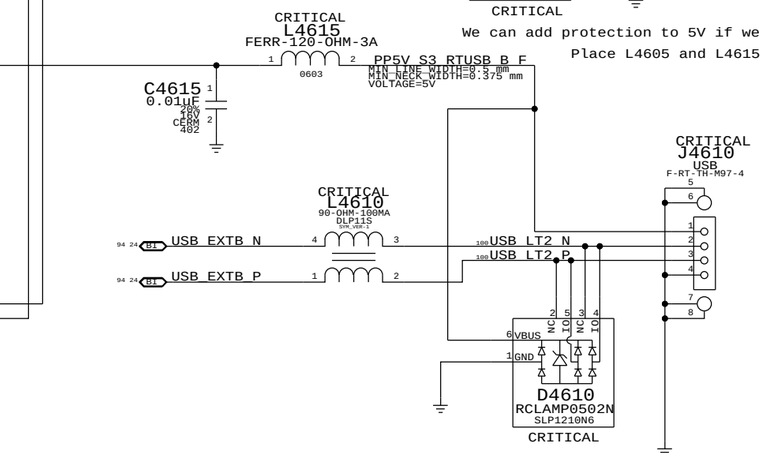
Current limit per port (R4600): 2.18A min / 2.63A max

Left USB Port A

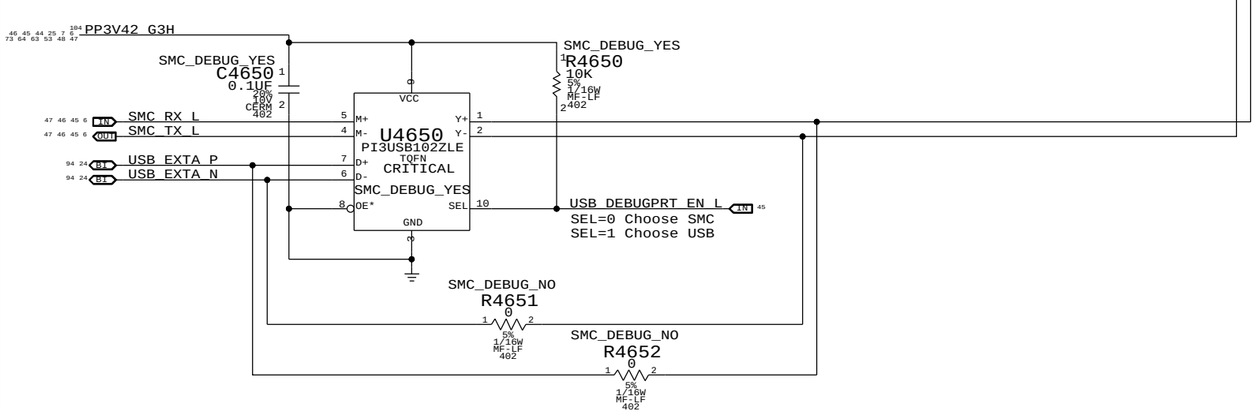


We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin



USB/SMC Debug Mux



SYNC_MASTER=K92_ERIC SYNC_DATE=08/24/2010

PAGE TITLE
External USB Connectors

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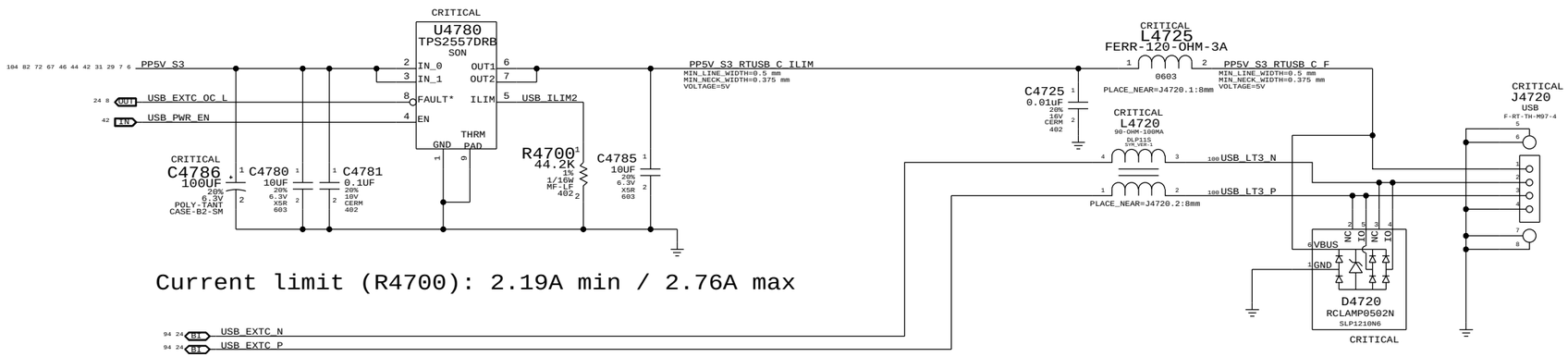
USB Port Power Switch

LEFT USB PORT C



Current limit (R4700): 2.19A min / 2.76A max

SYNC_MASTER=K92_ERIC SYNC_DATE=07/22/2010

PAGE TITLE

PROJECT SPECIFIC CONNS

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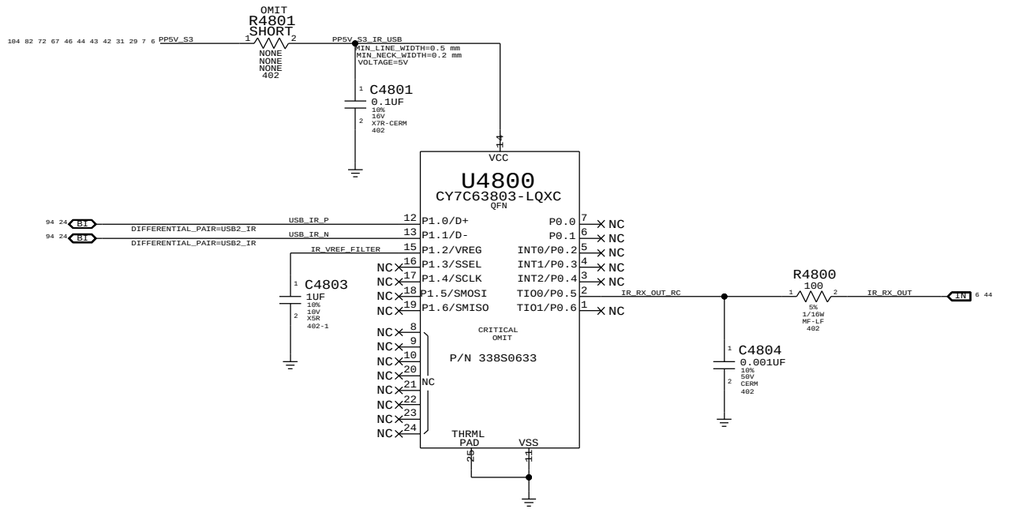

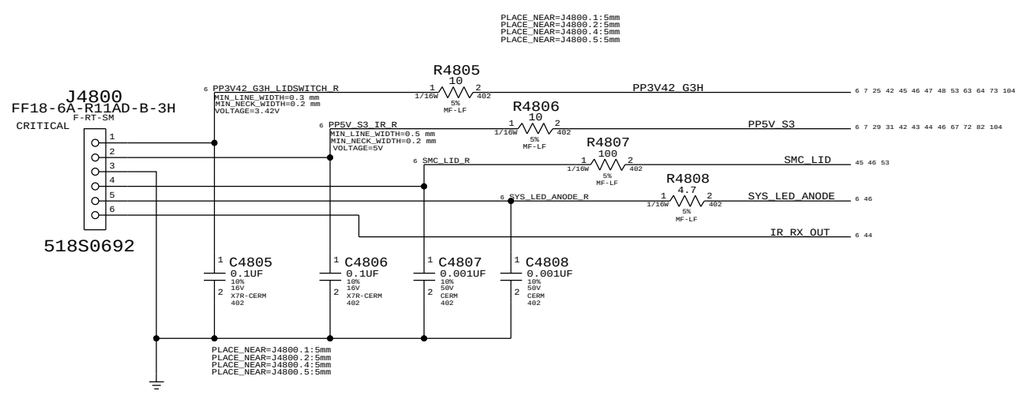

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

Front Flex Support

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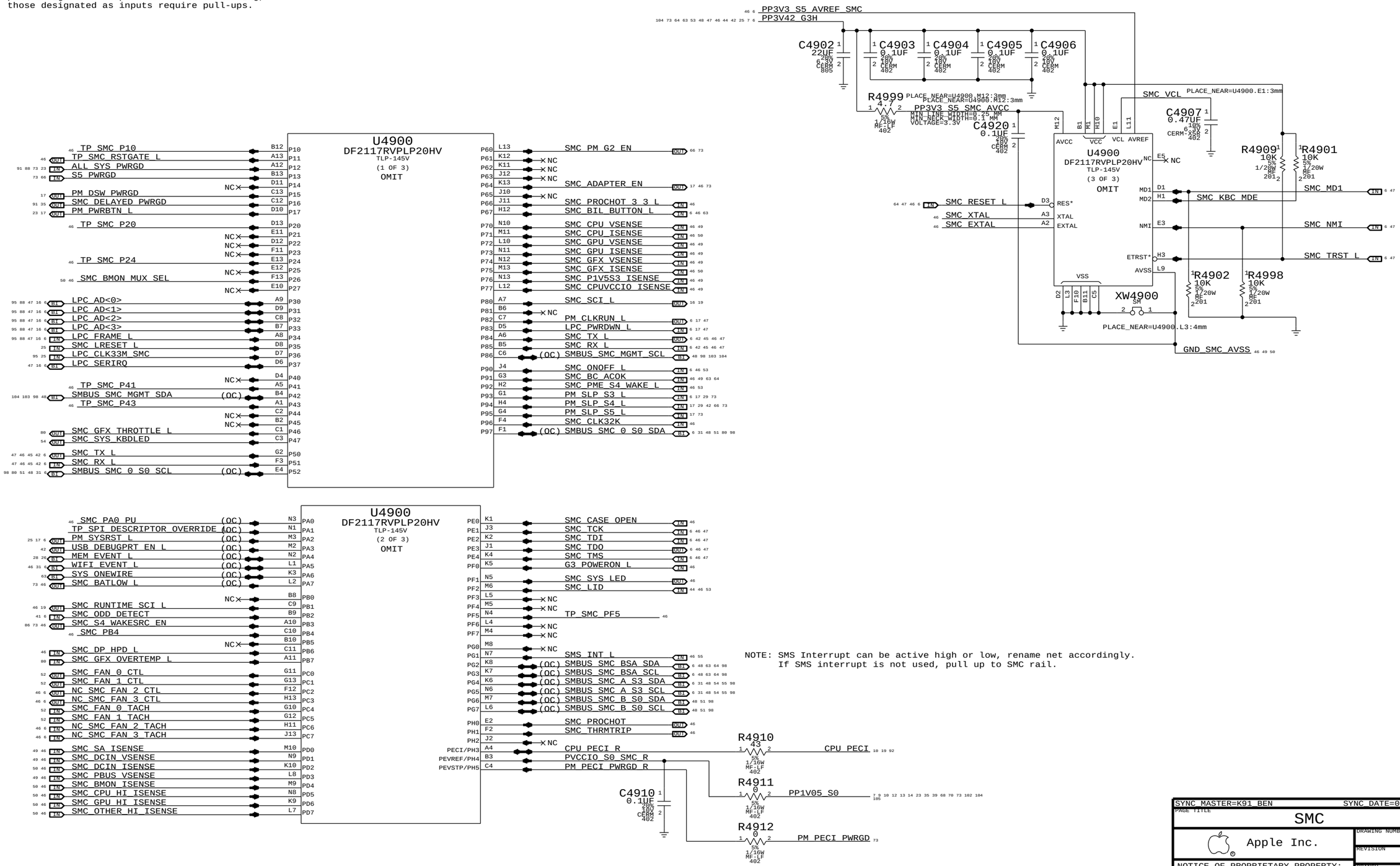
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designed as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=K91_BEN SYNC_DATE=07/12/2010

PAGE TITLE: SMC

Apple Inc.

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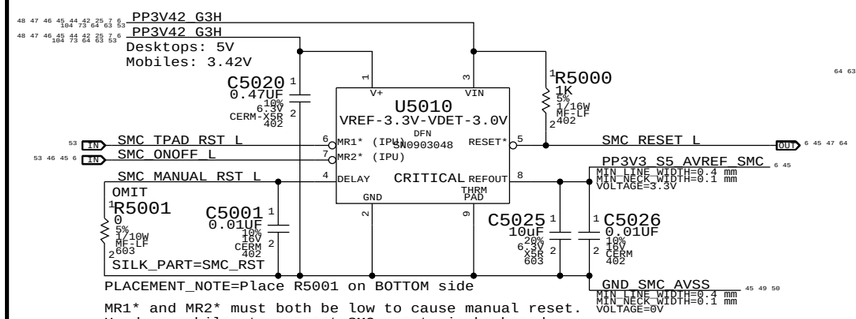
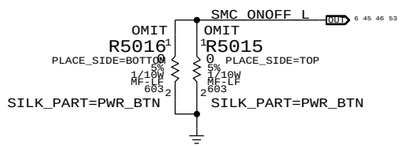
SMC Reset "Button", Supervisor & AVREF Supply



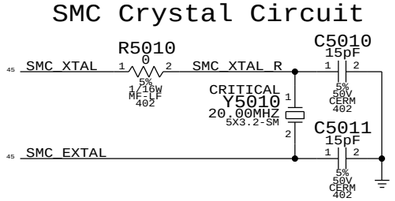
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

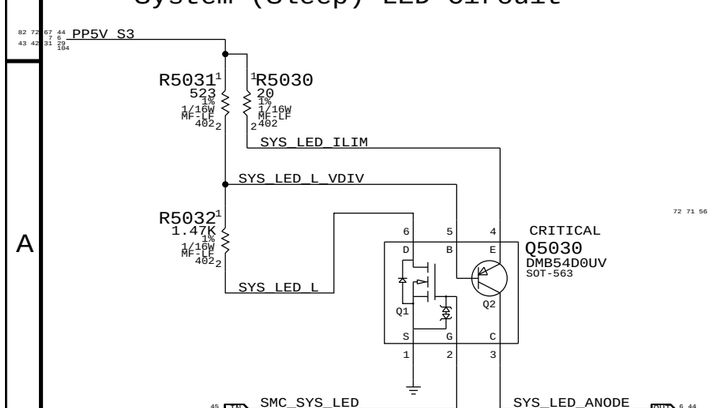
Debug Power "Buttons"

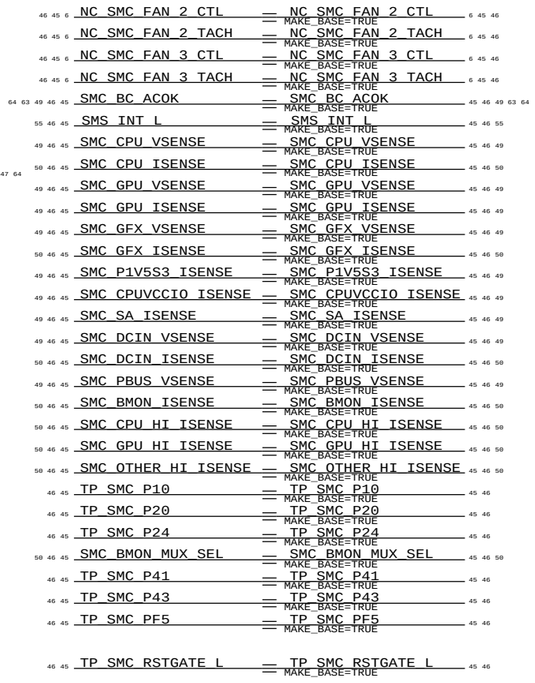


SMC Crystal Circuit

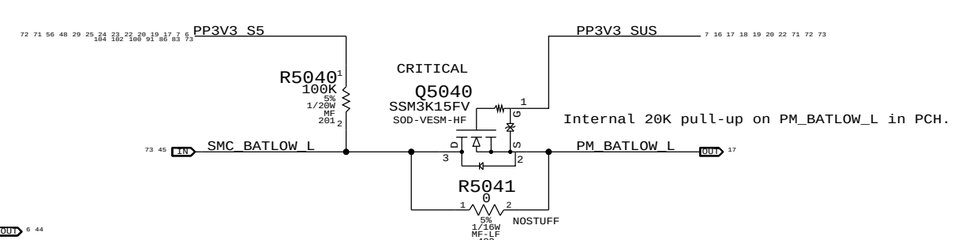


System (Sleep) LED Circuit

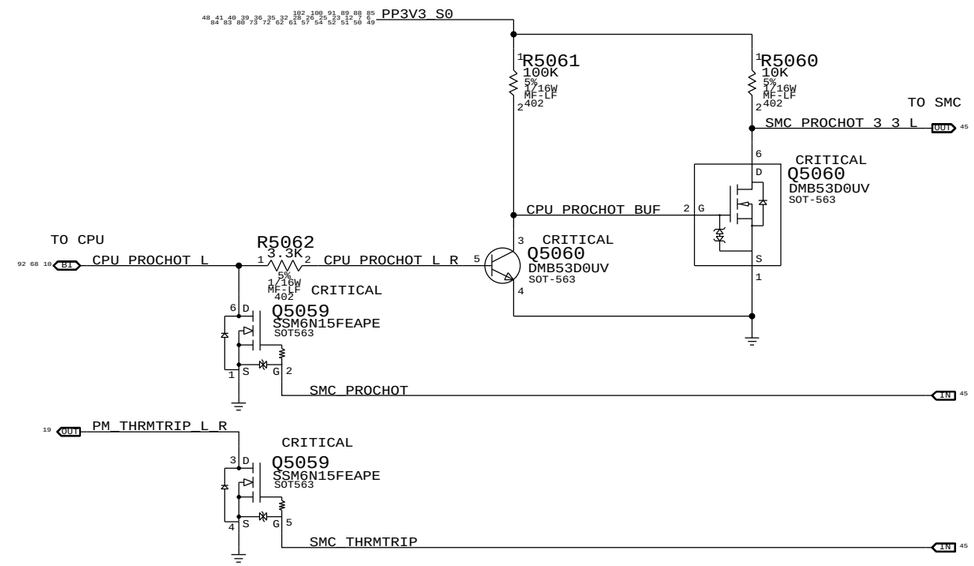


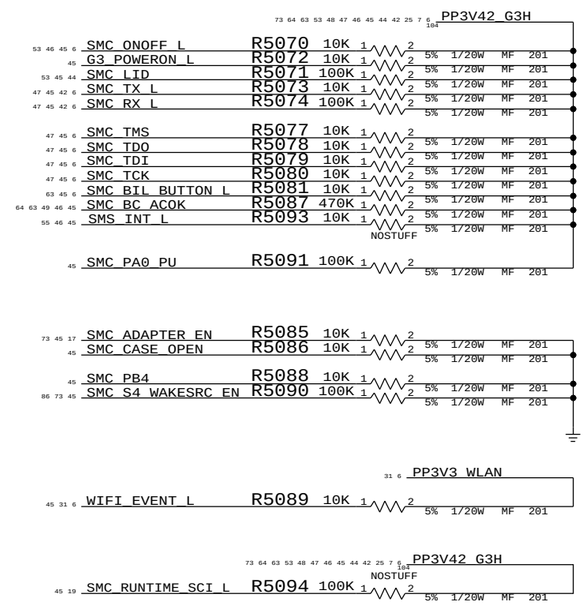


BATLOW# Isolation



SMC FSB to 3.3V Level Shifting





SYNC MASTER=K91_BEN	SYNC DATE=07/12/2010
PAGE TITLE: SMC Support	
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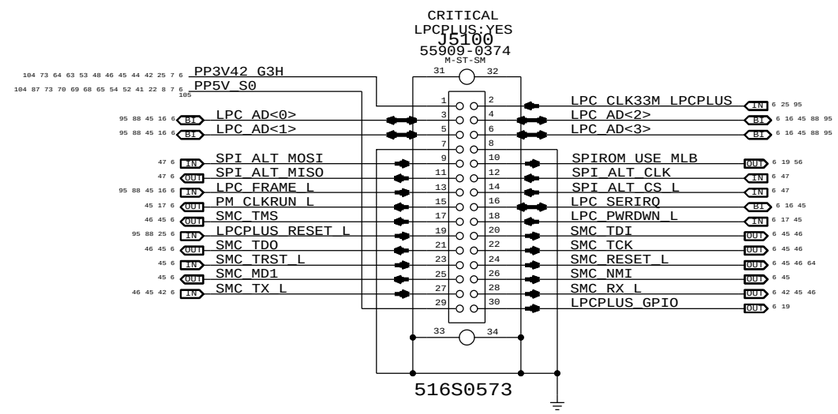
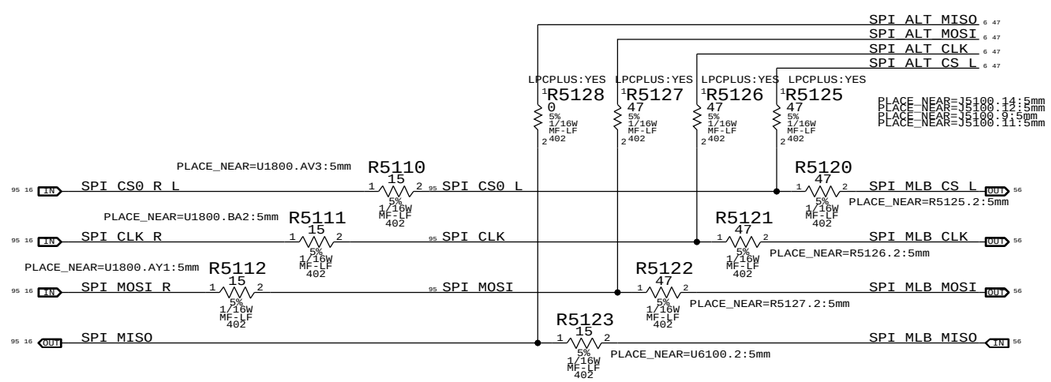
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K91_YUN SYNC_DATE=09/23/2010

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

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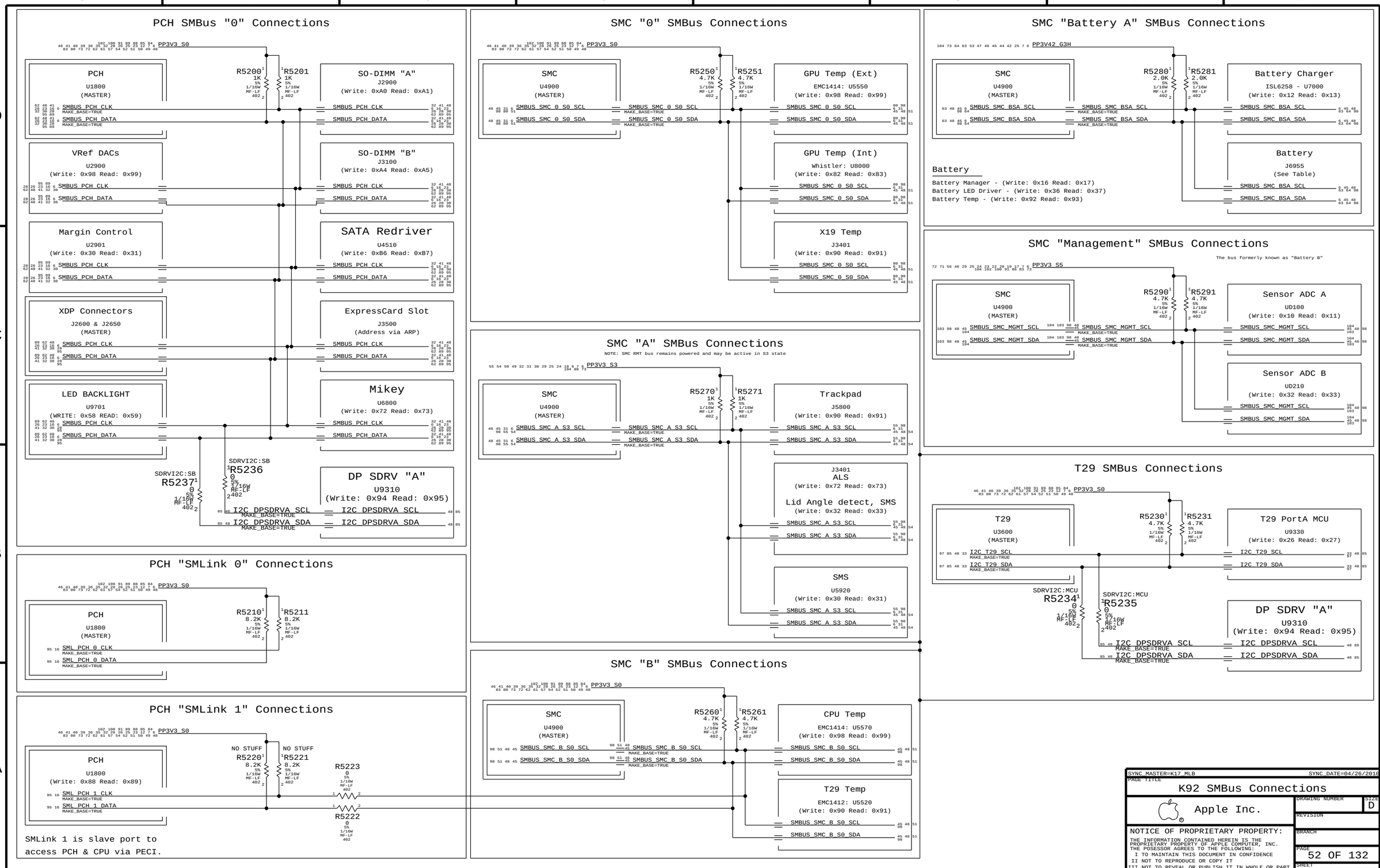

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE

K92 SMBus Connections

Apple Inc.

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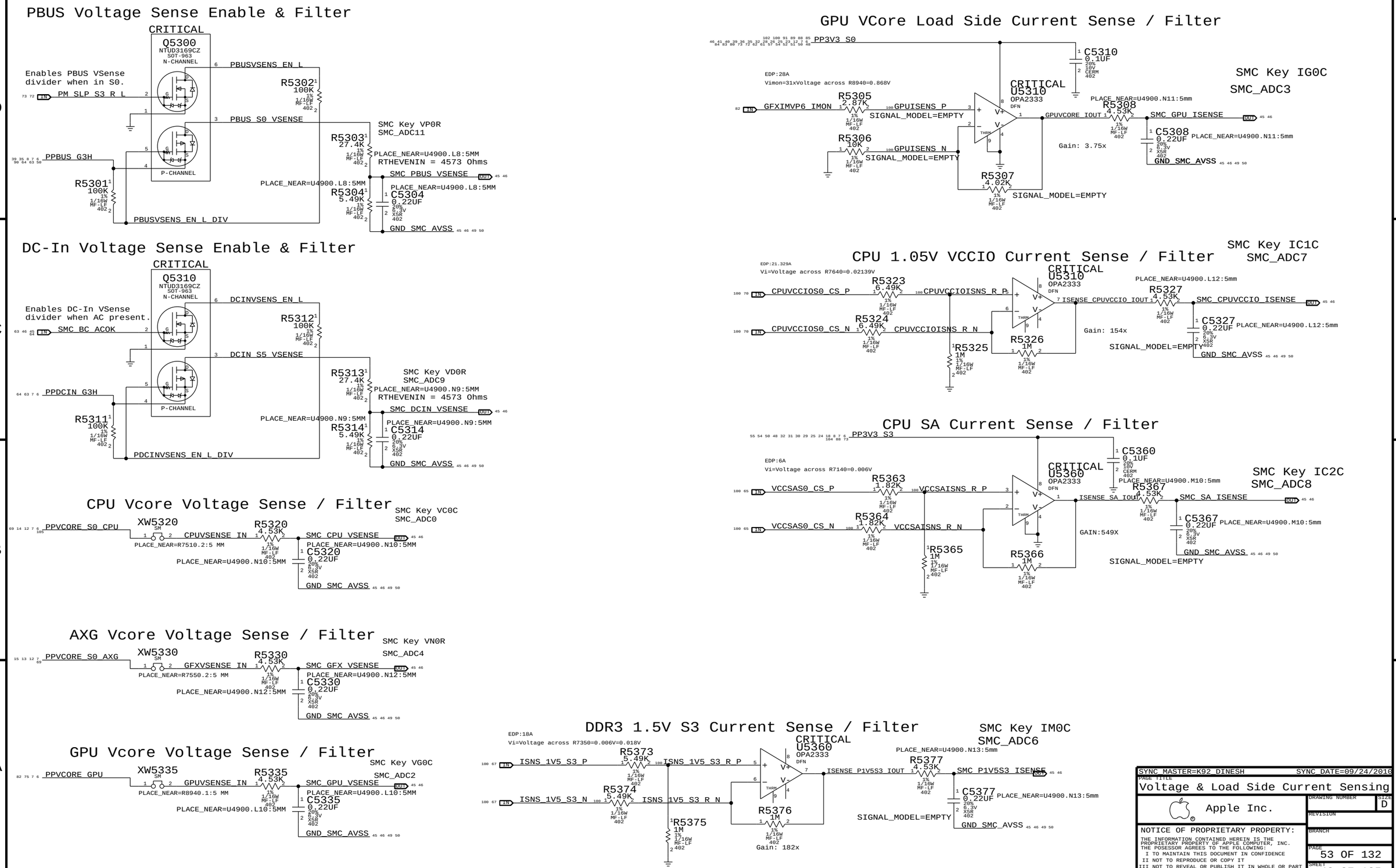

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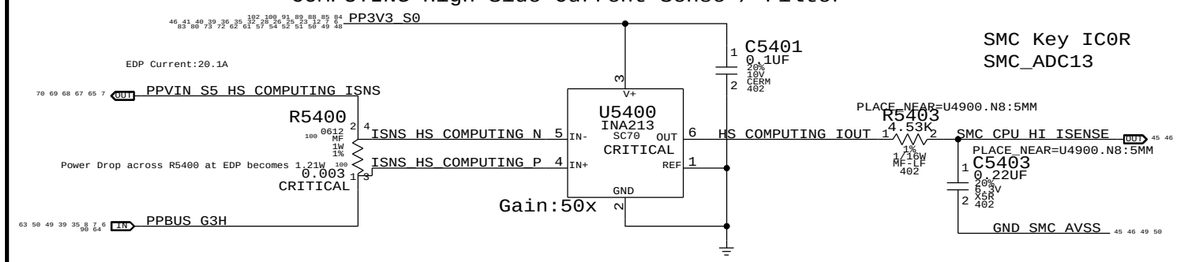
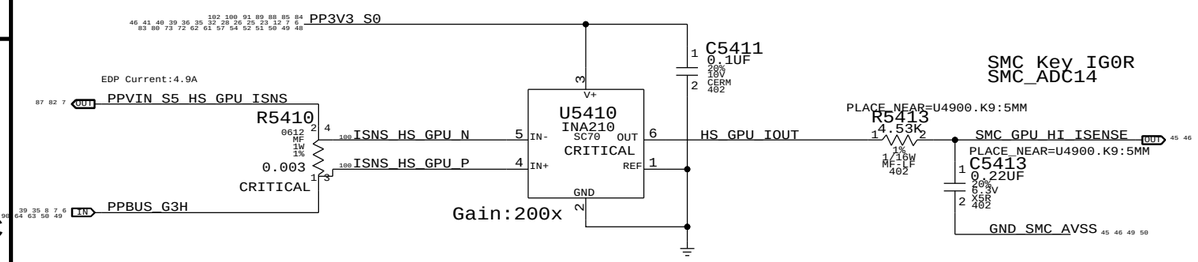
Rsense value and INA gain need to be scrubbed!!

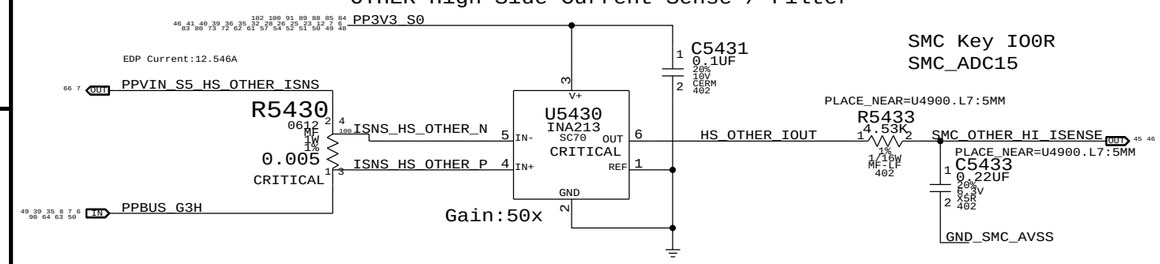
COMPUTING High Side Current Sense / Filter



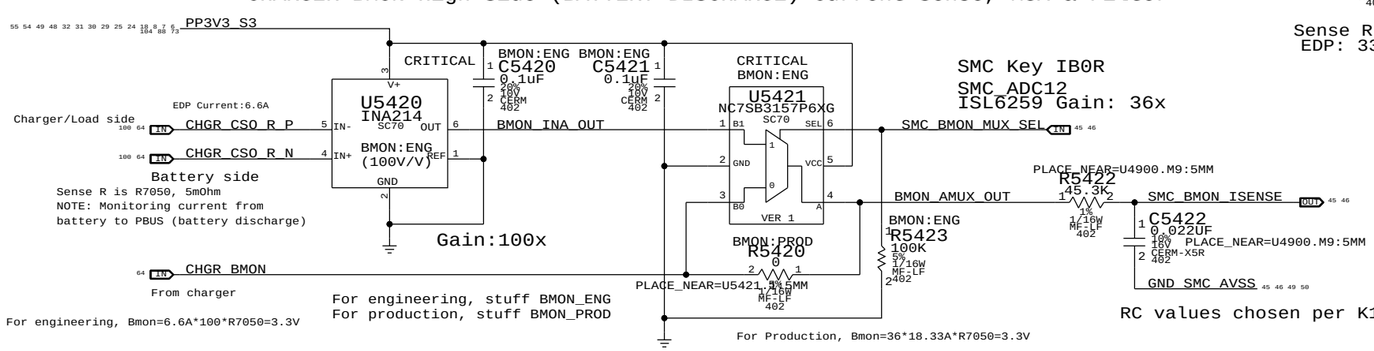
GRAPHICS High Side Current Sense / Filter



OTHER High Side Current Sense / Filter

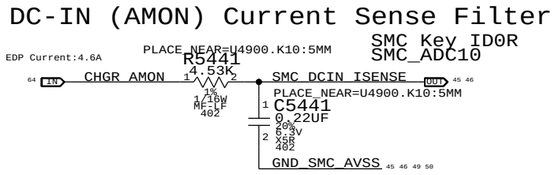


CHARGER BMON High Side (BATTERY DISCHARGE) Current Sense, MUX & Filter

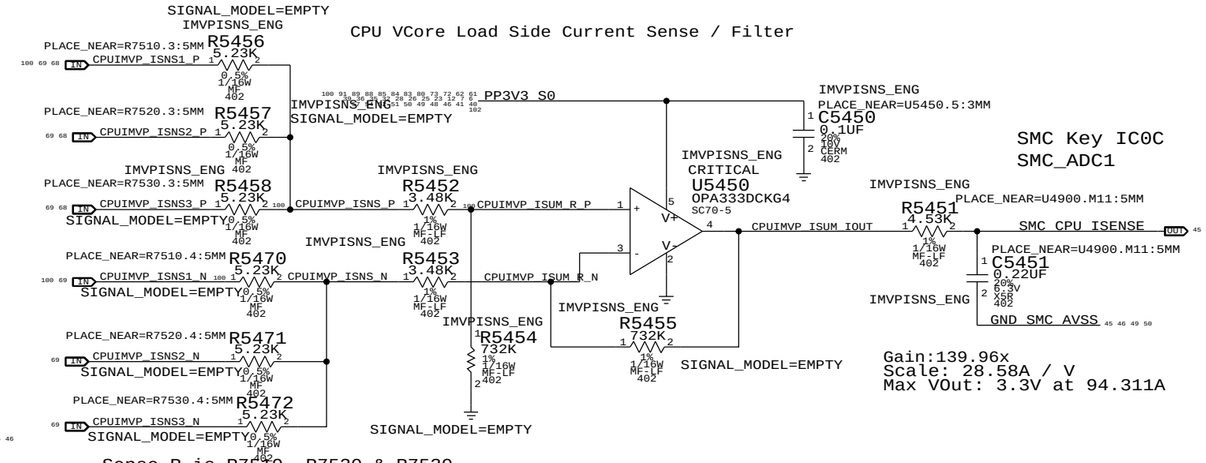


RC values chosen per K17 Radar 7337775

DC-IN (AMON) Current Sense Filter

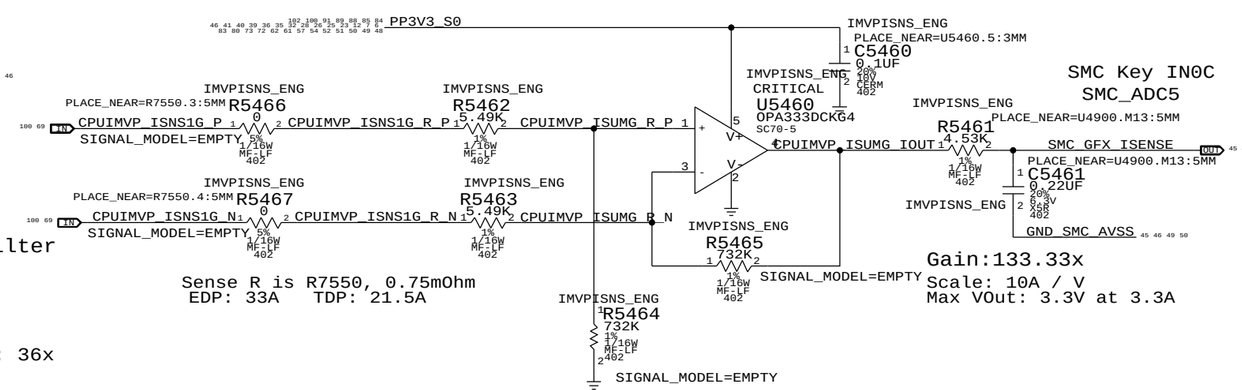


CPU VCore Load Side Current Sense / Filter



Sense R is R7510, R7520 & R7530
Sense R is 0.75mOhm
EDP: 94A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 cores)

GFX/IG VCore Load Side Current Sense / Filter



Sense R is R7550, 0.75mOhm
EDP: 33A TDP: 21.5A

SYNC_MASTER=K92_DINESH	SYNC_DATE=10/29/2010
PAGE TITLE: High Side and CPU/AXG Current Sensing	
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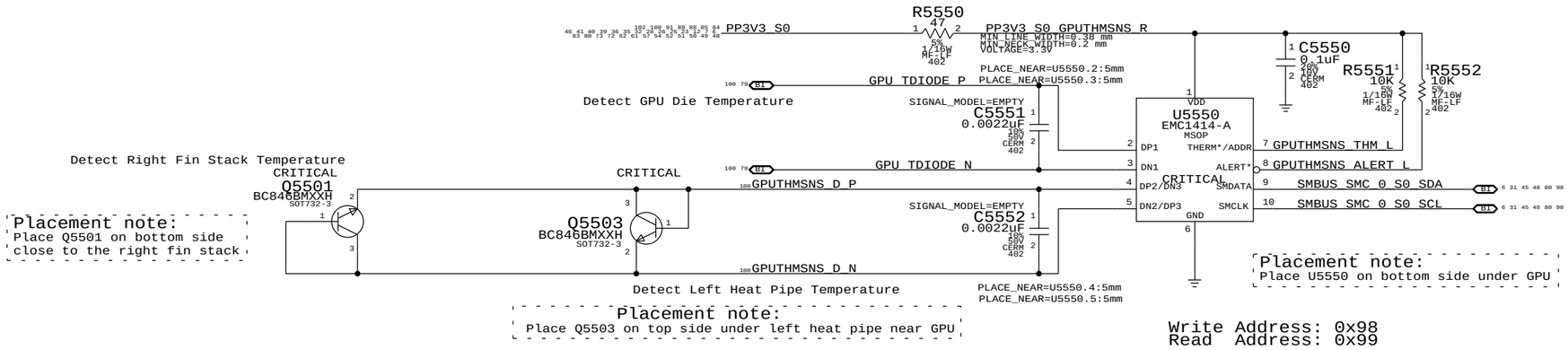
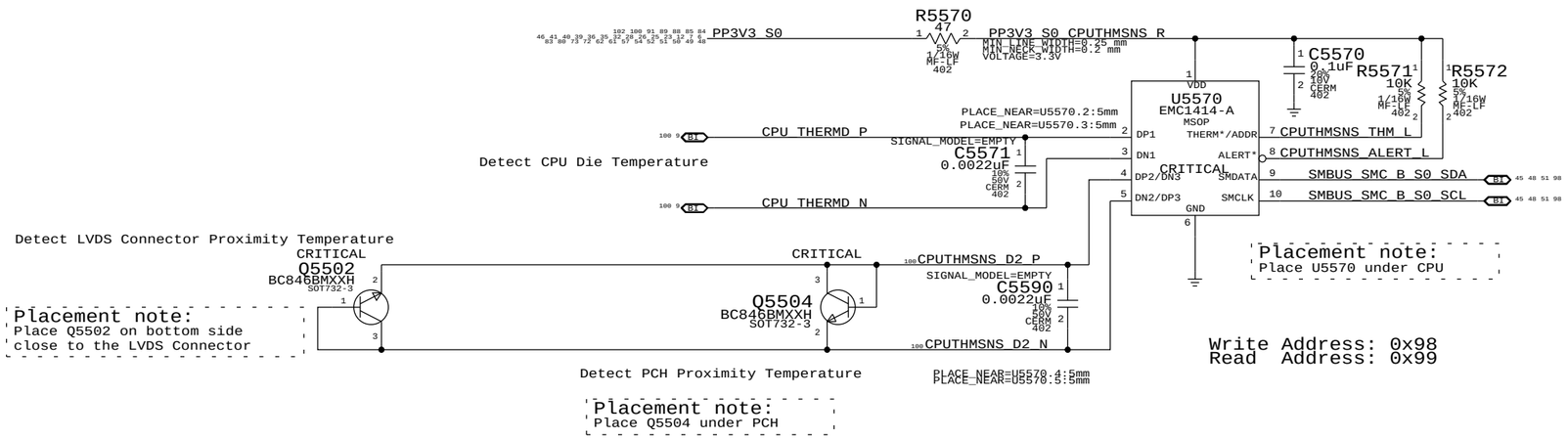
GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack

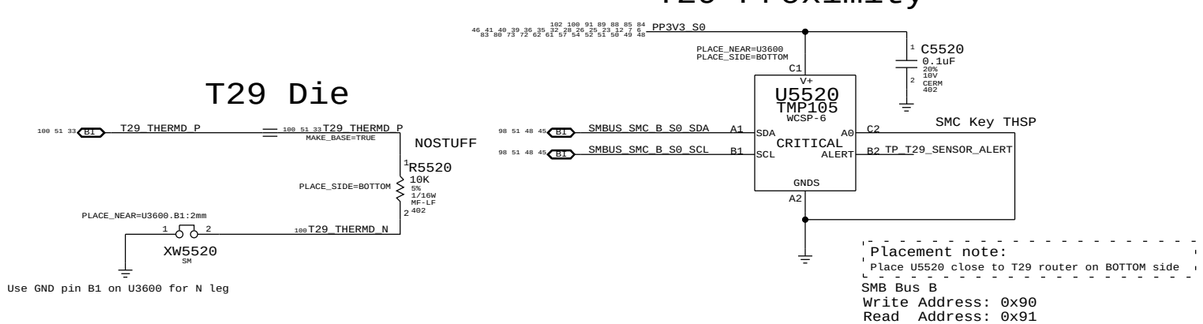


CPU Proximity/CPU Die/PCH Proximity/LVDS Connector Proximity



Note: EMC1414 can perform Beta Compensation for External Diode 1 only

T29 Proximity



T29 Die

SYNC_MASTER=K92_DINESH	SYNC_DATE=09/24/2010
PAGE TITLE: Thermal Sensors	
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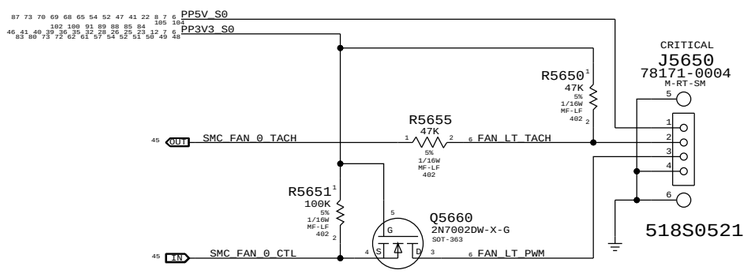
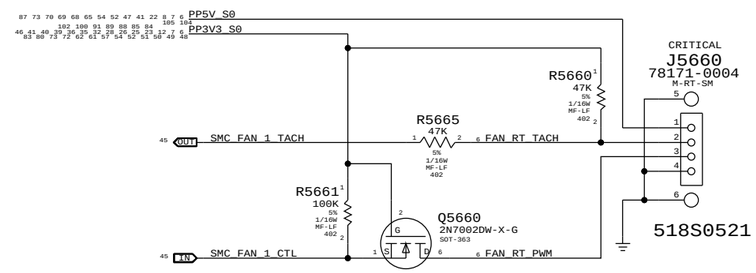
Left Fan



Right Fan



SYNC MASTER=K17 MLB SYNC DATE=04/26/2010

PAGE TITLE

Fan Connectors

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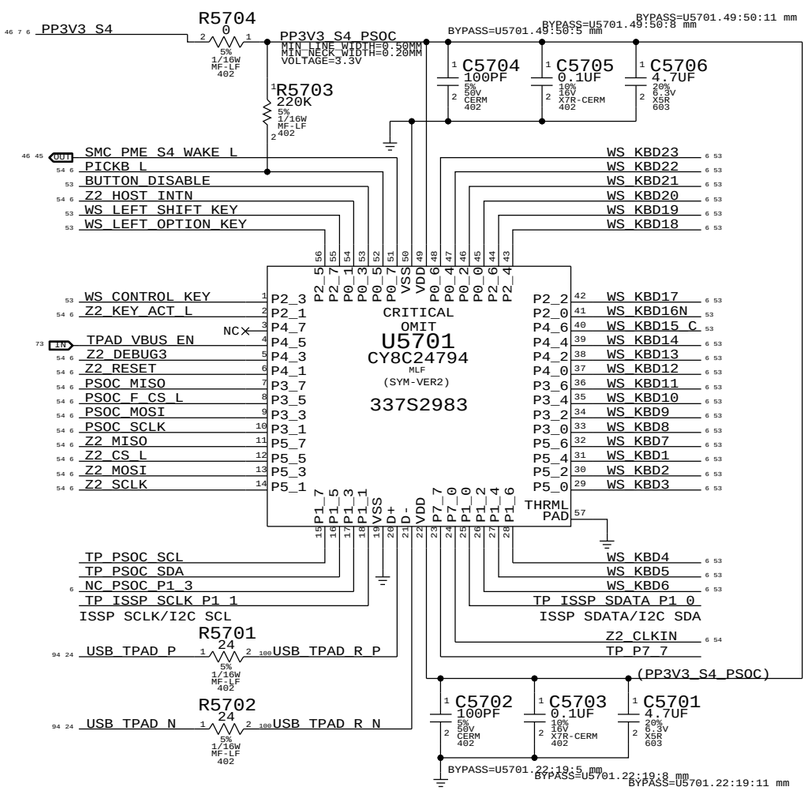
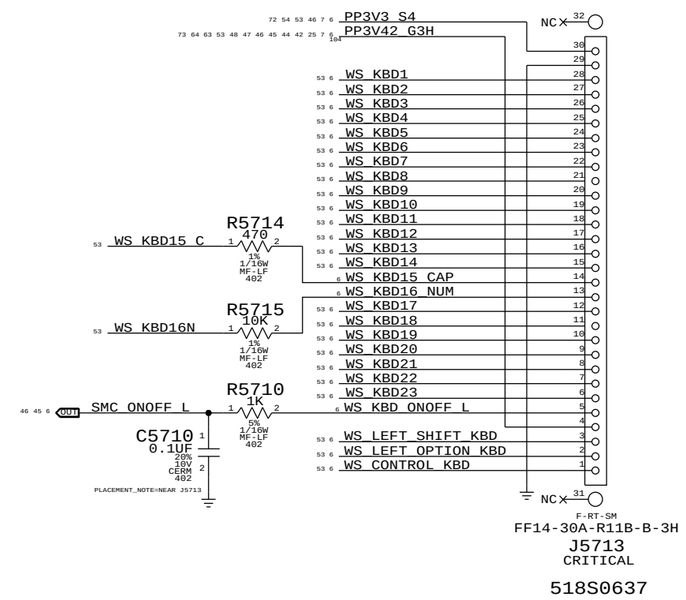
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



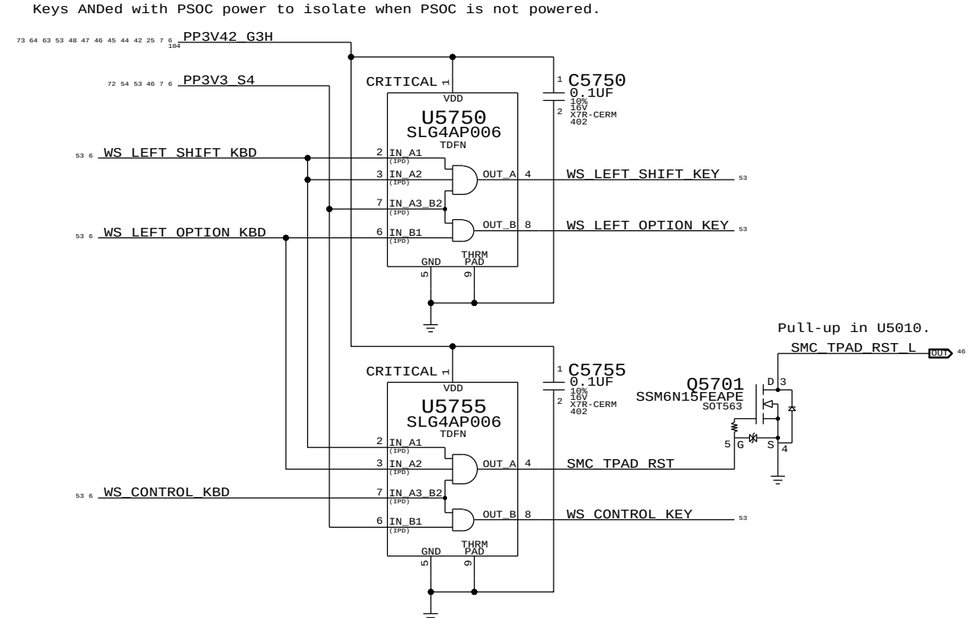
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA 80UA	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60MA (MAX) 60MA (MAX)	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

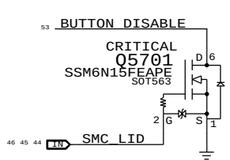


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC MASTER=K92 ERIC SYNC DATE=10/11/2010

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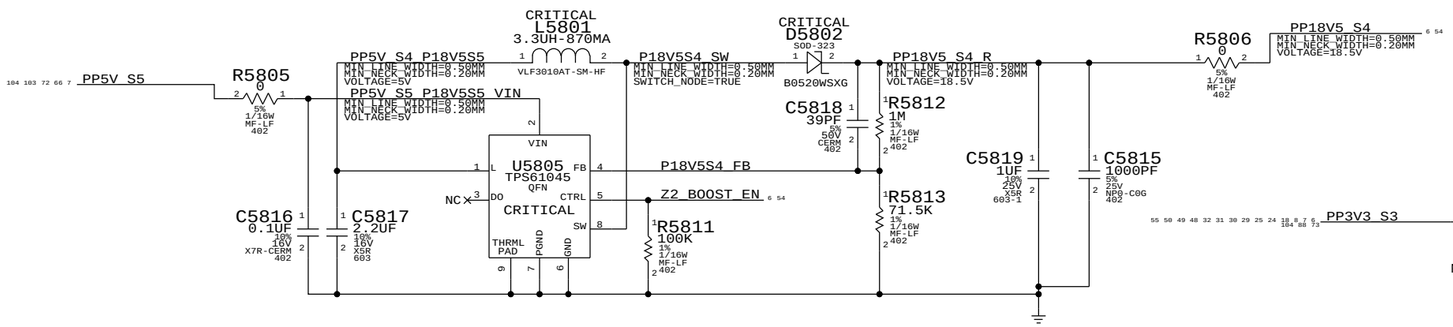
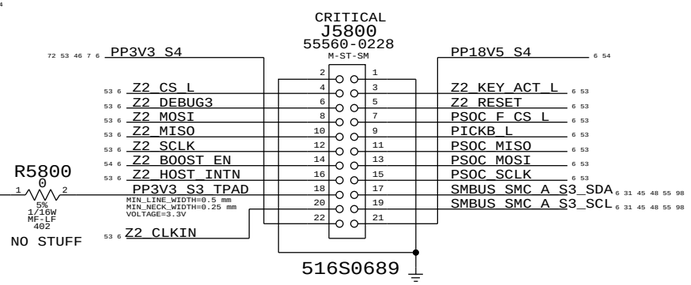
BOOSTER +18.5VDC FOR SENSORS

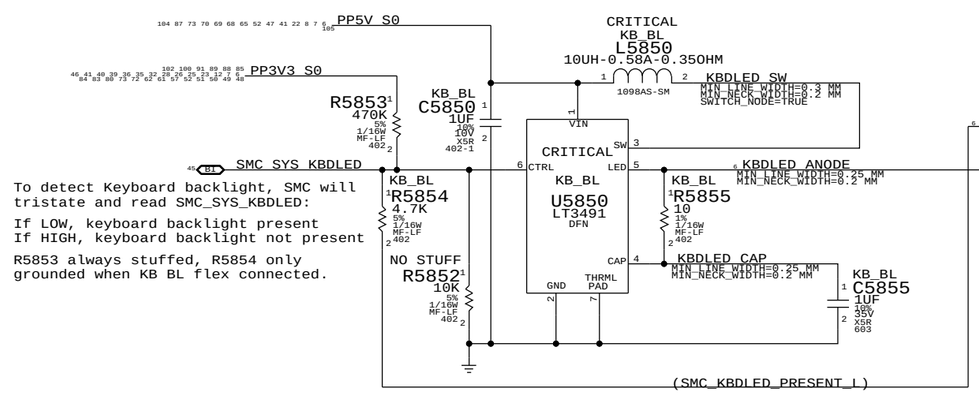
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

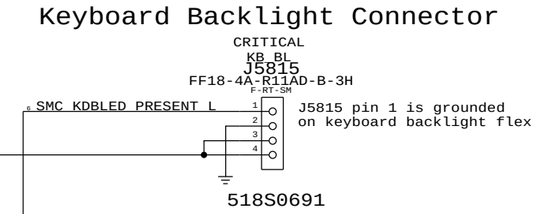


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



J5815 pin 1 is grounded on keyboard backlight flex

SYNC_MASTER=K92_ERIC SYNC_DATE=07/27/2010

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WELLSPRING 2

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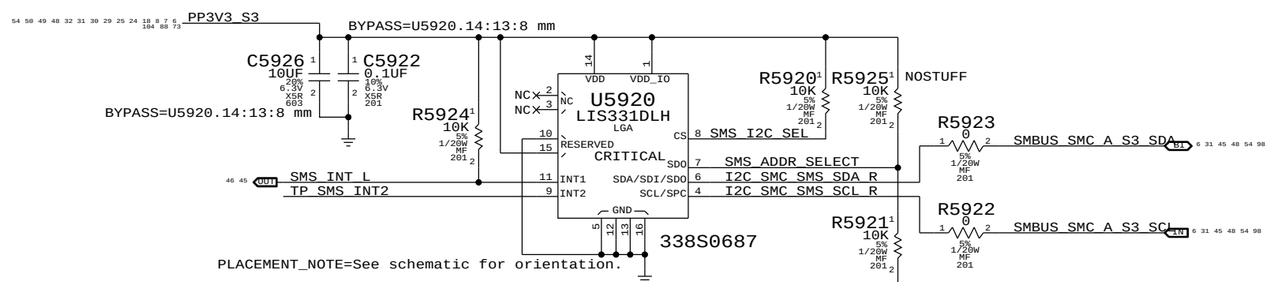
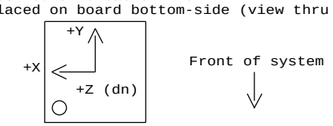


SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

NOTE: SDA and SCL have internal pull-ups to VDD_IO.

Desired orientation when
placed on board bottom-side (view thru top):



Circle indicates pin 1 location when placed
in correct orientation

SYNC MASTER=K92 DINESH SYNC DATE=06/02/2010

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Digital Accelerometer

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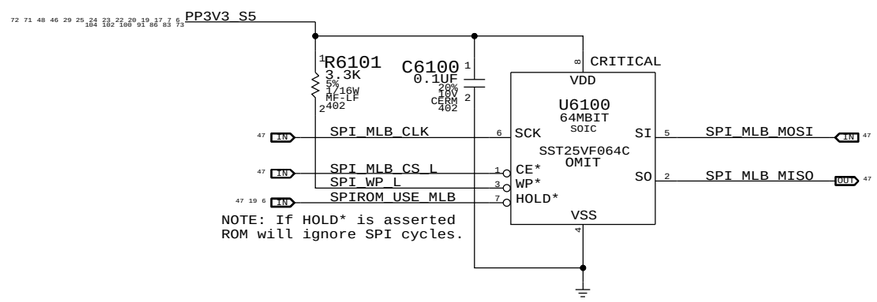

SYNC MASTER=K92 BEN SYNC DATE=05/27/2010

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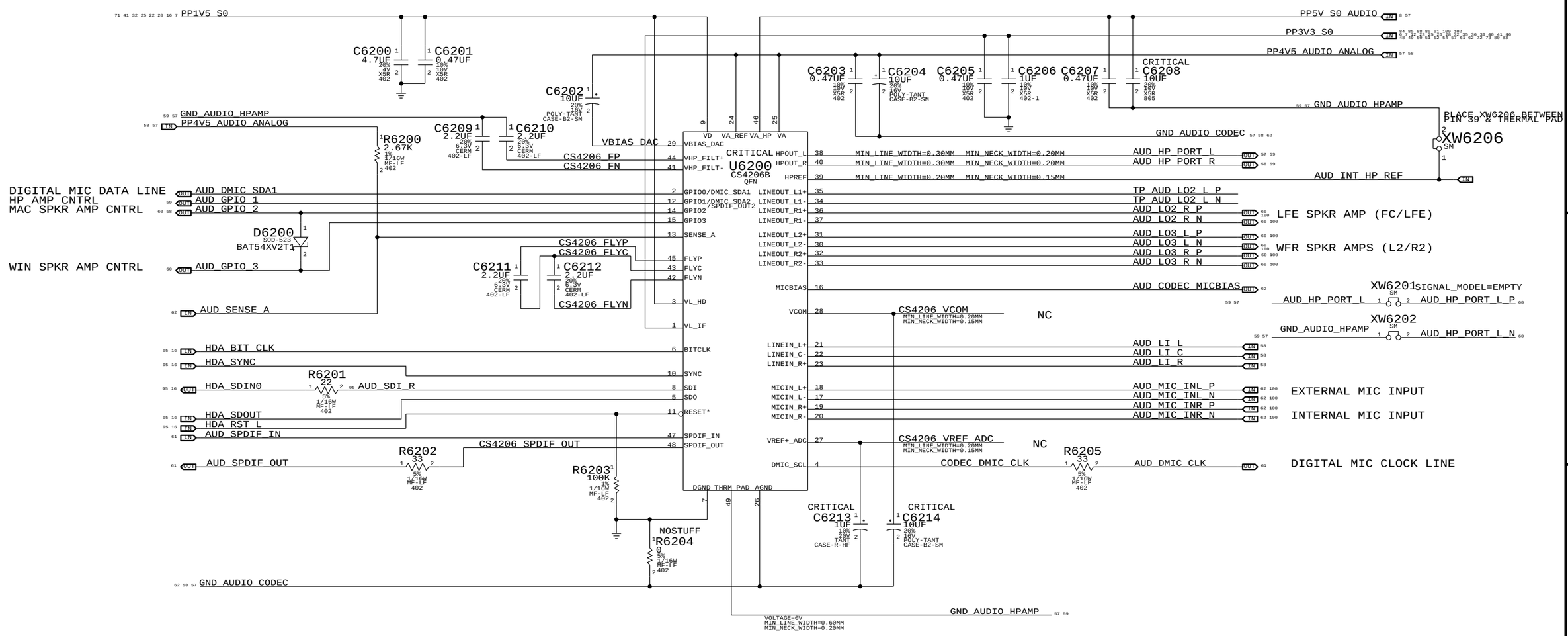
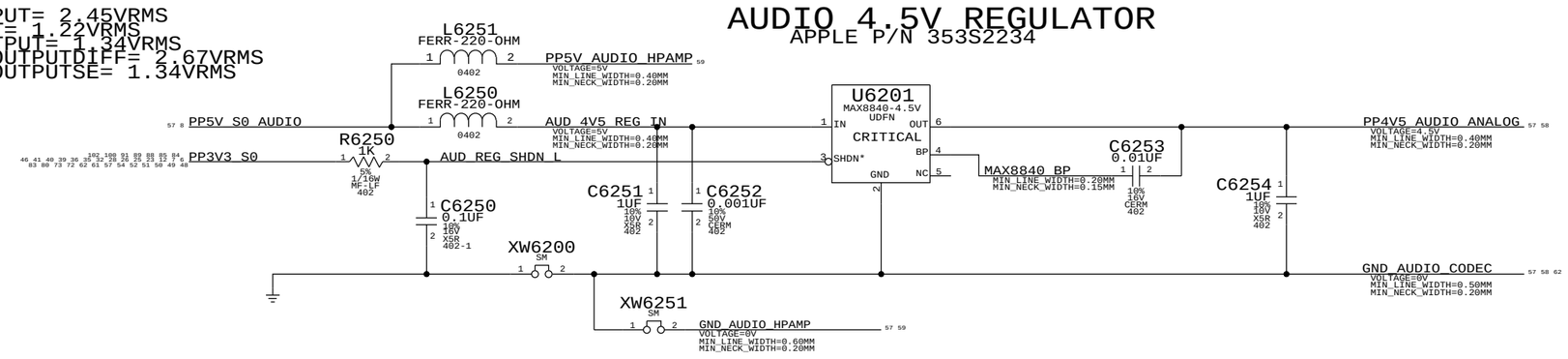
AUDIO CODEC
APPLE P/N 353S3199



DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

AUDIO 4.5V REGULATOR
APPLE P/N 353S2234



SYNC_MASTER=K92_KAVITHA SYNC_DATE=07/30/2010

PAGE TITLE
AUDIO:CODEC

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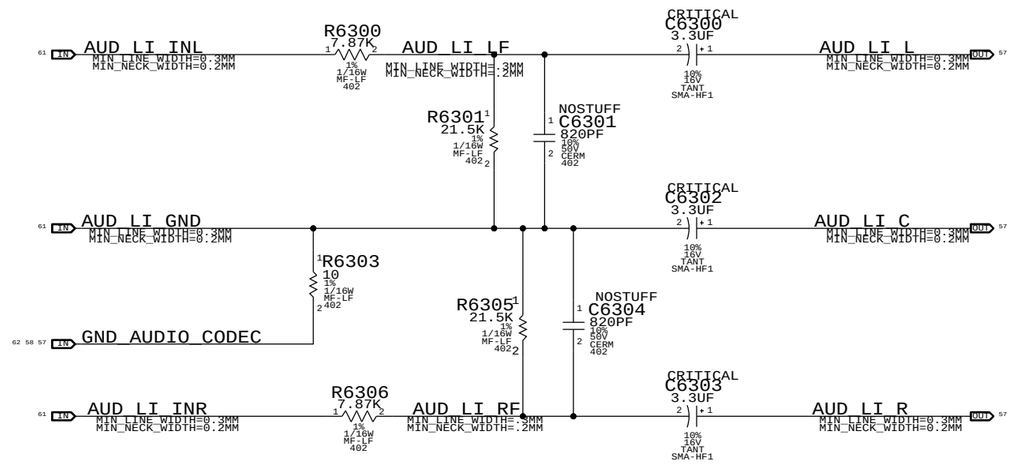
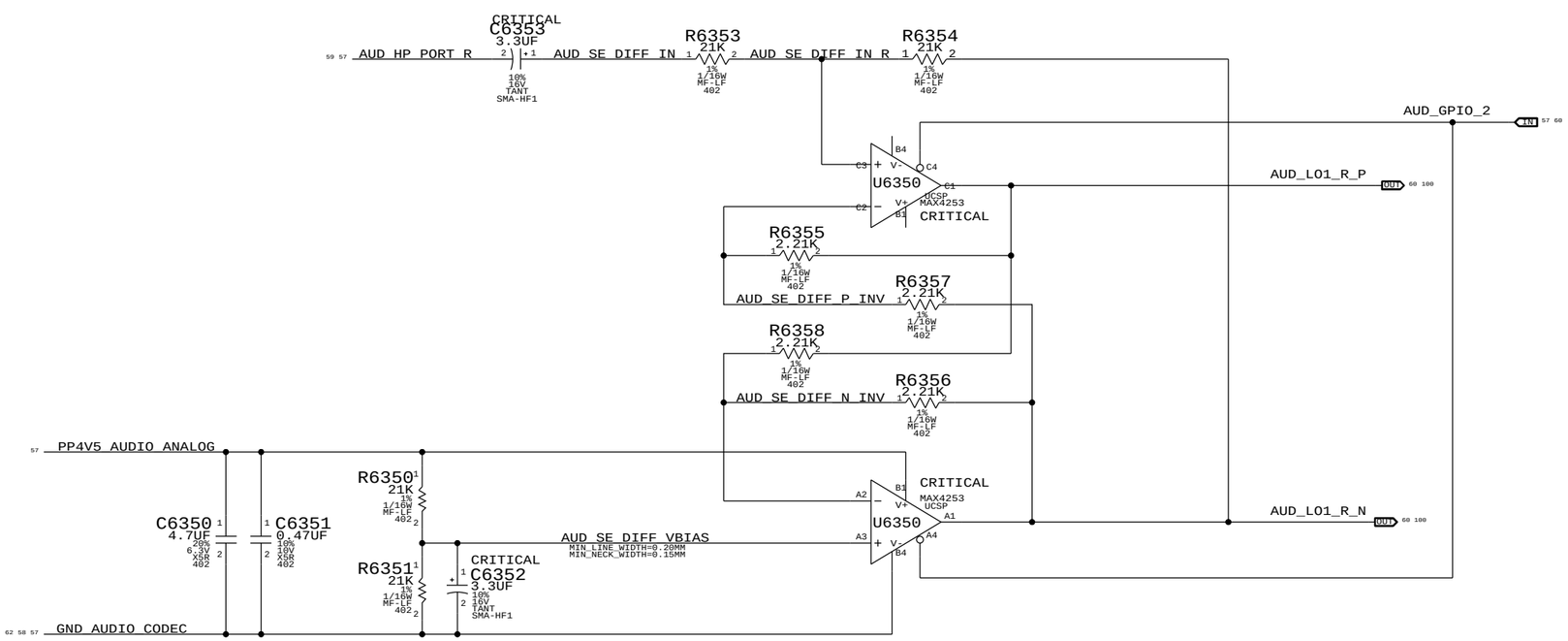
CODEC Nom SE RIN = 20K OHMS
FC = 5 HZ Max
VIN = 2VRMS CODEC VIN = 1.14 VRMS
NET RIN = 18K OHMS



SE-TO-DIFF CONVERTER



SYNC MASTER=K92_AUDIO SYNC DATE=06/16/2010

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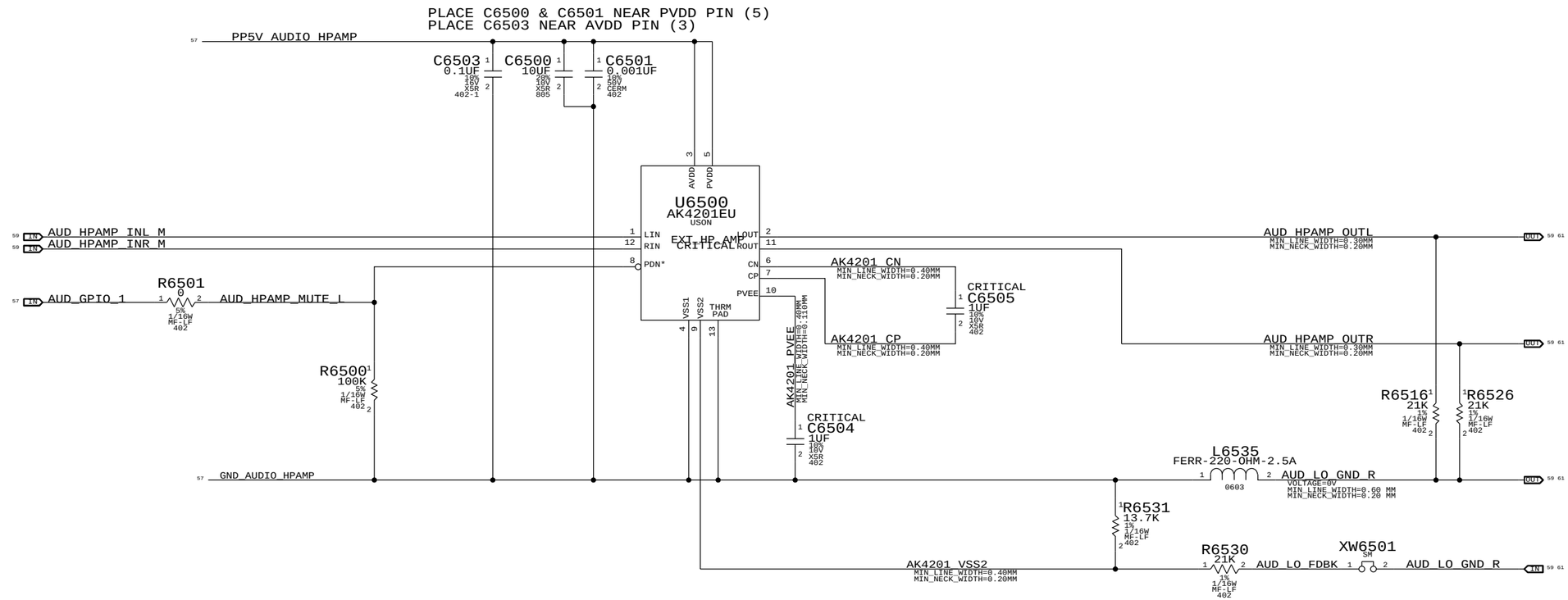
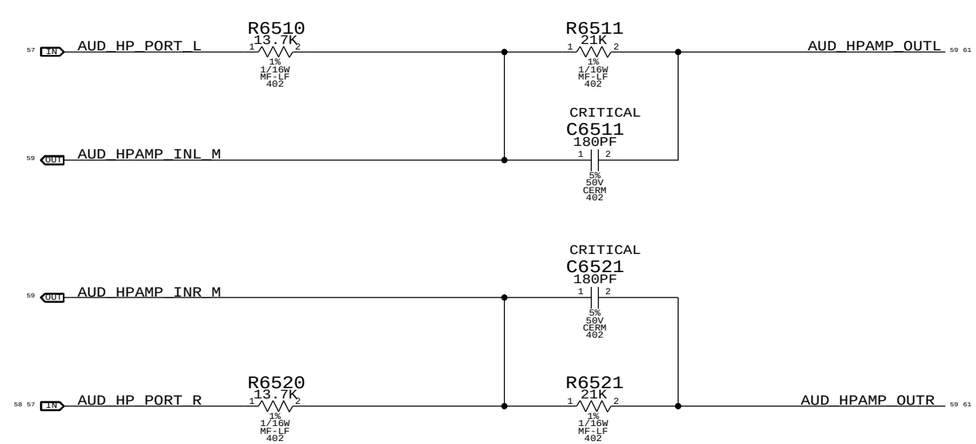
HEADPHONE AMPLIFIER (AK4201)
APN:353S2347
VOLTAGE GAIN:1.53



1ST ORDER DAC FILTER
LP:42.10 KHZ



SYNC_MASTER=K92_KAVITHA SYNC_DATE=10/22/2010

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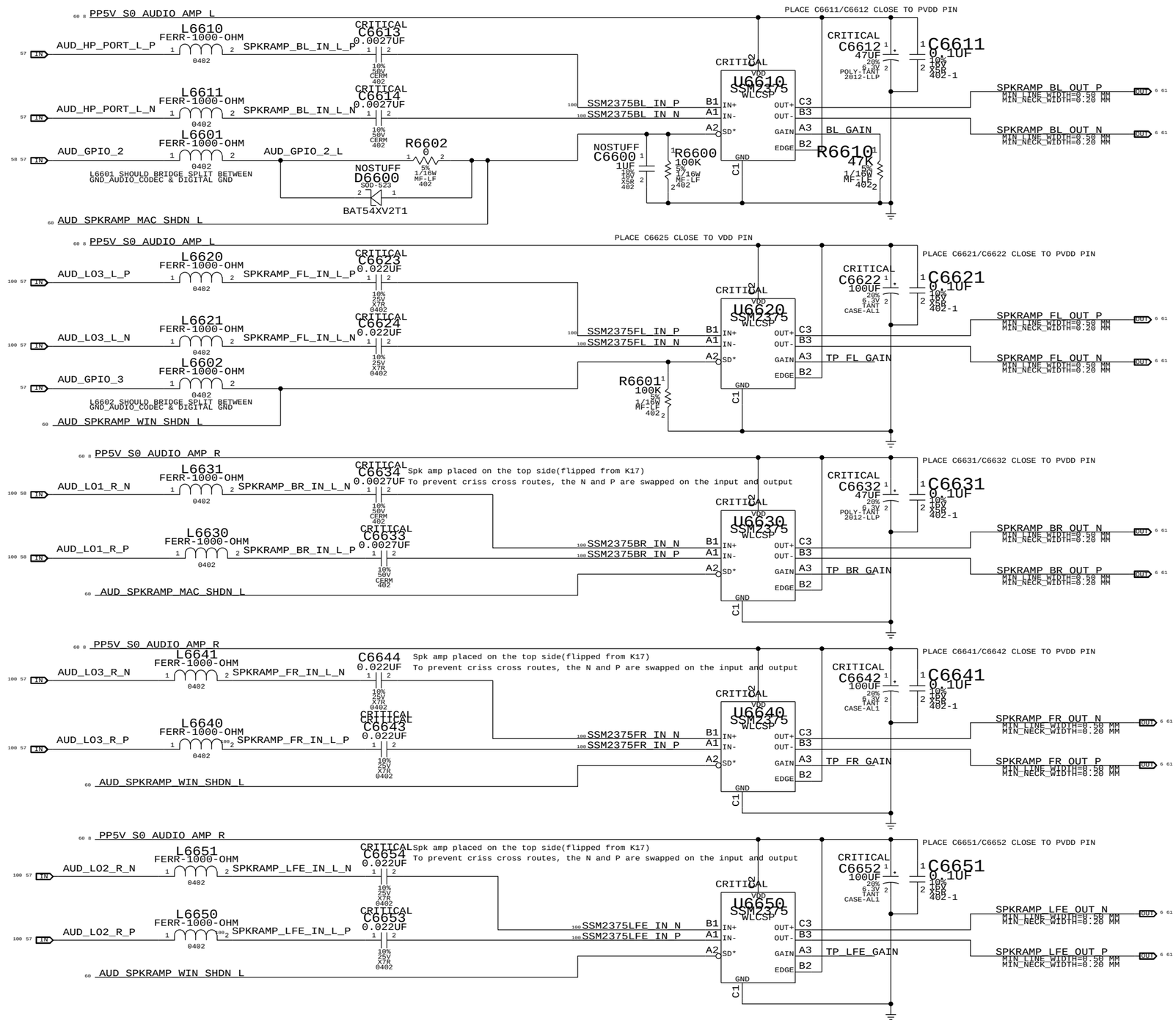
5X MONO SPEAKER AMPLIFIERS (SSM2375)
APN: 353S2958
GAIN = +3 DB (BR, FL, FR, LFE), +9 DB (BL)
FC (SPEAKERS BL/BR) = ~737 HZ
FC (SPEAKERS FL/FR/LFE) = ~90 HZ



SYNC MASTER=K92 KAVITHA SYNC DATE=10/22/2010

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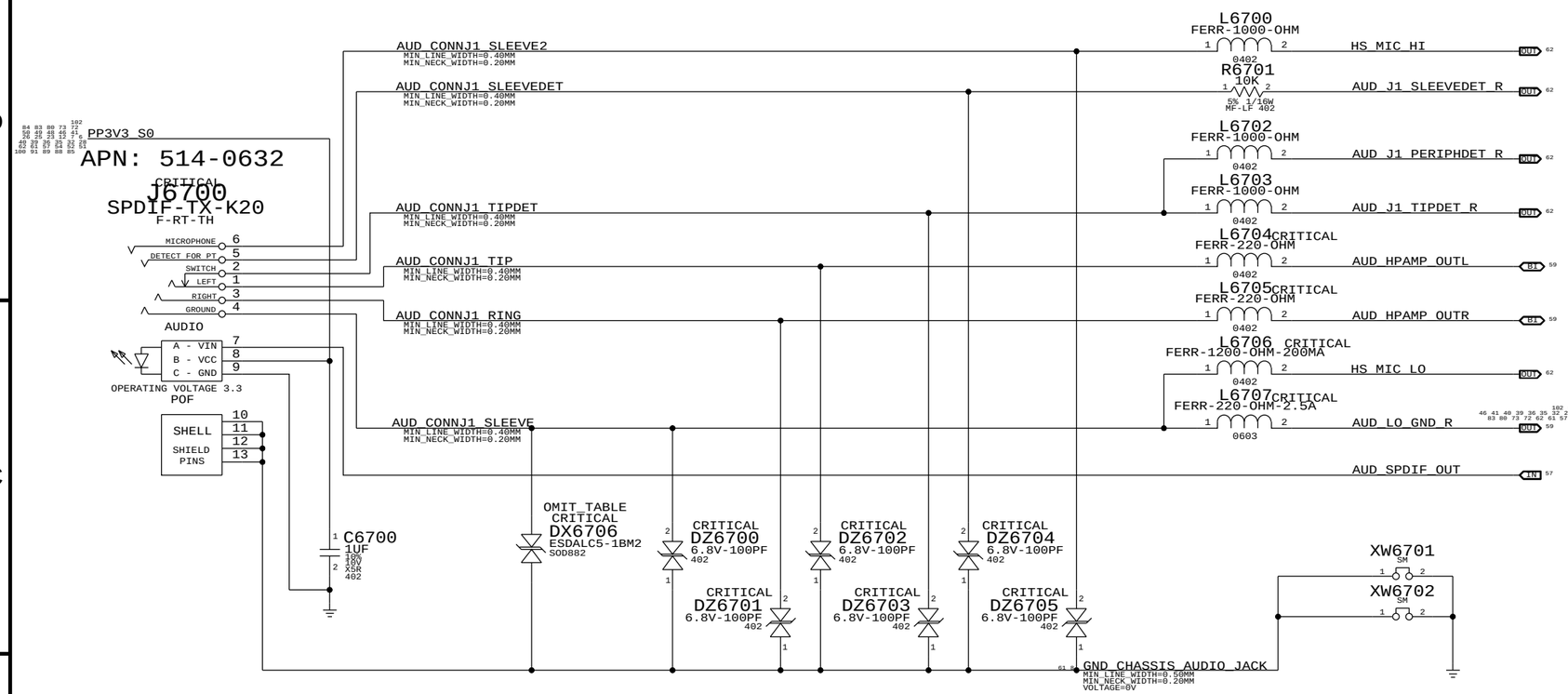
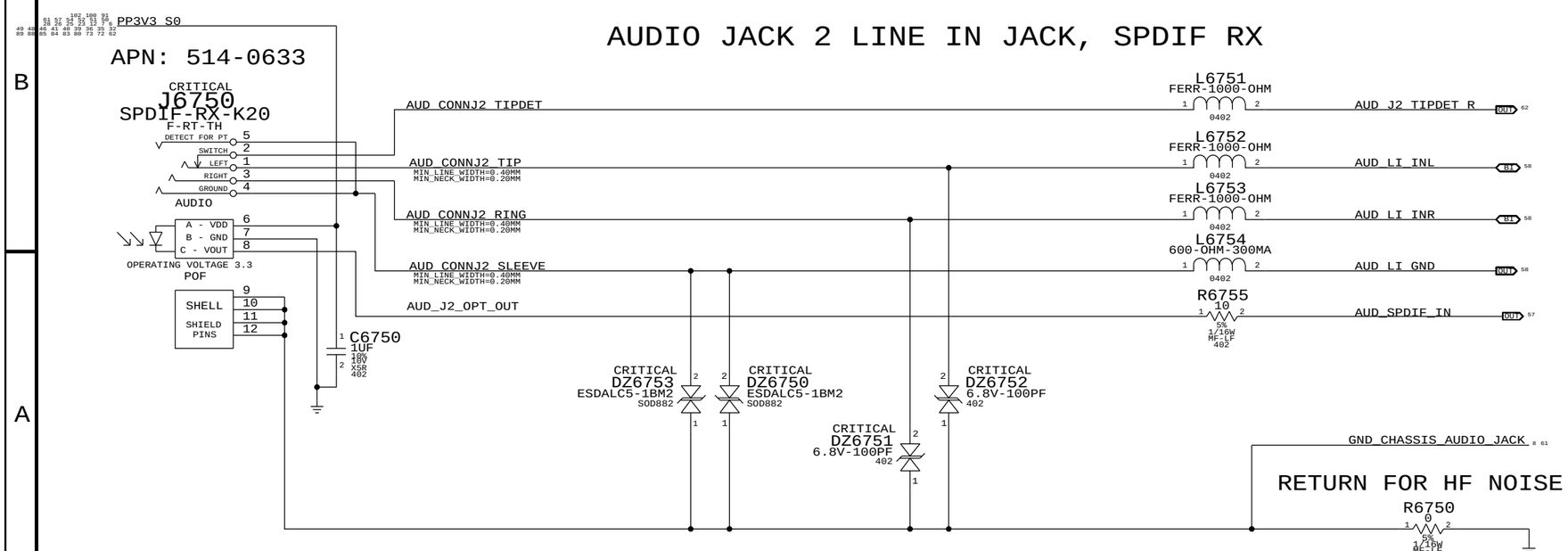
AUDIO JACK 1 LO/HP JACK, SPDIF TX

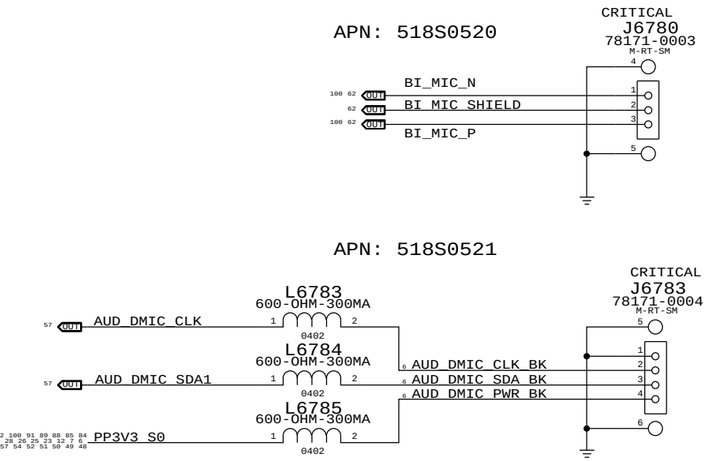


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
377S0112	1	EMC supressor	DX6706		

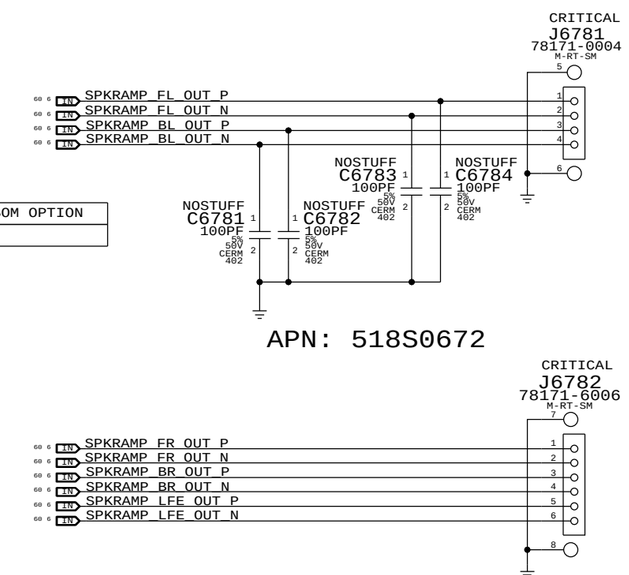
AUDIO JACK 2 LINE IN JACK, SPDIF RX



MIC CONNECTORS: single anlg mic + 1 dig mic



SPEAKER CONNECTORS
APN: 518S0521



SYNC MASTER=K92 KAVITHA SYNC DATE=11/02/2010

PAGE TITLE: AUDIO: JACKS

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DRAWING NUMBER: SIZE D

REVISION:

BRANCH:

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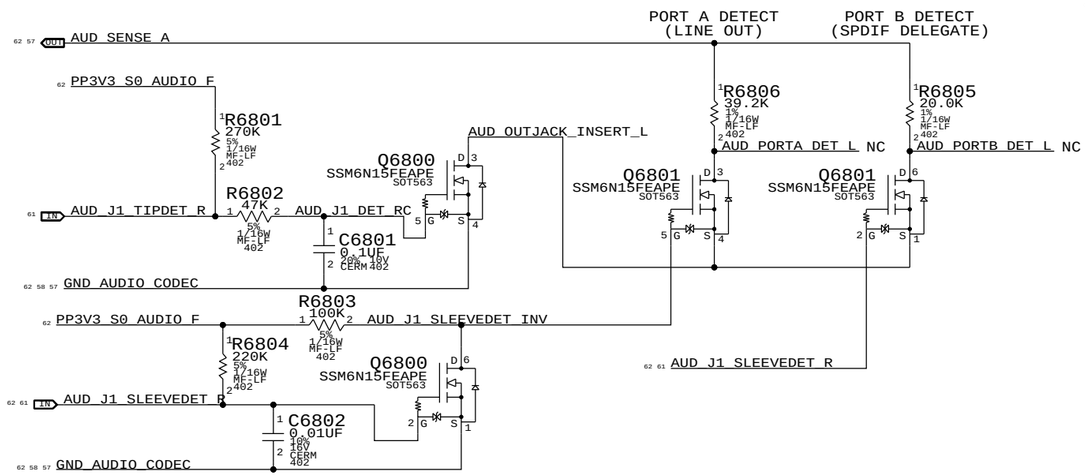
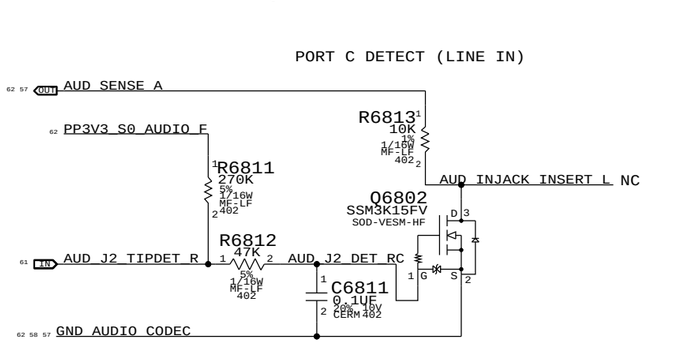
CODEC OUTPUT SIGNAL PATHS

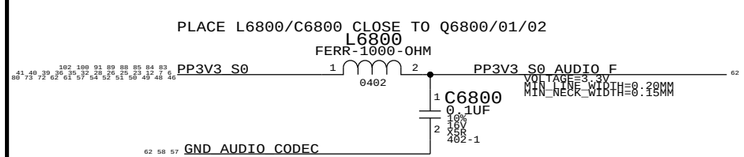
FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC OS SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	N/A	0X09 (A)
SPEAKERS BL/BR	0X02 (2)	0X02 (2)	0X09 (9,V23)	GPIO_2	N/A	N/A
SPEAKERS FL/FR	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_2	GPIO_3	N/A
SPEAKER LFE	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (B)

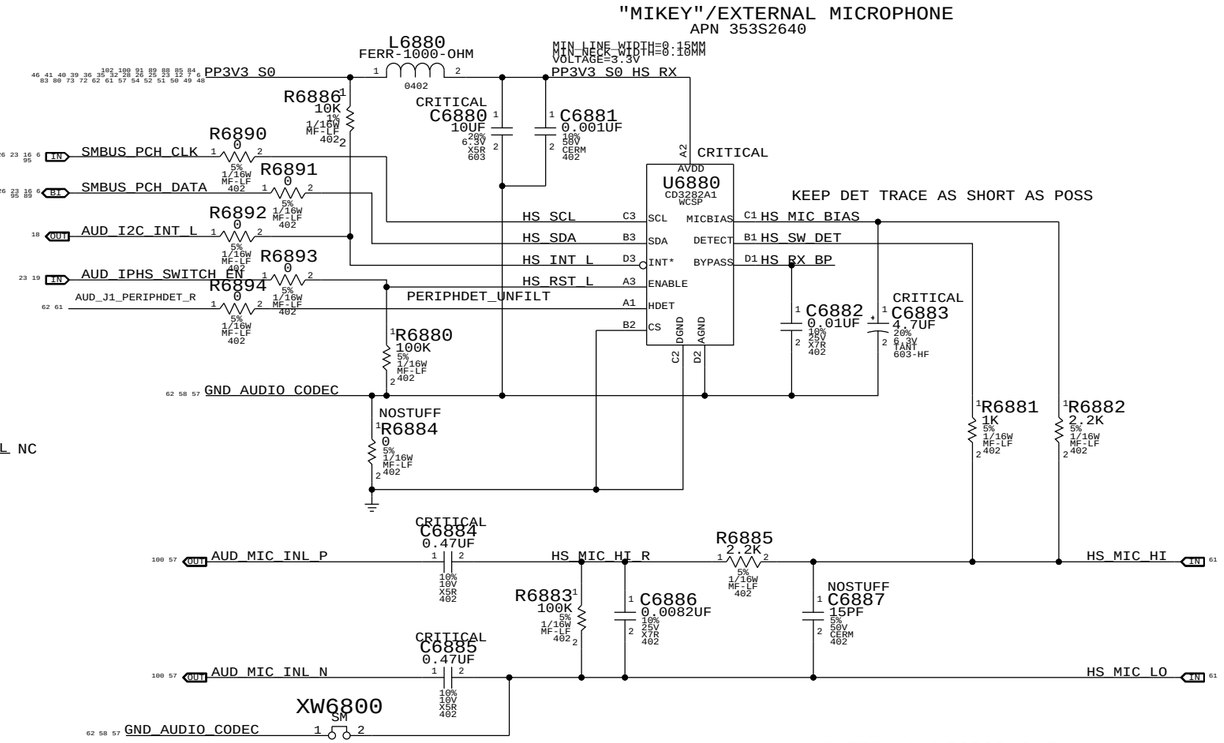
CODEC INPUT SIGNAL PATHS

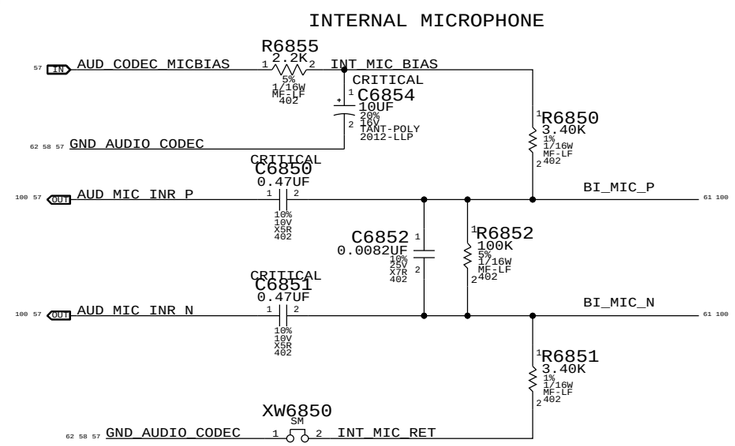
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X12 (12,C)	N/A	0X12 (C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
INTERNAL MIC	0X06 (6)	0X0D (13,B,RIGHT)	MICBIAS (80%)	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

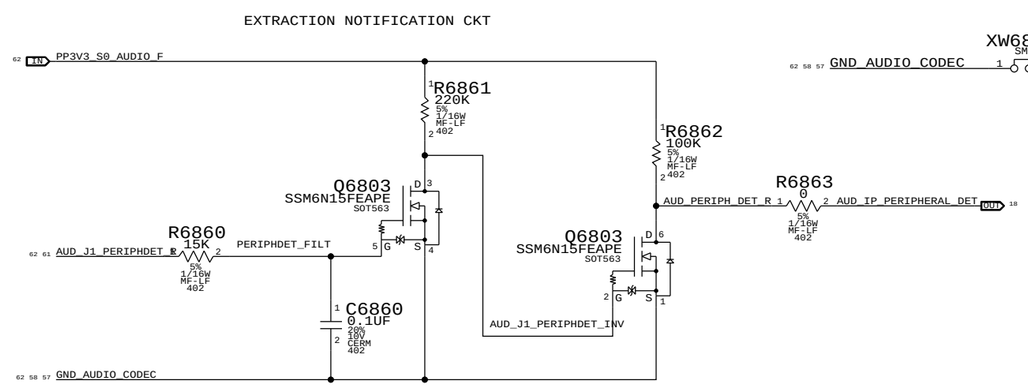












SYNC MASTER=K92 KAVITHA SYNC DATE=11/22/2010

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

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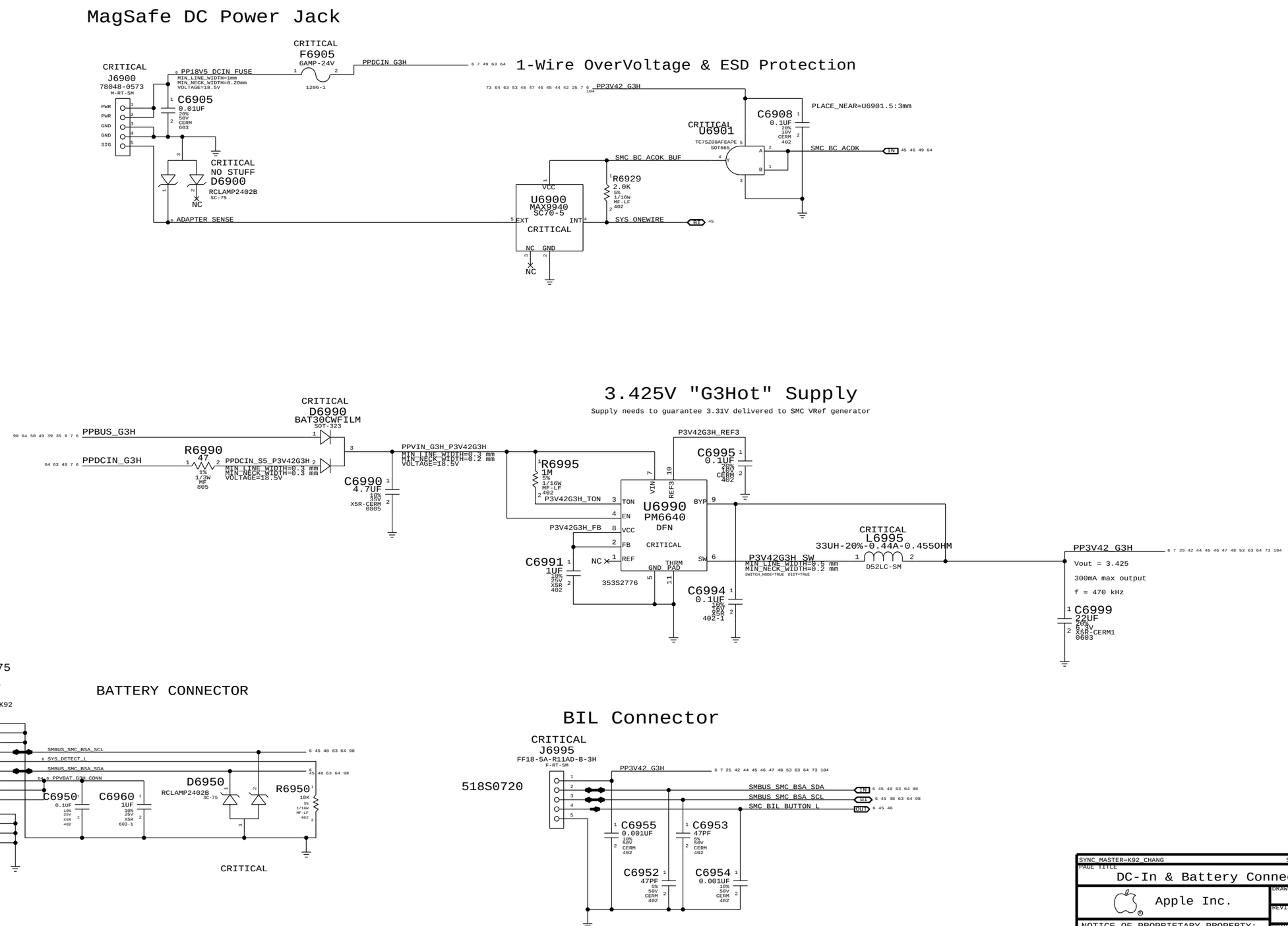

SYNC_MASTER=K92_CHANG SYNC_DATE=06/28/2010

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER
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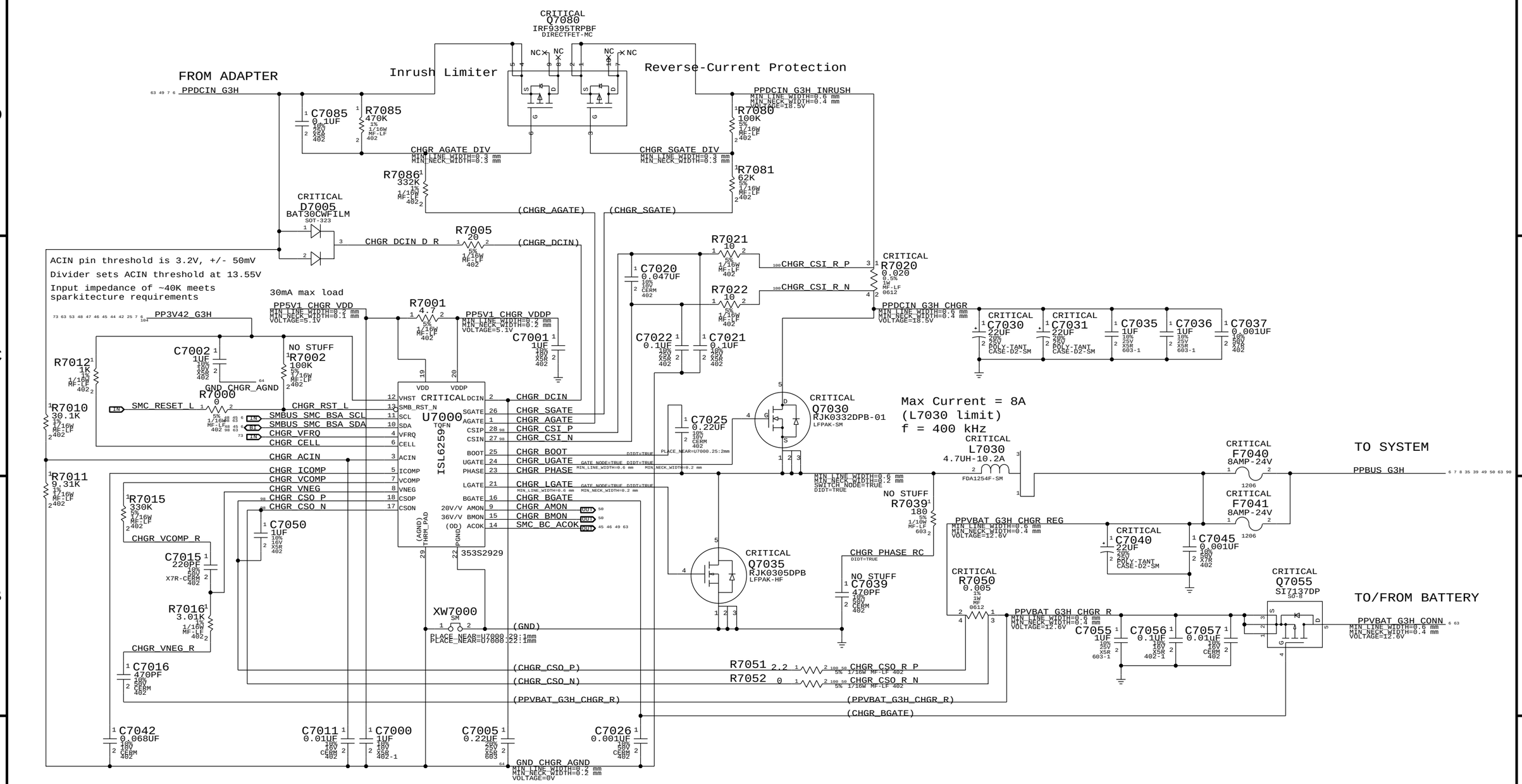

SYNC MASTER=K91 CHANG SYNC DATE=07/21/2010

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

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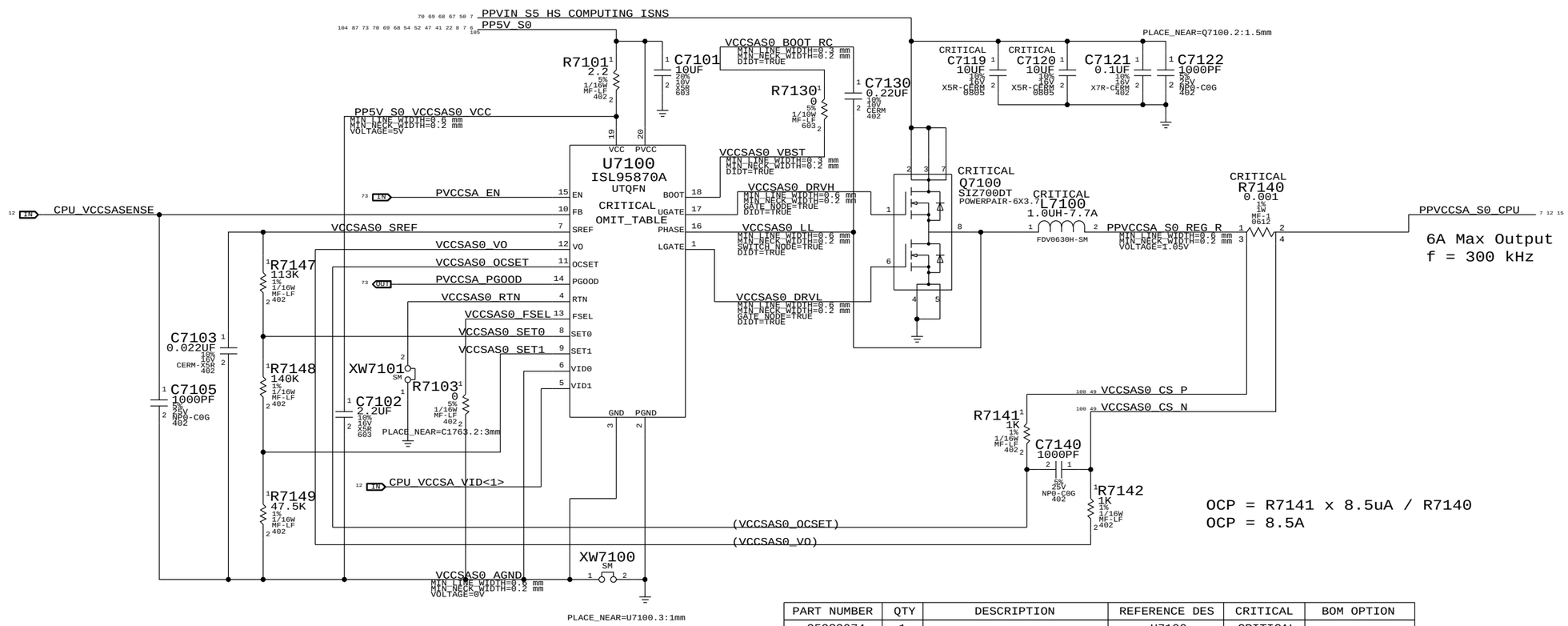

OCP = R7141 x 8.5uA / R7140
OCP = 8.5A

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20P	U7100	CRITICAL	

SYNC MASTER=K91 CHANG SYNC DATE=07/21/2010

PAGE TITLE
System Agent Supply

Apple Inc.

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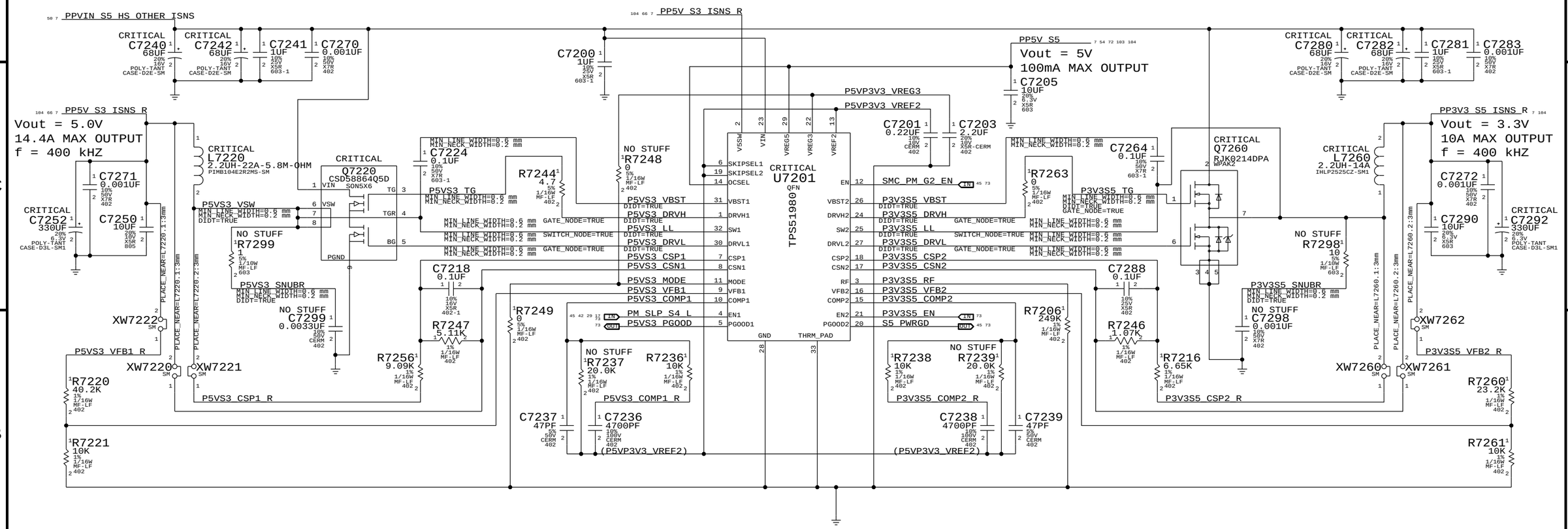

SYNC MASTER=K92_ERIC SYNC DATE=08/30/2010

PAGE TITLE
5V / 3.3V Power Supply

Apple Inc.

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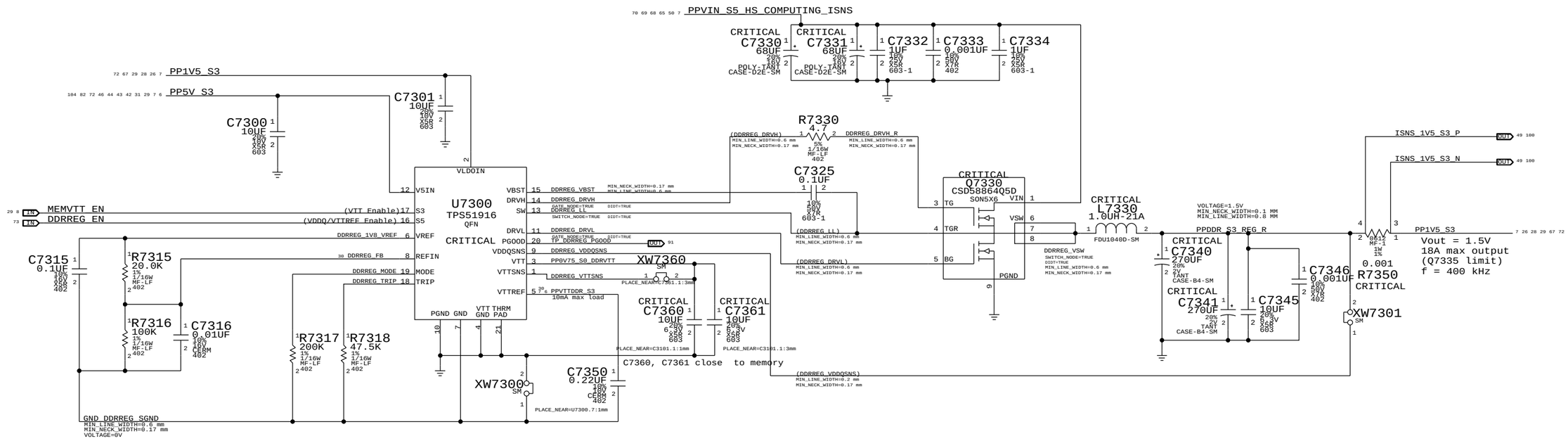

SYNC MASTER=K91_CHANG	SYNC DATE=07/21/2010
PAGE TITLE	1.5V DDR3 Supply
Apple Inc.	DRAWING NUMBER / SIZE D
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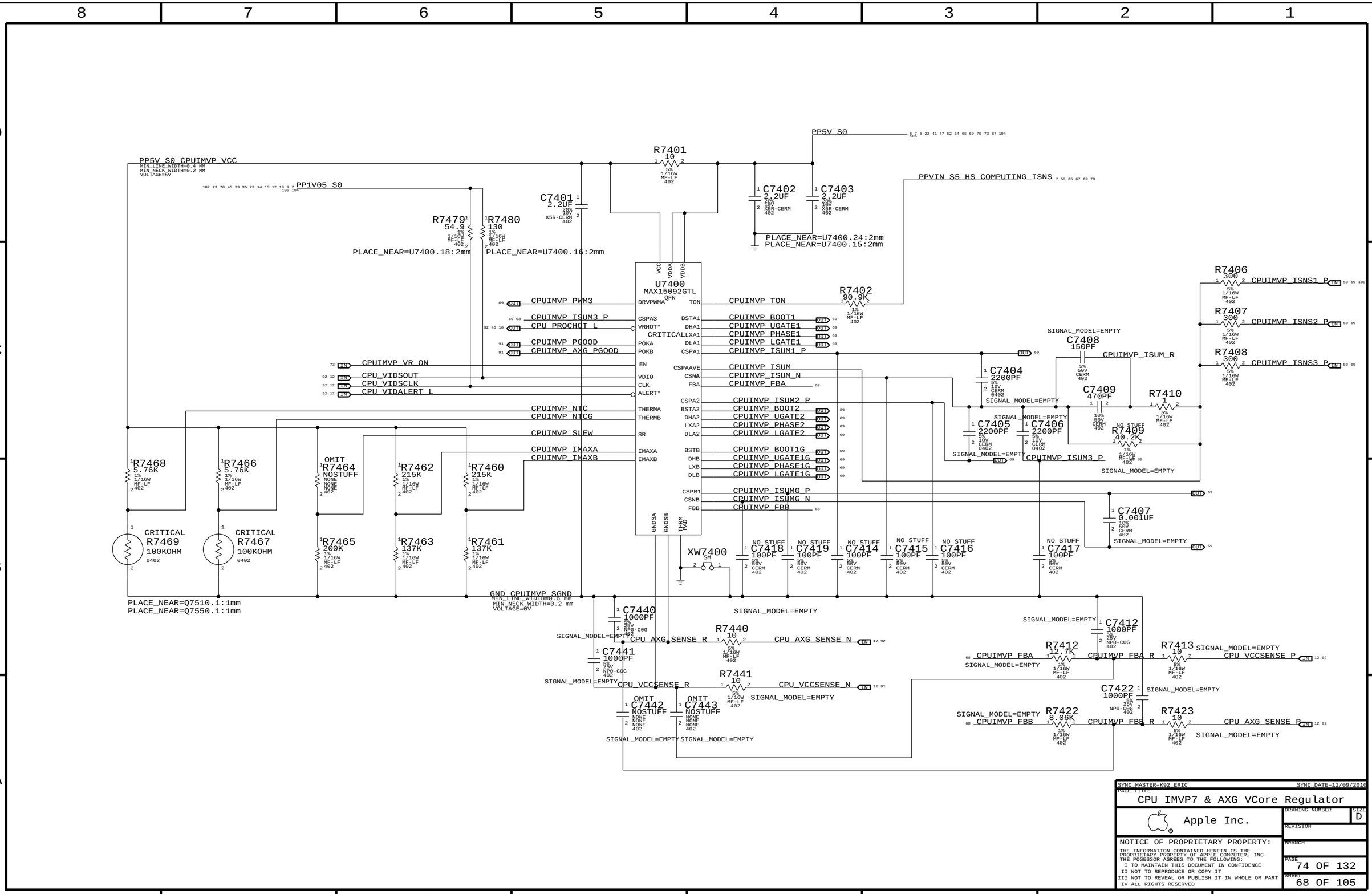

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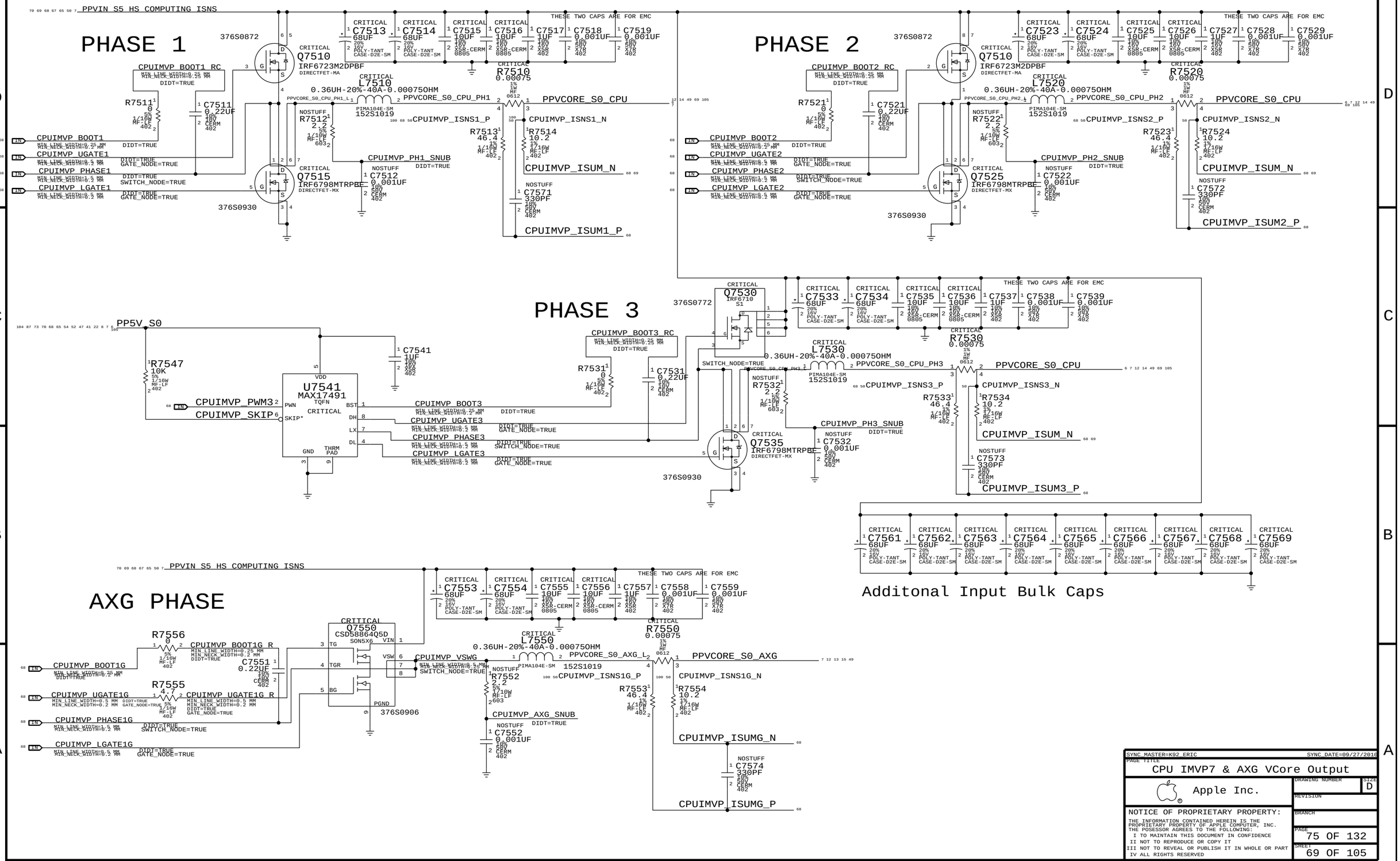

SYNC_MASTER=K92_ERIC SYNC_DATE=09/27/2010

PAGE TITLE
CPU IMVP7 & AXG VCore Output

Apple Inc.

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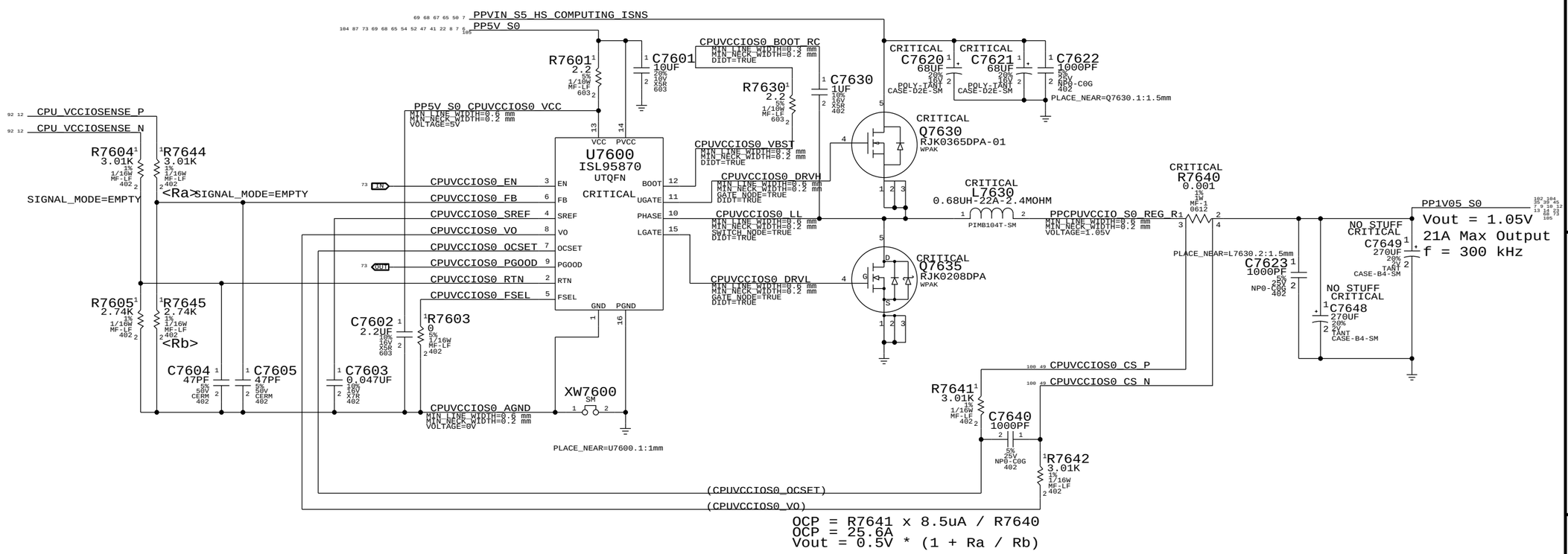
CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=K92_ERIC SYNC_DATE=09/23/2010

PAGE TITLE

CPU VCCIO (1.05V) Power Supply

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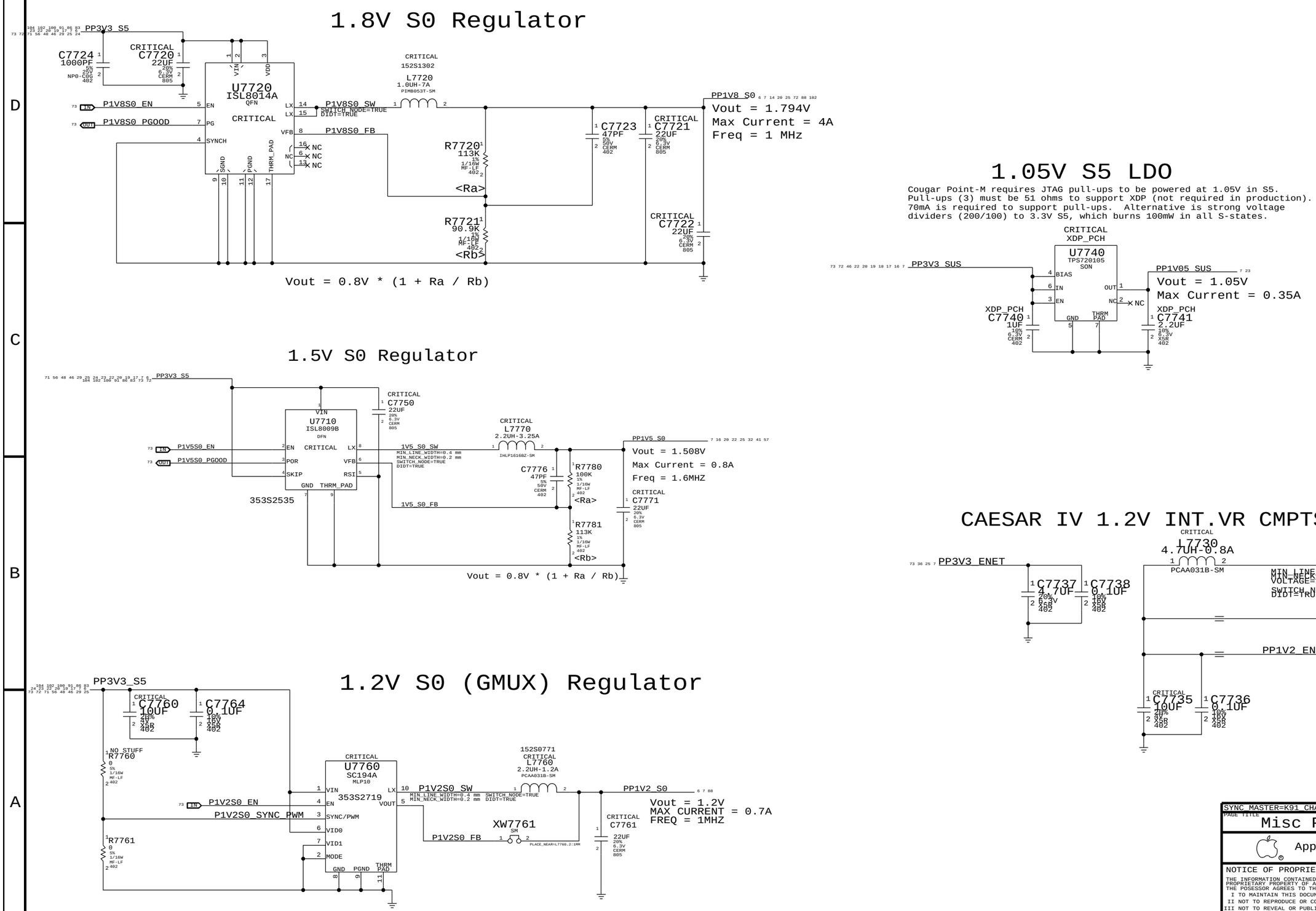

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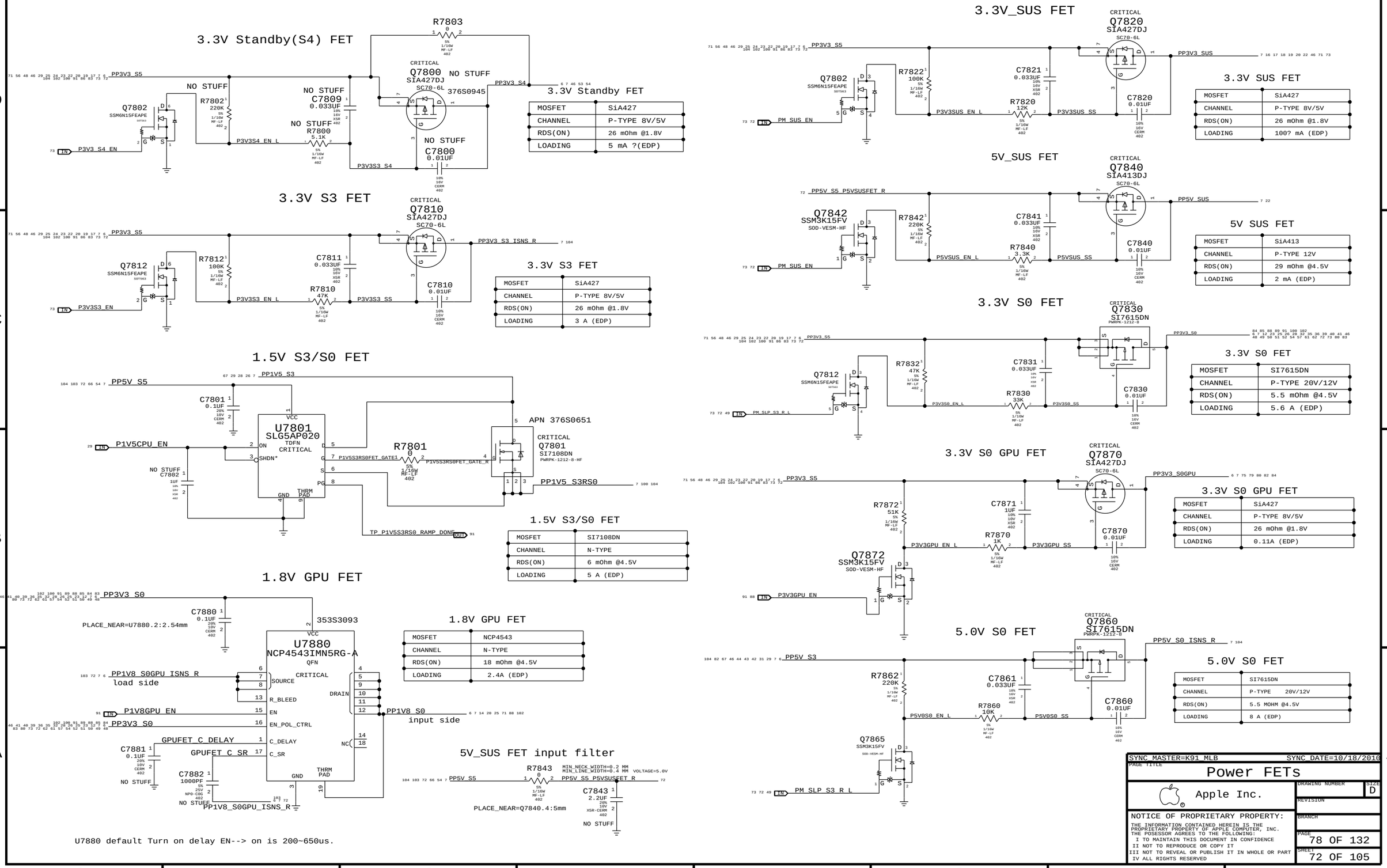

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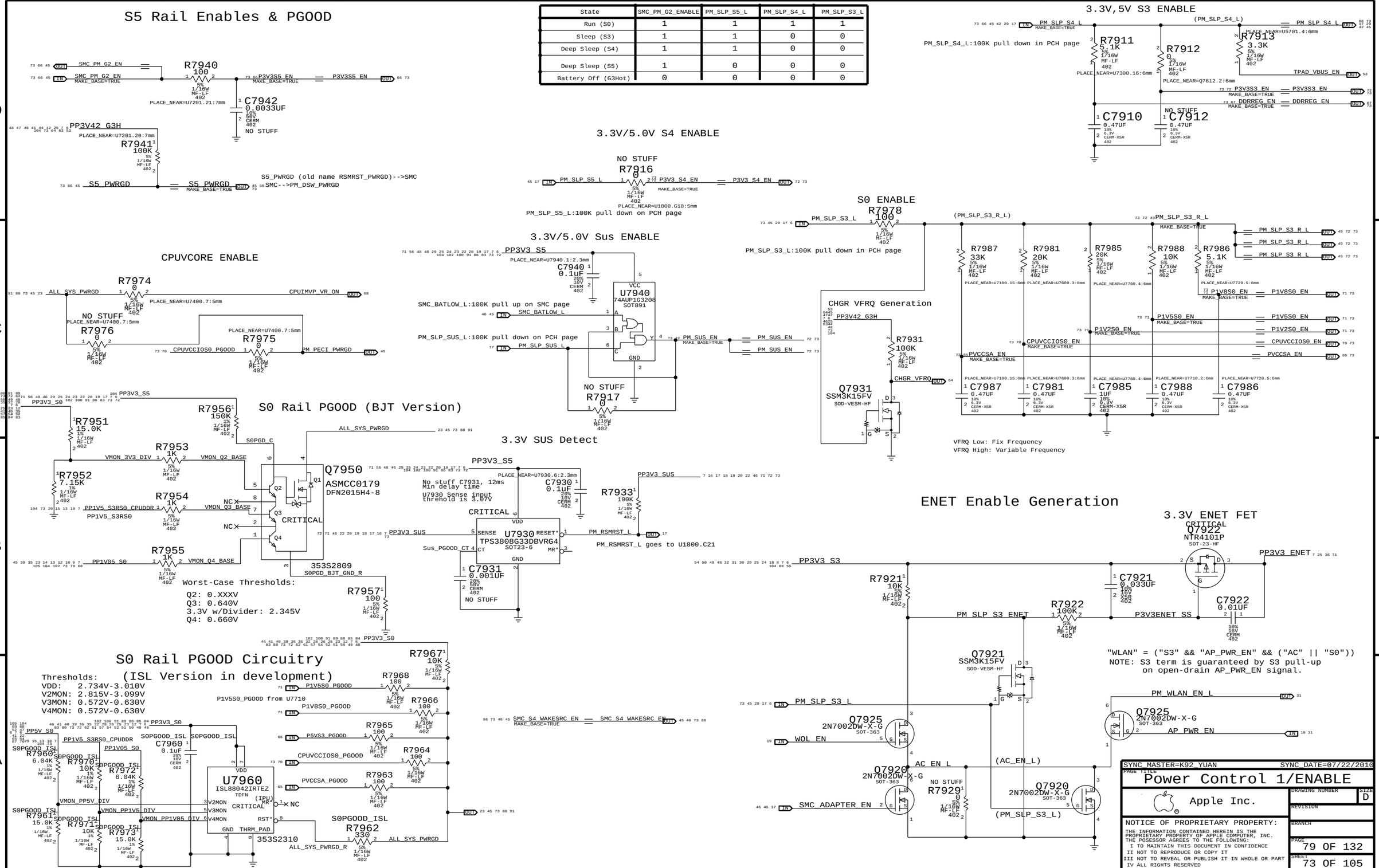
State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	0	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0



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Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC MASTER=K91_MLB SYNC DATE=10/19/2010

PAGE TITLE
Whistler PCI-E

Apple Inc.

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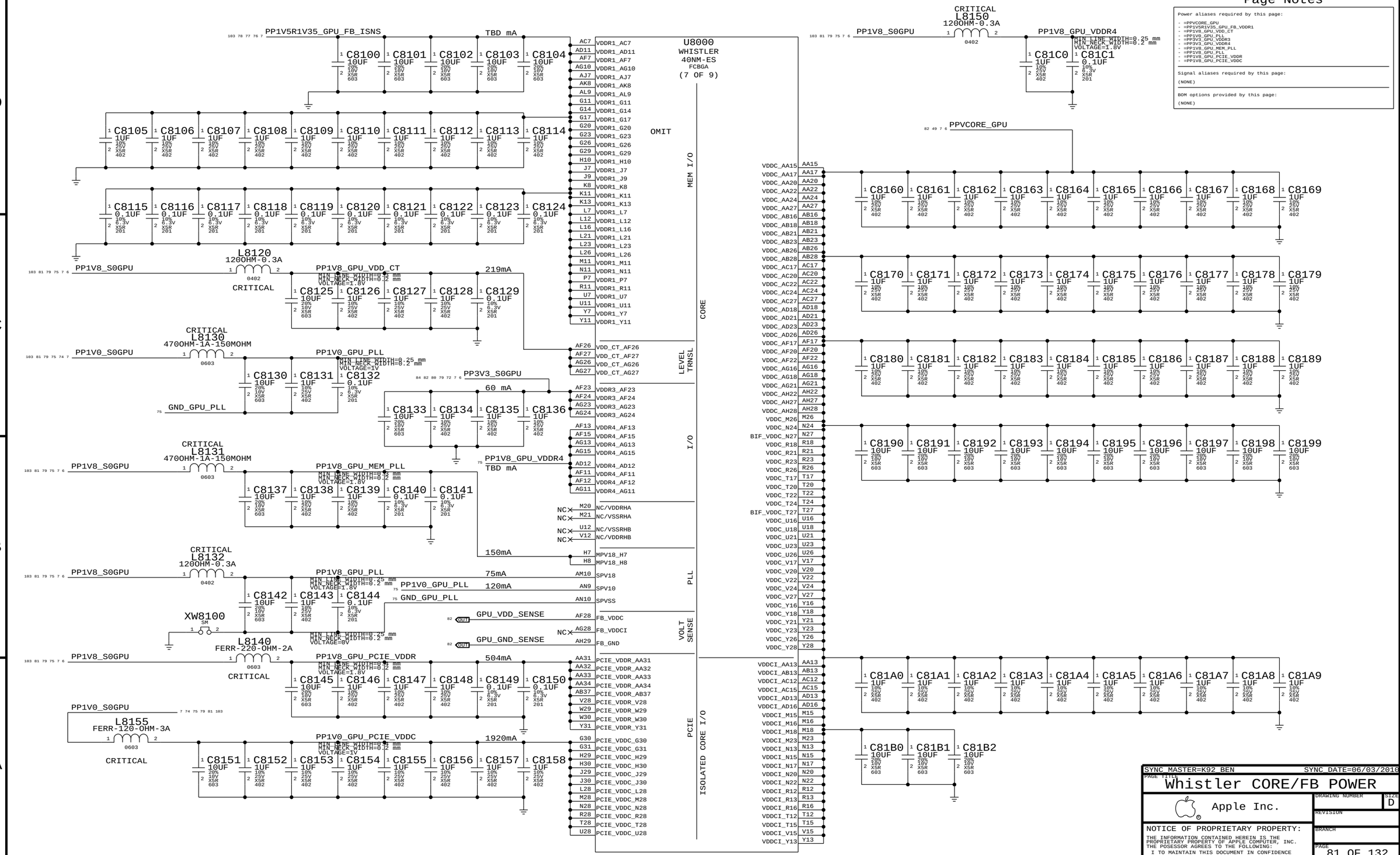

Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V5R1V35_GPU_FB_VDDR1
- =PP1V8_GPU_VDD_CT
- =PP1V0_GPU_PLL
- =PP3V3_GPU_VDDR3
- =PP3V3_GPU_VDDR4
- =PP1V8_GPU_MEM_PLL
- =PP1V8_GPU_PLL
- =PP1V8_GPU_PCIE_VDDR
- =PP1V8_GPU_PCIE_VDDC

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC_MASTER=K92_BEN	SYNC_DATE=06/03/2010
PAGE TITLE: Whistler CORE/FB POWER	
Apple Inc.	DRAWING NUMBER / SIZE D
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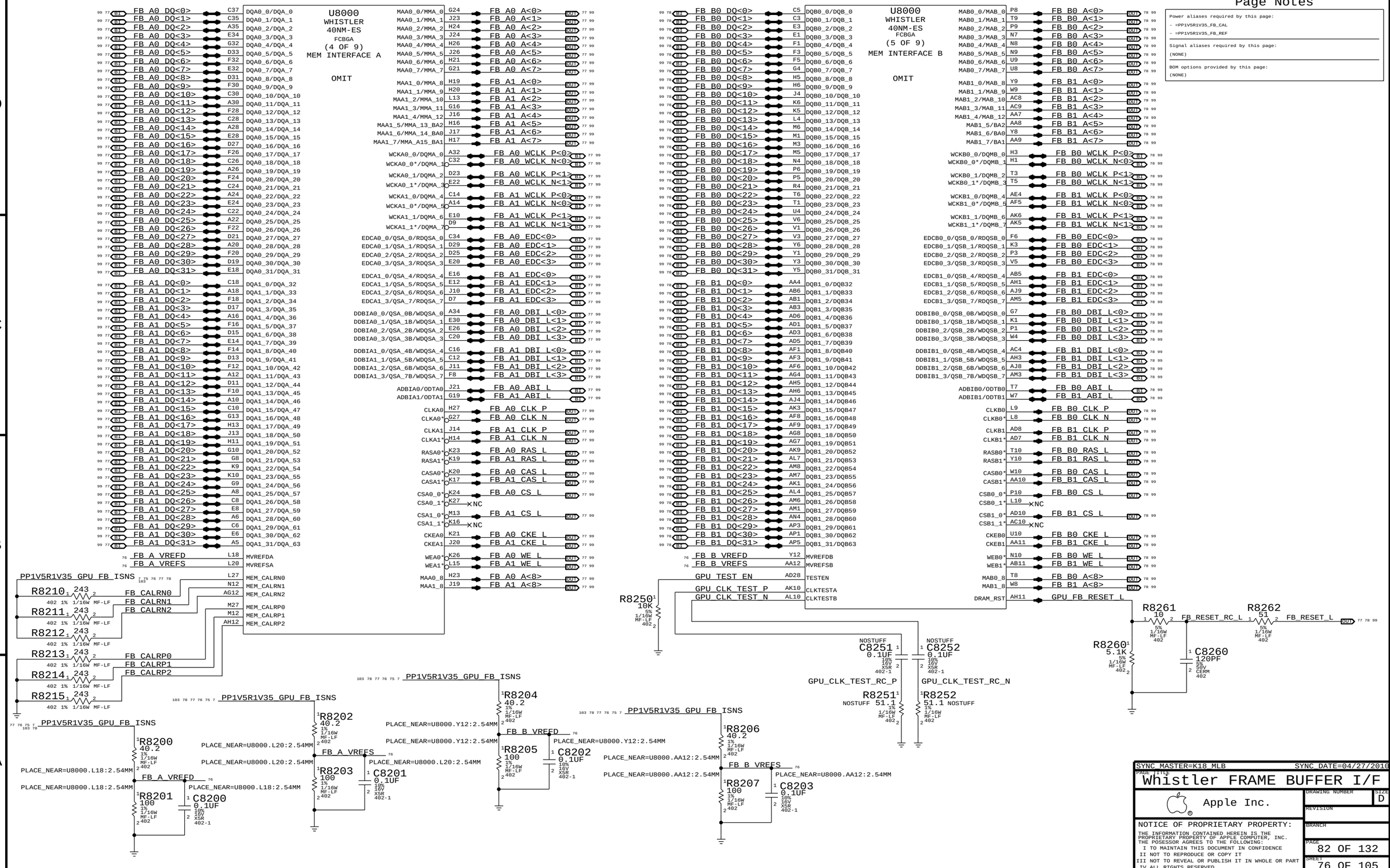

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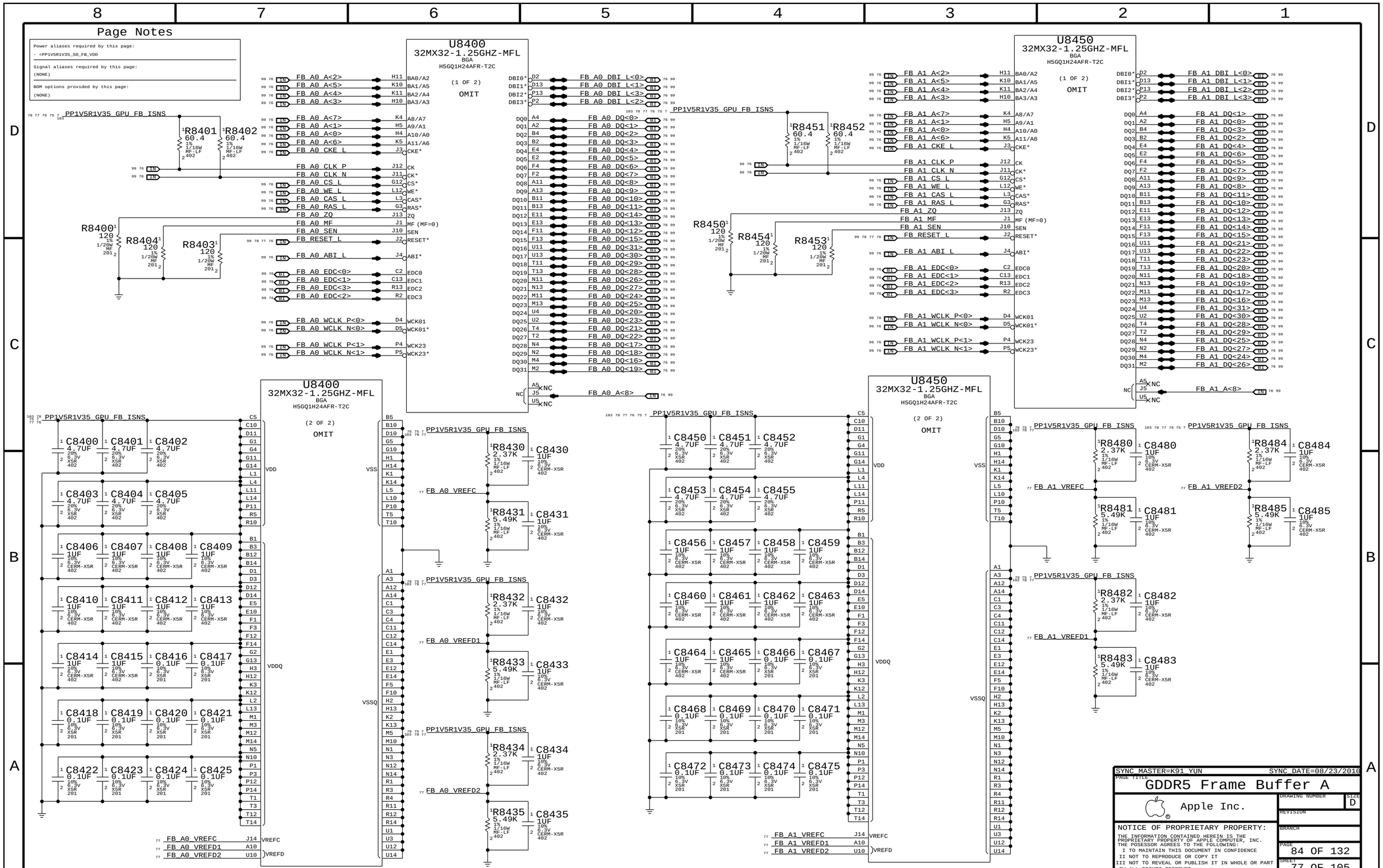

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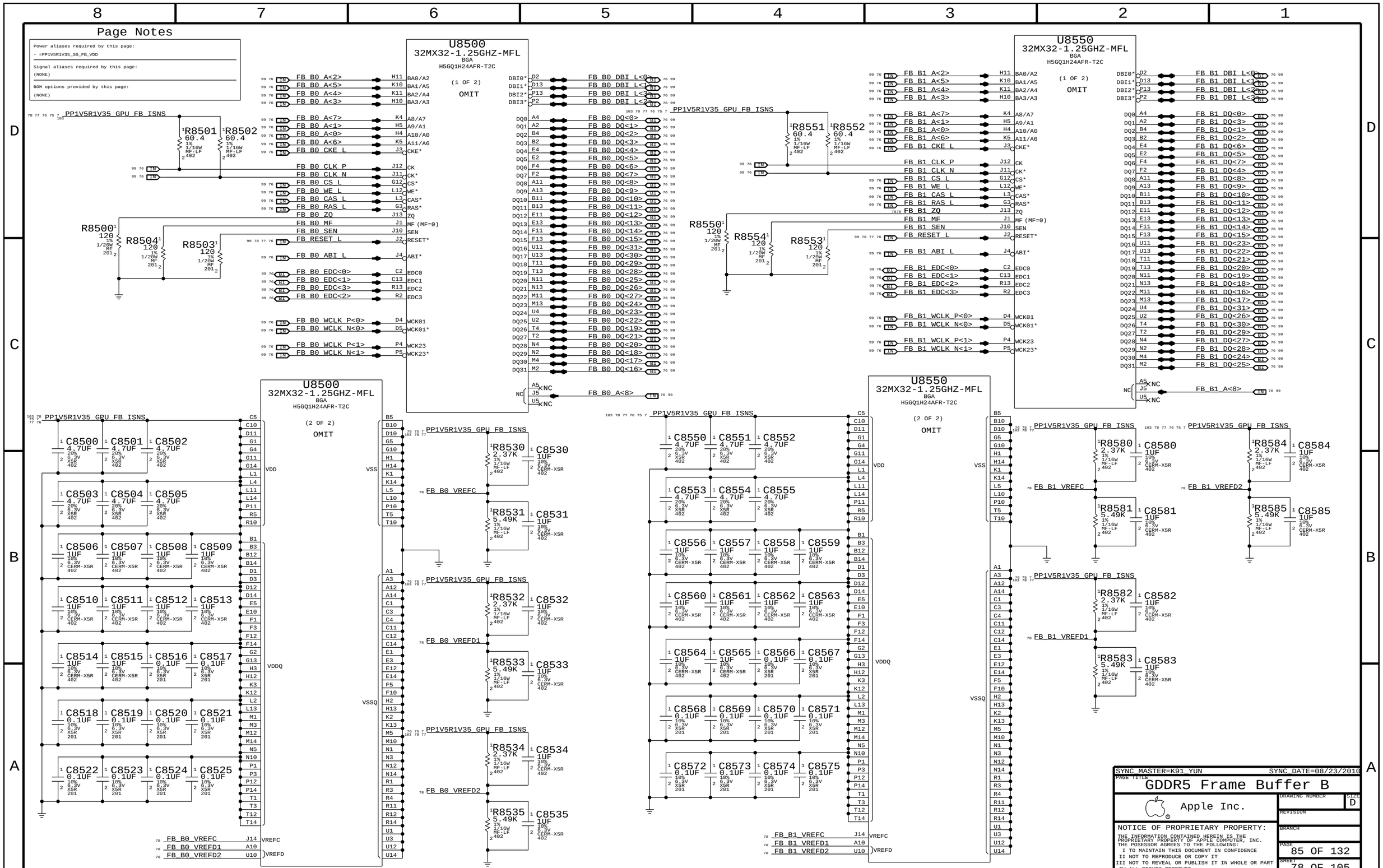

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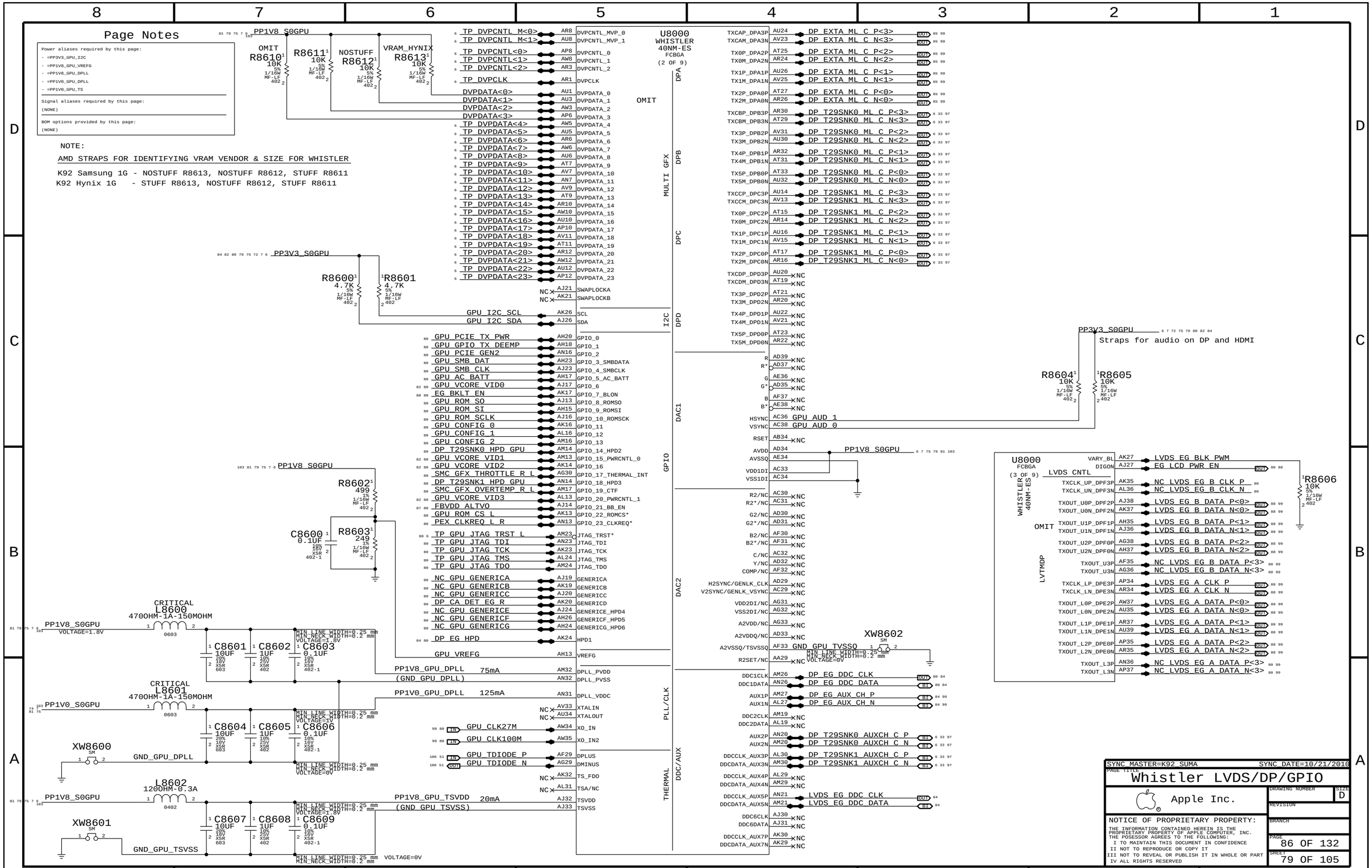

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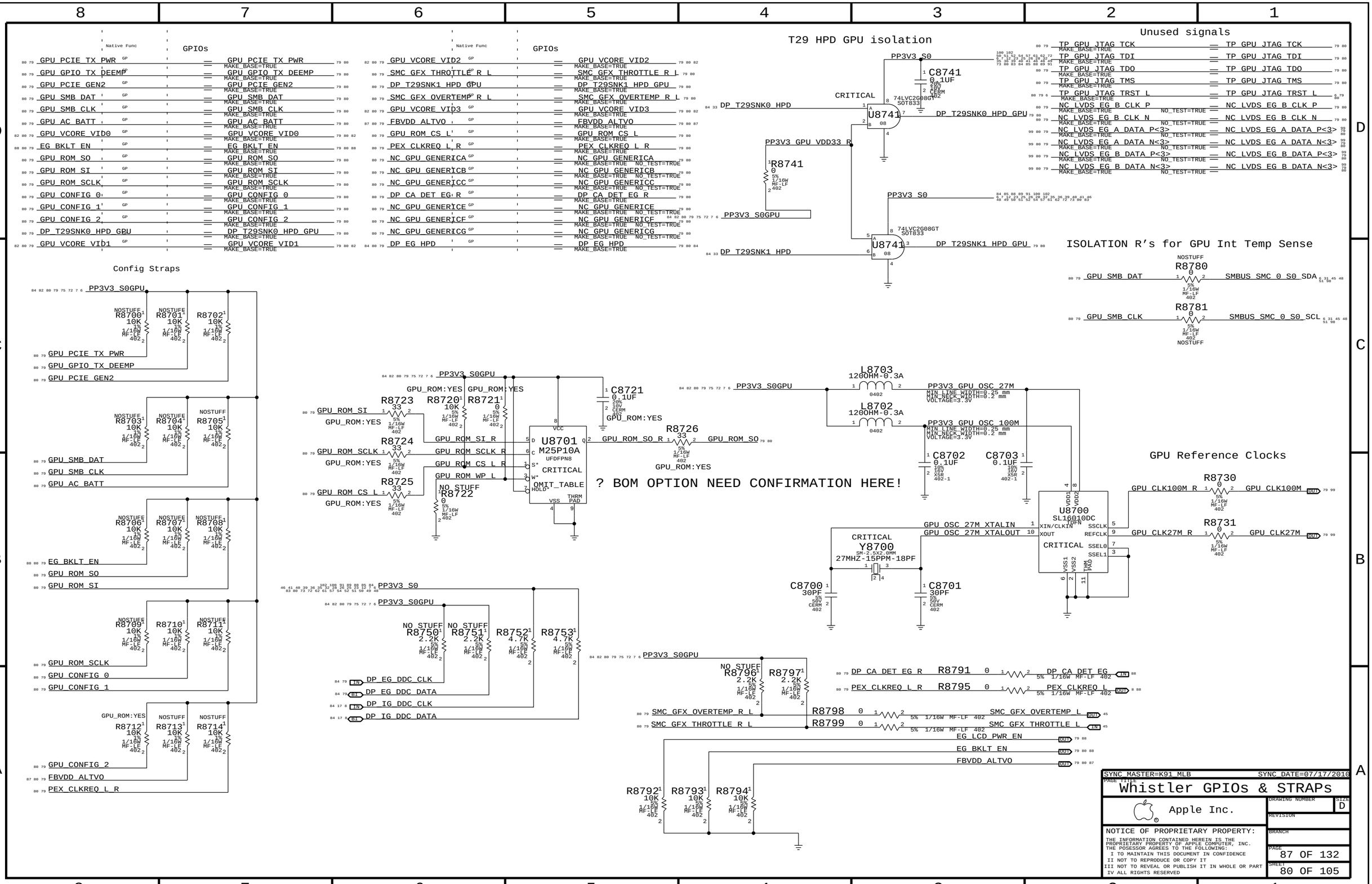

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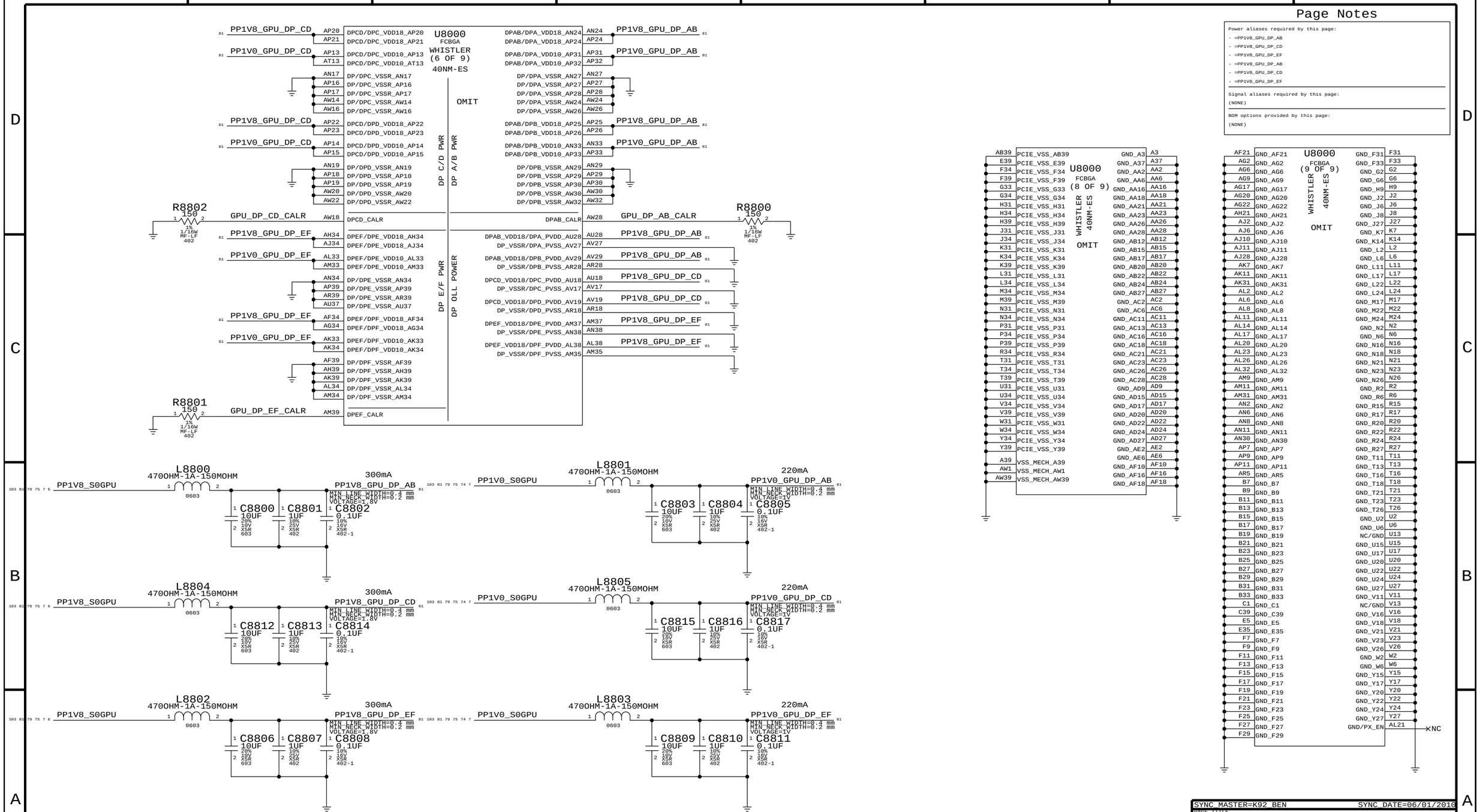

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=K92_BEN SYNC_DATE=06/01/2010

PAGE TITLE: Whistler DP PWR/GNDs

Apple Inc.

DRAWING NUMBER: SIZE D

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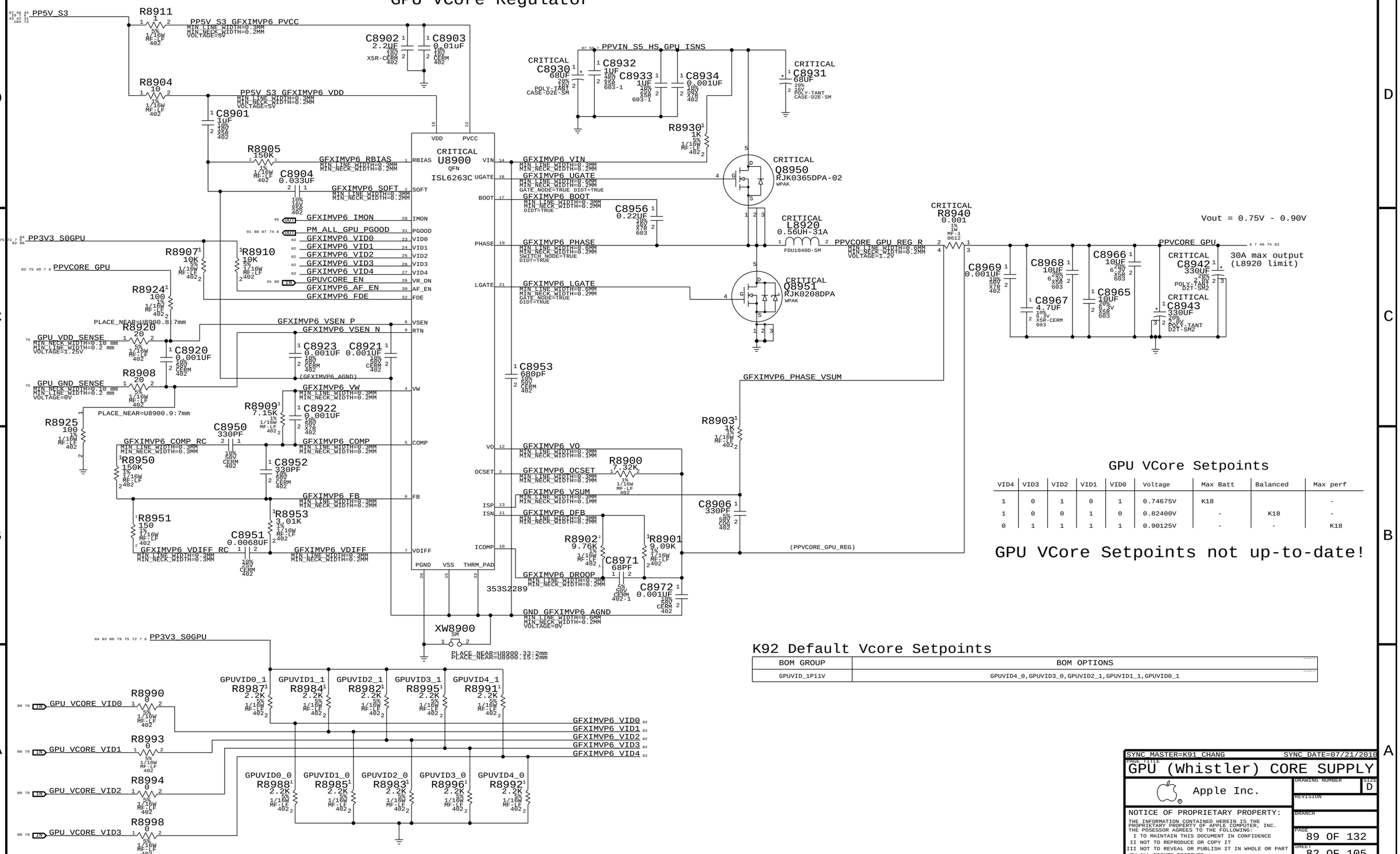
GPU VCore Regulator



GPU VCore Setpoints

VID4	VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	0	1	0	1	0.74675V	K18		-
1	0	0	1	0	0.82400V	-	K18	-
0	1	1	1	1	0.90125V	-	-	K18

GPU VCore Setpoints not up-to-date!

K92 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_1P11V	GPUVID4_0,GPUVID3_0,GPUVID2_1,GPUVID1_1,GPUVID0_1

SYNC_MASTER=K91_CHANG SYNC_DATE=07/21/2010

PAGE TITLE
GPU (Whistler) CORE SUPPLY

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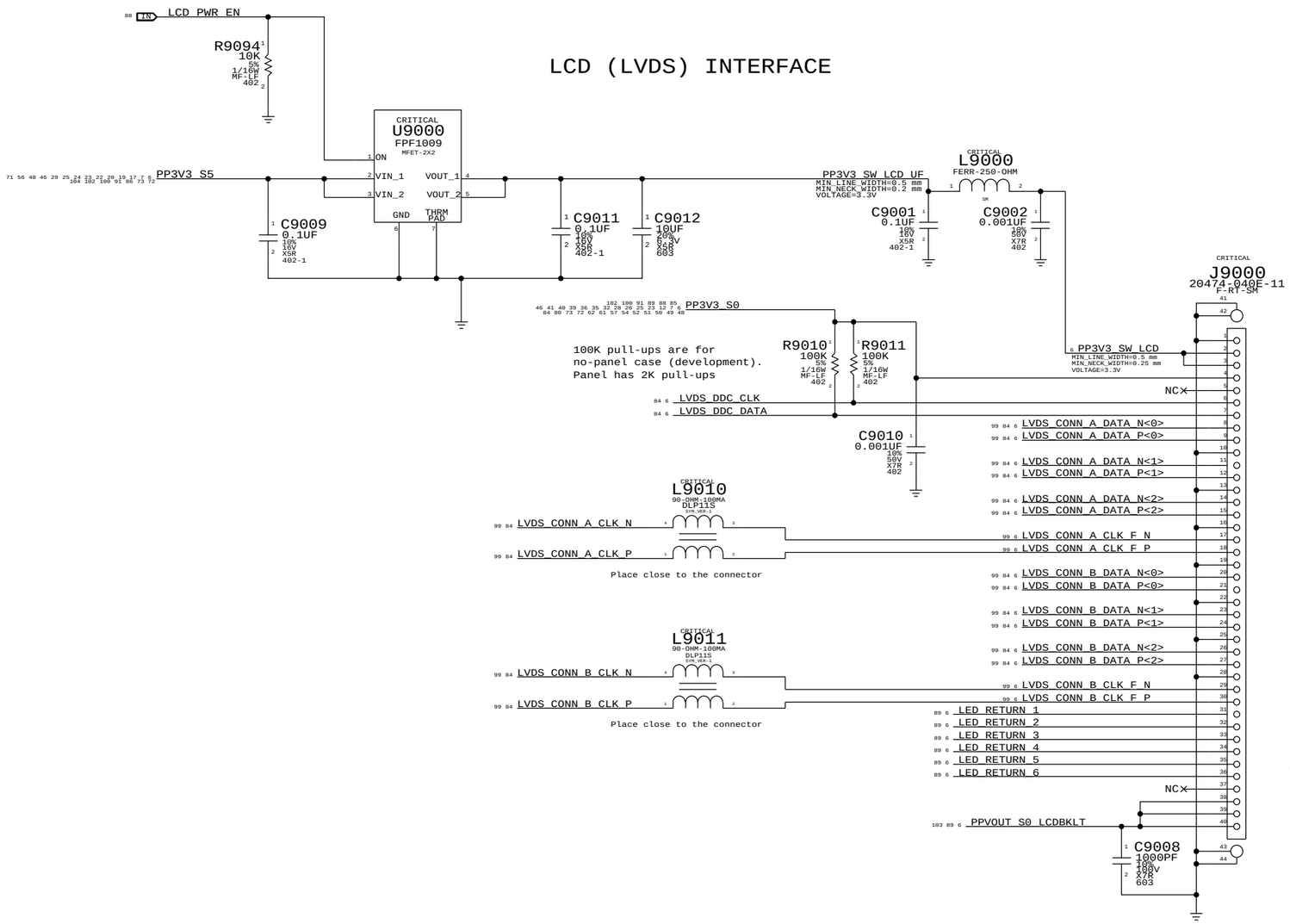
LCD (LVDS) INTERFACE



518S0651

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE
LVDS Display Connector

Apple Inc.

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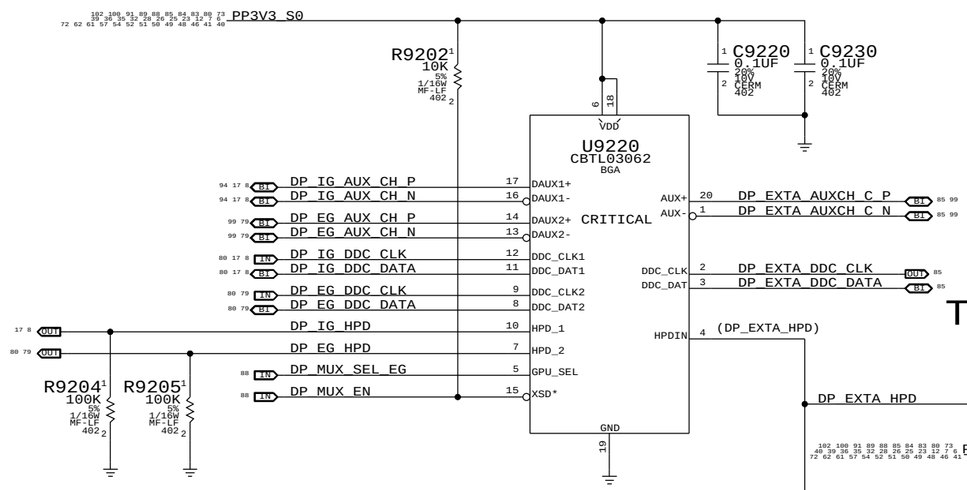
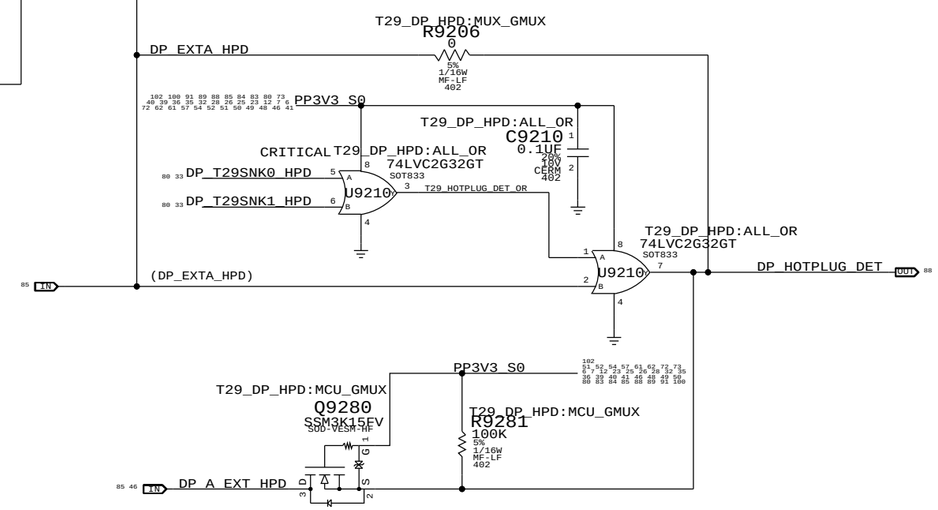
LVDS Transmitter Termination

All emulated LVDS outputs require this termination

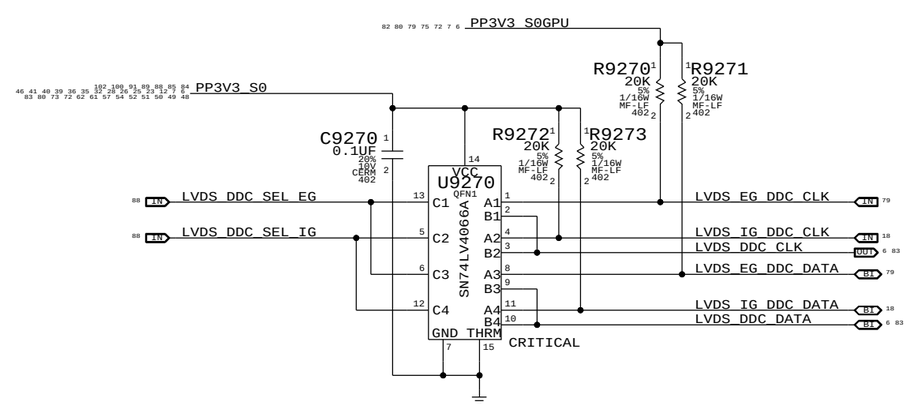
DP AUX, DDC, & HPD muxing to IG/EG



T29/DP HOT PLUG IN



LVDS DDC MUX



SYNC_MASTER=K92_YUN SYNC_DATE=06/25/2010

PAGE TITLE
Muxed Graphics Support

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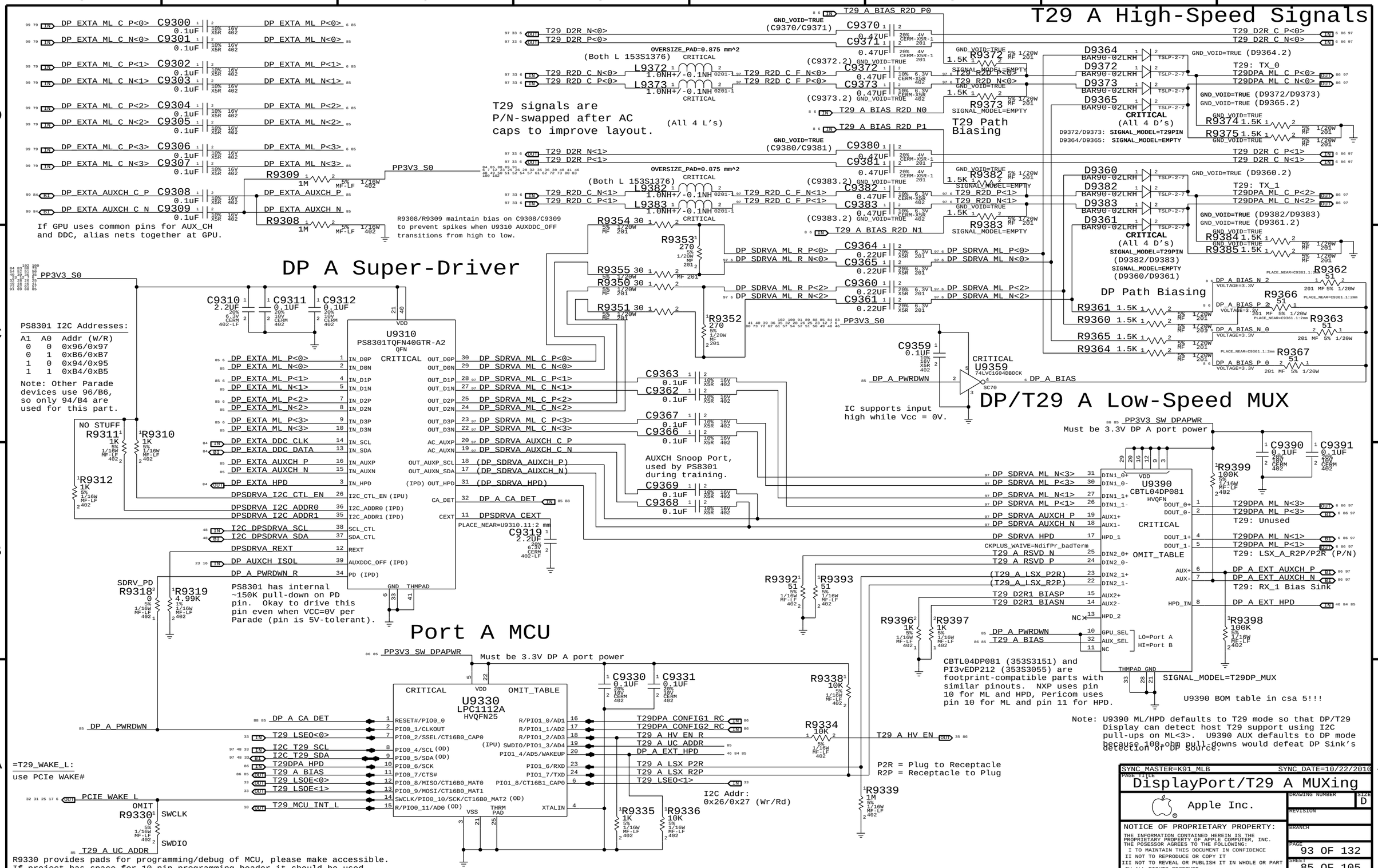

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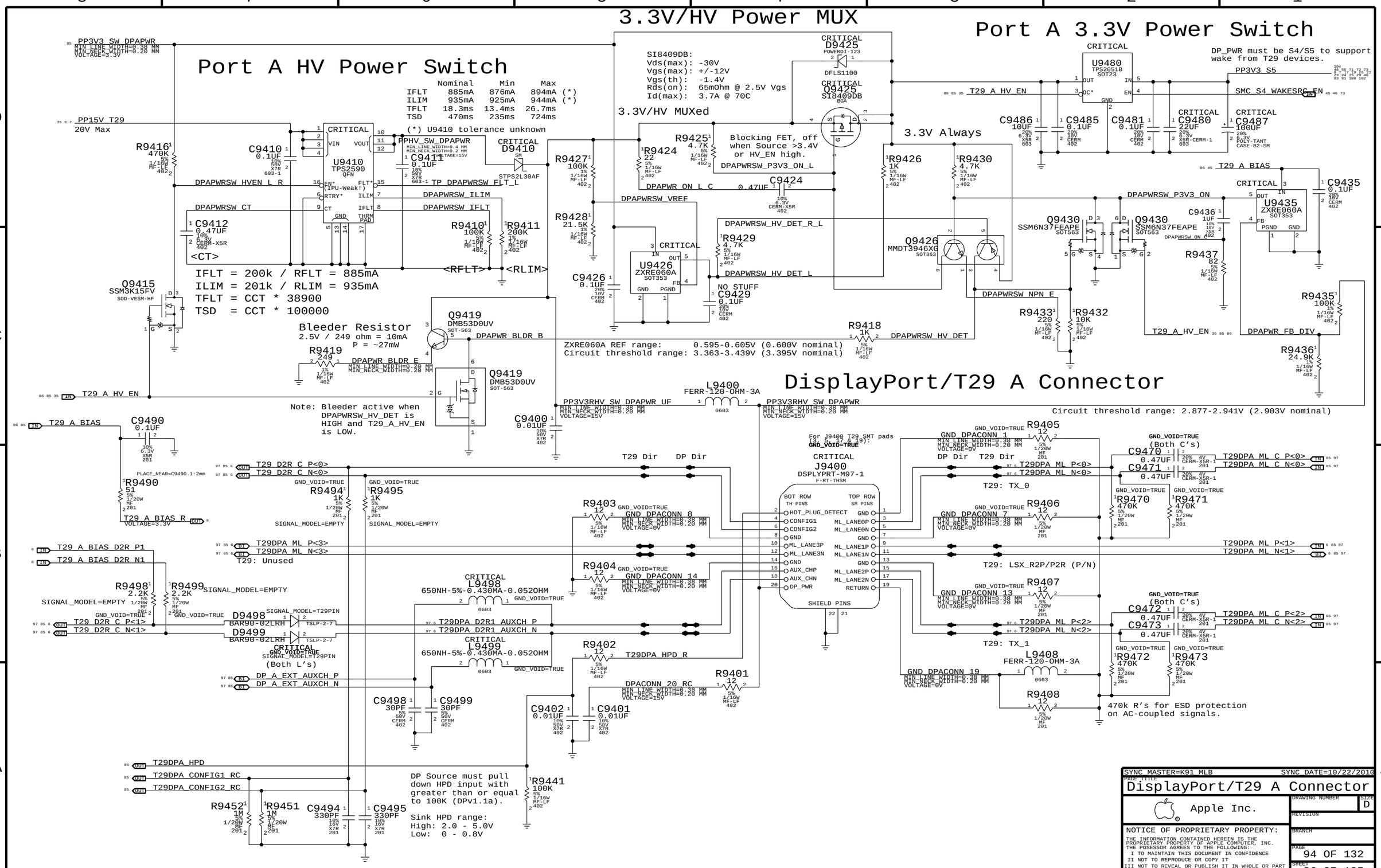

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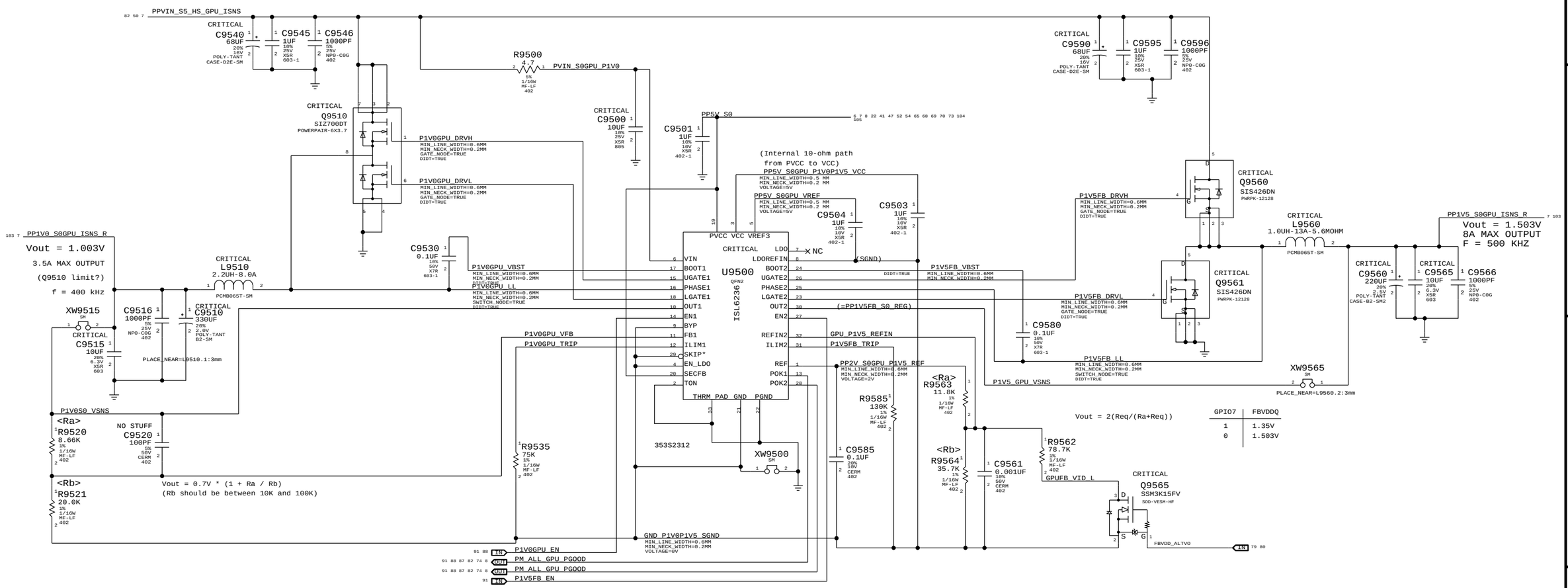

SYNC MASTER=K91 CHANG SYNC DATE=07/21/2010

PAGE TITLE
1V0 GPU / 1V5 FB Power Supply

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GMUX CPLD

LVDS Receiver Termination

LVDS IG A CLK P	R9650	100	PLACE NEAR=U9600.H3;5mm	LVDS IG A CLK N
LVDS IG A DATA P<0>	R9651	100	PLACE NEAR=U9600.E1;5mm	LVDS IG A DATA N<0>
LVDS IG A DATA P<1>	R9652	100	PLACE NEAR=U9600.E3;5mm	LVDS IG A DATA N<1>
LVDS IG A DATA P<2>	R9653	100	PLACE NEAR=U9600.G1;5mm	LVDS IG A DATA N<2>
LVDS IG B DATA P<0>	R9654	100	PLACE NEAR=U9600.G2;5mm	LVDS IG B DATA N<0>
LVDS IG B DATA P<1>	R9655	100	PLACE NEAR=U9600.G3;5mm	LVDS IG B DATA N<1>
LVDS IG B DATA P<2>	R9656	100	PLACE NEAR=U9600.B2;5mm	LVDS IG B DATA N<2>
LVDS EG A CLK P	R9660	100	PLACE NEAR=U9600.J12;5mm	LVDS EG A CLK N
LVDS EG A DATA P<0>	R9661	100	PLACE NEAR=U9600.D13;5mm	LVDS EG A DATA N<0>
LVDS EG A DATA P<1>	R9662	100	PLACE NEAR=U9600.E14;5mm	LVDS EG A DATA N<1>
LVDS EG A DATA P<2>	R9663	100	PLACE NEAR=U9600.F12;5mm	LVDS EG A DATA N<2>
LVDS EG B DATA P<0>	R9664	100	PLACE NEAR=U9600.G14;5mm	LVDS EG B DATA N<0>
LVDS EG B DATA P<1>	R9665	100	PLACE NEAR=U9600.G13;5mm	LVDS EG B DATA N<1>
LVDS EG B DATA P<2>	R9666	100	PLACE NEAR=U9600.H12;5mm	LVDS EG B DATA N<2>

Required Pullups

SIGNAL_MODEL=EMPTY

PP3V3_S0

EG PWRSEQ EN	R9684	1K
JTAG GMUX TDI	R9685	10K
JTAG GMUX TDO	R9686	10K
GMUX DEBUG RESET L	R9680	1K

NO STUFF R9679 10K 1% 1/16W MF-LF 402 SILK_PART=GMUX_RST

Required Pulldowns

DP MUX SEL EG	R9681	10K
LVDS DDC SEL IG	R9682	10K
LVDS DDC SEL EG	R9683	10K
EG RESET L	R9691	100K
LCD BKLT PWM	R9693	100K

NO STUFF

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

PP3V3_S0 R9600 0 5% 1/16W MF-LF 402

PP1V8_S0 R9610 0 5% 1/16W MF-LF 402

C9610 0.1UF 20% 10V CERM 402 — C9621 0.1UF 20% 10V CERM 402 — C9622 0.1UF 20% 10V CERM 402 — C9623 0.1UF 20% 10V CERM 402 — C9624 0.1UF 20% 10V CERM 402 — C9625 0.1UF 20% 10V CERM 402 — C9626 0.1UF 20% 10V CERM 402 — C9627 0.1UF 20% 10V CERM 402 — C9628 0.1UF 20% 10V CERM 402 — C9629 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_R MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.09 mm VOLTAGE=3.3V

PP1V8_S0_GMUX_R MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.09 mm VOLTAGE=1.8V

C9611 0.1UF 20% 10V CERM 402 — C9612 0.1UF 20% 10V CERM 402 — C9613 0.1UF 20% 10V CERM 402 — C9614 0.1UF 20% 10V CERM 402 — C9615 0.1UF 20% 10V CERM 402 — C9616 0.1UF 20% 10V CERM 402 — C9617 0.1UF 20% 10V CERM 402

PP1V2_S0: C9600 4.7UF 20% 4V X5R 402 — C9604 0.1UF 20% 10V CERM 402 — C9605 0.1UF 20% 10V CERM 402 — C9606 0.1UF 20% 10V CERM 402 — C9607 0.1UF 20% 10V CERM 402 — C9608 0.1UF 20% 10V CERM 402 — C9609 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_ULC_VCCPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.09 mm VOLTAGE=3.3V — L9621 FERR-220-OHM 0402 — C9631 0.1UF 20% 10V CERM 402

PP3V3_S0_GMUX_LRC_VCCPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.09 mm VOLTAGE=3.3V — L9620 FERR-220-OHM 0402 — C9630 0.1UF 20% 10V CERM 402

PP3V3_S0: R9645 10K 1% 1/20W MF 201 — R9640 10K 1% 1/20W MF 201

NO STUFF R9646 10K 1% 1/20W MF 201 — NO STUFF R9641 10K 1% 1/20W MF 201

JTAG ISP TCK	K14	TCK	
JTAG GMUX TDI	L13	TDI	
JTAG GMUX TDO	K13	TDO	
JTAG GMUX TMS	L12	TMS	
GMUX TOE	K2	TOE	
GMUX CFG0	K1	CFG0	
LCD BKLT EN	P2	PB7A	BANK5
LCD BKLT PWM	N2	PB7B	BANK5
LVDS DDC SEL EG	P4	PB14A	BANK5
LVDS DDC SEL IG	N4	PB14B	BANK5
DP MUX EN	N3	PB15A(OD)	BANK5
DP MUX SEL EG	M4	PB15B	BANK5
EG RESET L	P5	PB16A	BANK5
P3V3GPU EN	M5	PB16B	BANK5
GPUVCORE EN	P6	PB17A	BANK5
P1V0GPU EN	M6	PB17B	BANK5
P1V5FB1V8GPU R EN	P7	PB18A	BANK5
PEG CLKREQ L	M7	PB18B(OD)	BANK5
DP CA DET EG	N7	PB19A	BANK5
LCD PWR EN	N8	PB19B	BANK5
LPC AD<0>	P9	PB20A	BANK4
LPC AD<1>	N9	PB20B	BANK4
LPC AD<2>	P10	PB26A	BANK4
LPC AD<3>	M10	PB26B	BANK4
LPC FRAME L	P12	PB27A	BANK4
LPCPLUS RESET L	P13	PB27B	BANK4
LPC CLK33M GMUX	N12	PB28A	BANK4
GMUX INT	P14	PB28B	BANK4
LVDS IG B DATA P<2>	B1	PL2A	BANK7
LVDS IG B DATA N<2>	B2	PL2B	BANK7
GMUX PL6A	C2	PL6A	BANK7
TP GMUX PL6B	D3	PL6B	BANK7
LVDS IG A DATA P<0>	D1	PL7A	BANK7
LVDS IG A DATA N<0>	E1	PL7B	BANK7
LVDS IG A DATA P<1>	D2	PL8A	BANK7
LVDS IG A DATA N<1>	E3	PL8B	BANK7
LVDS IG A DATA P<2>	F1	PL9A	BANK7
LVDS IG A DATA N<2>	G1	PL9B	BANK7
LVDS IG B DATA P<0>	F3	PL10A	BANK7
LVDS IG B DATA N<0>	G2	PL10B	BANK7
LVDS IG B DATA P<1>	H2	PL11A	BANK7
LVDS IG B DATA N<1>	G3	PL11B	BANK7
LVDS IG A CLK P	H1	PL12A	BANK7
LVDS IG A CLK N	H3	PL12B	BANK7
TP LVDS MUX SEL EG	L1	PL14A	BANK6
TP GMUX PL14B	L3	PL14B	BANK6
GMUX RESET L	K3	PL15A	BANK6
GMUX VSYNC	L2	PL15B	BANK6
PM ALL GPU PGOOD	N1	PL25A	BANK6
PEX CLKREQ L	P1	PL25B	BANK6

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

OMIT CRITICAL

U9600 XP25-5 CSBGA

LVDS B DATA P<0>	A2	PT7A	BANK0
LVDS B DATA N<0>	A3	PT7B	BANK0
LVDS B DATA P<1>	A1	PT8A	BANK0
LVDS B DATA N<1>	B3	PT8B	BANK0
LVDS B DATA P<2>	C5	PT9A	BANK0
LVDS B DATA N<2>	A5	PT9B	BANK0
EG PWRSEQ EN	B6	PT14A	BANK0
GMUX DEBUG RESET L	C7	PT14B	BANK0
LVDS A CLK P	A6	PT15A	BANK0
LVDS A CLK N	A7	PT15B	BANK0
LVDS B CLK P	C8	PT16A	BANK0
LVDS B CLK N	C9	PT16B	BANK0
LVDS A DATA P<0>	A8	PT17A	BANK0
LVDS A DATA N<0>	B9	PT17B	BANK0
LVDS A DATA P<1>	A9	PT18A	BANK0
LVDS A DATA N<1>	C10	PT18B	BANK0
LVDS A DATA P<2>	B10	PT19A	BANK0
LVDS A DATA N<2>	A10	PT19B	BANK0
GND	A11	PT20A	BANK1
GND	B12	PT20B	BANK1
GND	B13	PT28A	BANK1
GND	A13	PT28B	BANK1
DP A CA DET	A14	PR2A	BANK2
DP HOTPLUG DET	B14	PR2B	BANK2
LVDS EG A DATA P<0>	D12	PR6A	BANK2
LVDS EG A DATA N<0>	D13	PR6B	BANK2
LVDS EG A DATA P<1>	D14	PR7A	BANK2
LVDS EG A DATA N<1>	E14	PR7B	BANK2
LVDS EG A DATA P<2>	E12	PR8A	BANK2
LVDS EG A DATA N<2>	F12	PR8B	BANK2
LVDS EG B DATA P<0>	F14	PR9A	BANK2
LVDS EG B DATA N<0>	G14	PR9B	BANK2
LVDS EG B DATA P<1>	G12	PR10A	BANK2
LVDS EG B DATA N<1>	G13	PR10B	BANK2
LVDS EG B DATA P<2>	H13	PR11A	BANK2
LVDS EG B DATA N<2>	H12	PR11B	BANK2
LVDS EG A CLK P	H14	PR12A	BANK2
LVDS EG A CLK N	J12	PR12B	BANK2
LVDS IG PANEL PWR	L14	PR14A	BANK3
EG LCD PWR EN	M13	PR14B	BANK3
LVDS IG BKL ON	N14	PR24A	BANK3
EG BKLT EN	N13	PR24B	BANK3

CRITICAL J9600 1909782 M-RT-SM GMUX_JTAG_CONN

PP3V3_S0	1
JTAG GMUX TDO	2
JTAG GMUX TDI	3
JTAG GMUX TMS	4
	5
JTAG ISP TCK	6
	8

NO STUFF R9647 10K 1% 1/20W MF 201

NO STUFF R9670 10K 1% 1/20W MF 201 — GMUX_VSYNC

R9605 1K 5% 1/16W MF-LF 402 — PP3V3_T29 — T29_JTAG_FET

Q9605 SSM6N15FEAPE SOT563 — JTAG_GMUX_TDI — JTAG_ISP_TDI

Q9605 SSM6N15FEAPE SOT563 — JTAG_GMUX_TDO — JTAG_ISP_TDO

PP3V3_S3 — R9676 100K 5% 1/20W MF 201 — GMUX_S3_PD_EN — Q9607 SSM6N15FEAPE SOT563

Q9607 SSM6N15FEAPE SOT563 — ALL_SYS_PWRGD

P1V5FB1V8GPU R EN	R9674	4.7K
P1V0GPU EN	R9673	4.7K
GPUVCORE EN	R9672	4.7K
P3V3GPU EN	R9671	4.7K
LCD PWR EN	R9678	4.7K

GMUX_S3_PD_GND

NO STUFF R9675 0 5% 1/16W MF-LF 402

PP3V3_S0 — R9684 1K — R9685 10K — R9686 10K — R9680 1K

SYNC_MASTER=K92_YUAN	SYNC_DATE=07/28/2010	
PAGE TITLE	Graphics MUX (GMUX)	
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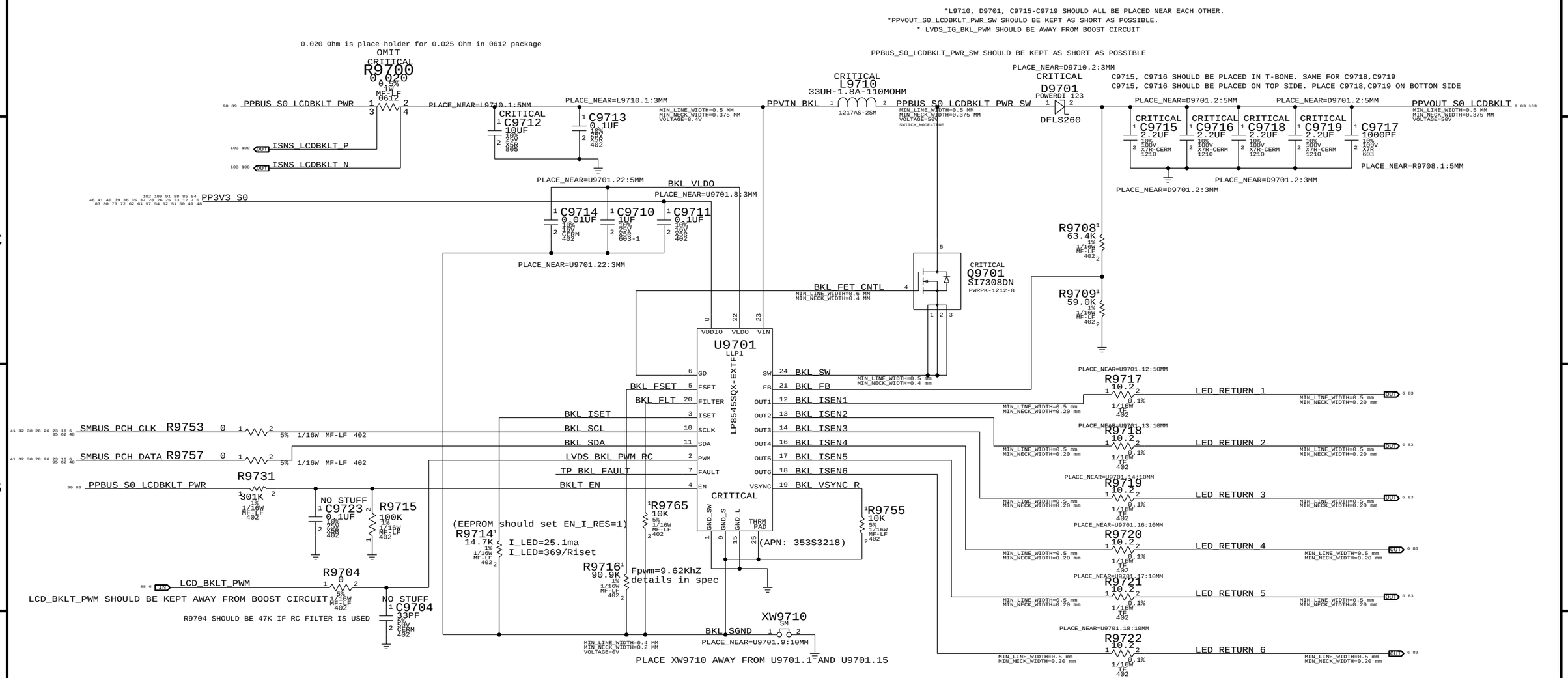

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0196	1	0.025OHM,1W,0612,MTL FILM RES	R9700	CRITICAL	

SYNC_MASTER=K92_DINESH SYNC_DATE=09/07/2010

PAGE TITLE
LCD Backlight Driver (LP8545)

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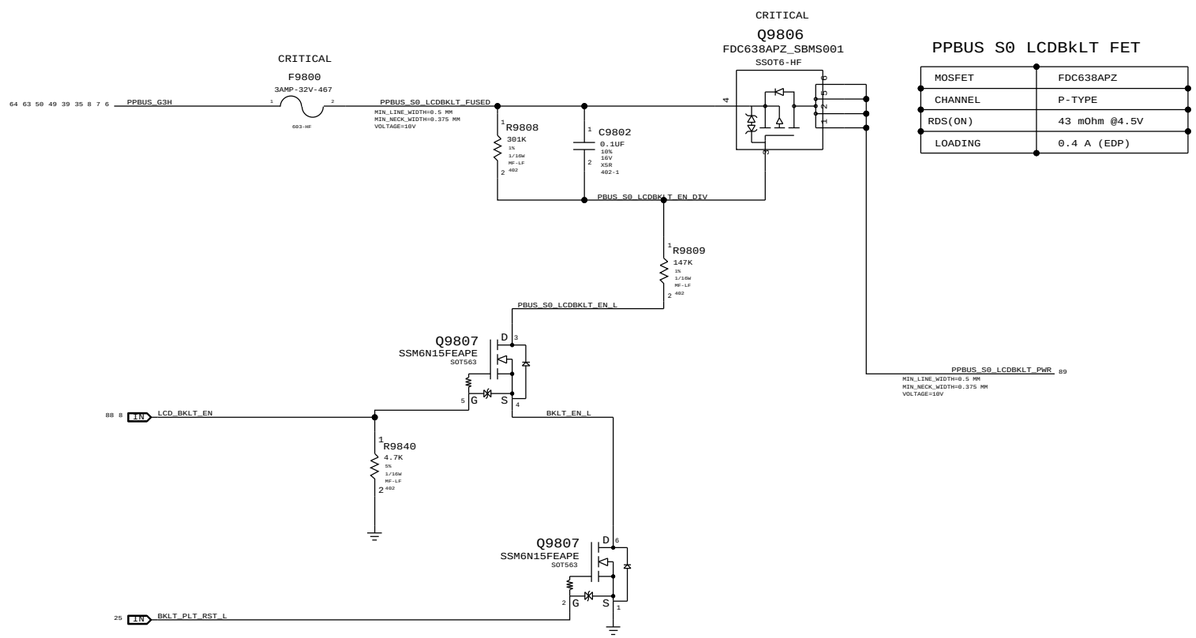

PPBUS S0 LCDBkLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

SYNC_MASTER=K17_MLB SYNC_DATE=04/26/2010

PAGE TITLE
LCD Backlight Support

Apple Inc.

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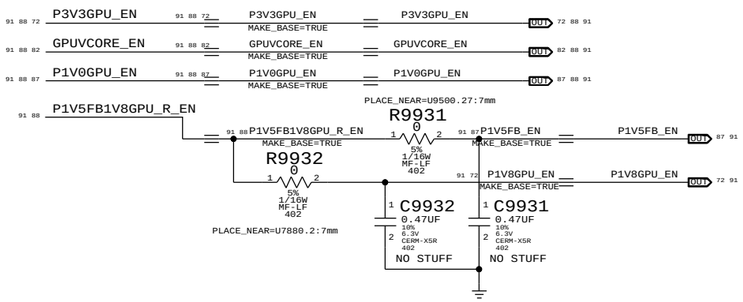
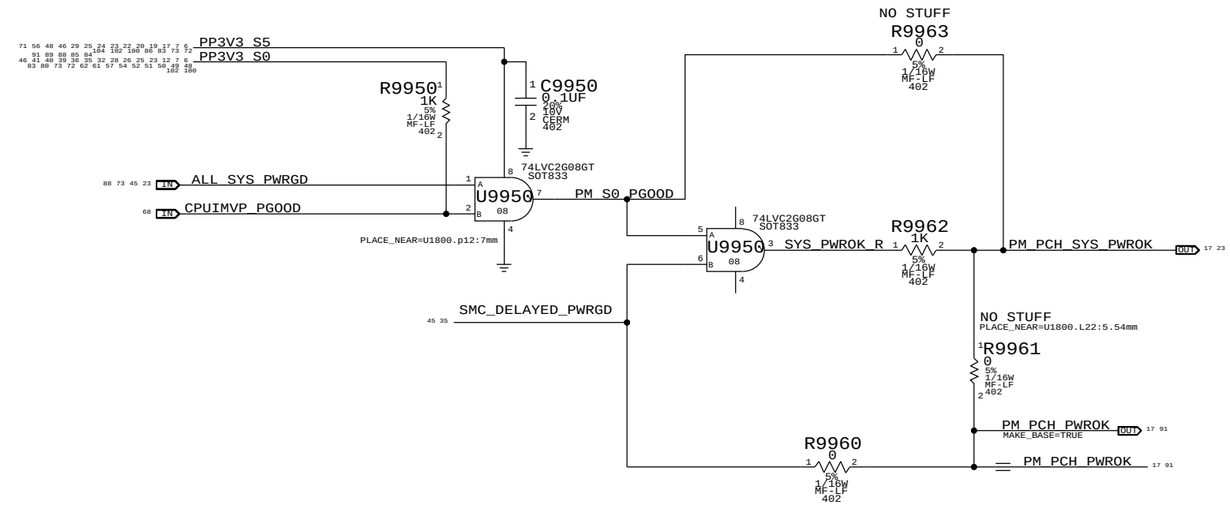
GPU Rail Sequencing

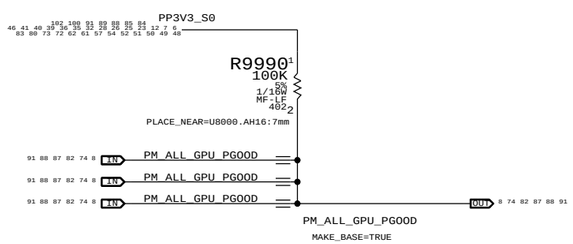
Whistler GPU requires rails to come up in the following order:
1) GPU_3.3V
2) GPUVcore
3) GPU_1.0V
4) GPU_1.8V;GDDR5 1.5/1.35V



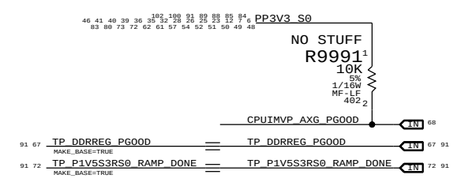
PCH S0 PWRGD



EXT GPU PWRGD Pullup



Unused PGOOD signal



SYNC_MASTER=K92_YUAN SYNC_DATE=07/30/2010

PAGE TITLE
Power Sequencing EG/PCH S0

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NEECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Calpella SFF DG (DG-407364_v1.5), Section 2.8

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	6 9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	6 9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	6 9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 45
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 29
XDP_CPU_PWRGOOD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	23
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
XDP_PREQ_l	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP0	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP1	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP2	
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..16>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	10 17
	CPU_50S	CPU_AGTL	TP_CPU_VTT_SELECT	8
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_55S	CPU_8MIL	CPU_PSI_L	
PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_RBIAS	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP3	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP2	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP1	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP0	
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	10 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
	CPU_55S	CPU_8MIL	CPU_VID<6..0>	8
	CPU_50S	CPU_AGTL	CPUIMVP_IMON	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 68
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	12
	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	12
	CPU_55S	CPU_8MIL	GFX_VID<6..0>	8
PM_DPRSLPVR	CPU_50S	CPU_AGTL	GFX_DPRSLPVR	
	CPU_50S	CPU_AGTL	GFX_VR_EN	
	CPU_50S	CPU_AGTL	GFXIMVP_IMON	
	PCIE_85D	PCIE	PEG_R2D_P<7..0>	74
	PCIE_85D	PCIE	PEG_R2D_N<7..0>	74
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<7..0>	8 74
	PCIE_85D	PCIE	PEG_R2D_C_N<7..0>	8 74
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<7..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_N<7..0>	8 74
	PCIE_85D	PCIE	PEG_D2R_C_P<7..0>	74
	PCIE_85D	PCIE	PEG_D2R_C_N<7..0>	74
	CPU_50S	CPU_VID	CPU_VIDSOUT	12 68
	CPU_50S	CPU_VID	CPU_VIDSCLK	12 68
	CPU_50S	CPU_VID	CPU_VIDALERT_L	12 68

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3:
DQ/DM signals should be matched within 0.508mm of associated DQS pair.
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-12.7mm] and [CLK+25.4mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-12.7mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from procesor ball to SODIMM pad is 114.3mm.

SOURCE: Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	11 26
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM A CKE<3..0>	11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM A CS L<3..0>	11 26
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM A ODT<3..0>	11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	11 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	11 26
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	11 26 27
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	11 27
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	11 27
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	11 26 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	11 27
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	11 27
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	11 27
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	11 27
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM B CKE<3..0>	11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM B CS L<3..0>	11 28
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM B ODT<3..0>	11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	11 28
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	11 28
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	11 27
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	11 27
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	11 27
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	11 27
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	11 27 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	11 27
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	11 27
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	11 27
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	11 27 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	11 27 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	11 27
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	11 27
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	11 27
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	11 27
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	11 27
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	11 27
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	11 27
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	11 27

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_85D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
LVDS	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?
LVDS	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	ISL3,ISL4,ISL9,ISL10	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	ISL3,ISL4,ISL9,ISL10	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8 17 84
DP_AUX_CH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8 17 84
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_P	18 88
LVDS_IG_A_CLK	LVDS_85D	LVDS	LVDS_IG_A_CLK_N	18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 88
LVDS_IG_A_DATA	LVDS_85D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 88
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 18
LVDS_IG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 18
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 88
LVDS_IG_B_DATA	LVDS_85D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 88
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	6 16 41
	SATA_90D	SATA	SATA_HDD_R2D_C_N	6 16 41
SATA_HDD_RDVR_R2D	SATA_90D	SATA	SATA_HDD_R2D_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_N	6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_UF_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_UF_N	6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N	6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N	6 41
DP_SATA_G3_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_UF_P	6 41
	SATA_90D	SATA	SATA_HDD_R2D_RC_UF_N	6 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	6 16 41
	SATA_90D	SATA	SATA_HDD_D2R_N	6 16 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P	6 41
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N	6 41
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P	6 41
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N	6 41
SATA_HDD_RDVR_D2R	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 41
	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	16 41
	SATA_90D	SATA	SATA_ODD_R2D_C_N	16 41
	SATA_90D	SATA	SATA_ODD_R2D_P	6 41
	SATA_90D	SATA	SATA_ODD_R2D_N	6 41
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_UF_P	41
	SATA_90D	SATA	SATA_ODD_R2D_UF_N	41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	16 41
	SATA_90D	SATA	SATA_ODD_D2R_N	16 41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_C_P	41
	SATA_90D	SATA	SATA_ODD_D2R_C_N	41
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_UF_P	6 41
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	6 41
PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP	16
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	18 24
	USB_85D	USB	USB_HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	18 24
	USB_85D	USB	USB_HUB2_UP_N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P	24 42
	USB_85D	USB	USB_EXTA_N	24 42
USB_EXTB	USB_85D	USB	USB_EXTB_P	24 42
	USB_85D	USB	USB_EXTB_N	24 42
USB_EXTC	USB_85D	USB	USB_EXTC_P	24 43
	USB_85D	USB	USB_EXTC_N	24 43
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 31
	USB_85D	USB	USB_CAMERA_CONN_N	6 31
USB_BT	USB_85D	USB	USB_BT_P	6 24 31
	USB_85D	USB	USB_BT_N	6 24 31
USB_TPAD	USB_85D	USB	USB_TPAD_P	24 53
	USB_85D	USB	USB_TPAD_N	24 53
USB_IR	USB_85D	USB	USB_IR_P	24 44
	USB_85D	USB	USB_IR_N	24 44
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	18
USB_T29A	USB_85D	USB	USB_T29A_P	8 24
	USB_85D	USB	USB_T29A_N	8 24

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC AD<3..0>	6 16 45 47 88
LPC_FRAME_L	LPC_50S	LPC	LPC FRAME L	6 16 45 47 88
LPC_RESET_L	LPC_50S	LPC	LPCPLUS RESET L	6 25 47 88
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R	18 25
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC	25 45
PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS	6 25 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS PCH CLK	6 16 23 26 28 30 32 41 48 62 89
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS PCH DATA	6 16 23 26 28 30 32 41 48 62 89
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML PCH 0 CLK	16 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML PCH 0 DATA	16 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML PCH 1 CLK	16 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML PCH 1 DATA	16 48
HDA_BIT_CLK	HDA_50S	HDA	HDA BIT CLK	16 57
	HDA_50S	HDA	HDA BIT CLK R	16
HDA_SYNC	HDA_50S	HDA	HDA SYNC	16 57
	HDA_50S	HDA	HDA SYNC R	16
HDA_RST_L	HDA_50S	HDA	HDA RST R L	16
	HDA_50S	HDA	HDA RST L	16 57
HDA_SDIN0	HDA_50S	HDA	HDA SDIN0	16 57
	HDA_50S	HDA	AUD SDI R	57
HDA_SDOUT	HDA_50S	HDA	HDA SDOUT	16 57
	HDA_50S	HDA	HDA SDOUT R	16
SPI_CLK	SPI_55S	SPI	SPI CLK R	16 47
SPI_CLK	SPI_55S	SPI	SPI CLK	47
SPI_MOSI	SPI_55S	SPI	SPI MOSI R	16 47
SPI_MOSI	SPI_55S	SPI	SPI MOSI	47
SPI_MISO	SPI_55S	SPI	SPI MISO	16 47
SPI_CS0	SPI_55S	SPI	SPI CS0 R L	16 47
	SPI_55S	SPI	SPI CS0 L	47
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D P	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D N	36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C P	16 36
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R P	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R C P	36
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R C N	36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D P	6 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D N	6 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C P	16 31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C N	16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R P	6 16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R N	6 16 31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R PI P	31
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R PI N	31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D PI P	31
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D PI N	31
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D P	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D N	38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D C P	16 38
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D C N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R P	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R C P	38
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R C N	38
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH P	16
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH N	16
PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 P	16 33
PCIE_CLK100M_T29_	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M T29 N	16 33
	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT P	16
	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT N	16
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA P	16
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA N	16
	CPU_50S	CLK_PCIE	PCH CLK14P3M REFCLK	16
	CPU_50S	CLK_PCIE	PCH CLK33M PCIIN	16 25
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M P	16 74
	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M N	16 74
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET N	16 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP P	16 31
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP N	16 31
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW N	16 38
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M EXCARD P	16 32
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M EXCARD N	16 32
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D C P<3..0>	8 33
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D C N<3..0>	8 33
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D P<3..0>	33
PCIE_T29_R2D	PCIE_85D	PCIE	PCIE T29 R2D N<3..0>	33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R P<3..0>	8 33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R N<3..0>	8 33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R C P<3..0>	33
PCIE_T29_D2R	PCIE_85D	PCIE	PCIE T29 D2R C N<3..0>	33

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CAESAR II (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

CAESAR II (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	32 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
I16 FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	38 40
I16 FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	38 40
I16 FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	38 40
I16 FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	38 40

Port 0 and 2 Not Used

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_85D	DISPLAYPORT	DP T29SNK0 ML C P<3..0>	6 33 79
	DP_85D	DISPLAYPORT	DP T29SNK0 ML C N<3..0>	6 33 79
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML P<3..0>	6 33
DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP T29SNK0 ML N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C P	6 33 79
	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH C N	6 33 79
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH P	6 33
DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK0 AUXCH N	6 33
	DP_85D	DISPLAYPORT	DP T29SNK1 ML C P<3..0>	6 33 79
	DP_85D	DISPLAYPORT	DP T29SNK1 ML C N<3..0>	6 33 79
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML P<3..0>	6 33
DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP T29SNK1 ML N<3..0>	6 33
	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C P	6 33 79
	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH C N	6 33 79
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH P	6 33
DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP T29SNK1 AUXCH N	6 33
	DP_85D	DISPLAYPORT	DP T29SRC ML C P<3..0>	
	DP_85D	DISPLAYPORT	DP T29SRC ML C N<3..0>	
	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C P	
	DP_85D	DISPLAYPORT	DP T29SRC AUXCH C N	
	T29_I2C_55S	T29_I2C	I2C T29 SCL	33 48 85
	T29_I2C_55S	T29_I2C	I2C T29 SDA	33 48 85
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29 SPI CLK	33
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29 SPI MOSI	33
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29 SPI MISO	33
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29 SPI CS L	33
	T29DP_80D	T29DP	T29 R2D C P<3..0>	6 8 33 85
	T29DP_80D	T29DP	T29 R2D C N<3..0>	6 8 33 85
	T29DP_100D	T29DP	T29 D2R P<3..0>	6 8 33 85
	T29DP_100D	T29DP	T29 D2R N<3..0>	6 8 33 85

Only used on hosts supporting T29 video-in

T29/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T29_R2D0	T29DP_80D	T29DP	T29 R2D P<0>	6 85
T29_R2D0	T29DP_80D	T29DP	T29 R2D N<0>	6 85
T29_R2D1	T29DP_80D	T29DP	T29 R2D P<1>	6 85
T29_R2D1	T29DP_80D	T29DP	T29 R2D N<1>	6 85
	T29DP_80D	T29DP	T29 R2D C F P<1..0>	85
	T29DP_80D	T29DP	T29 R2D C F N<1..0>	85
T29_D2R0	T29DP_100D	T29DP	T29 D2R C P<0>	6 85 86
T29_D2R0	T29DP_100D	T29DP	T29 D2R C N<0>	6 85 86
T29_D2R1	T29DP_100D	T29DP	T29 D2R C P<1>	6 85 86
T29_D2R1	T29DP_100D	T29DP	T29 D2R C N<1>	6 85 86
	T29DP_100D	T29DP	T29DPA D2R1 AUXCH P	6 86
	T29DP_100D	T29DP	T29DPA D2R1 AUXCH N	6 86
	T29DP_80D	T29DP	DP SDRVA ML C P<3..0>	6 85
	T29DP_80D	T29DP	DP SDRVA ML C N<3..0>	6 85
	T29DP_80D	T29DP	DP SDRVA ML R P<3..0>	6 85
	T29DP_80D	T29DP	DP SDRVA ML R N<3..0>	6 85
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP SDRVA ML P<2..0:2>	6 85 97
DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP SDRVA ML N<2..0:2>	6 85 97
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML P<3..1:2>	85
DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP SDRVA ML N<3..1:2>	85
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH P	85
DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP SDRVA AUXCH N	85
	T29DP_80D	T29DP	DP SDRVA AUXCH C P	85
	T29DP_80D	T29DP	DP SDRVA AUXCH C N	85
	T29DP_80D	T29DP	T29DPA ML P<3..0>	6 85 86
	T29DP_80D	T29DP	T29DPA ML N<3..0>	6 85 86
	T29DP_80D	T29DP	T29DPA ML C P<3..0>	85 86
	T29DP_80D	T29DP	T29DPA ML C N<3..0>	85 86
	T29DP_80D	T29DP	DP A EXT AUXCH P	85 86
	T29DP_80D	T29DP	DP A EXT AUXCH N	85 86
T29_R2D2	T29DP_80D	T29DP	T29 R2D P<2>	
T29_R2D2	T29DP_80D	T29DP	T29 R2D N<2>	
T29_R2D3	T29DP_80D	T29DP	T29 R2D P<3>	
T29_R2D3	T29DP_80D	T29DP	T29 R2D N<3>	
	T29DP_80D	T29DP	T29 R2D C F P<3..2>	
	T29DP_80D	T29DP	T29 R2D C F N<3..2>	
T29_D2R2	T29DP_100D	T29DP	T29 D2R C P<2>	
T29_D2R2	T29DP_100D	T29DP	T29 D2R C N<2>	
T29_D2R3	T29DP_100D	T29DP	T29 D2R C P<3>	
T29_D2R3	T29DP_100D	T29DP	T29 D2R C N<3>	
	T29DP_100D	T29DP	T29DPB D2R3 AUXCH P	
	T29DP_100D	T29DP	T29DPB D2R3 AUXCH N	
	T29DP_80D	T29DP	DP SDRVB ML C P<3..0>	
	T29DP_80D	T29DP	DP SDRVB ML C N<3..0>	
	T29DP_80D	T29DP	DP SDRVB ML R P<3..0>	
	T29DP_80D	T29DP	DP SDRVB ML R N<3..0>	
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP SDRVB ML P<2..0:2>	97
DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP SDRVB ML N<2..0:2>	97
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP SDRVB ML P<3..1:2>	
DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP SDRVB ML N<3..1:2>	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP SDRVB AUXCH P	
DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP SDRVB AUXCH N	
	T29DP_80D	T29DP	DP SDRVB AUXCH C P	
	T29DP_80D	T29DP	DP SDRVB AUXCH C N	
	T29DP_80D	T29DP	T29DPB ML P<3..0>	
	T29DP_80D	T29DP	T29DPB ML N<3..0>	
	T29DP_80D	T29DP	T29DPB ML C P<3..0>	
	T29DP_80D	T29DP	T29DPB ML C N<3..0>	
	T29DP_80D	T29DP	DP B EXT AUXCH P	
	T29DP_80D	T29DP	DP B EXT AUXCH N	

Only used on dual-port hosts.

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T29 Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	6 31 45 48 54 55
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	6 31 45 48 54 55
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	6 31 45 48 51 80
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	6 31 45 48 51 80
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 45 48 63 64
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 45 48 63 64
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	45 48 103 104
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	45 48 103 104

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	64
	1TO1_DIFFPAIR		CHGR_CSI_N	64
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	64
	1TO1_DIFFPAIR		CHGR_CSO_N	64

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=2x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 0.127 mm. Pairs should be within 0.508mm of entire channel.
DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
Max length of LVDS/DisplayPort/TMDS traces: 13 inches.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK P	76 77
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB A0 CLK N	76 77
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK P	76 77
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB A1 CLK N	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 A<8..0>	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 A<8..0>	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 ABI L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 ABI L	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 RAS L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 RAS L	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CAS L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CAS L	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 WE L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 WE L	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CKE L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CKE L	76 77
FB_A0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A0 CS L	76 77
FB_A1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB A1 CS L	76 77
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<0>	76 77
L293 FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<1>	76 77
L292 FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<2>	76 77
L290 FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB A0 EDC<3>	76 77
L295 FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<0>	76 77
L297 FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<1>	76 77
L298 FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<2>	76 77
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB A1 EDC<3>	76 77
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<0>	76 77
L299 FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<1>	76 77
L384 FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<2>	76 77
L383 FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A0 DBI L<3>	76 77
L382 FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<0>	76 77
L381 FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<1>	76 77
L380 FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<2>	76 77
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB A1 DBI L<3>	76 77
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<0>	76 77
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<0>	76 77
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK P<1>	76 77
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB A0 WCLK N<1>	76 77
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<0>	76 77
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<0>	76 77
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK P<1>	76 77
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB A1 WCLK N<1>	76 77
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<7..0>	76 77
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<15..8>	76 77
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<23..16>	76 77
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A0 DQ<31..24>	76 77
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<7..0>	76 77
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<15..8>	76 77
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<23..16>	76 77
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB A1 DQ<31..24>	76 77
FB_AB_RESET	GDDR5_45R50SE	GDDR5_CMD	FB RESET L	76 77 78

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK P	76 78
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB B0 CLK N	76 78
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK P	76 78
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB B1 CLK N	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 A<8..0>	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 A<8..0>	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 ABI L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 ABI L	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 RAS L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 RAS L	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 CAS L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 CAS L	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 WE L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 WE L	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 CKE L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 CKE L	76 78
FB_B0_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B0 CS L	76 78
FB_B1_CMD	GDDR5_45R50SE	GDDR5_CMD	FB B1 CS L	76 78
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<0>	76 78
L308 FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<1>	76 78
L306 FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<2>	76 78
L307 FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB B0 EDC<3>	76 78
L313 FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<0>	76 78
L309 FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<1>	76 78
L308 FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<2>	76 78
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB B1 EDC<3>	76 78
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<0>	76 78
L311 FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<1>	76 78
L312 FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<2>	76 78
L314 FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B0 DBI L<3>	76 78
L316 FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<0>	76 78
L315 FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<1>	76 78
L317 FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<2>	76 78
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB B1 DBI L<3>	76 78
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<0>	76 78
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<0>	76 78
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK P<1>	76 78
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB B0 WCLK N<1>	76 78
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<0>	76 78
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<0>	76 78
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK P<1>	76 78
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB B1 WCLK N<1>	76 78
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<7..0>	76 78
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<15..8>	76 78
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<23..16>	76 78
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B0 DQ<31..24>	76 78
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<7..0>	76 78
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<15..8>	76 78
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<23..16>	76 78
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB B1 DQ<31..24>	76 78

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LVDS_A_CLK	LVDS_85D	LVDS	LVDS A CLK P	84 88
LVDS_A_CLK	LVDS_85D	LVDS	LVDS A CLK N	84 88
LVDS_A_DATA	LVDS_85D	LVDS	LVDS A DATA P<2..0>	84 88
LVDS_A_DATA	LVDS_85D	LVDS	LVDS A DATA N<2..0>	84 88
LVDS_B_CLK	LVDS_85D	LVDS	LVDS B CLK P	84 88
LVDS_B_CLK	LVDS_85D	LVDS	LVDS B CLK N	84 88
LVDS_B_DATA	LVDS_85D	LVDS	LVDS B DATA P<2..0>	84 88
LVDS_B_DATA	LVDS_85D	LVDS	LVDS B DATA N<2..0>	84 88
	LVDS_85D	LVDS	LVDS CONN A CLK F P	6 83
	LVDS_85D	LVDS	LVDS CONN A CLK F N	6 83
	LVDS_85D	LVDS	LVDS CONN B CLK F P	6 83
	LVDS_85D	LVDS	LVDS CONN B CLK F N	6 83
	LVDS_85D	LVDS	LVDS CONN A CLK P	83 84
	LVDS_85D	LVDS	LVDS CONN A CLK N	83 84
	LVDS_85D	LVDS	LVDS CONN A DATA P<2..0>	6 83 84
	LVDS_85D	LVDS	LVDS CONN A DATA N<2..0>	6 83 84
	LVDS_85D	LVDS	LVDS CONN B CLK P	83 84
	LVDS_85D	LVDS	LVDS CONN B CLK N	83 84
	LVDS_85D	LVDS	LVDS CONN B DATA P<2..0>	6 83 84
	LVDS_85D	LVDS	LVDS CONN B DATA N<2..0>	6 83 84

Whistler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
GPU_CLK27M	CLK_SLOW_55S	CLK_SLOW	GPU CLK27M	79 80
GPU_CLK100M	CLK_SLOW_55S	CLK_SLOW	GPU CLK100M	79 80
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS EG A CLK P	79 88
LVDS_EG_A_CLK	LVDS_85D	LVDS	LVDS EG A CLK N	79 88
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS EG A DATA P<2..0>	79 88
LVDS_EG_A_DATA	LVDS_85D	LVDS	LVDS EG A DATA N<2..0>	79 88
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_P<3>	79 80
LVDS_EG_A_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_A_DATA_N<3>	79 80
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS EG B DATA P<2..0>	79 88
LVDS_EG_B_DATA	LVDS_85D	LVDS	LVDS EG B DATA N<2..0>	79 88
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_P<3>	79 80
LVDS_EG_B_DATA3	LVDS_85D	LVDS	NC_LVDS_EG_B_DATA_N<3>	79 80
DP_MI	DP_85D	DISPLAYPORT	DP EXTA ML C P<3..0>	79 85
	DP_85D	DISPLAYPORT	DP EXTA ML C N<3..0>	79 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EXTA AUXCH C P	84 85
	DP_85D	DISPLAYPORT	DP EXTA AUXCH C N	84 85
DP_AUX_CH	DP_85D	DISPLAYPORT	DP EG AUX CH P	79 84
	DP_85D	DISPLAYPORT	DP EG AUX CH N	79 84

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GPU (Whistler) CONSTRAINTS

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_85D	BGA	LVDS_85D
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K92 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	49 65
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	49 65
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_P	49
	SENSE_1TO1_55S	SENSE	VCCSAISNS_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	49
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	49 70
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	49 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_P	49
	SENSE_1TO1_55S	SENSE	CPUVCCIOISNS_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUISENS_N	49
	SENSE_1TO1_55S	SENSE	GPUISENS_P	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	49 67
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	49 67
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	31 103
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	31 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	41 103
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	41 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	89 103
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	89 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	41 103
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	41 103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	50 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	50 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	50 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_P	50
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_R_N	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V8_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_PP1V5_S0GPU_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	103
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	103
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	103
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	BI_MIC_P	61 62
			BI_MIC_N	61 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	58 60
	AUDIODIFF	AUDIO	AUD_LO1_R_N	58 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	57 60
	AUDIODIFF	AUDIO	AUD_LO2_R_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	57 60
	AUDIODIFF	AUDIO	AUD_LO3_R_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	57 60
	AUDIODIFF	AUDIO	AUD_LO3_L_N	57 60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INR_P	57 62
	AUDIODIFF	AUDIO	AUD_MIC_INR_N	57 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	57 62
	AUDIODIFF	AUDIO	AUD_MIC_INL_N	57 62
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_BL_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_BL_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_FL_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_FL_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_BR_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_BR_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_FR_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_FR_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LFE_IN_L_P	60
	AUDIODIFF	AUDIO	SPKRAMP_LFE_IN_L_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375BL_IN_P	60
	AUDIODIFF	AUDIO	SSM2375BL_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375FL_IN_P	60
	AUDIODIFF	AUDIO	SSM2375FL_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375BR_IN_P	60
	AUDIODIFF	AUDIO	SSM2375BR_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375FR_IN_P	60
	AUDIODIFF	AUDIO	SSM2375FR_IN_N	60
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SSM2375LFE_IN_P	60
	AUDIODIFF	AUDIO	SSM2375LFE_IN_N 60	

K92 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_P	6 32
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_N	6 32
PCIE_EXCARD_D2R	PCIE_85D	PCIE	PCIE_EXCARD_D2R_P	6 16 32
	PCIE_85D	PCIE	PCIE_EXCARD_D2R_N	6 16 32
PCIE_EXCARD_R2D	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_P	16 32
	PCIE_85D	PCIE	PCIE_EXCARD_R2D_C_N	16 32
PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P	6 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N	6 32
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 31
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 31
	1TO1_DIFFPAIR		CHGR_CSI_R_P	64
	1TO1_DIFFPAIR		CHGR_CSI_R_N	64
	1TO1_DIFFPAIR		CHGR_CSO_R_P	50 64
	1TO1_DIFFPAIR		CHGR_CSO_R_N	50 64
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	42
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	42
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	42
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
(USB_EXTB)	USB_85D	USB	USB_LT2_P	42
	USB_85D	USB	USB_LT2_N	42
USB_EXCARD	USB_85D	USB	USB_EXCARD_P	8 24 32
	USB_85D	USB	USB_EXCARD_N	8 24 32
USB_EXCARD	USB_85D	USB	USB2_EXCARD_CONN_P	6 32
	USB_85D	USB	USB2_EXCARD_CONN_N	6 32
(USB_EXTC)	USB_85D	USB	USB_LT3_P	43
	USB_85D	USB	USB_LT3_N	43
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
		SB_POWER	PP3V3_S5	48 56 71 72 73 83 86 91 102 104 6 7 17 19 20 22 23 24 25 39 46
		SB_POWER	PP3V3_S0	63 62 72 73 80 83 84 86 88 89 6 7 12 23 24 26 29 32 35 36 39 40 41 46 48 49 50 51 52 54 57 91 102
		SB_POWER	PP1V5_S3RS0	7 72 104
		GND	GND	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 51
	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	51
	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	51 79
	THERM_1TO1_55S	THERM	GPU_TDIODE_N	51 79
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	33 51
	THERM_1TO1_55S	THERM	T29_THERMD_N	51

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K91 does not have

SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_P	104
	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S3_N	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP3V3_S5_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S3_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0PCH_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP1V05_S0PCH_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_N	104
	SENSE_1TO1_55S	SENSE	ISNS_PP5V_S0_P	104
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_DDR_N	104
	SENSE_1TO1_55S	SENSE	ISNS_CPU_DDR_P	104

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K92 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.095 MM			
37_OHM_SE	*	Y	0.155 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.13 MM	0.13 MM			
45_OHM_SE	*	Y	0.099 MM	0.099 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL9,ISL10	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.154 MM	0.154 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.110 MM	0.090 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.090 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.102 MM	0.090 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.090 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

NOTE: Based on K92 mlb stackup.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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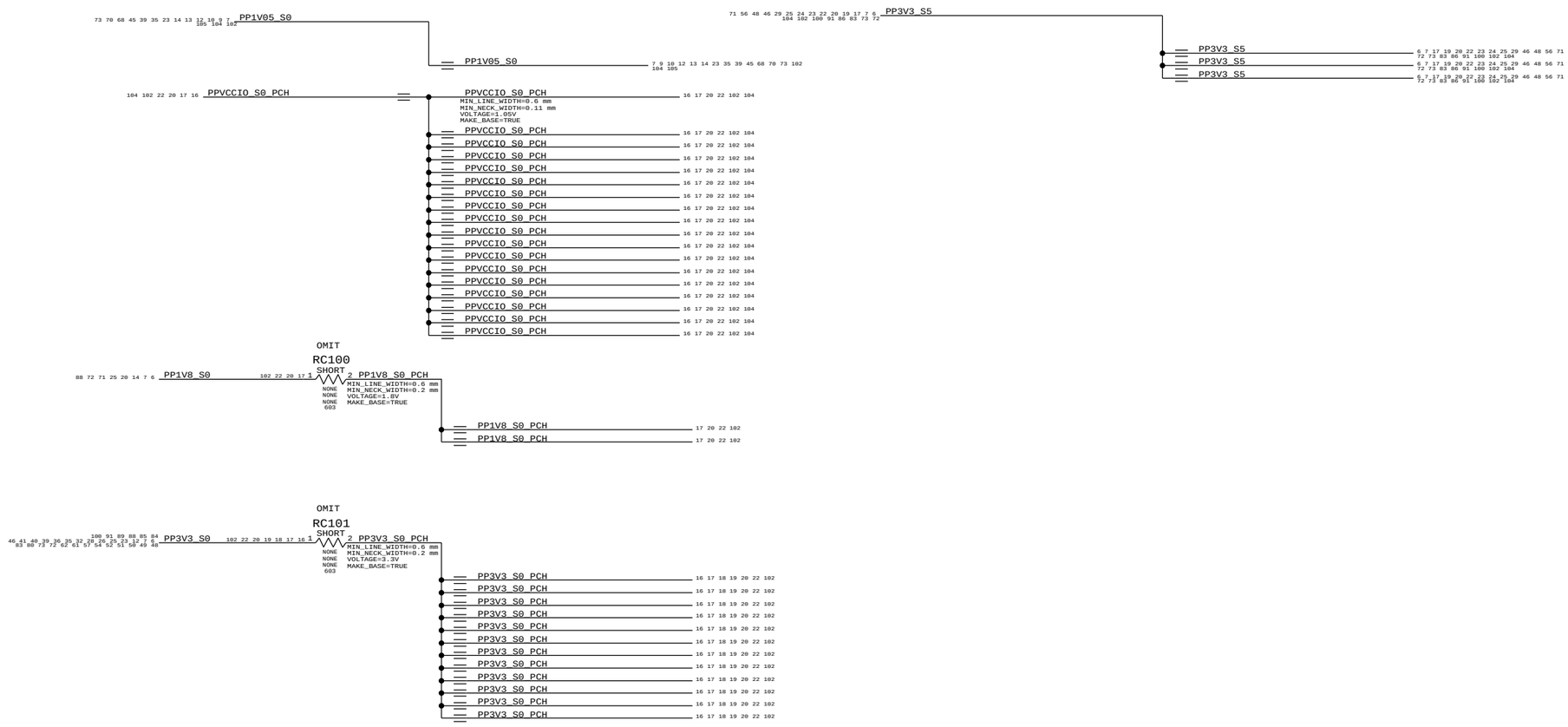
PCH "S5" Rail



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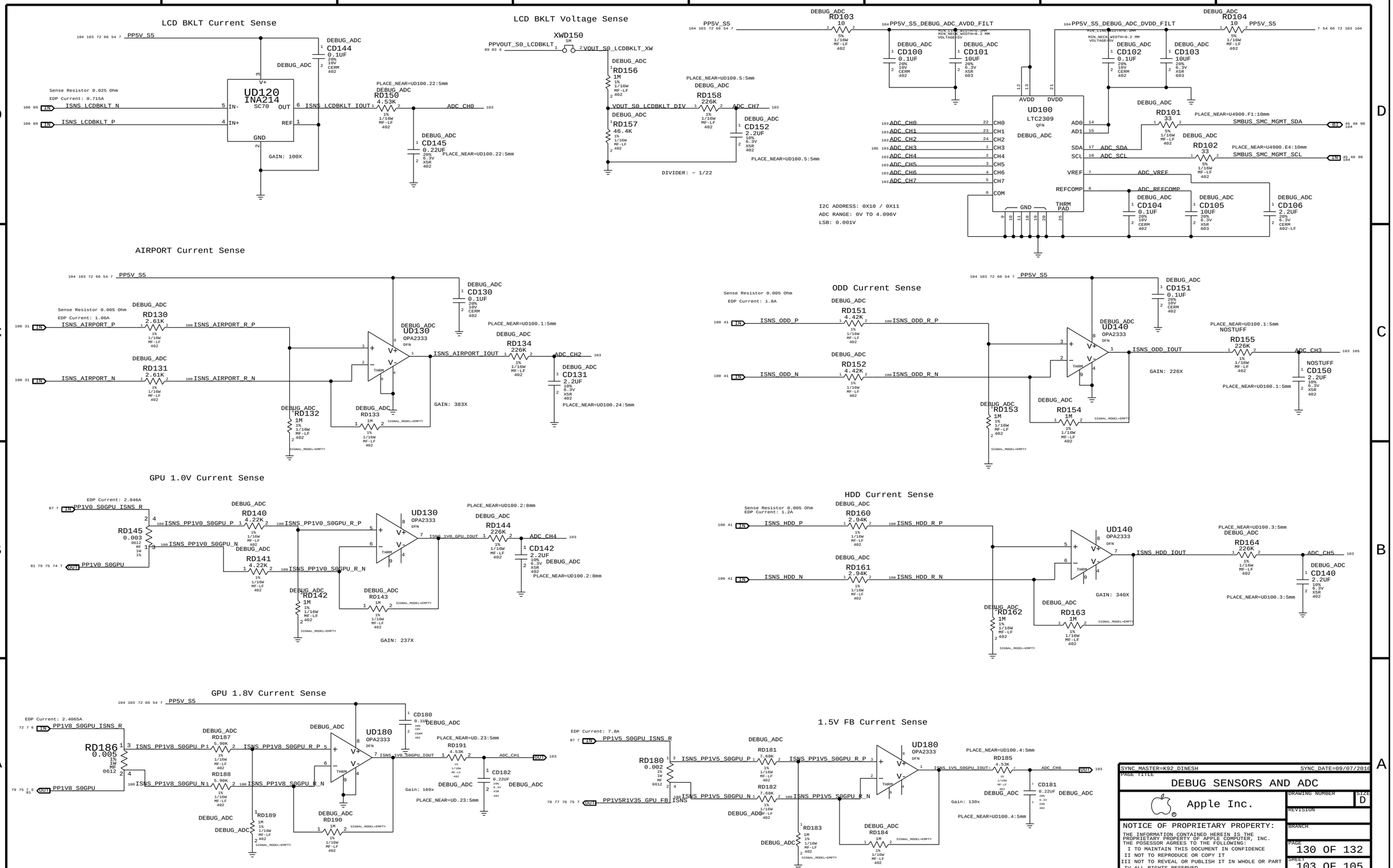

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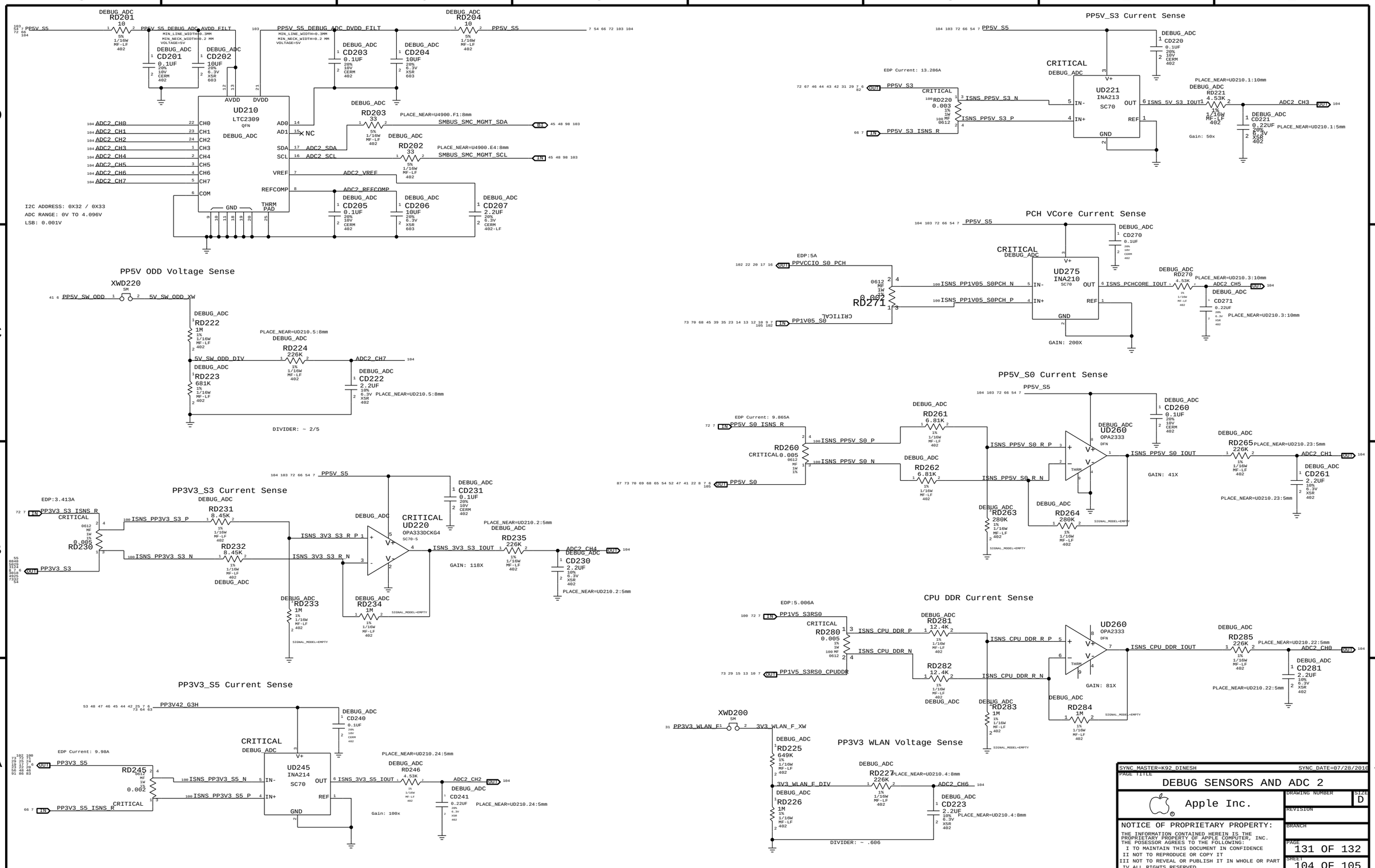

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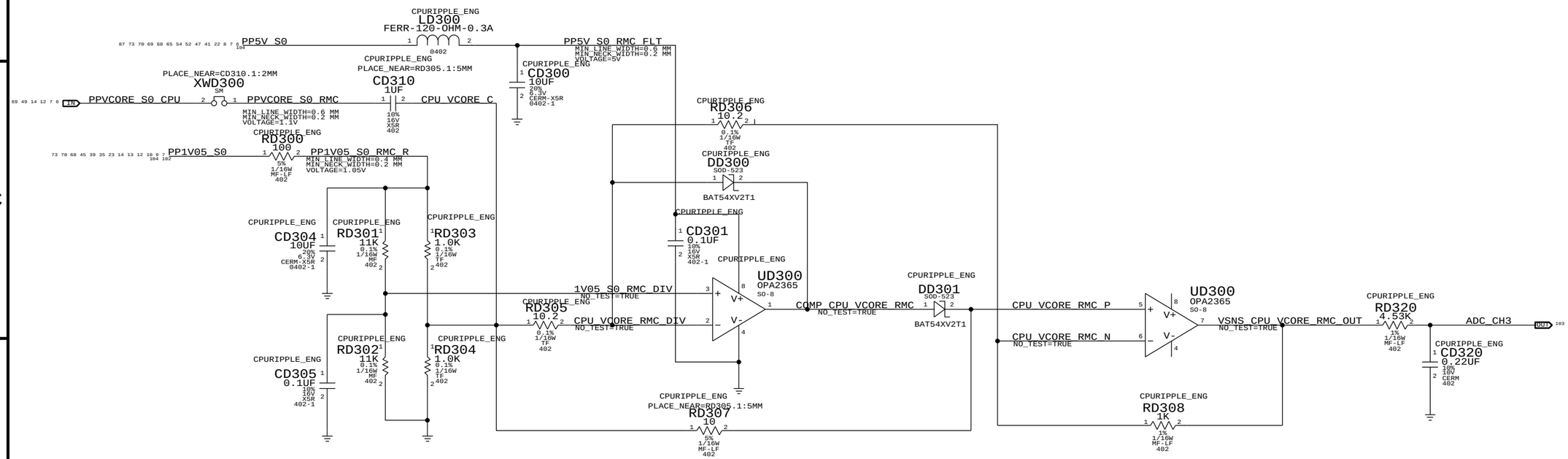

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