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Suzhou_L

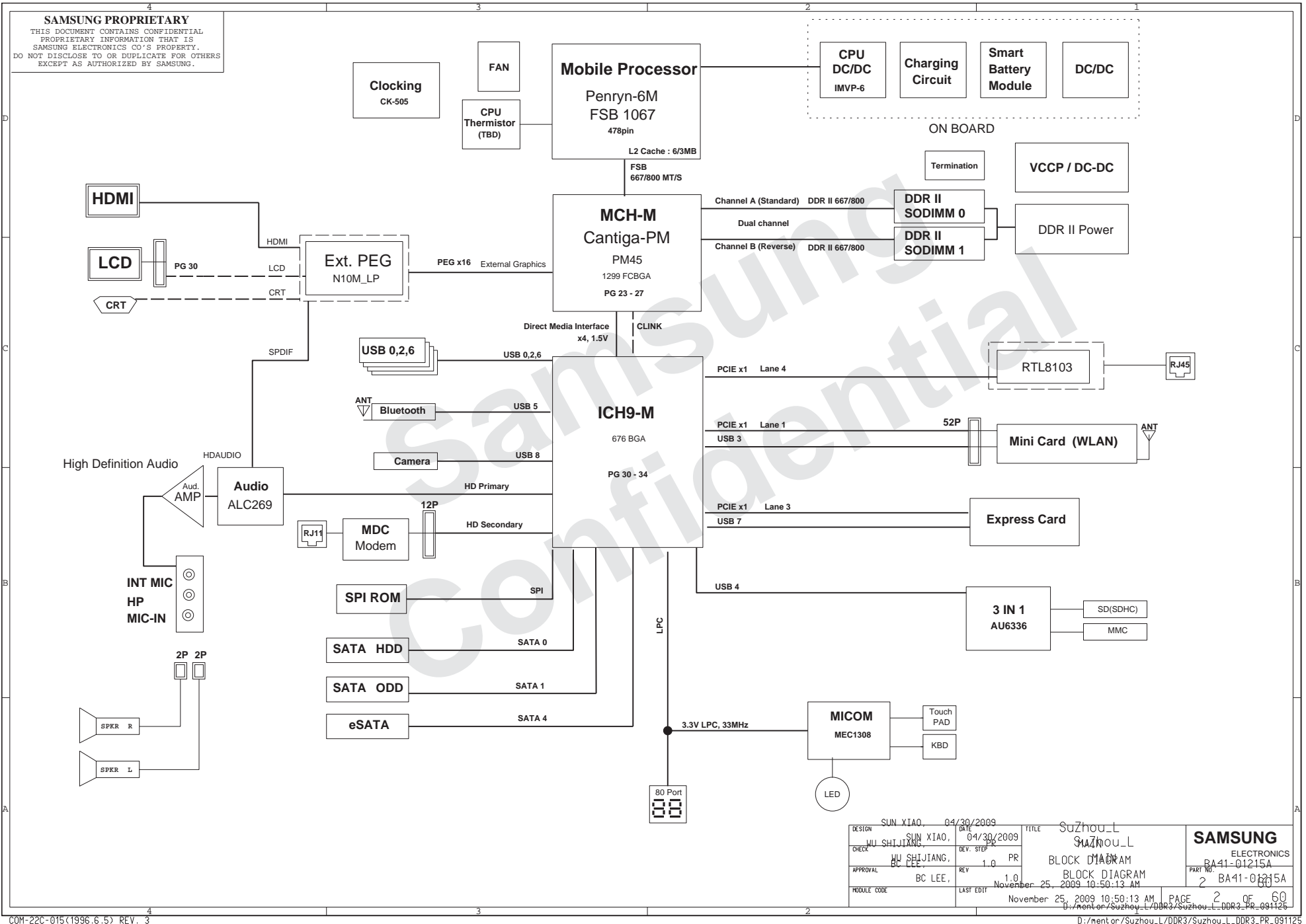
CPU : Intel Penryn
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

Model Name : Suzhou_L_DDR3
PCB Code : GCE BA41-01215A
NY BA41-01217A
HAN BA41-01216A

Dev. Step : P R
Revision : 1.0
T.R. Date : 2009.08.16

DESIGN	CHECK	APPROVAL

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_L	SAMSUNG
CHECK	WU SHIJIANG,	DEV. STEP	PR			ELECTRONICS
APPROVAL	BC LEE,	REV	1.0	COVER		PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	1	OF 60



BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	F
GLAN	-	-	F

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	RealTek 88E8057

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	0	NC
1	SYSTEM PORT 1	1	Mini Card 1 (WLAN)
2	SYSTEM PORT 2	2	NC
3	NC	3	LOM
4	NC	4	Mini Card 2 (ROBSON or DVB-T)
5	Bluetooth	5	NC
6	Mini PCI Express 2		
7	Camera		
8	NC		
9	NC		

PCI Express Assign

PORT #	ASSIGNED TO
0	NC
1	Mini Card 1 (WLAN)
2	NC
3	LOM
4	Mini Card 2 (ROBSON or DVB-T)
5	NC

(This table will be update.)

REVISION HISTORY

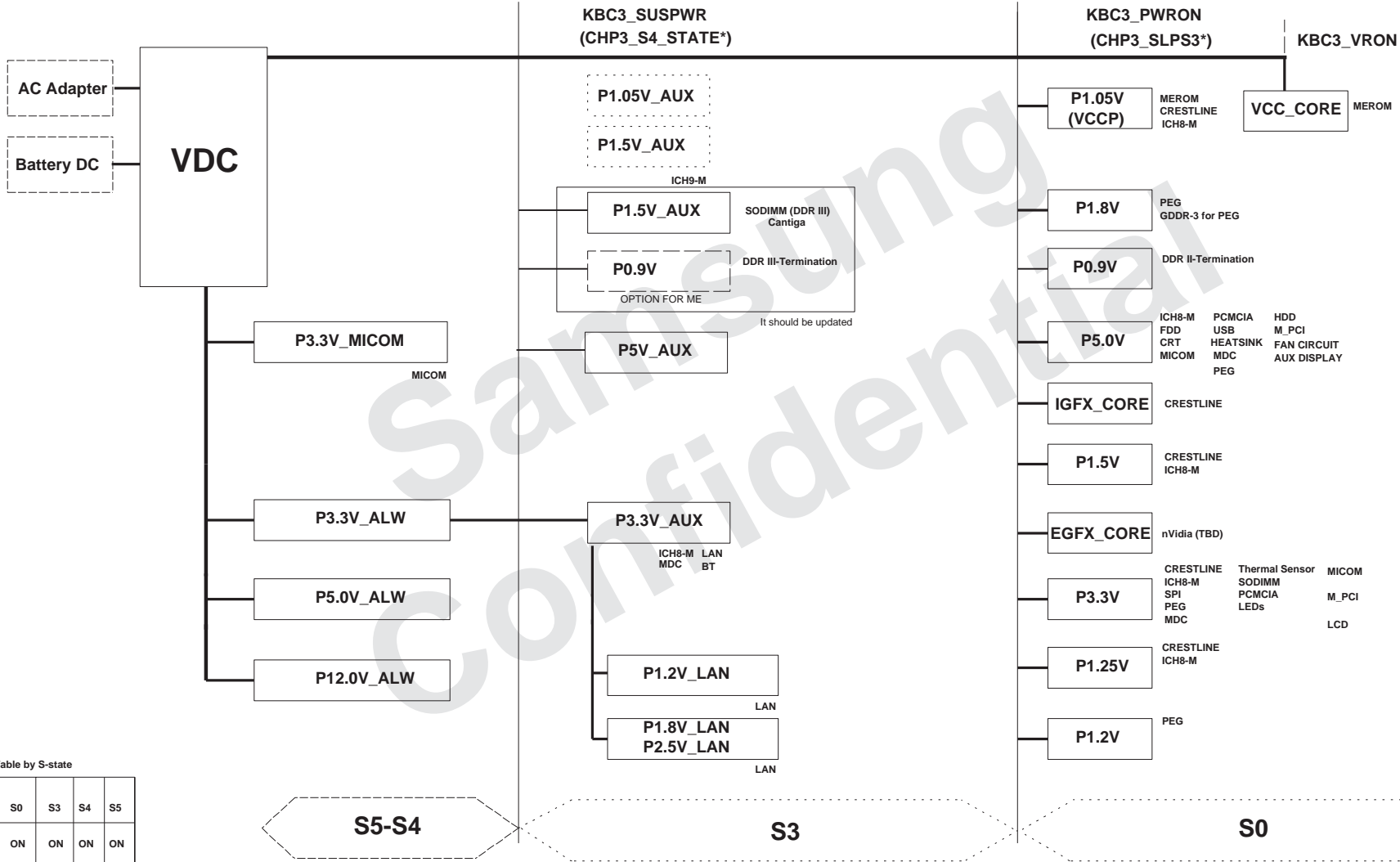
See rev notes for more information.

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_L	SAMSUNG ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR		MAIN	
APPROVAL	BC LEE,	REV	1.0		BCAFDINFO	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	3 OF 60	

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POWER DIAGRAM

Rev 0.1



Power On/Off Table by S-state

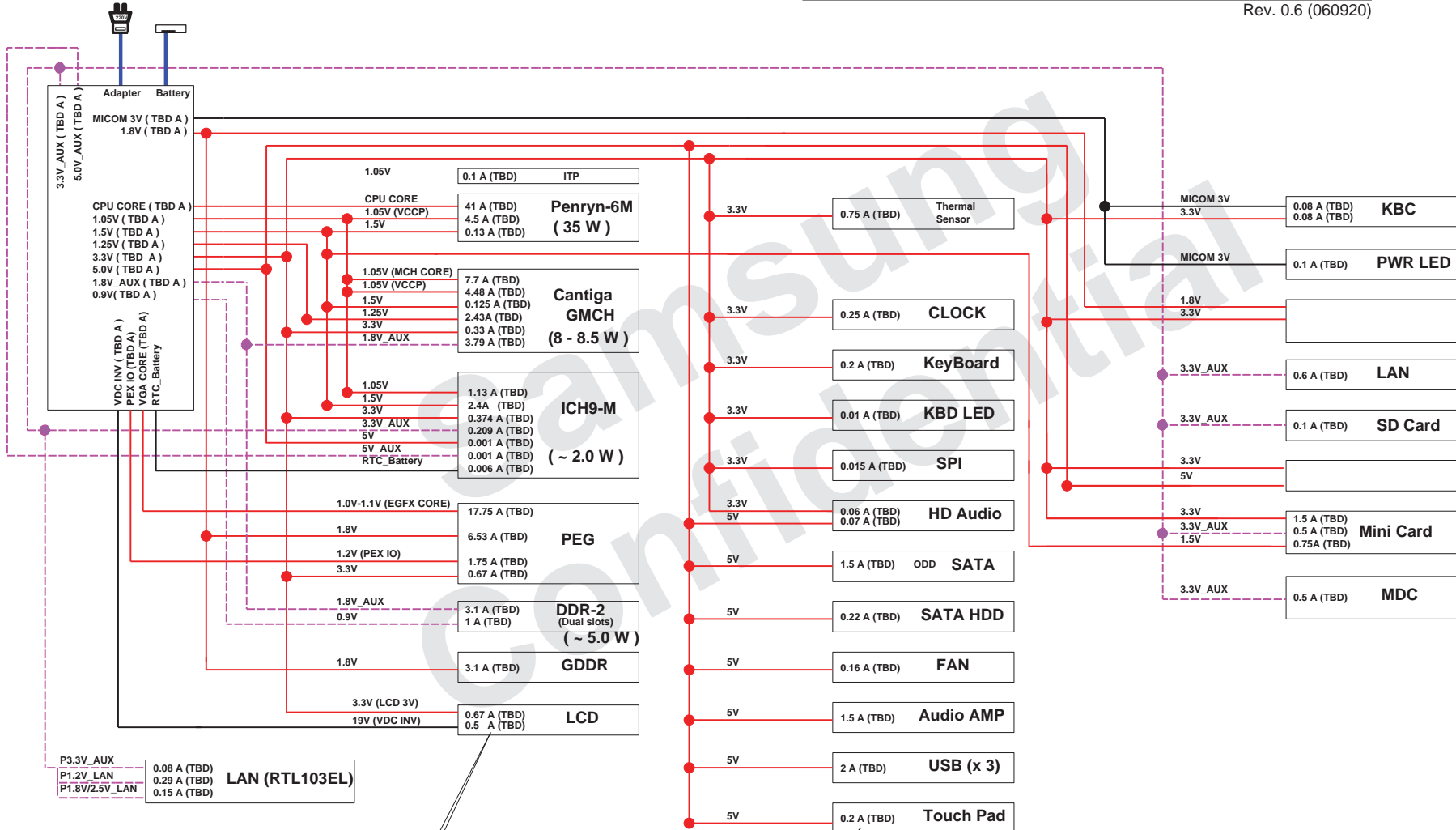
Rail	S0	S3	S4	S5
State	S0	S3	S4	S5
+V*(LWS)	ON	ON	ON	ON
+V*LAN	ON	ON	ON	ON
+1.8V_AUX	ON	ON	ON	ON
+0.9V	ON	ON	ON	ON
+V*AUX	ON	ON	ON	ON
+V	ON	ON	ON	ON
+V* (CORE)	ON	ON	ON	ON

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN	POWER DIAGRAM	
APPROVAL	BC LEE,	REV	1.0			
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POWER RAILS ANALYSIS

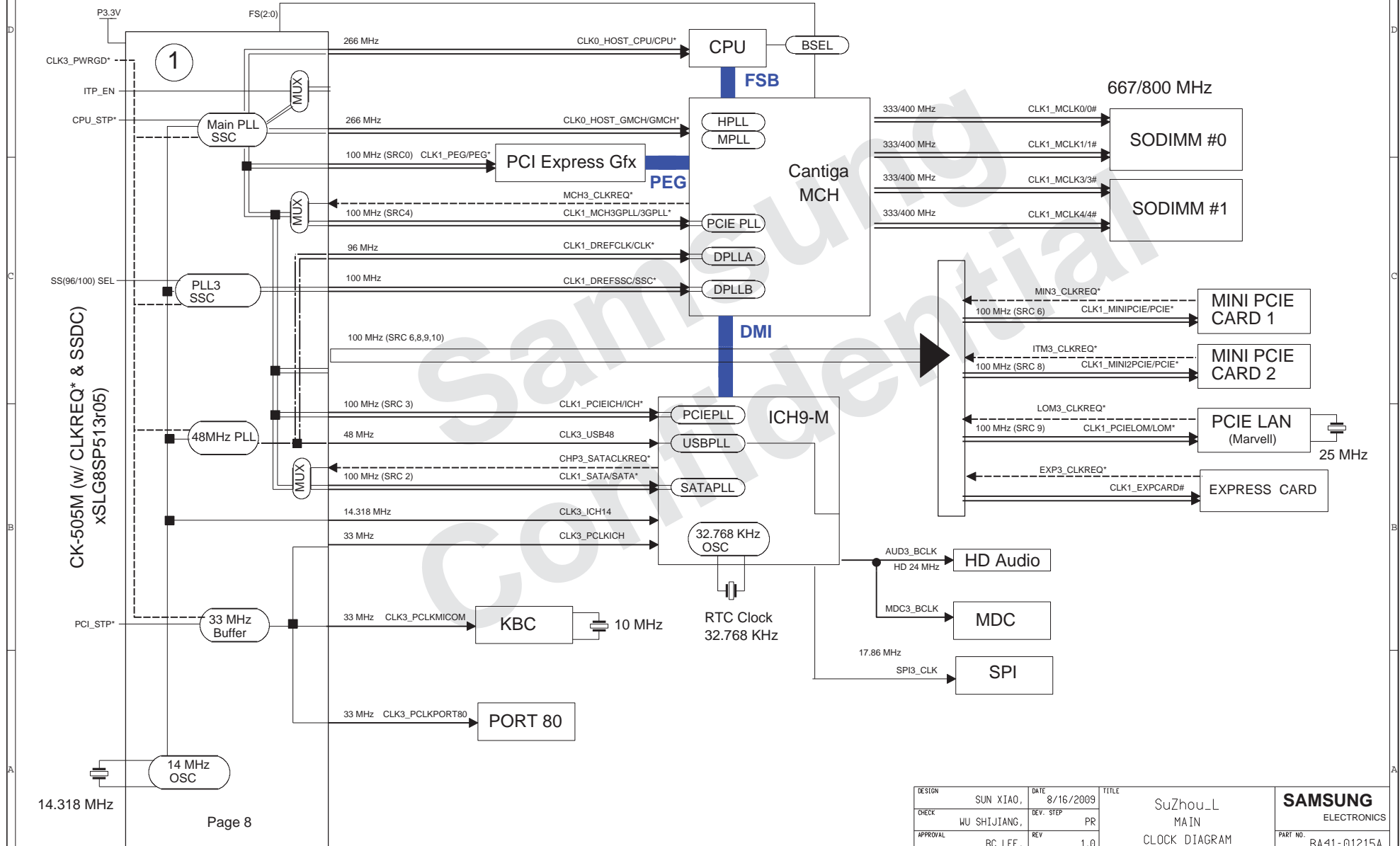
Rev. 0.6 (060920)



DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	SuZhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN	POWER RAILS	
APPROVAL	BC LEE,	REV	1.0			
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CLOCK DISTRIBUTION Rev. 0.1

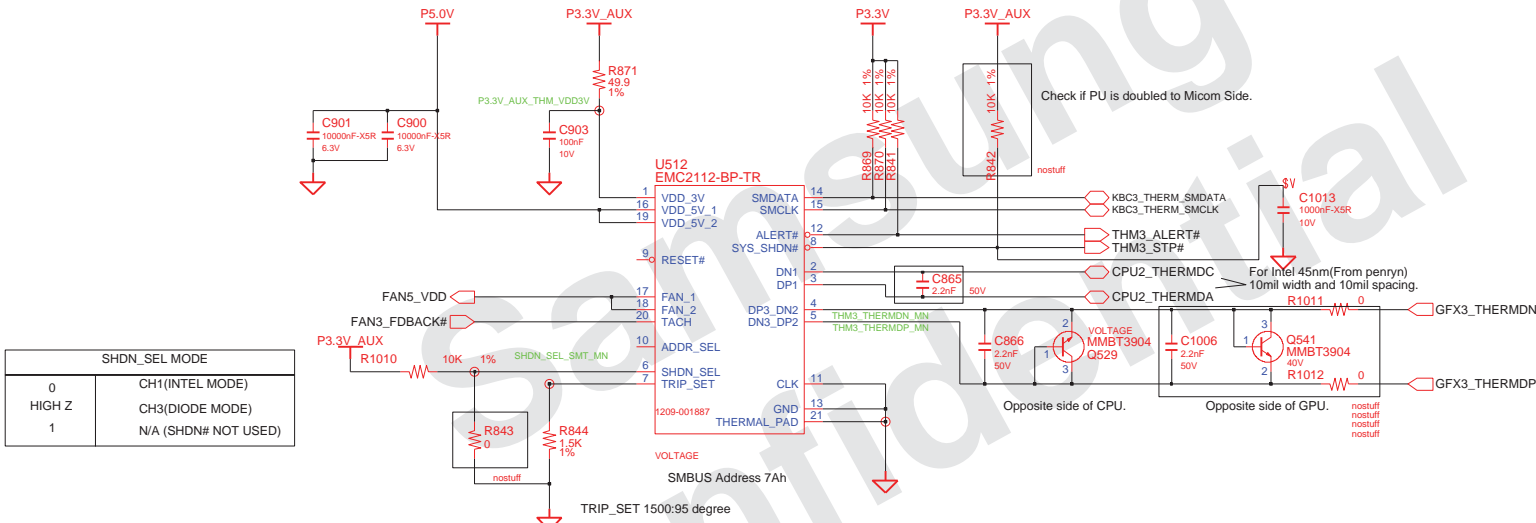


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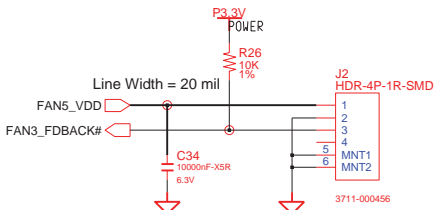
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CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	CLOCK DIAGRAM		
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	7 OF 60	

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THERMAL SENSOR & FAN CONTROL

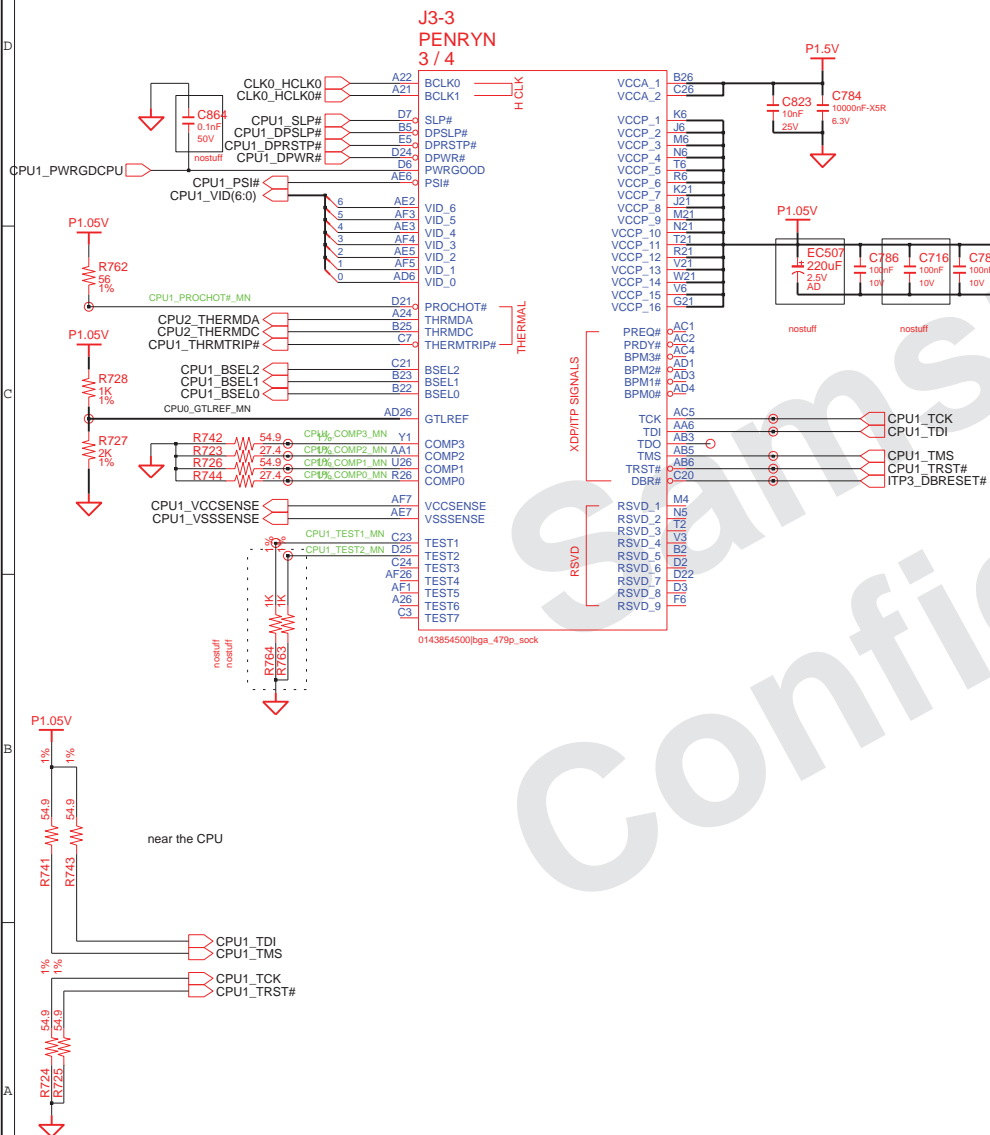


SHDN_SEL MODE	
0	CH1(INTEL MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)



DESIGN	SUN XIAO,	DATE	6/17/2008	TITLE	SuZhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		Thermal Sensor EMC2102	
APPROVAL	BC LEE,	REV	1.0			PART NO.
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			8A41-01215A
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CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 1 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 1	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 1 0 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 1 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 1 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 1 0 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 1 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 1 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 1 0 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 1 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 1 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 1 0 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 1	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 1 0	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 1	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 1 0 0 0	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 1	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 1 0	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 1	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 1 0 0	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 1	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				**11111111*: OV power good asserted.	
DPRSLPVR	Active	DPRSLPVR	Deeper Slp		
DPRSTP*	0	DPRSTP*	1		
PSI2*	0 or 1	PSI2*	0 or 1		

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5"
of the first GTLREF0 pin with Zo=55ohm trace.
Minimize coupling of any switching signals to this net.

COMP0.2(COMP1.3) should be connected with Zo=27.4ohm(55ohm)
trace shorter than 1/2" to their respective Banias socket pins.

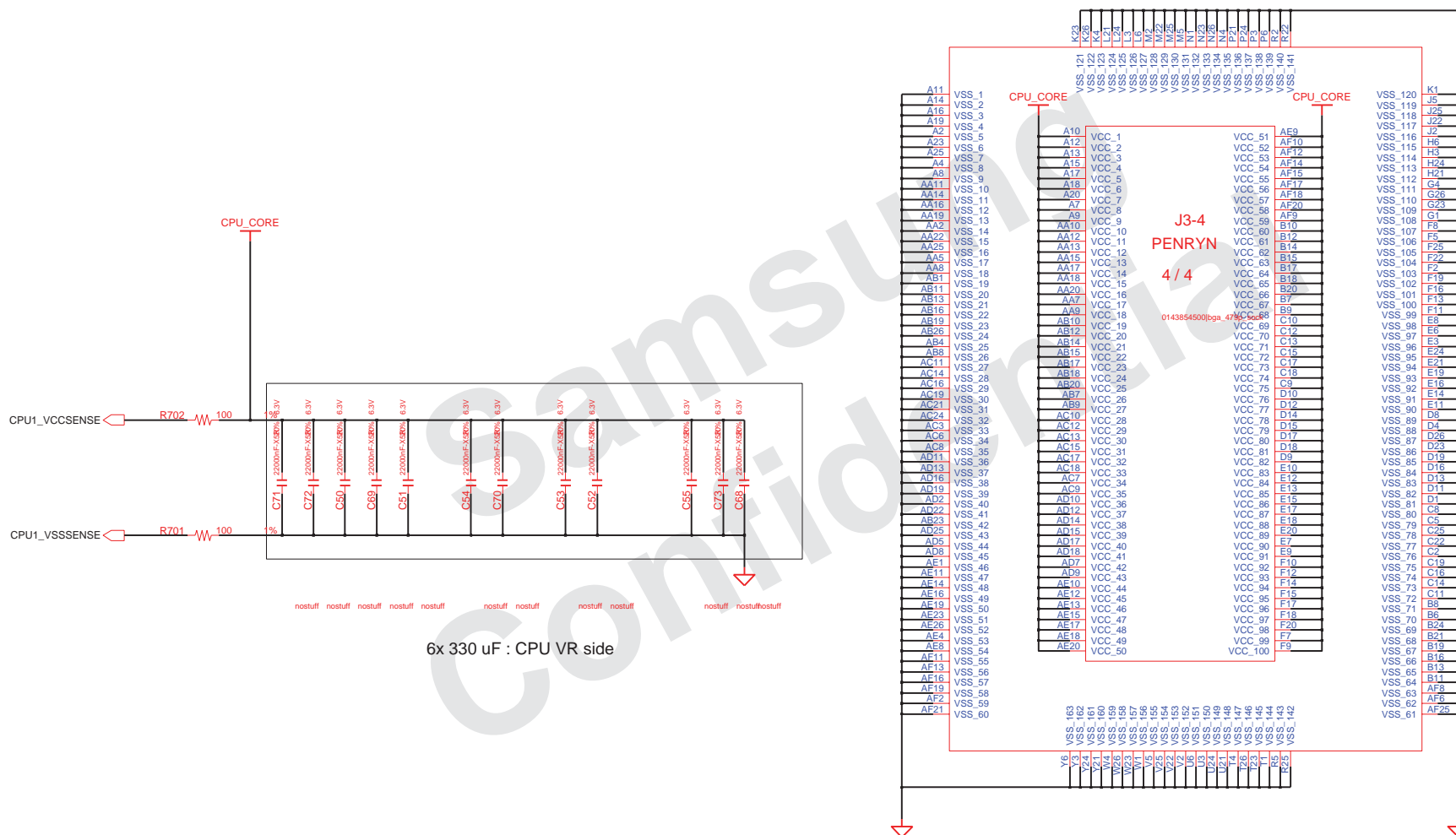
GND test points within 100mil of the VCC/VSSense at the end of the line.
Route the VCC/VSSense as a Zo=55ohm traces with equal length.
Observe 3:1 spacing b/w VCC/VSSense lines and 25mil away
(preferred 50mil) from any other signal. And GND via 100mil away
from each of the VCC/VSS test point vias.

BSEL

FSB 1067 MHz		Pull-down
FSB 800 MHz		BSEL0, BSEL1, BSEL2
		BSEL0, BSEL2

DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou.L	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		CPU	
APPROVAL	BC LEE,	REV	1.0		PENRYN (2/3)	PART NO. BA41-01215A
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	10	OF 60

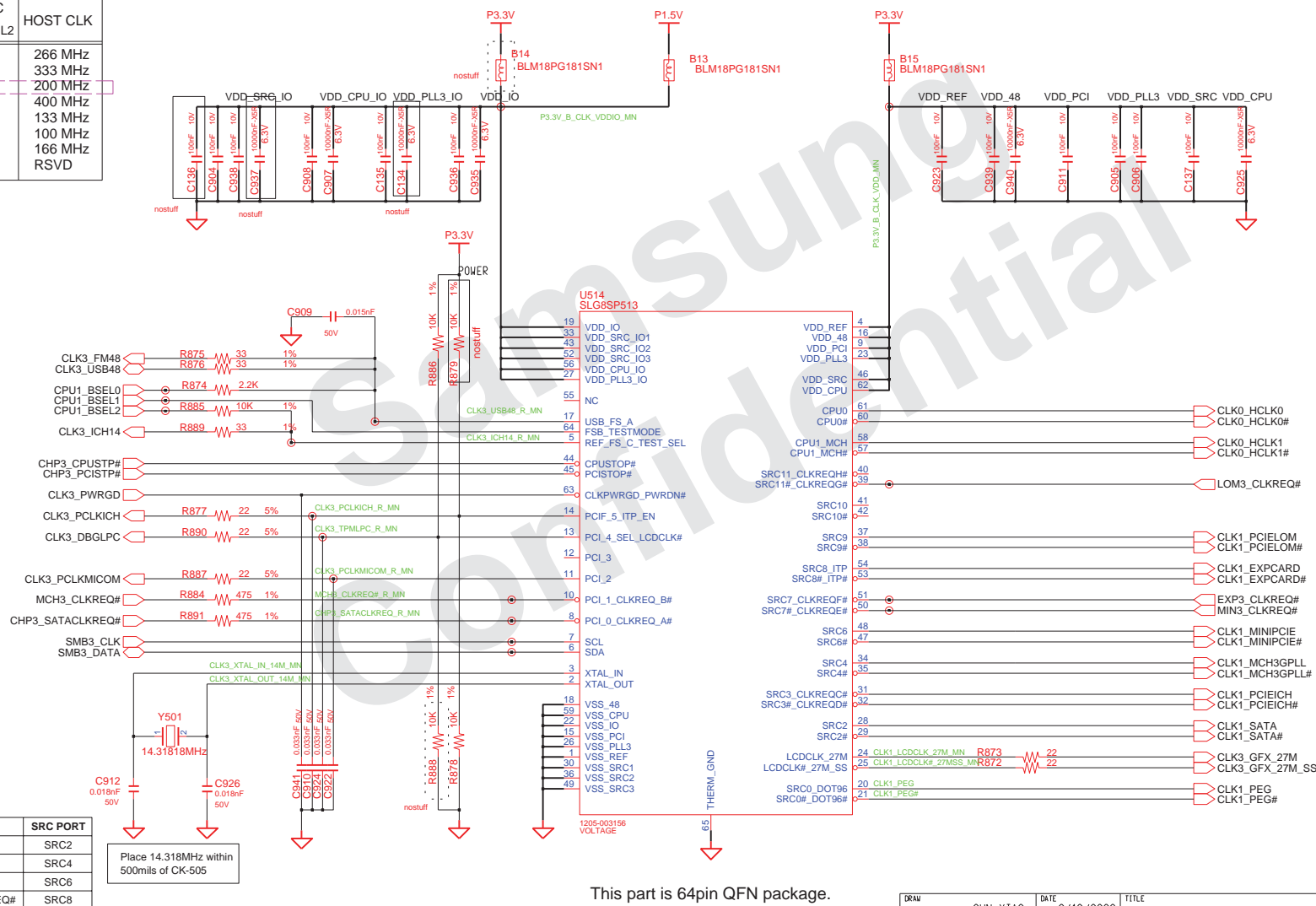
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DRWN	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou_L CPU PENRYN (3/3)	SAMSUNG ELECTRONICS	
CHECK	WU SHIJIANG,	DEV. STEP	PR				
APPROVAL	BC LEE,	REV	1.0				
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM				PAGE

CK505M

FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



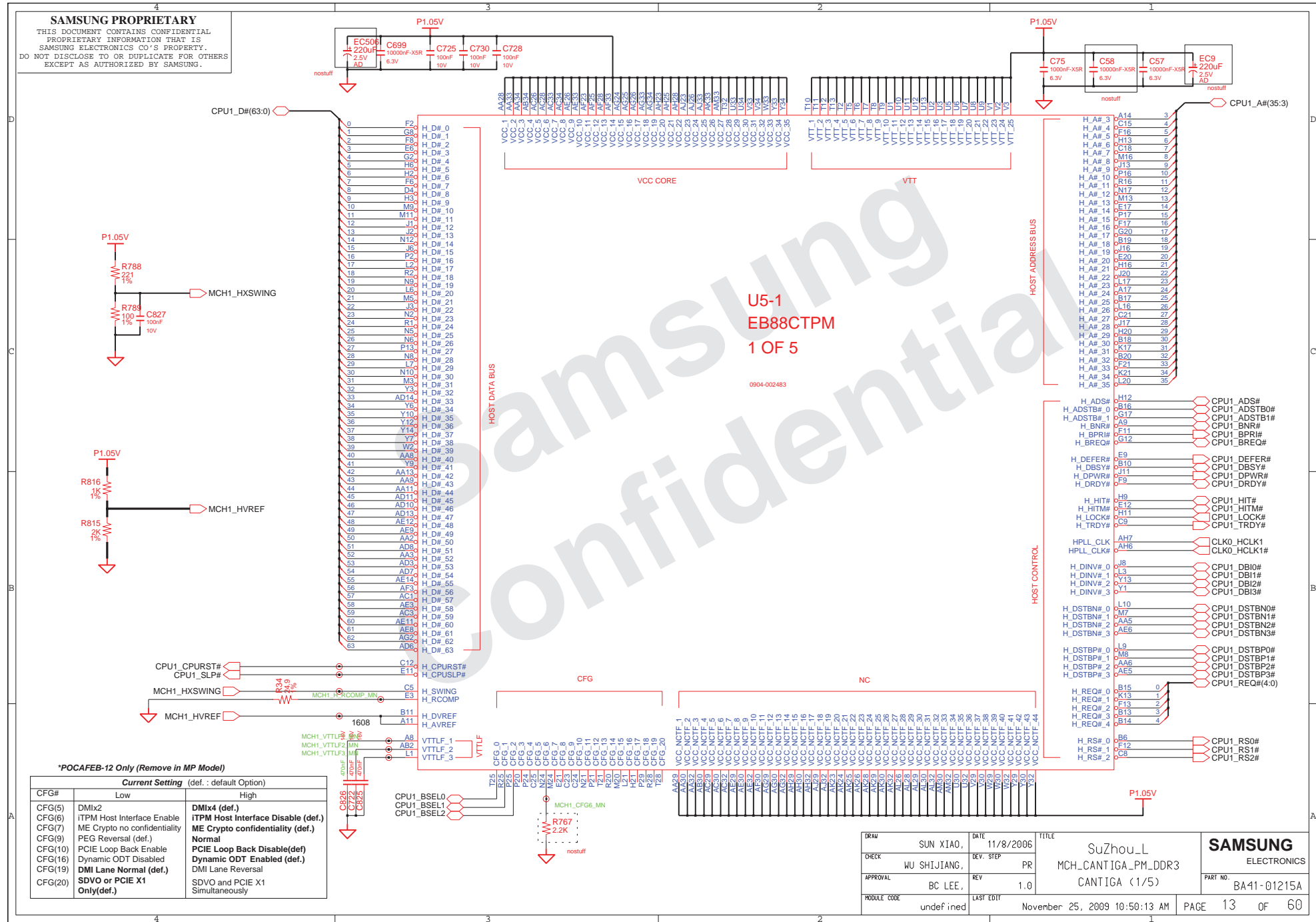
IDT: 1205-003159
SL: 1205-003533

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

DRAW	SUN XIAO,	DATE	8/12/2006	TITLE	SuZhou_L Main_Clock_Circuit CK_Clock_505M	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM			
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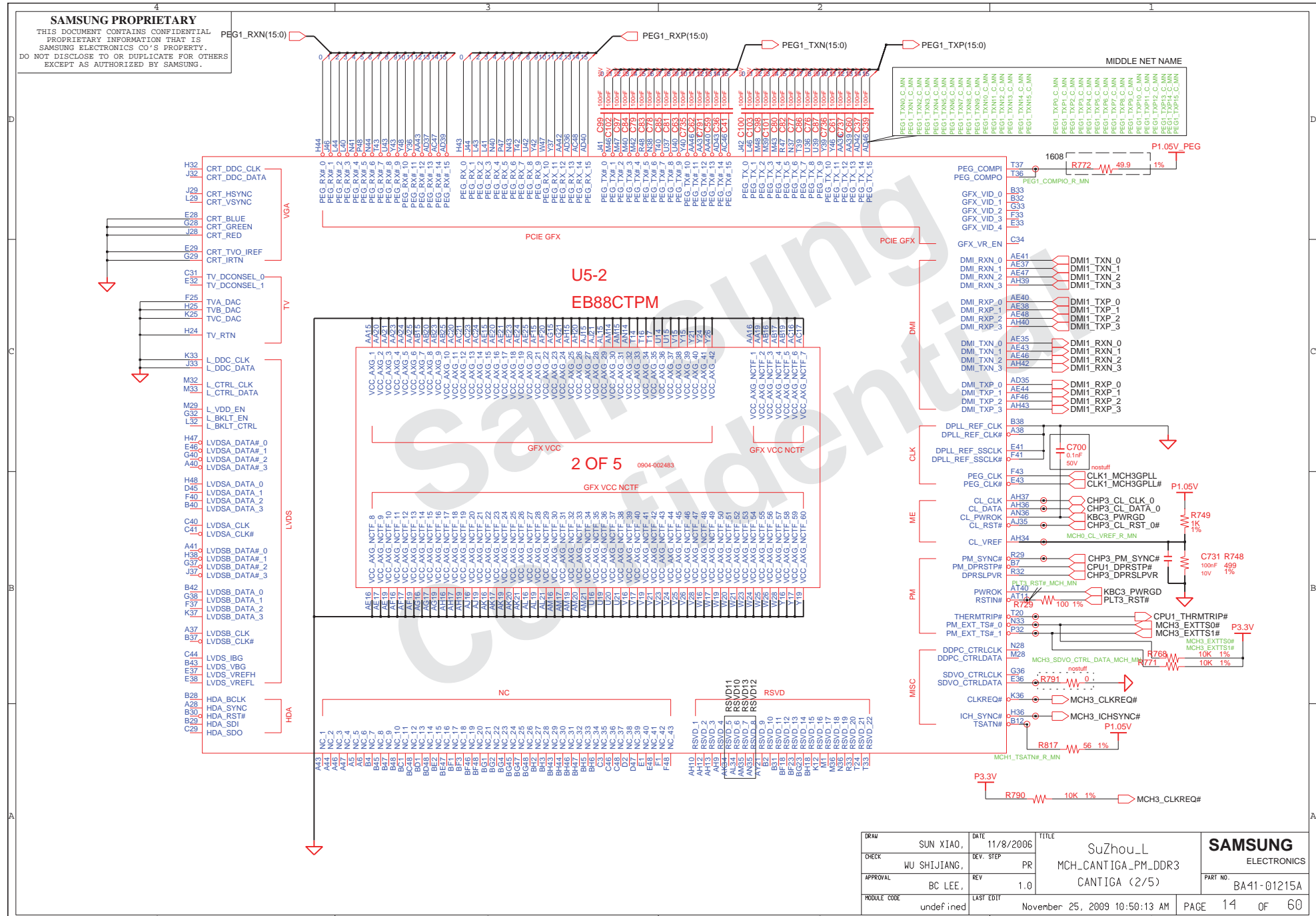


*POCAFEB-12 Only (Remove in MP Model)

CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	iTPM Host Interface Enable	iTPM Host Interface Disable (def.)
CFG(7)	ME Crypto no confidentiality	ME Crypto confidentiality (def.)
CFG(9)	PEG Reversal (def.)	Normal
CFG(10)	PCIe Loop Back Enable	PCIe Loop Back Disable(def)
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(19)	DMI Lane Normal (def.)	DMI Lane Reversal
CFG(20)	SDVO or PCIe X1 Only(def.)	SDVO and PCIe X1 Simultaneously

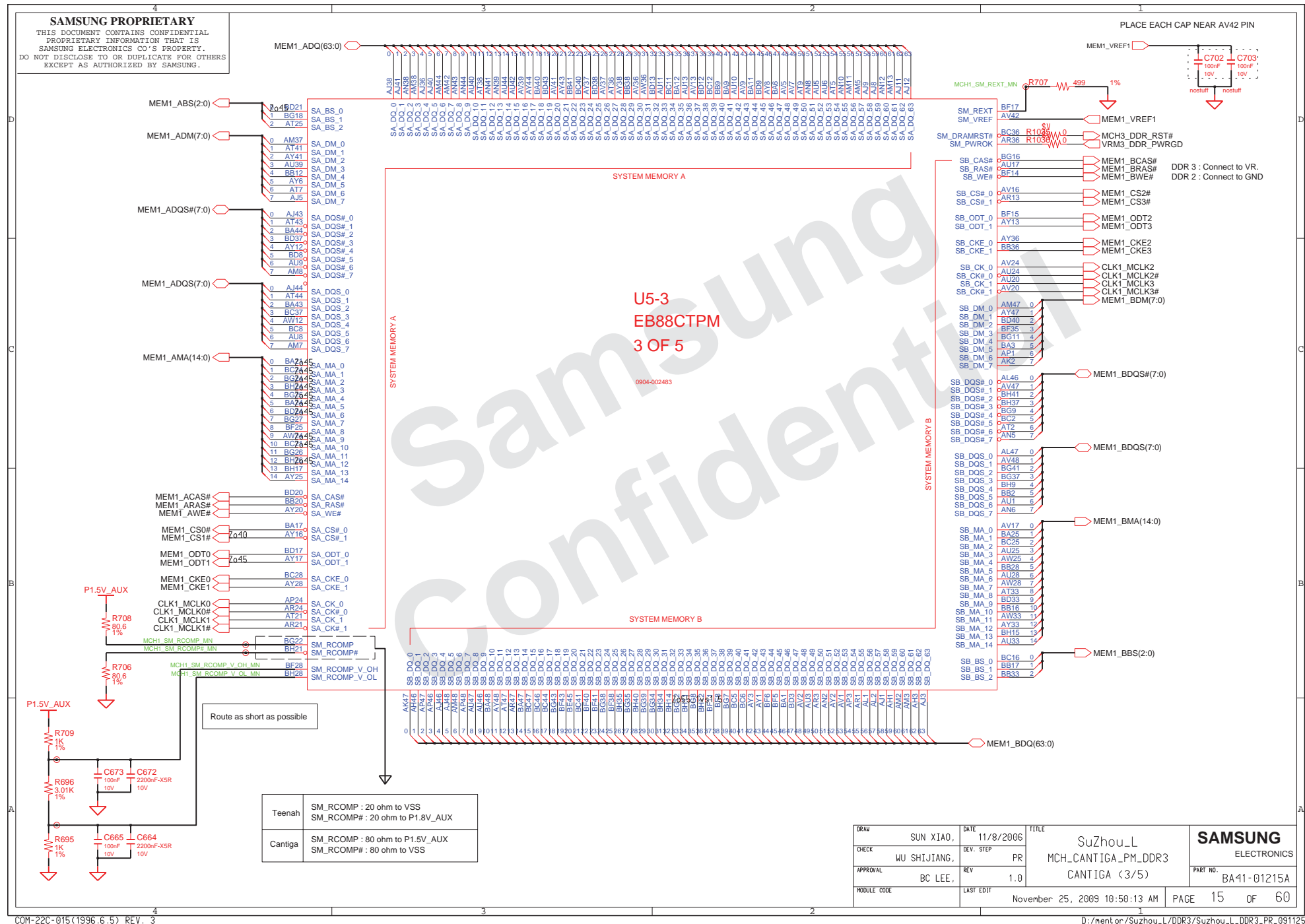
DATE	SUN XIAO,	11/8/2006	TITLE	SuZhou_L MCH_CANTIGA_PM_DDR3 CANTIGA (1/5)	SAMSUNG ELECTRONICS	
CHECK	WU SHIJIANG,	PR				DEV. STEP
APPROVAL	BC LEE,	1.0				REV
MODULE CODE			LAST EDIT	November 25, 2009 10:50:13 AM	PART NO.	BA41-01215A
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DATE	11/8/2006	TITLE	SuZhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG, PR	DEV. STEP	MCH_CANTIGA_PM_DDR3	
APPROVAL	BC LEE, REV	1.0	CANTIGA (2/5)	PART NO. BA41-01215A
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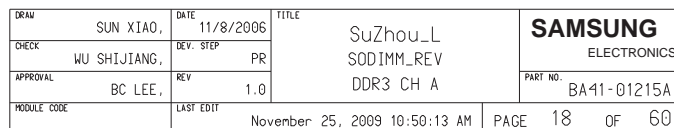


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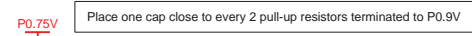


COM-22C-015(1996.6.5) REV. 3

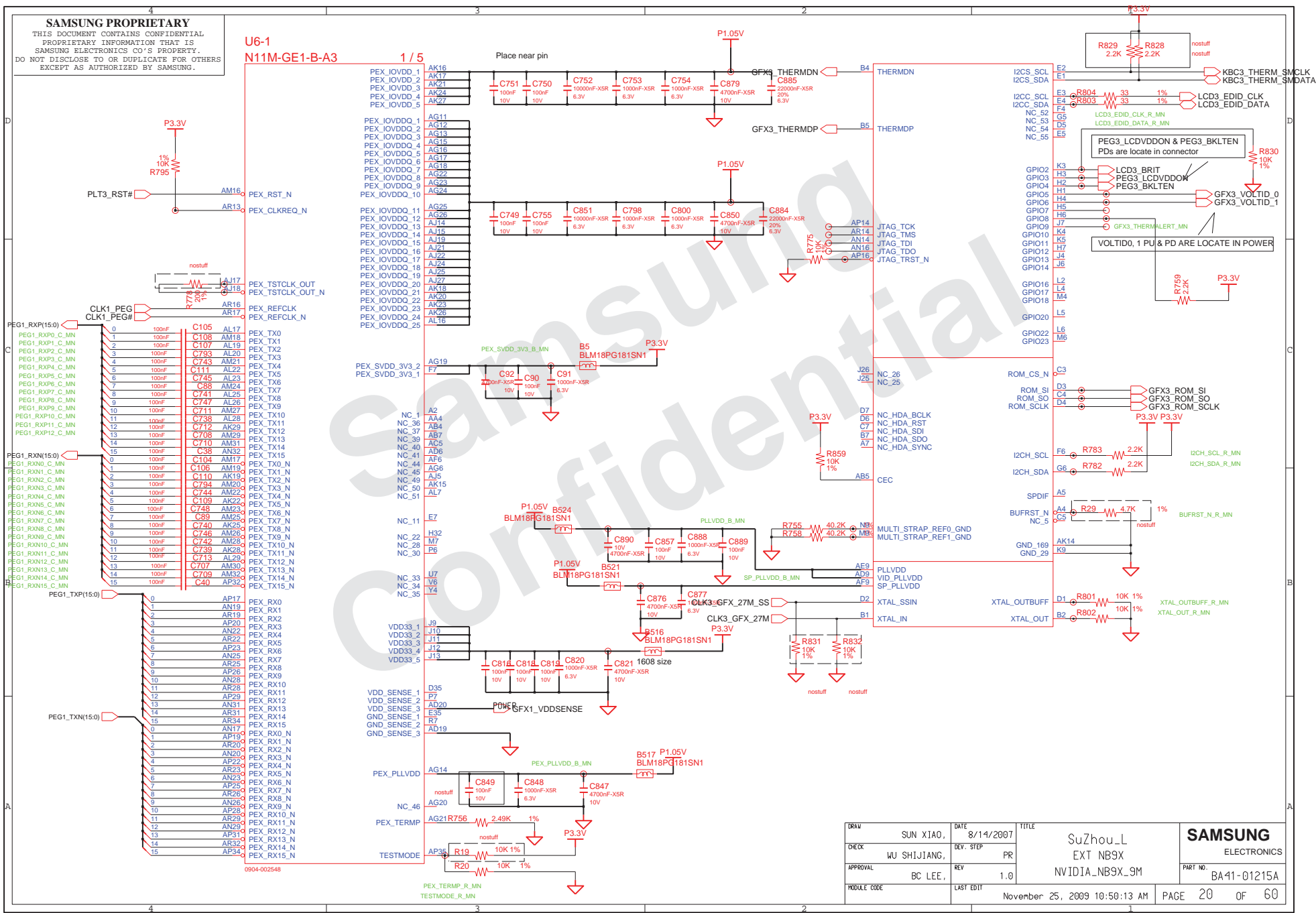
DDR SO-DIMM #0



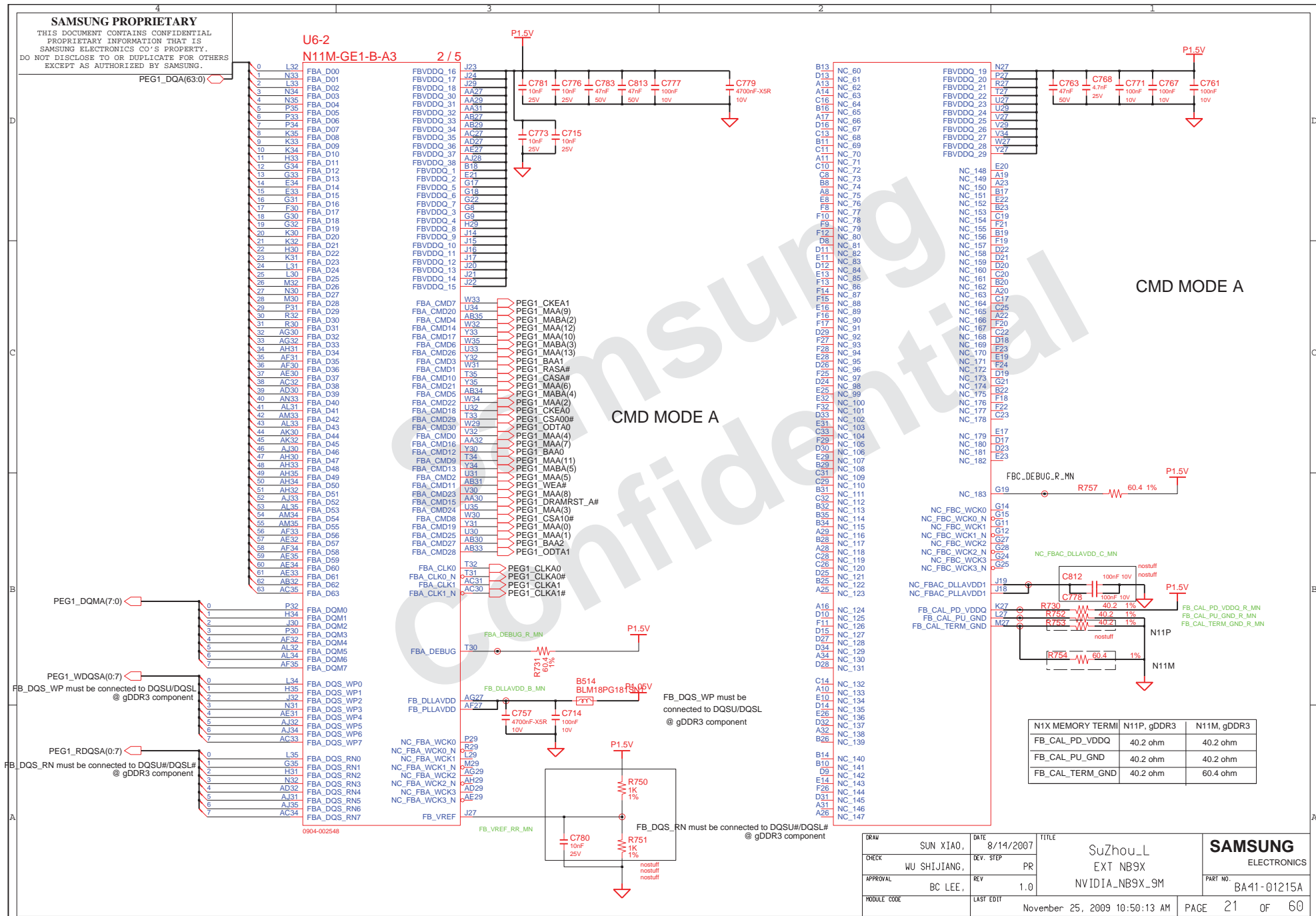
DDR SO-DIMM #1

D:/mentor/Suzhou I/DDR3/Suzhou I DDR3 PR 091125

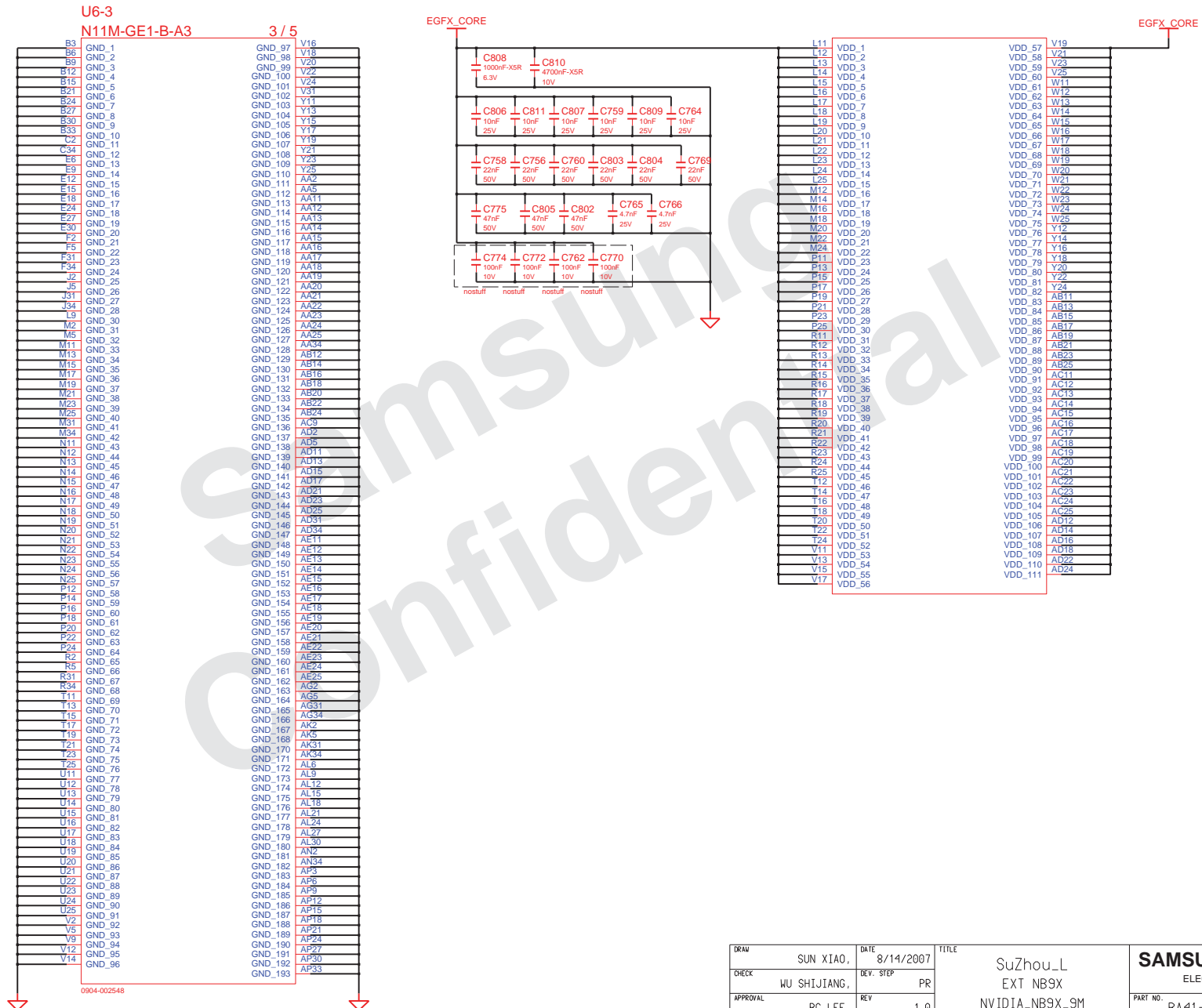
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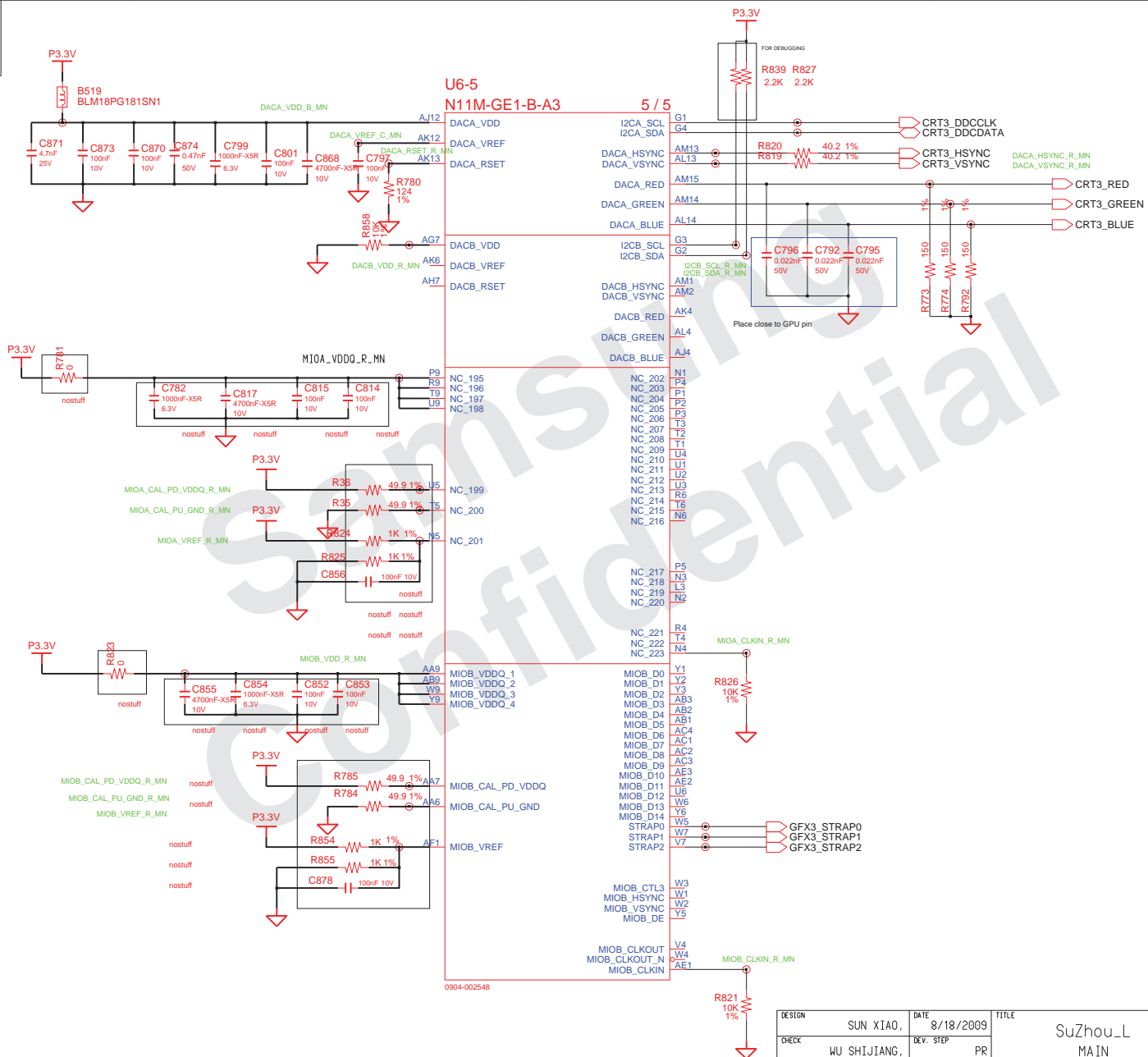


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DRAM	SUN XIAO,	DATE	8/14/2007	TITLE	SuZhou_L EXT NB9X NVIDIA_NB9X_9M		
CHECK	WU SHIJIANG,	DEV. STEP	PR				
APPROVAL	BC LEE,	REV	1.0				
MODULE CODE	LAST EDIT		November 25, 2009 10:50:13 AM				PAGE
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DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	Suzhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	N11M-GS	PART NO.	BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	24	OF 60

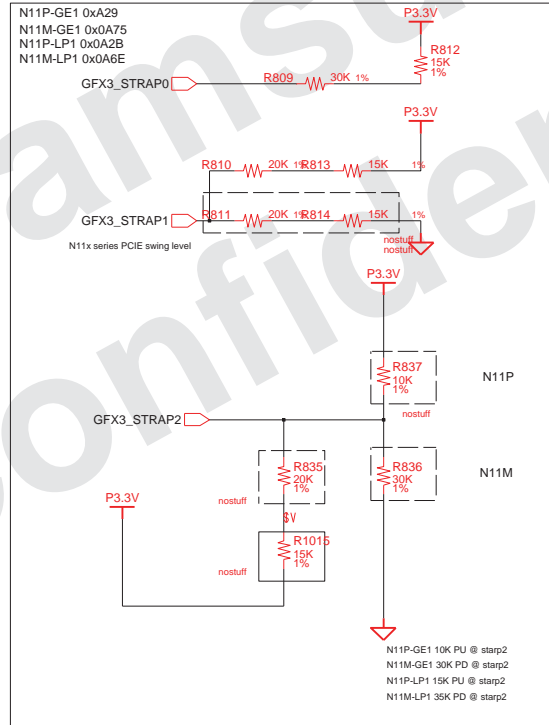
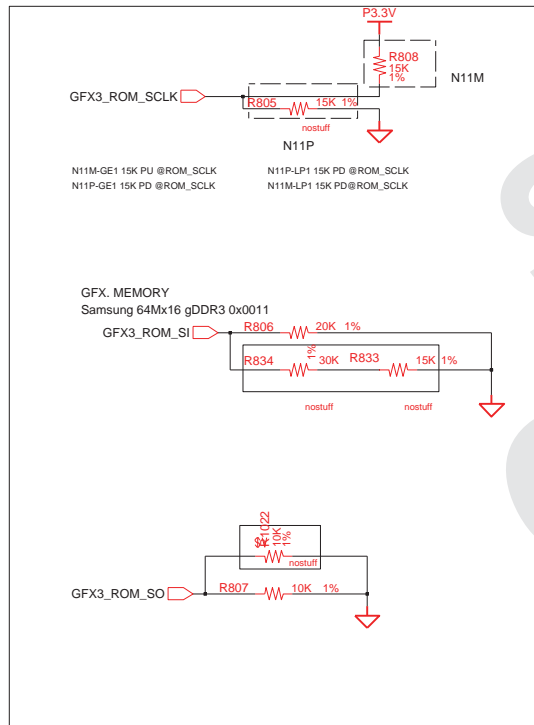
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N11x_40nm STRAP

Pin	Description	Activate	Pin	Description	Activate
GPIO(0)	General Purpose	NC	GPIO(12)	PWR_LEVEL	NC
GPIO(1)	HPD-C	NC	GPIO(13)	MEM_VID	NC
GPIO(2)	LCD0_BL_PWM	High	GPIO(14)	PWR_CTRL1	NC
GPIO(3)	LCD0_VDD	High	GPIO(15)	HPD-E	High
GPIO(4)	LCD0_BL_EN	High	GPIO(16)	FAN_PWM	NC
GPIO(5)	GPU VID0	00 0.8v 10 0.95v	GPIO(17)	Reserved	NC
GPIO(6)	GPU VID1	01 0.85v 11 1.03v	GPIO(18)	Reserved	NC
GPIO(7)	GPU VID2	NC	GPIO(19)	HPD-D	NC
GPIO(8)	OVERT	LOW			
GPIO(9)	ALERT	NC			
GPIO(10)	MEM_VREF	NC			
GPIO(11)	SLI_SYNC	NC			

STRAP PIN	BIT 3	BIT 2	BIT 1	BIT0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

RESISTOR	PULL UP	PULL DOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



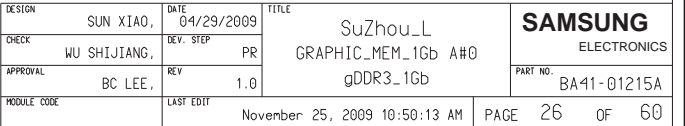
N11P-GE1	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	1	0	0	1	N11P-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

N11M-GE1	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	0	1	0	1	N11M-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

DESIGN	SUN XIAO,	DATE	8/21/2009	TITLE SuZhou_L MAIN N11M-GS	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		
APPROVAL	BC LEE,	REV	1.0		
MODULE CODE	LAST EDIT				
November 25, 2009 10:50:13 AM				PAGE	25 OF 60

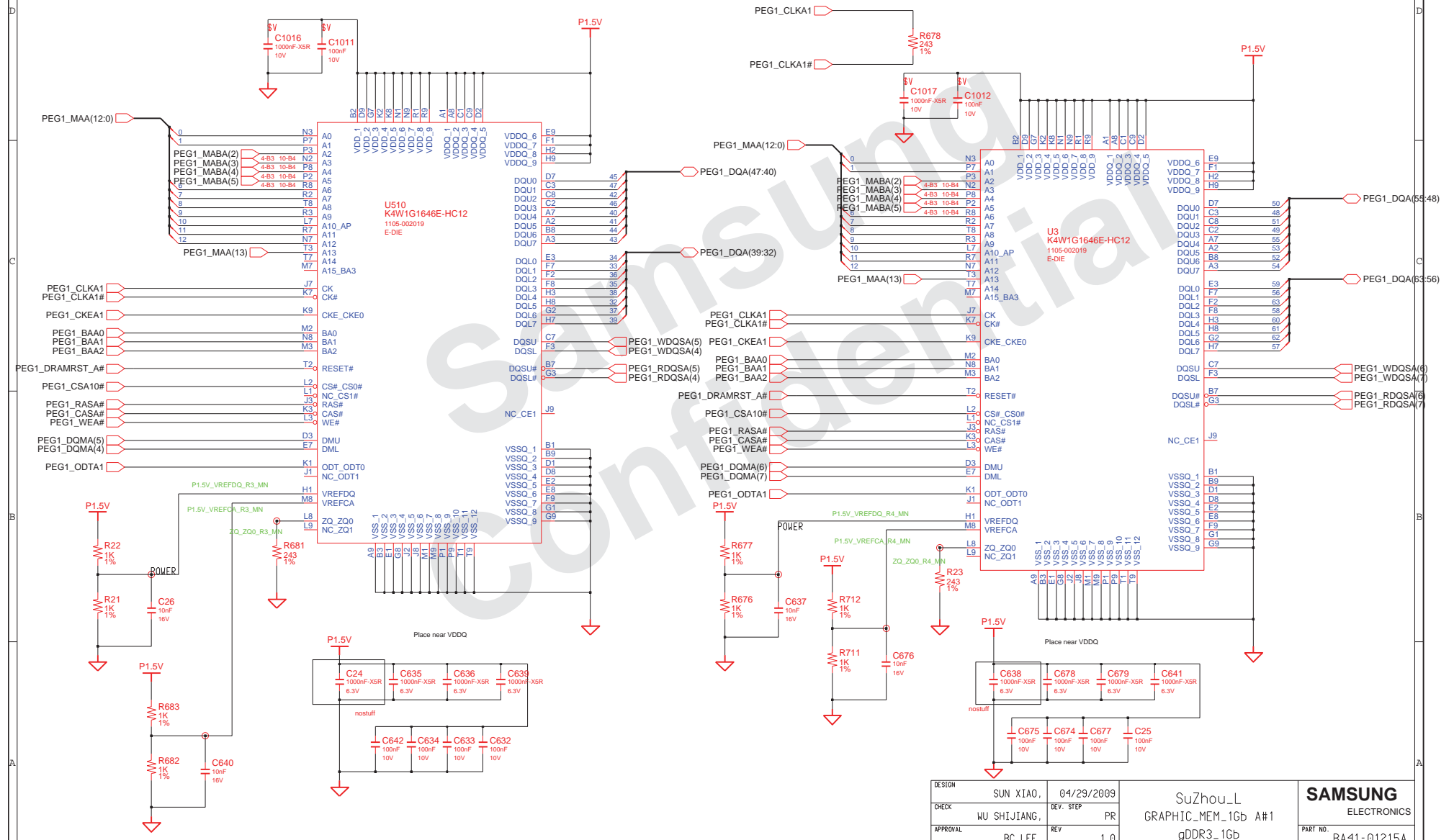
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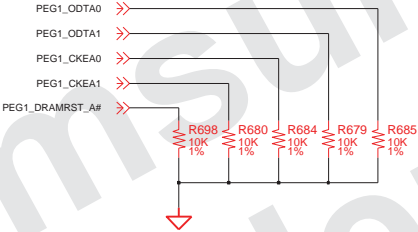
A-Channel #1



DESIGN	SUN XIAO,	04/29/2009	SuZhou_L GRAPHIC_MEM_1Gb A#1 gDDR3-1Gb	SAMSUNG ELECTRONICS	
CHECK	WU SHIJIANG,	DEV. STEP PR			
APPROVAL	BC LEE,	REV 1.0		PART NO.	BA41-01215A
MODULE CODE	LAST EDIT		November 25, 2009 10:50:13 AM	PAGE 27	OF 60

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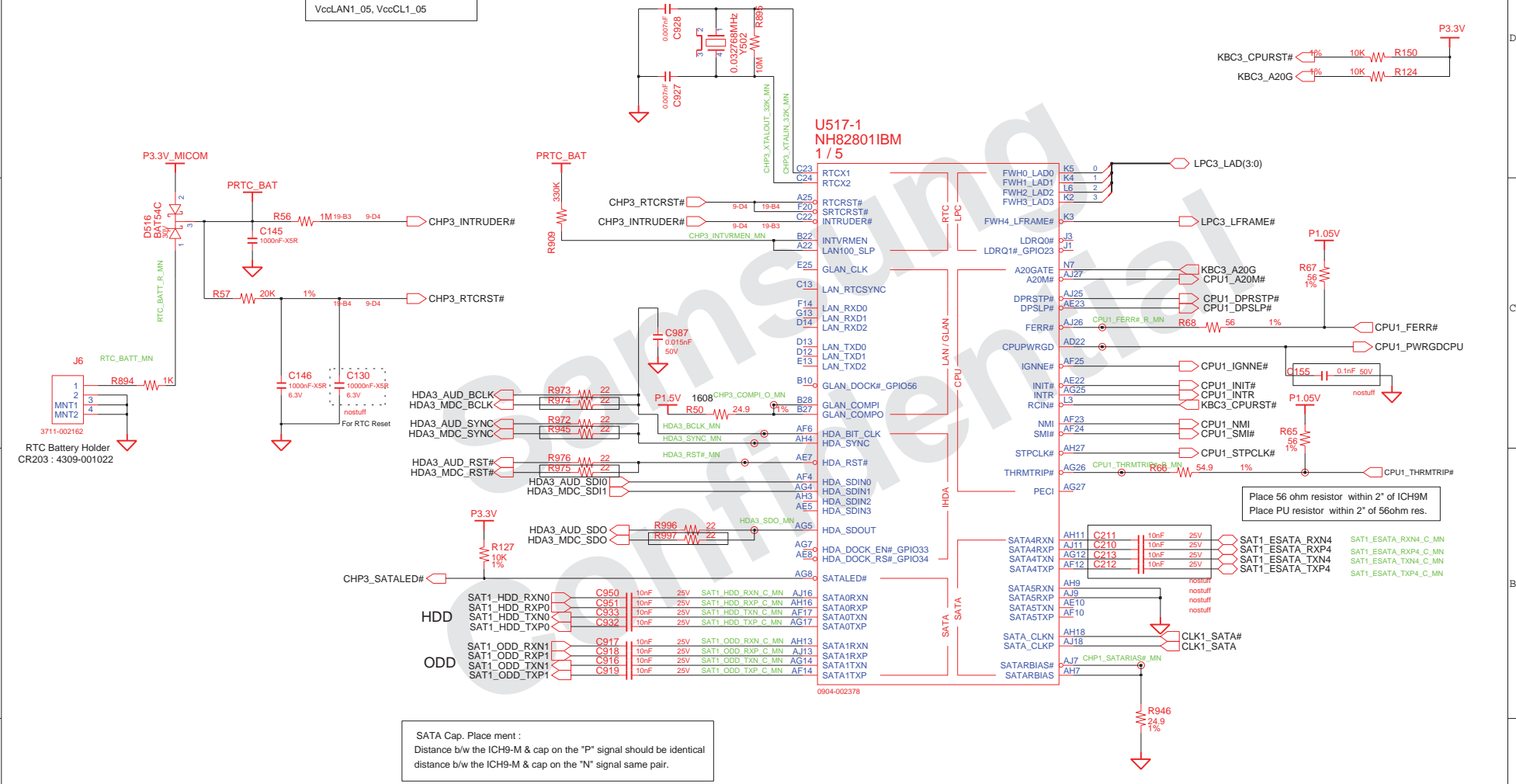
gDDR3 Memory PULL UP & PULL DOWN



DESIGN	SUN XIAO,	DATE	03/14/2009	TITLE	SuZhou_L	SAMSUNG ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR	PULL-UP&PULL-DOWN		
APPROVAL	BC LEE,	REV	1.0	gDDR3_1Gb		
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE 28 OF 60		

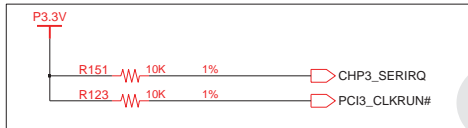
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Internal VR Strap
INTVRMEN Pull up
VccSus1_05, VccSus1_5, VccCL1_5
VccLAN1_05, VccCL1_05

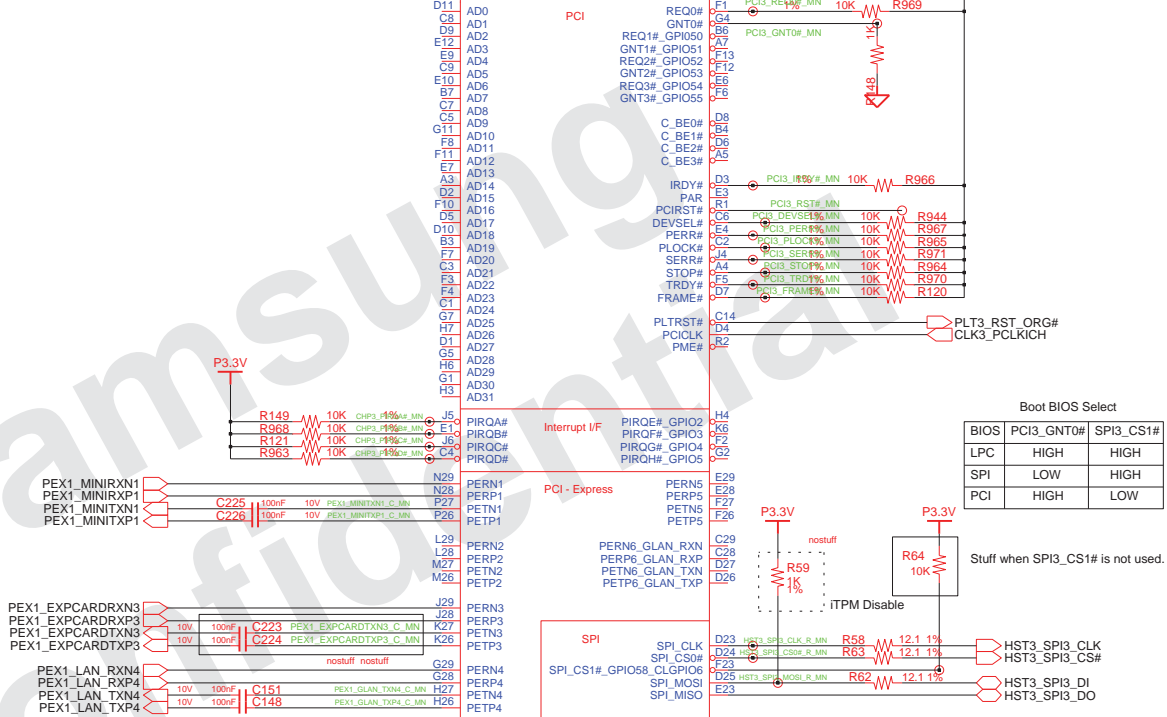


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U517-2
NH82801IBM
2/5



LPC option ; These are used with LPC

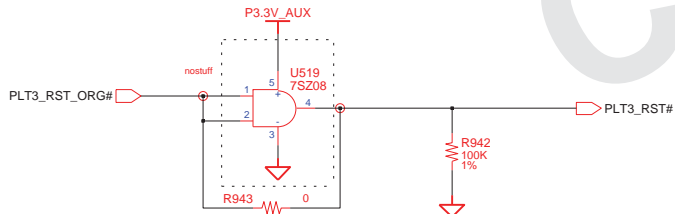


Boot BIOS Select

BIOS	PCI3_GNT0#	SPI3_CS1#
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW

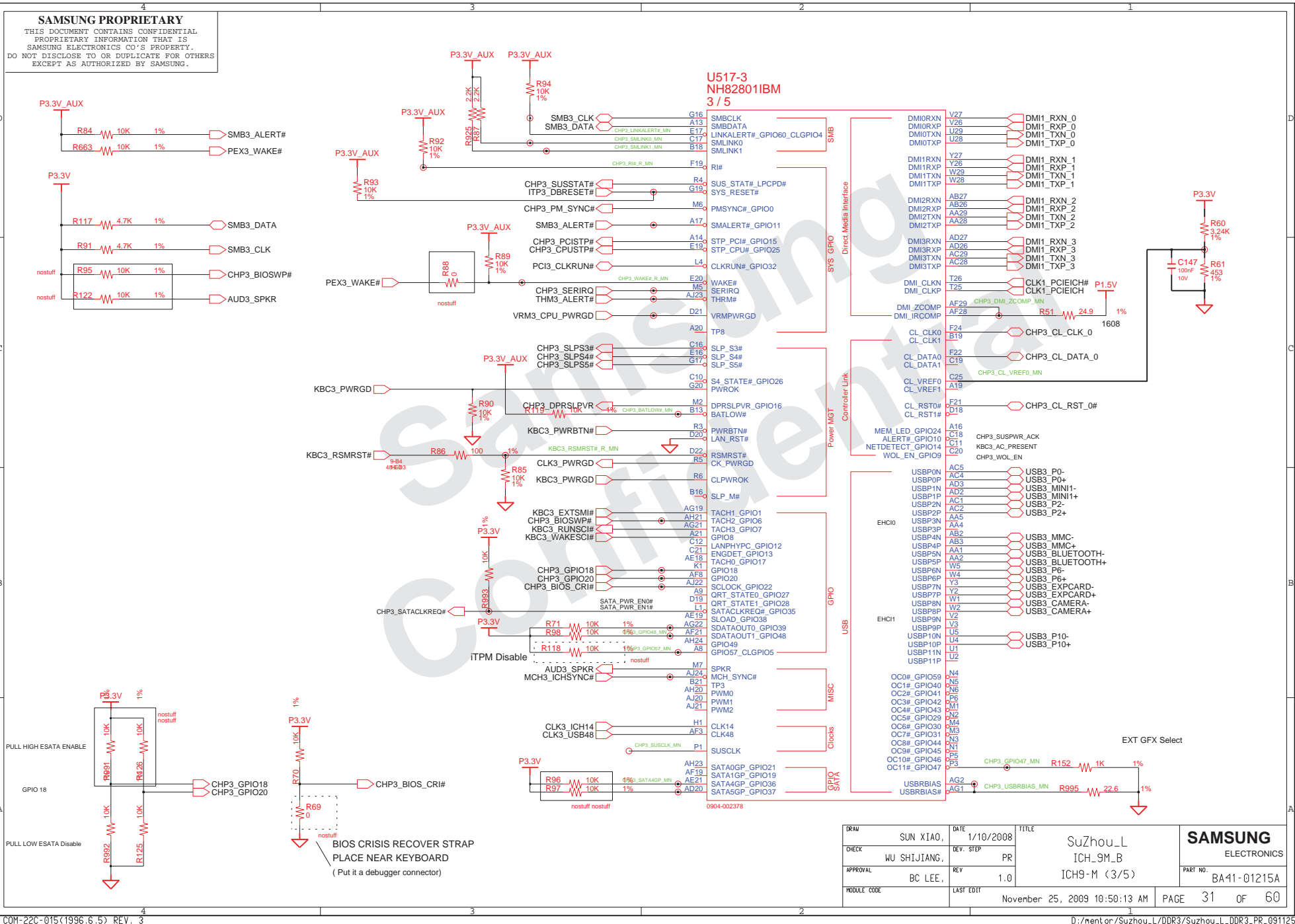
Stuff when SPI3_CS1# is not used.

AC caps : PCIe need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs



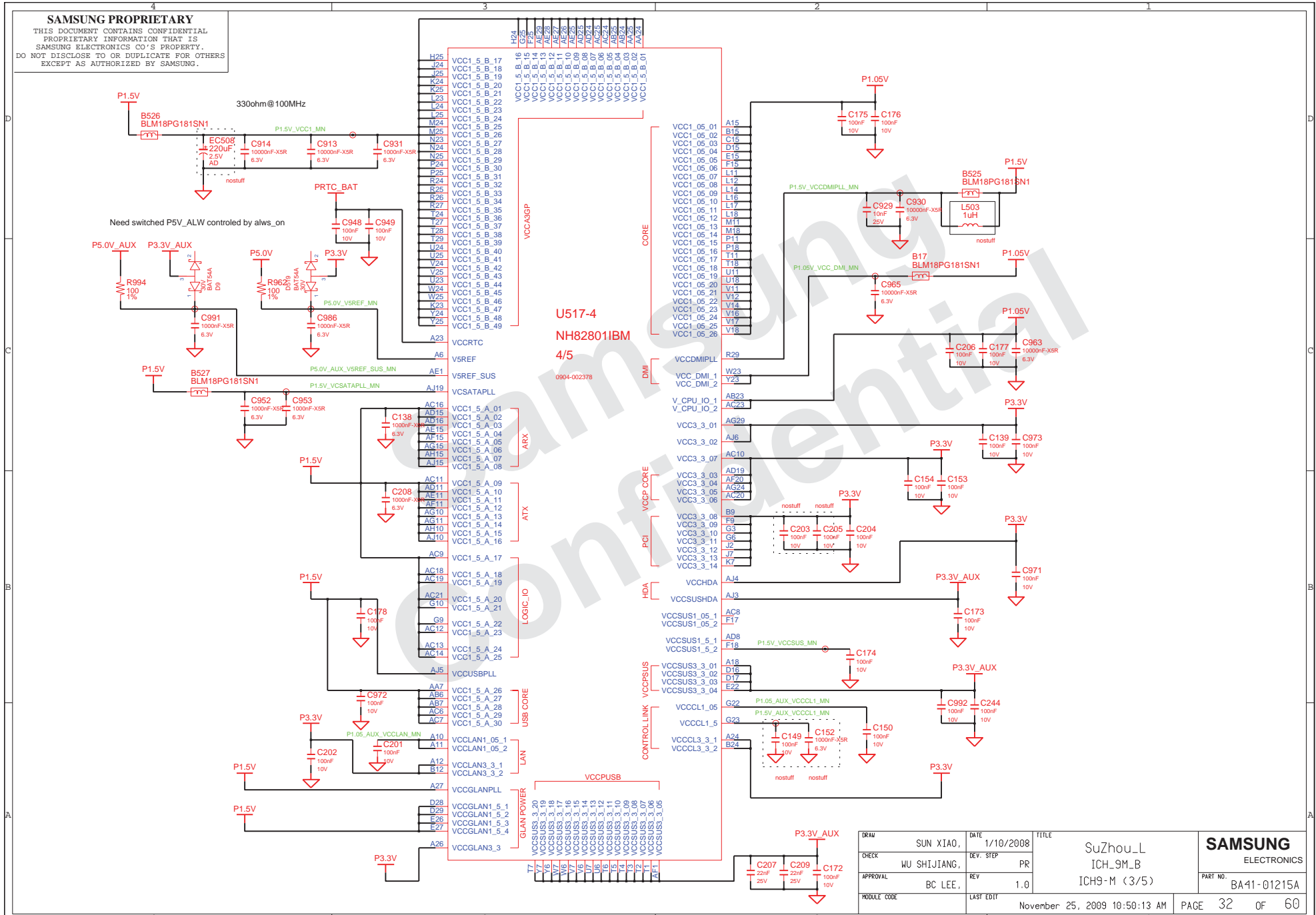
DRAW	SUN XIAO,	DATE	1/10/2008	TITLE	Suzhou_L ICH_9M_B ICH9-M (2/5)	SAMSUNG ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	30 OF 60	

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DATE	SUN XIAO,	1/10/2008	TITLE	SuZhou_L ICH_9M_B ICH9-M (3/5)	SAMSUNG ELECTRONICS	
CHECK	WU SHIJIANG,	DEV. STEP				PR
APPROVAL	BC LEE,	REV				1.0
			PART NO.	BA41-01215A		
MODULE CODE	LAST EDIT		November 25, 2009 10:50:13 AM			
			PAGE	31	OF 60	

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DATE	1/10/2008	TITLE	SuZhou_L ICH9M_B ICH9-M (3/5)	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	PART NO. BA41-01215A
APPROVAL	BC LEE,	REV	1.0	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE 32 OF 60

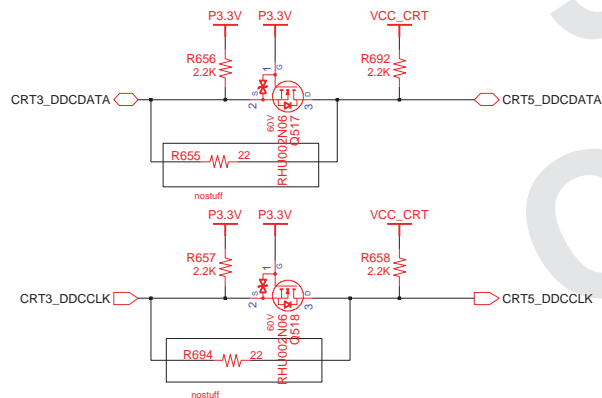
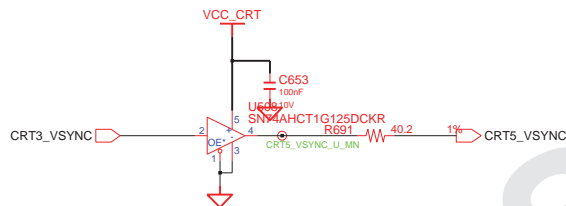
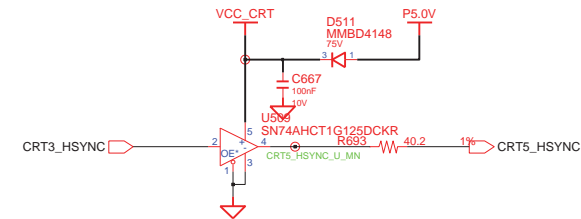
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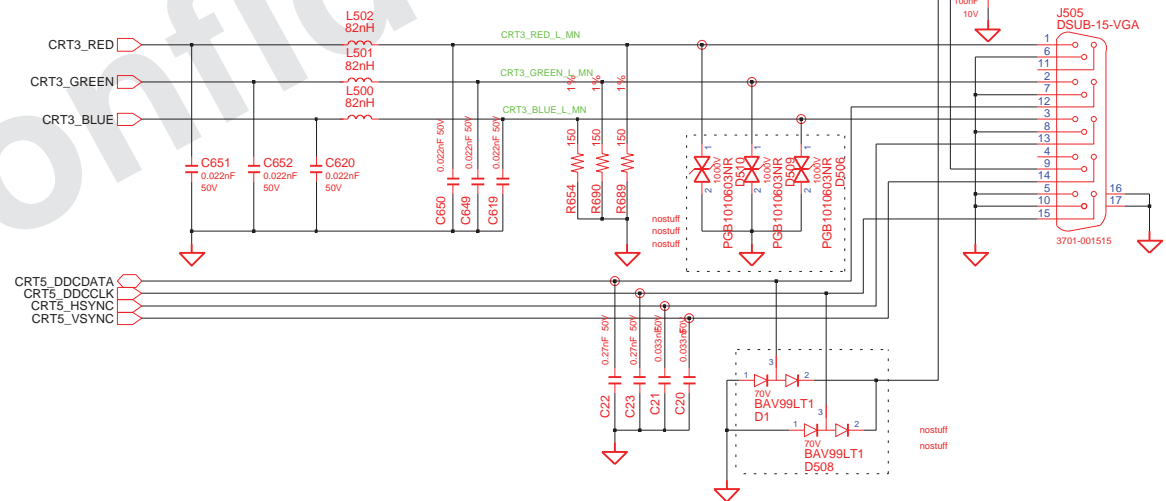
CRT

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Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

CRT CONNECTOR

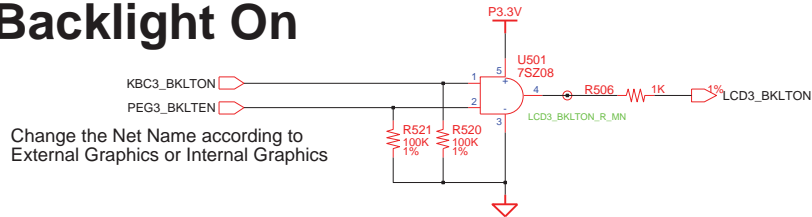


DESIGN	SUN XIAO,	DATE	01/08/2009	TITLE	SuZhou_L GRAPHICS_IF CRT	SAMSUNG ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	35 OF 60	

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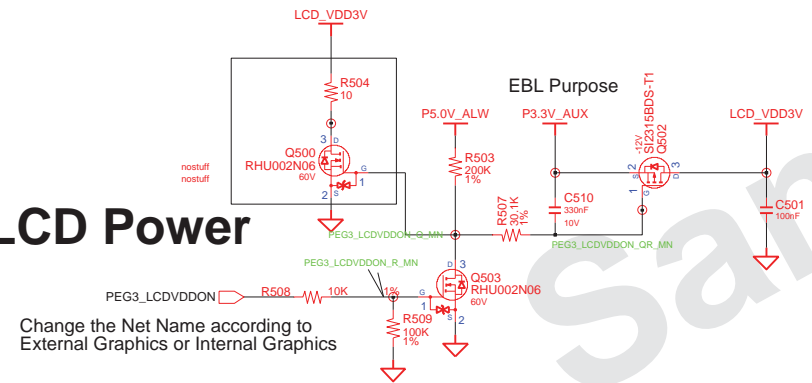
LVDS

Backlight On



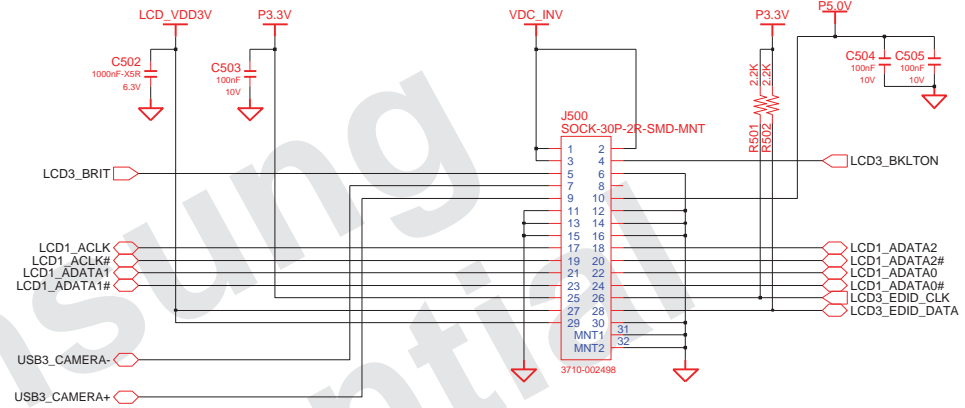
Change the Net Name according to
External Graphics or Internal Graphics

LCD Power

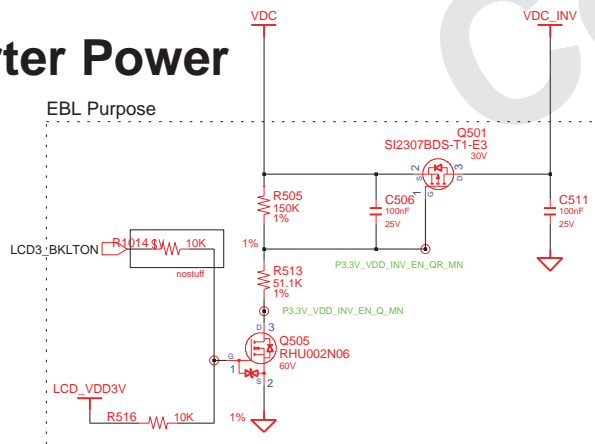


Change the Net Name according to
External Graphics or Internal Graphics

1Ch. LCD Connector



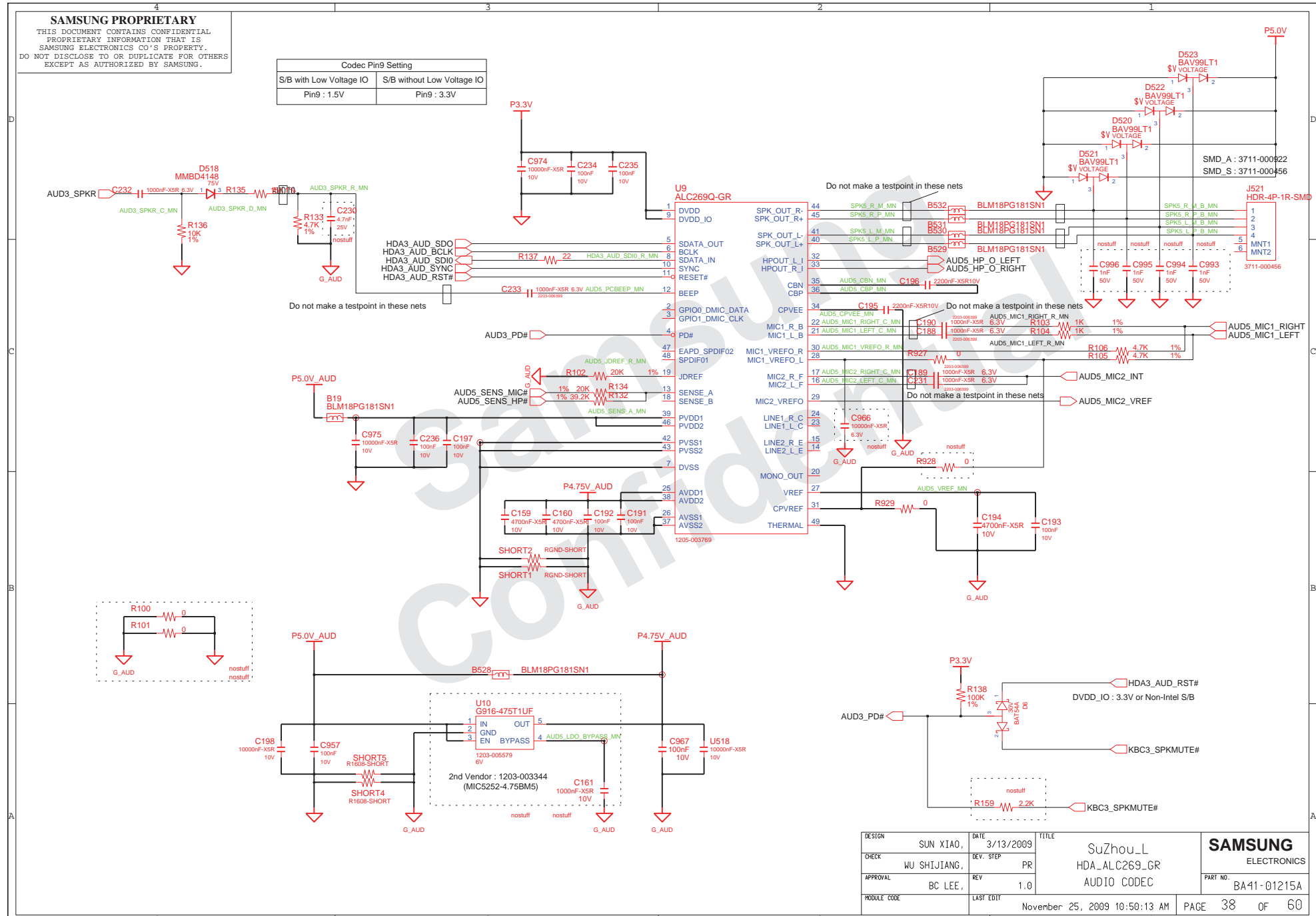
Inverter Power



DESIGN	SUN XIAO,	DATE	01/08/2009	TITLE	SuZhou_L GRAPHICS_IF LVDS	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			PART NO. BA41-01215A
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	36	OF 60

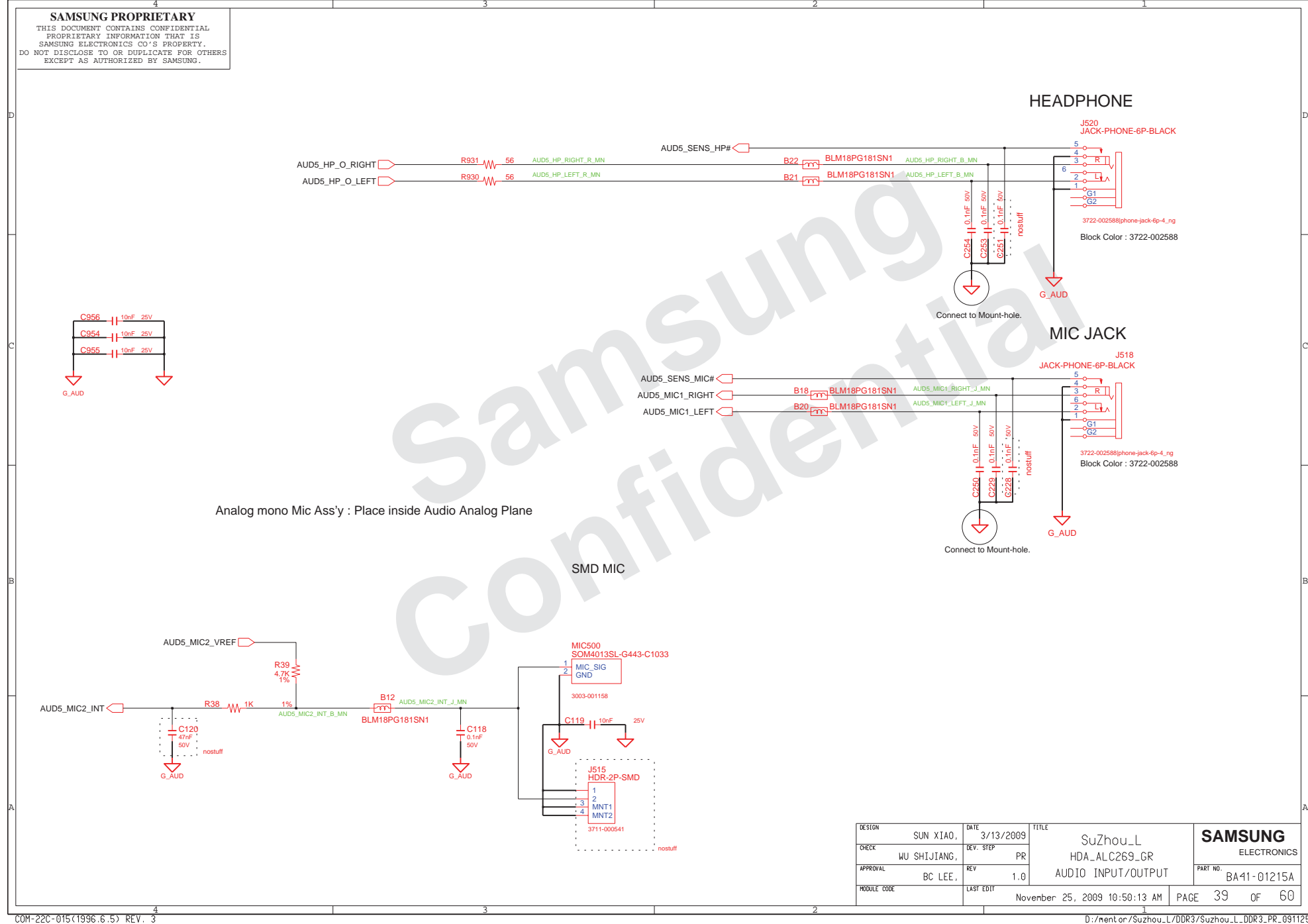
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Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



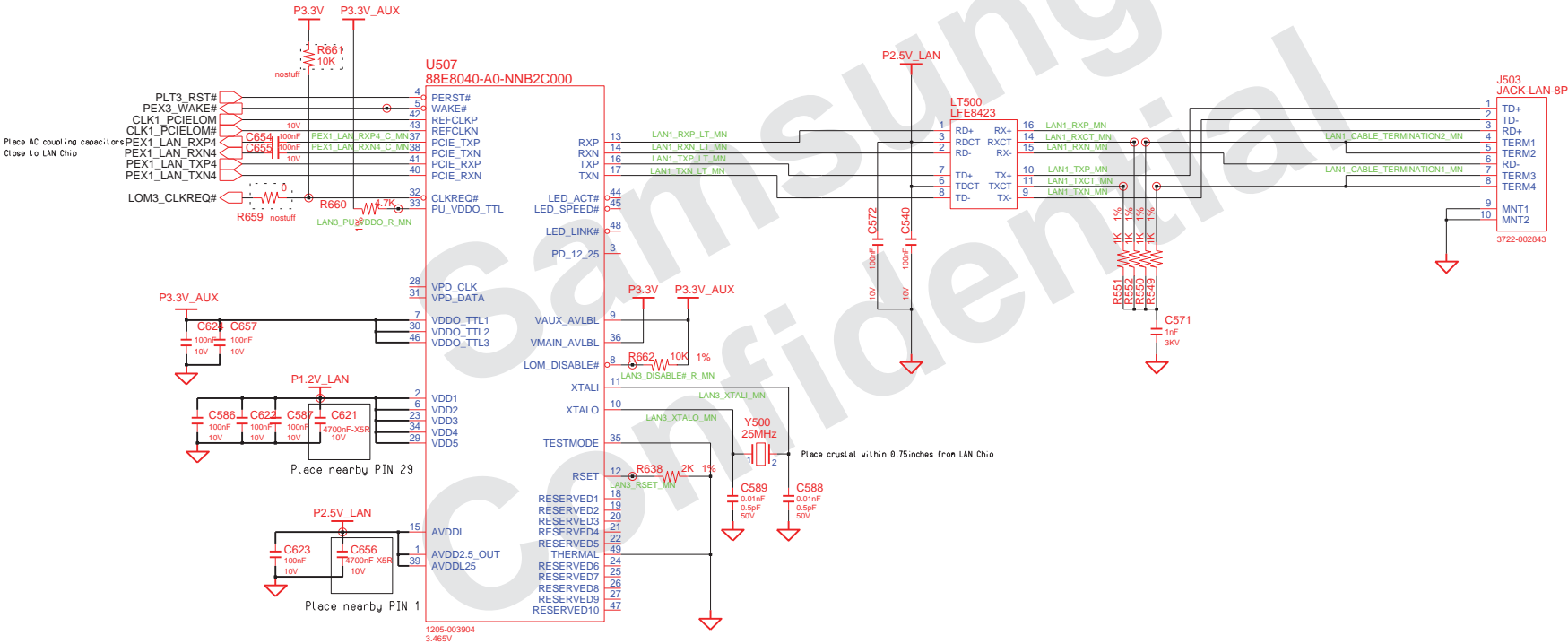
DESIGN	SUN XIAO,	DATE	3/13/2009	TITLE	SuZhou_L	SAMSUNG ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR		HDA_ALC269_GR	
APPROVAL	BC LEE,	REV	1.0		AUDIO CODEC	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	38 OF 60	

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MARVELL 88E8040T

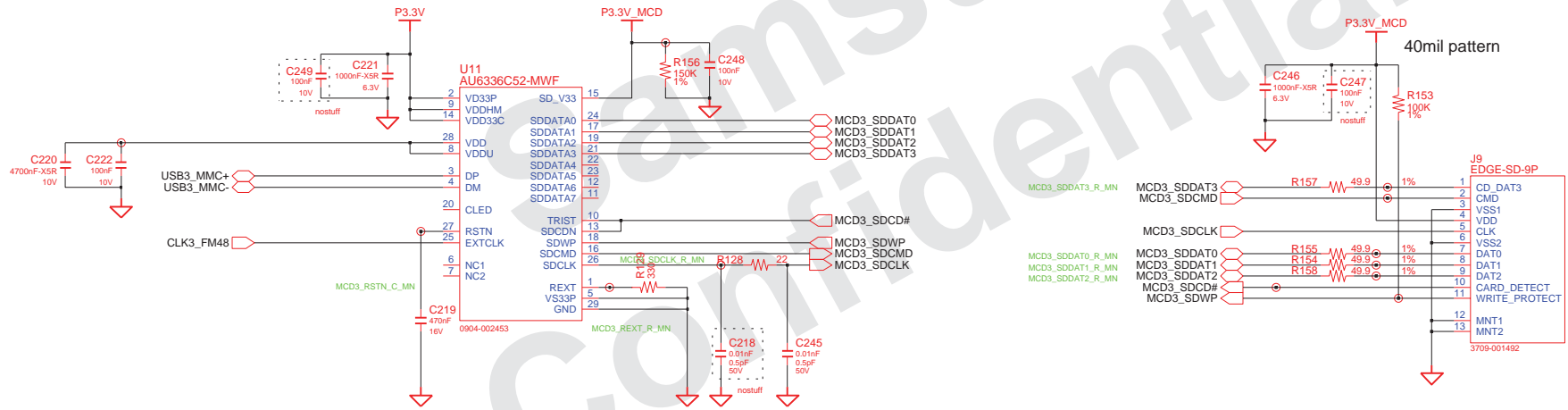


DESIGN	SUN XIAO,	DATE	3/17/2009	TITLE	SuZhou_L	SAMSUNG ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	40 OF 60	

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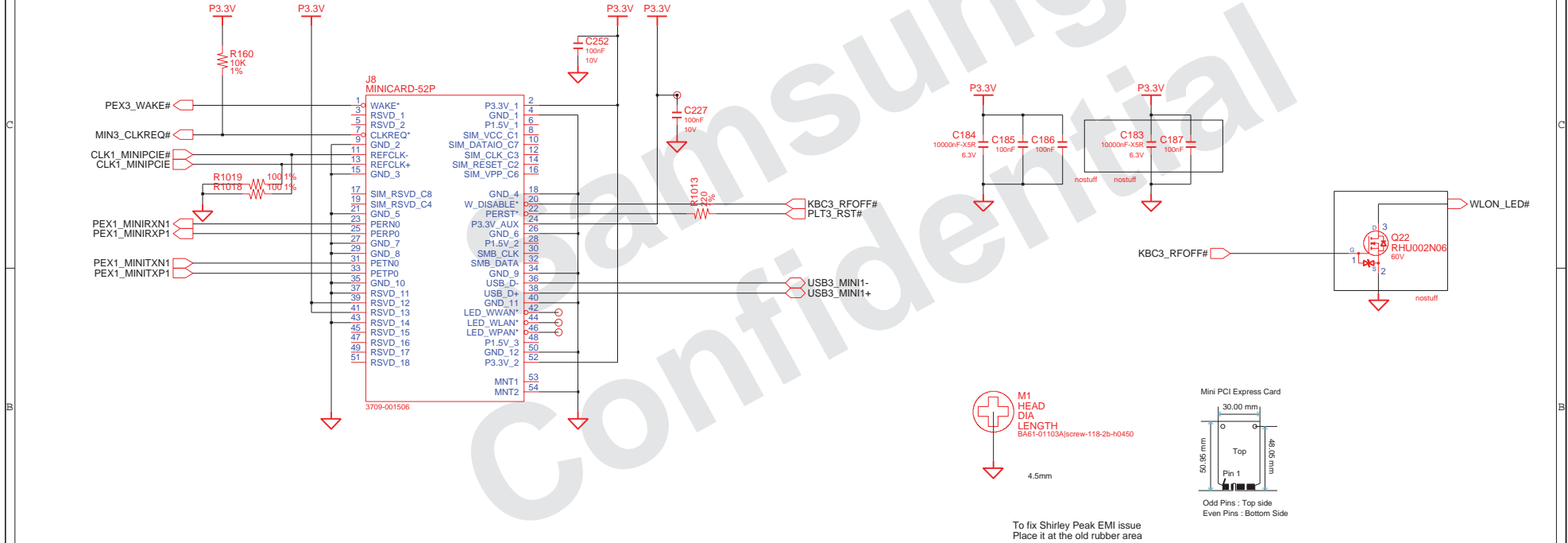
3 IN 1

P3.3V_MCD distance between R5U880 and socket should be less than 2 inches



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WLAN, 7mm

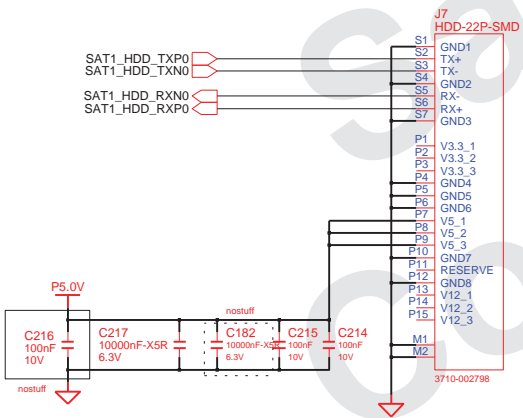


DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	SuZhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		MINI_PCIE_CONN	
APPROVAL	BC LEE,	REV	1.0			PART NO.
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			BA41-01215A
					PAGE	42 OF 60

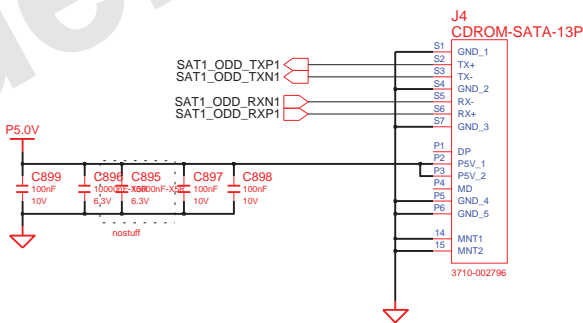
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SATA I/F CONN

SATA HDD CONN



SATA ODD CONN



DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	SuZhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		SATA_DEVICES	
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	43 OF 60	

MAIN BOARD (MICOM)

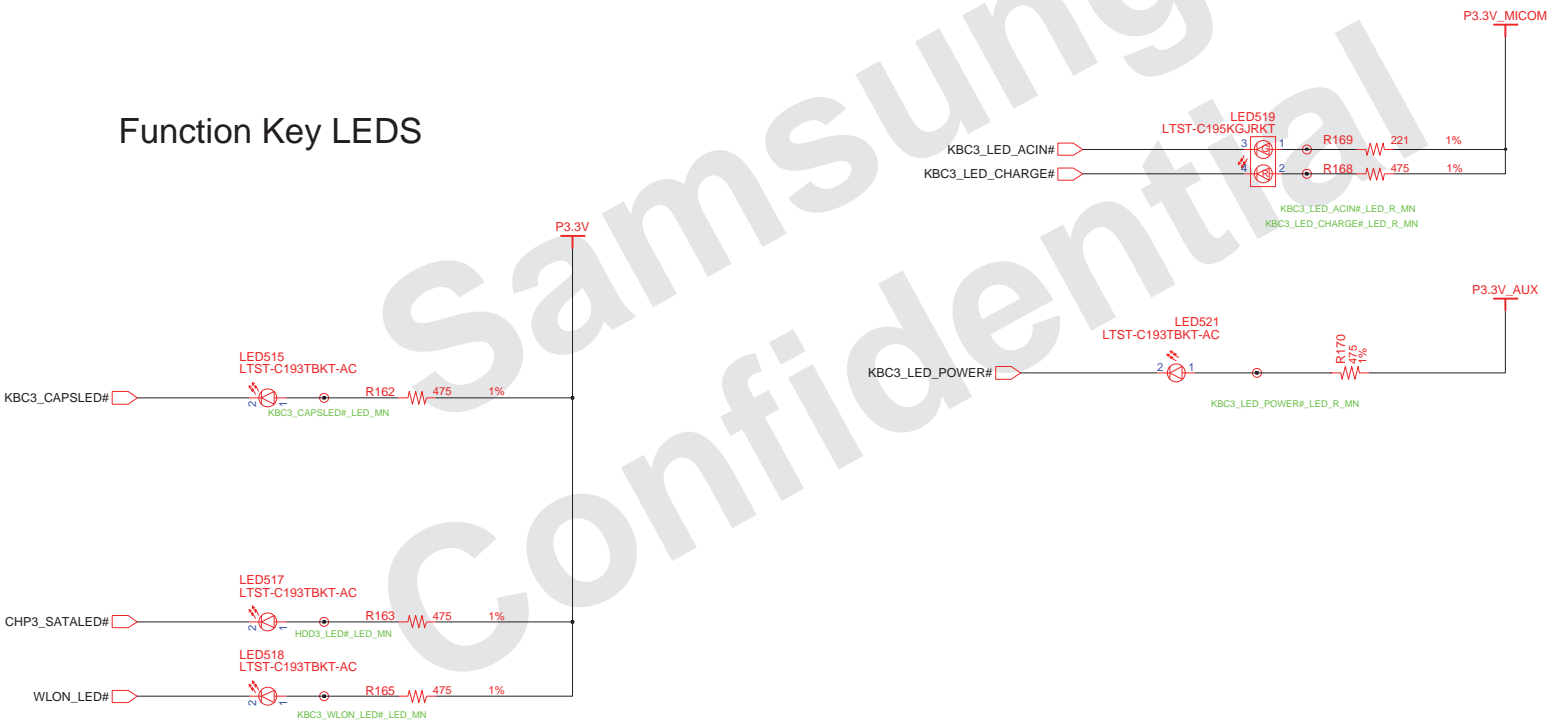
MICOM POWER RESET



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LED SWITCH LOGIC

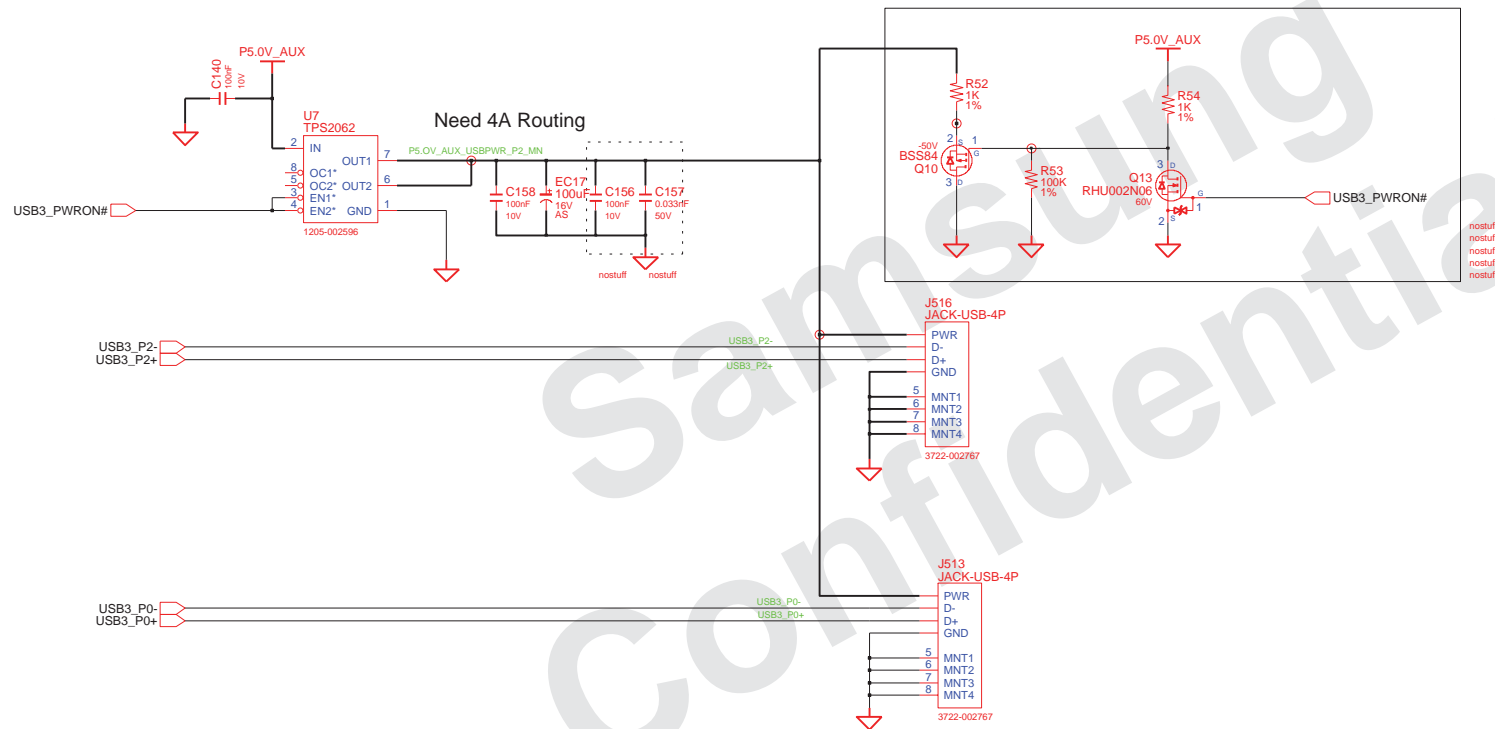
Function Key LEDs



DRAWN	SUN XIAO,	DATE	8/12/2006	TITLE	SuZhou_L	SAMSUNG
CHECK	WU SHUIJANG,	REV. STEP	PR	LED_Switch	LED_Switch	ELECTRONICS
APPROVAL	BC LEE,	REV	1.0	LED_Switch		PART NO.
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			BA41-01215A
				PAGE	46	OF 60

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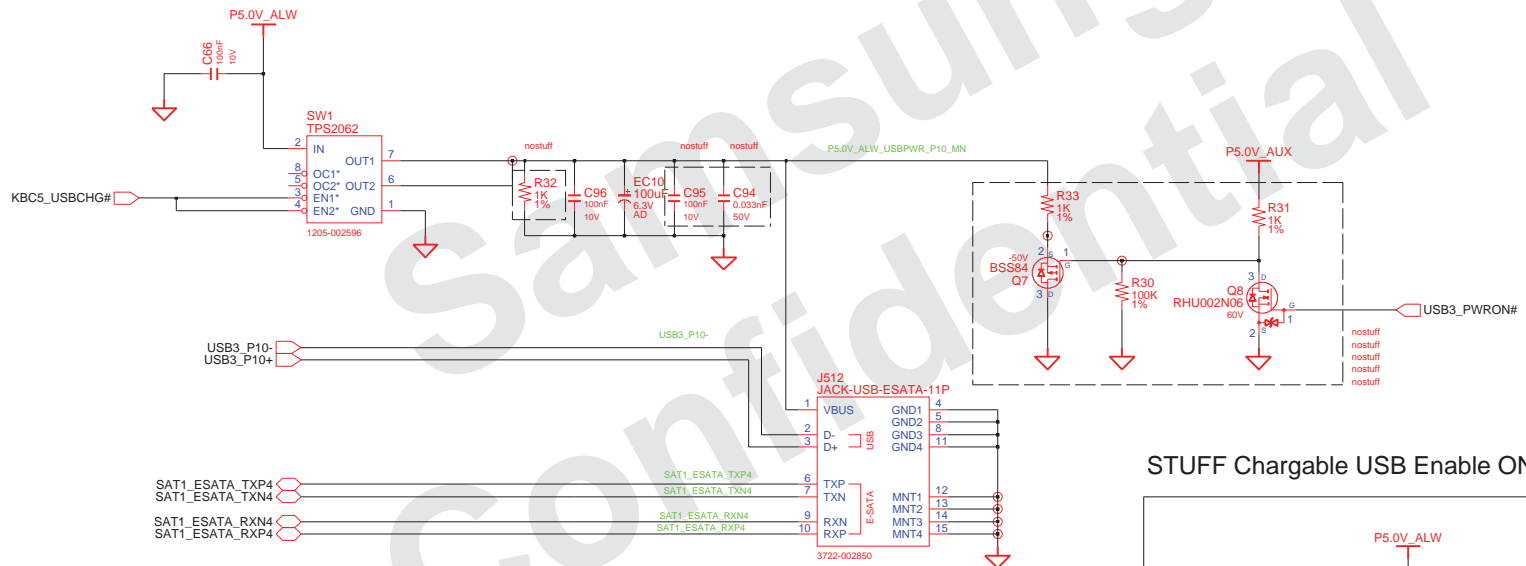
1/2 PORT USB CONNECTOR



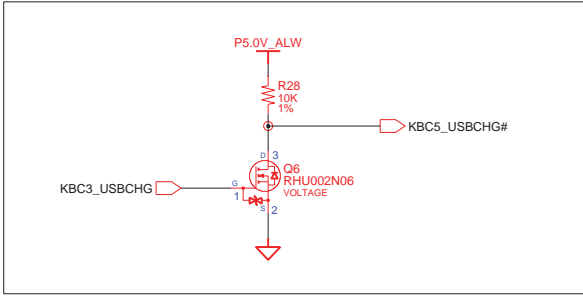
DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	SuZhou_L USB_CONN	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			PART NO. BA41-01215A
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	47	OF 60

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eSATA



STUFF Chargeable USB Enable ONLY

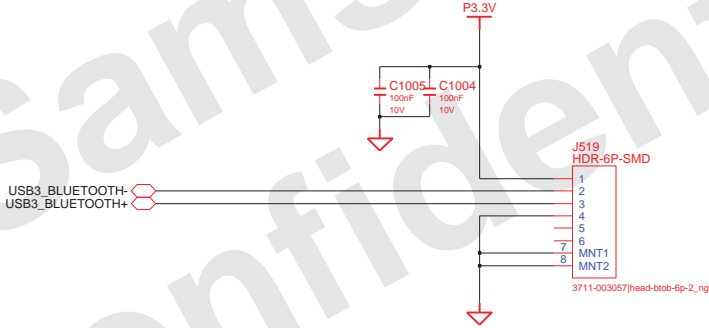


DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	Suzhou_L	SAMSUNG ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN	ESATA	
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	48 OF 60	

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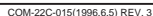
Bluetooth Interface

Samsung
Confidential

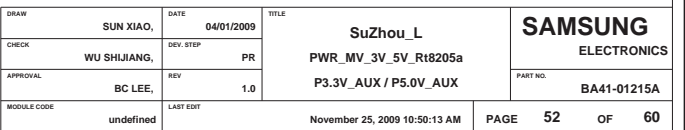


DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	SuZhou_L USB_DEVICES	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			PART NO. BA41-01215A
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	50	OF 60

CHARGER & POWER MANAGEMENT

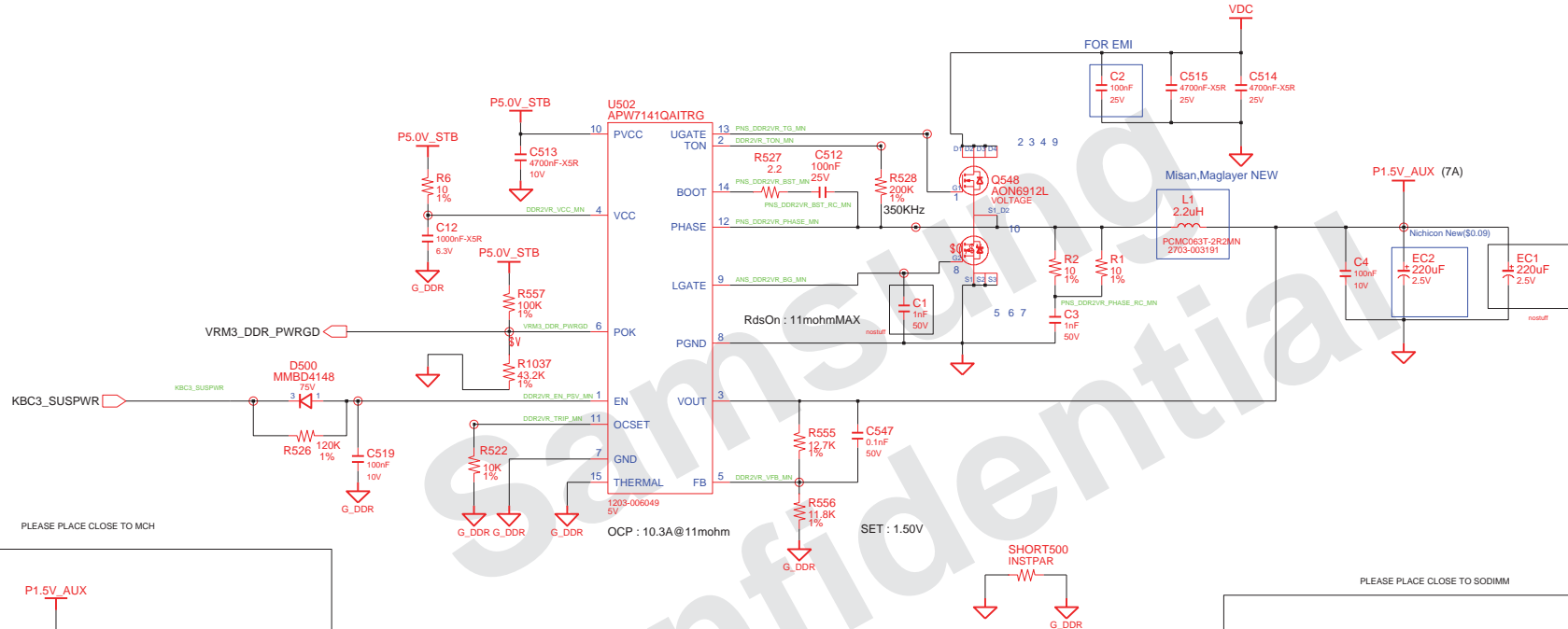


P3.3V_AUX & P5.0V_AUX

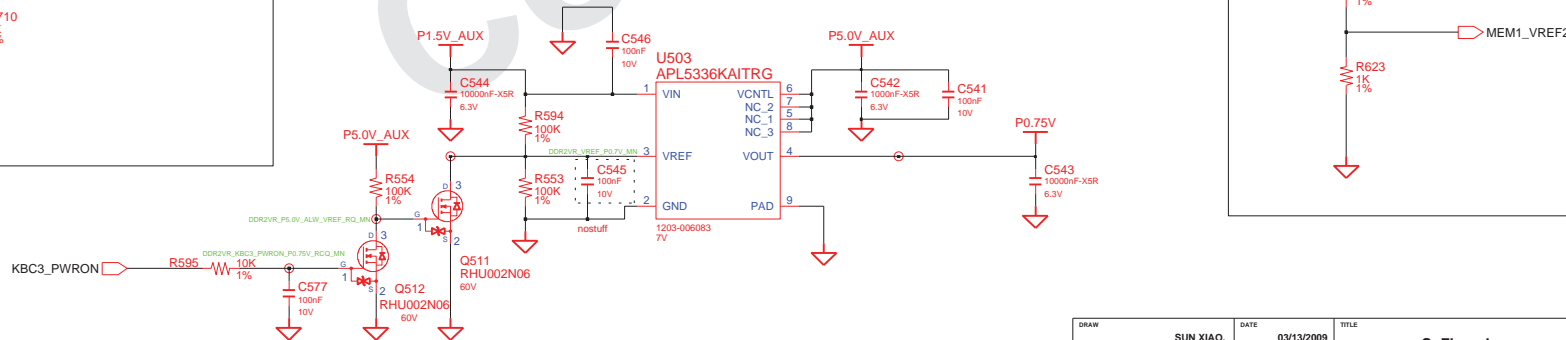


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DDR3 Power



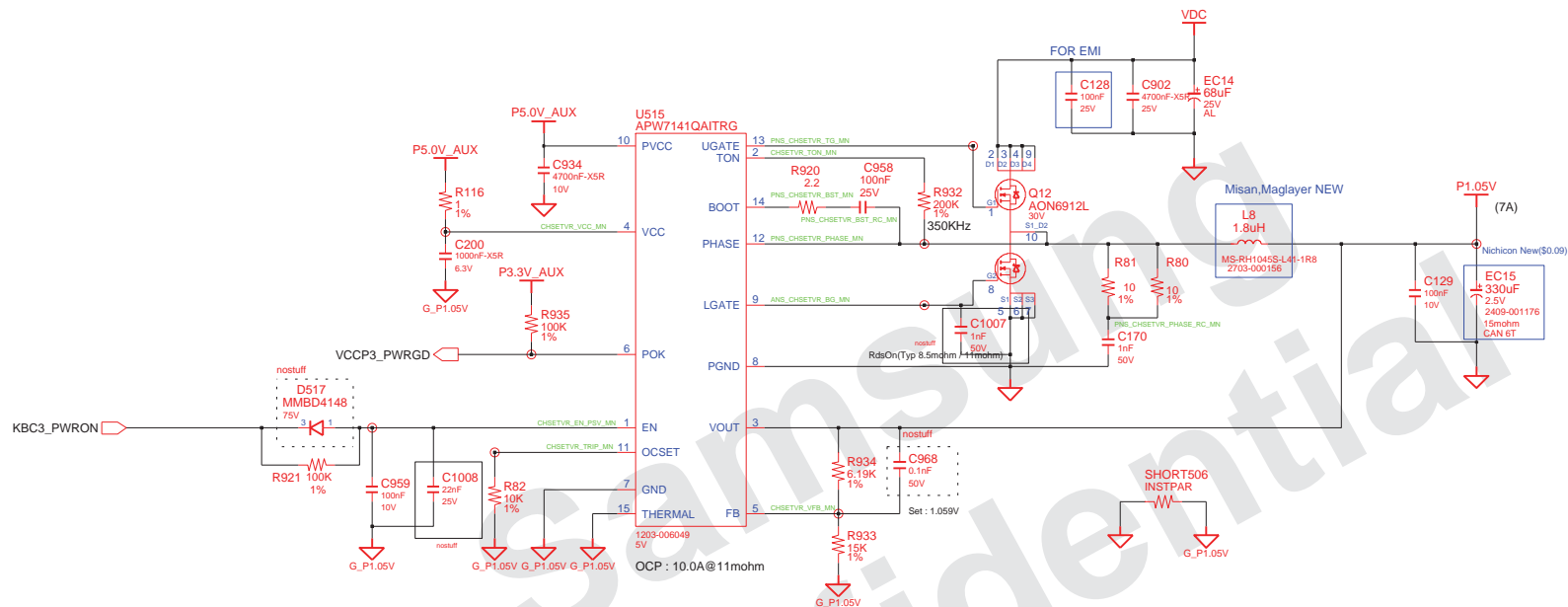
DDR3 VTT(0.75V)



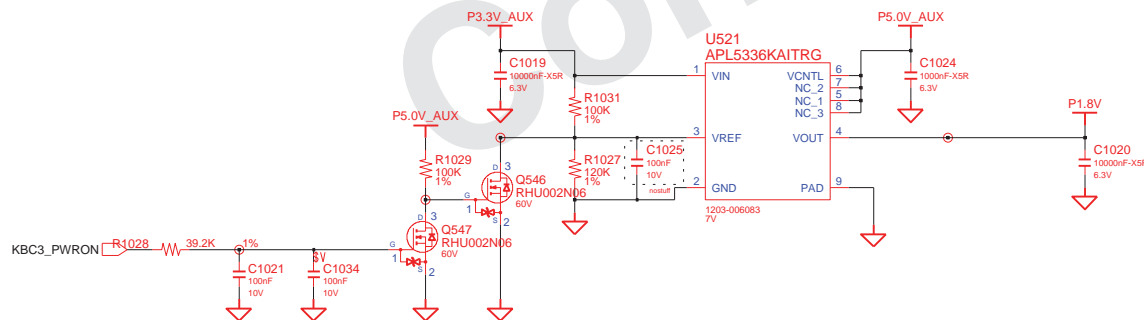
DRAW	SUN XIAO,	DATE	03/13/2009	TITLE	SuZhou_L	SAMSUNG
CHECK	WU SHUIJANG,	REV. STEP	PR	PWR_MV_Memory_Rt8207	DDR3 POWER (P1.5V_AUX)	ELECTRONICS
APPROVAL	BC LEE,	REV	1.0			PART NO.
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	53	OF 60

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CHIPSET POWER (P1.05V)



P1.8V(LDO)

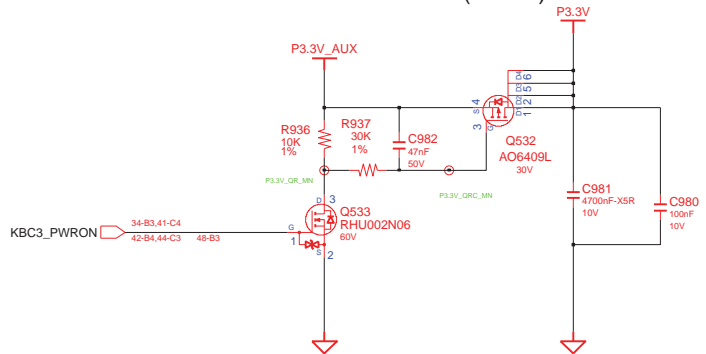


DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	SuZhou_L	SAMSUNG
CHECK	WU SHUJIANG,	REV. STEP	PR	PWR_MV_Cantiga		ELECTRONICS
APPROVAL	BC LEE,	REV	1.0	Chipset Power (P1.05V_M,P1.2V)	PART NO.	BA41-01215A
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	54	OF 60

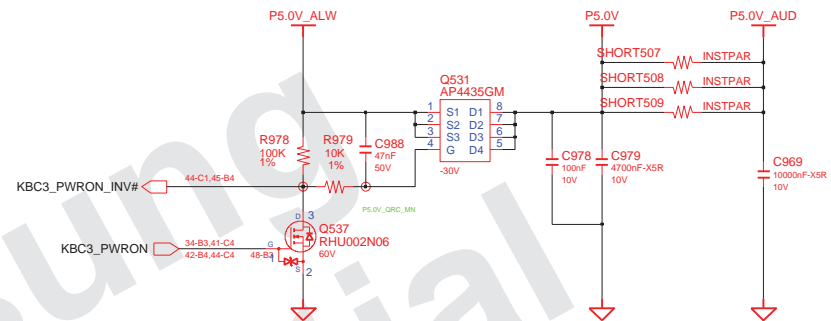
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Switched Power

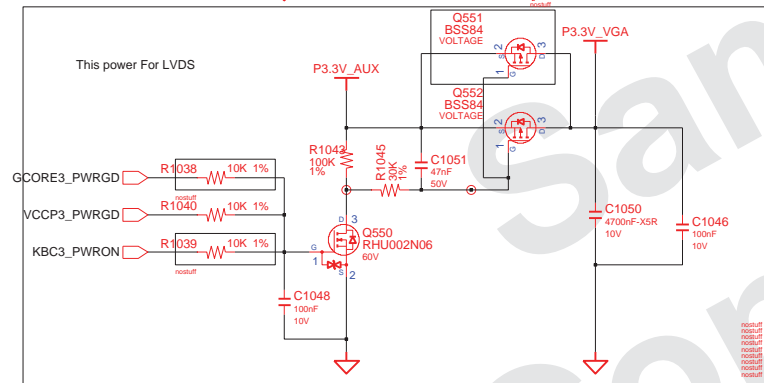
Switched Power On (P3.3V)



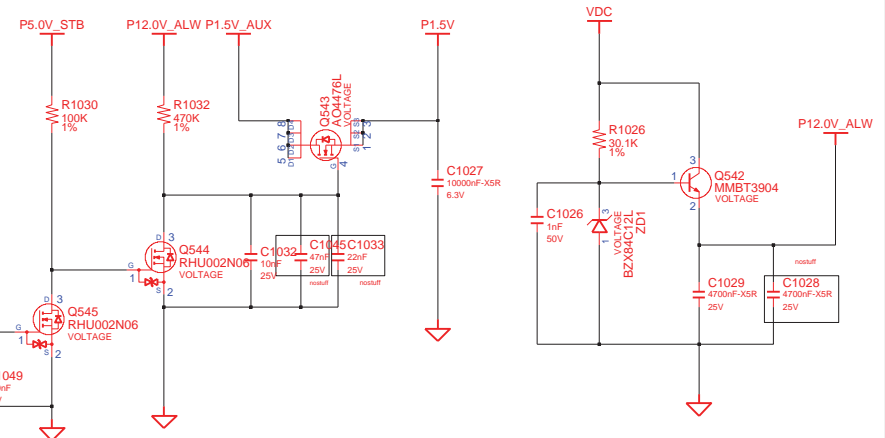
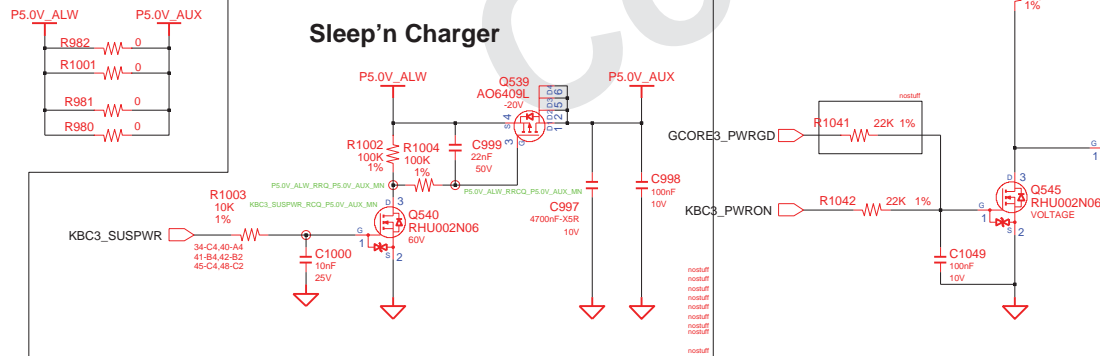
Switched Power On (P5.0V)



This power For LVDS



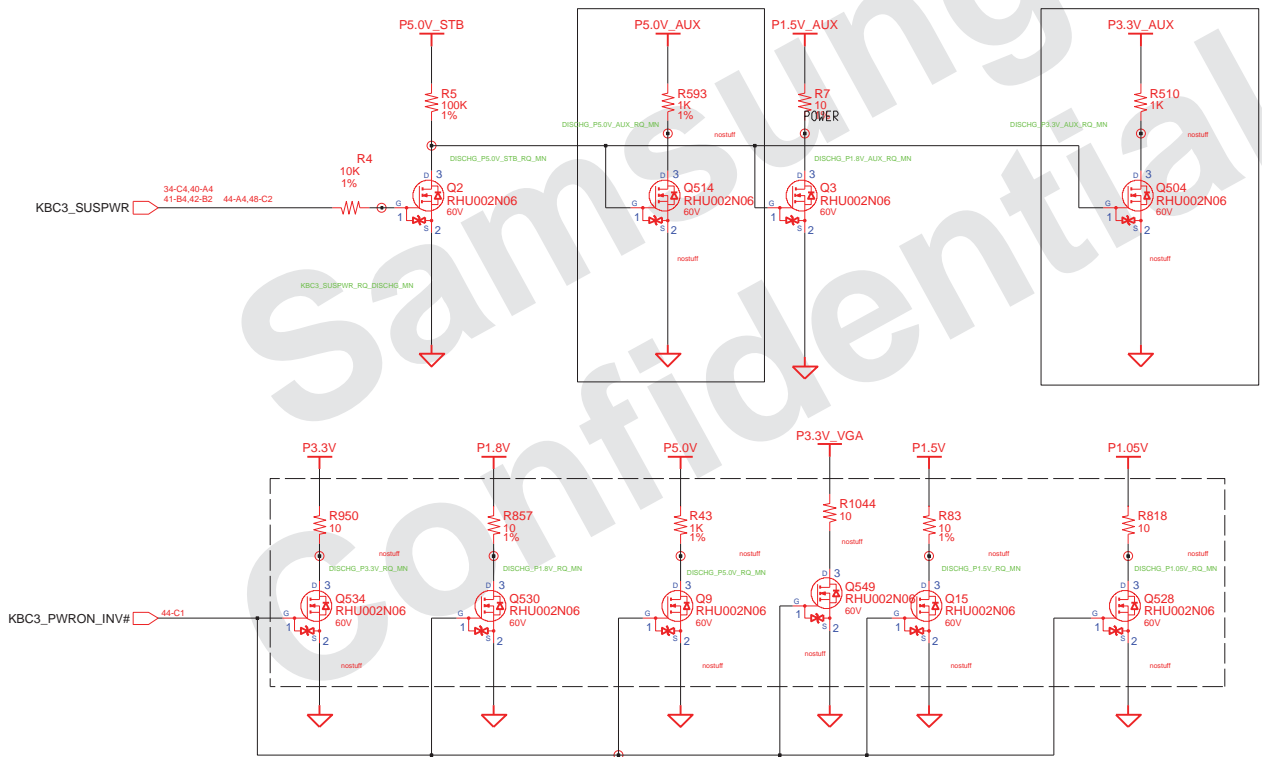
Sleep'n Charger



DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	SuZhou_L	SAMSUNG
CHECK	WU SHUJIANG,	REV. STEP	PR	PWR_MV_Switched		ELECTRONICS
APPROVAL	BC LEE,	REV	1.0	SWITCHED POWER	PART NO.	BA41-01215A
MODULE CODE		LAST EDIT		November 25, 2009 10:50:13 AM	PAGE	57 OF 60

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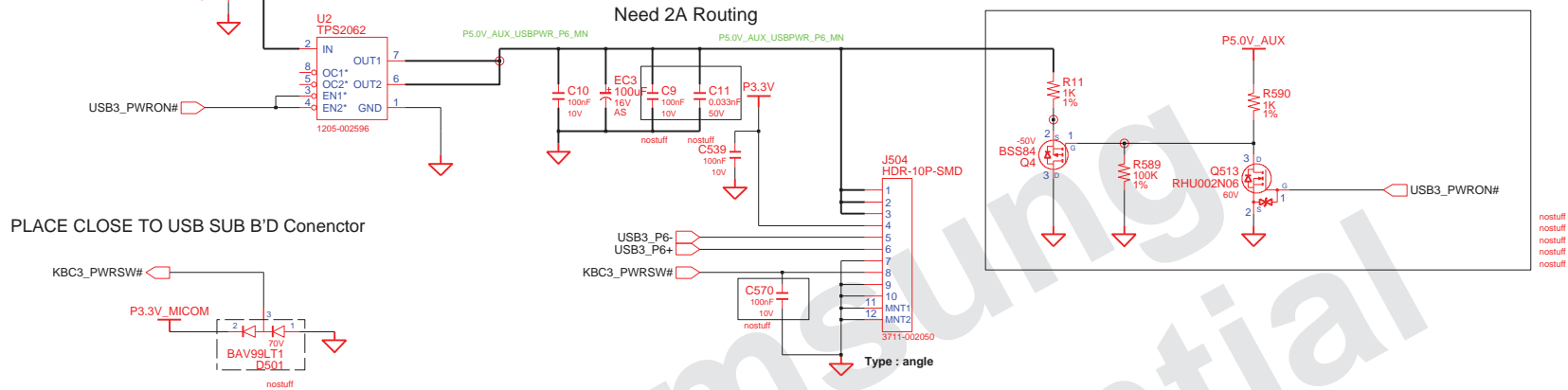
POWER DISCHARGER



DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	SuZhou_L	SAMSUNG
CHECK	WU SHUIJANG,	REV. STEP	PR	PWR_MV_DisCharger	DISCHARGING LOGIC	ELECTRONICS
APPROVAL	BC LEE,	REV	1.0			PART NO.
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM			BA41-01215A
				PAGE	58	OF 60

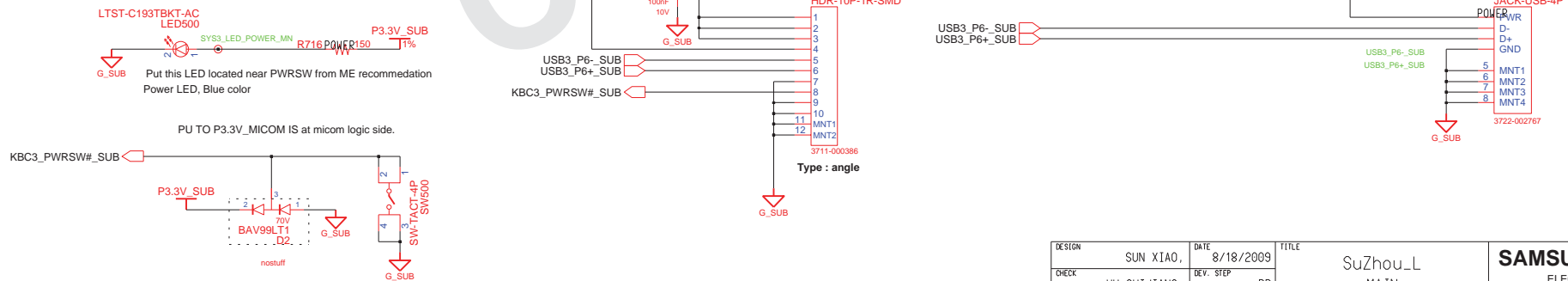
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Main Board



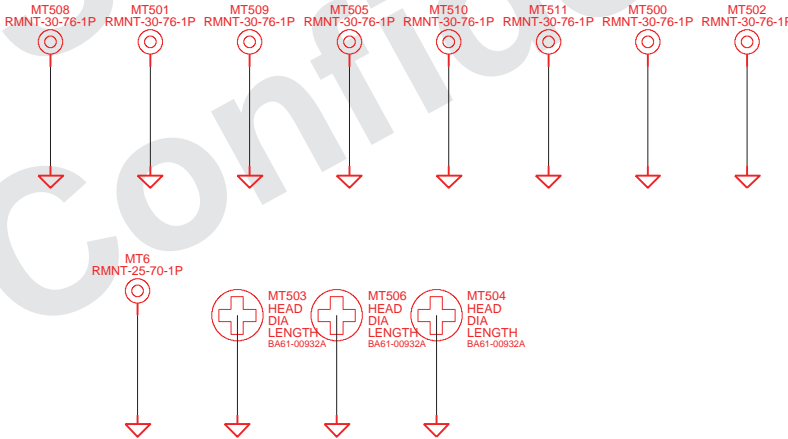
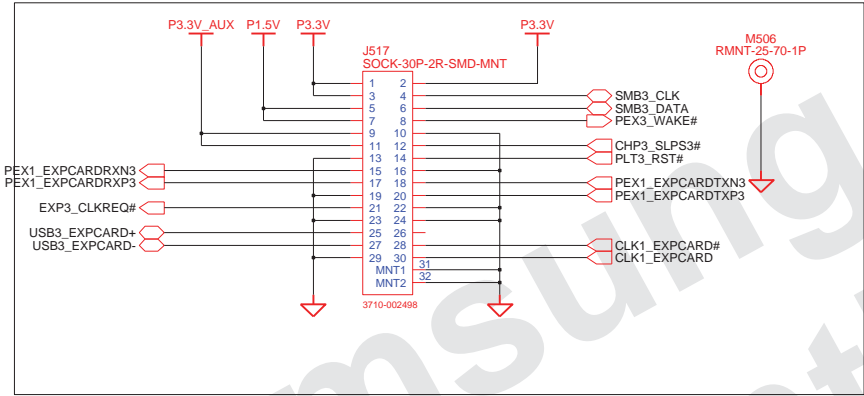
SUB Board

Power Switch Button



DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	Suzhou_L MAIN SUB BOARD	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			PART NO. BA41-01215A
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	59	OF 60

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DESIGN	SUN XIAO,	DATE	9/9/2009	TITLE	SuZhou_L	SAMSUNG ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR		MAIN	
APPROVAL	BC LEE,	REV	1.0		EXPRESS CARD	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	60 OF 60	