

Compal Confidential

QIWG5/QIWG6 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N13X

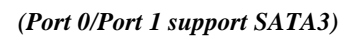
2012-02-01

LA-7981P

REV:1.0

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				Date: Wednesday, February 15, 2012	Rev 1.0
				Sheet 1 of 60	

QIWG6
LS7981P CardReader/B
LS7982P USB/B
LS7983P PWR/B
LS7984P LED/B
LS7985P ODD/B



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Voltage Rails

power plane	State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0		○	○	○	○
S3		○	○	○	✗
S5 S4/AC		○	○	✗	✗
S5 S4/ Battery only		○	✗	✗	✗
S5 S4/AC & Battery don't exist		✗	✗	✗	✗

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VAIW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%	Board ID / SKU ID Table for AD channel				
Ra/Rc/Re	100K +/- 5%					
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB Port (Right Side CR-BD)
		2	USB Port (Left Side) USB3.0
		3	USB Port (Left Side) USB3.0
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
		8	
		9	USB/B (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
GPU:N13P-GL	N13P@
GPU:N13M-GE	N13M@
HDMI	HDMI@
Interna-Intel-USB3.0	IU3@
External-NEC-USB3.0	EU3@
Blue Tooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8162@
GIGA LAN	GIGA@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
Cameara	CMOS@
For QIWG5 (14")	14@
For QIWG6 (15")	15@
Unpop	@
G5/G6/G9(Low/Mid END)	nonBBH@
G9 High-END	BBH@
G9	G9 @
G5/G6/G9(Low/Mid END)	15_nonBBH@

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

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				Date: Wednesday, February 15, 2012	Sheet 3 of 60	

Hot plug detect for IFP link C

VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	

Performance Mode P0 TDP at Tj = 102 C* (GDDR3)

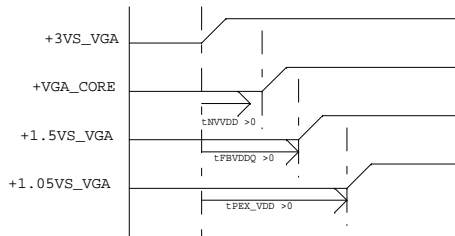
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

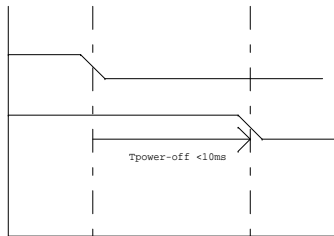
	Device ID
N13P-GL (28nm)	??
N13M-GE (28nm)	???

GPU	FB Memory (GDDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N13P-GL N13M-GE	Samsung 2500MHz	K4G10325FG-HC04						
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ1H24BFR-T2C						
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
	Samsung 2500MHz	K4G20325FG-HC04						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 2500MHz	H5GQ2H24MFR-T2C						
		64Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K

X76



1. all power rail ramp up time should be larger than 40us
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



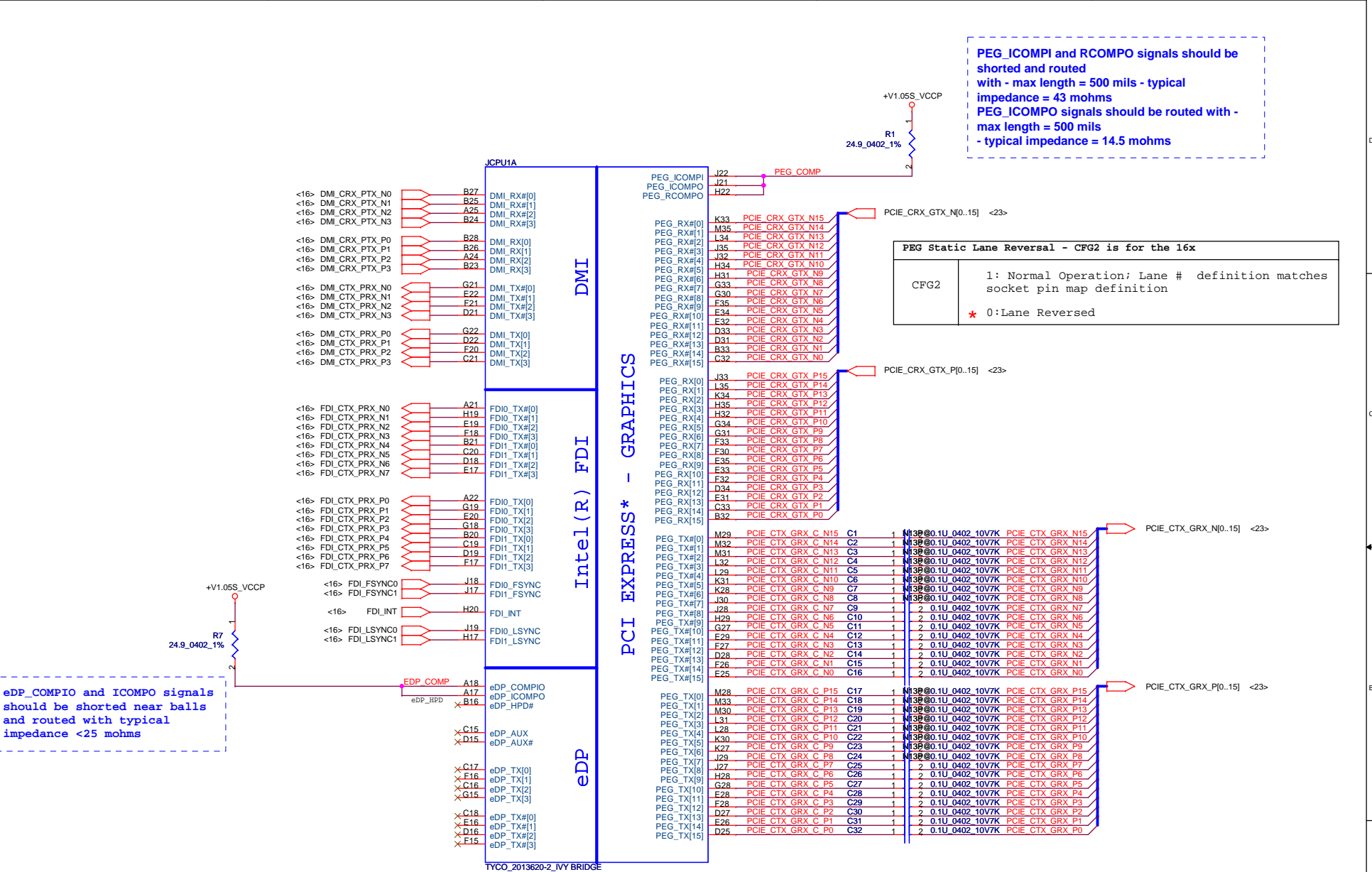
1. all GPU power rails should be turned off within 10ms

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						Custom	LA-7981P			0.2
Date:		Tuesday, February 14, 2012		Sheet		4		of 60		

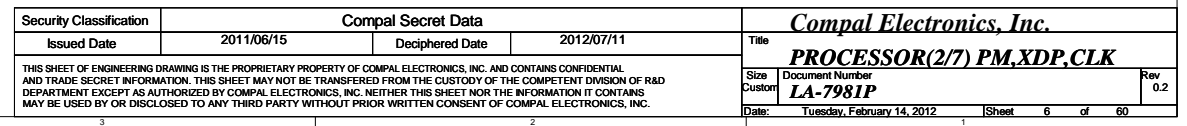
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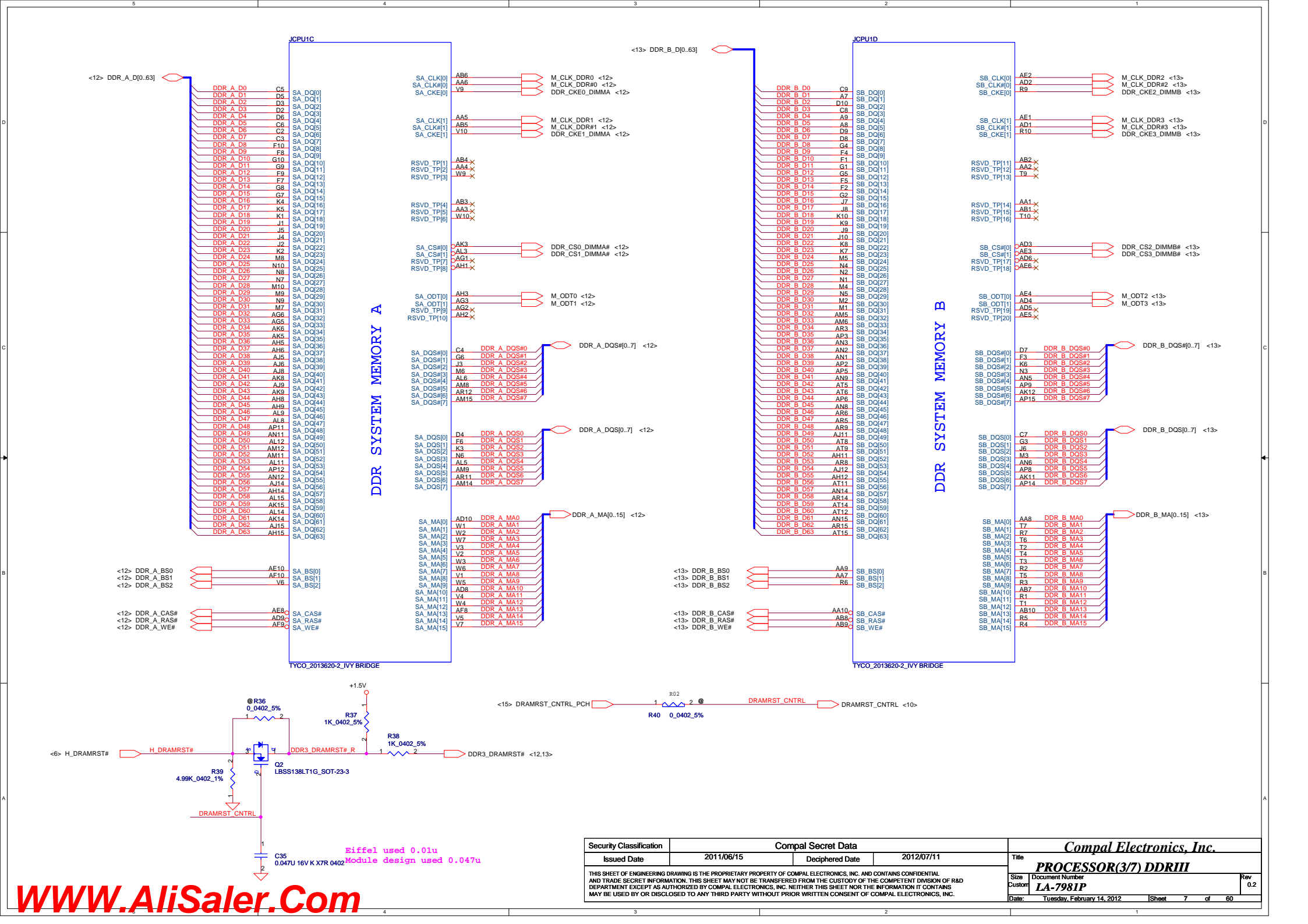
Size Custom
Document Number
LA-7981P
Rev 0.2
Date: Tuesday, February 14, 2012
Sheet 4 of 60

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

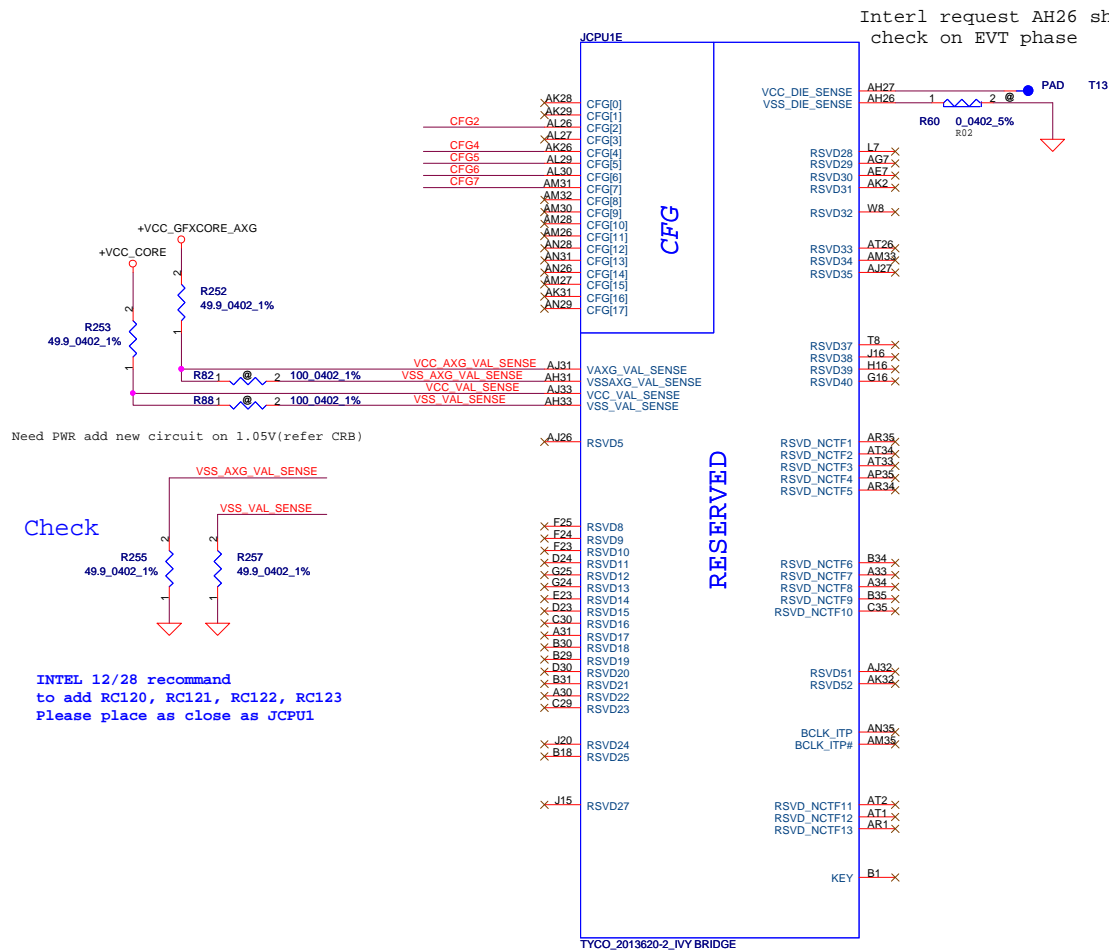


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						Custom		LA-7981P		0.2	
						Date:		Tuesday, February 14, 2012		Sheet 5 of 60	





CFG Straps for Processor



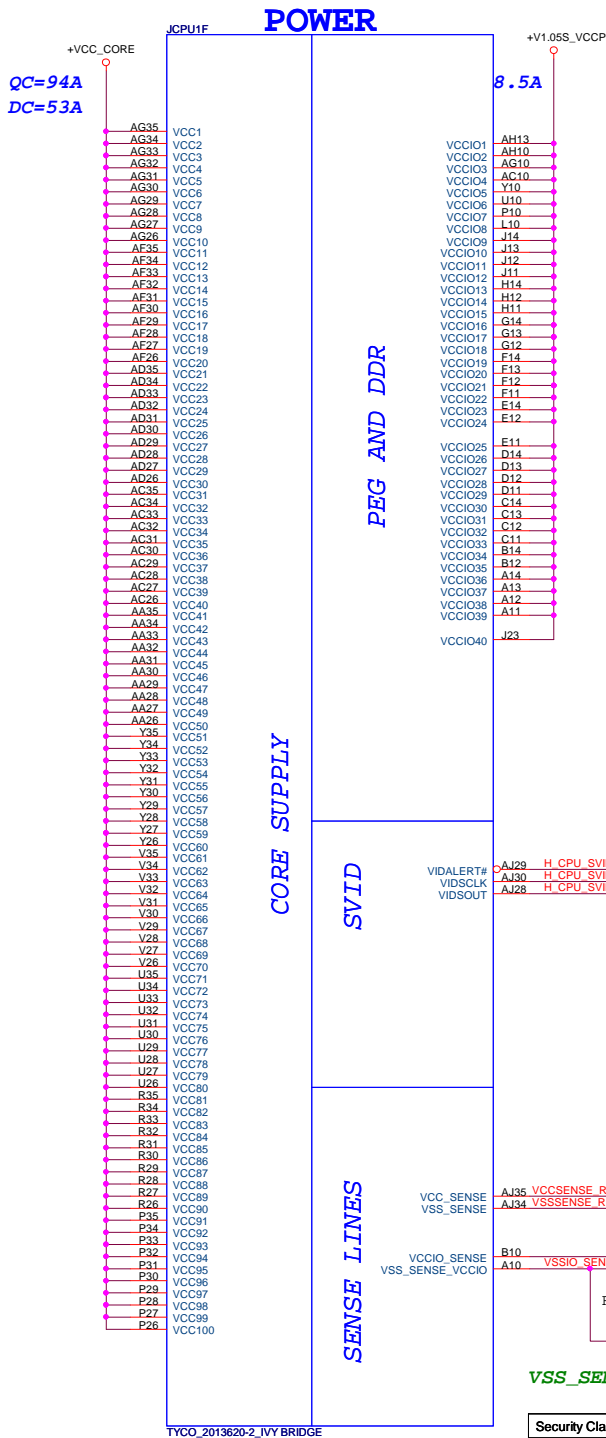
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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				Date	Tuesday, February 14, 2012
				Sheet	8 of 60
				Rev	0.2

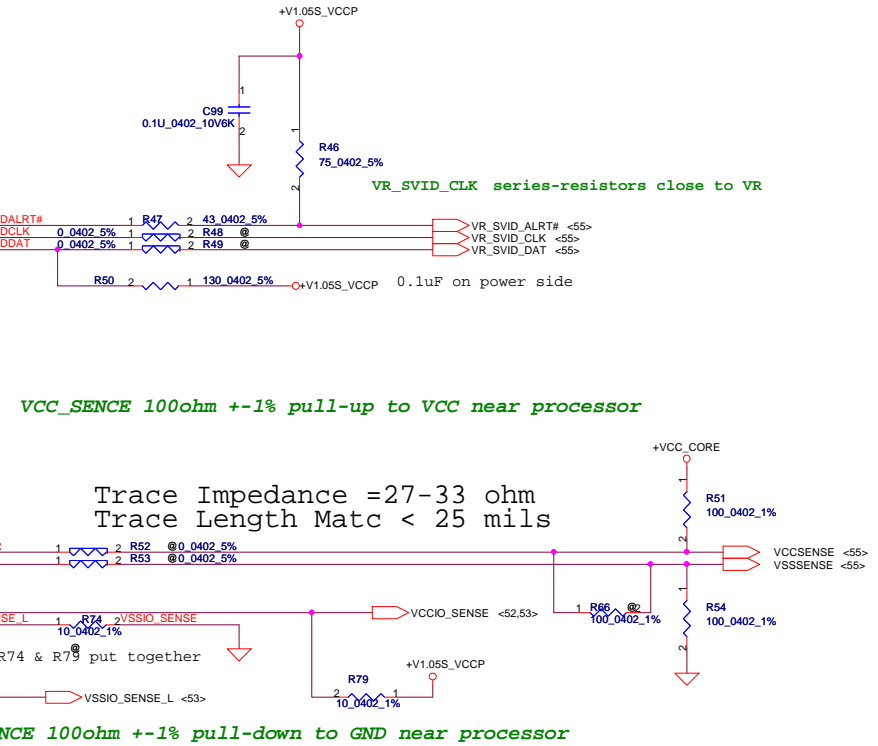


PEG AND DDR

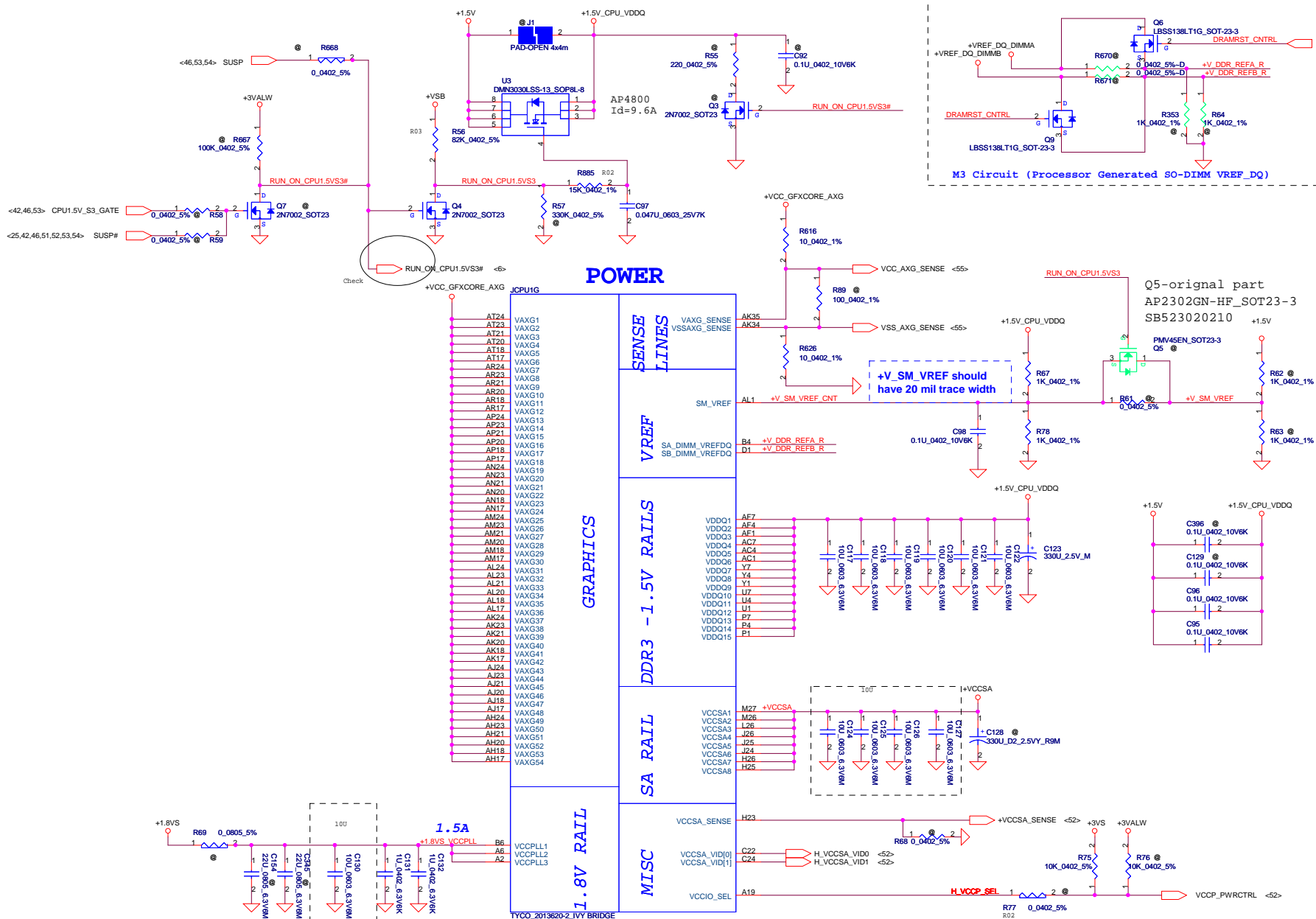
CORE SUPPLY

SVID

SENSE LINES

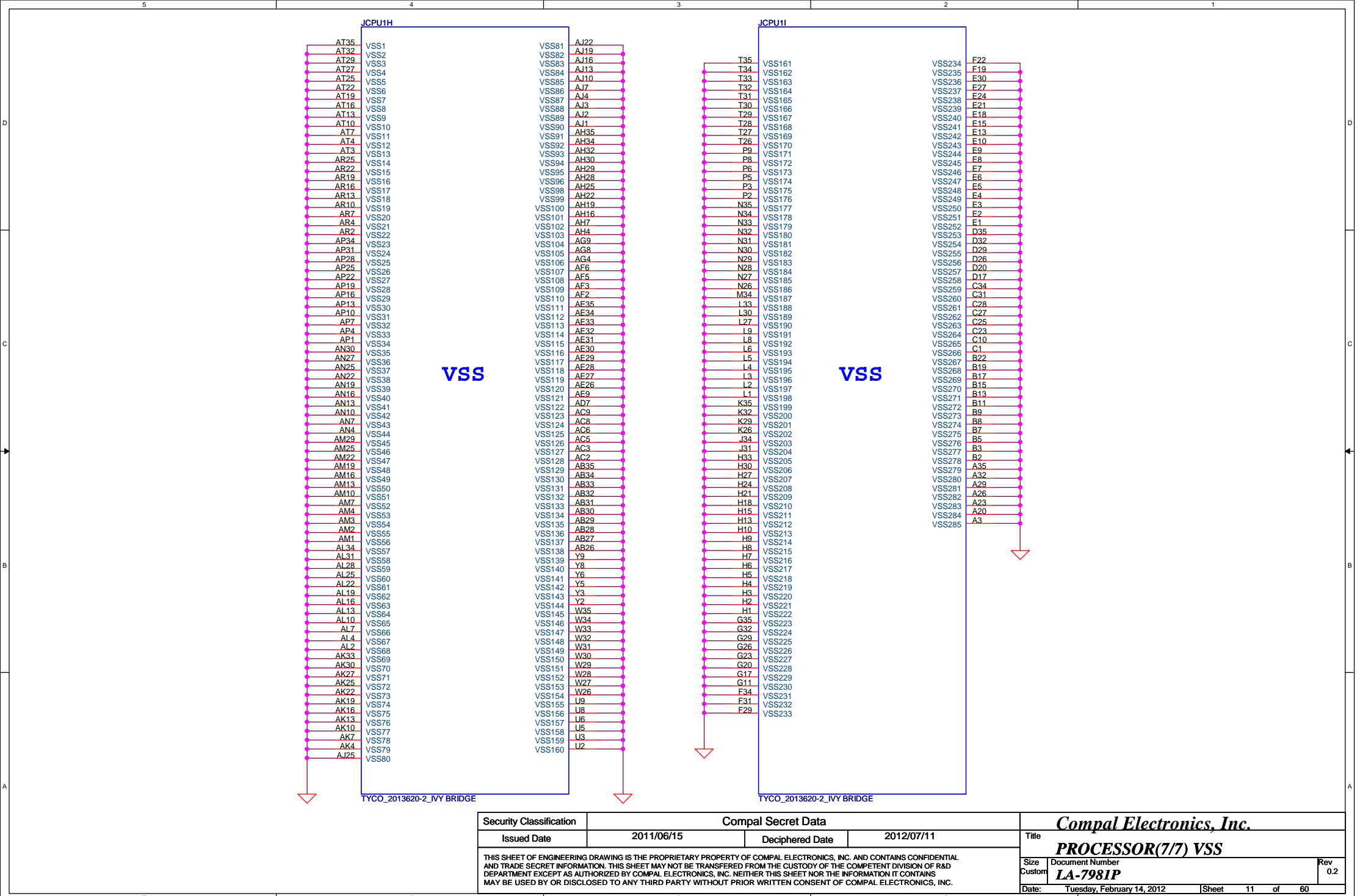


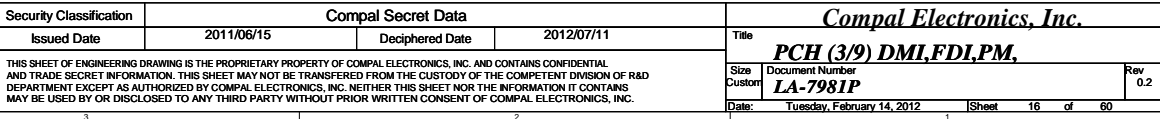
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Date: Tuesday, February 14, 2012				Sheet	9 of 60

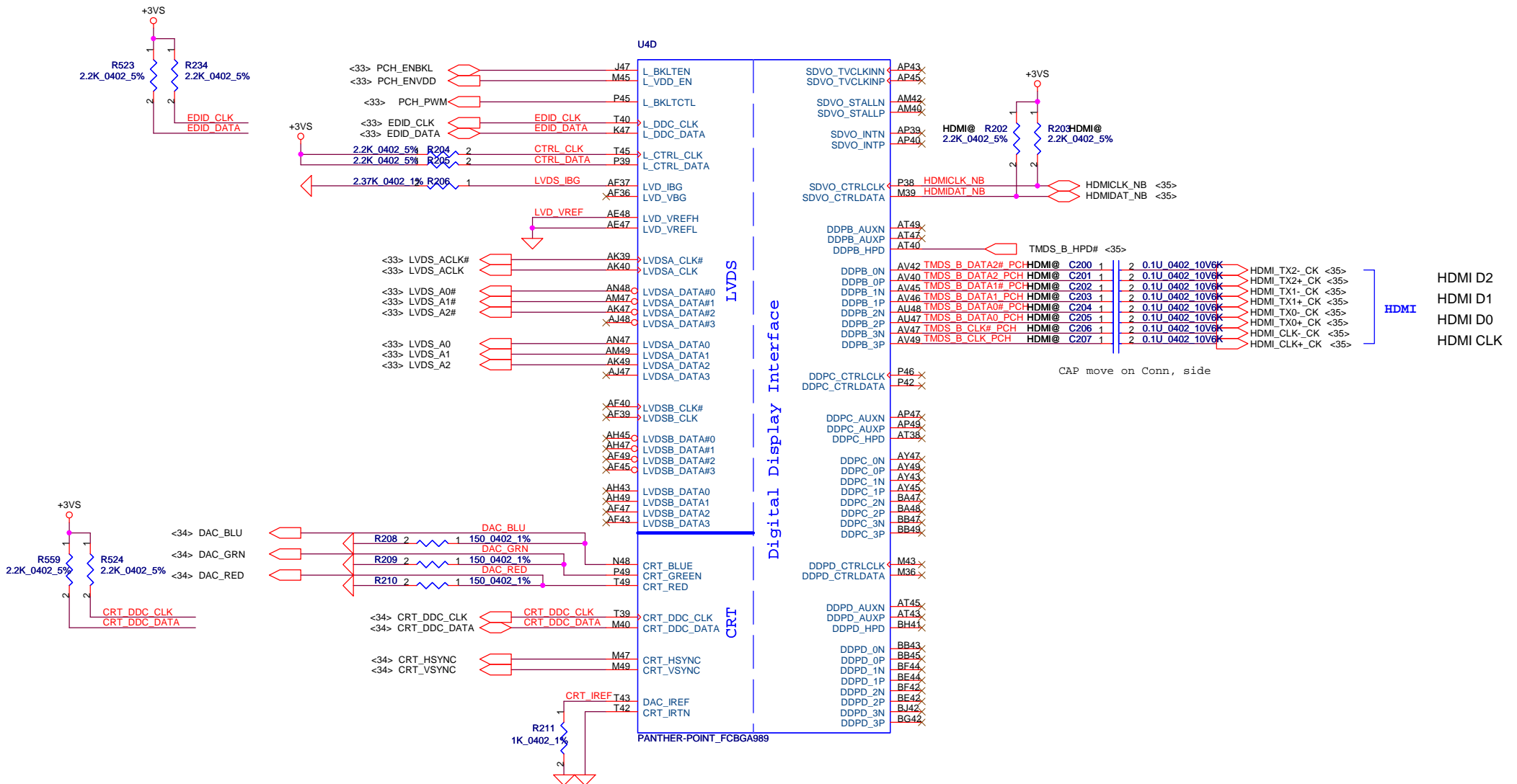


IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0
Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

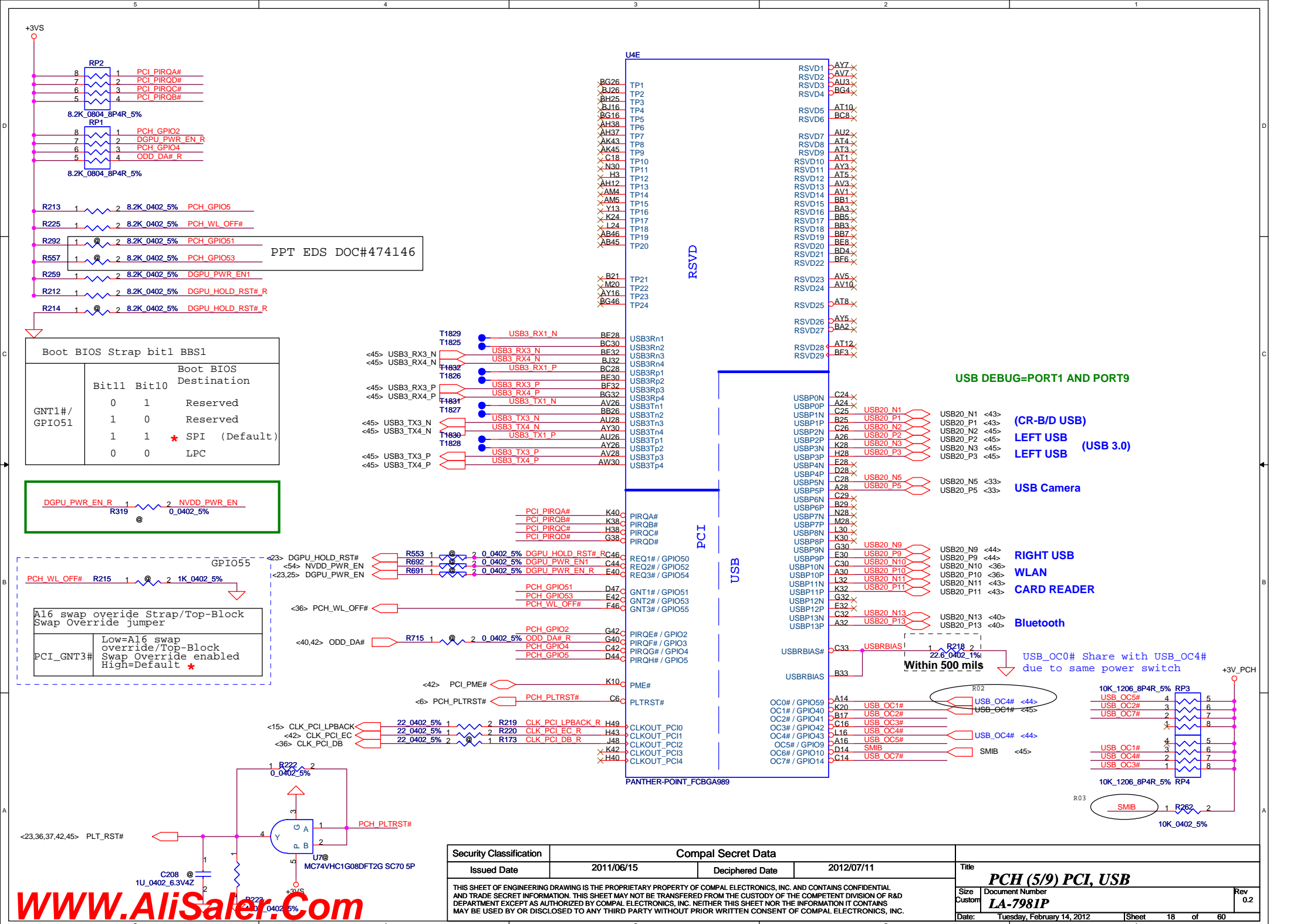
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				Date	Rev
				Tuesday, February 14, 2012	0.2
				Sheet	10 of 60

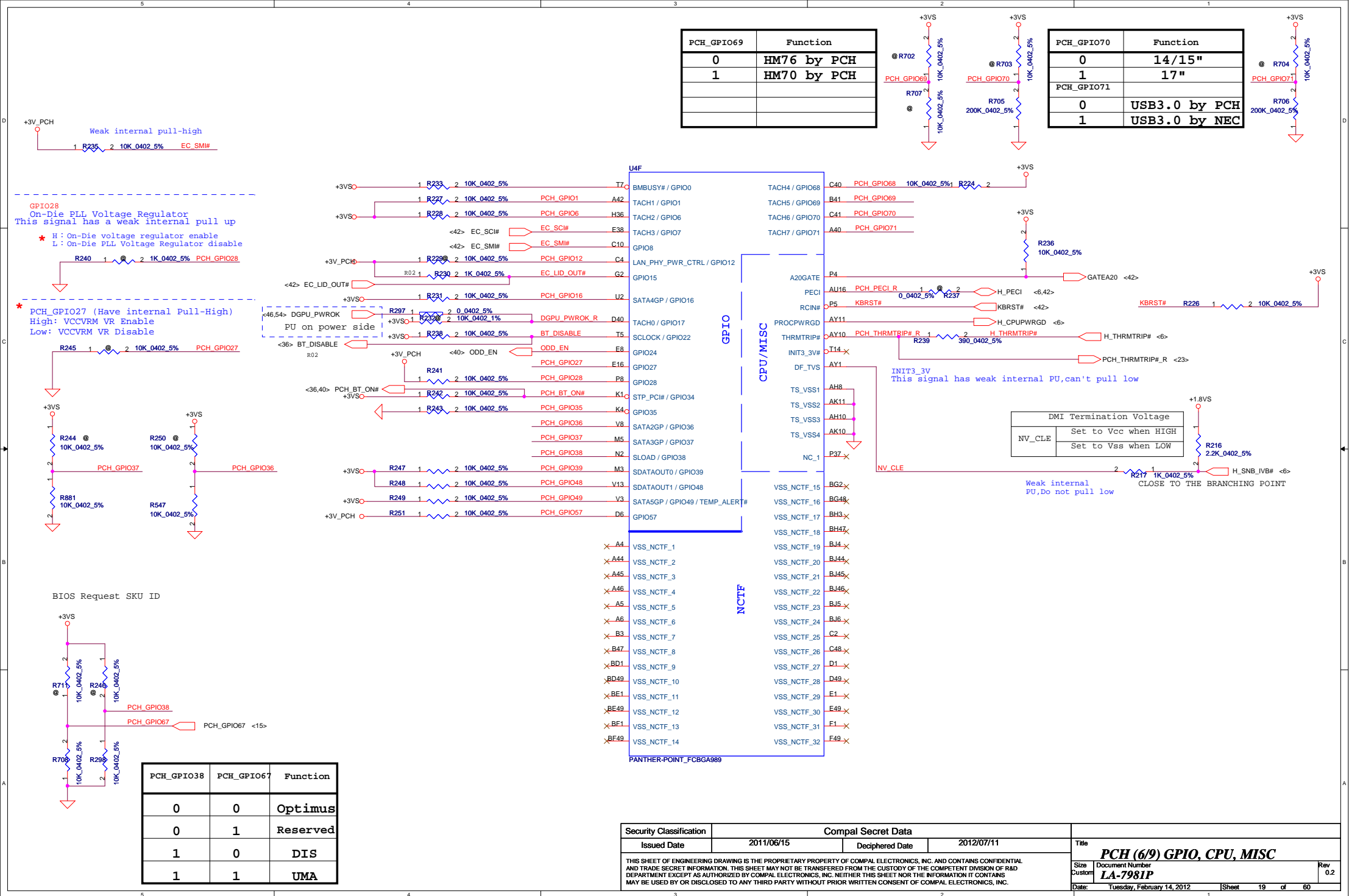


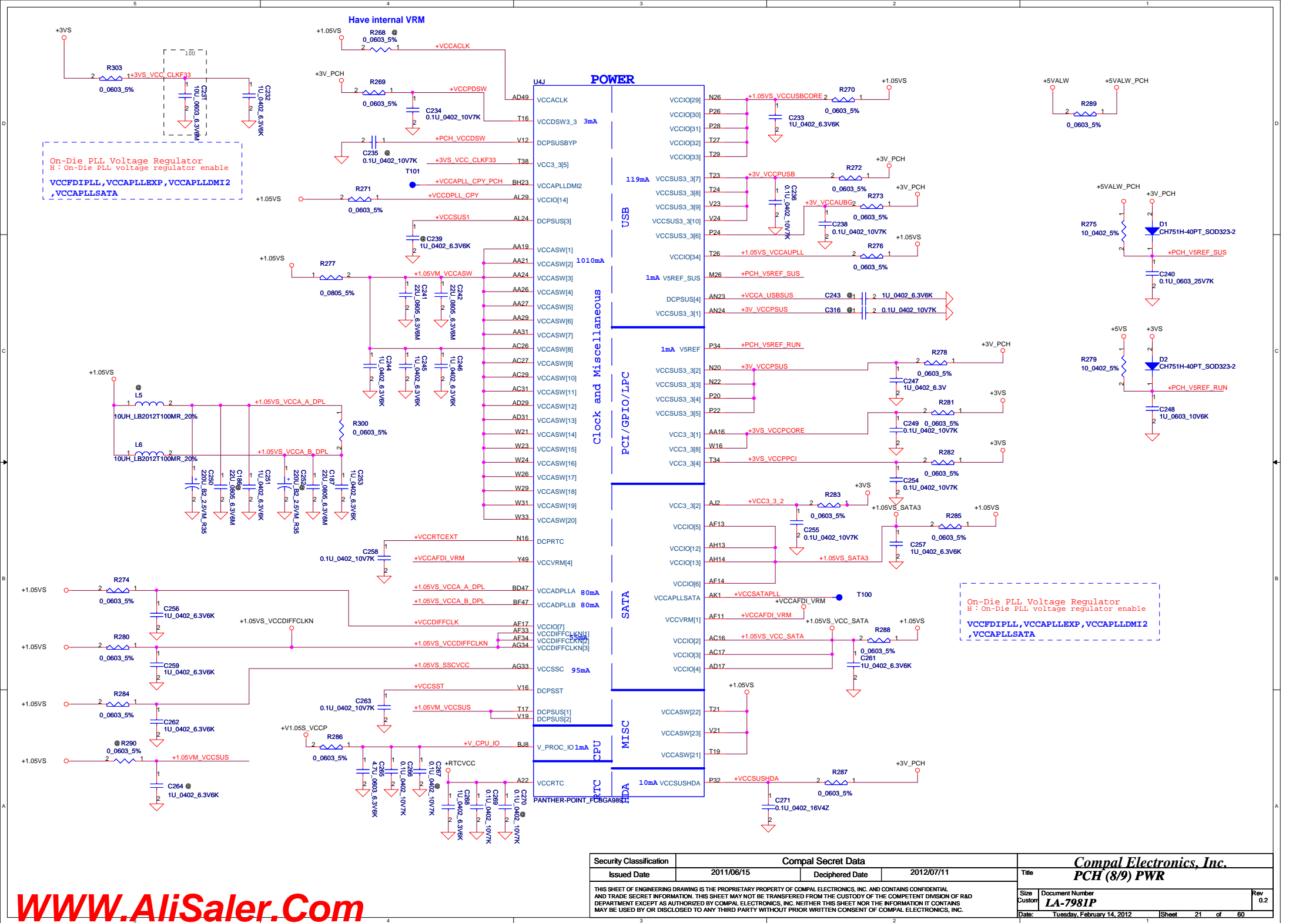




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						Size	Document Number		Rev
						B	LA-7981P		0.2
Date:		Tuesday, February 14, 2012		Sheet 17 of 60					

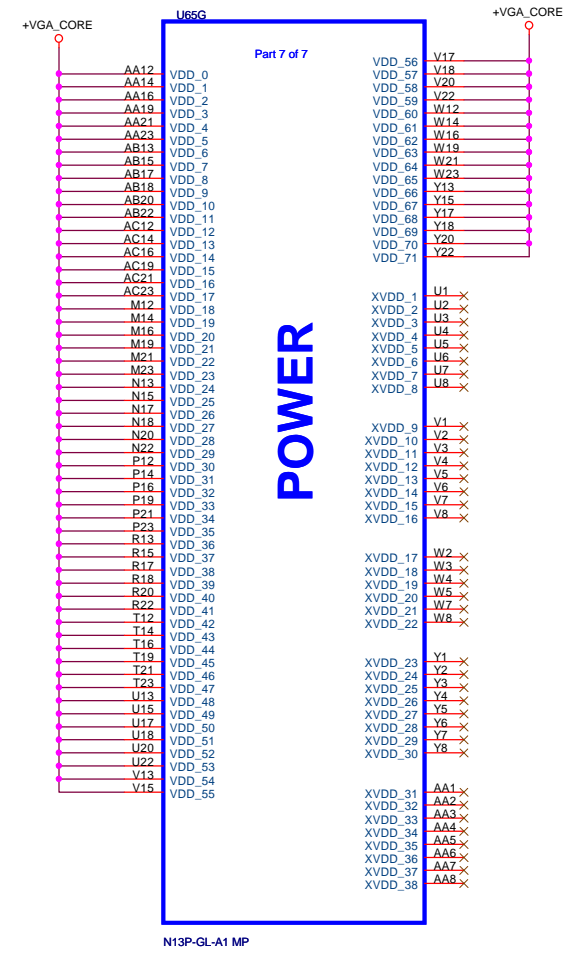
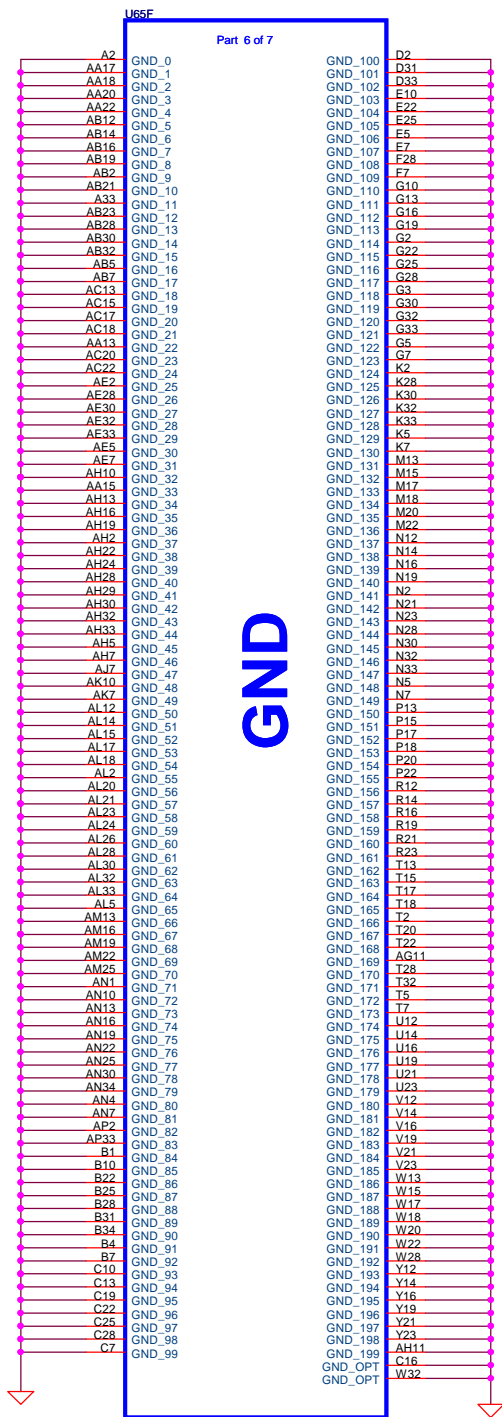






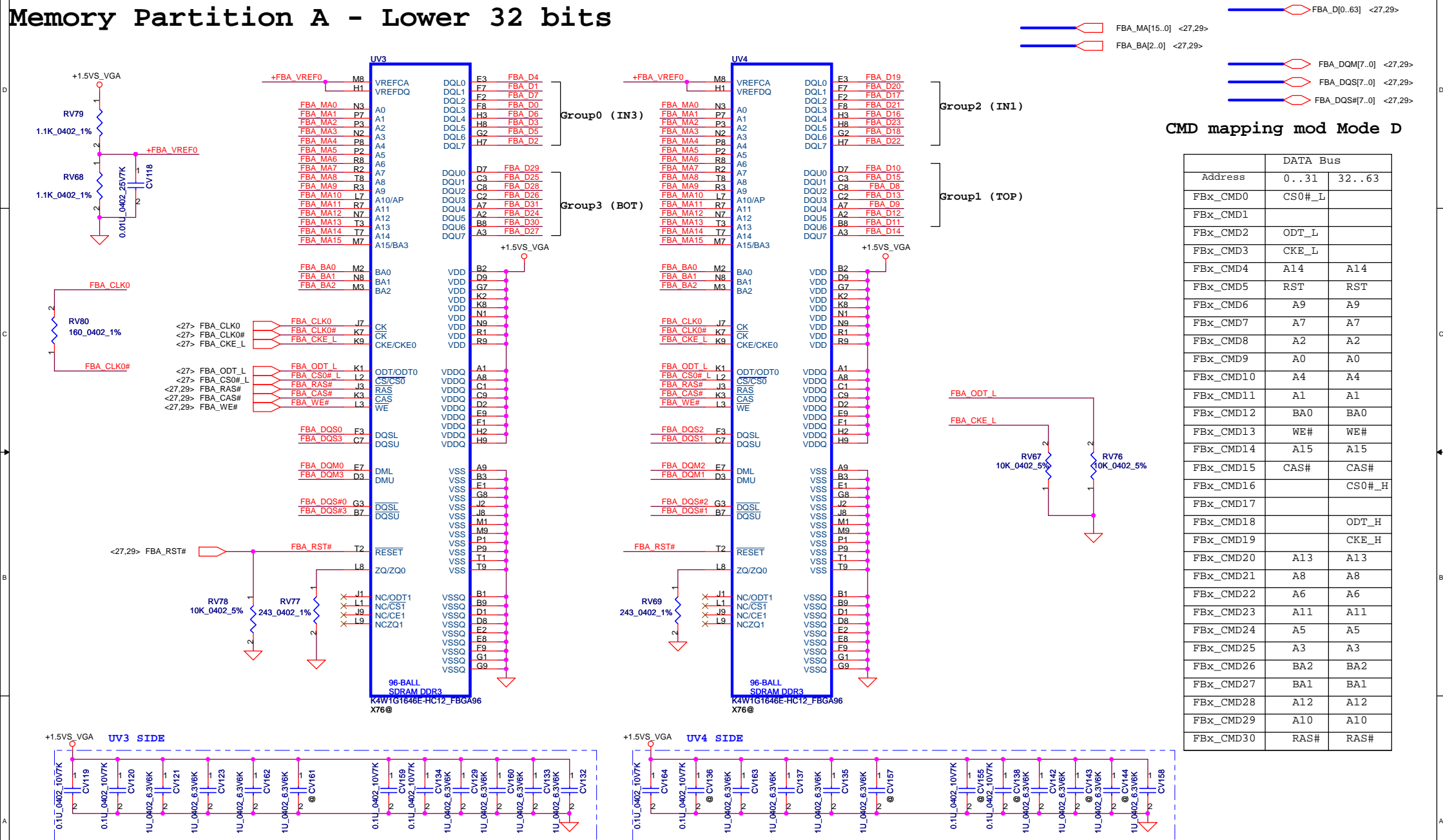
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				Size		Document Number		Rev 0.2
				Custom		LA-7981P		
				Date:		Tuesday, February 14, 2012		





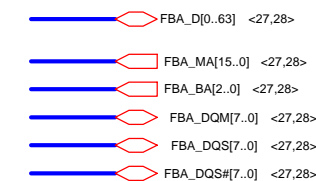
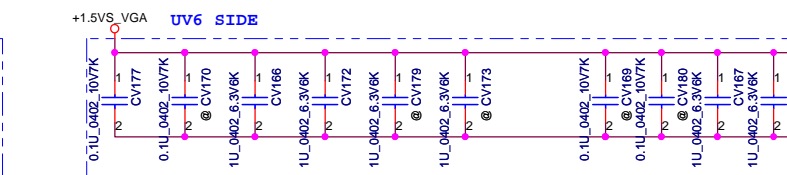
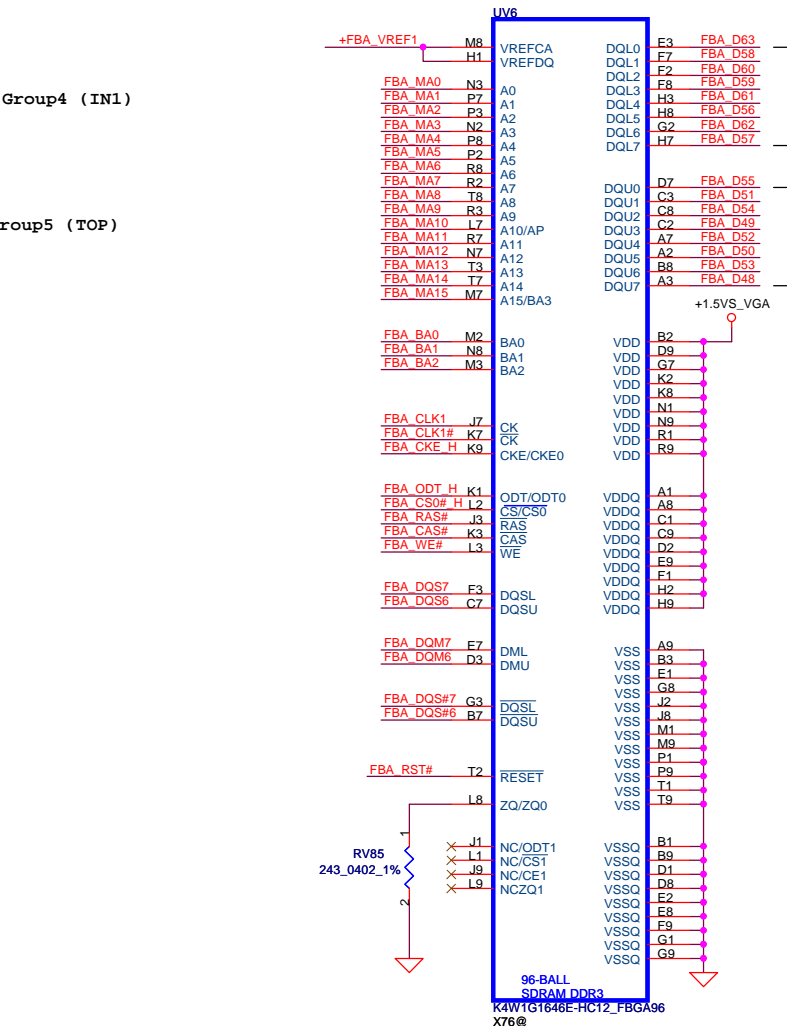
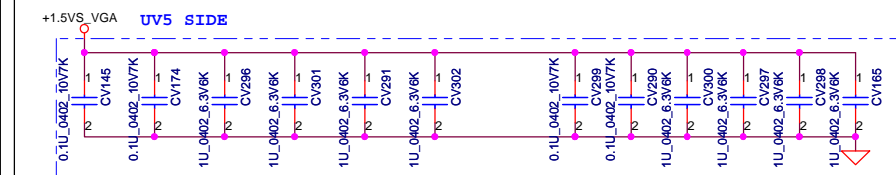
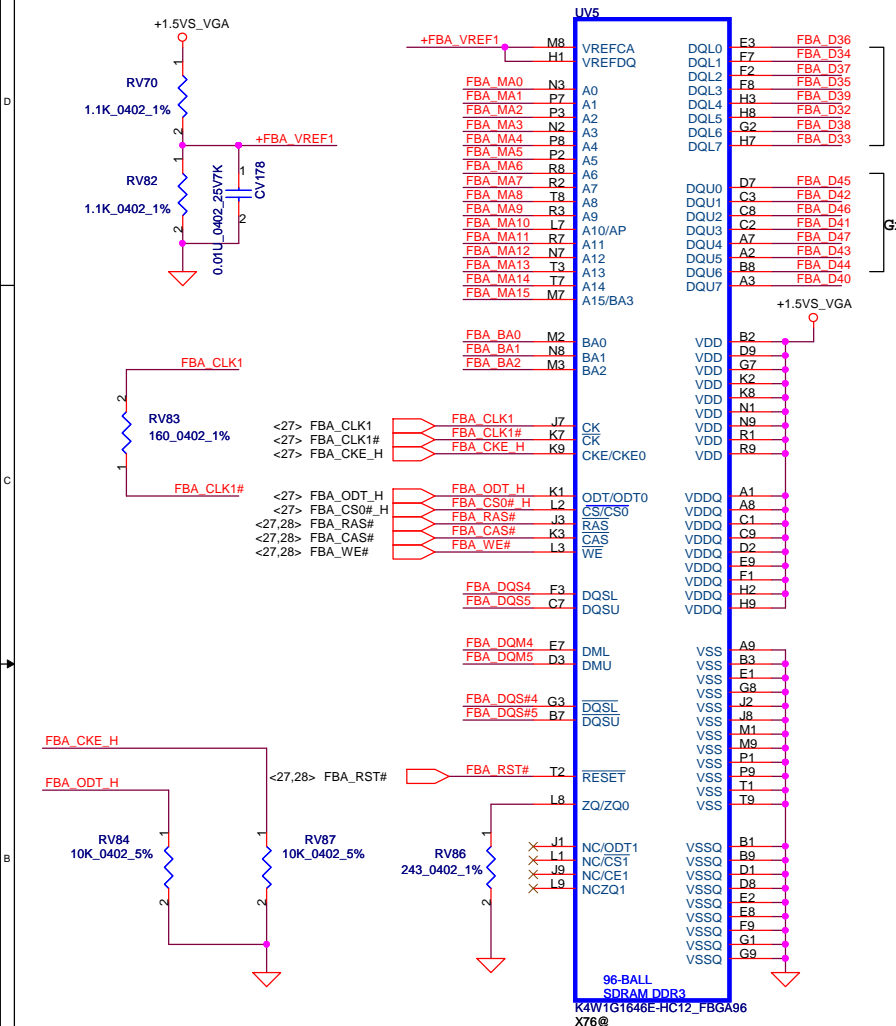
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										LA-7981P		0.2	
								Date:		Tuesday, February 14, 2012		Sheet 26 of 60	

Memory Partition A - Lower 32 bits



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				Sheet	28 of 60

```
Memory Partition A - Upper 32
bits
```

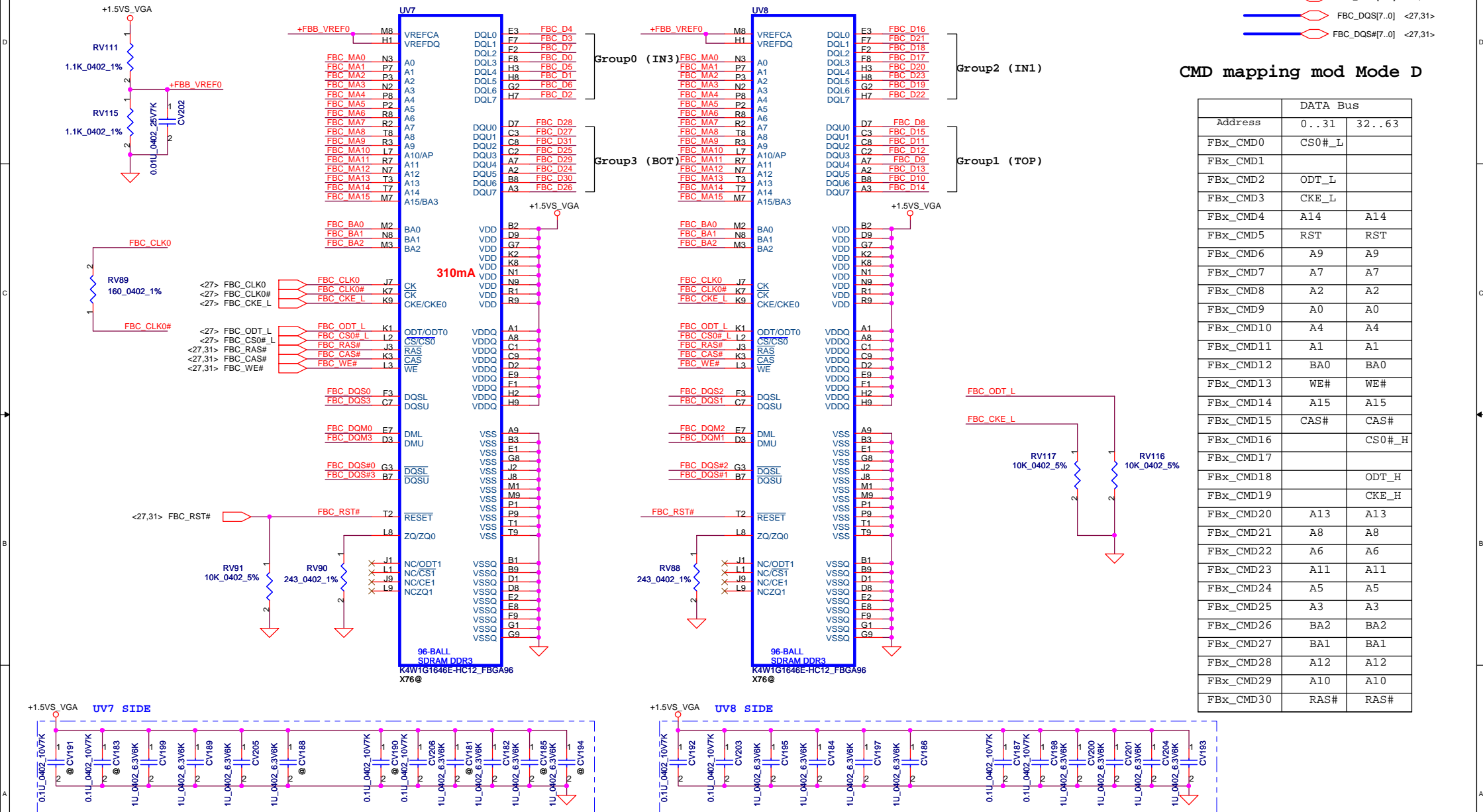


CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

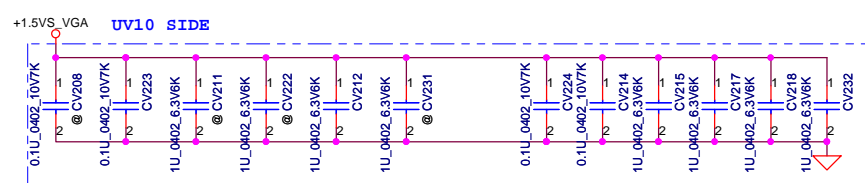
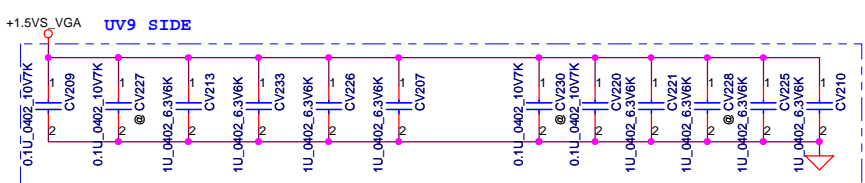
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title N13X-VRAM A Upper		
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				Date:	Tuesday, February 14, 2012	Sheet 29 of 60

Memory Partition C - Lower 32 bits



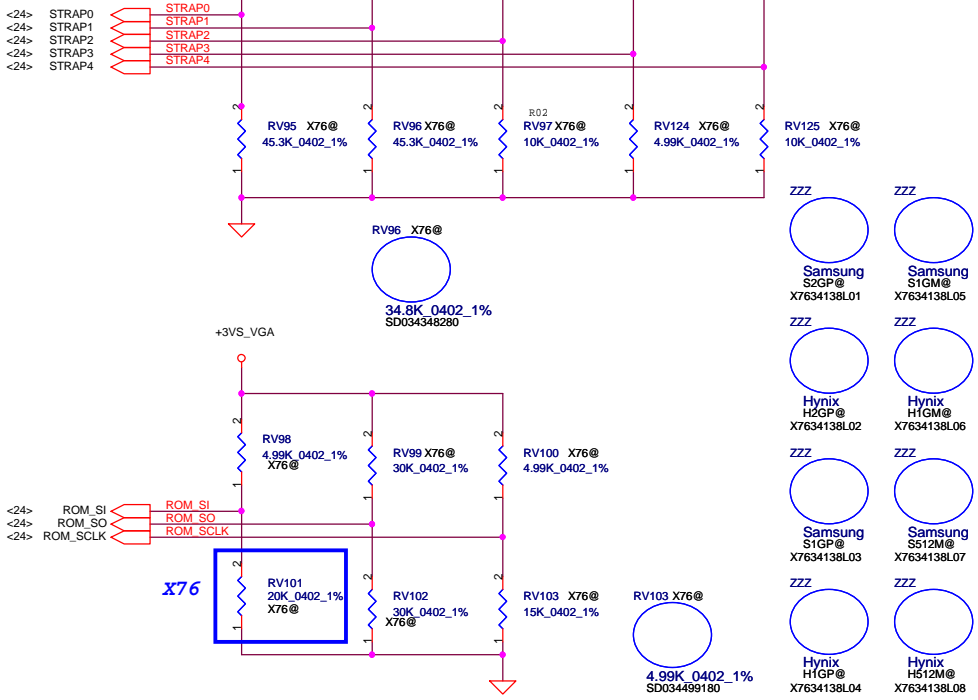
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				Custom	LA-7981P
				Date	Tuesday, February 14, 2012
				Sheet	30 of 60
				Rev	0.2

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	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

<24> STRAP0
<24> STRAP1
<24> STRAP2
<24> STRAP3
<24> STRAP4



For N13P-GL strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8	Samsung (2Gb)	R	R	R	n/a	n/a	PD 45K	PD 10K	PD 15K
N13P-GL	900 MHz	128M* 16* 8	Hynix (2Gb)	R	R	R	n/a	n/a	PD 45K	PD 10K	PD 15K
N13P-GL	900 MHz	64M* 16* 8	Samsung (1Gb)	R	R	R	n/a	n/a	PD 45K	PD 10K	PD 15K
N13P-GL	900 MHz	64M* 16* 8	Hynix (1Gb)	R	R	R	n/a	n/a	PD 45K	PD 10K	PD 15K

For N13M-GE strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GE	900 MHz	128M* 16* 4	Samsung (2Gb)	R	R	R	R	R	PD 10K	PD 10K	PD 10K
N13M-GE	900 MHz	128M* 16* 4	Hynix (2Gb)	R	R	R	R	R	PD 10K	PD 10K	PD 10K
N13M-GE	900 MHz	64M* 16* 4	Samsung (1Gb)	R	R	R	R	R	PD 10K	PD 10K	PD 10K
N13M-GE	900 MHz	64M* 16* 4	Hynix (1Gb)	R	R	R	R	R	PD 10K	PD 10K	PD 10K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

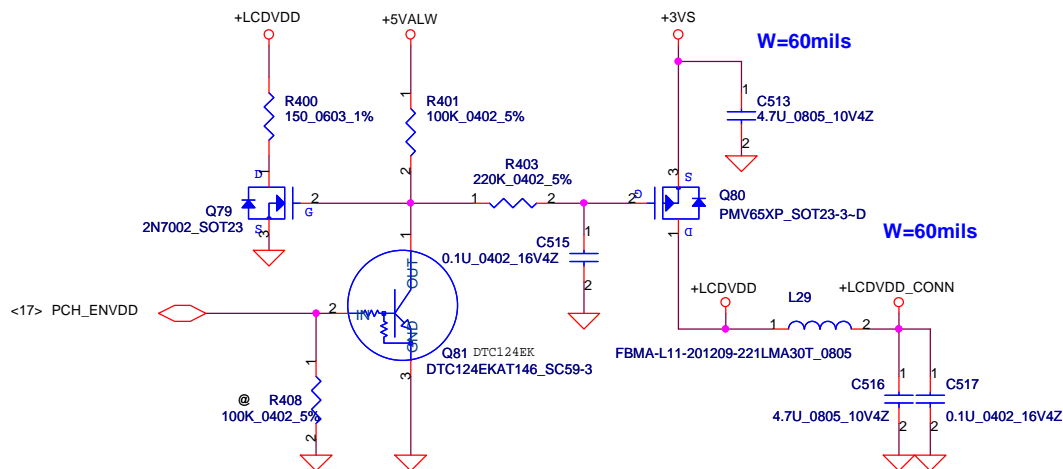
VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

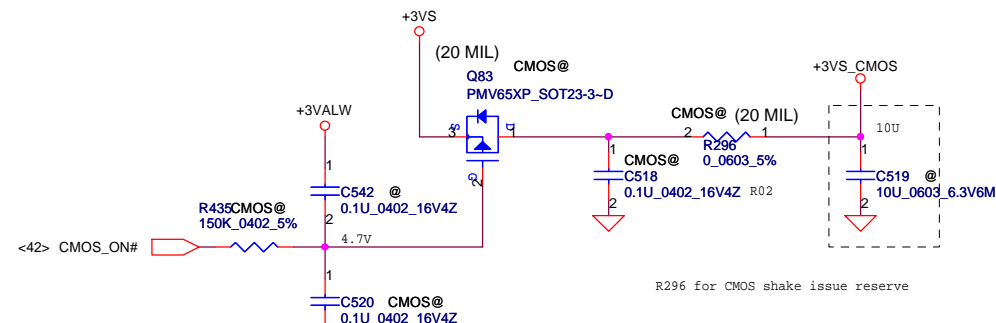
PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

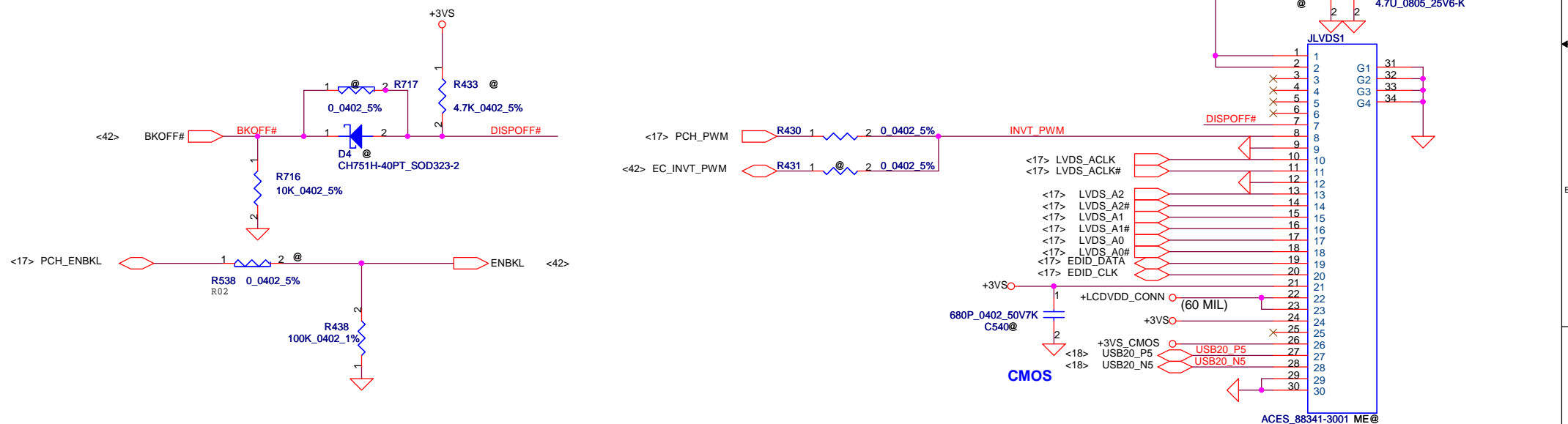
LCD POWER CIRCUIT



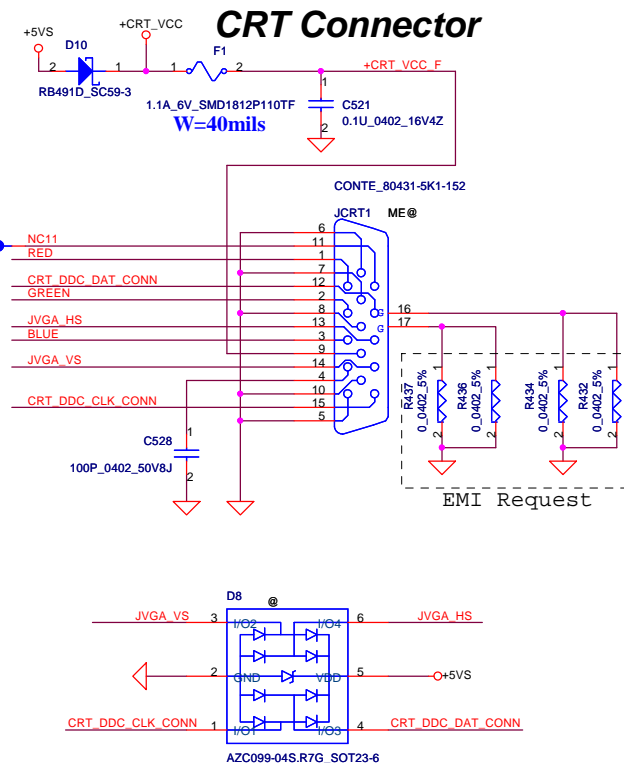
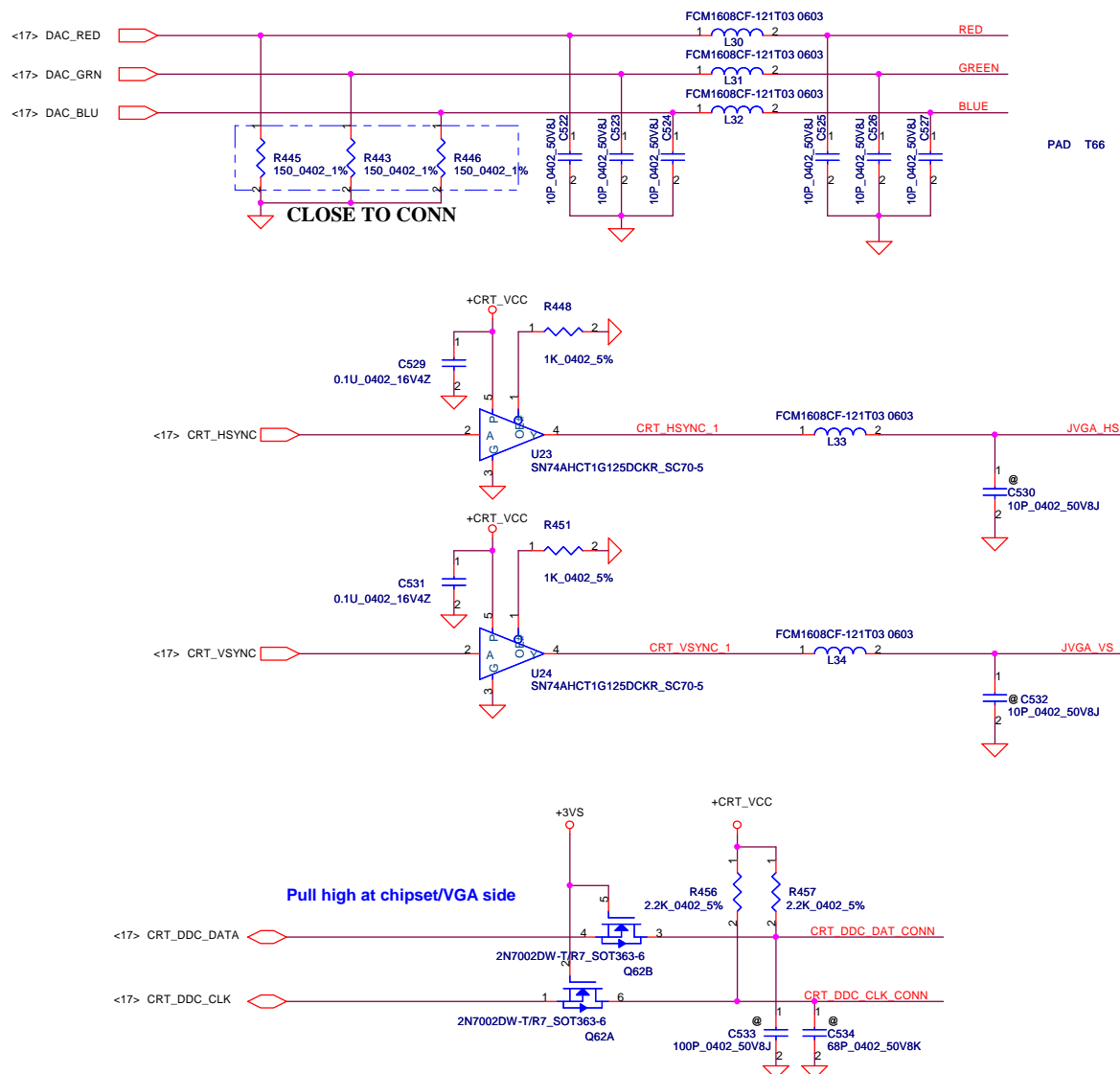
CMOS Camera



VGA LCD/PANEL BD. Conn.

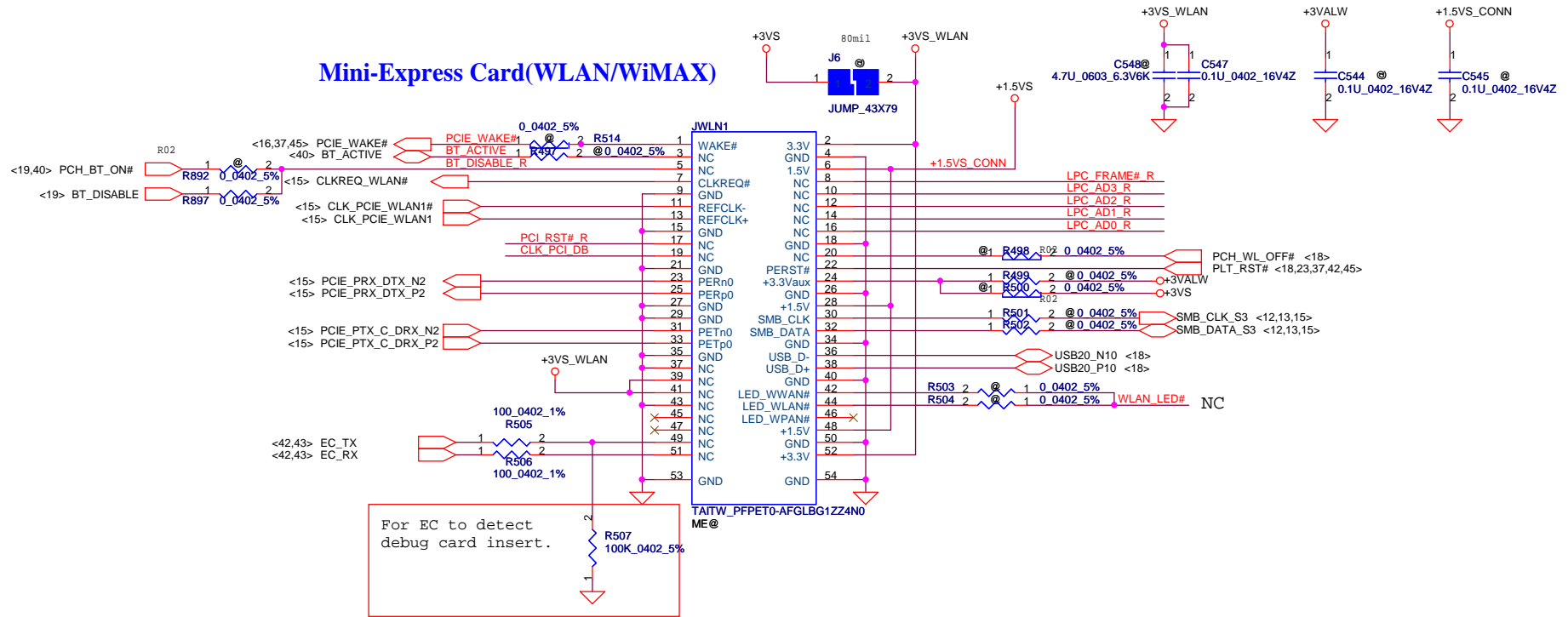


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Size	Custom	Document Number	LA-7981P		Rev 0.2
Date:	Tuesday, February 14, 2012	Sheet	33	of	60



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				Custom	LA-7981P
				Date:	Tuesday, February 14, 2012
				Sheet	34 of 60
				Rev	0.2

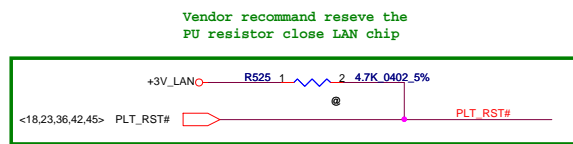
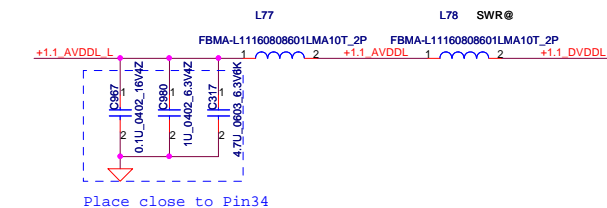
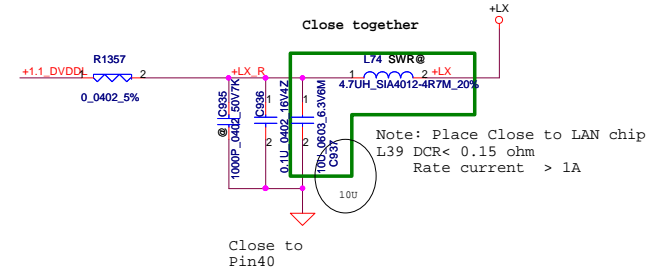
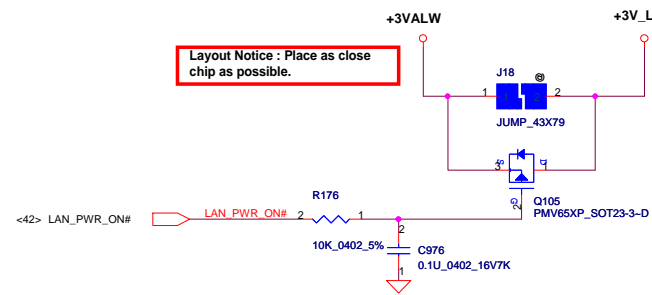
Mini-Express Card for WLAN/WiMAX(Half)



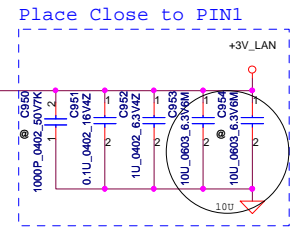
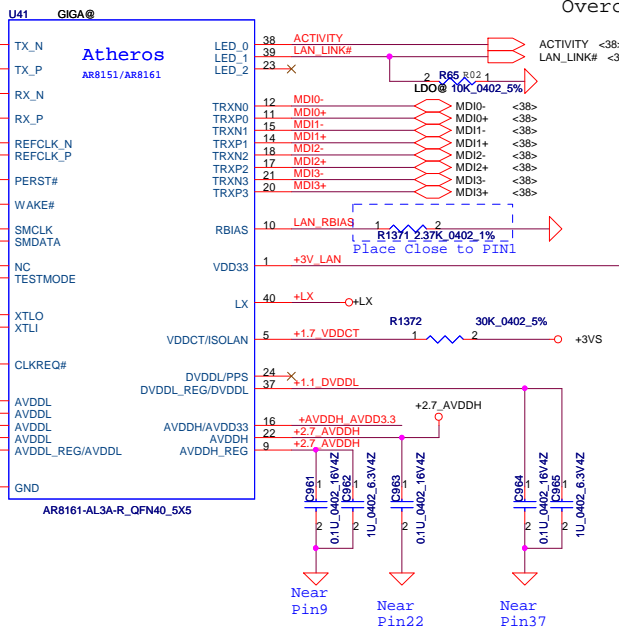
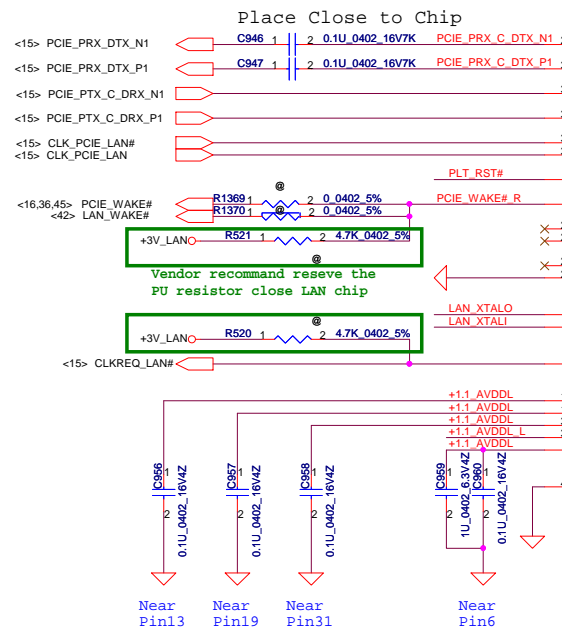
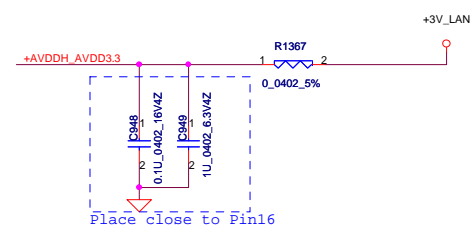
**Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.**

LPC_FRAME# R	R508	1	2	0.0402 5%	LPC_FRAME#	LPC_FRAME# <14,42>
LPC_AD3 R	R509	1	2	0.0402 5%	LPC_AD3	LPC_AD3 <14,42>
LPC_AD2 R	R510	1	2	0.0402 5%	LPC_AD2	LPC_AD2 <14,42>
LPC_AD1 R	R511	1	2	0.0402 5%	LPC_AD1	LPC_AD1 <14,42>
LPC_AD0 R	R512	1	2	0.0402 5%	LPC_AD0	LPC_AD0 <14,42>
PLT_RST#	R513	1	2	0.0402 5%	PLT_RST#	PLT_RST# <18>
CLK_PCI_DB					CLK_PCI_DB	CLK_PCI_DB <18>

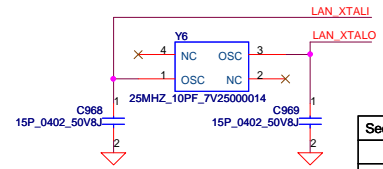
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				Size	Document Number
				LA-7981P	
				Date	Tuesday, February 14, 2012
				Sheet	36 of 60
				Rev	0.2



SA000050E00_S IC AR8161-AL3A-R QFN 40P E-LAN CTRL
 SA000052J10_S IC AR8162-AL3A-R QFN 40P E-LAN CTRL
 H --> Overclocking mode
 L --> Not overclocking mode

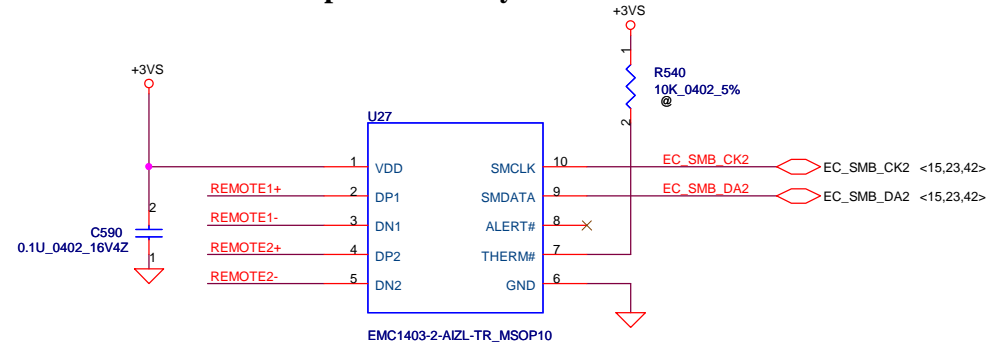
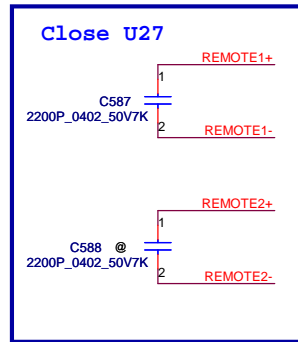


3.3V : Enable switching regulator
 0V : Disable switching regulator

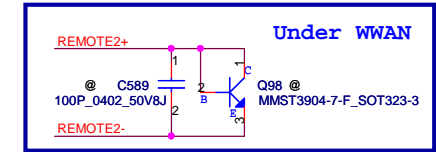
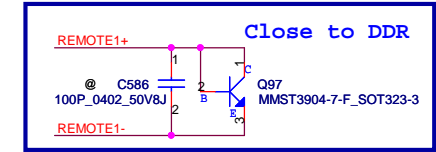


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				Custom	LA-7981P
				Date	Tuesday, February 14, 2012
				Sheet	37 of 60
				Rev	0.2

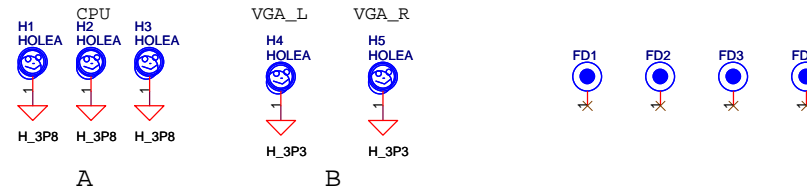
SMSC thermal sensor placed near by VRAM



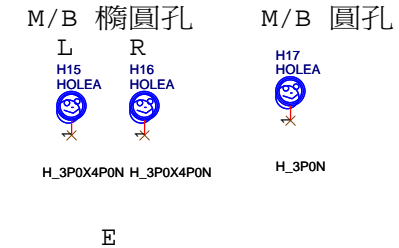
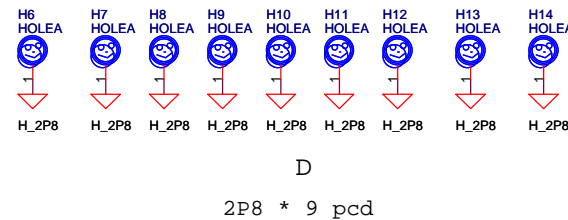
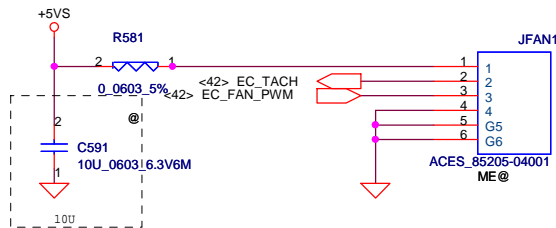
Address 1001_101xb



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

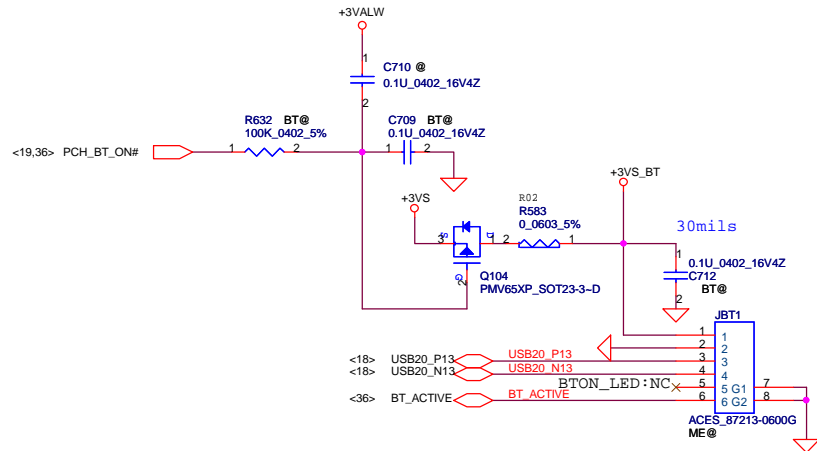


FAN1 Conn

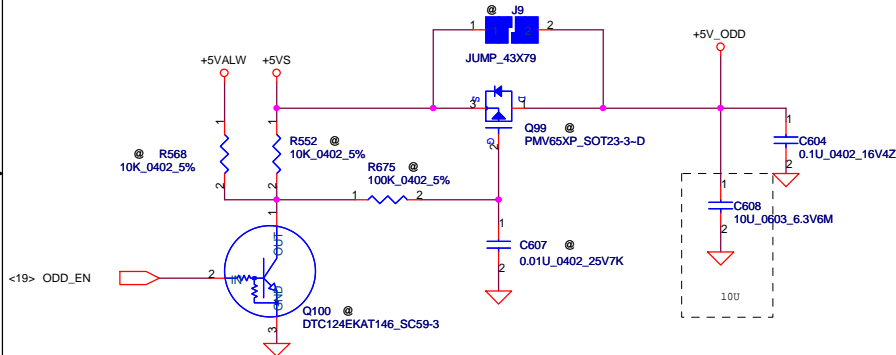


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				Document Number LA-7981P	
				Date: Tuesday, February 14, 2012	Sheet 39 of 60

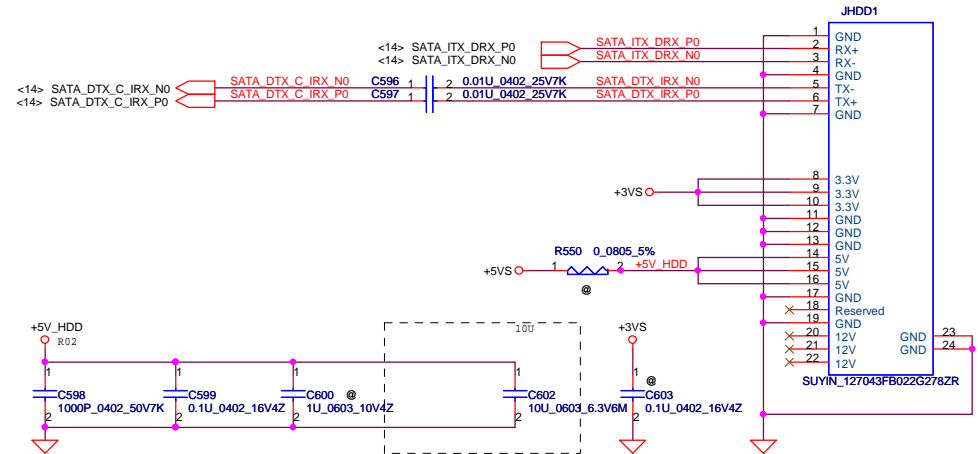
BT MODULE CONN



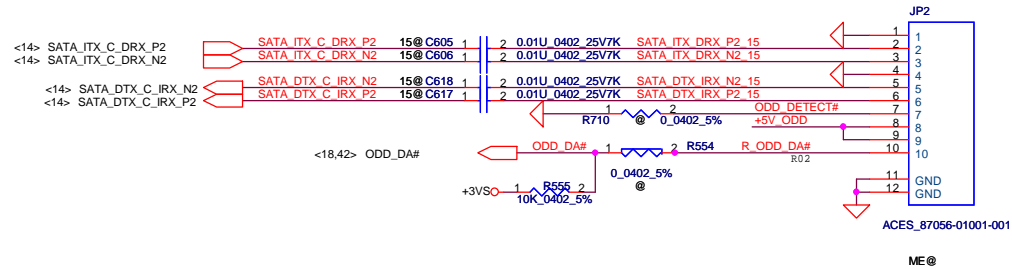
ODD Power Control



SATA HDD Conn.

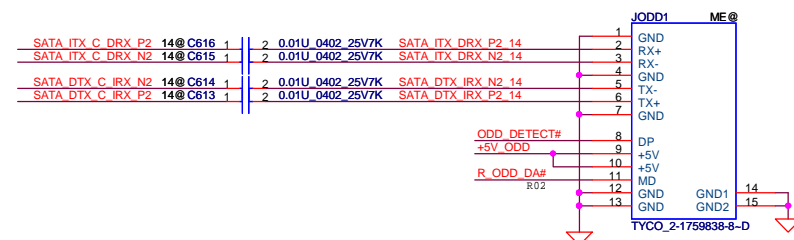


FOR 15"
SATA ODD FFC Conn.



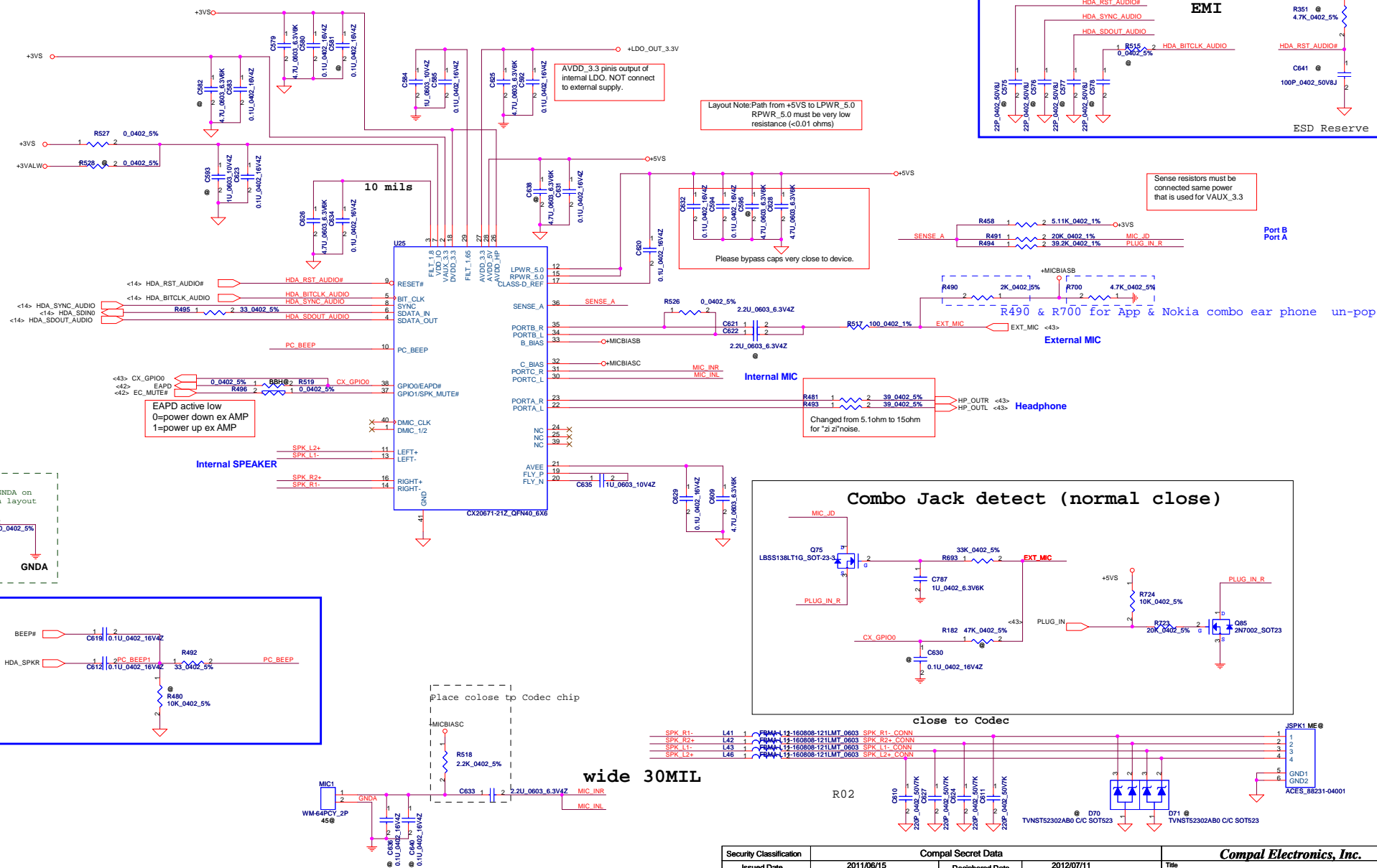
Co-lay

FOR 14"
SATA ODD Conn.



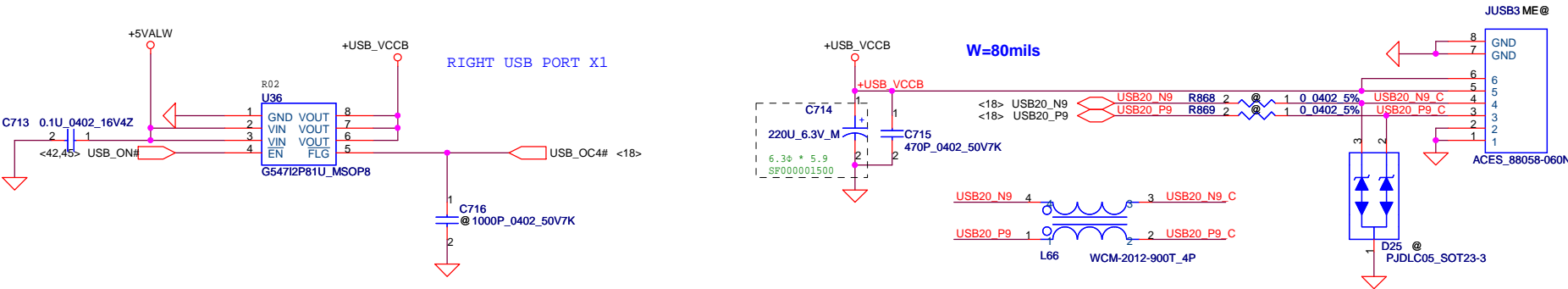
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
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				Date:	Tuesday, February 14, 2012
				Sheet	40 of 60

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

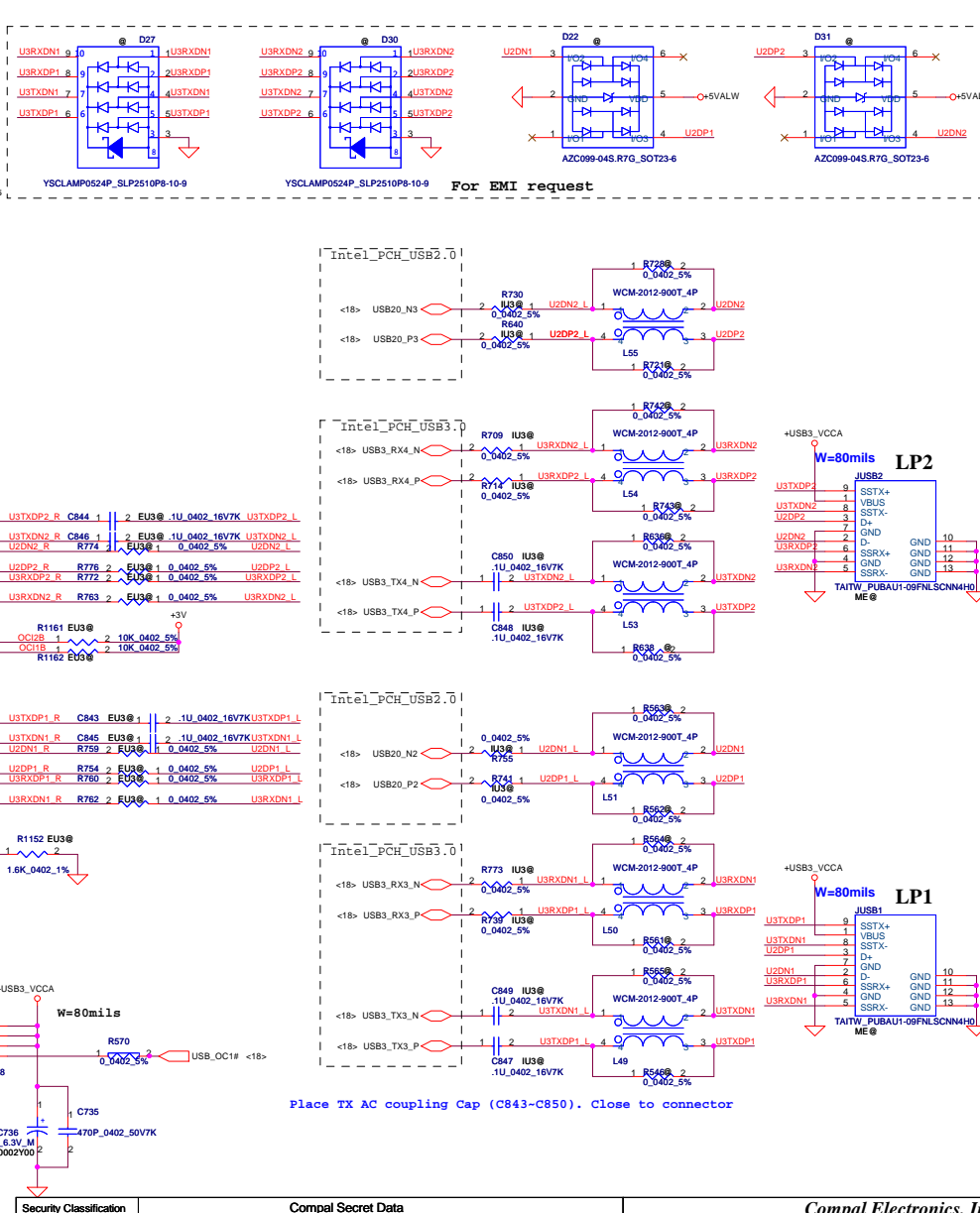
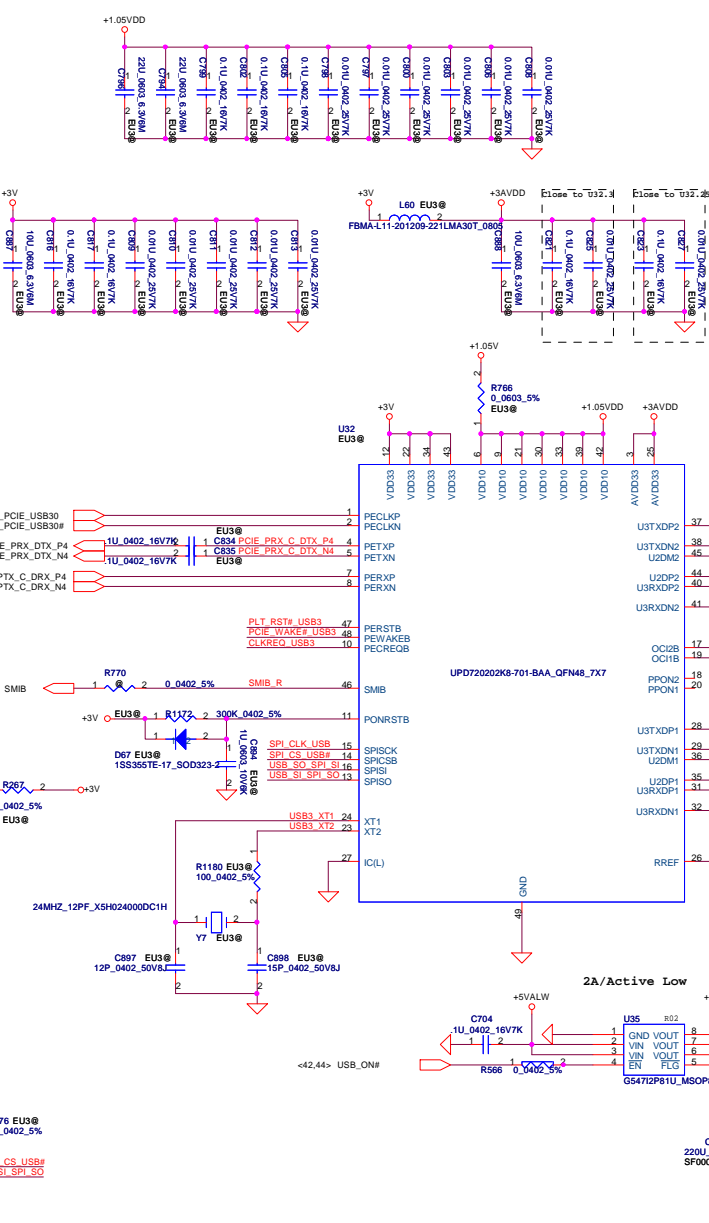
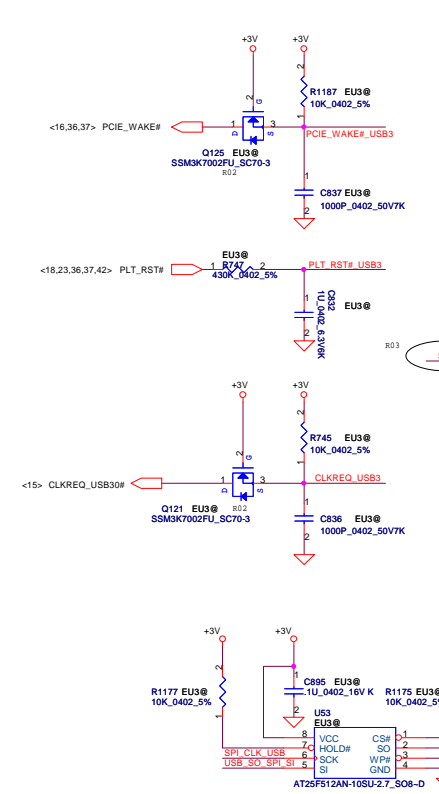
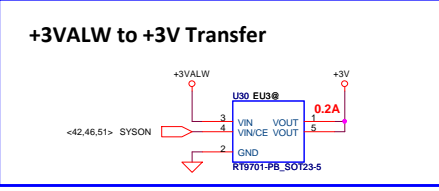
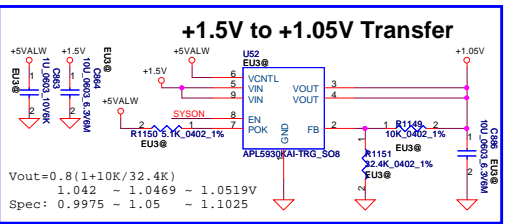




Right Ext.USB Conn.

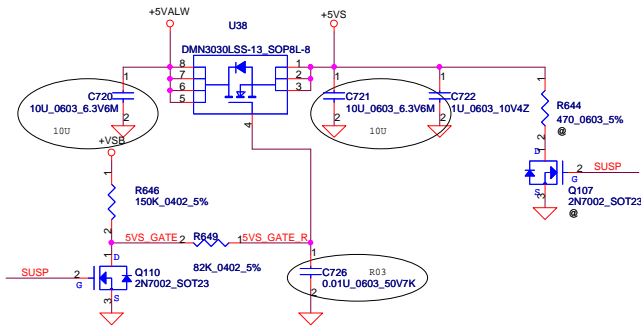


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				Size B	Document Number	Rev 0.2
				LA-7981P		
				Date:	Tuesday, February 14, 2012	Sheet 44 of 60

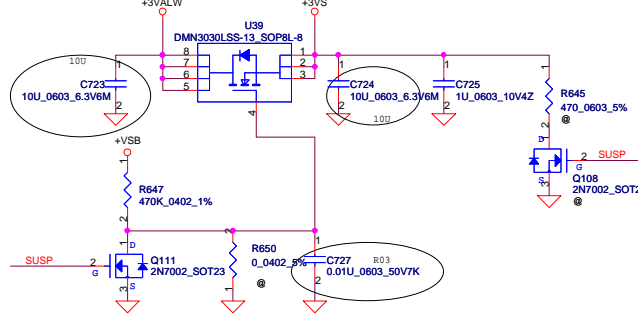


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				45				of			

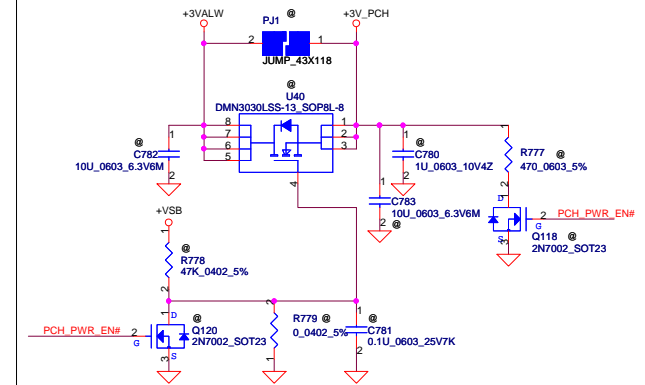
+5VALW TO +5VS



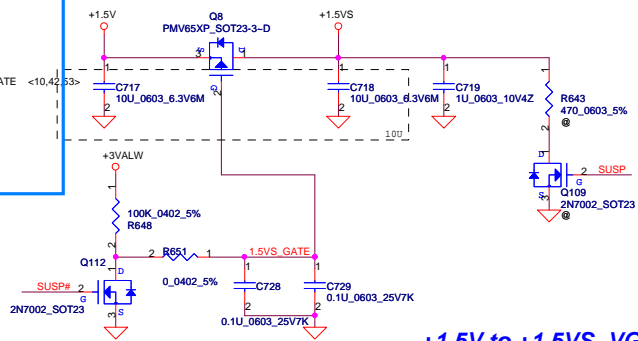
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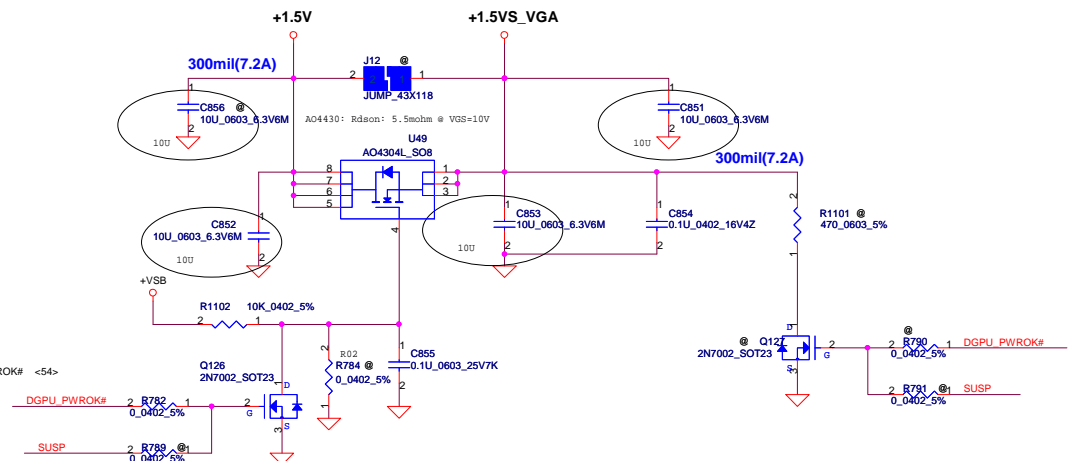
+3VALW TO +3VALW(PCH AUX Power)



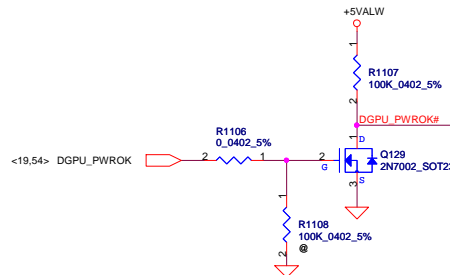
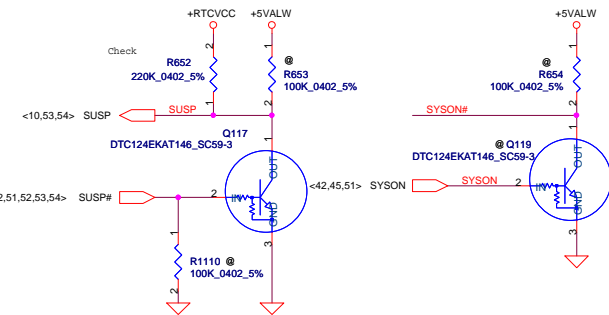
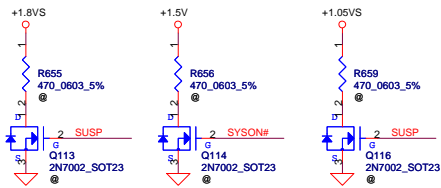
+1.5V to +1.5VS



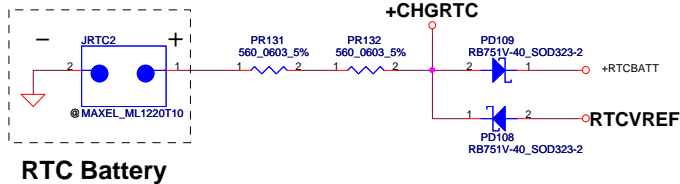
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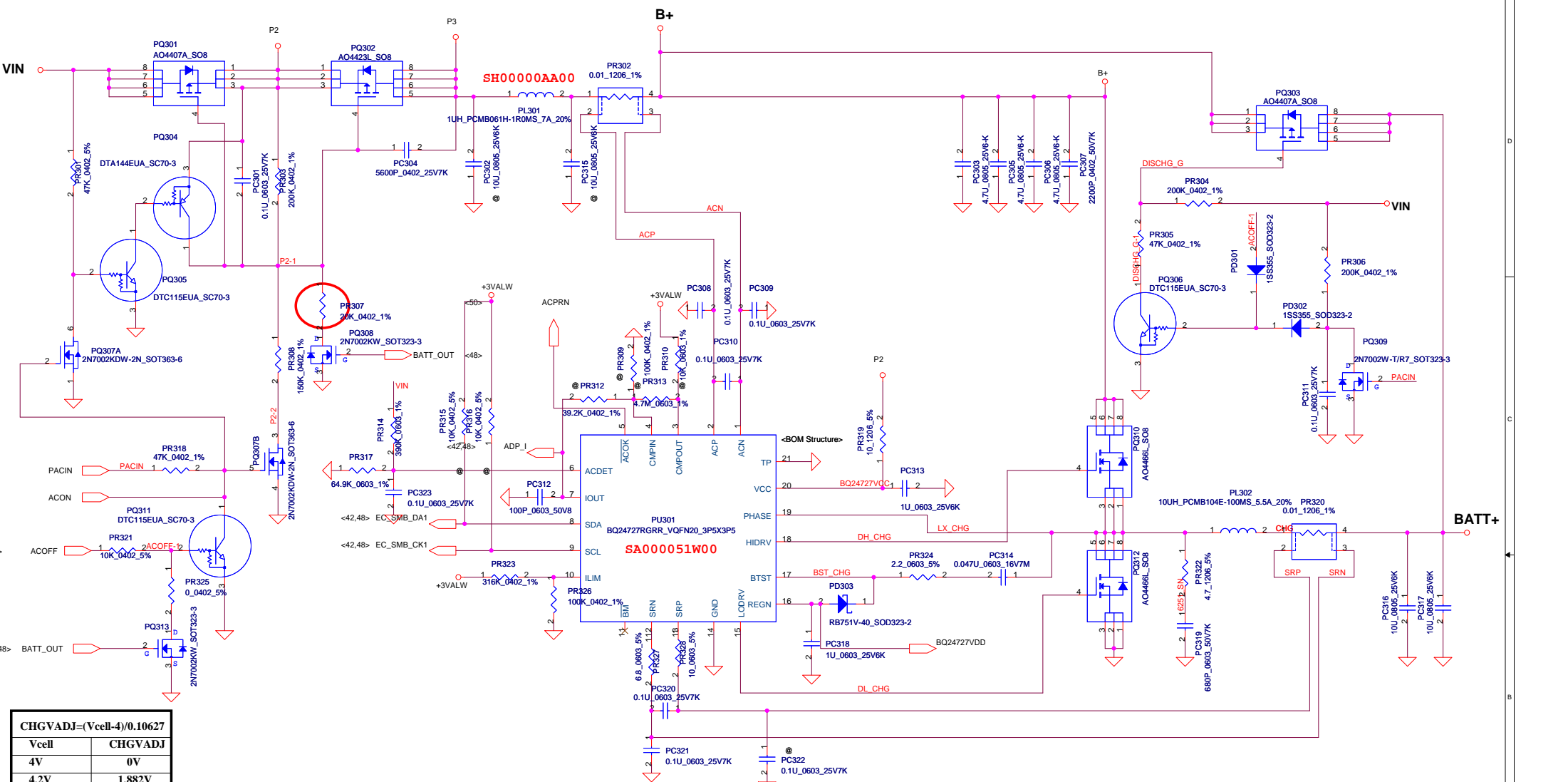


For Intel S3 Power Reduction.



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Date:				Tuesday, February 14, 2012				Sheet 46 of 60			

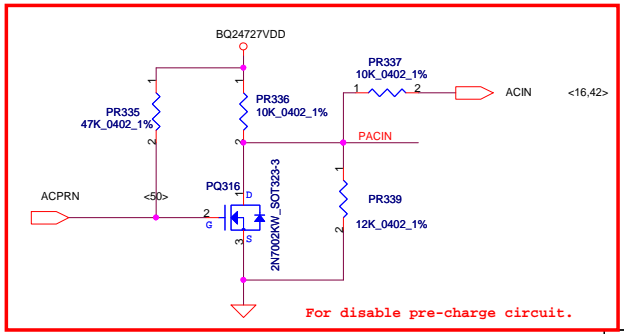
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CHGVADJ=(Vcell-4)/0.10627

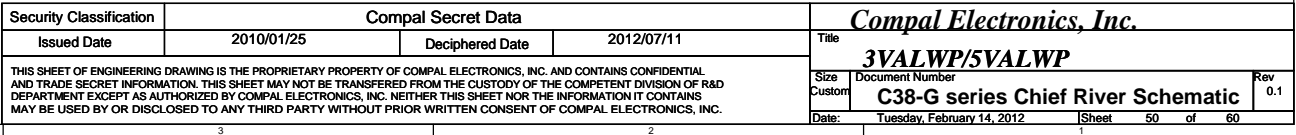
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

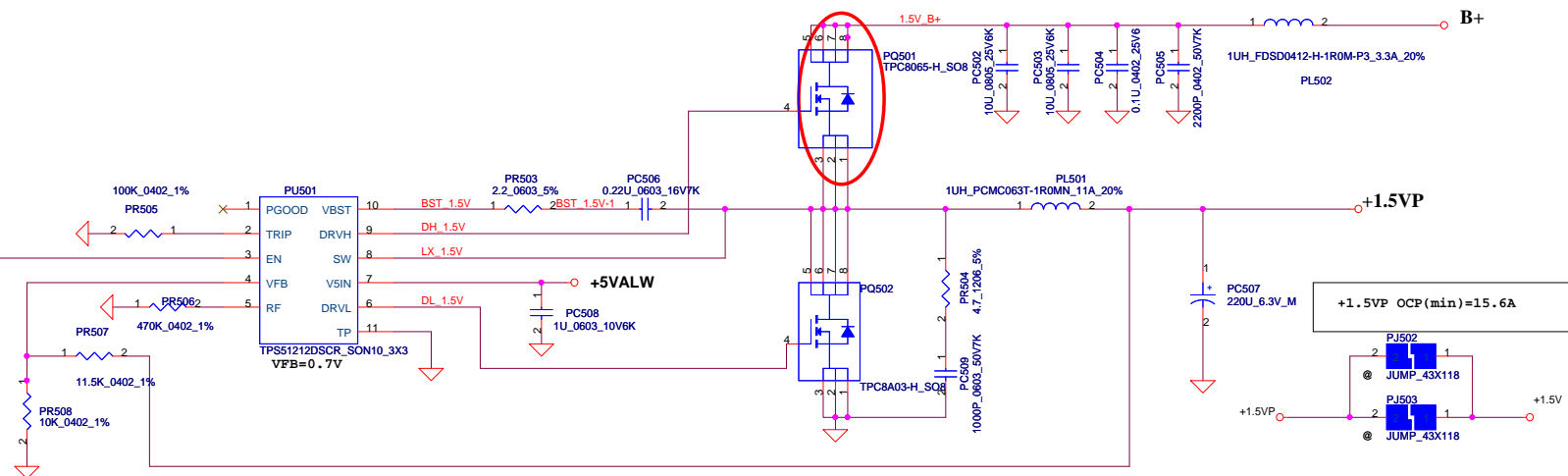


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				Size	Document Number
				C38-G series Chief River Schematic	
Date: Tuesday, February 14, 2012		Sheet 49 of 60		Rev 0.1	

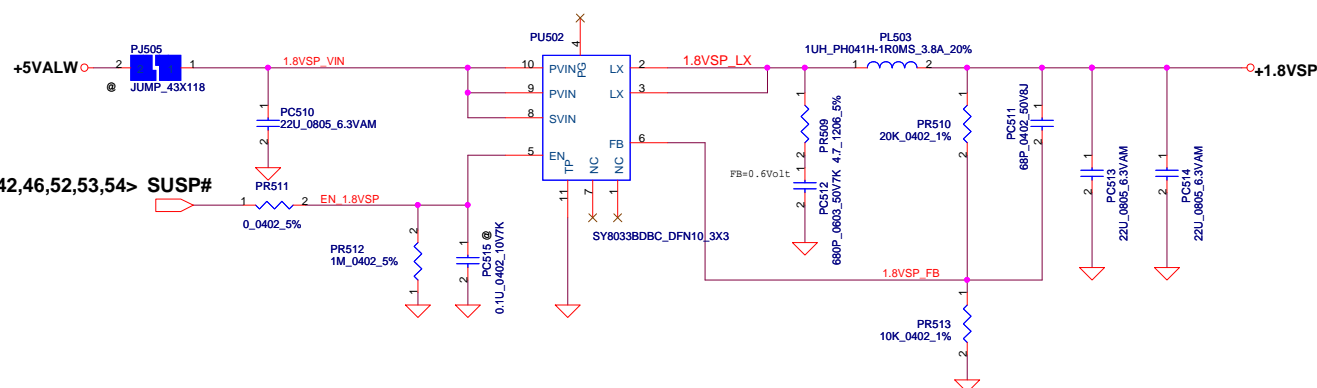
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<42,45,46> SYSON



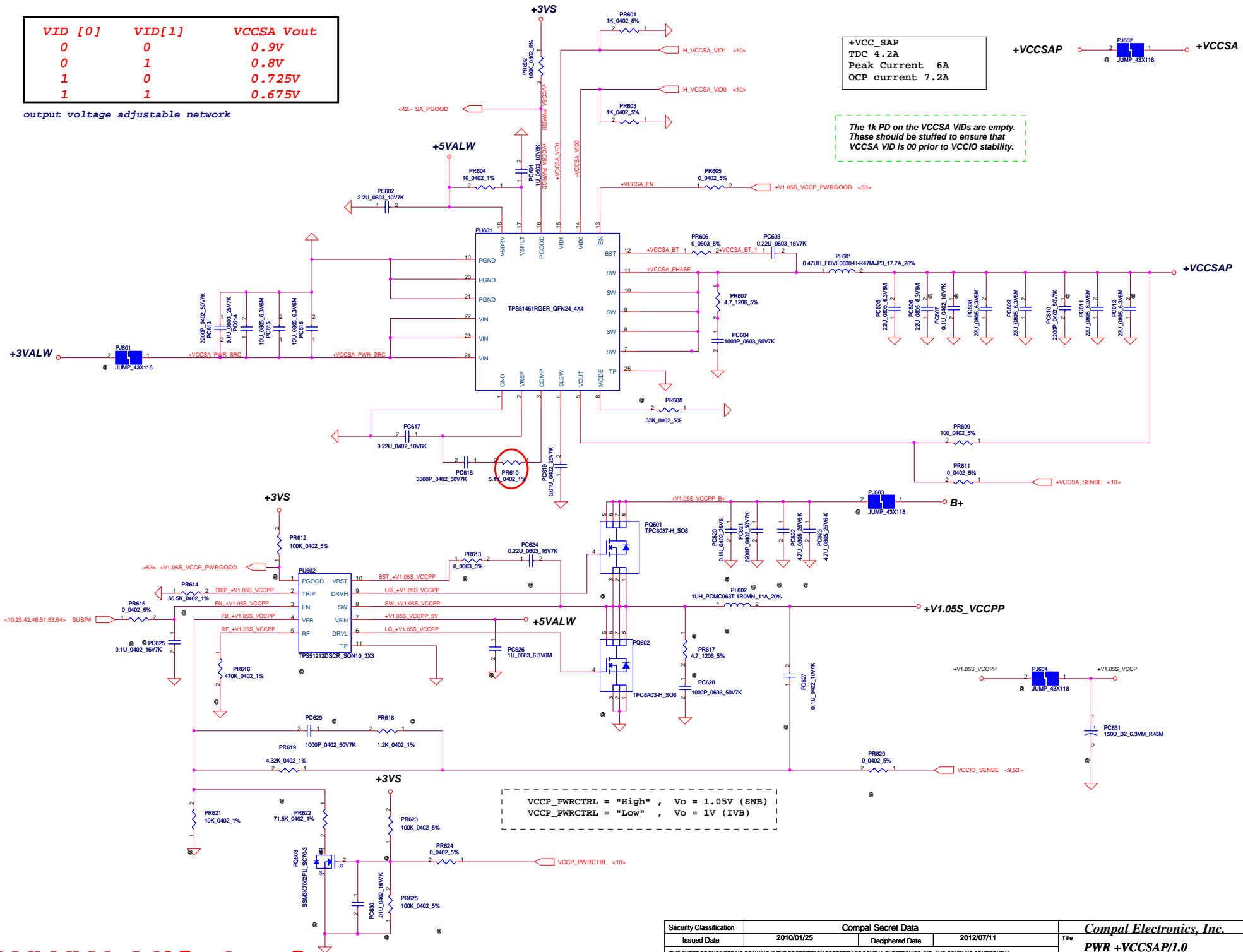
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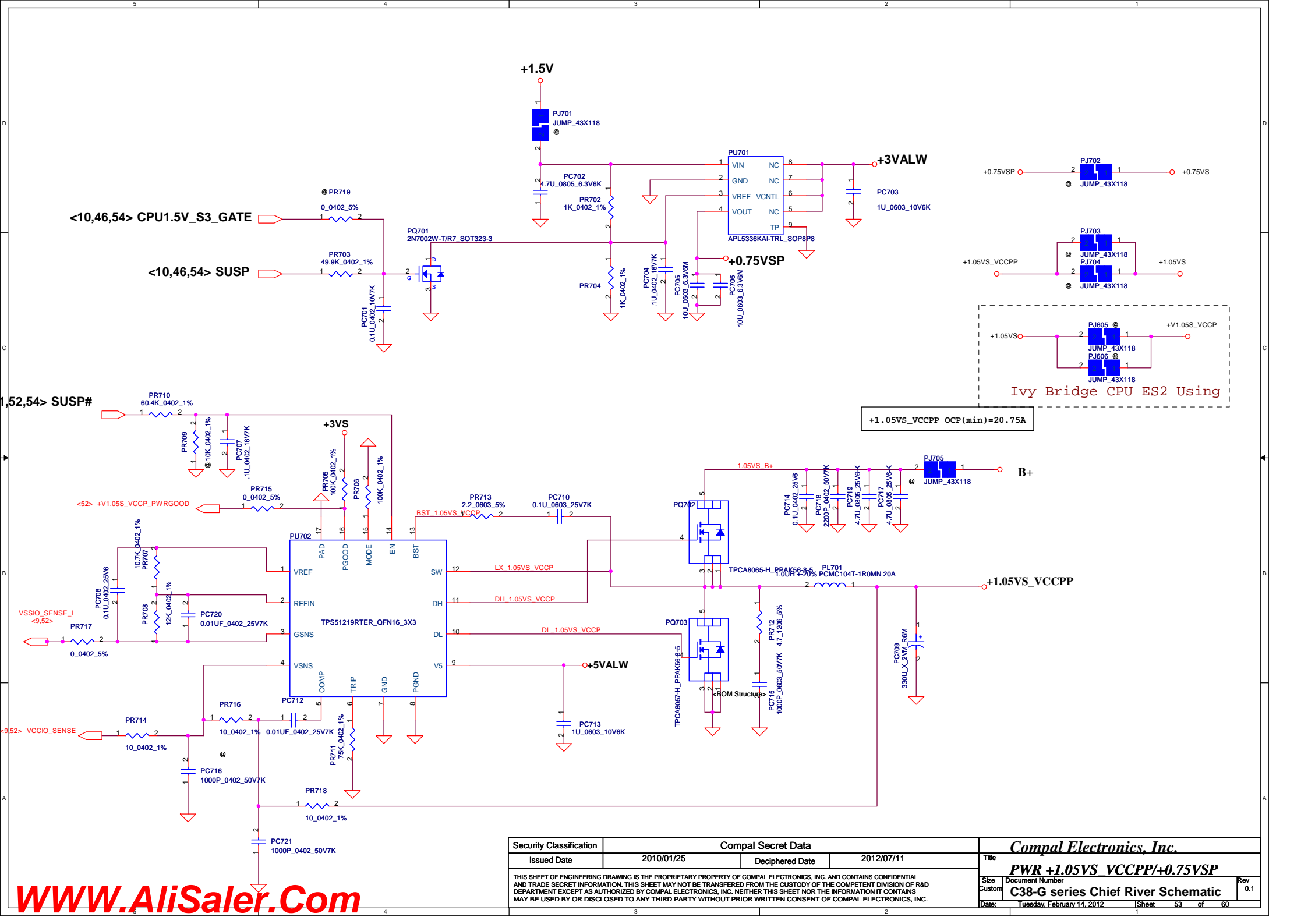
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Size	Custom	Document Number	C38-G series Chief River Schematic	Rev	0.1
Date:	Tuesday, February 14, 2012	Sheet	51	of	60

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

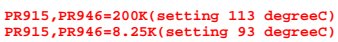


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		C38-G series Chief River Schematic
		Rev 0.1
		Date: Tuesday, February 14, 2012
		Sheet 52 of 60

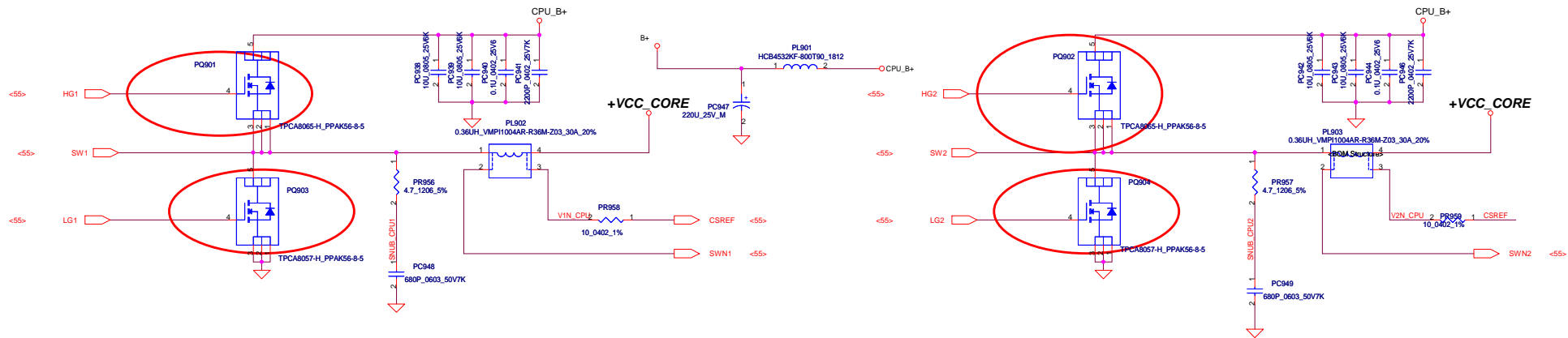


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				Date	Tuesday, February 14, 2012
				Sheet	53 of 60
				Rev	0.1

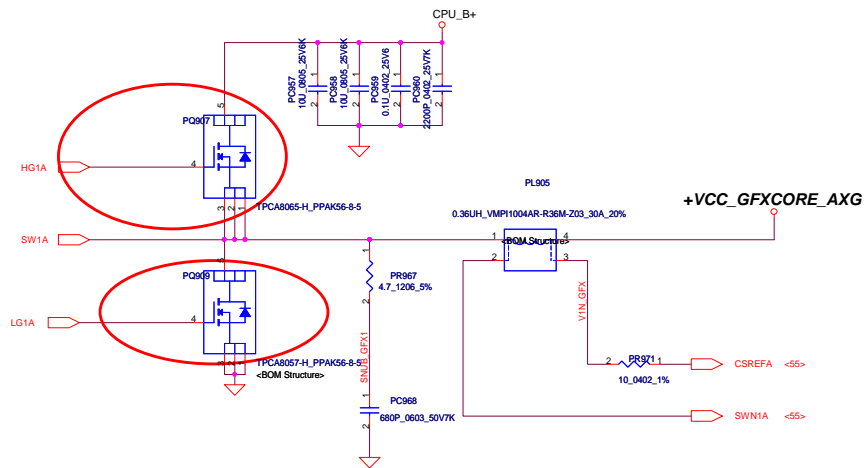


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QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP-110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP-65A



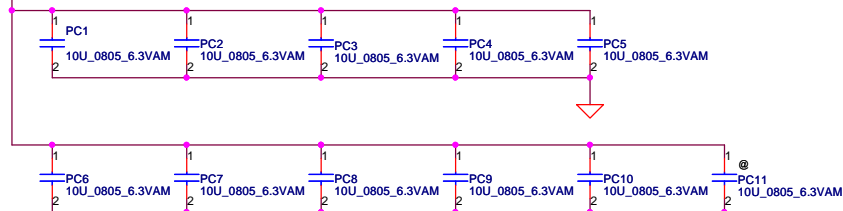
QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP-55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP-40A

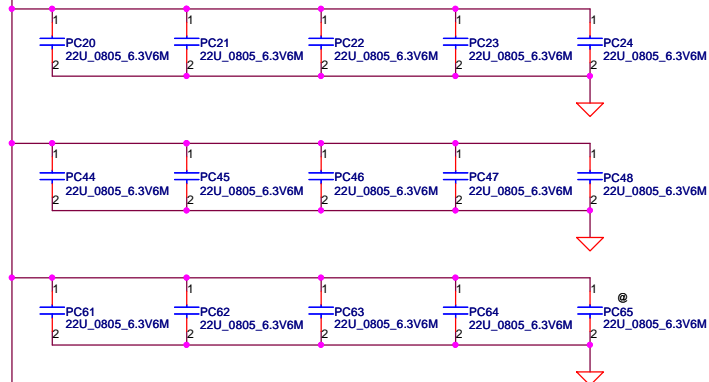
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2009/12/01		2012/07/11		PWR-CPU CORE	
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		C		C38-G series Chief River Schematic	
		Date:		Tuesday, February 14, 2012	
		Sheet		56 of 60	
		Rev		0.1	

+VCC_CORE

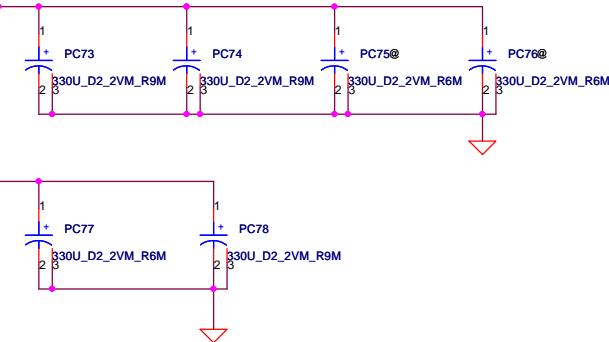
+VCC_CORE



+VCC_CORE

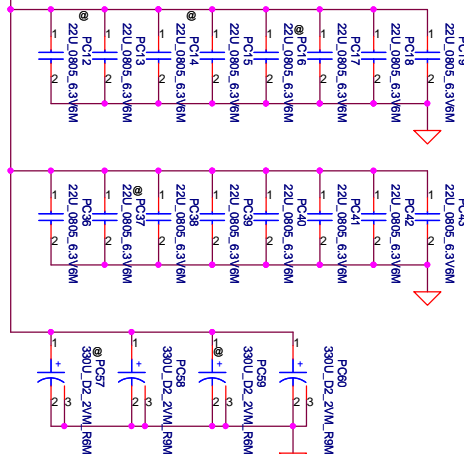


+VCC_CORE



+VCC_GFXCORE_AXG

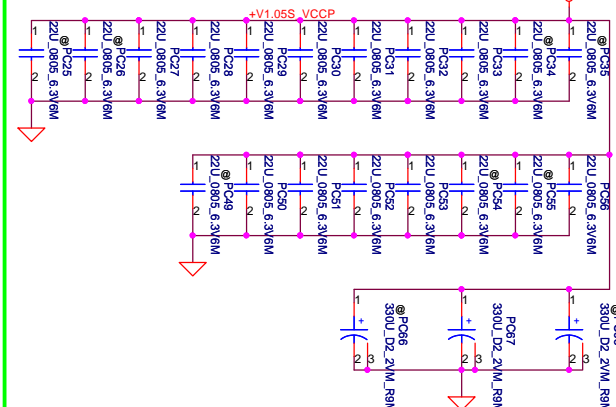
+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+V1.05S_VCCP



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Date: Tuesday, February 14, 2012				Sheet 57	of 60

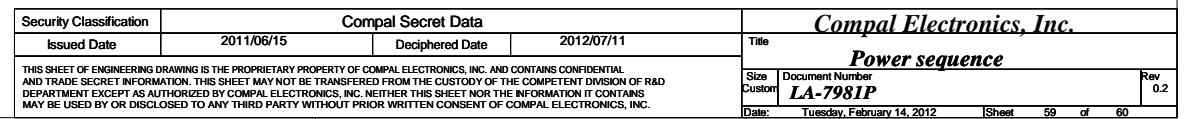
Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	add PR865 for ISL62883 one phase solution and unpop for two phase solution.	P54	add PR865	2011.08.29	DVT
2	unpop PR315,PR316 for SMBus SPEC.	P49	unpop PR315,PR316	2011.08.29	DVT
3	delet PSI#_VGA for NV chip.	P54		2011.10.14	DVT2
4	change NTC_V pull high voltage from +3VLP to +3VALW	P48			
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				Size	Document Number	Rev
				Custom	C38-G series Chief River Schematic	0.1
Date:				Tuesday, February 14, 2012	Sheet 58 of 60	

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



Version change list (P.I.R. List)

Page 1 of 2 for HW PIR

Item	Reason for change	PG#	Modify List	Date	Phase
1	GPU 13M GPU Device loss (Pcie lan x8 issue)	8	Add R43		DVT
2	HDD no function	40	Add R550		DVT
3	10/100 lan no function & change to overclocking mode	37	ADD R1372 ; DEL R31		DVT
4	For DGPU_PWROK leakage issue.(Let timing +5VS > +3VS)	46	Change C726 from 0.1uF to 0.01uF		DVT
5	For S3 can't wake up	10	Change R56 from 15K to 4.7K change R885 from 0 ohm to 15K		DVT
6	Can unstuff RV66 for N13P-GL & as NV DG	27	RV66 change to N13M@		DVT
7	GPU N13P-GL QS sample change strap	32	RV94 change from 45.3K to 10K		DVT
8	PCH 25Mhz for vender crystal test report change CL to 12pF	15	C196;C197		DVT
9	GPU 27Mhz for vender crystal test report change CL to 15pF	23	CV37;CV38		DVT
10	EC_LID_OUT# internal PD 20K, follow ORB change R230 from 10k to 1K	19	R230		DVT
11	For GPIO70;GPIO71 voltage level issue (internal Pull High 20k)	19	R705;R706 Change from 10K to 200K		DVT
12	for DVT board ID Change R695 from 33k to 18k	42	R695		DVT
13	LAN Surge test fail change P/N from SP050006E00 to SP050006W00	27	T1;T2		DVT
14	Del ODD Power Control function component	40	R568;Q100;R675;C607;Q99		DVT
15	AO4430L(SB000007010)EOL Change to AO4304 (SB00000RV00)	46	U49		DVT
16	Del (PCH AUX Power) Reserve component no use	46	C780;C781;C782;C783;R778;Q120;U40		DVT
17	PCH(U4) P/N Change from SA00004NQ30 to SA00004NQ80	14	U4		DVT
18	NV-GPU (U65)P/N change N13M from SA00004V000 to SA00004V010 N13P Keep SA000051A00	23	U65		DVT
19	EXT USB 3.0 IC PCIE_WAKE# ; CLKREQ_USB30# leakage on S4	45	Swap Q125;Q121 pin1 & pin3		DVT
20	No function	45	DEL R769		DVT
21	add LAN LDO mode function	37;38	ADD R65;R596;R1449;R1380		DVT
22	USB_OC0# Share with USB_OC4# due to same power switch	18	short USB_OC0#;USB_OC4# ; del R267		DVT
23	Add Capsensor B/D Conn. For best buy use	42	ADD JCAP1 Conn.		DVT

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				Custom	0.1
				Document Number	LA-7981P
				Date:	Tuesday, February 14, 2012
				Sheet	60 of 60

Version change list (P.I.R. List)

Page 2 of 2 for HW PIR

Item	Reason for change	PG#	Modify List	Date	Phase
24	L1 change to 1 ohm R	20	L1 change to R footprint		DVT
25	Reserve 0 ohm for CMOS Camera shake	33	add R296 0 ohm		DVT
26	Reserve 0 ohm for U49 MOS VGS 20V will burn out issue	46	add R784 0 ohm		DVT
27	For HDD +5VS Power plant del C601; change C598 pin1 power name for good power plant	40	change from +5VS to +5V_HDD ;DEL C601		DVT
28	For Audio jack support APPLE and NOKIA function Reserve	43	add R684;R685;R688;R686 0ohm R		DVT
29	For standard part cost down change 10uF 0805 type to 0603 type	10,20 21,33 37,39 40,46	C124;C125;C126;C127;C130;C221;C215;C395; C231;C519;C937;C953;C954;C591;C608;C602; C720;C721;C723;C724;C782;C783;C717;C718; C856;C852;C851;C853		DVT
30	change Crystal foot print follow standard parts from 5032 to 3225 package	15;23; 37	Y2;Y6;YV1		DVT
31	change 0ohm to short-pad (R0402_0ohm)	7;8; 10;15 16;20; 33;36; 40;43	R40;R60;R77;R144;R190;R193;R198;R181;R185; R265;R538;R498;R500;R583;R614		DVT
32	Reserve BT_DISABLE (GPIO22) for combo card(BT+WLAN)	19	ADD R892;R897		DVT
33	U35;U36 Change footprint without thermal PAD type	44;45	U35;U36		DVT
34	PU 10K with 3V3 on N13P-GL/ for CEC signal	24	RV230		DVT
35	VGA_GPIO3;VGA_GPIO16 change connect DPRSLPVR_VGA to PSI#_VGA	23;54	RV113;RV114		DVT
36	Fix VGA power on CLKREQ has drop (QV2 gate add 0.1uF)	23	CV42		DVT
37	LED5 和LED2 Location sawp ; Location name D9 change to LED6	43	LED2;LED5;LED6		DVT
38	For Lan surge fail add 0 ohm on MDO2-;MDO2+;MDO3-;MDO3+	38	R304;R305;R306;R307		DVT
39	Change UV2 PN from SA007080B90 to SA000000H00	23	UV2	09/28	DVT
40	Change 2M BIOS ROM from SA00003FO00 to SA00003FO10	14	U6	09/29	DVT
41	Correct PCIE_PRX_DTX_P4/N4 of U32 (SWAP)	45	U32	10/03	DVT
42	Reserve +5VS to JCR1, add R689 ,R690	43	R689 (@),R690	10/03	DVT
43	Update Power sheet of 1003 version	47~58		10/04	

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				Custom	LA-7981P	0.1
				Date:	Tuesday, February 14, 2012	Sheet 61 of 60

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				LA-7981P	
Date:				Tuesday, February 14, 2012	Sheet 62 of 60