

Compal Confidential

Schematics Document

NIWE1

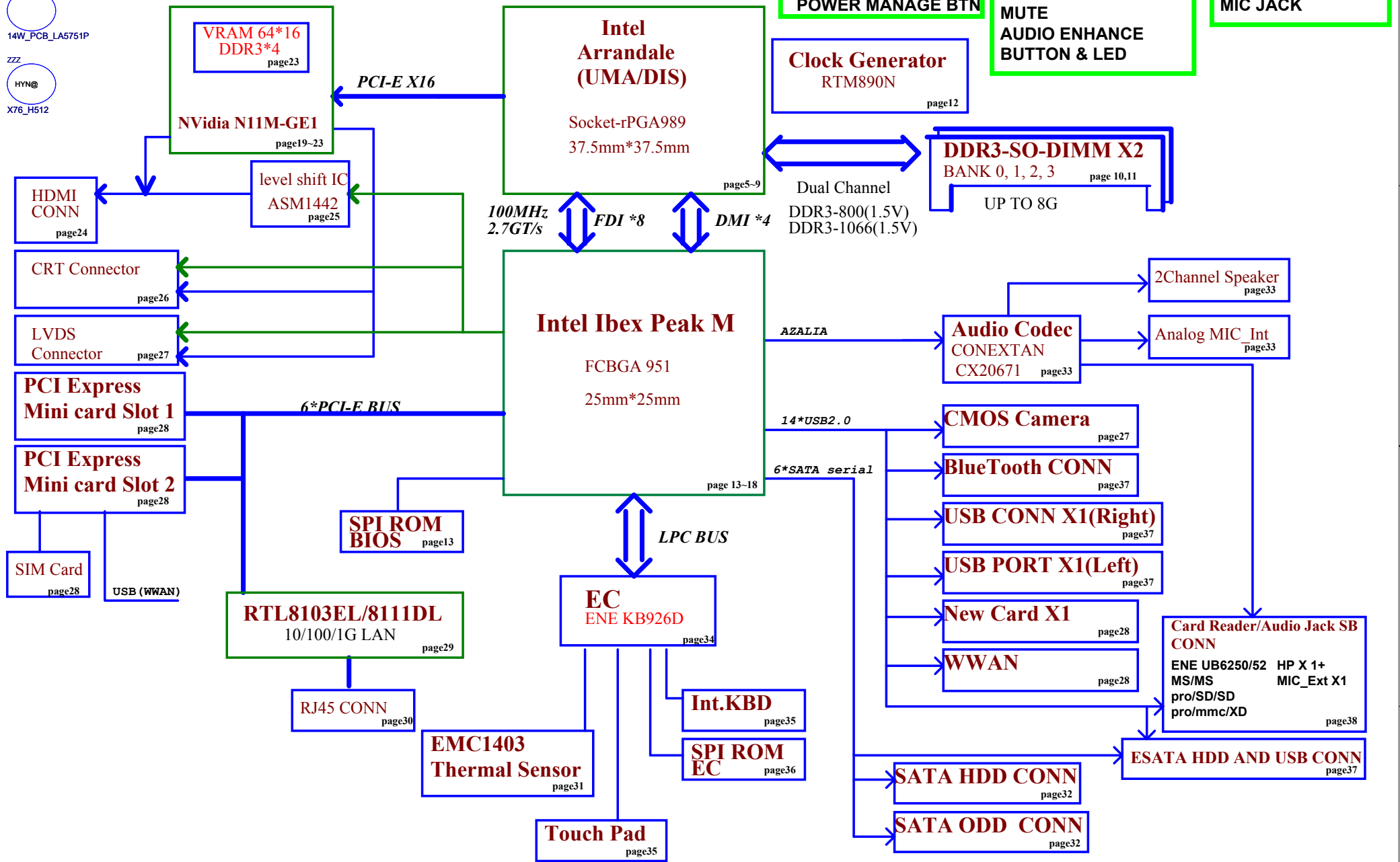
Arrandale

with Intel IBEX PEAK-M core logic

REV : 0 . 3

Security Classification	Compal Secret Data			Compal Electronics,Ltd.		
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Cover Sheet	
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14W_PCB_LA5751P
ZZZ
HYN@
X76_H512



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						Size Custom	Document Number			LA-5751		Rev
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						Sheet		2 of 51				

DDR3 Voltage Rails

power plane				+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
State	+B	+5VALW +3VALW	+1.5V	
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW											+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	V	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS					+3VS	
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	V	X	V	X	X
SML1DATA	+3VALW			+3VALW				+3VS		+3VS		

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

@ FUNCTION

Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
3G@	3G function (WWAN)	
CAP@	CAP Sensor function	
CMOS@	CMOS CAMERA function	
ESATA@	E-SATA function	
HDMI@	HDMI function (UMA or DIS)	
UMA HDMI@	HDMI function (UMA only)	
X76@	X76 BOM	
100@	10/100 LAN function	
GIGA@	GIGA LAN function	
UMA@	UMA only (Arrandale)	
DIS@	DIS only (Arrandale)	

SKU

Arrandale (dGPU) DIS only	DIS@
Arrandale (iGPU) UMA only	UMA@

PCIE PORT LIST

PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

VGA and DDR3 Voltage Rails (N11x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	N/A	
GPIO8	I/O	N/A	
GPIO9	OUT	N/A	
GPIO10	OUT	N/A	
GPIO11	I/O	-	Reserve 10K pull low.
GPIO12	IN	N/A	
GPIO13	OUT	N/A	
GPIO14	OUT	-	Reserve 10K pull low.
GPIO15	IN	N/A	
GPIO16	OUT	N/A	
GPIO17	IN	-	PAD
GPIO18	IN	N/A	
GPIO19	IN	N/A	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

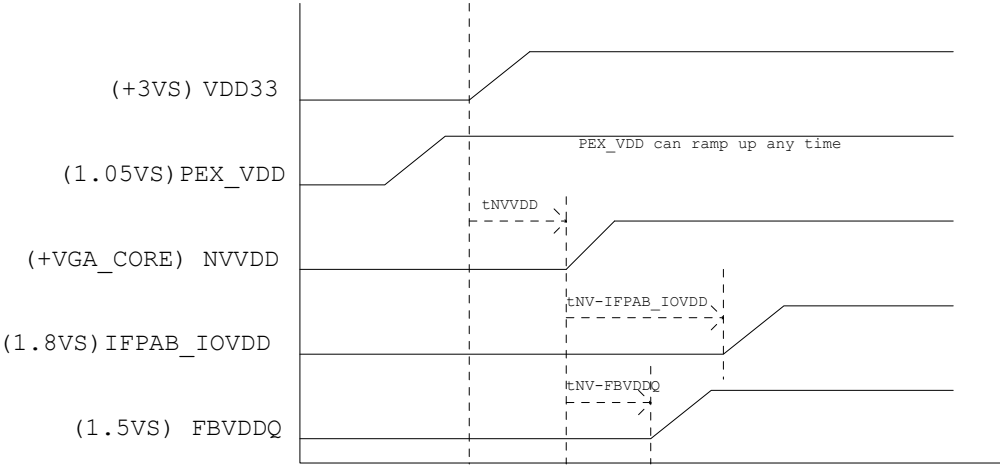
	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N11M-GE1 64bit 512MB DDR3	14.02	2.16	TBD	TBD	12.9	12.26	0.66	0.99	1.3	1.95	530	0.56	84	0.15	140	0.15	38	0.13

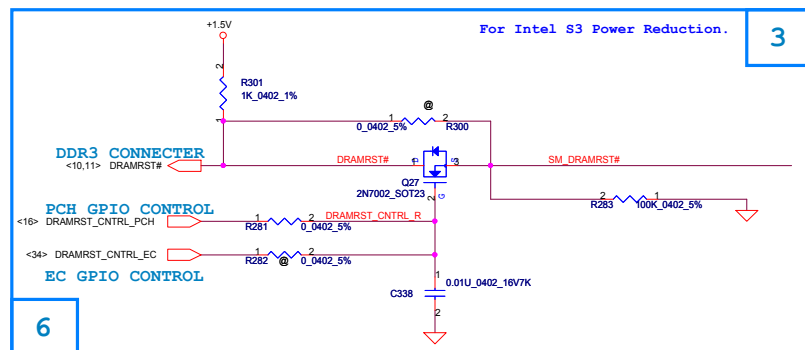
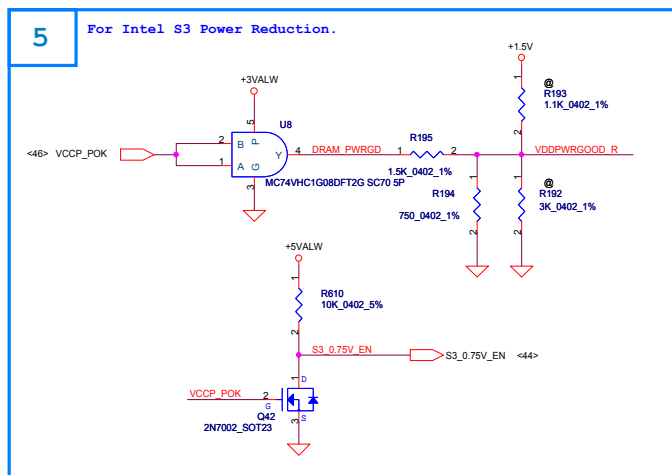
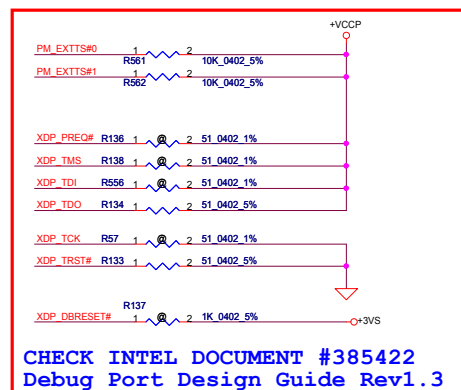
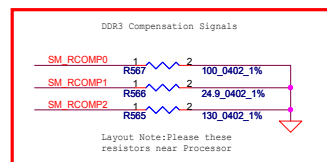
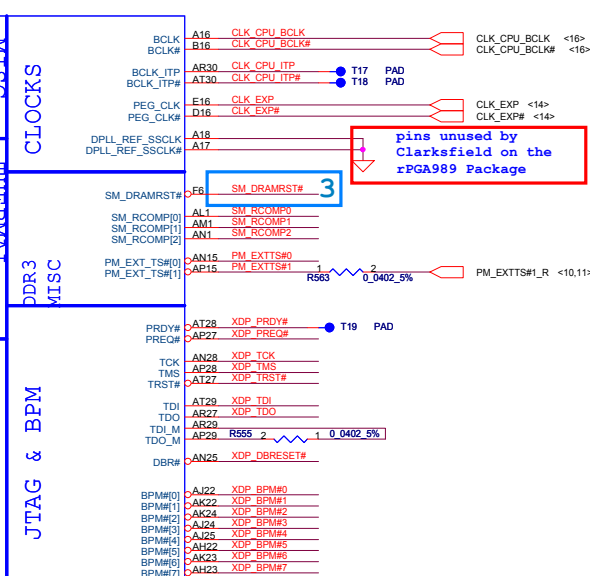
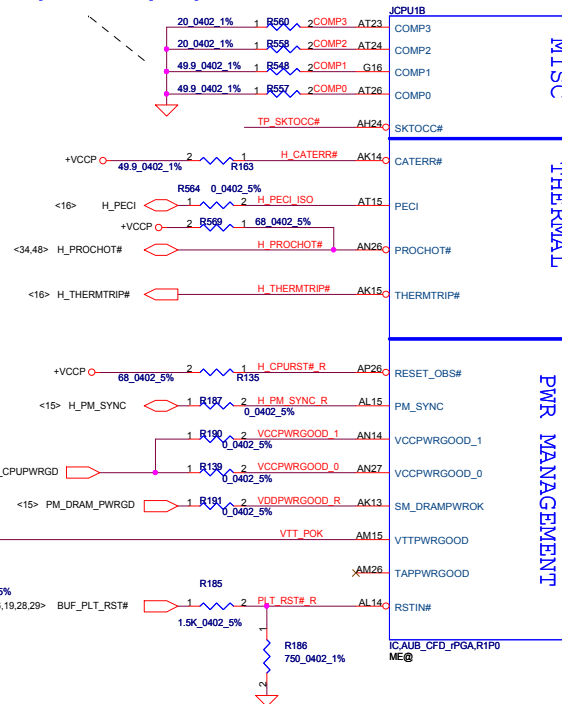
GPIO5 GPIO6

	Device ID	GPU_VID0	GPU_VID1	VGA_CORE	P-State
N11M-GE1/LP1 (40nm)	0x0A7D	0	0	0.8V	Deep P12
		0	1	0.85V	P8
		1	1	1.03V	P0

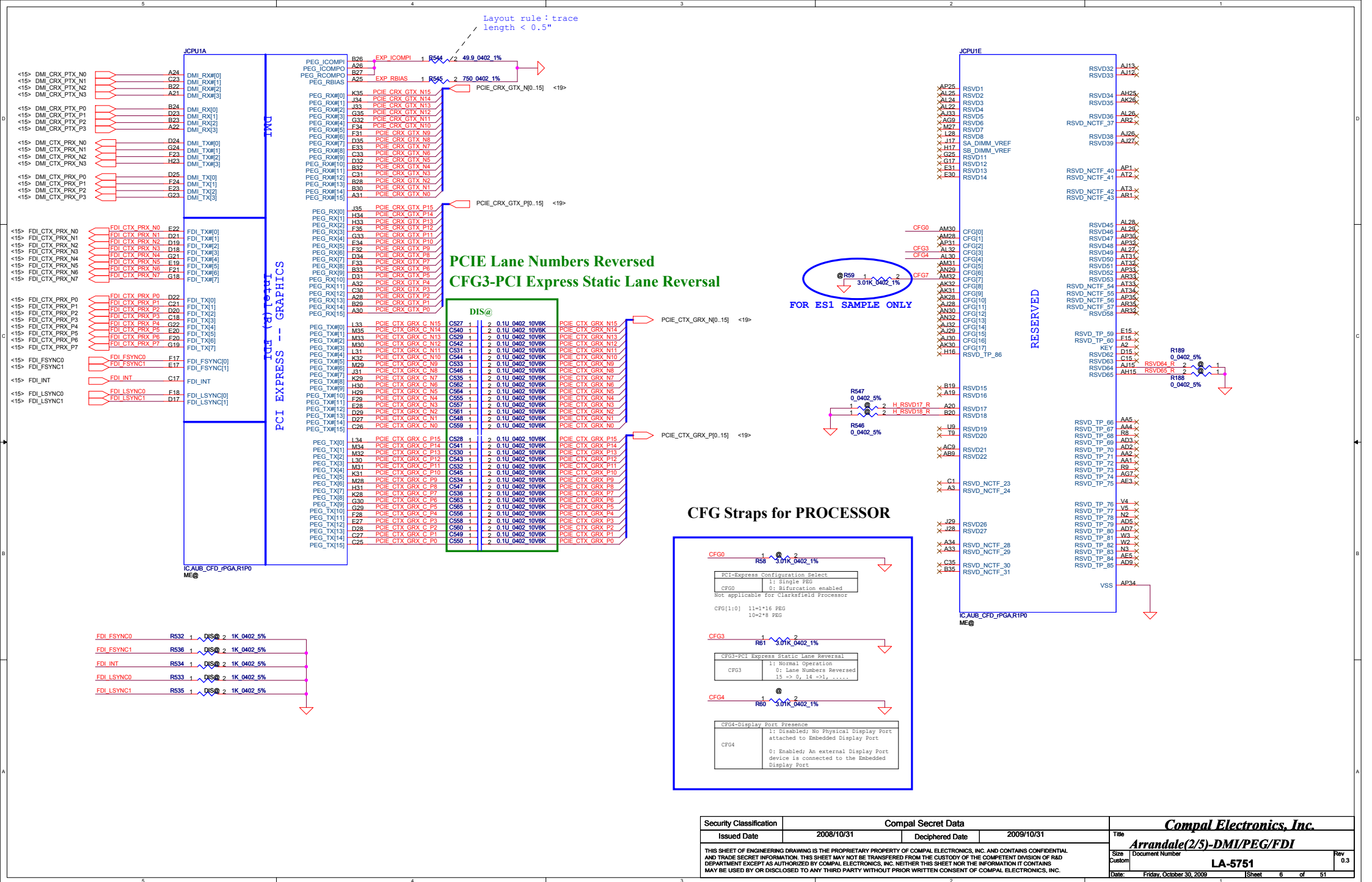
Power Sequence

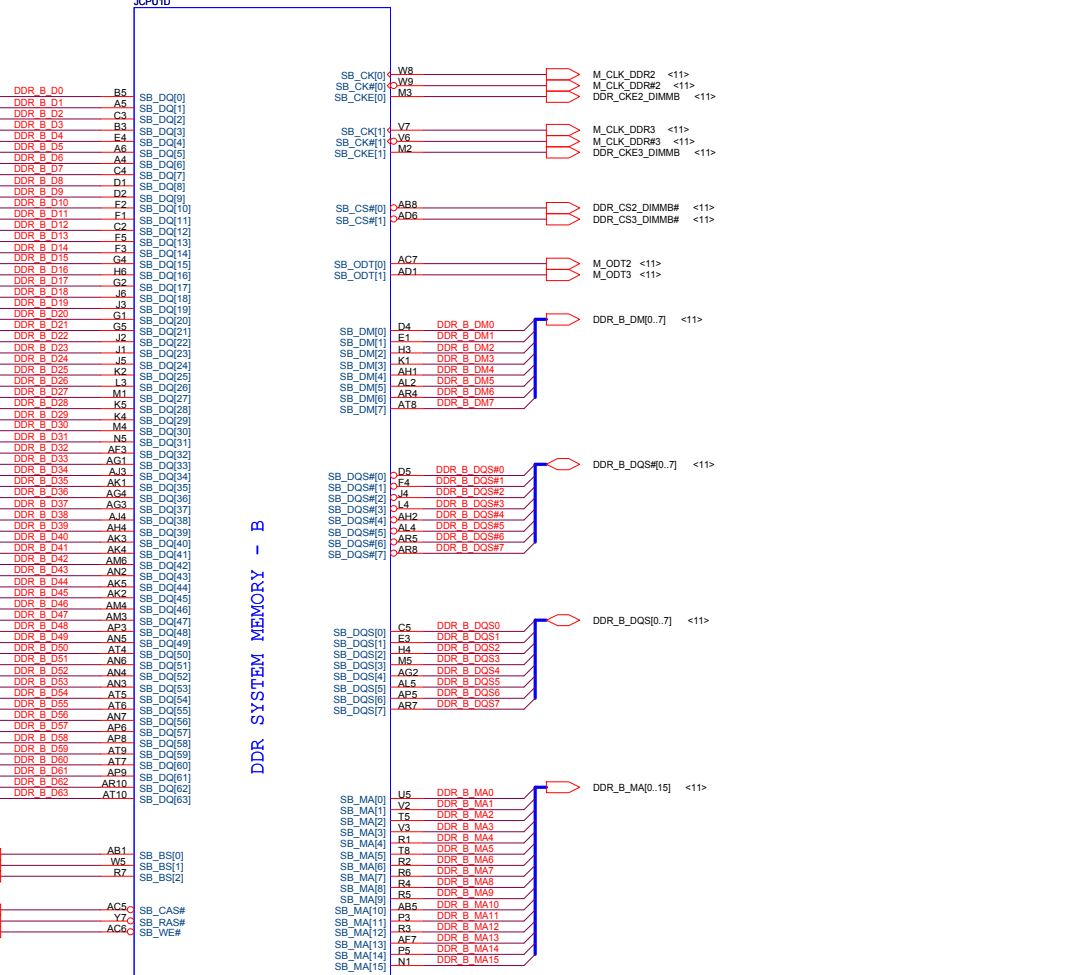
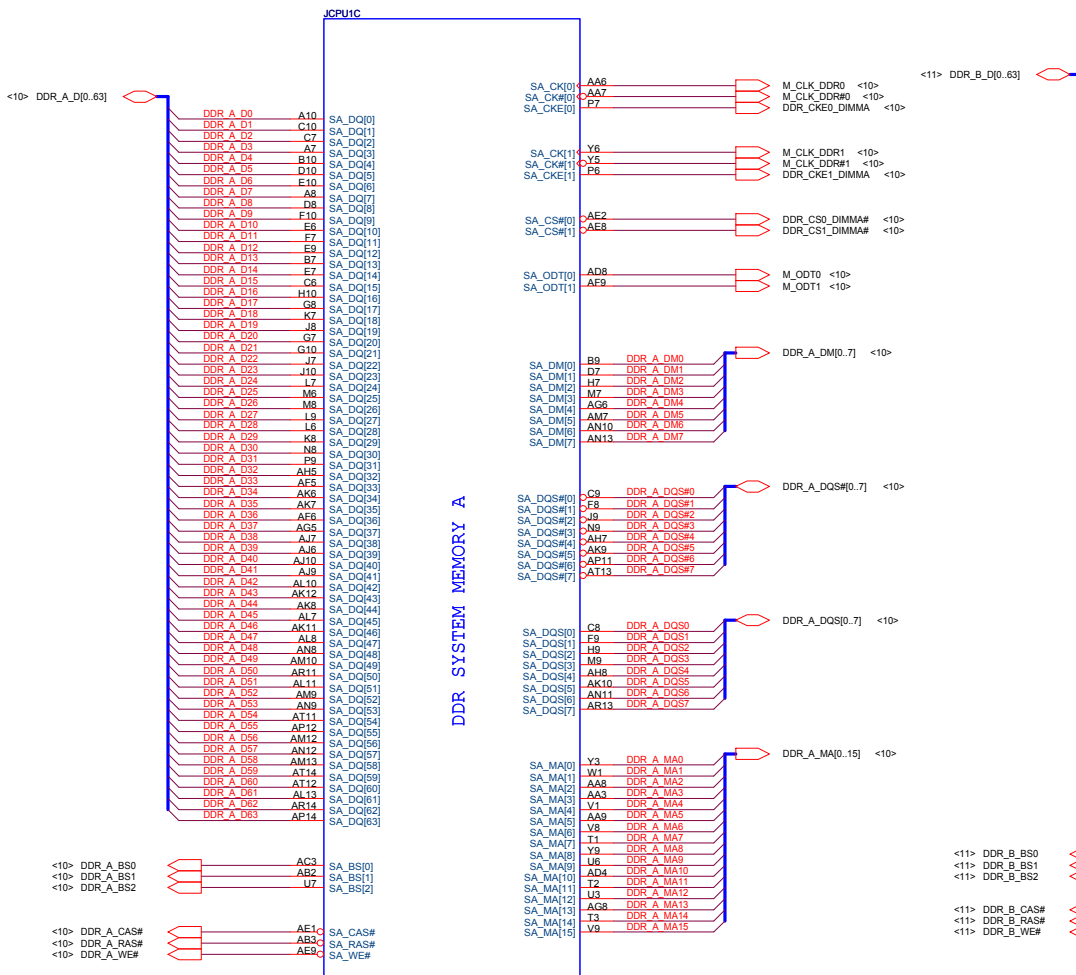
The ramp time for any rail must be more than 40us



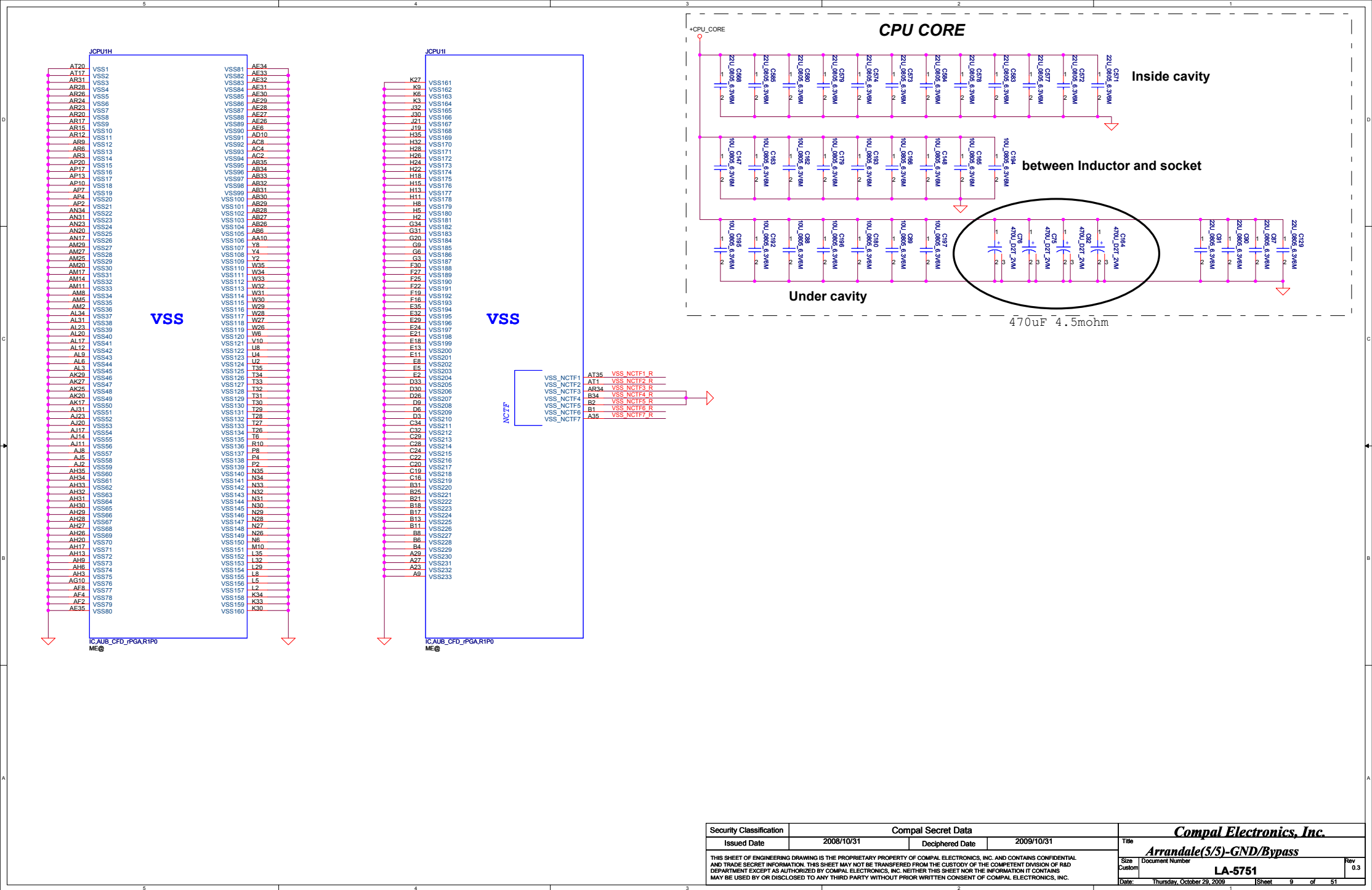


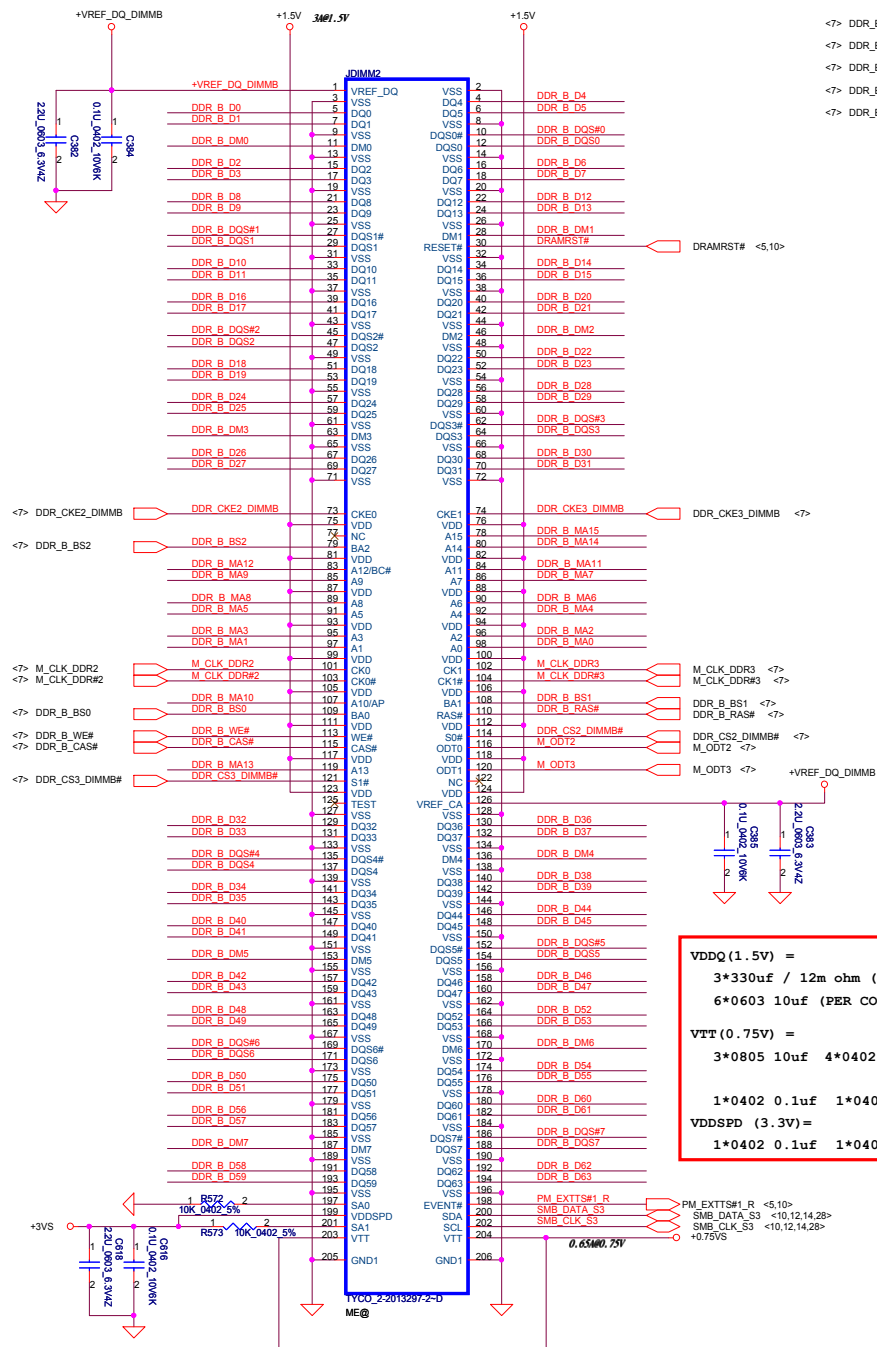
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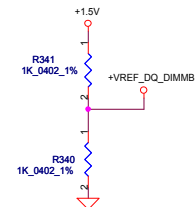


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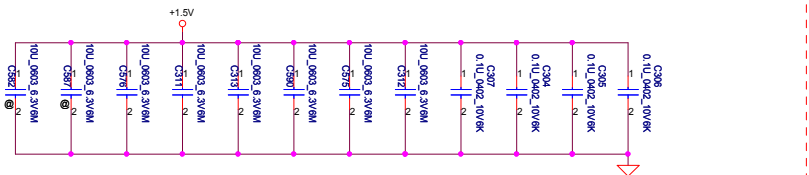


<7> DDR_B_DQS#0..7
 <7> DDR_B_DQ[0..63]
 <7> DDR_B_DM[0..7]
 <7> DDR_B_DQS#0..7
 <7> DDR_B_MA[0..15]



For Arranale only +VREF_DQ_DIMMB
 supply from a external 1.5V voltage divide
 circuit.
 07/17/2009

Layout Note:
 Place near DIMM



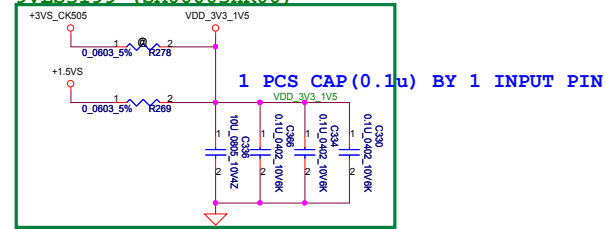
Layout Note:
 Place near DIMM



VDDQ (1.5V) =
 $3 \times 330\text{uF} / 12\text{m ohm (TOTAL FOR 2 SO-DIMMs)}$
 $6 \times 0603 10\text{uF (PER CONNECTOR)}$
VTT (0.75V) =
 $3 \times 0805 10\text{uF} \quad 4 \times 0402 1\text{uF}$
VDDSPD (3.3V) =
 $1 \times 0402 0.1\text{uF} \quad 1 \times 0402 2.2\text{uF}$

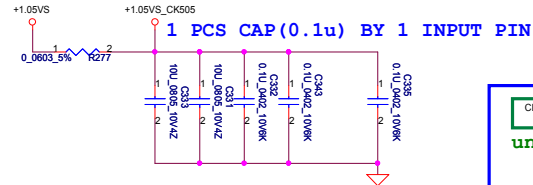
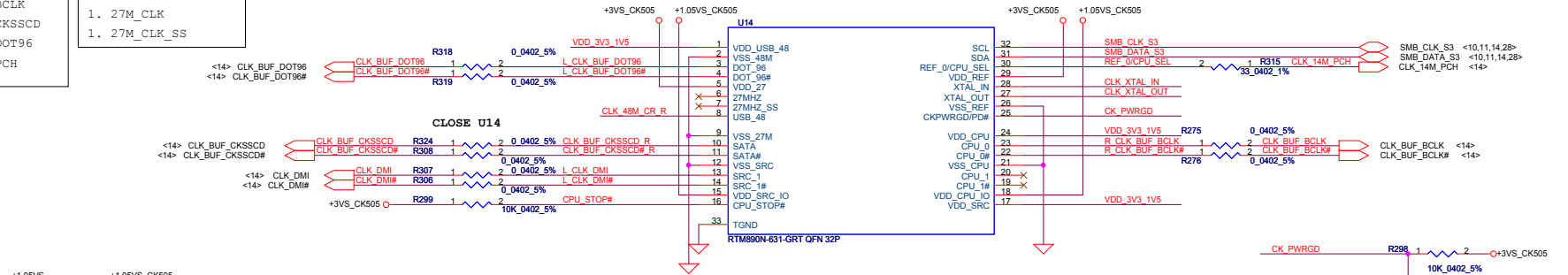
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				DDR3-SODIMM SLOT2	
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Reserve for Low Power CLK GEN.
RTM890N-631 (SA00003HQ00)
SLG8LV597VTR
9VLS3199 (SA00003HR00)



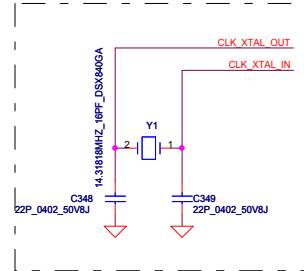
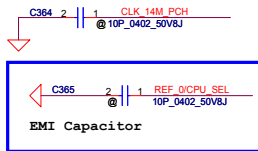
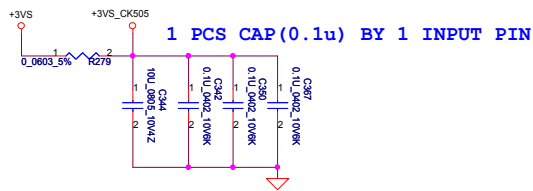
CLK GEN TO PCH
1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

CLK GEN TO VGA
Unused
1. 27M_CLK
1. 27M_CLK_SS

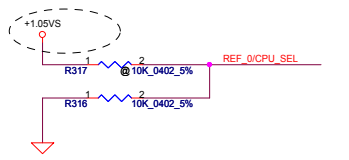


S IC SLG8SP587VTR QFN 32P CLK GEN (SA00002XY00)
S IC ICS9LRS3199AKLFT MLF 32P CLK GEN (SA000030P00)

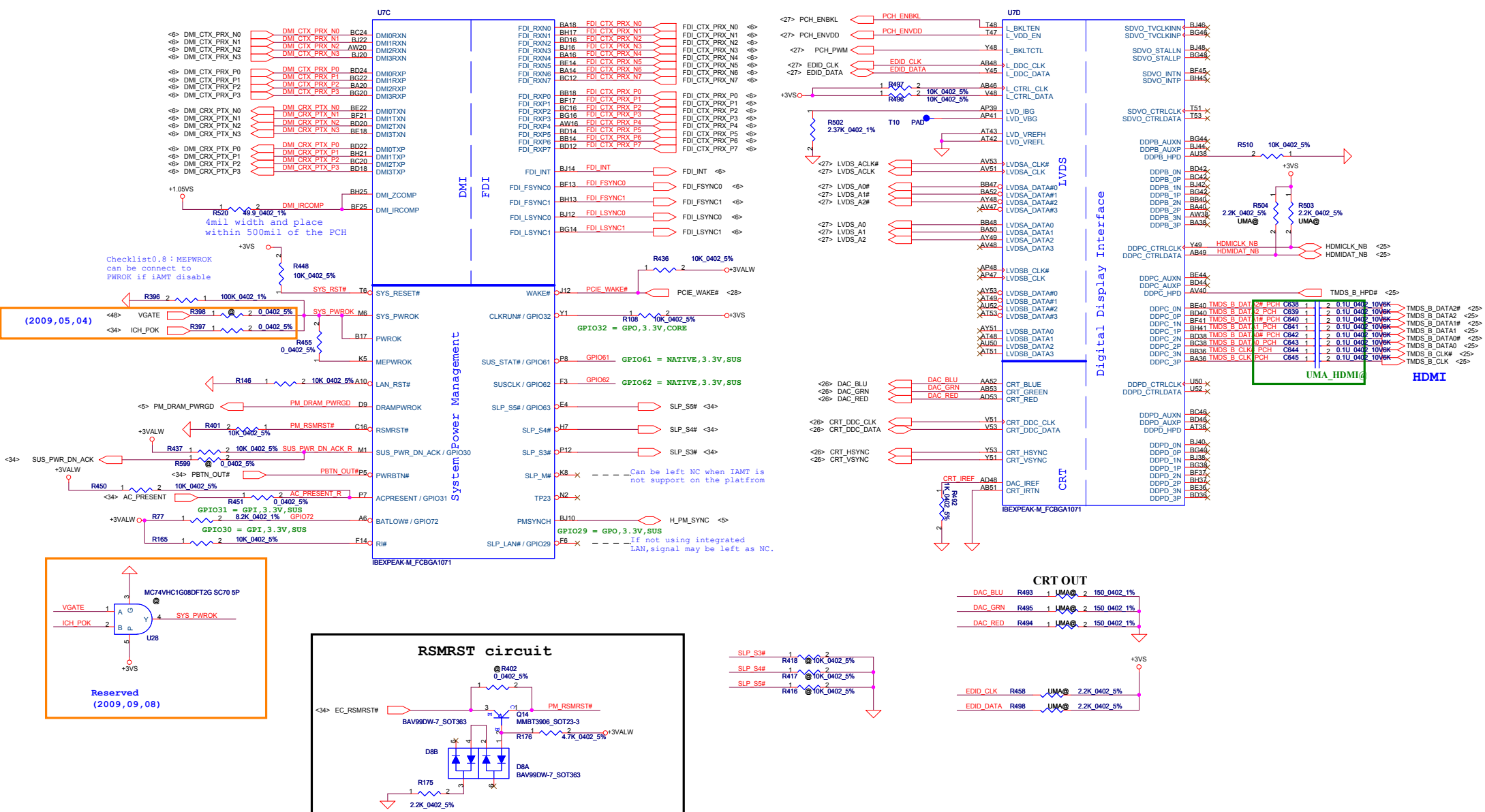
CLK_48M_CR 33_0402_1%
unstuff 09.09.08
PIN8 IS GND FOR ICS3197
PIN8 IS 48MHz FOR ICS3199



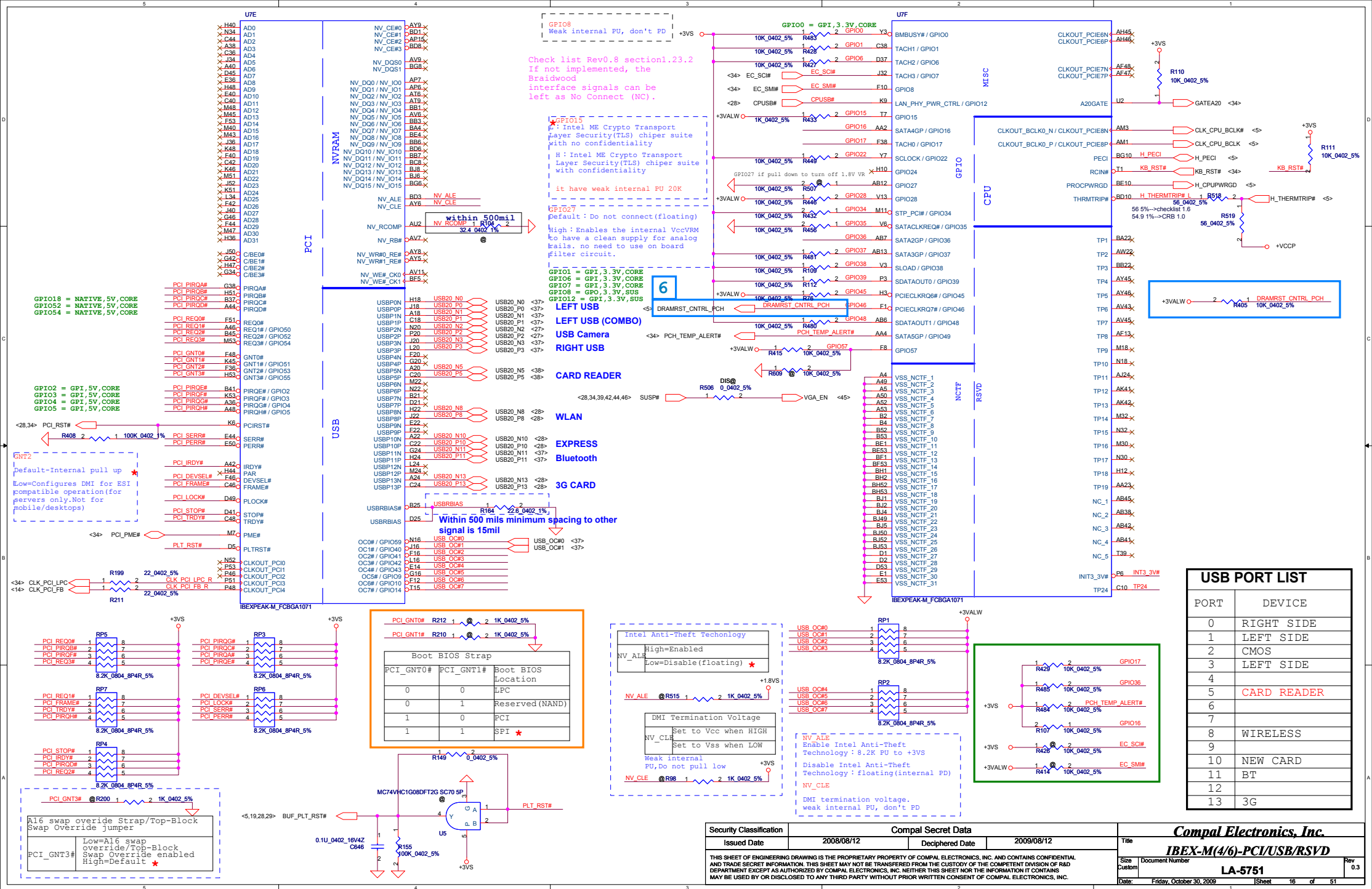
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

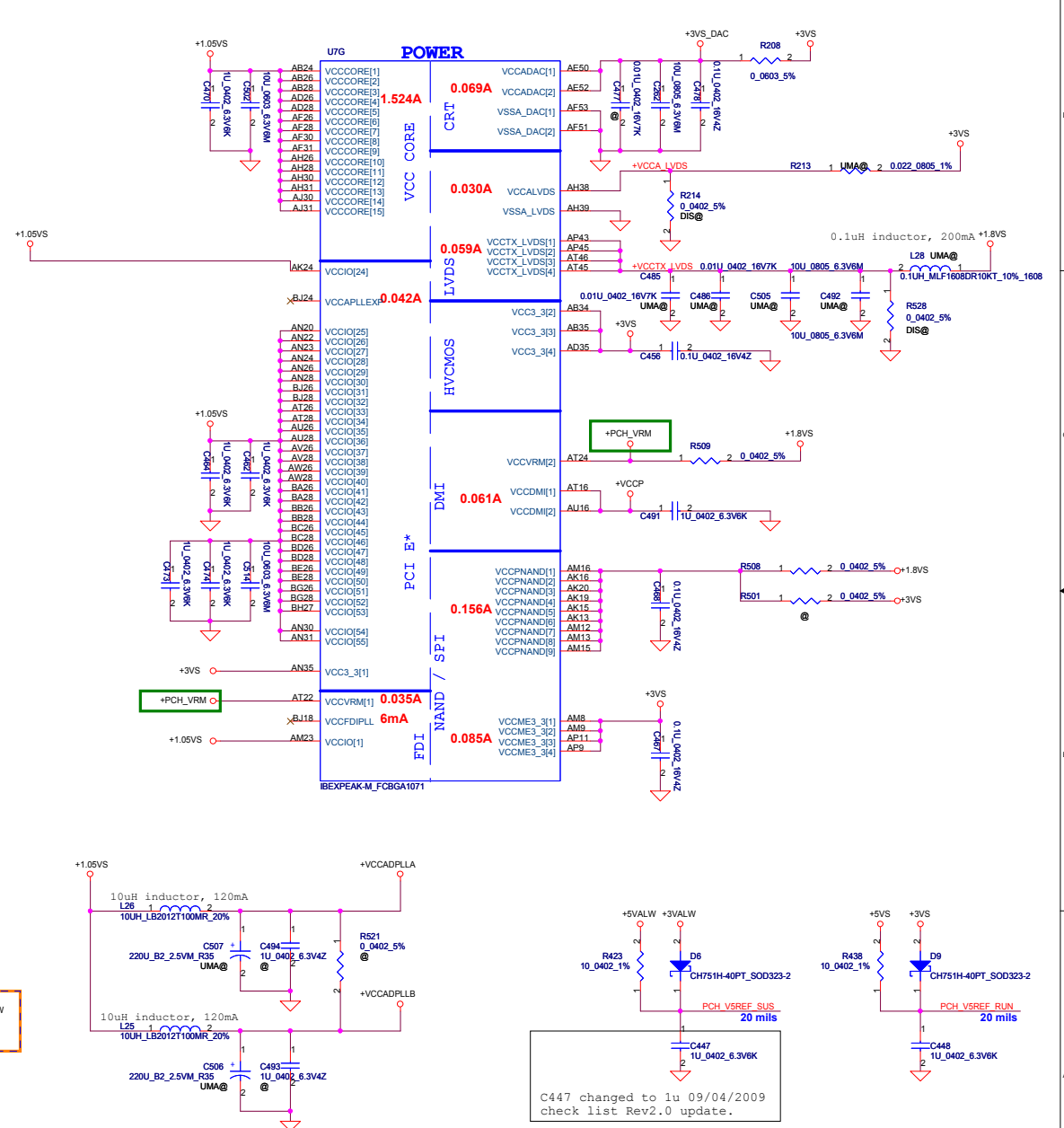


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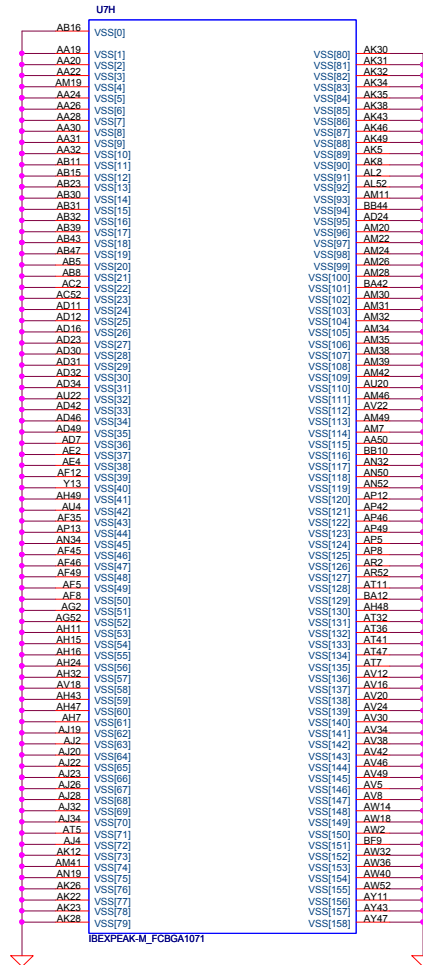
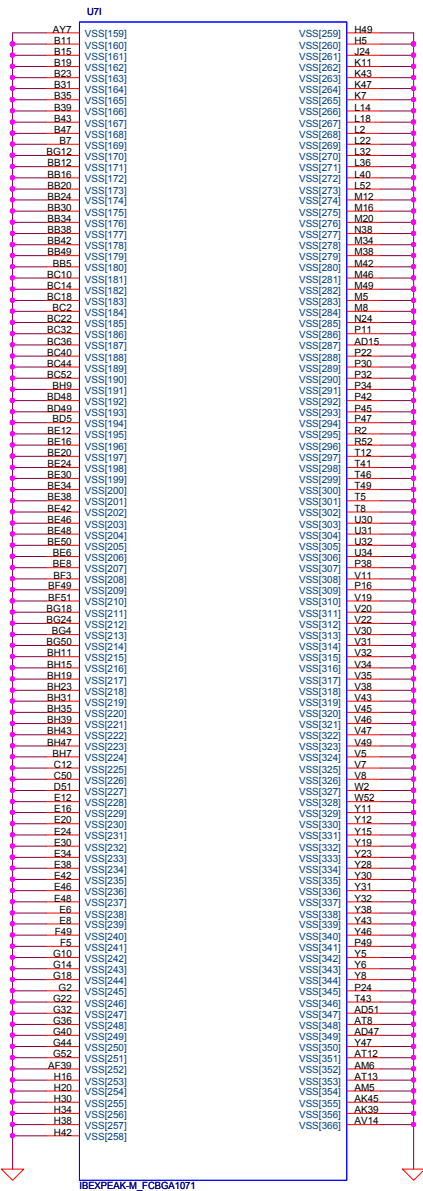


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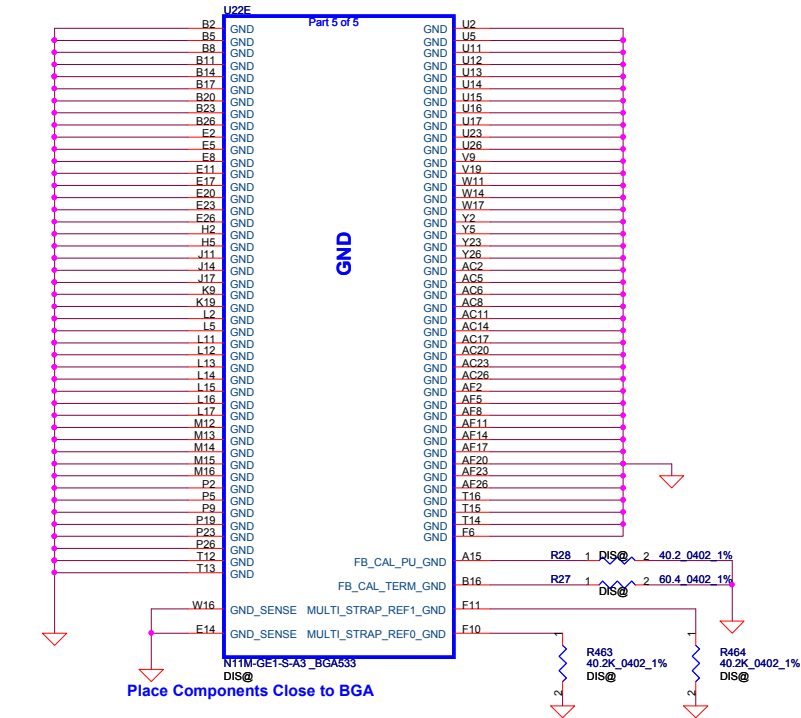


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A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available

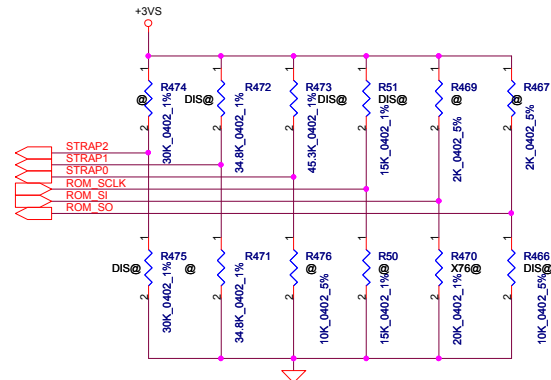


N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resistor for driver calibration

DG-04642-001-V01(May 22, 2009)

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 <20> STRAP1
 <20> STRAP0
 <20> ROM_SCLK
 <20> ROM_SI
 <20> ROM_SO

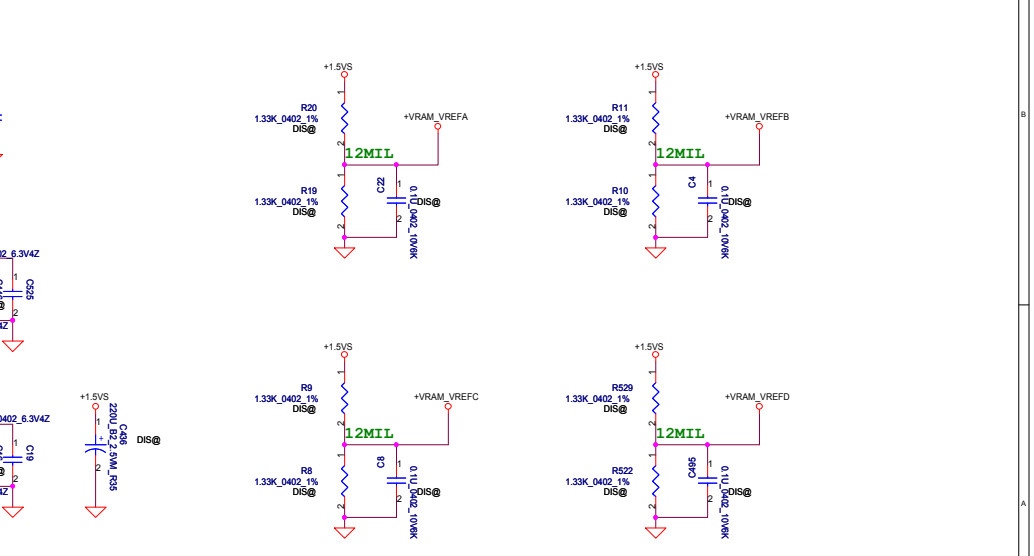
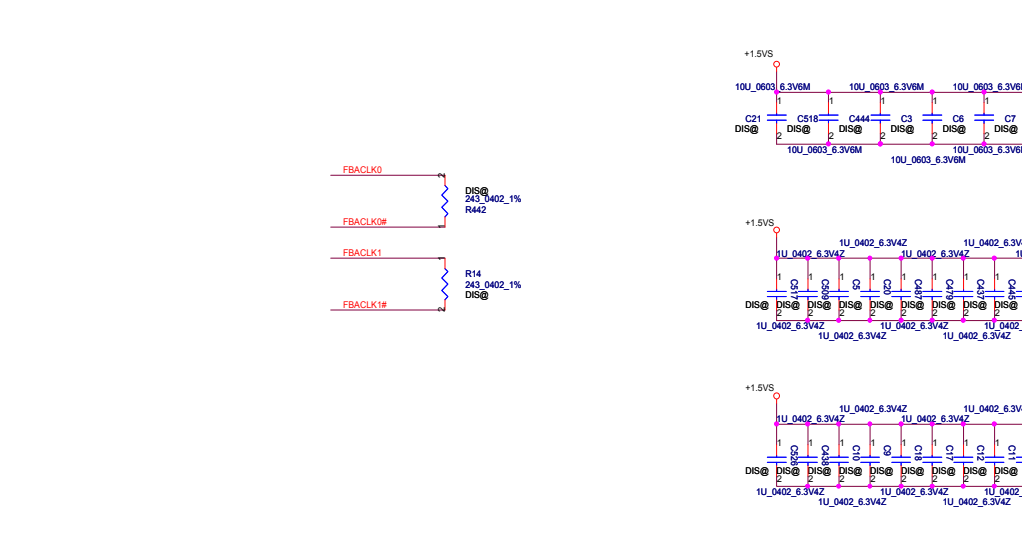
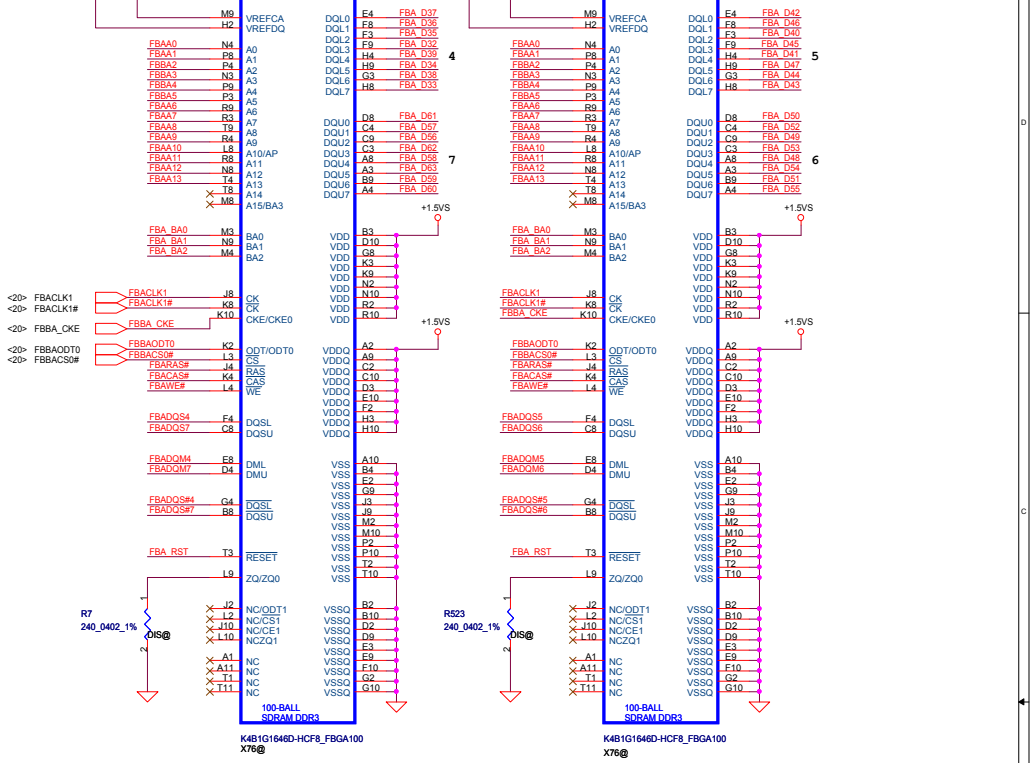
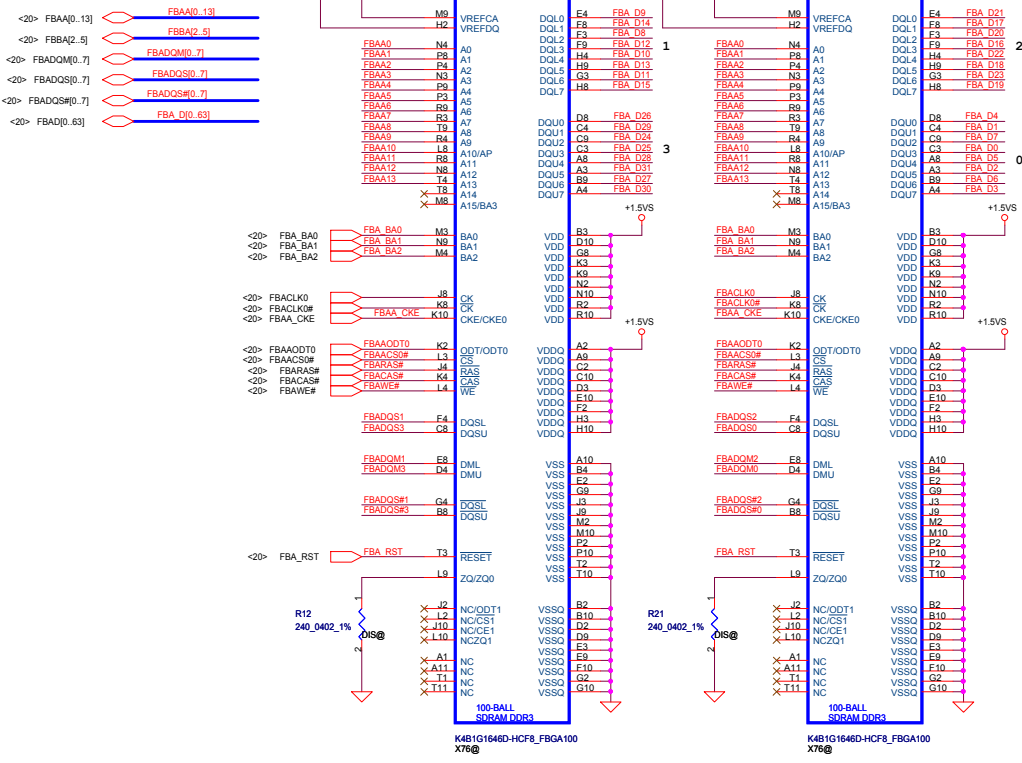


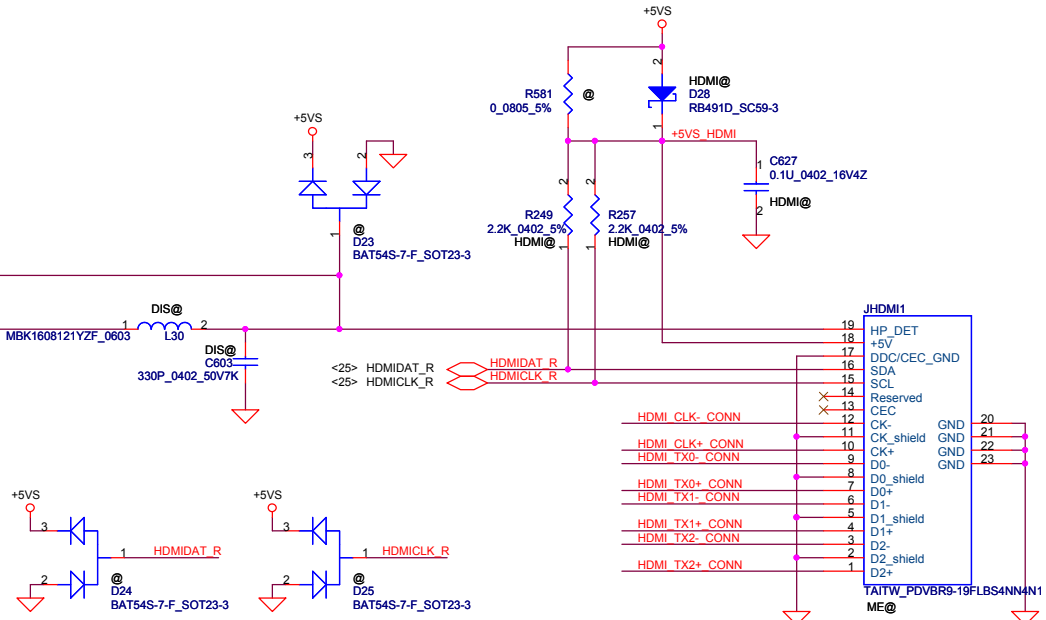
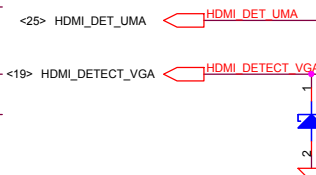
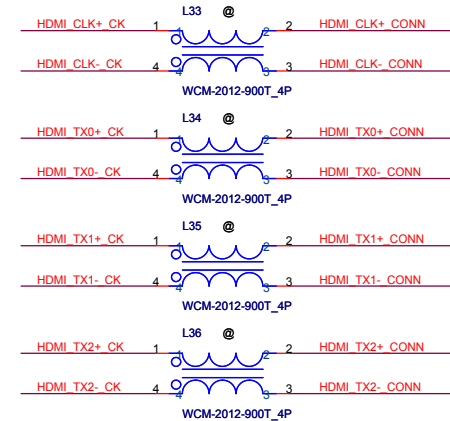
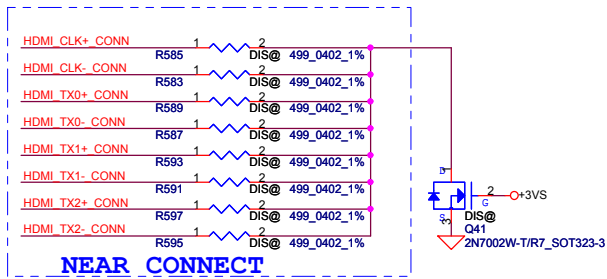
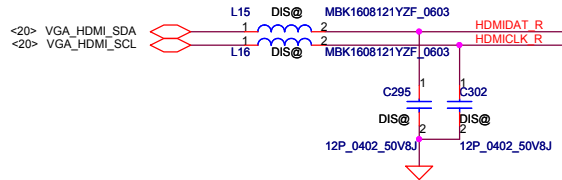
STRAP1 use for 3GIO_PADCFG to set 35K pull up.
 (PUN-04335-001_V10 HW9 update)

GPU	FB Memory (DDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (default)	K4W1G1646E-HC12					
		64Mx16	PD 10K	PU 15K	PD 20K	PD 30K	PU 35K
	Hynix 800MHz	H5TQ1G63BFR-12C					
		64Mx16	PD 10K	PU 15K	PD 15K	PD 30K	PU 35K
				X76			

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N11x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001





Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date		2008/03/25		Deciphered Date	
		2008/04/		Title	
				HDMI CONN	
				Size	
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P/N:SA00003GT00 (ASM1442)

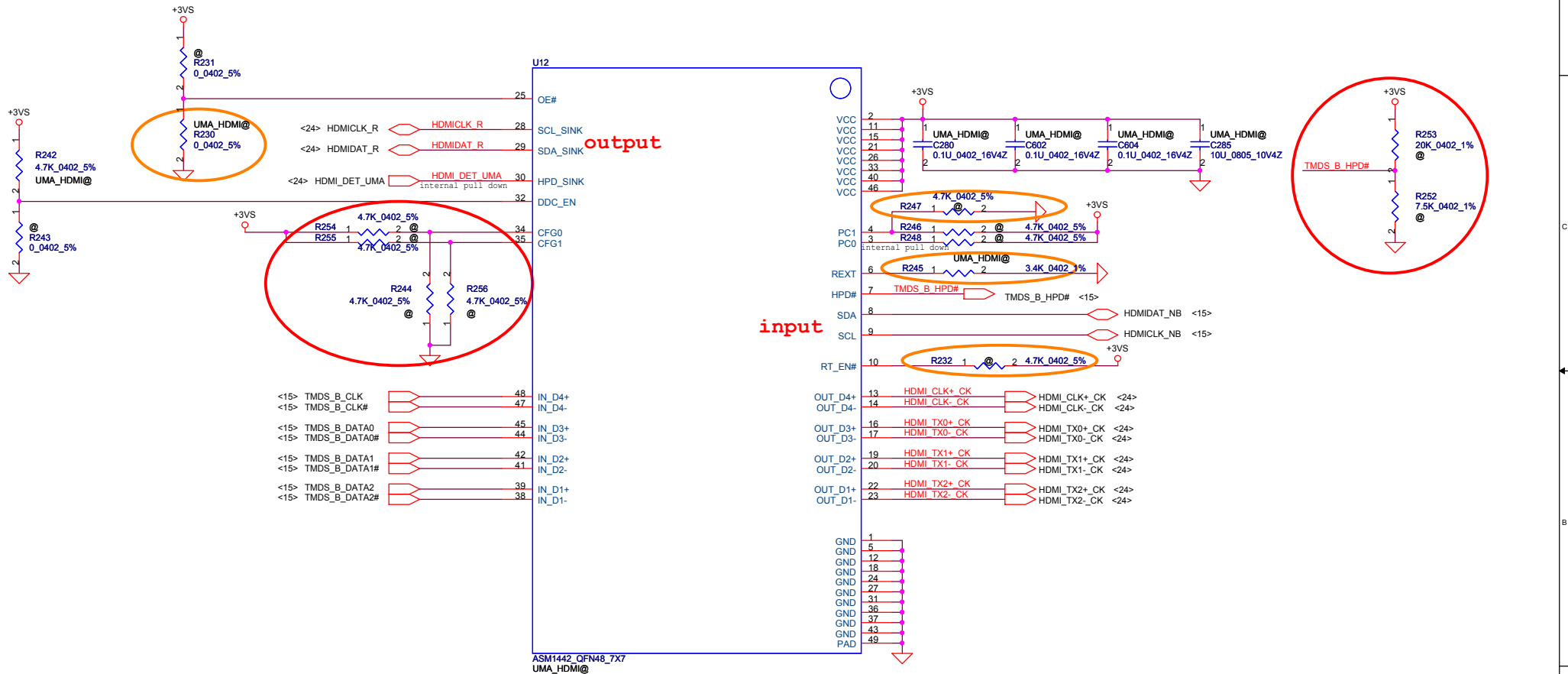
FOR asmedia R230 STUFF

RESERVE THE R232 PULL UP TO 3VS
RESERVE THE R247 PULL DOWN TO GND
CHANGE R245 FROM 499 TO 3.4K OHM

P/N:SA00002D700 (8101T)
P/N:SA00001U900 (CH7318A)

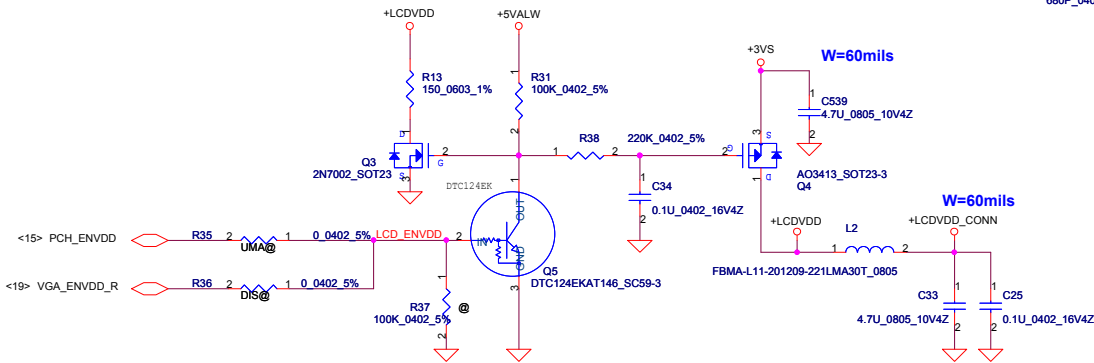
FOR 7318C

PIN6 PULL DOWN 1.2Kohm
PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm



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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Level Shifter ASM1442
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				Custom	LA-5751
				Date	Thursday, October 29, 2009
				Sheet	25 of 51
				Rev	0.3

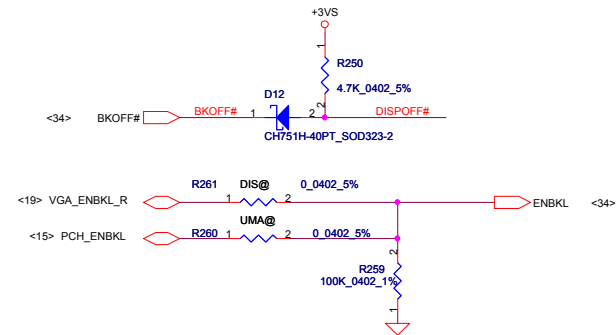
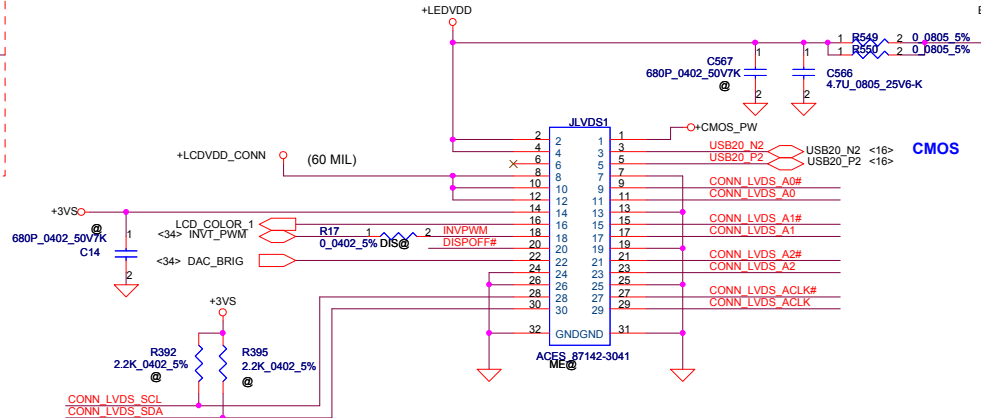
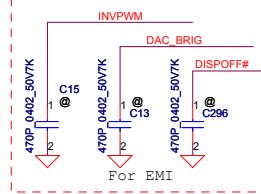
LCD POWER CIRCUIT



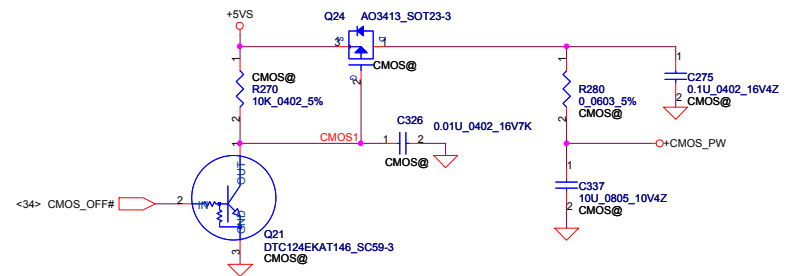
For GMCH DPST

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<15> EDID_CLK <15> EDID_DATA <15> LVDS_A0 <15> LVDS_A0# <15> LVDS_A1 <15> LVDS_A1# <15> LVDS_A2 <15> LVDS_A2# <15> LVDS_ACLK <15> LVDS_ACLK#



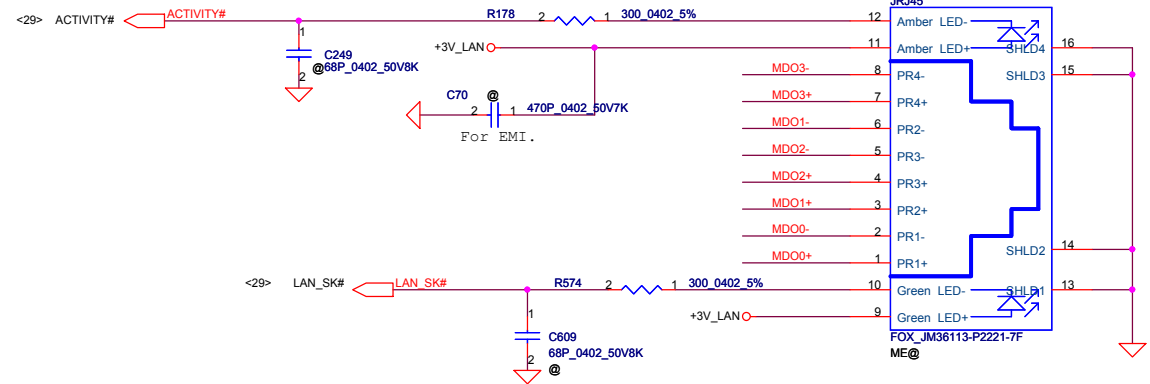
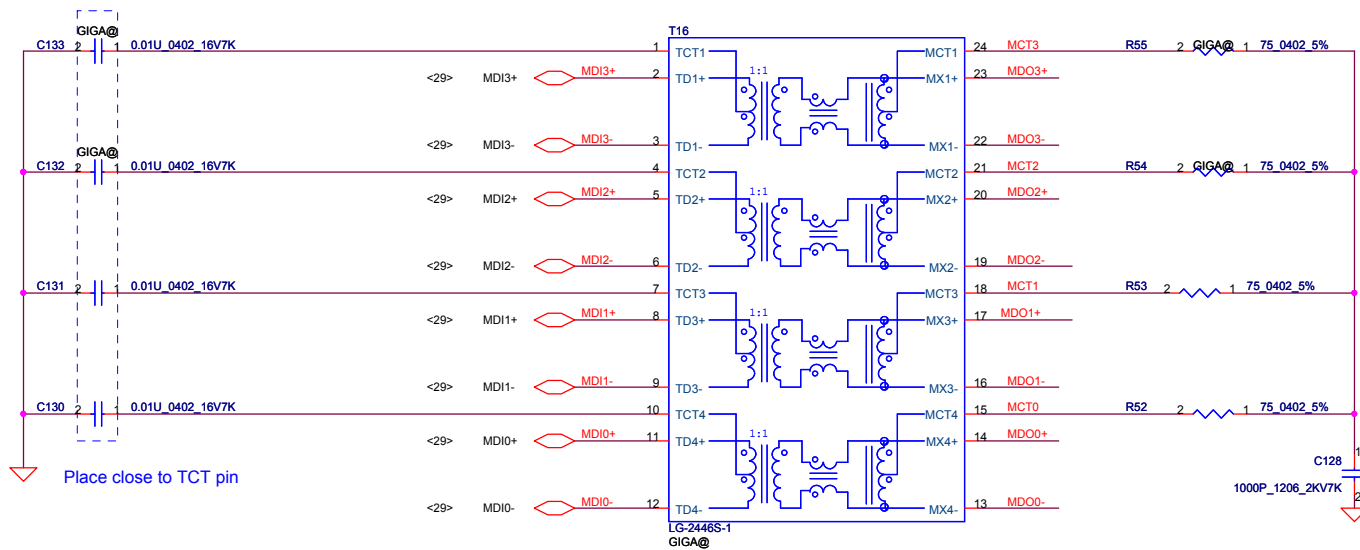
CMOS Camera



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Size B	Document Number	LA-5751		Rev 0.3	
Date:	Friday, October 30, 2009	Sheet	27	of 51	

WWW.AliSaler.Com

Close to T14

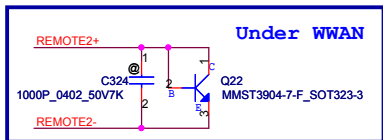
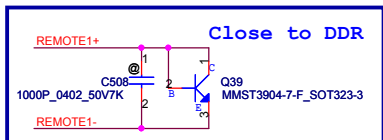
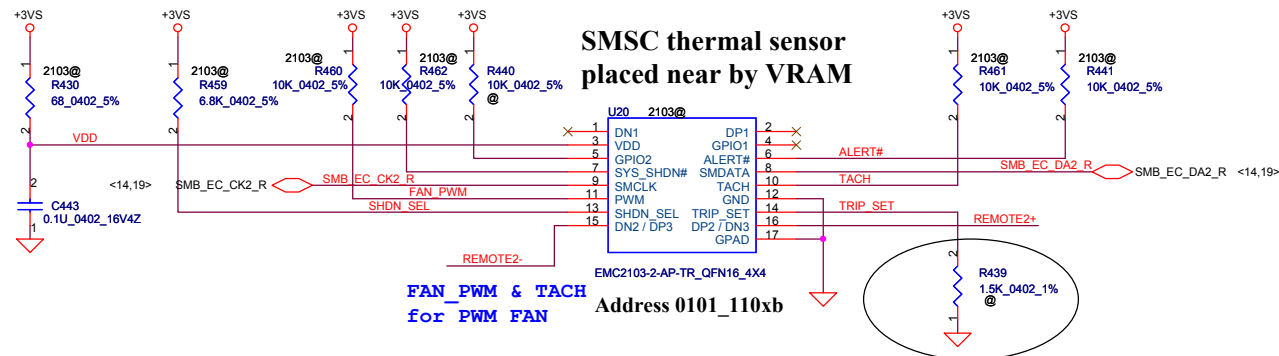


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						Size		Document Number		Rev	
						Custom		LA-5751		0.3	
						Date:		Friday, October 30, 2009		Sheet 30 of 51	

R430 1403@
0_0402_5%

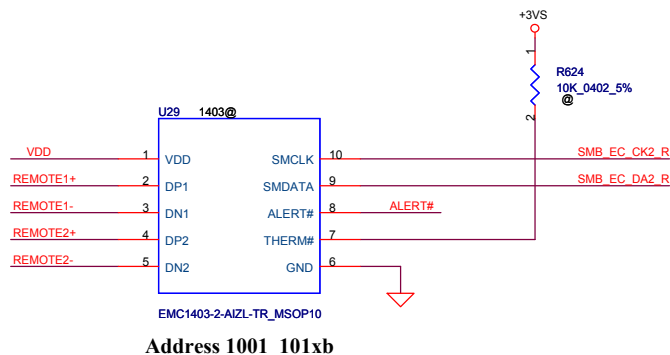
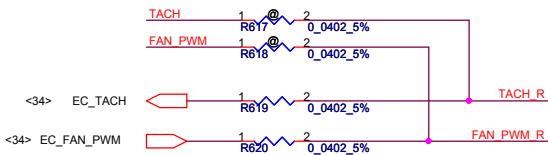
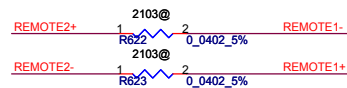
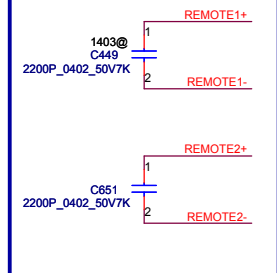
1403:
@C508/@C324=100p

SMSC thermal sensor placed near by VRAM

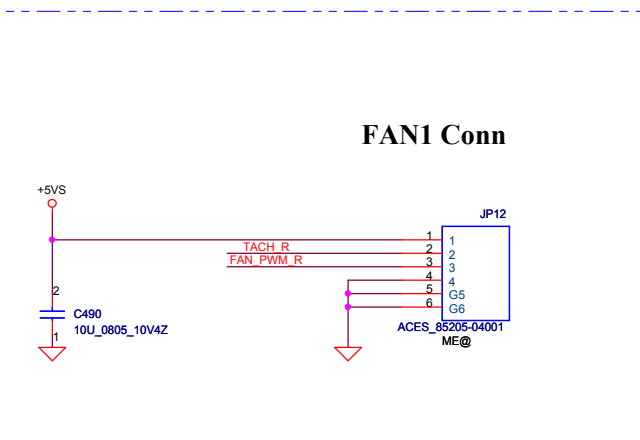


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Close U20



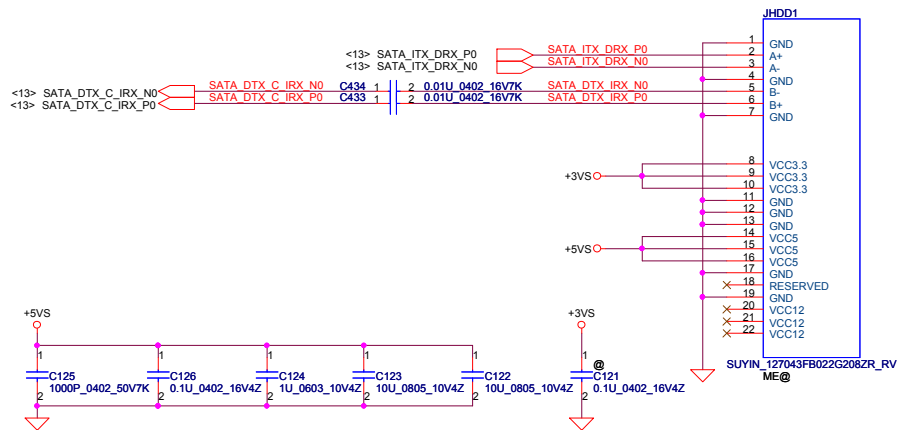
FAN1 Conn



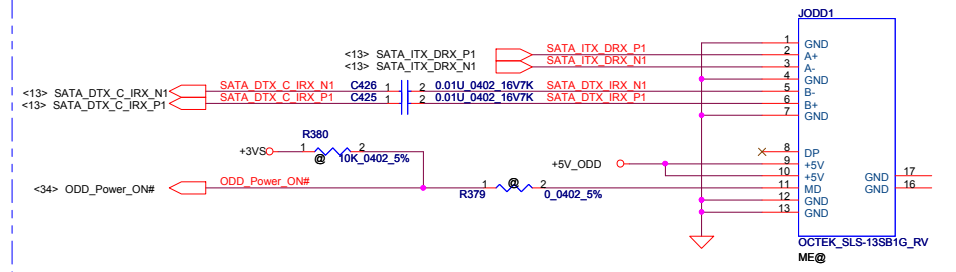
Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

Security Classification		Compal Secret Data		Compal Electronics,Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	EMC2103/1403_Thermal sensor/FAN
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				Date: Friday, October 30, 2009	Rev 0.3
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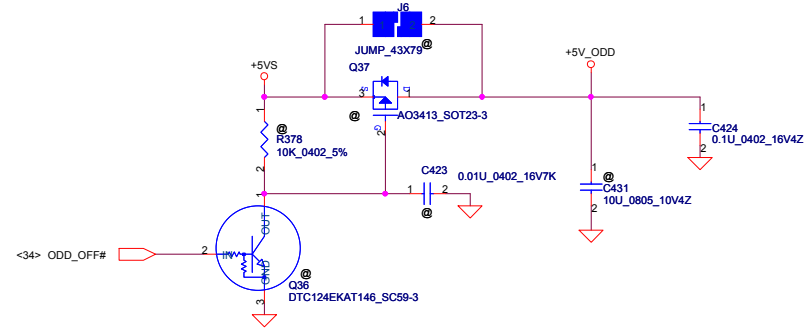
SATA HDD Conn.



SATA ODD Conn.

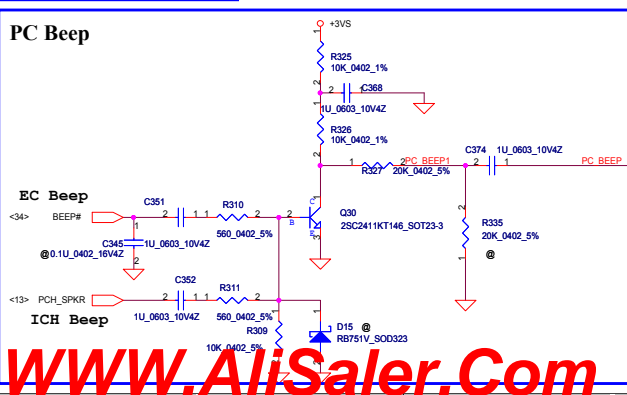
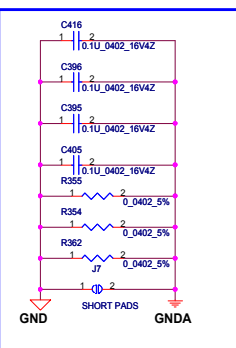
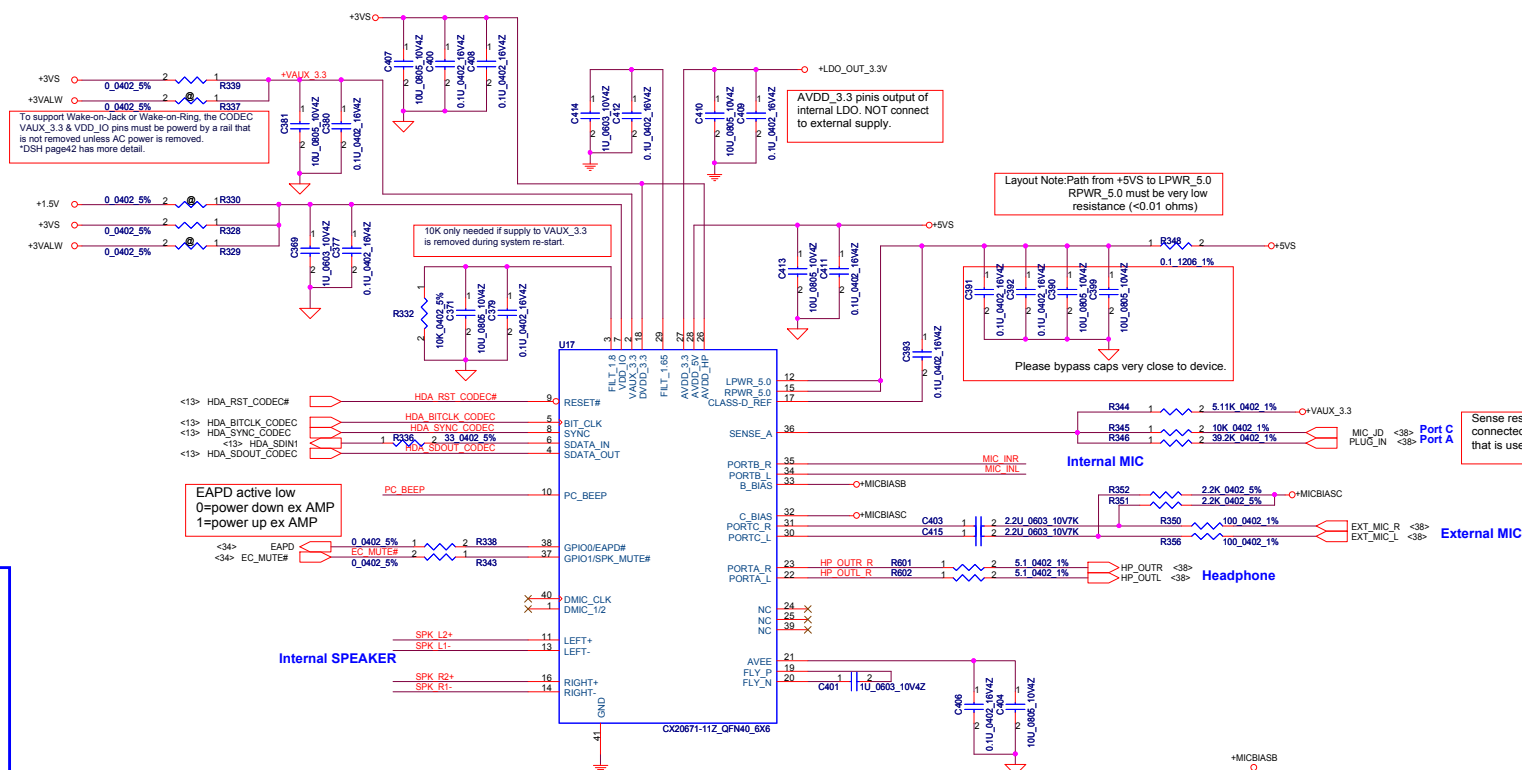
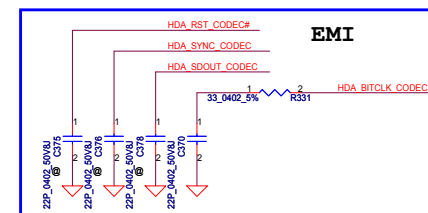


ODD Power Control

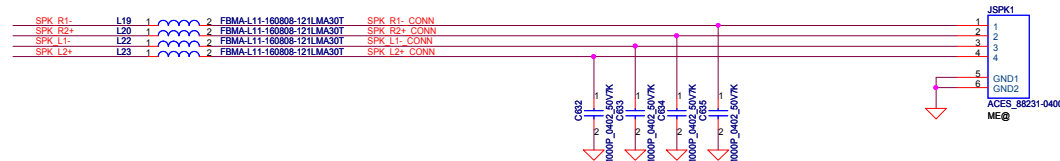


Security Classification	Compal Secret Data			Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	HDD/ODD Connector	
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CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



wide 20MIL

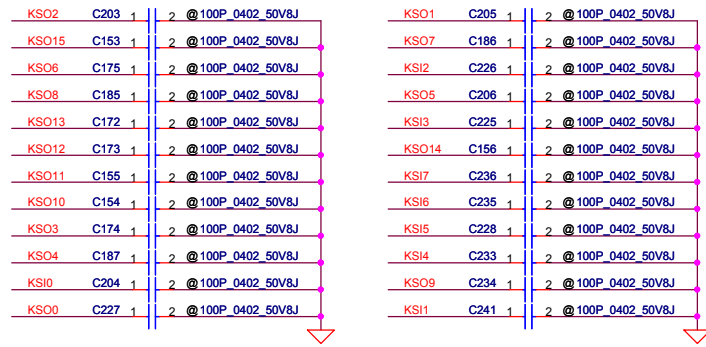


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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	CX20671 Codec	
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				Date:	Friday, October 30, 2009	Sheet 33 of 51



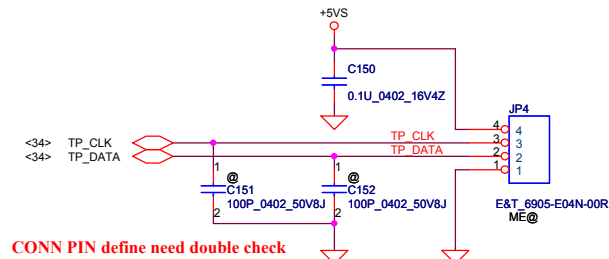
INT_KBD Conn.

KSII[0..7] <34>
KSO[0..15] <34>

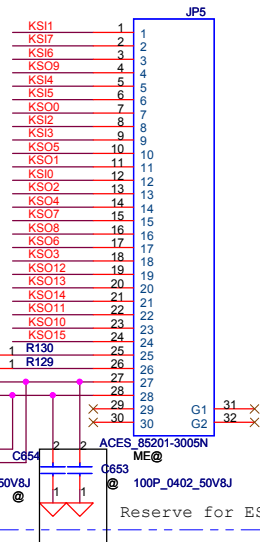


CONN PIN define need double check

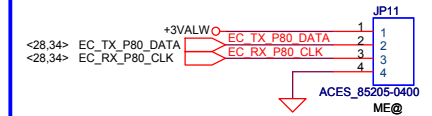
To TP/B Conn.



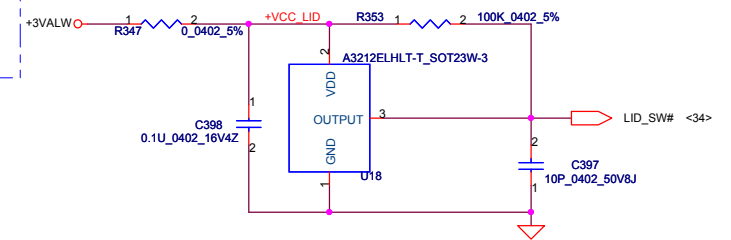
CONN PIN define need double check



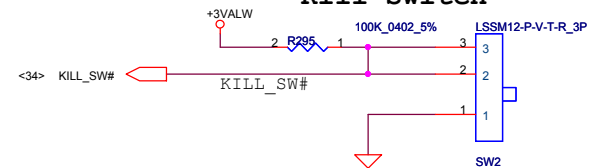
EC DEBUG PORT



Lid Switch



Kill Switch

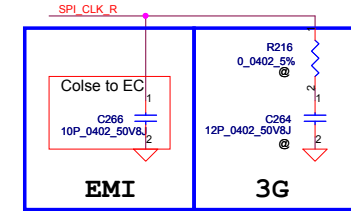
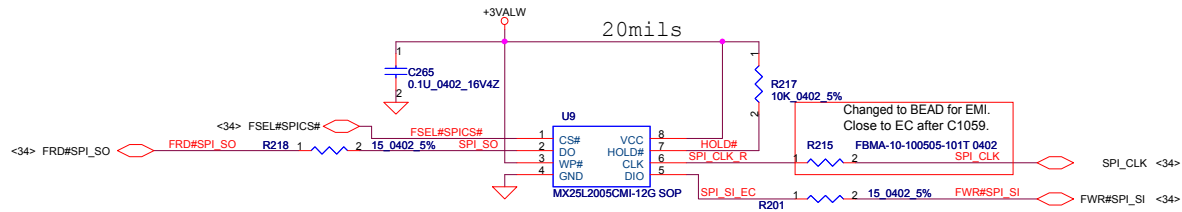


Kill

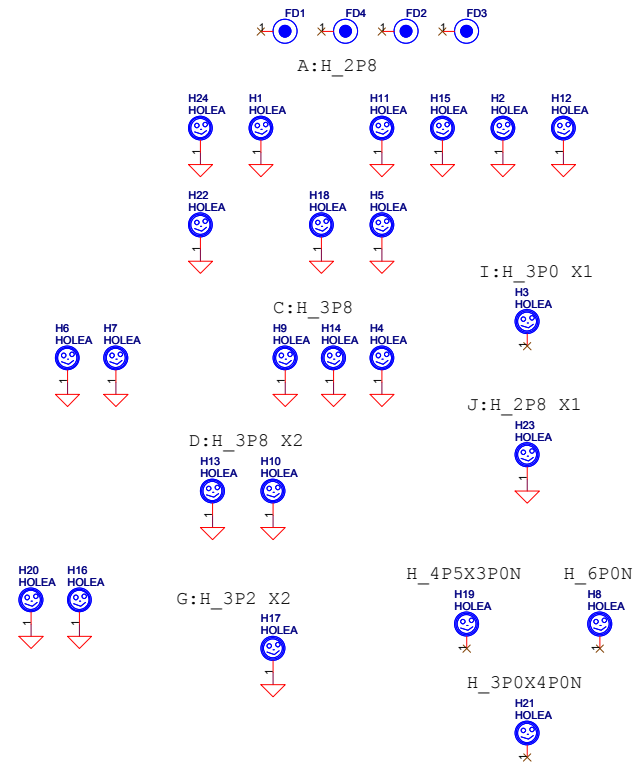
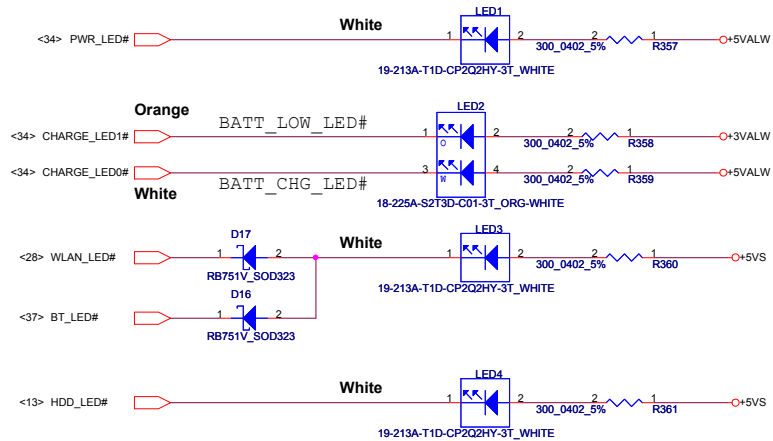
STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	KB /SW /LPC Debug Conn.	
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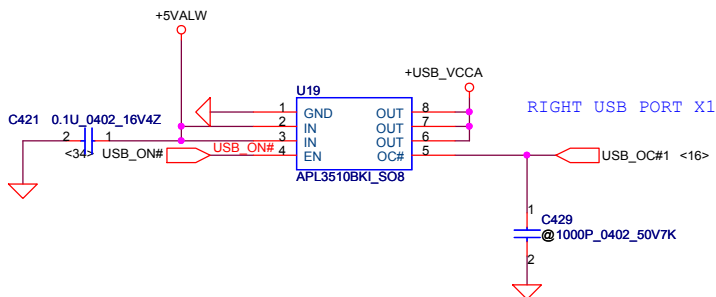
**FOR EC 256KB SPI ROM
(150mil PACKAGE)**



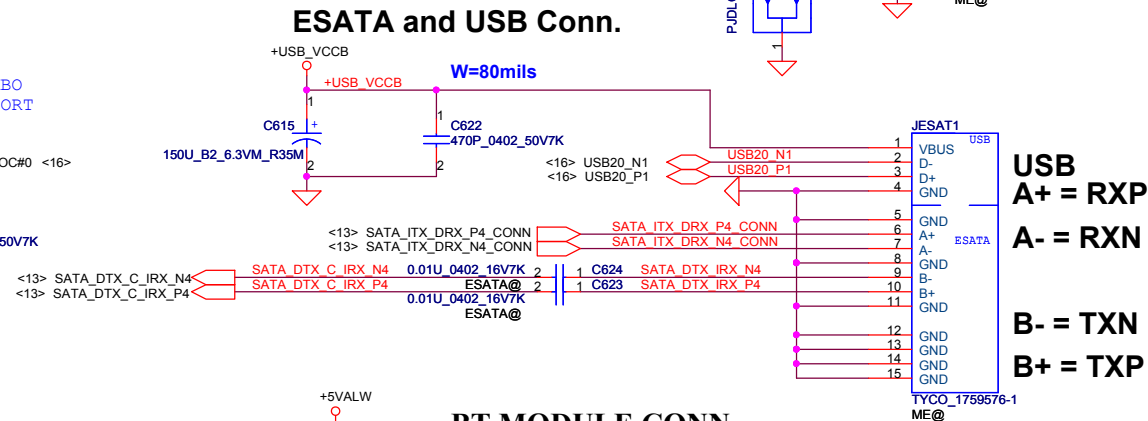
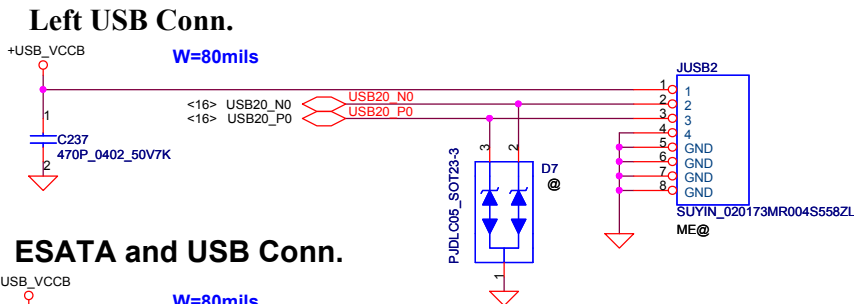
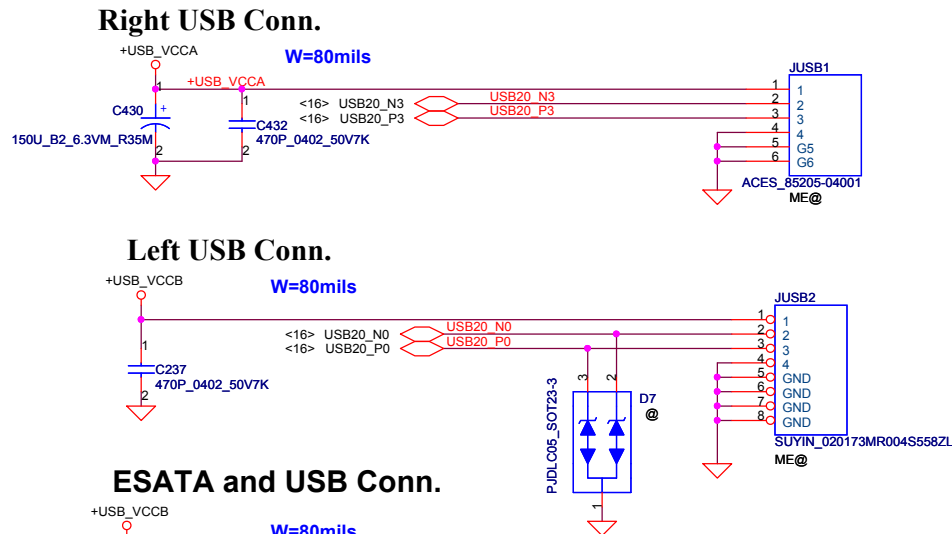
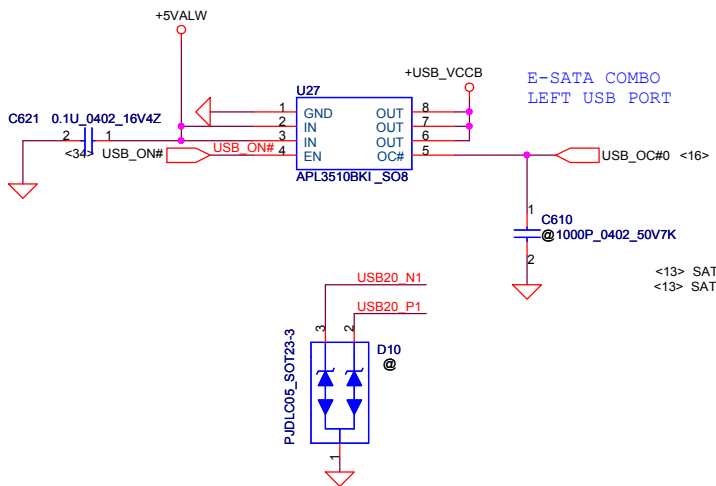
LED



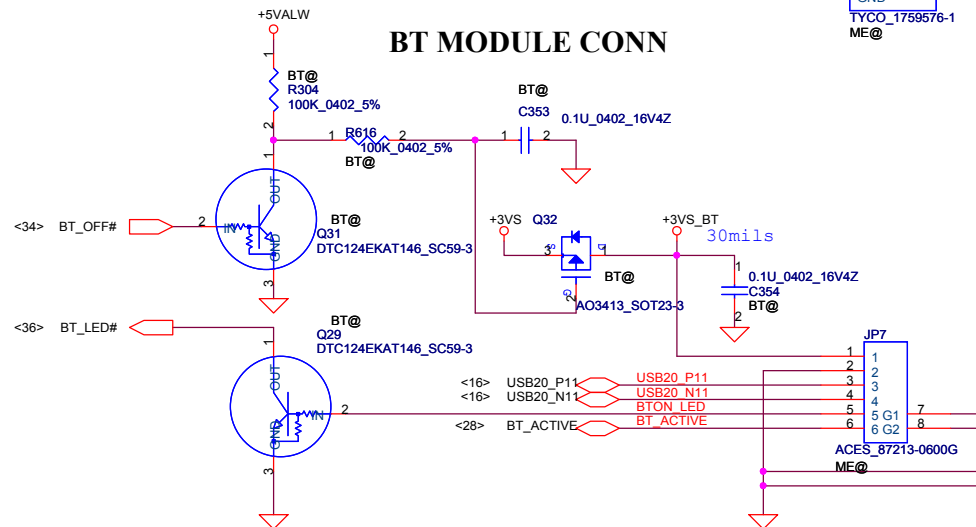
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	LED/EC SPI ROM		
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				Size B	Document Number	Rev 0.3
				LA-5751		
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U19/U27 USB power switch need update symbol to SA000039E00 (Low enable)

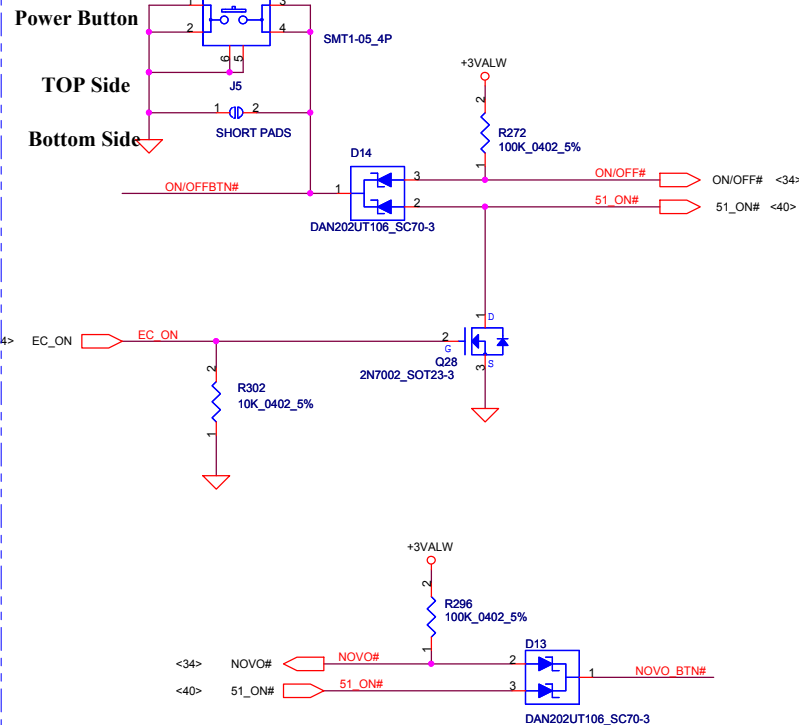


USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

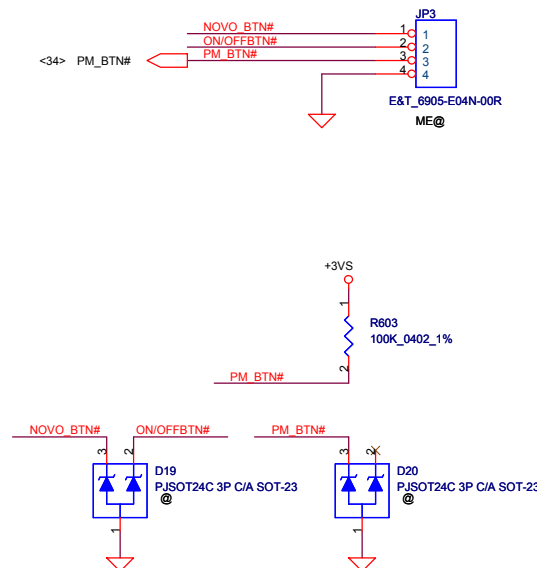


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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ON/OFF switch



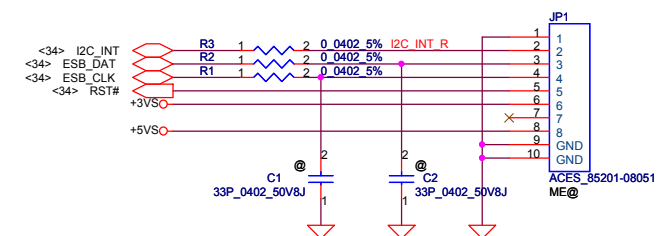
Power Bottom Board Conn. 4pin



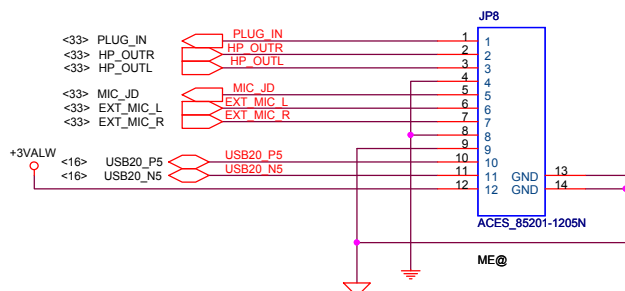
EMI REQUEST 1ST = SCA000000E00
2ST = SCA000000R00

Cap Sensor Board Conn. 6pin

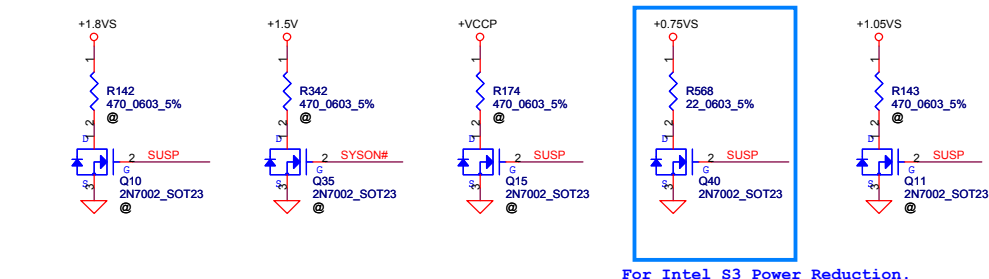
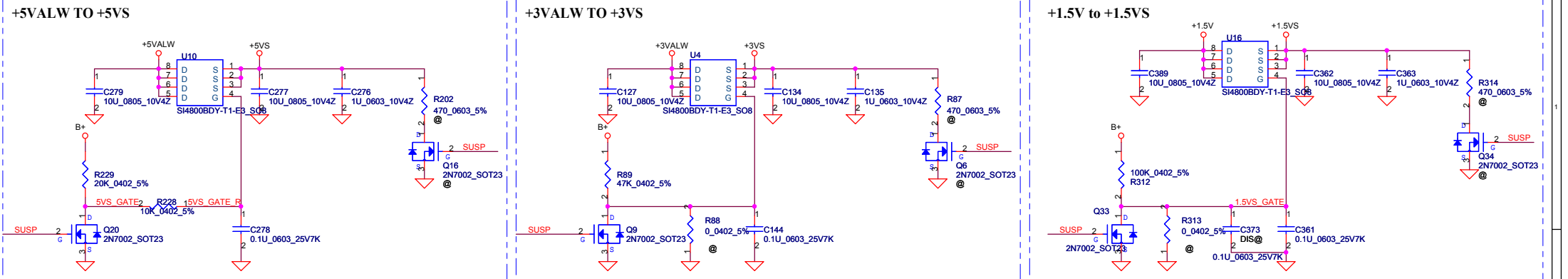
ENE SB3534



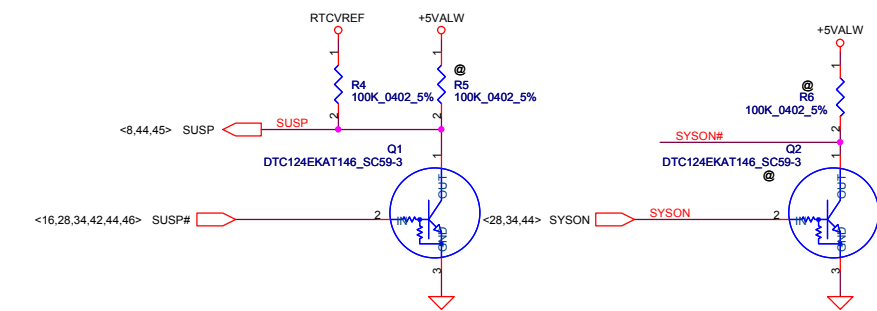
Card Reader/Audio Jack SB CONN



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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title
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Size Custom		Document Number		Rev 0.3
Date: Friday, October 30, 2009		Sheet 38 of 51		LA-5751

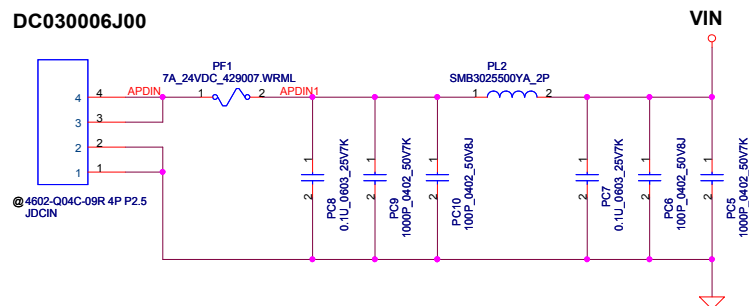


For Intel S3 Power Reduction.



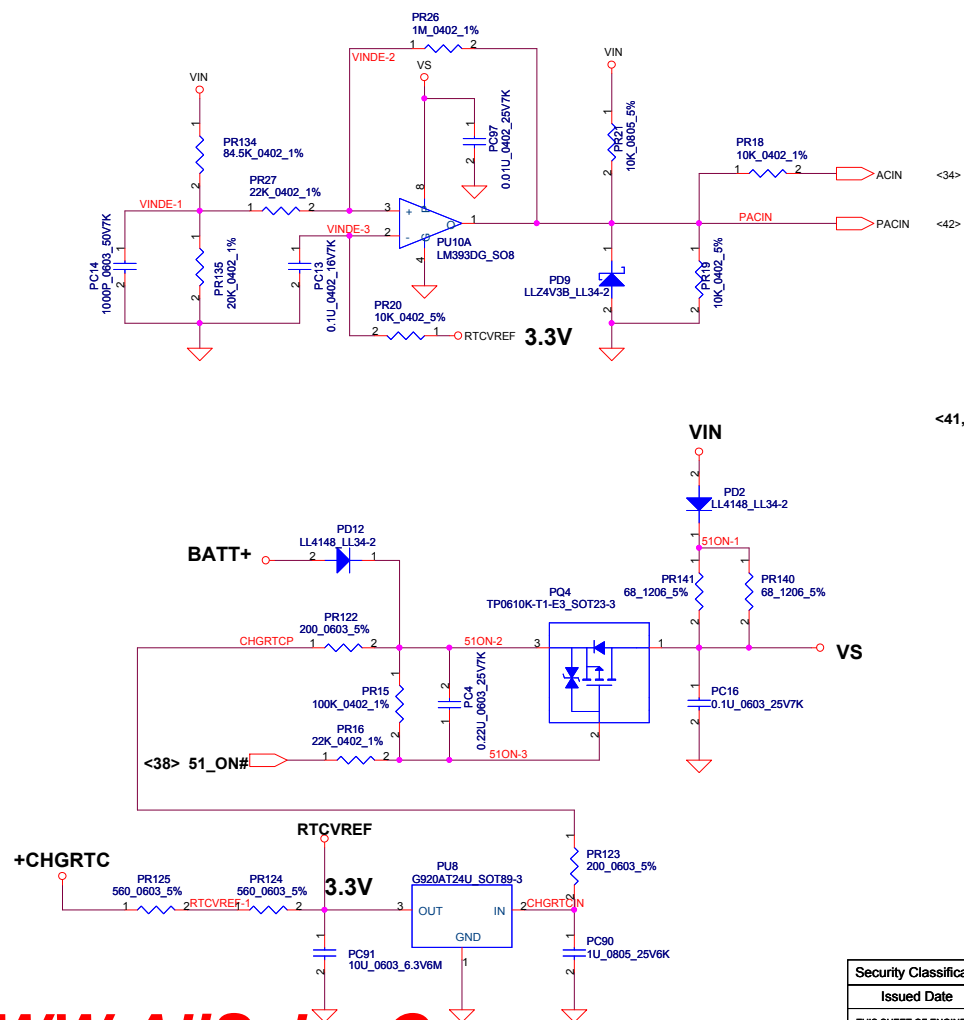
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Issued Date		2006/08/18	Deciphered Date	2007/8/18		Title
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				Size	Document Number	Rev
				Custpm	LA-5751	0.3
				Date:	Thursday, October 29, 2009	Sheet 39 of 51

DC030006J00



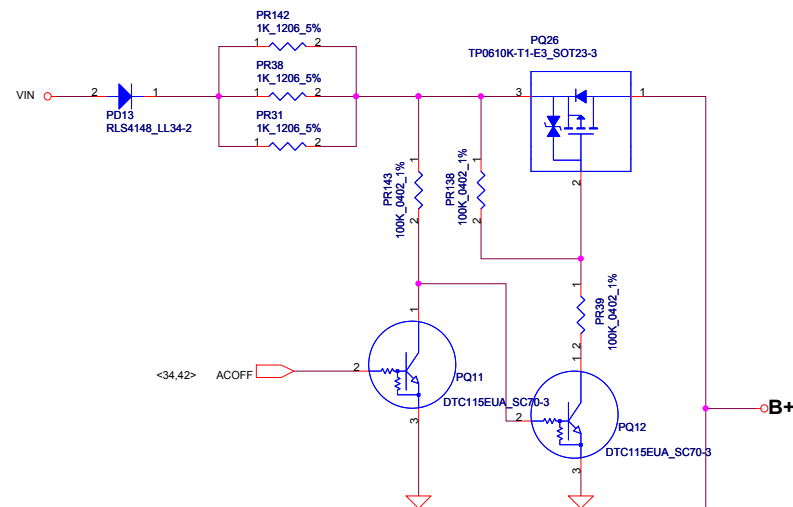
Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



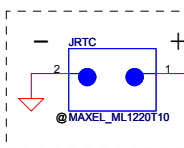
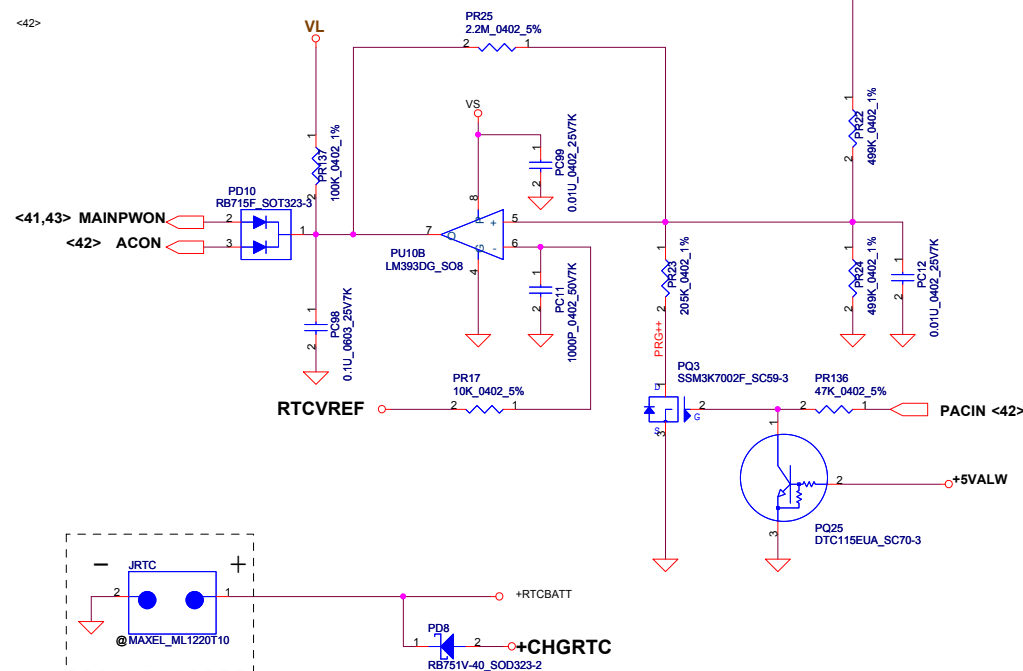
ACIN

	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V



BATT ONLY

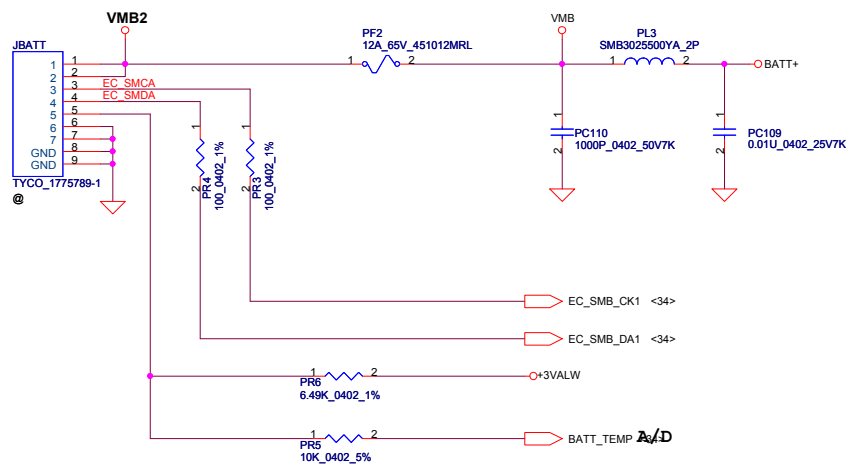
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



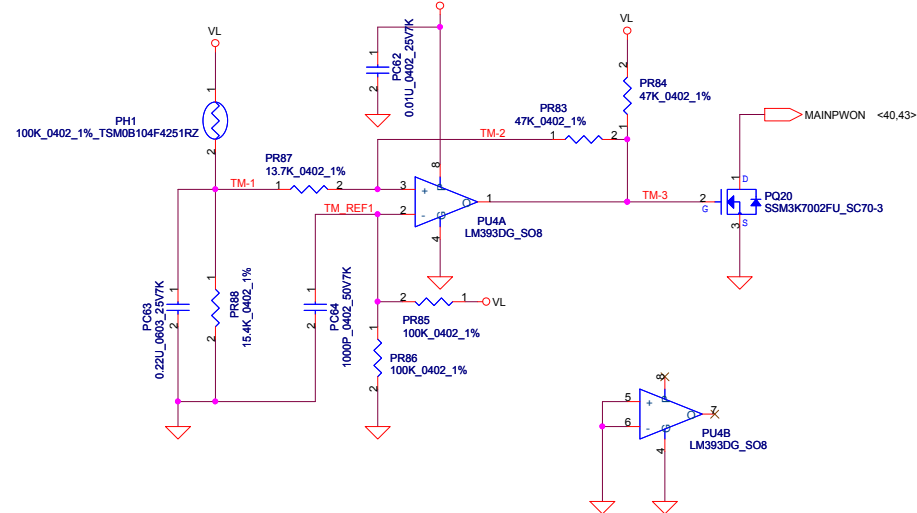
RTC Battery

Security Classification				Compal Secret Data				Compal Electronics, Inc.		
Issued Date				2009/01/06				Title		
Deciphered Date				2010/01/06				DCIN & DETECTOR		
Size				Document Number				Rev		
Custom								0.1		
Date:				Friday, October 30, 2009				Sheet		
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				51						

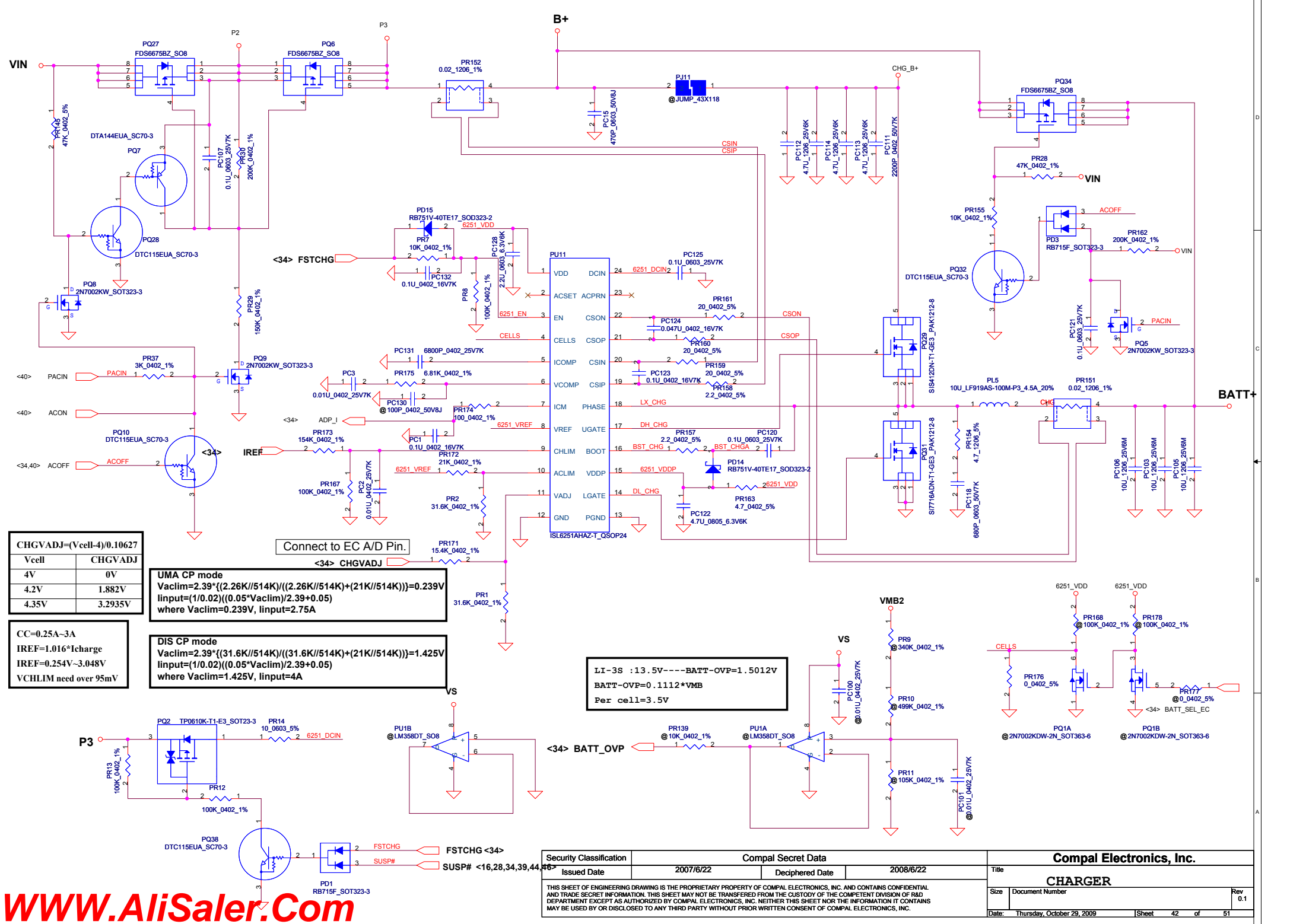
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PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A	
IREF=1.016*Icharge	
IREF=0.254V~3.048V	
VCHLIM need over 95mV	

UMA CP mode
 $V_{acim}=2.39*((2.26K//514K)/((2.26K//514K)+(21K//514K)))=0.239V$
 $input=(1/0.02)((0.05*V_{acim})/2.39+0.05)$
where $V_{acim}=0.239V$, $input=2.75A$

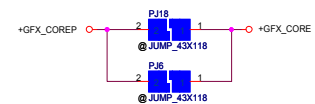
DIS CP mode
 $V_{acim}=2.39*((31.6K//514K)/((31.6K//514K)+(21K//514K)))=1.425V$
 $input=(1/0.02)((0.05*V_{acim})/2.39+0.05)$
where $V_{acim}=1.425V$, $input=4A$

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

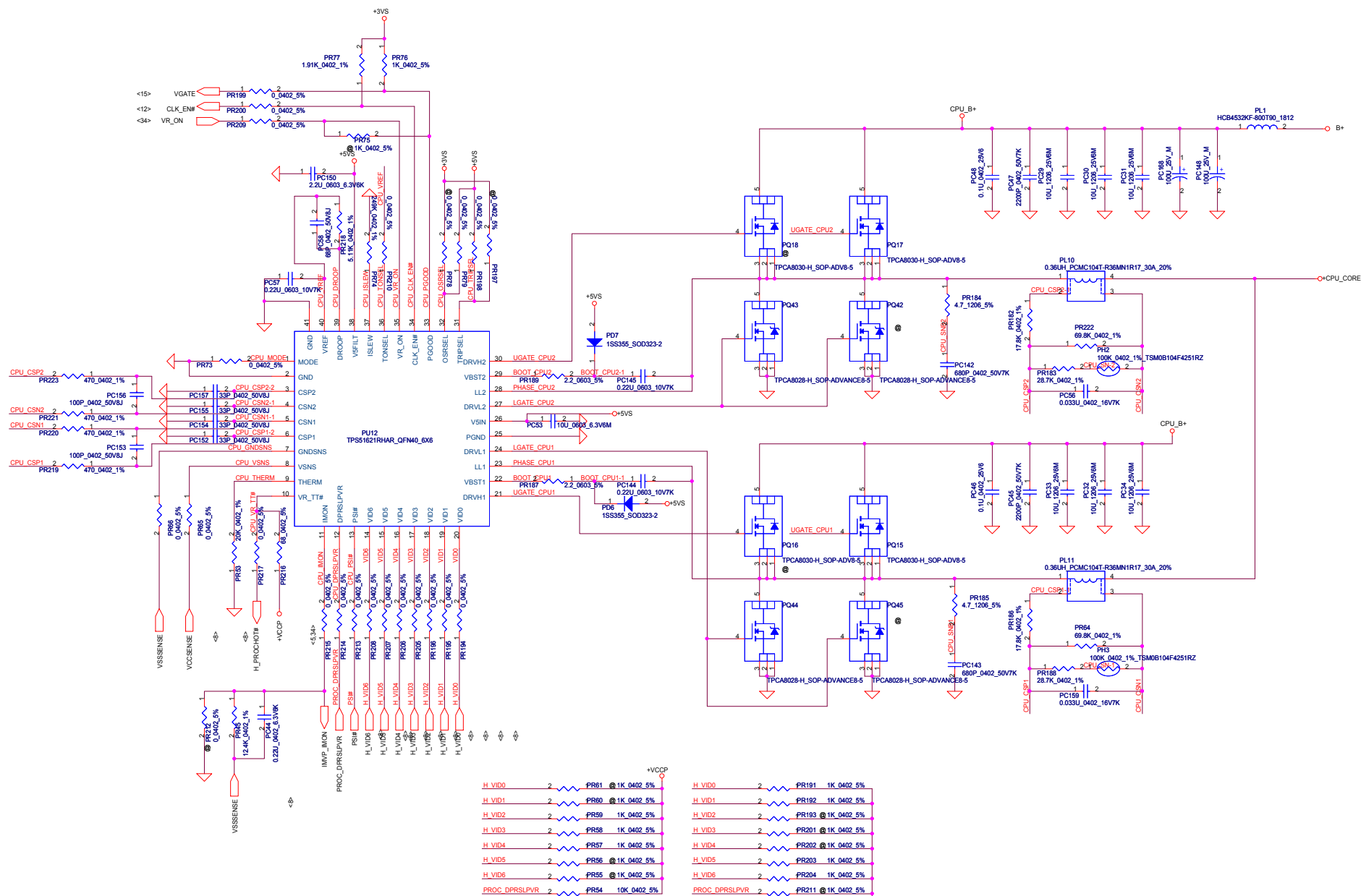
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									Size	
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Clarkfield: VID(0-5):001101
 Auburndale: VID(0-5):001110

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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE	EVT TO DVT
1		P15	Add C638~C645	For UMA HDMI	
2		P05	Add test point for BCLK_ITP, BCLK_ITP#, PRDY#	For XDP connector	
3		P32, P28	Change J6 size & unstuff ODD power control components Change J4 size	Disable ODD power control circuit	
4		P17	Stuff C262	For UMA CRT	
5		P34	Change R291, R294 from +3VALW to +3VS		
6		P38	Add R603 pull high to +3VS	For PM_BTN#	
7		P38	Change JP1 from 6 pin to 8 pin , Change JP8 from 14 pin to 12 pin , unstuff R322	For LED color changed Remove CLK_48M_CR	
8		P29, P34	Change EN_WOL to EN_WOL#	For identify clearly	
9		P34	EC pin26-> EC_FAN_PWM , pin75->PCH_TEMP_ALERT , pin34->PROCHOT# , pin66->NOVO#	EC GPIO arrangement	
10		P31	Change JP12 pin define	For EC FAN control	
11		P16	Change U5 pin3, pin5	POWER , GND reversed	
12		P15	Add U28 for ICH_POK & VGATE	Reserved	
13		P12	Unstuff R278, stuff R269 and change U14 to SA00003HQ00	For low power CLK GEN	
14		P13	Change U3 from 2MBytes to 4MBytes	For 4MBytes SPI ROM for PCH	
15		P29	Correct Q17 to P/N:SB000007600	For +3V_LAN power	
16		P16	Add C646 for BUF_PLT_RST#	Reserved for BUF_PLT_RST# overshoot problem	
17		P36	Change U9 from 2MBytes to 256KBytes	For 256KBytes SPI ROM for EC	
18		P03	UMA_HDMI@ , HDMI@ , BT@ , 3G@ , ESATA@ , CMOS@	New BOM structure	
19		P08	Add R608	For PSI# pull down	
20		P37	Delete D18		
21		P16	Unstuff R210, R212	Set Boot BIOS Strap to SPI	
22		P22	Change & stuff R475 to 30K, R51 to 15K Unstuff R474, R50	For N11M-GE1 QS sample	
23		P25	Unstuff R246	Level shift default setting	
24		P39	Change C373 to DIS@	for DIS power sequence	
25		P15, P16, P17	Change R436 from 1K to 10K Change C447 from 0.1u to 1u Delete R514 Unstuff C493, C494 Reserve R609	Check list Rev2.0 update	
27		P34	Add R607	Reserved for KB926 SPI STRAP PIN	
28		P36	Change LED1, LED3, LED4 to white color LED2 to orang\white color and orange connect to +3VALW		
29		P14	Change exp-card from PCIE port 1 to port 5	SW BIOS request	
30		P38	Unstuff SW1		
31		P13, P34	Change X1, X2 footprint		
32		P12	Change C348 to 22p, C349 to 22p	For Crystal matching	
33		P13, P20	Add C647~C650 12p, stuff C370->22p, R331->33	Reserved for RF team	
34		P36	Delete JP6	SPI ROM socket	
35		P37	Change C430, C615 footprint to B2 type		
36		P27, P32, P37	Change Q4, Q24, Q32, Q37 footprint to A03413		

Compal Electronics, Inc.		
Title		
HW PIR		
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5		4		3		2		1	
NO	DATE	PAGE	MODIFICATION LIST		PURPOSE		EVT TO DVT		
37		P34	Change C320 to 0805 type						
38		P08	Unstuff C268		For CPU VDDQ (DDR3 1.5V rails)				
39		P34	Change C252,C258 from 10u to 22u						
			Change ODD_power_on# from U13 pin28 to pin 76		EC GPIO arrangement				
40		P31	Add EC_TACH on U13 pin28 to JP12						
			Change U20 to EMC1403, add C651		Change thermal sensor solution to EMC1403				
41		P05	Add Q42,R610		Reserve for +0.75V enable option				
42		P34, P35	Add C652, C653, C654		Reserve for NUM_LED#,CAPS_LED# ESD request				
43		P34	Add R611, R612, R613		For EC_FAN_PWM, EC_TACH				
NO	DATE	PAGE	MODIFICATION LIST		PURPOSE		DVT TO PVT		
1		P34	Reseve R614,R615.		EC_ID to identify KB926 D or E				
2		P34	Stuff R607		KB926 SPI STRAP PIN				
3		P33	Stuff C632~C635		EMI request				
4		P16	Stuff C646		For PLT_RST# singnal quality				
5		P37	Add R616 100K, change R304 to 100K, C353 to 0.1u		For +3VS_BT power on rising time				
6		P37	Changed R304 pin1 from +5VS to +5VALW		For +3VS_BT power on leakage				
7		P5	Stuff R283, C338 0.01u		For S3 power reduction				
8		P31	Add U29		Colay EMC2103/EMC1403 thermal sensor				
5		4		3		2		1	
<div>Compal Electronics, Inc.</div> <div>HW PIR</div> <div><div>Size B</div><div>Document Number LA-5751</div><div>Rev 0.3</div></div> <div><div>Date:</div><div>Thursday, October 29, 2009</div><div>Sheet</div><div>51</div><div>of</div><div>51</div></div>									