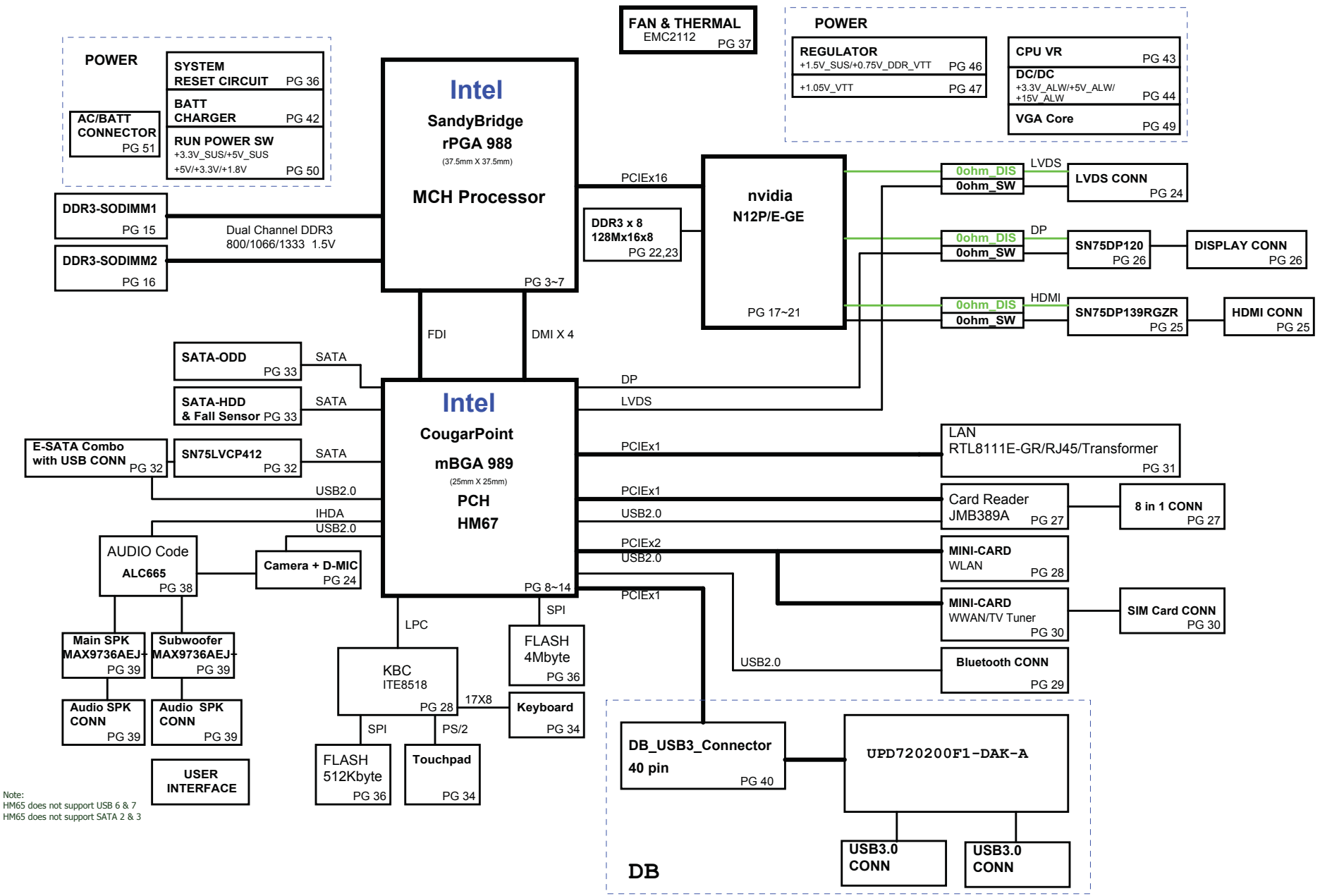
_DIS ==> Discrete Only
_SW ==> Optimus Only
_UMA ==> UMA Only

GM6C MLK Optimus, Discrete & UMA

VER : 1A
PWA:
PWB:



Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Block Diagram	1A

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Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
⏚ GND	ALL	

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

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	Frontage	1A

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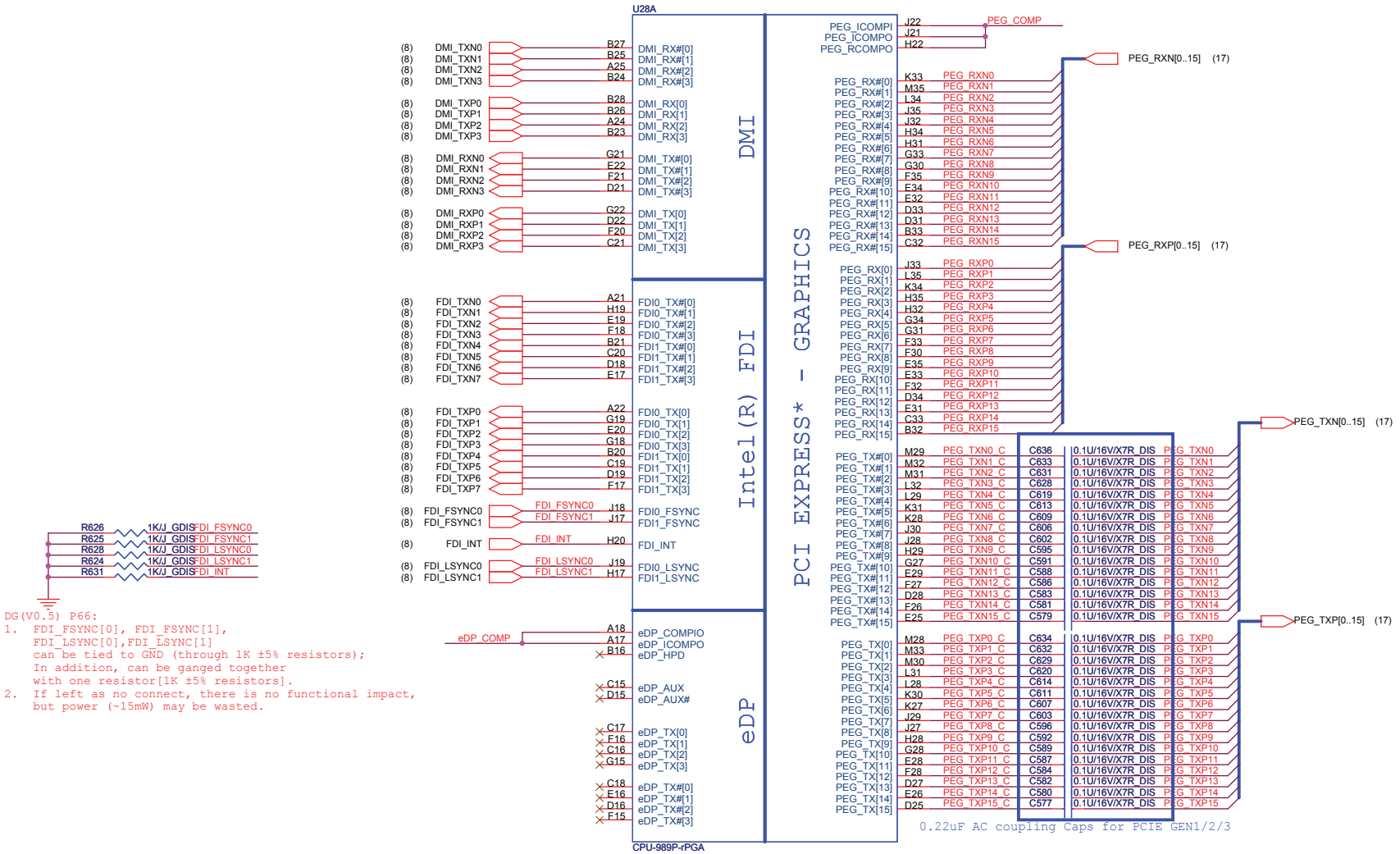
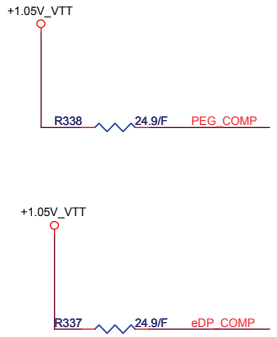
Sandy Bridge Processor (DMI,PEG,FDI)



R626 R625 R628 R624 R631 — 1K/J_GDIS

DG(V0.5) P66:
1. FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],FDI_LSYNC[1] can be tied to GND (through 1K ±5% resistors); In addition, can be ganged together with one resistor[1K ±5% resistors].
2. If left as no connect, there is no functional impact, but power (~15mW) may be wasted.

DP & PEG Compensation



Quanta Computer Inc.	
PROJECT : GM6C MLK DIS	
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Sandy Bridge Processor (CLK,MISC,JTAG)

WW31.MOW Page 5 (SNB_IVB# N.A at SNB EDS #27637 0.7v1)

U28B

MISC: PROC_SELECT# (TP19, H_SNB_IVB#, C26); SKTOCC# (AN34, (28) H_CPUDET#)

CLOCKS: BCLK (A28), BCLK# (A27) → CLK_CPU_BCLKP (10), CLK_CPU_BCLKN (10) DMI clock

DPLL_REF_CLK (A16), DPLL_REF_CLK# (A15) → CLK_DPLL_SSCLKP_R, CLK_DPLL_SSCLKN_R; R629 Ra *0_NC; → CLK_DPLL_SSCLKP (10), CLK_DPLL_SSCLKN (10) eDP clock

R627 Rb 1K/J, R630 1K/J → +1.05V_VTT; Rc

	DIS	SW
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

THERMAL: CATERR# (AL33, TP21, TP_CATERR#); PECI (AN33, (28) EC_PECI, R352 43/J H_PECI); PROCHOT# (AL32, (28,42,43) VR_HOT#, R358 56/J H_PROCHOT#); THERMTRIP# (AN32, (12) H_THERM#)

shut down when asserted

Over 130 degree C will drive low

DDR3 MISC: SM_DRAMRST# (R8) → CPU_DRAMRST#

S3 Power reduce

SM_RCOMP[0] (AK1), SM_RCOMP[1] (A5), SM_RCOMP[2] (A4) → SM_RCOMP_0 R322 140/F, SM_RCOMP_1 R312 25.5/F, SM_RCOMP_2 R313 200/F

26.1 change to 25 ohm

PWR MANAGEMENT: PM_SYNC (AM34, (8) PM_SYNC, R372 *0/J_short_NC PM_SYNC_R); UNCOREPWRGOOD (AP33, (12) H_PWRGOOD, R373 *0/J_short_NC PWRGOOD_R, R374 10K/J); SM_DRAMPWROK (V8, PM_DRAM_PWRGD_R); RESET# (AR33, +1.05V_VTT R368 *75/J_NC, CPU_PLTRST# R359 *43/J_NC CPU_PLTRST#_R)

provide power management status (form PCH to CPU)

JTAG & BPM: PRDY# (AP29), PREQ# (AP27 XDP_PREQ#) → T5; TCK (AR26 XDP_TCLK), TMS (AR27 XDP_TMS), TRST# (AP30 XDP_TRST#); TDI (AR28 XDP_TDI), TDO (AP26) → T2; DBR# (AL35) → T11; BPM#[0] (AT28) → T3, BPM#[1] (AR29) → T6, BPM#[2] (AR30) → T7, BPM#[3] (AT30) → T10, BPM#[4] (AP32) → T9, BPM#[5] (AR31) → T4, BPM#[6] (AT31) → T12, BPM#[7] (AR32) → T8

CPU-989P-rPGA

+1.05V_VTT

XDP_TMS R364 51/J
XDP_TDI R363 51/J
XDP_PREQ# R365 *51/J_NC
XDP_TCLK R341 51/J
XDP_TRST# R375 51/J

Option for Prochot# function
68 ohm for unused, 62 ohm for used

+1.05V_VTT

H_PROCHOT# R367 *68/J_NC
VR_HOT# R366 62/J

IN	OUT
L	L
H	High-Z

+3.3V_SUS

U19 *74LVC1G07GW_NC: NC, VCC (5), IN (2), GND, OUT (4) CPU_PLTRST#

C414 *0.1U/16V/X7R_NC

level shift for reset pin(07/12)

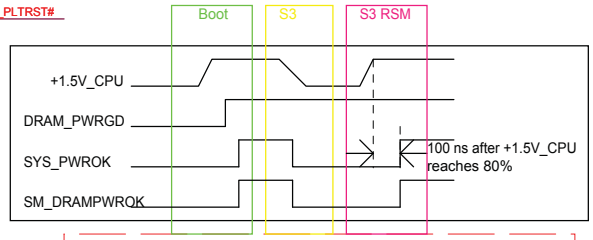
(11,17,27,28,29,30,31,40) PLTRST#

R714 1.5K/F

CPU_PLTRST#_R

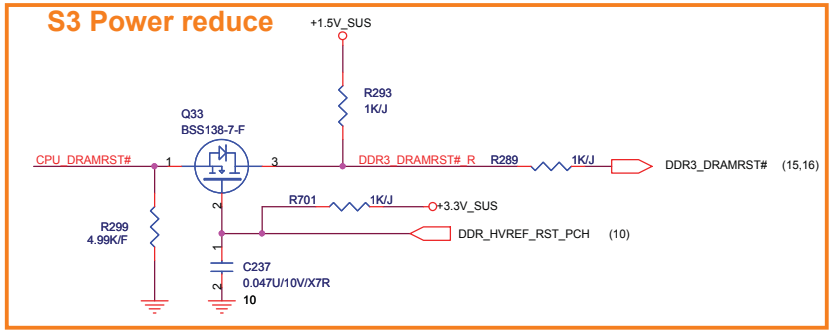
R723 750/F

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	High-Z

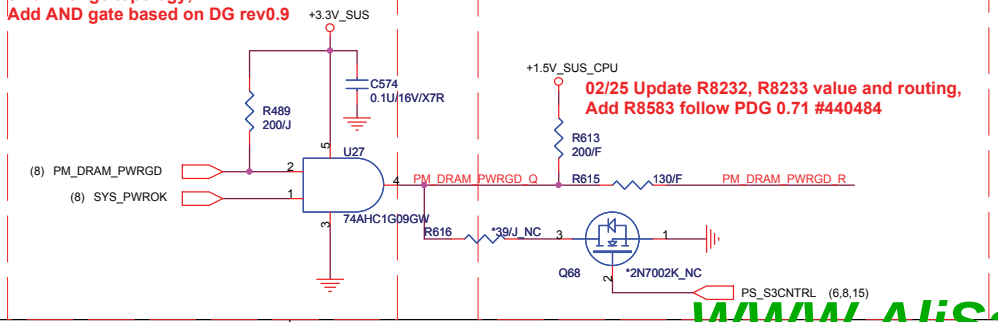


+1.5V_SUS keep DDR3_DRAMRST# high to avoid CPU_DRAMRST# low when into S3 (Because can't reset DRAM when into S3)

S3 Power reduce



3/16 Change topology; Add AND gate based on DG rev0.9



Quanta Computer Inc.

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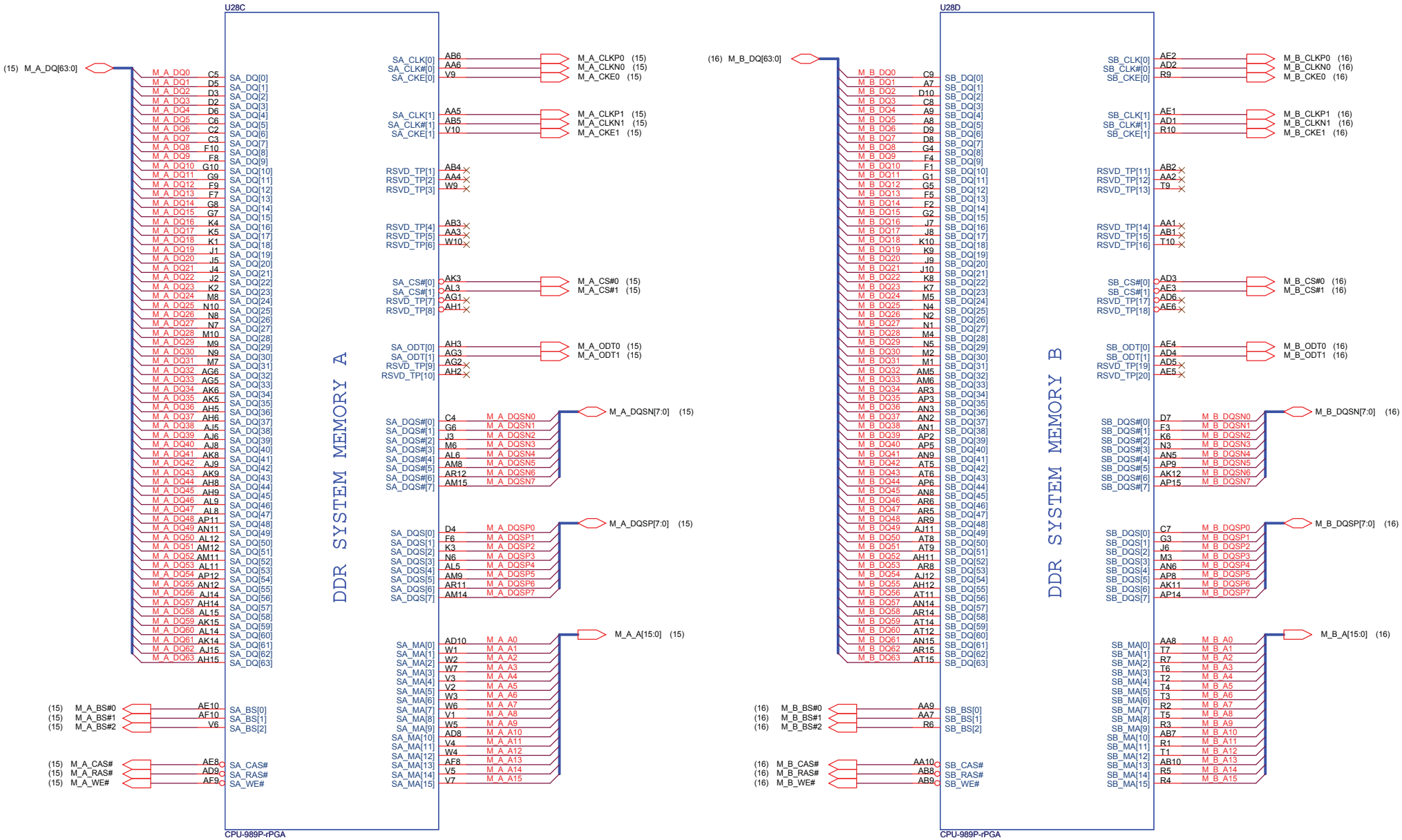
Sandy Bridge Processor (DDR3)



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

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	Sandy Bridge 3/5	1A
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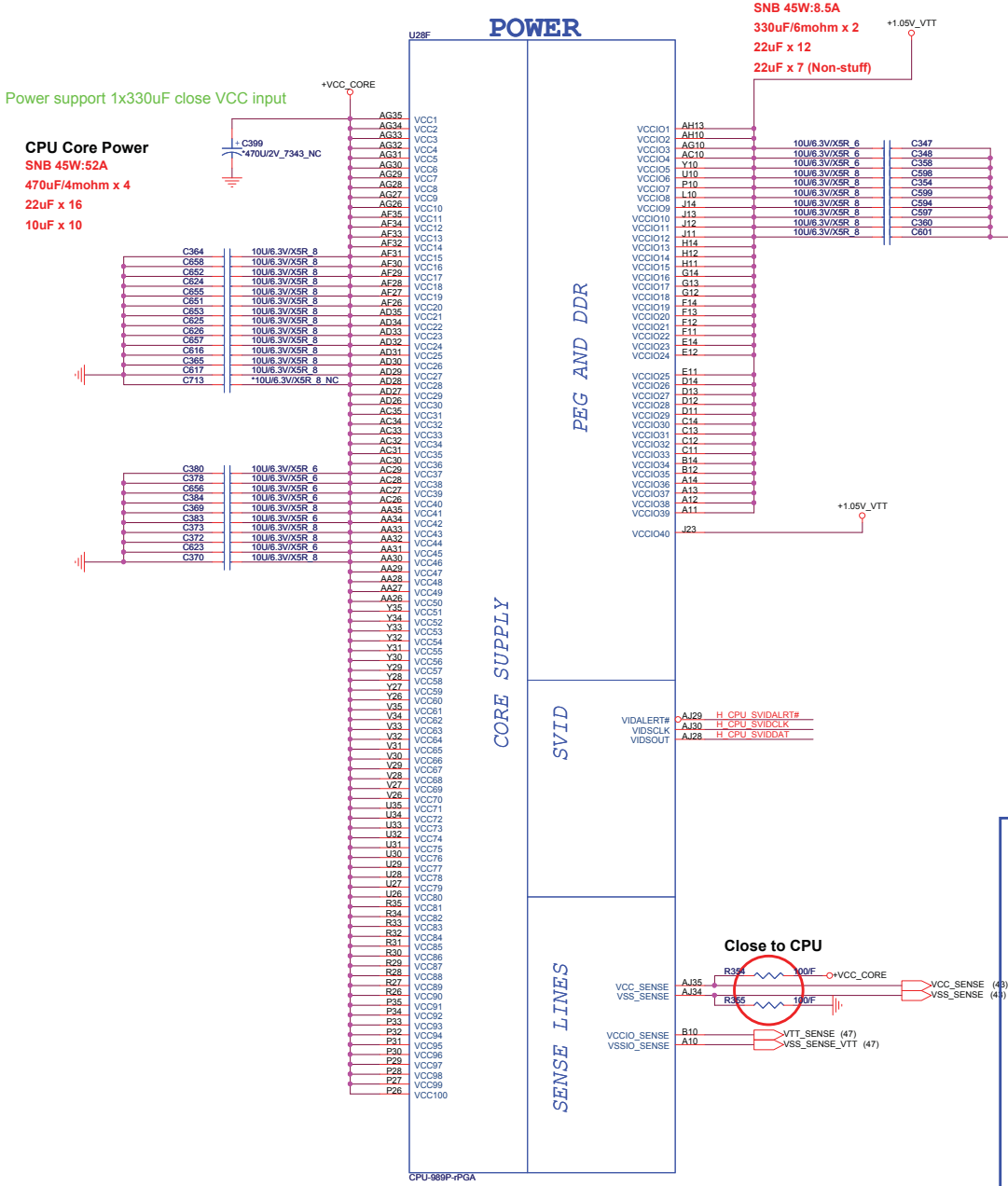
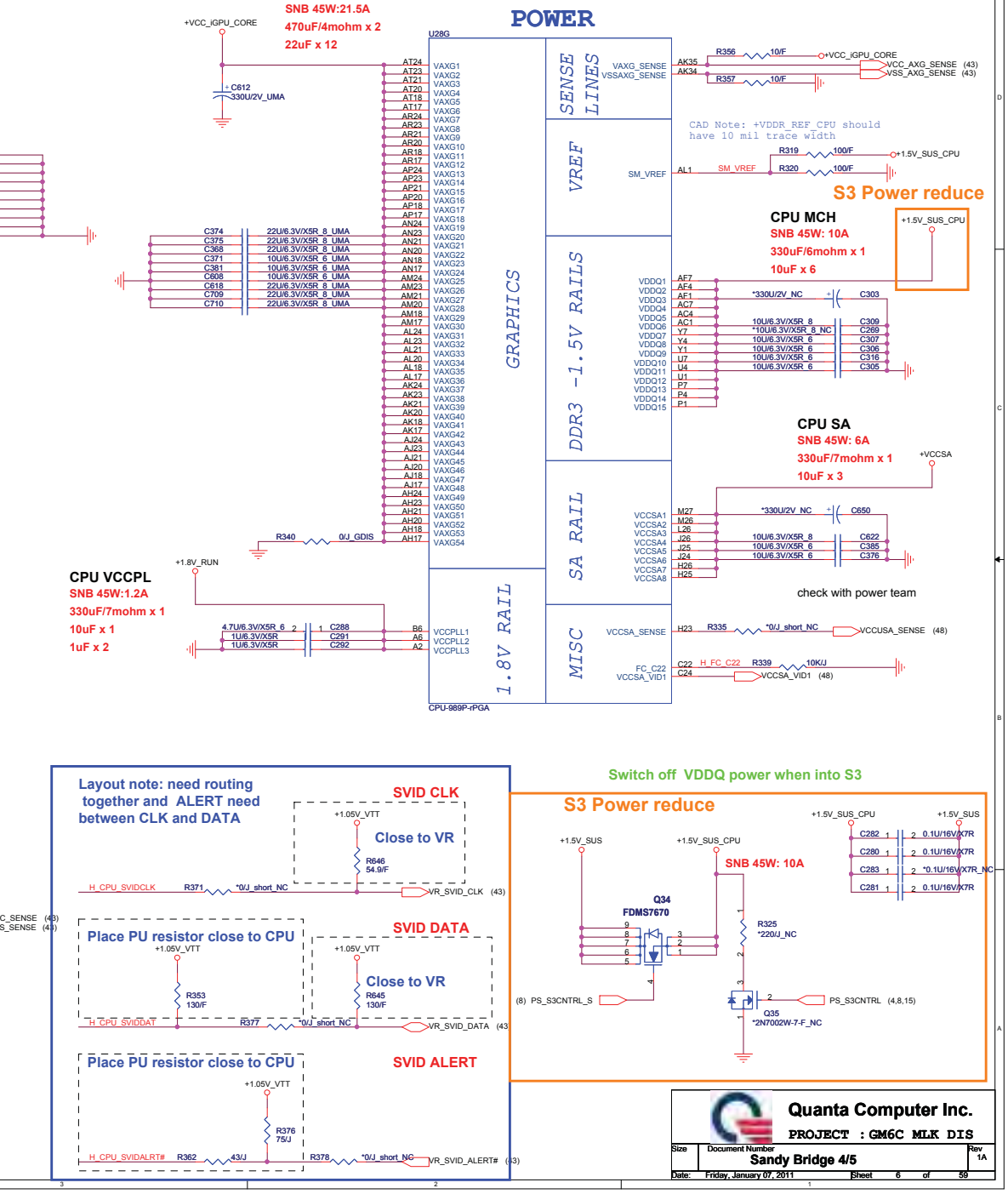
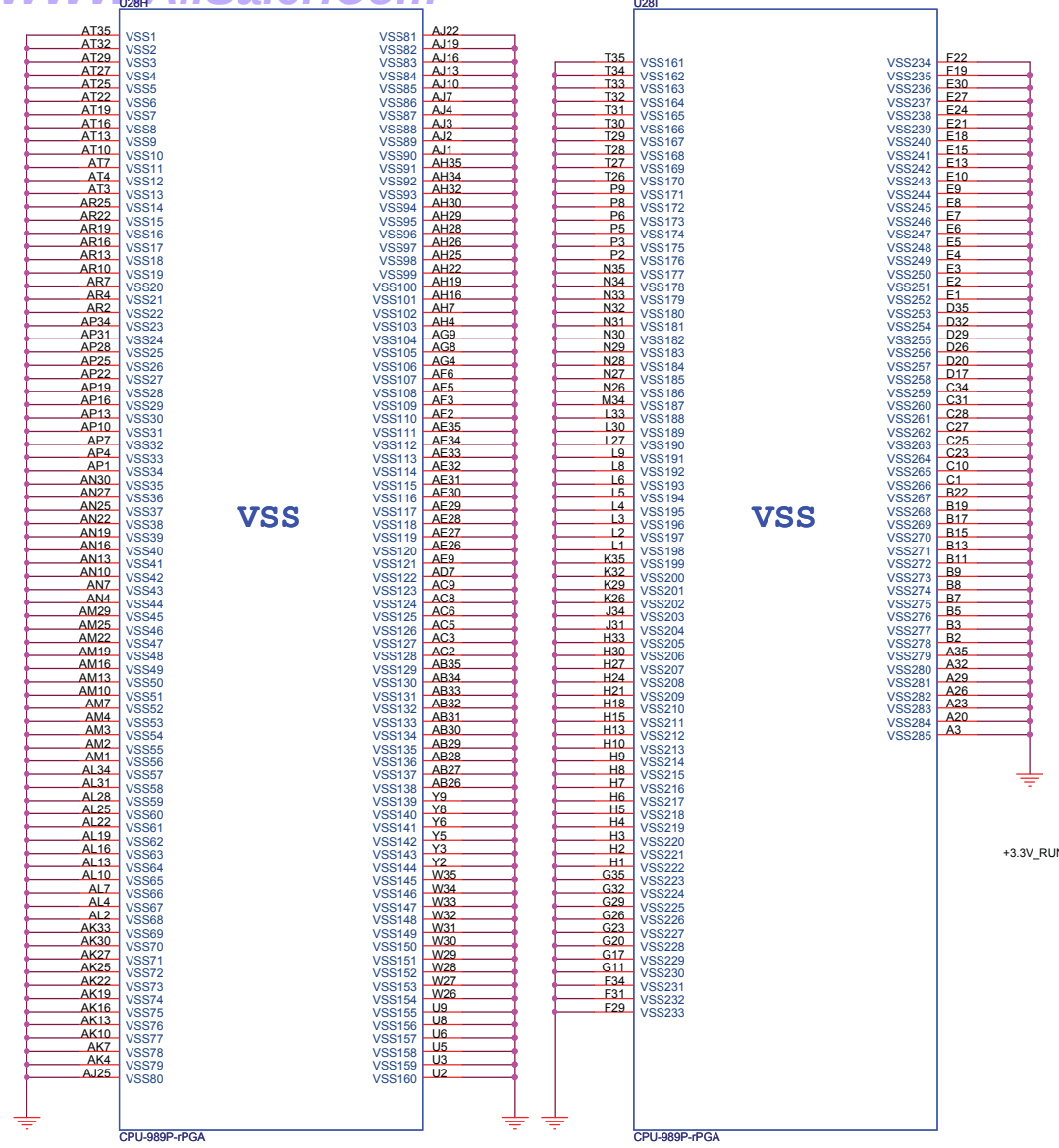
Sandy Bridge Processor (POWER)



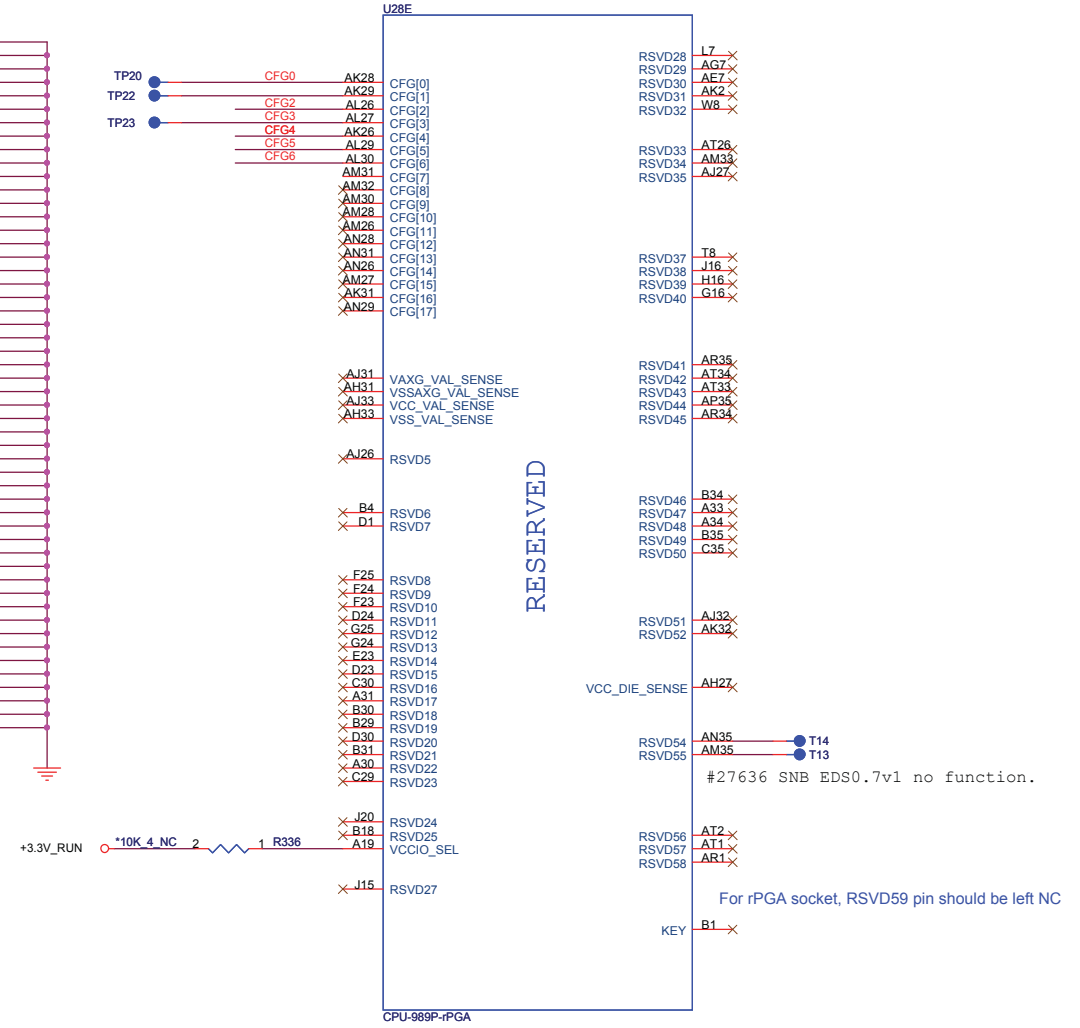
Sandy Bridge Processor (GRAPHIC POWER)



Sandy Bridge Processor (GND)



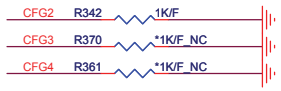
Sandy Bridge Processor (RESERVED, CFG)

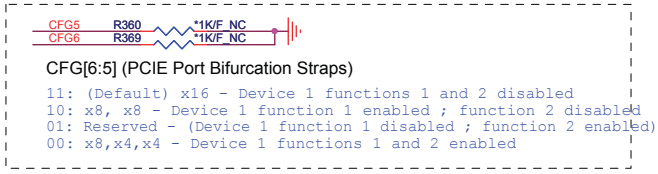


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Number Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	PCI-E Static x4 Lane Reversal	PEG wait for BIOS training
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP





Quanta Computer Inc.

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	Sandy Bridge 5/5	1A

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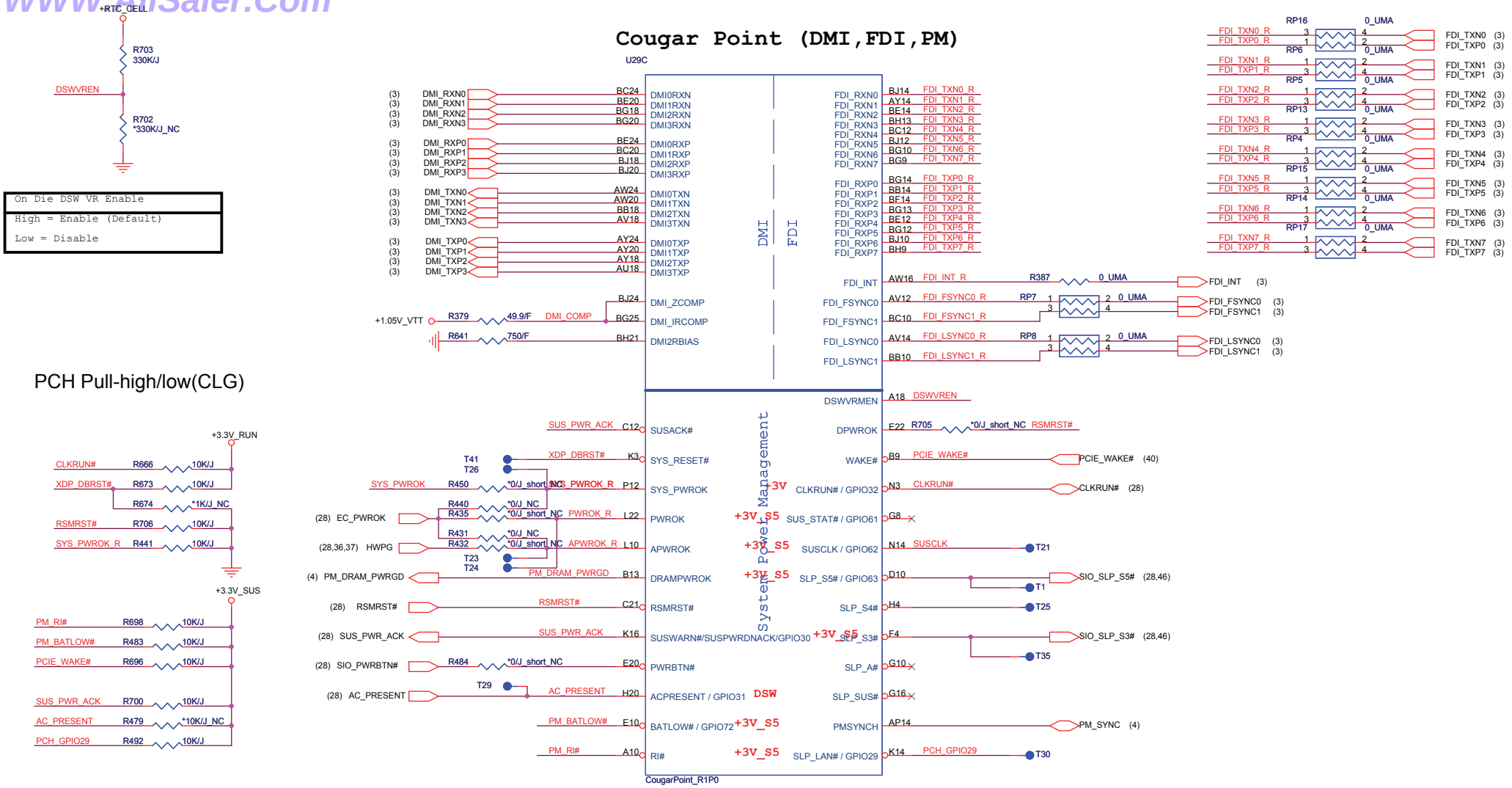
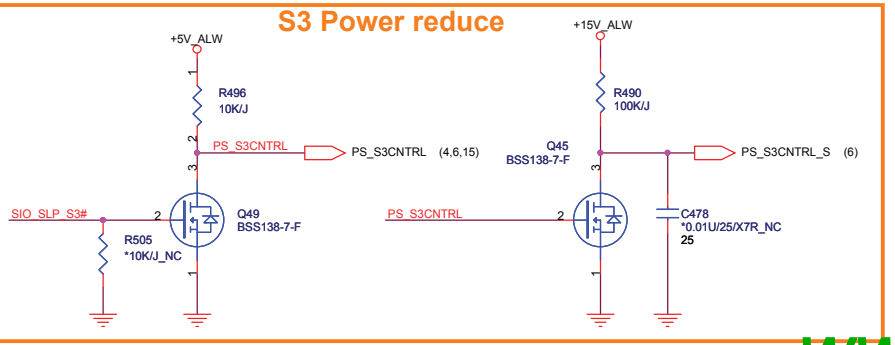
Cougar Point (DMI,FDI,PM)

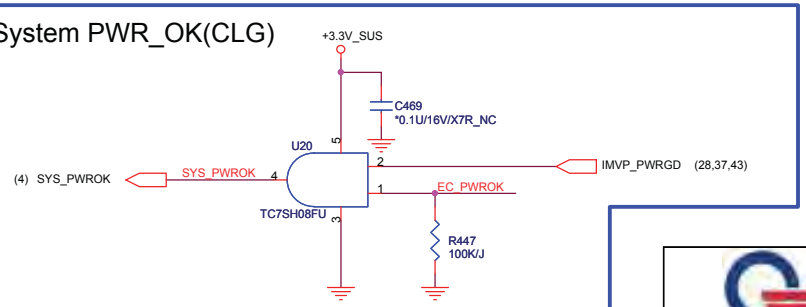


PCH Pull-high/low(CLG)

S3 Power reduce



System PWR_OK(CLG)



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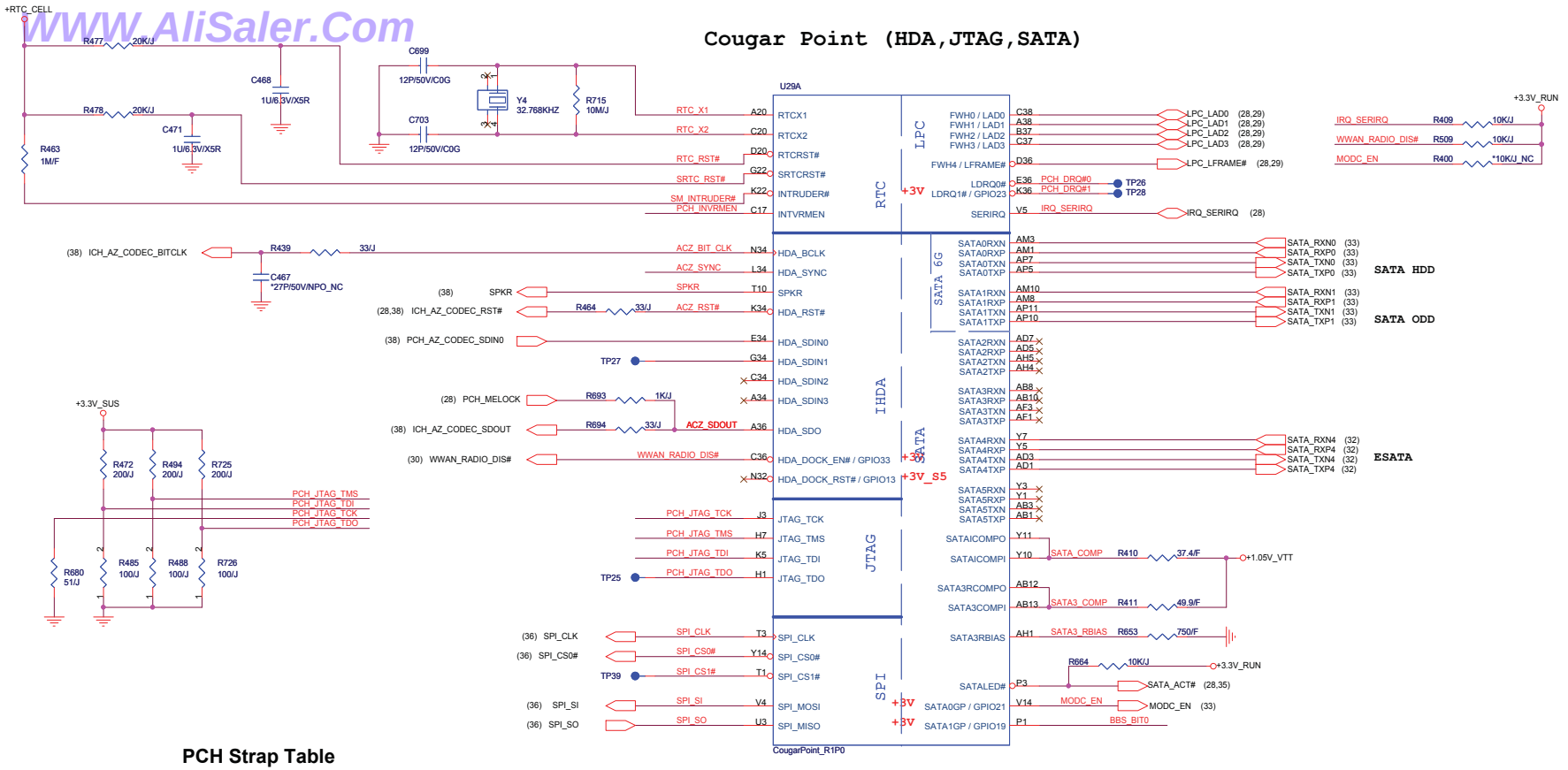
Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN R408 *1K/J_NC SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R454 *1K/J_NC PCI_GNT3# (11)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI * 0 / 0 / LPC	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]** R688 *1K/J_NC BBS_BIT1 (11) R665 *1K/J_NC BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS R469 *0/J_short_NC Q44 *2N7002W-7-F_NC R461 1K/J 33/J R470 (38) ICH_AZ_CODEC_SYNC ACZ_SYNC +5V_RUN
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	+3.3V_SUS R692 *1K/J_NC ACZ_SDOUT
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	+3.3V_SUS R418 R424 *1K/J_NC 10K/J PLL_ODVR_EN (12)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+RTC_CELL R704 330K/J PCH_INVRMEN
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm **0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**	+1.8V_RUN R382 2.2K/J DF_TVS (12)

Quanta Computer Inc.
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Cougar Point-M (PCI-E,SMBUS,CLK)

Note:Place TX DC blocking caps close to PCH.

U29B

Mini WWAN
(30) PCIE_RXN1 — BG34 PERN1
(30) PCIE_RXP1 — BJ34 PERP1
(30) PCIE_TXN1 — C402 0.1U/16V/X7R PCIE_TXN1_C — AV32 PETN1
(30) PCIE_TXP1 — C403 0.1U/16V/X7R PCIE_TXP1_C — AU32 PETP1

Mini WLAN
(29) PCIE_RXN2 — BE34 PERN2
(29) PCIE_RXP2 — BF34 PERP2
(29) PCIE_TXN2 — C400 0.1U/16V/X7R PCIE_TXN2_C — BB32 PETN2
(29) PCIE_TXP2 — C401 0.1U/16V/X7R PCIE_TXP2_C — AY32 PETP2

BG36 PERN3
BJ36 PERP3
AV34 PETN3
AU34 PETP3

USB 3.0
(40) PCIE_RXN4 — BF36 PERN4
(40) PCIE_RXP4 — BE36 PERP4
(40) PCIE_TXN4 — C405 0.1U/16V/X7R PCIE_TXN4_C — AY34 PETN4
(40) PCIE_TXP4 — C404 0.1U/16V/X7R PCIE_TXP4_C — BB34 PETP4

Card Reader
(27) PCIE_RXN5 — BG37 PERN5
(27) PCIE_RXP5 — BH37 PERP5
(27) PCIE_TXN5 — C407 0.1U/16V/X7R PCIE_TXN5_C — AY36 PETN5
(27) PCIE_TXP5 — C406 0.1U/16V/X7R PCIE_TXP5_C — BB36 PETP5

Giga Bit LOM
(31) PCIE_RXN6 — BJ38 PERN6
(31) PCIE_RXP6 — BG38 PERP6
(31) PCIE_TXN6 — C408 0.1U/16V/X7R PCIE_TXN6_C — AU36 PETN6
(31) PCIE_TXP6 — C409 0.1U/16V/X7R PCIE_TXP6_C — AV36 PETP6

BG40 PERN7
BJ40 PERP7
AY40 PETN7
BB40 PETP7

BE38 PERN8
BC38 PERP8
AW38 PETN8
AY38 PETP8

PCI-E*

+3V_S5

SMBUS
+3V_S5 SMBALERT# / GPIO11 — E12 RSV_SMBALERT#
SMBCLK — H14 PCH_SMBCLK — PCH_SMBCLK (29)
SMBDATA — C9 PCH_SMBDATA — PCH_SMBDATA (29)
+3V_S5 SML0ALERT# / GPIO60 — A12 — DDR_HVREF_RST_PCH (4)
SML0CLK — C8 SMB_CLK_ME0
SML0DATA — G12 SMB_DATA_ME0
SML1ALERT# / PCHHOT# / GPIO74 — C13 PCH_GPIO74
+3V_S5 SML1CLK / GPIO58 — E14 SMB_CLK_ME1
+3V_S5 SML1DATA / GPIO75 — M16 SMB_DATA_ME1

Controller Link
CL_CLK1 — M7
CL_DATA1 — T11
CL_RST1# — P10

CLOCKS
+3V_S5 PEG_A_CLKRQ# / GPIO47 — M10 PEG_CLKREQ# — PEG_CLKREQ# (17)
CLKOUT_PEG_A_N — AB37 — CLK_PCIE_VGAN (17)
CLKOUT_PEG_A_P — AB38 — CLK_PCIE_VGAP (17)
CLKOUT_DMI_N — AV22 — CLK_CPU_BCLKN (4)
CLKOUT_DMI_P — AU22 — CLK_CPU_BCLKP (4)
CLKOUT_DP_N — AM12 — CLK_DPLL_SSCLKN (4)
CLKOUT_DP_P — AM13 — CLK_DPLL_SSCLKP (4)
CLKIN_DMI_N — BF18 CLK_BUF_PCIE_3GPLLN — R381 10K/J
CLKIN_DMI_P — BE18 CLK_BUF_PCIE_3GPLLP — R383 10K/J
CLKIN_GND1_N — BJ30 CLK_BUF_BCLKN — R642 10K/J
CLKIN_GND1_P — BG30 CLK_BUF_BCLKP — R643 10K/J
CLKIN_DOT_96N — G24 CLK_BUF_DREFCLKN — R453 10K/J
CLKIN_DOT_96P — E24 CLK_BUF_DREFCLKP — R452 10K/J
CLKIN_SATA_N — AK7 CLK_BUF_DREFSSCLKN — R403 10K/J
CLKIN_SATA_P — AK5 CLK_BUF_DREFSSCLKP — R402 10K/J
REFCLK14IN — K45 CLK_PCH_14M — R434 10K/J
CLKIN_PCILOOPBACK — H45 CLK_PCI_FB — CLK_PCI_FB (11)
XTAL25_IN — V47 XTAL25_IN
XTAL25_OUT — V49 XTAL25_OUT
XCLK_RCOMP — Y47 XCLK_RCOMP — R661 90.9/F — +1.05V_VTT

Y40 CLKOUT_PCIE0N
Y39 CLKOUT_PCIE0P
CLK_PEG0_REQ# — J2 — PCIECLKRQ0# / GPIO73 — +3V_S5

Mini WLAN
(29) CLK_PCIE_MINI1N — AB49 CLKOUT_PCIE1N
(29) CLK_PCIE_MINI1P — AB47 CLKOUT_PCIE1P
(29) MINI1CLK_REQ# — MINI1CLK_REQ# — M1 — PCIECLKRQ1# / GPIO18 — +3V

Card Reader
(27) CLK_PCIE_CRN — AA48 CLKOUT_PCIE2N
(27) CLK_PCIE_CRP — AA47 CLKOUT_PCIE2P
Enable Free-Running (confirm with BIOS) 0628
CLK_PCIE_REQ2# — V10 — PCIECLKRQ2# / GPIO20 — +3V

Mini WWAN
(30) CLK_PCIE_MINI3N — Y37 CLKOUT_PCIE3N
(30) CLK_PCIE_MINI3P — Y36 CLKOUT_PCIE3P
(30) MINI2CLK_REQ# — MINI2CLK_REQ# — A8 — PCIECLKRQ3# / GPIO25 — +3V_S5

USB3.0
(40) CLK_PCIE_USB30N — Y43 CLKOUT_PCIE4N
(40) CLK_PCIE_USB30P — Y45 CLKOUT_PCIE4P
(40) CLK_PCIE_USB30_REQ# — CLK_PCIE_USB30_REQ# — L12 — PCIECLKRQ4# / GPIO26 — +3V_S5

Giga Bit LOM
(31) CLK_PCIE_LOMN — V45 CLKOUT_PCIE5N
(31) CLK_PCIE_LOMP — V46 CLKOUT_PCIE5P
(31) LOM_CLK_REQ# — LOM_CLK_REQ# — L14 — PCIECLKRQ5# / GPIO44 — +3V_S5

AB42 CLKOUT_PEG_B_N
AB40 CLKOUT_PEG_B_P
PEG_B_CLKRQ# — E6 — PEG_B_CLKRQ# / GPIO56 — +3V_S5

T18 CLK_PCH_SRC6N — V40 CLKOUT_PCIE6N
T19 CLK_PCH_SRC6P — V42 CLKOUT_PCIE6P
CLK_PCIE_REQ6# — T13 — PCIECLKRQ6# / GPIO45 — +3V_S5

V38 CLKOUT_PCIE7N
V37 CLKOUT_PCIE7P
CLK_PCIE_REQ7# — K12 — PCIECLKRQ7# / GPIO46 — +3V_S5

T16 CLK_PCIE_XDPN — AK14 CLKOUT_ITPXDP_N
T15 CLK_PCIE_XDPP — AK13 CLKOUT_ITPXDP_P

FLEX CLOCKS
+3V CLKOUTFLEX0 / GPIO64 — K43 HDMI_PWR_CTRL — HDMI_PWR_CTRL (25)
+3V CLKOUTFLEX1 / GPIO65 — F47 CLK_VGA_27M_R — R684 22/J_GDIS — CLK_VGA_27M (19)
+3V CLKOUTFLEX2 / GPIO66 — H47 TEST_WOOFER_EN — TEST_WOOFER_EN (39)
+3V CLKOUTFLEX3 / GPIO67 — K49 CLK_VGA_27M_SS_R — R442 *22/J_NC — CLK_VGA_27M_SS (19)

CougarPoint_R1P0

+3.3V_SUS
PCH_SMBCLK 2.2K/F R482
PCH_SMBDATA 2.2K/F R697
SMB_CLK_ME0 2.2K/F R713
SMB_DATA_ME0 2.2K/F R476
SMB_CLK_ME1 2.2K/F R462
SMB_DATA_ME1 2.2K/F R457
RSV_SMBALERT# 10K/F R471
PCH_GPIO74 10K/F R712

WLAN, WWAN, DIMM0, DIMM1, 3-axis fall sensor

+3.3V_SUS
Q43 2N7002W-7-F
SMB_CLK_ME1 — SMBCLK1 (28)
+3.3V_SUS
Q42 2N7002W-7-F
SMB_DATA_ME1 — SMBDAT1 (28)

EC

PCIE Clock Request

+3.3V_SUS
R695 10K/J MINI2CLK_REQ#
R685 10K/J CLK_PEG0_REQ#
R481 10K/J LOM_CLK_REQ#
R475 10K/J PEG_B_CLKRQ#
R473 10K/J PEG_CLKREQ#
R451 10K/J CLK_PCIE_REQ6#
R467 10K/J CLK_PCIE_USB30_REQ#
R480 10K/J CLK_PCIE_REQ7#

+3.3V_RUN
R436 10K/J HDMI_PWR_CTRL
R667 10K/J MINI1CLK_REQ#
R405 10K/J CLK_PCIE_REQ2#

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

Change as big package (UM9)

25MHz Clock for DCI Function

XTAL25_IN
R662 1M/J
Y3 25MHz
XTAL25_OUT
C683 22P/50V/NPO
C685 22P/50V/NPO

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Cougar Point 3/7	1A
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Cougar Point (LVDS,DDI)

U29D

LVDS_IBG to other single 20 mils

Digital Display Interface

CougarPoint_R1P0

Cougar Point-M (PCI,USB,NVRAM)

U29E

RSVD

PCI

USB

CougarPoint_R1P0

TBC if there's OC issue 0629 (It's OK, DP has redriver IC)

PUSB/ESATA

Mini Card (WLAN)

Mini Card (WWAN)

BlueTooth

Camera

Touch Screen Module

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

change to R01 schematic

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Cougar Point 4/7	1A
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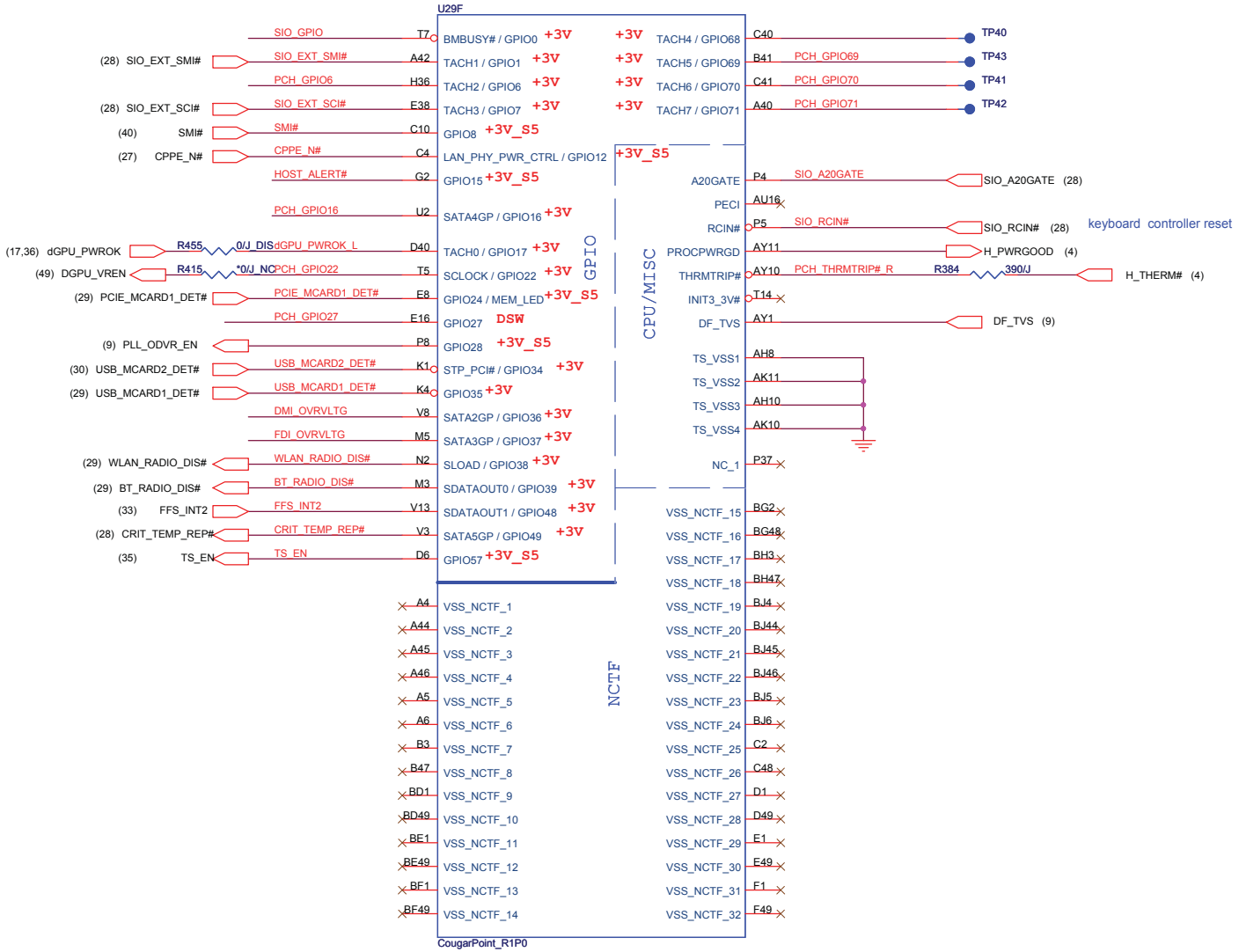
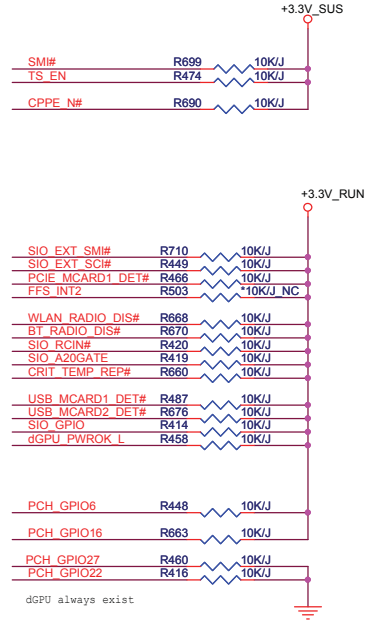
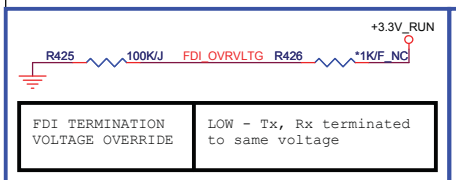
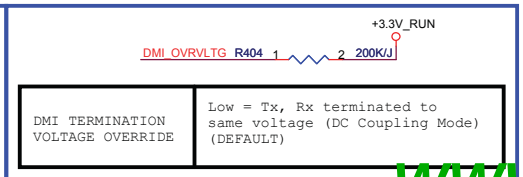
Cougar Point (GPIO,VSS_NCTF,RSVD)

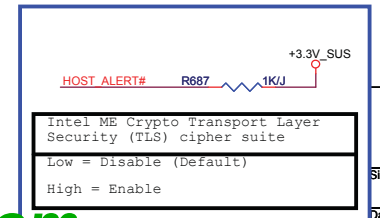








internal PD resistor 20K-ohm
To avoid voltage be divided,
please change GPIO36 PU resistor from
10K-ohm to 200K-ohm. (07/12)



Quanta Computer Inc.
PROJECT : GM6C MLK DIS

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	Cougar Point 5/7	1A
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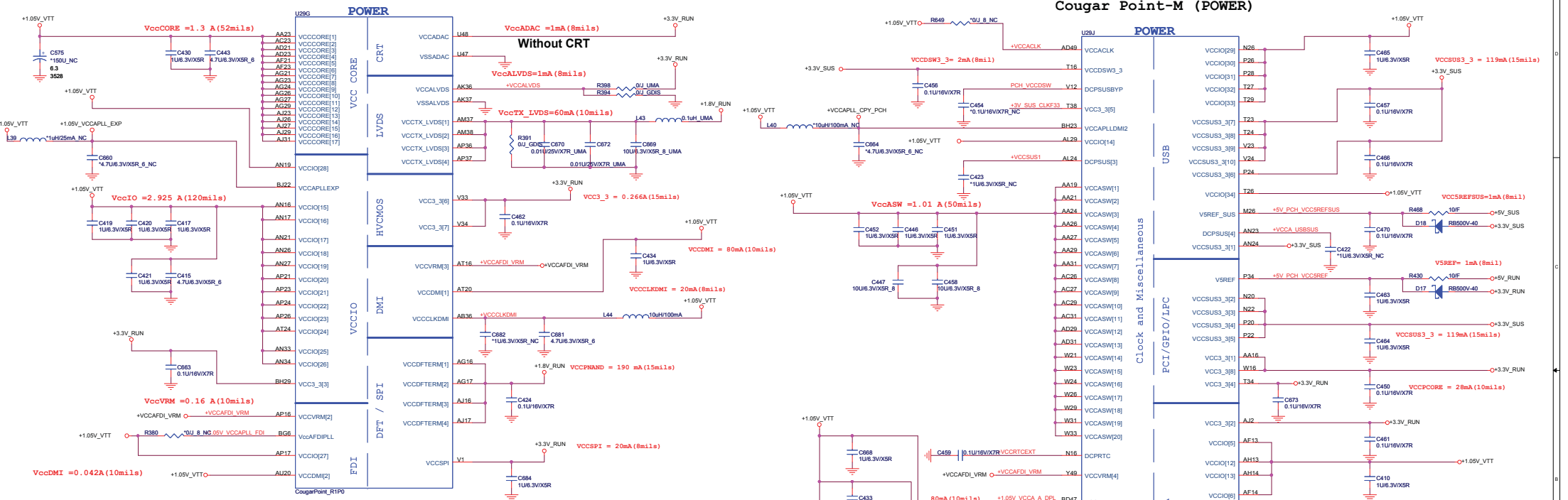
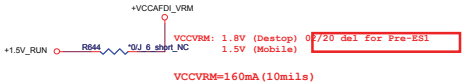
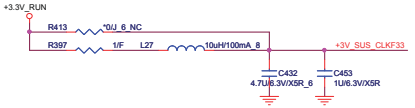
COUGAR POINT (POWER)







Cougar Point-M (POWER)

Quanta Computer Inc.	
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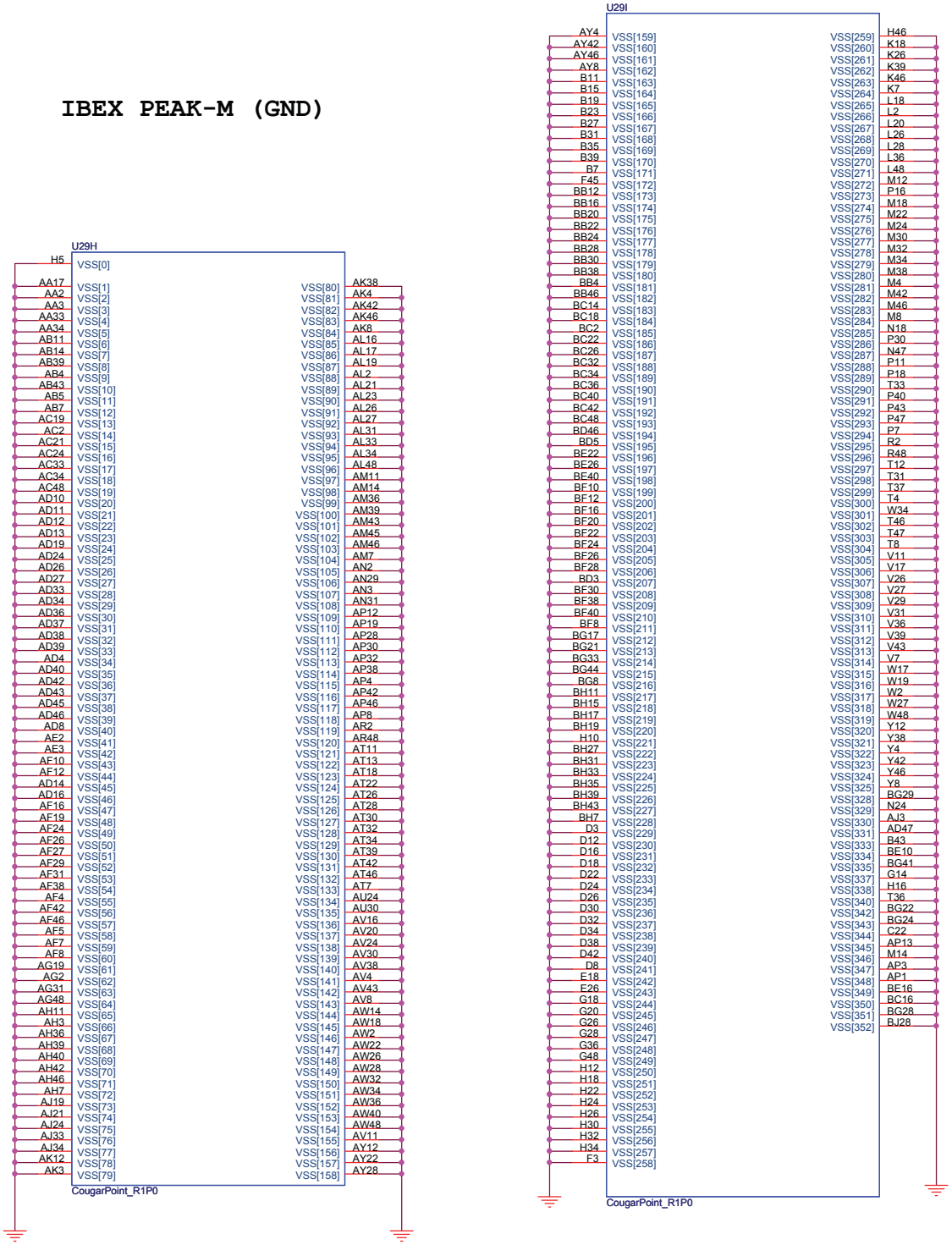
PCH6(CLG)

IBEX PEAK-M (GND)



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
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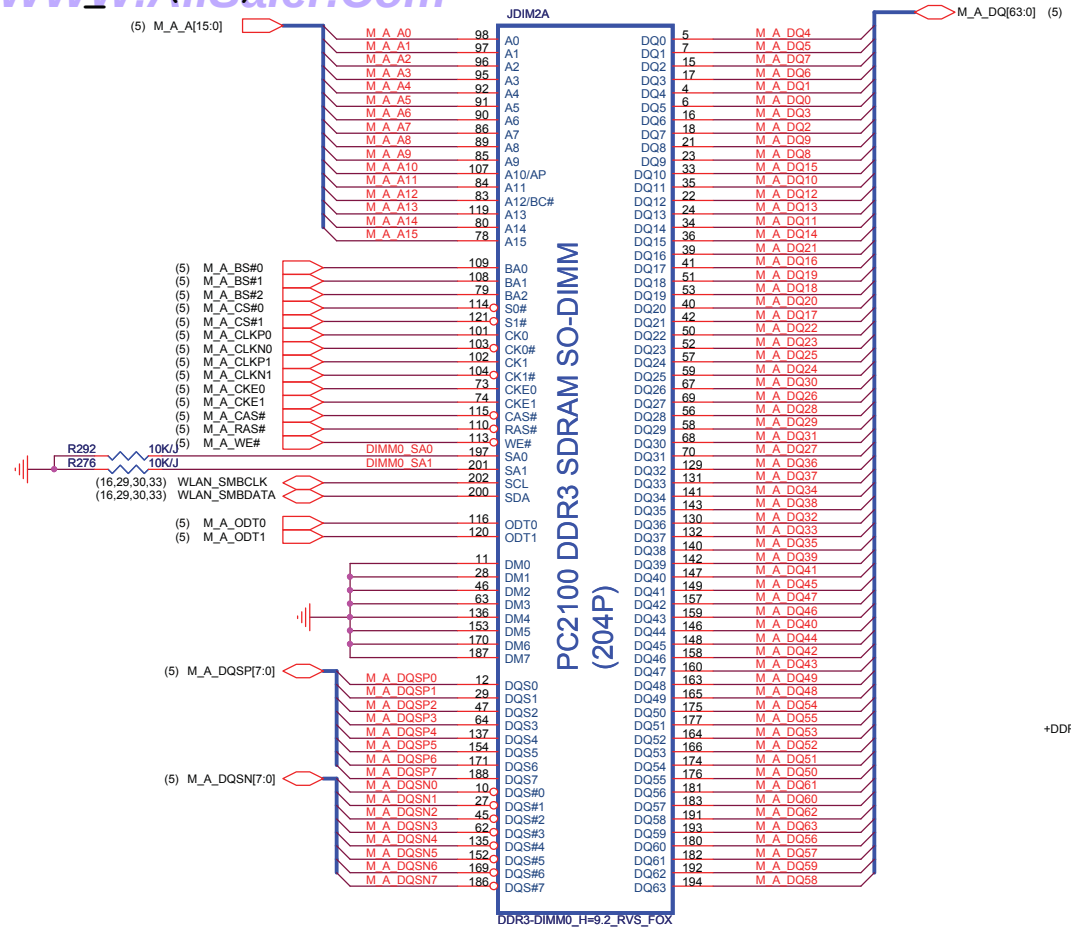
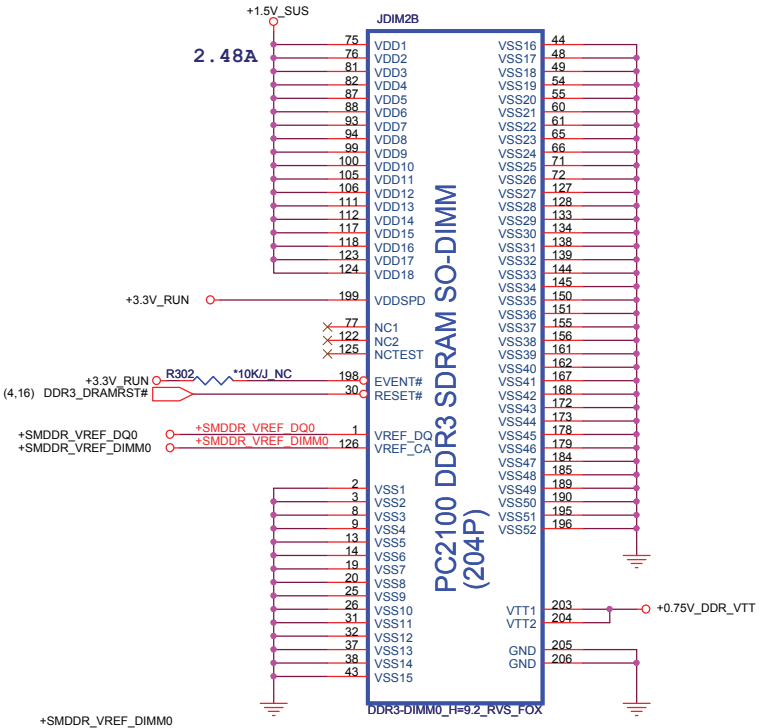
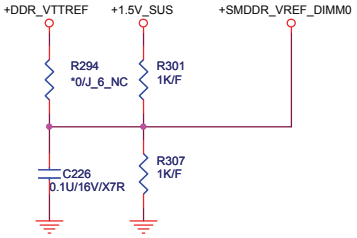
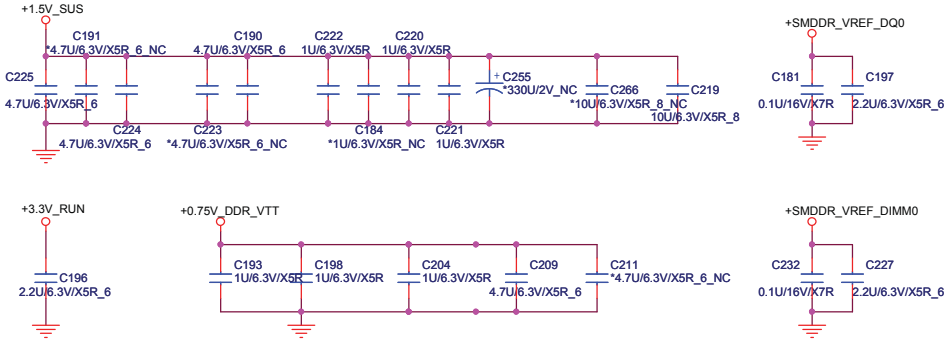
DDR_STD(DDR)



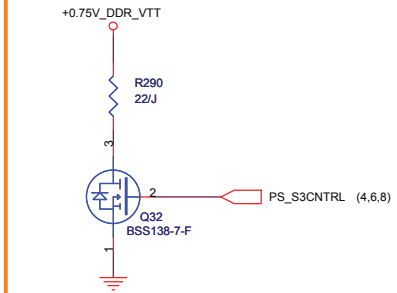




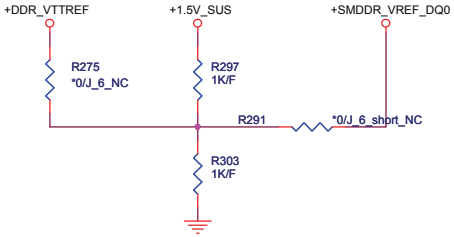
Place these Caps near So-Dimm0.



S3 Power reduce



M1 VREF Solution



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
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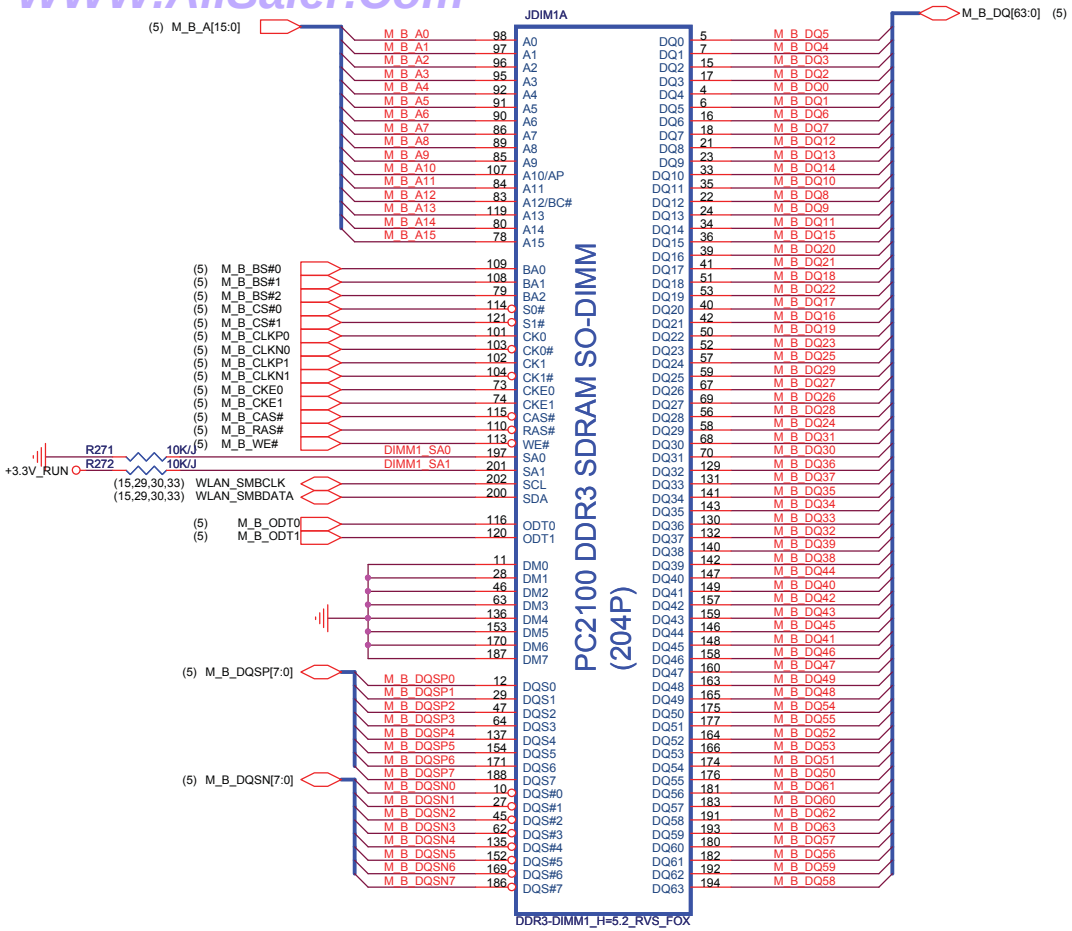

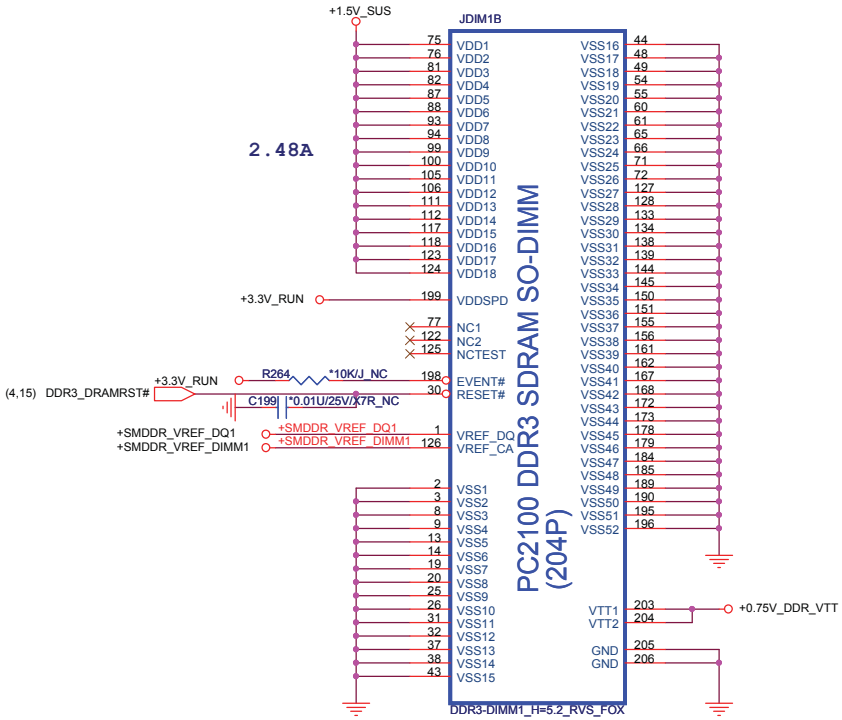

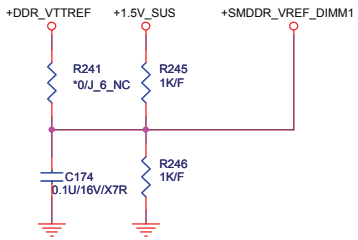

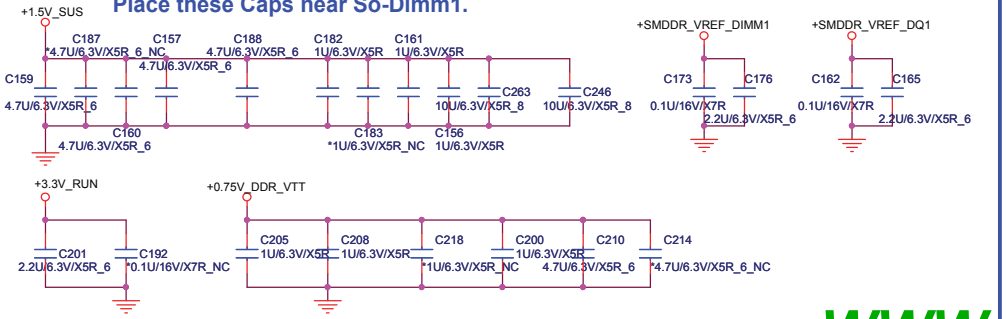

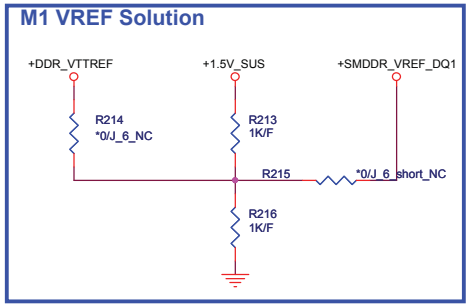

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A

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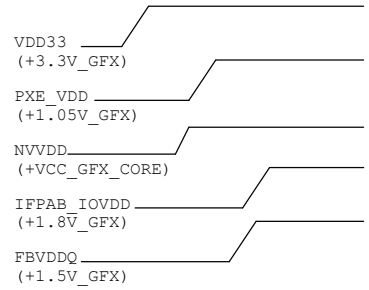
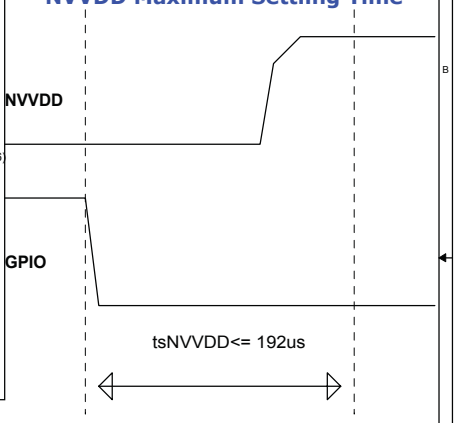
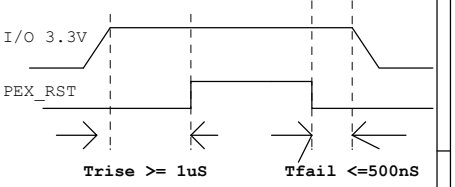
power up sequence

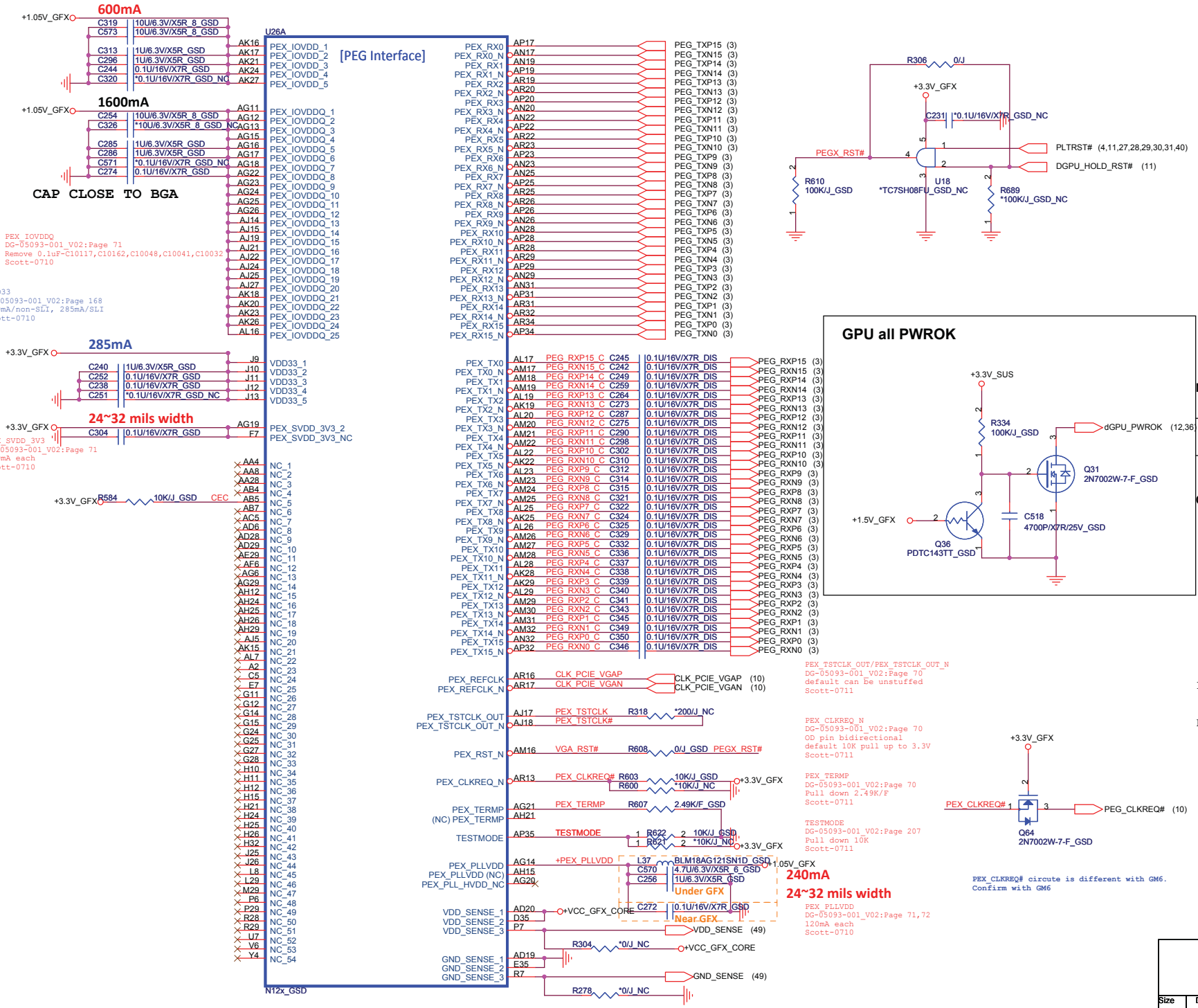


NVVDD Maximum Settling Time



PEX_RST timing





Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: DGPU 1/5 (PEG)	Rev: 1A
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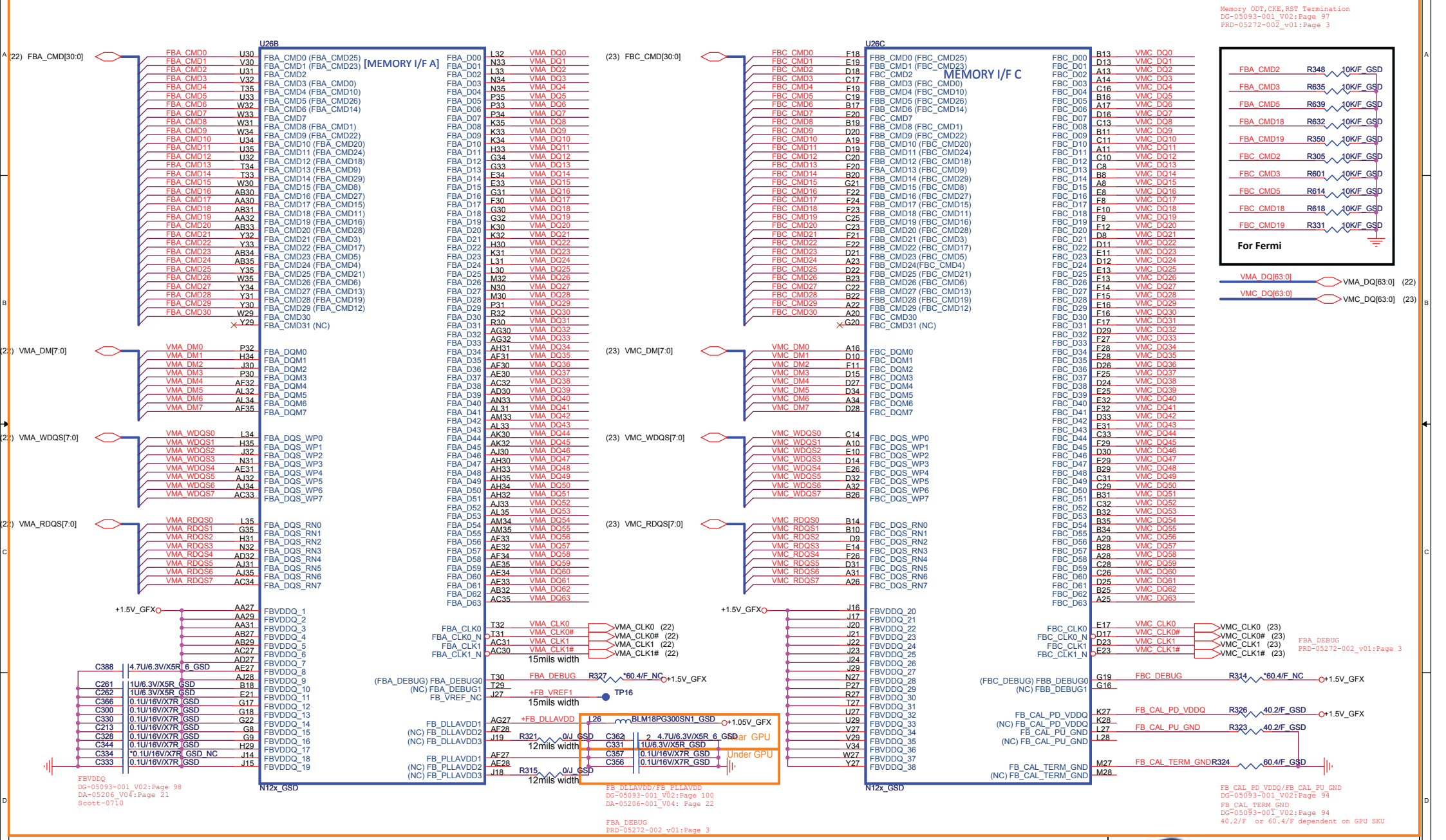

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 2/5 (Memory)	1A

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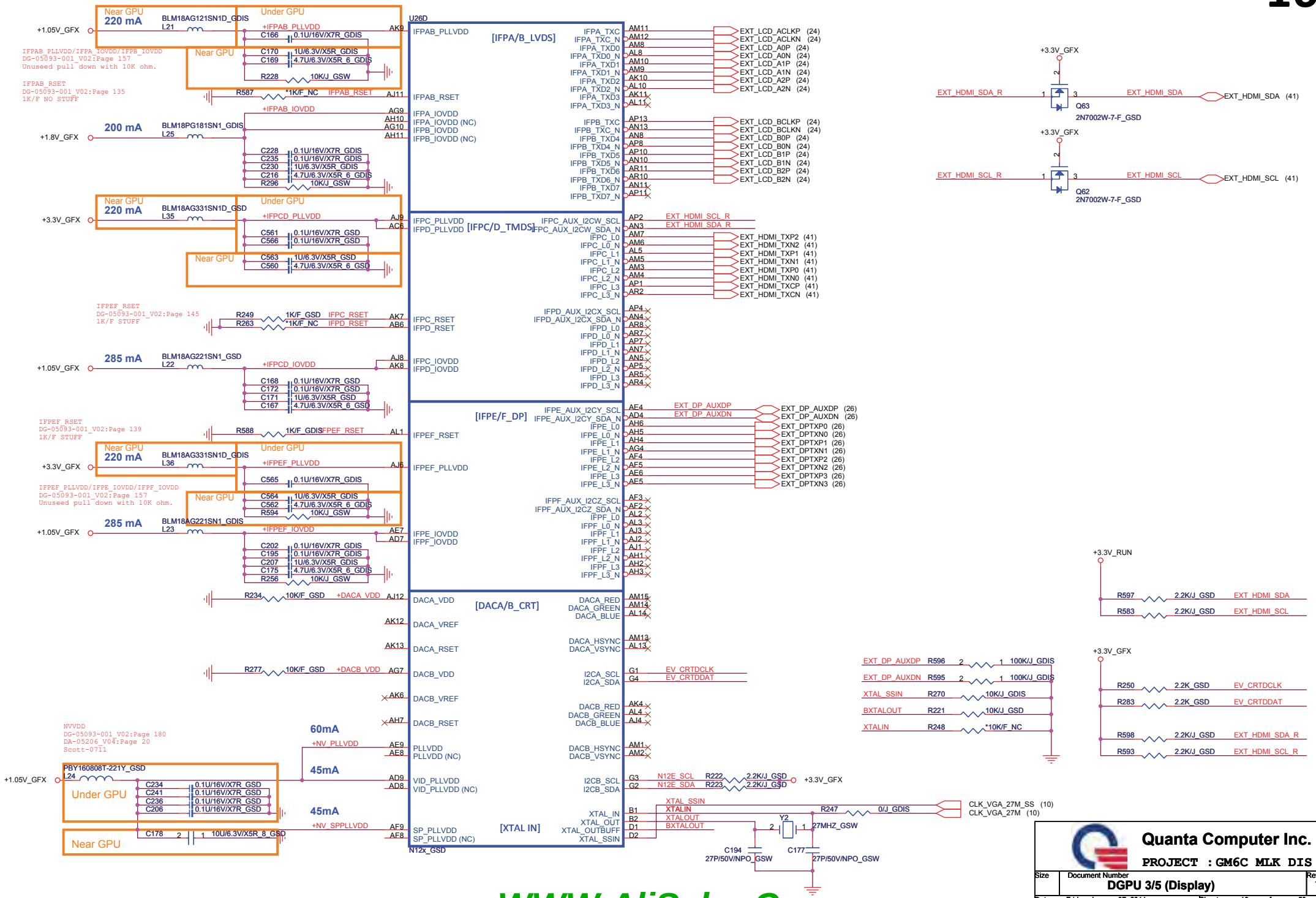

Quanta Computer Inc.	
PROJECT : GM6C MLK DIS	
Size	Document Number: DGPU 3/5 (Display) — Rev: 1A
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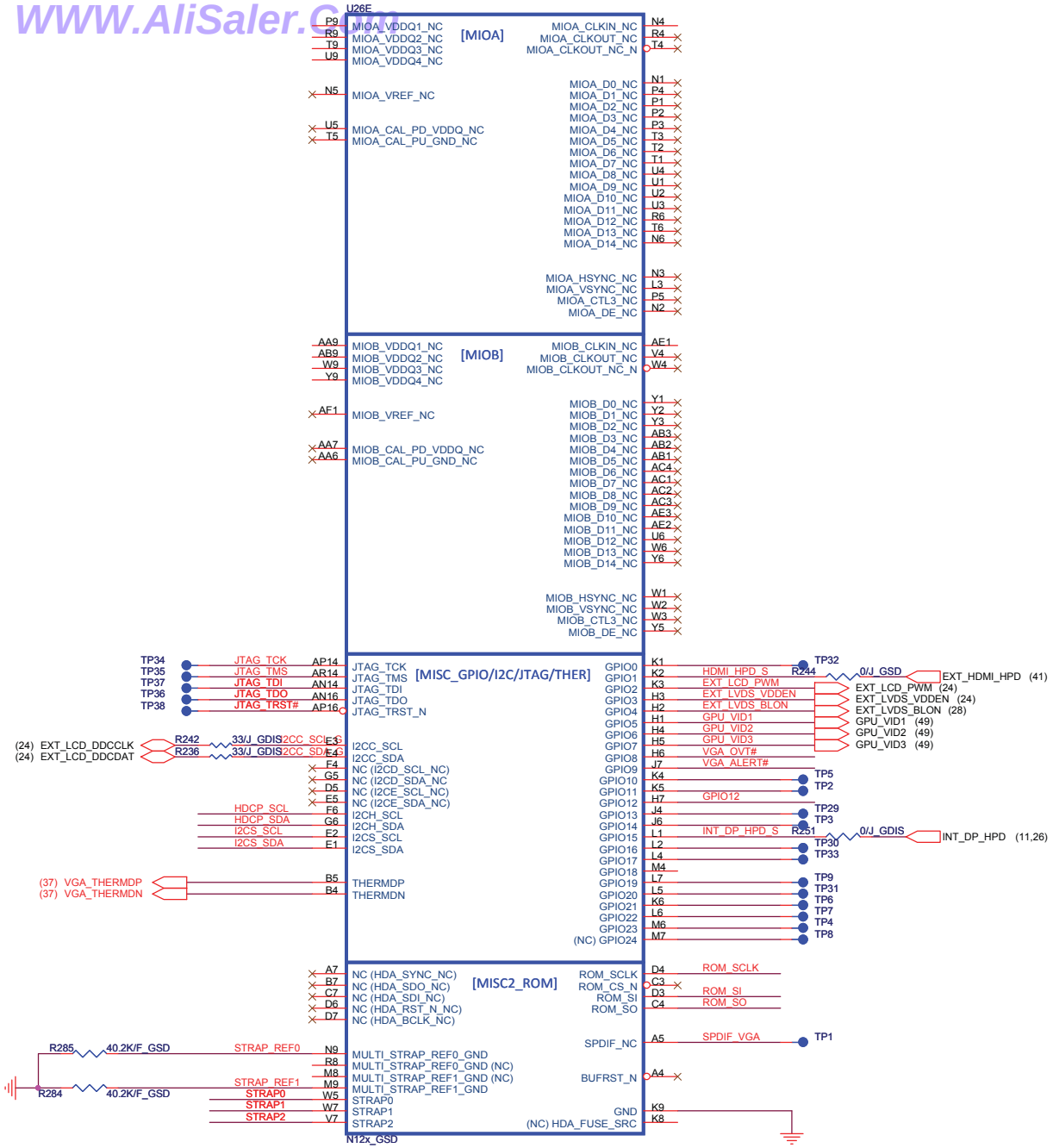


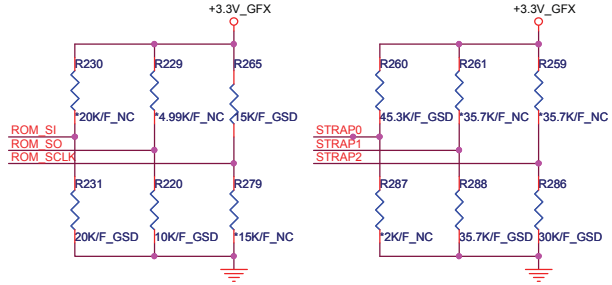
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C
0x6(0110)	900MHz 1GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 1GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

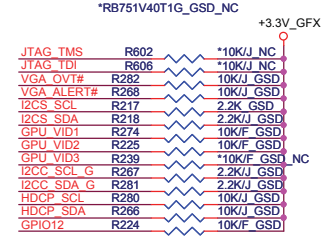
ROM_SI Strap Bit for RAM Mapping

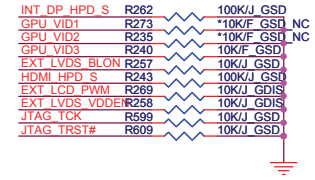
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



STRAP2 ROM_SCLK

N12P-GE (AJ0N12P0T02)	PD 30K	PU 15K	0xDF5	
N12P-GT (AJ0N12P0T03)	PD 35K	PU 15K	0xDF6	
N12P-GS (AJ0N12P0T04)	PD 25K	PU 15K	0xDF4	





GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI Raster Sync
12	IN	N/A	AC PWR Detect Input
13	OUT	N/A	Power Supply Control
14	OUT	N/A	Power Supply Control
15	OUT	N/A	Hot plug detect for IFP link E
16	OUT	N/A	Programmable Fan Control
17	OUT	N/A	Reserved
19	OUT	N/A	Reserved
20	OUT	N/A	Hot plug detect for IFP link D
21	OUT	N/A	Reserved
22	OUT	N/A	Hot plug detect for IFP link F
23	OUT	N/A	SLI Swap Ready single
23	OUT	N/A	

Quanta Computer Inc.
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	DGPU 4/5 (MIO/GPIO)	1A

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31.56A

+VCC_GFX_CORE

U26F

[GPU VDD]

AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T16
AC24	VDD_022	VDD_078	T18
AC25	VDD_023	VDD_079	T20
AD12	VDD_024	VDD_080	T22
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V17
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

N12x_GSD

+VCC_GFX_CORE

U26G

[GPU GND]

AA2	GND_1	GND_97	E9
AA5	GND_2	GND_98	E12
AA11	GND_3	GND_99	E15
AA12	GND_4	GND_100	E18
AA13	GND_5	GND_101	E24
AA14	GND_6	GND_102	E27
AA15	GND_7	GND_103	E30
AA16	GND_8	GND_104	F2
AA17	GND_9	GND_105	F5
AA18	GND_10	GND_106	F31
AA19	GND_11	GND_107	F34
AA20	GND_12	GND_108	J2
AA21	GND_13	GND_109	J5
AA22	GND_14	GND_110	J31
AA23	GND_15	GND_111	J34
AA24	GND_16	GND_112	L9
AA25	GND_17	GND_113	M2
AA34	GND_18	GND_114	M5
AB12	GND_19	GND_115	M11
AB14	GND_20	GND_116	M13
AB16	GND_21	GND_117	M15
AB18	GND_22	GND_118	M17
AB20	GND_23	GND_119	M19
AB22	GND_24	GND_120	M21
AB24	GND_25	GND_121	M23
AC9	GND_26	GND_122	M25
AD11	GND_27	GND_123	M31
AD13	GND_28	GND_124	M34
AD15	GND_29	GND_125	N11
AD17	GND_30	GND_126	N12
AD2	GND_31	GND_127	N13
AD5	GND_32	GND_128	N14
AD21	GND_33	GND_129	N15
AD23	GND_34	GND_130	N16
AD25	GND_35	GND_131	N17
AD31	GND_36	GND_132	N18
AD34	GND_37	GND_133	N19
AE11	GND_38	GND_134	N20
AE12	GND_39	GND_135	N21
AE13	GND_40	GND_136	N22
AE14	GND_41	GND_137	N23
AE15	GND_42	GND_138	N24
AE16	GND_43	GND_139	N25
AE17	GND_44	GND_140	P12
AE18	GND_45	GND_141	P14
AE19	GND_46	GND_142	P16
AE20	GND_47	GND_143	P18
AE21	GND_48	GND_144	P20
AE22	GND_49	GND_145	P22
AE23	GND_50	GND_146	P24
AE24	GND_51	GND_147	R2
AE25	GND_52	GND_148	R5
AG2	GND_53	GND_149	R31
AG31	GND_54	GND_150	R34
AG34	GND_55	GND_151	T11
AK2	GND_56	GND_152	T13
AK5	GND_57	GND_153	T15
AK31	GND_58	GND_154	T17
AK34	GND_59	GND_155	T19
AK5	GND_60	GND_156	T21
AK14	GND_61	GND_157	T23
AL6	GND_62	GND_158	T25
AL9	GND_63	GND_159	U11
AL12	GND_64	GND_160	U12
AL15	GND_65	GND_161	U13
AL18	GND_66	GND_162	U14
AL21	GND_67	GND_163	U15
AL24	GND_68	GND_164	U16
AL27	GND_69	GND_165	U17
AL30	GND_70	GND_166	U18
AN2	GND_71	GND_167	U19
AN34	GND_72	GND_168	U20
AP3	GND_73	GND_169	U21
AP6	GND_74	GND_170	U22
AP9	GND_75	GND_171	U23
AP12	GND_76	GND_172	U24
AP15	GND_77	GND_173	U25
AP18	GND_78	GND_174	V2
AP21	GND_79	GND_175	V5
AP24	GND_80	GND_176	V9
AP27	GND_81	GND_177	V12
AP30	GND_82	GND_178	V14
AP33	GND_83	GND_179	V16
B3	GND_84	GND_180	V18
B6	GND_85	GND_181	V20
B9	GND_86	GND_182	V22
B12	GND_87	GND_183	V24
B15	GND_88	GND_184	V31
B21	GND_89	GND_185	Y11
B24	GND_90	GND_186	Y13
B27	GND_91	GND_187	Y15
B30	GND_92	GND_188	Y17
B33	GND_93	GND_189	Y19
C2	GND_94	GND_190	Y21
C34	GND_95	GND_191	Y23
E6	GND_96	GND_192	Y25

N12x_GSD

PLACE UNDER BALLS

+VCC_GFX_CORE

NVVDD
DA-05206_V04:Page 20
Scott-0710

C250	0.01U/25V/X7R_GSD
C247	0.01U/25V/X7R_GSD
C243	0.01U/25V/X7R_GSD
C265	*0.01U/25V/X7R_GSD_NC
C284	0.01U/25V/X7R_GSD
C311	0.01U/25V/X7R_GSD
C289	*0.01U/25V/X7R_GSD_NC
C257	*0.01U/25V/X7R_GSD_NC
C253	0.022U/16V/X7R_GSD
C277	0.022U/16V/X7R_GSD
C267	0.022U/16V/X7R_GSD
C248	0.047U/10V/X7R_GSD
C271	0.047U/10V/X7R_GSD
C239	0.047U/10V/X7R_GSD
C301	0.1U/16V/X7R_GSD
C299	0.1U/16V/X7R_GSD
C258	0.22U/6.3V/X5R_GSD
C295	0.22U/6.3V/X5R_GSD
C297	0.22U/6.3V/X5R_GSD
C276	1U/6.3V/X5R_GSD

PLACE NEAR BALLS

+VCC_GFX_CORE

C294	4.7U/6.3V/X5R_6_GSD
C711	22U/6.3V/X5R_8_GSD
C712	22U/6.3V/X5R_8_GSD
C270	22U/6.3V/X5R_8_GSD
C308	22U/6.3V/X5R_8_GSD
C317	22U/6.3V/X5R_8_GSD
C318	22U/6.3V/X5R_8_GSD

Quanta Computer Inc.

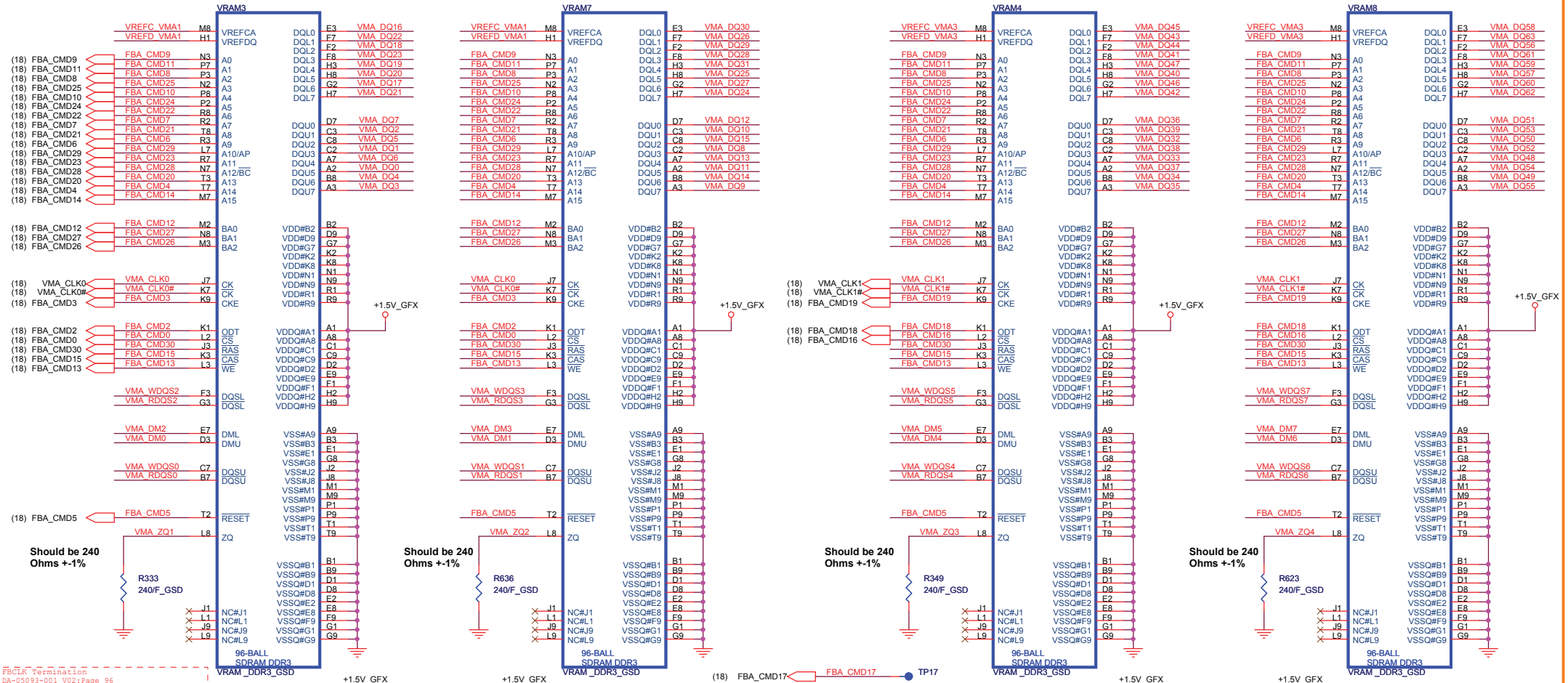
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	1A

Date: Friday, January 07, 2011 Sheet 21 of 59

CHANNEL A: 256MB/512MB DDR3

(18) VMA_DQ[63..0]
(18) VMA_DM[7..0]
(18) VMA_WDQS[7..0]
(18) VMA_RDQS[7..0]



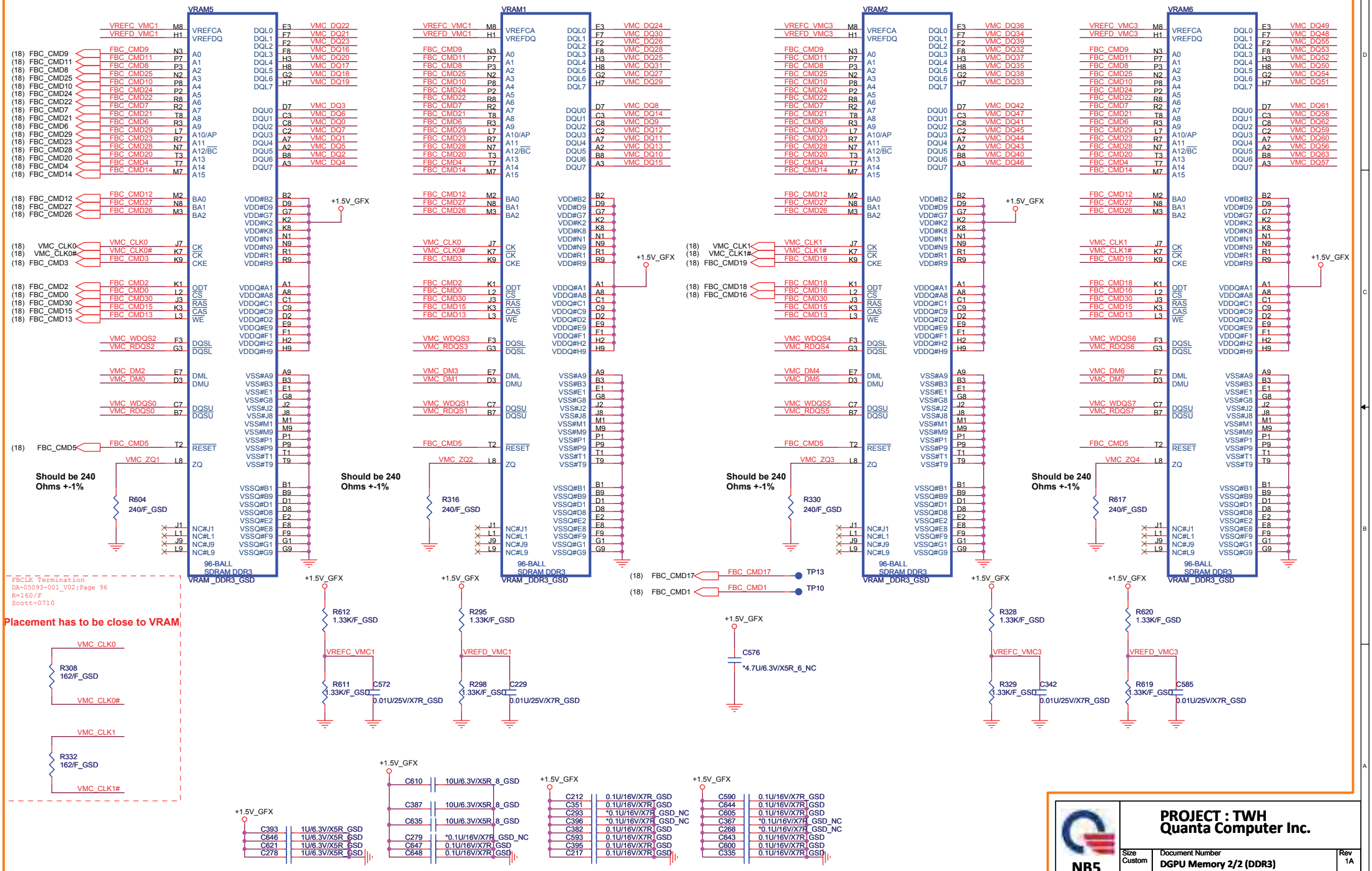
NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory 1/2 (DDR3)	1A
Date: Friday, January 07, 2011	Sheet 22 of 59	

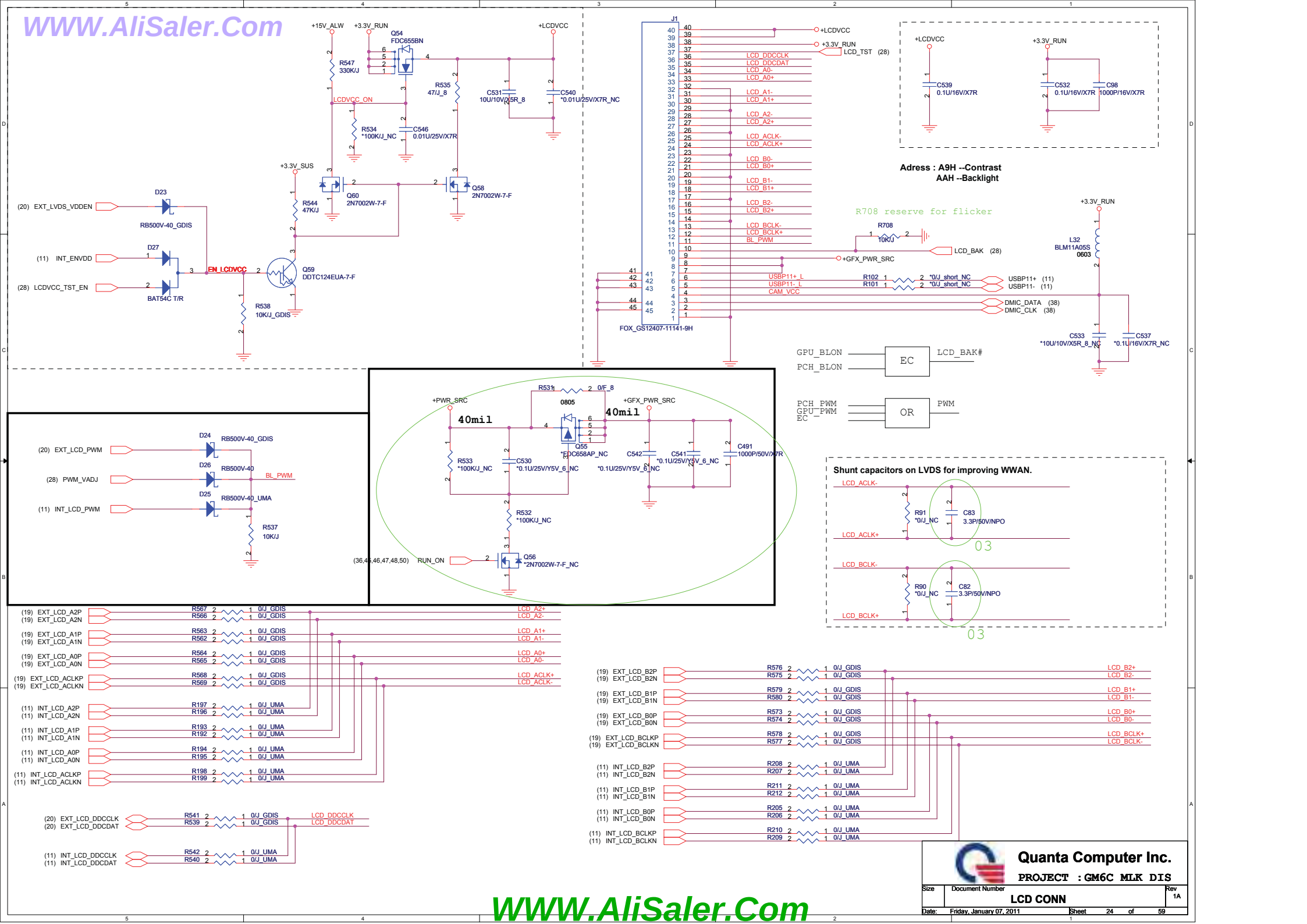
CHANNEL B: 256MB/512MB DDR3

(18) VMC_DQ[63..0]
(18) VMC_DM[7..0]
(18) VMC_WDQS[7..0]
(18) VMC_RDQS[7..0]



PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory 2/2 (DDR3)	1A
NB5	Date: Friday, January 07, 2011	Sheet 23 of 59



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	LCD CONN	1A
Date: Friday, January 07, 2011	Sheet 24 of 59	

HDMI

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V

+3.3V_RUN
L9 *BLM18PG181SN1_NC
+VCC_HDMI
C46 *1U/6.3V/X5R_NC
C78 *0.1U/16V/X7R_NC
C63 *0.1U/16V/X7R_NC

U5
POWER: VCC x8
GND: GND x16, EPAD
CONTROL: DDC_EN, PC0, PC1, DDCBUF_EN, CFG, RT_EN#, OE#, REXT
*SN75DP139RGZR_NC

(41) HDMI_TXCP_L / HDMI_TXCN_L — C51 / C49 0.1U/16V/X7R — HDMI_TXCP_R / HDMI_TXCN_R
(41) HDMI_TXP0_L / HDMI_TXN0_L — C55 / C52 0.1U/16V/X7R — HDMI_TXP0_R / HDMI_TXN0_R
(41) HDMI_TXP1_L / HDMI_TXN1_L — C60 / C56 0.1U/16V/X7R — HDMI_TXP1_R / HDMI_TXN1_R
(41) HDMI_TXP2_L / HDMI_TXN2_L — C64 / C61 0.1U/16V/X7R — HDMI_TXP2_R / HDMI_TXN2_R
(41) HDMI_SCL_S
(41) HDMI_SDA_S
(11,41) INT_HDMI_HPD
HDMI_CLK+_C / HDMI_CLK-_C
HDMI_TX0+_C / HDMI_TX0-_C
HDMI_TX1+_C / HDMI_TX1-_C
HDMI_TX2+_C / HDMI_TX2-_C
HDMI_CLK
HDMI_DAT
HDMI_DET_L — R38 *1K/J_NC — HDMI_DET
R388 *100K/J_NC

+3.3V_RUN
R40 *4.7K/J_NC DDC_EN
R86 *4.7K/J_NC PC0
R73 *4.7K/J_NC PC1
CFG00
R49 *100K/J_NC
(10) HDMI_PWR_CTRL — R37 *0/J_NC — OE#
R74 *3.9K/J_NC
R72 *4.7K/J_NC PC0
R47 *0/J_NC
PQ1 *2N7002W-7-F_NC — HDMI_DET
R46 *4.7K/J_NC CFG00

+5V_HDMI
R7 2.2K/J
R3 2.2K/J
HDMI_DET
+5V_RUN — HDMIF1 NANOSMDC110F-2 — +5V_HDMI
C513 *0.1U/16V/X7R_NC
C514 0.1U/16V/X7R

CN2
SHELL1 SHELL2 D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL3 SHELL4
LTS_ABA-HDM-024-P07

Reserve for EMI and close to HDMI CONN

*EXC24CG900U_NC L1 — HDMI_TX2+_C / HDMI_TX2-_C — HDMI_TX2+ / HDMI_TX2-
*EXC24CG900U_NC L4 — HDMI_TX0+_C / HDMI_TX0-_C — HDMI_TX0+ / HDMI_TX0-
*EXC24CG900U_NC L2 — HDMI_TX1+_C / HDMI_TX1-_C — HDMI_TX1+ / HDMI_TX1-
*EXC24CG900U_NC L3 — HDMI_CLK+_C / HDMI_CLK-_C — HDMI_CLK+ / HDMI_CLK-

change

HDMI_TXCP_R / HDMI_TXCN_R — HDMI_CLK+_C / HDMI_CLK-_C
HDMI_TXP0_R / HDMI_TXN0_R — HDMI_TX0+_C / HDMI_TX0-_C
HDMI_TXP1_R / HDMI_TXN1_R — HDMI_TX1+_C / HDMI_TX1-_C
HDMI_TXP2_R / HDMI_TXN2_R — HDMI_TX2+_C / HDMI_TX2-_C

UMA change to 680ohm

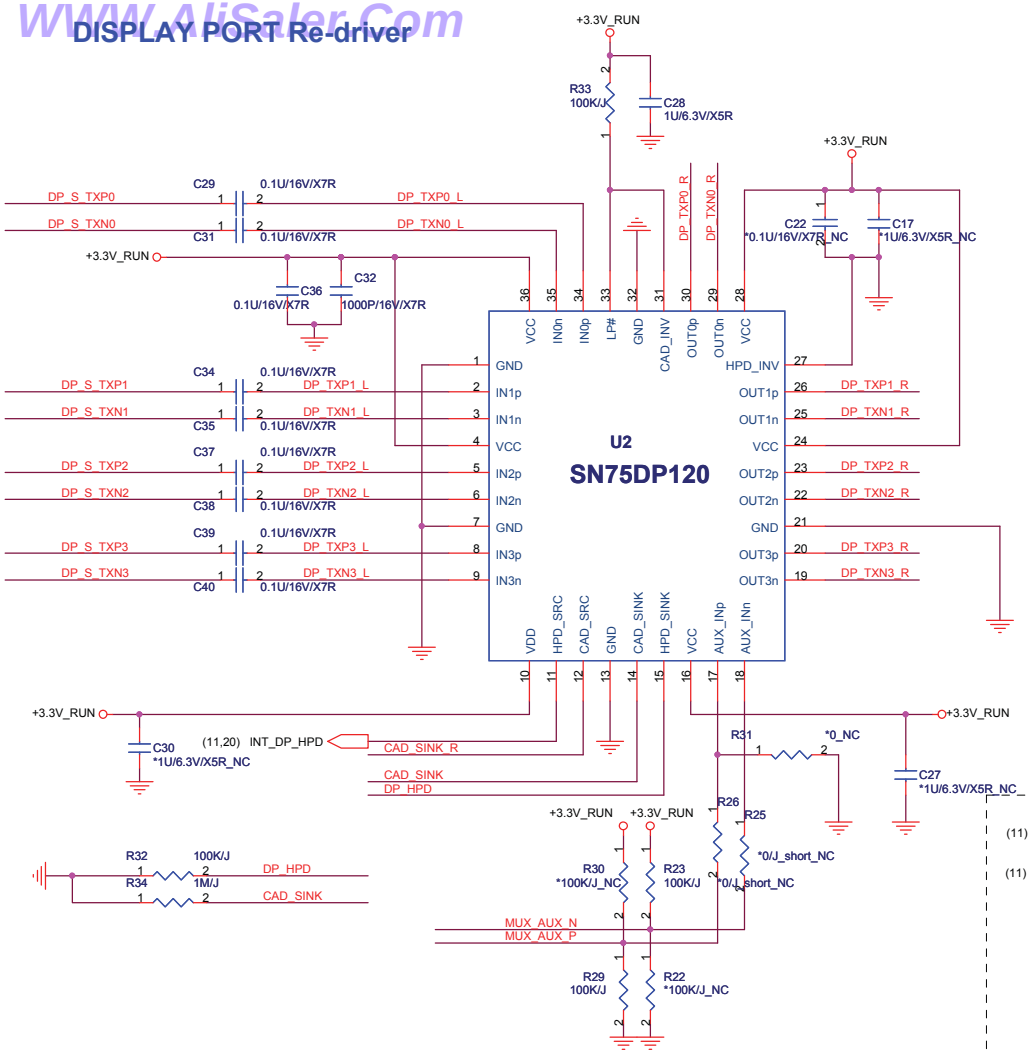
+3.3V_RUN
R736 499/F HDMI_TX2+
R734 499/F HDMI_TX2-
R737 499/F HDMI_TX1+
R731 499/F HDMI_TX1-
R729 499/F HDMI_TX0+
R733 499/F HDMI_TX0-
R735 499/F HDMI_CLK+
R730 499/F HDMI_CLK-
Q75 2N7002W-7-F
R732 1M

+3.3V_RUN
Q74 MMST3904-7-F
(11,41) INT_HDMI_HPD — HDMI_HPD — R727 150K — HDMI_DET
R728 10K

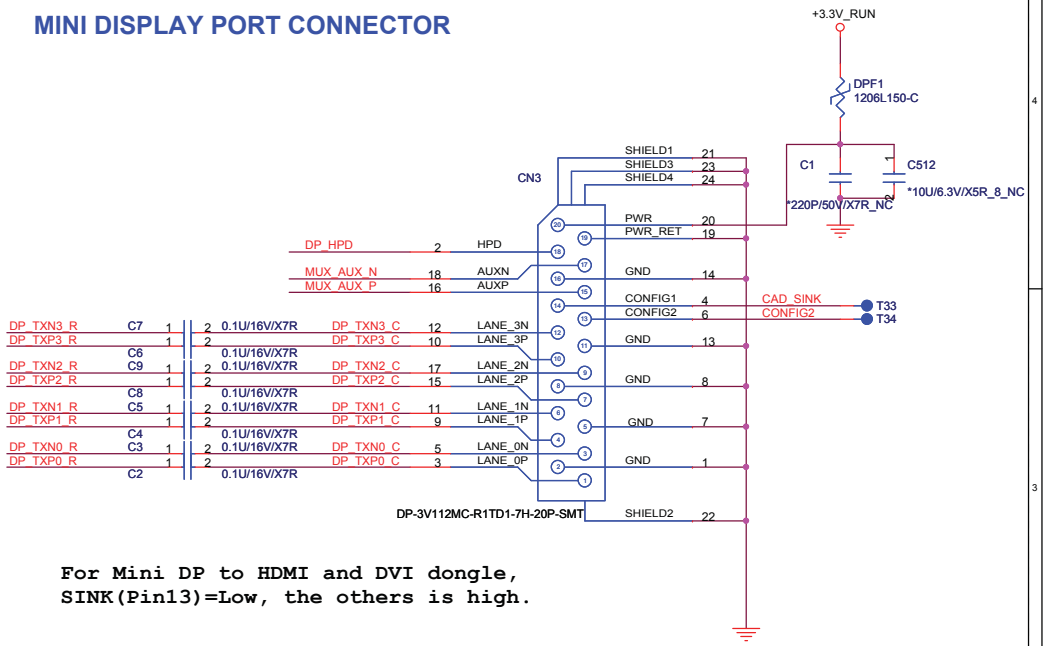
+3.3V_RUN
R709 2.2K/J
R437 2.2K/J
(41) HDMI_SCL_S — HDMI_SCL_S — Q73 FDV301N — HDMI_CLK
+3.3V_RUN
(41) HDMI_SDA_S — HDMI_SDA_S — Q72 FDV301N — HDMI_DAT

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: HDMI CONN | Rev: 1A
Date: Friday, January 07, 2011 | Sheet 25 of 59

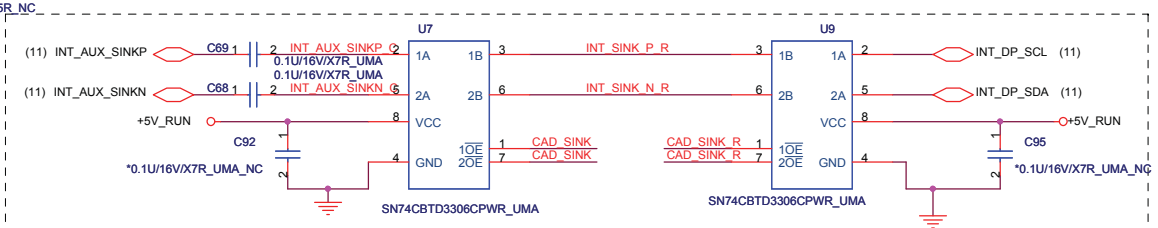
DISPLAY PORT Re-driver

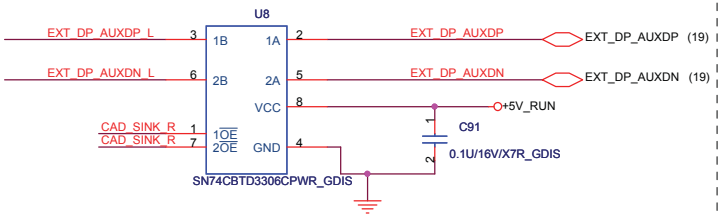


MINI DISPLAY PORT CONNECTOR

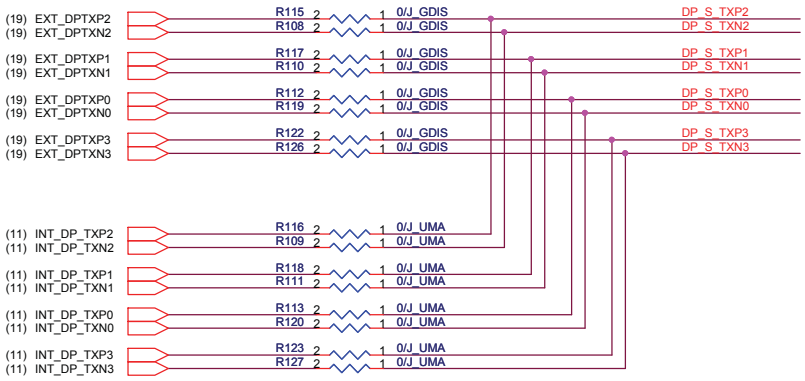


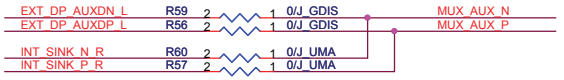
For Mini DP to HDMI and DVI dongle,
SINK(Pin13)=Low, the others is high.





OE	Output
L	A=B
H	Z





Quanta Computer Inc.			
PROJECT : GM6C MLK DIS			
Size	Document Number		Rev
	MINI DP CONN		1A
Date: Friday, January 07, 2011	Sheet 26 of 59		

+CR_PWR
+3.3V_CARD
R517
(>20mil)
*0/J_6_short_NC
C475
*10U/6.3V/X5R_8_NC

+DVDD18
+APVDD
(>40mil)
R514
*0/J_6_short_NC

+3.3V_RUN
+VDD33
(>40mil)
R512
*0/J_6_short_NC

2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.

+3.3V_CARD
C511
10U/6.3V/X5R_8

CON3
ALPS
5in1-5-250907001000-9-45p

SD_MS_XD-D2
SD_MS_XD-D3
SD_MS_XD-D4
SD-CMD_MS-BS_XD-WE#
SD_MS_XD-D5
SD-CLK_MS-CLK_XD-CE#
SD_MS_XD-D3
MS_CD#
SD_MS_XD-D2
SD_MS_XD-D0
SD_MS_XD-D1
SD-CMD_MS-BS_XD-WE#
SD-CLK_MS-CLK_XD-CE#
SD_MS_XD-D6
SD_MS_XD-D7
SD_MS_XD-D0
SD_MS_XD-D1

SD-9(D2)
SD-1(D3)
MMC-10(D4)
SD-2(SD_CMD)
MMC-11(D5)
SD-3(VSS)
SD-4(VDD)
MS-10(VSS)
MS-9(VCC)
MS-8(SCLK)
MS-7(D3)
MS-6(INS)
MS-5(D2)
MS-4(D0)
MS-3(D1)
MS-2(BS)
MS-1(VSS)
SD-5(CLK)
MMC-12(D6)
SD-6(GND)
MMC-13(D7)
SD-7(D0)
SD-8(D1)

SD(SW.COM)
SD(SW.CD)
XD-1(CDSW)
XD-0(GND)
XD-2(R/-B)
XD-3(RE)
XD-4(CE)
XD-5(CLE)
XD-6(ALE)
XD-7(WE)
XD-8(-WP)
XD-9(GND)
XD-10(D0)
XD-11(D1)
XD-12(D2)
XD-13(D3)
XD-14(D4)
XD-15(D5)
XD-16(D6)
XD-17(D7)
XD-18(VCC)
SD(SW.WP)

+3.3V_CARD
SD_CD#
XD_CD#
XD-R/B#
XD-RE#
SD-CLK_MS-CLK_XD-CE#
XD-CLE
XD-ALE
SD-CMD_MS-BS_XD-WE#
SD-WP_XD-WP#
SD_MS_XD-D0
SD_MS_XD-D1
SD_MS_XD-D2
SD_MS_XD-D3
SD_MS_XD-D4
SD_MS_XD-D5
SD_MS_XD-D6
SD_MS_XD-D7
SD-WP_XD-WP#

C509
270P/50V/X7R
C690
*10P/50V/C0G_NC
C689
*10P/50V/C0G_NC
C508
*270P/50V/X7R_NC
C694
*270P/50V/NPO_NC

+DVDD18
C496
*0.1U/16V/X7R_NC

+VDD33
C494
*0.1U/16V/X7R_NC

+3.3V_CARD
R519
1K/J
SD-WP_XD-WP#
R516
1K/J
XD-R/B#

+3.3V_RUN
R511
10K/J
XD-CLE
R520
*200K/J_NC
XD-ALE

+VDD33
U22
JMB389
C493
0.1U/16V/X7R
+DVDD18
XD-CLE
SD-CMD_MS-BS_XD-WE#
SD-CLK_MS-CLK_XD-CE#_R
R510
*0/J_short_NC
SD-CLK_MS-CLK_XD-CE#
C484
*22P/50V/NPO_NC
+VDD33
C489
2.2U/6.3V/X5R_6
C498
0.1U/16V/X7R
SD_MS_XD-D3
SD_MS_XD-D2
SD_MS_XD-D1
SD_MS_XD-D0

DV18
GND
TXIN
MDIO7
MDIO4
MDIO5
SDDV33_18
DV33
MDIO3
MDIO2
MDIO1
MDIO0

MDIO6
MDIO13
MDIO14
CR1_LEDN
DV33
DV33
DV18
CR1_PCTLN
CR1_CD0N
CR1_CD1N
CR1_CD2N
CPPE_N

SD-WP_XD-WP#
XD-R/B#
XD-ALE
SD_CD#
MS_CD#
XD_CD#

XRSTN
XTEST
APCLKP
APCLKN
APVDD
APGND
ARREXT
APRXP
APRXN
APVTX
APTXN
APTXP

JMB389

MIDO Single End = 50 ohm

MIDO[0..5] Single Skew
Should be smaller +/- 100 mil
for SDA3.Application

+VDD33
C500
0.1U/16V/X7R
+DVDD18
+CR_PWR
C510
*10U/6.3V/X5R_8_NC
C507
0.1U/16V/X7R
CPPE_N# C

Needs close to Pin17: 12mil/<250mil

+3.3V_SUS
R518
*10K/J_NC
CPPE_N# (12)
Q51
*2N7002W-7-F_NC

For AMD Platform only, Intel doesn't need to connect to PCH(Vendor)

Layout Note:
Place this cap close to pin 18

SD_MS_XD-D1
R508
*0/J_NC
C485
*10P/50V/C0G_NC

(4,11,17,28,29,30,31,40) PLTRST#
R507
*0_short_NC
C490
*0.1U/16V/X7R_NC
16
X7R

(10) CLK_PCIE_CRN
(10) CLK_PCIE_CRP
R515 12K/J

+APVDD
W/L=20mil/<200mil
C504
10U/6.3V/X5R_8
C501
*0.1U/16V/X7R_NC
C502
*1000P/16V/X7R_NC
C503
0.1U/16V/X7R

(10) PCIE_TXP5
(10) PCIE_TXN5
PCIE_TXP5
PCIE_TXN5

(10) PCIE_RXN5
(10) PCIE_RXP5
C505
C506
0.1U/16V/X7R PCIE_RXN5_C
0.1U/16V/X7R PCIE_RXP5_C

Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/xD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Card Reader (JMB389)	1A
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BX1 leakage issue workaround circuit
R96,C104 no stuff,R100 stuff
BX2 will close it.
R96,C104 stuff,R100 no stuff

Layout Note: Place these caps close to ITE8502

Layout Note: Place PC169 close to ITE8502

IT8518E/CX

prochot pin level shift

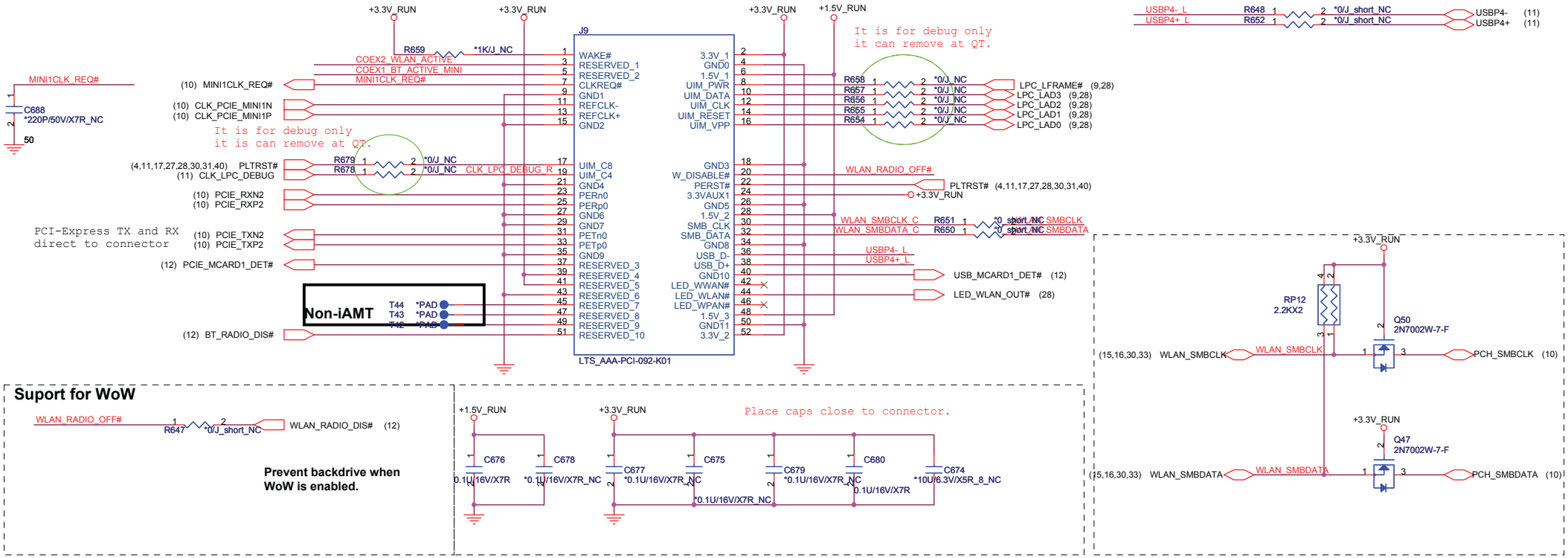
Board ID Straps

Config_0	Config_1	GM6/GM6C
0	0	UMA
0	1	Optimum-GE
1	0	Studio Discrete
1	1	Optimum-GS

USB_BACK_EN#	BID1	GM6/GM6C
0	0	SSI (X00)
0	1	PT (X01)
1	0	ST (X02)
1	1	QT (A00)
0	0	(A01)

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size: Document Number: SIO (ITE8518) Rev: 1A
Date: Friday, January 07, 2011 Sheet 28 of 59

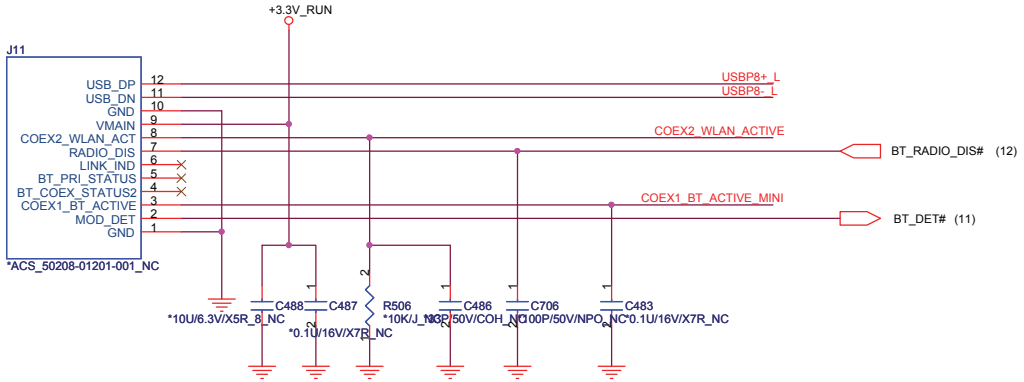
MiniCard WLAN connector

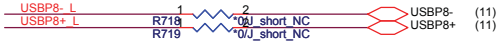


Suport for WoW

Prevent backdrive when WoW is enabled.

Support Dell BT375 (Little Stone) module (XPS) W TO B



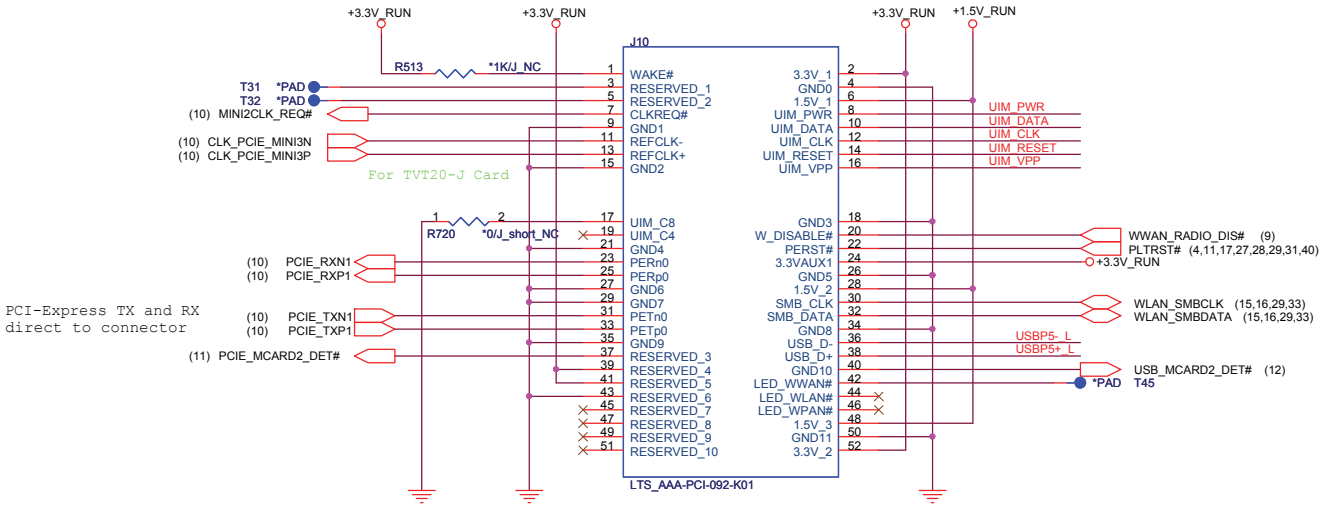


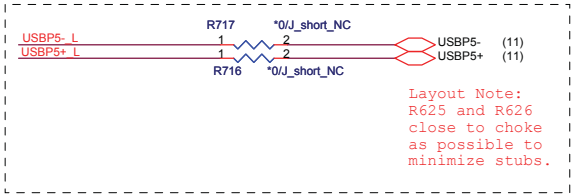
Quanta Computer Inc.

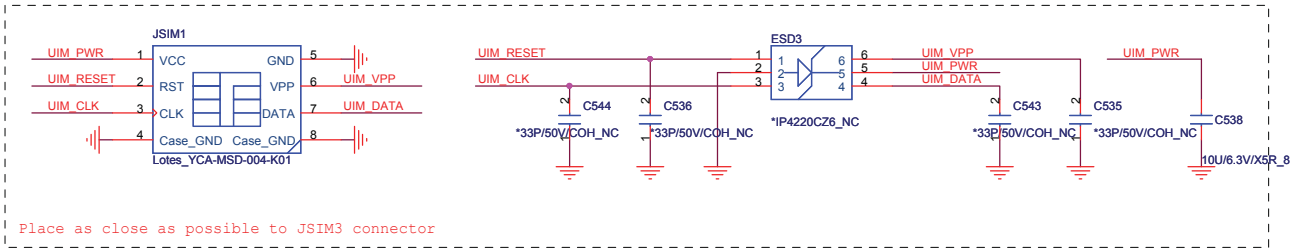
PROJECT : GM6C MLK DIS

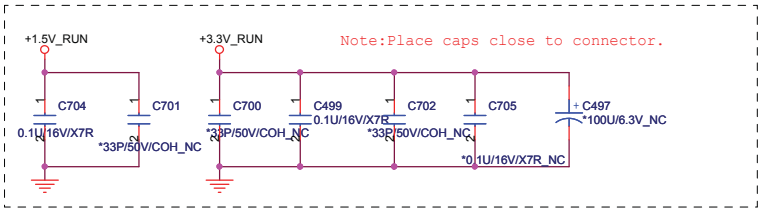
Size	Document Number	Rev
	MINI-Card (WLAN/WPAN)	1A
Date: Friday, January 07, 2011	Sheet 29 of 59	

MiniCard WWAN connector









Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	MINI-Card (WWAN)	1A

Date: Friday, January 07, 2011 Sheet 30 of 59

+1.05V_LAN_S
L18
4.7uH_680mA_DCR=0.12 @7.96MHz
R176
*0_short_NC
+1.05V_LAN
C147 4.7U/6.3V/X5R_6
C150 0.1U/16V/X7R
C148 0.1U/16V/X7R
C106 0.1U/16V/X7R
C111 *0.1U/16V/X7R_NC
C128 *0.1U/16V/X7R_NC
For L50, C420, C62 need to check layout guild
Close to pin 3, 6, 9, 13, 29, 41 and 45

+3.3V_LAN
R105 603
+3.3V_SUS
*0/J_6_short_NC

+3.3V_LAN
C109 0.1U/16V/X7R
C102 0.1U/16V/X7R
C103 0.1U/16V/X7R
C136 0.1U/16V/X7R
C104 *0.1U/16V/X7R_NC
*0.1U/16V/X7R_NC
Place Close to LAN chip, pin 12, 27, 39, 42, 47 48

+3.3V_LAN
C146 4.7U/6.3V/X5R_6
C149 *0.1U/16V/X7R_NC
Place Close to LAN chip, pin 34 and 35

9 VIA ON CHIP SET, FOOTPRINT UPDATE

U13
RTL8111E-VB-GR
+1.05V_LAN +3.3V_LAN +1.05V_LAN +3.3V_LAN +3.3V_LAN
R124 2.49K/F
+3.3V_LAN
R157 1K/J
LAN_XTALO
LAN_XTALI
R130 *0/J_short_NC
Y1 25MHz
C114 22P/50V/NPO
C113 22P/50V/NPO
GND
MDIP0 MDIN0 AVDD1(NC) MDIP1 MDIN1 AVDD1(NC) MDIP2(NC) MDIN2(NC) AVDD1(NC) MDIP3(NC) MDIN3(NC) AVDD3(NC)
TRD0+ TRD0- TRD1+ TRD1- TRD2+ TRD2- TRD3+ TRD3-
AVDD33 AVDD33(NC) RSET AVDD1 CKXTAL2 CKXTAL1 AVDD3(AVDD1) VDD1(NC) LED0 LED3 GPIO/SMBALERT LED1/EESK
SROUT1 VDDSR VDDSR ENSR EEDI/SDA LED3/EDO EECS/SCL DVDD1 LANWAKEB VDD3 ISOLATEB PERSTP
Enable +1.05VLAN_S
ISOLATE#
+1.05V_LAN_S +3.3V_LAN +3.3V_LAN
R174 *0/J_short_NC
R175 *0/J_NC
R173 10K/J
R172 10K/J
+3.3V_SUS
R746 10K/J
02
+1.05V_LAN
+3.3V_LAN
EC_PCIE_WAKE# (28)
R184 *0/J_short_NC
PLTRST# (4,11,17,27,28,29,30,40)
DVDD1 SMBCLK(NC) SMBDATA(NC) CLKREQB HSIP HSIN REFCLK_P REFCLK_M EVDD1 HSOP HSON GNDTX

RJ-45 Connector
CON1 ALLTOP_C100A3
RJ45-TX3- RJ45-TX3+ RJ45-TX1- RJ45-TX2- RJ45-TX2+ RJ45-TX1+ RJ45-TX0- RJ45-TX0+
CHSGND1 CHSGND2
Wait for Connector list to update

+1.05V_LAN
R125 10K/J
(10) LOM_CLK_REQ#
R135 *0/J_short_NC
R144 *0/J_short_NC
+1.05V_LAN
(10) PCIE_TXP6
(10) PCIE_TXN6
(10) CLK_PCIE_LOMP
(10) CLK_PCIE_LOMN
(10) PCIE_RXP6
(10) PCIE_RXN6
C137 0.1U/16V/X7R PCIE_RXP6_C
C141 0.1U/16V/X7R PCIE_RXN6_C
C131 1U/6.3V/X5R
C130 0.1U/16V/X7R

+3.3V_RUN
R170 *1K/F_NC
R171 *15K/F_NC
ISOLATE#
R169 100/F
LAN_PCIE_PWR_CTRL# (28)
D13 *RB501V-40_NC

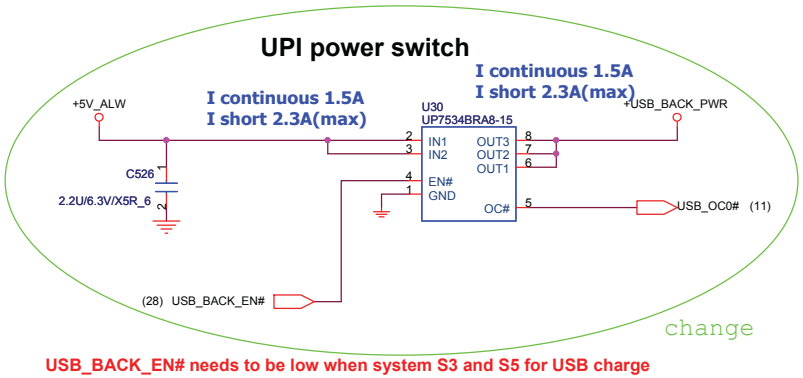
Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needs to be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side

Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state

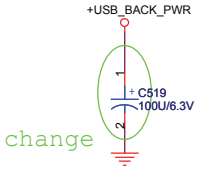
R526 75/F TXCT0
R525 75/F TXCT1
R524 75/F TXCT2
R523 75/F TXCT3
C517 1000P
ESD2 *CM1293A-04SO_NC
TRD2- TRD2+ TRD3+ TRD3-
+3.3V_LAN
C529 *0.1U/16V/X7R_NC
ESD1 *CM1293A-04SO_NC
TRD0- TRD0+ TRD1+ TRD1-
+3.3V_LAN
C528 *0.1U/16V/X7R_NC
C527 0.01U/25V/X7R
L31
LFE9276C-R
TDCT
TCT0 TD0+ TD0- TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3-
MCT0 TX0+ TX0- MCT1 TX1+ TX1- MCT2 TX2+ TX2- MCT3 TX3+ TX3-
TXCT0 RJ45-TX0+ RJ45-TX0- TXCT1 RJ45-TX1+ RJ45-TX1- TXCT2 RJ45-TX2+ RJ45-TX2- TXCT3 RJ45-TX3+ RJ45-TX3-
Reserver for EMI

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: LAN (RTL8111EL/RJ45) | Rev: 1A
Date: Friday, January 07, 2011 | Sheet 31 of 59

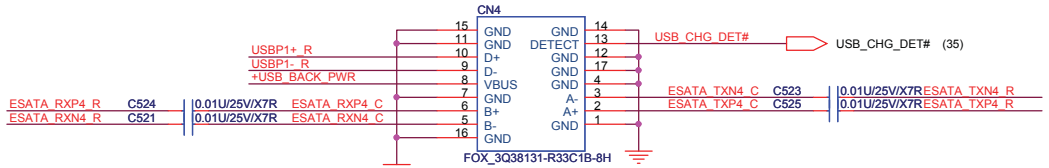
ESATA + USB Conn + Power Share

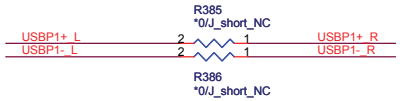


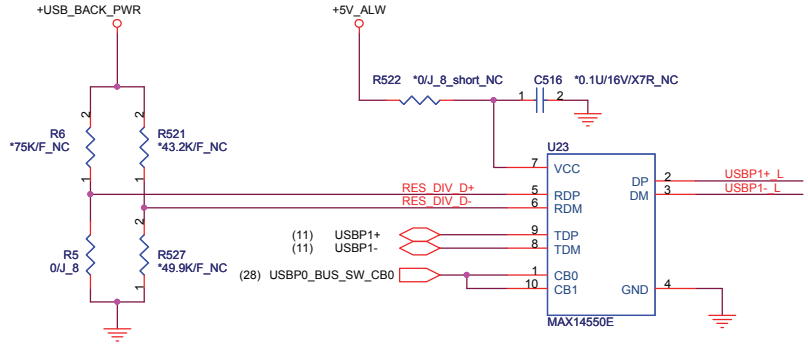
USB_BACK_EN# needs to be low when system S3 and S5 for USB charge



This pin connects to 3VALW ON POWER LOGIC







EC needs to drive CB0/CB1 pins to low
when system S3/S5 and dirve high when system S0.

U49 PN and Footprint needs to double check

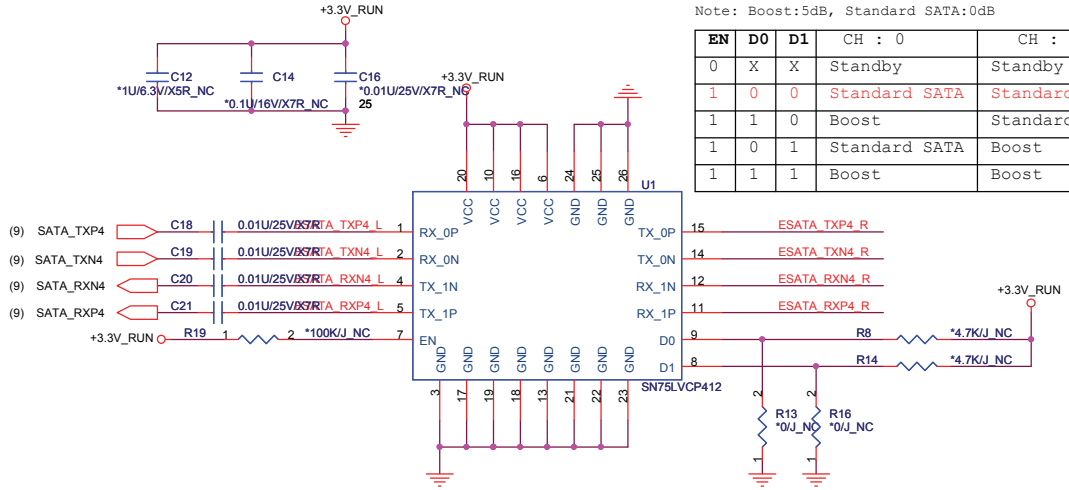
R15 needs to be 49.9K_F if we use external resisters.

CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only

(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



Note: Boost:5dB, Standard SATA:0dB

EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Righ PUSB/ESATA	1A
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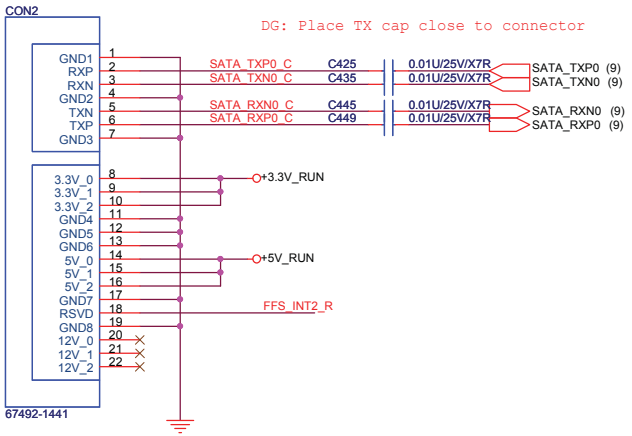
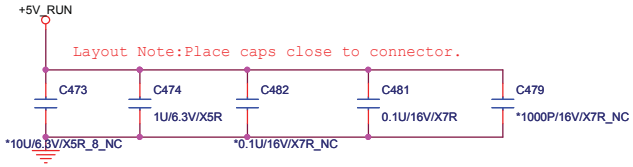
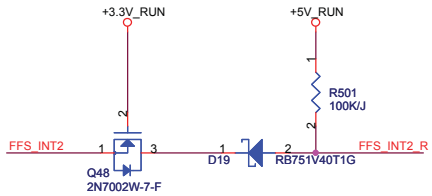
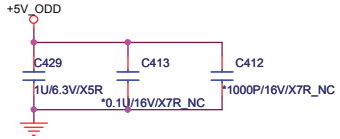
SATA Connector.



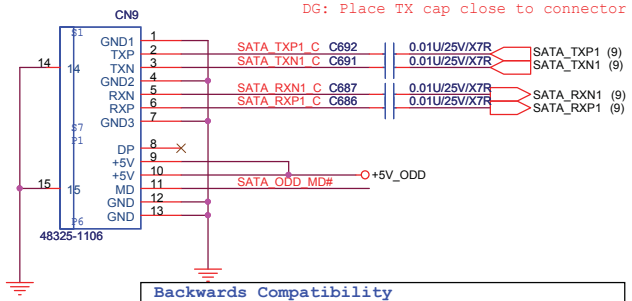




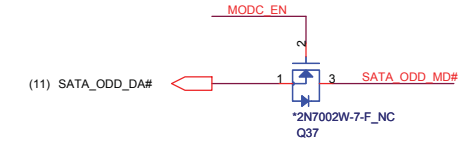
ODD Connector



Layout Note:Place caps close to connector.



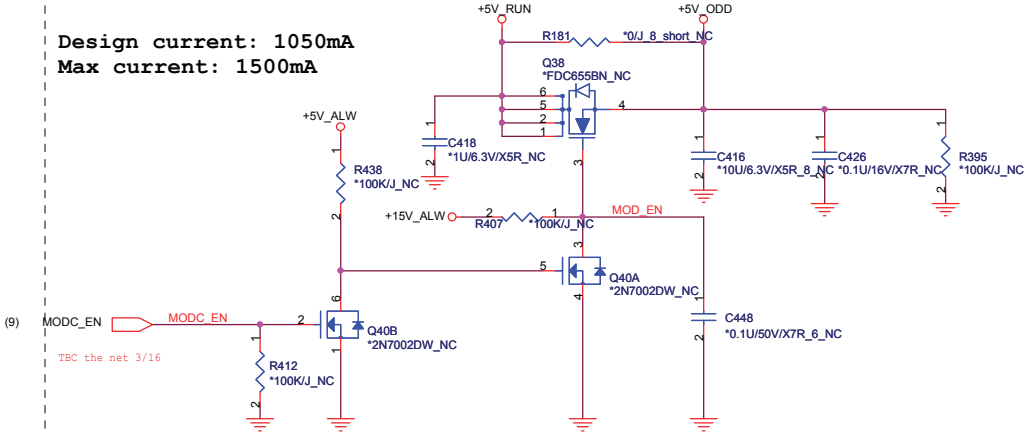
Backwards Compatibility



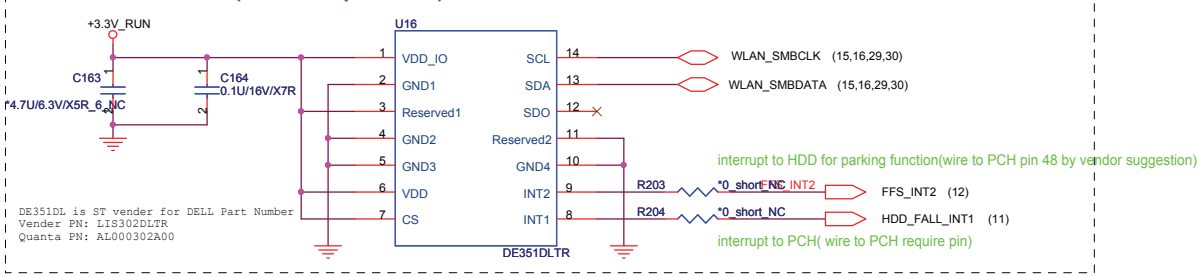
Drive powered on, MD# is High
Drive powered off, MD# is Low

Because the drive does not support ZPODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive

Design current: 1050mA
Max current: 1500mA



3-axis Fall Sensor (HDD data protector)



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: SATA (HDD&ODD)	Rev 1A
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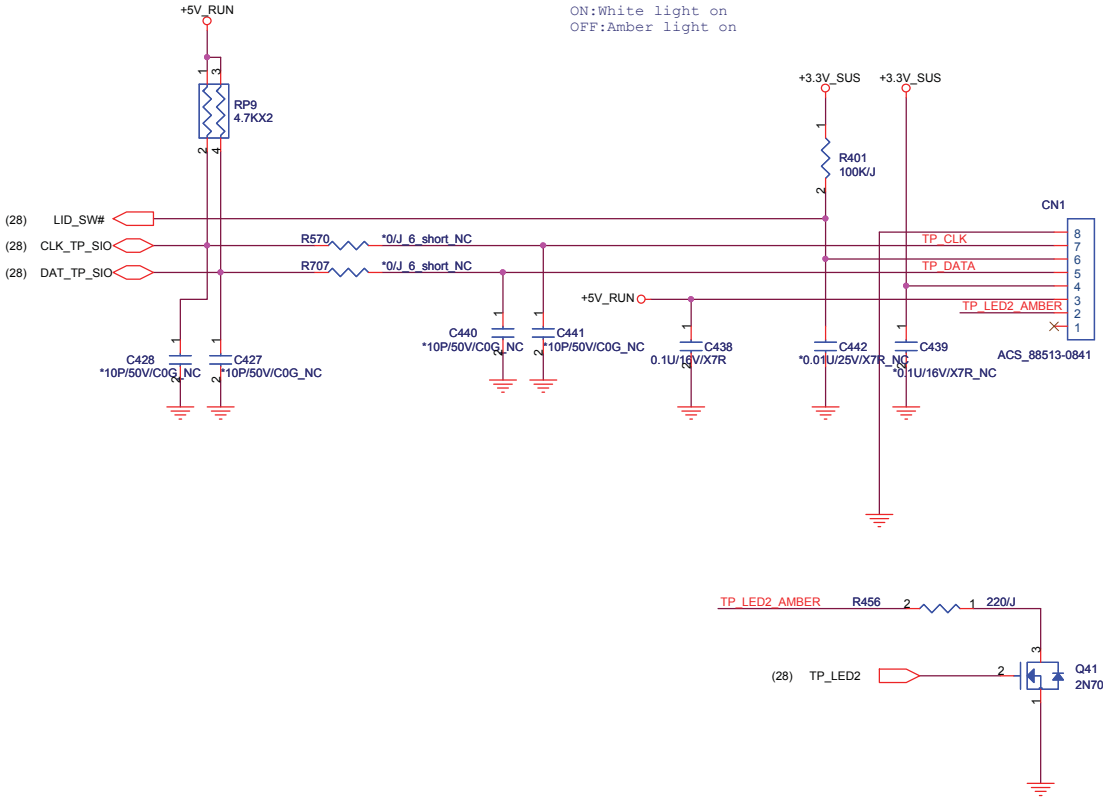
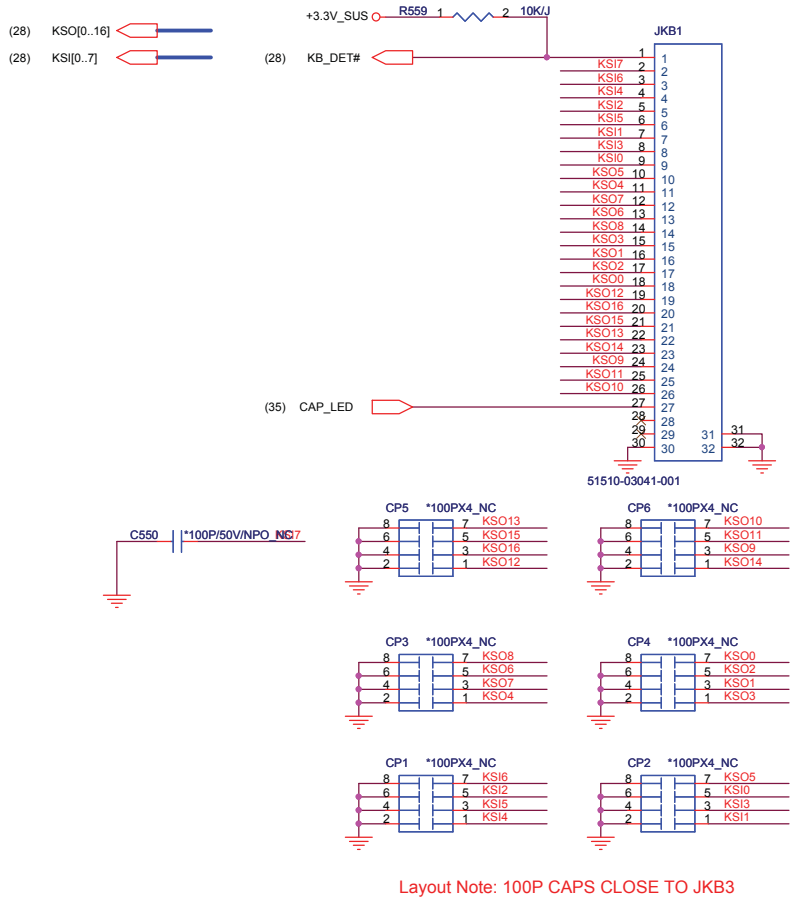
Touch Pad

ON:White light on
OFF:Amber light on



KEYBOARD CONNECTOR



Layout Note: 100P CAPS CLOSE TO JKB3

Key board illumination

+KB_LED power trace width >10 mil

Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number TP/KB	Rev 1A
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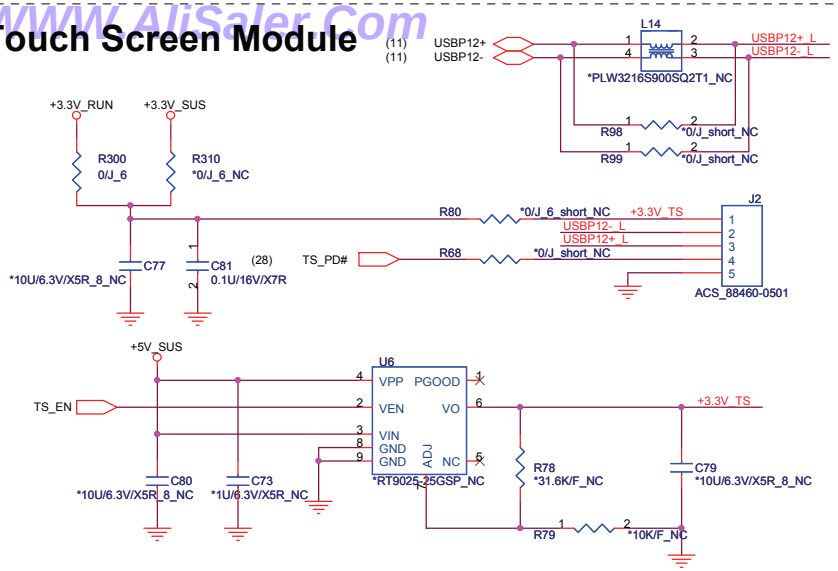
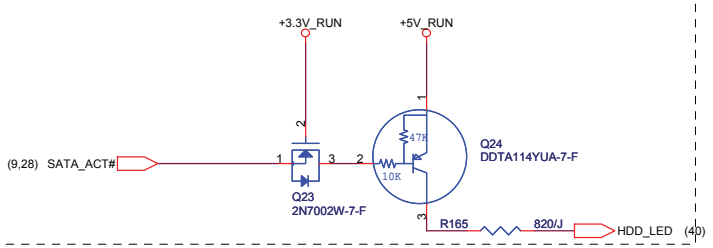
Touch Screen Module

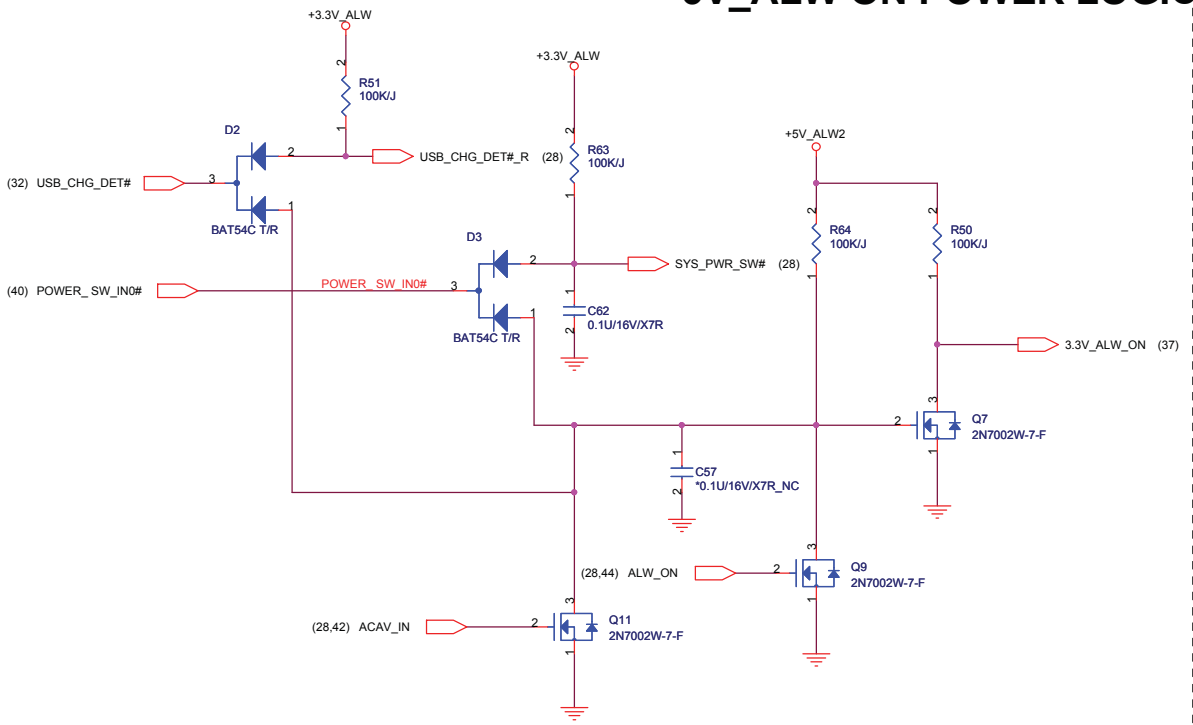


HDD activity LED.

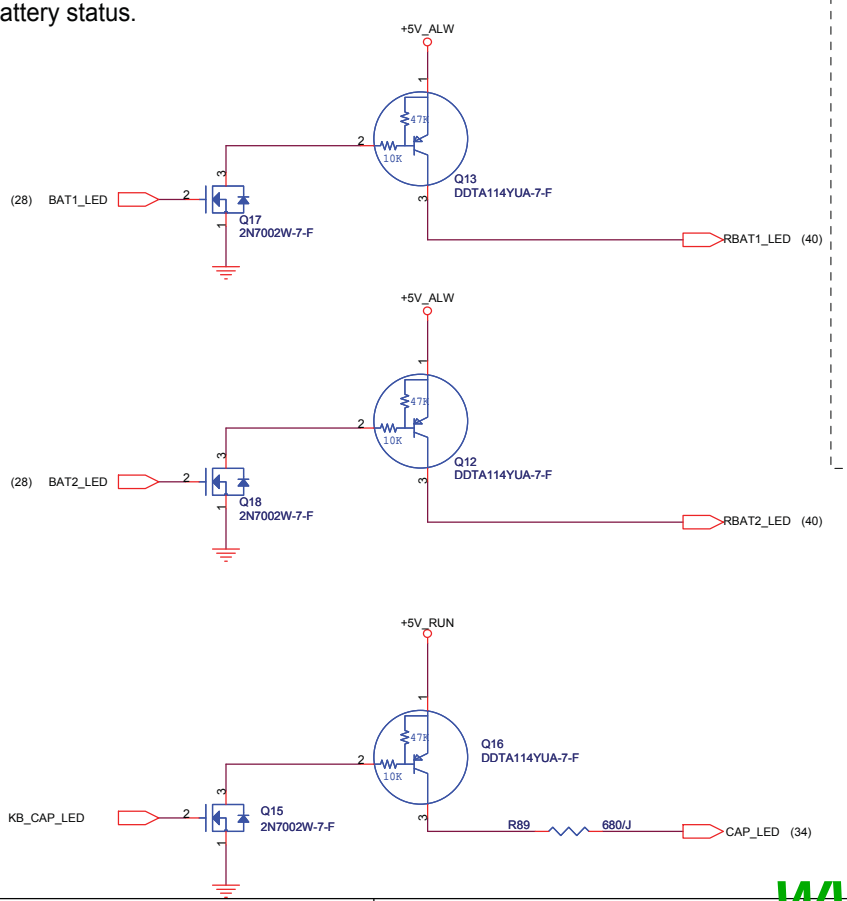


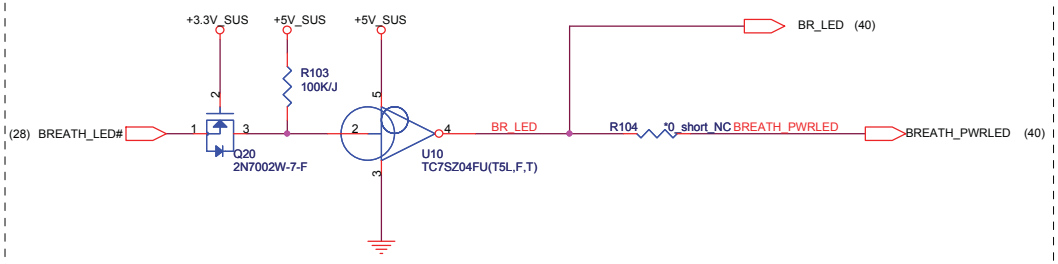
Power button for Engineer

3V_ALW ON POWER LOGIC



Battery status.



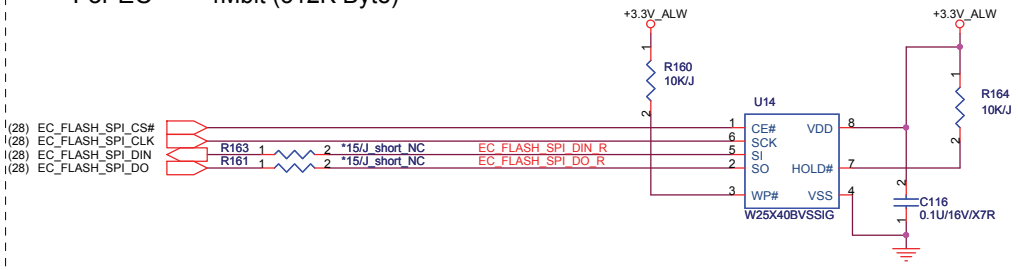


Quanta Computer Inc.

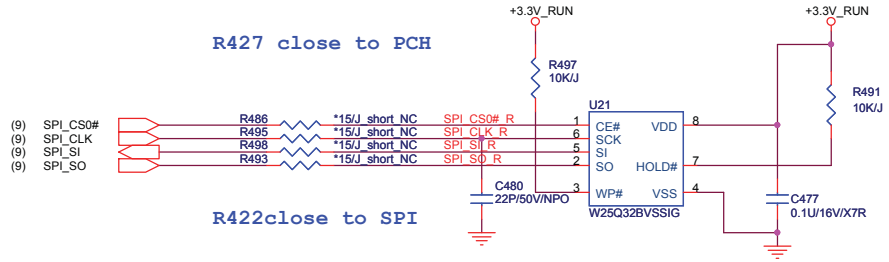
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	SWITCH/LED/T-Screen	1A
Date: Friday, January 07, 2011	Sheet 35 of 59	

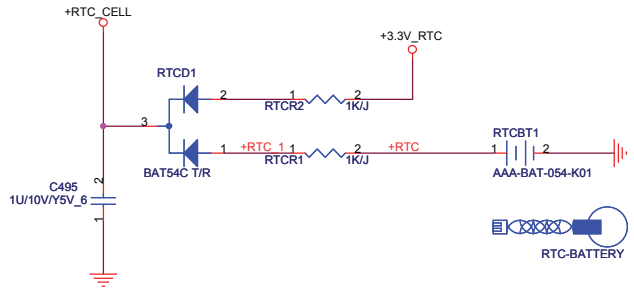
For EC 4Mbit (512K Byte)



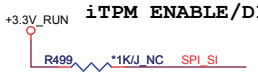
For PCH 32Mbit (4M Byte)



RTC BATTERY

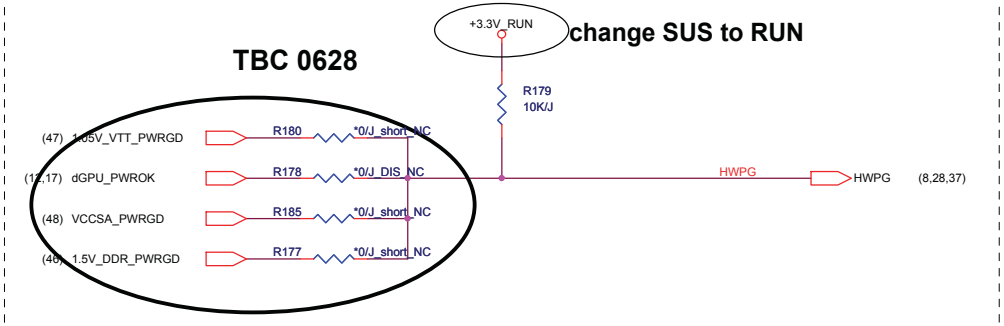


iTPM ENABLE/DISABLE

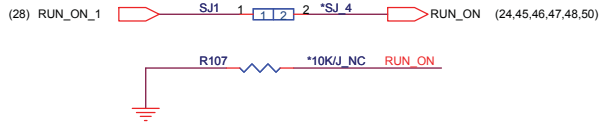


TPM Function	R428
Enable	Mount
Disable	NC (Default)

RESET CIRCUIT



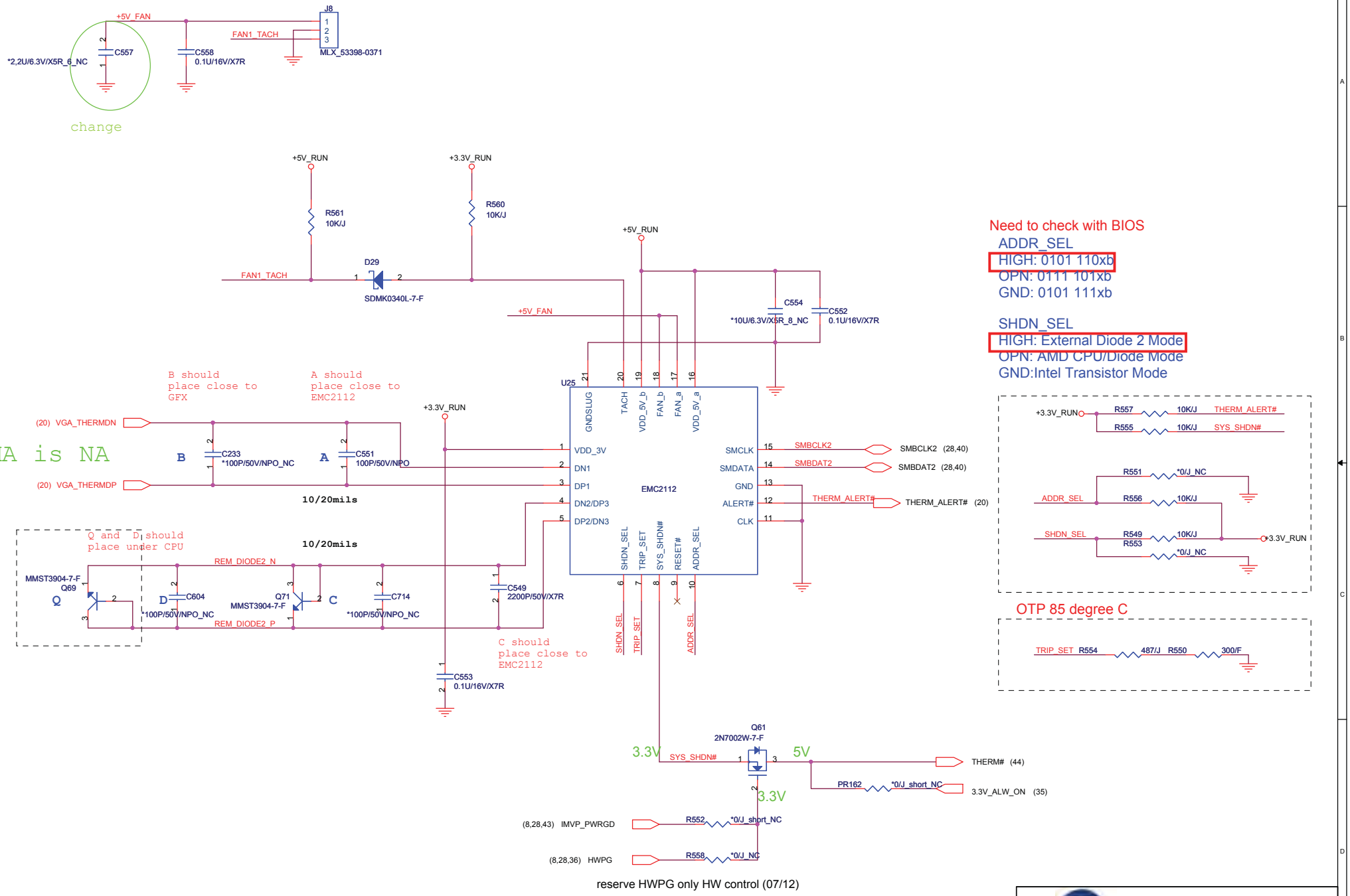
delet VTT_POWERGOOD(07/12)



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

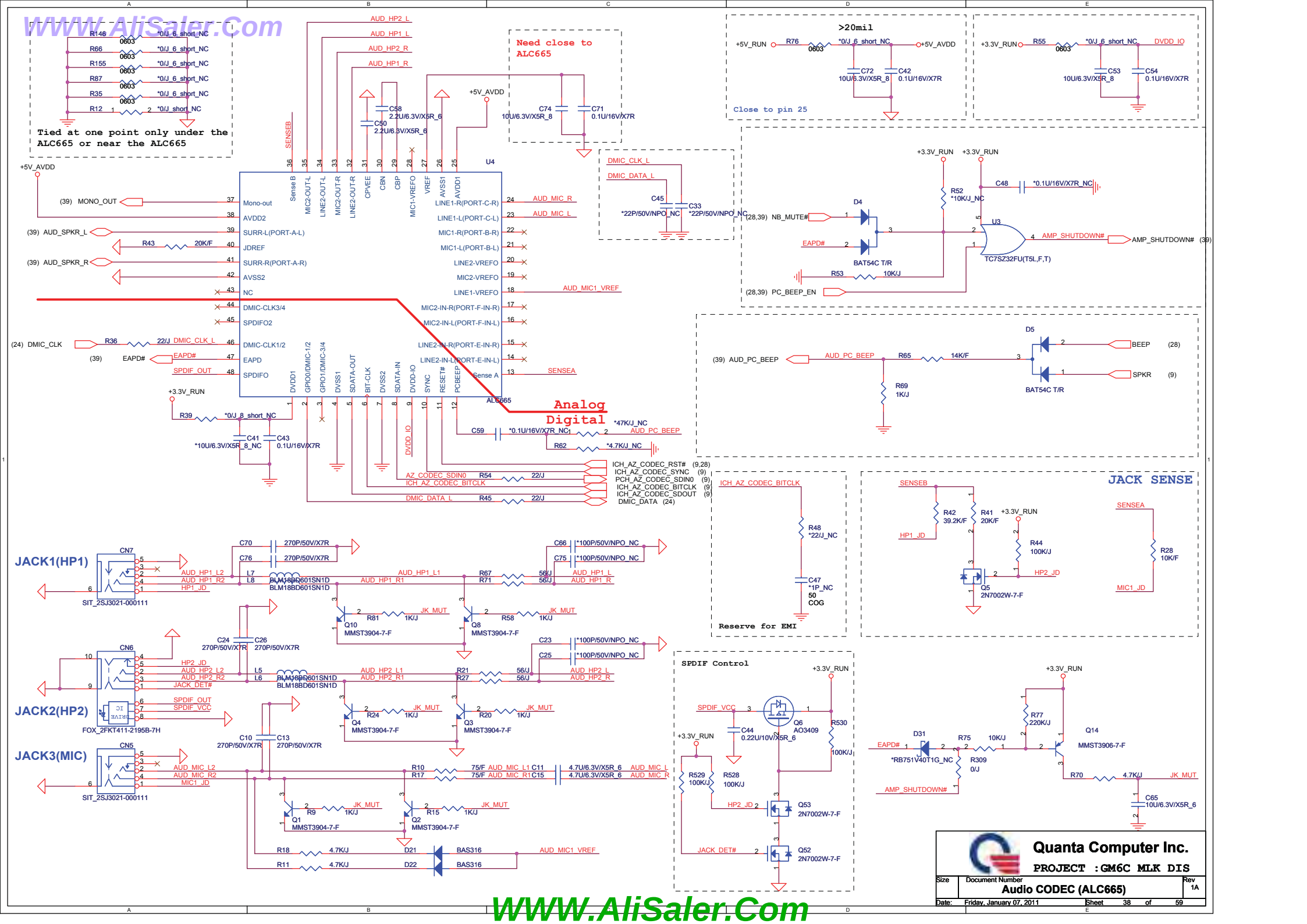
Size	Document Number	Rev
	FLASH/RTC/RESET CIRCUIT	1A
Date: Friday, January 07, 2011	Sheet 36 of 59	



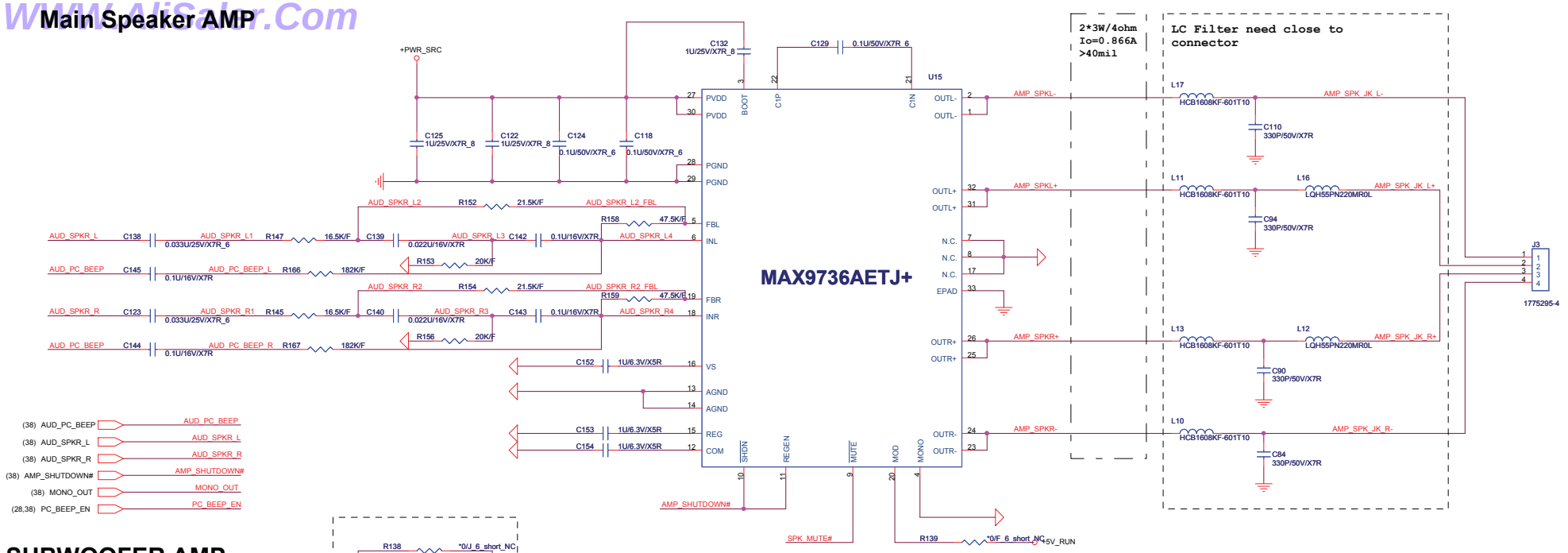
for UMA is NA

reserve HWPG only HW control (07/12)

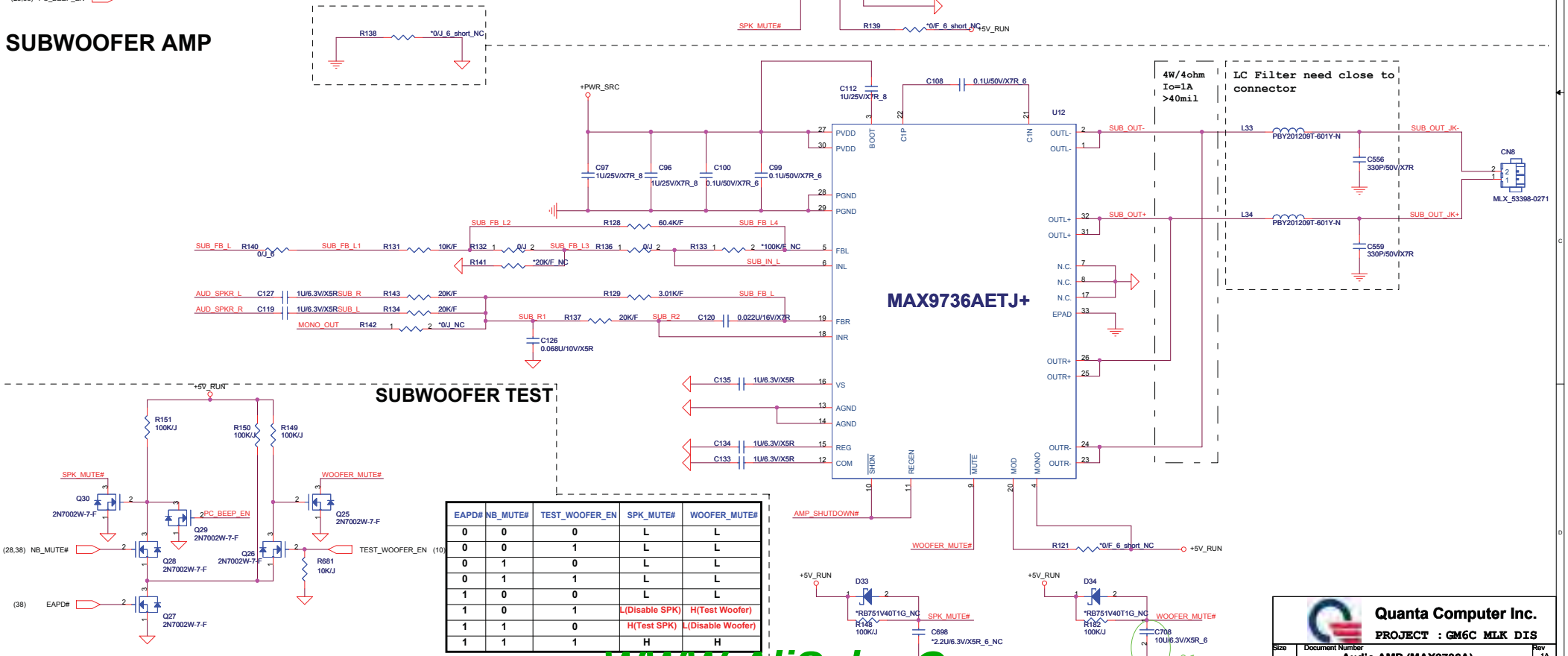
Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: FAN/THERMAL	Rev: 1A
Date: Friday, January 07, 2011	Sheet 37 of 59	



Main Speaker AMP



SUBWOOFER AMP

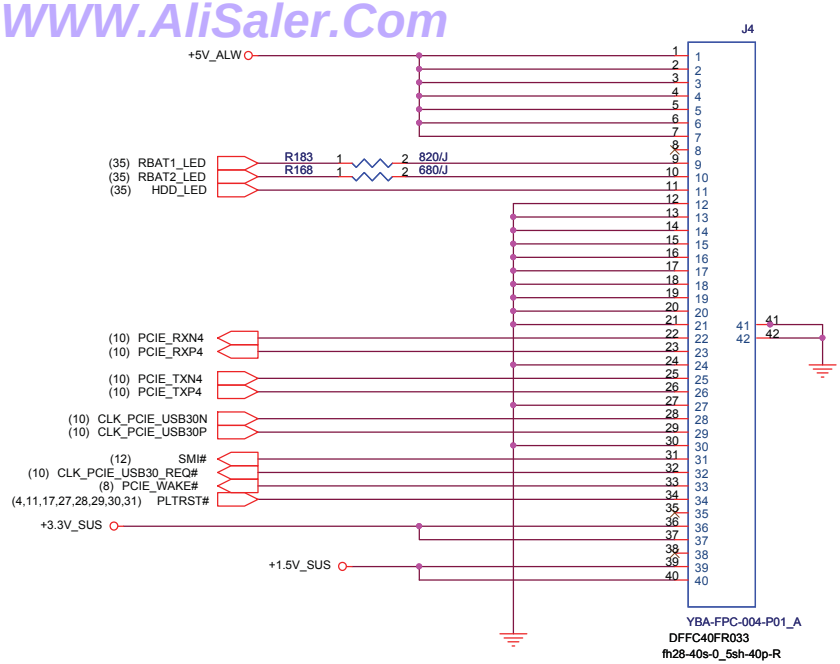


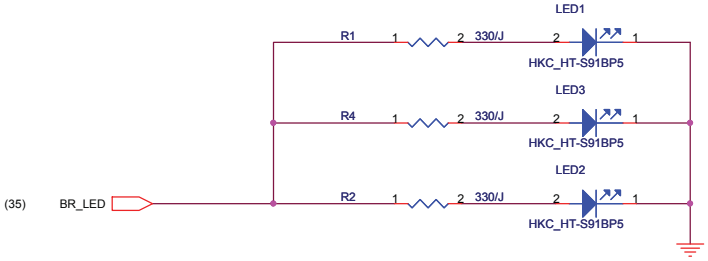
SUBWOOFER TEST

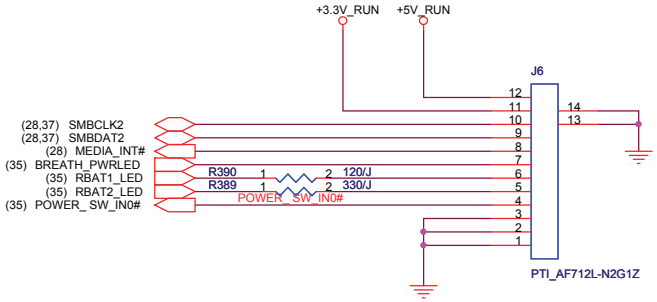
EAPD#	NB_MUTE#	TEST_WOOFER_EN	SPK_MUTE#	WOOFER_MUTE#
0	0	0	L	L
0	0	1	L	L
0	1	0	L	L
0	1	1	L	L
1	0	0	L	L
1	0	1	L(Disable SPK)	H(Test Woofer)
1	1	0	H(Test SPK)	L(Disable Woofer)
1	1	1	H	H

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Audio AMP (MAX9736A)	1A
Date: Friday, January 07, 2011	Sheet 39 of 59	





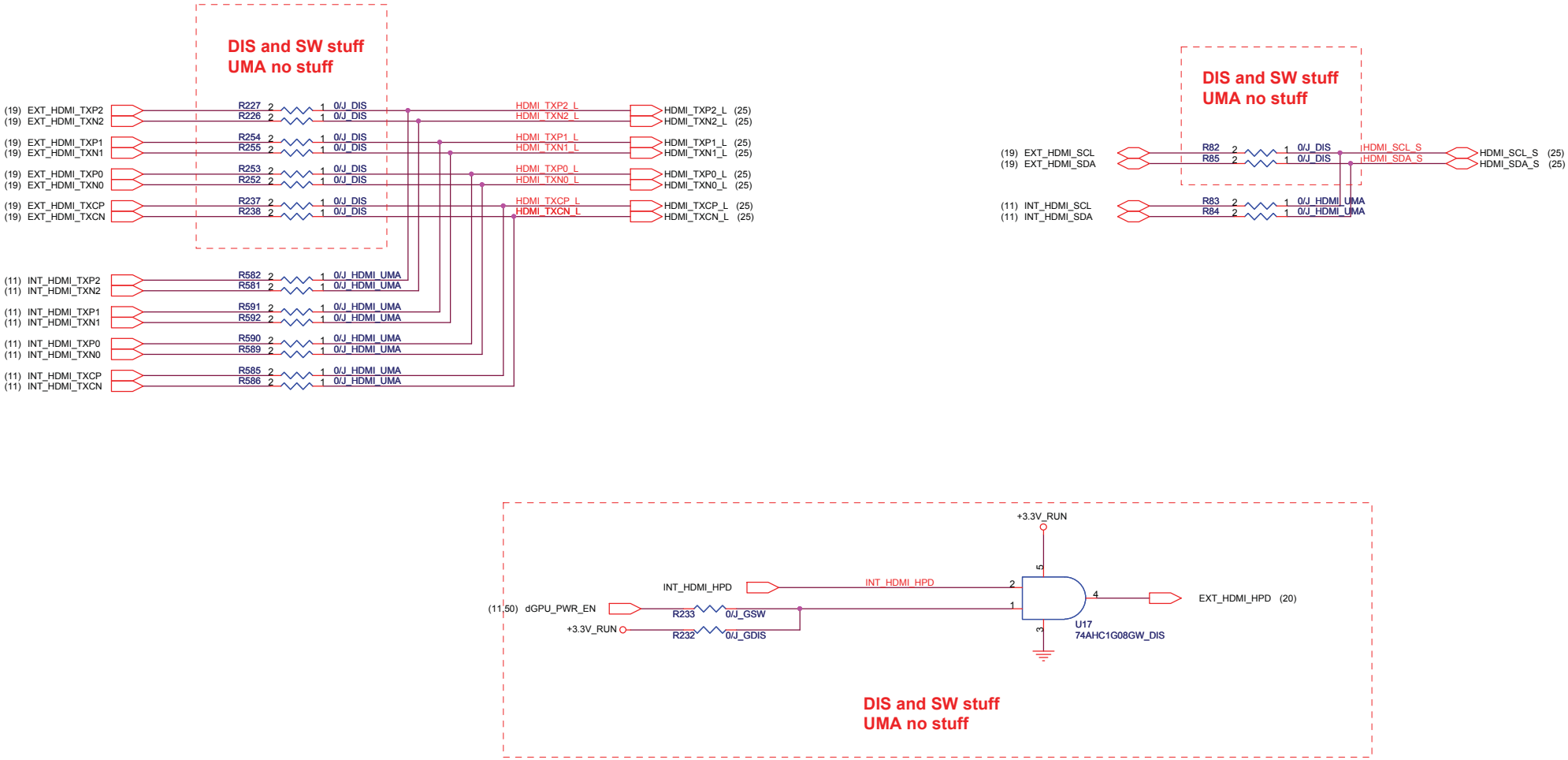


Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Left USB/MMB CONN	1A
Date: Friday, January 07, 2011	Sheet 40 of 59	

HDMI Switch

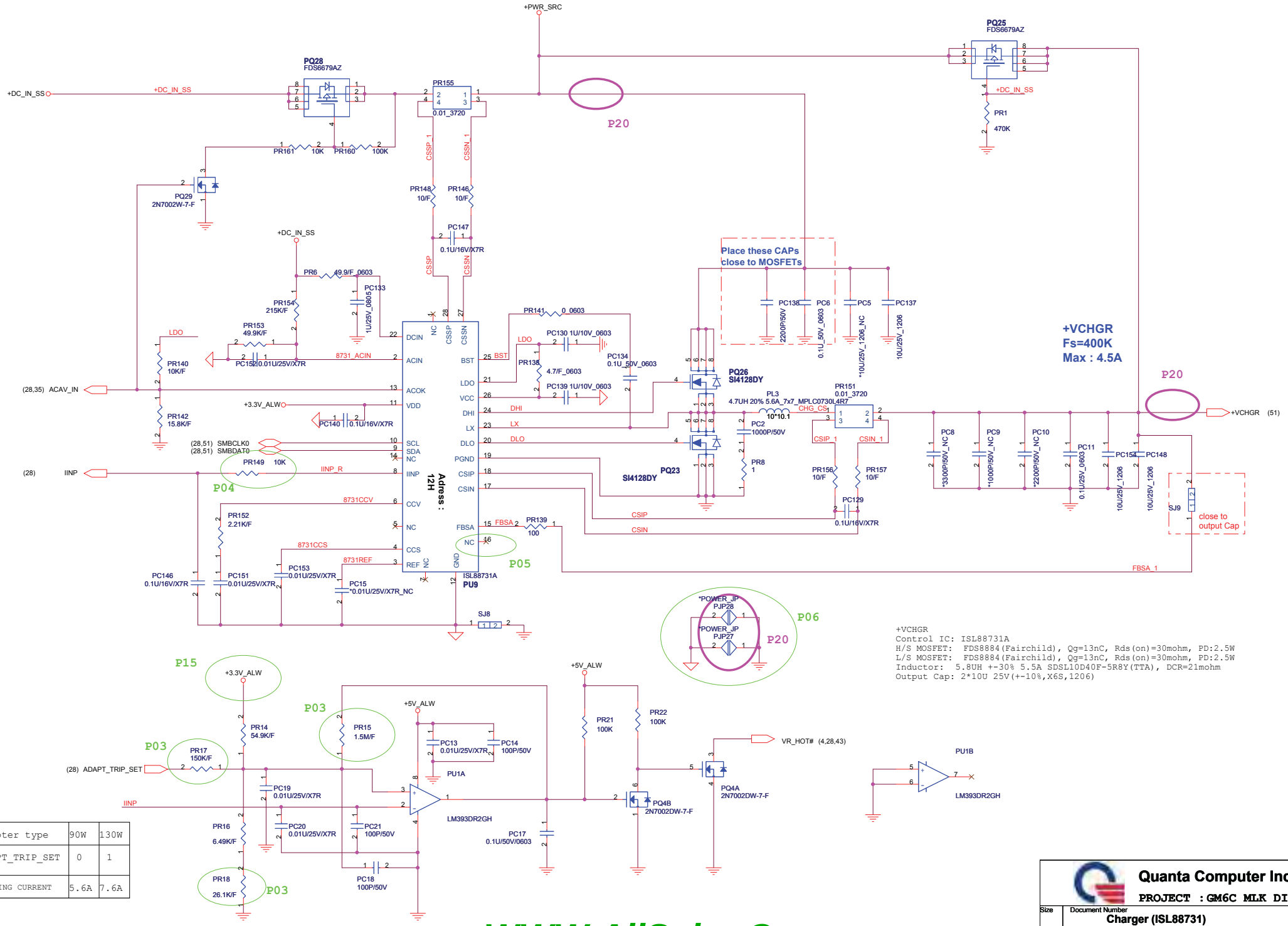


Quanta Computer Inc.

PROJECT : GM6C MLK DIS

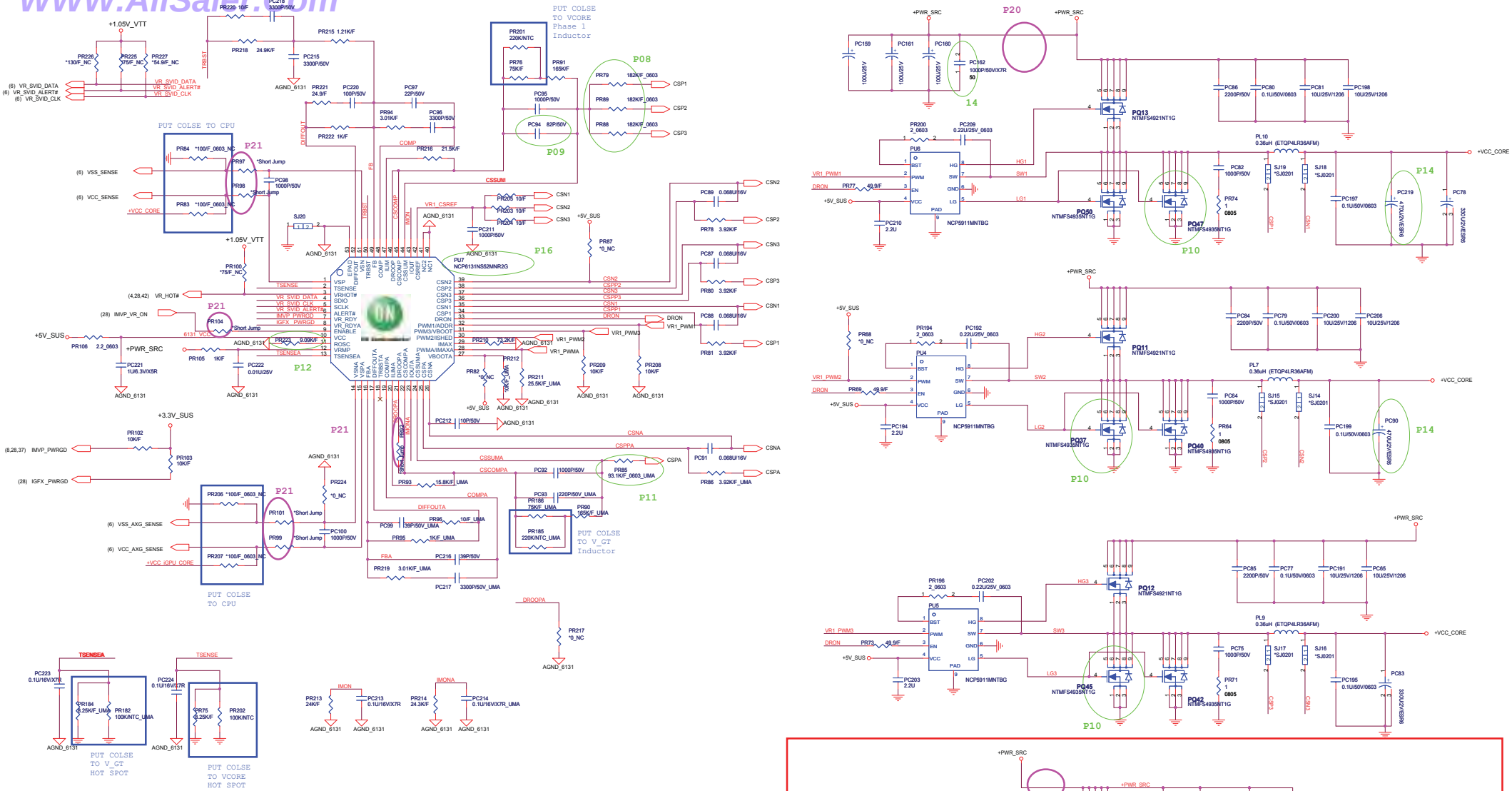
Size	Document Number	Rev
	BLANK	1A

Date: Friday, January 07, 2011 Sheet 41 of 59



Adapter type	90W	130W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	5.6A	7.6A

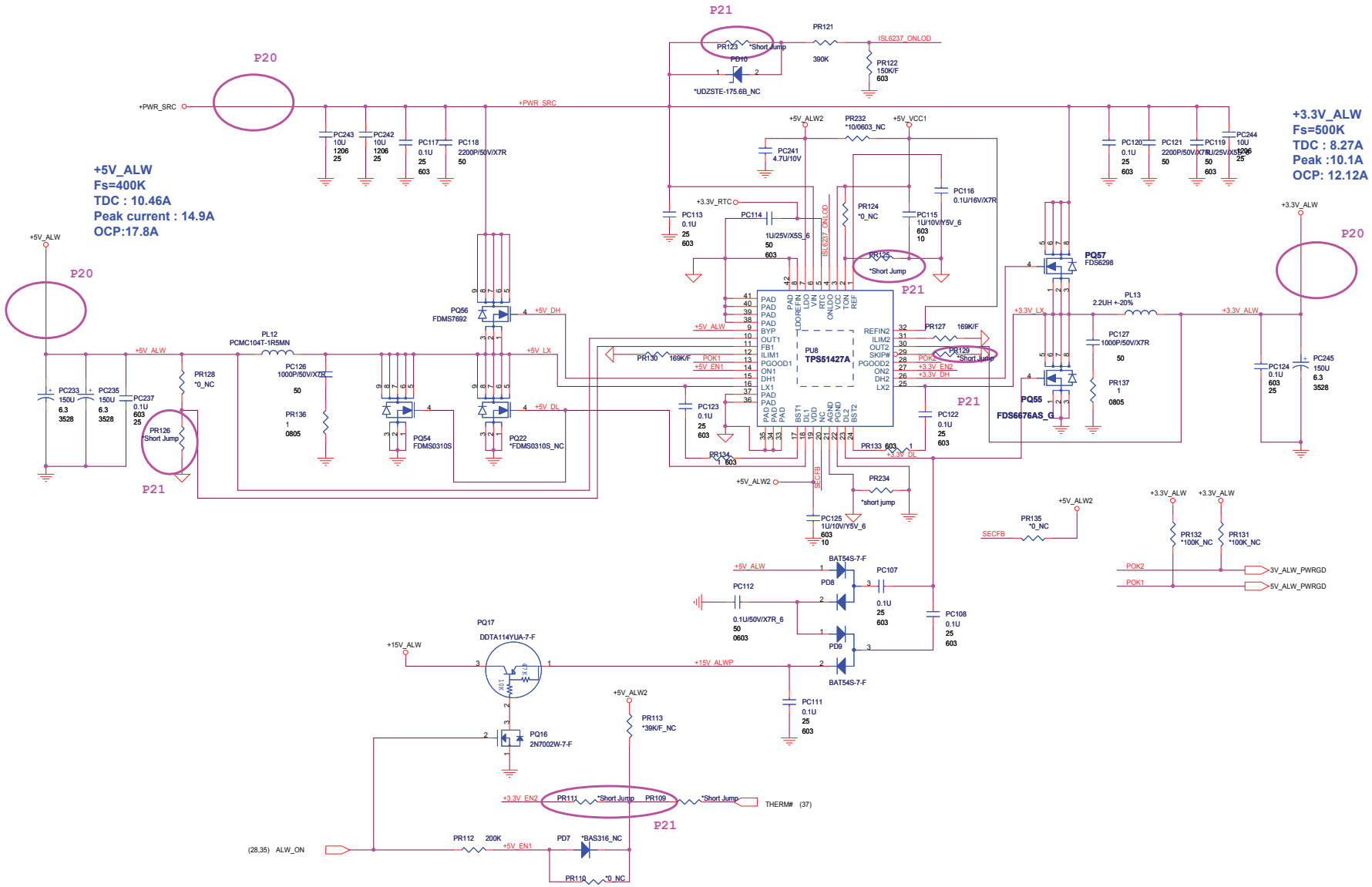
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: Charger (ISL88731) | Rev 1A
Date: Friday, January 07, 2011 Sheet 42 of 59



Reference	Discrete	UMA	Optimus
PR82	0(CS00002JB38)	NC	NC
PC91	0(CS00002JB38)	0.068U/16V(CH3683K1B09)	0.068U/16V(CH3683K1B09)
PC92	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PC212	0(CS00002JB38)	10P/50V(CH01006JB08)	10P/50V(CH01006JB08)
PR217	0(CS00002JB38)	NC	NC
PC216	0(CS00002JB38)	39P/50V(CH03906JB06)	39P/50V(CH03906JB06)
PC100	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PR224	0(CS00002JB38)	NC	NC
PR214	0(CS00002JB38)	24.3K/F(CS32432FB19)	24.3K/F(CS32432FB19)
PC223	0(CS00002JB38)	0.1U/10V(CH4102K1B03)	0.1U/10V(CH4102K1B03)

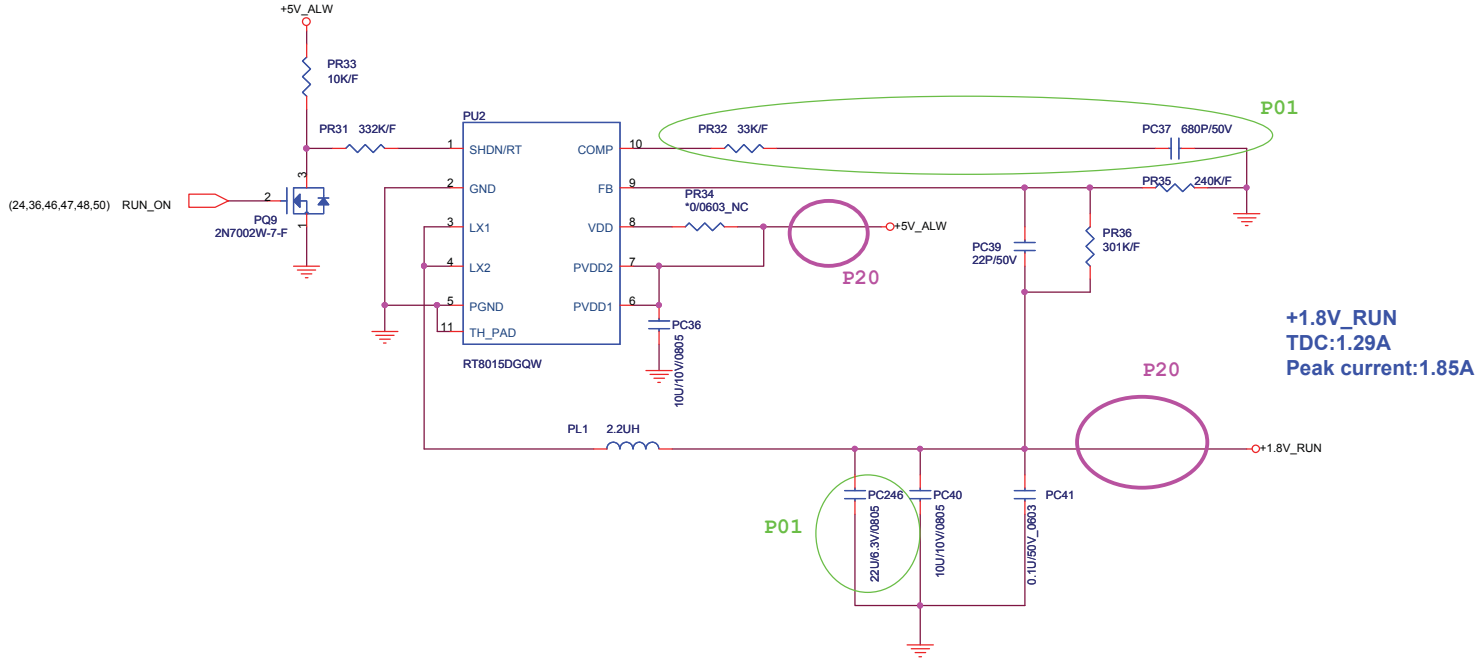
	UMA	Optimus
PC180, C612	470uF CH747RM8800	330uF CH733RM8831

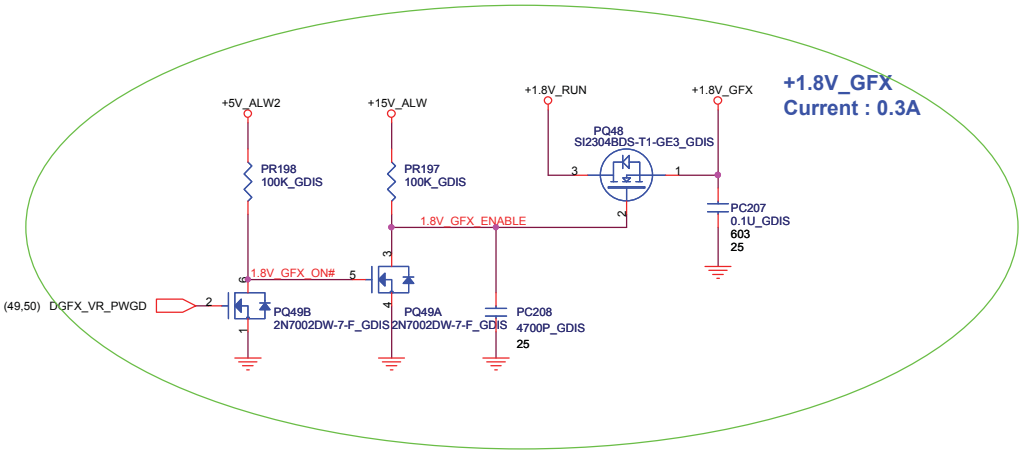
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: CPU_VCORE (NCP6131S) | Rev: 1A
Date: Friday, January 07, 2011 | Sheet 43 of 59



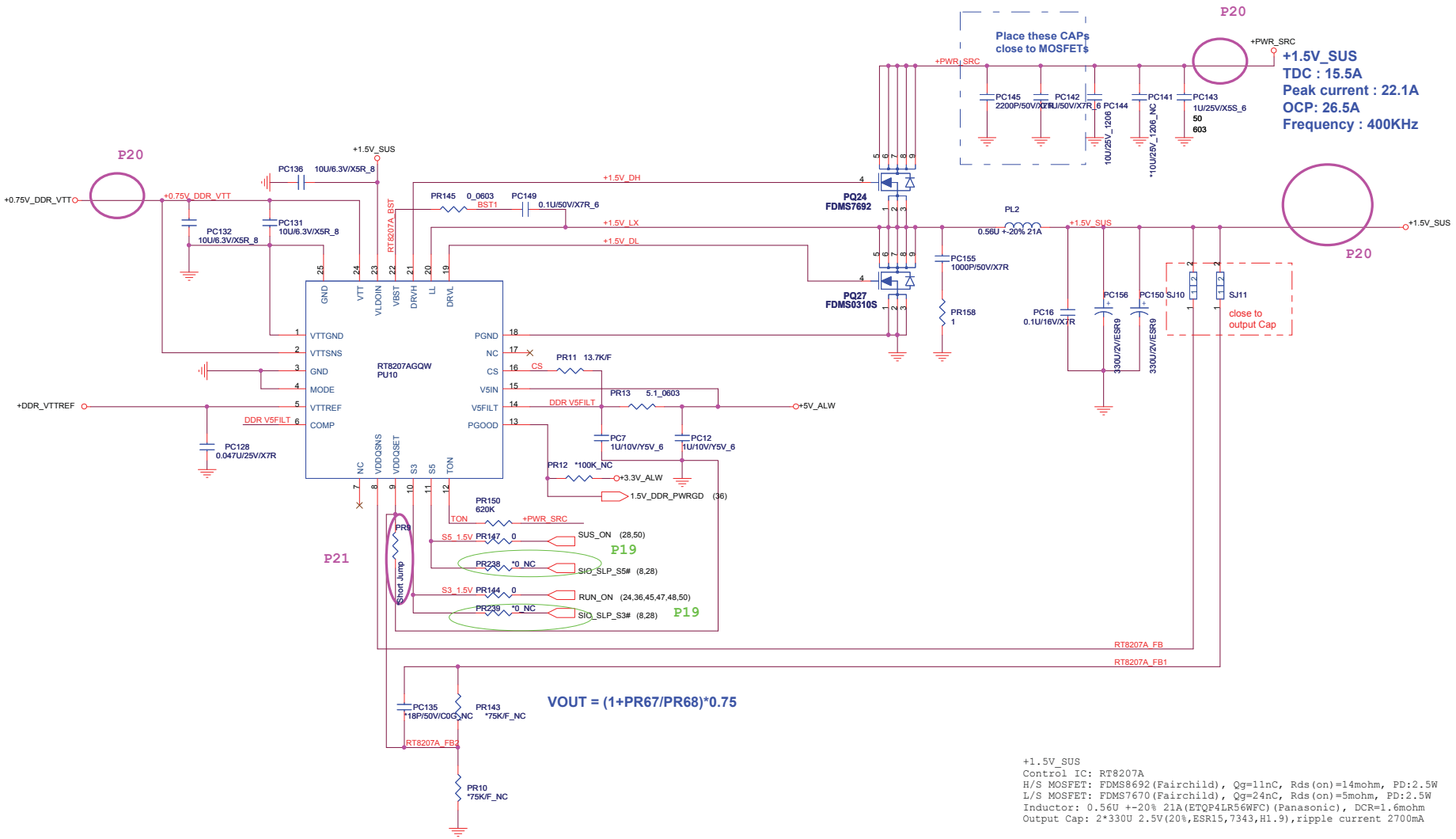
Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	3.3V_ALW / 5V_ALW(TPS51427A)	1A
Date: Friday, January 07, 2011	Sheet 44 of 59	





Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: 1.8V_RUN & 1.8V_RUN_GFX	Rev: 1A
Date: Friday, January 07, 2011	Sheet 45 of 59	



+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: 1.5V_SUS & 0.75_DDR_VTT (RT8207) | Rev 1A
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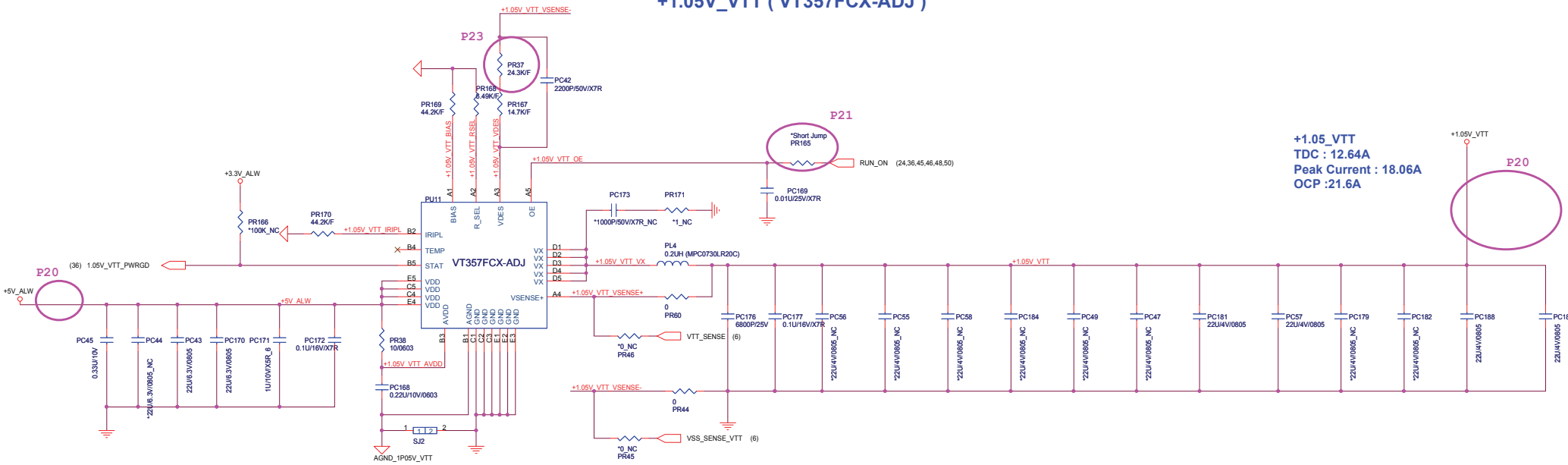
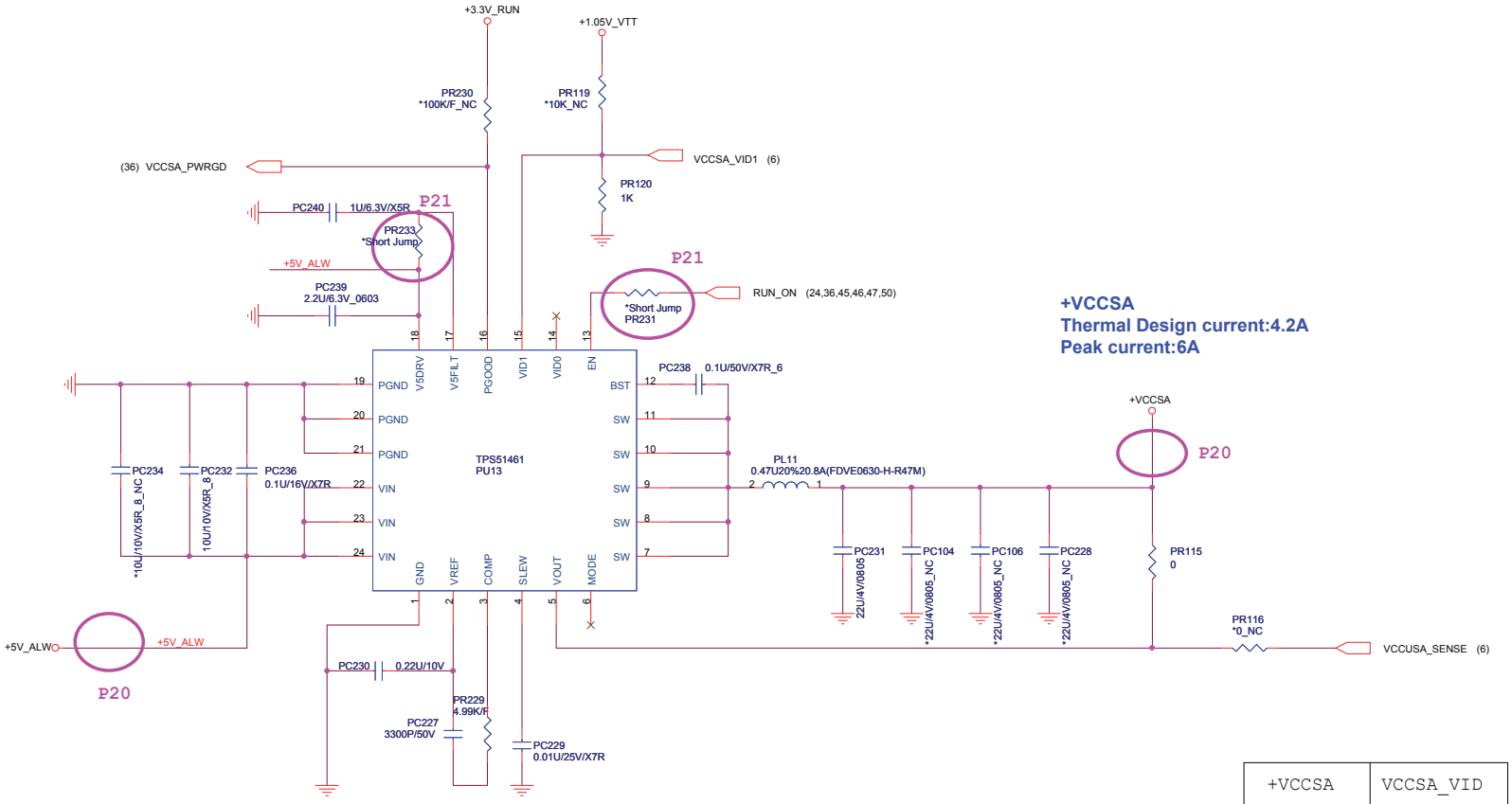
+1.05V_VTT (VT357FCX-ADJ)



Route +1.05V_VTT_VSENSE+ and +1.05V_VTT_VSENSE- as differential pair

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	1.05V_VTT	1A
Date: Friday, January 07, 2011	Sheet 47 of 59	



+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low

Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: VCCSA (TPS51461)	Rev 1A
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N12P-GE:

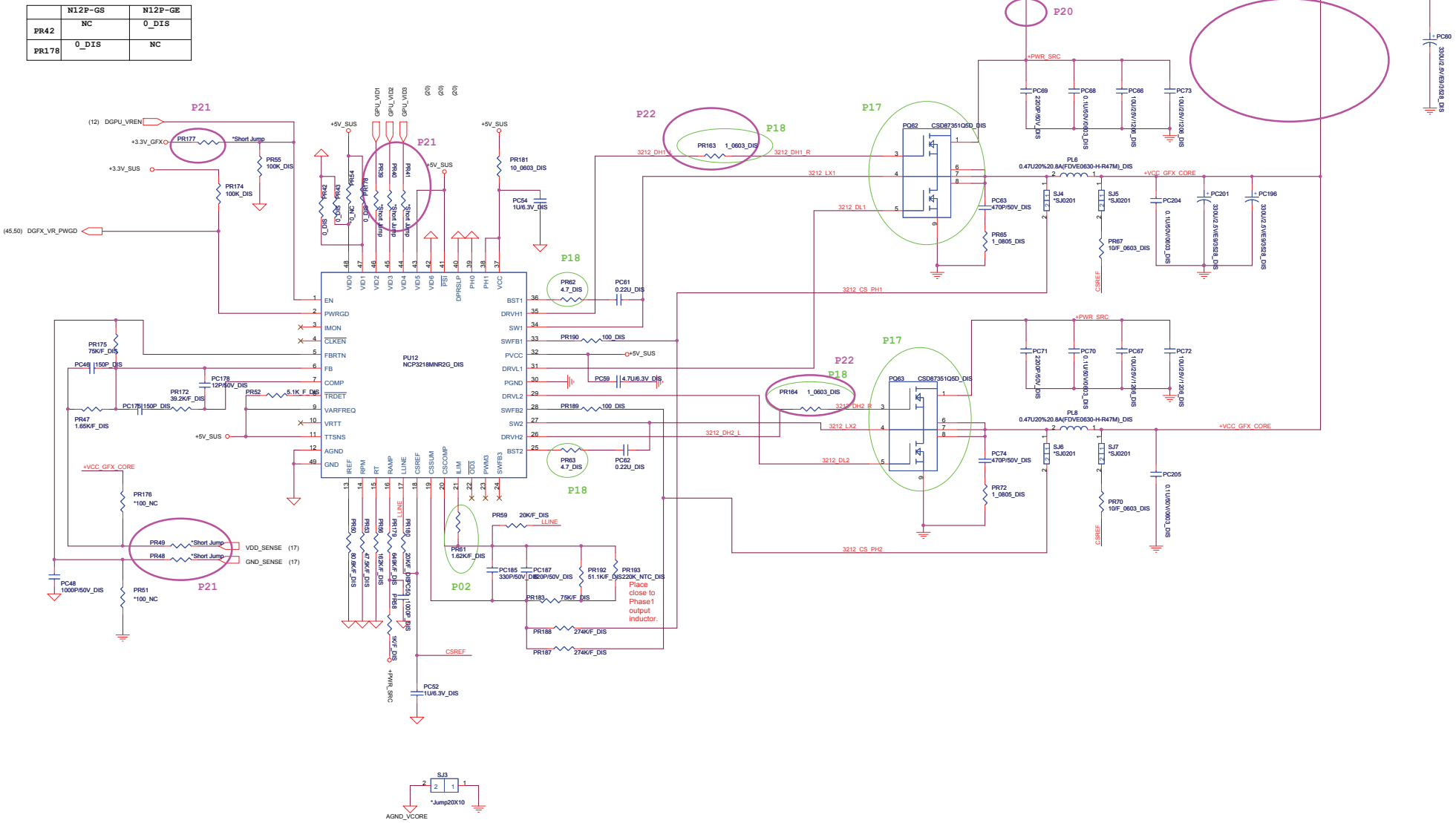
	GPU_VID3	GPU_VID2	GPU_VID1
0.85V	1	0	1
0.95V	0	1	1
1.0V	0	1	0

N12P-GS:

	GPU_VID3	GPU_VID2	GPU_VID1
0.825V	1	0	1
0.975V	0	1	0
1.0V	0	0	1

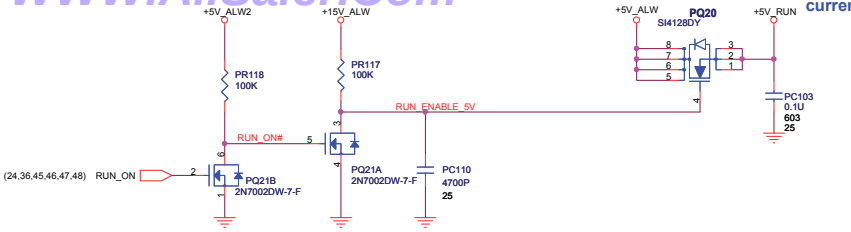
	N12P-GS	N12P-GE
PR42	NC	0_DIS
PR178	0_DIS	NC

+VCC_GFX_CORE
Fs=300K
Current:21.81A
OCP:52A

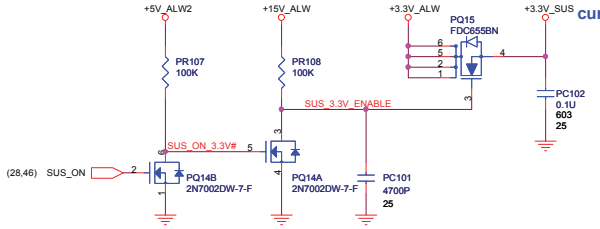


Quanta Computer Inc.	PROJECT : GM6C MLK DIS
Size	Document Number: VGA_N11P-dGFX (NCP3218MNR2G) Rev 1A
Date: Friday, January 07, 2011	Sheet 49 of 59

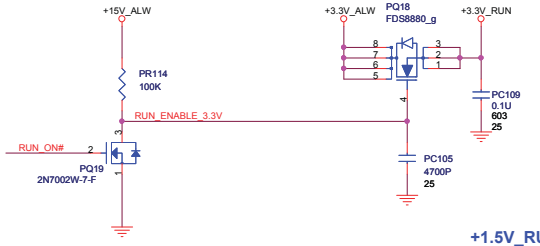
+5V_RUN
current : 2.52A



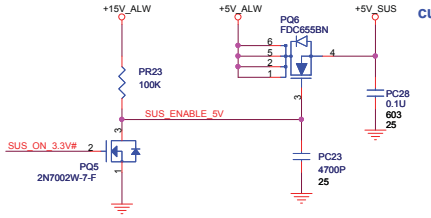
+3.3V_SUS
current : 0.35A



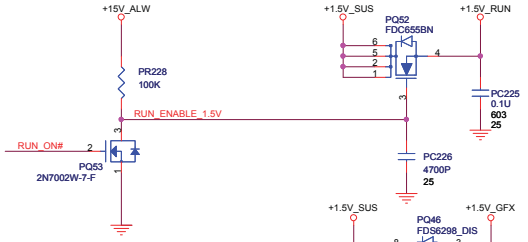
+3.3V_RUN
current : 5.12A



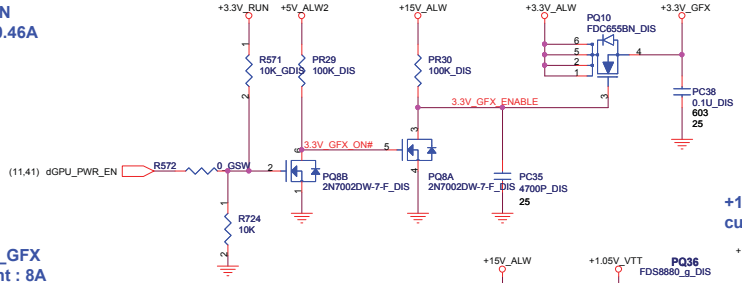
+5V_SUS
current : 2.1A



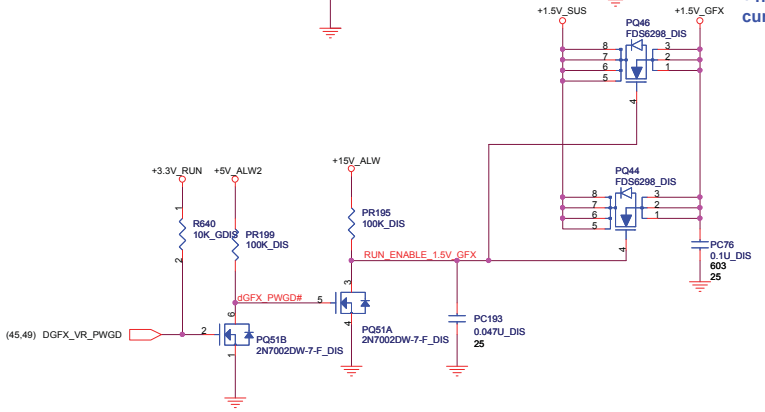
+1.5V_RUN
current : 0.46A



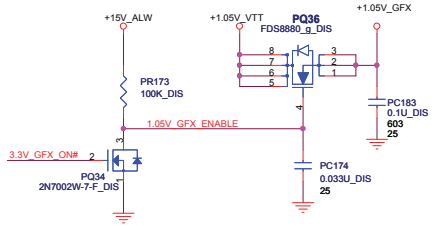
+3.3V_GFX
current: 1.38A



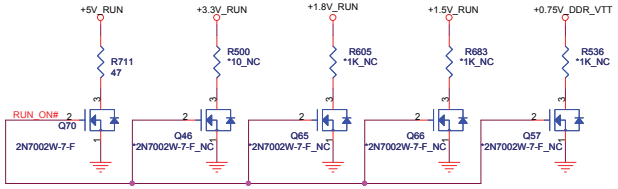
+1.5V_GFX
current : 8A

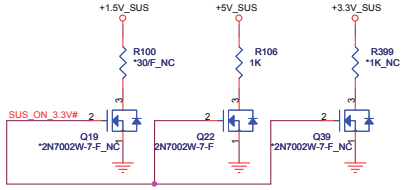


+1.05V_GFX
current : 3.83A



Reserve discharge path





Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Run Power Switch	1A
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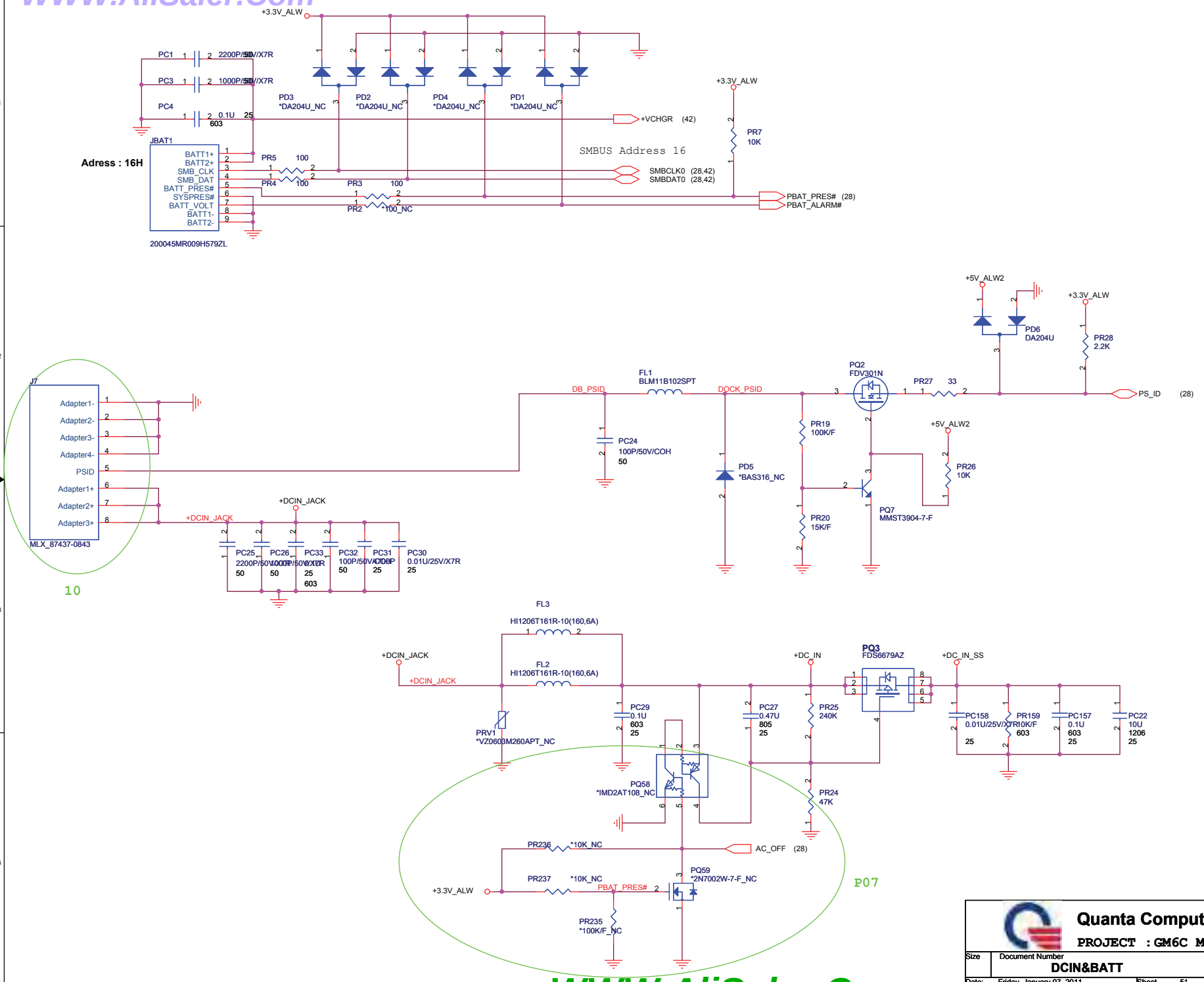
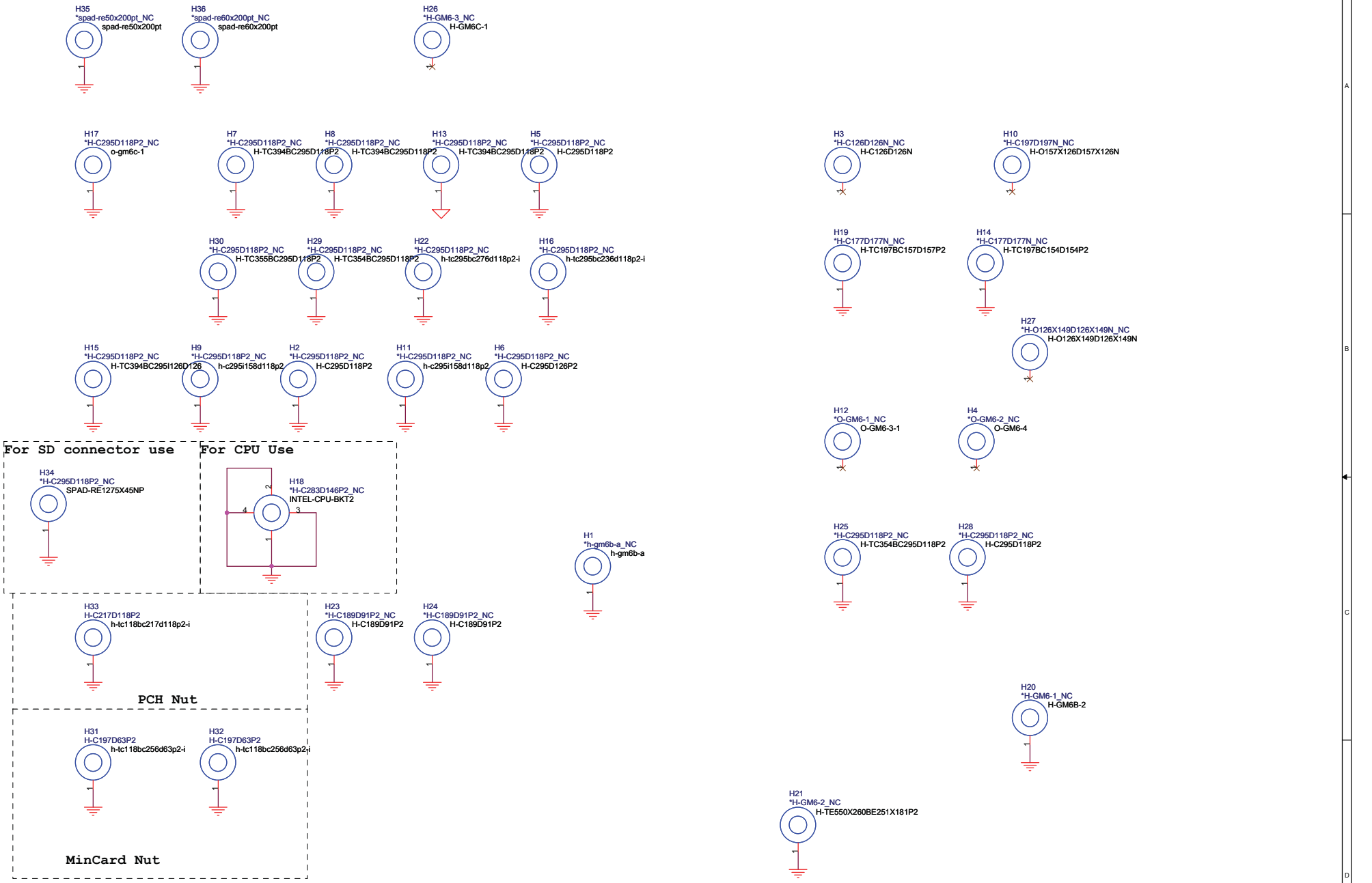
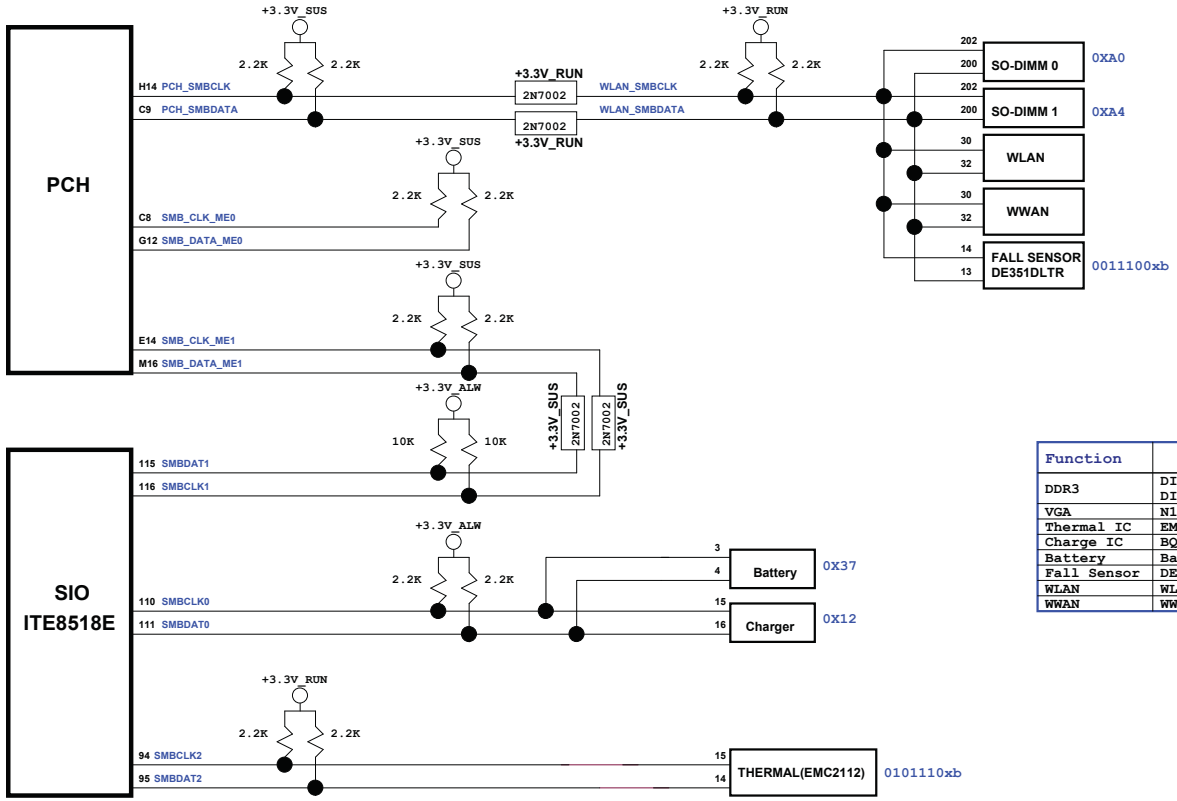


Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: DCIN&BATT	Rev: 1A
Date: Friday, January 07, 2011	Sheet 51 of 59	



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: PAD & SCREW	Rev: 1A
Date: Friday, January 07, 2011	Sheet 52 of 59	



Function	IC	SMBus Address
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC2112	0011100xb
Charge IC	BQ24765RUVR	0x12
Battery	Battery	0X37
Fall Sensor	DE351DLTR	0101110xb
WLAN	WLAN Module	X
WWAN	WWAN Module	X

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: SMBUS | Rev: 1A
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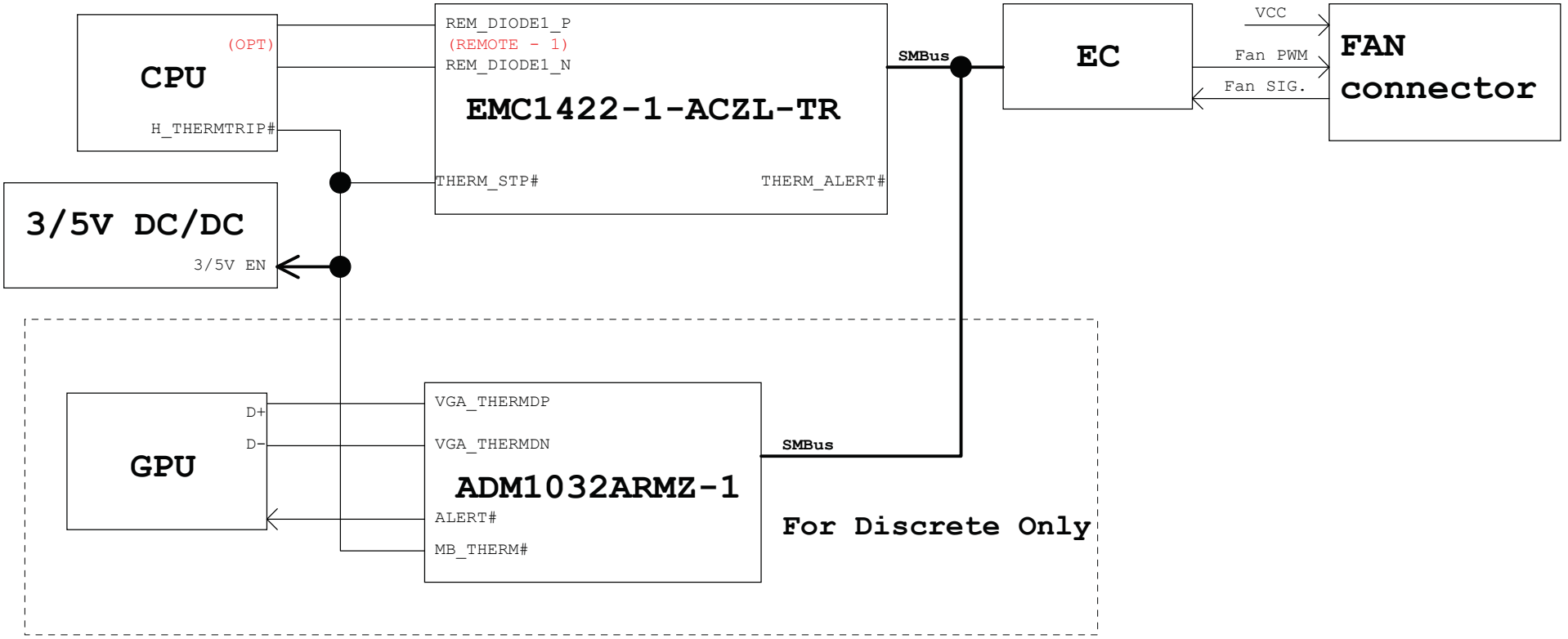

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	THERMAL MAP	1A

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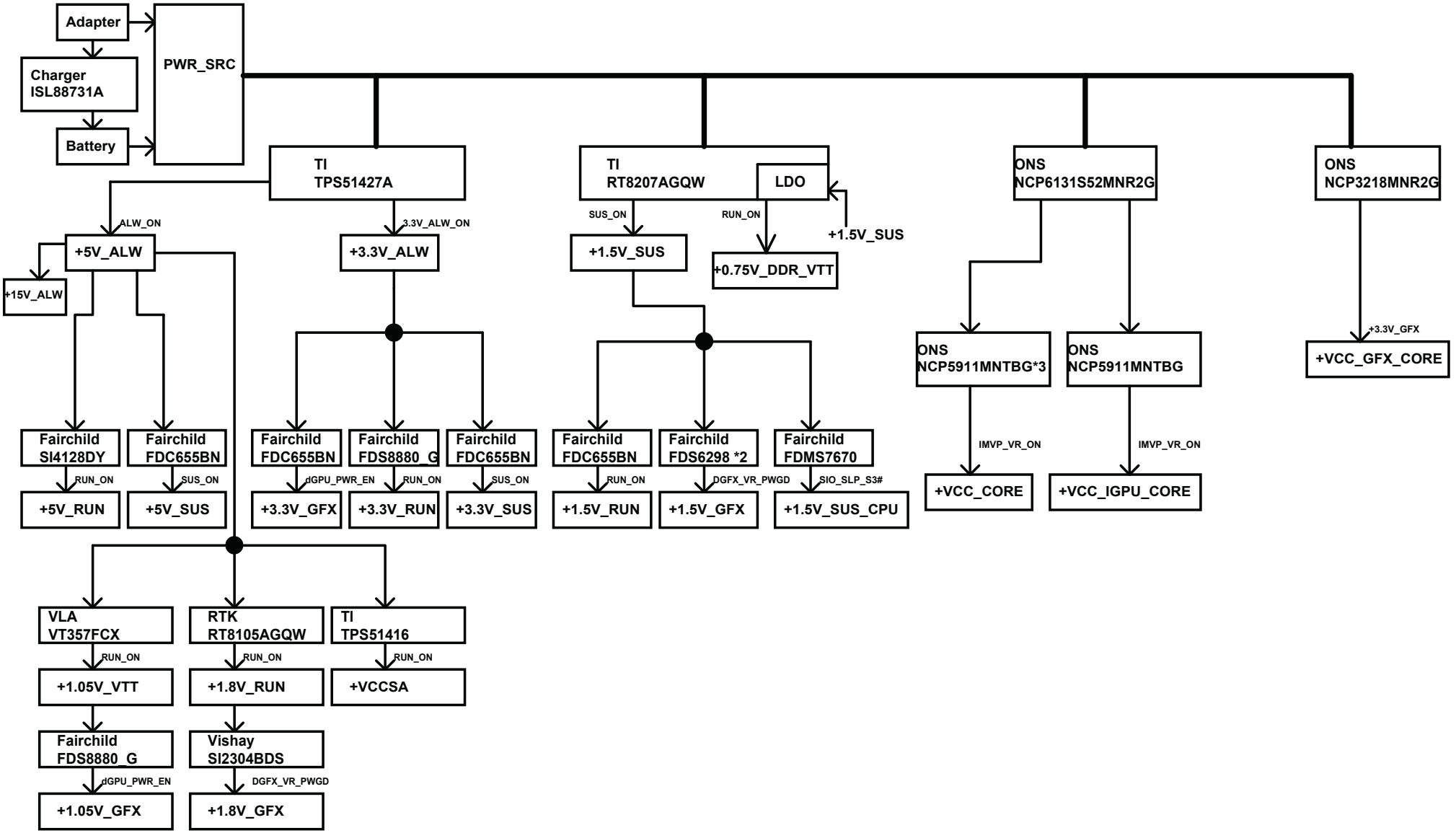
VER : 1A



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Power Block Diagram	1A

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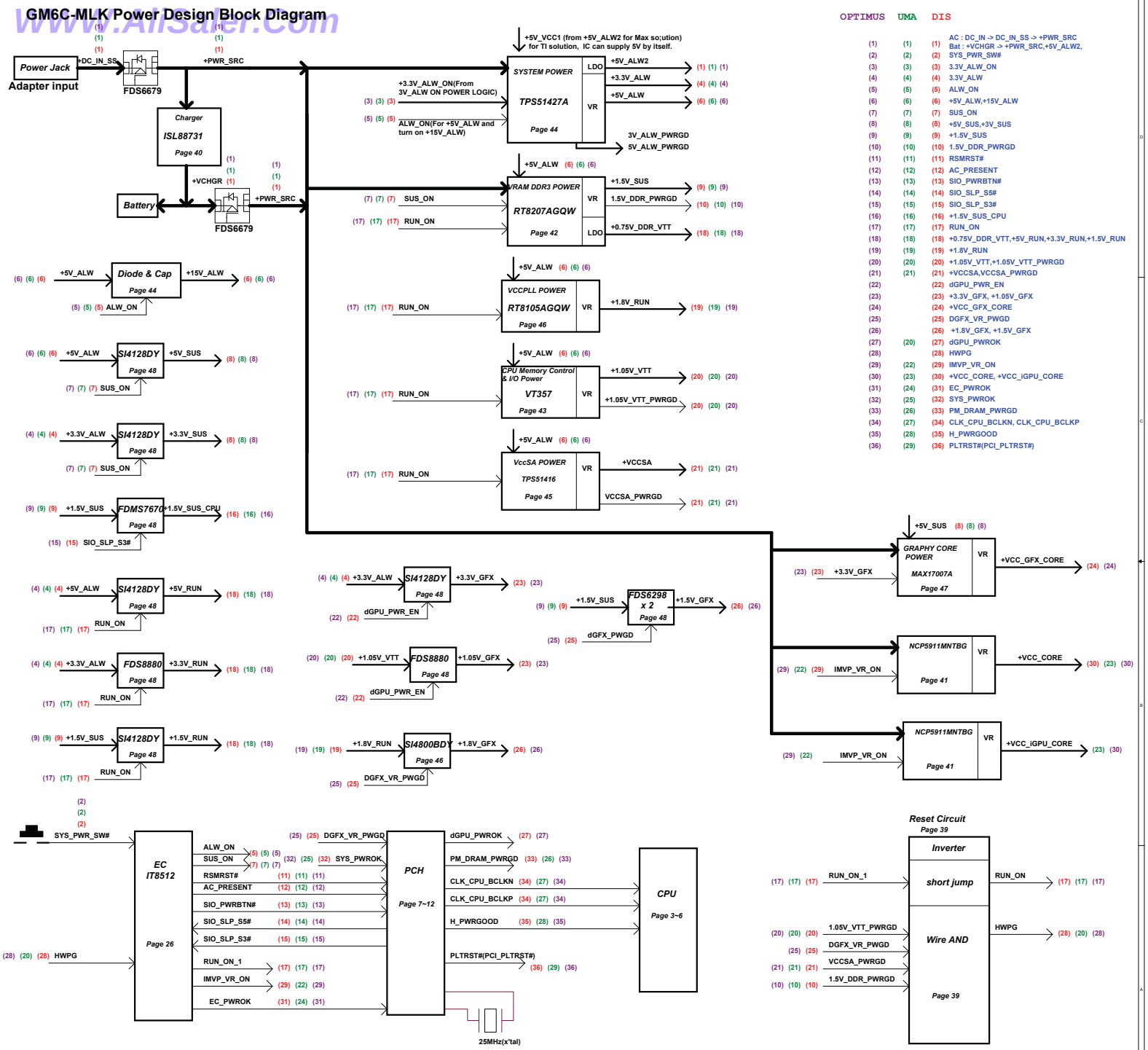
GM6C-MLK Power Design Block Diagram



OPTIMUS	UMA	DIS	
(1)	(1)	(1)	AC : DC_IN -> DC_IN_SS -> +PWR_SRC Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2)	(2)	(2)	SYS_PWR_SW#
(3)	(3)	(3)	3.3V_ALW_ON
(4)	(4)	(4)	3.3V_ALW
(5)	(5)	(5)	ALW_ON
(6)	(6)	(6)	+5V_ALW,+15V_ALW
(7)	(7)	(7)	SUS_ON
(8)	(8)	(8)	+5V_SUS,+3V_SUS
(9)	(9)	(9)	+1.5V_SUS
(10)	(10)	(10)	1.5V_DDR_PWRGD
(11)	(11)	(11)	RSMRST#
(12)	(12)	(12)	AC_PRESENT
(13)	(13)	(13)	SIO_PWRBTN#
(14)	(14)	(14)	SIO_SLP_S5#
(15)	(15)	(15)	SIO_SLP_S3#
(16)	(16)	(16)	+1.5V_SUS_CPU
(17)	(17)	(17)	RUN_ON
(18)	(18)	(18)	+0.75V_DDR_VTT,+5V_RUN,+3.3V_RUN,+1.5V_RUN
(19)	(19)	(19)	+1.8V_RUN
(20)	(20)	(20)	+1.05V_VTT,+1.05V_VTT_PWRGD
(21)	(21)	(21)	+VCCSA,VCCSA_PWRGD
(22)		(22)	dGPU_PWR_EN
(23)		(23)	+3.3V_GFX, +1.05V_GFX
(24)		(24)	+VCC_GFX_CORE
(25)		(25)	DGFX_VR_PWGD
(26)		(26)	+1.8V_GFX, +1.5V_GFX
(27)	(20)	(27)	dGPU_PWROK
(28)		(28)	HWPG
(29)	(22)	(29)	IMVP_VR_ON
(30)	(23)	(30)	+VCC_CORE, +VCC_iGPU_CORE
(31)	(24)	(31)	EC_PWROK
(32)	(25)	(32)	SYS_PWROK
(33)	(26)	(33)	PM_DRAM_PWRGD
(34)	(27)	(34)	CLK_CPU_BCLKN, CLK_CPU_BCLKP
(35)	(28)	(35)	H_PWRGOOD
(36)	(29)	(36)	PLTRST#(PCI_PLTRST#)

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Power sequence Block
Rev 1A
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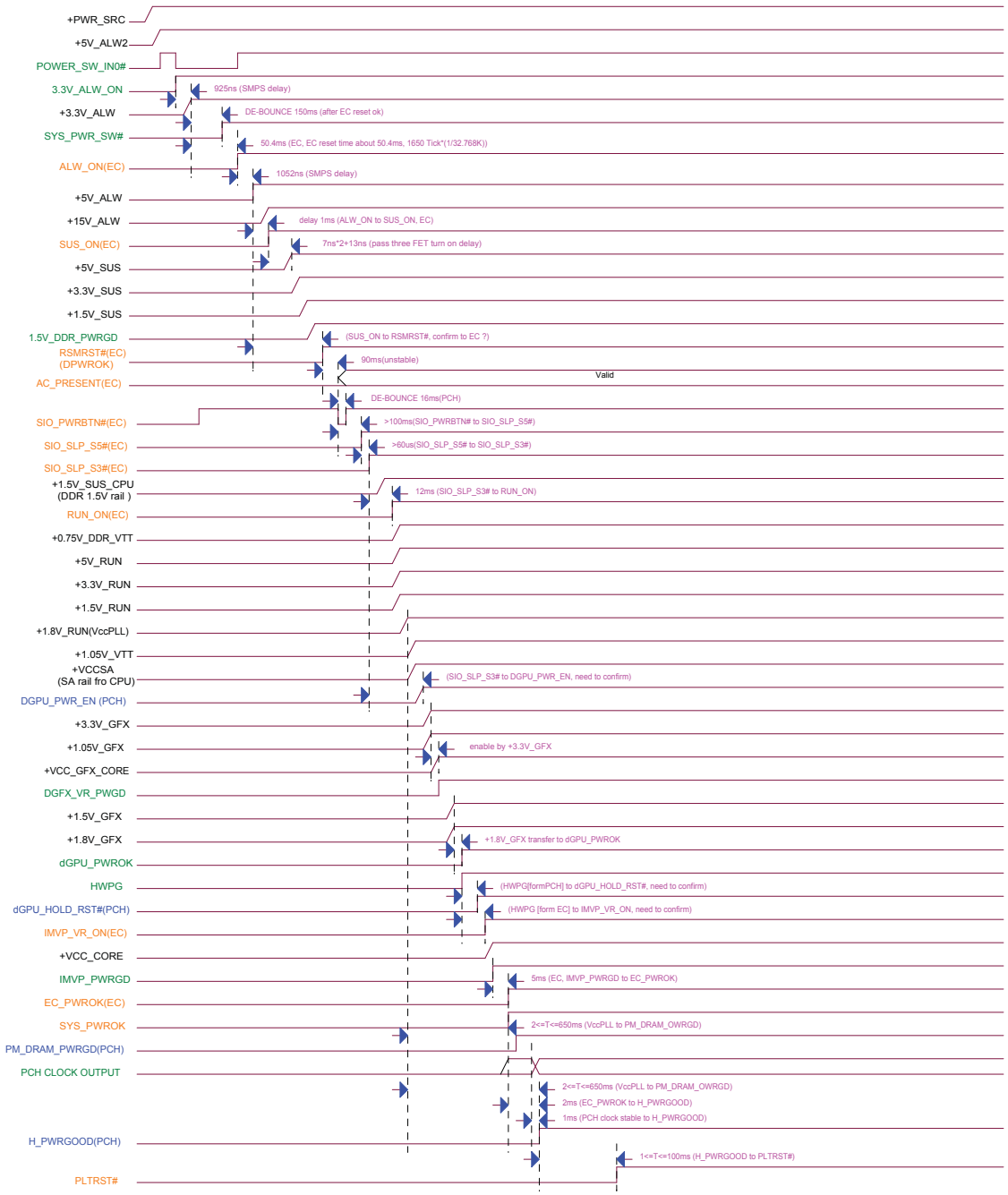
GM6C_MLK_DIS Power on Timing(BATTERY MODE)



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: POWER SEQUENCE(DIS)	Rev: 1A
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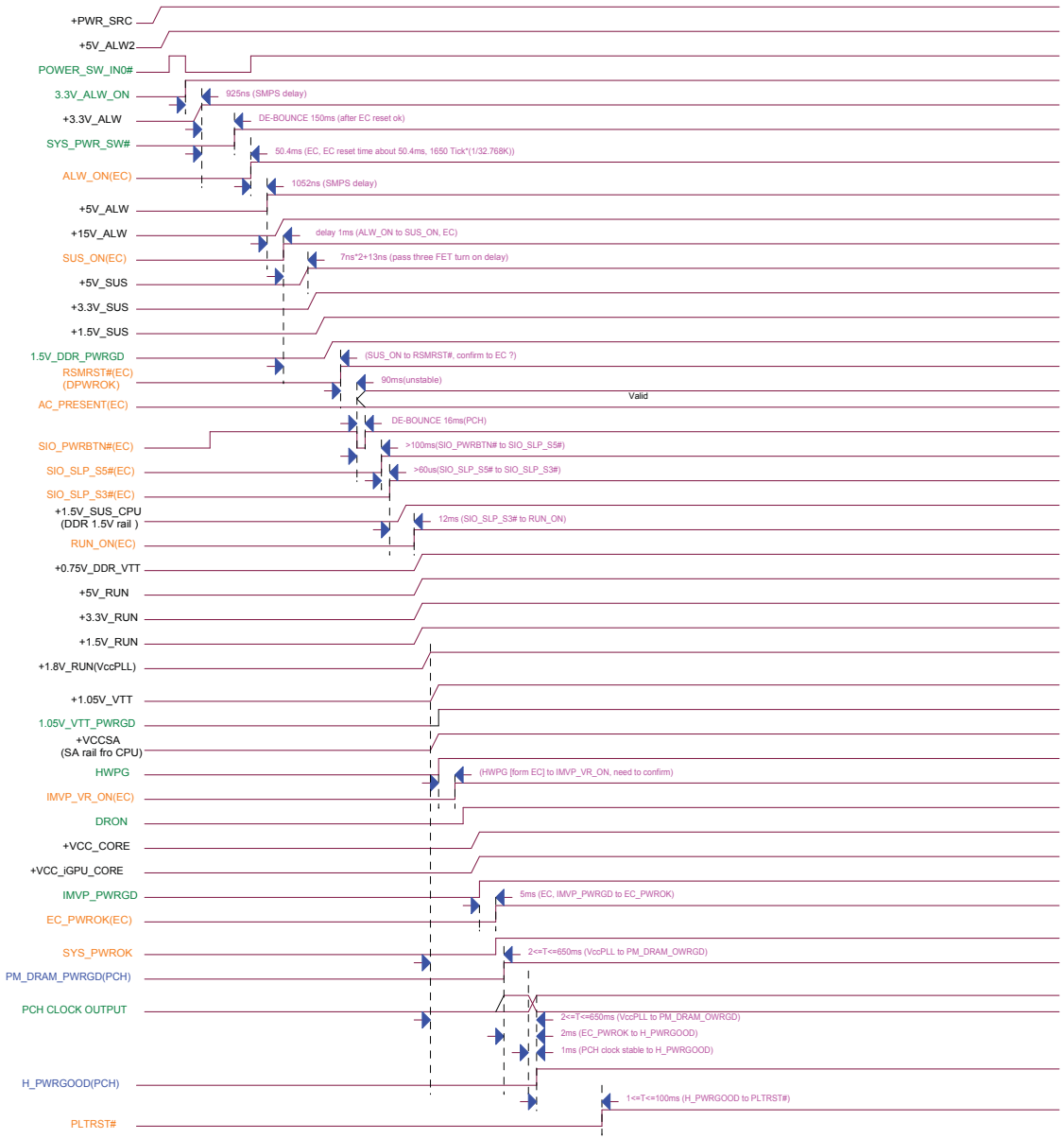
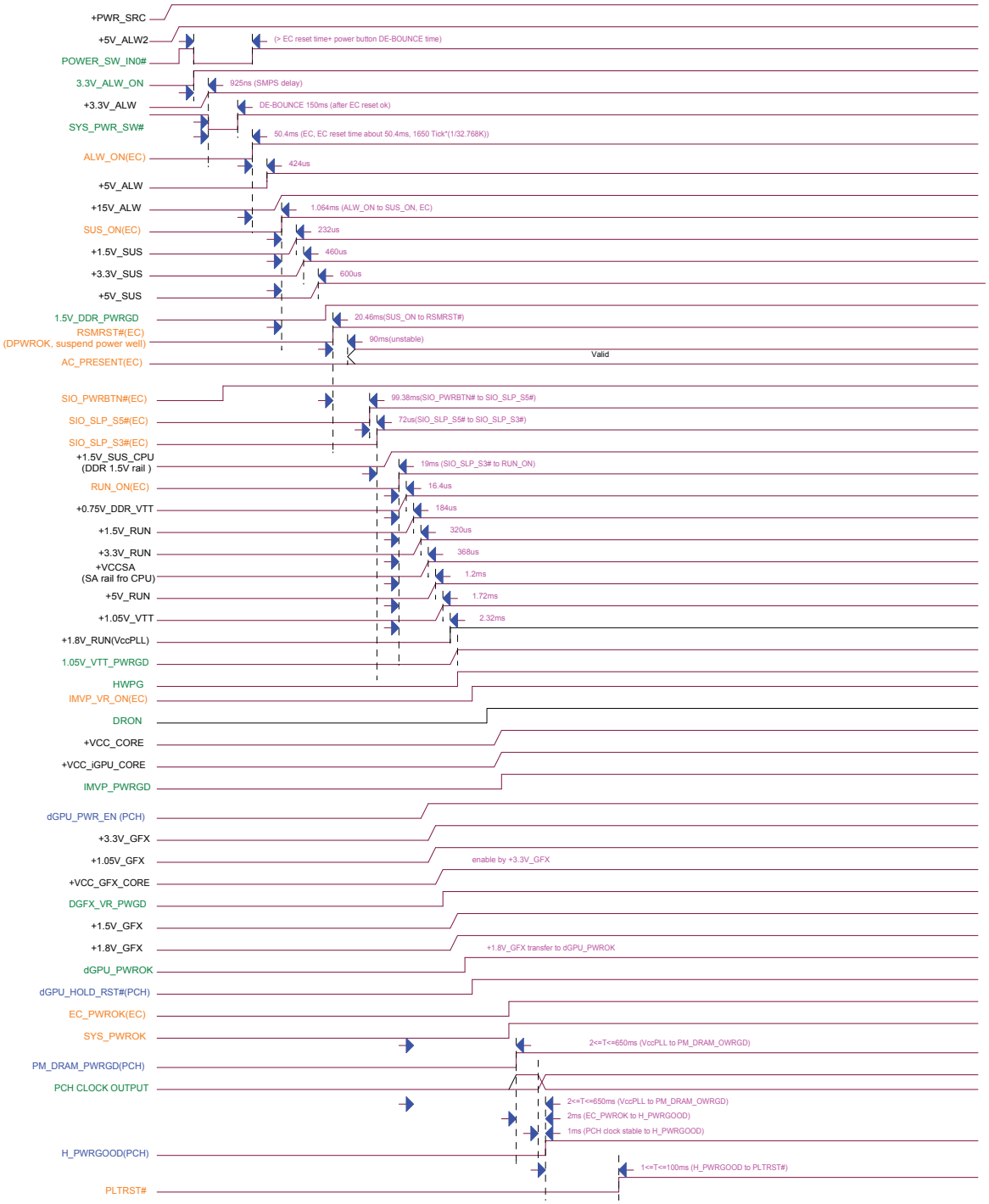
GM6C_MLK_UMA Power on Timing(BATTERY MODE)



Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: POWER SEQUENCE(UMA) | Rev: 1A
Date: Friday, January 07, 2011 | Sheet 58 of 59

GM6C_MLK_OPTIMUS Power on Timing(BATTERY MODE)



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: POWER SEQUENCE(OPTIMUS)	Rev: 1A
Date: Friday, January 07, 2011	Sheet 59 of 59	