MODEL NAME : ***AAM00***

PCB NO : ***LA-C361P***

BOM P/N :

Dell/Compal Confidential

Schematic Document

SKYLAKE-H

2014-05-22

Rev: 0.0 (M00)

@ : Nopop Component
CONN@ : Connector Component
R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB
TPM@ : TPM function
EMC@ : Pop of EMI parts
VRAMS@ : Samsung GDDR5 for GPU
VRAMH@ : Hynix GDDR5 for GPU
VRAMM@ : Micron GDDR5 for GPU
BreakDown@ : for measure power consumption
CSMB@ : CSMB sku
BC@ : BC sku (GPU N16P-Q1)
GX@ : GPU N16P-GX
UMA@ / DIS@ : UMA/DIS

PCB	*CPU*	*PCH*	*GPU*
ZZZ R1@ PCB 1BG LA-C361P REV0	UH1 R1@ MB SKL-H_BGA1440	UH2 R1@ SKY-H-PCH_BGA837	UV1 BC@ N16P-Q1-A2 UV1 GX@ N16P-GX-A2

Samsung 2G

RV312 20K_0402_1% VRAMS@

UV5 K4G41325FC-HC03_FBGA170P~D VRAMS@
UV6 K4G41325FC-HC03_FBGA170P~D VRAMS@
UV9 K4G41325FC-HC03_FBGA170P~D VRAMS@
UV10 K4G41325FC-HC03_FBGA170P~D VRAMS@

Hynix 2G

RV312 34.8K_0402_1% VRAMH@

UV5 H5GC4H24AJR-R0C_FBGA170P~D VRAMH@
UV6 H5GC4H24AJR-R0C_FBGA170P~D VRAMH@
UV9 H5GC4H24AJR-R0C_FBGA170P~D VRAMH@
UV10 H5GC4H24AJR-R0C_FBGA170P~D VRAMH@

Micron 2G

RV312 24.9K_0402_1% VRAMM@

UV5 EDW4032BABG-60-F_FBGA170P~D VRAMM@
UV6 EDW4032BABG-60-F_FBGA170P~D VRAMM@
UV9 EDW4032BABG-60-F_FBGA170P~D VRAMM@
UV10 EDW4032BABG-60-F_FBGA170P~D VRAMM@

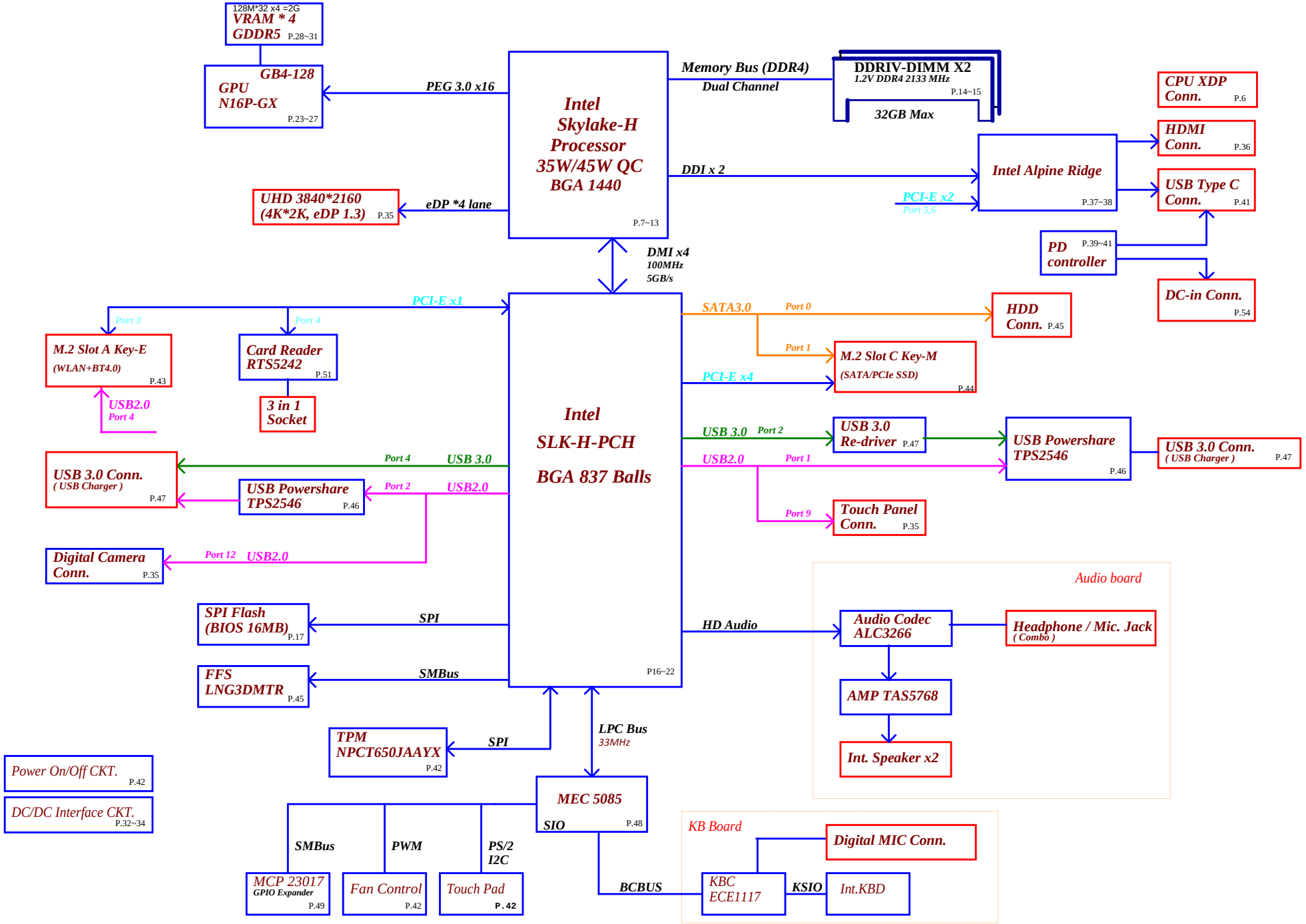
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: ***Cover Page***

Size: | Document Number: ***LA-C361P*** | Rev: 0.1(M00)

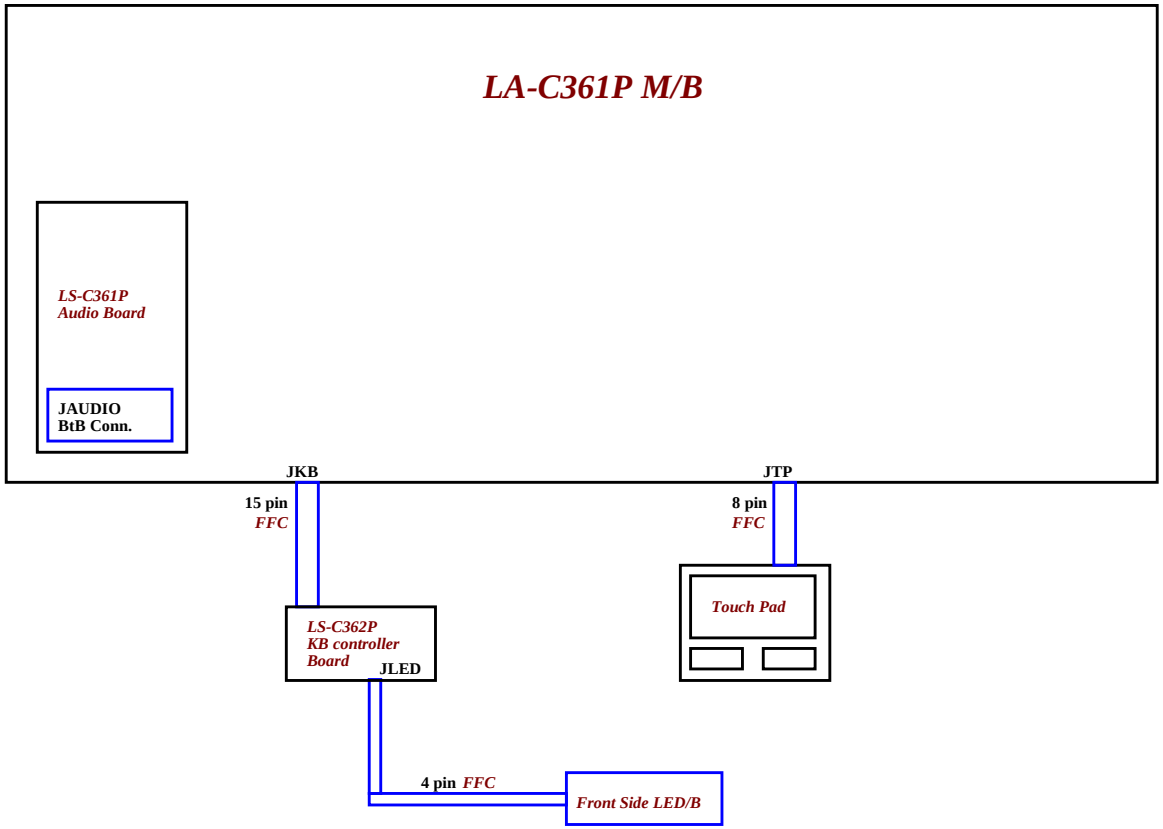
Date: Thursday, August 06, 2015 | Sheet 1 of 71



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2011/08/25	Title: Block diagram
Size	Document Number: LA-C361P		Rev: 0.1(000)
Date: Thursday, August 06, 2015	Sheet 2 of 71		

Compal Confidential

Project Code : AAM00
File Name :



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title	DB block diagram		
Size	Document Number		Rev 0.1(000)
Date: Thursday, August 06, 2015		Sheet 3 of 71	

Board ID	Resistor
X00	N/A
X01	
X02	
X03	
A00	

USB3	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	None
8	None
9	Touch screen
10	None
11	None
12	CAMERA

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	None

LPC	DESTINATION
LPC0	MEC5085
LPC1	DEBUG PORT

PCI EXPRESS	DESTINATION
Lane 1	NGFF-1 WLAN + BT
Lane 2	CARD READER
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None
Lane 9	SSD
Lane 10	SSD
Lane 11	SSD
Lane 12	SSD
Lane 13	None
Lane 14	None
Lane 15	Alpine Ridge
Lane 16	Alpine Ridge

USB3	DESTINATION
7	None
8	None
9	None
10	None

SATA	DESTINATION
0A	SSD
1A	N/A
N/A	N/A
N/A	N/A
0B	None
1B	HDD
2	None
3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

Symbol Note :

: means Digital Ground : means Analog Ground

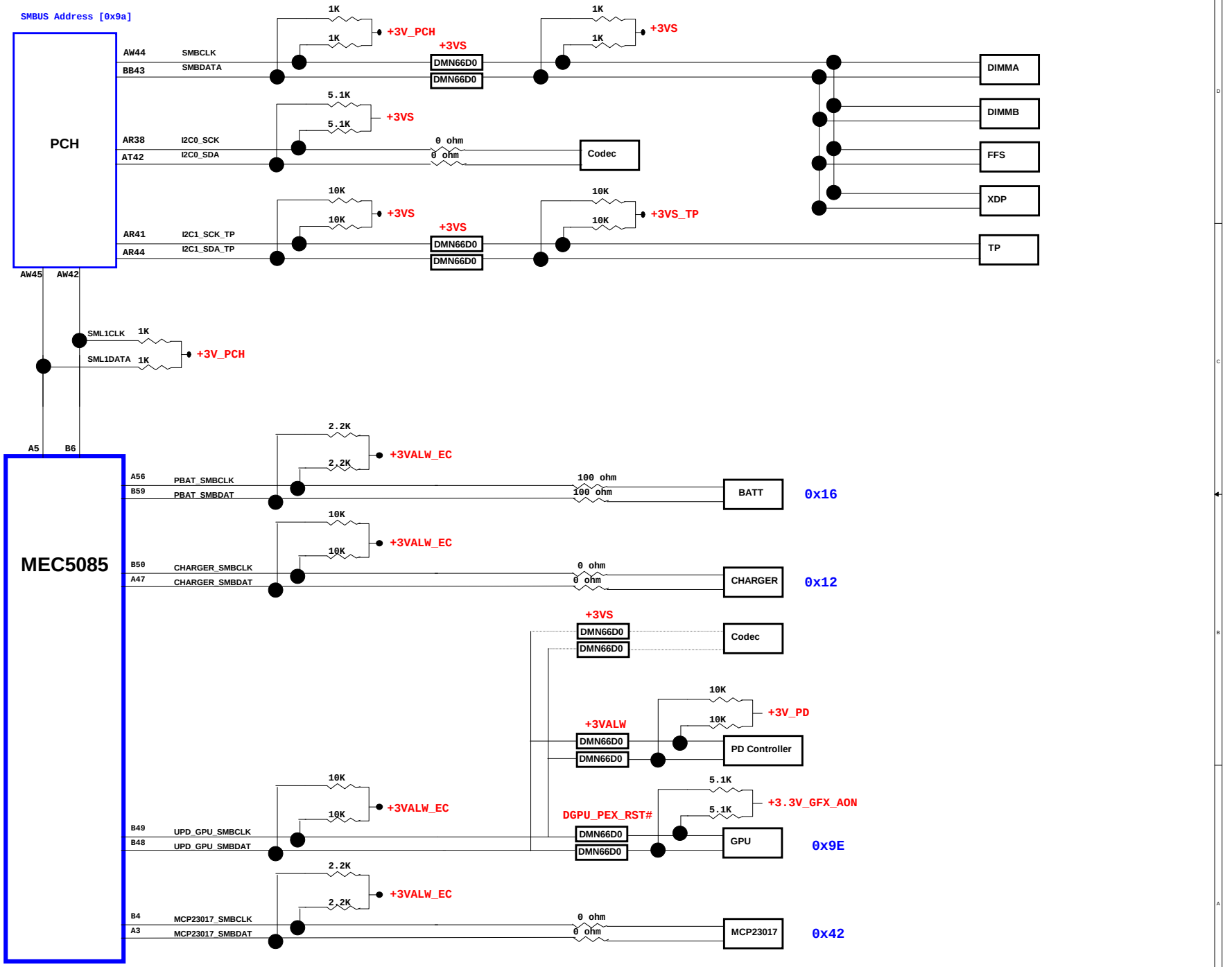
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: Notes List

Size | Document Number: LA-C361P | Rev: 0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 4 of 71



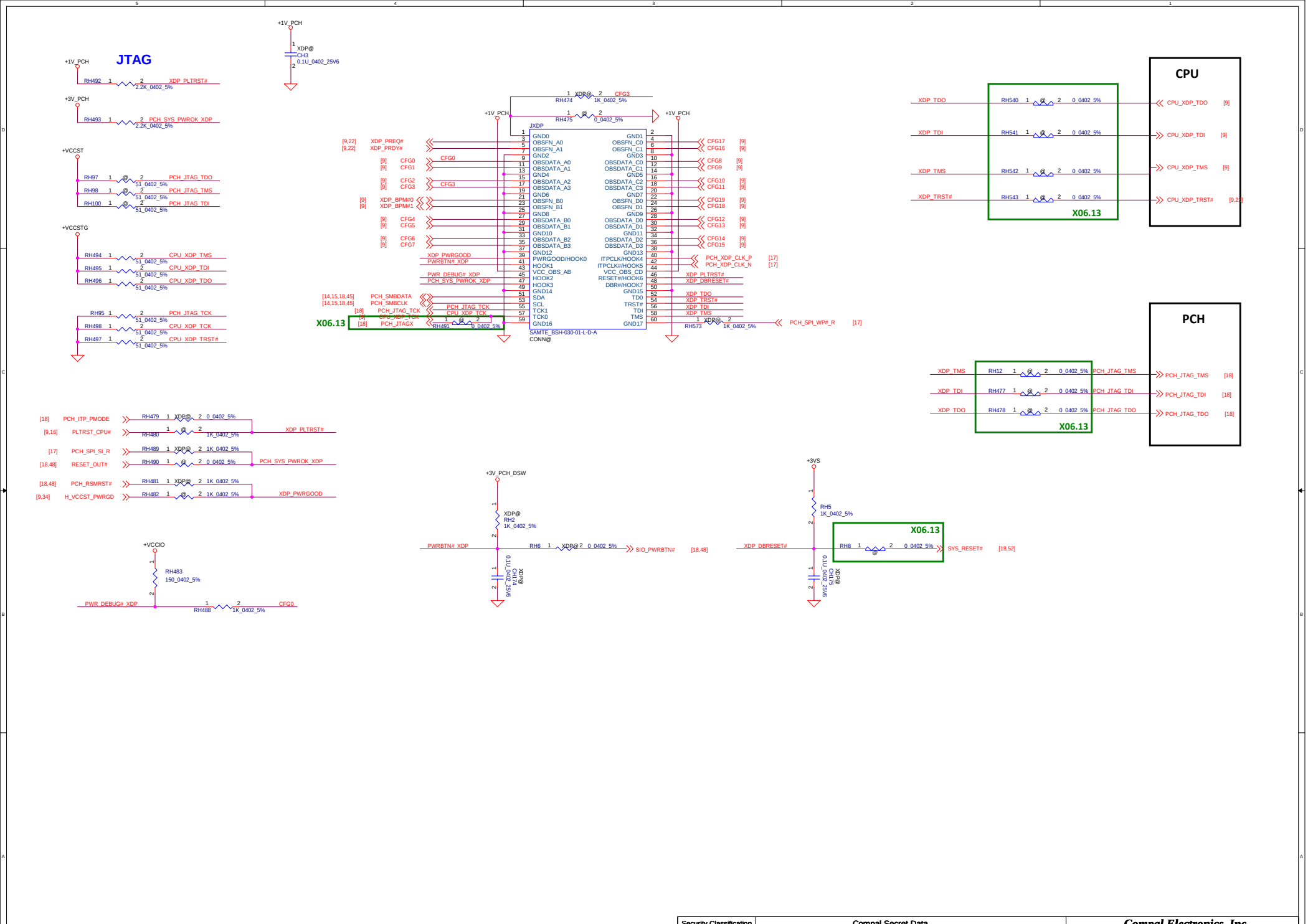
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: SMBus Block Diagram

Size	Document Number	Rev
Custom		0.1(X00)

Date: Thursday, August 06, 2015 Sheet 5 of 71



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: XDP CONN

Size	Document Number	Rev
		0.1(000)

Date: Thursday, August 06, 2015 Sheet 6 of 71

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

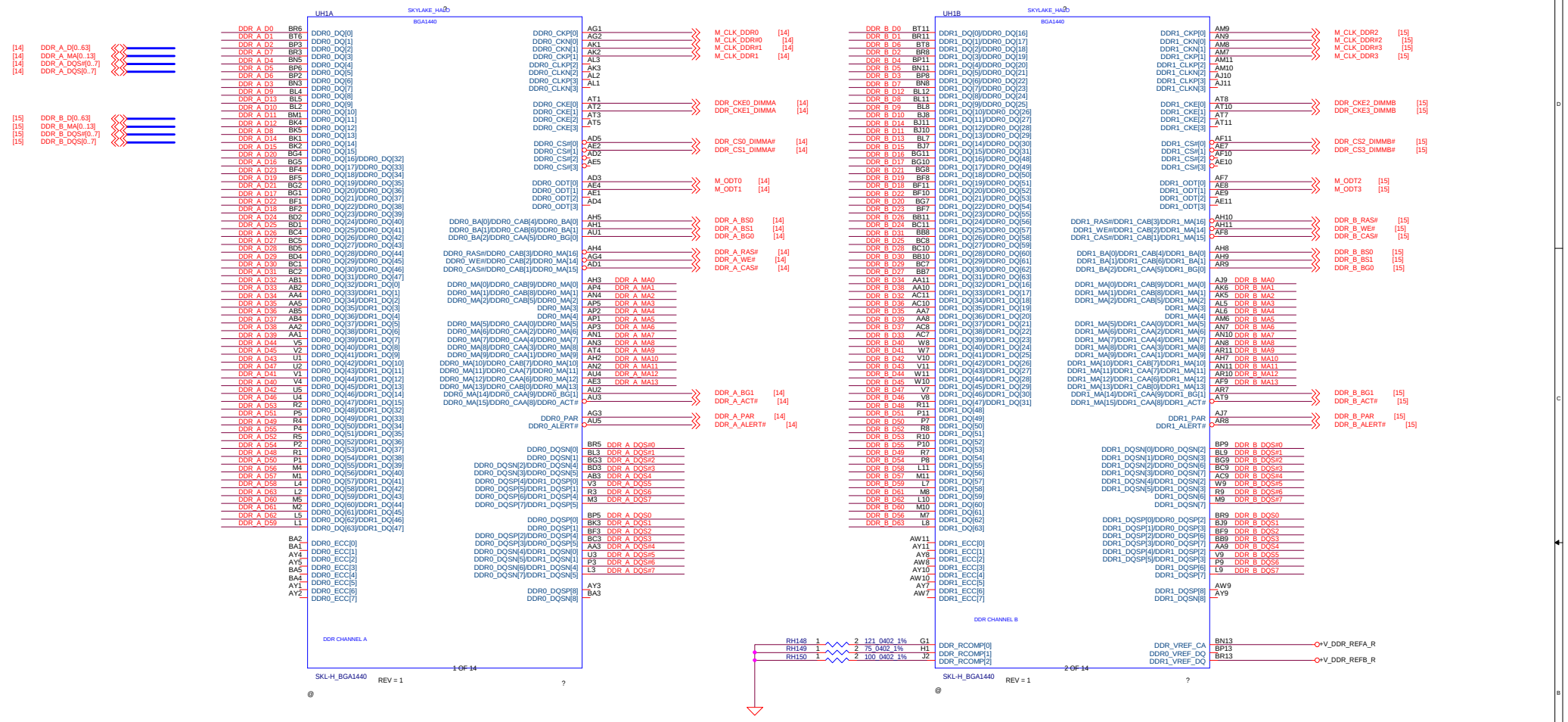
Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
C		0.1(000)

Date: Thursday, August 06, 2015 | Sheet 7 of 71

Interleave



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **PROCESSOR(3/7) DDRIII**

Size	Document Number	Rev
C		0.1(000)

Date: Thursday, August 06, 2015 | Sheet 8 of 71

CFG Straps for Processor

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

CFG0 — RH183 1K_0402_5%

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

CFG2 — RH184 1K_0402_5%

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

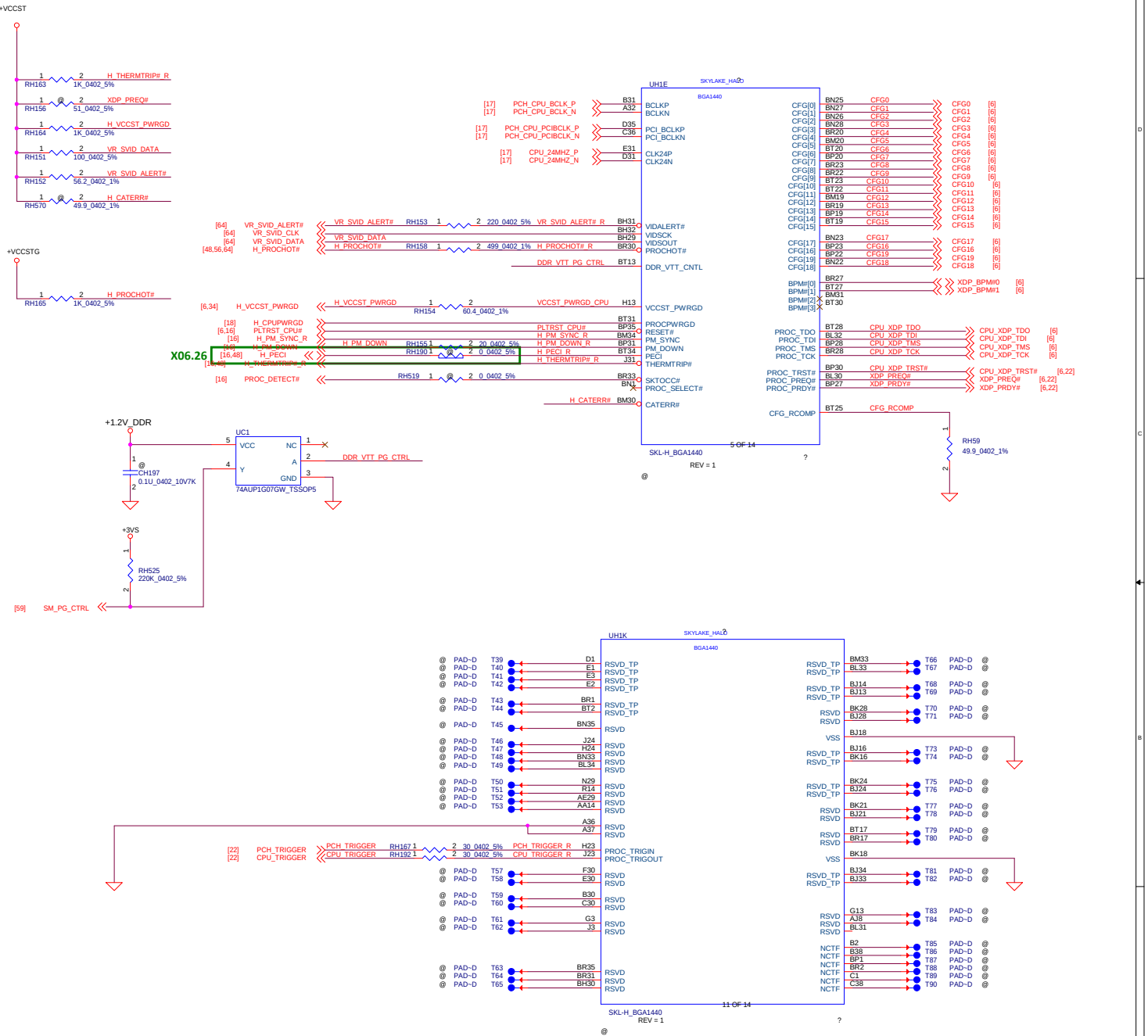
CFG4 — RH185 1K_0402_5%

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

CFG5 — RH186 1K_0402_5%
CFG6 — RH187 1K_0402_5%

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG7 — RH188 1K_0402_5%



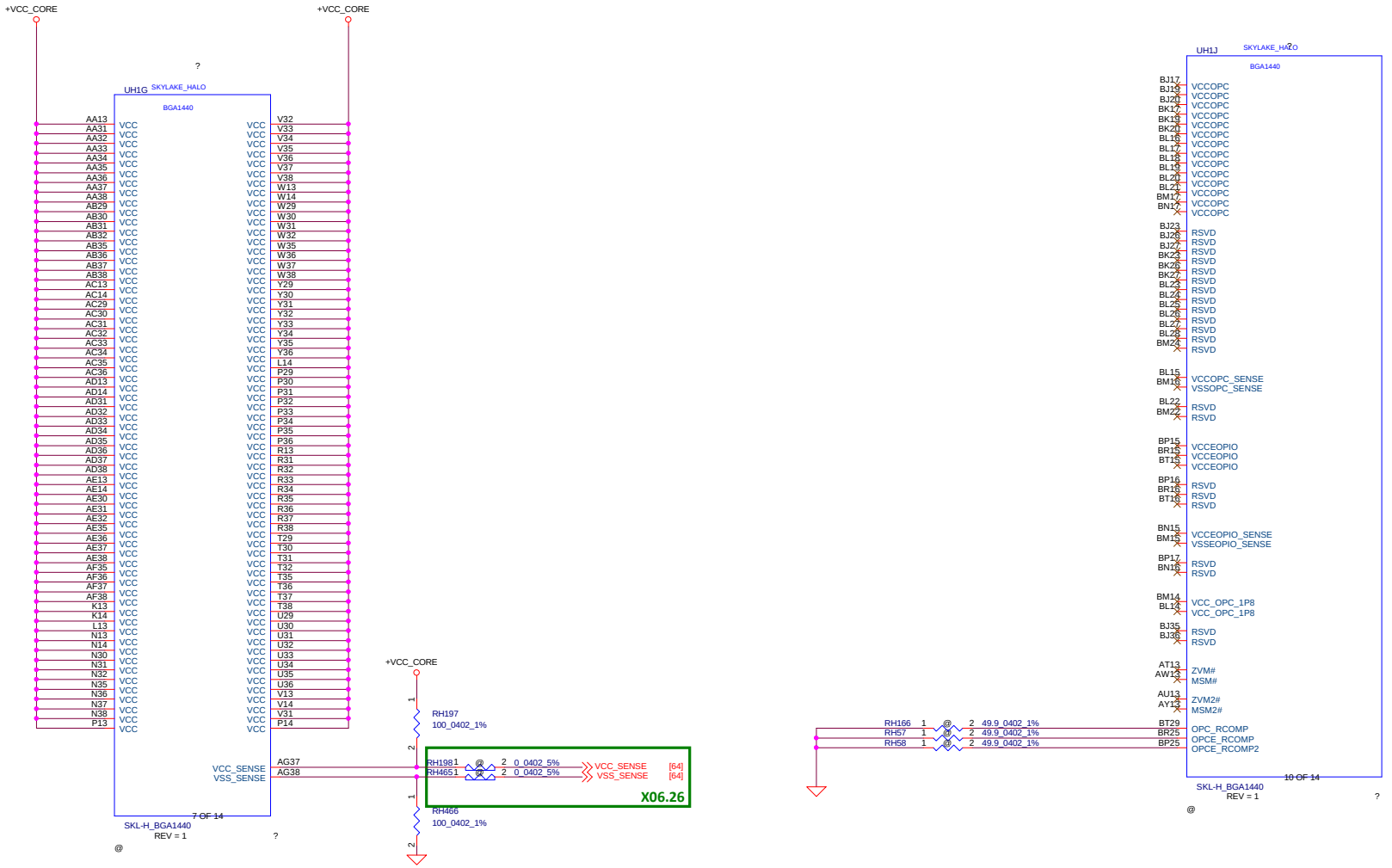
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
C		0.1(000)

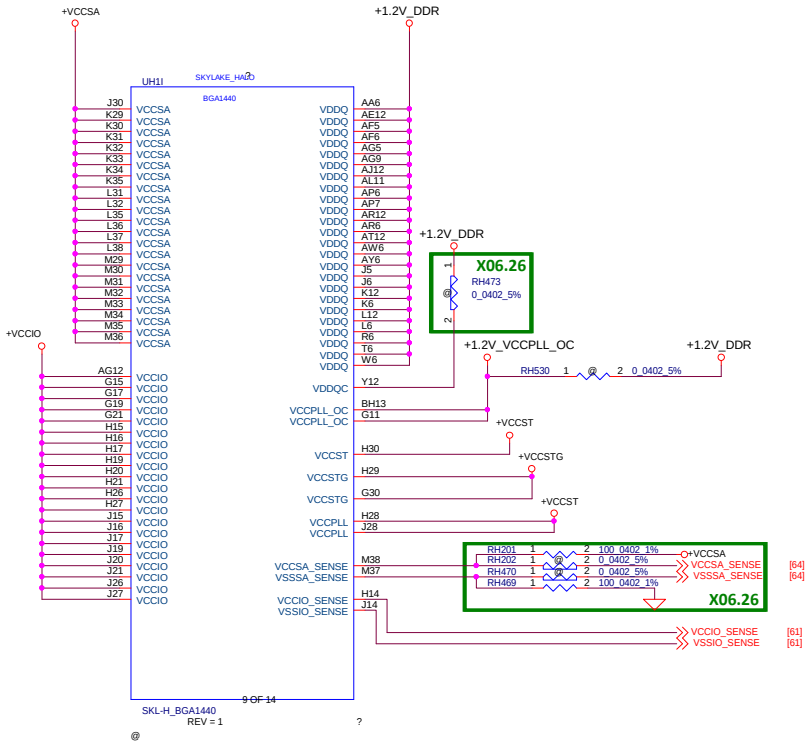
Date: Thursday, August 06, 2015 Sheet 9 of 71

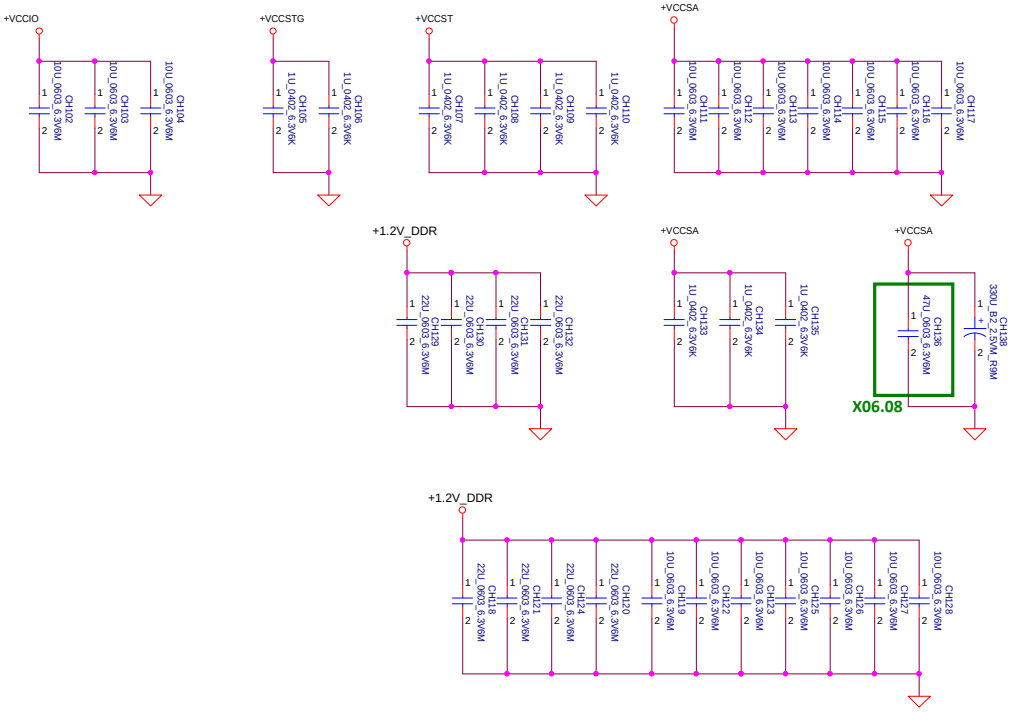


Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **PROCESSOR(5/7) PWR,BYPASS**

Size: Custom	Document Number	Rev: 0.1(X00)
Date: Thursday, August 06, 2015	Sheet 10 of 71	





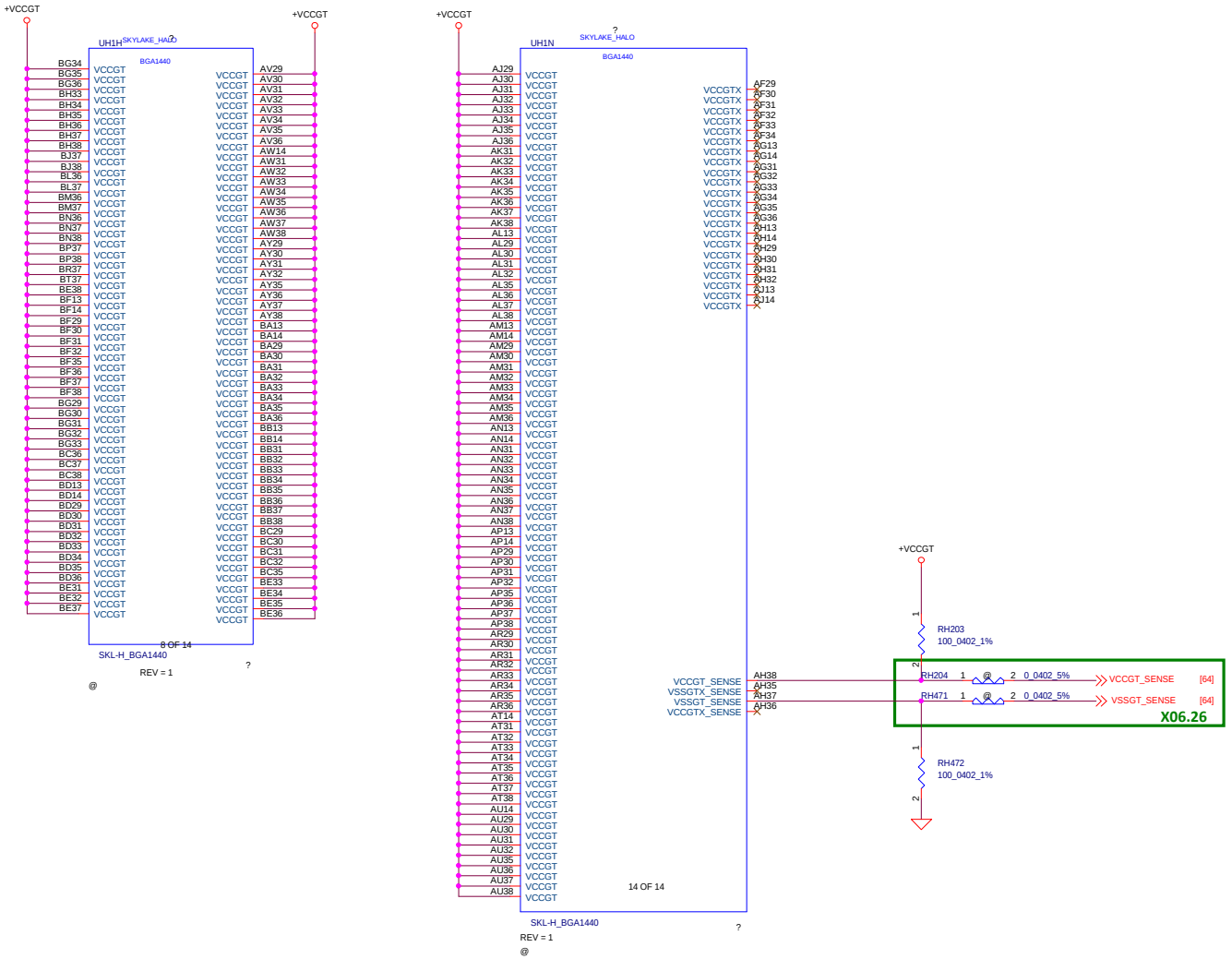
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PROCESSOR(6/7) PWR**

Size	Document Number	Rev
Custom		0.1(X00)

Date: Thursday, August 06, 2015 | Sheet 11 of 71



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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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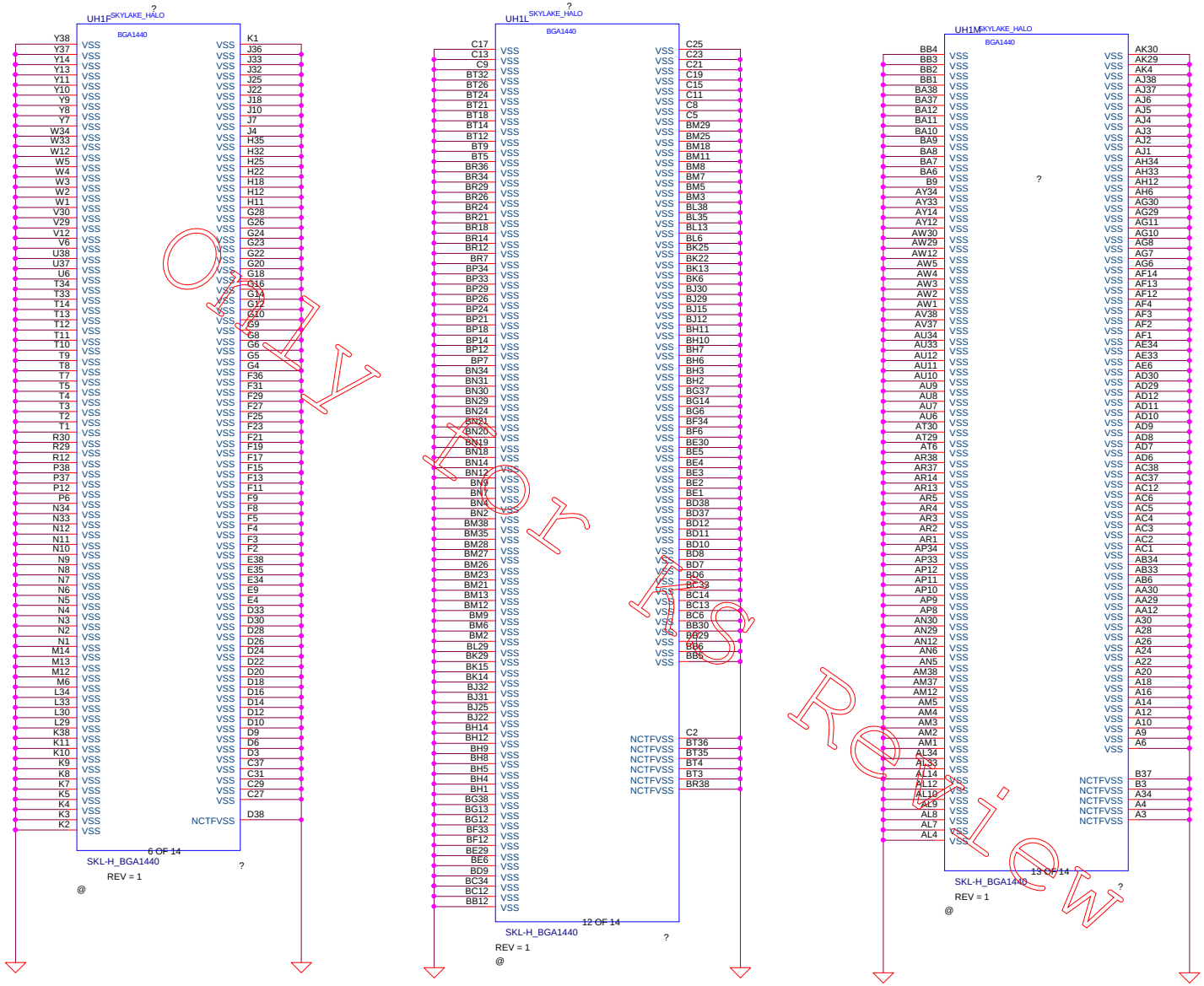
Title: **PROCESSOR(2/7) PM,XDP,CLK**

Size	Document Number	Rev
Custom		0.1(X00)

Date: Thursday, August 06, 2015 Sheet 12 of 71



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom		0.1(X00)

Date: Thursday, August 06, 2015 Sheet 13 of 71

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1

[8] DDR_A_D[0..63]
[8] DDR_A_MA[0..13]
[8] DDR_A_DQS#[0..7]
[8] DDR_A_DQS[0..7]

JDIMM1
JP7

+1.2V_DDR
+2.5V_MEM
+0.6VS
+3VS

All VREF traces should have 10 mil trace width

X06.16
X06.12

BELLW_SD-80886-1021
CONN@

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size: Document Number: LA-C361P Rev: 0.1(000)

Date: Thursday, August 06, 2015 Sheet 14 of 71

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMMB

All VREF traces should have 10 mil trace width

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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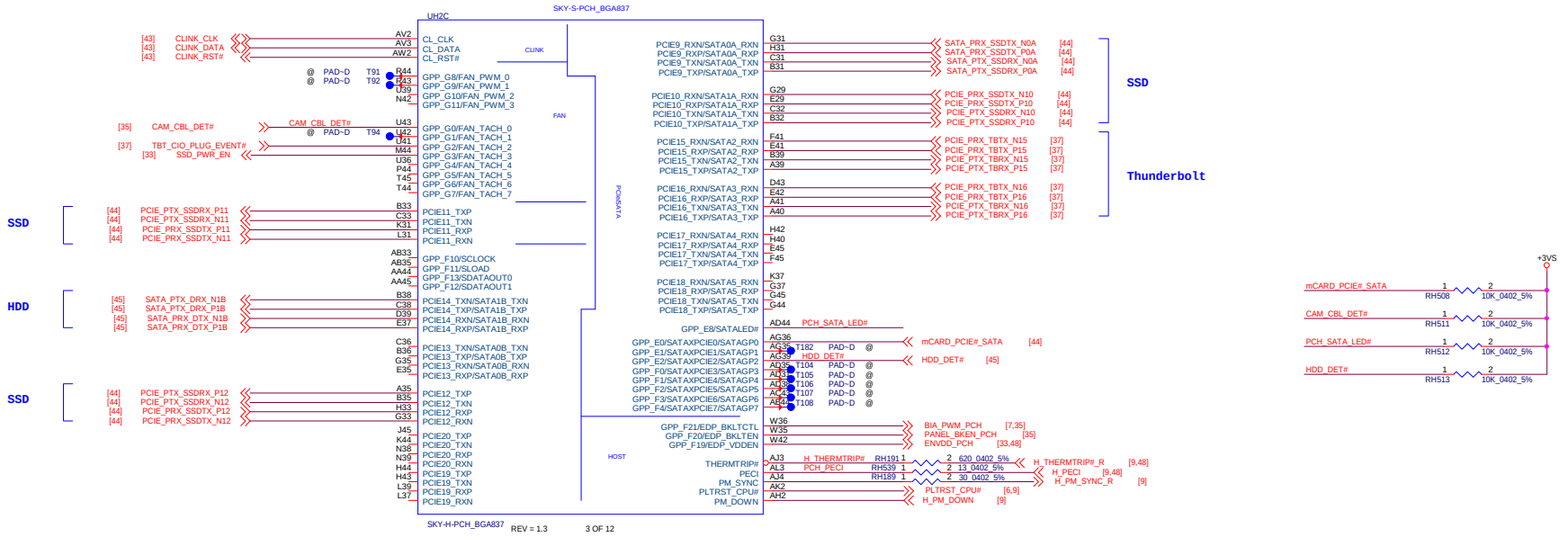
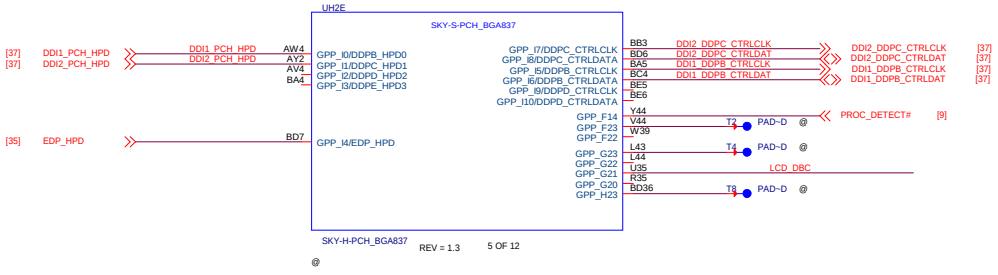
Compal Electronics, Inc.

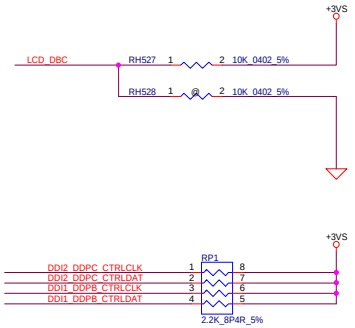
Title: **DDRIII DIMMB**

Size: Document Number: **LA-C361P** Rev: 0.1(000)

Date: Thursday, August 06, 2015 Sheet 15 of 71







PCH Strap PIN

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: PCH (1/8) SATA,HDA			
Size	Document Number: LA-C361P		Rev: 0.1(000)
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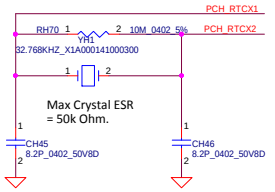
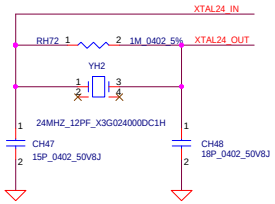
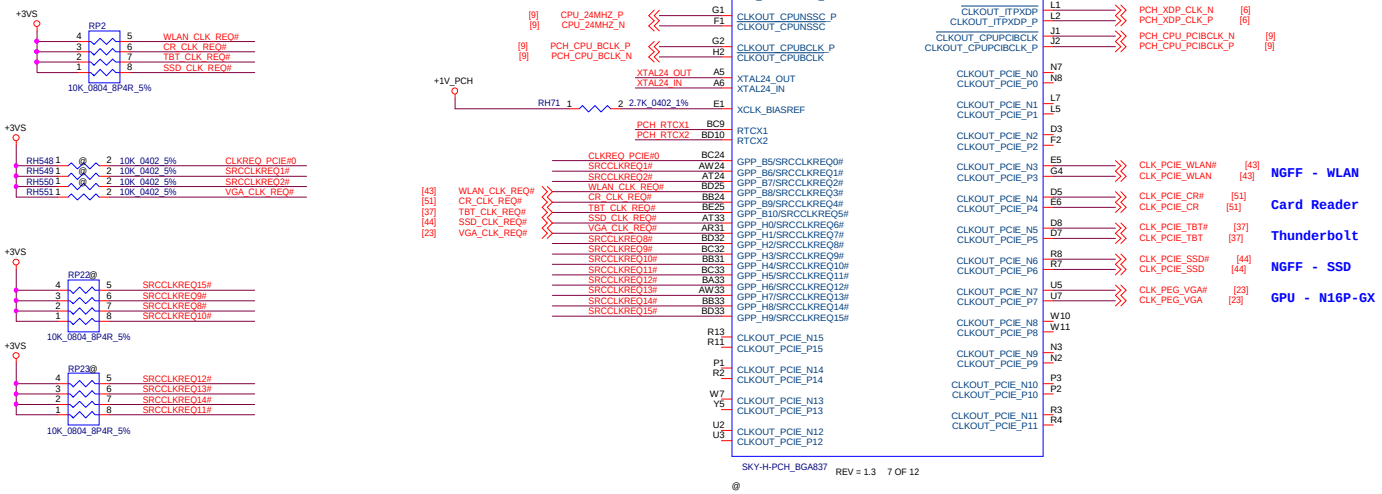
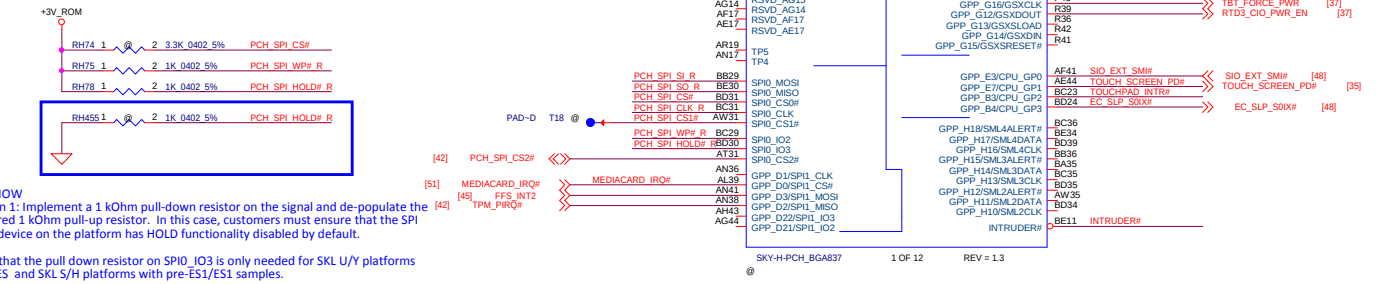
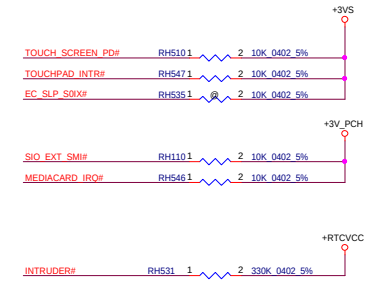
RTC CRYSTAL





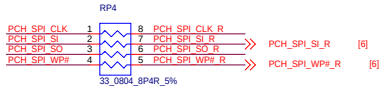


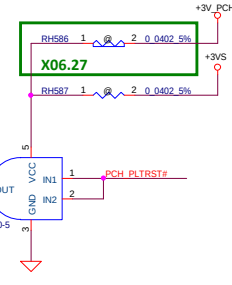


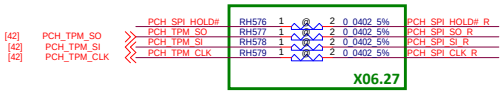


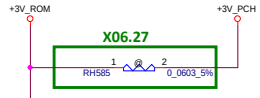
9/5 MOW
Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

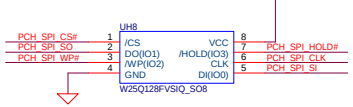








SPI ROM FOR ME (16MByte)



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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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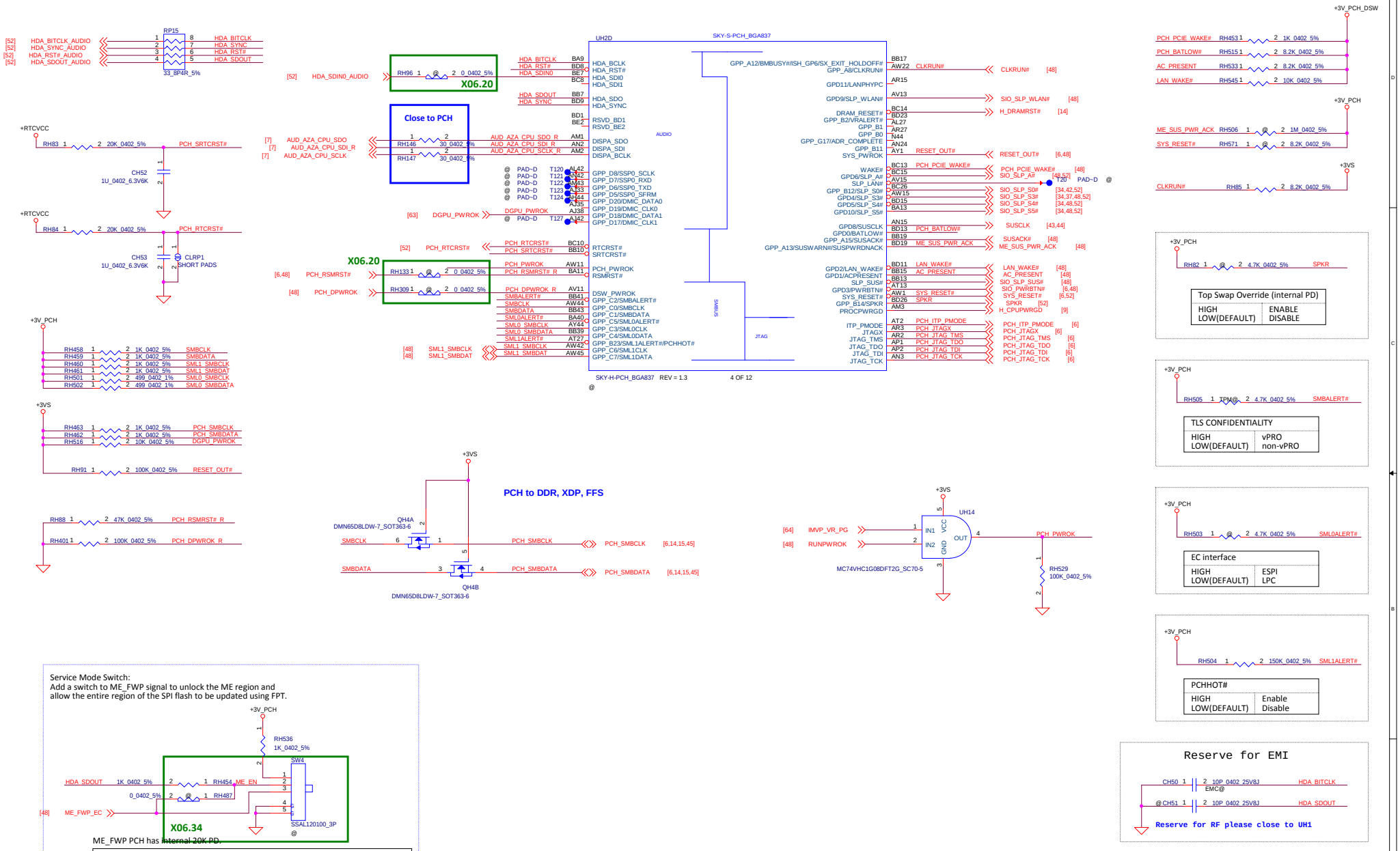
Compal Electronics, Inc.

Title: **PCH (2/8) SMBUS, CLK, SPI, LPC**

Size	Document Number	Rev
	LA-C361P	0.1(000)

Date: Thursday, August 06, 2015 | Sheet 17 of 71



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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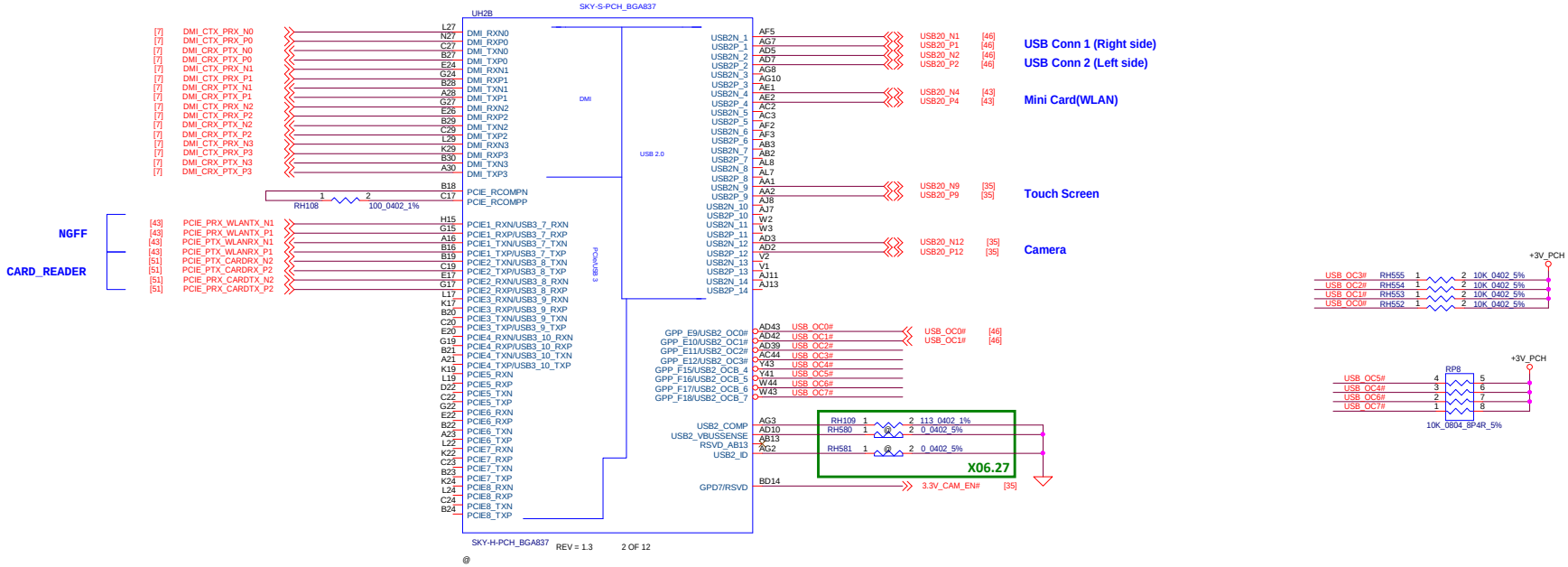
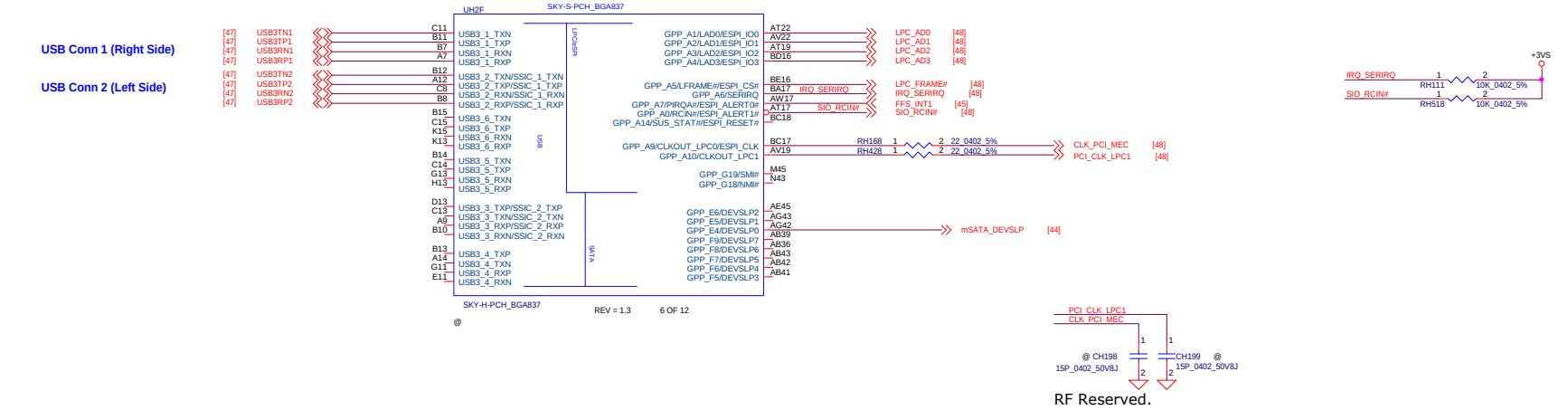
Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size	Document Number	Rev
	LA-C361P	0.1(000)

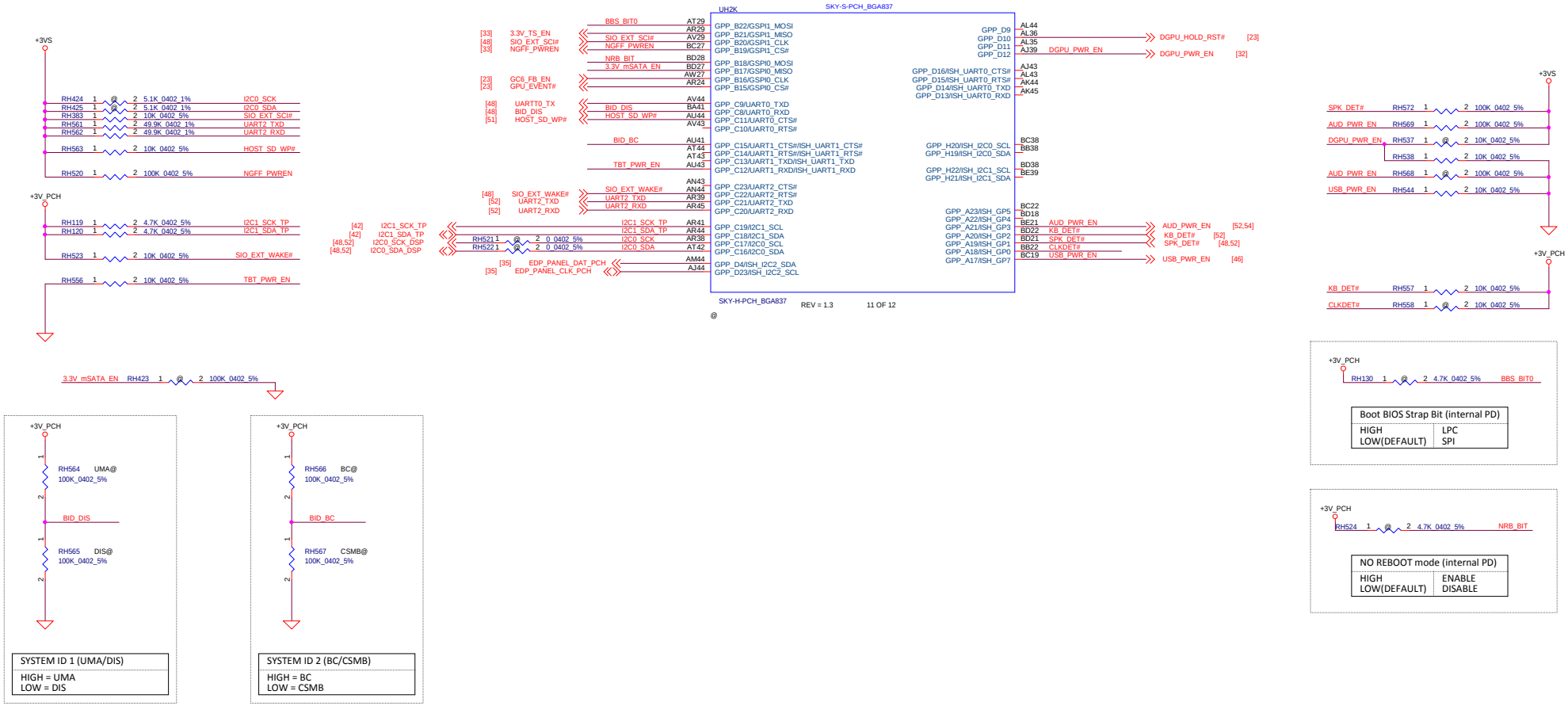
Date: Thursday, August 06, 2015 Sheet 18 of 71





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: PCH (4/8) PCI, USB			
Size	Document Number: LA-C361P		Rev: 0.1(000)
Date: Thursday, August 06, 2015	Sheet 19 of 71		



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size	Document Number	Rev
	LA-C361P	0.1(000)

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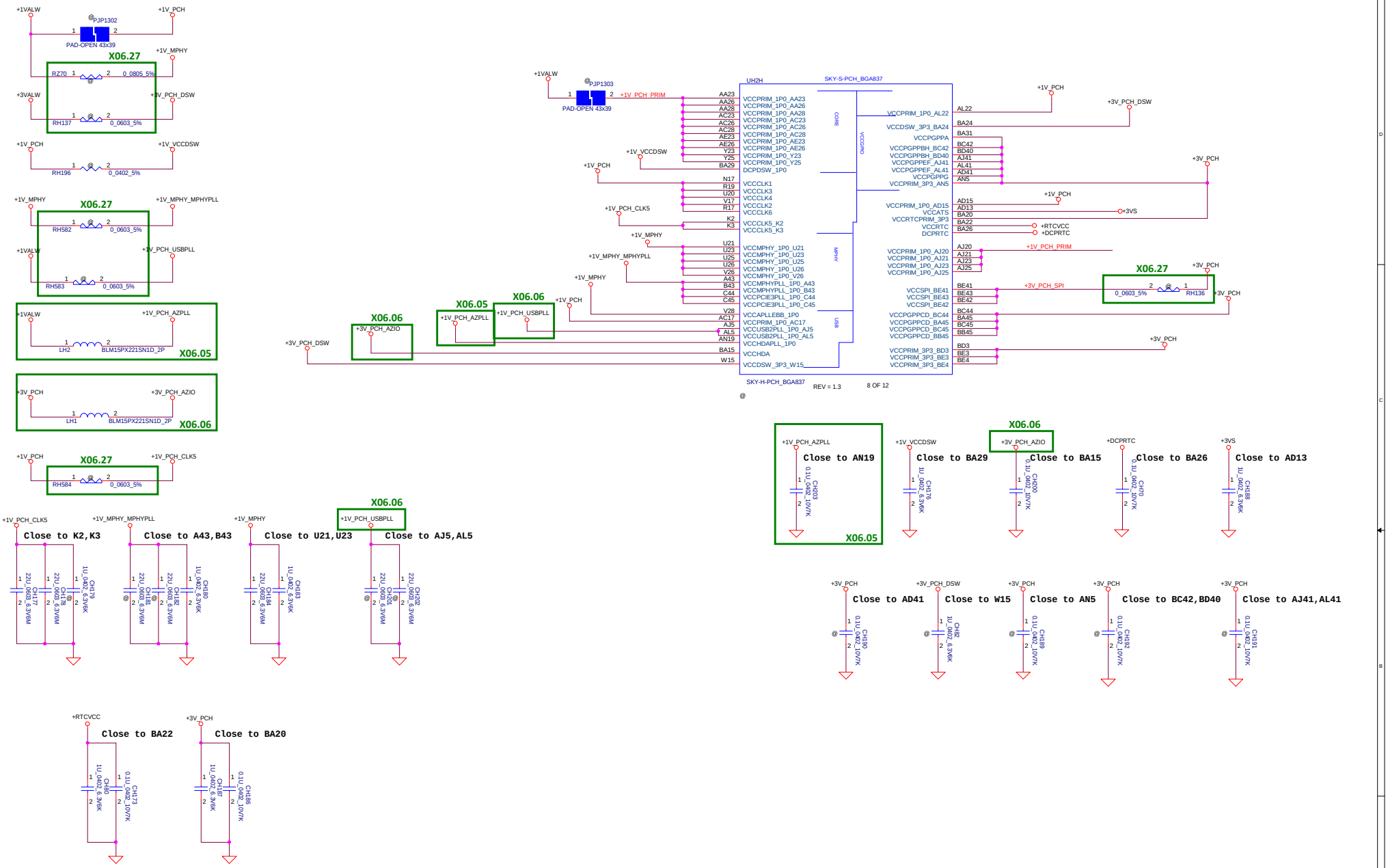

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Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (6/8) PWR**

Size	Document Number	Rev
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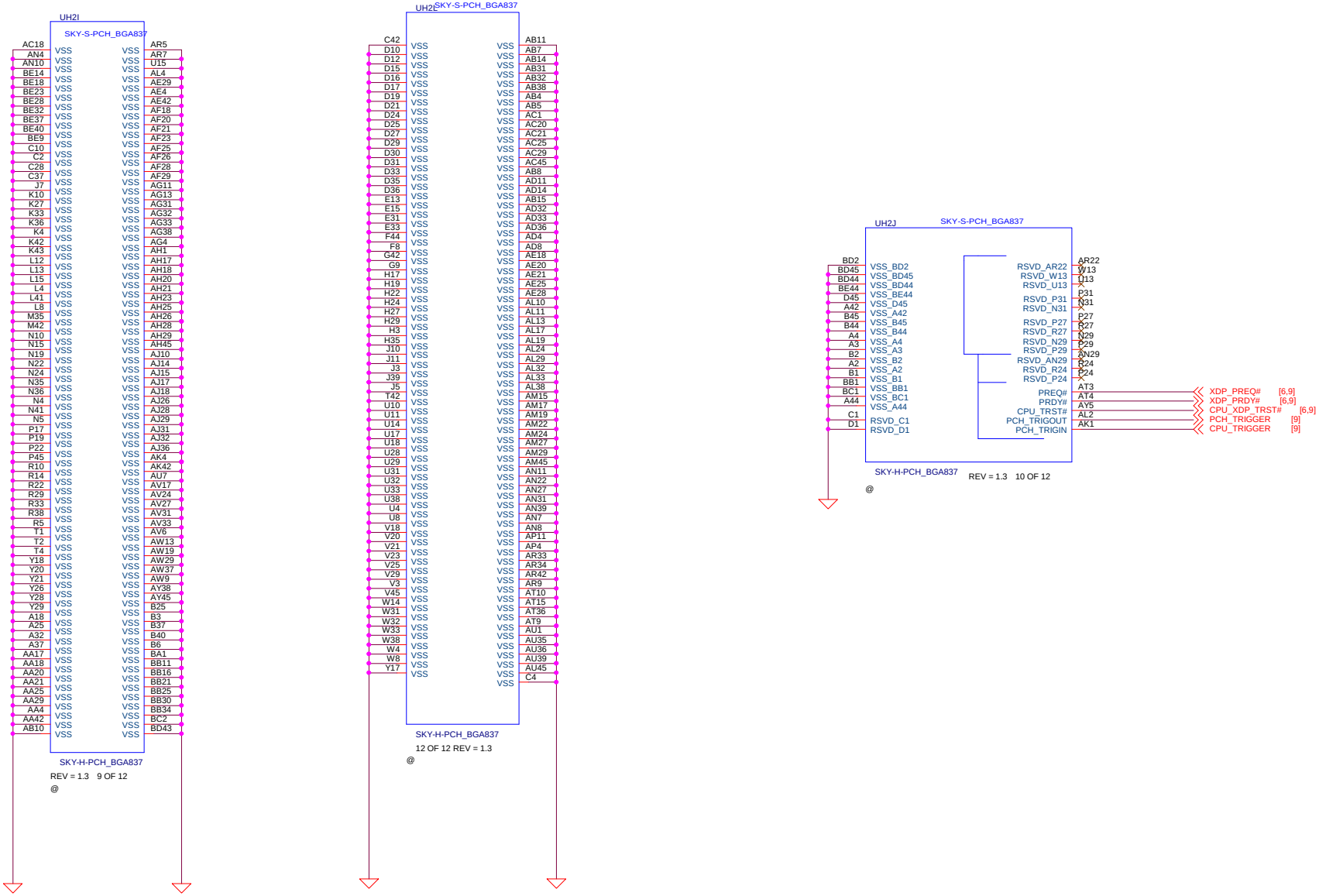

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Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size: Document Number: **LA-C361P** Rev: 0.1(X00)

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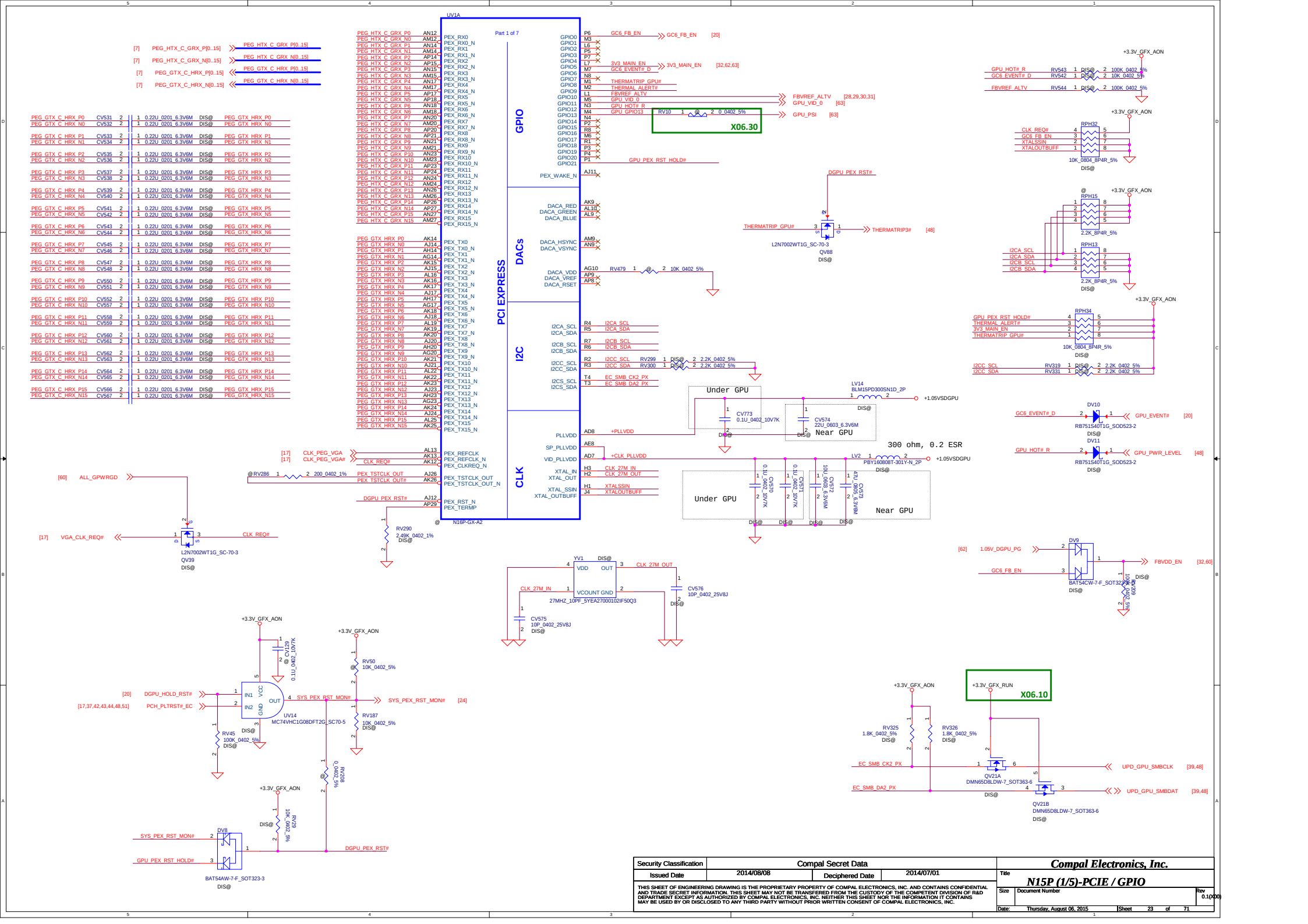

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Issued Date	2014/08/08	Deciphered Date	2014/07/01

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Compal Electronics, Inc.

Title: **N15P (1/5)-PCIE / GPIO**

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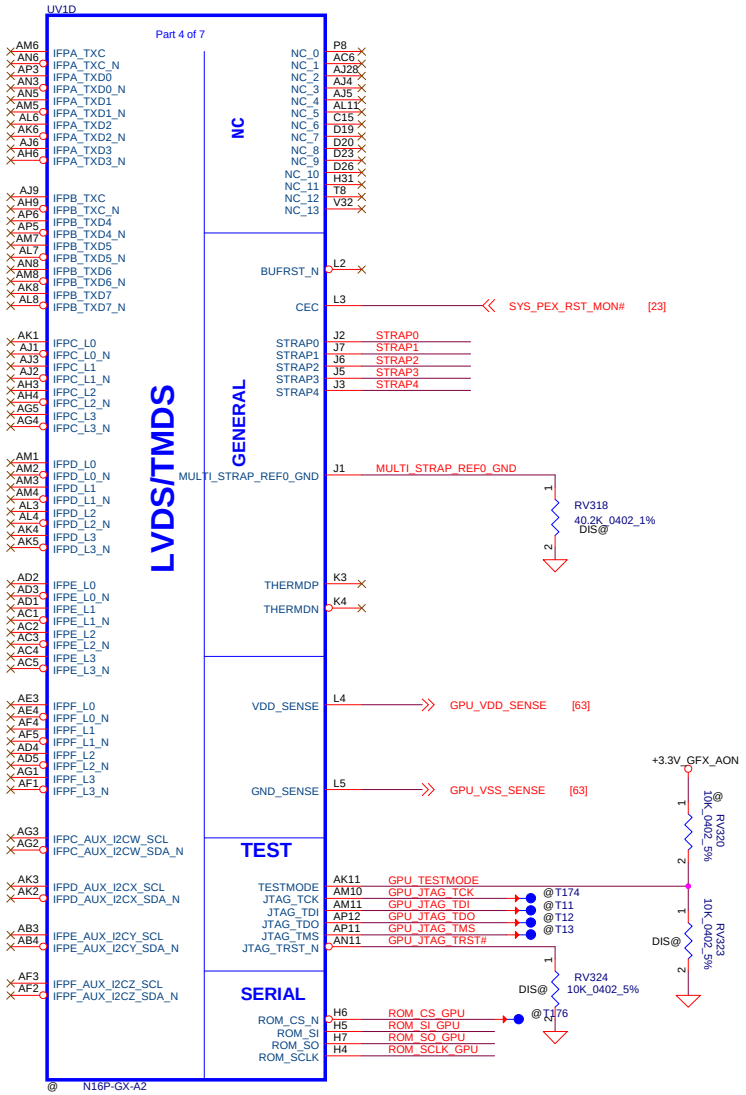
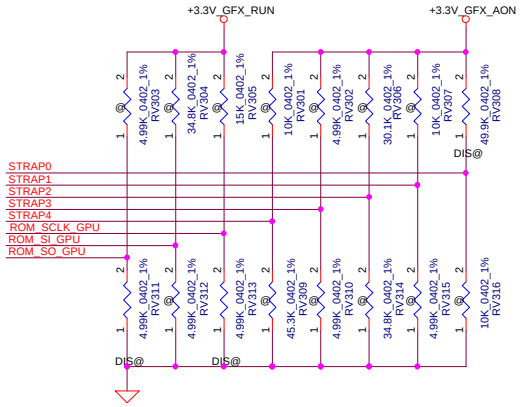


Straps



	Berlinetta	Berlinetta-P
Memory	N16P-GX	N16P-Q1
Hynix_H5GC4H24AJR-R0C	0x6 (0110)	0x6 (0110)
Samsung_K4G41325FC-HC03	0x3 (0011)	0x3 (0011)
Micron_EDW4032BABG-60-F	0x4 (0100)	None RVL

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

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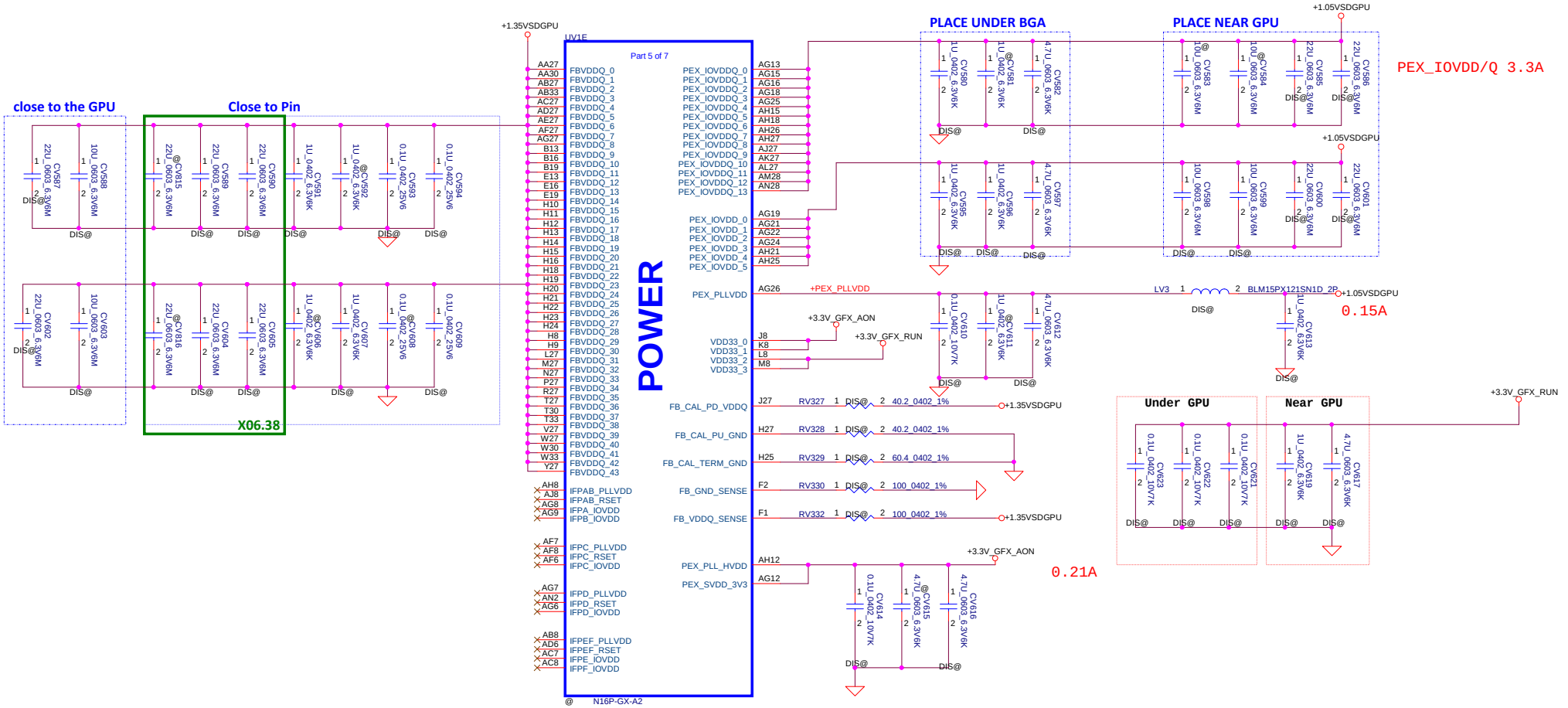

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Title: **N15P (3/5)-Power**

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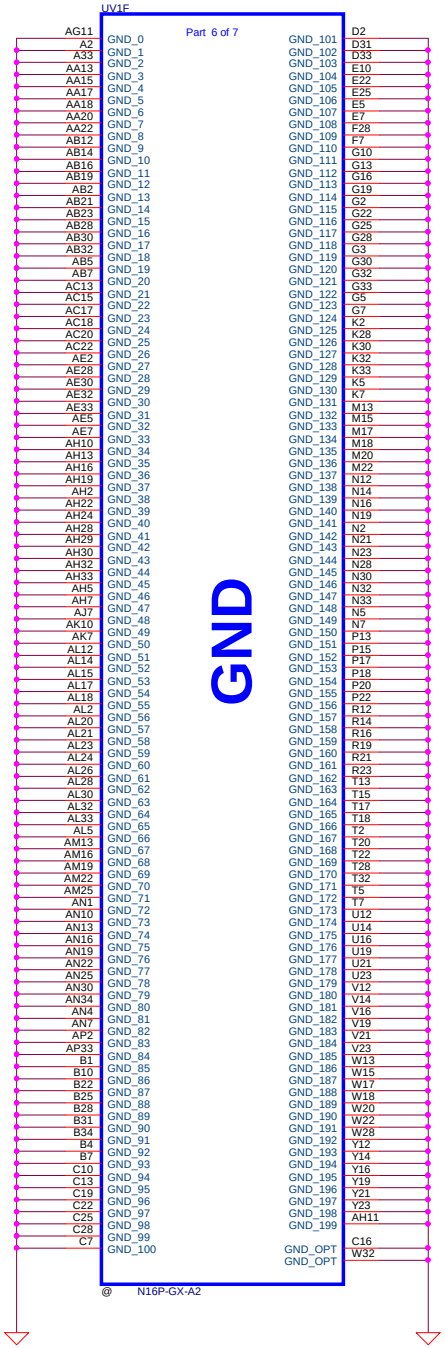

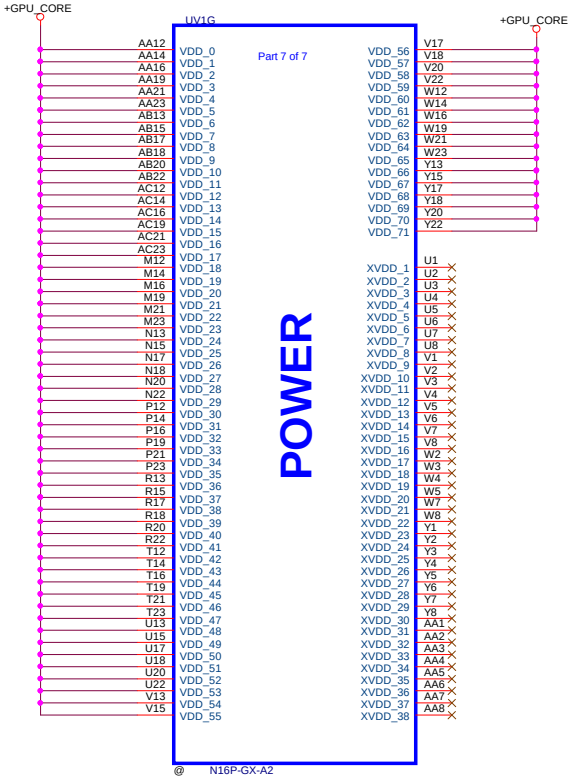

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Title: **N15P (4/5)-Power / GND**

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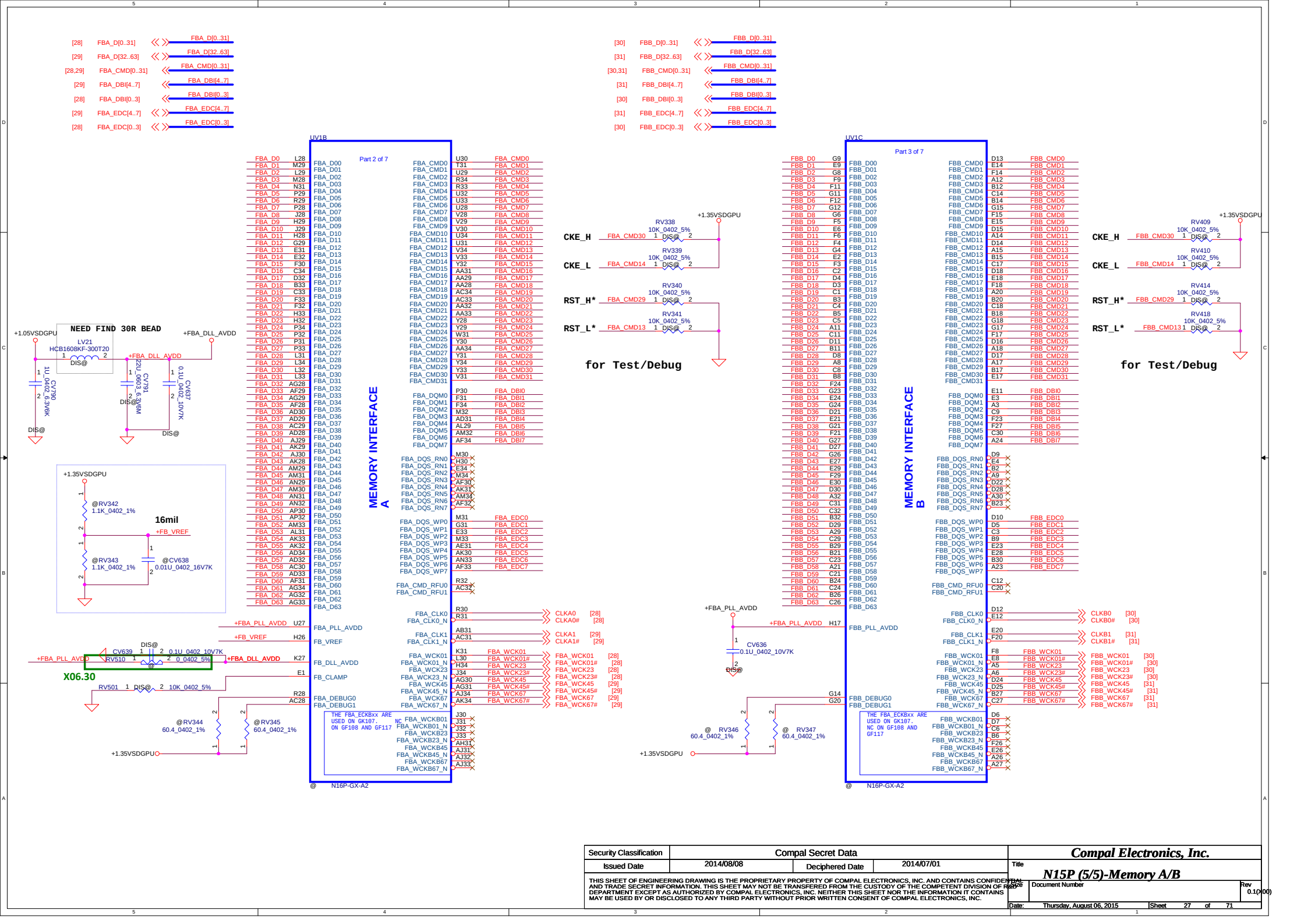

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Title: **N15P (5/5)-Memory A/B**

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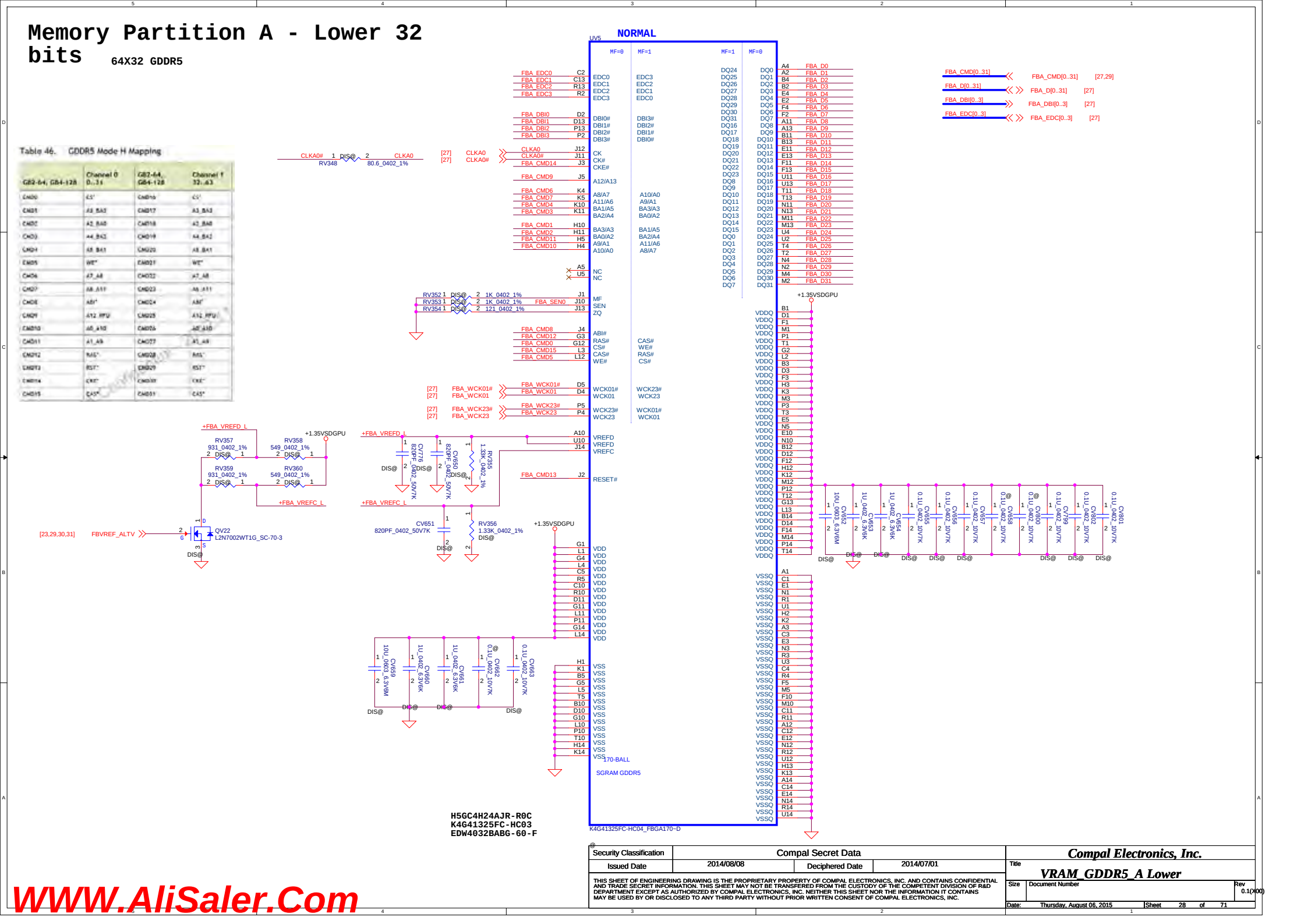
Memory Partition A - Lower 32 bits

64X32 GDDR5

NORMAL

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS0	CMD16	CS1
CMD1	A8_BA3	CMD17	A3_BA3
CMD2	A9_BA5	CMD18	A5_BA5
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE0	CMD21	WE1
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI0	CMD24	ABI1
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS0	CMD28	RAS1
CMD13	RST0	CMD29	RST1
CMD14	CKE0	CMD30	CKE1
CMD15	CAS0	CMD31	CAS1



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Compal Electronics, Inc.

Title: VRAM_GDDR5_A Lower

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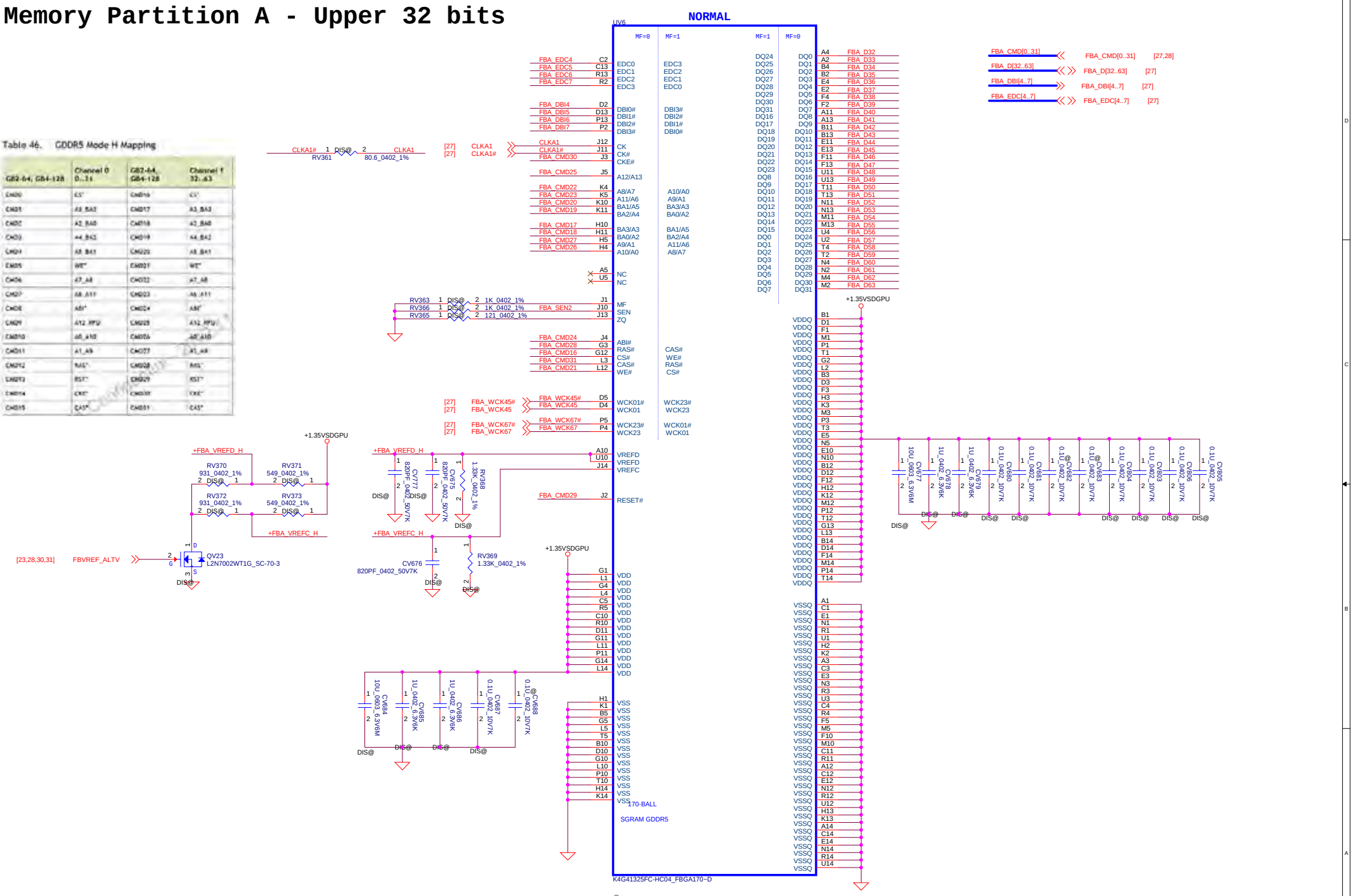
Memory Partition A - Upper 32 bits

NORMAL

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA2	CMD18	A2_BA2
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A8_A11	CMD23	A8_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A6_A10	CMD26	A6_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



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Security Classification	Compal Secret Data		
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Title: VRAM_GDDR5_A Upper

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Memory Partition B - Lower 32 bits

64X32 GDDR5

NORMAL

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 D..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS'	CMD16	CS'
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA2	CMD18	A2_BA2
CMD3	A4_BA1	CMD19	A4_BA1
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE'	CMD21	WE'
CMD6	A7_A8	CMD22	A7_A8
CMD7	A8_A11	CMD23	A8_A11
CMD8	ABI'	CMD24	ABI'
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A9_A10	CMD26	A9_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS'	CMD28	RAS'
CMD13	RST'	CMD29	RST'
CMD14	CKE'	CMD30	CKE'
CMD15	CAS'	CMD31	CAS'

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Compal Electronics, Inc.

Title: VRAM_GDDR5_B Lower

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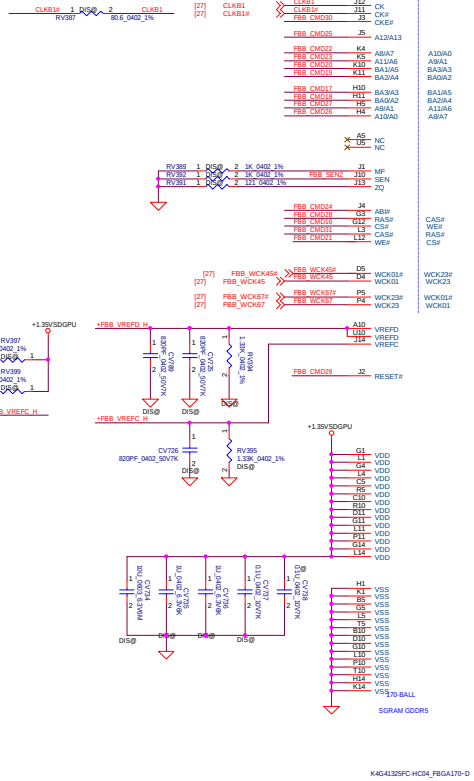
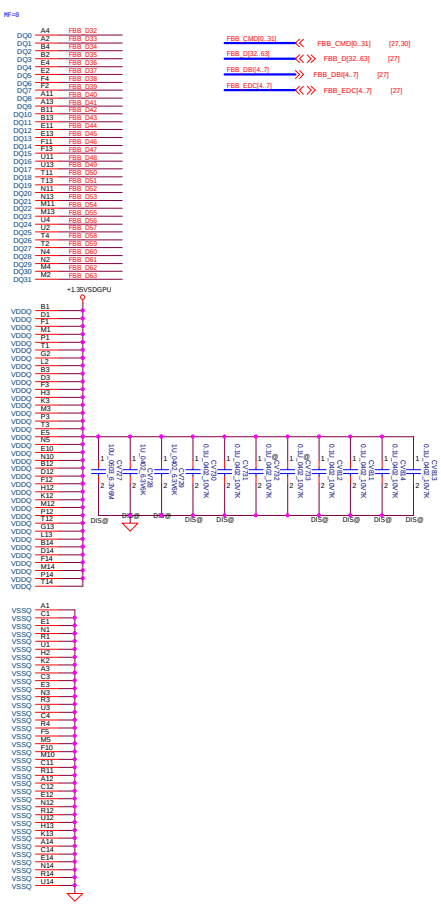
Memory Partition B - Upper 32 bits

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0...31	GB2-64, GB4-128	Channel 1 32...63
CMD0	CS*	CMD16	CS*
CMD1	A0_BA2	CMD17	A3_BA2
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A8_A11	CMD23	A9_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A6_A10	CMD26	A6_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*





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Compal Electronics, Inc.

Title: VRAM_GDDR5_B Upper

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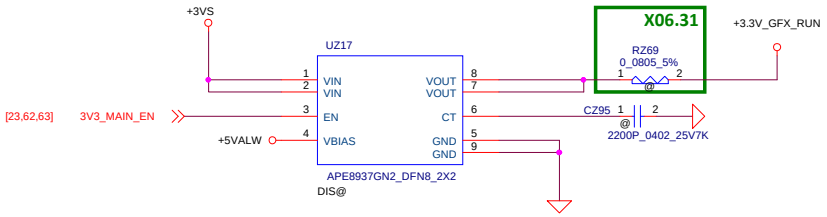
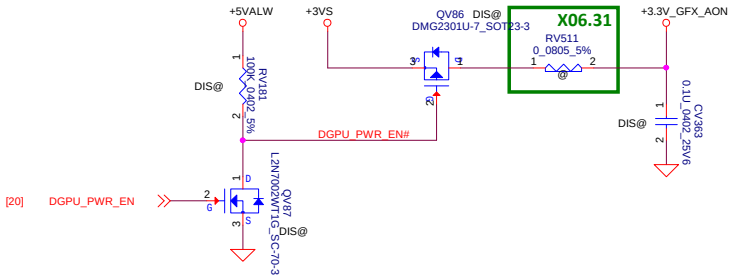
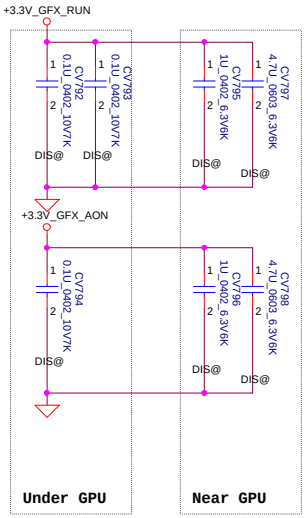
+3.3V_GFX_RUN

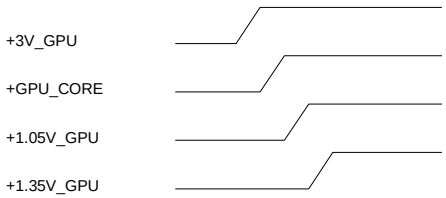


+3VALW to +3.3V_GFX_AON



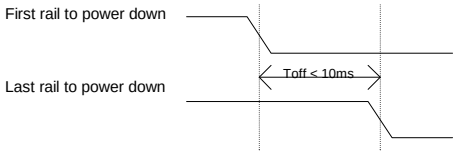


GPU Power Up Power Rail Sequence

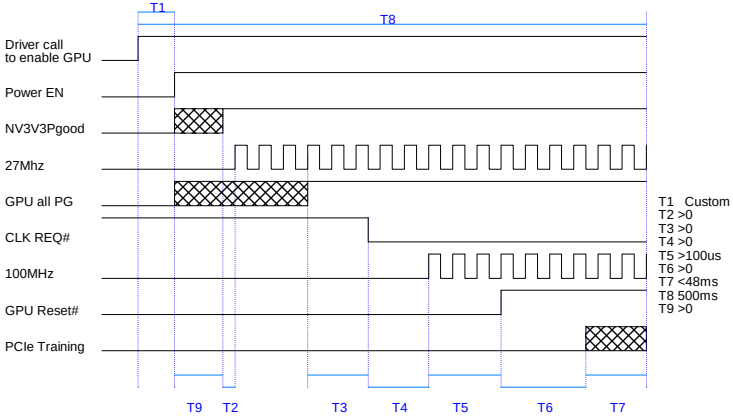


The ramp time for any rail must be more than 40us.

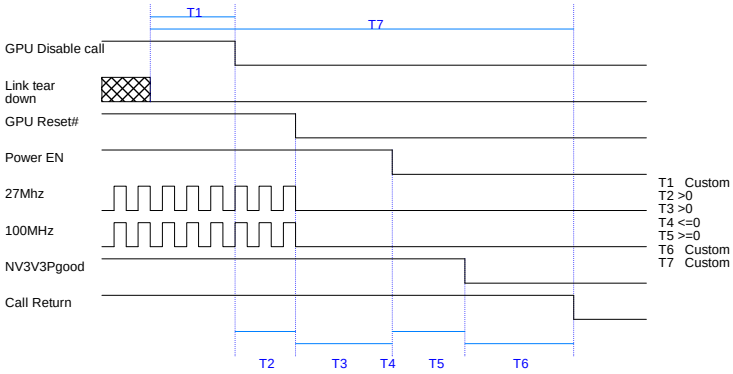
GPU Power Down Sequence



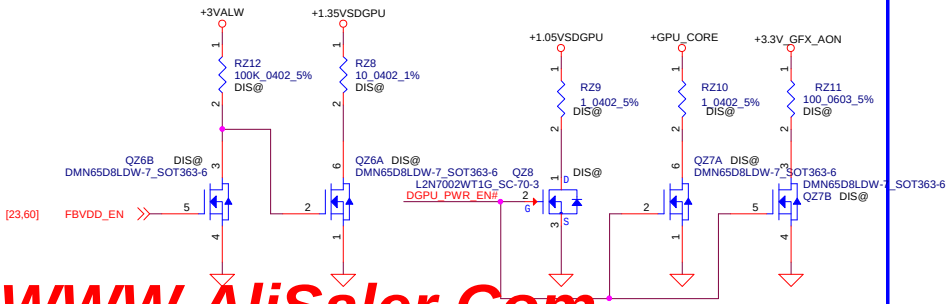
GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence



Discharge



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Title: GPU DC/DC interface

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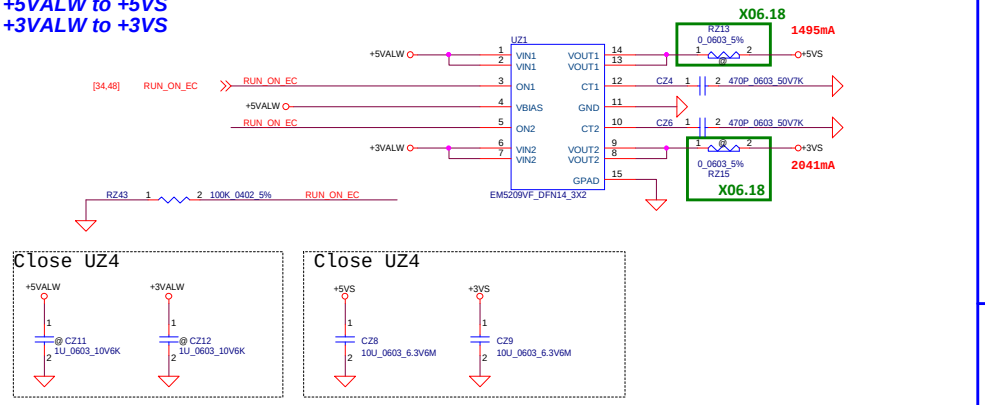
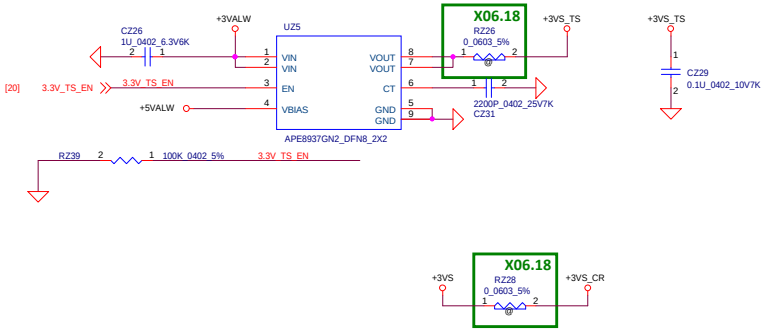
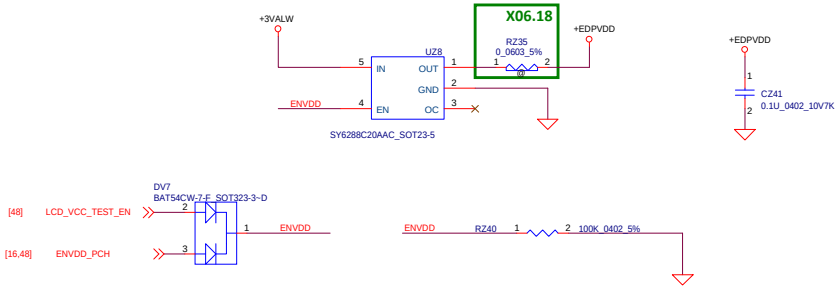
+5VALW to +5VS
+3VALW to +3VS



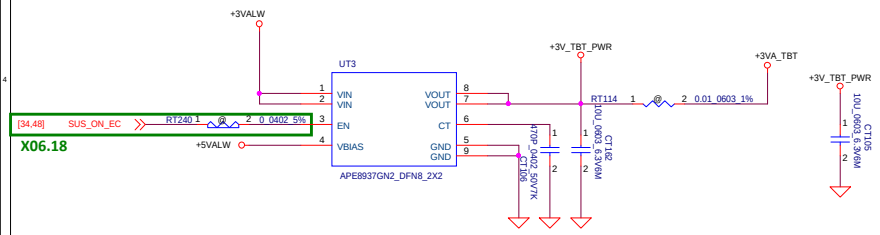
Touch Screen Load Switch & Card Reader



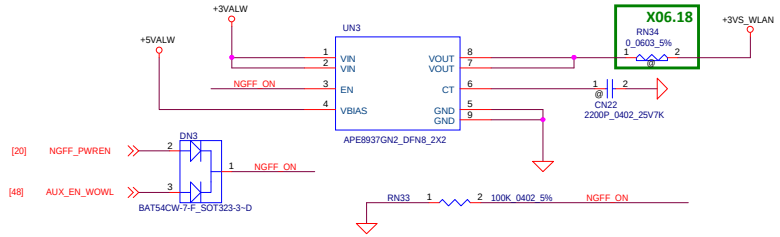
eDP & Camera Load Switch



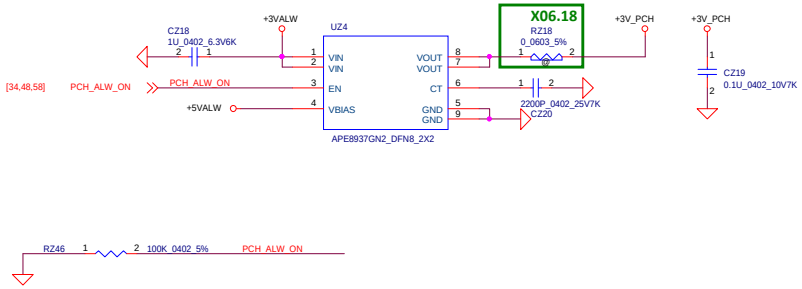
Alpine Ridge(TBT) Load Switch



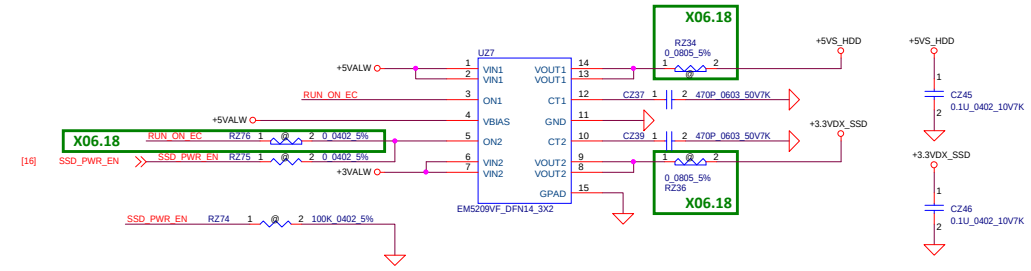
WLAN Load Switch



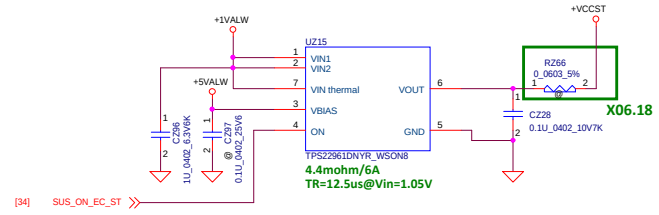
+3VALW to +3V_PCH



HDD, SSD Load Switch



+VCCST Load Switch



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Title: **SYS DC/DC Interface**

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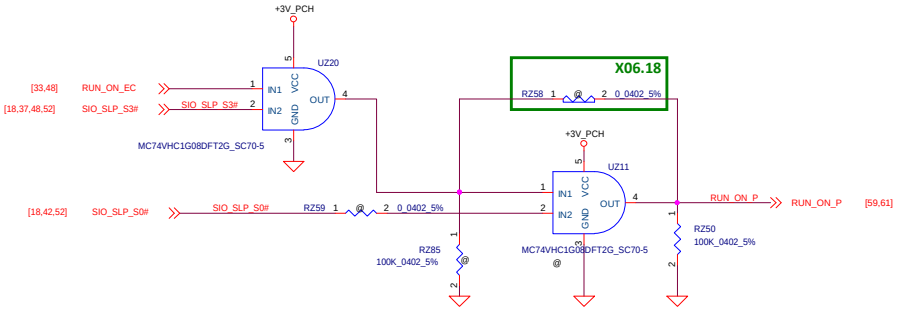
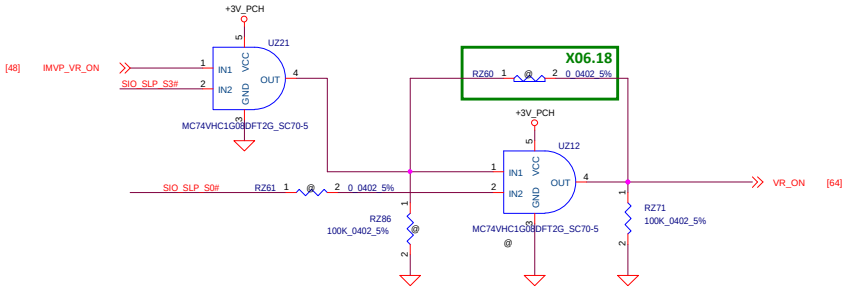
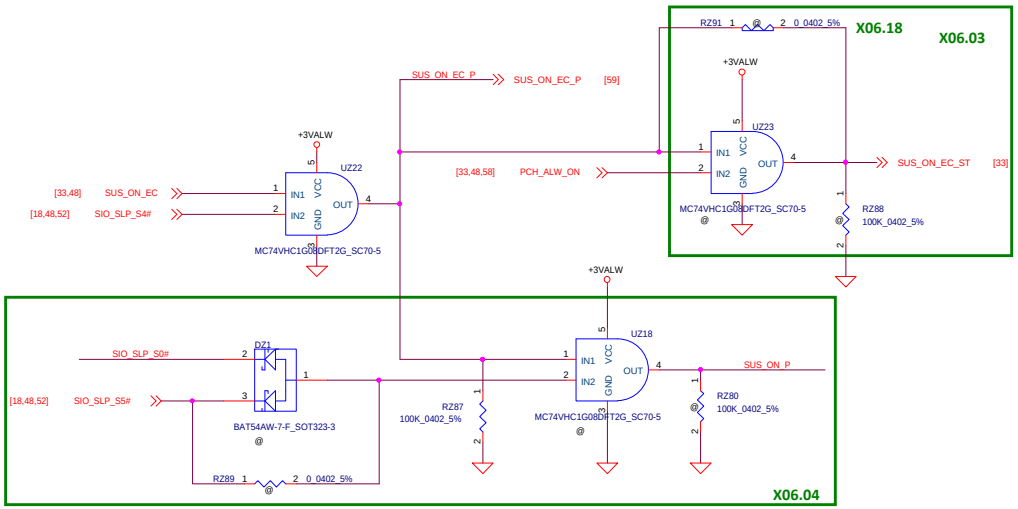
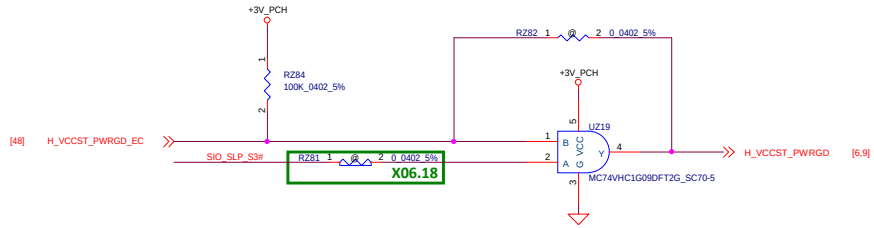
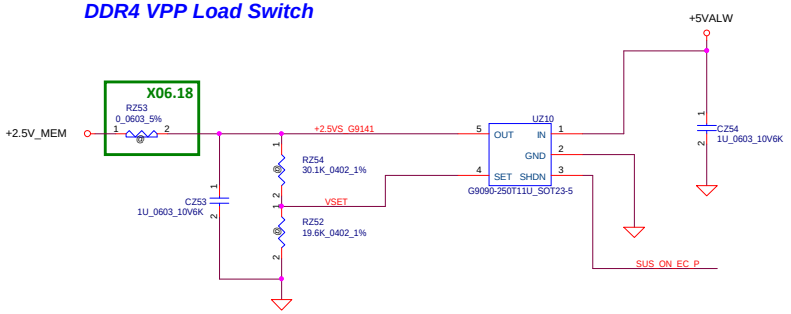




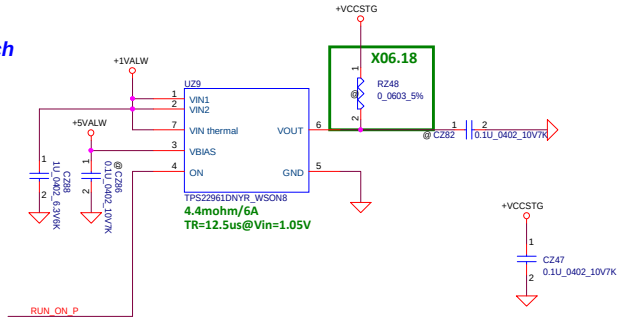




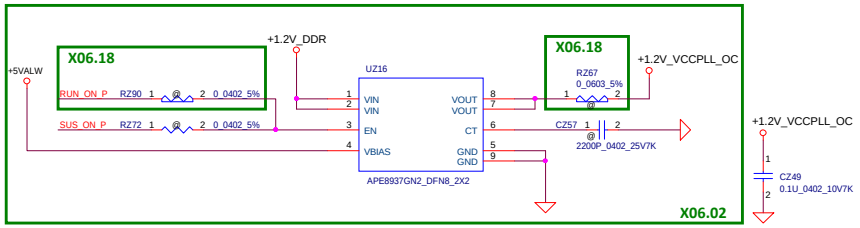
DDR4 VPP Load Switch



+VCCSTG Load Switch



+VCCPLL_OC Load Switch



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Title	EC ENE-KB9012/ KC3810		
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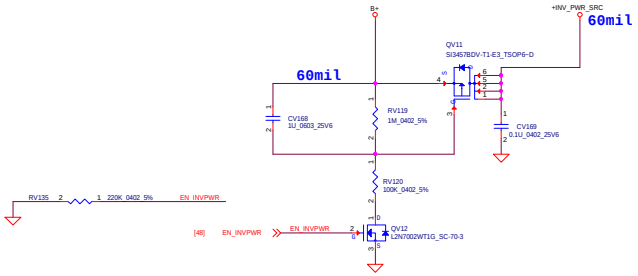
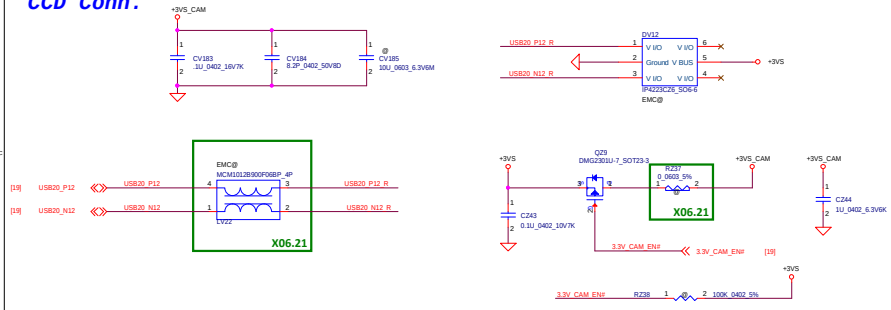
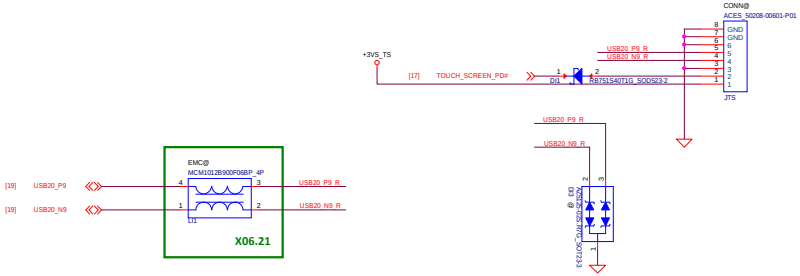
LCD backlight PWR CTRL



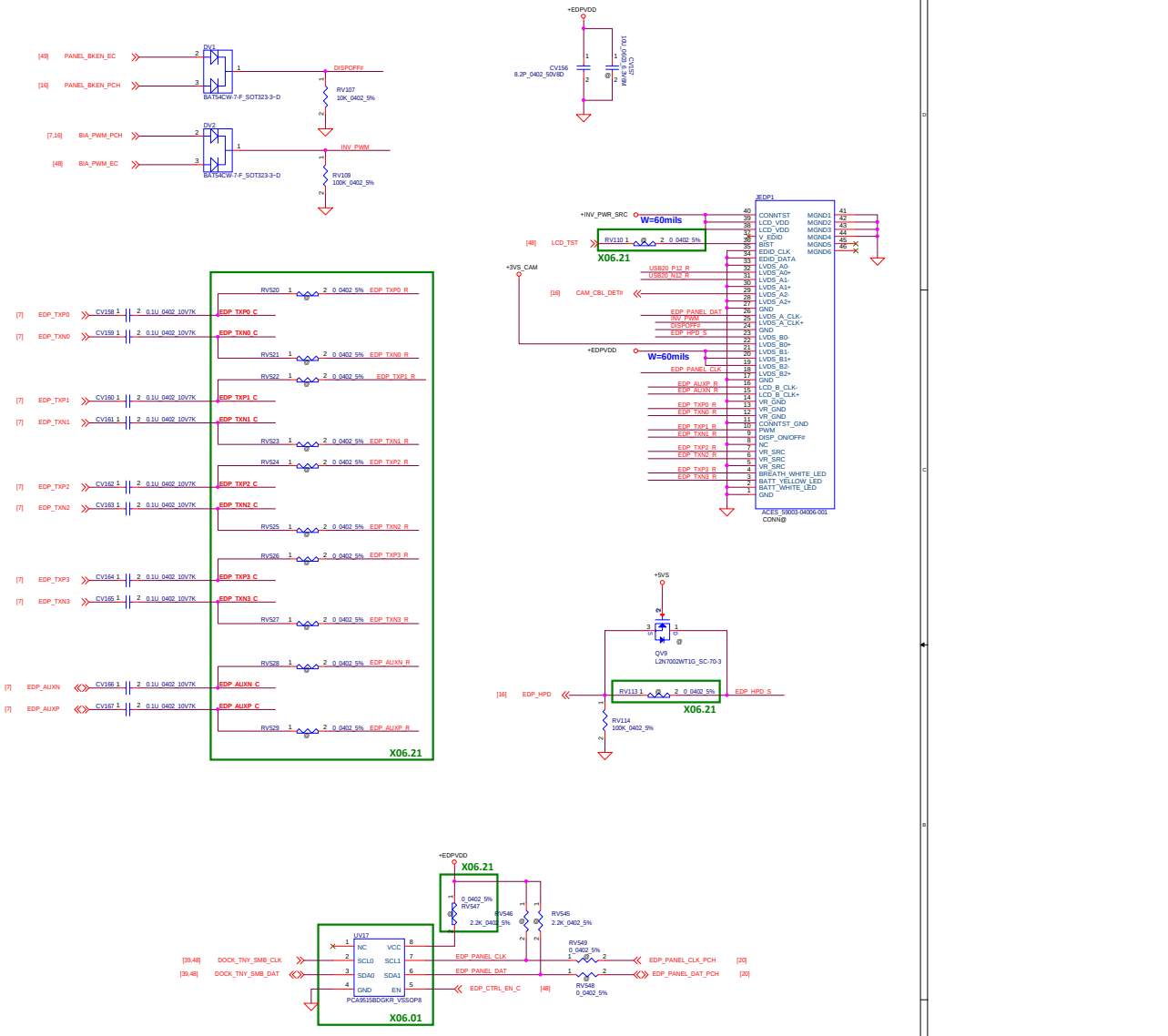
CCD Conn.



Touch Screen Conn.



eDP & TS Conn.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: eDP /TS conn.
Size	Document Number: LA-C361P		Rev: 0.1(X00)
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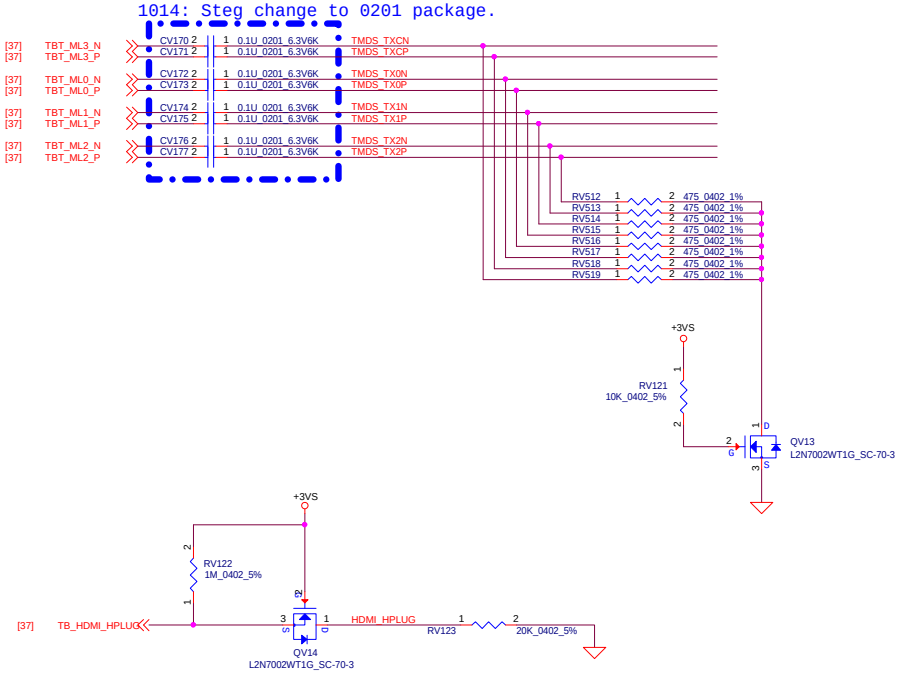
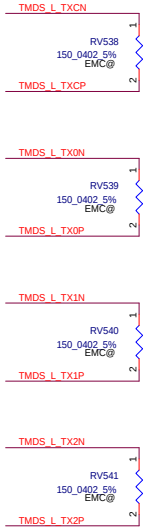
HDMI Active Level Shift(ALS type)

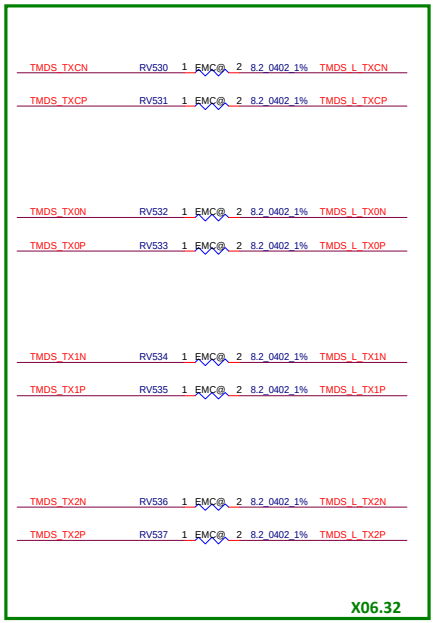
1014: Steg change to 0201 package.

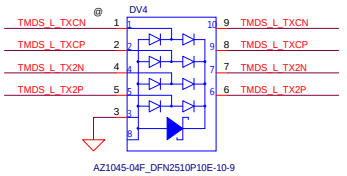


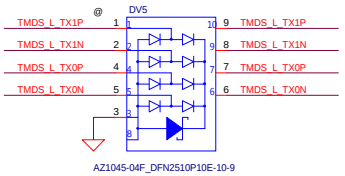
Place between ESD and CM-Choke



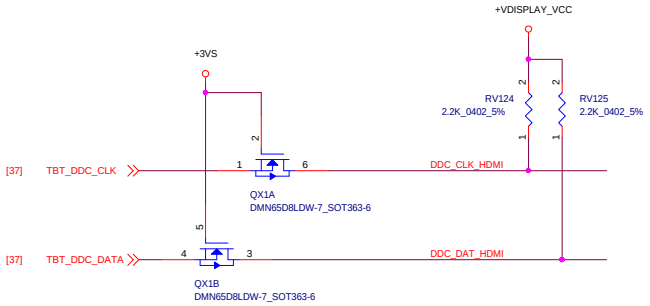
Place close to JHDMI1



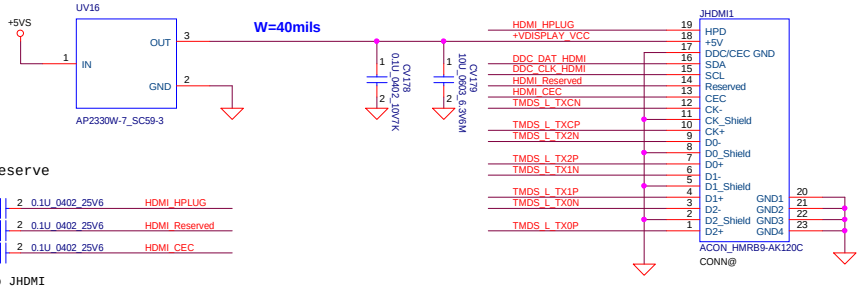




HDMI DDC



HDMI conn



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: HDMI

Size: Custom | Document Number: LA-C361P | Rev: 0.1(X00)

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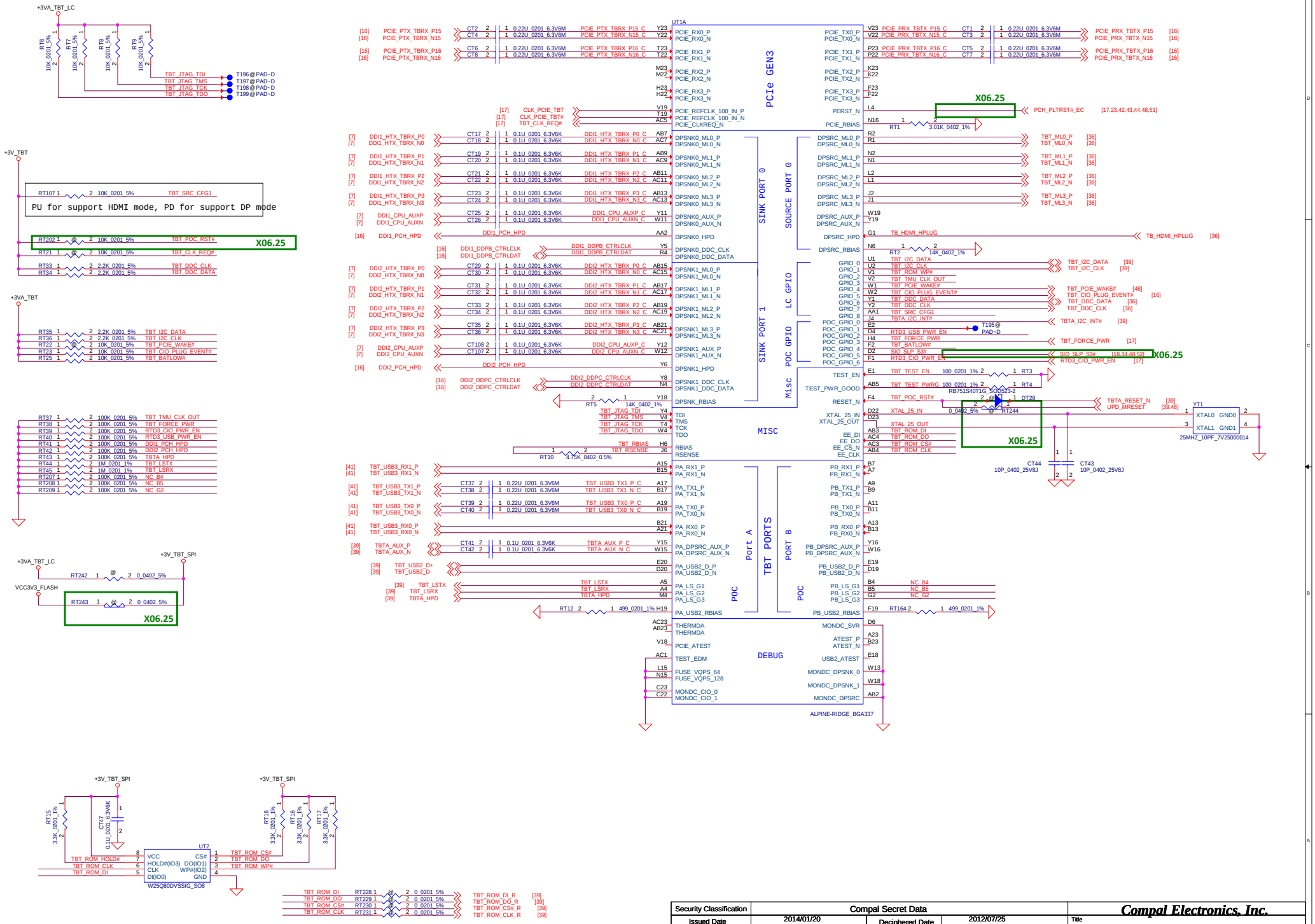

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: AR_TBT (1/2) DP / PCIE

Size	Document Number	Rev
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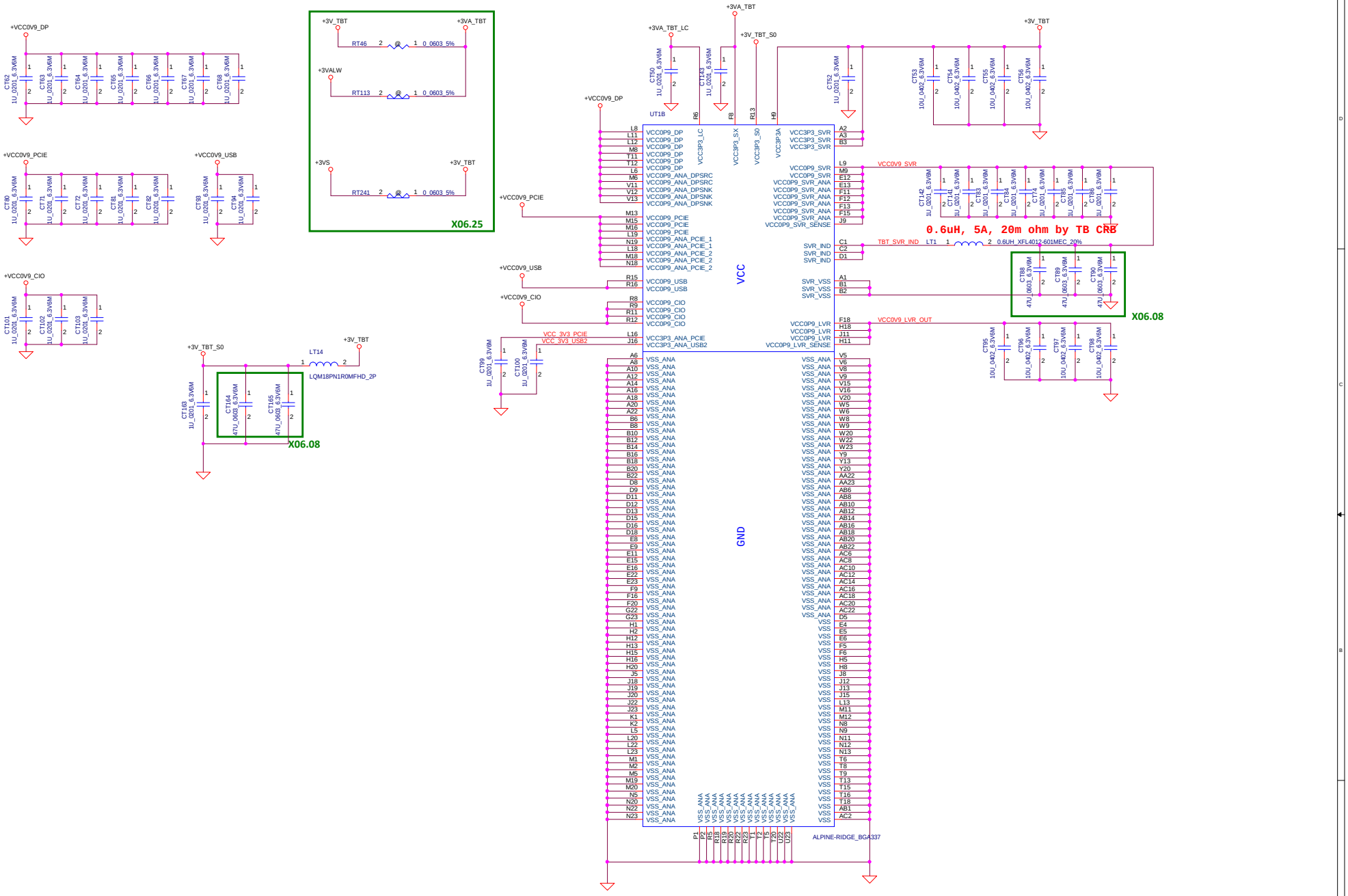

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2012/07/25

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Compal Electronics, Inc.

Title: AR_TBT (2/2) PWR / GND

Size	Document Number	Rev
C	LA-C361P	0.1(X00)

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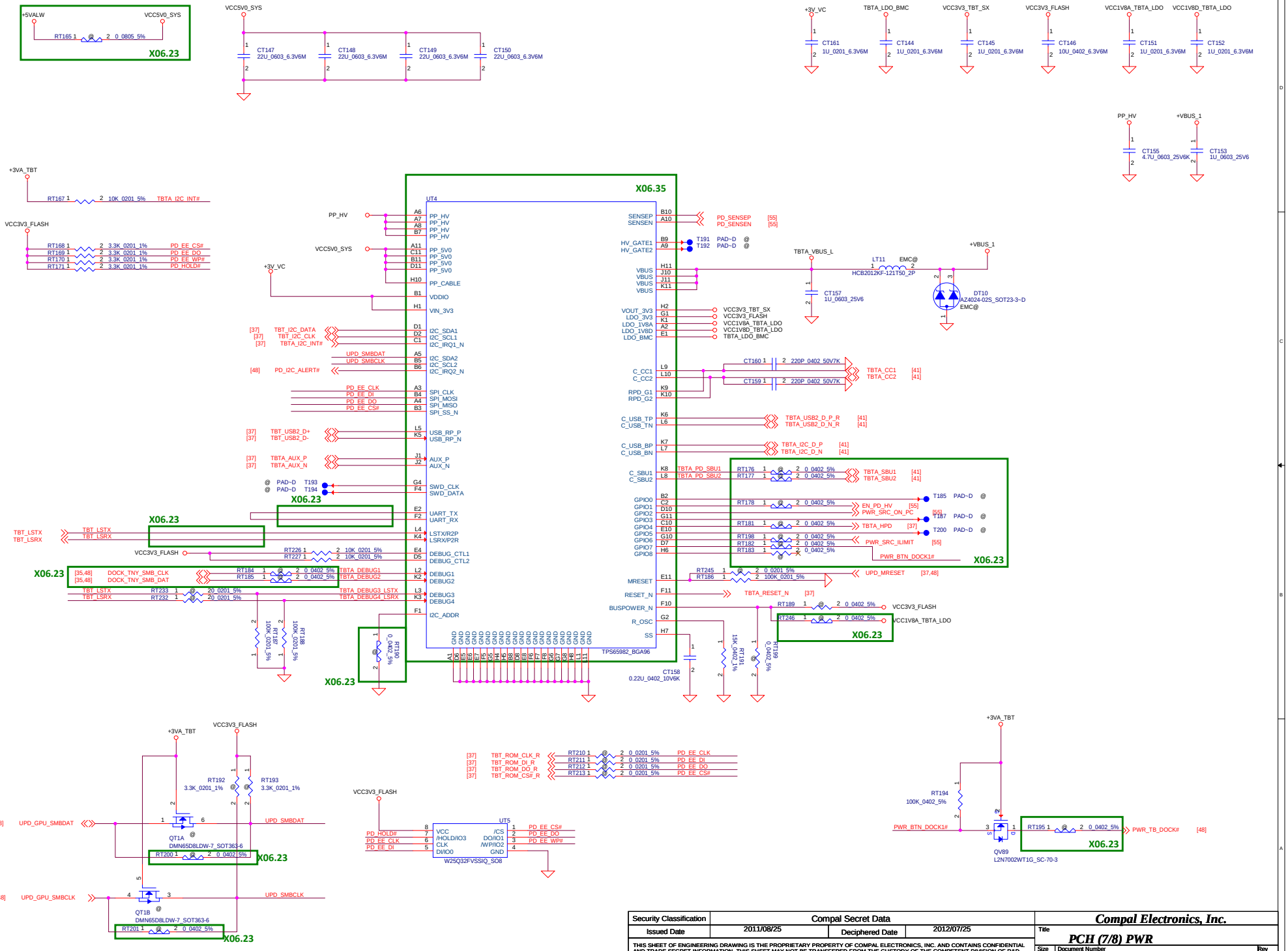

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

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Reserve

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: Power on Sequence			
Size	Document Number		Rev 0.1(X00)
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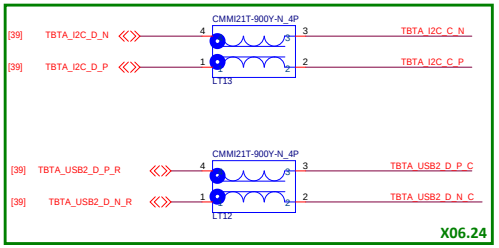

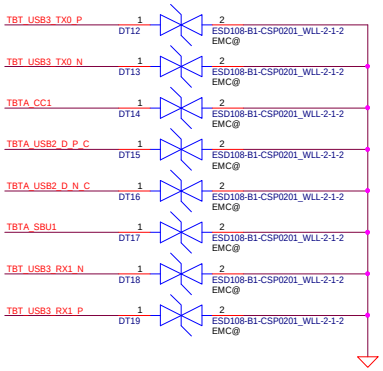

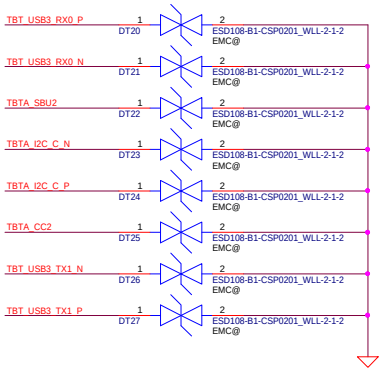

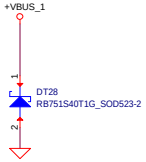

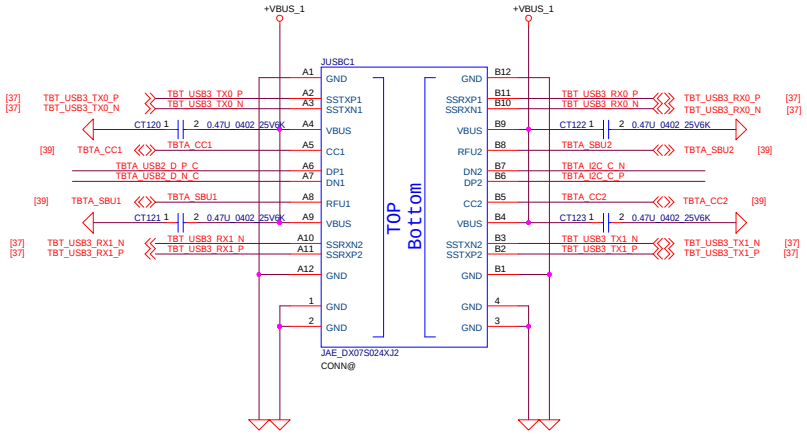

Security Classification	Compal Secret Data		
Issued Date	2014/01/20	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PD USB TYPE-C**

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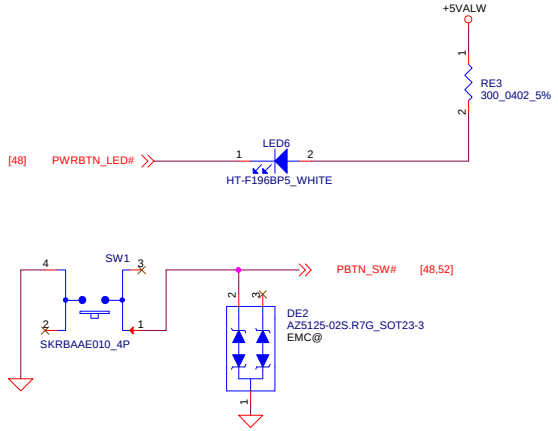
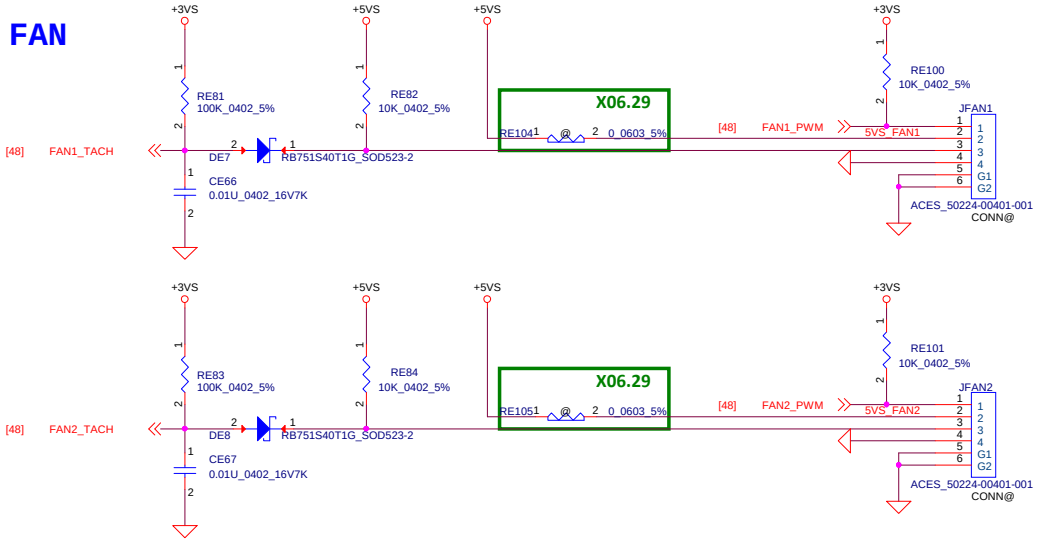
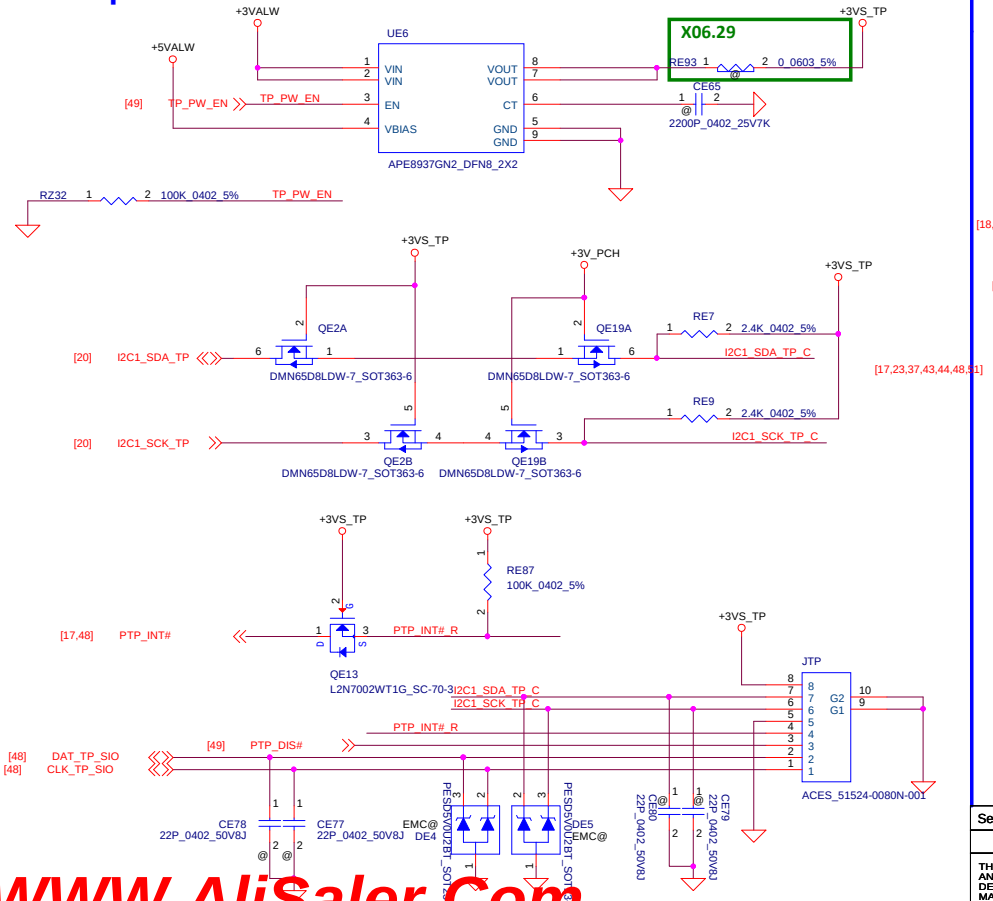
Power Button and LED



PWM FAN

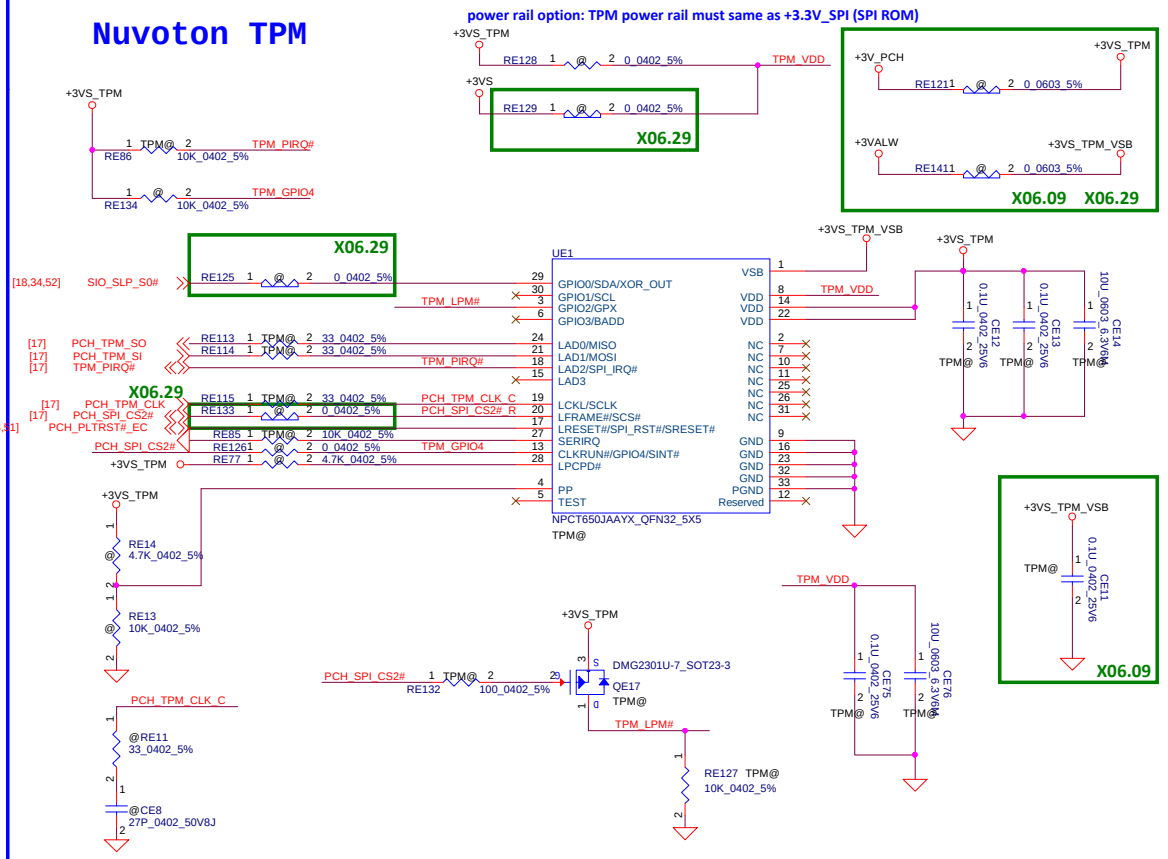


Touch pad



Nuvoton TPM

power rail option: TPM power rail must same as +3.3V_SPI (SPI ROM)



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: FAN/TP/KB/PWR SW

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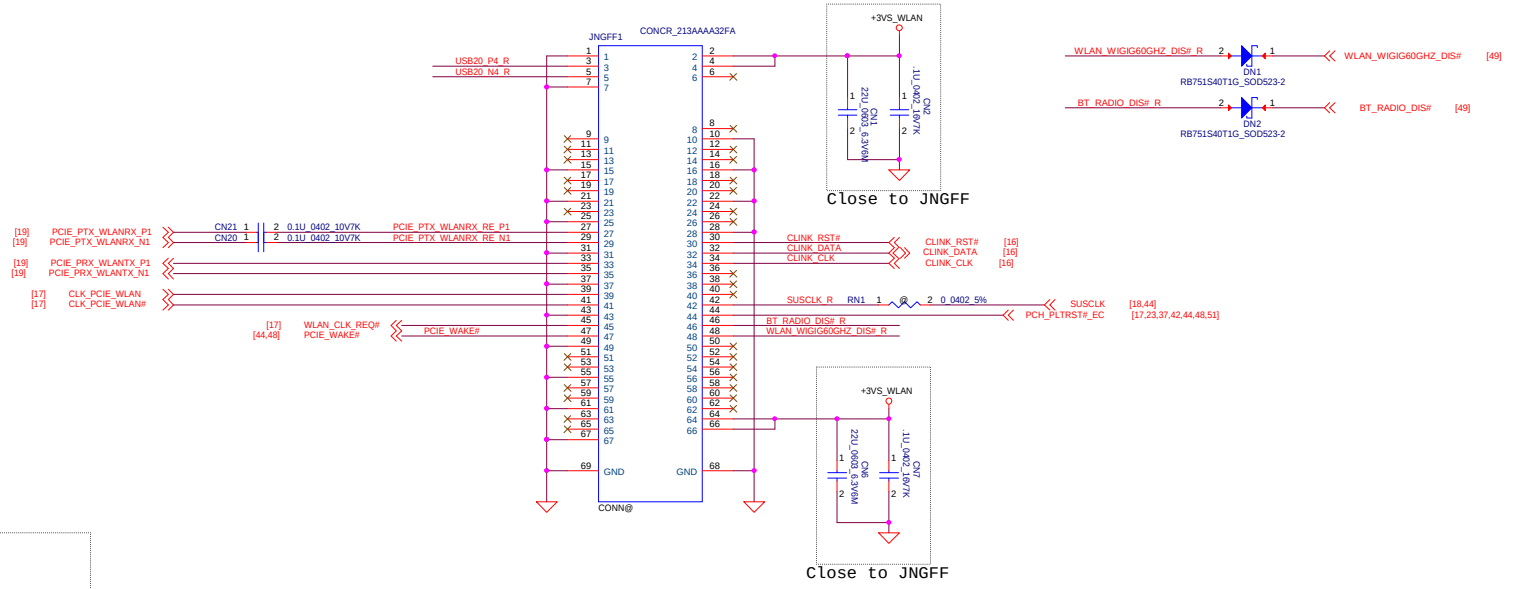
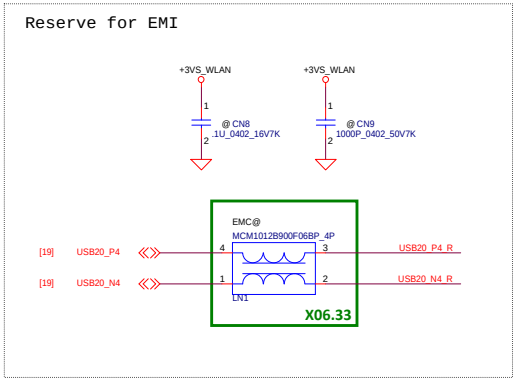
M.2 Slot-A Key-A (WLAN + BT)



Reserve for EMI



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title NGFF
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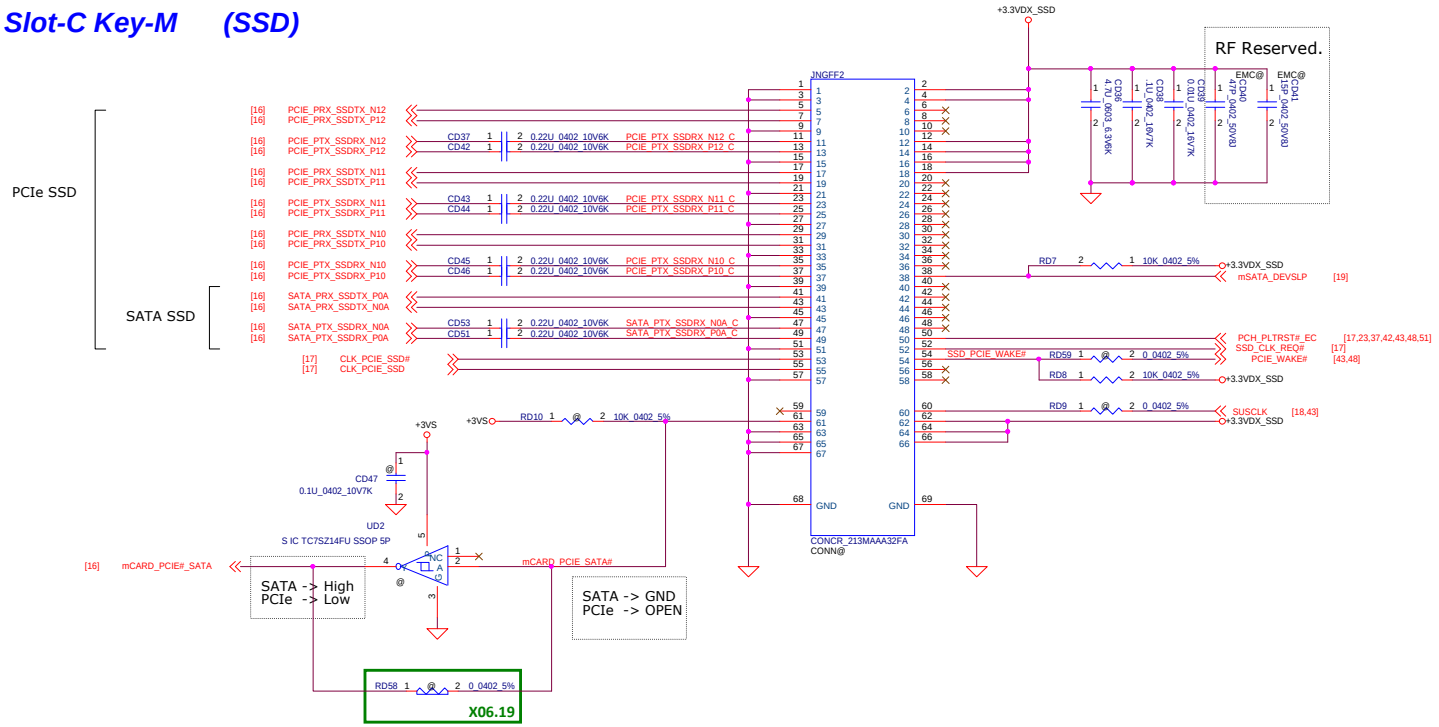
M.2 Slot-C Key-M (SSD)



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: SSD			
Size: C	Document Number: LA-C361P		Rev: 0.1(000)
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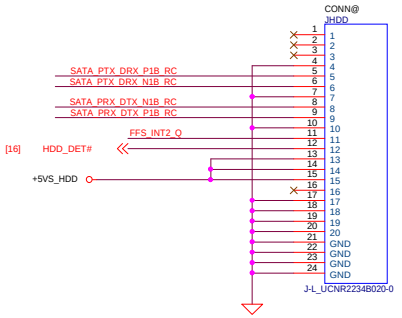
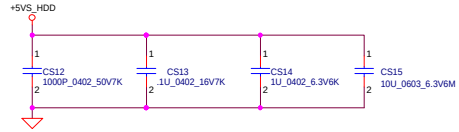
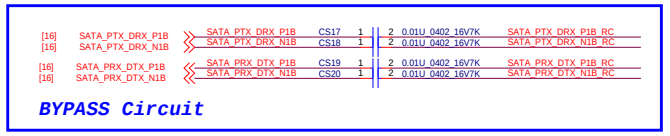
HDD CONN



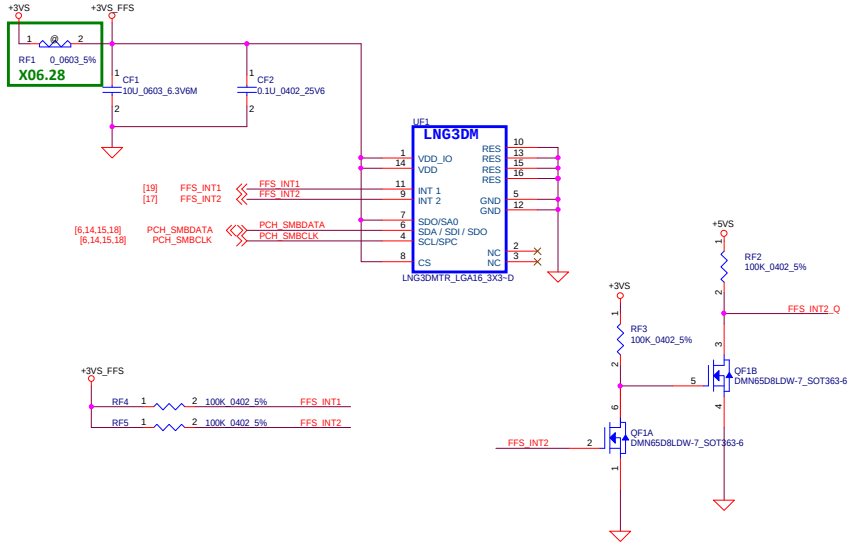
Place near HDD CONN (JHDD1)





BYPASS Circuit

Free Fall Sensor



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **DC/DC INTERFACE**

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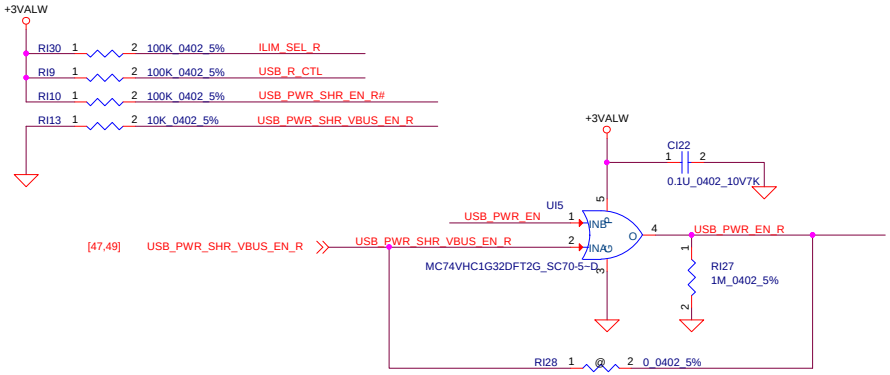
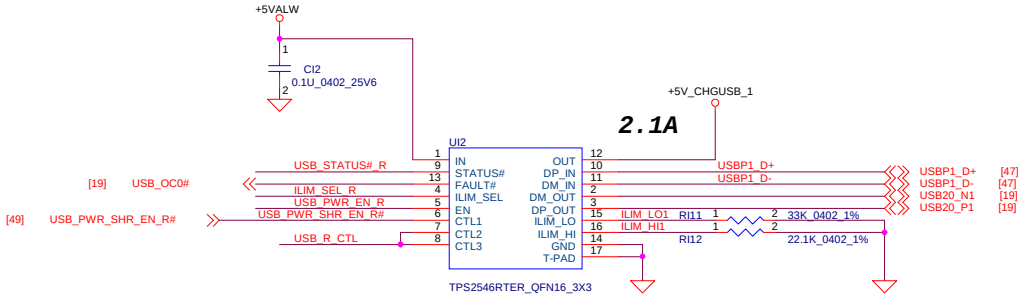
USB Powershare

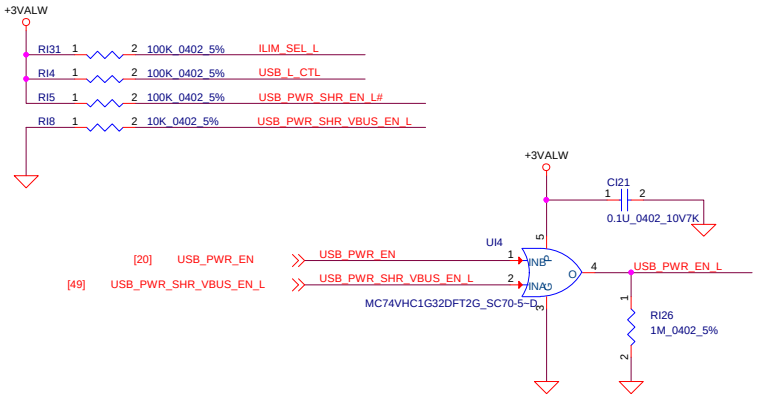
Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

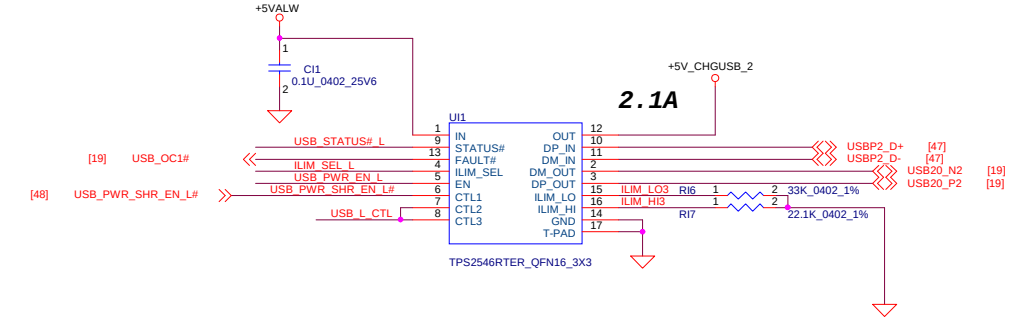


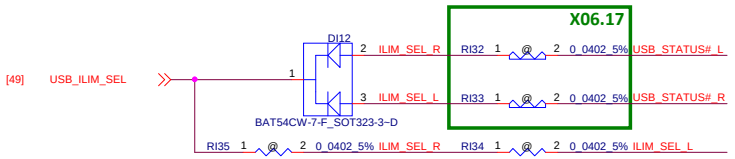
USB3.0 / USB2.0 Port1 (Right Side)





USB3.0 / USB2.0 Port2 (Left Side)





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: USB Powershare

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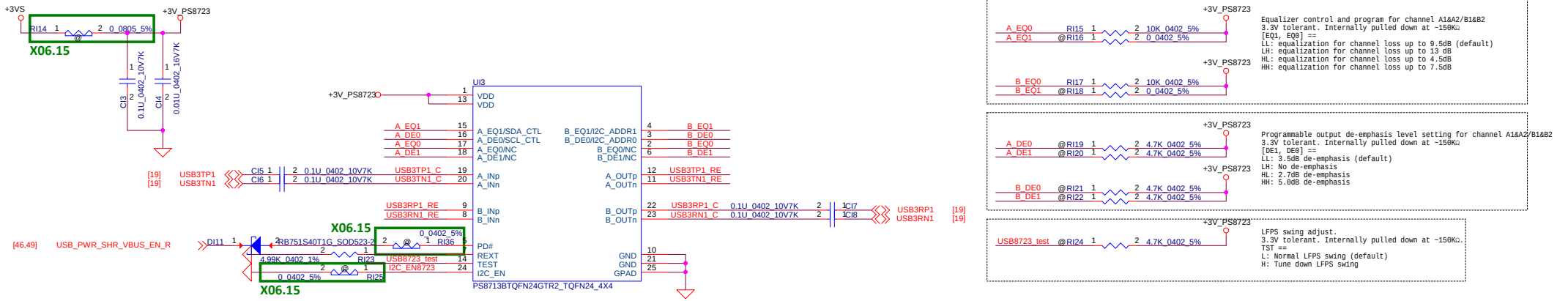
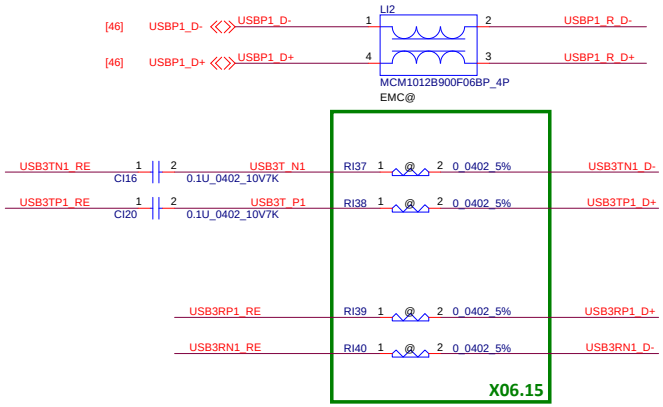
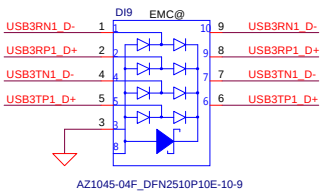
USB3.0 Re-driver

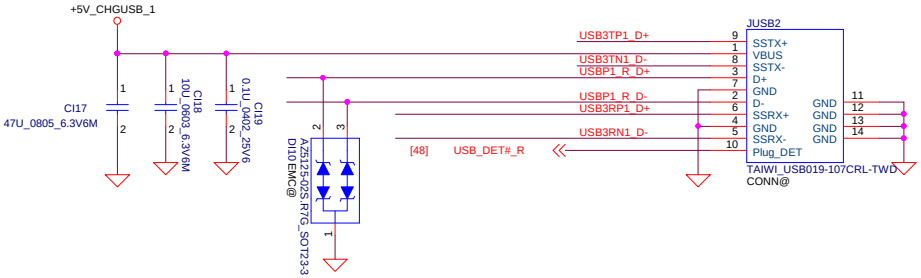


USB3.0 / USB2.0 Port1 (Right Side)

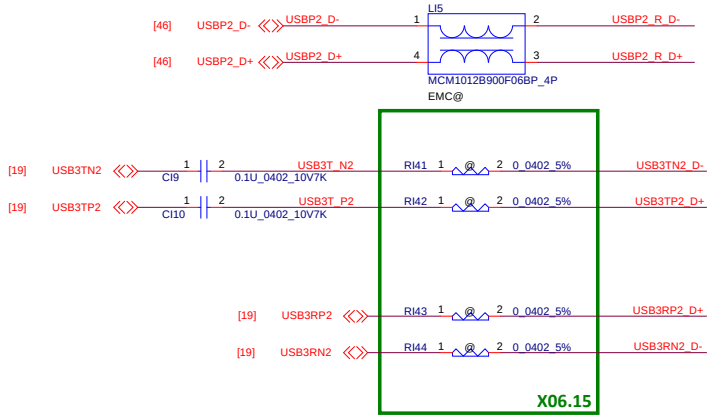


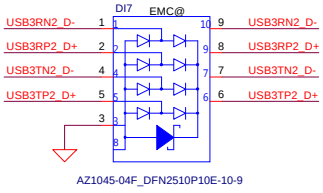


Place close to JUSB2

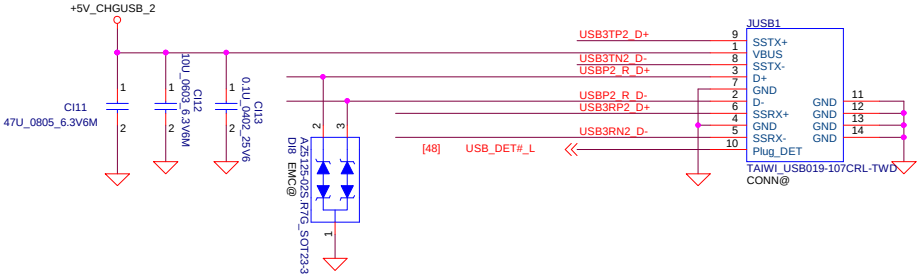


USB3.0 / USB2.0 Port2 (Left Side)





Place close to JUSB1



Compal Electronics, Inc.

Title: USB conn.

Size | Document Number: LA-C361P | Rev: 0.1(X00)

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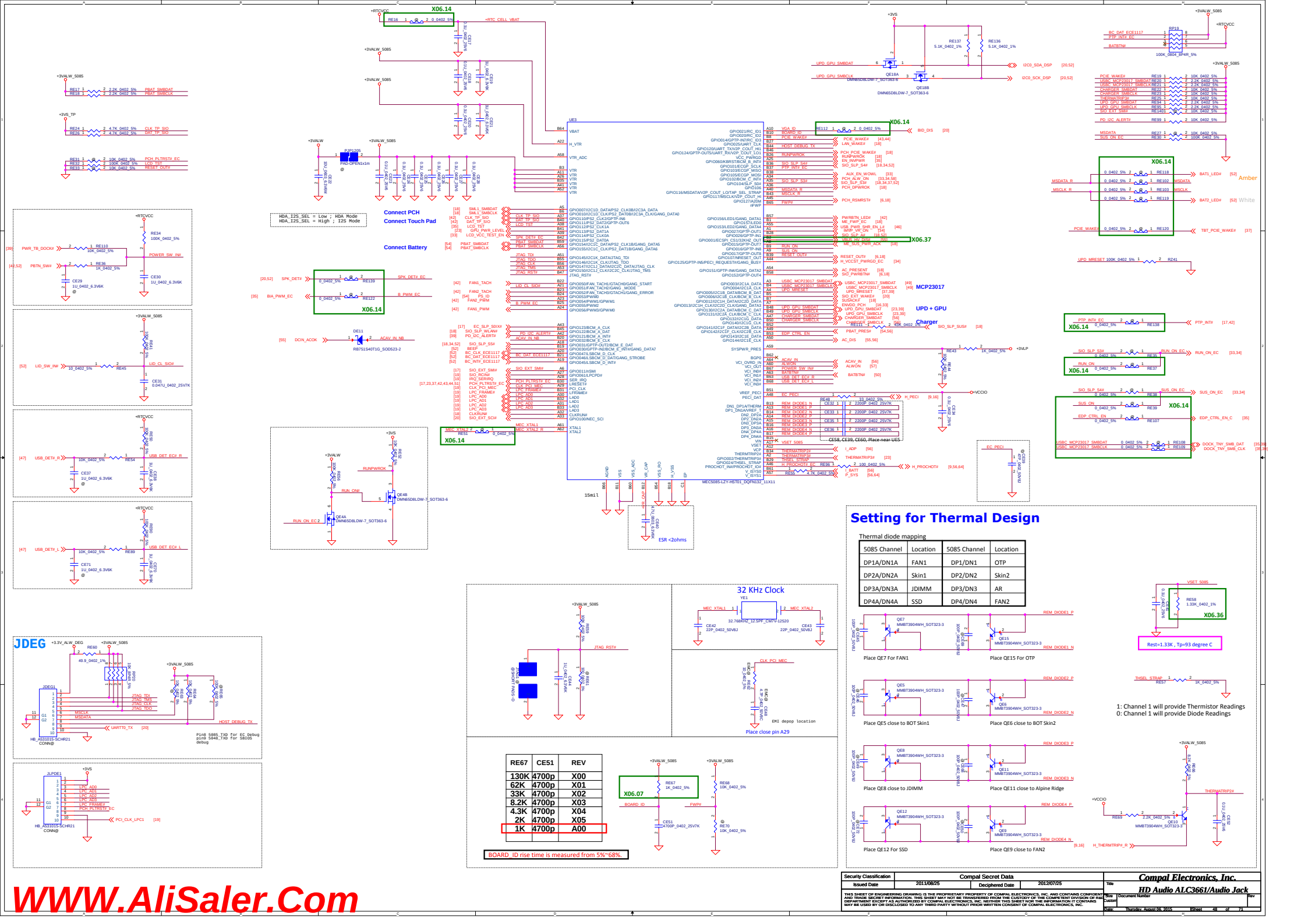

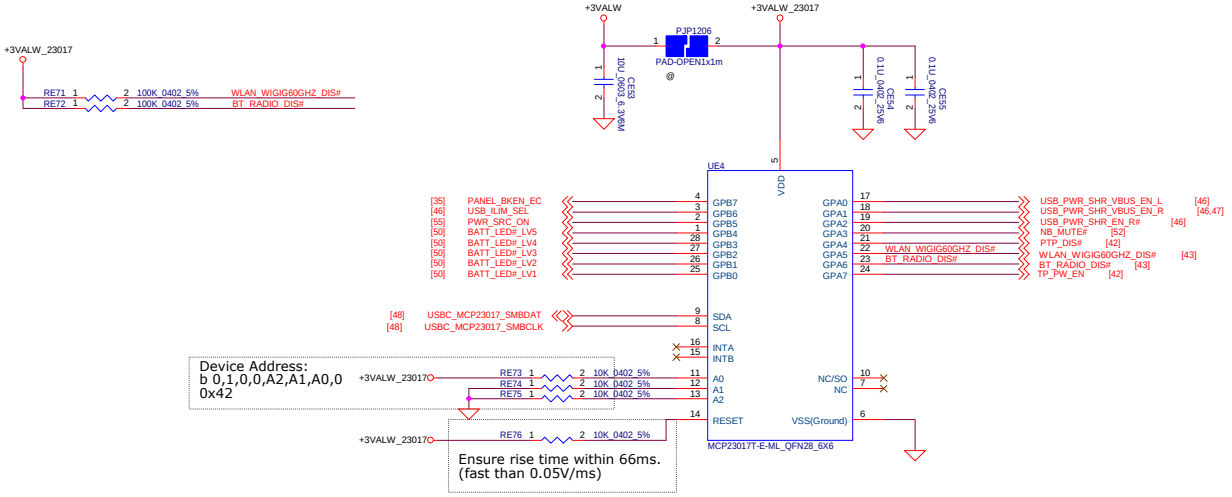

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/21

Compal Electronics, Inc.

Title: AMP TPA3113/SPK conn.

Size	Document Number	Rev
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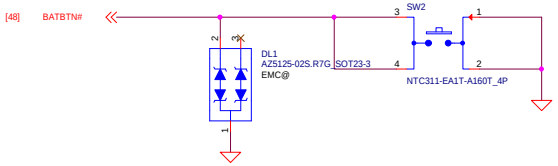
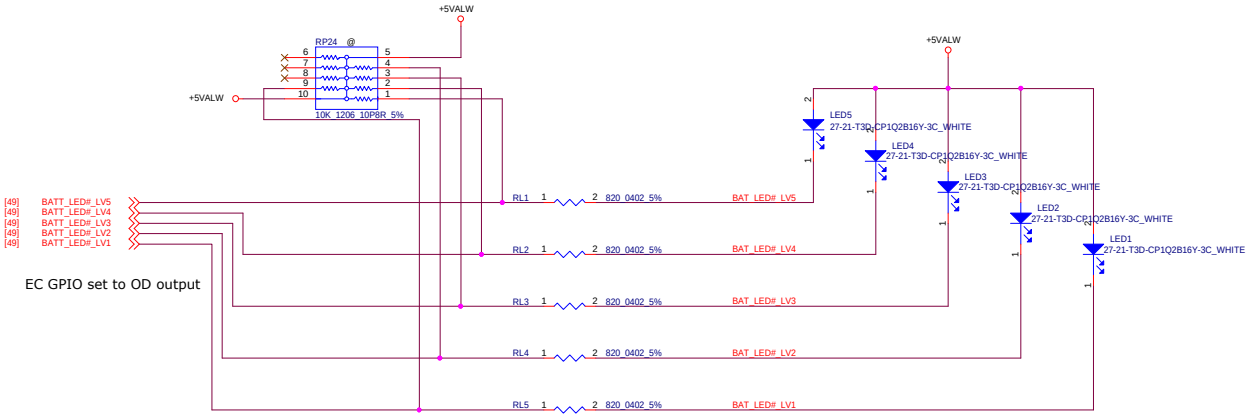
BATT LED Power Button



Battery Gauge LED



EC GPIO set to OD output

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/15
Title	LED indicator		
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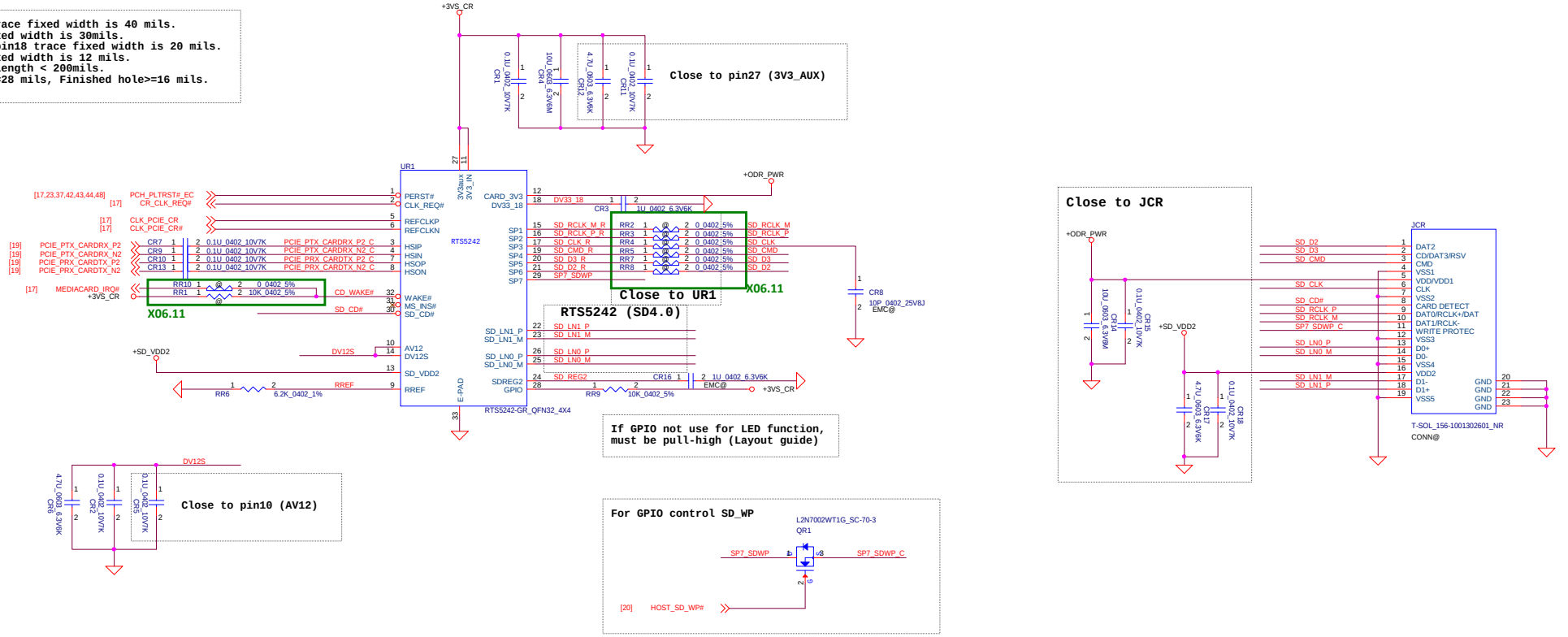
Card Reader

Pin11, Pin12 trace fixed width is 40 mils.
Pin27 trace fixed width is 30mils.
Pin10, pin14, pin18 trace fixed width is 20 mils.
Pin 9 trace fixed width is 12 mils.
Trace routing length < 200mils.
Via size: Pad>=28 mils, Finished hole>=16 mils.



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

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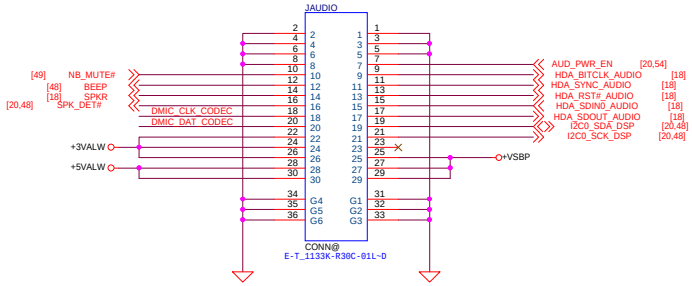
Compal Electronics, Inc.

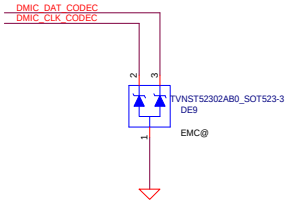
Title: **Card Reader**

Size	Document Number	Rev
		0.1(000)

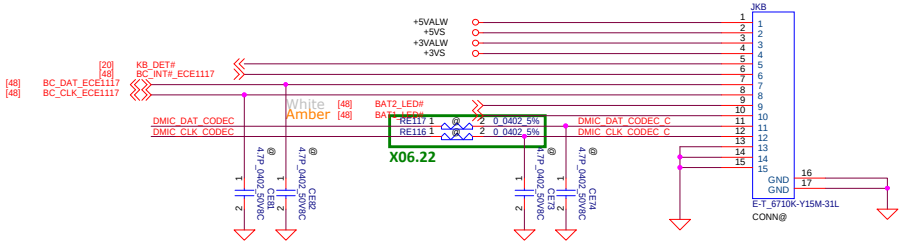
Date: Thursday, August 06, 2015 | Sheet 51 of 71

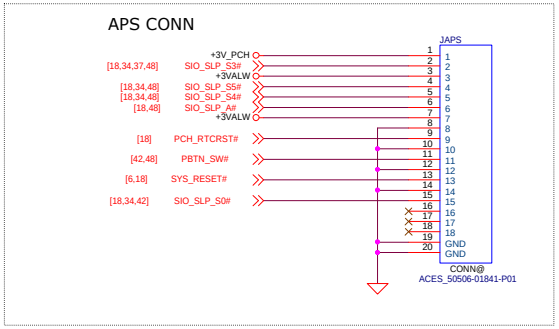
AUDIO Board Conn.

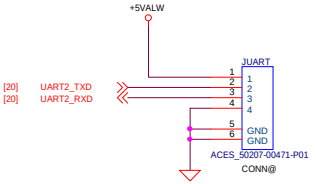




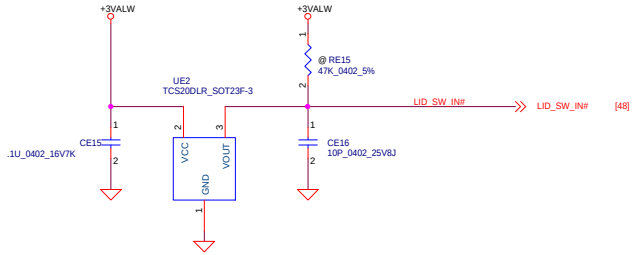
Keyboard Controller board + DMIC



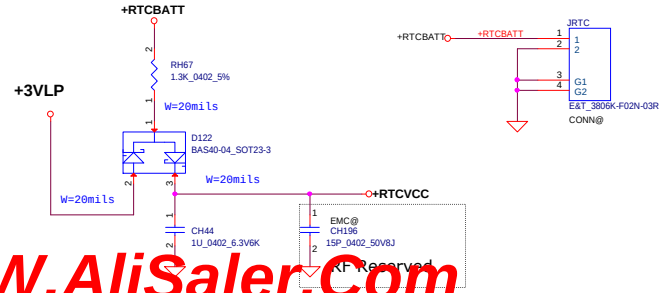




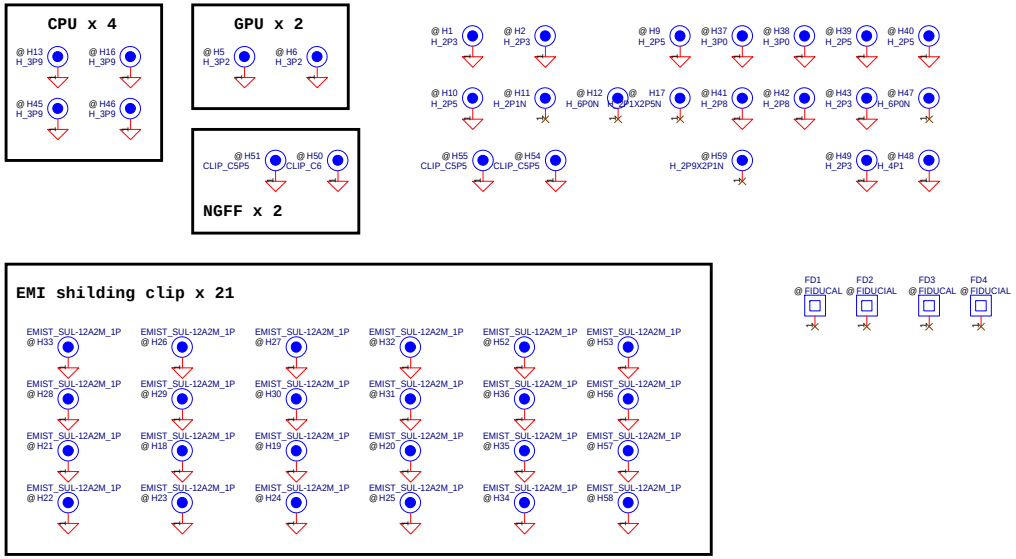
Lid Switch



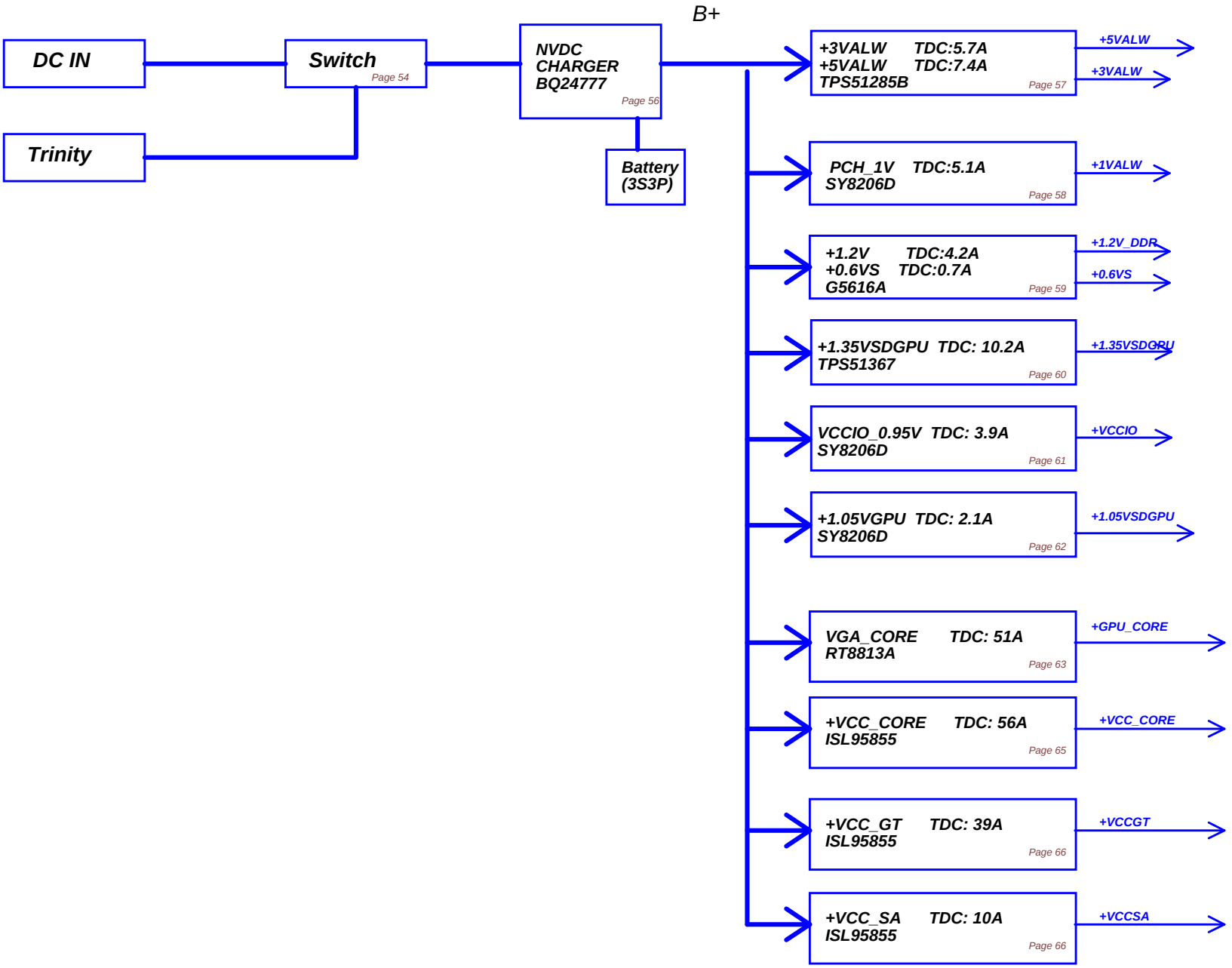
RTC Battery With Charge Function



Screw Hole

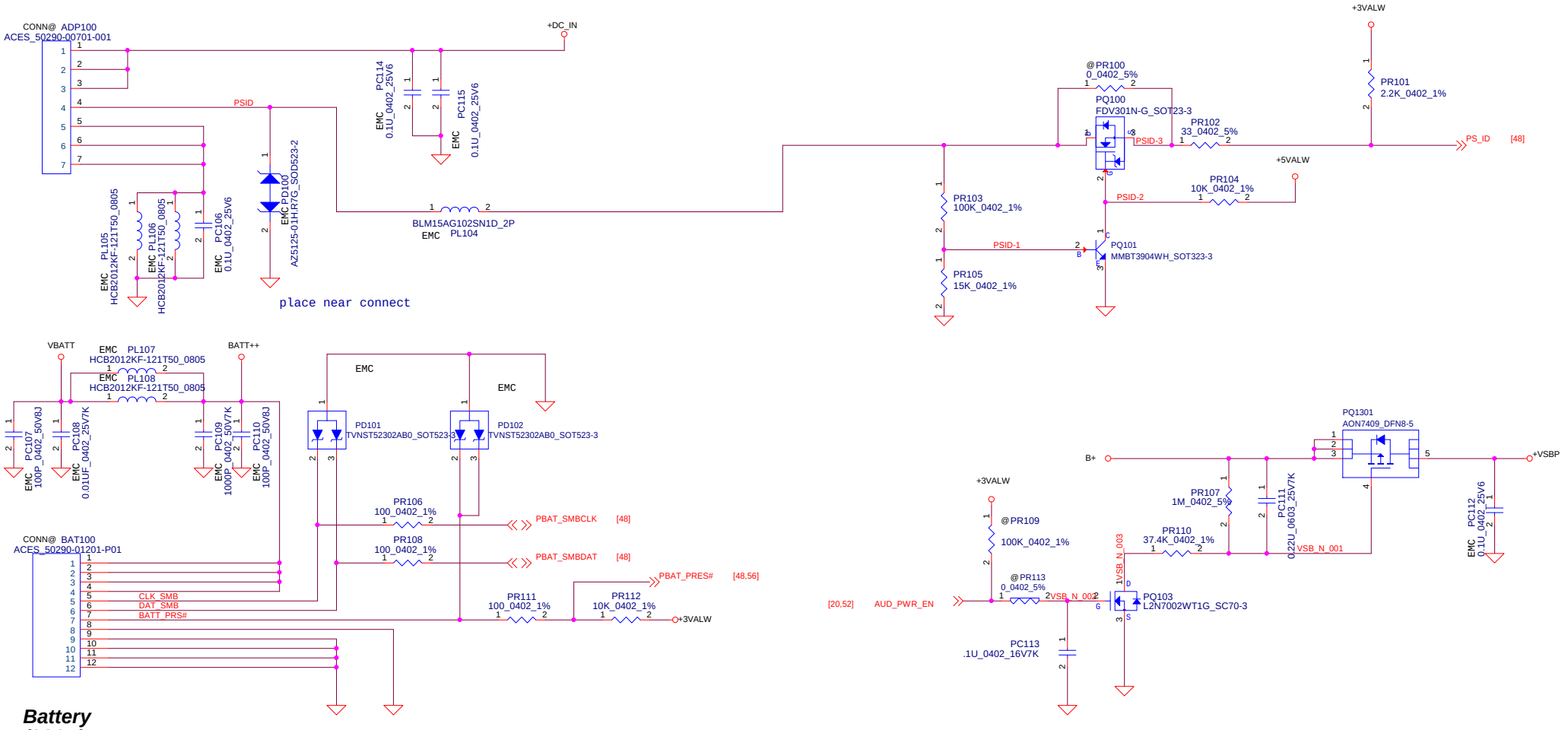


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25
Title	TPM/BTB conn.		
Size	Document Number		Rev
	LA-C361P		0.1(000)
Date:	Thursday, August 06, 2015	Sheet	52 of 71



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date 2012/07/25	Title: Power Sequence diagram

Size	Document Number		Rev 0.1(X00)
Date: Tuesday, August 11, 2015	Sheet 53 of 71		



Battery (3S3P)

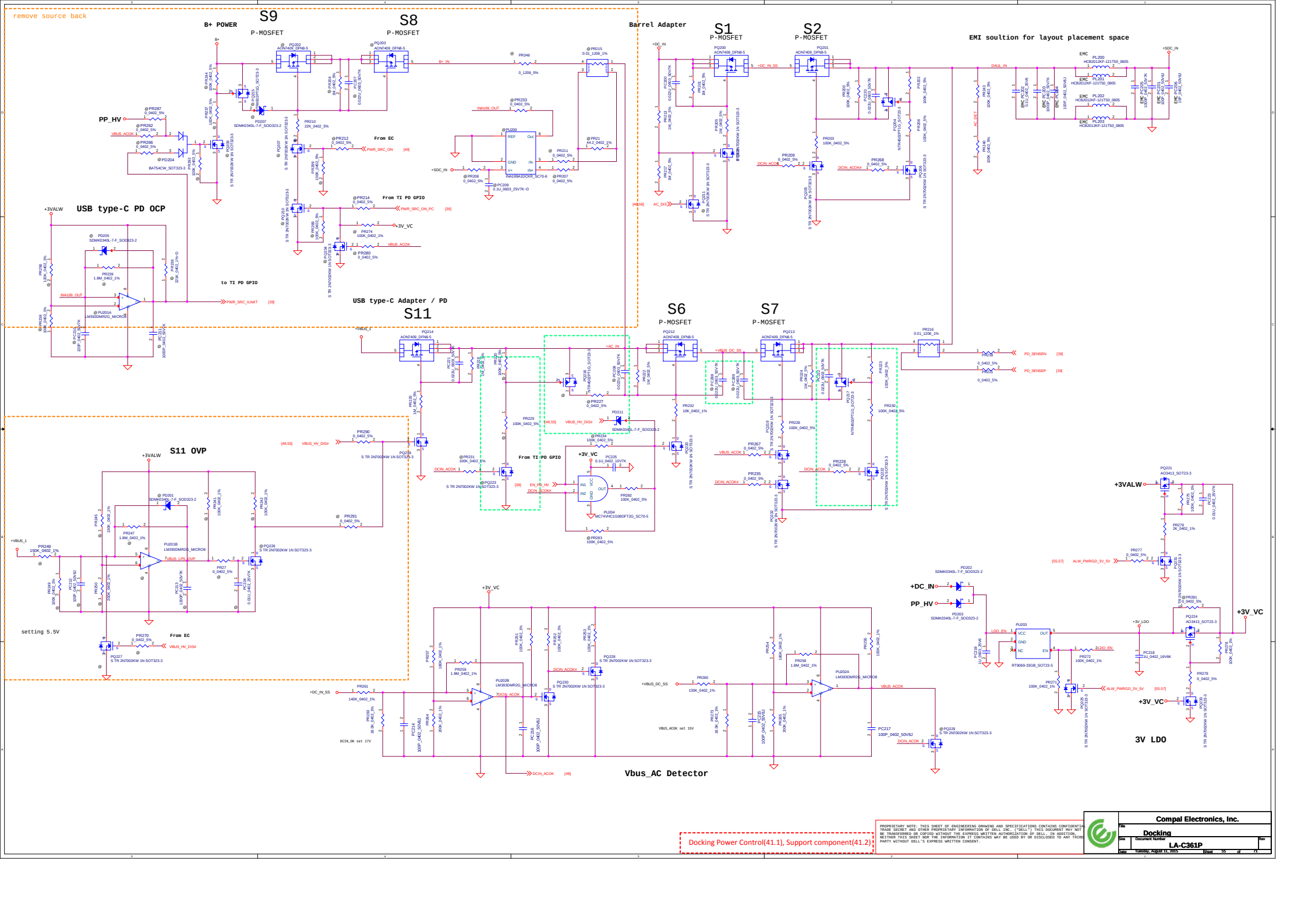
JIMBTY battery connector

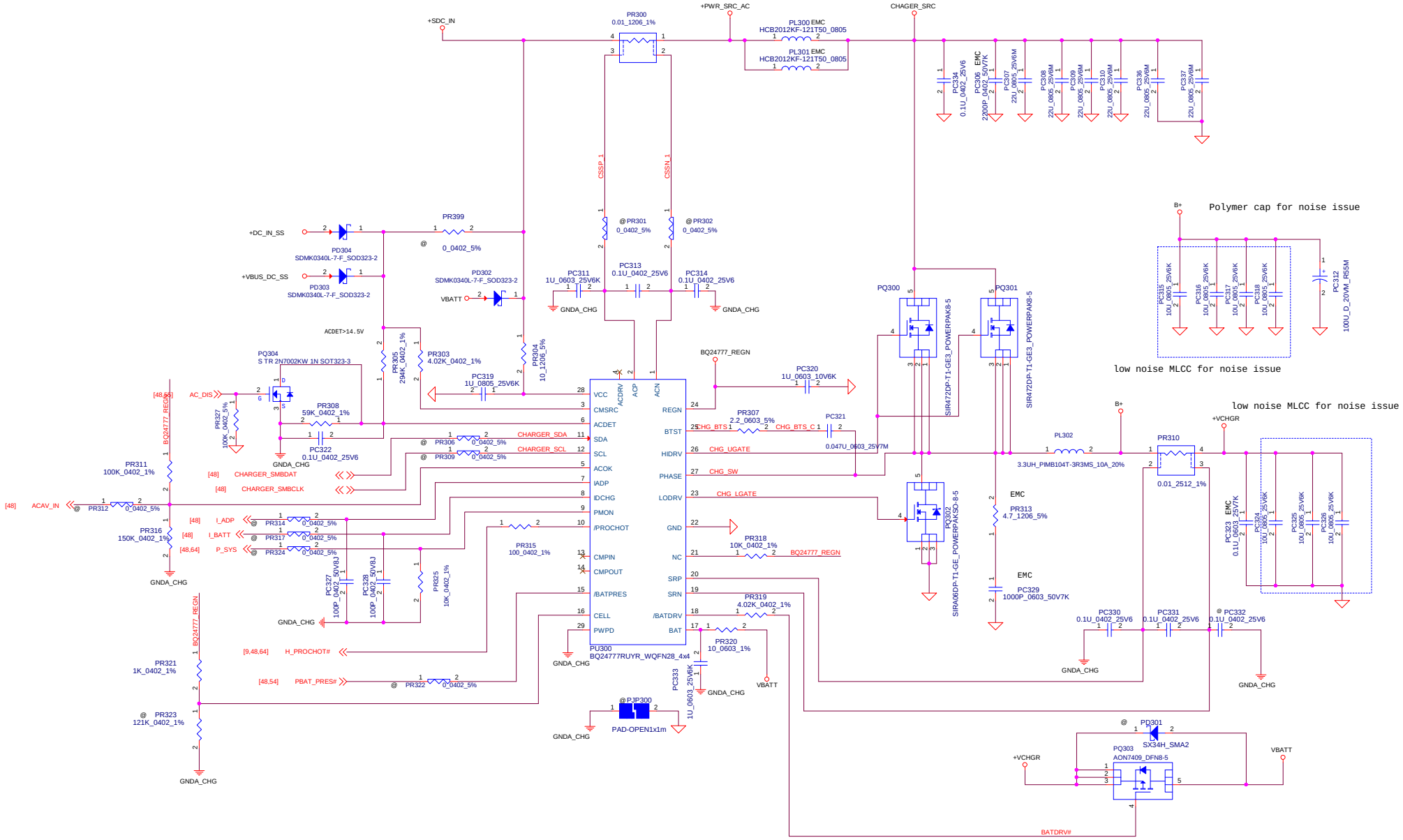
SMART Battery:

01.BAT+
02.BAT+
03.BAT+
04.BAT+
05.CLK_SMB
06.DAT_SMB
07.BATT_PRS
08.SYS_PRS
09.GND
10.GND
11.GND
12.GND

Smart Adapter circuit (39.1)

Compal Electronics, Inc.
Title: PWR-DCIN / BATT CONN / OTP
Size: Document Number: LA-C361P
Rev: 0.1(X00)
Date: Tuesday, August 11, 2015
Sheet 54 of 71


remove source back
B+ POWER
S9
P-MOSFET
S8
P-MOSFET
Barrel Adapter
S1
P-MOSFET
S2
P-MOSFET
EMI soultion for layout placement space
PP_HV
USB type-C PD OCP
to TI PD GPIO
From TI PD GPIO
From EC
USB type-C Adapter / PD
S11
S6
P-MOSFET
S7
P-MOSFET
S11 OVP
setting 5.5V
Vbus_AC Detector
3V LDO
Docking Power Control(41.1), Support component(41.2)
Compal Electronics, Inc.
Docking
LA-C361P
Tuesday, August 11, 2015



Charger controller(40.1), Support component(40.2)

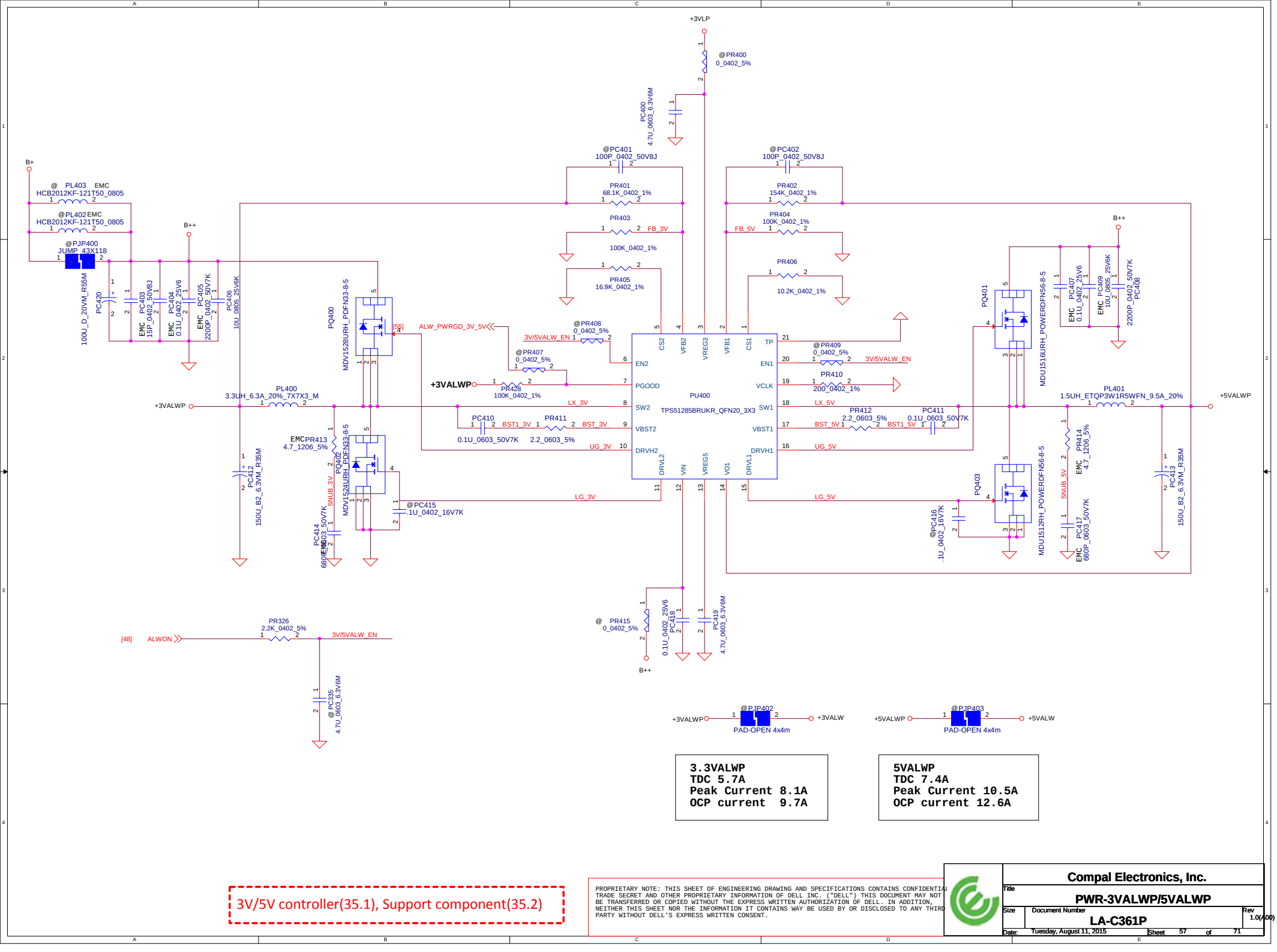
Compal Electronics, Inc.

Title: Charger

Size: Document Number: LA-C361P

Rev: 0.1(X00)

Date: Tuesday, August 11, 2015 Sheet 56 of 71



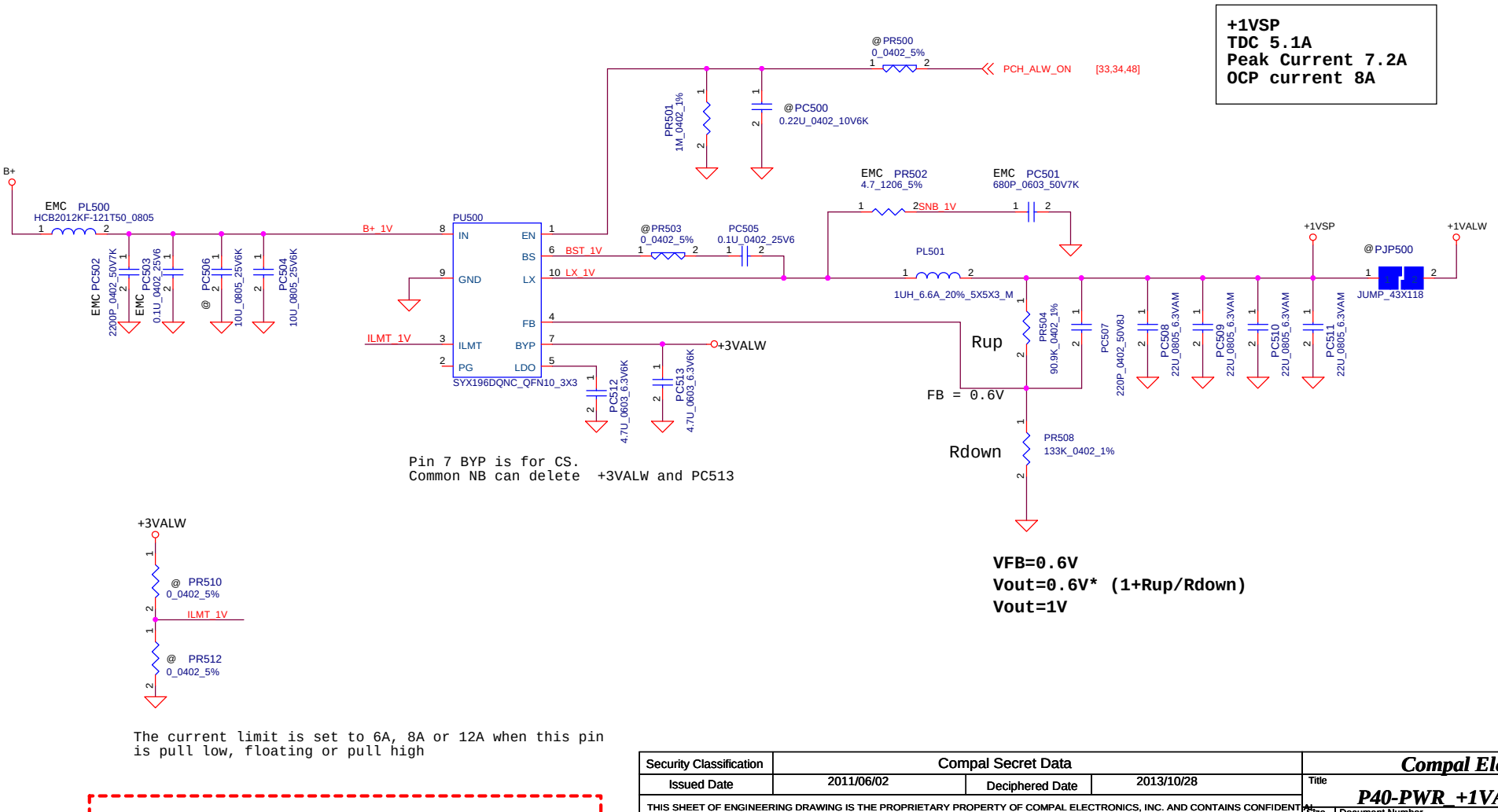
3V/5V controller(35.1), Support component(35.2)

Compal Electronics, Inc.

Title: PWR-3VALWP/5VALWP

Size: | Document Number: LA-C361P | Rev: 1.0(A00)

Date: Tuesday, August 11, 2015 | Sheet 57 of 71



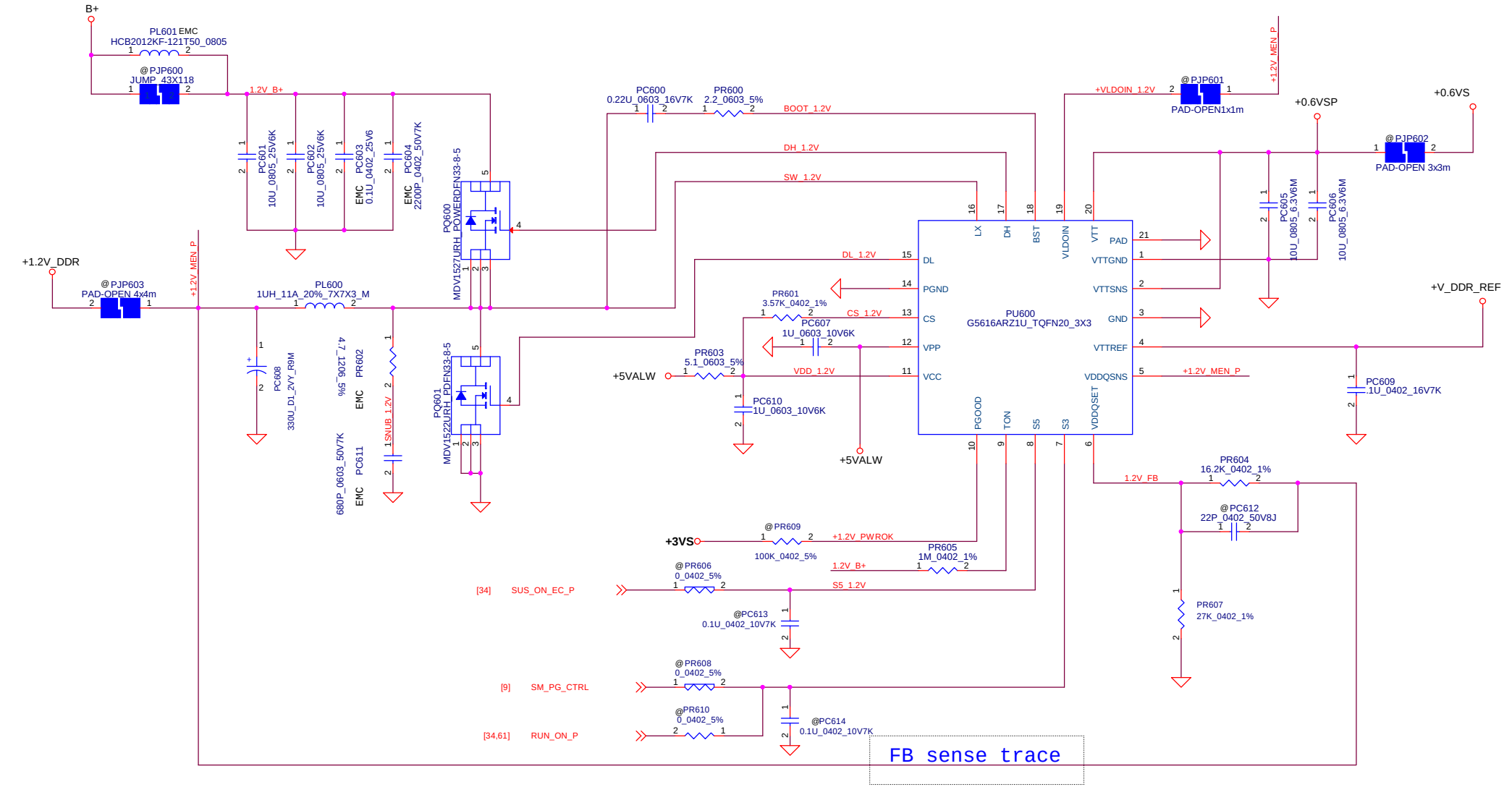
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: P40-PWR_+1VA

Size: A | Document Number: LA-C361P | Rev: 0.1

Date: Tuesday, August 11, 2015 | Sheet 58 of 71



1.2Volt +/- 5%
TDC 4.2A
Peak Current 6A
OCP current 7.2A

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.2A

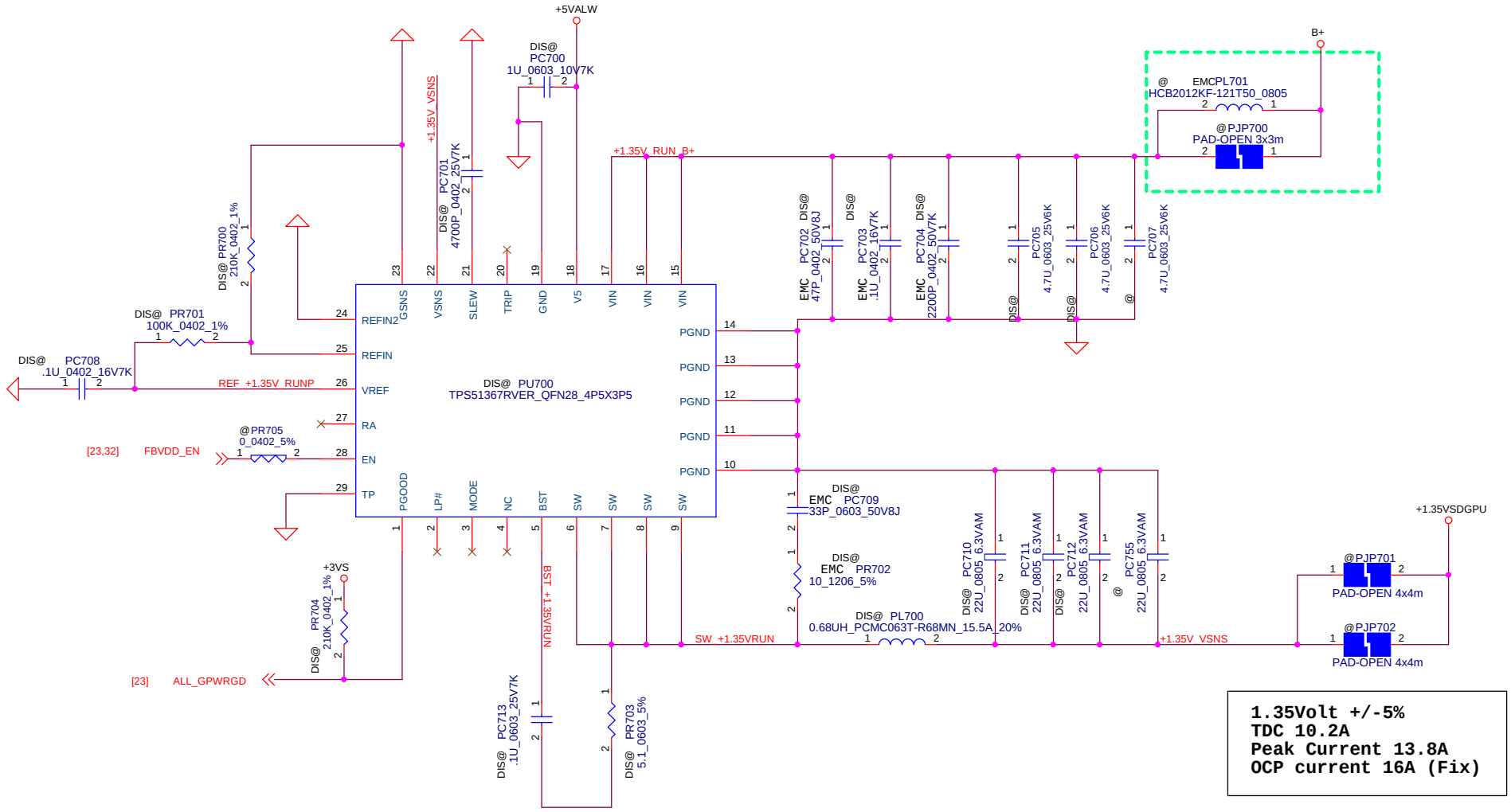
DDR controller(35.3), Support component(35.4)

Compal Electronics, Inc.

Title: +1.35V_MEN/+0.675V_DDR_VTT

Size | Document Number: LA-C361P | Rev: 1.0(A00)

Date: Tuesday, August 11, 2015 | Sheet 59 of 71

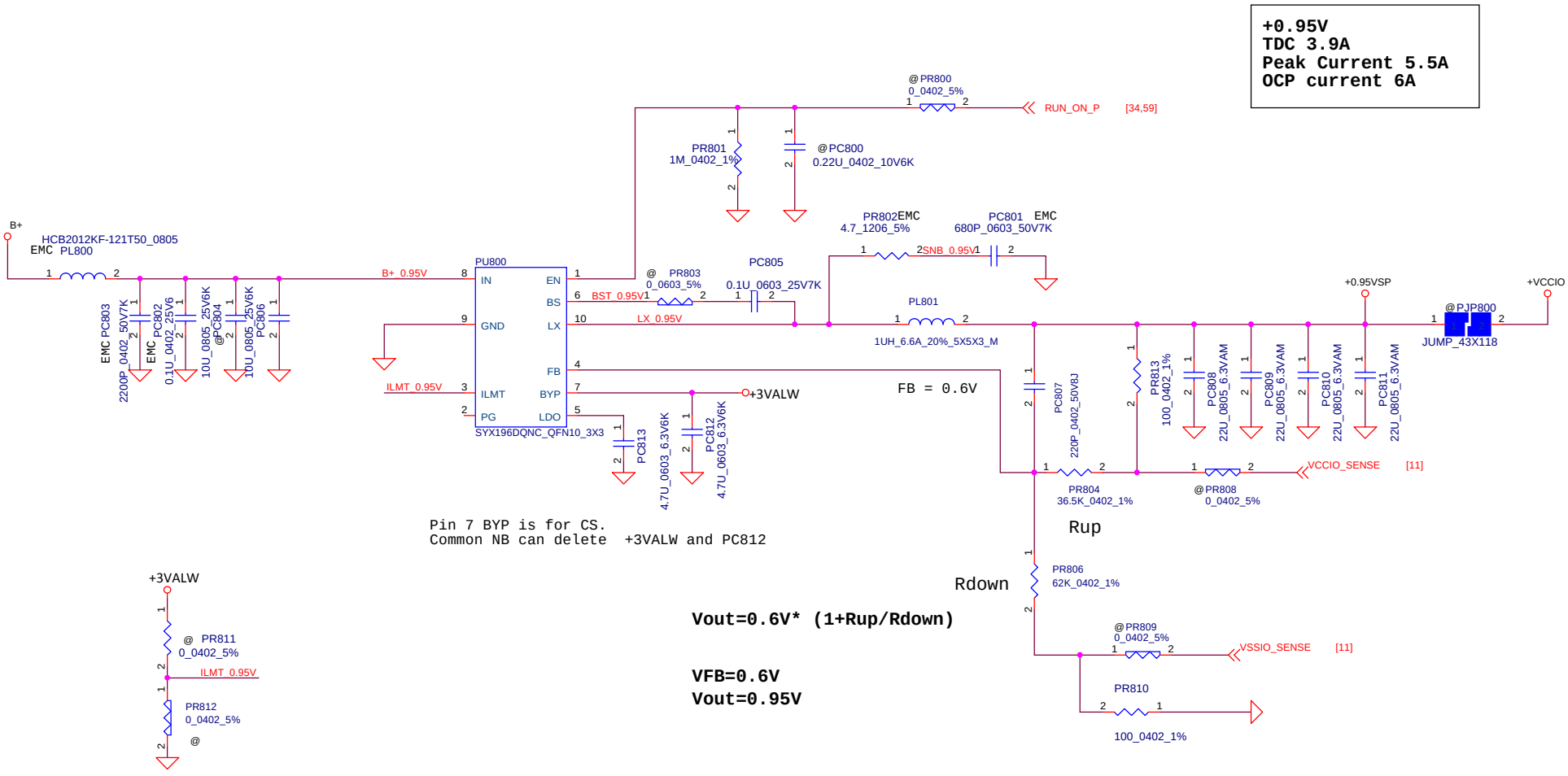


1.35Volt +/-5%
TDC 10.2A
Peak Current 13.8A
OCP current 16A (Fix)

DDR controller(35.3), Support component(35.4)

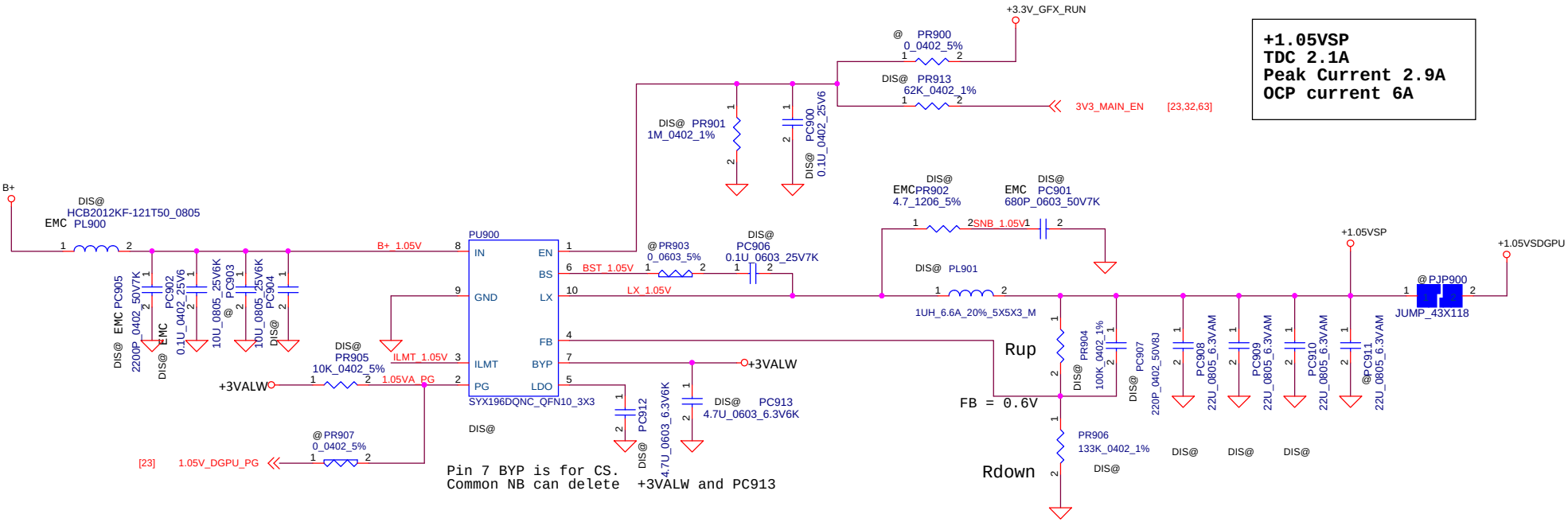
Compal Electronics, Inc.

Title	PWR_+1.5VDGPU	
Size	Document Number: LA-C361P	Rev: 1.0(400)
Date: Tuesday, August 11, 2015	Sheet 60 of 71	



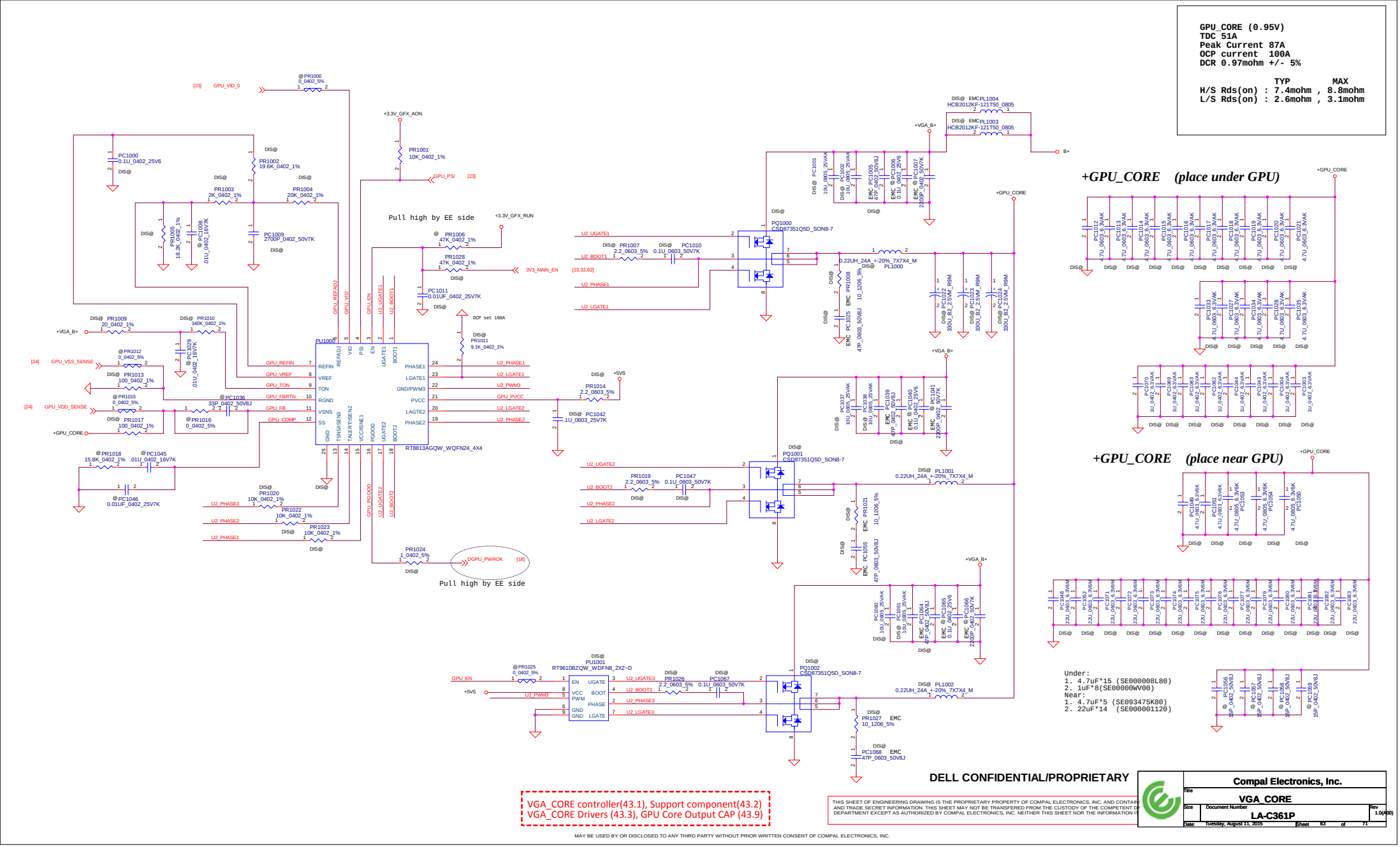
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P40-PWR_+0.95VA			
Size	Document Number: LA-C361P		Rev: 0.1
Date: Tuesday, August 11, 2015	Sheet 61 of 71		



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P40-PWR_+1.05VA			
Size	Document Number: LA-C361P		Rev: 0.1
Date: Tuesday, August 11, 2015	Sheet 62 of 71		


GPU_CORE (0.95V)
TDC 51A
Peak Current 87A
OCP current 100A
DCR 0.97mohm +/- 5%
TYP MAX
H/S Rds(on) : 7.4mohm , 8.8mohm
L/S Rds(on) : 2.6mohm , 3.1mohm
+GPU_CORE (place under GPU)
+GPU_CORE (place near GPU)
Under:
1. 4.7uF*15 (SE000008L80)
2. 1uF*8(SE00000WV00)
Near:
1. 4.7uF*5 (SE093475K80)
2. 22uF*14 (SE000001120)
Pull high by EE side
Pull high by EE side
PU1000
RT8813AGQW_WQFN24_4X4
PU1001
RT9610BZQW_WDFN8_2X2~D
PU1002
PQ1000
CSD87351Q5D_SON8-7
PQ1001
CSD87351Q5D_SON8-7
PU1001
CSD87351Q5D_SON8-7
PL1000
0.22UH_24A_+-20%_7X7X4_M
PL1001
0.22UH_24A_+-20%_7X7X4_M
PL1002
0.22UH_24A_+-20%_7X7X4_M
PL1003
HCB2012KF-121T50_0805
PL1004
HCB2012KF-121T50_0805
VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)
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Compal Electronics, Inc.
VGA_CORE
LA-C361P
1.0(A00)
Tuesday, August 11, 2015
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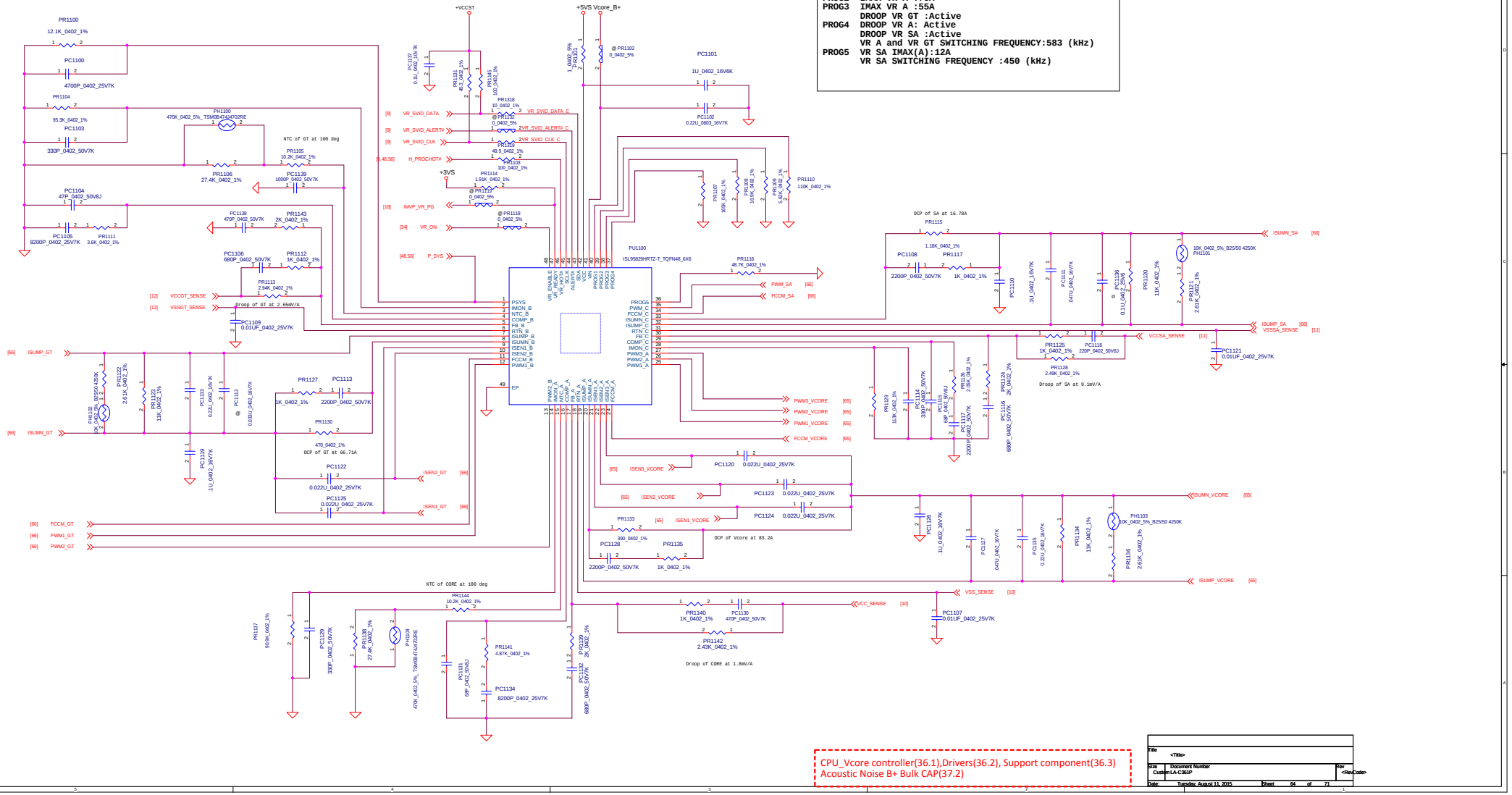
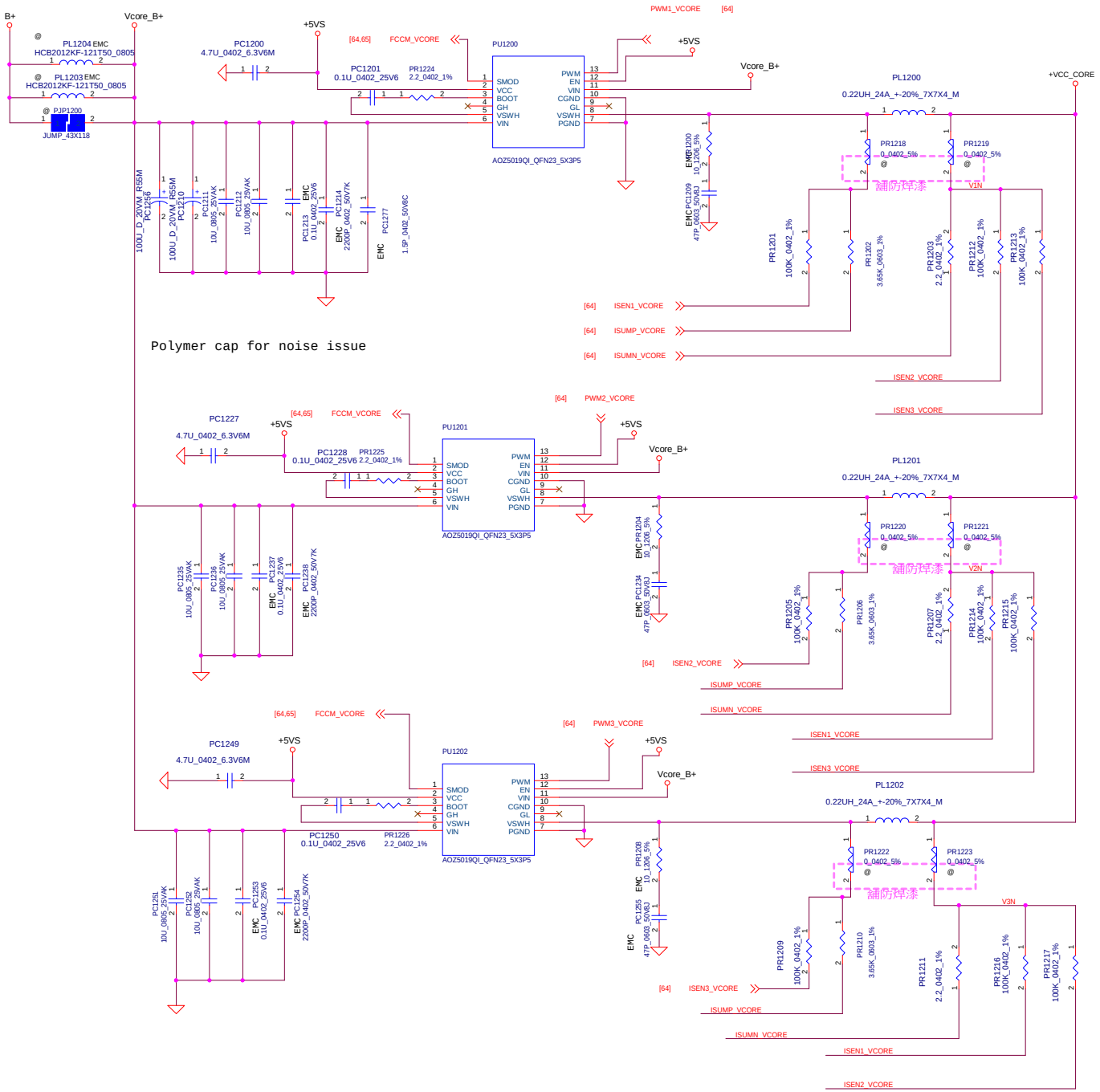
71





VCC_core (Base on PDDG rev 0.7)
PL2 TDC__default):TB
PL2 TDC_max (40Sec):56A
Peak Current 68A
DC Load line -1.8mV/A
AC Load line -1.8mV/A
OCP Current 83.2A
DCR 0.97mohm +/-5%

CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3),
CPU_Core output CAP(36.4),Acoustic Noise B+ Bulk CAP(37.2)

Title	<Title>	
Size C	Document Number LA-C361P	Rev <RevCode>
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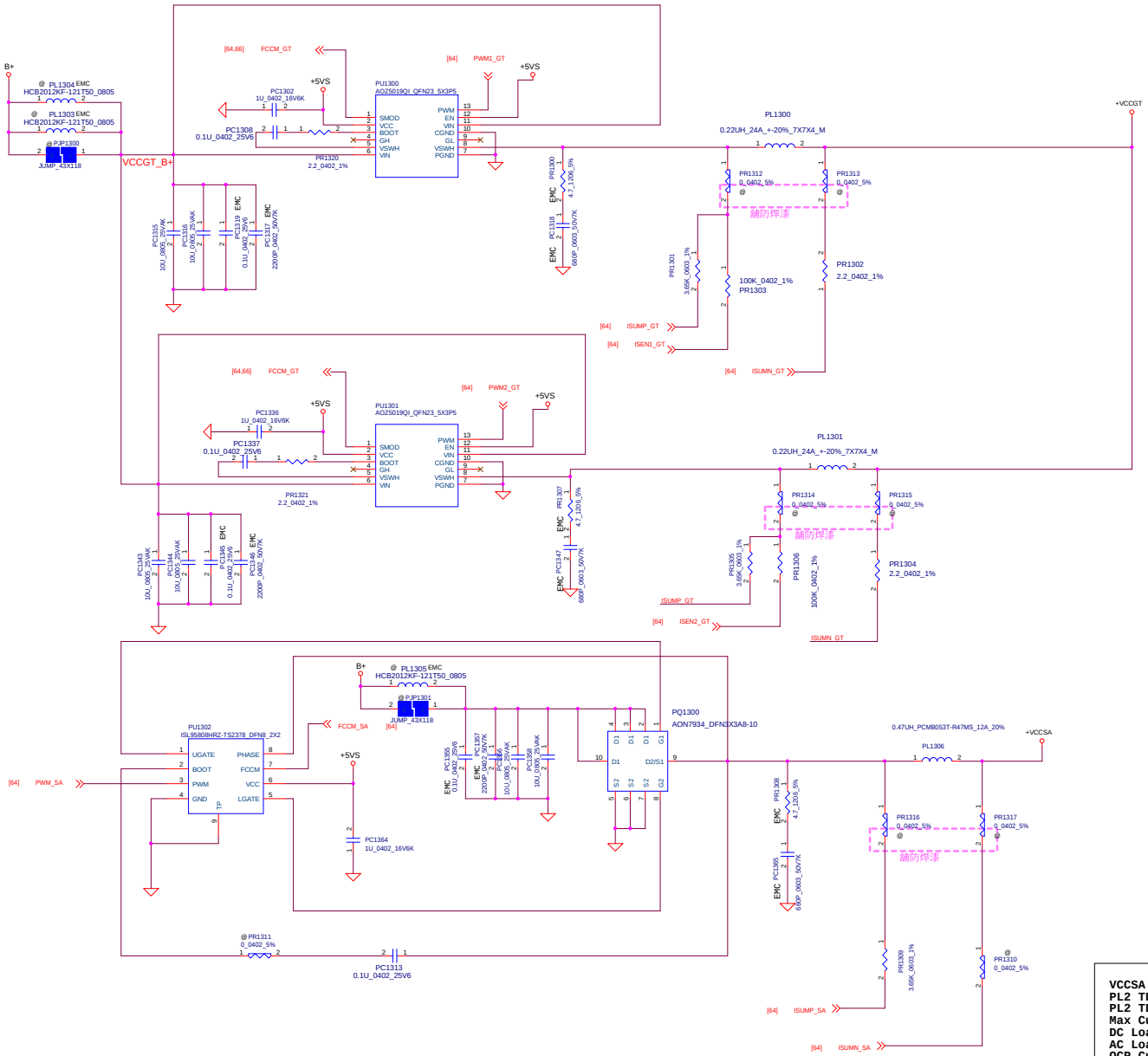

VCCGT (Base on PDDG rev 0.7)
PL2 TDC__default):TB
PL2 TDC_max (40Sec):39A
Max Current 55A
DC Load line -2.65mV/A
AC Load line -2.65mV/A
OCP Current 66.7A
DCR 0.97mohm +/-5%

VCCSA (Base on PDDG rev 0.7)
PL2 TDC__default):TBD
PL2 TDC_max (40Sec):10A
Max Current 11A
DC Load line -9.1mV/A
AC Load line -9.1mV/A
OCP Current 20A
DCR 7.4mohm/8.5mohm +/-5%

CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3), GFX output CAP(36.5)

Title	<Title>
Size	Custom LA-C361P
Document Number	
Rev	<RevCode>
Date:	Tuesday, August 11, 2015
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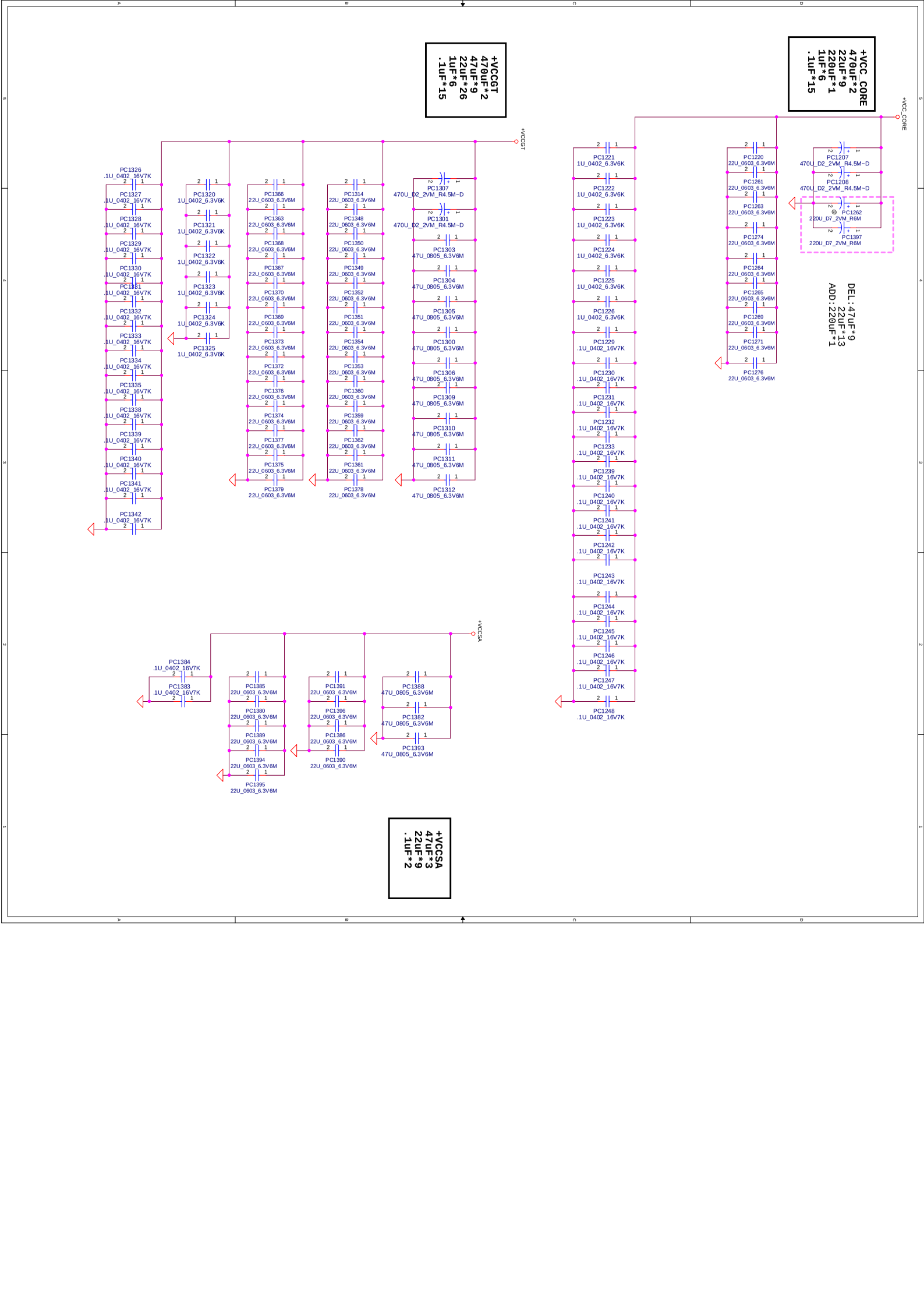
+VCCGT
470uF*2
47uF*9
22uF*26
1uF*6
.1uF*15
+VCC_CORE
470uF*2
22uF*9
220uF*1
1uF*6
.1uF*15
+VCCSA
47uF*3
22uF*9
.1uF*2
DEL:47uF*9
22uF*13
ADD:220uF*1
+VCCGT
+VCC_CORE
+VCCSA
PC1326 .1U_0402_16V7K
PC1327 .1U_0402_16V7K
PC1328 .1U_0402_16V7K
PC1329 .1U_0402_16V7K
PC1330 .1U_0402_16V7K
PC1331 .1U_0402_16V7K
PC1332 .1U_0402_16V7K
PC1333 .1U_0402_16V7K
PC1334 .1U_0402_16V7K
PC1335 .1U_0402_16V7K
PC1338 .1U_0402_16V7K
PC1339 .1U_0402_16V7K
PC1340 .1U_0402_16V7K
PC1341 .1U_0402_16V7K
PC1342 .1U_0402_16V7K
PC1320 1U_0402_6.3V6K
PC1321 1U_0402_6.3V6K
PC1322 1U_0402_6.3V6K
PC1323 1U_0402_6.3V6K
PC1324 1U_0402_6.3V6K
PC1325 1U_0402_6.3V6K
PC1366 22U_0603_6.3V6M
PC1363 22U_0603_6.3V6M
PC1368 22U_0603_6.3V6M
PC1367 22U_0603_6.3V6M
PC1370 22U_0603_6.3V6M
PC1369 22U_0603_6.3V6M
PC1373 22U_0603_6.3V6M
PC1372 22U_0603_6.3V6M
PC1376 22U_0603_6.3V6M
PC1374 22U_0603_6.3V6M
PC1377 22U_0603_6.3V6M
PC1375 22U_0603_6.3V6M
PC1379 22U_0603_6.3V6M
PC1314 22U_0603_6.3V6M
PC1348 22U_0603_6.3V6M
PC1350 22U_0603_6.3V6M
PC1349 22U_0603_6.3V6M
PC1352 22U_0603_6.3V6M
PC1351 22U_0603_6.3V6M
PC1354 22U_0603_6.3V6M
PC1353 22U_0603_6.3V6M
PC1360 22U_0603_6.3V6M
PC1359 22U_0603_6.3V6M
PC1362 22U_0603_6.3V6M
PC1361 22U_0603_6.3V6M
PC1378 22U_0603_6.3V6M
PC1307 470U_D2_2VM_R4.5M~D
PC1301 470U_D2_2VM_R4.5M~D
PC1303 47U_0805_6.3V6M
PC1304 47U_0805_6.3V6M
PC1305 47U_0805_6.3V6M
PC1300 47U_0805_6.3V6M
PC1306 47U_0805_6.3V6M
PC1309 47U_0805_6.3V6M
PC1310 47U_0805_6.3V6M
PC1311 47U_0805_6.3V6M
PC1312 47U_0805_6.3V6M
PC1221 1U_0402_6.3V6K
PC1222 1U_0402_6.3V6K
PC1223 1U_0402_6.3V6K
PC1224 1U_0402_6.3V6K
PC1225 1U_0402_6.3V6K
PC1226 1U_0402_6.3V6K
PC1229 .1U_0402_16V7K
PC1230 .1U_0402_16V7K
PC1231 .1U_0402_16V7K
PC1232 .1U_0402_16V7K
PC1233 .1U_0402_16V7K
PC1239 .1U_0402_16V7K
PC1240 .1U_0402_16V7K
PC1241 .1U_0402_16V7K
PC1242 .1U_0402_16V7K
PC1243 .1U_0402_16V7K
PC1244 .1U_0402_16V7K
PC1245 .1U_0402_16V7K
PC1246 .1U_0402_16V7K
PC1247 .1U_0402_16V7K
PC1248 .1U_0402_16V7K
PC1220 22U_0603_6.3V6M
PC1261 22U_0603_6.3V6M
PC1263 22U_0603_6.3V6M
PC1274 22U_0603_6.3V6M
PC1264 22U_0603_6.3V6M
PC1265 22U_0603_6.3V6M
PC1269 22U_0603_6.3V6M
PC1271 22U_0603_6.3V6M
PC1276 22U_0603_6.3V6M
PC1207 470U_D2_2VM_R4.5M~D
PC1208 470U_D2_2VM_R4.5M~D
PC1262 220U_D7_2VM_R6M
PC1397 220U_D7_2VM_R6M
PC1384 .1U_0402_16V7K
PC1383 .1U_0402_16V7K
PC1385 22U_0603_6.3V6M
PC1380 22U_0603_6.3V6M
PC1389 22U_0603_6.3V6M
PC1394 22U_0603_6.3V6M
PC1395 22U_0603_6.3V6M
PC1391 22U_0603_6.3V6M
PC1396 22U_0603_6.3V6M
PC1386 22U_0603_6.3V6M
PC1390 22U_0603_6.3V6M
PC1388 47U_0805_6.3V6M
PC1382 47U_0805_6.3V6M
PC1393 47U_0805_6.3V6M

Version Change List (P. I. R. List)

Page 1

Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Version Change List (P. I. R. List)   Page 1

Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	XDP	2014/12/12	EE	Change Pull high power for leakage issue	Change RH494,RH495,RH496 from +VCCST to +VCCSTG, de-POP RH97,RH98,RH100, POP RH494,RH495.	X01
2	18	GPIO	2014/12/12	EE	Change Pull high power for double pull high the same power rail	Change RH571 power rail from +3VS to +3V_PCH, de-pop RH571, delete RH532.	X01
3	18	SPI	2014/12/12	EE	Change SPI ROM for ME register setting	Change UH8 from W25Q128FVSIG_SO8 to W25Q128FVSIQ_SO8	X01
4	18	S0iX	2014/12/12	EE	Change by pass circuit design for CS mode function	Change RZ58 connection from UZ11.2 to UZ11.4, Change RZ60 connection from UZ12.2 to UZ12.4	X01
5	18	+1V_MPHY	2014/12/12	EE	Delete +1V_MPHY load switch & discharge circuit for useless.	Delete RH514,RH559,RH144,QH9,UH13,CH193,CH194,CH195. Delete net MPHYP_PWR_EN, move RZ70 to page 21	X01
6	18	PD	2014/12/22	EE	Update TI PD controller circuit follow Mirama	Update UT5 from W25Q80BLZPIG_WSON8 to W25Q80DVSSIG_SO8,Delete RT166,Change net VCC3V3_TBTA_LDO to VCC3V3_FLASH. Change net VCC3V3_SX_SYS to +3VA_TBT. Add RT198 to PWR_SRC_ILIMIT.Swap UT4.B2/C2 net. Update RT165 from 1206 to 0805, RT167,RT168, RT169.RT170,RT171,RT179,RT186,RT187,RT188,RT189,RT192,RT192,RT196,RT197 from 0402 to 0201. Add RT200,RT201 to net UPD_SMBDAT/UPD_SMBCLK"	X01 X01
7	18	EC	2014/12/15	EE	Update Board ID for EC	Update RE67 to 62K	X01
8	18	PM	2014/12/15	EE	modify for support deep sleep function	De-pop RH506	X01
9	18	DDR	2014/12/15	EE	change Power rail for correct design	Change RH525 power rail from +3VALW to +3VS	X01
10	18	SPK	2014/12/15	EE	Add pull high resistor for MB side	Add RH572 to +3VS for SPK_DET#	X01
11	18	GPIO	2014/12/15	EE	Change GPIO for sync common GPIO table	Change net DGPU_PWR_EN from GPP_D13 to GPP_D12	X01
12	18	PD	2014/12/15	EE	Pin swap for DFB review	pin swap DT4,DT9	X01
13	18	PCH	2014/12/15	EE	Add Capacitor for follow Schematic check list	Add CH200 to +3V_PCH (Close to UH2.BA15)	X01
14	18	DIS	2014/12/15	EE	Add pull high resistor by vendor request	Add RPH34 replace to RV520,RV521,RV522 and add net THERMAL_ALERT#.	X01
15	18	SPI	2014/12/15	EE	Follow CRB XDP design	Add RH574,RH575 for SPI to XDP connector	X01
16	18	VDDQC	2014/12/16	EE	Follow CRB boardfile	POP RH473	X01
17	18	DEBUG	2014/12/16	EE	Add Debug signal by EC request	Change net BID_BC to GPP_C15, Add Net UARTT0_TX from GPP_C9 to JDEG1.pin 9	X01
18	18	DEBUG	2014/12/16	EE	Modify Debug UART from closed Chassis to Open Chassis	Delet UI6,RI29.Add JUART for UART2_TXD/UART2_RXD connect.	X01
19	18	SCI	2014/12/16	EE	Change PU resistor follow Miramar	RH383 change from 100K to 10K	X01
20	18	HOLE	2014/12/16	EE	Add 2 PAD for ME NUT	Add H50, H51	X01
21	18	EC	2014/12/16	EE	Add series resistor follow CRB	Add RE111 43K series SIO_SLP_SUS#	X01
22	18	PCH	2014/12/16	EE	Change BOM to follow CRB	Change RH88 from 10K to 47K, De-POP RE33.	X01
23	18	EC	2014/12/17	EE	Modify GPIO for follow GPIO MAP by Dell	Add RE112 and Connect net BID_DIS to UE3.A10, swap Net BAT1_LED#(UE3.B1=>UE3.A40)/BAT2_LED#(UE3.A55=>UE3.B43)/ PCH_PCIE_WAKE#(UE3.A40=>UE3.B46)/ME_FWP_EC(UE3.B46=>UE3.B1)/USB_PWR_SHR_LFT_EN#(UE3.B43=>UE3.A55)	X01
24	18	EC	2014/12/17	EE	Update BOM for design change	de-POP RE27, RE63, POP RH453	X01
25	18	NGFF	2014/12/17	EE	Update NGFF from Key E. to Key A.	Change JNGFF1 to CONCR_213AAAA32FA	
26	18	PCH	2014/12/17	EE	Change array resistor to resistor for routing	Change RP21 to RH576,RH577,RH578,RH579. Add RE113,RE114,RE115 for UE1.	
27	18	USB	2014/12/18	EE	Change net name by EC request	USB_PWR_SHR_VBUS_LFT_EN -> USB_PWR_SHR_VBUS_EN_L, USB_PWR_SHR_VBUS_RHT_EN1 -> USB_PWR_SHR_VBUS_EN_R, USB_PWR_SHR_LFT_EN# -> USB_PWR_SHR_EN_L#, USB_PWR_SHR_RHT_EN1# -> USB_PWR_SHR_EN_R#, USB2_DET_EC# -> USB_DET_EC_L#, USB1_DET_EC# -> USB_DET_EC_R#	
28	18	TS	2014/12/18	EE	Update Touch Screen Connector by ME request	Update JTS to ACES_50208-00601-P01	
29	18	USB	2014/12/18	EE	Add Pull down resistor for USB2.0	Add RH580,RH581 to UH2.AD10,UH2.AG2 to GND	
30	18	AR	2014/12/19	EE	Reserve test point for Alpine Ridge	Add T199,T200,T201	
31	18	PD	2014/12/22	EE	Delete commmon mode chok & ESD for vendor feedback	Delete LT10,DT5	
32	18	EC	2014/12/22	EE	Delete I2C signal from EC to Codec.	Delete QE14	
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