1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
				2012-02-23

SCHEM,MLB,J13

2/23/12

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9277	1	SCHEM,MLB,J13	SCH	CRITICAL	
820-3209	1	PCBF,MLB,J13	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Thu Feb 23 17:52:06 2012

DRAWING TITLE: SCHEM,MLB,J13

Apple Inc.

DRAWING NUMBER: 051-9277 | SIZE: D

REVISION: 2.8.0

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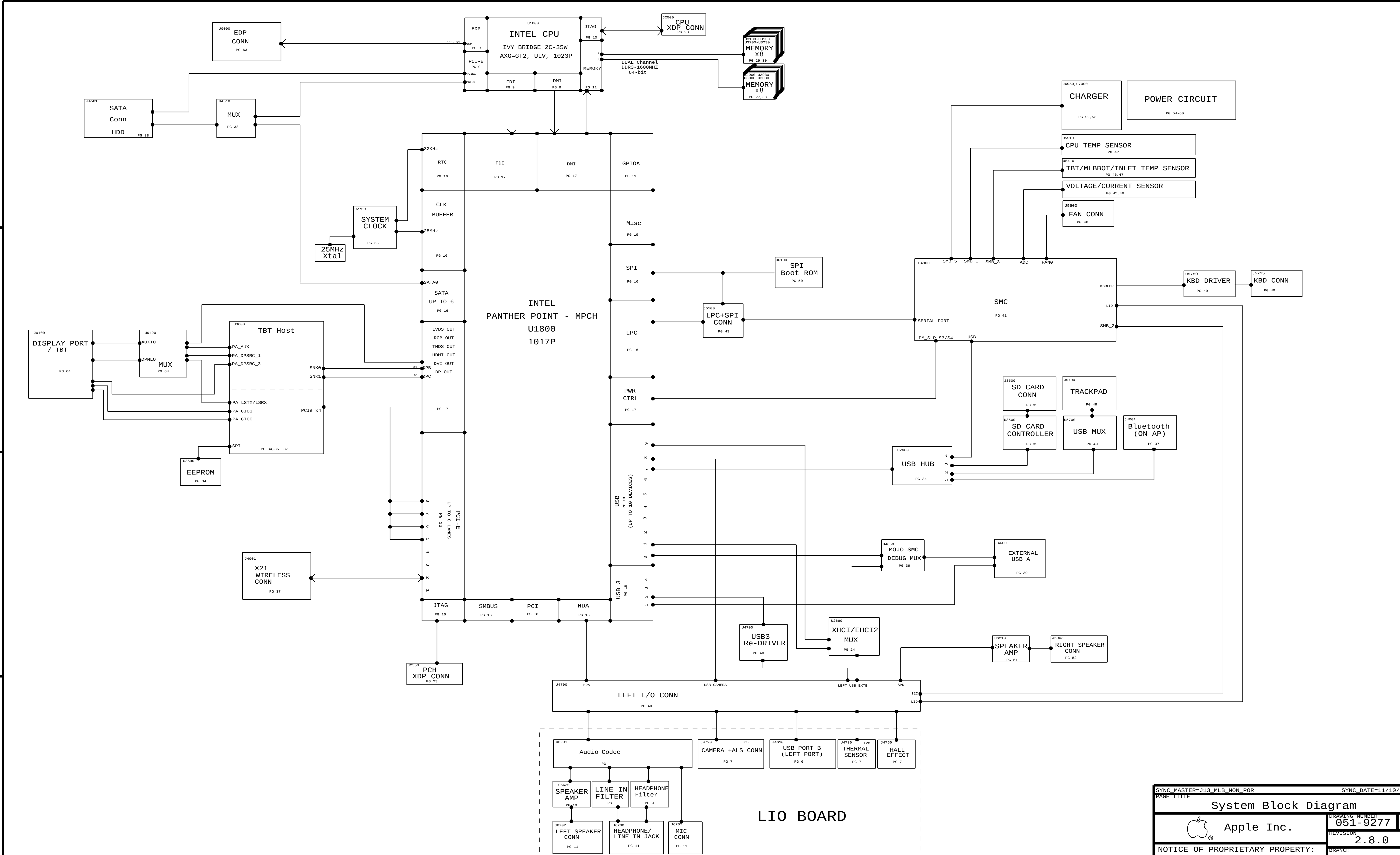

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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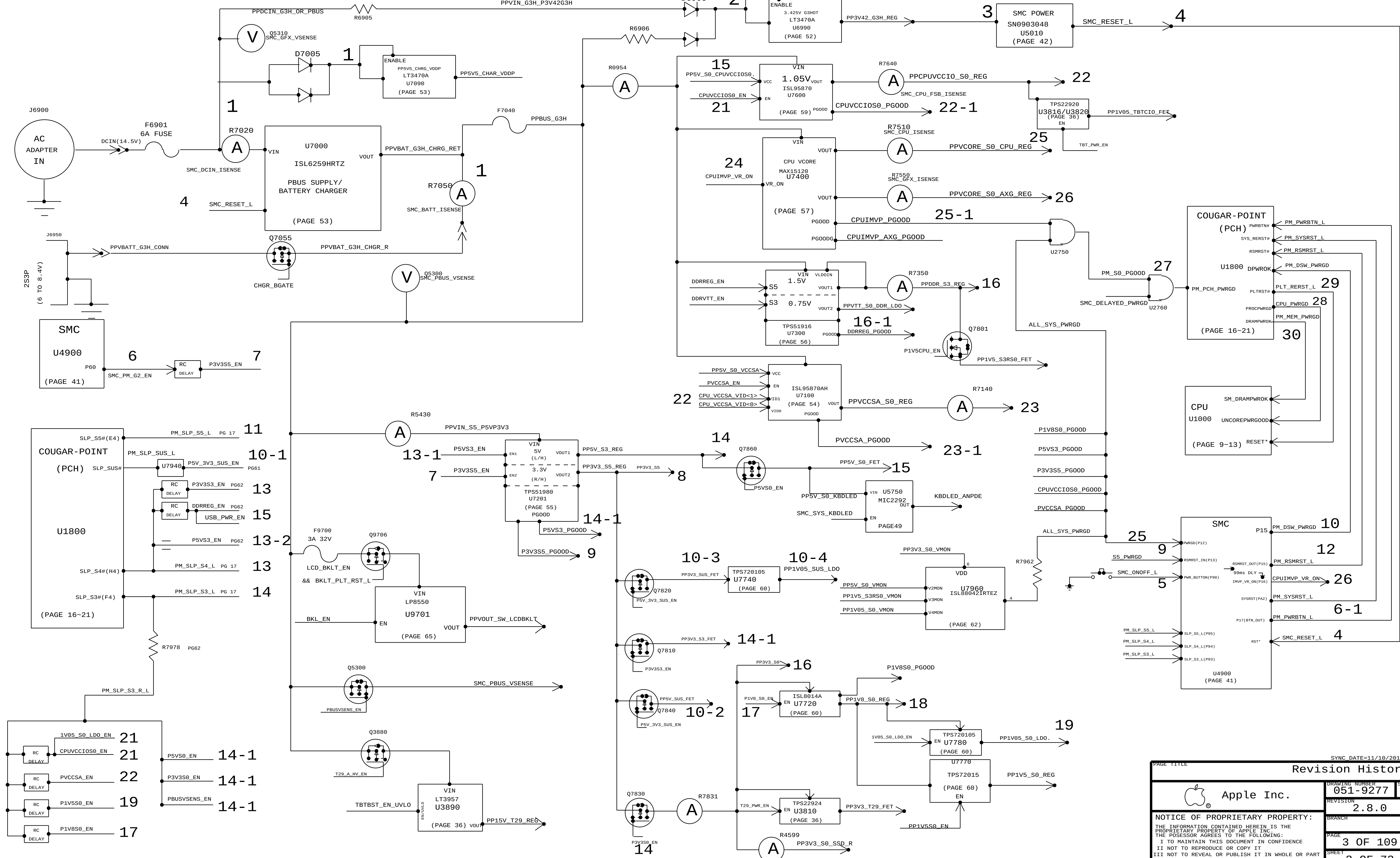
NOTICE OF PROPRIETARY PROPERTY:

J13 POWER SYSTEM ARCHITECTURE



SYNC_DATE=11/10/2011

PAGE TITLE
Revision History

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-3939	J13 MLB DEVELOPMENT BOM	J13_DEVEL:ENG
607-9090	CMN PTS,PCBA,MLB,J13	J13_COMMON
639-3552	PCBA,MLB,1.7GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:DYRQ,CPU:1.7GHZ,DDR3:SAMSUNG_4GB
639-3553	PCBA,MLB,1.5GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:DYRM,CPU:1.5GHZ,DDR3:SAMSUNG_4GB
639-3554	PCBA,MLB,1.5GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:DYRN,CPU:1.5GHZ,DDR3:HYNIX_4GB
639-3555	PCBA,MLB,1.5GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:DYRL,CPU:1.5GHZ,DDR3:HYNIX_8GB
639-3556	PCBA,MLB,1.7GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:DYRK,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-3557	PCBA,MLB,1.7GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:DYRP,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-3645	PCBA,MLB,1.5GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F0TC,CPU:1.5GHZ,DDR3:ELPIDA_8GB
639-3644	PCBA,MLB,1.7GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F0TD,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-3760	PCBA,MLB,1.8GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:F25Q,CPU:1.8GHZ,DDR3:SAMSUNG_4GB
639-3761	PCBA,MLB,1.8GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:F25T,CPU:1.8GHZ,DDR3:HYNIX_8GB
639-3762	PCBA,MLB,1.8GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:F25Y,CPU:1.8GHZ,DDR3:HYNIX_4GB
639-3763	PCBA,MLB,1.8GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F25P,CPU:1.8GHZ,DDR3:ELPIDA_8GB
639-3764	PCBA,MLB,2.0GHZ,SA 4GB,J13	J13_CMNPTS,EEEE:F25N,CPU:2.0GHZ,DDR3:SAMSUNG_4GB
639-3765	PCBA,MLB,2.0GHZ,HY 8GB,J13	J13_CMNPTS,EEEE:F25W,CPU:2.0GHZ,DDR3:HYNIX_8GB
639-3766	PCBA,MLB,2.0GHZ,HY 4GB,J13	J13_CMNPTS,EEEE:F25R,CPU:2.0GHZ,DDR3:HYNIX_4GB
639-3767	PCBA,MLB,2.0GHZ,EL 8GB,J13	J13_CMNPTS,EEEE:F25V,CPU:2.0GHZ,DDR3:ELPIDA_8GB
639-3790	PCBA,MLB,1.7GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27V,CPU:1.7GHZ,DDR3:SAMSUNG_8GB
639-3791	PCBA,MLB,1.8GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27Q,CPU:1.8GHZ,DDR3:SAMSUNG_8GB
639-3792	PCBA,MLB,2.0GHZ,SA 8GB,J13	J13_CMNPTS,EEEE:F27R,CPU:2.0GHZ,DDR3:SAMSUNG_8GB
639-3793	PCBA,MLB,1.7GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27W,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-3794	PCBA,MLB,1.8GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27Y,CPU:1.8GHZ,DDR3:ELPIDA_4GB
639-3795	PCBA,MLB,2.0GHZ,EL 4GB,J13	J13_CMNPTS,EEEE:F27T,CPU:2.0GHZ,DDR3:ELPIDA_4GB

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRK]	CRITICAL	EEEE:DYRK
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRL]	CRITICAL	EEEE:DYRL
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRM]	CRITICAL	EEEE:DYRM
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRN]	CRITICAL	EEEE:DYRN
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRP]	CRITICAL	EEEE:DYRP
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DYRQ]	CRITICAL	EEEE:DYRQ
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F0TC]	CRITICAL	EEEE:F0TC
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F0TD]	CRITICAL	EEEE:F0TD
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25N]	CRITICAL	EEEE:F25N
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25P]	CRITICAL	EEEE:F25P
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25Q]	CRITICAL	EEEE:F25Q
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25R]	CRITICAL	EEEE:F25R
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25T]	CRITICAL	EEEE:F25T
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25V]	CRITICAL	EEEE:F25V
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25W]	CRITICAL	EEEE:F25W
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F25Y]	CRITICAL	EEEE:F25Y
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27Q]	CRITICAL	EEEE:F27Q
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27R]	CRITICAL	EEEE:F27R
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27T]	CRITICAL	EEEE:F27T
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27V]	CRITICAL	EEEE:F27V
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27W]	CRITICAL	EEEE:F27W
825-7670	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_F27Y]	CRITICAL	EEEE:F27Y

Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3939	1	J13 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-9090	1	CMN PTS,PCBA,MLB,J13	CMNPTS	CRITICAL	J13_CMNPTS

SYNC_MASTER=J30_MLB SYNC_DATE=07/27/2011

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J13 BOM GROUPS

BOM GROUP	BOM OPTIONS
J13_COMMON	ALTERNATE,COMMON,J13_MISC,J13_DEBUG:ENG,J13_PROGPARTS,USBHUB2514B,EDP:YES,PCH_C1
J13_MISC	CPUMEM_SLG:NO,HUB_3NONREM,TBT,MPM5:YES,PP5V5_DCIN:NO,TPAD_PCH:NO,SKIP_5V3V3:INAUDIBLE,BTPWR:S4,TBTHV:P15V,LVDDR3_HW:YES,AXG_ACOUSTIC:NO
J13_PROGPARTS	BOOTROM_PROG,SMC_PROG,TBTROM:PROG
J13_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCPLUS,DDRVREF_DAC,VREFDQ:M1_M3,VREFCA:LDO_DAC,S0PGOOD_ISL,S3_S0_LED,VCCIOISNS_ENG,AIRPORTISNS_ENG,HDDISNS_ENG,LCDBKLTISNS_ENG
J13_DEVEL:PVT	LPCPLUS,XDP_CONN
J13_DEBUG:ENG	DEVEL_BOM,MOJO:YES,XDP
J13_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,XDP,XDP_CPU:BPM,VREFDQ:LDO,VREFCA:LDO,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
J13_DEBUG:PROD	BKLT:PROD,MOJO:YES,XDP,XDP_CPU:BPM,VREFDQ:LDO,VREFCA:LDO,LPCPLUS,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	IC,SERIAL SPI EEPROM,256KBIT,20MHZ,MLP8	U3690	CRITICAL	TBTROM:BLANK
341S3475	1	IC,EEPROM,CR,V24.1,J11/J13	U3690	CRITICAL	TBTROM:PROG
338S1098	1	IC,SMC12-A3,40MHZ/50DMIPS MCU,9X9,157BGA	U4900	CRITICAL	SMC_BLANK
338S1065	1	IC,SMC12,40MHZ/50DMIPS MCU, 9X9,157BGA	U4900	CRITICAL	SMC_BLANK
341S3433	1	IC,SMC,V2.1A43,Proto1B,J13	U4900	CRITICAL	SMC_PROG
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Macronix	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Numonyx	U6100	CRITICAL	BOOTROM_BLANK
341S3482	1	IC,EFI ROM,PROTO1B,J13 J11	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
138S0676	138S0691		ALL	Murata alt to Samsung
371S0709	371S0652		ALL	NXP alt to NXP
138S0671	138S0673		ALL	Taiyo alt to Murata
376S0790	376S0928		ALL	TI alt to Fairchild
152S1462	152S1295		ALL	Toko alt for NEC inductor
152S1085	152S1307		ALL	Toko alt for Cyntec
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
152S1493	152S1300		ALL	Coilcraft alt to Murata
353S3238	353S1428		ALL	Intersil alt to OPA2333
372S0186	372S0185		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0903	376S0796		ALL	Fairchild alt to Siliconix
197S0431	197S0432		ALL	Epson alt to NDK
337S4198	337S4197		ALL	TDP 1.5GHZ alt to Nominal
337S4236	337S4196		ALL	TDP 1.7GHZ alt to Nominal
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0333	998-4435		ALL	Sanyo alt to Kemet
128S0357	998-4435		ALL	Sanyo alt to POS caps
998-4715	998-4435		ALL	Kemet_Rect alt to POS caps
998-4716	998-4435		ALL	Kemet_.0045 Flute alt to POS caps

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4197	1	IVB,QBP8,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZ
337S4299	1	IVB,QC55,QS,L0,1.7,17W,2+2,1.0,3M,ULVBGA	U1000	CRITICAL	CPU:1.7GHZ
337S4298	1	IVB,QC54,QS,L0,1.8,17W,2+2,1.1,3M,ULVBGA	U1000	CRITICAL	CPU:1.8GHZ
337S4296	1	IVB,QC52,QS,L0,2.0,17W,2+2,1.1,4M,ULVBGA	U1000	CRITICAL	CPU:2.0GHZ
337S4198	1	IVB,QBP8,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZTDP
337S4236	1	IVB,QBQF,ES2,K0,1.7,17W,2+2,1.0,4M,ULV,TDP	U1000	CRITICAL	CPU:1.7GHZTDP
337S4165	1	IC,PCH,PPT-MB,SFF,ES1	U1800	CRITICAL	PCH_ES1
337S4180	1	IC,PCH,PPT-MB,SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB,SFF,P-QS,C0	U1800	CRITICAL	PCH_C0
337S4275	1	IC,PCH,PPT-MB,QS77,C1,QS	U1800	CRITICAL	PCH_C1
338S1047	1	IC,TBT,CR-4C,ES1,288 FCBGA,12X12MM	U3600	CRITICAL	TBT

333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FPGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC,SDRAM,2GBIT,256MX8,DDR3-1600,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0625	4	IC,SDRAM,4GBIT,512MXB,DDR3-1600,82 FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MXB,DDR3-1600,82 FPGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MXB,DDR3-1600,82 FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC,SDRAM,4GBIT,512MXB,DDR3-1600,82 FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FBGA,D-DIE	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FBGA,D-DIE	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FGBA,D-DIE	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC,SDRAM,2GBIT,DDR3-1600,78P FBGA,D-DIE	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FBGA,C-DIE	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FBGA,C-DIE	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FGBA,C-DIE	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC,SDRAM,4GBIT,DDR3-1600,78P FBGA,C-DIE	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B.78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC,SDRAM,4GBIT,DDR3L-1600,REV B,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D.78P FBGA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FGBA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC,SDRAM,2GBIT,DDR3L-1600,REV D,78P FBGA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB

353S2929	1	IC,ISL6259,BATCHARGER,3%,4X4MM,QFN28	U7000	CRITICAL	
946-3115	1	MLB,DYMAX UV EB 0.22GRAM,K21	GLUE	CRITICAL	

PD Module Parts

806-3142	1	CAN,T29,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,T29,J11/J13	TBTCOVER	CRITICAL	
806-3214	1	CAN,TOPSIDE,J11/J13	TBTTOPSIDE_1P	CRITICAL	
806-3706	1	CAN,TOPSIDE_2Piece_Cover,J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAN,TOPSIDE_2Piece_Fence,J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
806-2377	1	K78, mDP Spring	MDPSPRING	CRITICAL	NOSTUFF

SYNC_MASTER=J30_MLB SYNC_DATE=07/27/2011
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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST (Need 5 TPs)

- PP3V3_WLAN_F
- WIFI_EVENT_L
- PCIE_AP_R2D_N
- PCIE_AP_R2D_P
- PCIE_CLK100M_AP_N
- PCIE_CLK100M_AP_P
- USB_BT_CONN_P
- USB_BT_CONN_N
- PCIE_AP_D2R_P
- PCIE_AP_D2R_N
- PCIE_WAKE_L
- AP_RESET_CONN_L
- AP_CLKREQ_Q_L
- PP3V3_S3RS4_BT_F

(Need to add 8 GND TPs)

J5715: KB BKLT CONNECTOR

FUNC_TEST

- KBDLED_FB
- KBDLED_ANODE

(Need to add 2 GND TP)

J4700: LIO Connector

FUNC_TEST

- =PP3V42_G3H_ONEWIRE
- =PP3V3_S0_AUDIO (Need 2 TPs)
- =PP3V3R1V5_S0_AUDIO
- SYS_ONEWIRE
- SMC_BC_ACOK
- =USB_PWR_EN
- SMC_LID
- =I2C_LIO_SDA
- =I2C_LIO_SCL
- =I2C_MIKEY_SCL
- =I2C_MIKEY_SDA
- AUD_IPHS_SWITCH_EN
- AUD_IP_PERIPHERAL_DET
- AUD_I2C_INT_L
- AUD_GPIO_3
- SPKRAMP_INR_N
- SPKRAMP_INR_P
- USB_EXTB_N
- USB_EXTB_P
- USB3_EXTB_TX_C_N
- USB3_EXTB_TX_C_P
- USB3_EXTB_RX_RC_N
- USB3_EXTB_RX_RC_P
- USB_CAMERA_N
- USB_CAMERA_P
- HDA_SDOUT
- HDA_BIT_CLK
- HDA_SDIN0
- USB_EXTB_OC_L
- HDA_RST_L
- HDA_SYNC

(Need to add 5 GND TPs)

J4800: SD Card Connector

FUNC_TEST

- PP3V3_SW_SD_PWR
- SD_CLK
- SD_CMD
- SD_D<7..0>
- SD_CD_L
- SD_WP

(Need to add 2 GND TPs)

J5100: LPC+SPI Connector

FUNC_TEST

- =PP3V3_S5_LPCPLUS
- =PP5V_S0_LPCPLUS
- LPC_AD<3..0>
- SPI_ALT_MOSI
- SPI_ALT_MISO
- LPC_FRAME_L
- PM_CLKRUN_L
- SMC_TMS
- LPCPLUS_RESET_L
- SMC_TDO
- TP_SMC_TRST_L
- TP_SMC_MD1
- SMC_TX_L
- LPC_CLK33M_LPCPLUS
- SPIROM_USE_MLB
- SPI_ALT_CLK
- SPI_ALT_CS_L
- LPC_SERIRQ
- LPC_PWRDWN_L
- SMC_TDI
- SMC_TCK
- SMC_RESET_L
- SMC_ROMBOOT
- SMC_RX_L
- LPCPLUS_GPIO

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST

- =PP5V_S0_FAN
- FAN_RT_TACH
- FAN_RT_PWM

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST

- PP3V3_TPAD_CONN
- PP5V_TPAD_FILT
- =PP3V42_G3H_TPAD
- USB_TPAD_CONN_P
- USB_TPAD_CONN_N
- =I2C_TPAD_SDA
- =I2C_TPAD_SCL
- SMC_ONOFF_L
- SMC_LID
- SMC_TPAD_RST_L
- SMC_PME_S4_WAKE_L

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST

- SPKRAMP_ROUT_P
- SPKRAMP_ROUT_N

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST (Need 4 TPs)

- PPVBAT_G3H_CONN
- =SMBUS_BATT_SCL
- =SMBUS_BATT_SDA
- SYS_DETECT_L

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST

- PPVOUT_SW_LCDBKLT (Need 2 TPs)
- PP3V3_SW_LCD (Need 2 TPs)
- I2C_TCON_SDA_R
- I2C_TCON_SCL_R
- LED_RETURN_6
- LED_RETURN_5
- LED_RETURN_4
- LED_RETURN_3
- LED_RETURN_2
- LED_RETURN_1
- DP_INT_HPD_CONN
- DP_INT_AUX_CH_C_N
- DP_INT_AUX_CH_C_P
- DP_INT_ML_F_P<0>
- DP_INT_ML_F_N<0>
- DP_INT_ML_F_P<1>
- DP_INT_ML_F_N<1>

(Need to add 5 GND TPs)

Misc Voltages & Control Signals

FUNC_TEST

- PPBUS_G3H
- PPVIN_SW_TBTBST
- PPBUS_S5_HS_COMPUTING_ISNS
- PPDCIN_G3H
- PP3V42_G3H
- PPVRTC_G3H
- PP5V_S5
- PP5V_SUS
- PP3V3_S5
- PP3V3_SUS
- PP3V3_S3
- PP1V8_S0
- PP3V3_S0
- PP1V5_S3
- PP1V5_S3RS0
- PP1V5_S0
- PP1V05_S0
- PPVTTDDR_S3
- PP0V75_S0_DDRVTT
- PPVCCSA_S0_CPU
- PP1V05_SUS
- PP15V_TBT
- PP3V3_TBTLC
- PP1V05_TBTLC
- PP1V05_S0_PCH_VCCADPLL
- PPVCORE_S0_CPU
- PPVCORE_S0_AXG
- PP1V5_S3_CPU_VCCDQ
- PP1V05_S0_CPU_VCCPQE
- PP1V8_S0_CPU_VCCPLL_R
- PP1V05_TBTCIO
- PPBUS_S5_HS_OTHER_ISNS
- PPDCIN_G3H_ISOL
- PP5V_S3
- PP5V_S0
- PP3V3_S4

(Need to add 27 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST

- PP3V3_S0_SSD_FLT (Need 5 TPs)
- SATA_SSD_D2R_P
- SATA_SSD_D2R_N
- SMC_OOB1_R_L
- SMC_OOB1_TX_L
- PCIE_CLK100M_SSD_P
- PCIE_CLK100M_SSD_N
- PCIE_SSD_R2D_P<1>
- PCIE_SSD_R2D_N<1>
- PCIE_SSD_D2R_P<1>
- PCIE_SSD_D2R_N<1>
- SATA_SSD_R2D_N
- SATA_SSD_R2D_P
- SSD_CLKREQ_L
- SATA_PCIE_SEL
- SSD_P3V3S0_EN
- SSD_RESET_L

(Need to add 6 GND TPs)

J6900: DC-In Connector

FUNC_TEST (Need 6 TPs)

- =PP18V5_DCIN_CONN
- =PP5V_S3_LIO_CONN

(Need to add 5 GND TPs)

NO_TEST Nets

POWER SIGNALS

- VCCSAS0_SREF
- VCCSAS0_SET1_R
- VCCSAS0_SET0
- VCCSAS0_SET1

NO_TEST

- TP_CRT_IG_BLUE — NC_CRT_IG_BLUE
- TP_CRT_IG_GREEN — NC_CRT_IG_GREEN
- TP_CRT_IG_RED — NC_CRT_IG_RED
- TP_CRT_IG_DDC_CLK — NC_CRT_IG_DDC_CLK
- TP_CRT_IG_DDC_DATA — NC_CRT_IG_DDC_DATA
- TP_CRT_IG_HSYNC — NC_CRT_IG_HSYNC
- TP_CRT_IG_VSYNC — NC_CRT_IG_VSYNC
- TP_LVDS_IG_CTRL_CLK — NC_LVDS_IG_CTRL_CLK
- TP_LVDS_IG_CTRL_DATA — NC_LVDS_IG_CTRL_DATA
- TP_PCH_LVDS_VBG — NC_PCH_LVDS_VBG
- TP_HDA_SDIN1 — NC_HDA_SDIN1
- TP_HDA_SDIN2 — NC_HDA_SDIN2
- TP_HDA_SDIN3 — NC_HDA_SDIN3
- TP_PCI_PME_L — NC_PCI_PME_L
- TP_PCI_CLK33M_OUT3 — NC_PCI_CLK33M_OUT3
- TP_CLINK_CLK — NC_CLINK_CLK
- TP_CLINK_DATA — NC_CLINK_DATA
- TP_CLINK_RESET_L — NC_CLINK_RESET_L
- TP_PCIE_CLK100M_PEBN — NC_PCIE_CLK100M_PEBN
- TP_PCIE_CLK100M_PEBP — NC_PCIE_CLK100M_PEBP
- XDP_PCH_AP_PWR_EN
- XDP_PCH_USB_HUB_SOFT_RST_L
- XDP_PCH_SDCONN_STATE_RST_L
- XDP_PCH_ENET_PWR_EN
- XDP_PCH_SDCONN_DET_L
- XDP_PCH_S5_PWRGD
- XDP_PCH_PWRBTN_L
- XDP_PCH_ISOLATE_CPU_MEM_L
- XDP_FW_CLKREQ_L
- XDP_AP_CLKREQ_L
- XDP_PCH_AUD_IPHS_SWITCH_EN
- TP_SDVO_TVCLKINN — NC_SDVO_TVCLKINN
- TP_SDVO_TVCLKINP — NC_SDVO_TVCLKINP
- TP_SDVO_STALLN — NC_SDVO_STALLN
- TP_SDVO_STALLP — NC_SDVO_STALLP
- TP_SDVO_INTN — NC_SDVO_INTN
- TP_SDVO_INTP — NC_SDVO_INTP
- TP_XDP_PCH_OBSFN_A<0..1> — NC_TP_XDP_PCH_OBSFN_A<0..1>
- TP_XDP_PCH_OBSFN_B<0..1> — NC_TP_XDP_PCH_OBSFN_B<0..1>
- TP_XDPPCH_HOOK2 — NC_TP_XDPPCH_HOOK2
- TP_XDPPCH_HOOK3 — NC_TP_XDPPCH_HOOK3
- TP_XDP_PCH_OBSFN_D<0..1> — NC_TP_XDP_PCH_OBSFN_D<0..1>
- TP_XDP_PCH_HOOK4 — NC_TP_XDP_PCH_HOOK4
- TP_XDP_PCH_HOOK5 — NC_TP_XDP_PCH_HOOK5
- TP_PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0
- TP_PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1
- TP_PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2
- TP_PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3

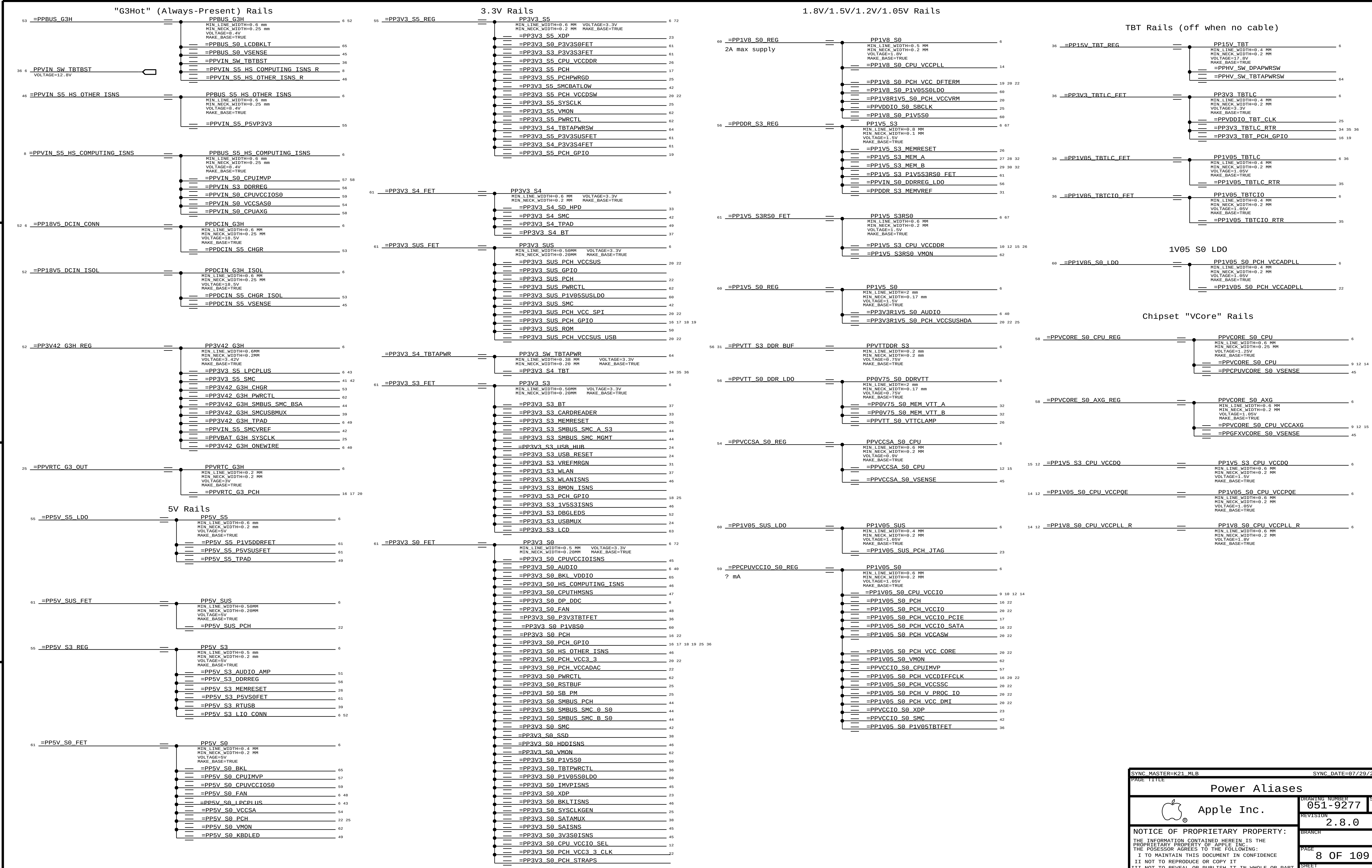
- NC_EDP_TXP<0..3> — TP_EDP_TX_P<0..3>
- NC_EDP_TXN<0..3> — TP_EDP_TX_N<0..3>
- NC_EDP_AUXP — TP_EDP_AUX_P
- NC_EDP_AUXN — TP_EDP_AUX_N
- NC_CPU_THERMDA — TP_CPU_THERMDA
- NC_CPU_THERMDC — TP_CPU_THERMDC
- NC_CPU_RSVD<30..45> — TP_CPU_RSVD<30..45>
- NC_CPU_RSVD<8..27> — TP_CPU_RSVD<8..27>
- NC_PEG_R2D_CP<15..2> — =PEG_R2D_C_P<15..2>
- NC_PEG_R2D_CN<15..2> — =PEG_R2D_C_N<15..2>
- NC_PEG_D2RP<15..2> — =PEG_D2R_P<15..2>
- NC_PEG_D2RN<15..2> — =PEG_D2R_N<15..2>

- TP_PCIE_CLK100M_PE4N — NC_PCIE_CLK100M_PE4N
- TP_PCIE_CLK100M_PE4P — NC_PCIE_CLK100M_PE4P
- TP_PCIE_CLK100M_PE5N — NC_PCIE_CLK100M_PE5N
- TP_PCIE_CLK100M_PE5P — NC_PCIE_CLK100M_PE5P
- TP_PCIE_CLK100M_PE6N — NC_PCIE_CLK100M_PE6N
- TP_PCIE_CLK100M_PE6P — NC_PCIE_CLK100M_PE6P
- TP_PCIE_CLK100M_PE7N — NC_PCIE_CLK100M_PE7N
- TP_PCIE_CLK100M_PE7P — NC_PCIE_CLK100M_PE7P
- TP_PSOC_P1_3 — NC_PSOC_P1_3
- TP_SATA_B_D2RN — NC_SATA_B_D2RN
- TP_SATA_B_D2RP — NC_SATA_B_D2RP
- TP_SATA_B_R2D_CN — NC_SATA_B_R2D_CN
- TP_SATA_B_R2D_CP — NC_SATA_B_R2D_CP
- TP_SATA_D_D2RN — NC_SATA_D_D2RN
- TP_SATA_D_D2RP — NC_SATA_D_D2RP
- TP_SATA_D_R2D_CN — NC_SATA_D_R2D_CN
- TP_SATA_D_R2D_CP — NC_SATA_D_R2D_CP
- TP_SATA_E_D2RN — NC_SATA_E_D2RN
- TP_SATA_E_D2RP — NC_SATA_E_D2RP
- TP_SATA_E_R2D_CN — NC_SATA_E_R2D_CN
- TP_SATA_E_R2D_CP — NC_SATA_E_R2D_CP
- TP_SATA_F_D2RN — NC_SATA_F_D2RN
- TP_SATA_F_D2RP — NC_SATA_F_D2RP
- TP_SATA_F_R2D_CN — NC_SATA_F_R2D_CN
- TP_SATA_F_R2D_CP — NC_SATA_F_R2D_CP

- TP_PCH_TP18 — NC_PCH_TP18
- TP_PCH_TP17 — NC_PCH_TP17
- TP_PCH_TP16 — NC_PCH_TP16
- TP_PCH_TP15 — NC_PCH_TP15
- TP_PCH_TP14 — NC_PCH_TP14
- TP_PCH_TP13 — NC_PCH_TP13
- TP_PCH_TP12 — NC_PCH_TP12
- TP_PCH_TP10 — NC_PCH_TP10
- TP_PCH_TP9 — NC_PCH_TP9
- TP_PCH_TP8 — NC_PCH_TP8
- TP_PCH_TP7 — NC_PCH_TP7
- TP_PCH_TP6 — NC_PCH_TP6
- TP_PCH_TP5 — NC_PCH_TP5
- TP_PCH_TP4 — NC_PCH_TP4
- TP_PCH_TP3 — NC_PCH_TP3
- TP_PCH_TP2 — NC_PCH_TP2
- TP_PCH_TP1 — NC_PCH_TP1

- PCH_VSS_NCTF<1>
- PCH_VSS_NCTF<2>
- PCH_VSS_NCTF<5>
- PCH_VSS_NCTF<9>
- PCH_VSS_NCTF<11>
- PCH_VSS_NCTF<12>
- PCH_VSS_NCTF<15>
- PCH_VSS_NCTF<17>
- PCH_VSS_NCTF<18>
- PCH_VSS_NCTF<19>
- PCH_VSS_NCTF<21>
- PCH_VSS_NCTF<25>
- PCH_VSS_NCTF<27>
- PCH_VSS_NCTF<29>

- TP_LVDS_IG_B_CLKN — NC_LVDS_IG_B_CLKN
- TP_LVDS_IG_B_CLKP — NC_LVDS_IG_B_CLKP
- TP_LVDS_IG_BKL_PWM — NC_LVDS_IG_BKL_PWM
- SMC_BS_ALRT_L — NC_SMC_BS_ALRT_L



SYNC_MASTER=K21_MLB SYNC_DATE=07/29/2011

PAGE TITLE

Power Aliases

Apple Inc.

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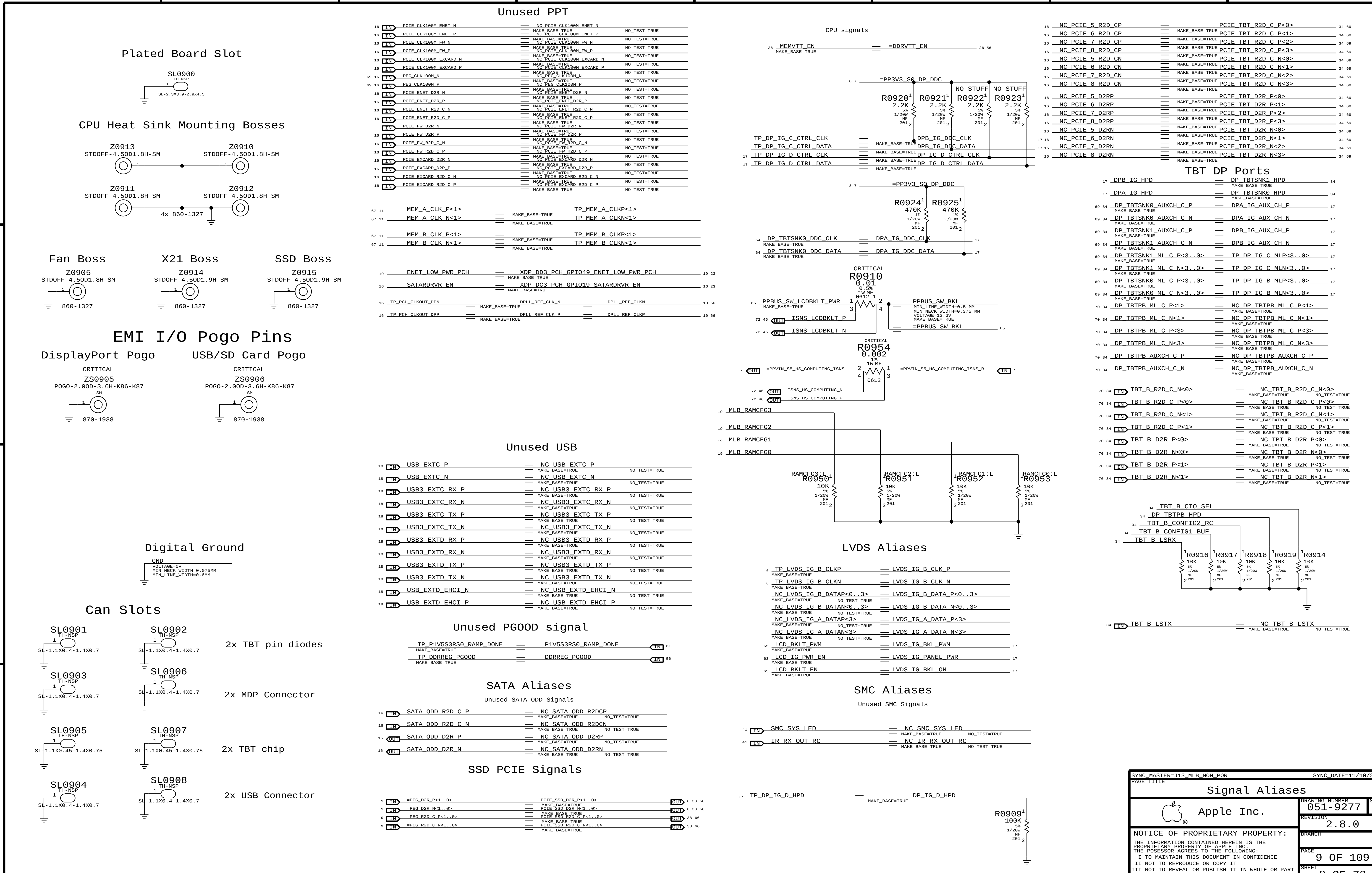

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

Signal Aliases

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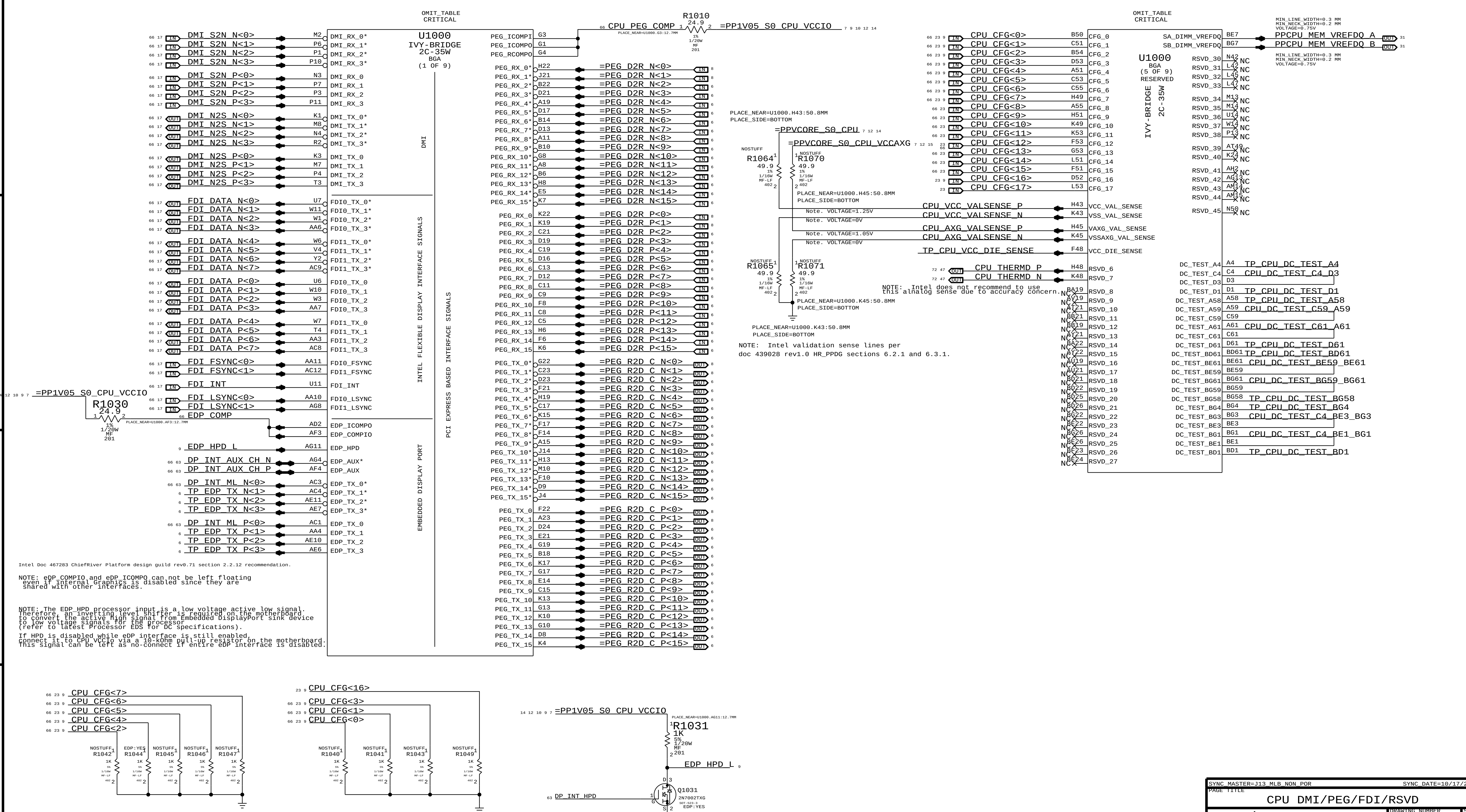
SHEET 8 OF 73

NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.



Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.

NOTE: Intel does not recommend to use this alnalog sense due to accuracy concern.

FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2011

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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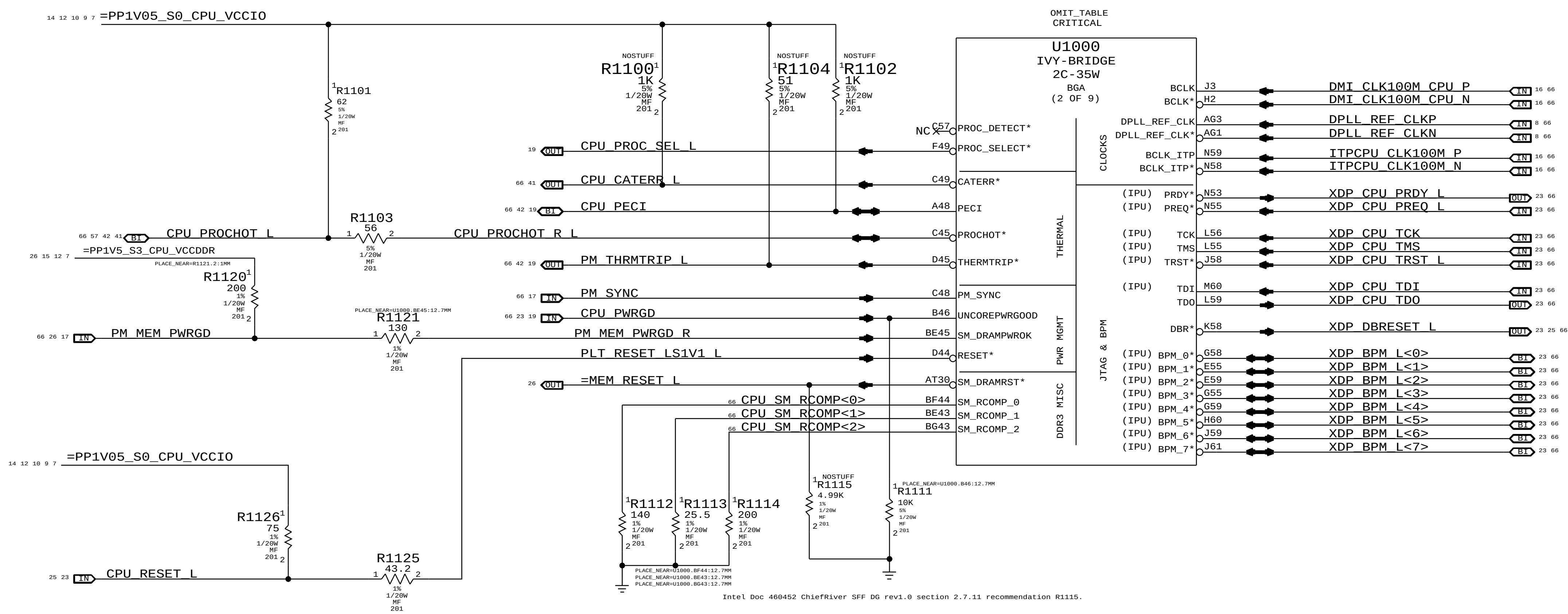

SYNC_MASTER=J30_MLB SYNC_DATE=07/27/2011

PAGE TITLE

CPU CLOCK/MISC/JTAG

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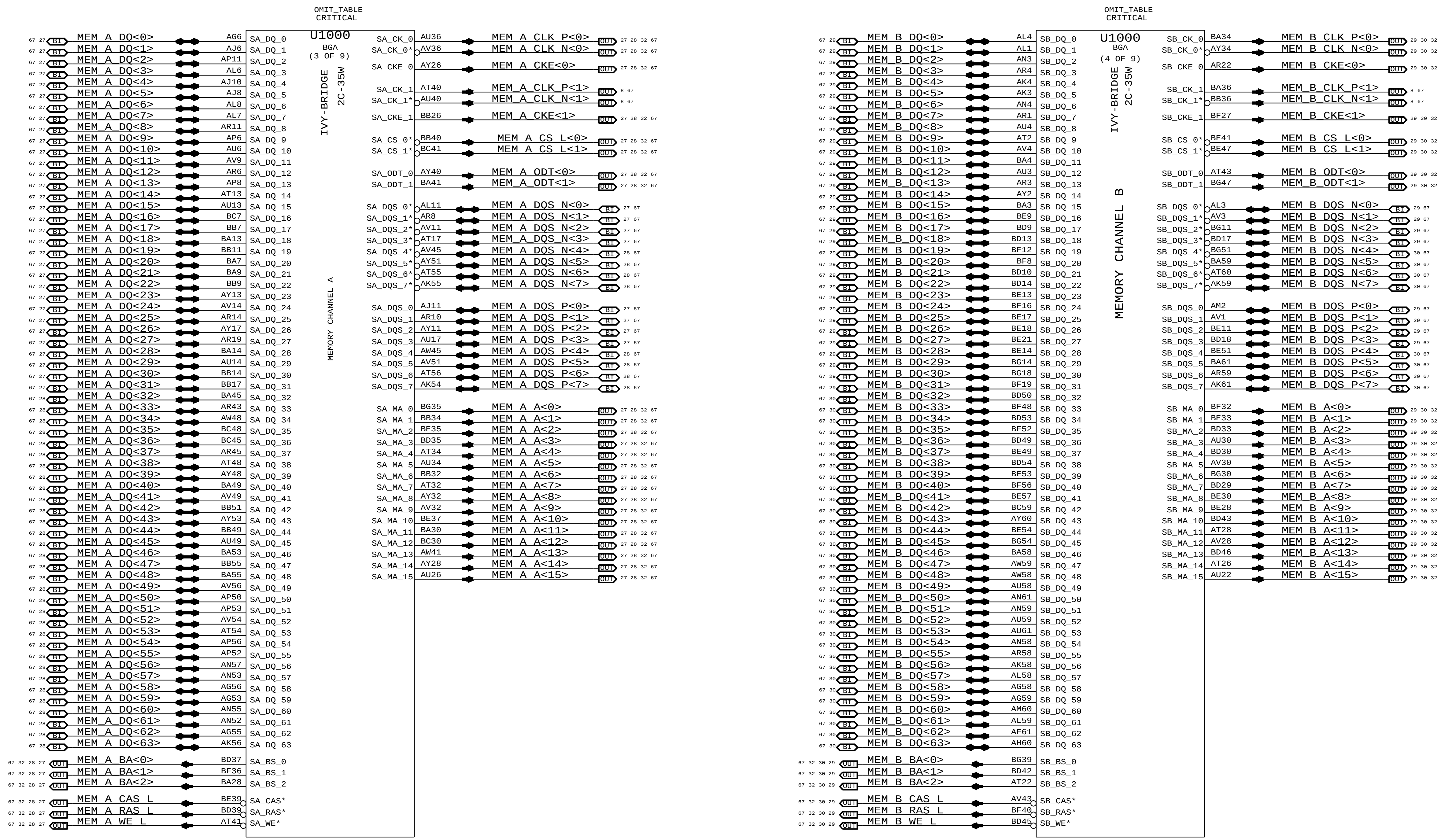
8 7 6 5 4 3 2 1



SYNC_MASTER=J30_MLB SYNC_DATE=07/27/2011

PAGE TITLE

CPU DDR3 INTERFACES

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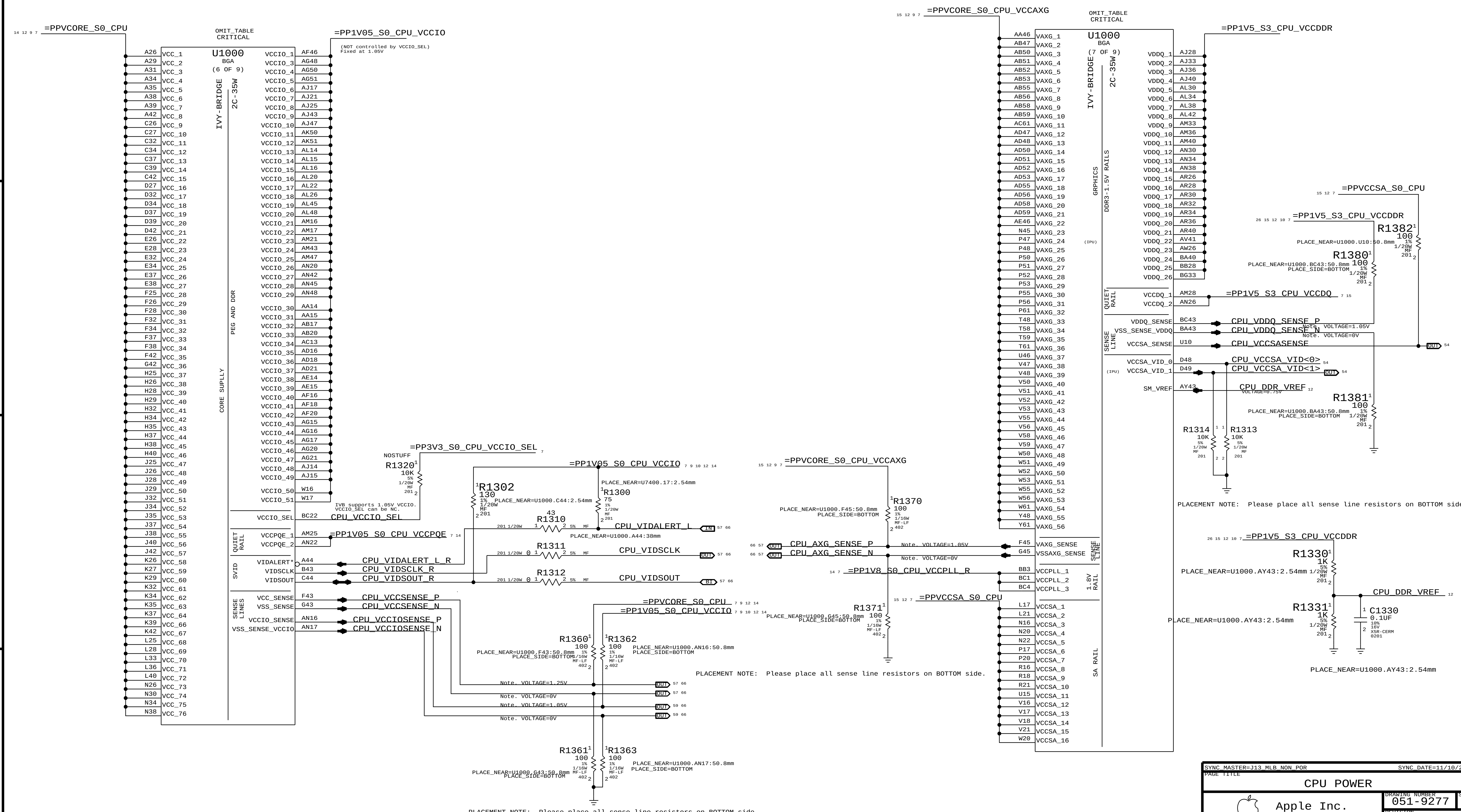
8 7 6 5 4 3 2 1



SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

CPU POWER

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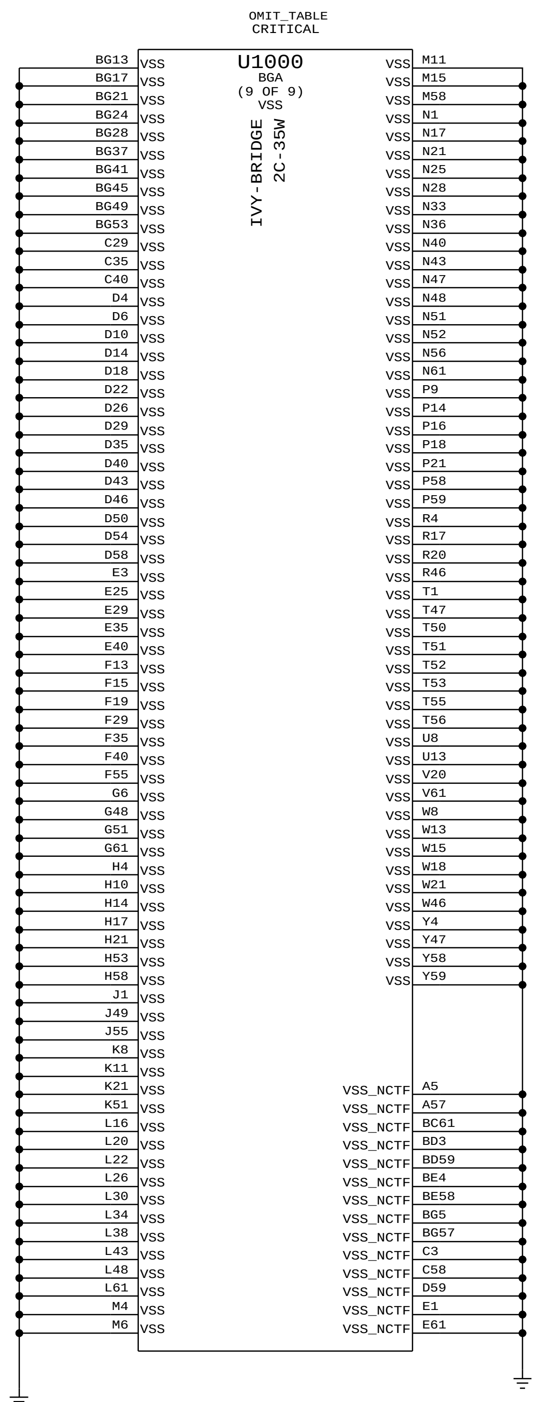

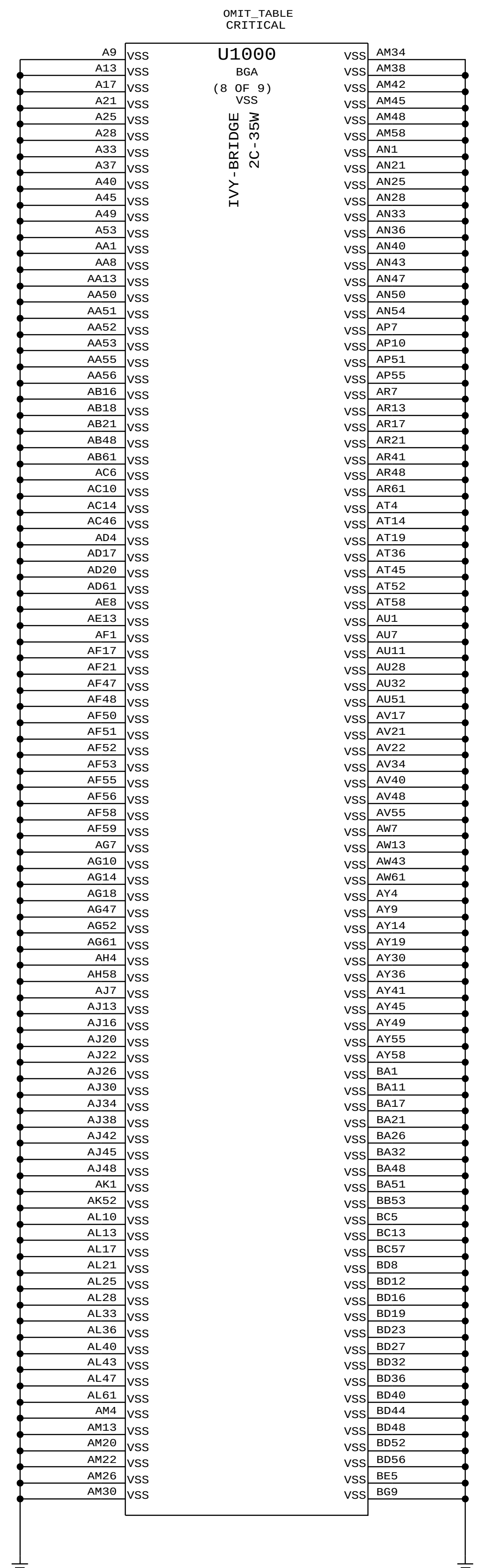

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PAGE TITLE
CPU GROUNDS

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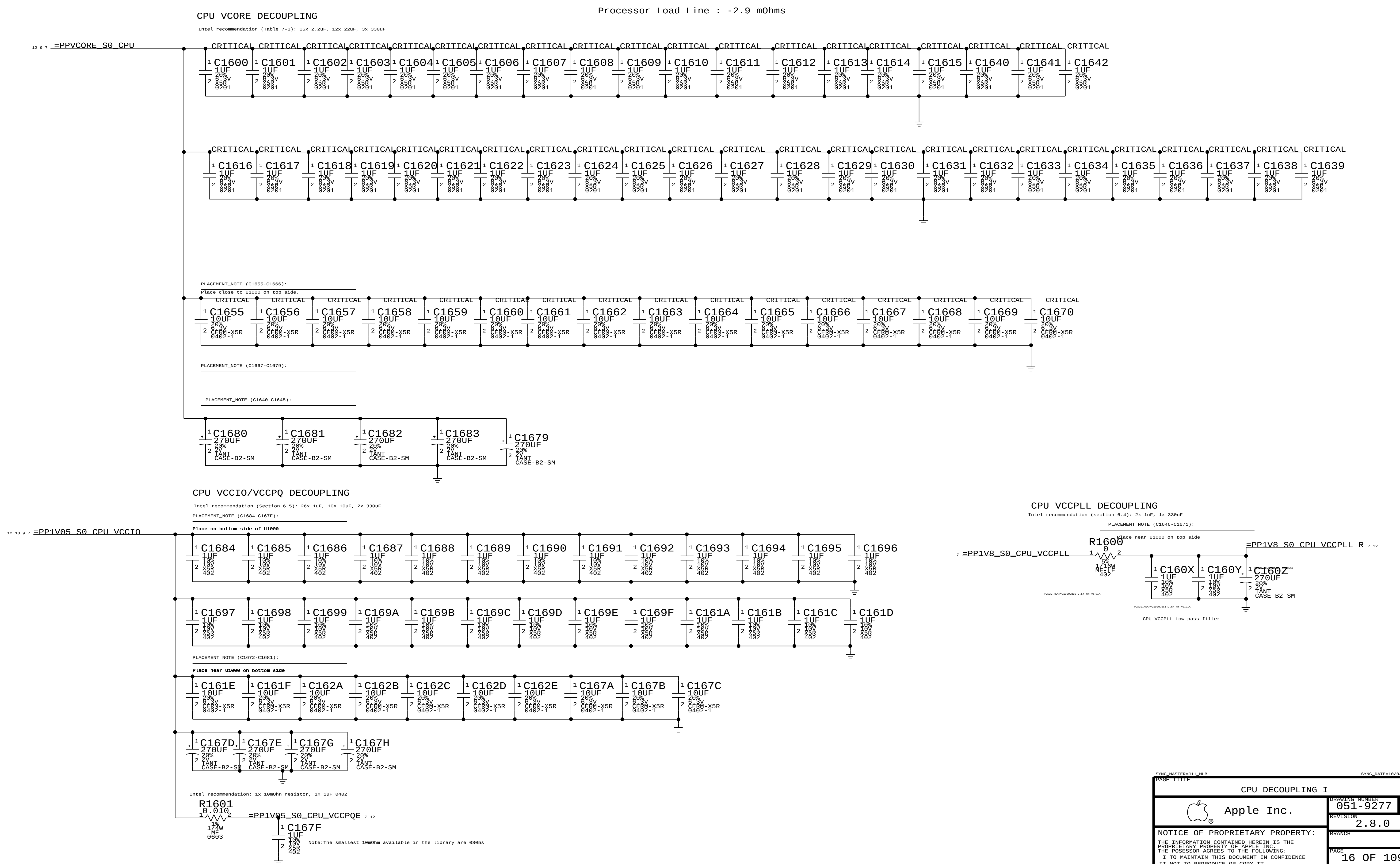
All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide



SYNC_MASTER=J11_MLB SYNC_DATE=10/03/2011

PAGE TITLE

CPU DECOUPLING-I

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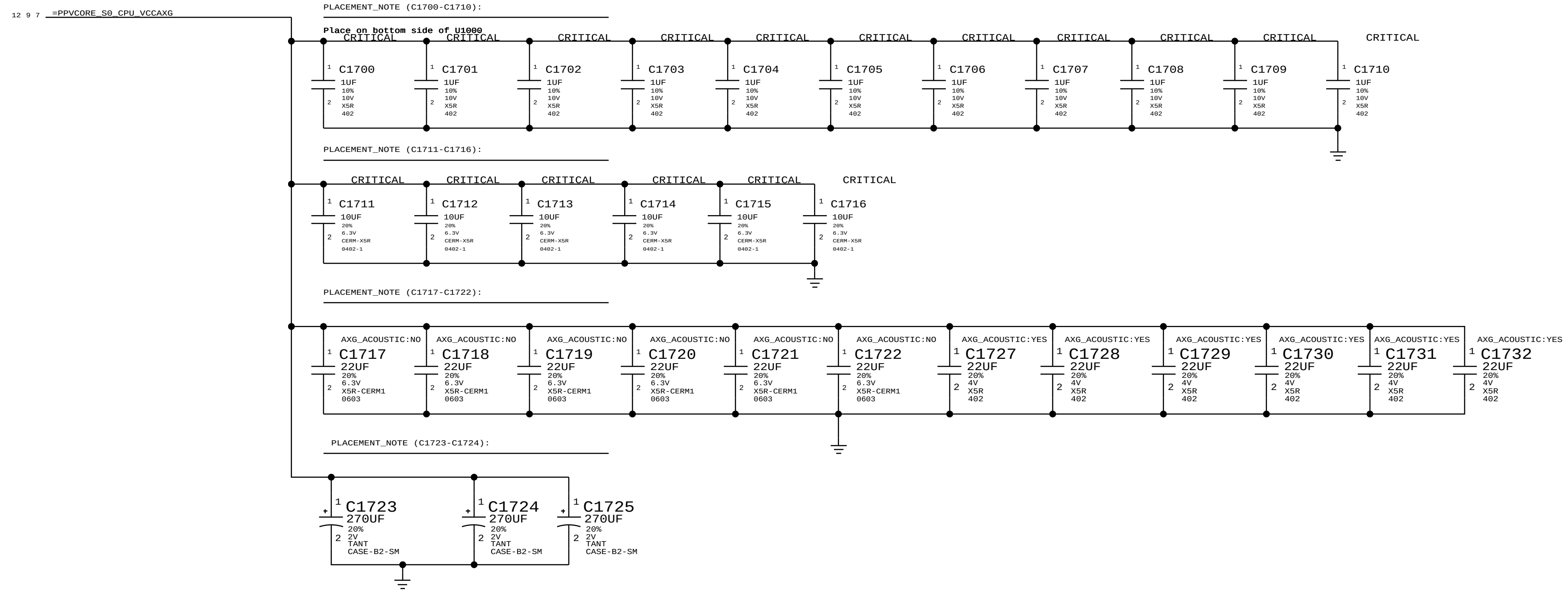
VAXG DECOUPLING

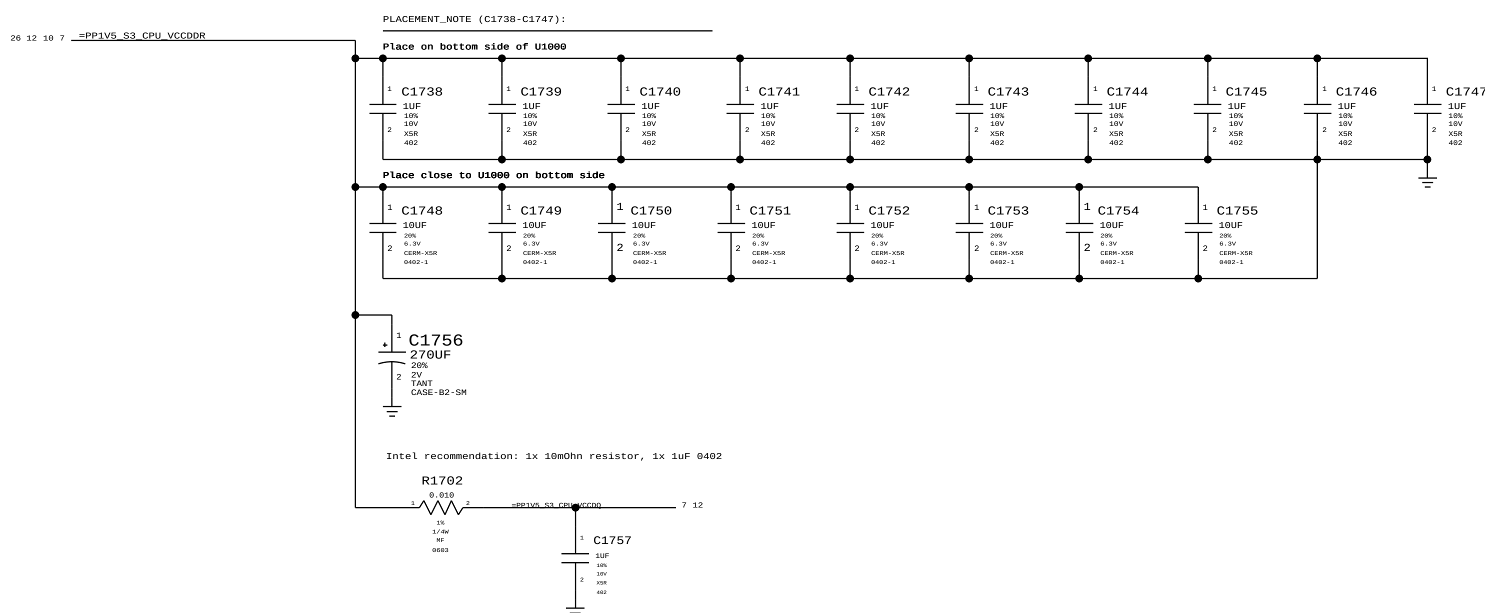
Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)



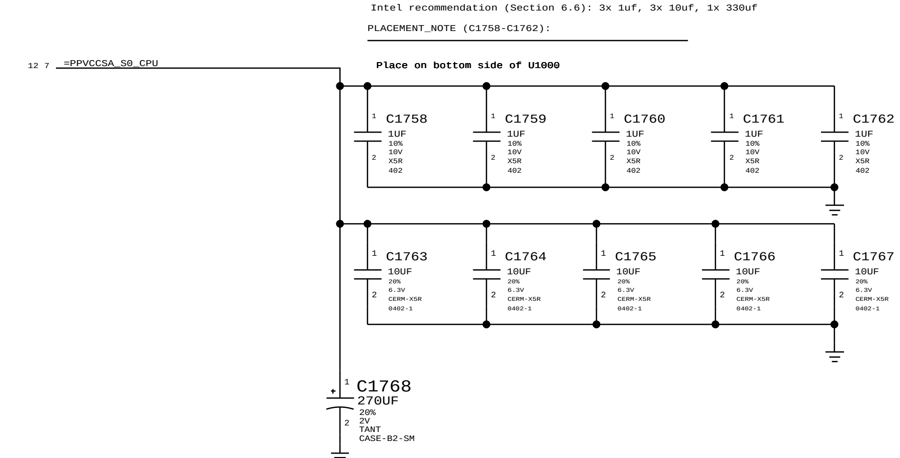
CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF



CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uf, 3x 10uf, 1x 330uf



SYNC_MASTER=K21_MLB SYNC_DATE=07/29/2011

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

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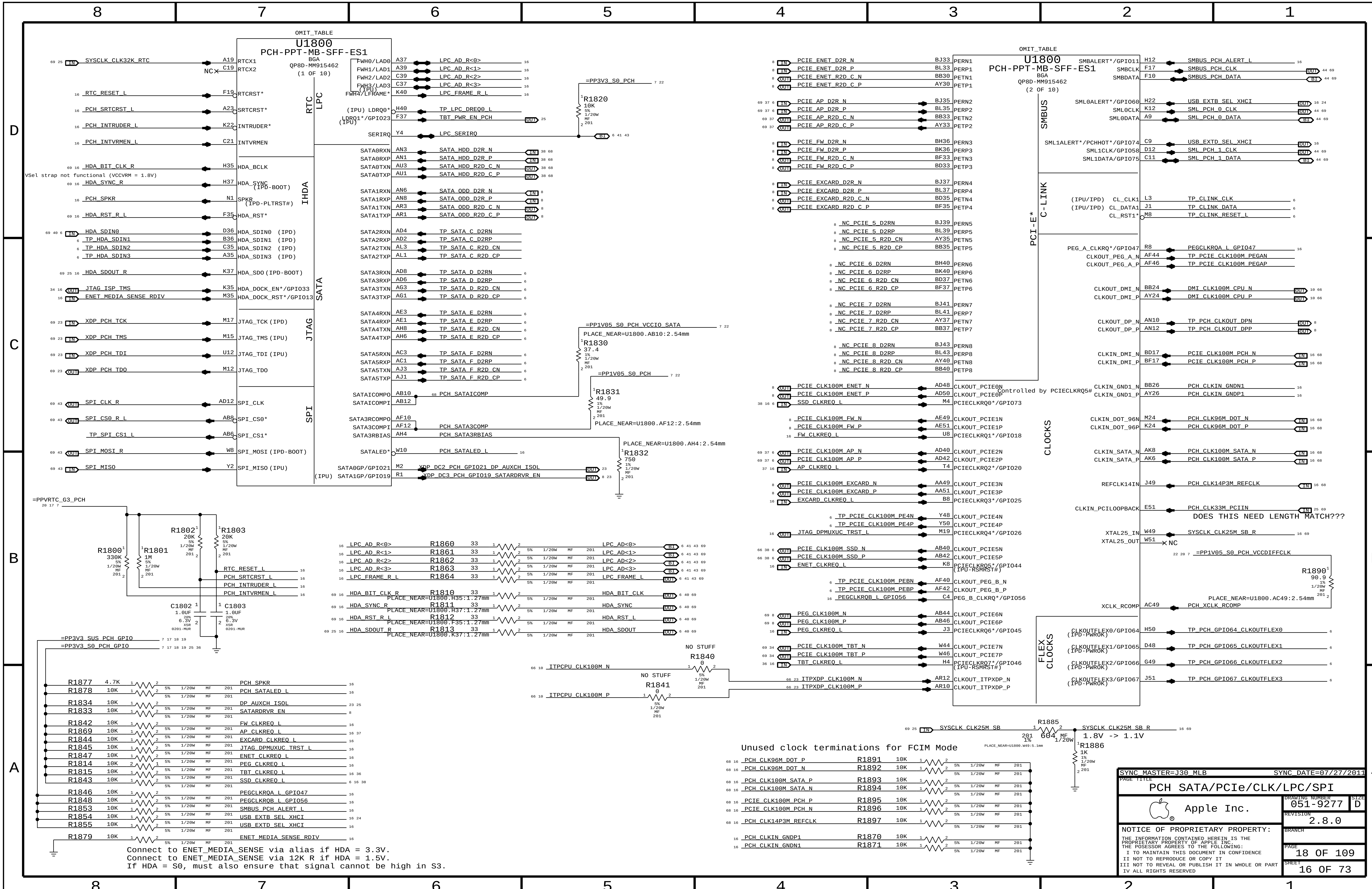

SYNC_MASTER=J30_MLB SYNC_DATE=07/27/2011

PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI

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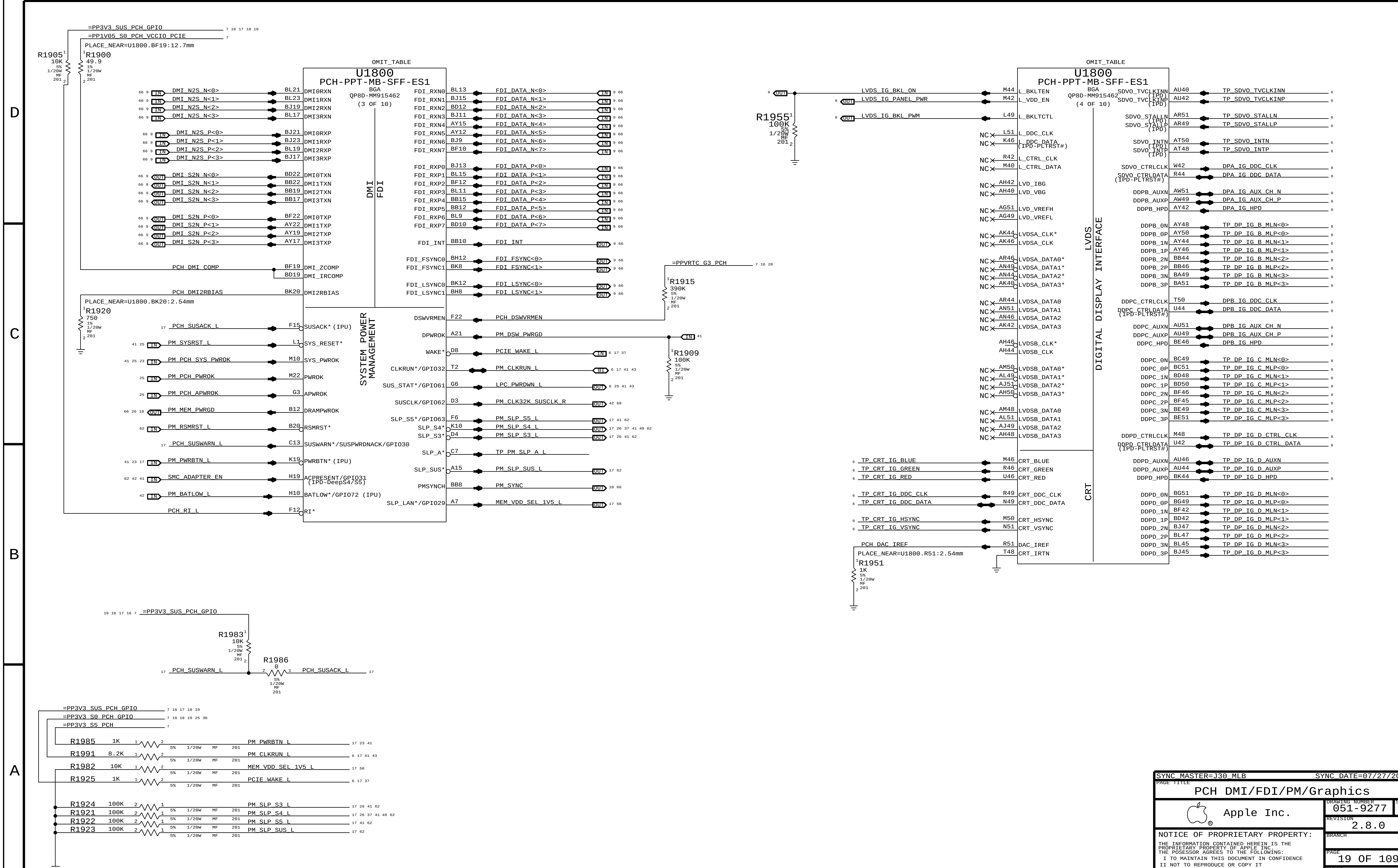

SYNC_MASTER=J30_MLB SYNC_DATE=07/27/2011

PAGE TITLE

PCH DMI/FDI/PM/Graphics

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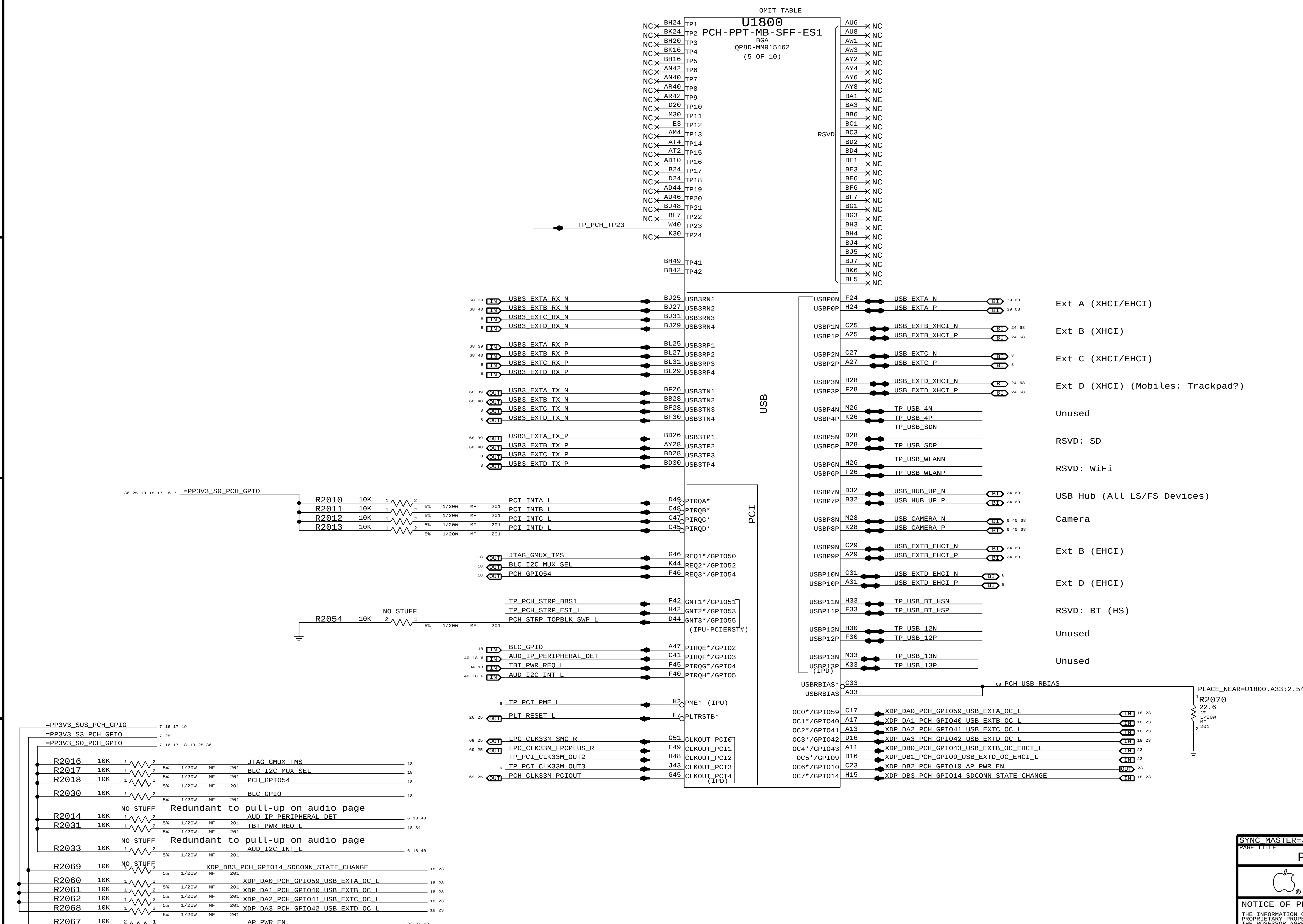

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

PCH PCI/USB/TP/RSVD

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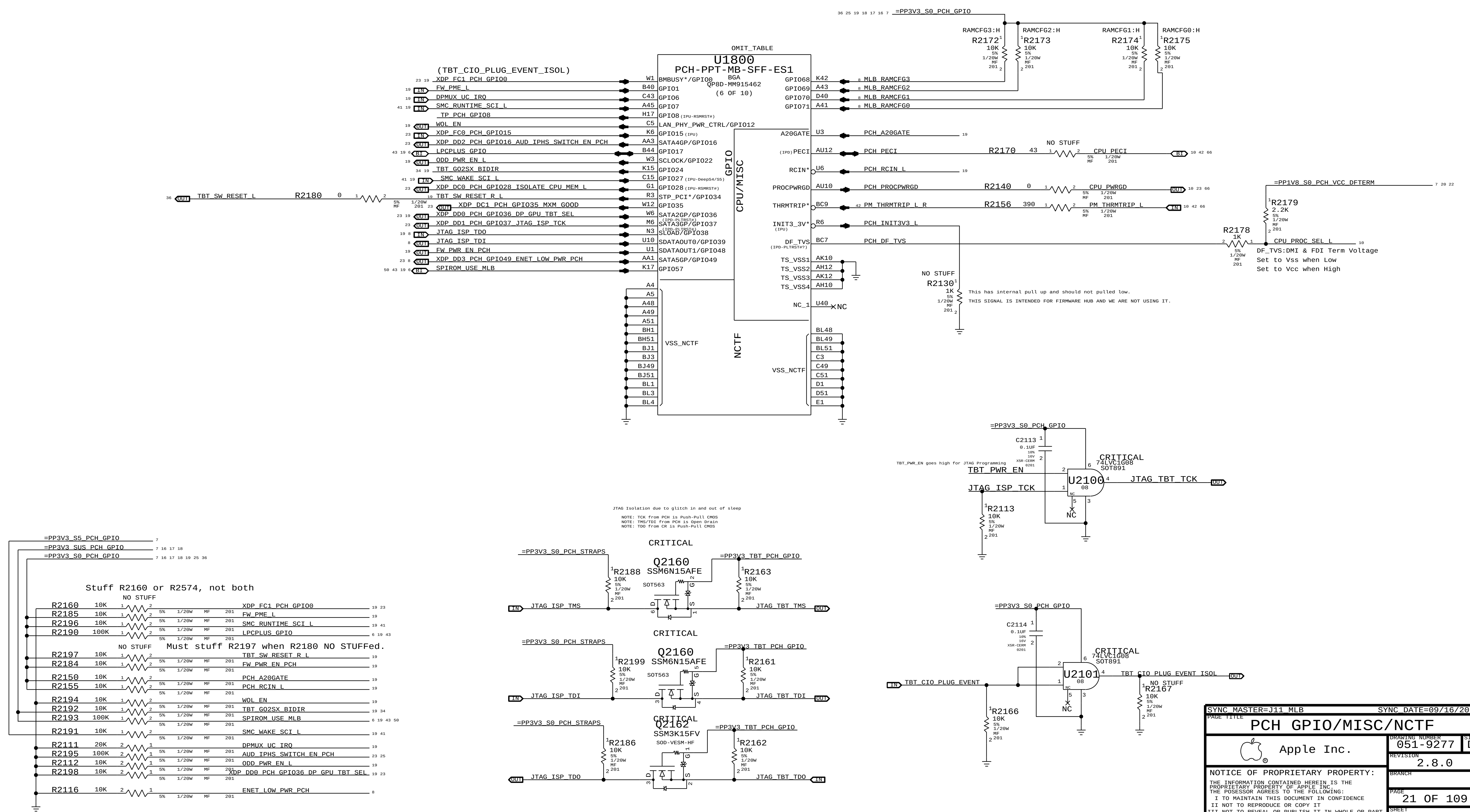
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.



SYNC_MASTER=J11_MLB SYNC_DATE=09/16/2011

PAGE TITLE
PCH GPIO/MISC/NCTF

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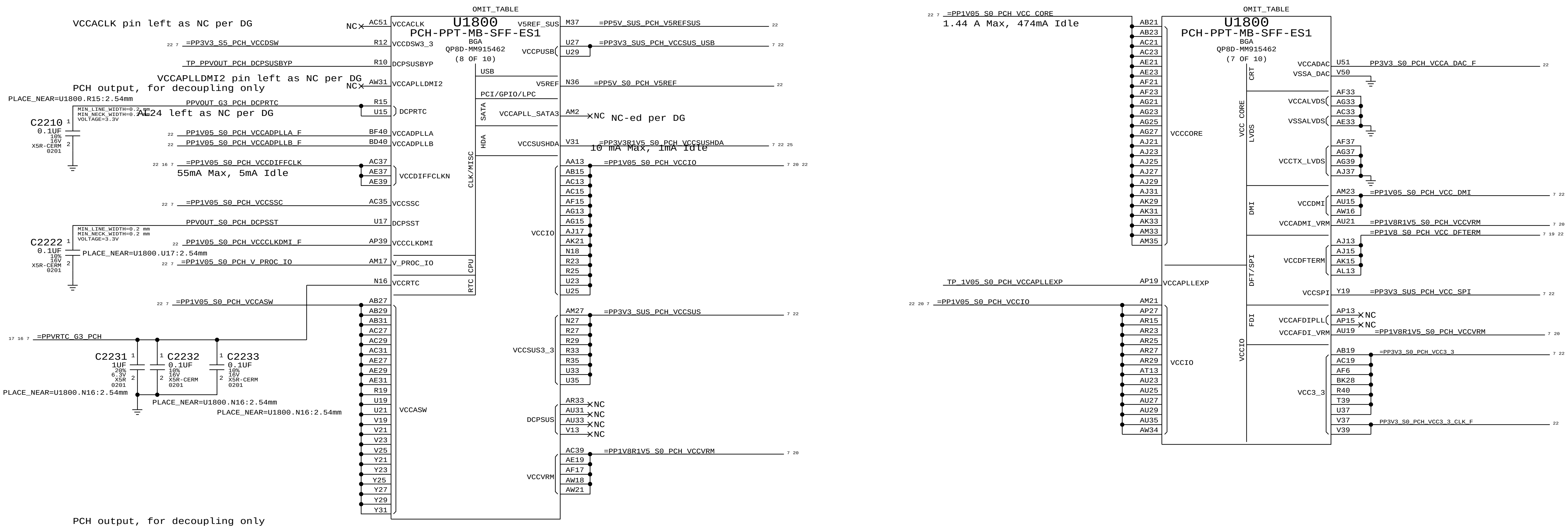

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PAGE TITLE	PCH POWER
DRAWING NUMBER	051-9277
SIZE	D
REVISION	2.8.0
BRANCH	
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SHEET	20 OF 73

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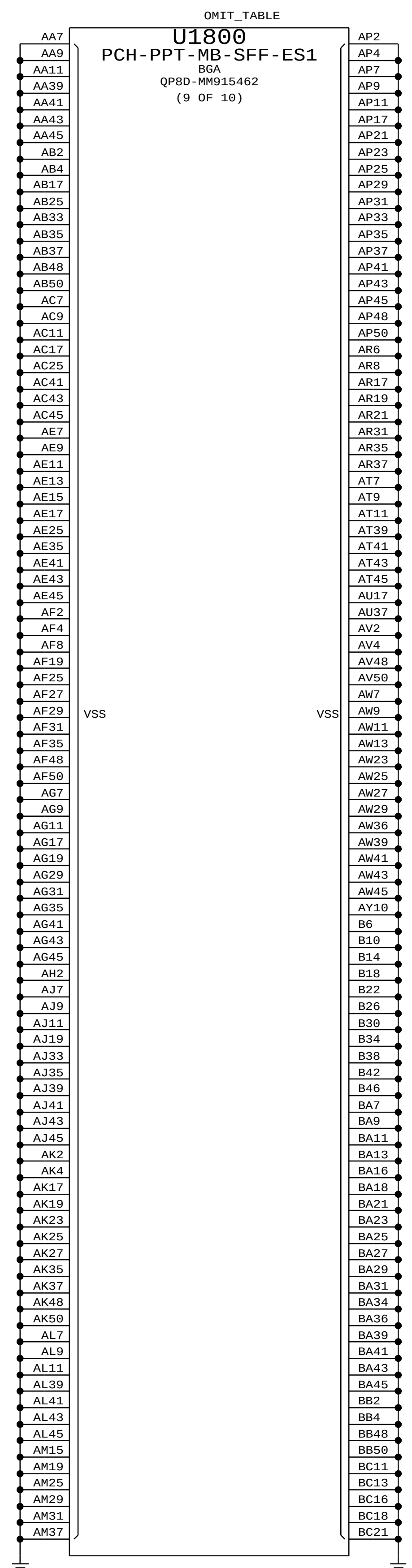

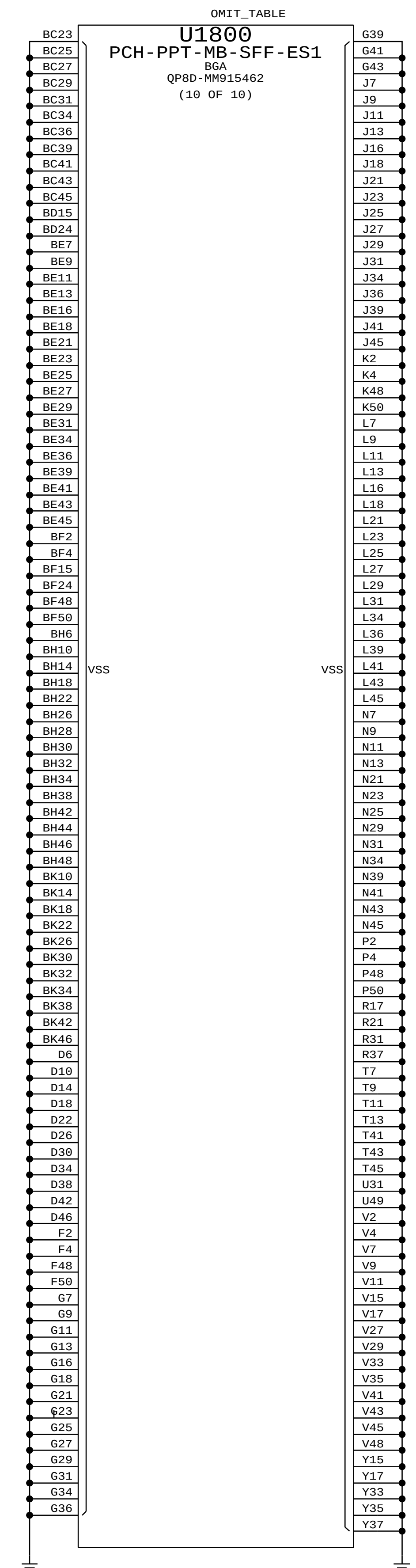

SYNC_MASTER=J30_MLB SYNC_DATE=07/27/2011

PAGE TITLE

PCH GROUNDS

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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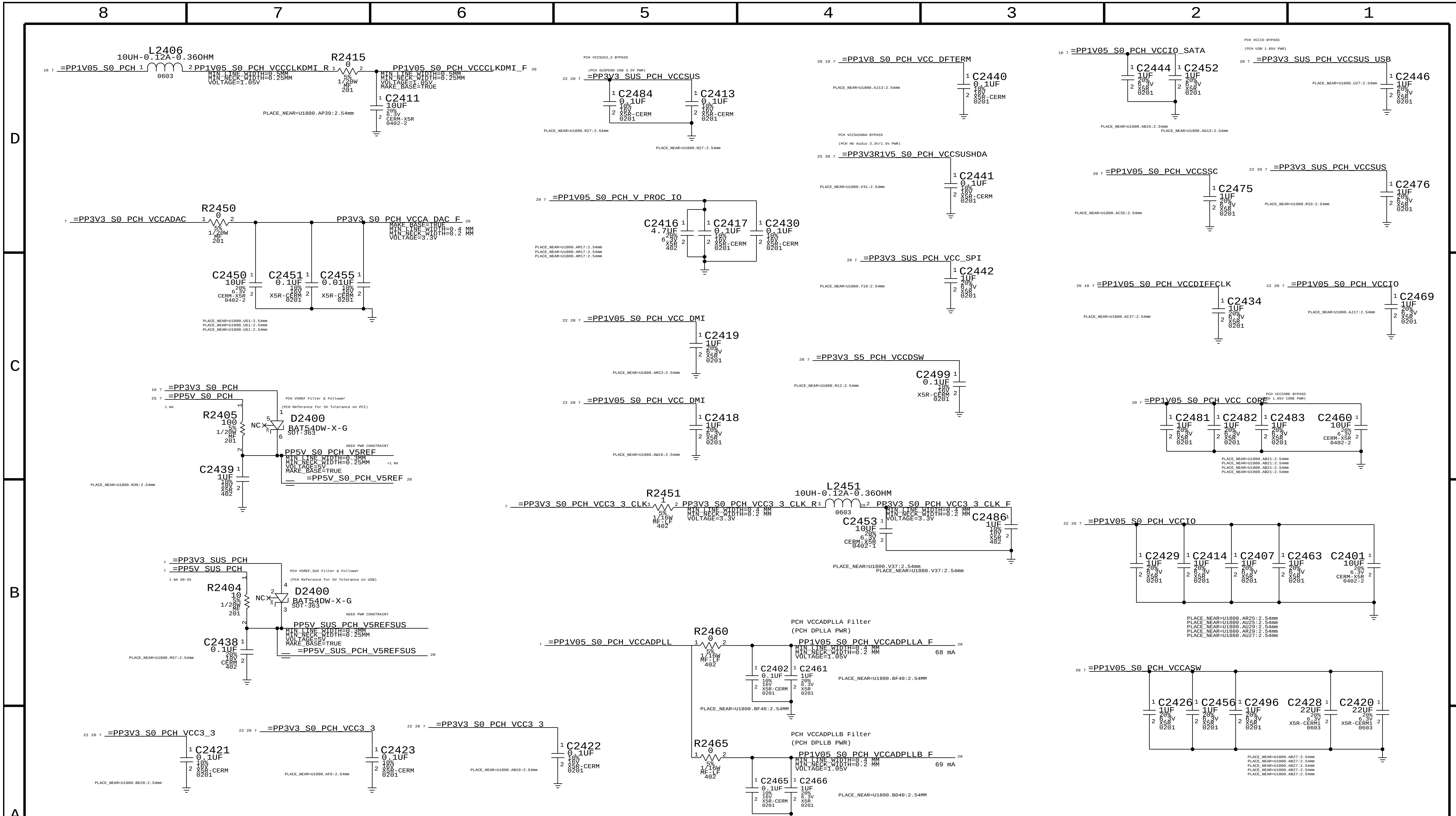
PAGE 23 OF 109

SHEET 21 OF 73



SYNC_MASTER=J11_MLB SYNC_DATE=10/03/2011

PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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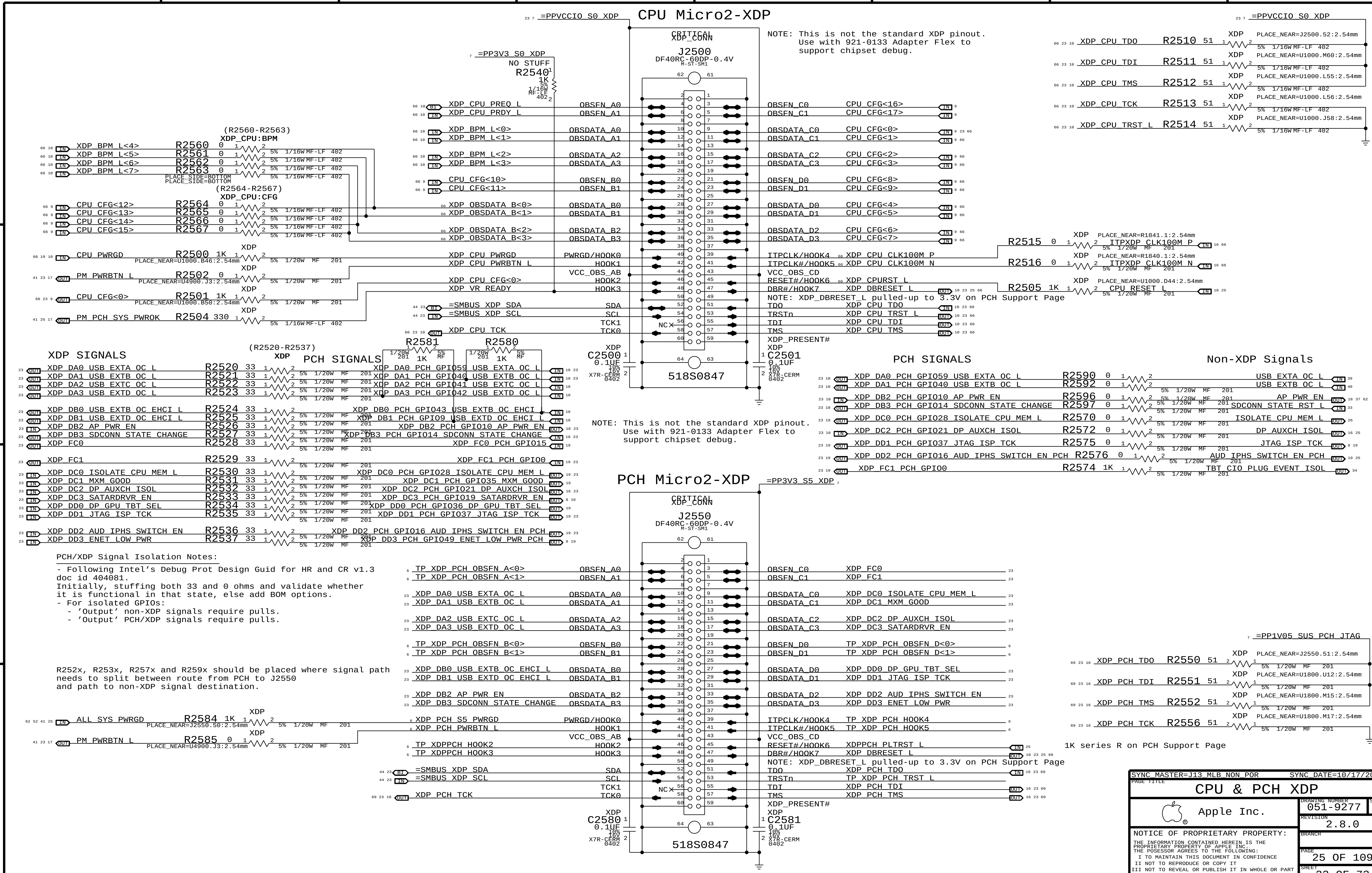
SHEET 22 OF 73



SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2011

PAGE TITLE: CPU & PCH XDP

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

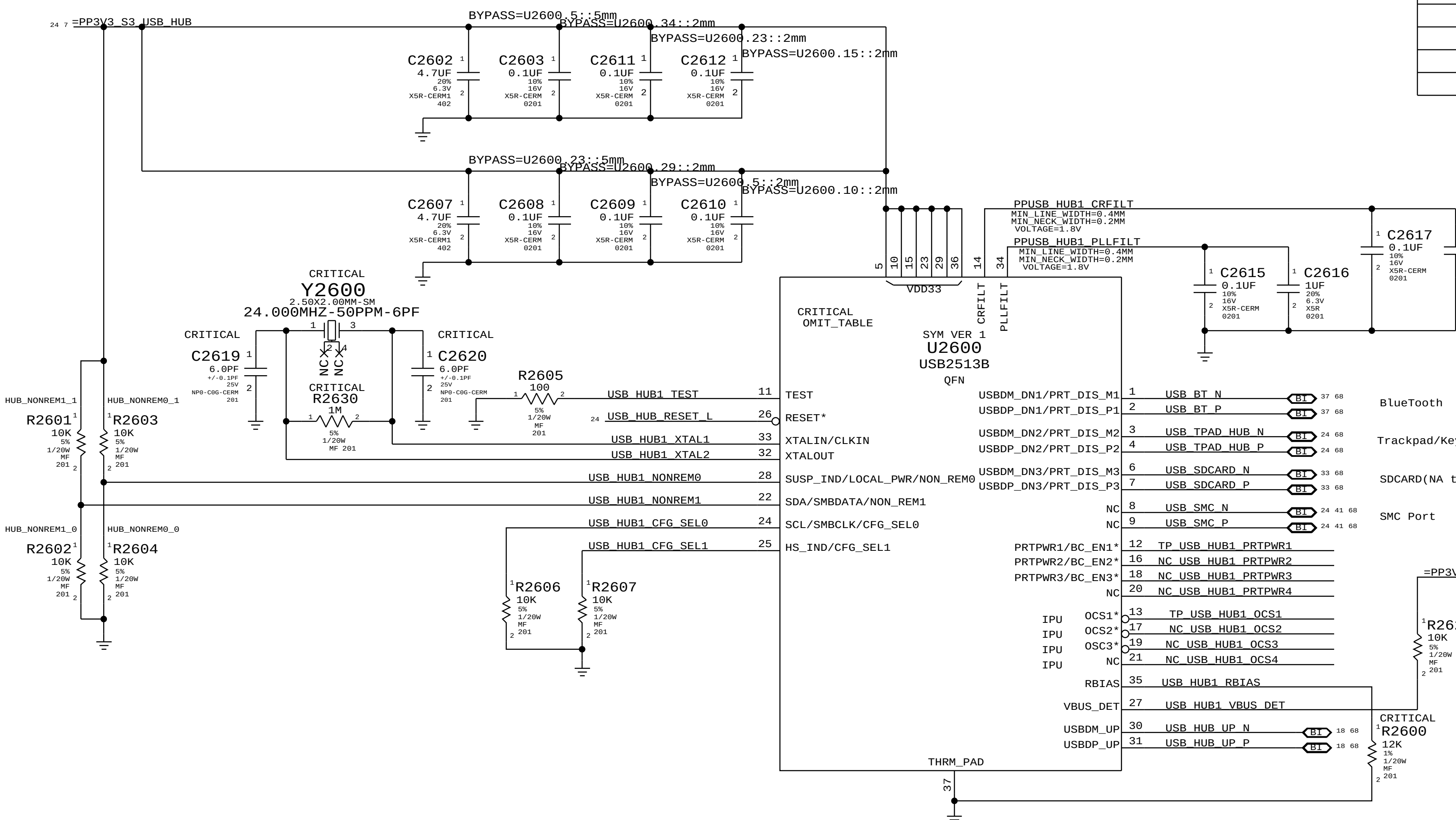
REVISION: 2.8.0

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

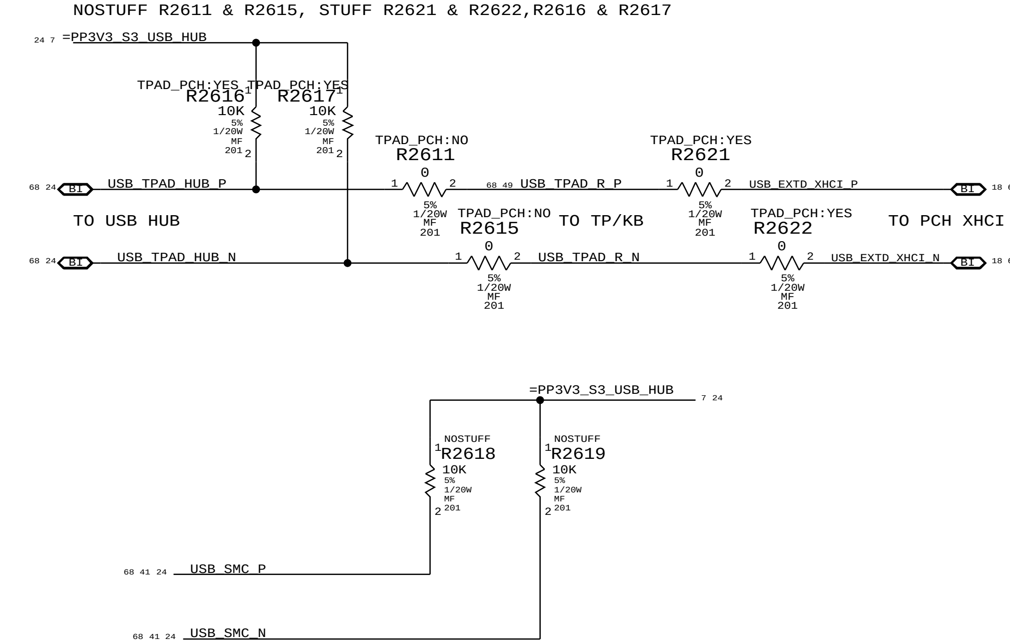
NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

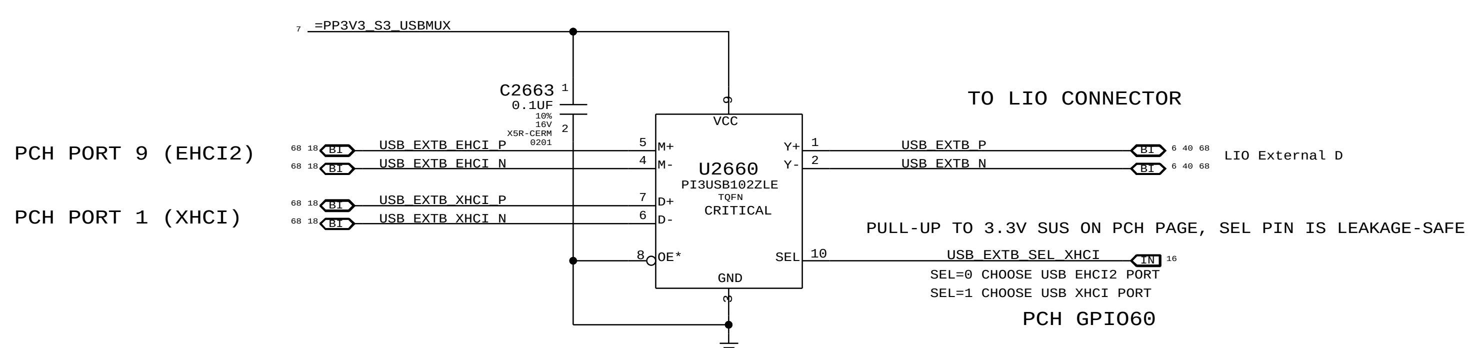
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0983	1	IC,USB2512B,USB 2.0 HUB CNTRL,36-QFN	U2600	CRITICAL	USBHUB2512B
338S0923	1	IC,USB2513B,USB 2.0,HUB CNTRL,3PRT,36QFN	U2600	CRITICAL	USBHUB2513B
338S0824	1	IC,USB2514B,USB 2.0,HUB CNTRL,4PRT	U2600	CRITICAL	USBHUB2514B

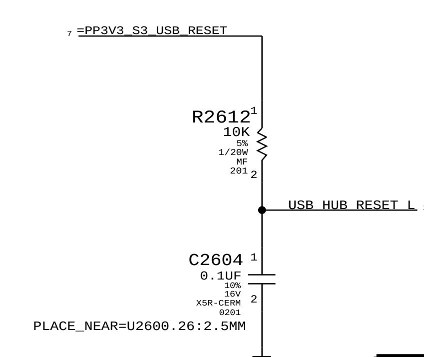


TO CONNECT TP/KB TO PCH XHCI
NOSTUFF R2611 & R2615, STUFF R2621 & R2622,R2616 & R2617



USB XHCI/EHCI2 PORT MUX FOR EXT B





SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE
USB HUB & MUX

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D
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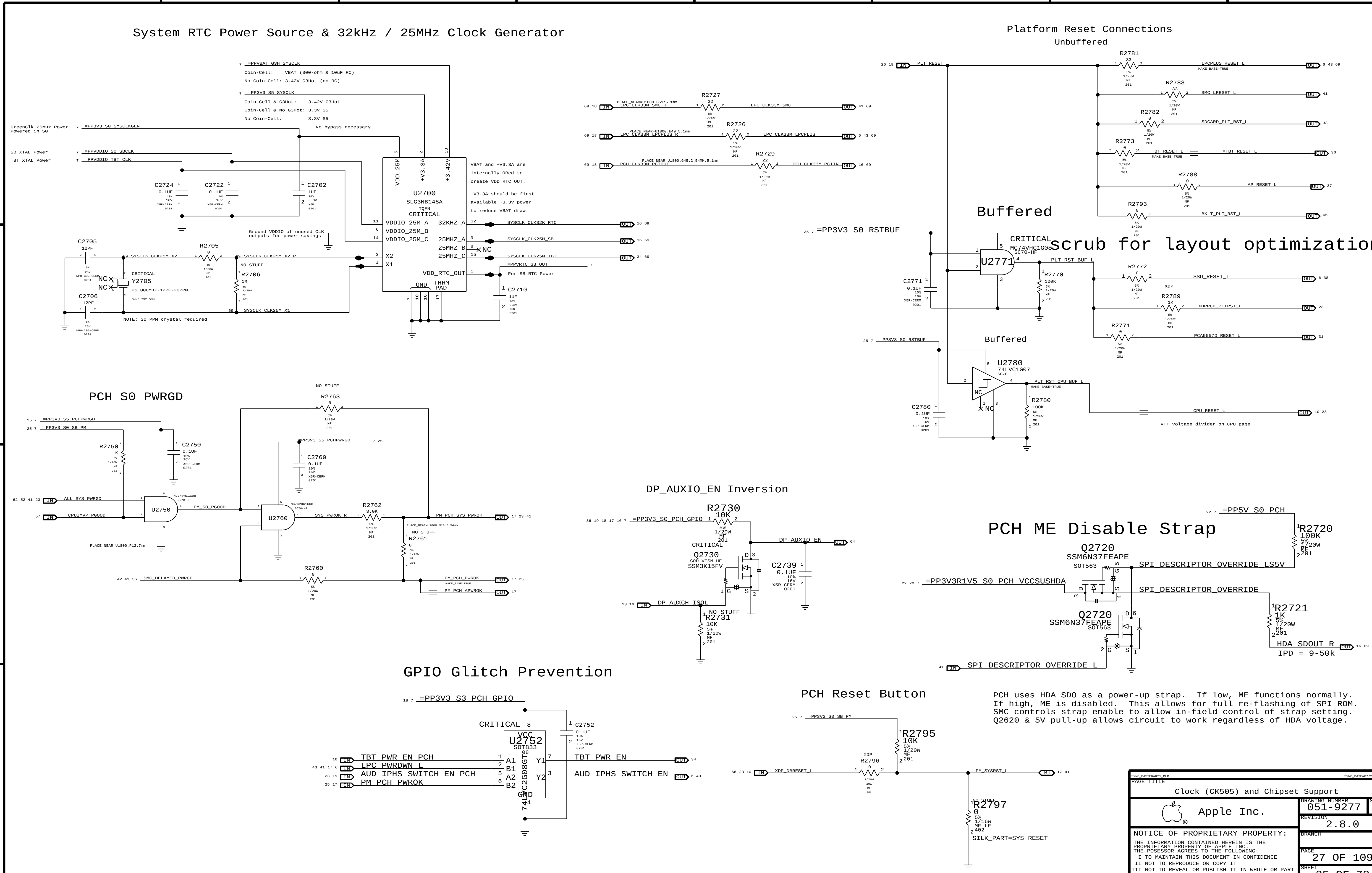

PAGE TITLE: Clock (CK505) and Chipset Support

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

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SHEET: 25 OF 73

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

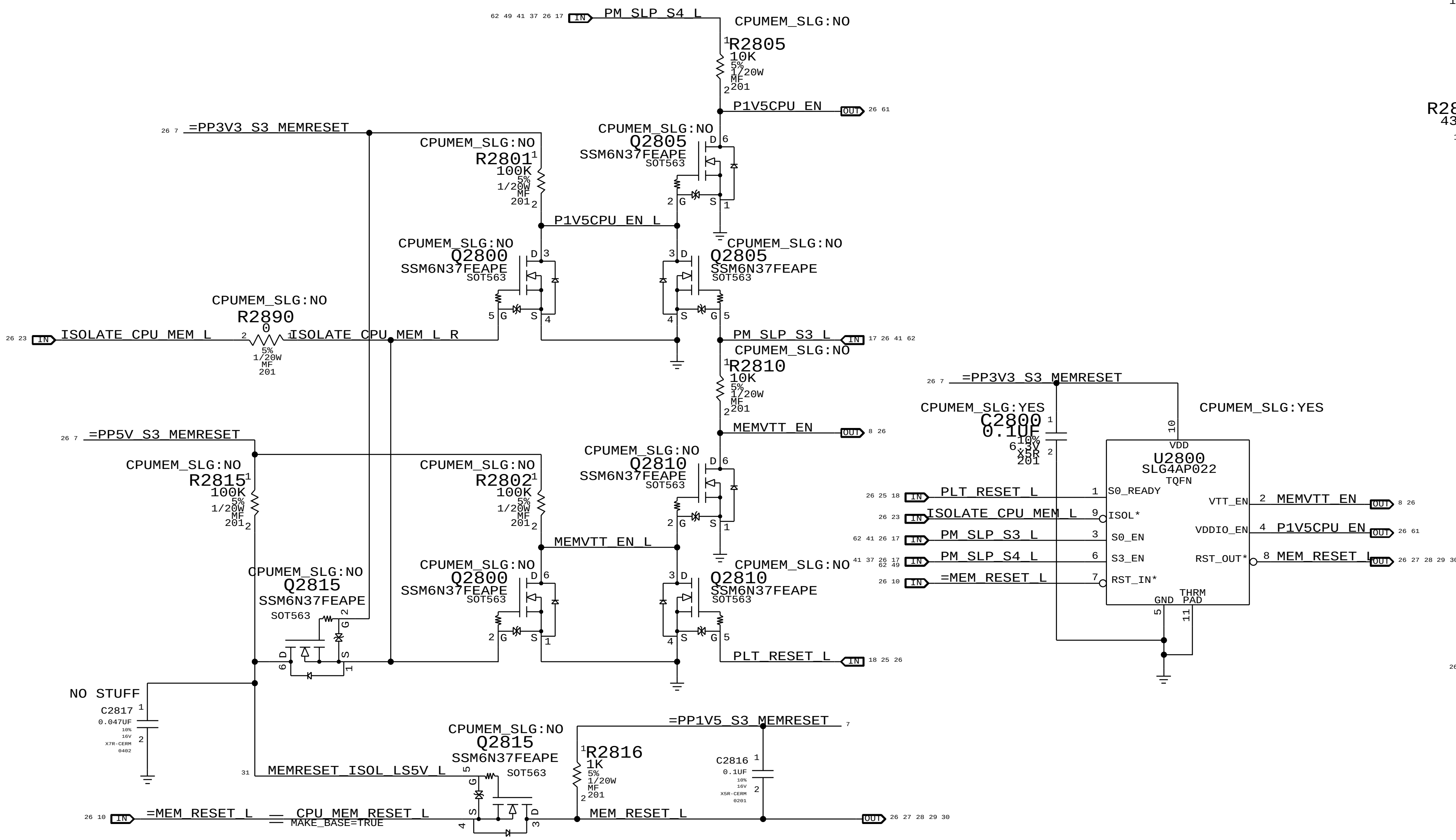
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

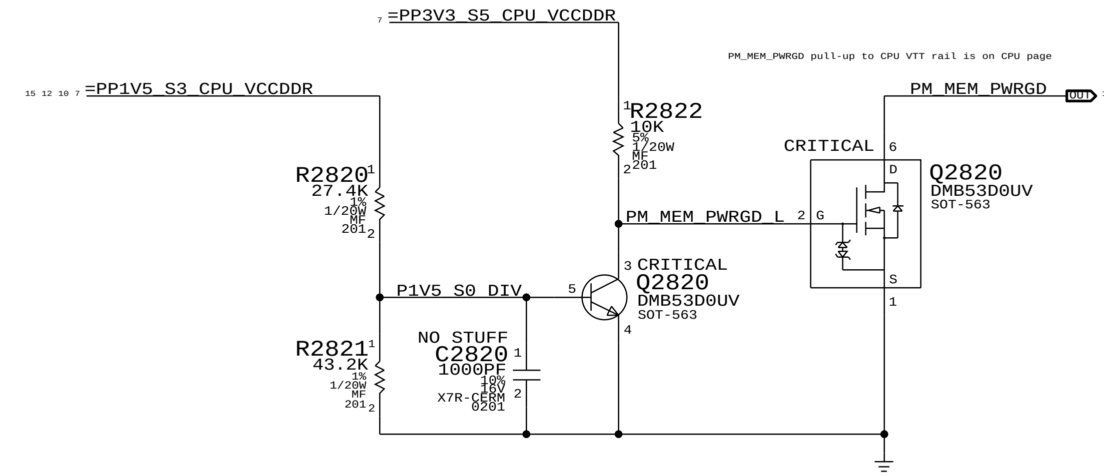
P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

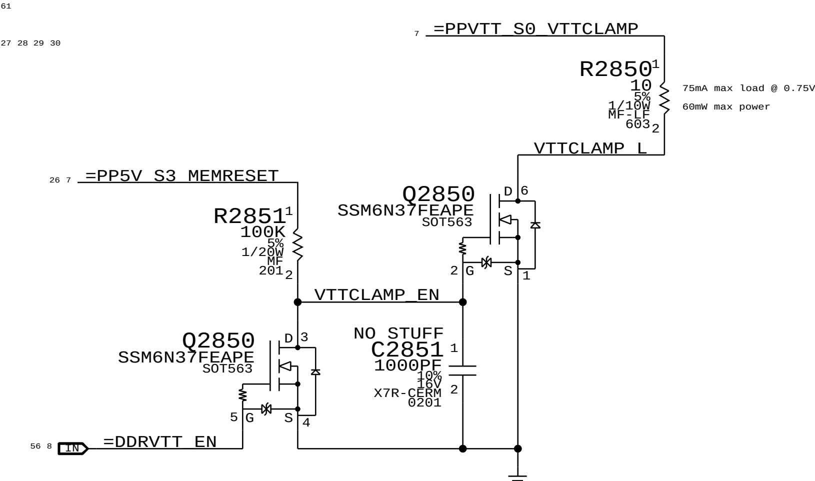


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
S3									
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

CPU Memory S3 Support

Apple Inc.

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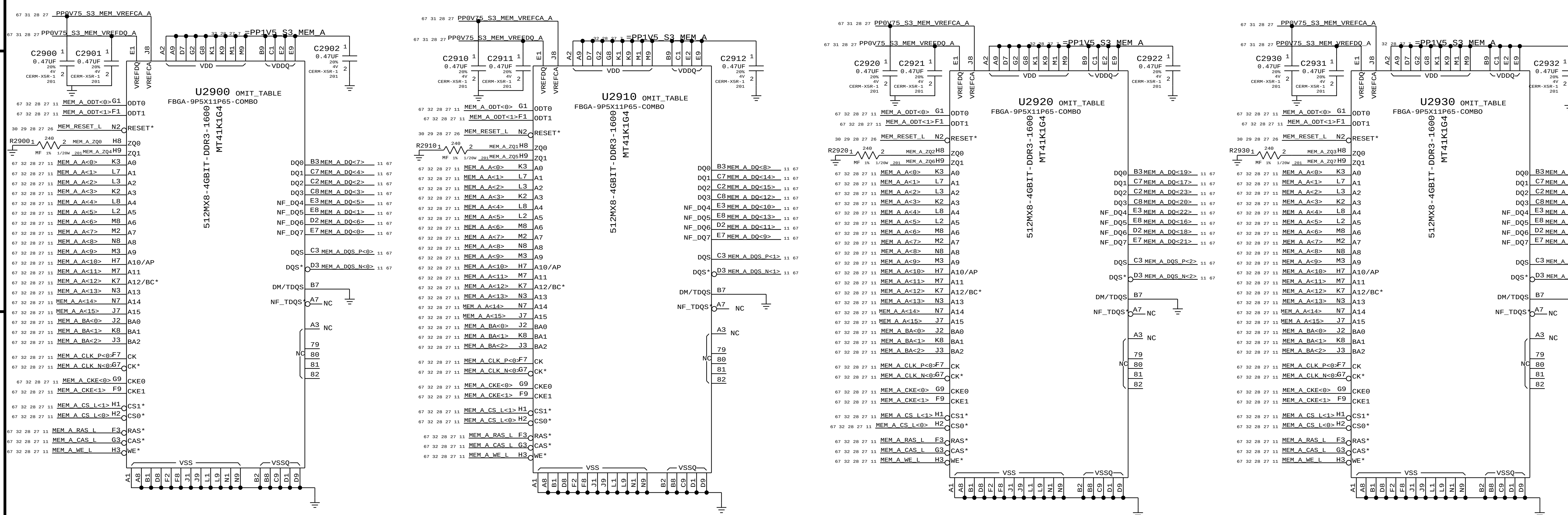
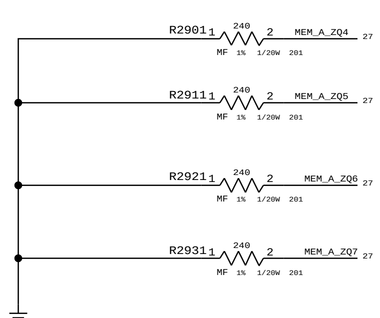


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

DDR3 DRAM CHANNEL A (0-31)

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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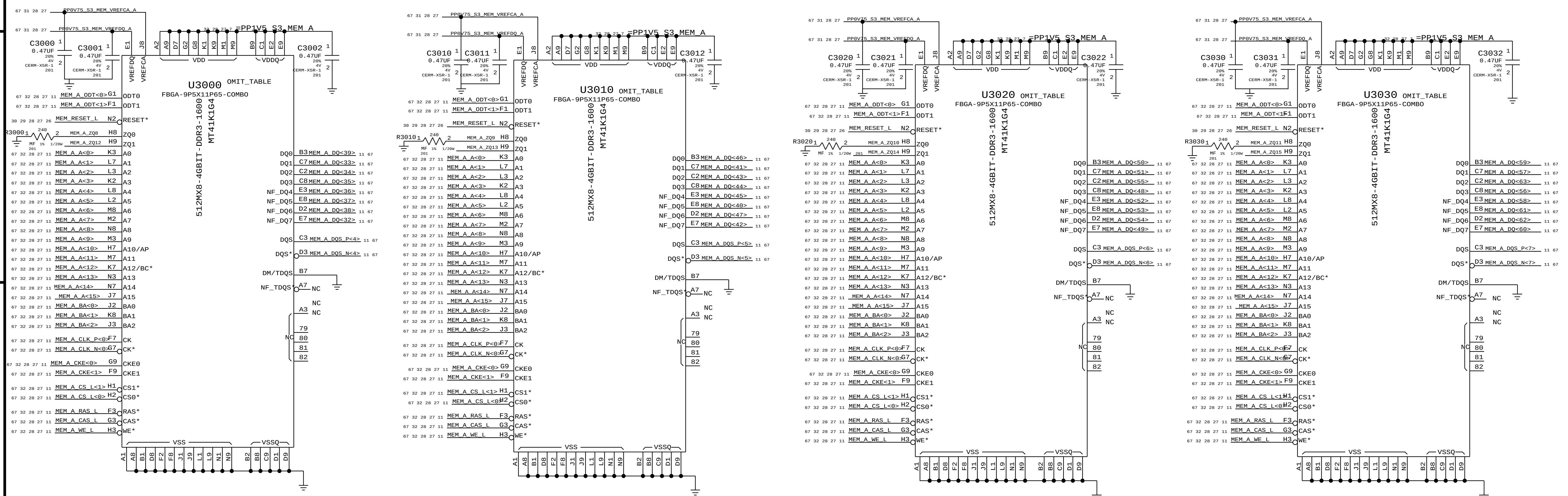
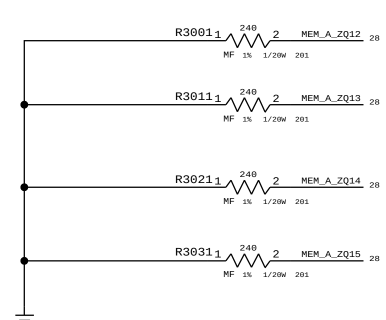
SHEET 27 OF 73



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL



SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

DDR3 DRAM CHANNEL A (32-63)

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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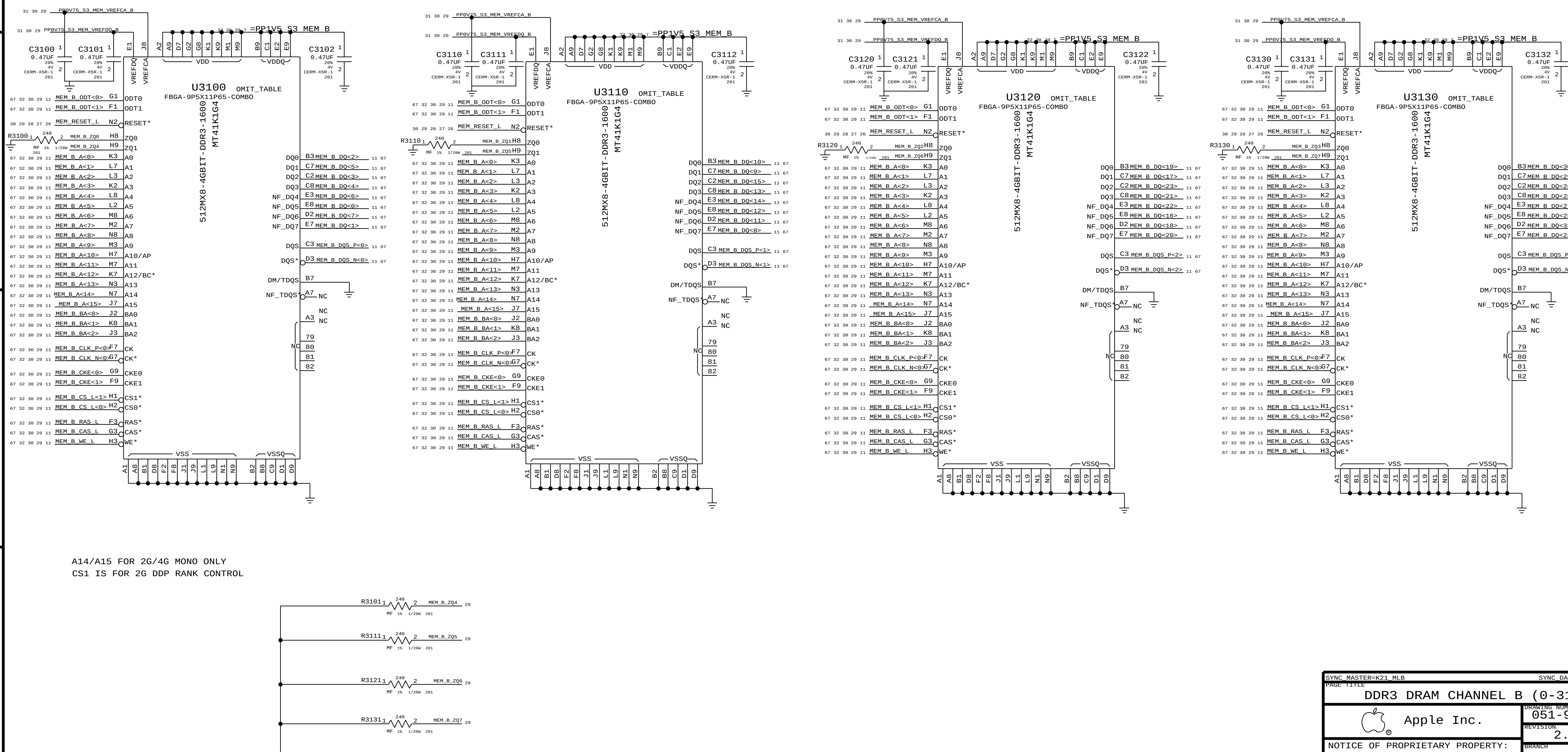

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

DDR3 DRAM CHANNEL B (0-31)

DRAWING NUMBER 051-9277 SIZE D

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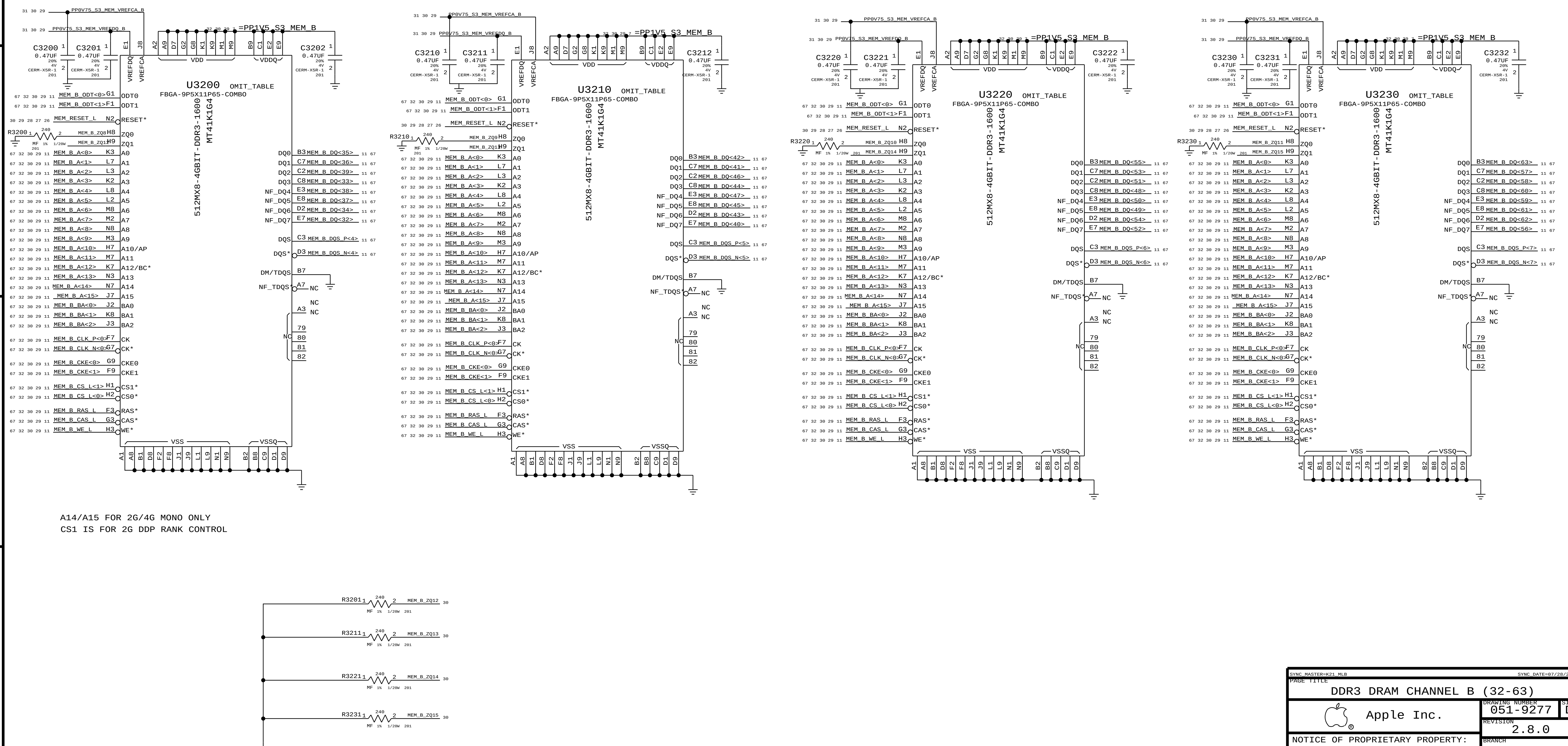
8 7 6 5 4 3 2 1

D

C

B

A



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

DDR3 DRAM CHANNEL B (32-63)

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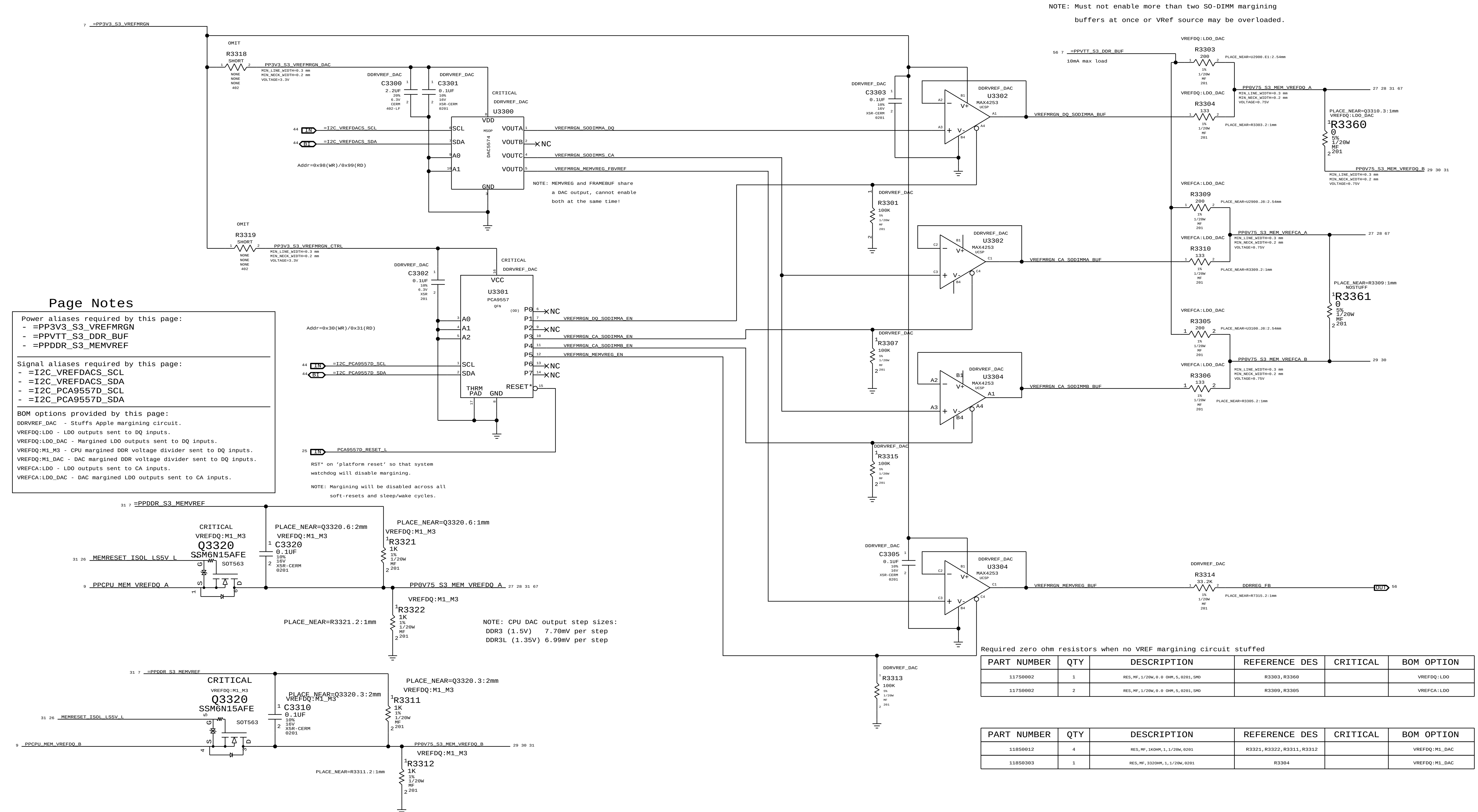
NOTICE OF PROPRIETARY PROPERTY:

8 7 6 5 4 3 2 1

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:

DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	1	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3303,R3360		VREFDQ:LDO
117S0002	2	RES,MF,1/20W,0.0 OHM,5,0201,SMD	R3309,R3305		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0012	4	RES,MF,1KOHM,1,1/20W,0201	R3321,R3322,R3311,R3312		VREFDQ:M1_DAC
118S0303	1	RES,MF,332OHM,1,1/20W,0201	R3304		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=J11_MLB SYNC_DATE=08/04/2011

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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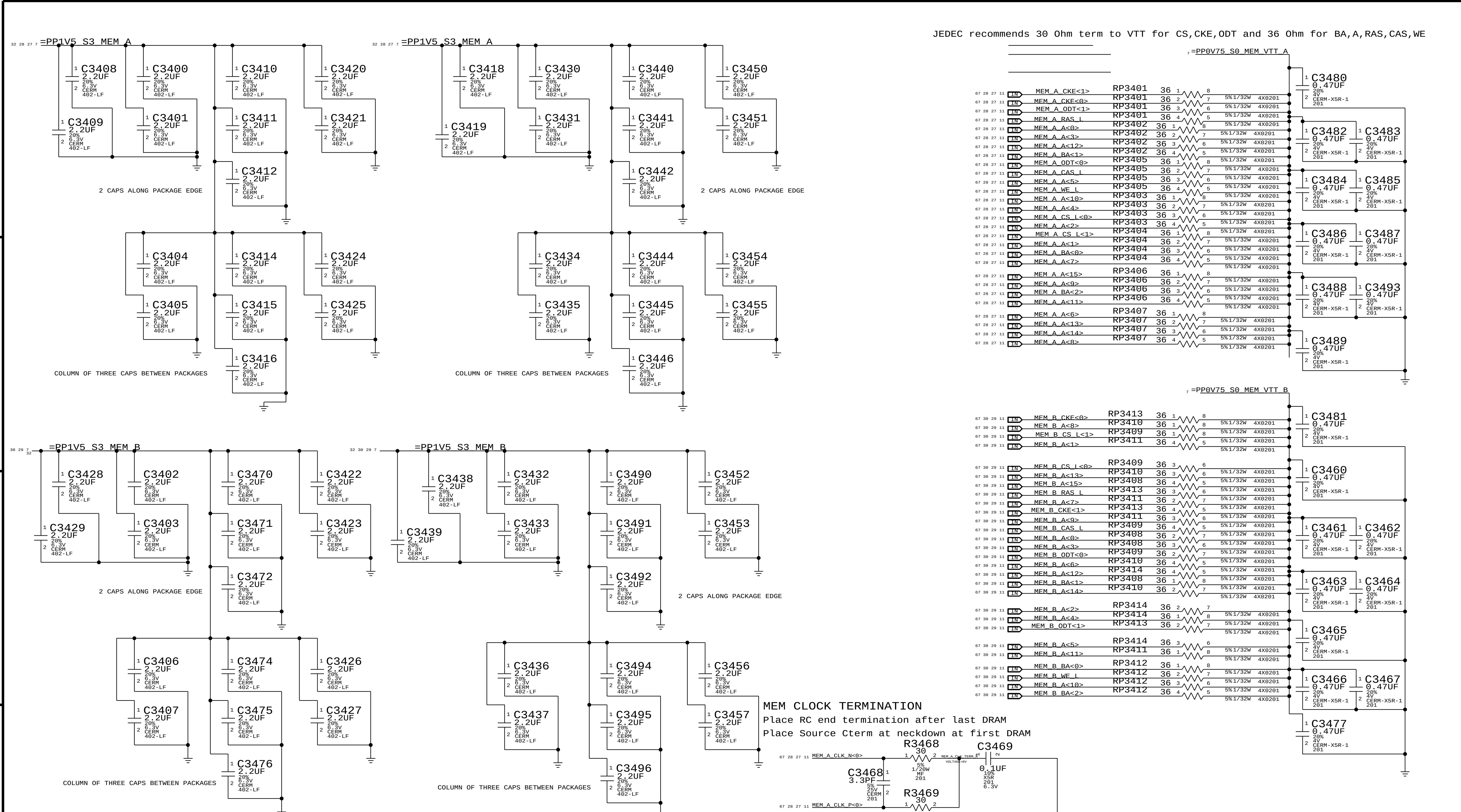

SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

DDR3 Bypassing/Termination

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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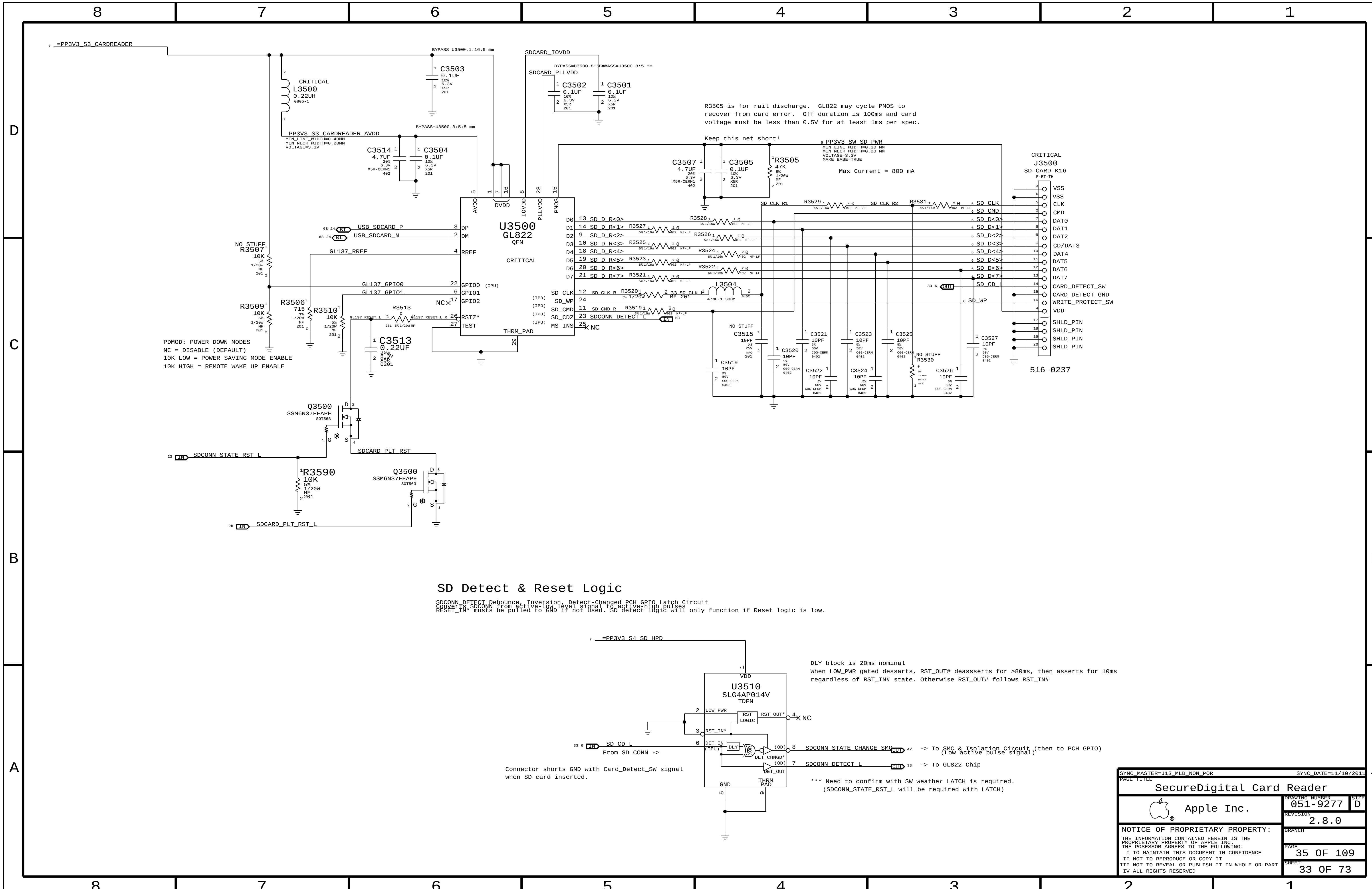
=PP3V3_S3_CARDREADER
CRITICAL
L3500
0.22UH
0805-1
C3503
0.1UF
C3502
0.1UF
C3501
0.1UF
SDCARD_IOVDD
SDCARD_PLLVDD
PP3V3_S3_CARDREADER_AVDD
MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
C3514
4.7UF
C3504
0.1UF
R3505 is for rail discharge. GL822 may cycle PMOS to
recover from card error. Off duration is 100ms and card
voltage must be less than 0.5V for at least 1ms per spec.
Keep this net short!
PP3V3_SW_SD_PWR
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
C3507
4.7UF
C3505
0.1UF
R3505
47K
Max Current = 800 mA
CRITICAL
J3500
SD-CARD-K16
F-RT-TH
VSS
VSS
CLK
CMD
DAT0
DAT1
DAT2
CD/DAT3
DAT4
DAT5
DAT6
DAT7
CARD_DETECT_SW
CARD_DETECT_GND
WRITE_PROTECT_SW
VDD
SHLD_PIN
SHLD_PIN
SHLD_PIN
SHLD_PIN
516-0237
U3500
GL822
QFN
CRITICAL
AVDD
DVDD
IOVDD
PLLVDD
PMOS
USB_SDCARD_P
USB_SDCARD_N
GL137_RREF
GL137_GPIO0
GL137_GPIO1
NO STUFF
R3507
10K
R3509
10K
R3506
715
R3510
10K
R3513
0
C3513
0.22UF
THRM_PAD
SD_CLK
SD_CMD
SD_D<0>
SD_D<1>
SD_D<2>
SD_D<3>
SD_D<4>
SD_D<5>
SD_D<6>
SD_D<7>
SD_CD_L
SD_WP
SDCONN_DETECT_L
L3504
47NH-1.3OHM
PDMOD: POWER DOWN MODES
NC = DISABLE (DEFAULT)
10K LOW = POWER SAVING MODE ENABLE
10K HIGH = REMOTE WAKE UP ENABLE
Q3500
SSM6N37FEAPE
SOT563
SDCONN_STATE_RST_L
SDCARD_PLT_RST
R3590
10K
SDCARD_PLT_RST_L
SD Detect & Reset Logic
SDCONN_DETECT Debounce, Inversion, Detect-Changed PCH GPIO Latch Circuit
Converts SDCONN from active-low level signal to active-high pulses
RESET_IN* musts be pulled to GND if not used. SD detect logic will only function if Reset logic is low.
=PP3V3_S4_SD_HPD
U3510
SLG4AP014V
TDFN
LOW_PWR
RST_IN*
DET_IN
RST LOGIC
DLY
RST_OUT*
DET_CHNGD*
DET_OUT
THRM PAD
GND
DLY block is 20ms nominal
When LOW_PWR gated dessarts, RST_OUT# deassserts for >80ms, then asserts for 10ms
regardless of RST_IN# state. Otherwise RST_OUT# follows RST_IN#
SD_CD_L
From SD CONN ->
SDCONN_STATE_CHANGE_SMC
-> To SMC & Isolation Circuit (then to PCH GPIO)
(Low active pulse signal)
SDCONN_DETECT_L
-> To GL822 Chip
Connector shorts GND with Card_Detect_SW signal
when SD card inserted.
*** Need to confirm with SW weather LATCH is required.
(SDCONN_STATE_RST_L will be required with LATCH)
SYNC_MASTER=J13_MLB_NON_POR
SYNC_DATE=11/10/2011
PAGE TITLE
SecureDigital Card Reader
Apple Inc.
DRAWING NUMBER
051-9277
SIZE
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REVISION
2.8.0
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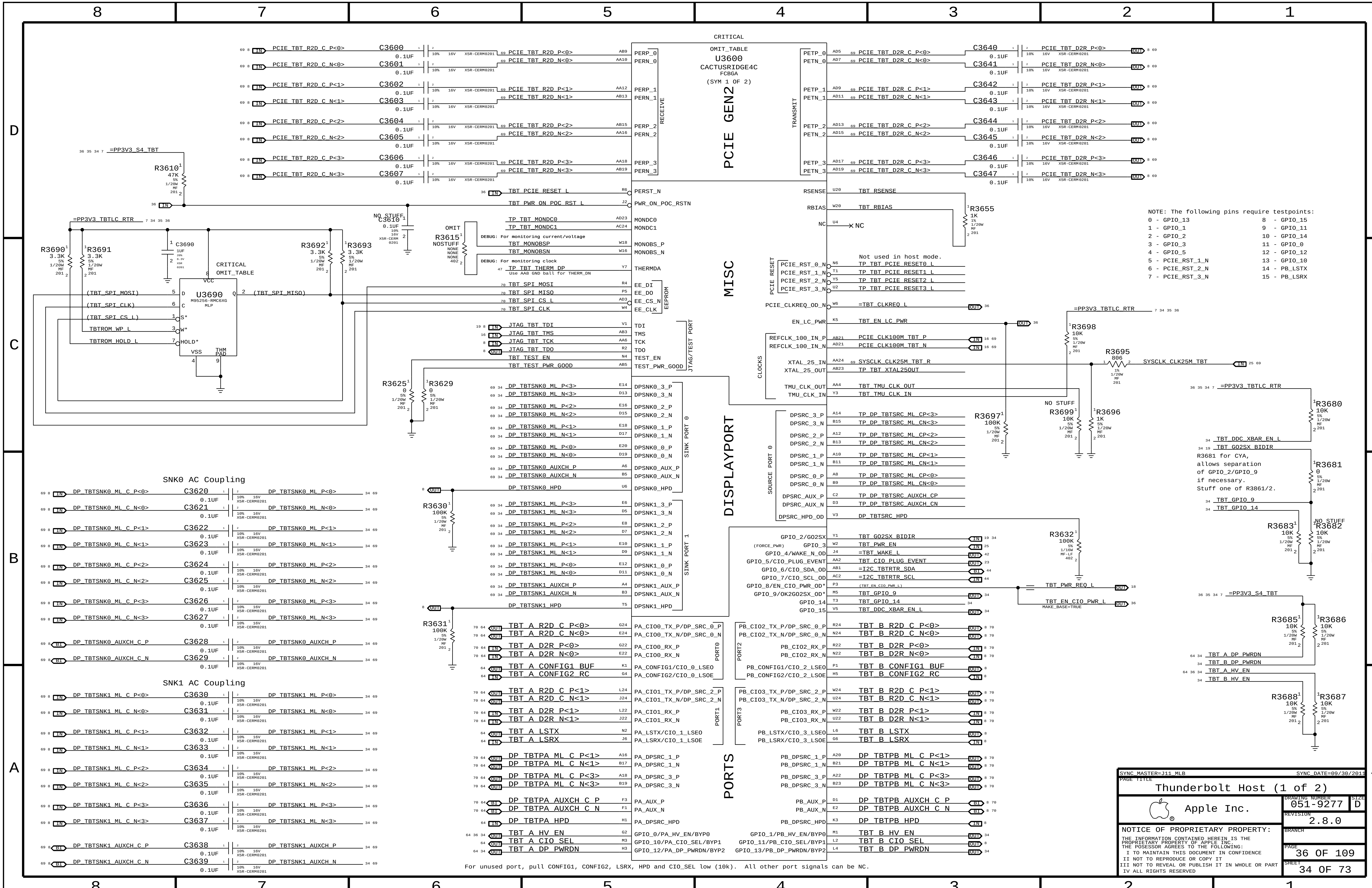
33 OF 73



CRITICAL
OMIT_TABLE
U3600
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)
PCIE GEN2
MISC
DISPLAYPORT
PORTS
RECEIVE
TRANSMIT
EEPROM
JTAG/TEST PORT
PCIE RESET
CLOCKS
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
PORT0
PORT1
PORT2
PORT3
U3690
M95256-RMC6XG
MLP
CRITICAL
OMIT_TABLE
DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
Not used in host mode.
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
R3681 for CYA,
allows separation
of GPIO_2/GPIO_9
if necessary.
Stuff one of R3861/2.
SNK0 AC Coupling
SNK1 AC Coupling
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=J11_MLB
SYNC_DATE=09/30/2011
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
051-9277
SIZE
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REVISION
2.8.0
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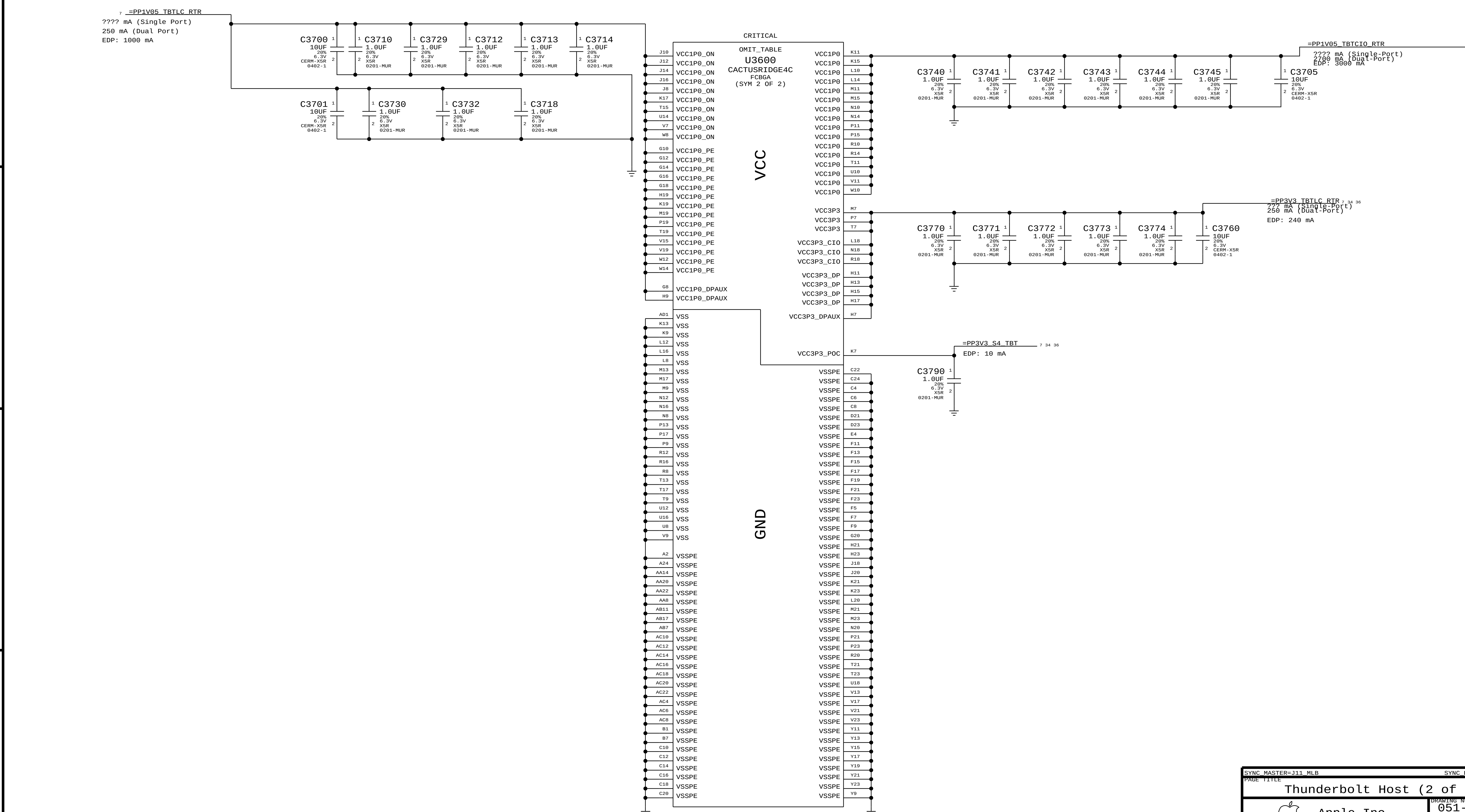

SYNC_MASTER=J11_MLB SYNC_DATE=10/04/2011

PAGE TITLE

Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER	SIZE
051-9277	D

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP18V_TBT_REG (18V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 18V boost circuitry.

TBT 15V Boost Regulator

Supervisor & CLKREQ# Isolation

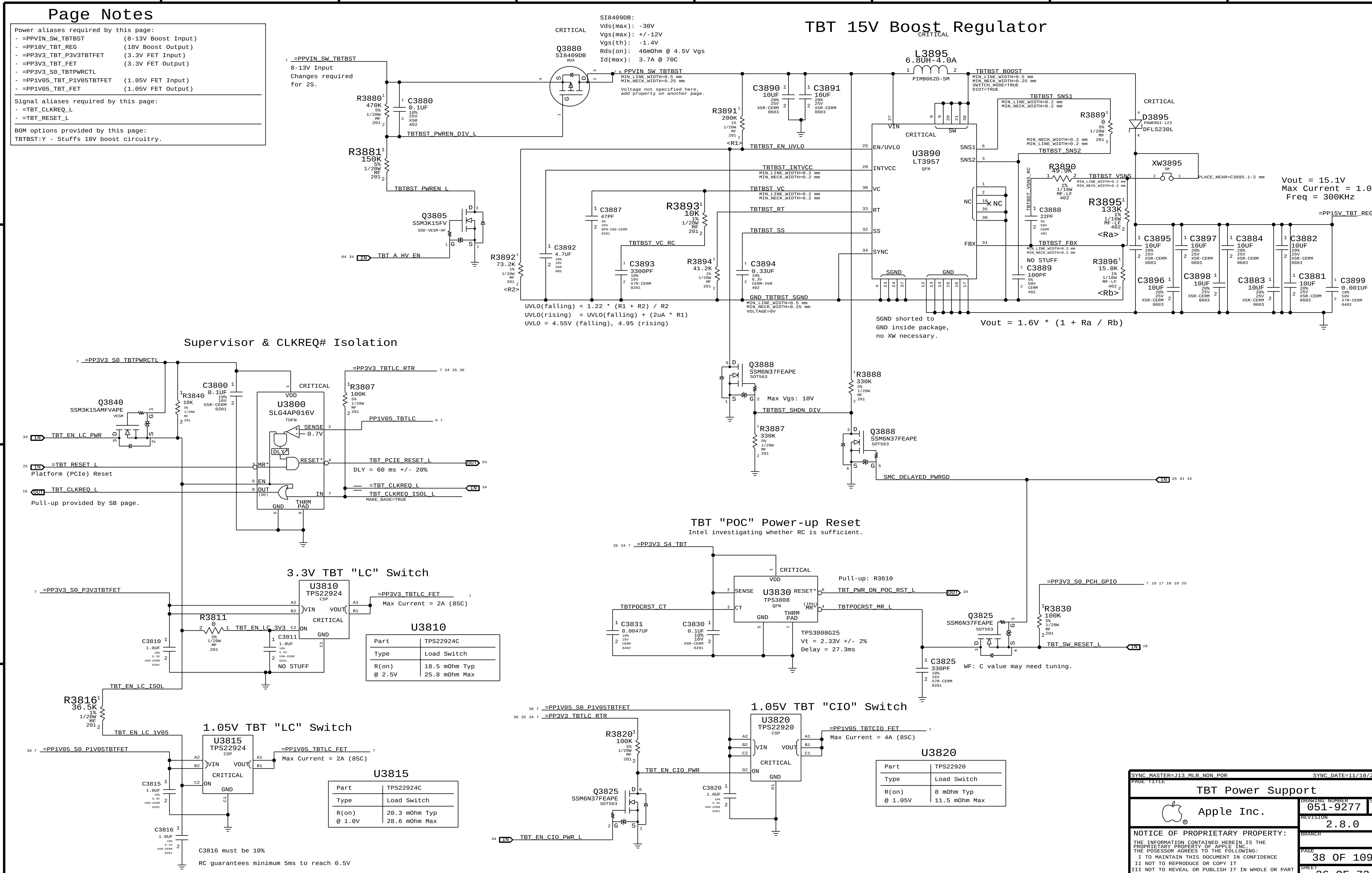
3.3V TBT "LC" Switch

1.05V TBT "LC" Switch

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

1.05V TBT "CIO" Switch



SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

Vout = 1.6V * (1 + Ra / Rb)

SGND shorted to GND inside package, no XW necessary.

C3816 must be 10%

RC guarantees minimum 5ms to reach 0.5V

U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

U3815

Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE: TBT Power Support

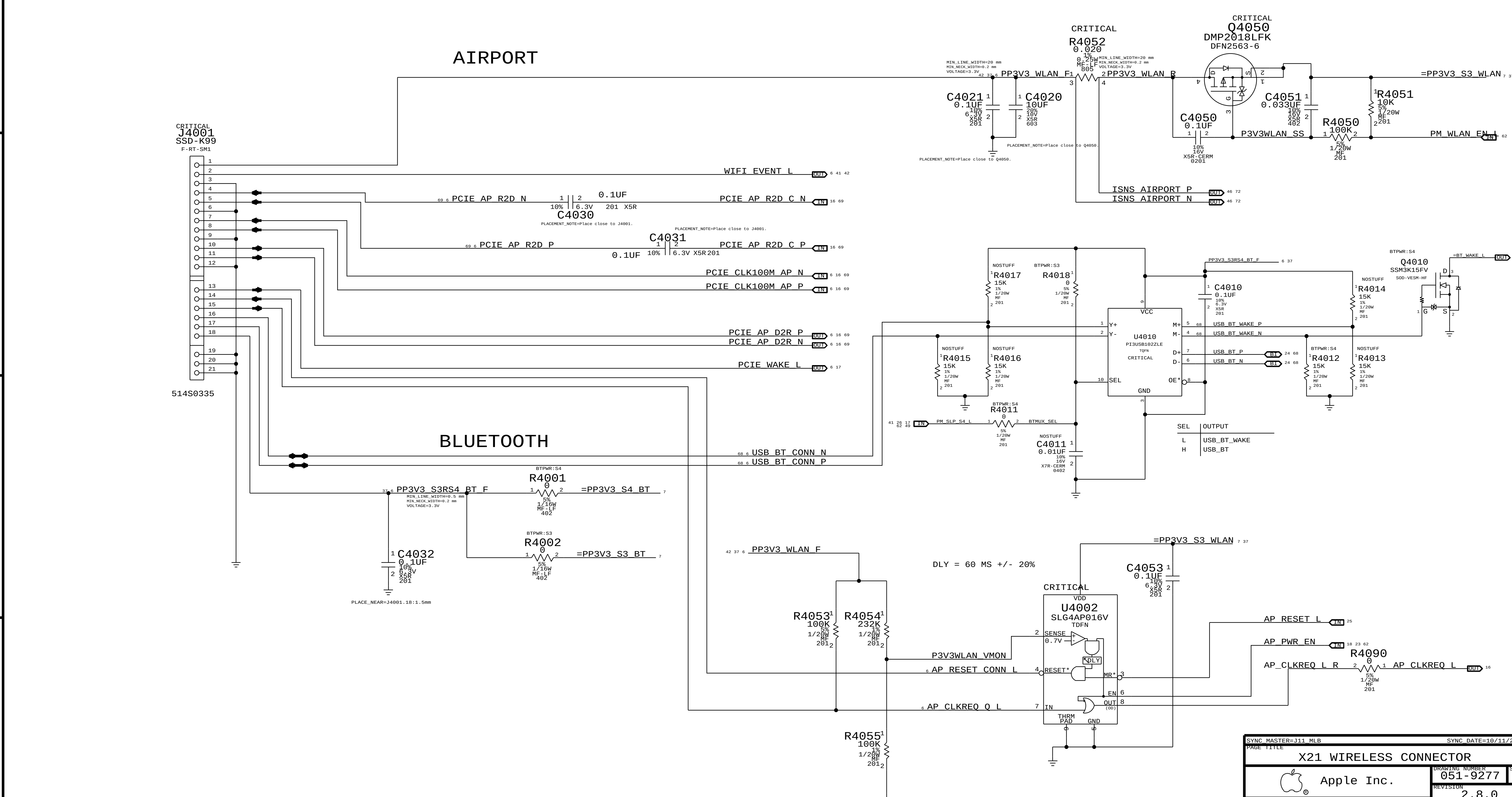
Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

3V S3 WLAN FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)



SYNC_MASTER=J11_MLB SYNC_DATE=10/11/2011

PAGE TITLE
X21 WIRELESS CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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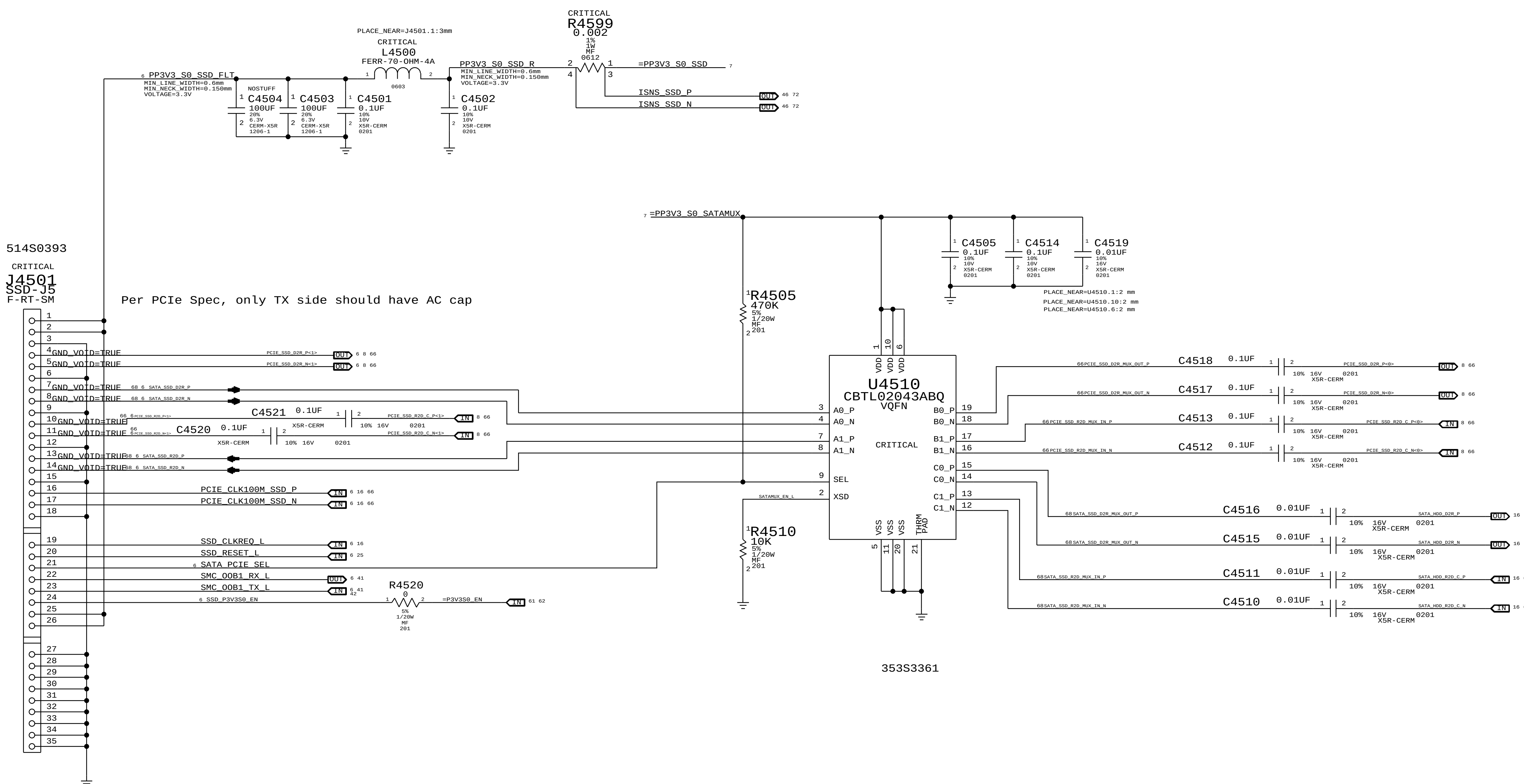

PCIE/SATA GUMSTICK2 CONNECTOR

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2011

PAGE TITLE

SSD CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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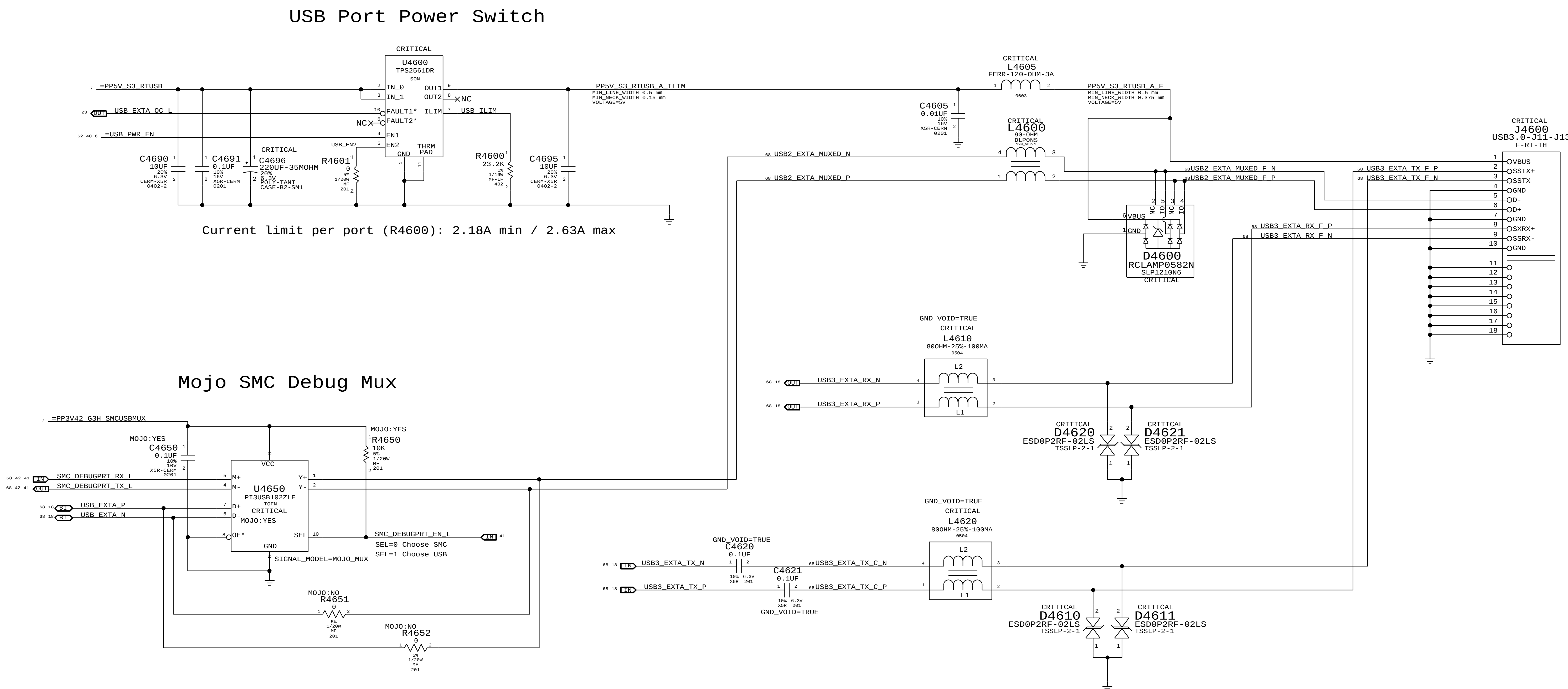
Right USB Port A



SYNC_MASTER=J11_MLB SYNC_DATE=09/30/2011

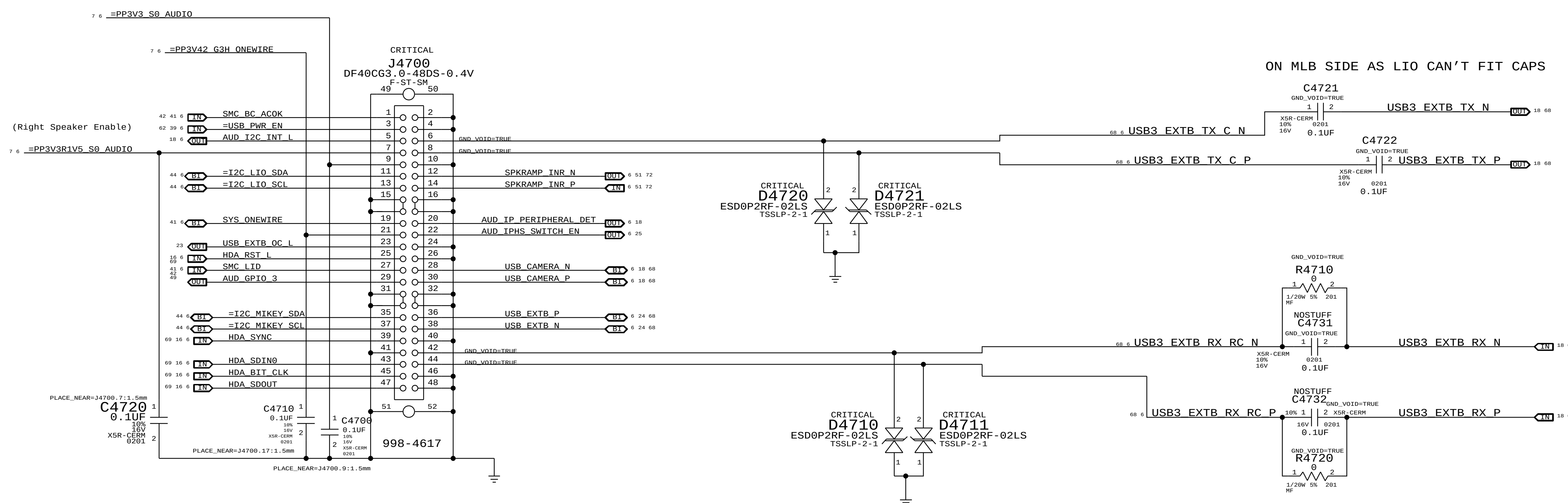
PAGE TITLE: External A USB3 Connector

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

BRANCH



SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

Left I/O (LIO) Connector

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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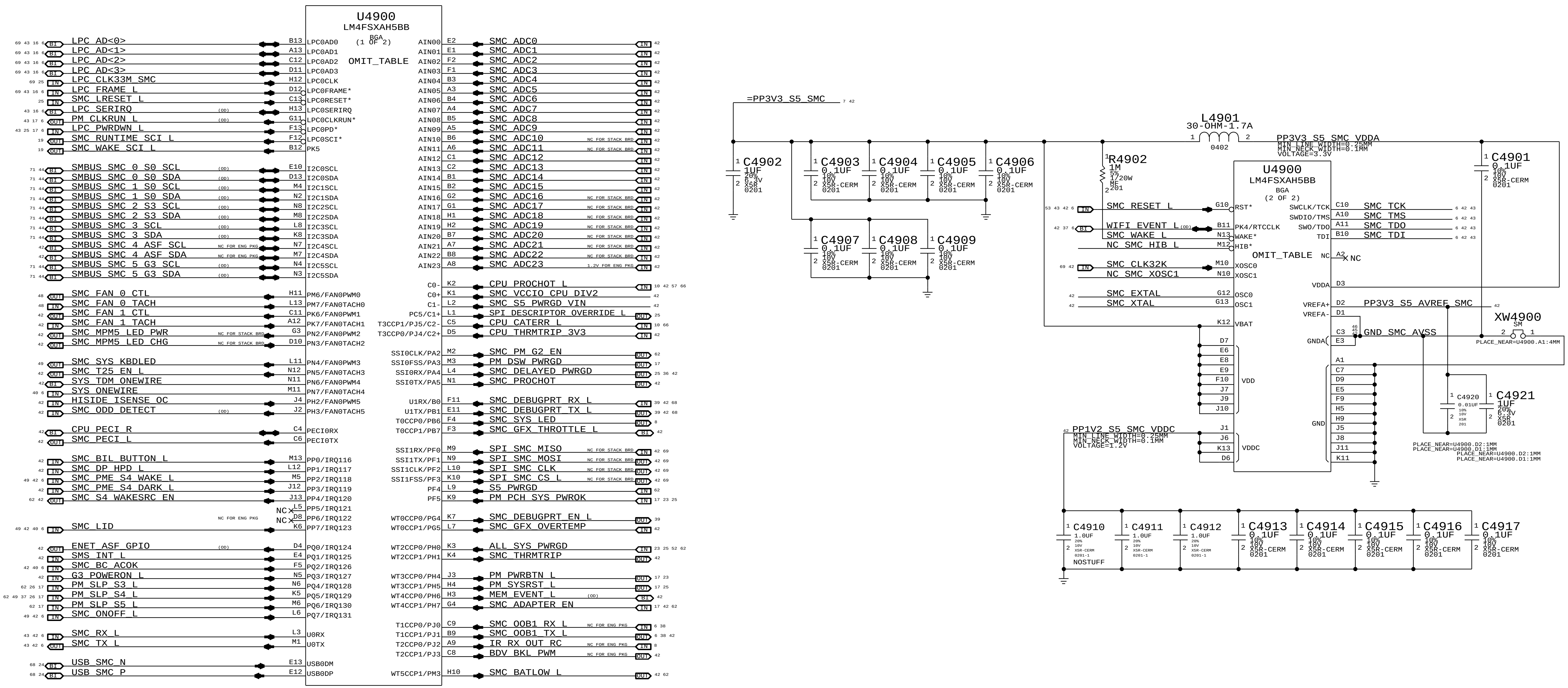
BRANCH

PAGE 47 OF 109

SHEET 40 OF 73



NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2011

PAGE TITLE
SMC

Apple Inc.

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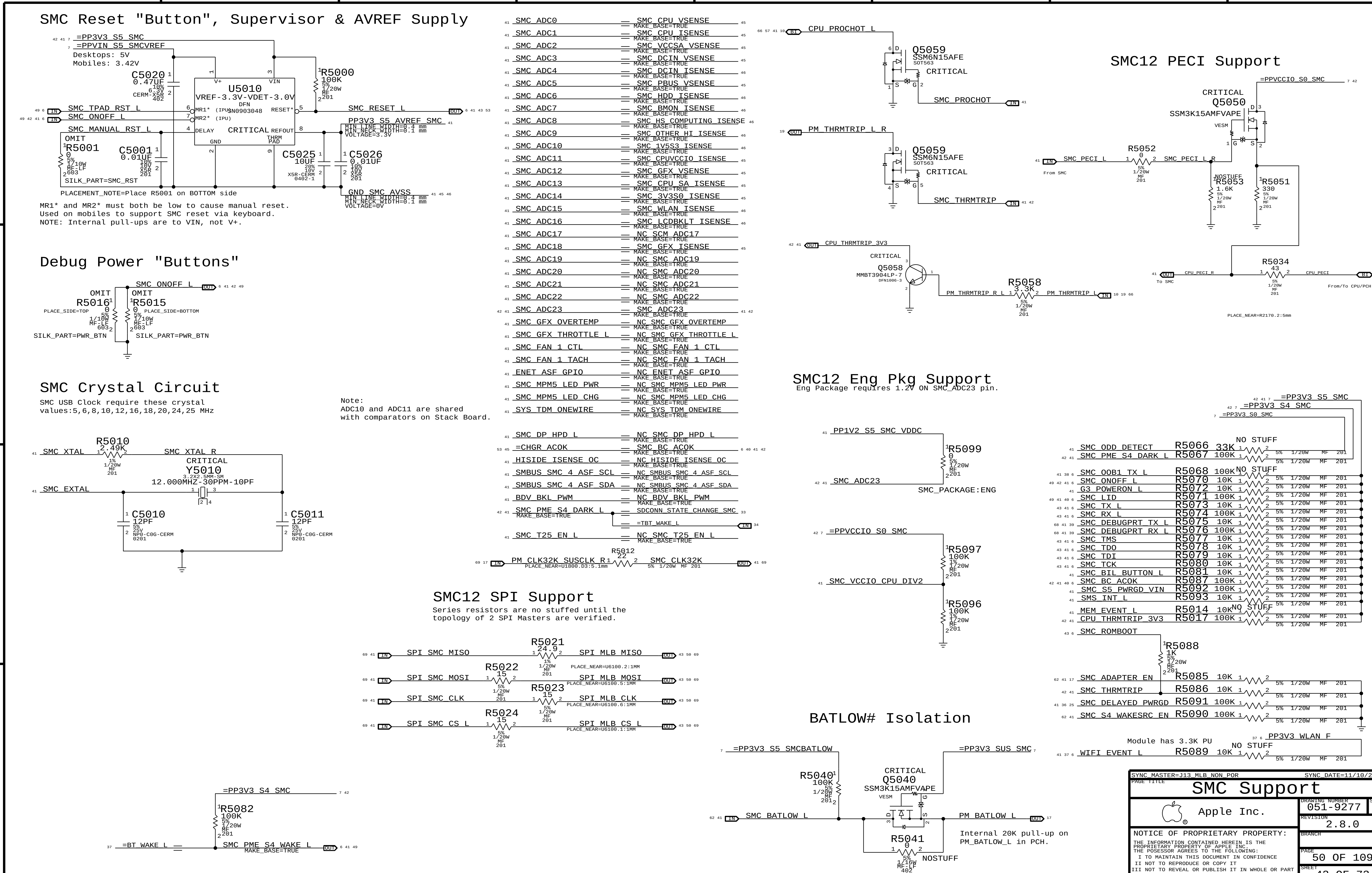

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

SMC Support

Apple Inc.

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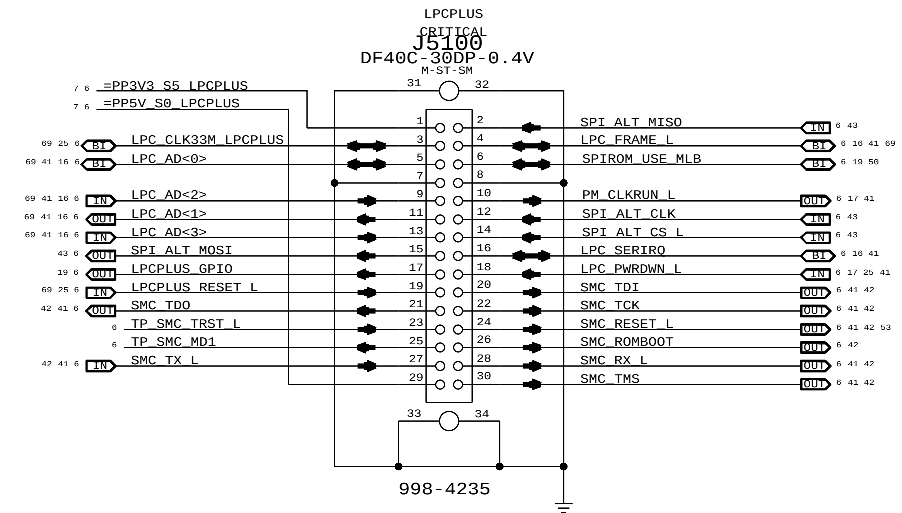
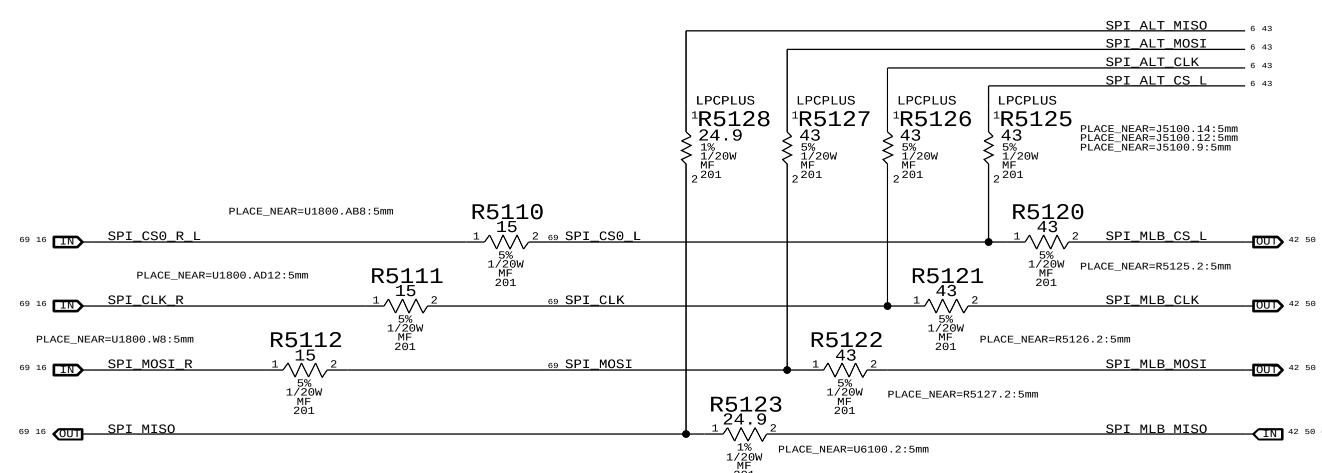
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=J11_MLB	SYNC_DATE=09/08/2011
PAGE TITLE	LPC+SPI Debug Connector
Apple Inc.	DRAWING NUMBER 051-9277 SIZE D
	REVISION 2.8.0
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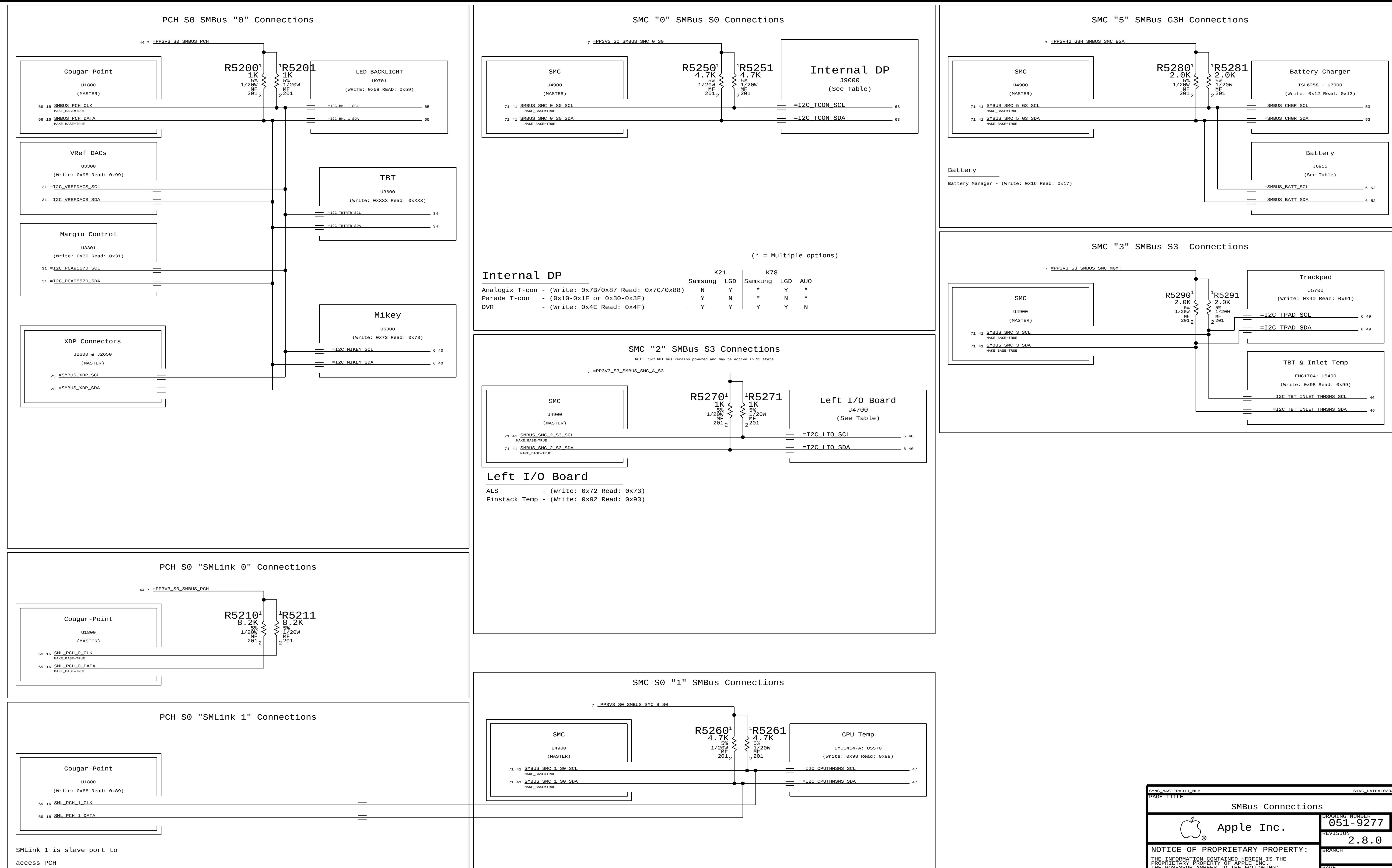
	SHEET 43 OF 73



Battery

Battery Manager - (Write: 0x16 Read: 0x17)

(* = Multiple options)

Internal DP

	K21		K78		
	Samsung	LGD	Samsung	LGD	AUO
Analogix T-con - (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con - (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR - (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

Left I/O Board

ALS - (Write: 0x72 Read: 0x73)
Finstack Temp - (Write: 0x92 Read: 0x93)

SMLink 1 is slave port to access PCH

SYNC_MASTER=J11_MLB SYNC_DATE=10/04/2011

PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

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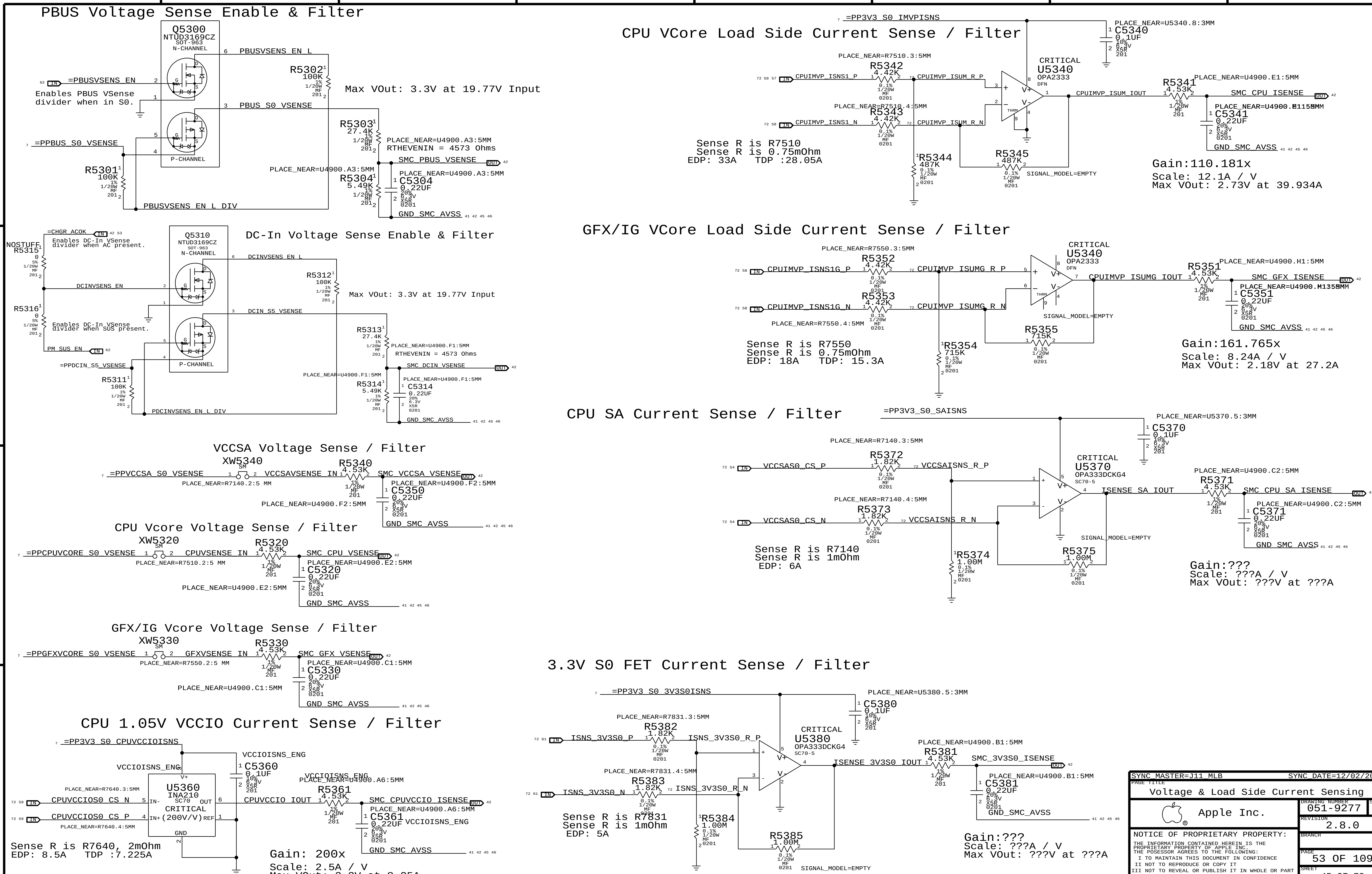
PAGE: 52 OF 109

SHEET: 44 OF 73



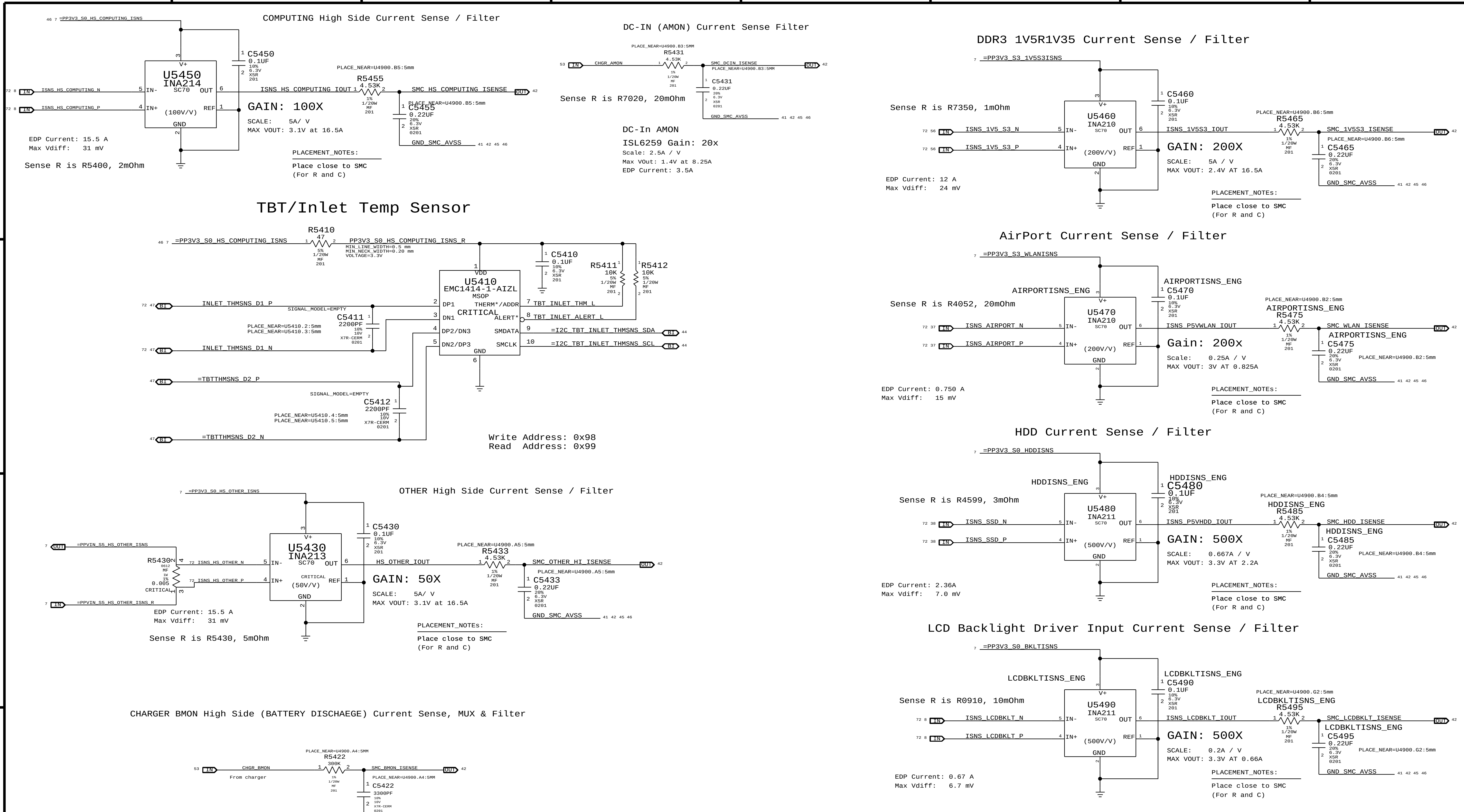
SYNC_MASTER=J11_MLB SYNC_DATE=12/02/2011

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0



SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2011

PAGE TITLE: High Side Current Sensing

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

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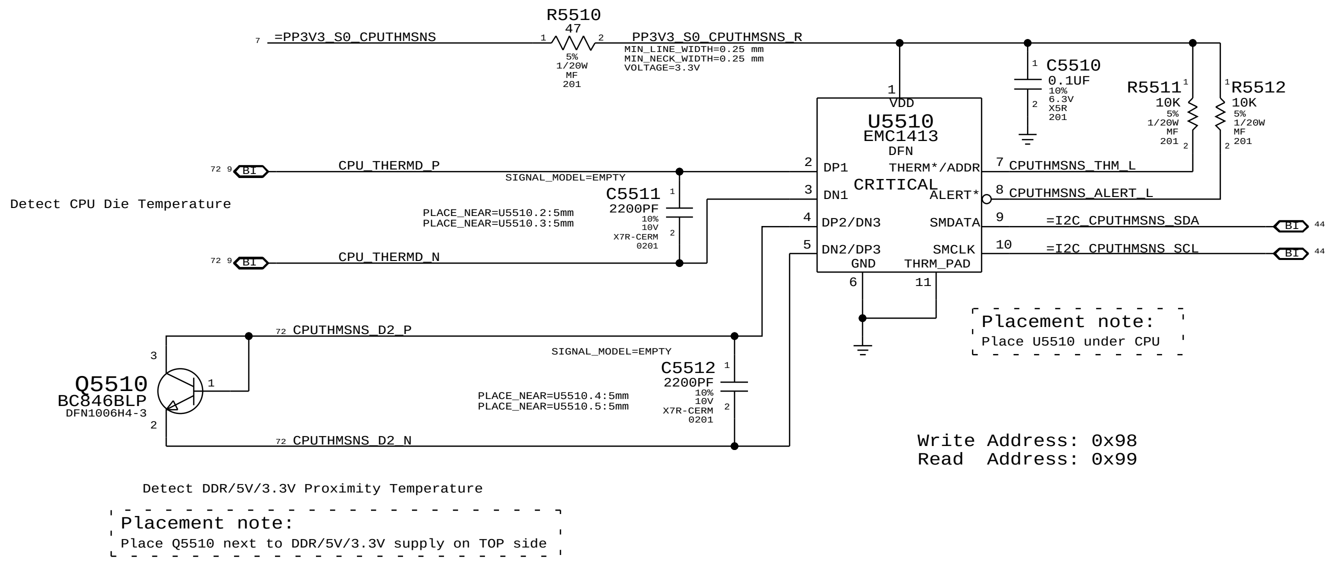
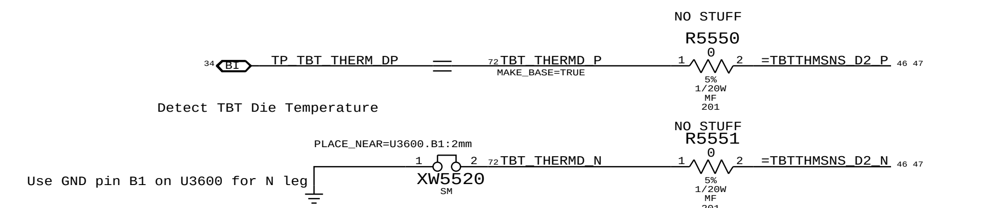
PAGE: 54 OF 109

SHEET: 46 OF 73

CPU Proximity Sensor



TBT Die

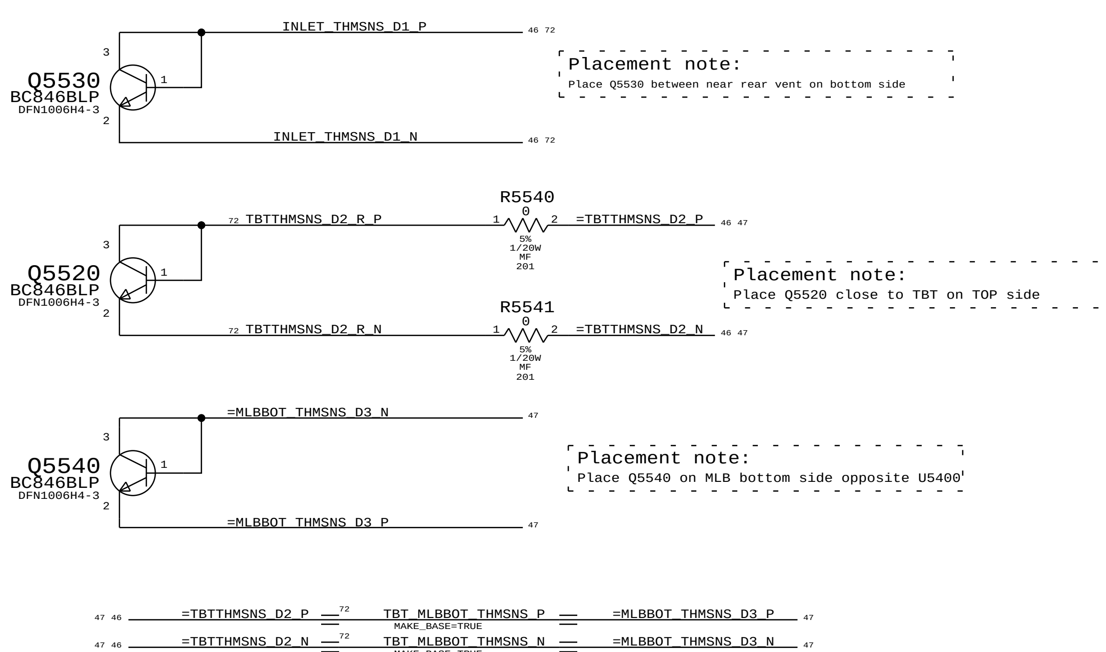


To connect Die Sensor, Stuff R5550 & R5551, No stuff R5540 & R5541
To connect Proximity Sensor, Stuff R5540 & R5541, No Stuff R5550,R5551

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors



SYNC_MASTER=J11_MLB SYNC_DATE=08/03/2011
PAGE TITLE
Thermal Sensors
Apple Inc.
DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
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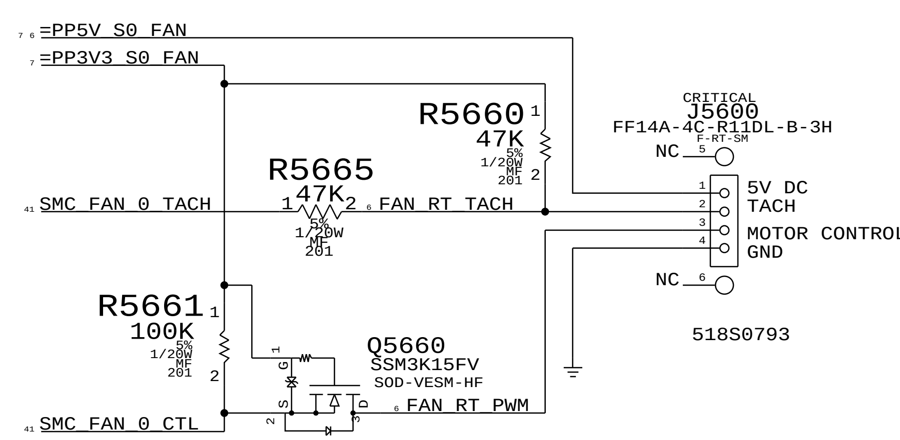
PAGE 55 OF 109
SHEET 47 OF 73

FAN CONNECTOR



SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

Fan

Apple Inc.

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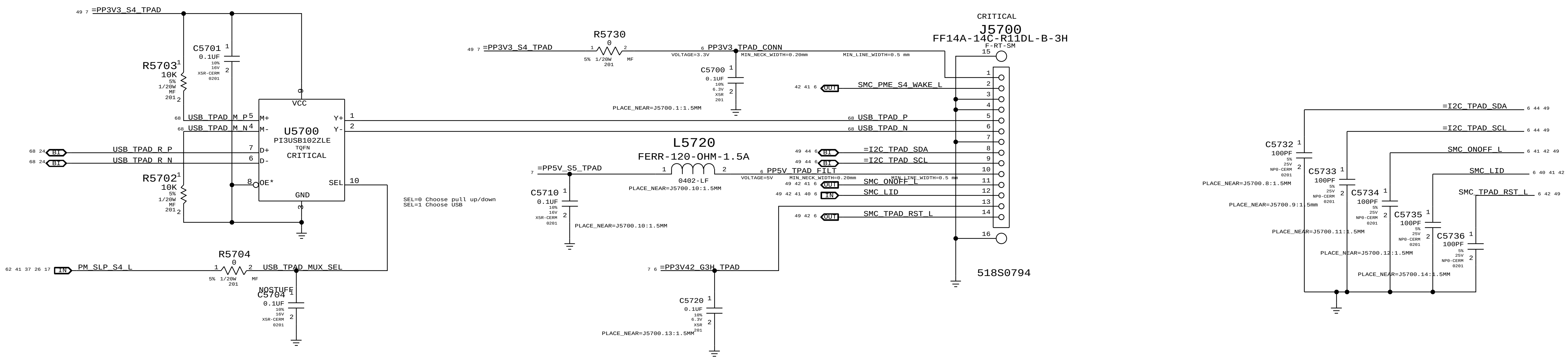
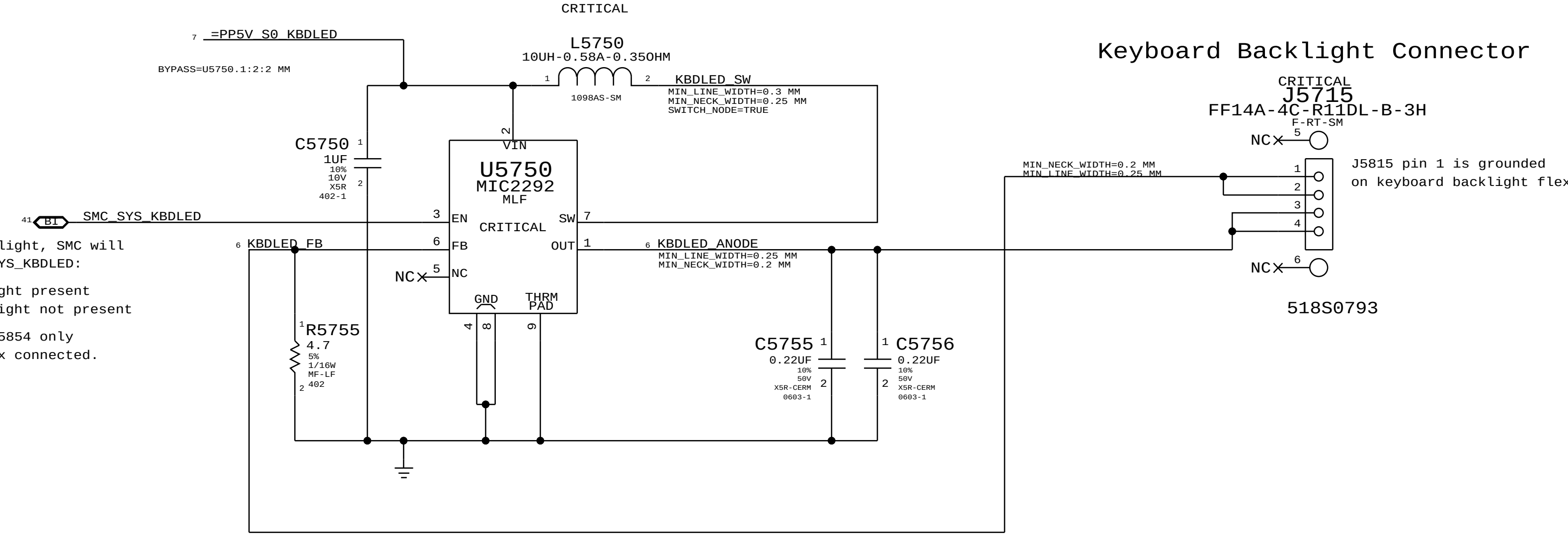
SHEET 48 OF 73





To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE: IPD / KBD Backlight

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

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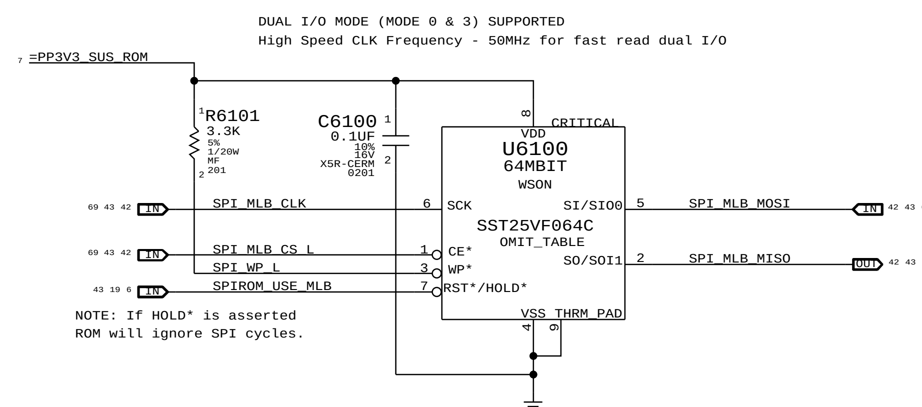
SHEET: 49 OF 73



SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

SPI ROM

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NOTICE OF PROPRIETARY PROPERTY:

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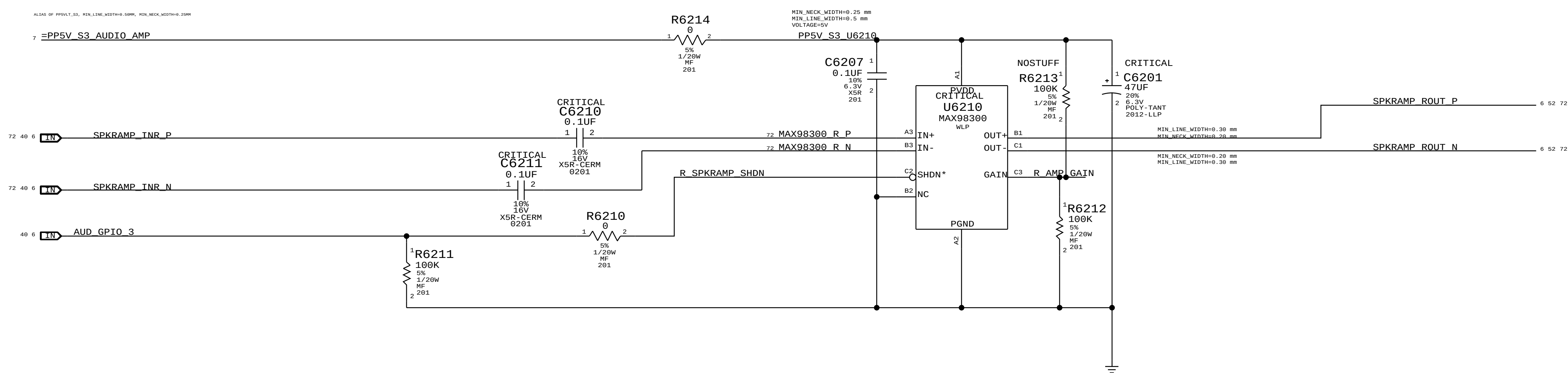
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



SYNC_MASTER=J11_MLB SYNC_DATE=09/30/2011

PAGE TITLE

AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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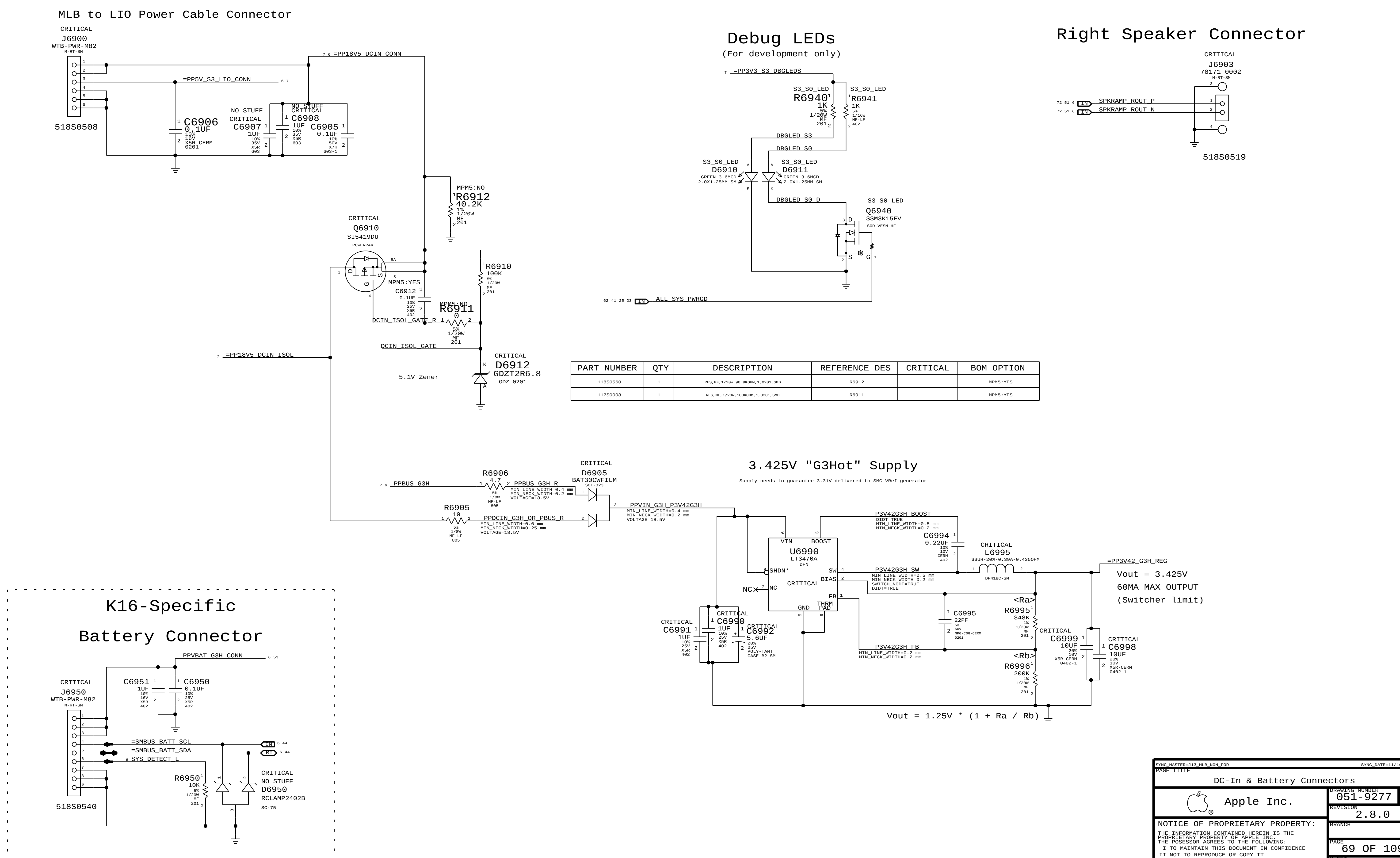

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0560	1	RES,MF,1/20W,90.9KOHM,1,0201,SMD	R6912		MPM5:YES
117S0008	1	RES,MF,1/20W,100KOHM,1,0201,SMD	R6911		MPM5:YES

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

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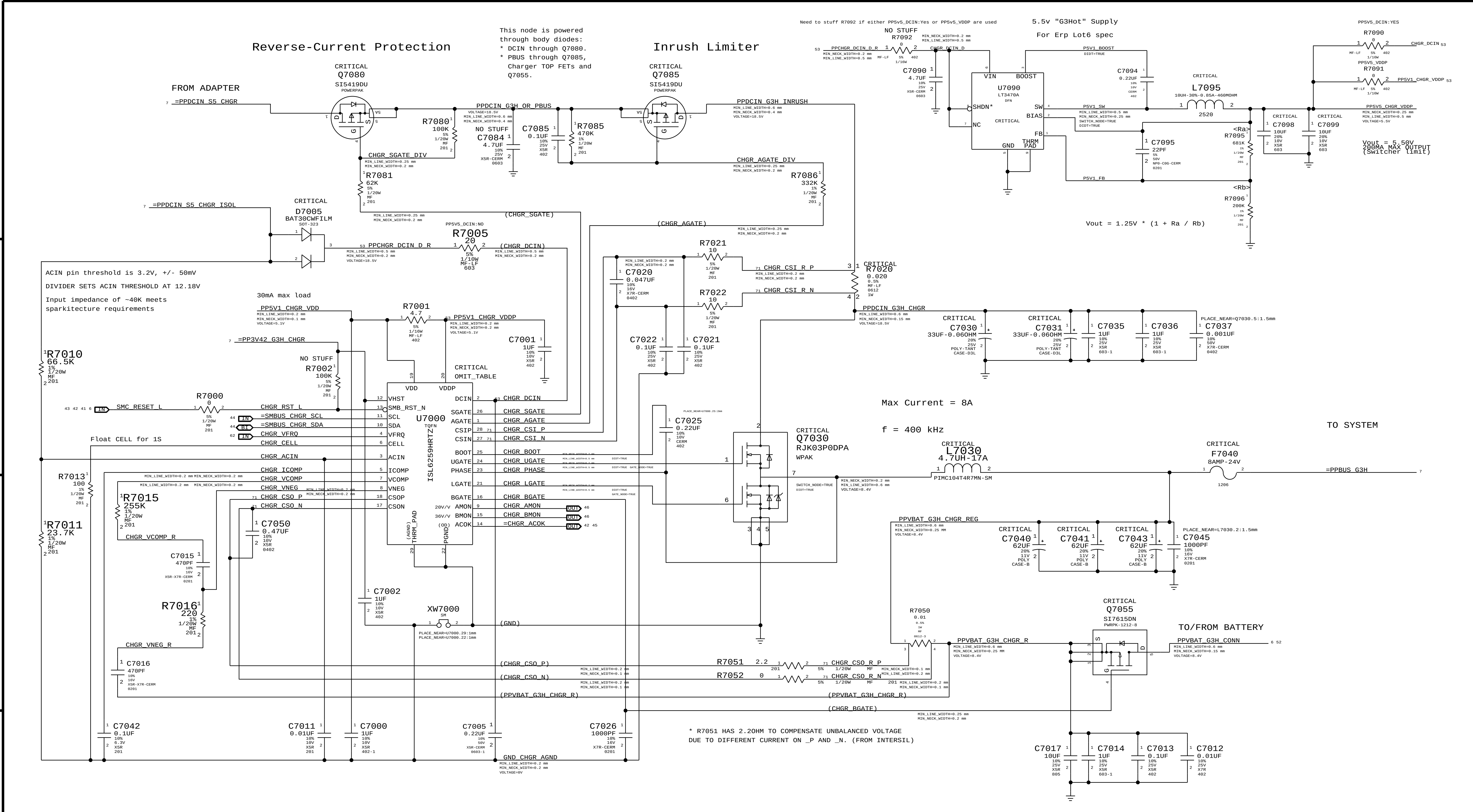

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

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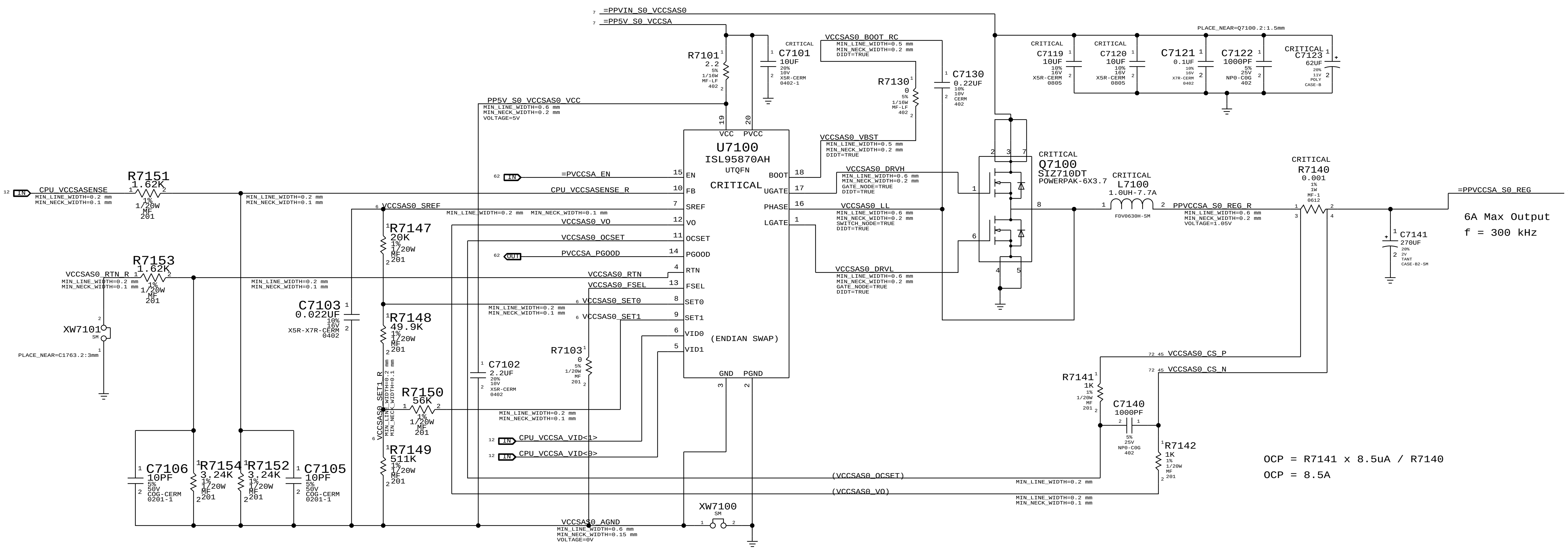

INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2011

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0

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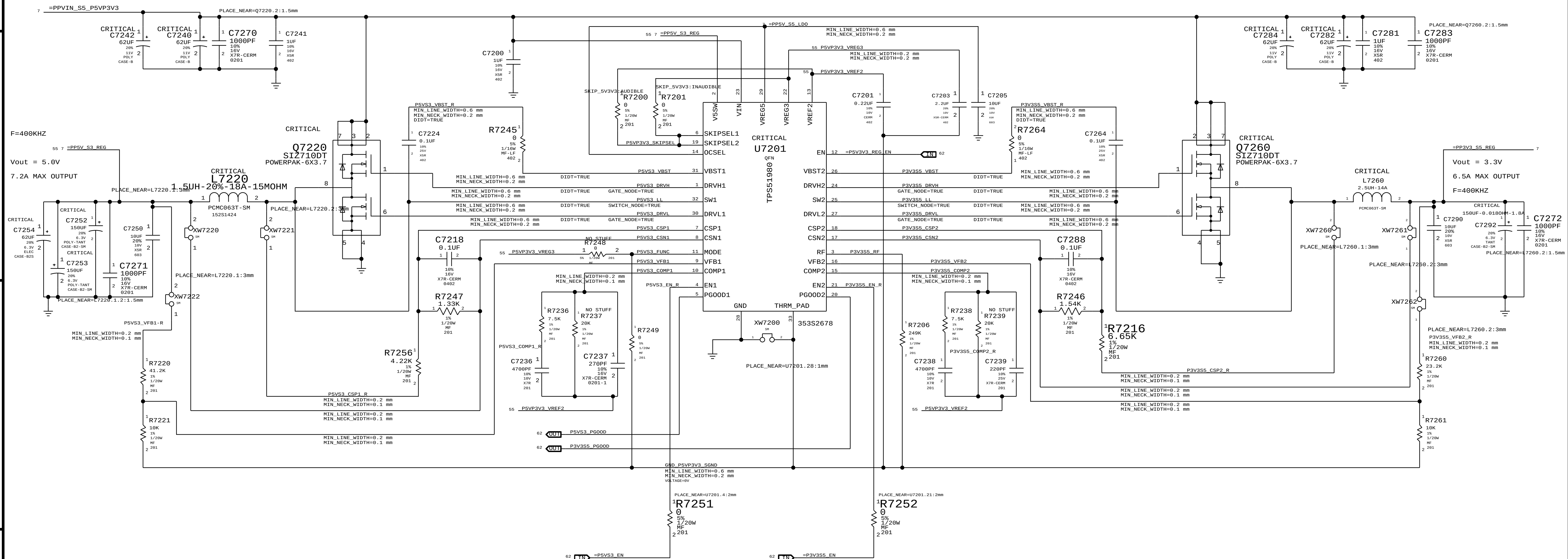

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2011

PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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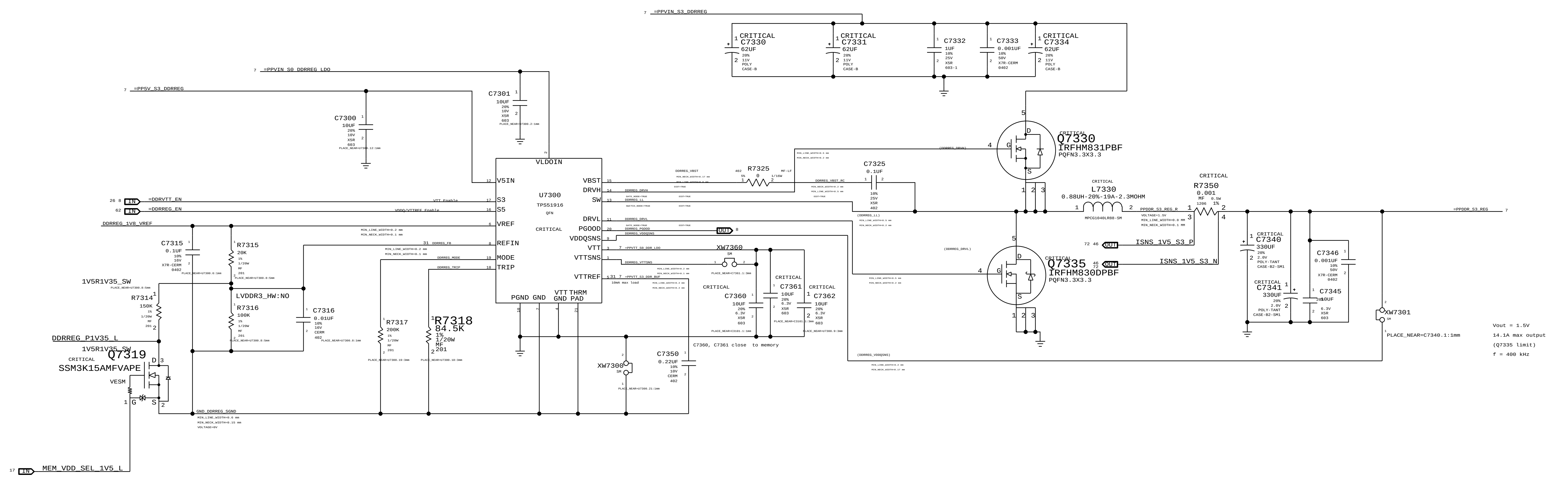
SHEET 55 OF 73



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0460	1	RES,MF,60.4KOHM,1,1/20W,0201	R7316		LVDDR3_HW:YES

If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON

SYNC_MASTER=J11_MLB SYNC_DATE=12/02/2011

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

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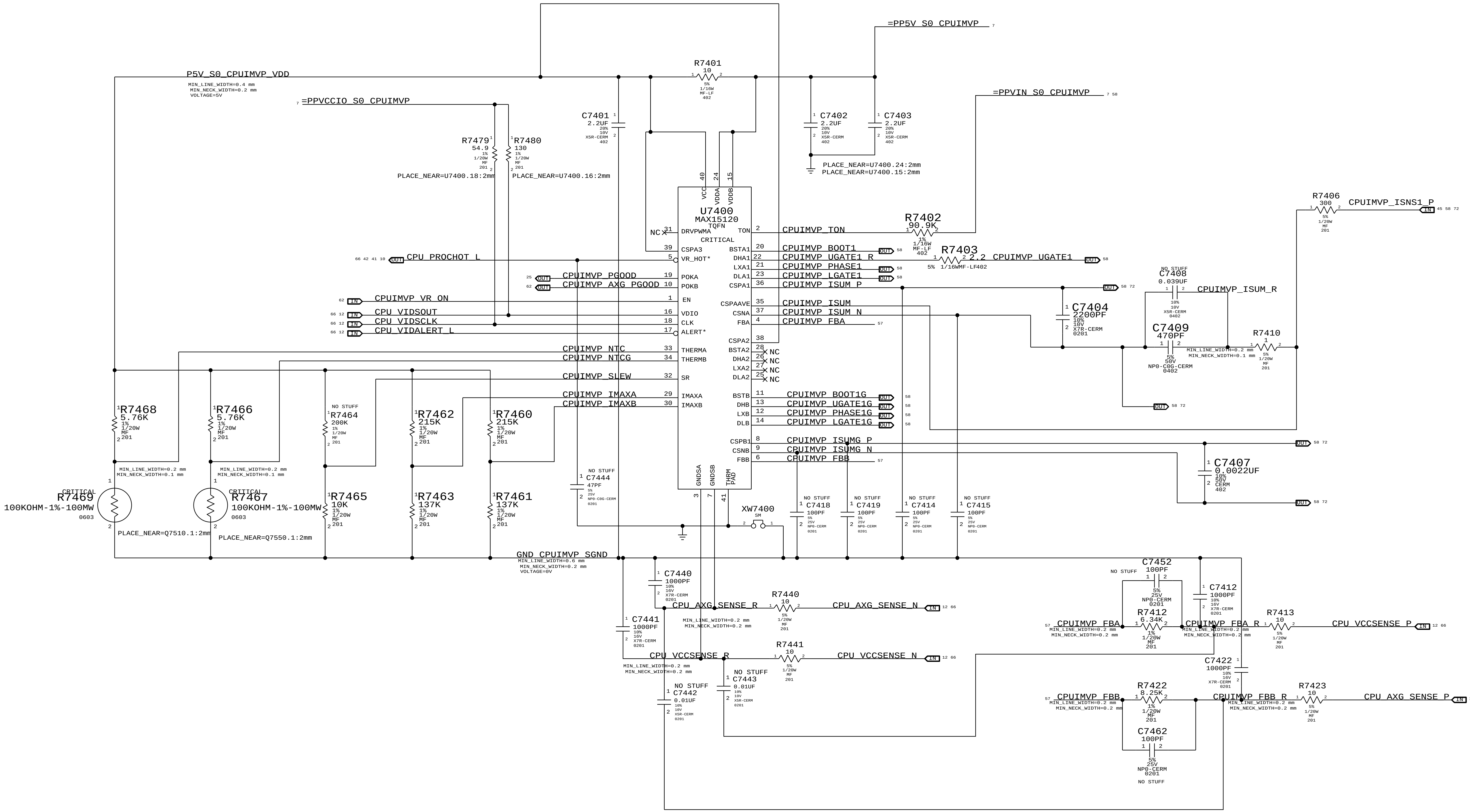

SYNC_MASTER=J11_MLB SYNC_DATE=10/14/2011

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

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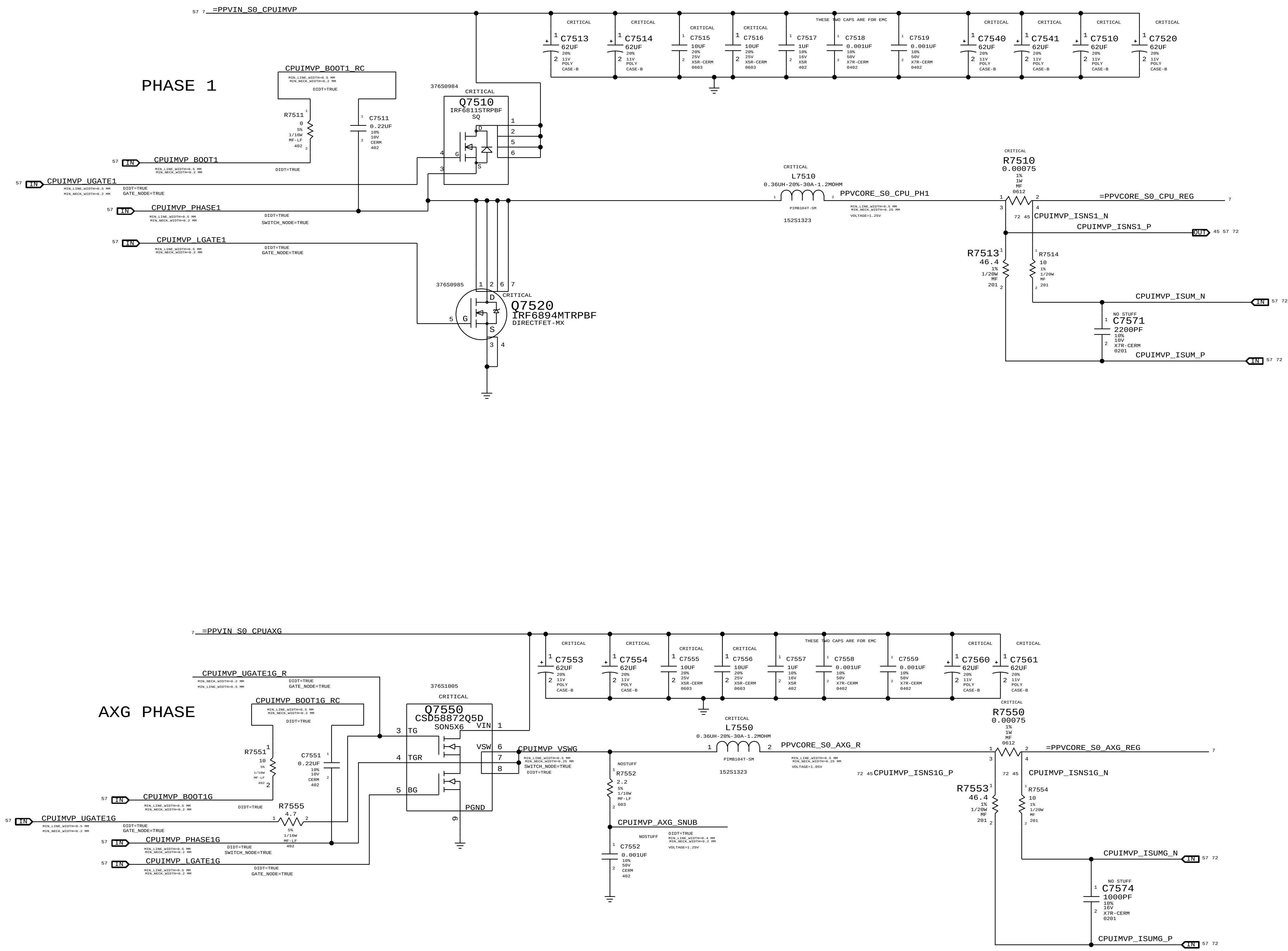
CPU=IV Bridge ULV, AXG=GT2



PAGE TITLE

CPU IMVP7 & AXG VCore Output

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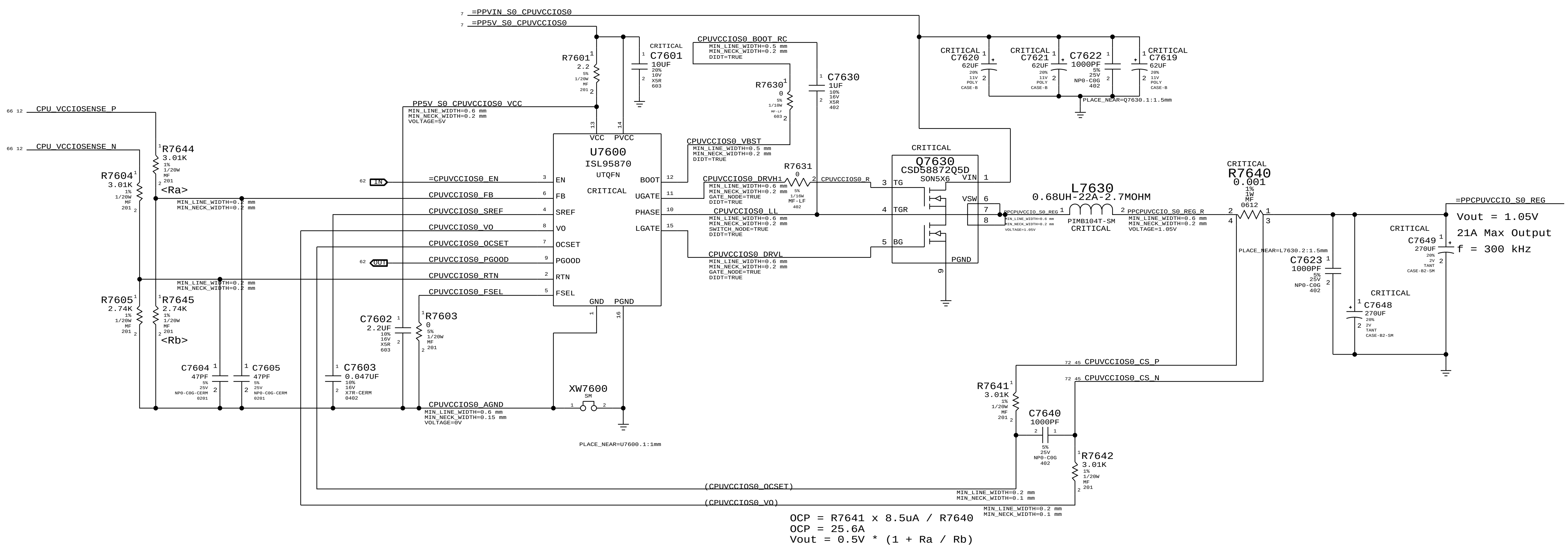
CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=10/17/2011

PAGE TITLE: CPU VCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

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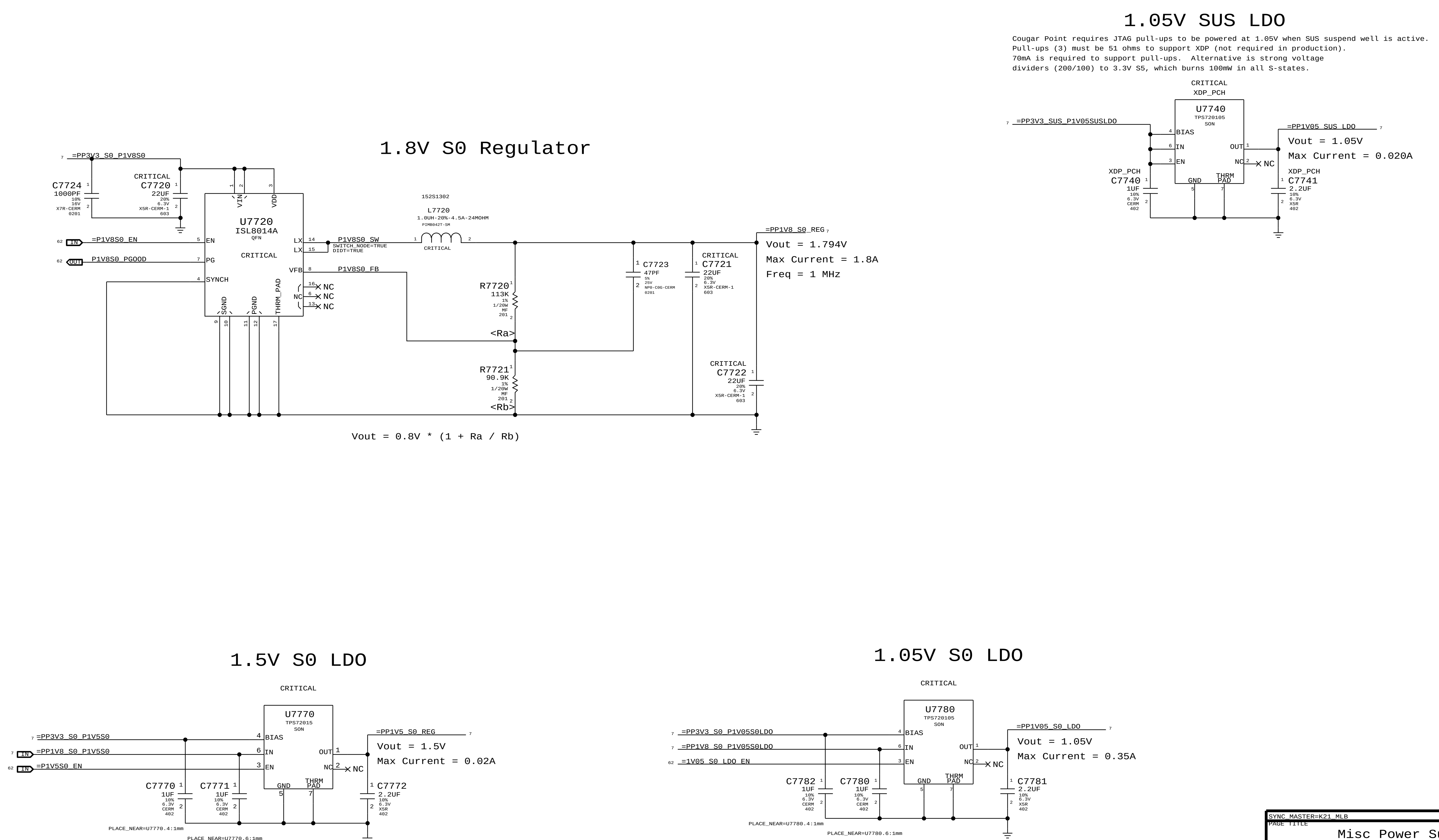

SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

Misc Power Supplies

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

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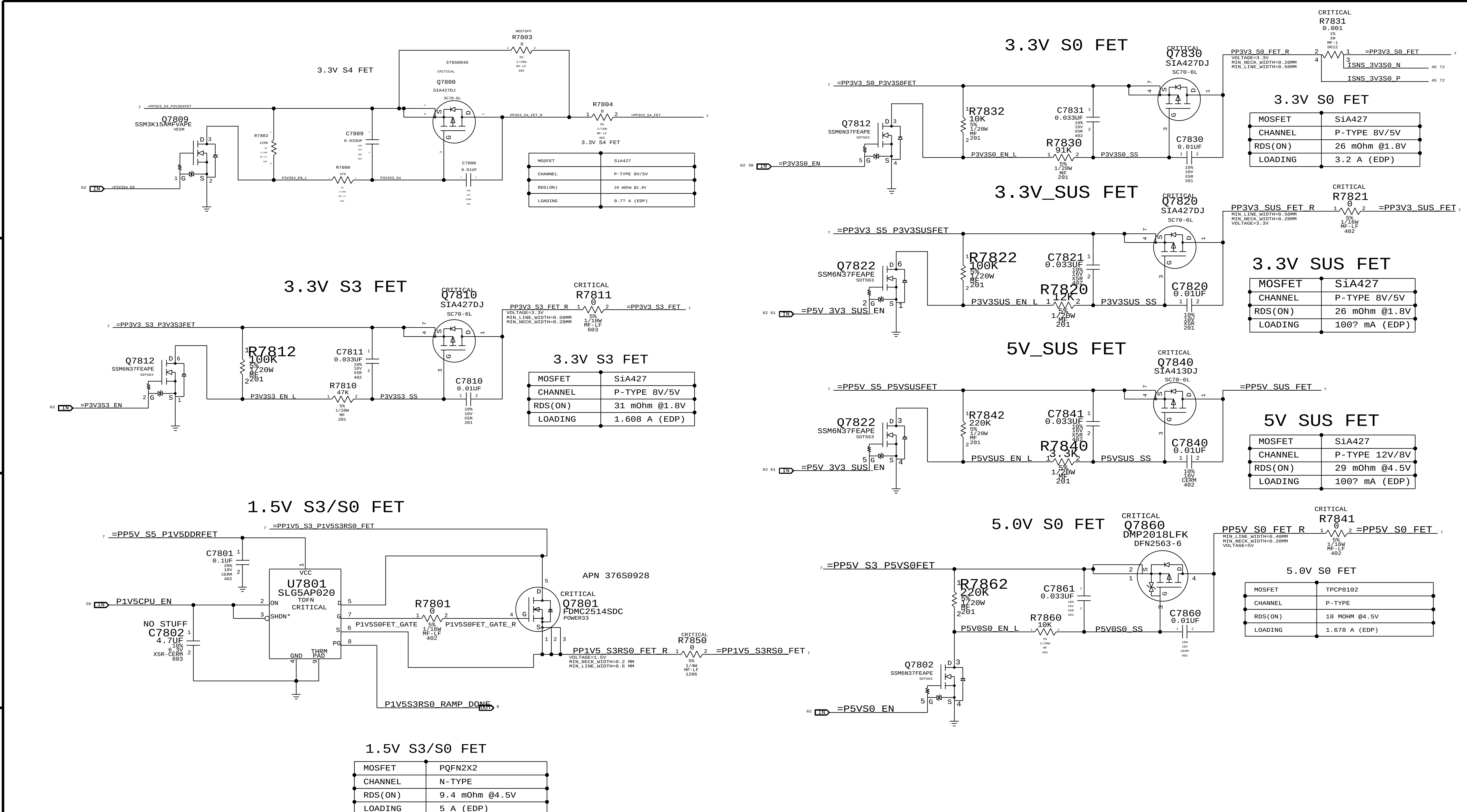

3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.7? A (EDP)

3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

1.5V S3/S0 FET

MOSFET	PQFN2X2
CHANNEL	N-TYPE
RDS(ON)	9.4 mOhm @4.5V
LOADING	5 A (EDP)

3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 mOhm @4.5V
LOADING	100? mA (EDP)

5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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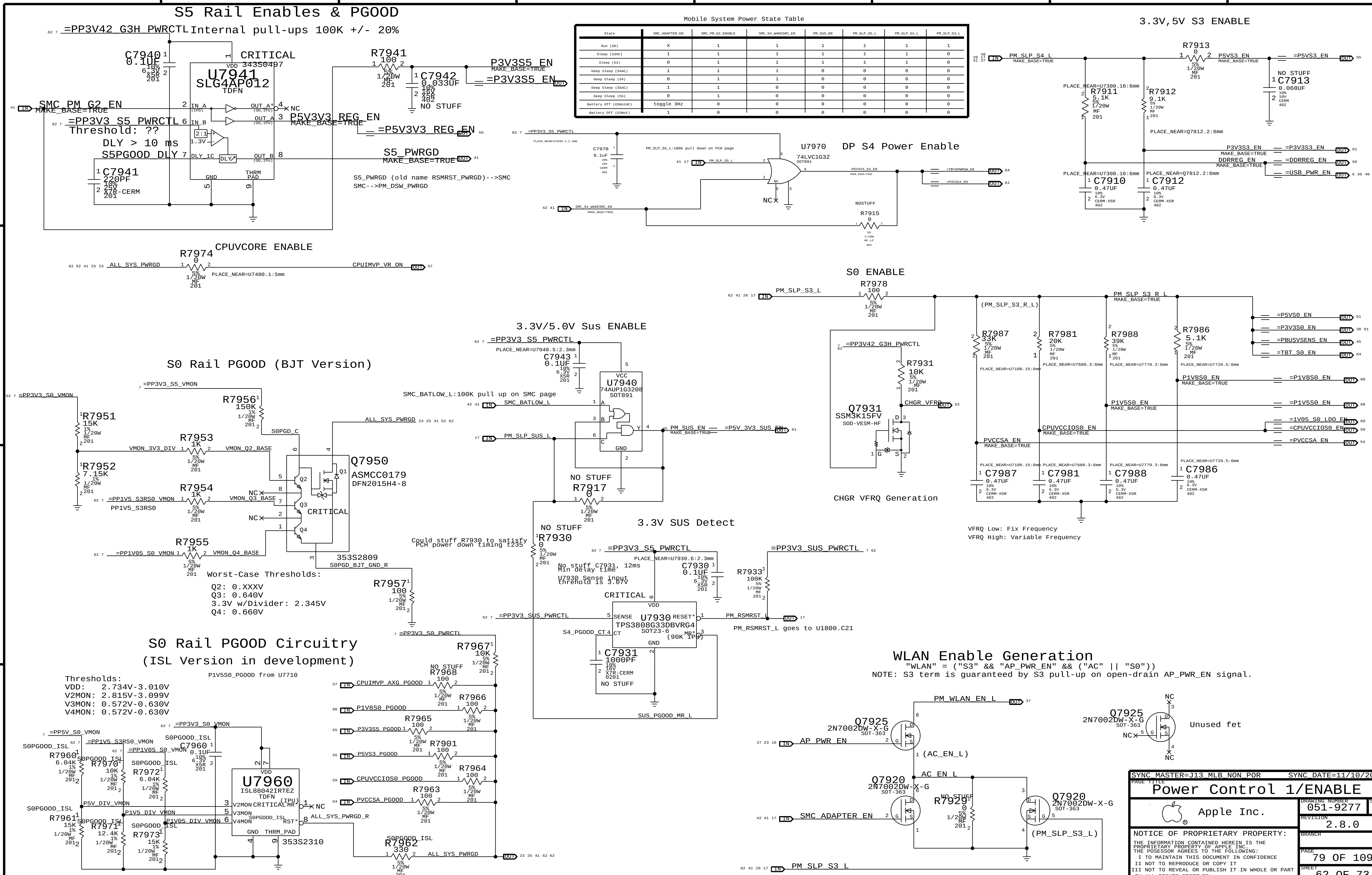

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

SYNC_MASTER=J13_MLB_NON_POR SYNC_DATE=11/10/2011

PAGE TITLE
Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D
REVISION 2.8.0
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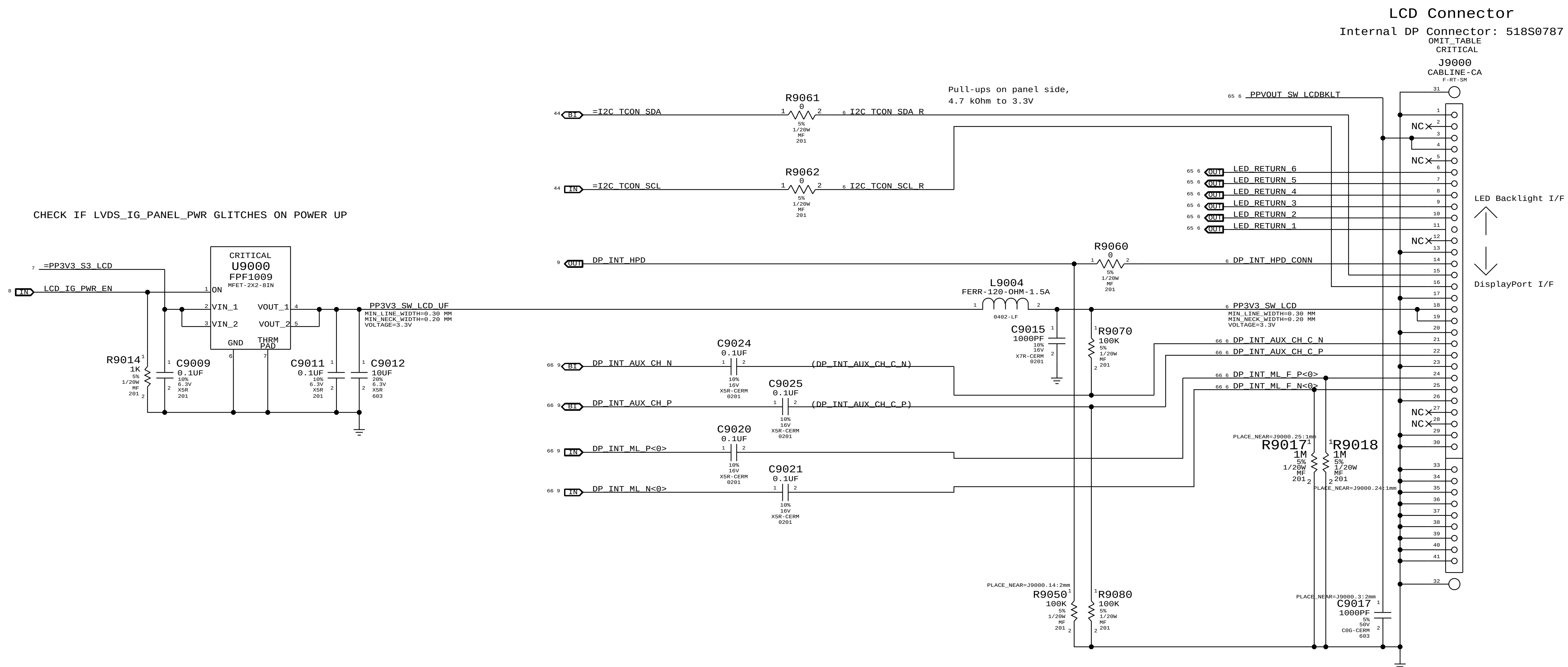
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
518S0829	1	CONNTWIN-AX,P=0.4,30P,W-BOSS,HF	J9000		



SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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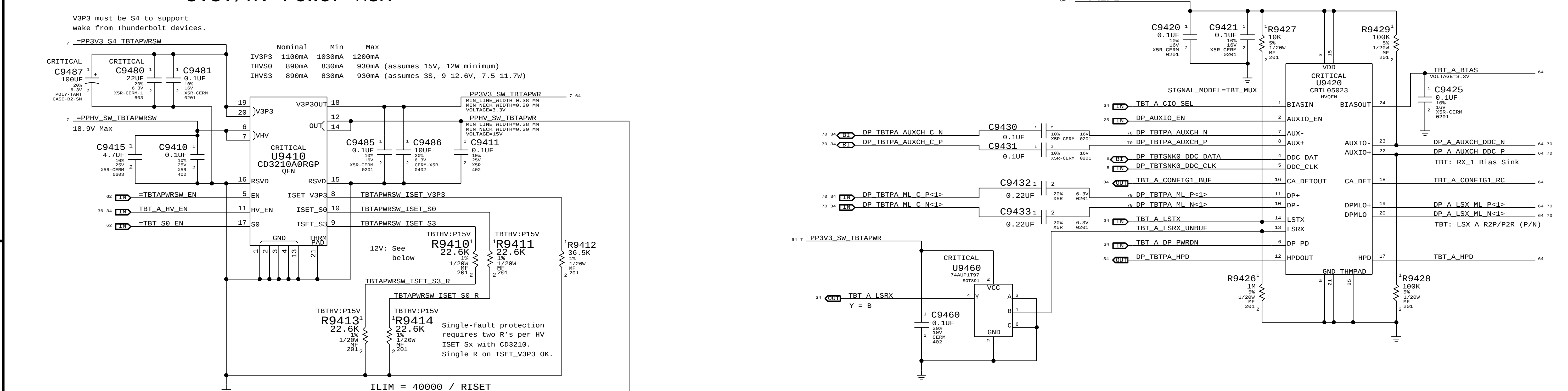
3.3V/HV Power MUX

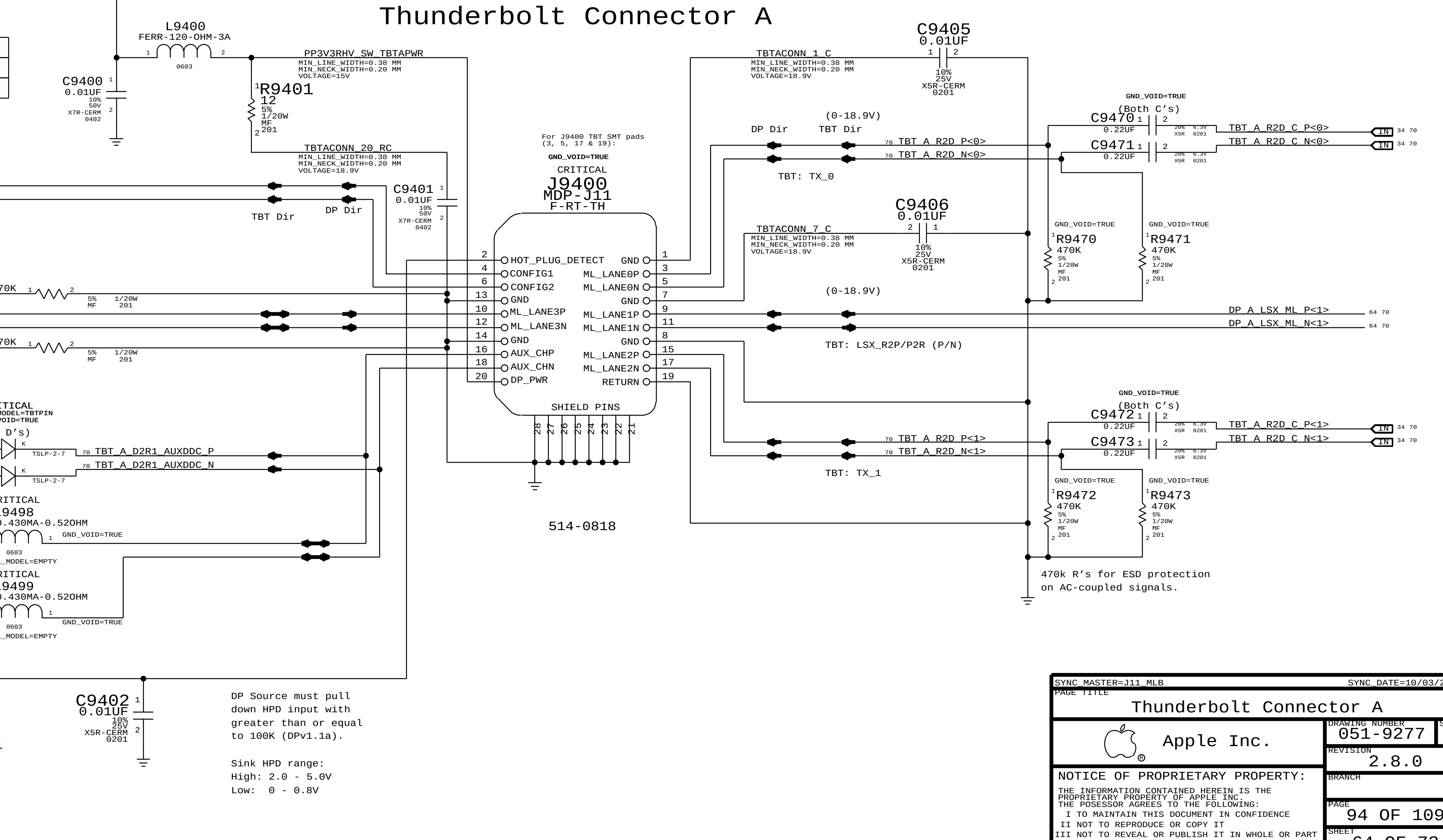


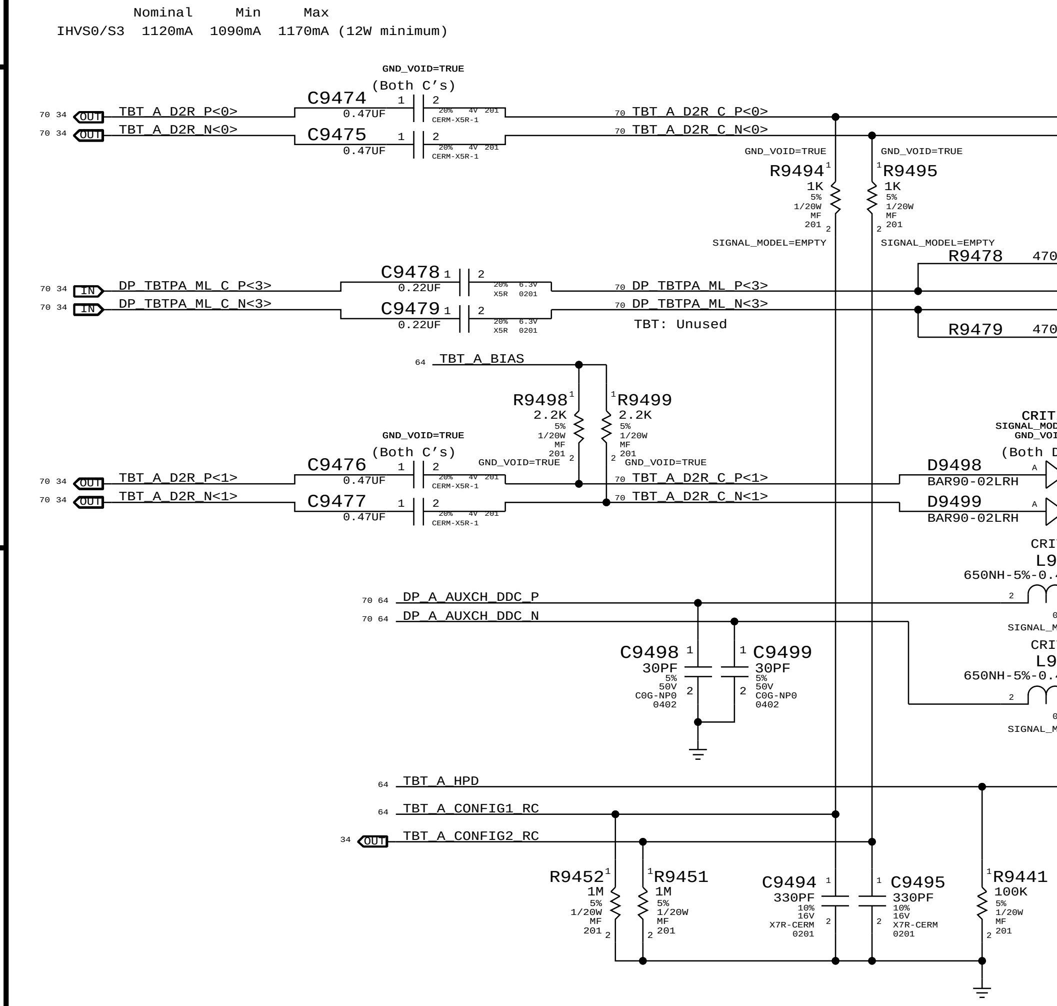
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MF,1/20W,17.8K,1,0201	R9411,R9414		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

Thunderbolt Connector A





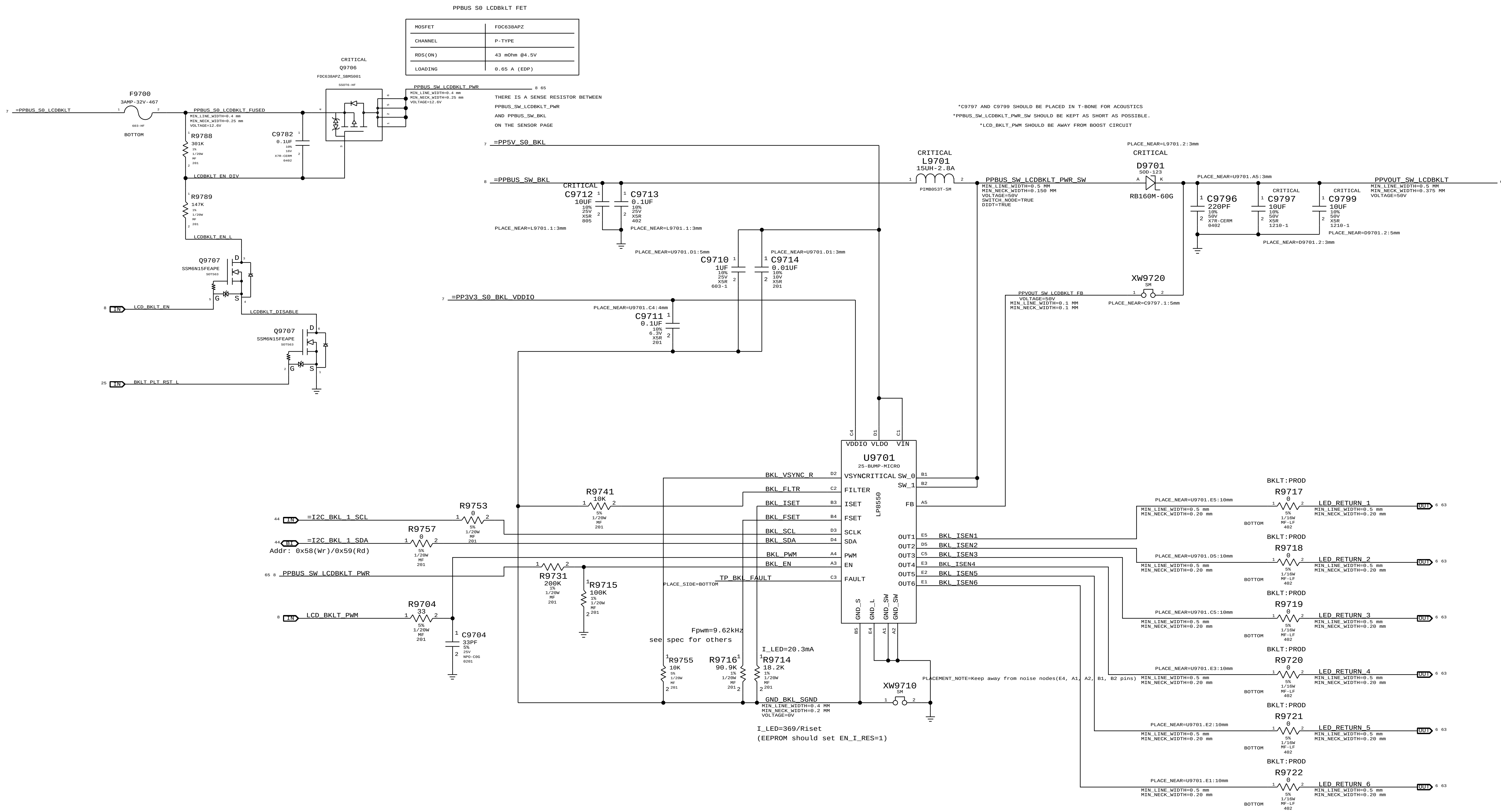
SYNC_MASTER=J11_MLB SYNC_DATE=10/03/2011

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-9277 SIZE: D

REVISION: 2.8.0



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=K21_MLB SYNC_DATE=07/28/2011

PAGE TITLE

LCD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

BRANCH

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

Note: CPU_8MIL and CPU_ITP can be converted
back to TABLE_SPACING_RULE
once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING			
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_P<3:0>	9 17	DMI/FDI
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_N<3:0>	9 17	
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_P<3:0>	9 17	
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_N<3:0>	9 17	
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_P<7:0>	9 17	
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_N<7:0>	9 17	
	CPU_45S	CPU_AGTL	FDI_FSYNC<1..0>	9 17	
	CPU_45S	CPU_AGTL	FDI_LSYNC<1..0>	9 17	
	CPU_45S	CPU_AGTL	FDI_INT	9 17	
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	10 19 42	
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	10 17	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	10 17 26	
	CPU_45S	CPU_ITP	XDP_DBRESET_L	10 23 25	
	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	10 23	
	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	10 23	
	CPU_27P4S	CPU_COMP	EDP_COMP	9	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10	
	CPU_45S	CPU_ITP	CPU_CFG<11..0>	9 23	
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	10 41	
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	12	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	10 41 42 57	
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	10 19 23	
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	10 19 42	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	8 10	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	8 10	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	10 16	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	10 16	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	16 23	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	16 23	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	23	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	23	
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	10 23	
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	10 23	
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	10 23	
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	10 23	
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPU_TRST_L	10 23	
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	10 23	
XDP_BPM_L_R_CFG	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	10 23	
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>	23	
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	CPU_CFG<15..12>	9 23	
(FSB_CPURST_L)	CPU_45S	CPU_ITP	XDP_CPURST_L	23	
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	12 57	
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	12 57	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 59	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 59	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 57	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 57	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	12 57	
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	12 57	
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	12 57	
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<0>	8 38	PCIe SSD
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<0>	8 38	
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_P	38	
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_N	38	
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<0>	8 38	
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<0>	8 38	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_P	38	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_N	38	
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_P<1>	8 38	
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_N<1>	8 38	
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<1>	6 38	
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<1>	6 38	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<1>	6 8 38	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<1>	6 8 38	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<1>		
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<1>		
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	6 16 38	
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	6 16 38	
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	9 63	DP
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	9 63	
	DP_80D	DP_TX	DP_INT_ML_F_P<3..0>	6 63	
	DP_80D	DP_TX	DP_INT_ML_F_N<3..0>	6 63	
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	6 63	
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	6 63	
	DP_80D	DP_AUX	DP_INT_AUX_CH_P	9 63	
	DP_80D	DP_AUX	DP_INT_AUX_CH_N	9 63	

Note: DisplayPort tables are on Page 103

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	PalPilot Spacing	"Real" Spacing
MEM_DATA2SELF	*	=2x_DIELECTRIC	?	=2x_DIELECTRIC	=2x_DIELECTRIC
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?	=5.7x_DIELECTRIC	=3x_DIELECTRIC
MEM_CMD2CMD	*	=3x_DIELECTRIC	?	=4x_DIELECTRIC	=3x_DIELECTRIC
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?	=4x_DIELECTRIC	=3x_DIELECTRIC
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?	=4x_DIELECTRIC	=3x_DIELECTRIC
MEM_CLK2CLK	*	=6x_DIELECTRIC	?	=8.6x_DIELECTRIC	=6x_DIELECTRIC
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?	=5.7x_DIELECTRIC	=4x_DIELECTRIC
MEM_2PWR	*	=PWR_P2MM	?	=PWR_P2MM	=PWR_P2MM
MEM_2GND	*	=GND_P2MM	?	=GND_P2MM	=GND_P2MM
MEM_2OTHER	*	=6x_DIELECTRIC	?	=8.6x_DIELECTRIC	=6x_DIELECTRIC

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_CKE<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_CS_L<3..0>	11 27 28 32
MEM_A_CTRL	MEM_45S	MEM_CTRL	MEM_A_ODT<3..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_A<15..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_RAS_L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_CAS_L	11 27 28 32
MEM_A_CMD	MEM_45S	MEM_CMD	MEM_A_WE_L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_P<0>	11 27
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_N<0>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_P<1>	11 27
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_N<1>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_P<2>	11 27
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_N<2>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_P<3>	11 27
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_N<3>	11 27
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_CKE<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_CS_L<3..0>	11 29 30 32
MEM_B_CTRL	MEM_45S	MEM_CTRL	MEM_B_ODT<3..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_A<15..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_RAS_L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_CAS_L	11 29 30 32
MEM_B_CMD	MEM_45S	MEM_CMD	MEM_B_WE_L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56>	11 30
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_P<0>	11 29
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_N<0>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_P<1>	11 29
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_N<1>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_P<2>	11 29
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_N<2>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_P<3>	11 29
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_N<3>	11 29
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_P<4>	11 30
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_N<4>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_P<5>	11 30
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_N<5>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_P<6>	11 30
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_N<6>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_P<7>	11 30
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_N<7>	11 30
		MEM_PWR	PP1V5_S3RS0	6 7
		MEM_PWR	PP1V5_S3	6 7
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	27 28 31
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	27 28 31

SYNC_MASTER=J13_CONSTRAINTS SYNC_DATE=01/11/2012

PAGE TITLE: Memory Constraints

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REVISION: 2.8.0

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	SATA3_PCH_TX	*	SATA3_TX2TX
SATA3_PCH_RX	SATA3_PCH_RX	*	SATA3_RX2RX
SATA3_PCH_TX	*_PCH_TX	*	SATA3_TX2OTHERTX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_RX2OTHERRX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_TX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_RX2TX
SATA3_PCH_TX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_TX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_RX	*_RX	*	SATA3_2OTHERHS
SATA3_PCH_TX	*	*	SATA3_2OTHER
SATA3_PCH_RX	*	*	SATA3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
SATA3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_TX2TX	*	=2.5x_DIELECTRIC	?
SATA3_RX2RX	*	=2.5x_DIELECTRIC	?
SATA3_TX2OTHERTX	*	=4x_DIELECTRIC	?
SATA3_RX2OTHERRX	*	=4x_DIELECTRIC	?
SATA3_TX2RX	*	=6x_DIELECTRIC	?
SATA3_RX2TX	*	=6x_DIELECTRIC	?
SATA3_2OTHERHS	*	=4x_DIELECTRIC	?
SATA3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES	
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_P	16 38	SATA SSD
SATA_PCH_MUX_R2D	SATA_80D	SATA3_PCH_TX	SATA_HDD_R2D_C_N	16 38	
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_P	38	
	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_MUX_IN_N	38	
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_P	6 38	
SATA_MUX_SSD_R2D	SATA_80D	SATA3_PCH_TX	SATA_SSD_R2D_N	6 38	
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_P	16 38	
SATA_PCH_MUX_D2R	SATA_80D	SATA3_PCH_RX	SATA_HDD_D2R_N	16 38	
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_P	38	
	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_MUX_OUT_N	38	
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_P	6 38	
SATA_MUX_SSD_D2R	SATA_80D	SATA3_PCH_RX	SATA_SSD_D2R_N	6 38	
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	18 24	USB Hub nets
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	18 24	
USB_BT	USB_80D	USB	USB_BT_P	24 37	
USB_BT	USB_80D	USB	USB_BT_N	24 37	
	USB_80D	USB	USB_BT_CONN_P	6 37	
	USB_80D	USB	USB_BT_CONN_N	6 37	
	USB_80D	USB	USB_BT_WAKE_P	37	
	USB_80D	USB	USB_BT_WAKE_N	37	
USB_TPAD	USB_80D	USB	USB_TPAD_P	49	
USB_TPAD	USB_80D	USB	USB_TPAD_N	49	
	USB_80D	USB	USB_TPAD_CONN_P	6	
	USB_80D	USB	USB_TPAD_CONN_N	6	
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_P	24	
USB_TPAD_HUB	USB_80D	USB	USB_TPAD_HUB_N	24	
	USB_80D	USB	USB_TPAD_R_P	24 49	
	USB_80D	USB	USB_TPAD_R_N	24 49	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	49	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	49	
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	24 33	
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	24 33	
USB_SMC	USB_80D	USB	USB_SMC_P	24 41	
USB_SMC	USB_80D	USB	USB_SMC_N	24 41	
USB_CAMERA	USB_80D	USB	USB_CAMERA_P	6 18 40	USB Camera nets
USB_CAMERA	USB_80D	USB	USB_CAMERA_N	6 18 40	
USB_EXTA	USB_80D	USB	USB_EXTA_P	18 39	USB EXTA nets (Right USB port)
USB_EXTA	USB_80D	USB	USB_EXTA_N	18 39	
	UART_45S	UART	SMC_DEBUGPRT_TX_L	39 41 42	
	UART_45S	UART	SMC_DEBUGPRT_RX_L	39 41 42	
	USB_80D	USB	USB2_EXTA_MUXED_P	39	
	USB_80D	USB	USB2_EXTA_MUXED_N	39	
	USB_80D	USB	USB2_EXTA_MUXED_F_P	39	
	USB_80D	USB	USB2_EXTA_MUXED_F_N	39	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_P	18 39	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_N	18 39	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_P	18 39	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_N	18 39	
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_P	39	
	USB_80D	USB3_PCH_RX	USB3_EXTA_RX_F_N	39	
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_P	39	
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_F_N	39	
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_P	39	
	USB_80D	USB3_PCH_TX	USB3_EXTA_TX_C_N	39	
USB_EXTB	USB_80D	USB	USB_EXTB_P	6 24 40	USB EXTB nets (Left USB port)
USB_EXTB	USB_80D	USB	USB_EXTB_N	6 24 40	
	USB_80D	USB	USB_EXTB_EHCI_P	18 24	
	USB_80D	USB	USB_EXTB_EHCI_N	18 24	
	USB_80D	USB	USB_EXTB_XHCI_P	18 24	
	USB_80D	USB	USB_EXTB_XHCI_N	18 24	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_P	18 40	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_N	18 40	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_P	6 40	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_RC_N	6 40	
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_P		
	USB_80D	USB3_PCH_RX	USB3_EXTB_RX_CONN_N		
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_P	18 40	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_N	18 40	
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_P	6 40	
	USB_80D	USB3_PCH_TX	USB3_EXTB_TX_C_N	6 40	
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_P	18 24	Unused USB nets
(USB_TPAD_HUB)	USB_80D	USB	USB_EXTD_XHCI_N	18 24	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	16	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	16	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	16	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	16	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	16	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	16	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16	

SYNC_MASTER=J13_CONSTRAINTS SYNC_DATE=01/11/2012

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DRAWING NUMBER 051-9277 SIZE D

REVISION 2.8.0

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	6 16 41 43
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	6 16 41 43
	LPC_45S	LPC	LPCPLUS_RESET_L	6 25 43
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	25 41
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 25 43
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	18 25
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIIN	16 25
	CLK_LPC_45S	CLK_LPC	PCH_CLK33M_PCIOUT	18 25
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	16 44
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	16 44
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	16 44
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	16 44
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SML_PCH_1_CLK	16 44
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SML_PCH_1_DATA	16 44
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	6 16 40
	HDA_45S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	6 16 40
	HDA_45S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	16
	HDA_45S	HDA	HDA_RST_L	6 16 40
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	6 16 40
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	6 16 40
	HDA_45S	HDA	HDA_SDOUT_R	16 25
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	17 42
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	41 42
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	16 43
	SPI_45S	SPI	SPI_CLK	43
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	16 43
	SPI_45S	SPI	SPI_MOSI	43
SPI_MISO	SPI_45S	SPI	SPI_MISO	16 43
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	16 43
	SPI_45S	SPI	SPI_CS0_L	43
	SPI_45S	SPI	SPI_SMC_CLK	41 42
	SPI_45S	SPI	SPI_SMC_MOSI	41 42
	SPI_45S	SPI	SPI_SMC_MISO	41 42
	SPI_45S	SPI	SPI_SMC_CS_L	41 42
	SPI_45S	SPI	SPI_MLB_CLK	42 43 50
	SPI_45S	SPI	SPI_MLB_MOSI	42 43 50
	SPI_45S	SPI	SPI_MLB_MISO	42 43 50
	SPI_45S	SPI	SPI_MLB_CS_L	42 43 50
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	6 37
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	6 37
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	16 37
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	16 37
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	6 16 37
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	6 16 37
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	6 16 37
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	6 16 37
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	34
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	34
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	8 34
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	8 34
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	8 34
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	8 34
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	34
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	34
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	16 34
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	16 34
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	8 16
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	8 16
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	16 23
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	16 23
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	16 23
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	16 23

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	34
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	8 34
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	8 34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	34
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	8 34
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	8 34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	34
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	34
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	8 34
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	8 34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	34
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	34
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	8 34
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	8 34

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	16 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	16
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	25 34
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	34
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	25

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	34 64
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	34 64
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0>	64
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0>	64
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1>	34 64
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1>	34 64
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3>	34 64
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3>	34 64
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2>	64
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2>	64
	DP_80D	DP_TX	DP_A_LSX_ML_P<1>	64
	DP_80D	DP_TX	DP_A_LSX_ML_N<1>	64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0>	64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0>	64
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1>	34 64
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1>	34 64
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0>	34 64
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0>	34 64
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P	34 64
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N	34 64
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P	64
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N	64
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P	64
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N	64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	64
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	64
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	8 34
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	8 34
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>	
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>	
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_P<3..1:2>	8 34
DP_TBTPB_ML	DP_80D	DP_TX	DP_TBTPB_ML_C_N<3..1:2>	8 34
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>	
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>	
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>	
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>	
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0>	8 34
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0>	8 34
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_P	8 34
TBT_B_AUXCH	DP_80D	DP_AUX	DP_TBTPB_AUXCH_C_N	8 34
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P	
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	34
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	34
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	34
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	34

Only used on hosts supporting Thunderbolt video-in

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	41 44
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	41 44
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	41 44
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	41 44
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL	41 44
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA	41 44
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	41 44
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	41 44
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	41 44
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	41 44

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_P	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSI_N	53
	1:1_DIFFPAIR		CHGR_CSI_R_P	53
	1:1_DIFFPAIR		CHGR_CSI_R_N	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_P	53
SENSE_DIFFPAIR	1:1_DIFFPAIR		CHGR_CSO_N	53
	1:1_DIFFPAIR		CHGR_CSO_R_P	53
	1:1_DIFFPAIR		CHGR_CSO_R_N	53

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1:1_DIFFPAIR	0.200 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	46 47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	46 47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P	47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_N	47
	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	47
	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	47
	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	47
	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_P	9 47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPU_THERMD_N	9 47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	47
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	45 59
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	45 59
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_P	45 57 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1_N	45 58
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_P	45
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUM_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_P	45 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISNS1G_N	45 58
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_P	45
	SENSE_1TO1_45S	SENSE	CPUIMVP_ISUMG_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_P	45 54
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	VCCSAS0_CS_N	45 54
	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_P	45
	SENSE_1TO1_45S	SENSE	VCCSAISNS_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_P	45 61
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_N	45 61
	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_P	45
	SENSE_1TO1_45S	SENSE	ISNS_3V3S0_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_P	57 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUMG_N	57 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_P	57 58
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUIMVP_ISUM_N	57 58
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	8 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	8 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_N	46 56
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_P	46 56
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	37 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	37 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	38 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	38 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	8 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	8 46
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 40 51
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 40 51
	1:1_DIFFPAIR	AUDIO	MAX98300_R_P	51
	1:1_DIFFPAIR	AUDIO	MAX98300_R_N	51
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	6 51 52
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	6 51 52
		SB_POWER	PP3V3_S5	6 7
		SB_POWER	PP3V3_S0	6 7
		GND	GND	

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Project Specific Constraints

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J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

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PCB Rule Definitions

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