1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2011-04-08

K78 MLB SCHEMATIC

04/08/11

Page	(.csa)	Contents	Sync	Date
1	1	Table of Contents	MASTER	MASTER
2	2	System Block Diagram	K6_MLB	12/11/2009
3	3	Power Block Diagram		19/01/2011
4	4	K78 BOM Variants	K21_MLB	11/16/2010
5	5	BOM Configuration	K21_MLB	11/16/2010
6	7	Functional Test / No Test	(K99_MLB)	(02/16/2010)
7	8	Power Aliases	K91_MLB	05/15/2010
8	9	Signal Aliases	K91_MLB	05/15/2010
9	10	CPU DMI/PEG/FDI/RSVD	K21_MLB	12/13/2010
10	11	CPU CLOCK/MISC/JTAG	K21_MLB	12/13/2010
11	12	CPU DDR3 INTERFACES	K21_MLB	12/13/2010
12	13	CPU POWER	K21_MLB	12/13/2010
13	14	CPU GROUNDS	K21_MLB	12/13/2010
14	16	CPU DECOUPLING-I	K21_MLB	12/13/2010
15	17	CPU DECOUPLING-II	K21_MLB	12/13/2010
16	18	PCH SATA/PCIE/CLK/LPC/SPI	K21_MLB	12/13/2010
17	19	PCH DMI/FDI/GRAPHICS	K21_MLB	12/13/2010
18	20	PCH PCI/FLASHCACHE/USB	K21_MLB	12/13/2010
19	21	PCH MISC	K21_MLB	12/13/2010
20	22	PCH POWER	K21_MLB	12/13/2010
21	23	PCH GROUNDS	K21_MLB	12/13/2010
22	24	PCH DECOUPLING	K21_MLB	12/13/2010
23	25	CPU & PCH XDP	K21_MLB	12/13/2010
24	26	USB HUBS	K21_MLB	12/13/2010
25	27	Clock (CK505) and Chipset Support	K21_MLB	11/30/2010
26	28	CPU Memory S3 Support	K21_MLB	12/13/2010
27	29	DDR3 DRAM CHANNEL A (0-31)	K21_MLB	12/13/2010
28	30	DDR3 DRAM CHANNEL A (32-63)	K21_MLB	12/13/2010
29	31	DDR3 DRAM CHANNEL B (0-31)	K21_MLB	12/13/2010
30	32	DDR3 DRAM CHANNEL B (32-63)	K21_MLB	12/13/2010
31	33	FSB/DDR3/FRAMEBUF Vref Margining	K21_MLB	12/13/2010
32	34	DDR3 DRAM Channel B (32-63)	K21_MLB	12/13/2010
33	36	T29 Host (1 of 2)	K21_MLB	12/13/2010
34	37	T29 Host (2 of 2)	K21_MLB	12/13/2010
35	38	T29 Power Support	K21_MLB	12/13/2010
36	40	X21 WIRELESS CONNECTOR	K21_MLB	12/13/2010
37	45	SATA CONNECTOR	K21_MLB	12/13/2010
38	46	External USB Connectors	K21_MLB	12/13/2010
39	47	LIO CONNECTORS	N/A	N/A
40	49	SMC	K21_MLB	12/13/2010
41	50	SMC Support	K21_MLB	12/13/2010
42	51	LPC+SPI Debug Connector	K21_MLB	12/13/2010
43	52	SMBus Connections	K21_MLB	12/13/2010
44	53	Voltage & Load Side Current Sensing	K21_MLB	12/13/2010
45	54	High Side Current Sensing	K21_MLB	12/13/2010
46	55	Thermal Sensors	K21_MLB	12/13/2010
47	56	Fan	K21_MLB	12/13/2010
48	57	IPD / KBD Backlight	K21_MLB	12/13/2010
49	61	SPI ROM	K21_MLB	12/13/2010
50	62	AUDI0: SPEAKER AMP	K21_MLB	12/13/2010
51	69	DC-In & Battery Connectors	K21_MLB	11/11/2010
52	70	PBus Supply & Battery Charger	K21_MLB	11/30/2010
53	71	System Agent Supply	K21_MLB	12/13/2010
54	72	5V / 3.3V Power Supply	K21_MLB	11/30/2010
55	73	1.5V DDR3 Supply	K21_MLB	12/13/2010
56	74	CPU IMVP7 & AXG VCore Regulator	K21_MLB	12/13/2010
57	75	CPU IMVP7 & AXG VCore Output	K21_MLB	12/13/2010
58	76	CPU VCCIO (1.05V) Power Supply	K21_MLB	12/13/2010
59	77	Misc Power Supplies	K21_MLB	12/13/2010
60	78	Power FETs	K21_MLB	12/13/2010
61	79	Power Control 1/ENABLE	K21_MLB	12/13/2010
62	90	Internal DisplayPort Connector	K21_MLB	12/13/2010
63	93	DisplayPort/T29 A MUXing	K21_MLB	12/13/2010
64	94	DisplayPort/T29 A Connector	K21_MLB	12/13/2010
65	97	LCD Backlight Driver	K21_MLB	12/13/2010
66	100	CPU Constraints	CONSTRAINTS	04/06/2011
67	101	Memory Constraints	CONSTRAINTS	04/06/2011
68	102	PCH Constraints 1	CONSTRAINTS	04/06/2011
69	103	PCH Constraints 2	CONSTRAINTS	04/06/2011
70	104	Ethernet/FW Constraints	CONSTRAINTS	04/06/2011
71	105	T29 Constraints	CONSTRAINTS	04/06/2011
72	106	SMC Constraints	CONSTRAINTS	04/06/2011
73	108	Project Specific Constraints	CONSTRAINTS	04/06/2011
74	109	PCB Rule Definitions	CONSTRAINTS	04/06/2011

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8871	1	SCHEM,MLB,K78	SCH	CRITICAL	
820-3024	1	PCBF,MLB,K78	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Apr 8 10:21:51 2011

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: SCHEM,MLB,K78

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DRAWING NUMBER: 051-8871 SIZE: D
REVISION: 2.5.0
BRANCH:
PAGE: 1 OF 109
SHEET: 1 OF 74

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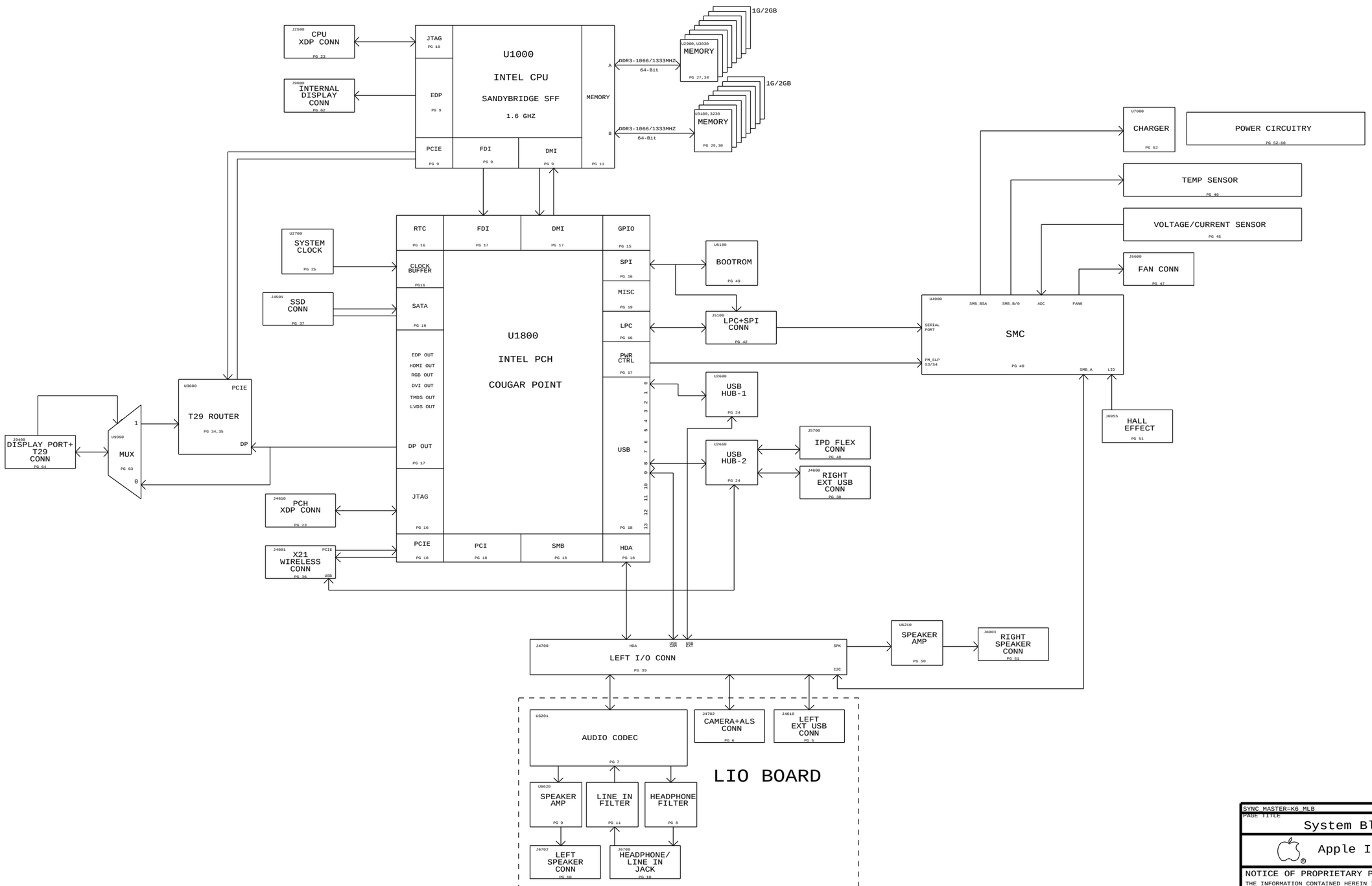

SYNC_MASTER=K6_MLB SYNC_DATE=12/11/2009

PAGE TITLE

System Block Diagram

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PAGE 2 OF 109

SHEET 2 OF 74

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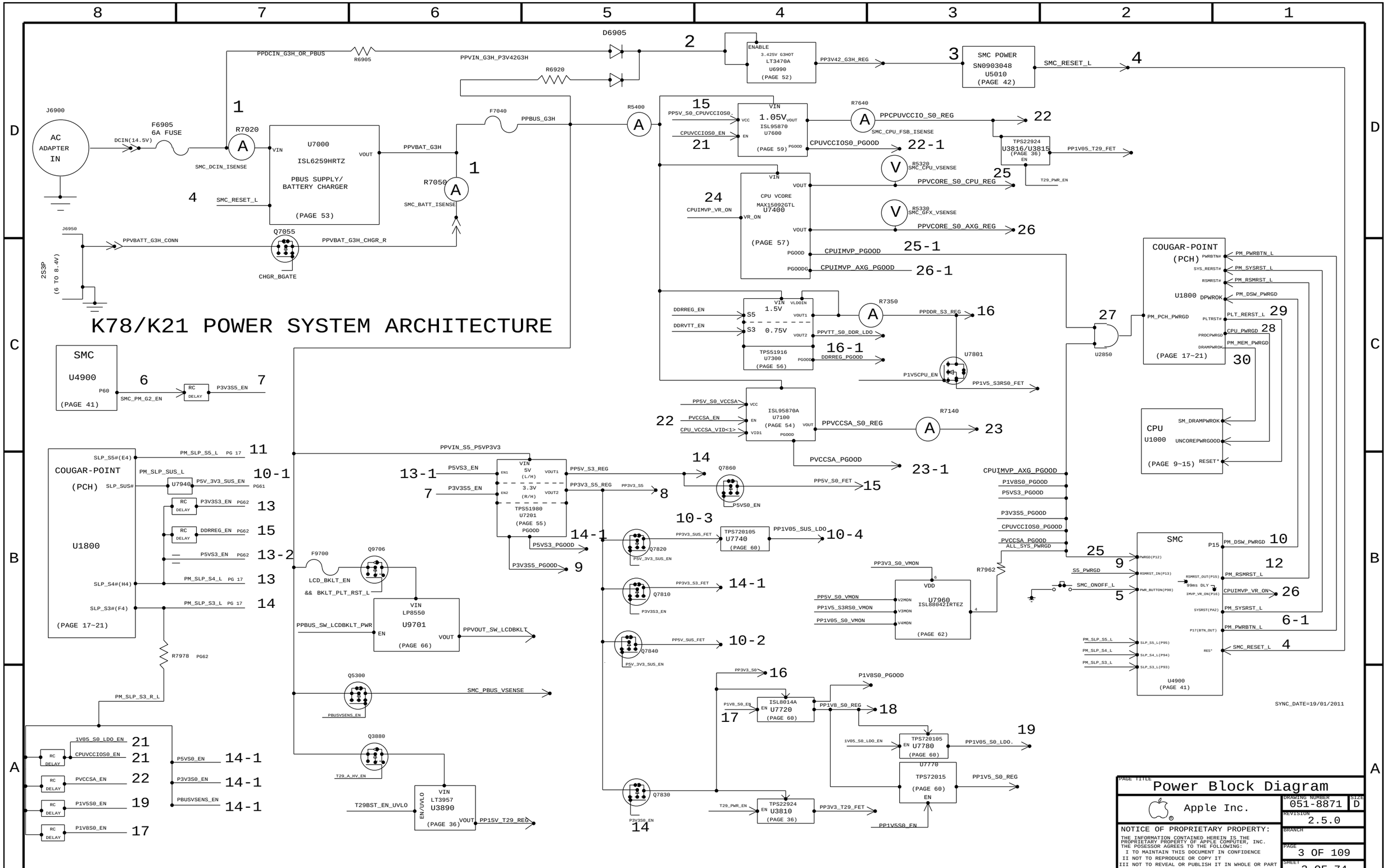

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1808	PCBA,MLB,K78	K78_CMNPTS,CPU:1.6GHZ,EEEE:DK9L,DDR3:HYNIX_2GB
639-1989	PCBA,MLB,1.6GHZ,HY 4GB,K78	K78_CMNPTS,CPU:1.6GHZ,EEEE:DLCR,DDR3:HYNIX_4GB
639-1990	PCBA,MLB,1.6GHZ,SA 2GB,K78	K78_CMNPTS,CPU:1.6GHZ,EEEE:DLCT,DDR3:SAMSUNG_2GB
639-1999	PCBA,MLB,1.6GHZ,SA 4GB,K78	K78_CMNPTS,CPU:1.6GHZ,EEEE:DLD6,DDR3:SAMSUNG_4GB
639-1987	PCBA,MLB,1.6GHZ,MI 2GB,K78	K78_CMNPTS,CPU:1.6GHZ,EEEE:DLCP,DDR3:MICRON_2GB
639-1995	PCBA,MLB,1.6GHZ,EL 4GB,K78	K78_CMNPTS,CPU:1.6GHZ,EEEE:DLD1,DDR3:ELPIDA_4GB
639-1998	PCBA,MLB,1.5GHZ,HY 2GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLD4,DDR3:HYNIX_2GB
639-1991	PCBA,MLB,1.5GHZ,HY 4GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLCV,DDR3:HYNIX_4GB
639-1986	PCBA,MLB,1.5GHZ,SA 2GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLCN,DDR3:SAMSUNG_2GB
639-1985	PCBA,MLB,1.5GHZ,SA 4GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLCM,DDR3:SAMSUNG_4GB
639-1992	PCBA,MLB,1.5GHZ,MI 2GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLCW,DDR3:MICRON_2GB
639-1993	PCBA,MLB,1.5GHZ,EL 4GB,K78	K78_CMNPTS,CPU:1.5GHZ,EEEE:DLCY,DDR3:ELPIDA_4GB
639-1994	PCBA,MLB,1.4GHZ,HY 2GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLD0,DDR3:HYNIX_2GB
639-1988	PCBA,MLB,1.4GHZ,HY 4GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLCQ,DDR3:HYNIX_4GB
639-1997	PCBA,MLB,1.4GHZ,SA 2GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLD3,DDR3:SAMSUNG_2GB
639-1984	PCBA,MLB,1.4GHZ,SA 4GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLCL,DDR3:SAMSUNG_4GB
639-2000	PCBA,MLB,1.4GHZ,MI 2GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLD5,DDR3:MICRON_2GB
639-1996	PCBA,MLB,1.4GHZ,EL 4GB,K78	K78_CMNPTS,CPU:1.4GHZ,EEEE:DLD2,DDR3:ELPIDA_4GB
085-2714	K78 MLB DEVELOPMENT BOM	K78_DEVEL:ENG
607-8084	CMN PTS,PCBA,MLB,K78	K78_COMMON

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7563	1	LABEL,LIO,K99	[EEEE_DK9L]	CRITICAL	EEEE:DK9L
825-7563	1	LABEL,LIO,K99	[EEEE_DLCL]	CRITICAL	EEEE:DLCL
825-7563	1	LABEL,LIO,K99	[EEEE_DLCM]	CRITICAL	EEEE:DLCM
825-7563	1	LABEL,LIO,K99	[EEEE_DLCN]	CRITICAL	EEEE:DLCN
825-7563	1	LABEL,LIO,K99	[EEEE_DLCP]	CRITICAL	EEEE:DLCP
825-7563	1	LABEL,LIO,K99	[EEEE_DLCQ]	CRITICAL	EEEE:DLCQ
825-7563	1	LABEL,LIO,K99	[EEEE_DLCR]	CRITICAL	EEEE:DLCR
825-7563	1	LABEL,LIO,K99	[EEEE_DLCT]	CRITICAL	EEEE:DLCT
825-7563	1	LABEL,LIO,K99	[EEEE_DLCV]	CRITICAL	EEEE:DLCV
825-7563	1	LABEL,LIO,K99	[EEEE_DLCW]	CRITICAL	EEEE:DLCW
825-7563	1	LABEL,LIO,K99	[EEEE_DLCY]	CRITICAL	EEEE:DLCY
825-7563	1	LABEL,LIO,K99	[EEEE_DLD0]	CRITICAL	EEEE:DLD0
825-7563	1	LABEL,LIO,K99	[EEEE_DLD1]	CRITICAL	EEEE:DLD1
825-7563	1	LABEL,LIO,K99	[EEEE_DLD2]	CRITICAL	EEEE:DLD2
825-7563	1	LABEL,LIO,K99	[EEEE_DLD3]	CRITICAL	EEEE:DLD3
825-7563	1	LABEL,LIO,K99	[EEEE_DLD4]	CRITICAL	EEEE:DLD4
825-7563	1	LABEL,LIO,K99	[EEEE_DLD5]	CRITICAL	EEEE:DLD5
825-7563	1	LABEL,LIO,K99	[EEEE_DLD6]	CRITICAL	EEEE:DLD6

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-2714	1	K78 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-8084	1	CMN PTS,PCBA,MLB,K78	CMNPTS	CRITICAL	K78_CMNPTS

SYNC_MASTER=K21_MLB SYNC_DATE=11/16/2010

PAGE TITLE
K78 BOM Variants

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DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
BRANCH
PAGE 4 OF 109
SHEET 4 OF 74

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K78 BOM GROUPS

BOM GROUP	BOM OPTIONS
K78_COMMON	ALTERNATE,COMMON,K78_MISC,K78_DEBUG:ENG,K78_PROGPARTS,USBHUB_2513B,T29BST:Y,EDP
K78_MISC	PCH:B3,CPUMEM_S0,HUB1_2NONREM,HUB2_2NONREM,T29:YES,SDRVI2C:MCU,SDRV_PD,KB_BL
K78_PROGPARTS	BOOTROM_PROG,SMC_PROG,T29ROM:PROG,T29MCU:PROG
K78_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCPLUS,VREFMRGN,S0PGOOD_IS4,S3_S0_LED,VCCIOISNS_ENG,AIRPORTISNS_ENG,HDDISNS_ENG,LCDBKLTISNS_ENG
K78_DEVEL:PVT	LPCPLUS,XDP_CONN,XDP_PCH
K78_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K78_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT
K78_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT,LPCPLUS,VCCIOISNS_PROD,AIRPORTISNS_PROD,HDDISNS_PROD,LCDBKLTISNS_PROD
DDR3:HYNIX_2GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:HYNIX_2GB
DDR3:HYNIX_4GB	DRAM_CFG0:L,DRAM_CFG1:L,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:SAMSUNG_2GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_2GB
DDR3:SAMSUNG_4GB	DRAM_CFG0:L,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:MICRON_2GB	DRAM_CFG0:H,DRAM_CFG1:L,DRAM_CFG2:L,DRAM_CFG3:L,DRAM_TYPE:MICRON_2GB
DDR3:ELPIDA_4GB	DRAM_CFG0:H,DRAM_CFG1:H,DRAM_CFG2:H,DRAM_CFG3:L,DRAM_TYPE:ELPIDA_4GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0550	1	EEPROM,32KBIT,2X3QFN	U3690	CRITICAL	T29ROM:BLANK
341T0354	1	IC,T29-ROM,K78	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341T0355	1	IC,T29-MCU,K78	U9330	CRITICAL	T29MCU:PROG
338S0895	1	IC,SMC,RENESAS,H8S/2117RP,9MM,TLP,HF	U4900	CRITICAL	SMC_BLANK
341T0350	1	IC,SMC,K78	U4900	CRITICAL	SMC_PROG
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_BLANK
341T0349	1	IC,EFI ROM,K21 K78	U6100	CRITICAL	BOOTROM_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
377S0107	377S0066		ALL	ONsemi alt to Semtech
138S0676	138S0691		ALL	Murata alt to Samsung
371S0679	371S0652		ALL	NXP alt to NXP
138S0671	138S0673		ALL	Taiyo alt to Murata
138S0679	138S0678		ALL	Murata/Samsung alt to Taiyo
353S3312	353S3055		ALL	NXP ALT TO PERICOM
104S0035	104S0011		ALL	Panasonic alt to Cyntec
152S1085	152S1307		ALL	Toko alt to Cyntec
152S1462	152S1295		ALL	Toko alt to NEC inductor
128S0333	128S0294		ALL	Sanyo alt to Sanyo/Frederick
337S4092	337S4100		ALL	EARLY 1.5GHZ CPU SAMPLES
337S4093	337S4101		ALL	EARLY 1.4GHZ CPU SAMPLES
376S0874	376S0895		ALL	FDMC8202S alt to RJK03E0DNS
376S1018	376S0617		ALL	FDMS0349 alt to RJK0305DPB
376S0826	376S0917		ALL	RJK0332DPB alt to FDMS0355
514-0744	998-3941		ALL	mDP connector alt

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4101	1	SNB,QAM1,QS,J1,1.6,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.6GHZ
337S4100	1	SNB,QAM2,QS,J1,1.5,17W,2+2,1.1,4M,BGA	U1000	CRITICAL	CPU:1.5GHZ
337S4099	1	SNB,QAM3,QS,J1,1.4,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.4GHZ
337S4098	1	SNB,QALV,QS,J1,1.3,17W,2+2,1.05,3M,BGA	U1000	CRITICAL	CPU:1.3GHZ
337S4080	1	COUGAR POINT,SLHAG,PRQ,BDB2QS67	U1800	CRITICAL	PCH:B2
337S4091	1	COUGAR POINT,B3,SLJ4K,PRQ,BDB2QS67	U1800	CRITICAL	PCH:B3
338S0976	1	IC,T29, FCBGA,PRQ 8x9MM	U3600	CRITICAL	T29:YES
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FGBA,T-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0585	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,T-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FGBA,B-DIE,HYNIX	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0586	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,B-DIE,HYNIX	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FGBA,G-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0587	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,G-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_2GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FGBA,D-DIE,SAMSUNG	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0588	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,D-DIE,SAMSUNG	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FGBA,V68A-D,MICRON	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FGBA,V68A-D,MICRON	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0590	4	IC,SDRAM,1GBIT,DDR3-1333,78P FBGA,V68A-D,MICRON	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:MICRON_2GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U2900,U2910,U2920,U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3000,U3010,U3020,U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FGBA,C-DIE,ELPIDA	U3100,U3110,U3120,U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0589	4	IC,SDRAM,2GBIT,DDR3-1333,78P FBGA,C-DIE,ELPIDA	U3200,U3210,U3220,U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	
353S2929	1	IC,ISL6259,BATCHARGER,3%,4C4MM,QFN28	U7000	CRITICAL	

DRAM CFG CHART

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
2GB	0
4GB	1

DIE REV	CFG 3
A	0
B	1

SYNC_MASTER=K21_MLB SYNC_DATE=11/16/2010

PAGE TITLE
BOM Configuration

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DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
BRANCH
PAGE 5 OF 109
SHEET 5 OF 74

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Functional Test Points

J4001: AirPort / BT Connector

FUNC_TEST

Net	Pages
PP3V3_WLAN_F (Need 6 TPs)	36
WIFI_EVENT_L	36 40
PCIE_AP_R2D_N	36 69
PCIE_AP_R2D_P	36 69
PCIE_CLK100M_AP_N	16 36 69
PCIE_CLK100M_AP_P	16 36 69
USB_BT_P	24 36 68
USB_BT_N	24 36 68
PCIE_AP_D2R_P	16 36 69
PCIE_AP_D2R_N	16 36 69
PCIE_WAKE_L	17 36
AP_RESET_CONN_L	36
AP_CLKREQ_Q_L	36
=PP3V3_S3_BT	7 36

(Need to add 8 GND TPs)

J4501: SATA SSD Connector

FUNC_TEST

Net	Pages
PP3V3_S0_HDD_R (Need 5 TPs)	37
SATA_HDD_D2R_C_P	37 68
SATA_HDD_D2R_C_N	37 68
SATA_HDD_R2D_N	37 68
SATA_HDD_R2D_P	37 68
SMC_HDD_OOB_TEMP_CONN	37
SMC_HDD_TEMP_CTL_CONN	37

(Need to add 6 GND TPs)

J4700: LIO Connector

FUNC_TEST

Net	Pages
=PP3V42_G3H_ONEWIRE	7 39
=PP3V3_S0_AUDIO	7 39
=PP3V3R1V5_S0_AUDIO	7 39
SYS_ONEWIRE	39 40
SMC_BC_ACOK	39 40 41
=USB_PWR_EN	38 39 61
=I2C_LIO_SDA	39 43
=I2C_LIO_SCL	39 43
=I2C_MIKEY_SCL	39 43
=I2C_MIKEY_SDA	39 43
AUD_IPHS_SWITCH_EN	19 39
AUD_IP_PERIPHERAL_DET	18 39
AUD_I2C_INT_L	18 39
AUD_GPIO_3	39 50
SPKRAMP_INR_N	39 50 73
SPKRAMP_INR_P	39 50 73
USB_EXTD_N	24 39 68
USB_EXTD_P	24 39 68
USB_CAMERA_N	18 39 68
USB_CAMERA_P	18 39 68
HDA_SDOUT	16 39 69
HDA_BIT_CLK	16 39 69
HDA_SDIN0	16 39 69
USB_EXTD_OC_L	24 39
HDA_RST_L	16 39 69
HDA_SYNC	16 39 69

(Need to add 5 GND TPs)

J5715: KB BKLT Connector

FUNC_TEST

Net	Pages
KBDLED_FB	48
KBDLED_ANODE	48

(Need to add 2 GND TPs)

J6955: HALL EFFECT Connector

FUNC_TEST

Net	Pages
SMC_LID_R	51
=PP3V42_G3H_HALL	7 51

J5100: LPC+SPI Connector

FUNC_TEST

Net	Pages
=PP3V3_S5_LPCPLUS	7 42
=PP5V_S0_LPCPLUS	7 42
LPC_AD<3..0>	16 40 42 69
SPI_ALT_MOSI	42
SPI_ALT_MISO	42
LPC_FRAME_L	16 40 42 69
PM_CLKRUN_L	17 40 42
SMC_TMS	40 41 42
LPCPLUS_RESET_L	25 42
SMC_TDO	40 41 42
SMC_TRST_L	40 42
SMC_MD1	40 42
SMC_TX_L	38 40 41 42
LPC_CLK33M_LPCPLUS	25 42 69
SPIROM_USE_MLB	19 42 49
SPI_ALT_CLK	42
SPI_ALT_CS_L	42
LPC_SERIRQ	16 40 42
LPC_PWRDWN_L	17 40 42
SMC_TDI	40 41 42
SMC_TCK	40 41 42
SMC_RESET_L	40 41 42 52
SMC_NMI	40 42
SMC_RX_L	38 40 41 42
LPCPLUS_GPIO	19 42

(Need to add 6 GND TPs)

J5600: Fan Connector

FUNC_TEST

Net	Pages
=PP5V_S0_FAN	7 47
FAN_RT_TACH	47
FAN_RT_PWM	47

(Need to add 1 GND TP)

J5700: IPD Flex Connector

FUNC_TEST

Net	Pages
SMC_PME_S4_WAKE_L	40 41 48
PP5V_TPAD_FILT	48
=PP3V42_G3H_TPAD	7 48
PP3V3_TPAD_CONN	48
USB_TPAD_CONN_P	48 73
USB_TPAD_CONN_N	48 73
=I2C_TPAD_SDA	43 48
=I2C_TPAD_SCL	43 48
SMC_ONOFF_L	40 41 48
SMC_LID	40 41 48 51
SMC_TPAD_RST_L	41 48

(Need to add 5 GND TPs)

J6900: DC-In Connector

FUNC_TEST

Net	Pages	Note
=PP18V5_DCIN_CONN	7 51	(Need 4 TPs)
=PP5V_S3_LIO_CONN	7 51	(Need 3 TPs)

(Need to add 5 GND TPs)

J6903: Speaker Connector

FUNC_TEST

Net	Pages
SPKRAMP_R_P_OUT	50 51 73
SPKRAMP_R_N_OUT	50 51 73

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

Net	Pages	Note
PPVBAT_G3H_CONN	51 52	(Need 4 TPs)
=SMBUS_BATT_SCL	43 51	
=SMBUS_BATT_SDA	43 51	
SYS_DETECT_L	51	

(Need to add 4 GND TPs near J6950 and 1 for shield)

J9000: Internal DP Connector

FUNC_TEST

Net	Pages	Note
PPVOUT_SW_LCDBKLT	62 65	(Need 2 TPs)
PP3V3_SW_LCD	62	(Need 2 TPs)
I2C_TCON_SDA_R	62	
LED_RETURN_6	62 65	
LED_RETURN_5	62 65	
LED_RETURN_4	62 65	
LED_RETURN_3	62 65	
LED_RETURN_2	62 65	
LED_RETURN_1	62 65	
DP_INT_HPD_CONN	62	
DP_INT_AUX_CH_C_N	62 69	
DP_INT_AUX_CH_C_P	62 69	
DP_INT_ML_F_P<0>	62 69	
DP_INT_ML_F_N<0>	62 69	
DP_INT_ML_F_P<1>	62 69	
DP_INT_ML_F_N<1>	62 69	
I2C_TCON_SCL_R	62	

(Need to add 5 GND TPs)

Misc Voltages & Control Signals

FUNC_TEST

Net	Pages
PPBUS_G3H	7 51
PPVIN_SW_T29BST	7 35
PPBUS_S5_HS_COMPUTING_ISNS	7
PPDCIN_G3H	7
PP3V42_G3H	7
PPVRTC_G3H	7
PP5V_S5	7
PP5V_SUS	7
PP3V3_S5	7 73
PP3V3_SUS	7
PP3V3_S3	7
PP1V8_S0	7
PP3V3_S0	7 73
PP1V5_S3	7 67
PP1V5_S3RS0	7 67
PP1V5_S0	7
PP1V05_S0	7
PPVTTDDR_S3	7
PP0V75_S0_DDRVTT	7
PPVCCSA_S0_CPU	7
PP1V05_SUS	7
PP15V_T29	7
PP3V3_T29	7
PP1V05_T29	7 35
PP1V05_S0_PCH_VCCADPLL	7
PPVCORE_S0_CPU	7
PPVCORE_S0_AXG	7
PP1V5_S3_CPU_VCCDQ	7
PP1V05_S0_CPU_VCCPQE	7
PP1V8_S0_CPU_VCCPLL_R	7

(Need to add 27 GND TPs)

NO_TEST Nets

NO_TEST (each net: TRUE, MAKE_BASE=TRUE)

Page	TP net	NC net	Page
	NC_EDP_TXP<0..3>	TP_EDP_TX_P<0..3>	9
	NC_EDP_TXN<0..3>	TP_EDP_TX_N<0..3>	9
	NC_EDP_AUXP	TP_EDP_AUX_P	
	NC_EDP_AUXN	TP_EDP_AUX_N	
	NC_CPU_THERMDA	TP_CPU_THERMDA	
	NC_CPU_THERMDC	TP_CPU_THERMDC	
	NC_CPU_RSVD<30..45>	TP_CPU_RSVD<30..45>	
	NC_CPU_RSVD<8..27>	TP_CPU_RSVD<8..27>	
	NC_PEG_R2D_CP<15..4>	=PEG_R2D_C_P<15..4>	9
	NC_PEG_R2D_CN<15..4>	=PEG_R2D_C_N<15..4>	9
	NC_PEG_D2RP<15..4>	=PEG_D2R_P<15..4>	9
	NC_PEG_D2RN<15..4>	=PEG_D2R_N<15..4>	9
17	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	
17	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	
17	TP_CRT_IG_RED	NC_CRT_IG_RED	
17	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	
17	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	
17	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	
17	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	
	TP_LVDS_IG_CTRL_CLK	NC_LVDS_IG_CTRL_CLK	
	TP_LVDS_IG_CTRL_DATA	NC_LVDS_IG_CTRL_DATA	
	TP_PCH_LVDS_VBG	NC_PCH_LVDS_VBG	
16	TP_HDA_SDIN1	NC_HDA_SDIN1	
16	TP_HDA_SDIN2	NC_HDA_SDIN2	
16	TP_HDA_SDIN3	NC_HDA_SDIN3	
18	TP_PCI_PME_L	NC_PCI_PME_L	
18	TP_PCI_CLK33M_OUT3	NC_PCI_CLK33M_OUT3	
16	TP_CLINK_CLK	NC_CLINK_CLK	
16	TP_CLINK_DATA	NC_CLINK_DATA	
16	TP_CLINK_RESET_L	NC_CLINK_RESET_L	
16	TP_PCIE_CLK100M_PEBN	NC_PCIE_CLK100M_PEBN	
16	TP_PCIE_CLK100M_PEBP	NC_PCIE_CLK100M_PEBP	
17	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINN	
17	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINP	
17	TP_SDVO_STALLN	NC_SDVO_STALLN	
17	TP_SDVO_STALLP	NC_SDVO_STALLP	
17	TP_SDVO_INTN	NC_SDVO_INTN	
17	TP_SDVO_INTP	NC_SDVO_INTP	
23	TP_XDP_PCH_OBSFN_A<0..1>	NC_TP_XDP_PCH_OBSFN_A<0..1>	
23	TP_XDP_PCH_OBSFN_B<0..1>	NC_TP_XDP_PCH_OBSFN_B<0..1>	
23	TP_XDPPCH_HOOK2	NC_TP_XDPPCH_HOOK2	
23	TP_XDPPCH_HOOK3	NC_TP_XDPPCH_HOOK3	
23	TP_XDP_PCH_OBSFN_D<0..1>	NC_TP_XDP_PCH_OBSFN_D<0..1>	
23	TP_XDP_PCH_HOOK4	NC_TP_XDP_PCH_HOOK4	
23	TP_XDP_PCH_HOOK5	NC_TP_XDP_PCH_HOOK5	
16	TP_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0	
16	TP_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1	
16	TP_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2	
16	TP_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3	
	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	
	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	
16	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	
16	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	
16	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	
16	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	
16	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7N	
16	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7P	
	TP_PSOC_P1_3	NC_PSOC_P1_3	
16	TP_SATA_B_D2RN	NC_SATA_B_D2RN	
16	TP_SATA_B_D2RP	NC_SATA_B_D2RP	
16	TP_SATA_B_R2D_CN	NC_SATA_B_R2D_CN	
16	TP_SATA_B_R2D_CP	NC_SATA_B_R2D_CP	
16	TP_SATA_D_D2RN	NC_SATA_D_D2RN	
16	TP_SATA_D_D2RP	NC_SATA_D_D2RP	
16	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CN	
16	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CP	
16	TP_SATA_E_D2RN	NC_SATA_E_D2RN	
16	TP_SATA_E_D2RP	NC_SATA_E_D2RP	
16	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CN	
16	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CP	
16	TP_SATA_F_D2RN	NC_SATA_F_D2RN	
16	TP_SATA_F_D2RP	NC_SATA_F_D2RP	
16	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CN	
16	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CP	
	TP_PCH_TP18	NC_PCH_TP18	
	TP_PCH_TP17	NC_PCH_TP17	
	TP_PCH_TP16	NC_PCH_TP16	
	TP_PCH_TP15	NC_PCH_TP15	
	TP_PCH_TP14	NC_PCH_TP14	
	TP_PCH_TP13	NC_PCH_TP13	
	TP_PCH_TP12	NC_PCH_TP12	
	TP_PCH_TP10	NC_PCH_TP10	
	TP_PCH_TP9	NC_PCH_TP9	
	TP_PCH_TP8	NC_PCH_TP8	
	TP_PCH_TP7	NC_PCH_TP7	
	TP_PCH_TP6	NC_PCH_TP6	
	TP_PCH_TP5	NC_PCH_TP5	
	TP_PCH_TP4	NC_PCH_TP4	
	TP_PCH_TP3	NC_PCH_TP3	
	TP_PCH_TP2	NC_PCH_TP2	
	TP_PCH_TP1	NC_PCH_TP1	
8	TP_LVDS_IG_B_CLKN	NC_LVDS_IG_B_CLKN	
8	TP_LVDS_IG_B_CLKP	NC_LVDS_IG_B_CLKP	
	TP_LVDS_IG_BKL_PWM	NC_LVDS_IG_BKL_PWM	
	SMC_BS_ALRT_L	NC_SMC_BS_ALRT_L	

Ref	Net	Pages
I566	PCH_VSS_NCTF<1>	69
I567	PCH_VSS_NCTF<2>	69
I568	PCH_VSS_NCTF<5>	69
I570	PCH_VSS_NCTF<9>	69
I571	PCH_VSS_NCTF<11>	69
I569	PCH_VSS_NCTF<12>	69
I500	PCH_VSS_NCTF<15>	69
I499	PCH_VSS_NCTF<17>	69
I501	PCH_VSS_NCTF<19>	6 69
I502	PCH_VSS_NCTF<19>	6 69
I503	PCH_VSS_NCTF<21>	69
I504	PCH_VSS_NCTF<25>	69
I505	PCH_VSS_NCTF<27>	69
I506	PCH_VSS_NCTF<29>	69

SYNC_MASTER=(K99_MLB) SYNC_DATE=(02/16/2010)

PAGE TITLE: Functional Test / No Test

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"G3Hot" (Always-Present) Rails

52 =PPBUS_G3H — PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPBUS_S0_LCDBKLT 65
- =PPBUS_S0_VSENSE 44
- =PPVIN_SW_T29BST 8 35
- =PPVIN_S5_HS_COMPUTING_ISNS_R 45
- =PPVIN_S5_P5VP3V3 54

35 6 PPVIN_SW_T29BST
VOLTAGE=12.6V

45 =PPVIN_S5_HS_COMPUTING_ISNS — PPBUS_S5_HS_COMPUTING_ISNS 6
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPVIN_S0_CPUIMVP 56 57
- =PPVIN_S3_DDRREG 55
- =PPVIN_S0_CPUVCCIOS0 58
- =PPVIN_S0_VCCSAS0 53
- =PPVIN_S0_CPUAXG 57

51 6 =PP18V5_DCIN_CONN — PPDCIN_G3H 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR 52
- =PPDCIN_S5_VSENSE 44

51 =PP3V42_G3H_REG — PP3V42_G3H 6
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V3_S5_LPCPLUS 6 42
- =PP3V3_S5_SMC 40 41
- =PP3V42_G3H_HALL 6 51
- =PP3V42_G3H_CHGR 52
- =PP3V42_G3H_PWRCTL 61
- =PP3V42_G3H_SMBUS_SMC_BSA 43
- =PP3V42_G3H_SMCUSBMUX 38
- =PP3V42_G3H_TPAD 6 48
- =PPVIN_S5_SMCVREF 41
- =PPVBAT_G3_SYSCLK 25
- =PP3V42_G3H_ONEWIRE 6 39

25 =PPVRTC_G3_OUT — PPVRTC_G3H 6
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE
- =PPVRTC_G3_PCH 16 17 20

5V Rails

54 =PP5V_S5_LDO — PP5V_S5 6
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_P1V5DDRFET 60
- =PP5V_S5_P5VSUSFET 60
- =PP5V_S5_TPAD 48

60 =PP5V_SUS_FET — PP5V_SUS 6
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP5V_SUS_PCH 22

54 =PP5V_S3_REG — PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_AUDIO_AMP 50
- =PP5V_S3_DDRREG 55
- =PP5V_S3_MEMRESET 26
- =PP5V_S3_P5VS0FET 60
- =PP5V_S3_RTUSB 38
- =PP5V_S3_LIO_CONN 6 51

60 =PP5V_S0_FET — PP5V_S0
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_BKL 65
- =PP5V_S0_CPUIMVP 56
- =PP5V_S0_CPUVCCIOS0 58
- =PP5V_S0_FAN 6 47
- =PP5V_S0_LPCPLUS 6 42
- =PP5V_S0_VCCSA 53
- =PP5V_S0_PCH 22
- =PP5V_S0_VMON 61
- =PP5V_S0_KBDLED 48

3.3V Rails

54 =PP3V3_S5_REG — PP3V3_S5 6 73
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
- =PP3V3_S5_XDP 23
- =PP3V3_S0_P3V3S0FET 60
- =PP3V3_S3_P3V3S3FET 60
- =PP3V3_S5_CPU_VCCDDR 26
- =PP3V3_S4_SMC 41
- =PP3V3_S5_LCD 62
- =PP3V3_S5_PCH 17 19
- =PP3V3_S5_PCHPWRGD 25
- =PP3V3_S5_SMCBATLOW 41
- =PP3V3_S5_ROM 49
- =PP3V3_S5_USB_RESET 24
- =PP3V3_S5_PCH_VCCDSW 20 22
- =PP3V3_S5_SYSCLK 25
- =PP3V3_S5_VMON 61
- =PP3V3_S5_PWRCTL 61
- =PP3V3_S5_PCH_VCC_SPI 20 22
- =PP3V3_S5_P3V3SUSFET 60
- =PP3V3_S5_TPAD 48
- =PP3V3_S4_DPAPWRSW 64

60 =PP3V3_SUS_FET — PP3V3_SUS 6
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_SUS_PCH_VCCSUS_USB 20 22
- =PP3V3_SUS_PCH_VCCSUS_GPIO 20 22
- =PP3V3_SUS_PCH_VCCSUS 20
- =PP3V3_SUS_GPIO 16 17 18 19
- =PP3V3_SUS_PCH 22
- =PP3V3_SUS_PWRCTL 61
- =PP3V3_SUS_P1V05SUSLDO 59
- =PP3V3_SUS_SMC 41

60 =PP3V3_S3_FET — PP3V3_S3 6
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S3_BT 6 36
- =PP3V3_S3_MEMRESET 26
- =PP3V3_S3_SMBUS_SMC_A_S3 43
- =PP3V3_S3_SMBUS_SMC_MGMT 43
- =PP3V3_S3_USB_HUB 8 24
- =PP3V3_S3_USB_RESET 24
- =PP3V3_S3_VREFMRGN 31
- =PP3V3_S3_WLAN 36
- =PP3V3_S3_WLANISNS 45
- =PP3V3_S3_BMON_ISNS 45
- =PP3V3_S3_PCH_GPIO 18 19
- =PP3V3_S3_1V5S3ISNS 45
- =PP3V3_S3_DBGLEDS 51

60 =PP3V3_S0_FET — PP3V3_S0 6 73
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S0_CPUVCCIOISNS 44
- =PP3V3_S0_AUDIO 6 39
- =PP3V3_S0_BKL_VDDIO 65
- =PP3V3_S0_HS_COMPUTING_ISNS 45
- =PP3V3_S0_CPUTHMSNS 46
- =PP3V3_S0_CPU_VCCIO_SEL 12
- =PP3V3_S0_DP_DDC 8
- =PP3V3_S0_FAN 47
- =PP3V3_S0_P3V3T29FET 35
- =PP3V3_S0_P1V8S0 59
- =PP3V3_S0_PCH 16 19 22
- =PP3V3_S0_PCH_GPIO 18
- =PP3V3_S0_PCH_VCC3_3_CLK 22
- =PP3V3_S0_PCH_VCC3_3_GPIO 20 22
- =PP3V3_S0_PCH_VCC3_3_HVCMOS 20 22
- =PP3V3_S0_PCH_VCC3_3_PCI 20 22
- =PP3V3_S0_PCH_VCC3_3_SATA 20 22
- =PP3V3_S0_PCH_VCCADAC 22
- =PP3V3_S0_PCH_STRAPS 16 17 19
- =PP3V3_S0_PWRCTL 61
- =PP3V3_S0_RSTBUF 25
- =PP3V3_S0_SB_PM 25
- =PP3V3_S0_SMBUS_PCH 43
- =PP3V3_S0_SMBUS_SMC_0_S0 43
- =PP3V3_S0_SMBUS_SMC_B_S0 43
- =PP3V3_S0_SMC 41
- =PP3V3_S0_HDD 37
- =PP3V3_S0_HDDISNS 45
- =PP3V3_S0_VMON 61
- =PP3V3_S0_P1V5S0 59
- =PP3V3_S0_T29PWRCTL 35
- =PP3V3_S0_DPSDRVA 63
- =PP3V3_S0_P1V05S0LDO 59
- =PP3V3_S0_IMVPISNS 44
- =PP3V3_S0_XDP 23
- =PP3V3_S0_T29I2C 43
- =PP3V3_S0_BKLTISNS 45
- =PP3V3_S0_SYSCLKGEN 25

1.8V/1.5V/1.2V/1.05V Rails

59 =PP1V8_S0_REG — PP1V8_S0 6
2A max supply
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S0_CPU_VCCPLL 14
- =PP1V8_S0_PCH_VCC_DFTERM 18 20 22
- =PP1V8_S0_P1V05S0LDO 59
- =PP1V8R1V5_S0_PCH_VCCVRM 20
- =PPVDDIO_S0_SBCLK 25
- =PP1V8_S0_P1V5S0 59

55 =PPDDR_S3_REG — PP1V5_S3 6 67
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_MEMRESET 26
- =PP1V5_S3_MEM_A 27 28 32
- =PP1V5_S3_MEM_B 29 30 32
- =PP1V5_S3_P1V5S3RS0_FET 60
- =PPVIN_S0_DDRREG_LDO 55

60 =PP1V5_S3RS0_FET — PP1V5_S3RS0 6 67
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_CPU_VCCDDR 10 12 15 26
- =PP1V5_S3RS0_VMON 61

59 =PP1V5_S0_REG — PP1V5_S0 6
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP3V3R1V5_S0_AUDIO 6 39
- =PP3V3R1V5_S0_PCH_VCCSUSHDA 16 20 22

55 31 =PPVTT_S3_DDR_BUF — PPVTTDDR_S3 6
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

55 =PPVTT_S0_DDR_LDO — PP0V75_S0_DDRVTT 6
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
- =PP0V75_S0_MEM_VTT_A 32
- =PP0V75_S0_MEM_VTT_B 32
- =PPVTT_S0_VTTCLAMP 26

53 =PPVCCSA_S0_REG — PPVCCSA_S0_CPU 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PPVCCSA_S0_CPU 12 15

59 =PP1V05_SUS_LDO — PP1V05_SUS 6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_SUS_PCH_JTAG 23

58 =PPCPUVCCIO_S0_REG — PP1V05_S0 6
? mA
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_PCH_VCCIO_PLLPCIE 20
- =PP1V05_S0_CPU_VCCIO 9 10 12 14
- =PP1V05_S0_PCH 16 22
- =PP1V05_S0_PCH_VCCIO 20 22
- =PP1V05_S0_PCH_VCCIO_PCIE 17
- =PP1V05_S0_PCH_VCCIO_SATA 16 20 22
- =PP1V05_S0_PCH_VCCASW 20 22
- =PP1V05_S0_PCH_VCCIO_USB 20 22
- =PP1V05_S0_PCH_VCC_CORE 20 22
- =PP1V05_S0_VMON 61
- =PP1V05_S0_PCH_VCCIO_CLK 20 22
- =PPVCCIO_S0_CPUIMVP 56
- =PP1V05_S0_PCH_VCCDIFFCLK 16 20 22
- =PP1V05_S0_PCH_VCCSSC 20 22
- =PP1V05_S0_PCH_V_PROC_IO 20 22
- =PP1V05_S0_PCH_VCCIO_PLLUSB 20
- =PP1V05_S0_PCH_VCC_DMI 20 22
- =PP1V05_S0_PCH_VCCIO_PLLFDI 20
- =PP1V05_S0_PCH_VCCDMI_FDI 20
- =PPVCCIO_S0_XDP 23
- =PPVCCIO_S0_SMC 40
- =PP1V05_S0_P1V05T29FET 35

T29 Rails (off when no cable)

35 8 =PP15V_T29_REG — PP15V_T29 6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.6V
MAKE_BASE=TRUE
- =PPHV_SW_DPAPWRSW 64

35 =PP3V3_T29_FET — PP3V3_T29 6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PPVDDIO_T29_CLK 25
- =PP3V3_T29_RTR 33 34 35
- =PP3V3_T29_PCH_GPIO 16 19

35 =PP1V05_T29_FET — PP1V05_T29 6 35
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_T29_RTR 34

1V05 S0 LDO

59 =PP1V05_S0_LDO — PP1V05_S0_PCH_VCCADPLL 6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_PCH_VCCADPLL 20

Chipset "VCore" Rails

57 =PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU 9 12 14
- =PPCPUVCORE_S0_VSENSE 44

57 =PPVCORE_S0_AXG_REG — PPVCORE_S0_AXG 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU_VCCAXG 9 12 15
- =PPGFXVCORE_S0_VSENSE 44

15 12 =PP1V5_S3_CPU_VCCDQ — PP1V5_S3_CPU_VCCDQ 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

14 12 =PP1V05_S0_CPU_VCCPQE — PP1V05_S0_CPU_VCCPQE 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

14 12 =PP1V8_S0_CPU_VCCPLL_R — PP1V8_S0_CPU_VCCPLL_R 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010
PAGE TITLE
Power Aliases

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DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
BRANCH
PAGE 8 OF 109
SHEET 7 OF 74

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CPU Heat Sink Mounting Bosses

Z0913 STDOFF-4.50D1.8H-SM
Z0910 STDOFF-4.50D1.8H-SM
Z0911 STDOFF-4.50D1.8H-SM
Z0912 STDOFF-4.50D1.8H-SM
4x 860-1327

Fan Boss
Z0905 STDOFF-4.50D1.8H-SM
860-1327

X21 Boss
Z0914 STDOFF-4.50D1.9H-SM
860-1327

SSD Boss
Z0915 STDOFF-4.50D1.9H-SM
860-1327

EMI I/O Pogo Pins

DisplayPort Pogo

CRITICAL
ZS0905
POGO-2.00D-3.6H-K86-K87
SM
870-1938

CRITICAL
ZS0904
POGO-2.00D-2.95H-K86-K87
SM
870-1940

USB/SD Card Pogo

CRITICAL
ZS0906
POGO-2.00D-3.6H-K86-K87
SM
870-1938

CRITICAL
ZS0907
1.4DIA-SHORT-SILVER-K99
SM
870-2015

T29 Can Slots

SL0901
TH-NSP
SL-1.1X0.4-1.4x0.7
998-2691

SL0902
TH-NSP
SL-1.1X0.4-1.4x0.7
998-2691

DisplayPort PCB Stiffener

(Provides PCB support for small finger above J9400)

NO STUFF
MT0900
STIFFENER-K16-K99
SM-SP
806-1176

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

CPU signals

26	MEMVTT_EN		=DDRVTT_EN 26 55
69 63	DP_EXTA_ML_C_P<3..0> 68	DP_IG_ML_P<3..0>	TP_DP_IG_B_MLP<3..0> 17
69 63	DP_EXTA_ML_C_N<3..0> 68	DP_IG_ML_N<3..0>	TP_DP_IG_B_MLN<3..0> 17
69 63	DP_EXTA_AUXCH_C_P 68	DP_IG_AUX_CH_P	DP_IG_B_AUX_P 17
69 63	DP_EXTA_AUXCH_C_N 68	DP_IG_AUX_CH_N	DP_IG_B_AUX_N 17
16	PCIE_EXCARD_D2R_N		NC_PCIE_EXCARD_D2RN
16	PCIE_EXCARD_D2R_P		NC_PCIE_EXCARD_D2RP
16	PCIE_EXCARD_R2D_C_N		NC_PCIE_EXCARD_R2D_CN
16	PCIE_EXCARD_R2D_C_P		NC_PCIE_EXCARD_R2D_CP
69 16	PCIE_CLK100M_EXCARD_N		NC_PCIE_CLK100M_EXCARDN
69 16	PCIE_CLK100M_EXCARD_P		NC_PCIE_CLK100M_EXCARDP
69 16	PEG_CLK100M_P		NC_PEG_CLK100MP
69 16	PEG_CLK100M_N		NC_PEG_CLK100MN
16	TP_PCH_CLKOUT_DPN	DPLL_REF_CLK_N	DPLL_REF_CLKN 10 66
16	TP_PCH_CLKOUT_DPP	DPLL_REF_CLK_P	DPLL_REF_CLKP 10 66
67 11	MEM_A_CLK_P<1>		TP_MEM_A_CLKP<1>
67 11	MEM_A_CLK_N<1>		TP_MEM_A_CLKN<1>
67 11	MEM_A_CKE<1>		NC_MEM_A_CKE<1>
67 11	MEM_A_CS_L<1>		NC_MEM_A_CS_L<1>
67 11	MEM_A_ODT<1>		NC_MEM_A_ODT<1>
67 11	MEM_B_CLK_P<1>		TP_MEM_B_CLKP<1>
67 11	MEM_B_CLK_N<1>		TP_MEM_B_CLKN<1>
67 11	MEM_B_CKE<1>		NC_MEM_B_CKE<1>
67 11	MEM_B_CS_L<1>		NC_MEM_B_CS_L<1>
67 11	MEM_B_ODT<1>		NC_MEM_B_ODT<1>
67 11	MEM_A_A<15>		TP_MEM_A_A<15>
67 11	MEM_B_A<15>		TP_MEM_B_A<15>

T29 DP Ports

9	=PEG_R2D_C_P<3..0> 66	PEG_R2D_C_P<3..0>	PCIE_T29_R2D_C_P<3..0> 33 69
9	=PEG_R2D_C_N<3..0> 66	PEG_R2D_C_N<3..0>	PCIE_T29_R2D_C_N<3..0> 33 69
9	=PEG_D2R_P<3..0> 66	PEG_D2R_P<3..0>	PCIE_T29_D2R_P<3..0> 33 69
9	=PEG_D2R_N<3..0> 66	PEG_D2R_N<3..0>	PCIE_T29_D2R_N<3..0> 33 69
17	TP_DP_IG_C_HPD		DP_T29SNK0_HPD 33
17	TP_DP_IG_C_MLP<3..0>		DP_T29SNK0_ML_C_P<3..0> 33 71
17	TP_DP_IG_C_MLN<3..0>		DP_T29SNK0_ML_C_N<3..0> 33 71
17	TP_DP_IG_C_AUXP		DP_T29SNK0_AUXCH_C_P 33 71
17	TP_DP_IG_C_AUXN		DP_T29SNK0_AUXCH_C_N 33 71
17	TP_DP_IG_D_HPD		DP_IG_D_HPD
17	TP_DP_IG_C_CTRL_CLK		DP_IG_C_CTRL_CLK
17	TP_DP_IG_C_CTRL_DATA		DP_IG_C_CTRL_DATA
17	TP_DP_IG_D_CTRL_CLK		DP_IG_D_CTRL_CLK
17	TP_DP_IG_D_CTRL_DATA		DP_IG_D_CTRL_DATA

8 7 =PP3V3_S0_DP_DDC
R0920 2.2K 5% 1/20W MF 201
R0921 2.2K 5% 1/20W MF 201
R0922 2.2K 5% 1/20W MF 201
R0923 2.2K 5% 1/20W MF 201
R0909 100K 5% 1/20W MF 201

8 7 =PP3V3_S0_DP_DDC
R0924 2.2K 5% 1/20W MF 201
R0925 2.2K 5% 1/20W MF 201

63	DP_EXTA_DDC_CLK	DP_IG_B_DDC_CLK 17
63	DP_EXTA_DDC_DATA	DP_IG_B_DDC_DATA 17
63	DP_EXTA_HPD	DP_IG_B_HPD 17

R0908 100K 5% 1/20W MF 201
CRITICAL
R0910 0.01 0.5% 1W MF 0612-1

65	PPBUS_SW_LCDBKLT_PWR	PPBUS_SW_BKL 65
73 45	ISNS_LCDBKLT_P	
73 45	ISNS_LCDBKLT_N	=PPBUS_SW_BKL

MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE

NC_USB_HUB1_OCS4		=USB_HUB1_OCS4 24
NC_USB_HUB2_OCS4		=USB_HUB2_OCS4 24

LVDS Aliases

6	TP_LVDS_IG_B_CLKP	LVDS_IG_B_CLK_P 68
6	TP_LVDS_IG_B_CLKN	LVDS_IG_B_CLK_N 68
	NC_LVDS_IG_B_DATAP<0..3>	LVDS_IG_B_DATA_P<0..3> 68
	NC_LVDS_IG_B_DATAN<0..3>	LVDS_IG_B_DATA_N<0..3> 68
	NC_LVDS_IG_A_DATAP<3>	LVDS_IG_A_DATA_P<3> 68
	NC_LVDS_IG_A_DATAN<3>	LVDS_IG_A_DATA_N<3> 68
65	LCD_BKLT_PWM	LVDS_IG_BKL_PWM 17
62	LCD_IG_PWR_EN	LVDS_IG_PANEL_PWR 17
65	LCD_BKLT_EN	LVDS_IG_BKL_ON 17

SATA Aliases

Unused SATA ODD Signals

68 16	IN	SATA_ODD_R2D_C_P	NC_SATA_ODD_R2DCP
68 16	IN	SATA_ODD_R2D_C_N	NC_SATA_ODD_R2DCN
68 16	OUT	SATA_ODD_D2R_P	NC_SATA_ODD_D2RP
68 16	OUT	SATA_ODD_D2R_N	NC_SATA_ODD_D2RN

UNUSED SDCARD USB Aliases

8 7 =PP3V3_S3_USB_HUB
R0901 10K 5% 1/20W MF 201
R0902 10K 5% 1/20W MF 201

68 24	OUT	USB_SDCARD_N
68 24	OUT	USB_SDCARD_P

T29_A_BIAS caps

SIGNAL_MODEL=EMPTY
R0926 51 5% 1/20W MF 201
64 8 T29_A_BIAS_R — T29_A_BIAS_D2RP1 64
C0906 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

SIGNAL_MODEL=EMPTY
R0927 51 5% 1/20W MF 201
64 8 T29_A_BIAS_R — T29_A_BIAS_D2RN1 64
C0907 0.01UF 10% 10V X5R 201 SIGNAL_=EMPTY

35 7 =PPVIN_SW_T29BST — R0960 0 5% 1/0W MF-LF 805 — =PP15V_T29_REG 7 35
T29BST:N
64 63 T29_A_BIAS
C0960 0.01UF 10% 10V X5R 201

T29_A_BIAS caps

SIGNAL_MODEL=EMPTY
R0931 51 5% 1/20W MF 201
64 8 T29_A_BIAS_R — T29_A_BIAS_R2DP0 63
C0901 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

SIGNAL_MODEL=EMPTY
R0932 51 5% 1/20W MF 201
64 8 T29_A_BIAS_R — T29_A_BIAS_R2DN0 63
C0902 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

SIGNAL_MODEL=EMPTY
R0933 51 5% 1/20W MF 201
64 8 T29_A_BIAS_R — T29_A_BIAS_R2DP1 63
C0903 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

SIGNAL_MODEL=EMPTY
R0934 51 5% 1/20W MF 201
64 8 T29_A_BIAS_R — T29_A_BIAS_R2DN1 63
C0904 0.01UF 10% 10V X5R 201 SIGNAL_MODEL=EMPTY

DP_A_BIAS caps

63 DP_A_BIAS_P_2 — C0962 0.01UF 10% 10V X5R 201
63 DP_A_BIAS_P_0 — C0964 0.01UF 10% 10V X5R 201
63 DP_A_BIAS_N_2 — SIGNAL_MODEL=EMPTY — C0905 0.01UF 10% 10V X5R 201
63 DP_A_BIAS_N_0 — SIGNAL_MODEL=EMPTY — C0908 0.01UF 10% 10V X5R 201

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE	P1V5S3RS0_RAMP_DONE	IN 60
TP_DDRREG_PGOOD	DDRREG_PGOOD	IN 55

T29 JTAG

R0990 0 5% 1/20W MF 201

23 19	IN	JTAG_ISP_TCK	JTAG_T29_TCK_R — JTAG_T29_TCK OUT 33
19	IN	JTAG_ISP_TDI	JTAG_T29_TDI OUT 33
19	OUT	JTAG_ISP_TDO	JTAG_T29_TDO IN 33

T29 Aliases

Unused USB ports

24 8 7 =PP3V3_S3_USB_HUB
R0915 10K 5% 1/20W MF 201
R0916 10K 5% 1/20W MF 201

NO STUFF
R0917 0 1/20W MF 201
R0918 0 1/20W MF 201

68 63	T29_A_RSVD_N	USB_T29A_N 24 68
68 63	T29_A_RSVD_P	USB_T29A_P 24 68

NO STUFF

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010
PAGE TITLE
Signal Aliases

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DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
BRANCH
PAGE 9 OF 109
SHEET 8 OF 74

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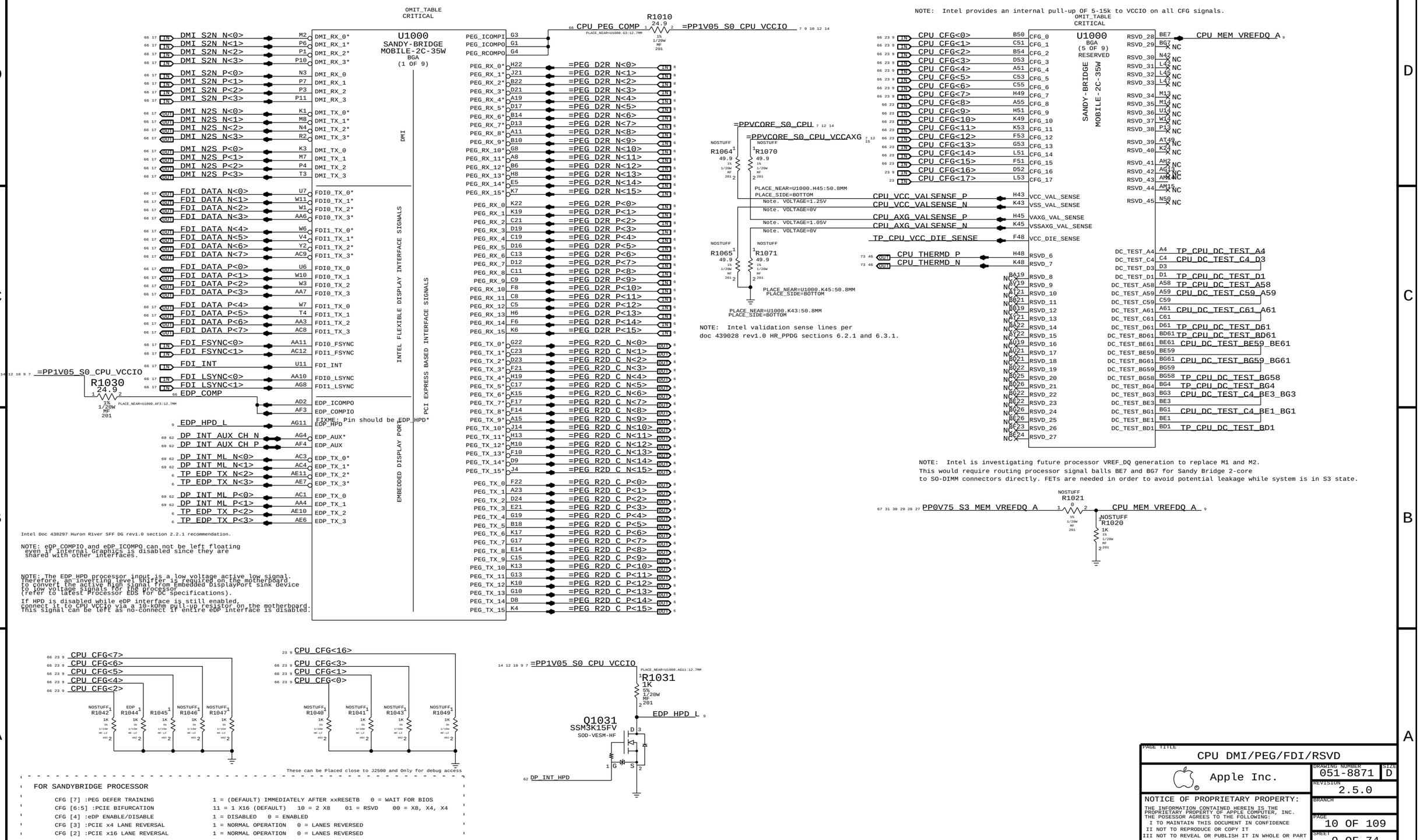

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
BRANCH
PAGE 10 OF 109
SHEET 9 OF 74

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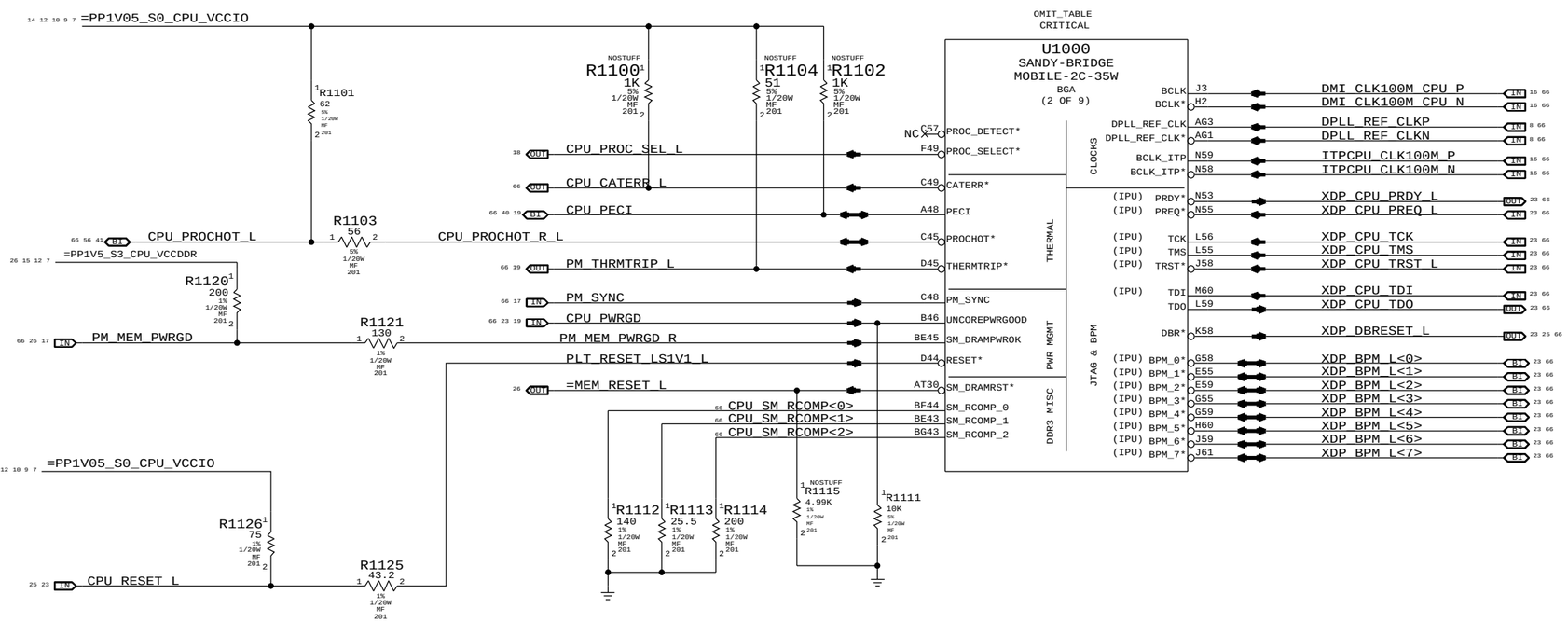

PAGE TITLE
CPU CLOCK/MISC/JTAG

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DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
BRANCH
PAGE 11 OF 109
SHEET 10 OF 74

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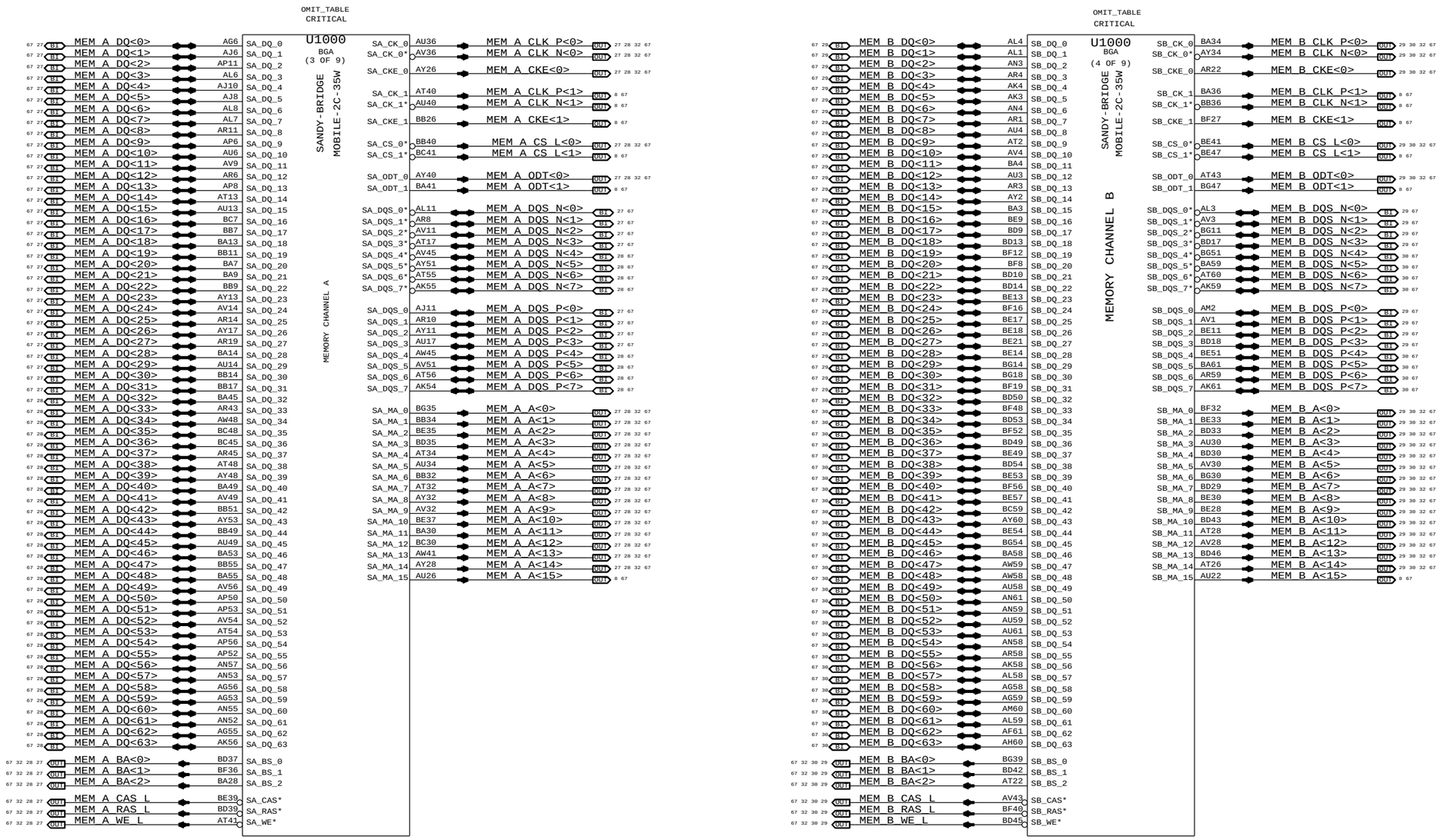

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PAGE TITLE
CPU DDR3 INTERFACES

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DRAWING NUMBER 051-8871
SIZE D
REVISION 2.5.0
BRANCH
PAGE 12 OF 109
SHEET 11 OF 74

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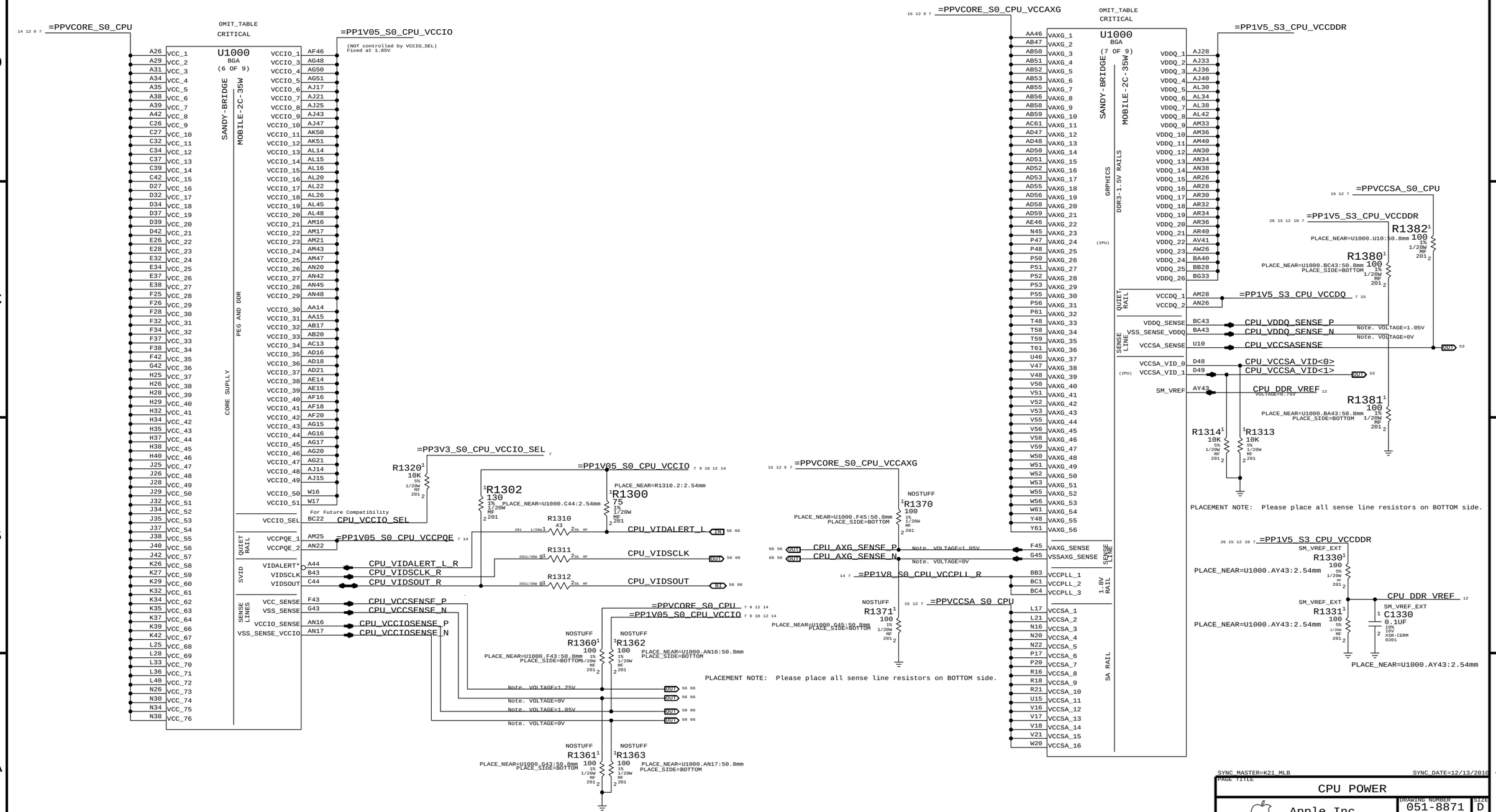

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PAGE TITLE: CPU POWER

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REVISION: 2.5.0

BRANCH:

PAGE: 13 OF 109

SHEET: 12 OF 74

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OMIT_TABLE
CRITICAL

U1000
BGA
(9 OF 9)
SANDY-BRIDGE
MOBILE-2C-35W

BG13	VSS	VSS	M11
BG17	VSS	VSS	M15
BG21	VSS	VSS	M58
BG24	VSS	VSS	N1
BG28	VSS	VSS	N17
BG37	VSS	VSS	N21
BG41	VSS	VSS	N25
BG45	VSS	VSS	N28
BG49	VSS	VSS	N33
BG53	VSS	VSS	N36
C29	VSS	VSS	N40
C35	VSS	VSS	N43
C40	VSS	VSS	N47
D4	VSS	VSS	N48
D6	VSS	VSS	N51
D10	VSS	VSS	N52
D14	VSS	VSS	N56
D18	VSS	VSS	N61
D22	VSS	VSS	P9
D26	VSS	VSS	P14
D29	VSS	VSS	P16
D35	VSS	VSS	P18
D40	VSS	VSS	P21
D43	VSS	VSS	P58
D46	VSS	VSS	P59
D50	VSS	VSS	R4
D54	VSS	VSS	R17
D58	VSS	VSS	R20
E3	VSS	VSS	R46
E25	VSS	VSS	T1
E29	VSS	VSS	T47
E35	VSS	VSS	T50
E40	VSS	VSS	T51
F13	VSS	VSS	T52
F15	VSS	VSS	T53
F19	VSS	VSS	T55
F29	VSS	VSS	T56
F35	VSS	VSS	U8
F40	VSS	VSS	U13
F55	VSS	VSS	V20
G6	VSS	VSS	V61
G48	VSS	VSS	W8
G51	VSS	VSS	W13
G61	VSS	VSS	W15
H4	VSS	VSS	W18
H10	VSS	VSS	W21
H14	VSS	VSS	W46
H17	VSS	VSS	Y4
H21	VSS	VSS	Y47
H53	VSS	VSS	Y58
H58	VSS	VSS	Y59
J1	VSS		
J49	VSS		
J55	VSS		
K8	VSS		
K11	VSS		
K21	VSS	VSS_NCTF	A5
K51	VSS	VSS_NCTF	A57
L16	VSS	VSS_NCTF	BC61
L20	VSS	VSS_NCTF	BD3
L22	VSS	VSS_NCTF	BD59
L26	VSS	VSS_NCTF	BE4
L30	VSS	VSS_NCTF	BE58
L34	VSS	VSS_NCTF	BG5
L38	VSS	VSS_NCTF	BG57
L43	VSS	VSS_NCTF	C3
L48	VSS	VSS_NCTF	C58
L61	VSS	VSS_NCTF	D59
M4	VSS	VSS_NCTF	E1
M6	VSS	VSS_NCTF	E61

OMIT_TABLE
CRITICAL

U1000
BGA
(8 OF 9)
SANDY-BRIDGE
MOBILE-2C-35W

A9	VSS	VSS	AM34
A13	VSS	VSS	AM38
A17	VSS	VSS	AM42
A21	VSS	VSS	AM45
A25	VSS	VSS	AM48
A28	VSS	VSS	AM58
A33	VSS	VSS	AN1
A37	VSS	VSS	AN21
A40	VSS	VSS	AN25
A45	VSS	VSS	AN28
A49	VSS	VSS	AN33
A53	VSS	VSS	AN36
AA1	VSS	VSS	AN40
AA8	VSS	VSS	AN43
AA13	VSS	VSS	AN47
AA50	VSS	VSS	AN50
AA51	VSS	VSS	AN54
AA52	VSS	VSS	AP7
AA53	VSS	VSS	AP10
AA55	VSS	VSS	AP51
AA56	VSS	VSS	AP55
AB16	VSS	VSS	AR7
AB18	VSS	VSS	AR13
AB21	VSS	VSS	AR17
AB48	VSS	VSS	AR21
AB61	VSS	VSS	AR41
AC6	VSS	VSS	AR48
AC10	VSS	VSS	AR61
AC14	VSS	VSS	AT4
AC46	VSS	VSS	AT14
AD4	VSS	VSS	AT19
AD17	VSS	VSS	AT36
AD20	VSS	VSS	AT45
AD61	VSS	VSS	AT52
AE8	VSS	VSS	AT58
AE13	VSS	VSS	AU1
AF1	VSS	VSS	AU7
AF17	VSS	VSS	AU11
AF21	VSS	VSS	AU28
AF47	VSS	VSS	AU32
AF48	VSS	VSS	AU51
AF50	VSS	VSS	AV17
AF51	VSS	VSS	AV21
AF52	VSS	VSS	AV22
AF53	VSS	VSS	AV34
AF55	VSS	VSS	AV40
AF56	VSS	VSS	AV48
AF58	VSS	VSS	AV55
AF59	VSS	VSS	AW7
AG7	VSS	VSS	AW13
AG10	VSS	VSS	AW43
AG14	VSS	VSS	AW61
AG18	VSS	VSS	AY4
AG47	VSS	VSS	AY9
AG52	VSS	VSS	AY14
AG61	VSS	VSS	AY19
AH4	VSS	VSS	AY30
AH58	VSS	VSS	AY36
AJ7	VSS	VSS	AY41
AJ13	VSS	VSS	AY45
AJ16	VSS	VSS	AY49
AJ20	VSS	VSS	AY55
AJ22	VSS	VSS	AY58
AJ26	VSS	VSS	BA1
AJ30	VSS	VSS	BA11
AJ34	VSS	VSS	BA17
AJ38	VSS	VSS	BA21
AJ42	VSS	VSS	BA26
AJ45	VSS	VSS	BA32
AJ48	VSS	VSS	BA48
AK1	VSS	VSS	BA51
AK52	VSS	VSS	BB53
AL10	VSS	VSS	BC5
AL13	VSS	VSS	BC13
AL17	VSS	VSS	BC57
AL21	VSS	VSS	BD8
AL25	VSS	VSS	BD12
AL28	VSS	VSS	BD16
AL33	VSS	VSS	BD19
AL36	VSS	VSS	BD23
AL40	VSS	VSS	BD27
AL43	VSS	VSS	BD32
AL47	VSS	VSS	BD36
AL61	VSS	VSS	BD40
AM4	VSS	VSS	BD44
AM13	VSS	VSS	BD48
AM20	VSS	VSS	BD52
AM22	VSS	VSS	BD56
AM26	VSS	VSS	BE5
AM30	VSS	VSS	BG9

PAGE TITLE
CPU GROUNDS

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DRAWING NUMBER 051-8871
SIZE D
REVISION 2.5.0
BRANCH
PAGE 14 OF 109
SHEET 13 OF 74

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

Processor Load Line : -2.9 mOhms

CPU VCORE DECOUPLING

Intel recommendation (Table 7-1): 16x 2.2uF, 12x 22uF, 3x 330uF

12 9 7 =PPVCORE_S0_CPU

CRITICAL C1600 2.2UF 20% 4V X5R 402
CRITICAL C1601 2.2UF 20% 4V X5R 402
CRITICAL C1602 2.2UF 20% 4V X5R 402
CRITICAL C1603 2.2UF 20% 4V X5R 402
CRITICAL C1604 2.2UF 20% 4V X5R 402
CRITICAL C1605 2.2UF 20% 4V X5R 402
CRITICAL C1606 2.2UF 20% 4V X5R 402
CRITICAL C1607 2.2UF 20% 4V X5R 402
CRITICAL C1608 2.2UF 20% 4V X5R 402
CRITICAL C1609 2.2UF 20% 4V X5R 402
CRITICAL C1610 2.2UF 20% 4V X5R 402
CRITICAL C1611 2.2UF 20% 4V X5R 402
CRITICAL C1612 2.2UF 20% 4V X5R 402
CRITICAL C1613 2.2UF 20% 4V X5R 402
CRITICAL C1614 2.2UF 20% 4V X5R 402
CRITICAL C1615 2.2UF 20% 4V X5R 402

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL C1655 22UF 20% 4V X5R 402
CRITICAL C1656 22UF 20% 4V X5R 402
CRITICAL C1657 22UF 20% 4V X5R 402
CRITICAL C1658 22UF 20% 4V X5R 402
CRITICAL C1659 22UF 20% 4V X5R 402
CRITICAL C1660 22UF 20% 4V X5R 402
CRITICAL C1661 22UF 20% 4V X5R 402
CRITICAL C1662 22UF 20% 4V X5R 402
CRITICAL C1663 22UF 20% 4V X5R 402
CRITICAL C1664 22UF 20% 4V X5R 402
CRITICAL C1665 22UF 20% 4V X5R 402
CRITICAL C1666 22UF 20% 4V X5R 402

PLACEMENT_NOTE (C1667-C1679):

PLACEMENT_NOTE (C1640-C1645):

C1680 270UF 20% 2V TANT CASE-B2-SM
C1681 270UF 20% 2V TANT CASE-B2-SM
C1682 270UF 20% 2V TANT CASE-B2-SM
C1683 270UF 20% 2V TANT CASE-B2-SM
C1679 270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):

Place on bottom side of U1000

12 10 9 7 =PP1V05_S0_CPU_VCCIO

C1684 1UF 10% 10V X5R 402
C1685 1UF 10% 10V X5R 402
C1686 1UF 10% 10V X5R 402
C1687 1UF 10% 10V X5R 402
C1688 1UF 10% 10V X5R 402
C1689 1UF 10% 10V X5R 402
C1690 1UF 10% 10V X5R 402
C1691 1UF 10% 10V X5R 402
C1692 1UF 10% 10V X5R 402
C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402
C1695 1UF 10% 10V X5R 402
C1696 1UF 10% 10V X5R 402

C1697 1UF 10% 10V X5R 402
C1698 1UF 10% 10V X5R 402
C1699 1UF 10% 10V X5R 402
C169A 1UF 10% 10V X5R 402
C169B 1UF 10% 10V X5R 402
C169C 1UF 10% 10V X5R 402
C169D 1UF 10% 10V X5R 402
C169E 1UF 10% 10V X5R 402
C169F 1UF 10% 10V X5R 402
C161A 1UF 10% 10V X5R 402
C161B 1UF 10% 10V X5R 402
C161C 1UF 10% 10V X5R 402
C161D 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):

Place near U1000 on bottom side

C161E 10UF 20% 6.3V CERM-X5R 0402-1
C161F 10UF 20% 6.3V CERM-X5R 0402-1
C162A 10UF 20% 6.3V CERM-X5R 0402-1
C162B 10UF 20% 6.3V CERM-X5R 0402-1
C162C 10UF 20% 6.3V CERM-X5R 0402-1
C162D 10UF 20% 6.3V CERM-X5R 0402-1
C162E 10UF 20% 6.3V CERM-X5R 0402-1
C167A 10UF 20% 6.3V CERM-X5R 0402-1
C167B 10UF 20% 6.3V CERM-X5R 0402-1
C167C 10UF 20% 6.3V CERM-X5R 0402-1

C167D 270UF 20% 2V TANT CASE-B2-SM
C167E 270UF 20% 2V TANT CASE-B2-SM
C167G 270UF 20% 2V TANT CASE-B2-SM
C167H 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603

=PP1V05_S0_CPU_VCCPQE 7 12

C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

Place near U1000 on top side

7 =PP1V8_S0_CPU_VCCPLL

R1600 0 5% 1/10W MF-LF 402

=PP1V8_S0_CPU_VCCPLL_R 7 12

C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402
C160Z 270UF 20% 2V TANT CASE-B2-SM

CPU VCCPLL Low pass filter

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2011

PAGE TITLE	CPU DECOUPLING-I
Apple Inc.	DRAWING NUMBER 051-8871 SIZE D
	REVISION 2.5.0
	BRANCH
	PAGE 16 OF 109
	SHEET 14 OF 74

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VAXG DECOUPLING

Graphics Load Line : -3.9 mOhms

Intel recommendation (section 6.3): 18x 1uF(9 no-stuff), 10x 104F(2 no-stuff), 8x 22uF(2 no stuff), 4x 470uF(2 no-stuff)

12 9 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R 402
CRITICAL C1701 1UF 10% 10V X5R 402
CRITICAL C1702 1UF 10% 10V X5R 402
CRITICAL C1703 1UF 10% 10V X5R 402
CRITICAL C1704 1UF 10% 10V X5R 402
CRITICAL C1705 1UF 10% 10V X5R 402
CRITICAL C1706 1UF 10% 10V X5R 402
CRITICAL C1707 1UF 10% 10V X5R 402
CRITICAL C1708 1UF 10% 10V X5R 402
CRITICAL C1709 1UF 10% 10V X5R 402
CRITICAL C1710 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1712 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1713 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1714 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1715 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL C1717 22UF 20% 6.3V X5R-CERM1 0603
CRITICAL C1718 22UF 20% 6.3V X5R-CERM1 0603
CRITICAL C1719 22UF 20% 6.3V X5R-CERM1 0603
CRITICAL C1720 22UF 20% 6.3V X5R-CERM1 0603
CRITICAL C1721 22UF 20% 6.3V X5R-CERM1 0603
CRITICAL C1722 22UF 20% 6.3V X5R-CERM1 0603

PLACEMENT_NOTE (C1723-C1724):

C1723 270UF 20% 2V TANT CASE-B2-SM
C1724 270UF 20% 2V TANT CASE-B2-SM
C1725 270UF 20% 2V TANT CASE-B2-SM

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.13): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

26 12 10 7 =PP1V5_S3_CPU_VCCDDR

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V CERM-X5R 0402-1
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V CERM-X5R 0402-1
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W ME 0603

=PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 3x 1uf, 3x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

12 7 =PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

C1768 270UF 20% 2V TANT CASE-B2-SM

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: CPU DECOUPLING-II

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DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

BRANCH

PAGE: 17 OF 109

SHEET: 15 OF 74

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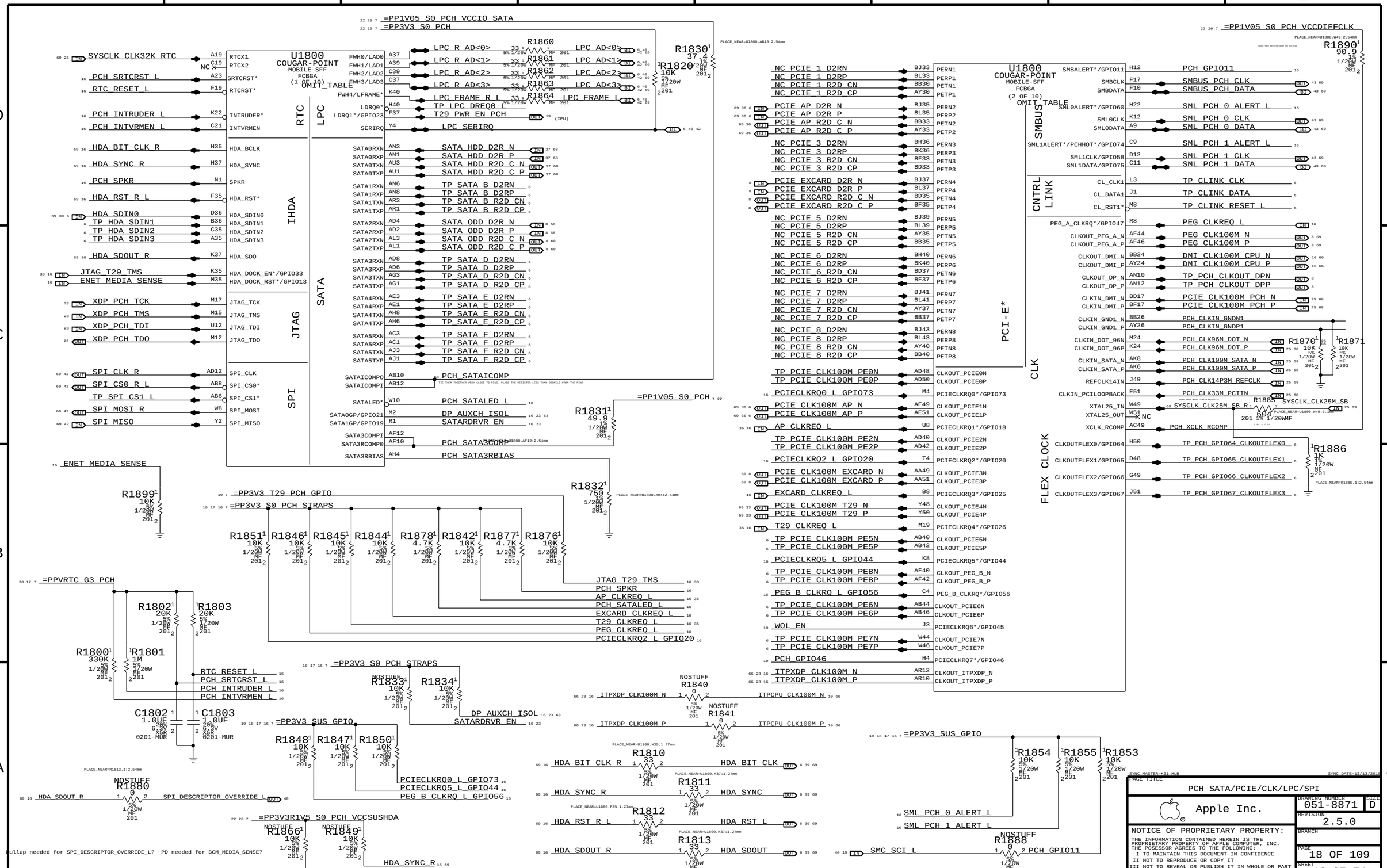

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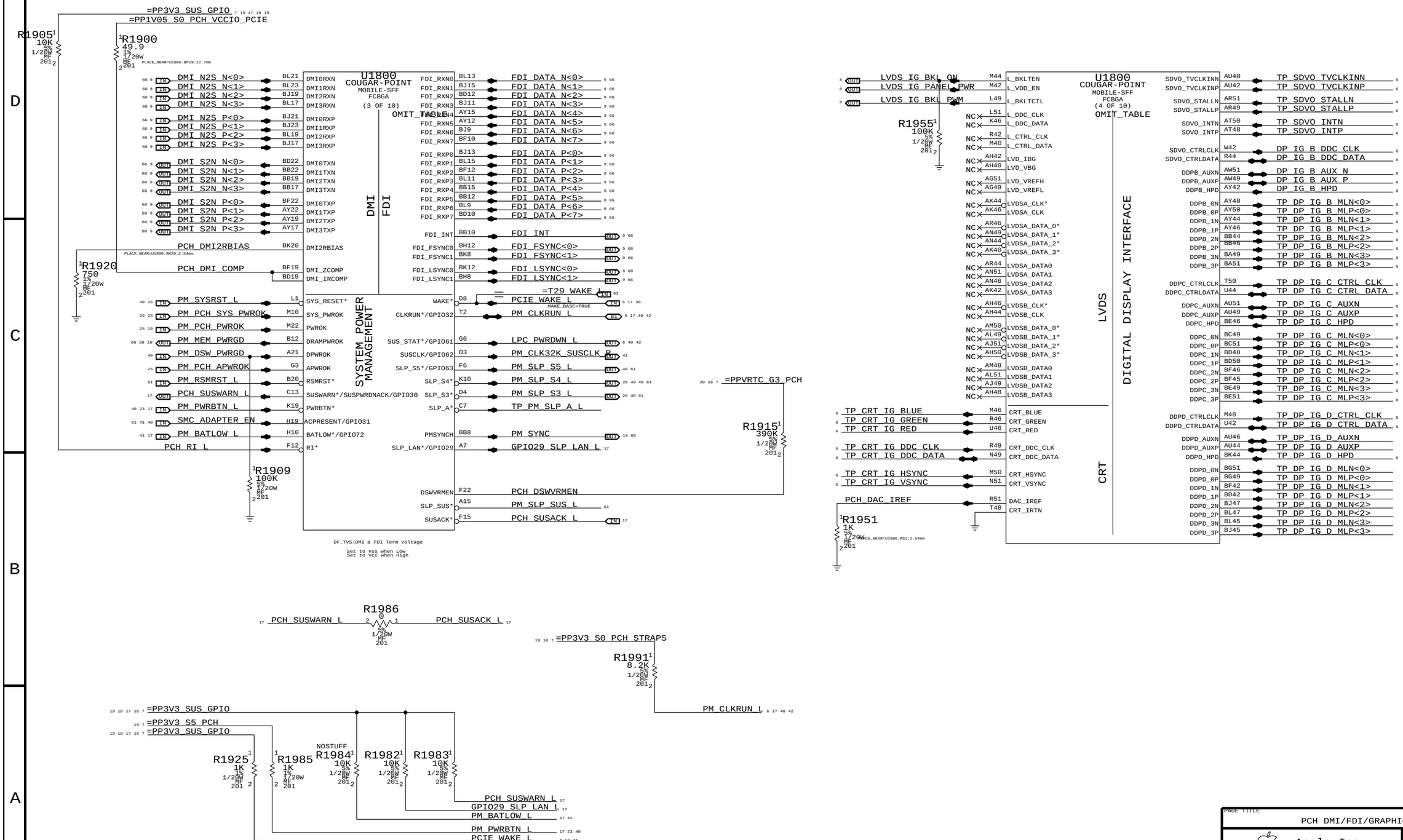

PAGE TITLE	PCH DMI/FDI/GRAPHICS
Apple Inc.	DRAWING NUMBER 051-8871 SIZE D
	REVISION 2.5.0
	BRANCH
	PAGE 19 OF 109
	SHEET 17 OF 74

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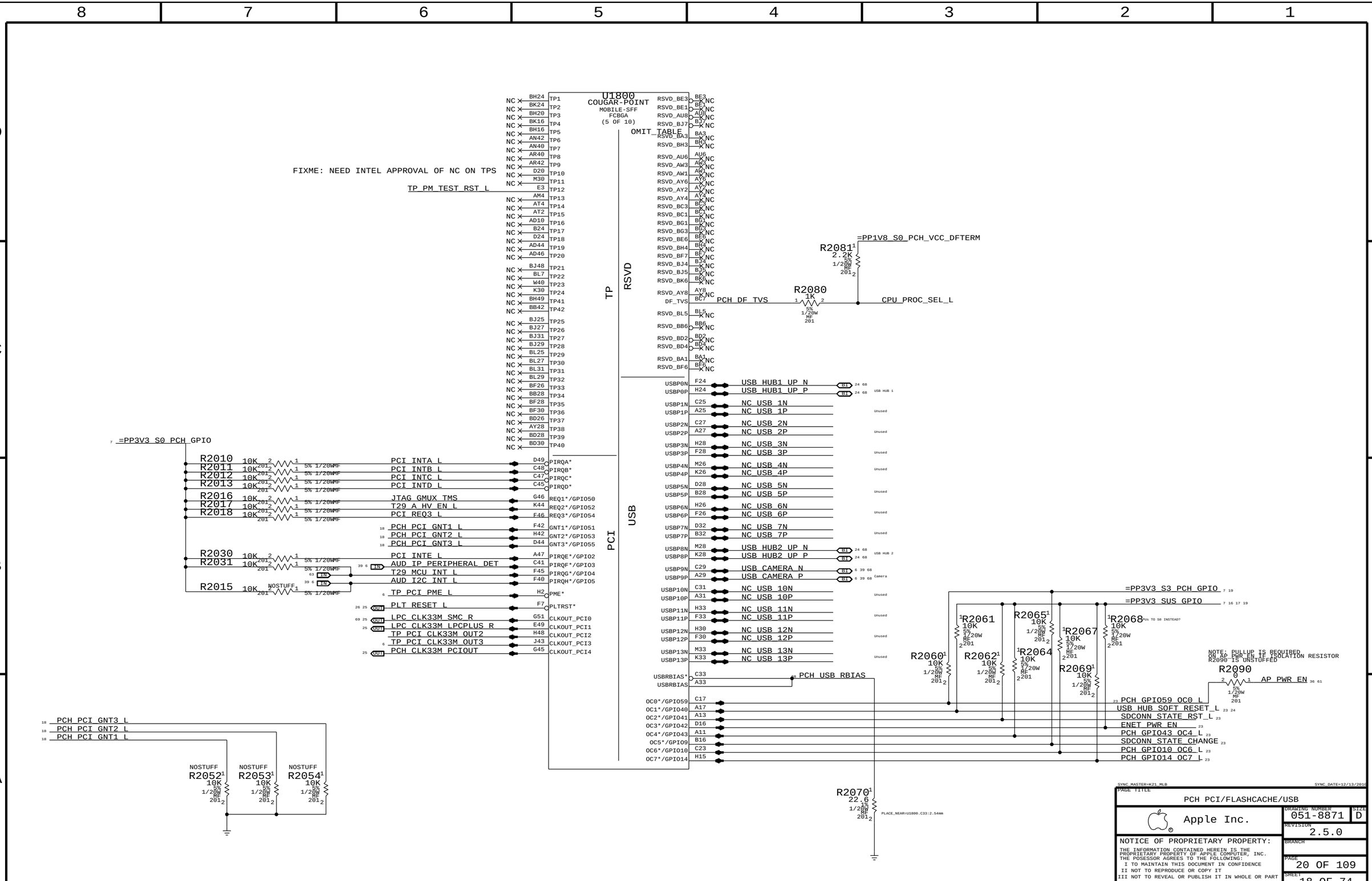

PAGE TITLE	PCH PCI/FLASHCACHE/USB
Apple Inc.	DRAWING NUMBER 051-8871 SIZE D
	REVISION 2.5.0
	BRANCH
	PAGE 20 OF 109
	SHEET 18 OF 74

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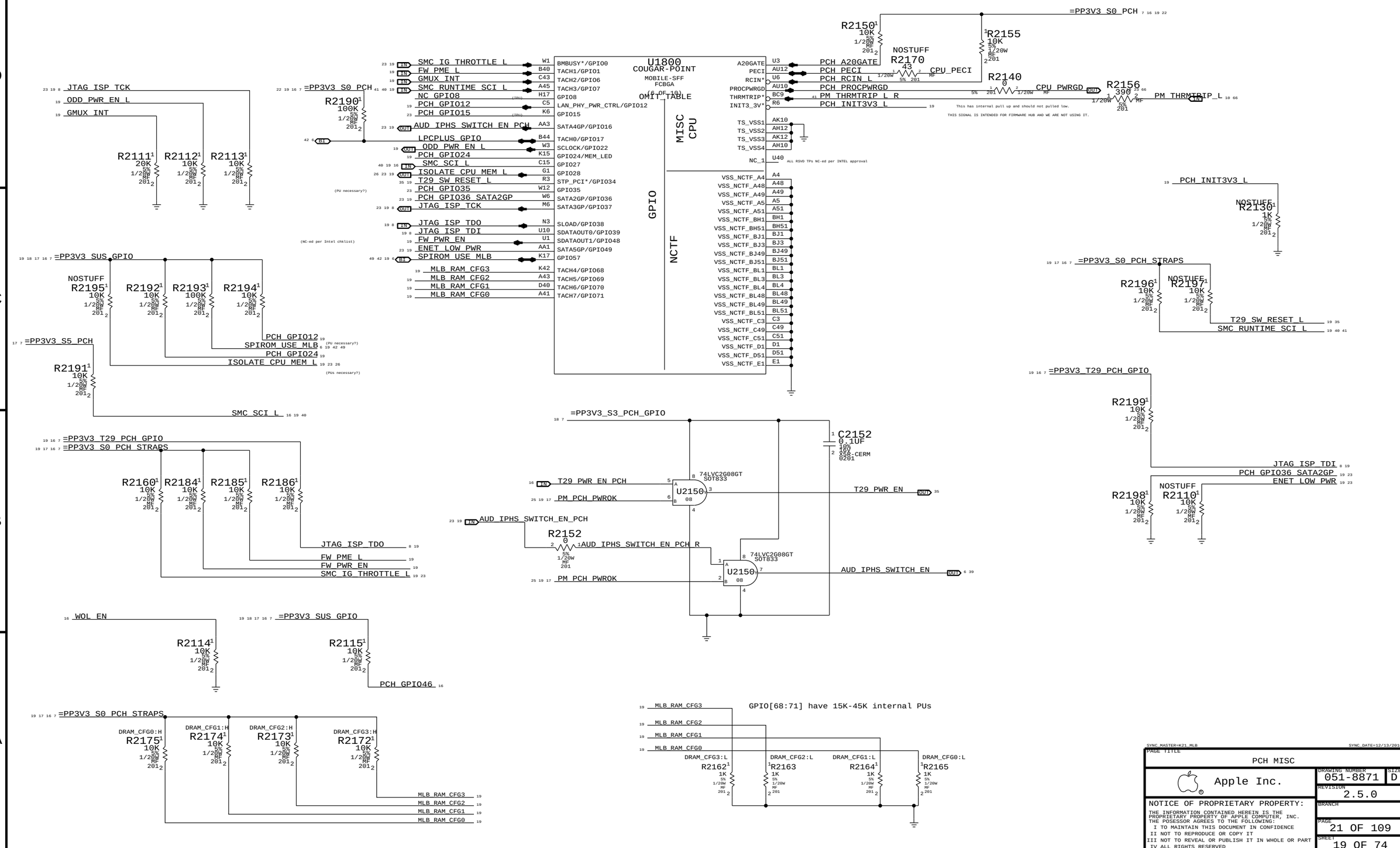

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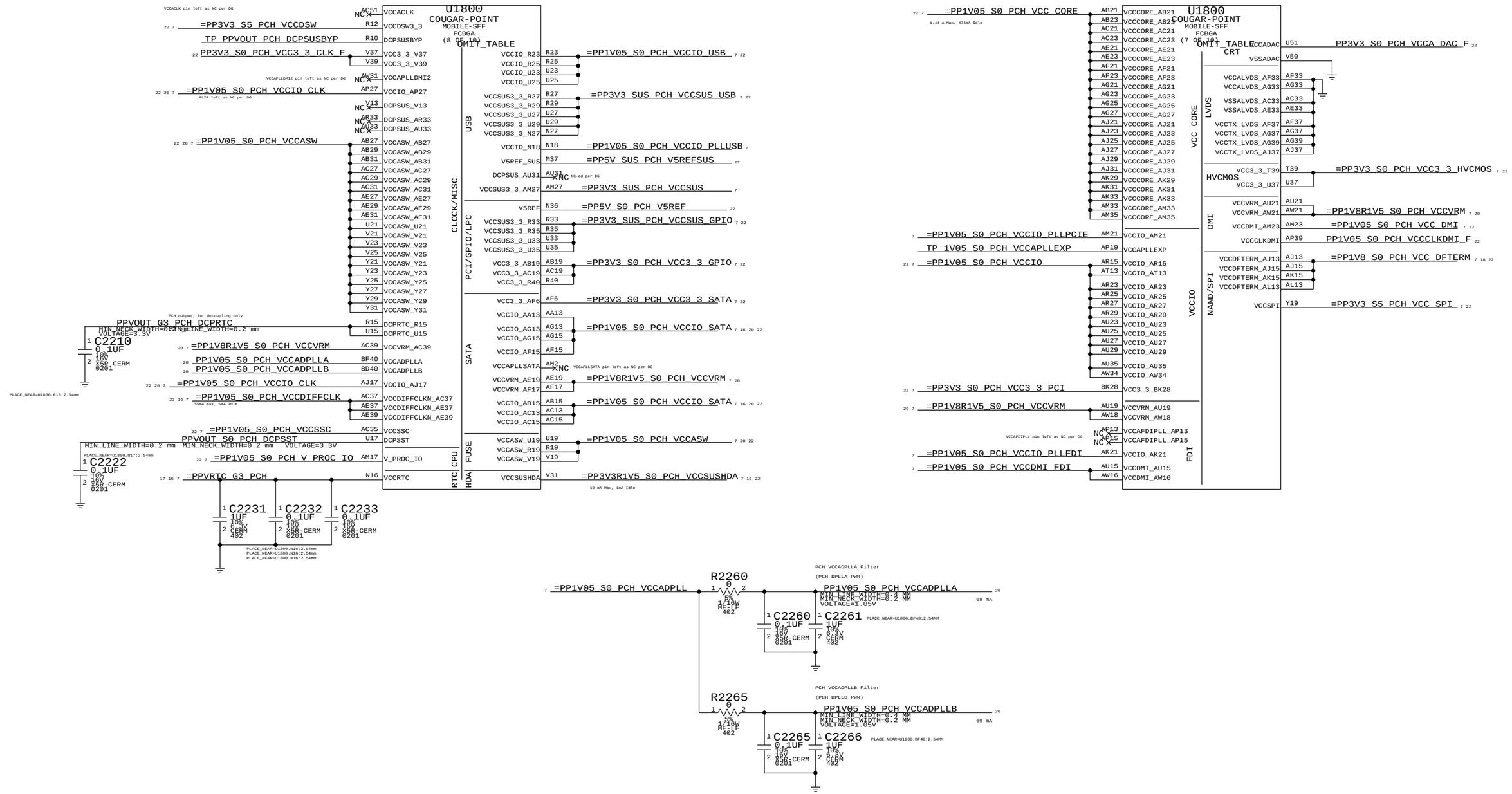

PAGE TITLE
PCH POWER

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
BRANCH
PAGE 22 OF 109
SHEET 20 OF 74

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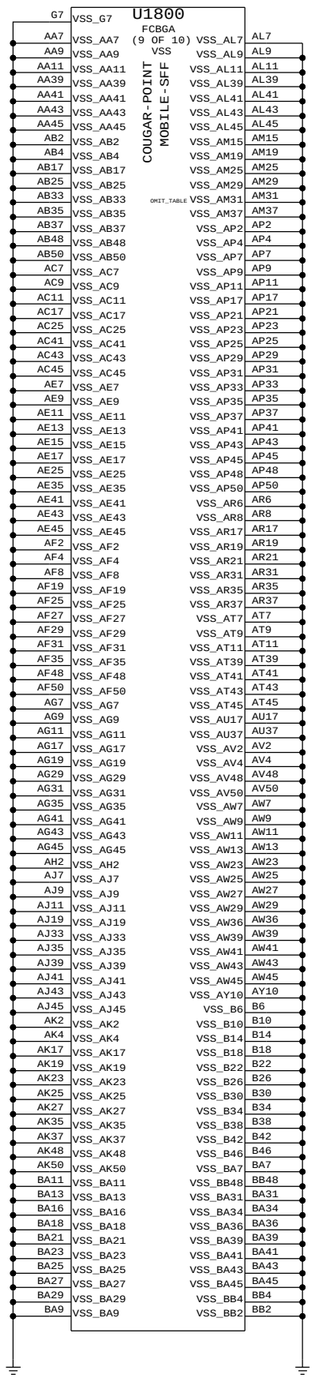

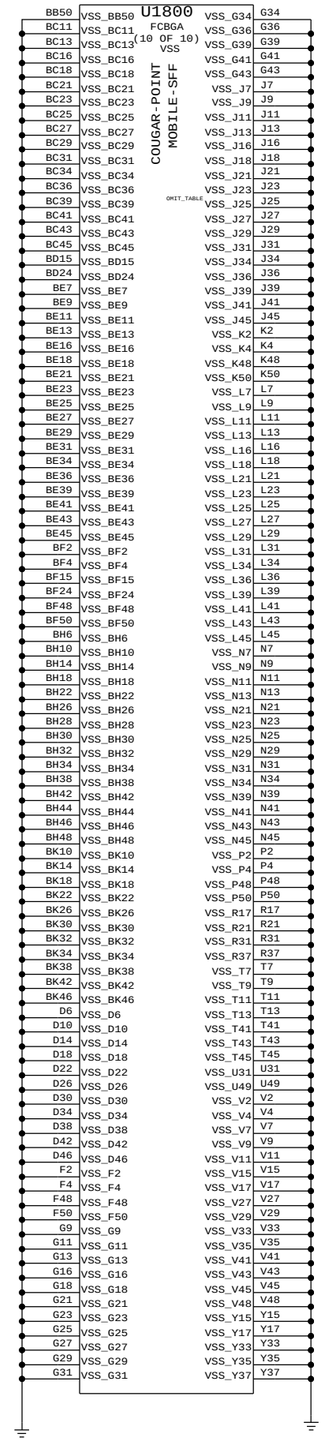

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

PCH GROUNDS

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PAGE 23 OF 109

SHEET 21 OF 74

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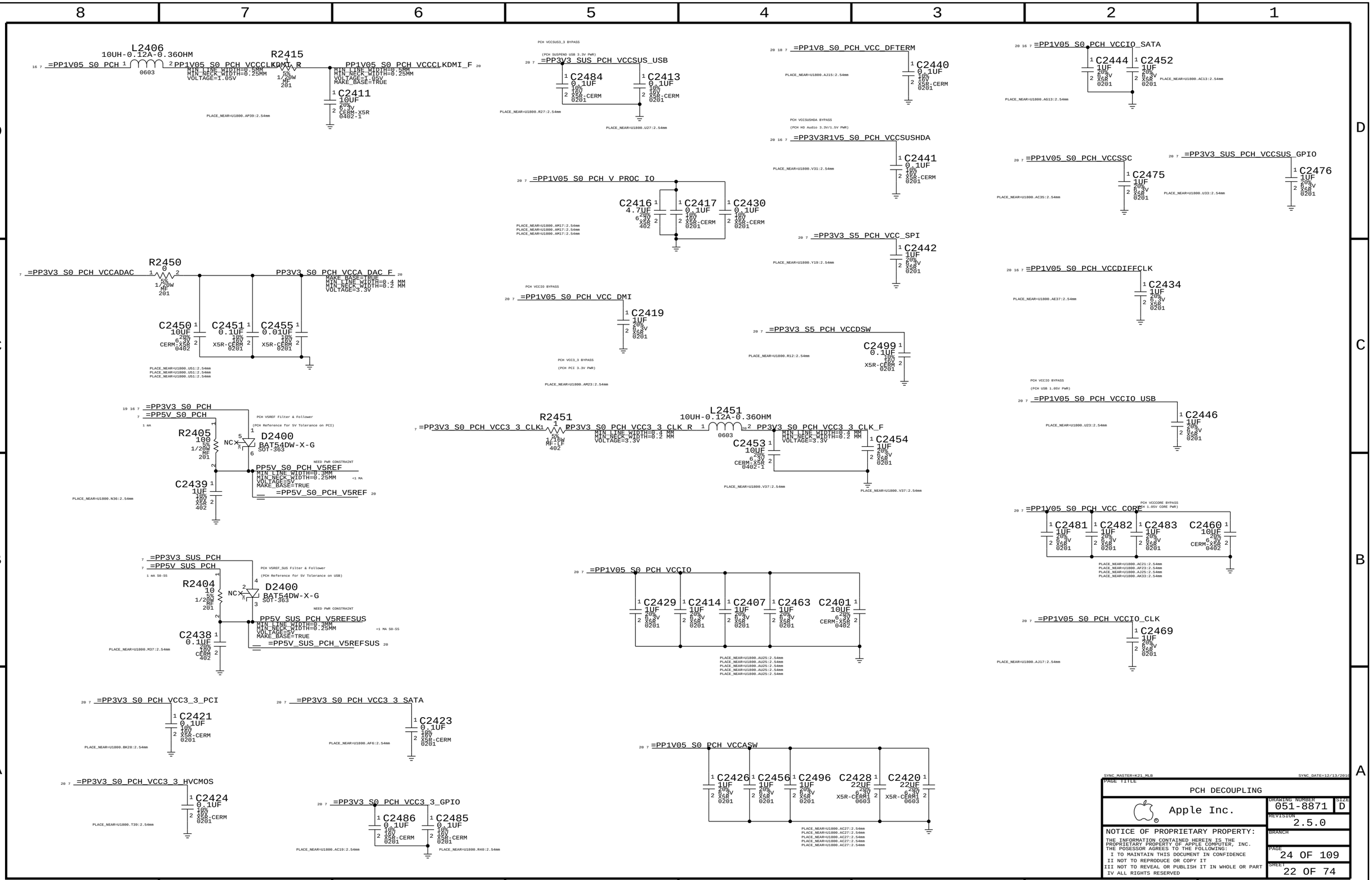

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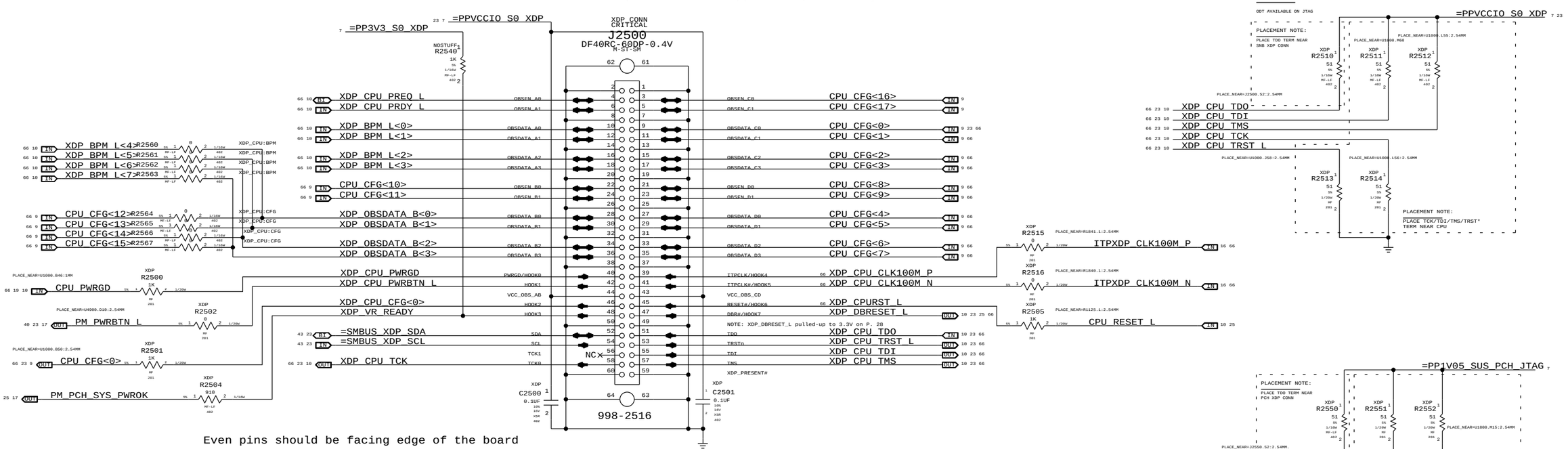
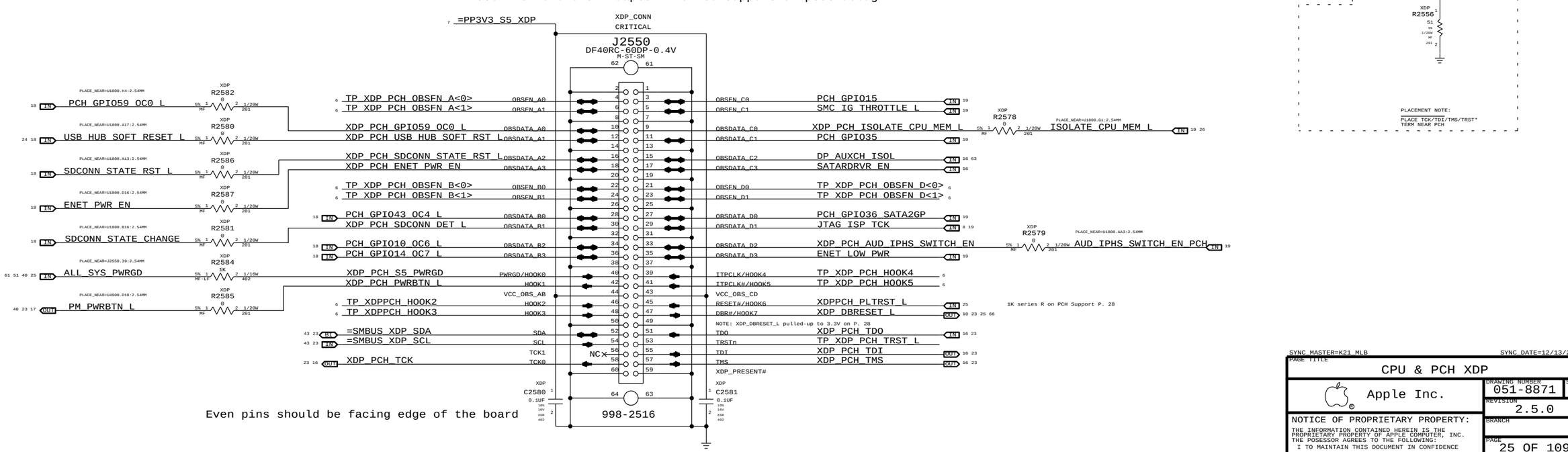
PROCESSOR MICRO2-XDP CONNECTOR

NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug



PCH MICRO2-XDP CONNECTOR

NOTE: This is not the standard XDP pinout
Use with 920-0782 Adapter Flex to support chipset debug



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2016

PAGE TITLE	CPU & PCH XDP
Apple Inc.	DRAWING NUMBER 051-8871 SIZE D
	REVISION 2.5.0
	BRANCH
	PAGE 25 OF 109
	SHEET 23 OF 74

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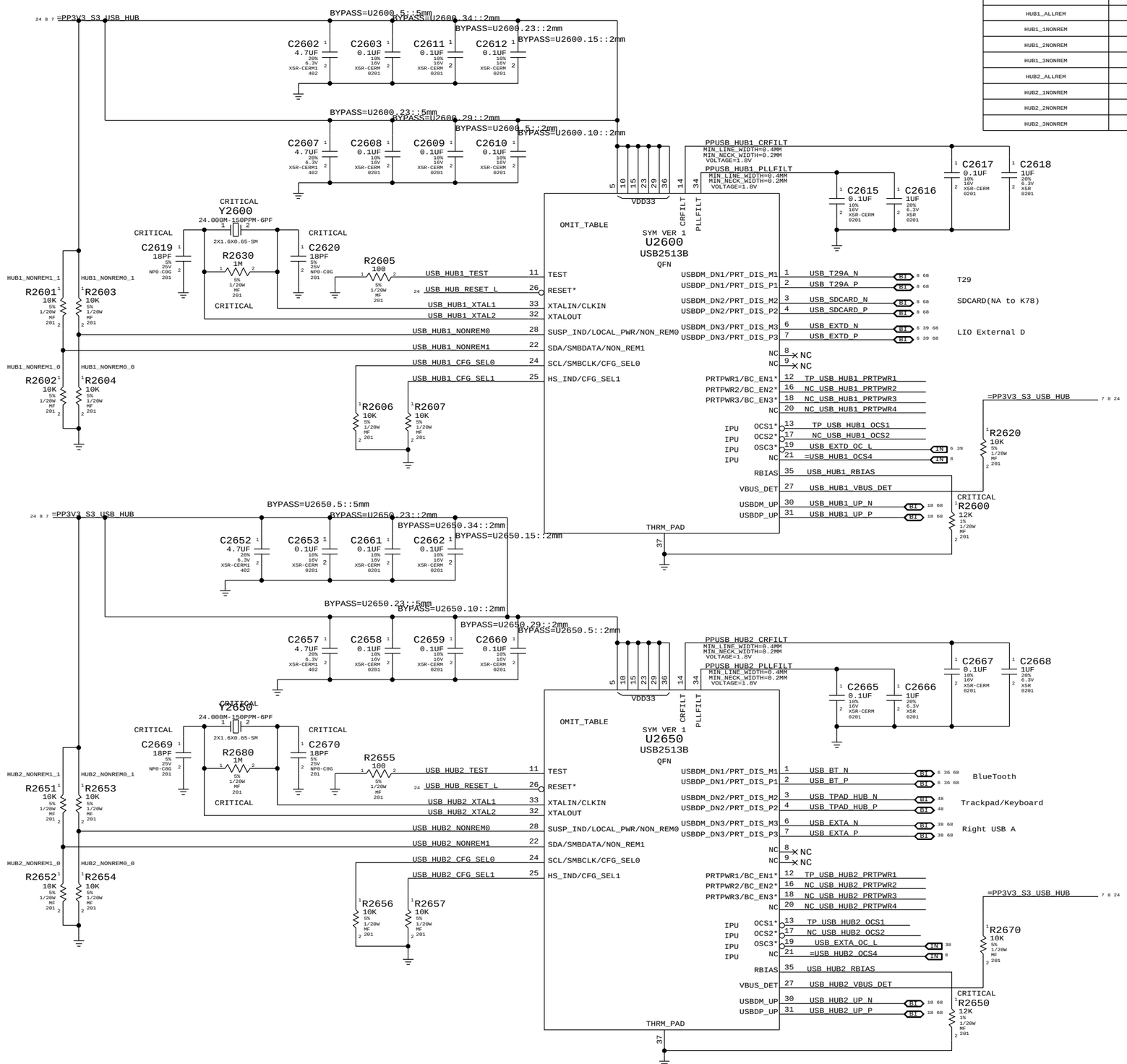
BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B



SYNC MASTER=K21_MLB SYNC DATE=12/13/2010

PAGE TITLE

USB HUBS

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REVISION 2.5.0

BRANCH

PAGE 26 OF 109

SHEET 24 OF 74

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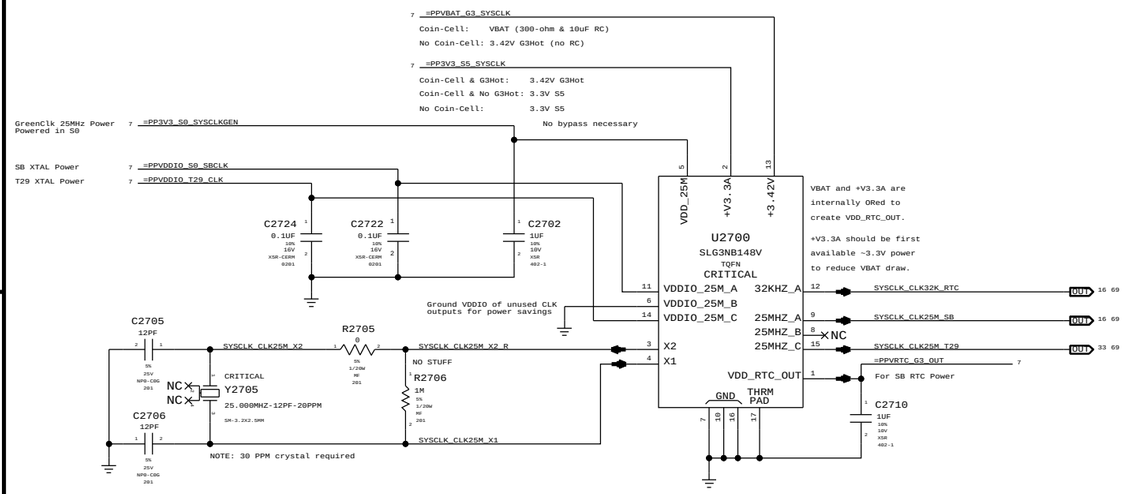
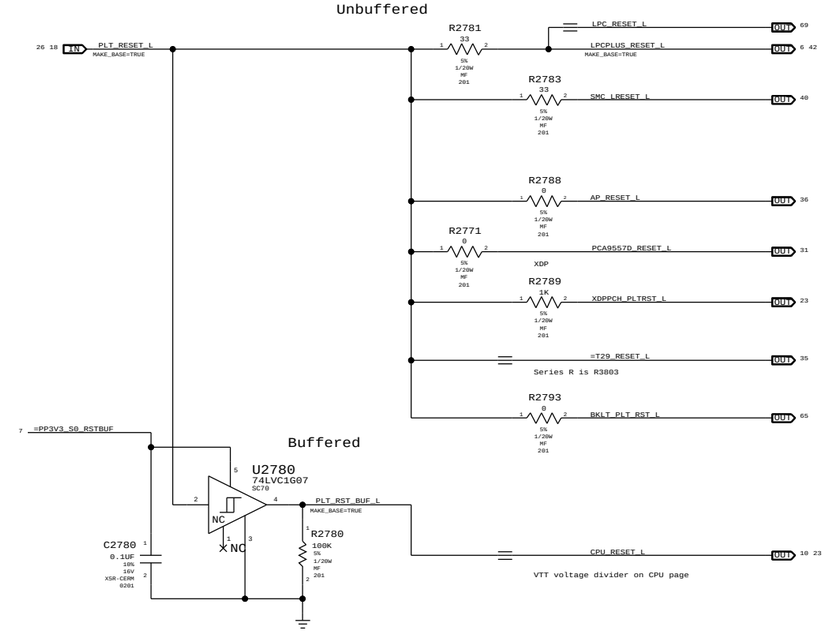
System RTC Power Source & 32kHz / 25MHz Clock Generator

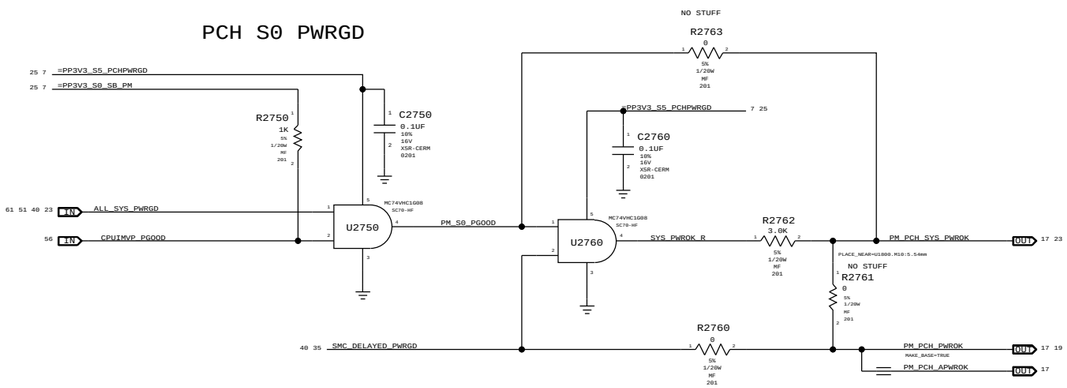


Platform Reset Connections

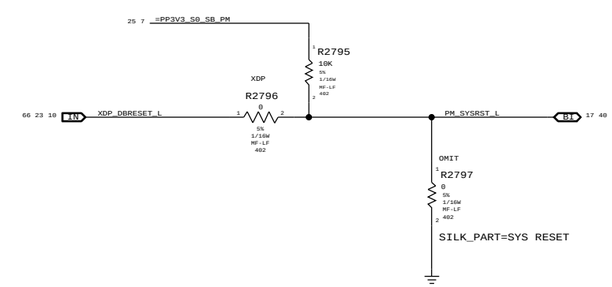
Unbuffered



PCH S0 PWRGD

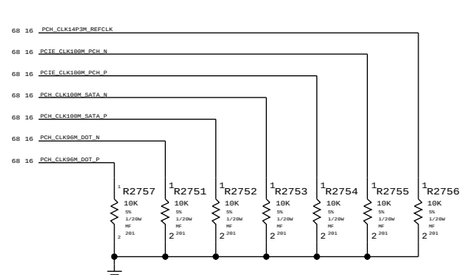


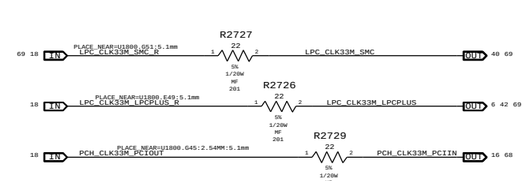
PCH Reset Button



CLOCK (CK505)

UNUSED clock terminations for FCIM MODE





SYNC_MASTER=K21_MLB SYNC_DATE=11/30/201

PAGE TITLE

Clock (CK505) and Chipset Support

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DRAWING NUMBER 051-8871 SIZE D

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PAGE 27 OF 109

SHEET 25 OF 74

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The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

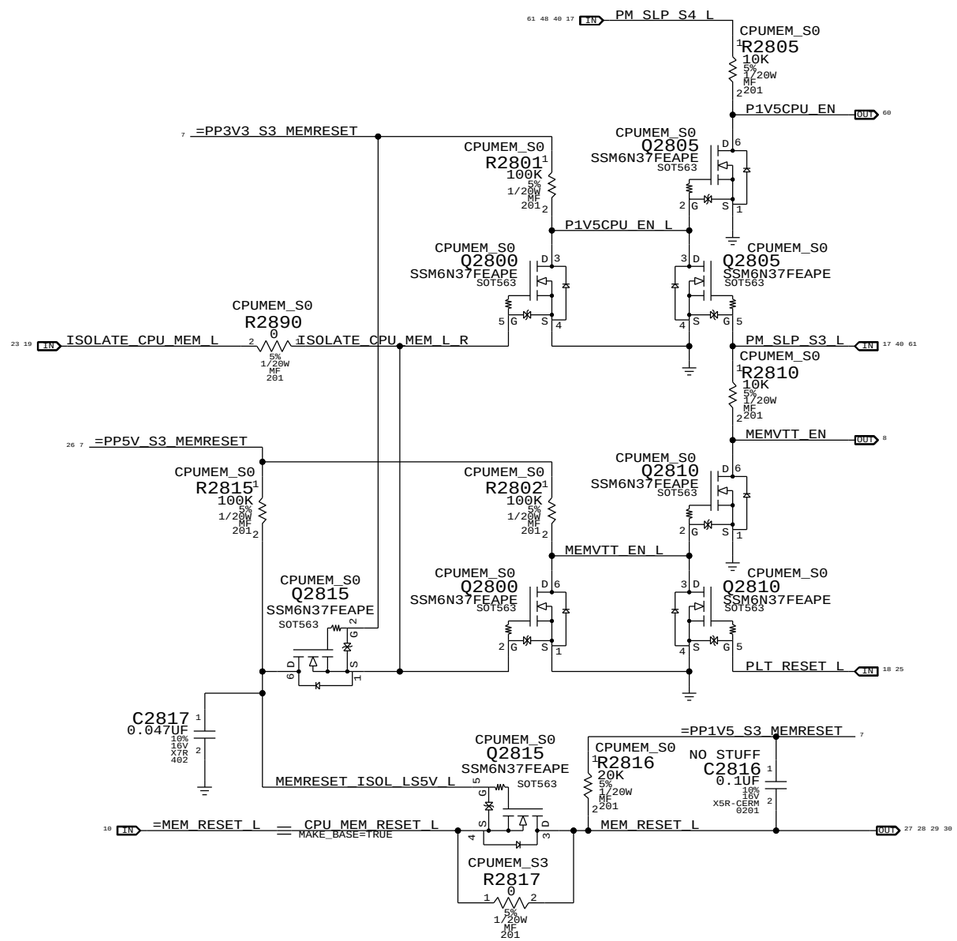
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

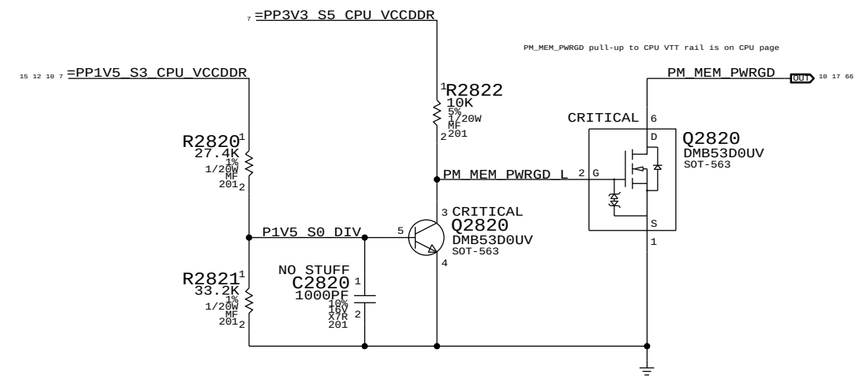
P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

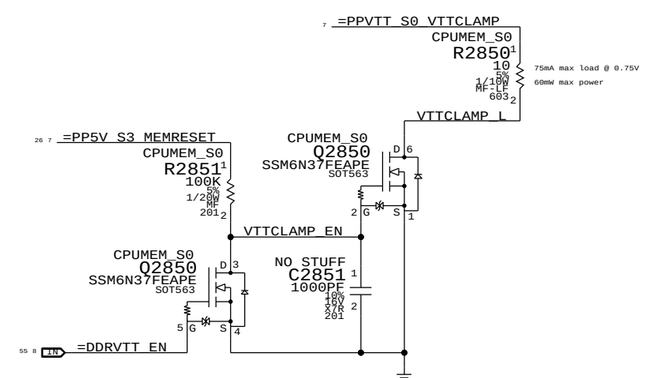


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
S3	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

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PAGE: 28 OF 109

SHEET: 26 OF 74

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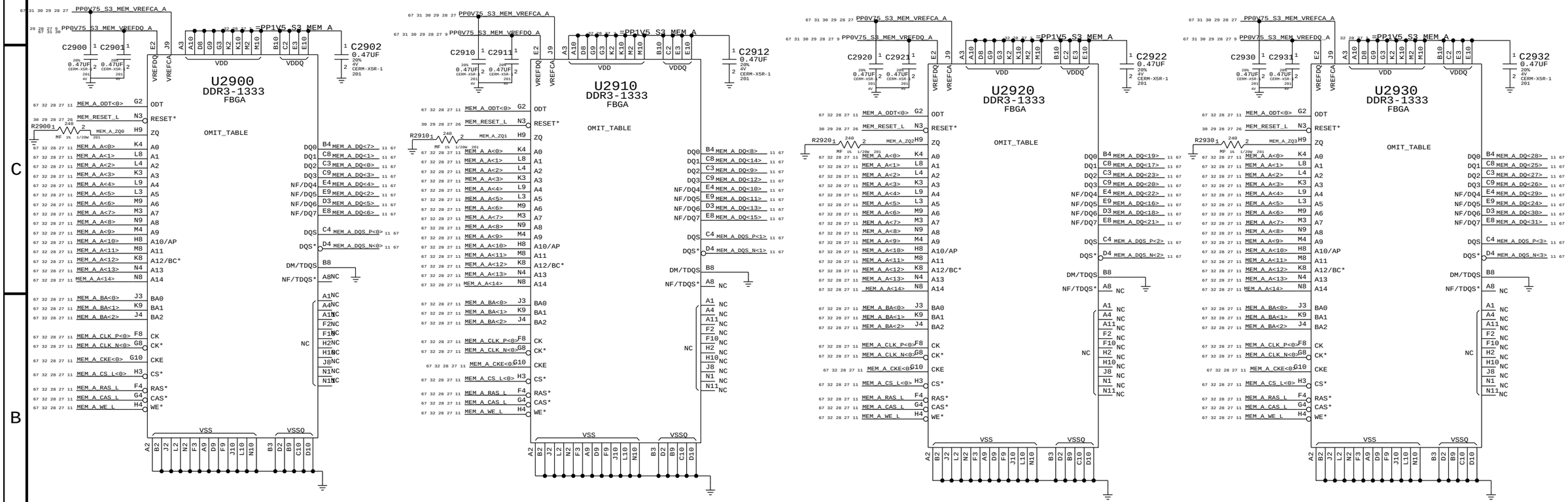

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
DDR3 DRAM CHANNEL A (0-31)

Apple Inc.

DRAWING NUMBER 051-8871
SIZE D
REVISION 2.5.0
BRANCH
PAGE 29 OF 109
SHEET 27 OF 74

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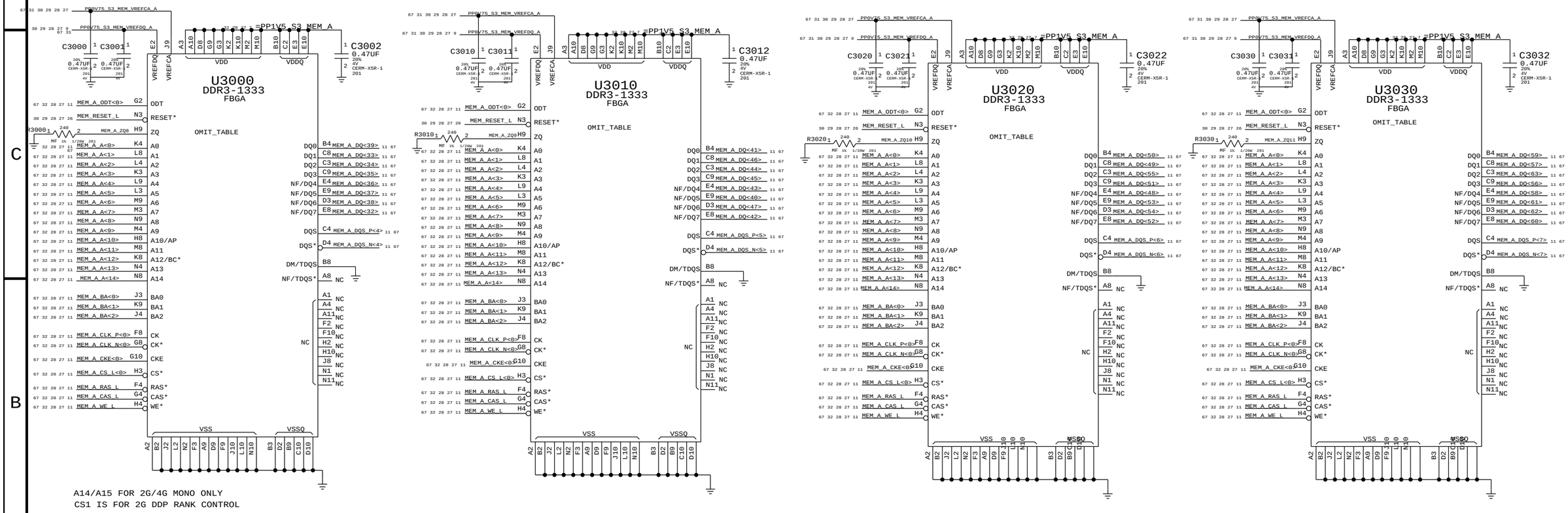

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
DDR3 DRAM CHANNEL A (32-63)

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BRANCH

PAGE 30 OF 109

SHEET 28 OF 74

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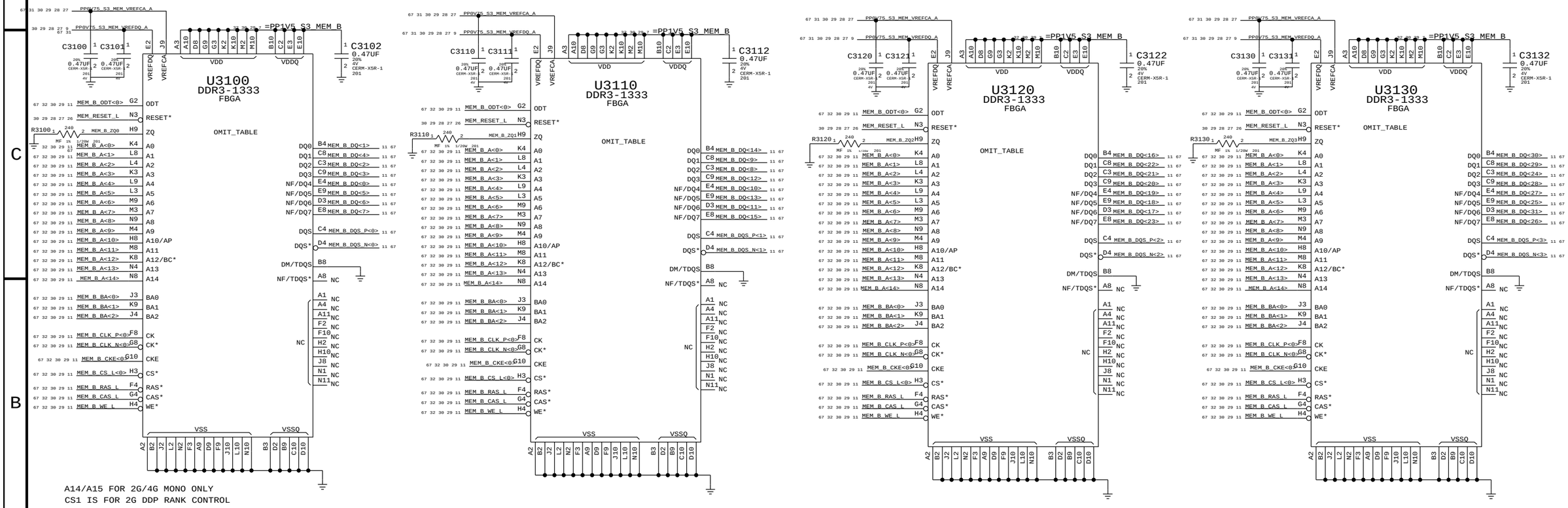

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

DDR3 DRAM CHANNEL B (0-31)

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PAGE 31 OF 109

SHEET 29 OF 74

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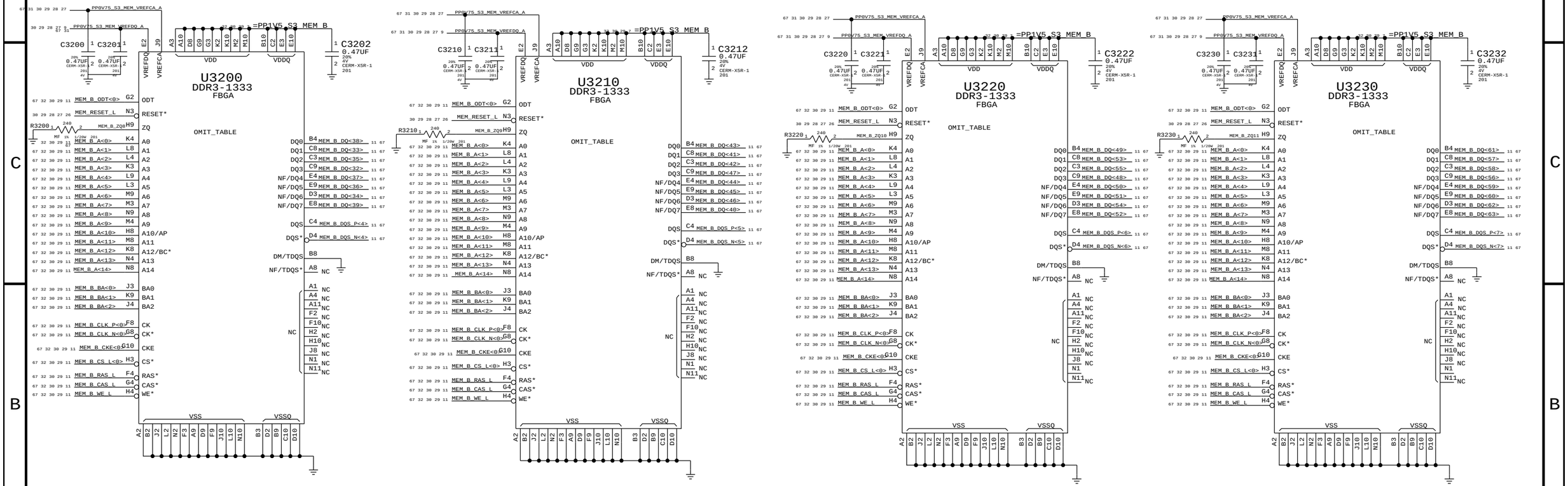

A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2011

PAGE TITLE
DDR3 DRAM CHANNEL B (32-63)

Apple Inc.

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REVISION 2.5.0
BRANCH
PAGE 32 OF 109
SHEET 30 OF 74

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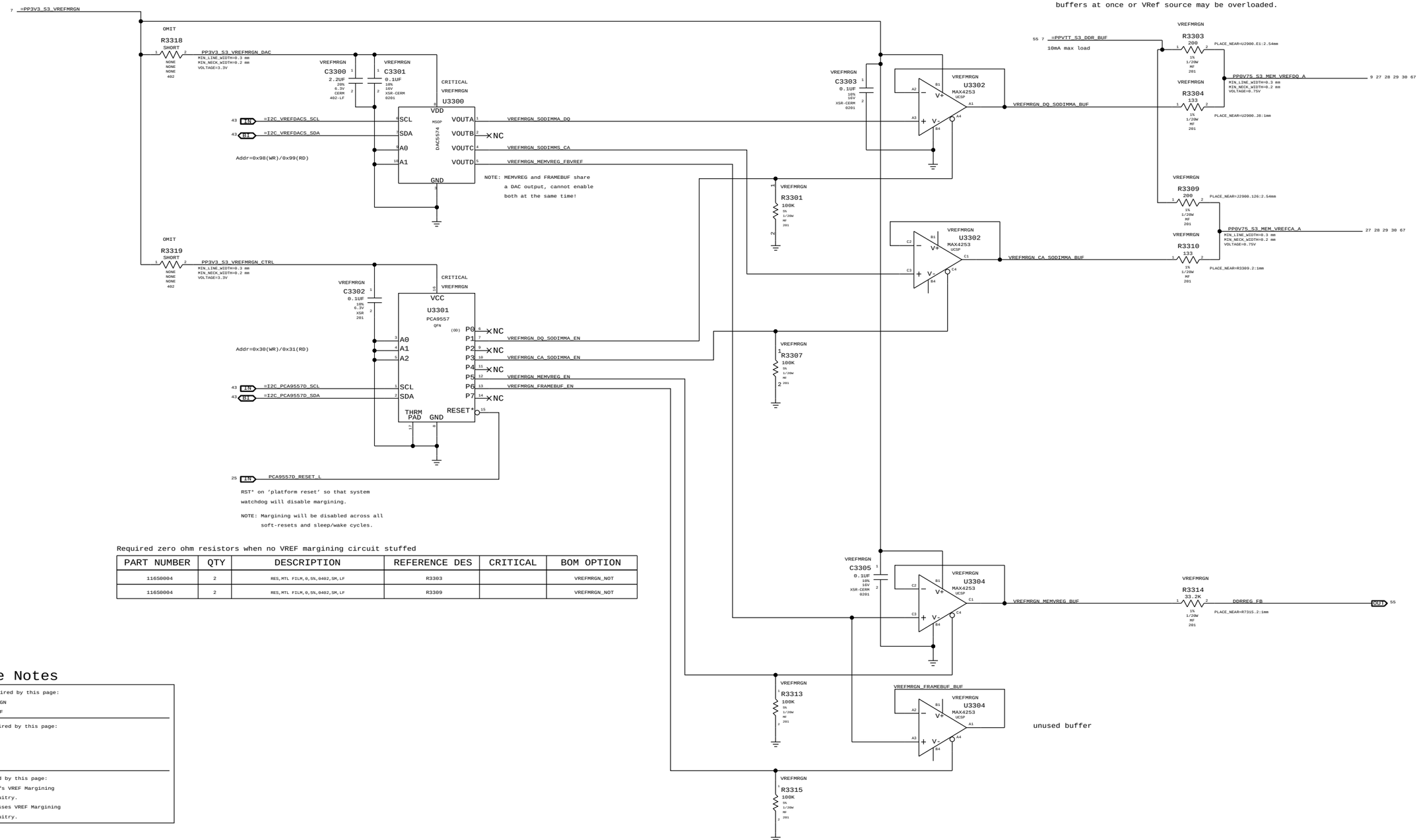

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2011

PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
BRANCH
PAGE 33 OF 109
SHEET 31 OF 74

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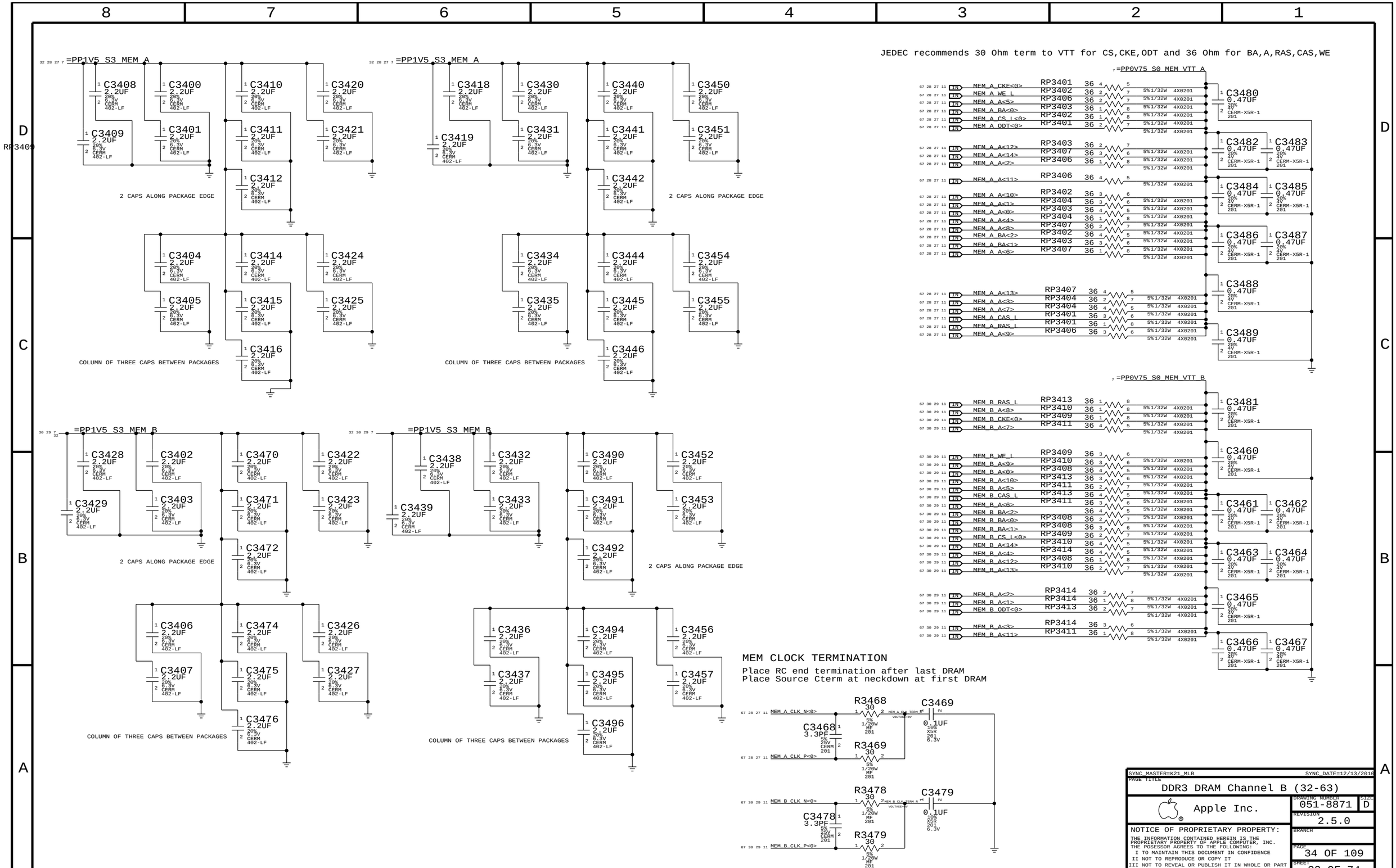

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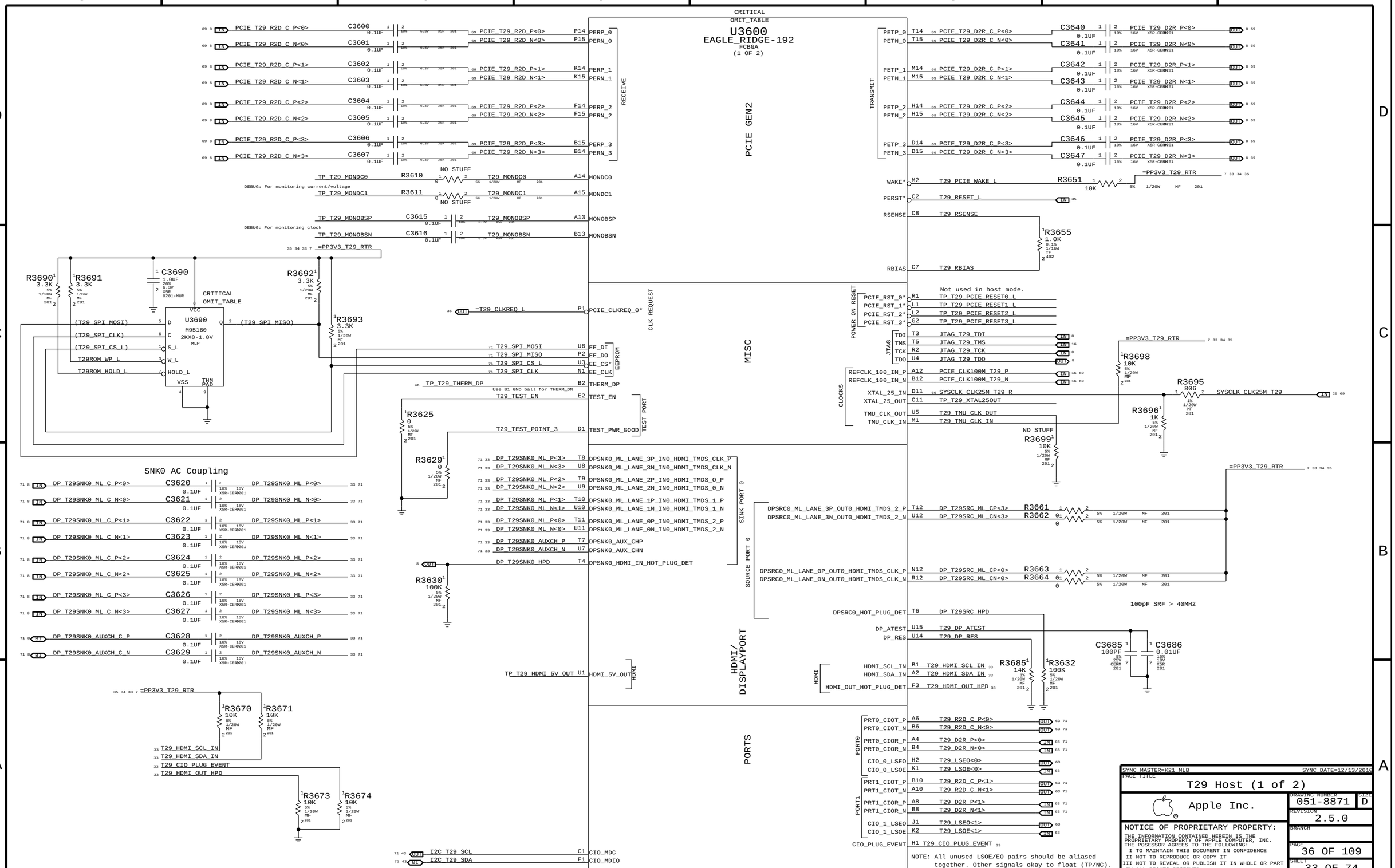

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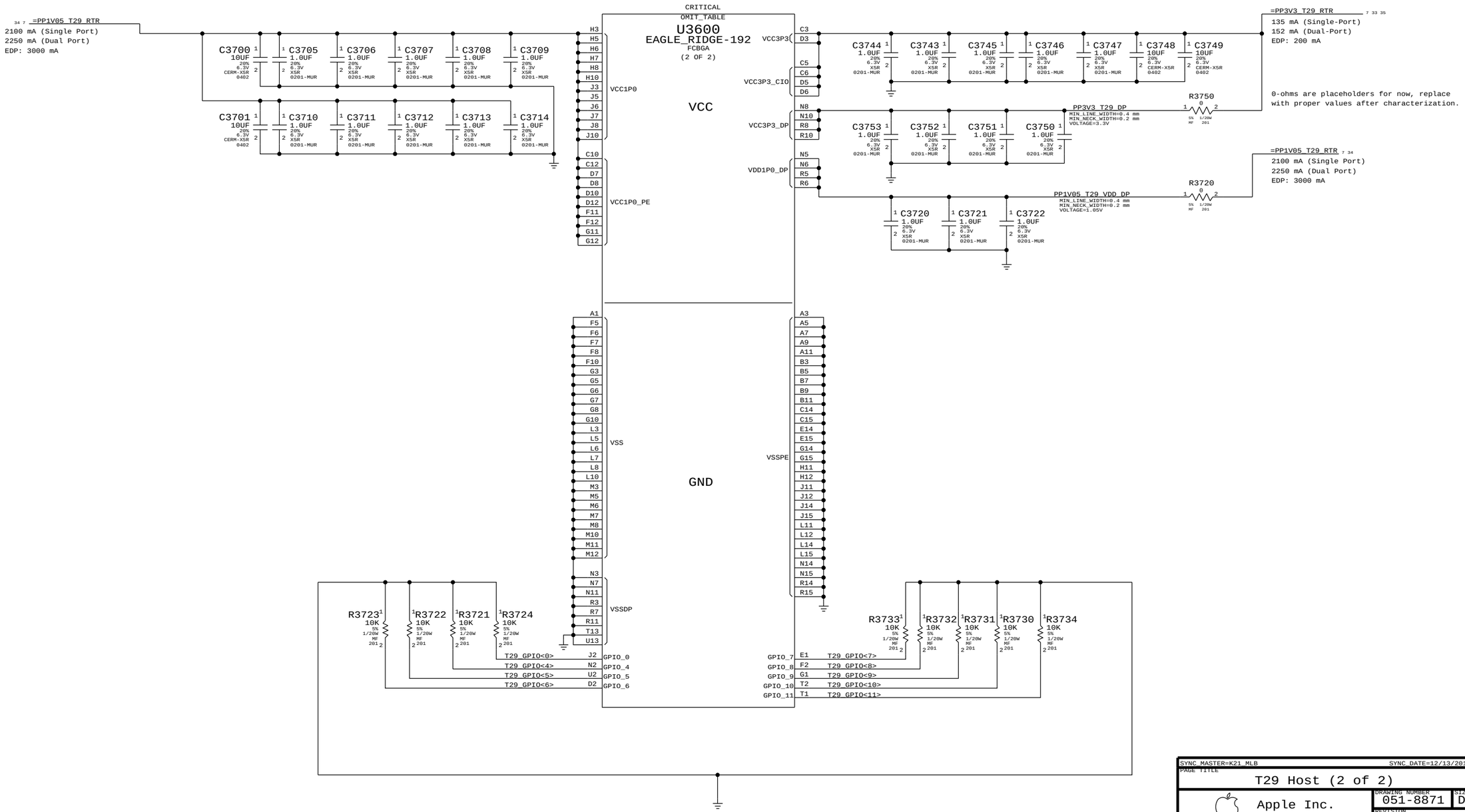

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: T29 Host (2 of 2)

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DRAWING NUMBER: 051-8871 SIZE: D

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PAGE: 37 OF 109

SHEET: 34 OF 74

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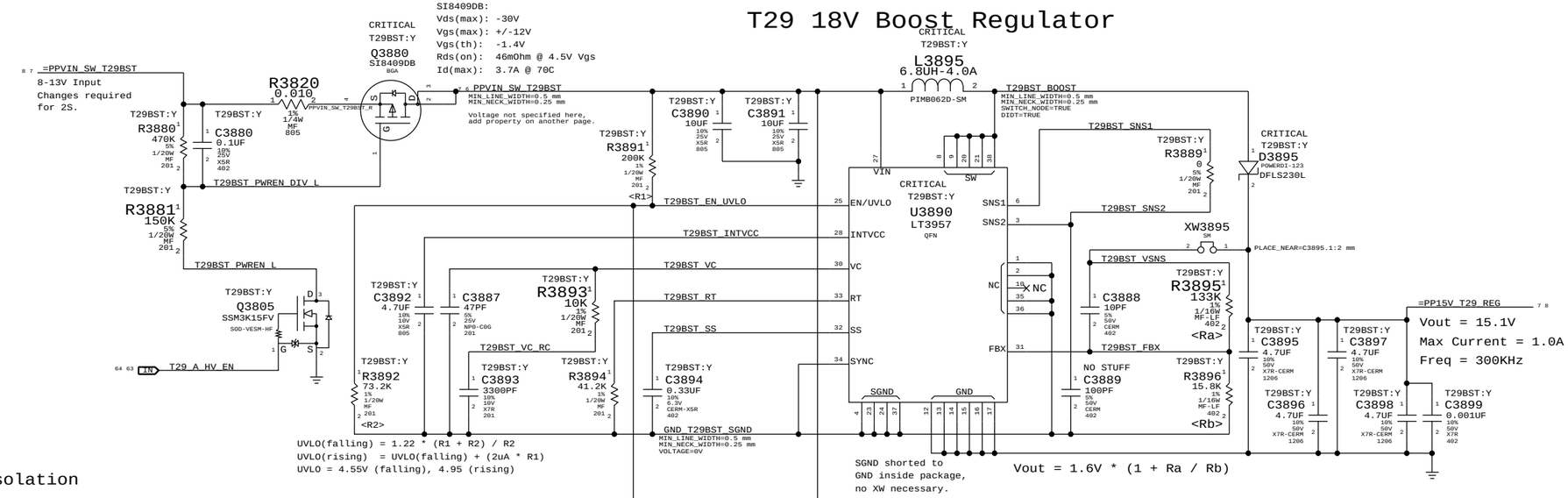
Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

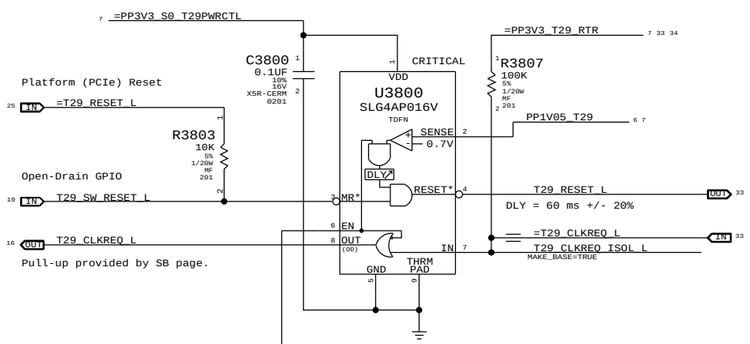
Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

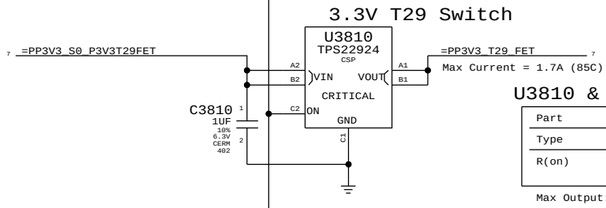
T29 18V Boost Regulator



Supervisor & CLKREQ# Isolation



3.3V T29 Switch

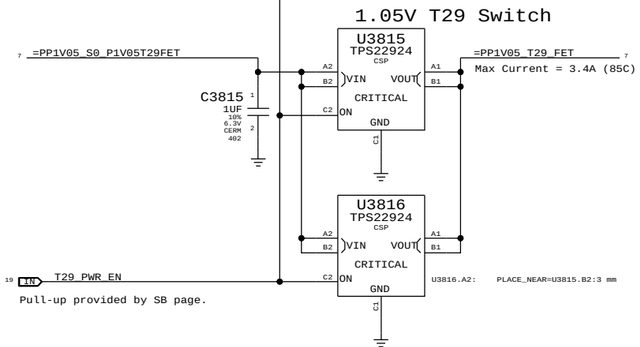


U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: T29 Power Support

Apple Inc.

DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

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PAGE: 38 OF 109

SHEET: 35 OF 74

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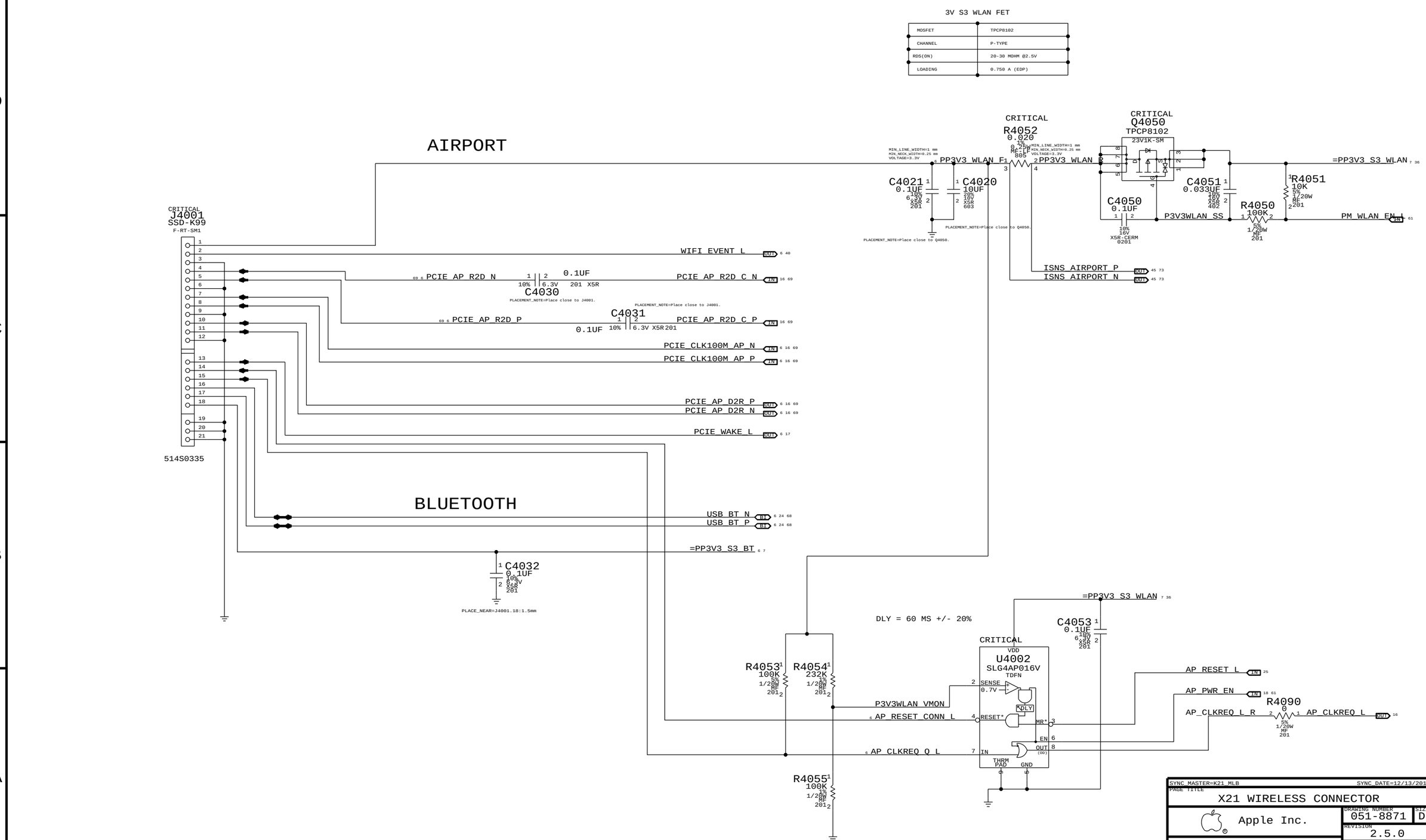

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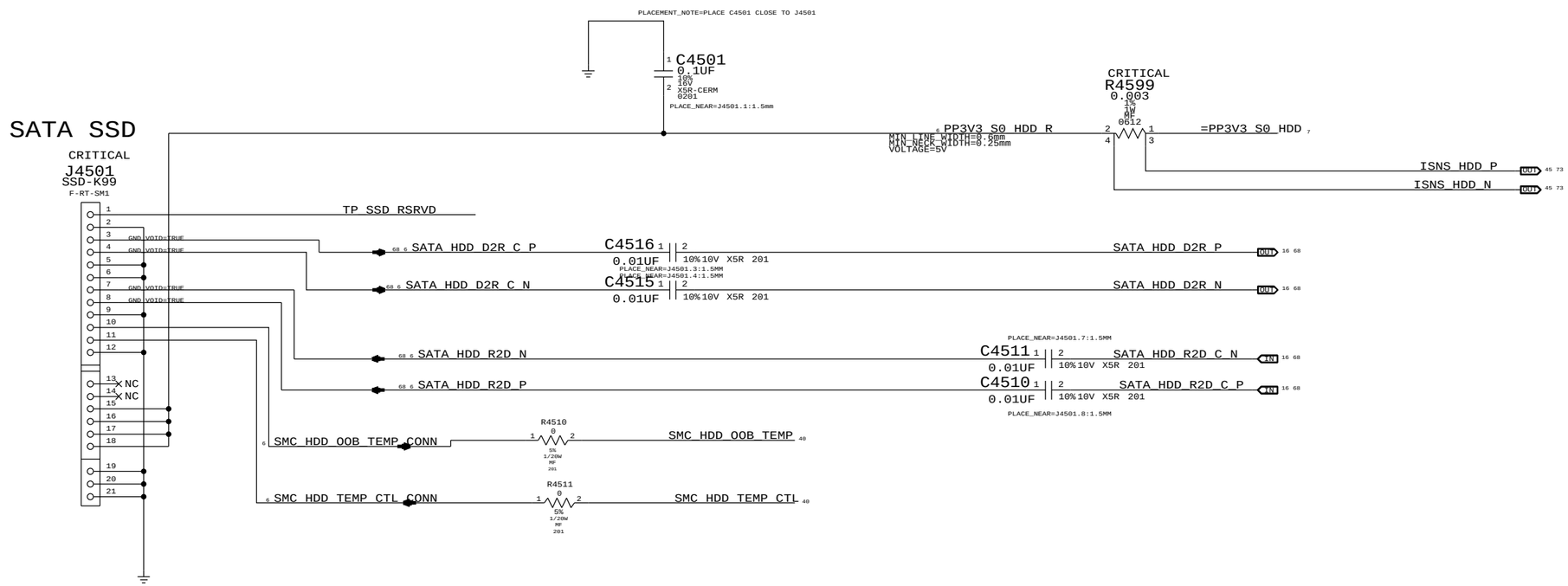

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SATA CONNECTOR

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PAGE 45 OF 109

SHEET 37 OF 74

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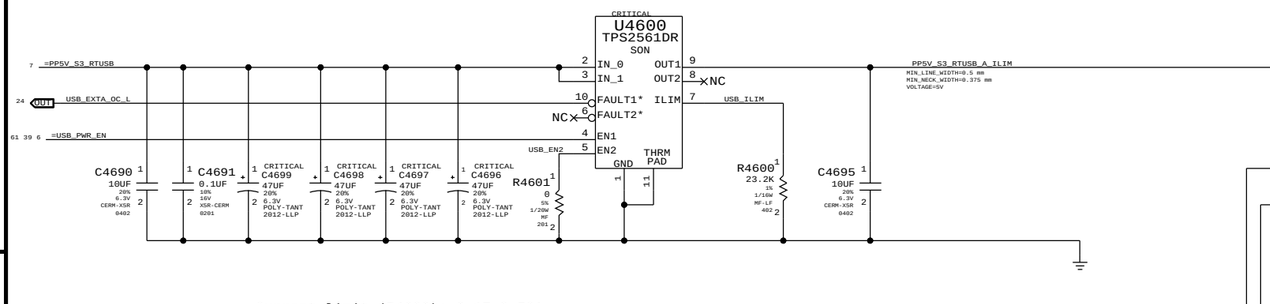
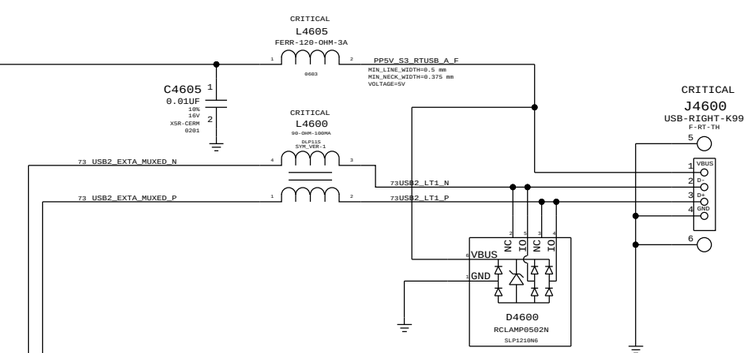
USB Port Power Switch



Current limit (R4600): 2.17-2.59A

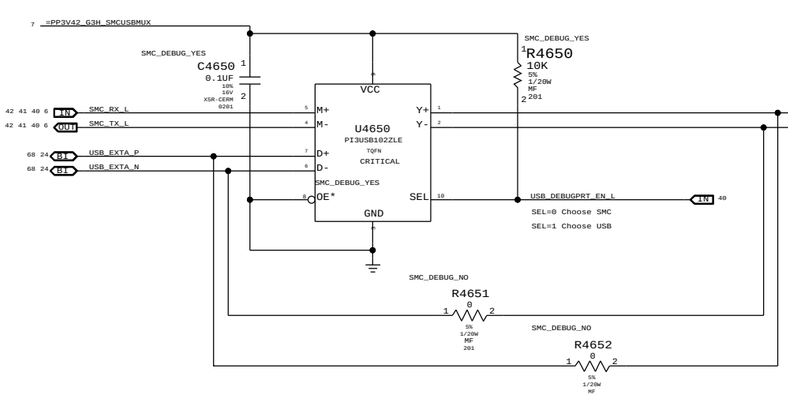
Right USB Port A



We can add protection to 5V if we want, but leaving NC for now

Place L4605 at connector pin

USB/SMC Debug Mux



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External USB Connectors

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SHEET 38 OF 74

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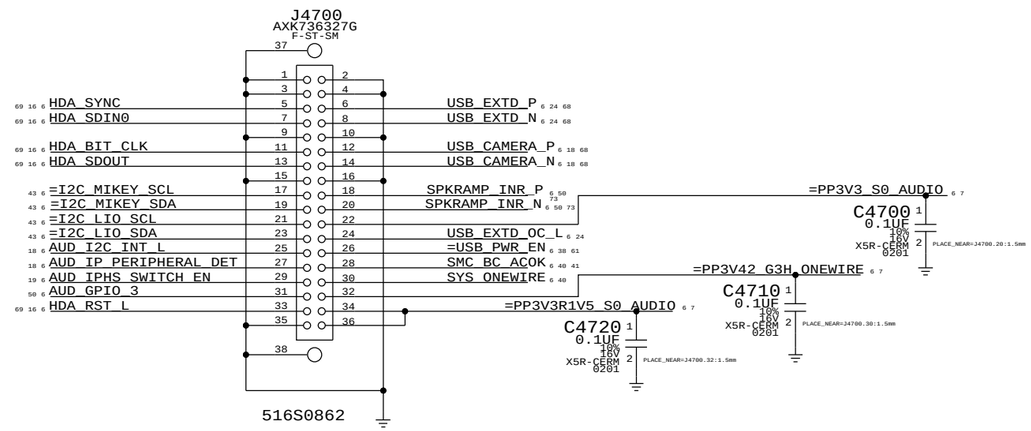
LIO CONNECTOR



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PAGE TITLE
LIO CONNECTORS

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PAGE 47 OF 109

SHEET 39 OF 74

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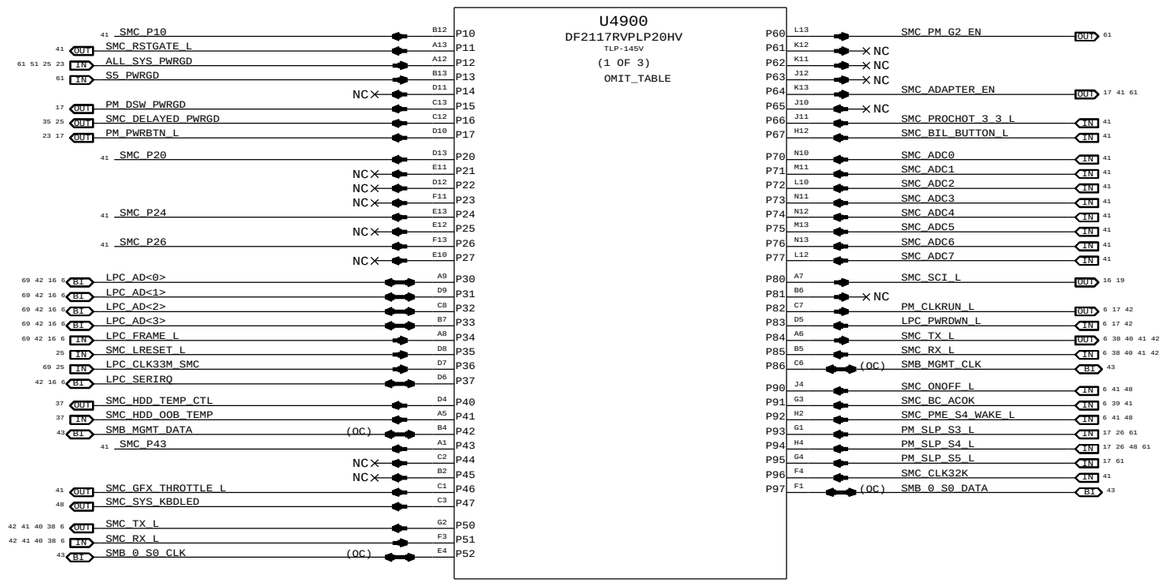
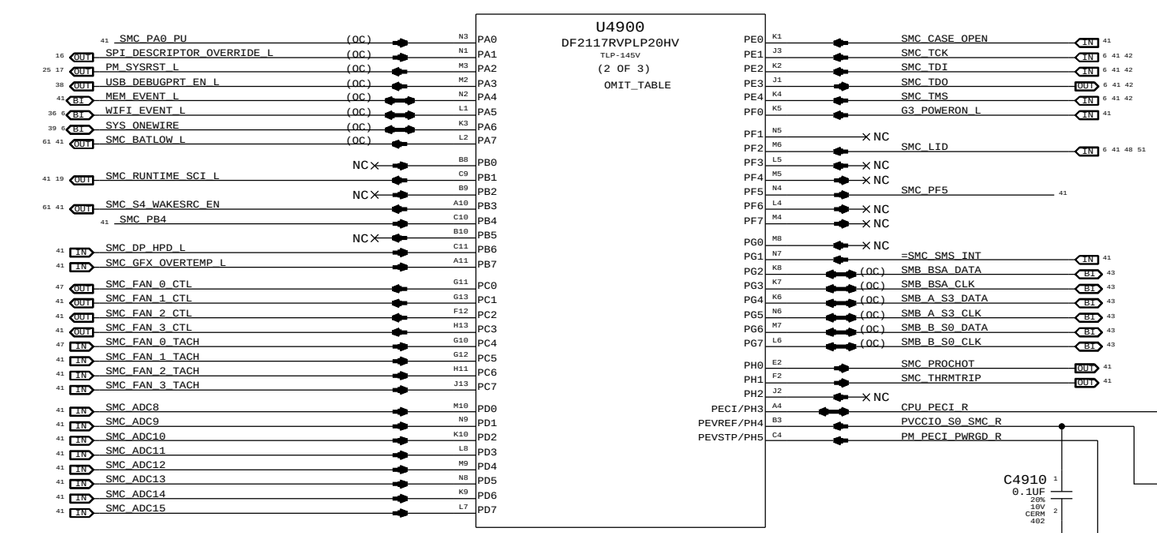
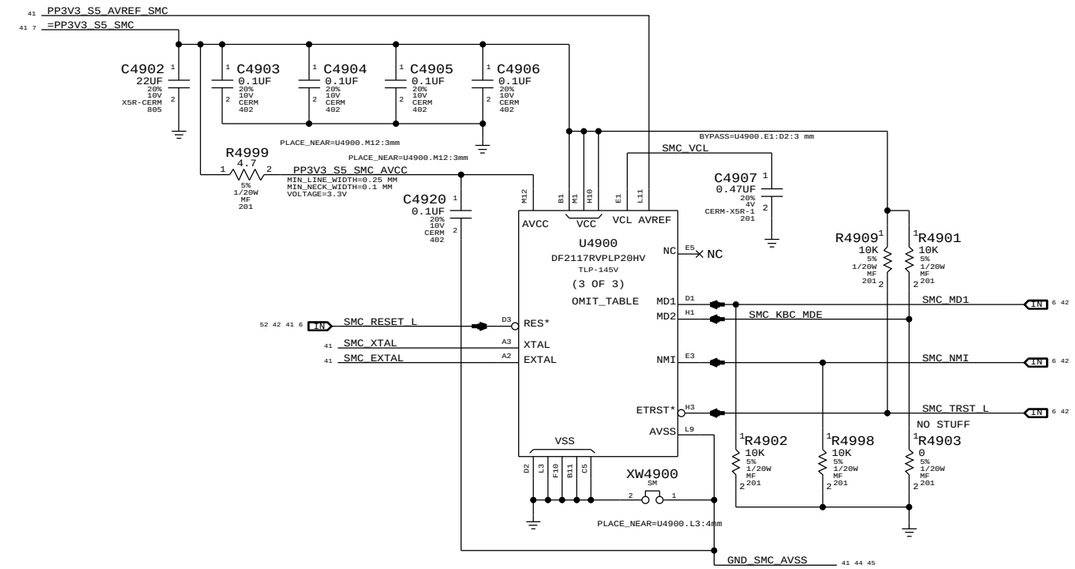
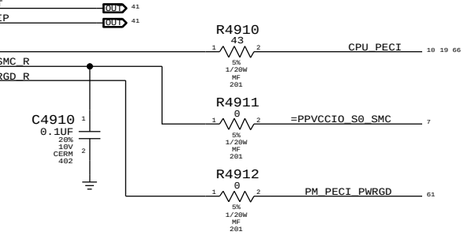
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designed as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.





SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
SMC

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PAGE 49 OF 109
SHEET 40 OF 74

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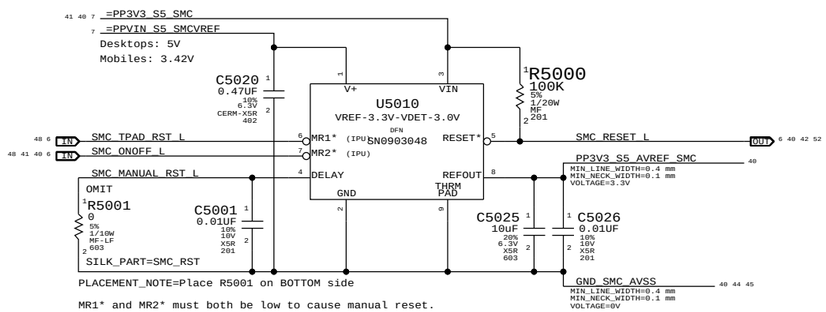
SMC Reset "Button", Supervisor & AVREF Supply

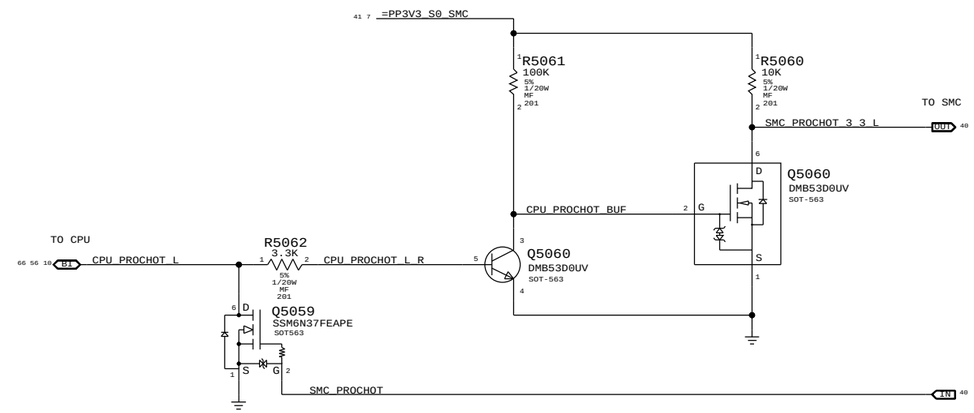


MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

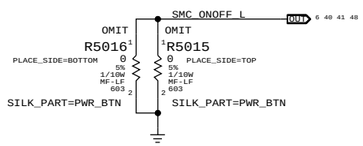
NOTE: Internal pull-ups are to VIN, not V+.

SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE
SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE
SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE
SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE
=CHGR_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
=SMC_SMS_INT	SMS_INT_L	MAKE_BASE=TRUE
SMC_ADC0	SMC_CPU_VSENSE	MAKE_BASE=TRUE
SMC_ADC1	SMC_CPU_ISENSE	MAKE_BASE=TRUE
SMC_ADC2	SMC_DCIN_VSENSE	MAKE_BASE=TRUE
SMC_ADC3	SMC_DCIN_ISENSE	MAKE_BASE=TRUE
SMC_ADC4	SMC_GFX_VSENSE	MAKE_BASE=TRUE
SMC_ADC5	SMC_GFX_ISENSE	MAKE_BASE=TRUE
SMC_ADC6	SMC_1V5S3_ISENSE	MAKE_BASE=TRUE
SMC_ADC7	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE
SMC_ADC8	SMC_LCDBKLT_ISENSE	MAKE_BASE=TRUE
SMC_ADC9	SMC_WLAN_ISENSE	MAKE_BASE=TRUE
SMC_ADC10	SMC_HDD_ISENSE	MAKE_BASE=TRUE
SMC_ADC11	SMC_PBUS_VSENSE	MAKE_BASE=TRUE
SMC_ADC12	SMC_BMON_ISENSE	MAKE_BASE=TRUE
SMC_ADC13	TP_SMC_ADC13	MAKE_BASE=TRUE
SMC_ADC15	TP_SMC_ADC15	MAKE_BASE=TRUE
SMC_P10	TP_SMC_P10	MAKE_BASE=TRUE
SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE
SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE
SMC_P26	SMC_BMON_MUX_SEL	MAKE_BASE=TRUE
SMC_P43	TP_SMC_P43	MAKE_BASE=TRUE
SMC_PF5	TP_SMC_PF5	MAKE_BASE=TRUE
SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE

PROCHOT Level Shifting to 3V3

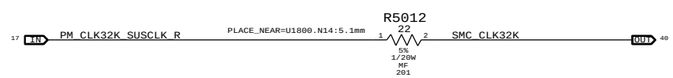


Debug Power "Buttons"

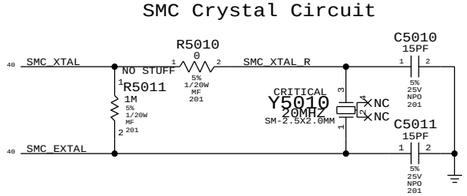


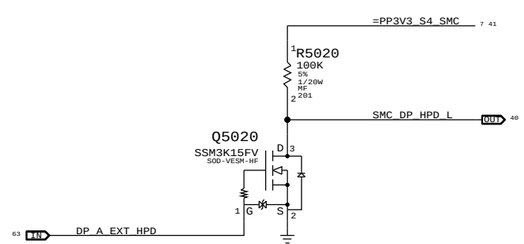
Check with SMC pullup S0

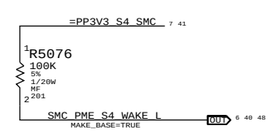
MEM_EVENT_L	R5075	10K	5%	1/20W	MF	201	=PP3V3_S0_SMC
SMC_ONOFF_L	R5070	10K	5%	1/20W	MF	201	=PP3V3_S5_SMC
G3_POWERON_L	R5072	10K	5%	1/20W	MF	201	
SMC_LID	R5071	100K	5%	1/20W	MF	201	
SMC_TX_L	R5073	10K	5%	1/20W	MF	201	
SMC_RX_L	R5074	100K	5%	1/20W	MF	201	
SMC_TMS	R5077	10K	5%	1/20W	MF	201	
SMC_TDO	R5078	10K	5%	1/20W	MF	201	
SMC_TDI	R5079	10K	5%	1/20W	MF	201	
SMC_TCK	R5080	10K	5%	1/20W	MF	201	
SMC_BIL_BUTTON_L	R5081	10K	5%	1/20W	MF	201	
SMC_BC_ACOK	R5087	470K	5%	1/20W	MF	201	
SMS_INT_L	R5093	10K	5%	1/20W	MF	201	
			NOSTUFF				
SMC_PA0_PU	R5091	100K	5%	1/20W	MF	201	
SMC_RUNTIME_SCI_L	R5094	100K	5%	1/20W	MF	201	
			NOSTUFF				
SMC_ADAPTER_EN	R5085	10K	5%	1/20W	MF	201	
SMC_CASE_OPEN	R5086	10K	5%	1/20W	MF	201	
SMC_PB4	R5088	10K	5%	1/20W	MF	201	
SMC_S4_WAKESRC_EN	R5090	100K	5%	1/20W	MF	201	



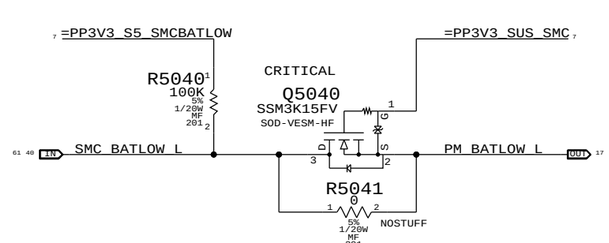
SMC Crystal Circuit







BATLOW# Isolation



Internal 20K pull-up on PM_BATLOW_L in PCH.

Below connections are different from K91

SMC_PA0_PU	HISIDE_ISENSE_OC	MAKE_BASE=TRUE
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE
SMC_ADC14	SMC_HS_COMPUTING_ISENSE	MAKE_BASE=TRUE
SMC_GFX_THROTTLE_L	TP_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE

SMC_GFX_OVERTEMP_L — R5095 10K 5% 1/20W MF 201 — =PP3V3_S5_SMC

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PAGE TITLE: SMC Support

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PAGE: 50 OF 109

SHEET: 41 OF 74

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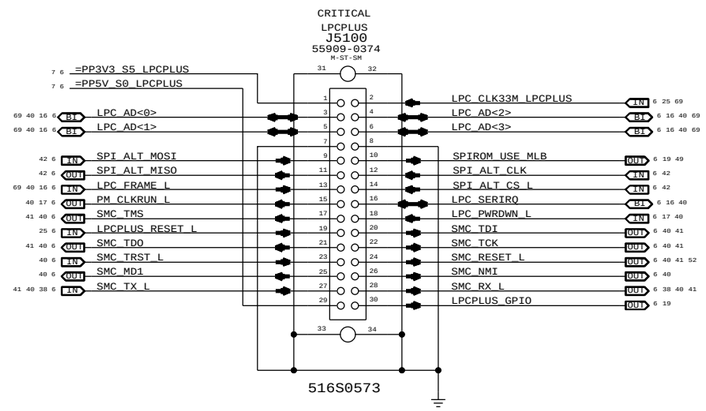
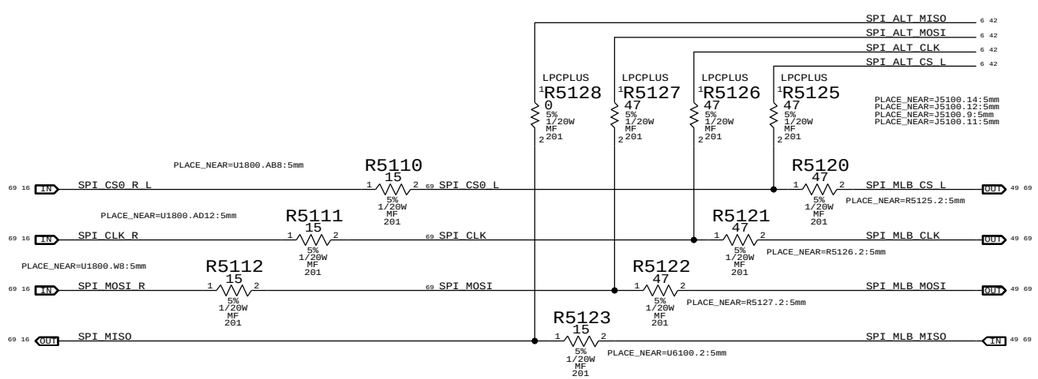
LPC+SPI Connector



SPI Bus Series Termination



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LPC+SPI Debug Connector

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PAGE 51 OF 109

SHEET 42 OF 74

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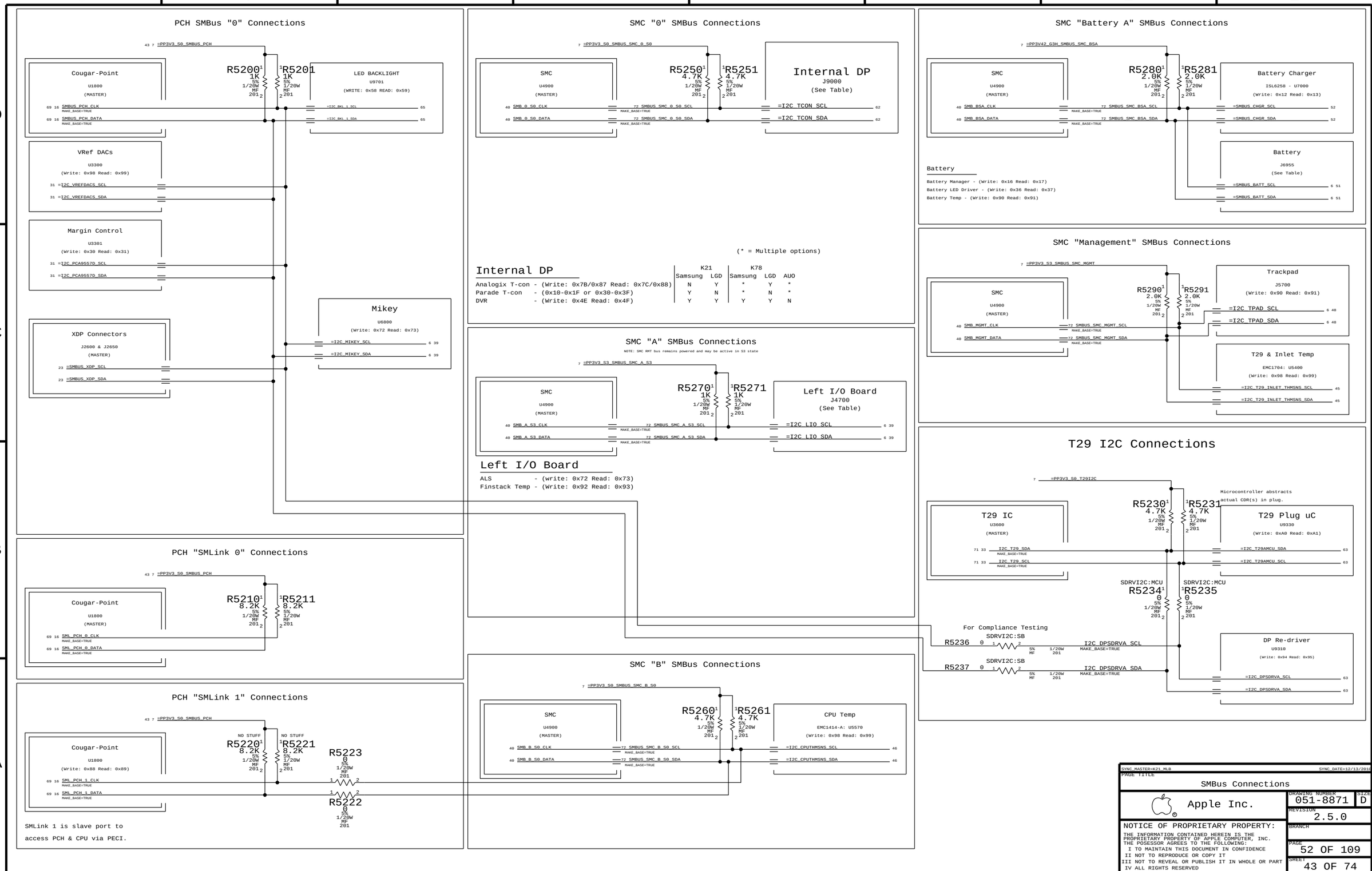

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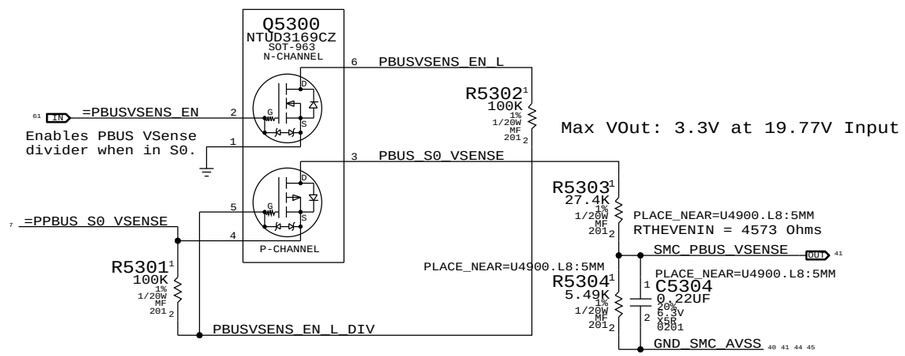
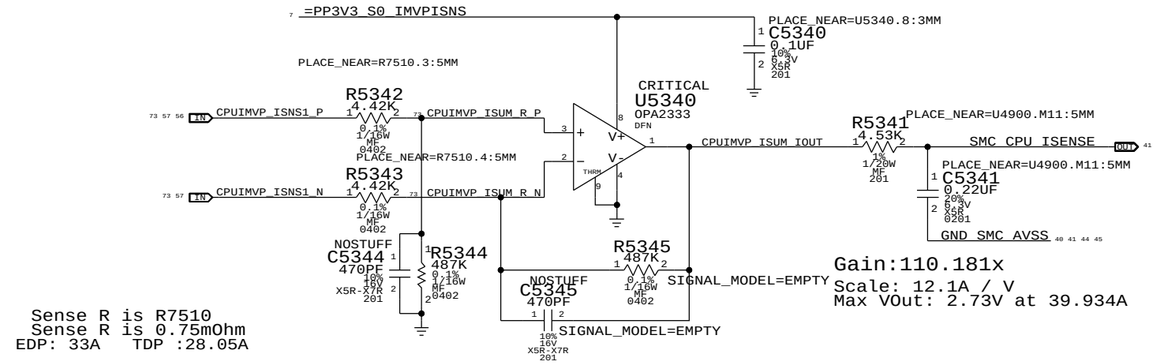
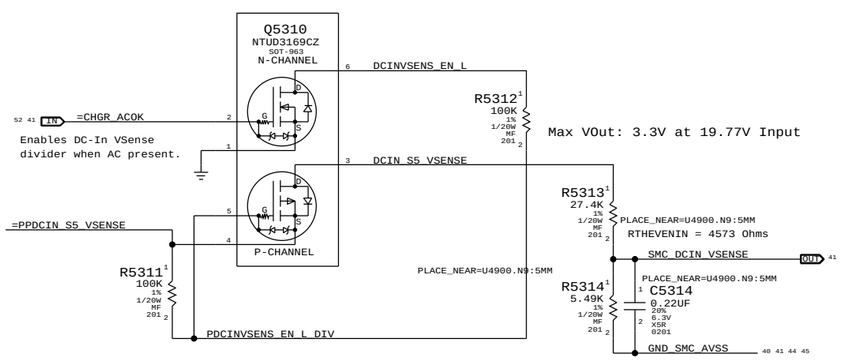
PBUS Voltage Sense Enable & Filter



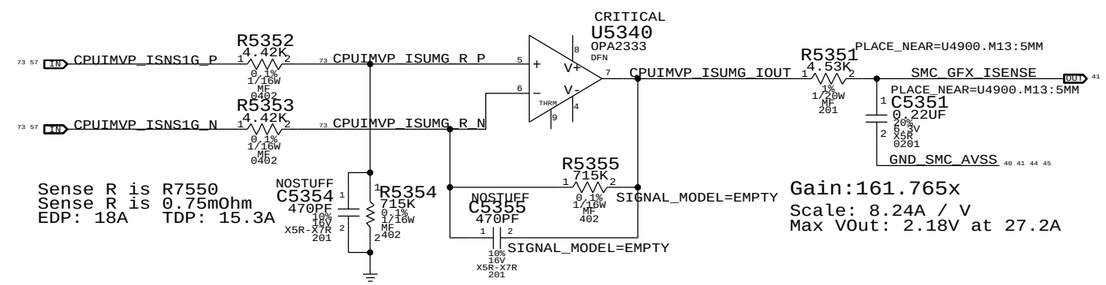
CPU VCore Load Side Current Sense / Filter



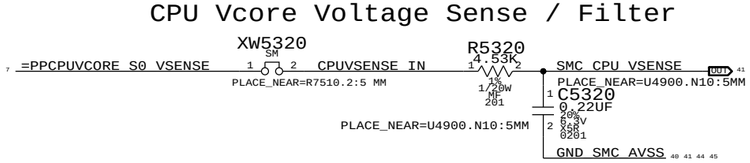
DC-In Voltage Sense Enable & Filter



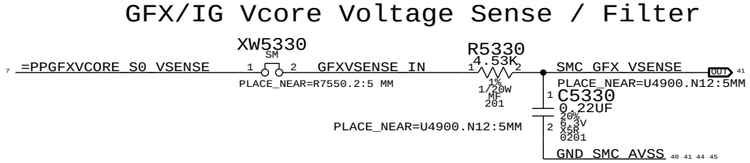
GFX/IG VCore Load Side Current Sense / Filter



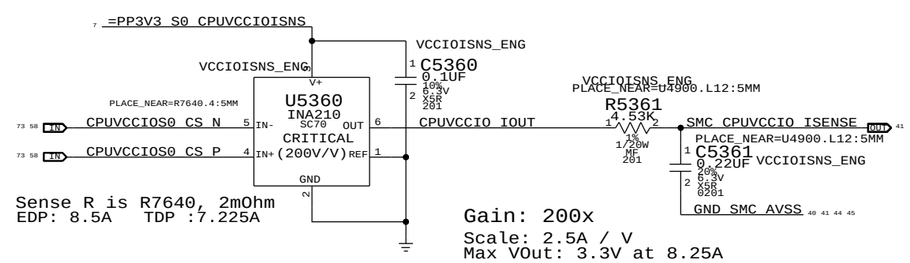
CPU Vcore Voltage Sense / Filter



GFX/IG Vcore Voltage Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter



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	SHEET 44 OF 74

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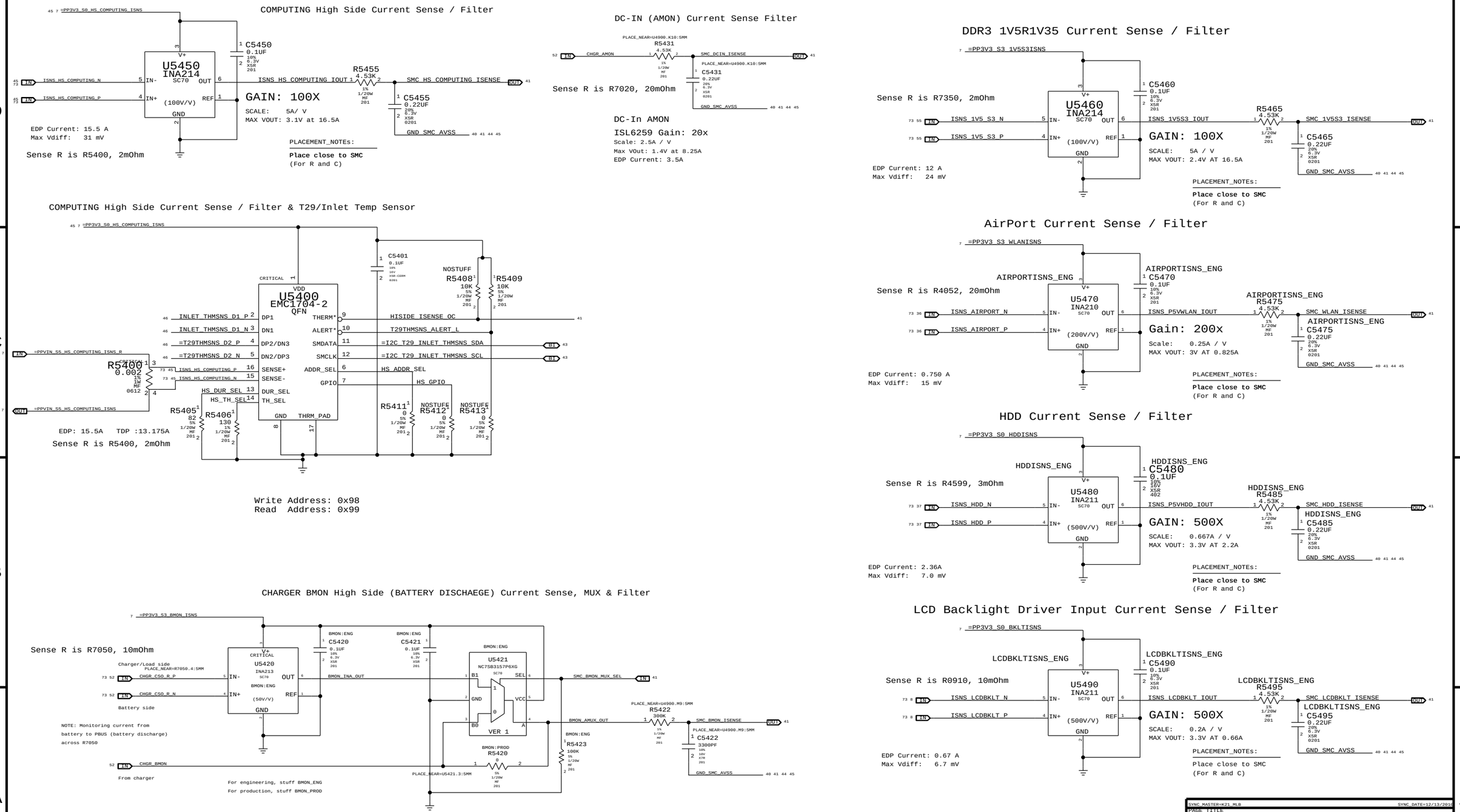

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
High Side Current Sensing

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
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PAGE 54 OF 109
SHEET 45 OF 74

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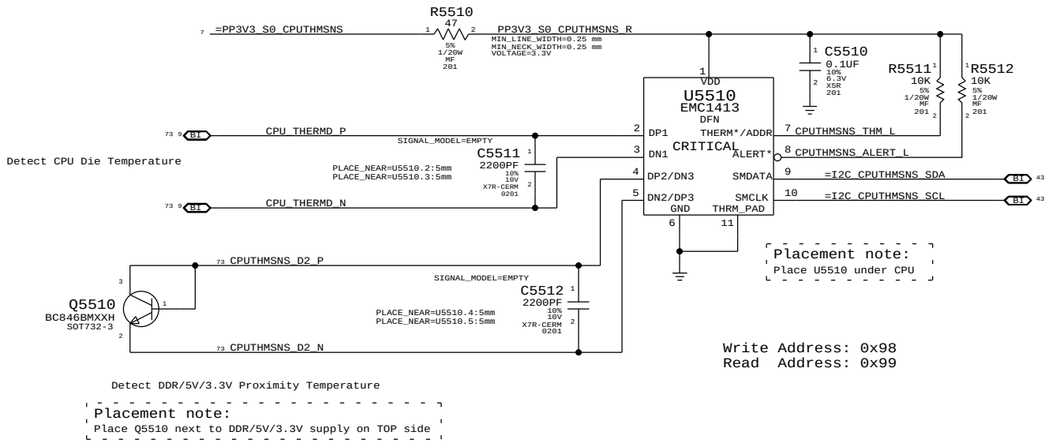
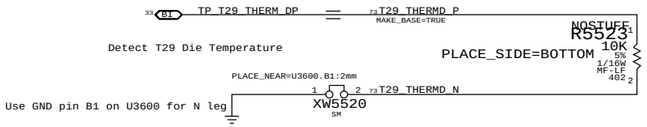
CPU Proximity Sensor



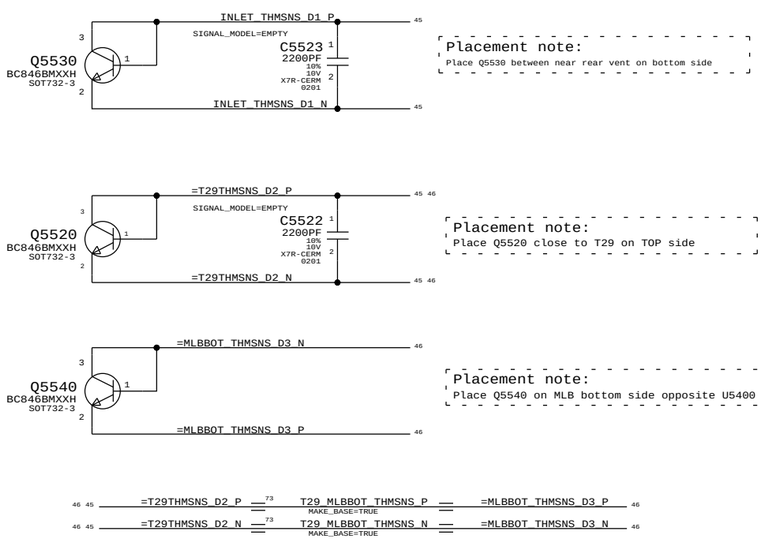
T29 Die



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

Replacing caps with 100K PD on ISENSE SMC inputs

T29,MLB Bottom & Inlet Proximity Sensors



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PAGE TITLE

Thermal Sensors

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PAGE 55 OF 109

SHEET 46 OF 74

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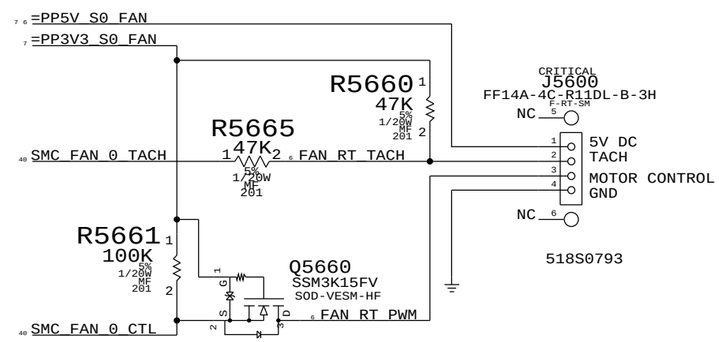
FAN CONNECTOR



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PAGE TITLE
Fan

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PAGE 56 OF 109

SHEET 47 OF 74

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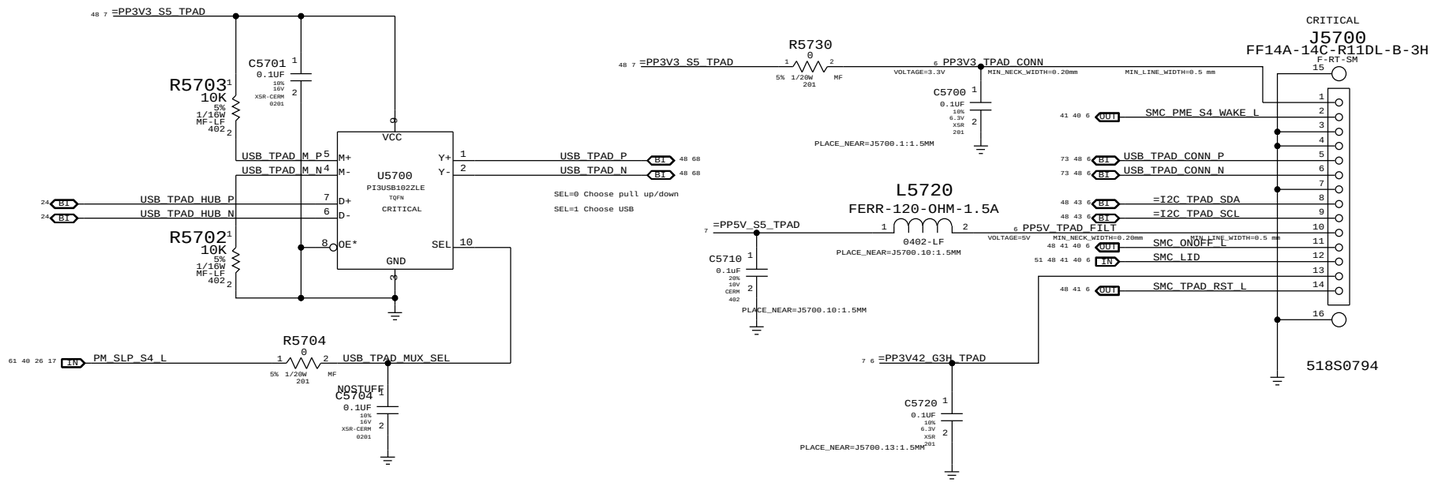
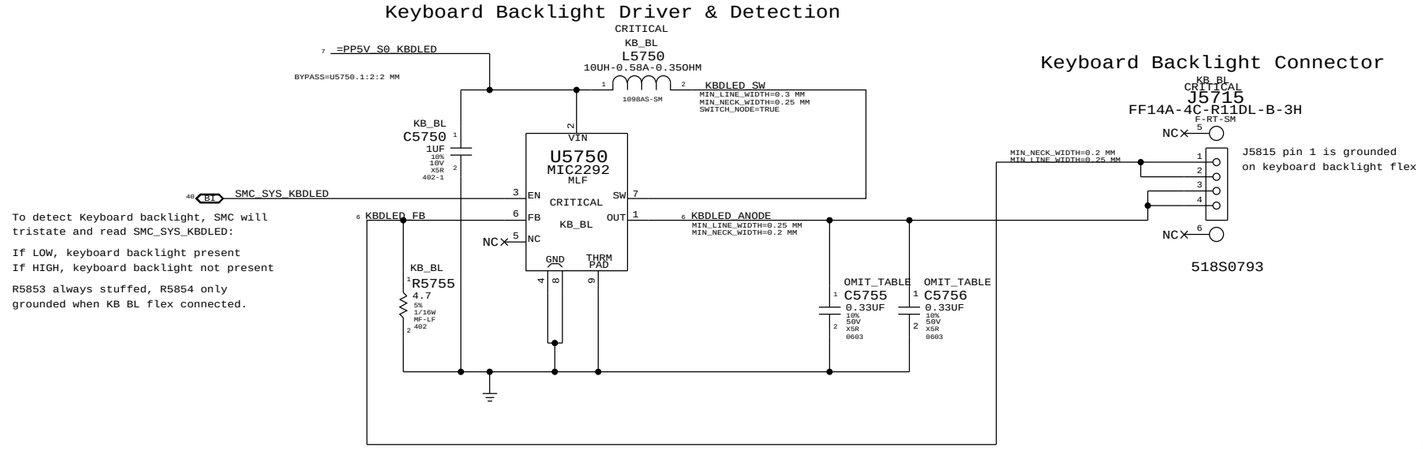
IPD Flex Connector



Keyboard Backlight Driver & Detection



Keyboard Backlight Connector

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0704	2	CAP,CER,0.22UF,10%,50V,X5R,0603	C5756,C5755		KB_BL

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE: IPD / KBD Backlight

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REVISION: 2.5.0

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PAGE: 57 OF 109

SHEET: 48 OF 74

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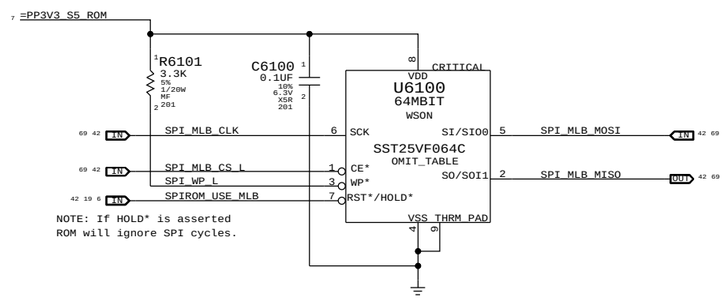

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PAGE TITLE

SPI ROM

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PAGE 61 OF 109

SHEET 49 OF 74

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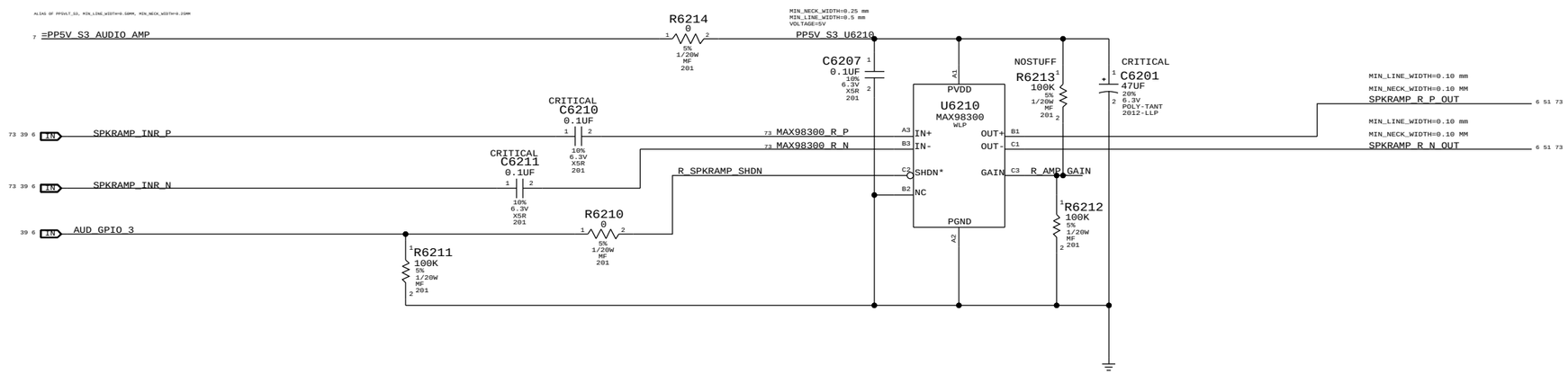
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB



SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

AUDI0: SPEAKER AMP

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PAGE 62 OF 109

SHEET 50 OF 74

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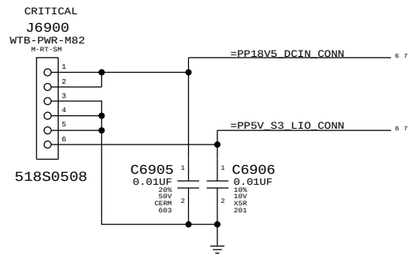
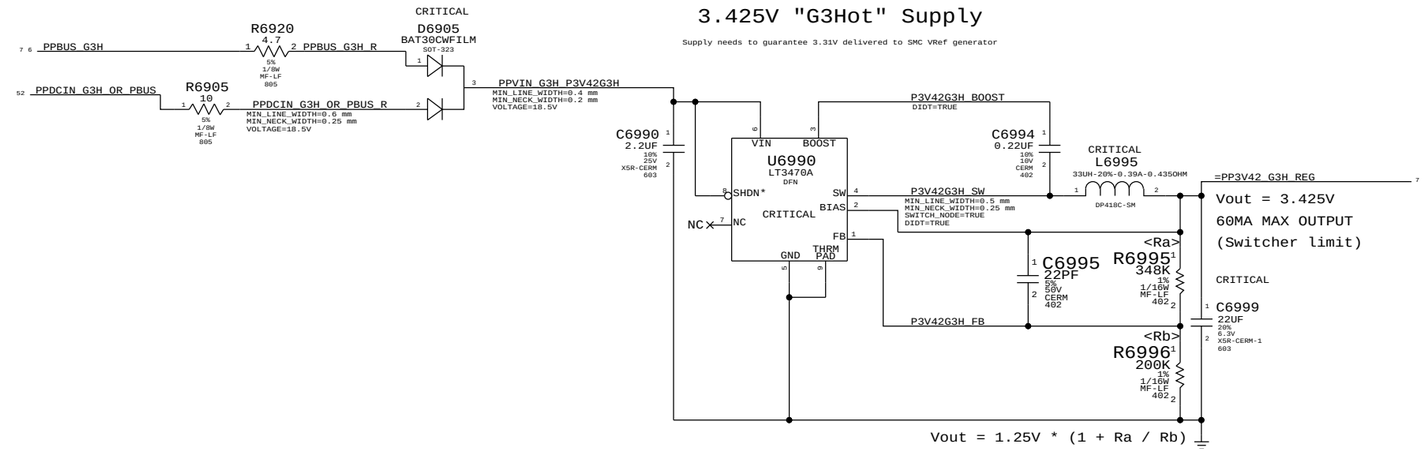
MLB to LIO Power Cable Connector



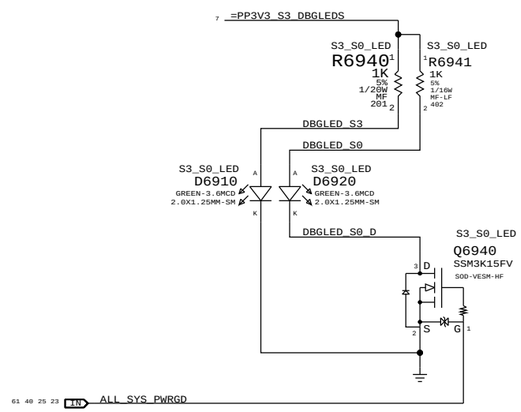
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

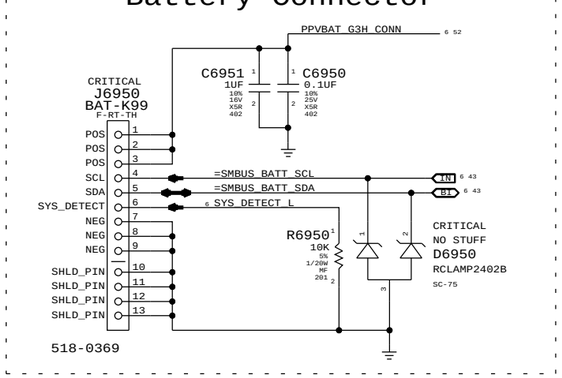


Debug LEDs

(For development only)

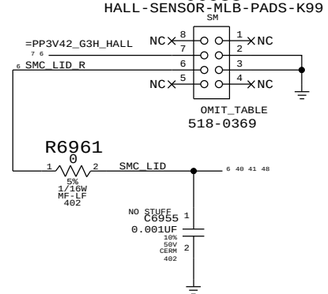


K99-Specific Battery Connector

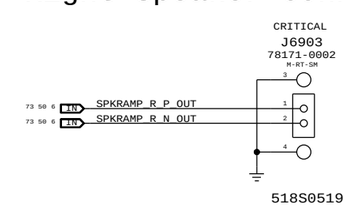


J6955

HALL-SENSOR-MLB-PADS-K99



Right Speaker Connector



SYNC_MASTER=K21_MLB	SYNC_DATE=11/11/2011
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: 051-8871 SIZE: D
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	PAGE: 69 OF 109
	SHEET: 51 OF 74

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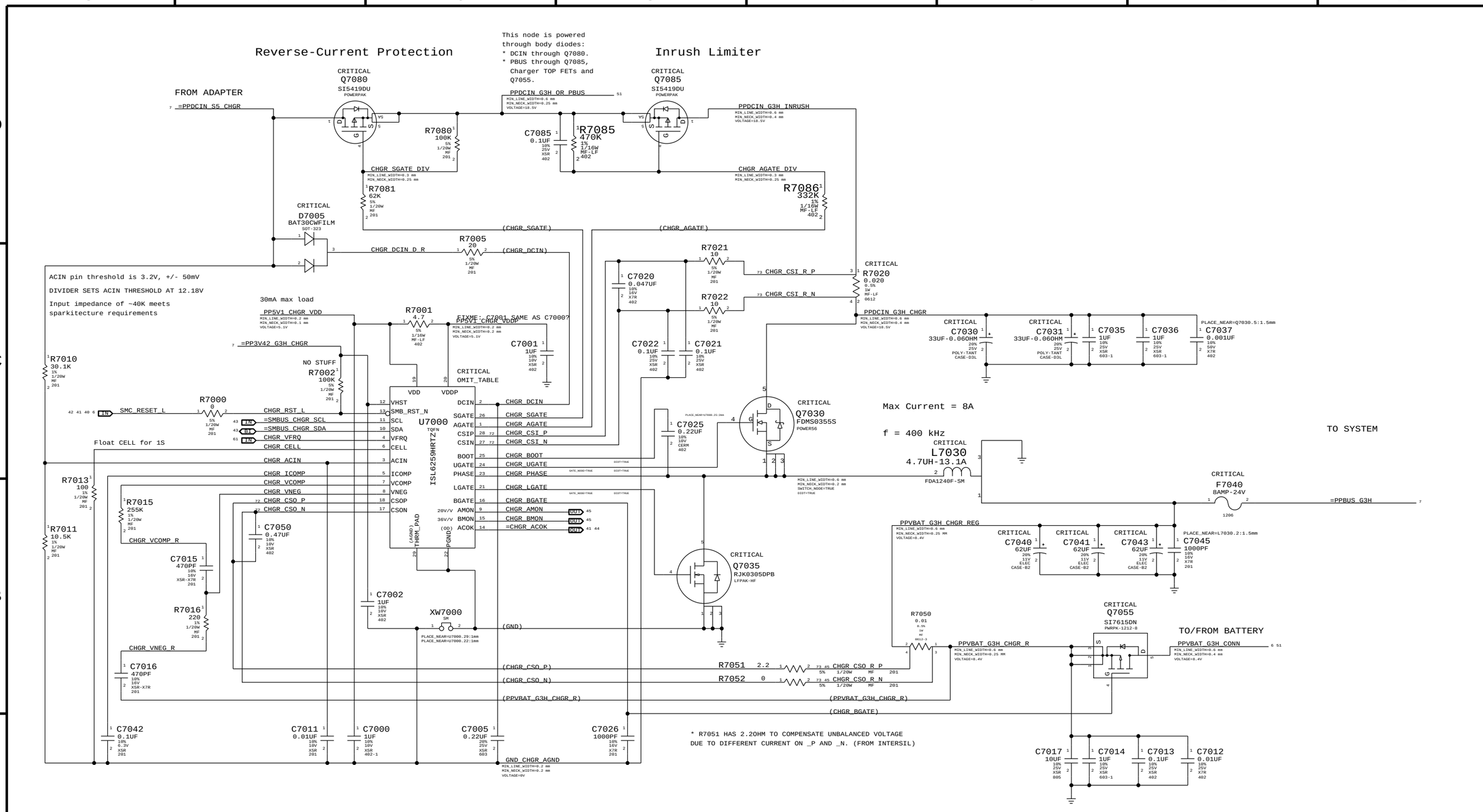

SYNC MASTER=K21_MLB SYNC DATE=11/30/2010

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

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PAGE 70 OF 109

SHEET 52 OF 74

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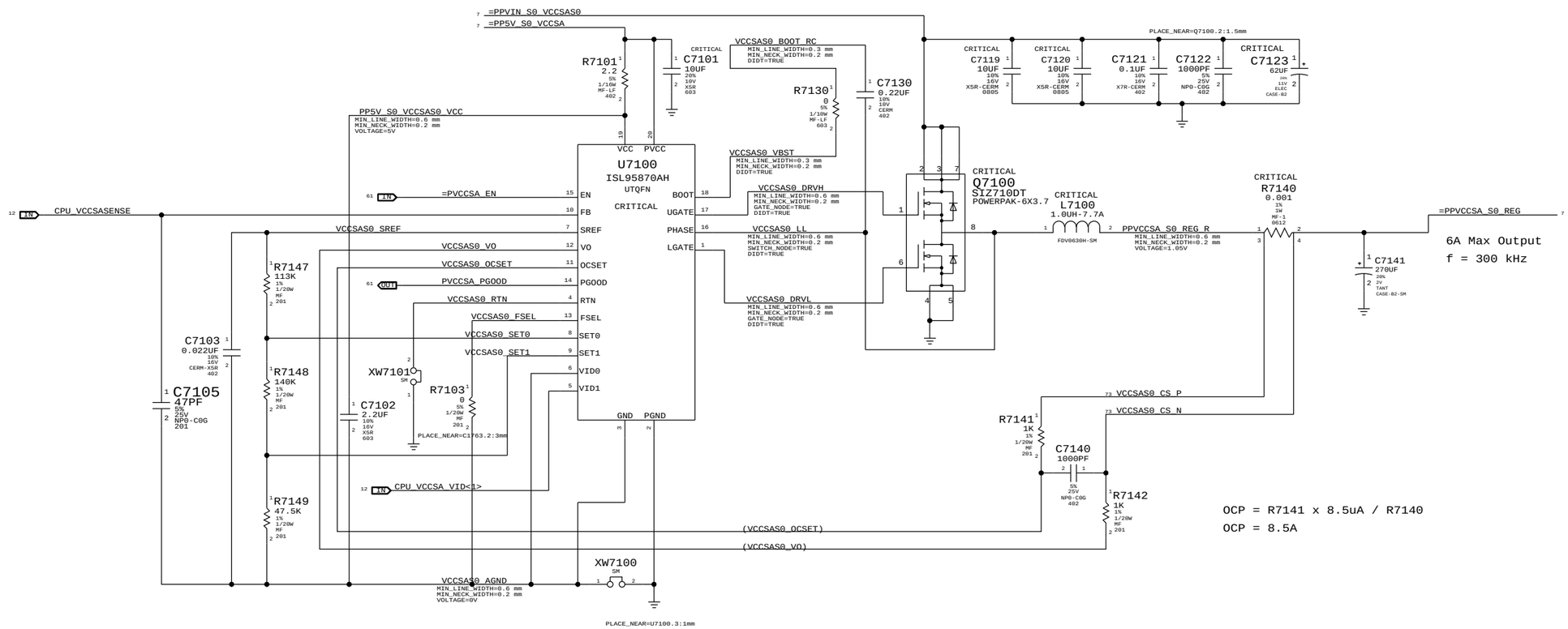

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V

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PAGE TITLE

System Agent Supply

Apple Inc.

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PAGE 71 OF 109

SHEET 53 OF 74

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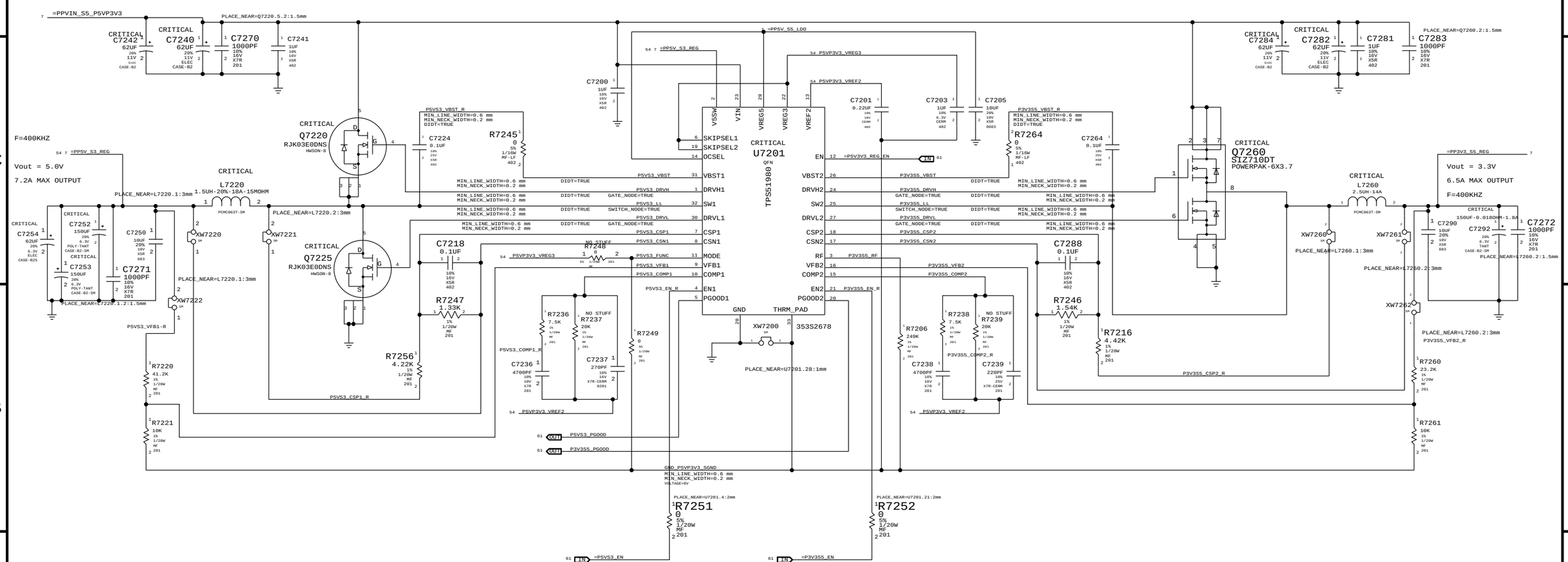

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PAGE TITLE

5V / 3.3V Power Supply

Apple Inc.

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PAGE 72 OF 109

SHEET 54 OF 74

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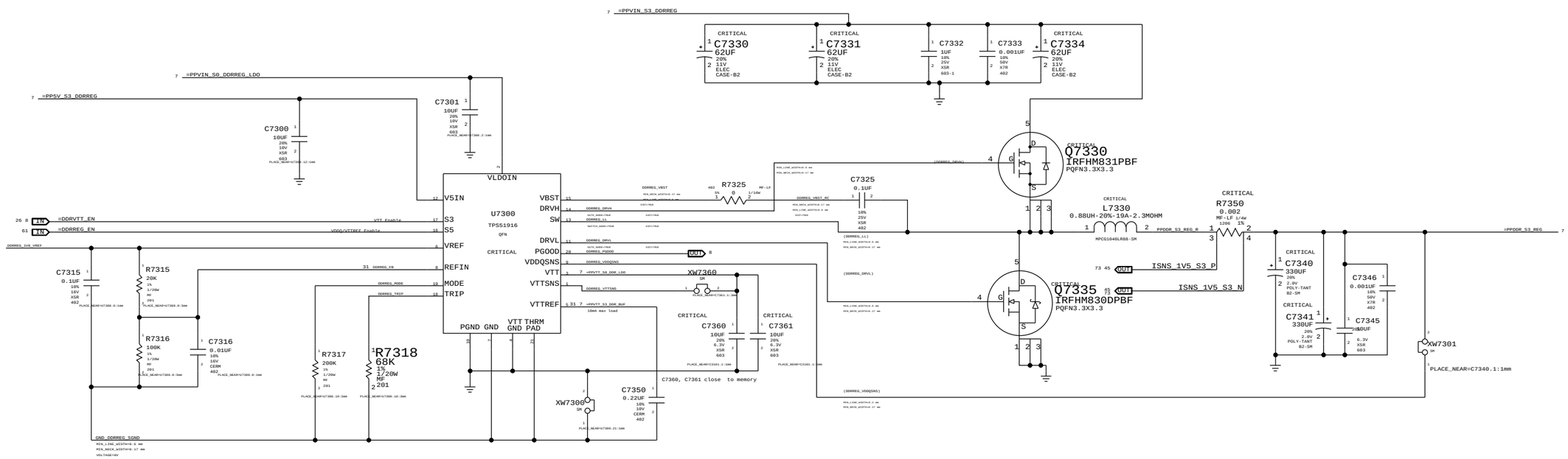

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PAGE TITLE

1.5V DDR3 Supply

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PAGE 73 OF 109

SHEET 55 OF 74

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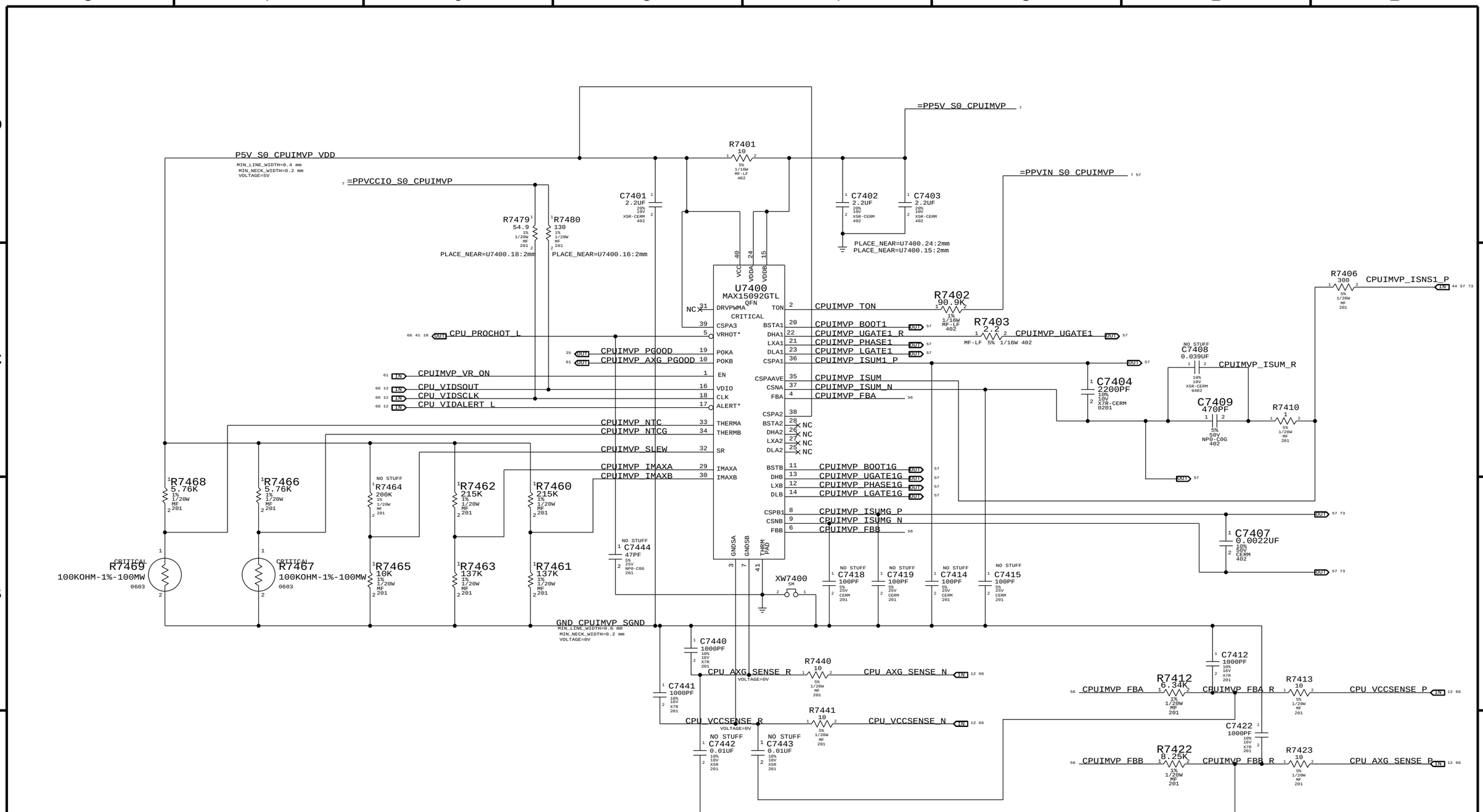

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

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PAGE 74 OF 109

SHEET 56 OF 74

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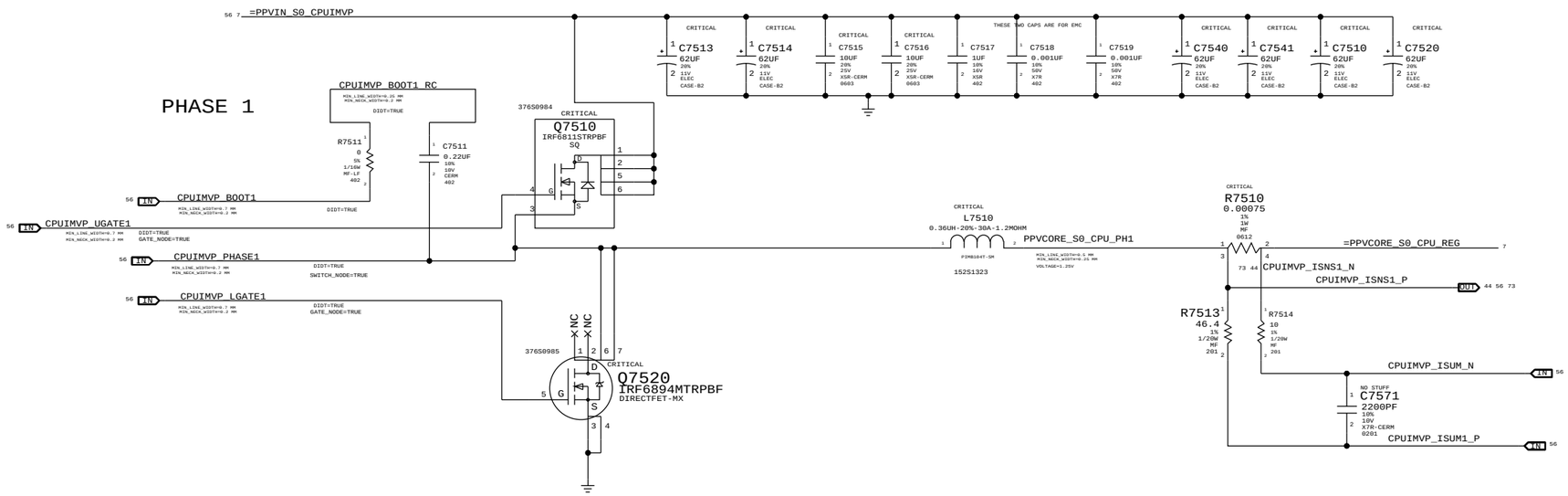
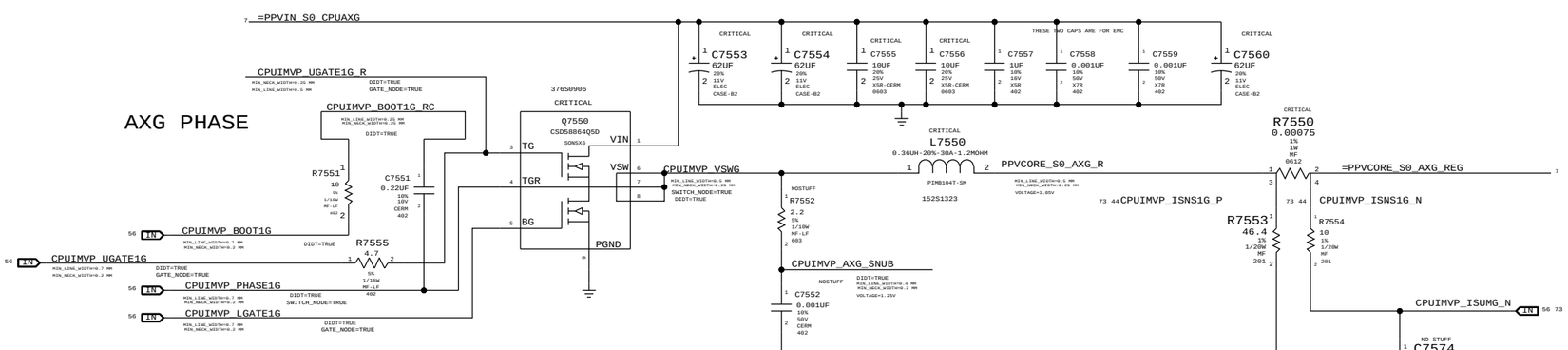
CPU=Sandy Bridge ULV, AXG=GT2





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PAGE TITLE
CPU IMVP7 & AXG VCore Output

Apple Inc.

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PAGE 75 OF 109
SHEET 57 OF 74

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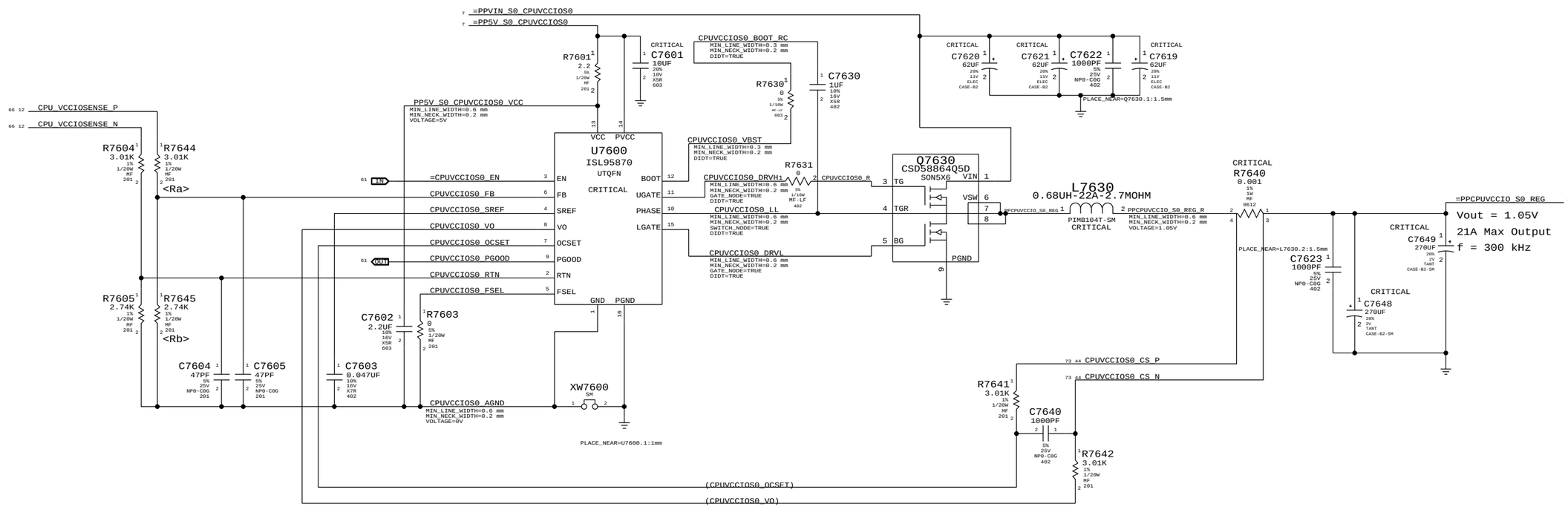
CPU VCCIO (1.05V S0) Regulator



OCP = R7641 x 8.5uA / R7640
OCP = 25.6A
Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2011

PAGE TITLE
CPU VCCIO (1.05V) Power Supply

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REVISION 2.5.0
BRANCH
PAGE 76 OF 109
SHEET 58 OF 74

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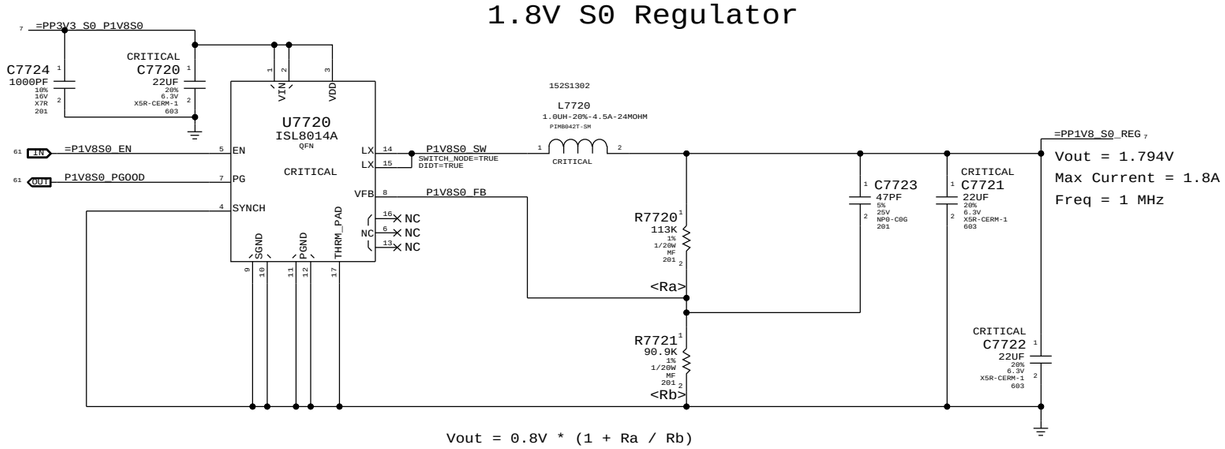
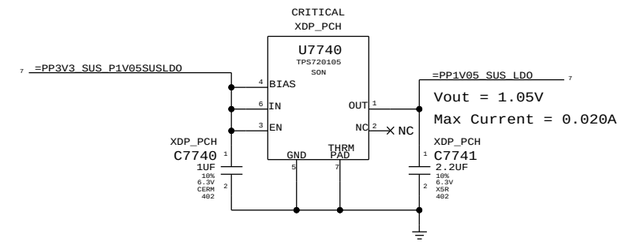
1.8V S0 Regulator



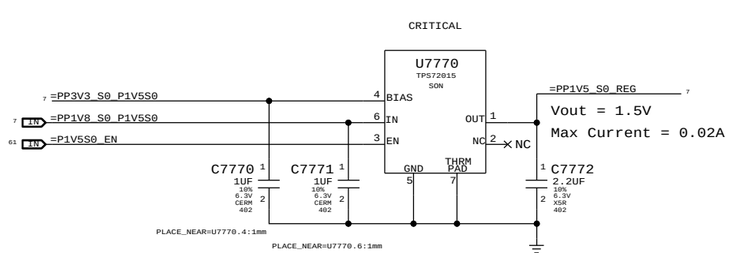
Vout = 0.8V * (1 + Ra / Rb)

1.05V SUS LDO

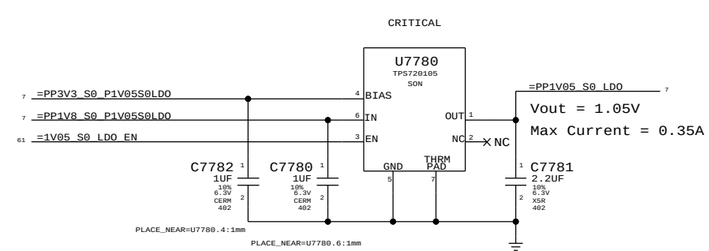
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



1.05V S0 LDO



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PAGE TITLE
Misc Power Supplies

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PAGE 77 OF 109

SHEET 59 OF 74

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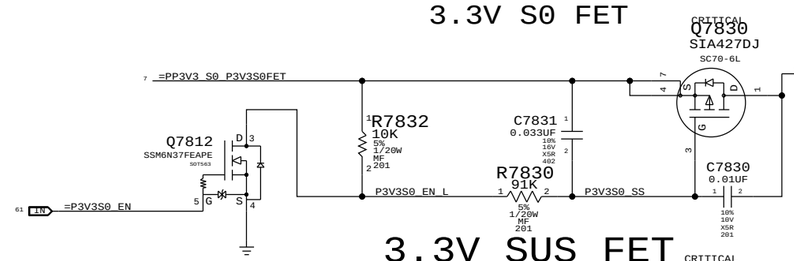
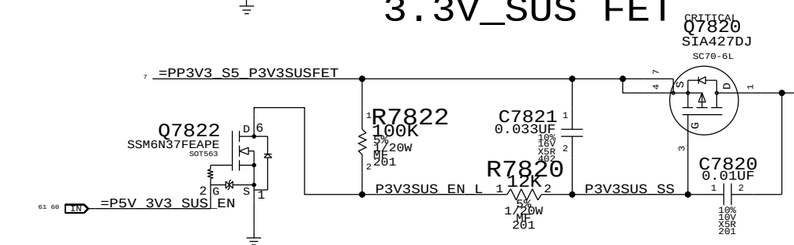
3.3V S0 FET



3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

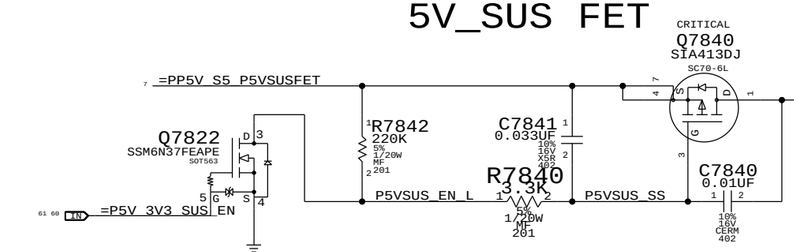
3.3V_SUS FET



3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

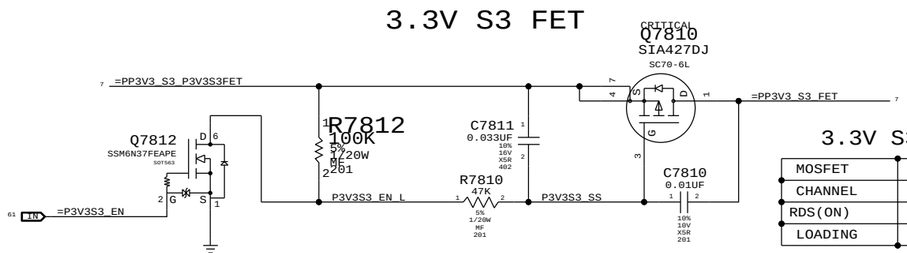
5V_SUS FET



5V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 12V/8V
RDS(ON)	29 mOhm @4.5V
LOADING	100? mA (EDP)

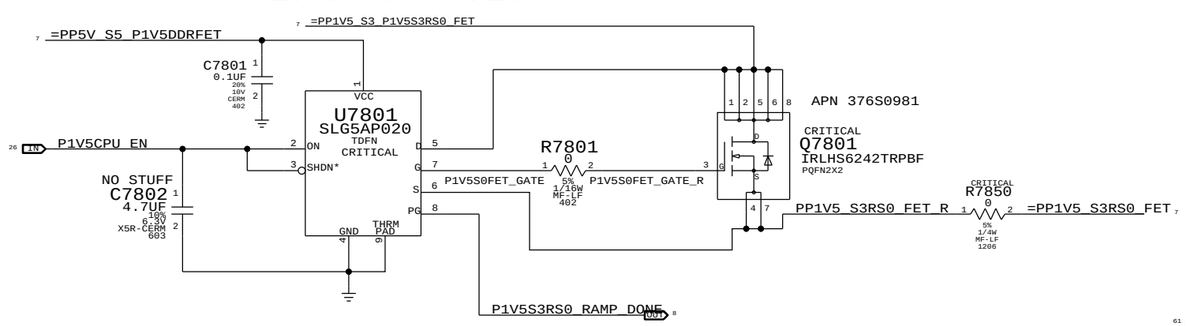
3.3V S3 FET



3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

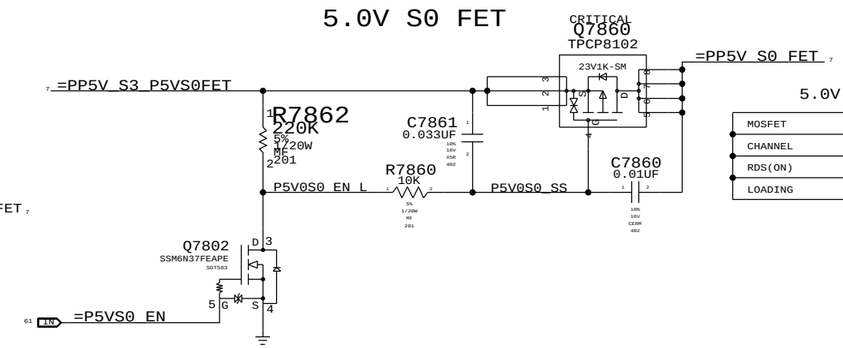
1.5V S3/S0 FET



1.5V S3/S0 FET

MOSFET	PQFN2X2
CHANNEL	N-TYPE
RDS(ON)	9.4 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET



5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=K21 MLB SYNC DATE=12/13/2010

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

REVISION 2.5.0

BRANCH

PAGE 78 OF 109

SHEET 60 OF 74

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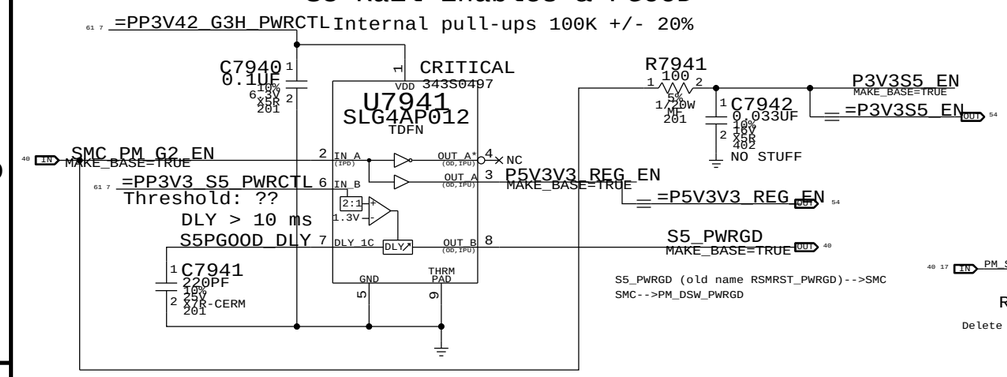
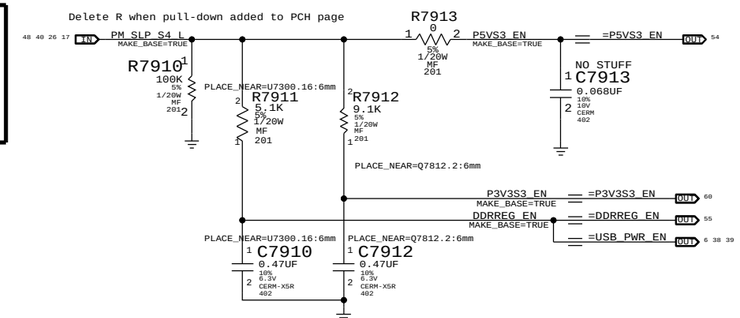
S5 Rail Enables & PGOOD

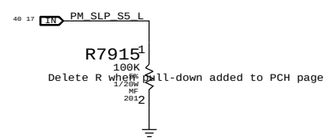


State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

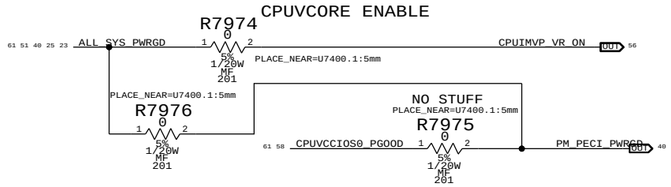
3.3V,5V S3 ENABLE



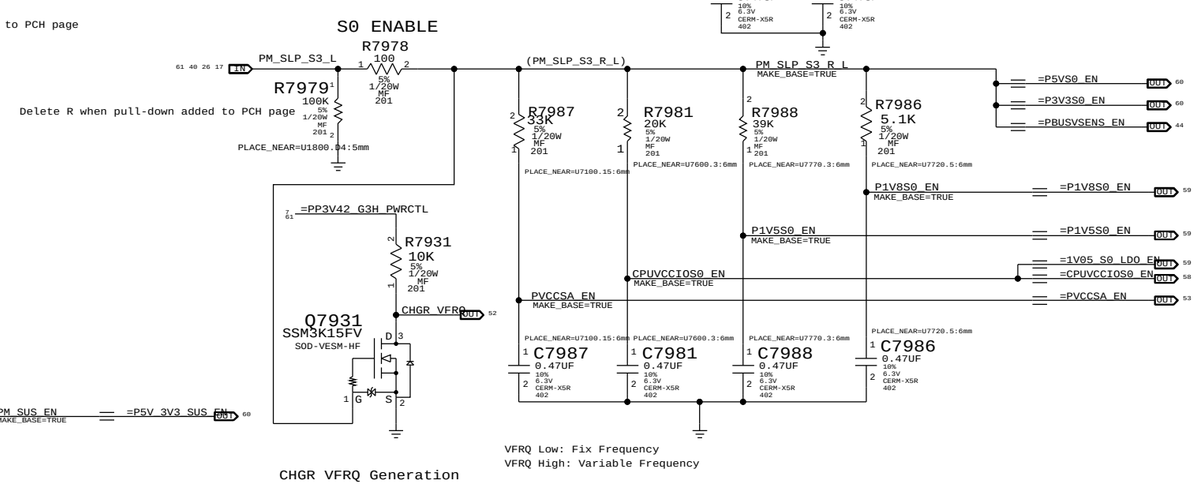
3.3V S4 ENABLE



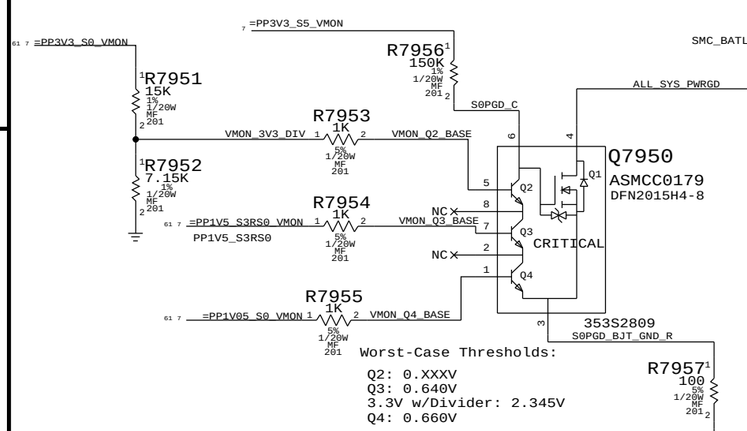
CPUVCORE ENABLE



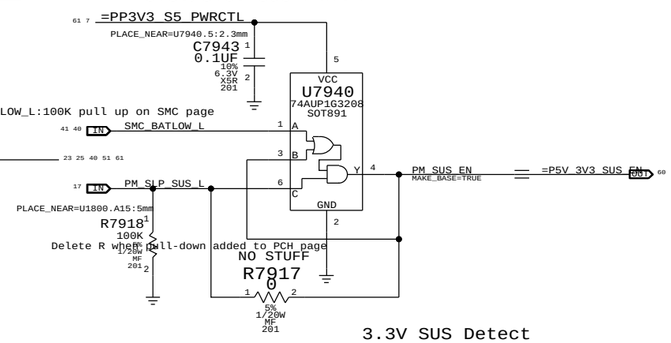
S0 ENABLE



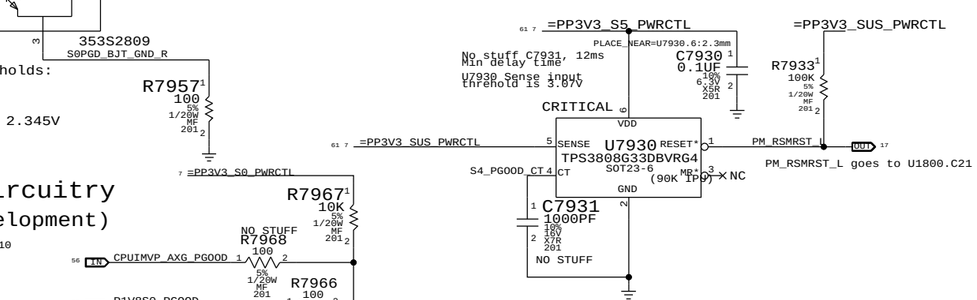
S0 Rail PGOOD (BJT Version)



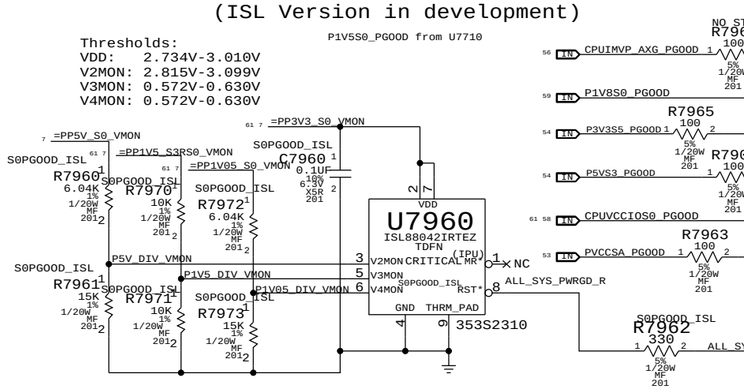
3.3V/5.0V Sus ENABLE



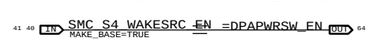
3.3V SUS Detect



S0 Rail PGOOD Circuitry
(ISL Version in development)



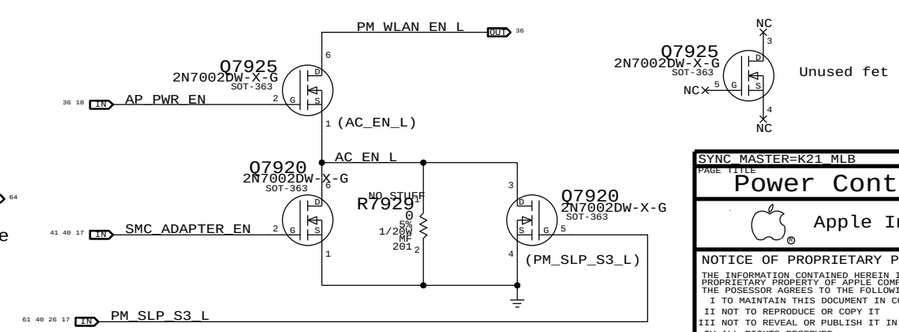
DP S4 Power Enable



PSOC USB Power Enable

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



SYNC_MASTER=K21_MLB	SYNC_DATE=12/13/2010
PAGE TITLE: Power Control 1/ENABLE	
Apple Inc.	DRAWING NUMBER 051-8871 / SIZE D
	REVISION 2.5.0
	BRANCH
	PAGE 79 OF 109
	SHEET 61 OF 74

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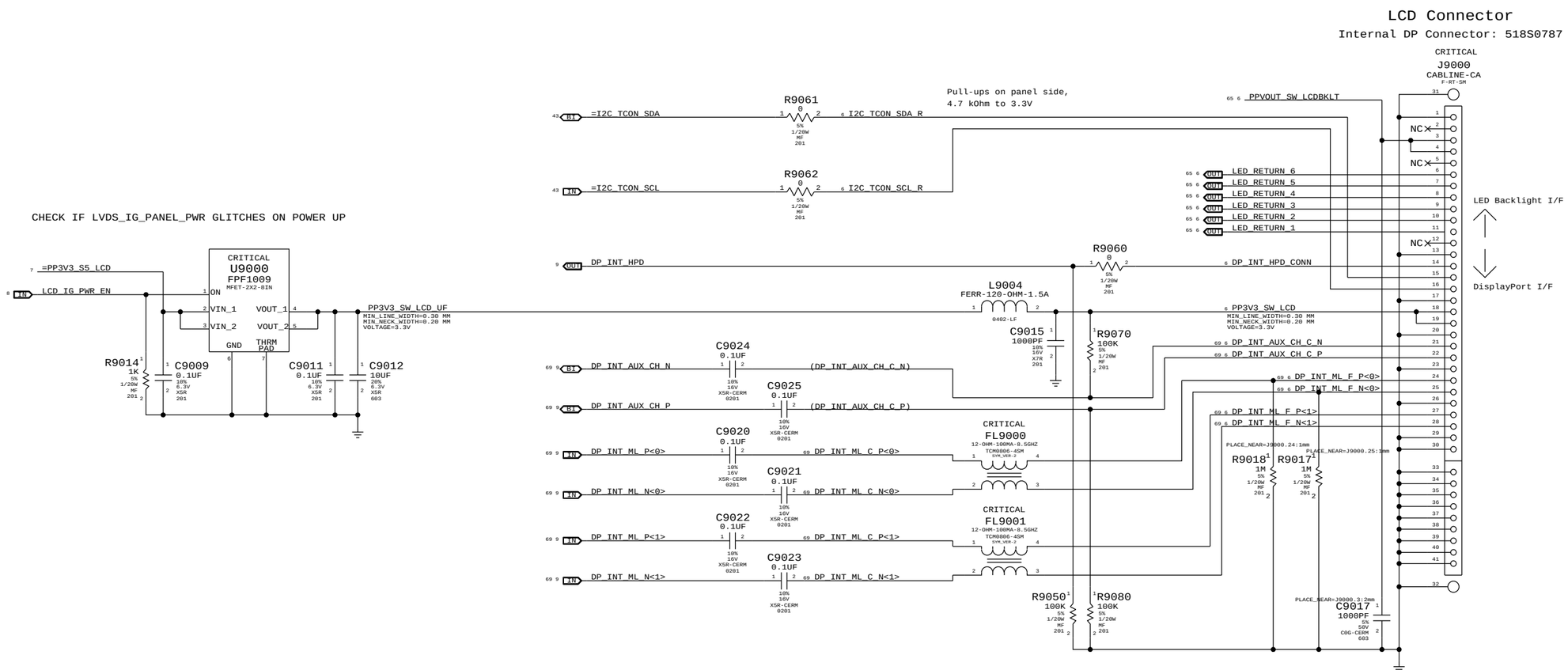

SYNC MASTER=K21_MLB	SYNC DATE=12/13/2016
PAGE TITLE: Internal DisplayPort Connector	
Apple Inc.	DRAWING NUMBER: 051-8871 — SIZE: D
	REVISION: 2.5.0
	BRANCH:
	PAGE: 90 OF 109
	SHEET: 62 OF 74

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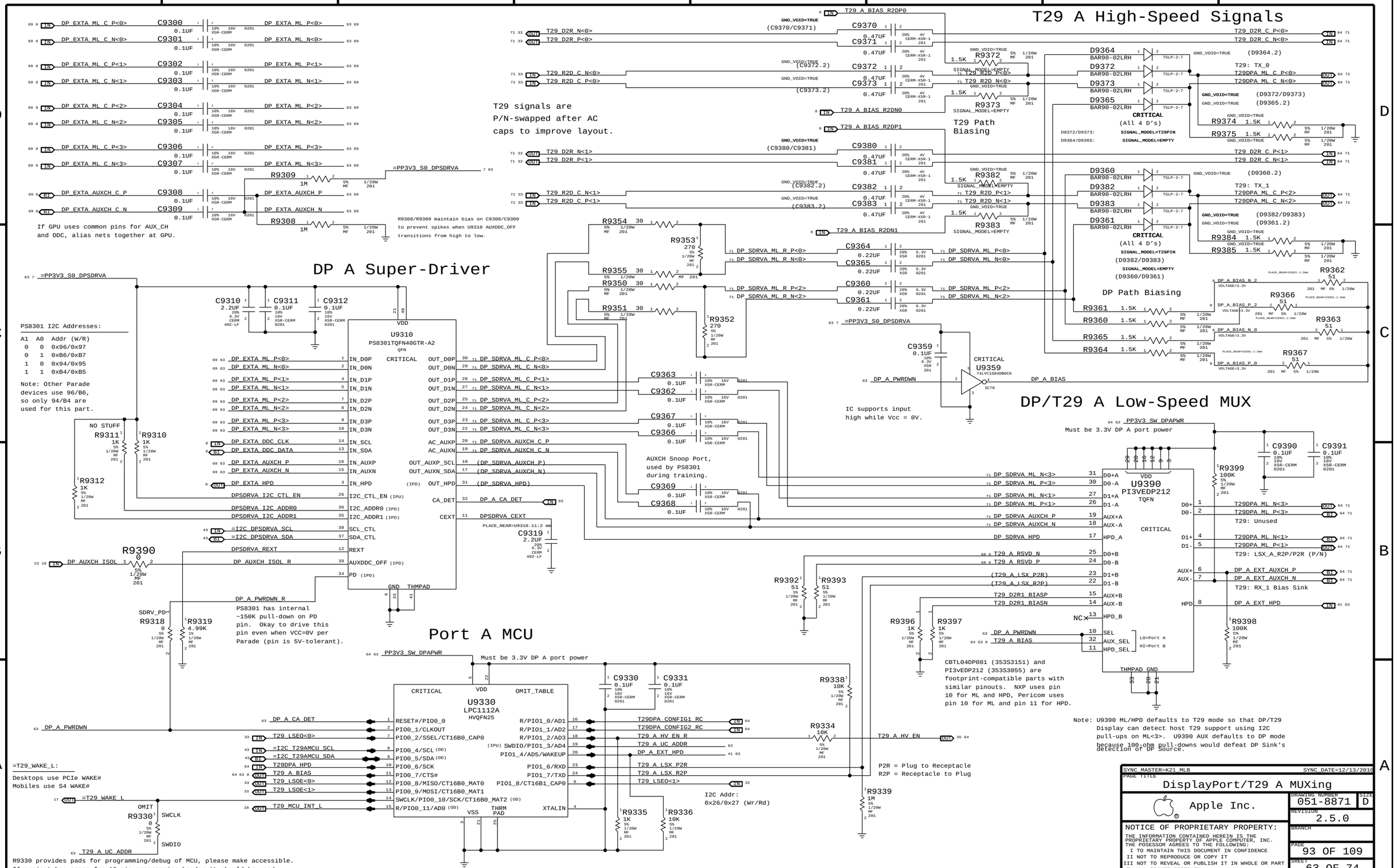

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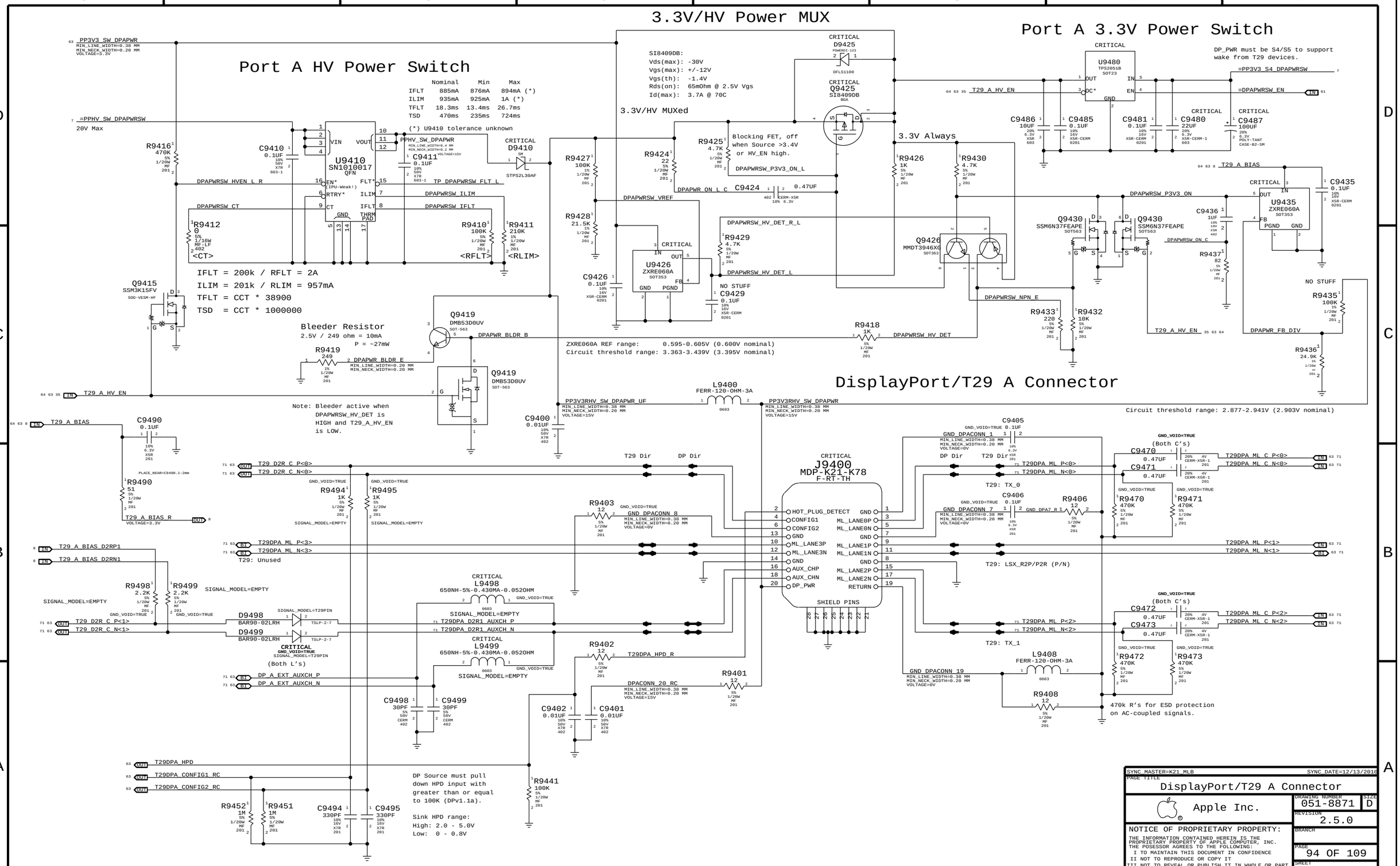

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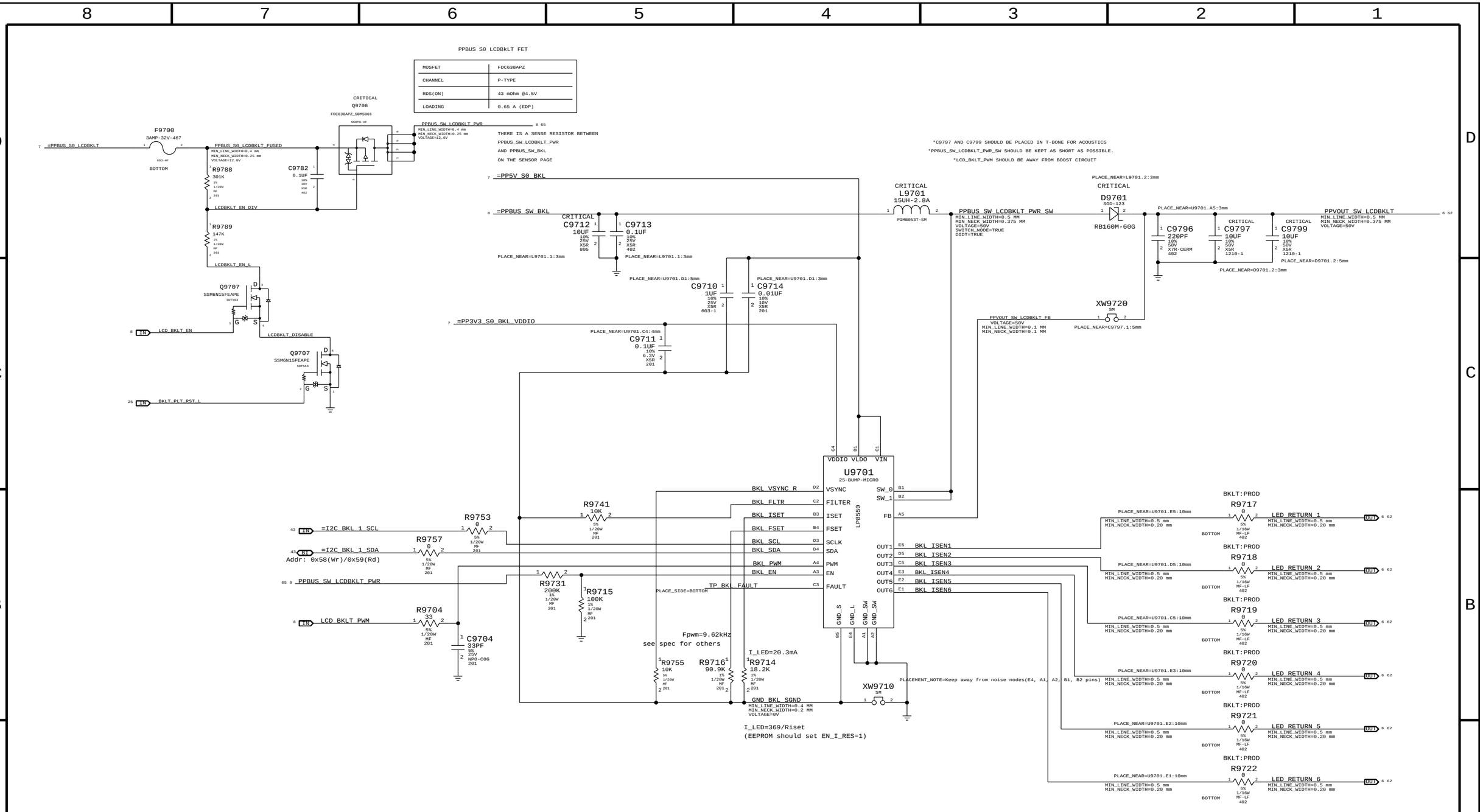

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=K21_MLB SYNC_DATE=12/13/2010

PAGE TITLE
LCD Backlight Driver

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

REVISION 2.5.0

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PAGE 97 OF 109

SHEET 65 OF 74

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_XDP_BPM	TOP,BOTTOM	100 MIL	100 MIL	100 MIL	100 MIL	=STANDARD	=STANDARD
CPU_XDP_BPM	*	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S	=CPU_50S

NOTE: CPU_XDP_BPM physical constraint is to prevent routing on outer layers.

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 40
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 25
	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 41 56
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MTL	PM_THRMTRIP_L	10 19
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKP	8 10
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLKN	8 10
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_XDP_BPM	CPU_ITP	XDP_BPM_L<7..0>	10 23
XDP_BPM_R_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 56
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 56
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 58
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 56
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 56
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 56
CPU_SVIDSCLK	CPU_50S	CPU_COMP	CPU_VIDSCLK	12 56
CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 56
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE

CPU Constraints

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

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PAGE 100 OF 109

SHEET 66 OF 74

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9,ISL10	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9,ISL10	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK P<5..0>	8 11 27 28 32
MEM_A_CLK	MEM_72D	MEM_CLK	MEM A CLK N<5..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM A CKE<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM A CS L<3..0>	8 11 27 28 32
MEM_A_CTRL	MEM_55S	MEM_CTRL	MEM A ODT<3..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A A<15..0>	8 11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A BA<2..0>	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A RAS L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A CAS L	11 27 28 32
MEM_A_CMD	MEM_55S	MEM_CMD	MEM A WE L	11 27 28 32
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM A DQ<7..0>	11 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM A DQ<15..8>	11 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM A DQ<23..16>	11 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM A DQ<31..24>	11 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM A DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM A DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM A DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM A DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	11 27
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	11 27
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	11 27
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	11 27
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>	11 27
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK P<5..0>	8 11 29 30 32
MEM_B_CLK	MEM_72D	MEM_CLK	MEM B CLK N<5..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM B CKE<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM B CS L<3..0>	8 11 29 30 32
MEM_B_CTRL	MEM_55S	MEM_CTRL	MEM B ODT<3..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<15..0>	8 11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BA<2..0>	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L	11 29 30 32
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L	11 29 30 32
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM B DQ<7..0>	11 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM B DQ<15..8>	11 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM B DQ<23..16>	11 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM B DQ<31..24>	11 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM B DQ<39..32>	11 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM B DQ<47..40>	11 30
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM B DQ<55..48>	11 30
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM B DQ<63..56>	11 30
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	11 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	11 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	11 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	11 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>	11 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	11 30
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	11 30
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	11 30
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	11 30
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	11 30
		MEM_PWR	PP1V5_S3RS0	6 7
		MEM_PWR	PP1V5_S3	6 7
		MEM_PWR	PP0V75_S3_MEM_VREFCA_A	27 28 29 30 31
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	9 27 28 29 30 31

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_PWR	*	MEM_2PWR
MEM_CTRL	MEM_PWR	*	MEM_2PWR
MEM_CMD	MEM_PWR	*	MEM_2PWR
MEM_DATA	MEM_PWR	*	MEM_2PWR
MEM_DQS	MEM_PWR	*	MEM_2PWR

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	MEM_2GND
MEM_CTRL	GND	*	MEM_2GND
MEM_CMD	GND	*	MEM_2GND
MEM_DATA	GND	*	MEM_2GND
MEM_DQS	GND	*	MEM_2GND

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2CLK	*	0.6 MM	?
MEM_CTRL2CTRL	*	0.2 MM	?
MEM_CMD2CTRL	*	0.2 MM	?
MEM_CMD2CMD	*	0.2 MM	?
MEM_DATA2DATA	*	0.14 MM	?
MEM_DQS2DQS	*	0.4 MM	?
MEM_MEM2OTHERMEM	*	0.4 MM	?
MEM_2PWR	*	=PWR_P2MM	?
MEM_2GND	*	=GND_P2MM	?
MEM_2OTHER	*	0.6 MM	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_CLK	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CLK	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CMD	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CMD2CTRL
MEM_CTRL	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_CTRL	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_MEM2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CTRL	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_CMD	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DATA	*	MEM_MEM2OTHERMEM
MEM_DQS	MEM_DQS	*	MEM_DQS2DQS

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines per Huron River SFF DG rev1.0 (#438297).

DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.

DQ to DQS matching per byte lane should be within 0.127mm.

DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].

CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.

CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.

A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.

DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.

Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.

SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

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PAGE TITLE: Memory Constraints

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DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

BRANCH:

PAGE: 101 OF 109

SHEET: 67 OF 74

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_P	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_N	8
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_P	
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<2..0>	
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<2..0>	
	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<3>	8
	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<3>	8
	LVDS_90D	LVDS	LVDS_IG_B_DATA_P<3..0>	8
	LVDS_90D	LVDS	LVDS_IG_B_DATA_N<3..0>	8
	LVDS_90D	LVDS	LVDS_IG_B_CLK_P	8
	LVDS_90D	LVDS	LVDS_IG_B_CLK_N	8
	SATA_90D	SATA	SATA_HDD_R2D_C_P	16 37
	SATA_90D	SATA	SATA_HDD_R2D_C_N	16 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_P	6 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_N	6 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	16 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N	16 37
	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 37
	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 37
	SATA_90D	SATA	SATA_ODD_R2D_C_P	8 16
	SATA_90D	SATA	SATA_ODD_R2D_C_N	8 16
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_N	
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	8 16
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_N	8 16
	SATA_90D	SATA	SATA_HDD_R2D_RC_P	
	SATA_90D	SATA	SATA_HDD_R2D_RC_N	
	SATA_90D	SATA	SATA_HDD_D2R_RC_P	
	SATA_90D	SATA	SATA_HDD_D2R_RC_N	
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	18 24
	USB_85D	USB	USB_HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	18 24
	USB_85D	USB	USB_HUB2_UP_N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P	24 38
USB_EXTA	USB_85D	USB	USB_EXTA_N	24 38
USB_EXTB	USB_85D	USB	USB_EXTB_P	
	USB_85D	USB	USB_EXTB_N	
USB_EXTC	USB_85D	USB	USB_EXTC_P	
	USB_85D	USB	USB_EXTC_N	
USB_EXTD	USB_85D	USB	USB_EXTD_P	6 24 39
	USB_85D	USB	USB_EXTD_N	6 24 39
USB_EXTD	USB_85D	USB	USB_T29A_P	8 24
	USB_85D	USB	USB_T29A_N	8 24
	USB_85D	USB	T29_A_RSVD_P	8 63
	USB_85D	USB	T29_A_RSVD_N	8 63
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	6 18 39
	USB_85D	USB	USB_CAMERA_N	6 18 39
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	
	USB_85D	USB	USB_CAMERA_CONN_N	
USB_BT	USB_85D	USB	USB_BT_P	6 24 36
USB_BT	USB_85D	USB	USB_BT_N	6 24 36
USB_TPAD	USB_85D	USB	USB_TPAD_P	48
	USB_85D	USB	USB_TPAD_N	48
USB_IR	USB_85D	USB	USB_IR_P	
	USB_85D	USB	USB_IR_N	
USB_SDCARD	USB_85D	USB	USB_SDCARD_P	8 24
	USB_85D	USB	USB_SDCARD_N	8 24
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	
	USB_85D	USB	USB_BRCRYPT_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16 25
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_P	
	CLK_PCIE_90D	CLK_PCIE	FSB_CLK133M_PCH_N	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16 25
PCH_DIFFCLK_UNUSED_	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16 25
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16 25
LPC_CLK33M	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 25
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	

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PAGE TITLE
PCH Constraints 1

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DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
BRANCH
PAGE 102 OF 109
SHEET 68 OF 74

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

DisplayPort Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	LPC_50S	LPC	LPC AD<3..0>	6 16 40 42
	LPC_50S	LPC	LPC FRAME L	6 16 40 42
	LPC_50S	LPC	LPC RESET L	25
	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R	18 25
	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC	25 40
	CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS	6 25 42
	SMB_50S	SMB	SMBUS PCH CLK	16 43
	SMB_50S	SMB	SMBUS PCH DATA	16 43
	SMB_50S	SMB	SML PCH 0 CLK	16 43
	SMB_50S	SMB	SML PCH 0 DATA	16 43
	SMB_50S	SMB	SML PCH 1 CLK	16 43
	SMB_50S	SMB	SML PCH 1 DATA	16 43
	HDA_50S	HDA	HDA BIT CLK	6 16 39
	HDA_50S	HDA	HDA BIT CLK R	16
	HDA_50S	HDA	HDA SYNC	6 16 39
	HDA_50S	HDA	HDA SYNC R	16
	HDA_50S	HDA	HDA RST R L	16
	HDA_50S	HDA	HDA RST L	6 16 39
	HDA_50S	HDA	HDA SDIN0	6 16 39
	HDA_50S	HDA	AUD SDI R	
	HDA_50S	HDA	HDA SDOUT	6 16 39
	HDA_50S	HDA	HDA SDOUT R	16
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	
	SPI_55S	SPI	SPI CLK R	16 42
	SPI_55S	SPI	SPI CLK	42
	SPI_55S	SPI	SPI MOSI R	16 42
	SPI_55S	SPI	SPI MOSI	42
	SPI_55S	SPI	SPI MISO	16 42
	SPI_55S	SPI	SPI CS0 R L	16 42
	SPI_55S	SPI	SPI CS0 L	42
	SPI_55S	SPI	SPI MLB CLK	42 49
	SPI_55S	SPI	SPI MLB MOSI	42 49
	SPI_55S	SPI	SPI MLB MISO	42 49
	SPI_55S	SPI	SPI MLB CS L	42 49
	PCIE_85D	PCIE	PCIE ENET R2D P	
	PCIE_85D	PCIE	PCIE ENET R2D N	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C P	
	PCIE_85D	PCIE	PCIE ENET R2D C N	
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R P	
	PCIE_85D	PCIE	PCIE ENET D2R N	
	PCIE_85D	PCIE	PCIE ENET D2R C P	
	PCIE_85D	PCIE	PCIE ENET D2R C N	
	PCIE_85D	PCIE	PCIE AP R2D P	6 36
	PCIE_85D	PCIE	PCIE AP R2D N	6 36
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C P	16 36
	PCIE_85D	PCIE	PCIE AP R2D C N	16 36
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R P	6 16 36
	PCIE_85D	PCIE	PCIE AP D2R N	6 16 36
	PCIE_85D	PCIE	PCIE FW R2D P	
	PCIE_85D	PCIE	PCIE FW R2D N	
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE FW R2D C P	
	PCIE_85D	PCIE	PCIE FW R2D C N	
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE FW D2R P	
	PCIE_85D	PCIE	PCIE FW D2R N	
	PCIE_85D	PCIE	PCIE FW D2R C P	
	PCIE_85D	PCIE	PCIE FW D2R C N	
PCIE_AP_D2R	PCIE_85D	PCIE	CONN PCIE AP D2R P	
	PCIE_85D	PCIE	CONN PCIE AP D2R N	
PCIE_AP_R2D	PCIE_85D	PCIE	CONN PCIE AP R2D P	
	PCIE_85D	PCIE	CONN PCIE AP R2D N	
	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M P	8 16
	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M N	8 16
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET P	
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET N	
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP P	6 16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP N	6 16 36
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW P	
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW N	
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M EXCARD P	8 16
	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M EXCARD N	8 16
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6
	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 69
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 69
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6
	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_EXTA_ML	DISPLAYPORT	DP EXTA ML C P<3..0>	8 63
	DP_EXTA_ML	DISPLAYPORT	DP EXTA ML C N<3..0>	8 63
	DP_EXTA_ML	DISPLAYPORT	DP EXTA ML P<3..0>	63
	DP_EXTA_ML	DISPLAYPORT	DP EXTA ML N<3..0>	63
	DP_EXTA_AUXCH	DISPLAYPORT	DP EXTA AUXCH C P	8 63
	DP_EXTA_AUXCH	DISPLAYPORT	DP EXTA AUXCH C N	8 63
	DP_EXTA_AUXCH	DISPLAYPORT	DP EXTA AUXCH P	63
	DP_EXTA_AUXCH	DISPLAYPORT	DP EXTA AUXCH N	63
	DP_INT_ML	DISPLAYPORT	DP INT ML C P<3..0>	62
	DP_INT_ML	DISPLAYPORT	DP INT ML C N<3..0>	62
	DP_INT_ML	DISPLAYPORT	DP INT ML P<3..0>	9 62
	DP_INT_ML	DISPLAYPORT	DP INT ML N<3..0>	9 62
	DP_INT_ML	DISPLAYPORT	DP INT ML F P<3..0>	6 62
	DP_INT_ML	DISPLAYPORT	DP INT ML F N<3..0>	6 62
	DP_INT_AUXCH	DISPLAYPORT	DP INT AUX CH C P	6 62
	DP_INT_AUXCH	DISPLAYPORT	DP INT AUX CH C N	6 62
	DP_INT_AUXCH	DISPLAYPORT	DP INT AUX CH P	9 62
	DP_INT_AUXCH	DISPLAYPORT	DP INT AUX CH N	9 62
	PCIE_85D	PCIE	PCIE T29 R2D C P<3..0>	8 33
	PCIE_85D	PCIE	PCIE T29 R2D C N<3..0>	8 33
	PCIE_PEG_D2R_LANE3	PCIE_85D	PCIE T29 D2R P<3>	8 33
	PCIE_PEG_D2R_LANE2	PCIE_85D	PCIE T29 D2R P<2>	8 33
	PCIE_PEG_D2R_LANE1	PCIE_85D	PCIE T29 D2R P<1>	8 33
	PCIE_PEG_D2R_LANE0	PCIE_85D	PCIE T29 D2R P<0>	8 33
	PCIE_PEG_D2R_LANE3	PCIE_85D	PCIE T29 D2R N<3>	8 33
	PCIE_PEG_D2R_LANE2	PCIE_85D	PCIE T29 D2R N<2>	8 33
	PCIE_PEG_D2R_LANE1	PCIE_85D	PCIE T29 D2R N<1>	8 33
	PCIE_PEG_D2R_LANE0	PCIE_85D	PCIE T29 D2R N<0>	8 33
	PCIE_PEG_R2D_LANE3	PCIE_85D	PCIE T29 R2D P<3>	33
	PCIE_PEG_R2D_LANE2	PCIE_85D	PCIE T29 R2D P<2>	33
	PCIE_PEG_R2D_LANE1	PCIE_85D	PCIE T29 R2D P<1>	33
	PCIE_PEG_R2D_LANE0	PCIE_85D	PCIE T29 R2D P<0>	33
	PCIE_PEG_R2D_LANE3	PCIE_85D	PCIE T29 R2D N<3>	33
	PCIE_PEG_R2D_LANE2	PCIE_85D	PCIE T29 R2D N<2>	33
	PCIE_PEG_R2D_LANE1	PCIE_85D	PCIE T29 R2D N<1>	33
	PCIE_PEG_R2D_LANE0	PCIE_85D	PCIE T29 R2D N<0>	33
	PCIE_85D	PCIE	PCIE T29 D2R C P<3..0>	33
	PCIE_85D	PCIE	PCIE T29 D2R C N<3..0>	33
	PCIE_CLK100M_T29	CLK_PCIE_90D	PCIE CLK100M T29 P	16 33
	PCIE_CLK100M_T29	CLK_PCIE_90D	PCIE CLK100M T29 N	16 33

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK CLK32K RTC	16 25
SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK CLK25M SB	16 25
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M SB R	16
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M ENET	
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M ENET R	
SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29	25 33
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29 R	33

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE

PCH Constraints 2

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DRAWING NUMBER 051-8871 SIZE D

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PAGE 103 OF 109

SHEET 69 OF 74

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO
	ENET_50S	ENET_3X	ENET_RESET_L
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>
1166 CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>
1167 CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_CMD
1168 CR_CLK	ENET_50S	ENET_CR_DATA	ENET_CR_CLK
1169 CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>
1170 CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_CMD
1171 CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
1158 FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P
1159 FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N
1160 FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P
1161 FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N
1162 FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P
1163 FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N
1164 FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P
1165 FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N

Port 2 Not Used

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE
Ethernet/FW Constraints

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DRAWING NUMBER 051-8871 SIZE D
REVISION 2.5.0
BRANCH
PAGE 104 OF 109
SHEET 70 OF 74

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

DP/T29 Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 Net Properties

T29 IC Net Properties

T29/DP Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T263		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	8 33
T262		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	8 33
T264	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	33
T260	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	33
T268		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	8 33
T267		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	8 33
T266	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	33
T269	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	33
T276		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	
T271		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	
T272	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	
T273	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	
T274		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	
T275		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	
T270	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	
T277	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	
T283		T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 43
T282		T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 43
T284	T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
T285	T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
T286	T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
T287	T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
T288		T29DP_80D	T29DP	T29_R2D_C_P<3..0>	33 63
T289		T29DP_80D	T29DP	T29_R2D_C_N<3..0>	33 63
T290		T29DP_80D	T29DP	T29_D2R_P<3..0>	33 63
T291		T29DP_80D	T29DP	T29_D2R_N<3..0>	33 63
T292	T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	63
T293	T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	63
T294	T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	63
T295	T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	63
T296		T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	
T297		T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	
T298	T29_D2R0	T29DP_80D	T29DP	T29_D2R_C_P<0>	63 64
T299	T29_D2R0	T29DP_80D	T29DP	T29_D2R_C_N<0>	63 64
T300	T29_D2R1	T29DP_80D	T29DP	T29_D2R_C_P<1>	63 64
T301	T29_D2R1	T29DP_80D	T29DP	T29_D2R_C_N<1>	63 64
T302		T29DP_80D	T29DP	T29DPA_D2R1_AUXCH_P	64
T303		T29DP_80D	T29DP	T29DPA_D2R1_AUXCH_N	64
T304		T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	63
T305		T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	63
T306		T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	63
T307		T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	63
T308	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<0>	63
T309	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<0>	63
T310	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<1>	63
T311	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<1>	63
T312	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2>	63
T313	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2>	63
T314	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3>	63
T315	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3>	63
T316	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	63
T317	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	63
T318		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	63
T319		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	63
T320	T29DPA_ML_ODD			T29DPA_ML_P<1>	63 64 71
T322	T29DPA_ML_ODD			T29DPA_ML_N<1>	63 64 71
T323	T29DPA_ML_ODD			T29DPA_ML_P<3>	63 64 71
T324	T29DPA_ML_ODD			T29DPA_ML_N<3>	63 64 71
T325		T29DP_80D	T29DP	T29DPA_ML_P<3..0>	63 64 71
T327		T29DP_80D	T29DP	T29DPA_ML_N<3..0>	63 64 71
T328		T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	63 64
T329		T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	63 64
T330	DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	63 64
T331	DP_A_EXT_AUXCH	T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	63 64

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE: T29 Constraints

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DRAWING NUMBER: 051-8871 SIZE: D

REVISION: 2.5.0

BRANCH

PAGE: 105 OF 109

SHEET: 71 OF 74

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	43
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	43
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	43
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	43
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	43
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	43
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	43
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	43
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	43
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	52
	1TO1_DIFFPAIR		CHGR_CSI_N	52
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	52
	1TO1_DIFFPAIR		CHGR_CSO_N	52

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE

SMC Constraints

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DRAWING NUMBER 051-8871 SIZE D

REVISION 2.5.0

BRANCH

PAGE 106 OF 109

SHEET 72 OF 74

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_48S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K21/K78 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN P<3..0>	
	ENET_100D	ENETCONN	ENETCONN N<3..0>	
	SATA_90D	SATA	SATA_ODD_D2R_UF_P	
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P	
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N	
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P	
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N	
1295	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P	
1296	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N	
1297	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P	
1298	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N	
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	46
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	46
CPU_THERMD	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 46
1387	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 46
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	46
	THERM_1TO1_55S	THERM	T29_THERMD_N	46
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_MLBBOT_THMSNS_P	46
	THERM_1TO1_55S	THERM	T29_MLBBOT_THMSNS_N	46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	45
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	44 58
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	44 58
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	44 56 57
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	44 57
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	44 57
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	44 57
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	44
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	44
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	53
	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	53
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_P	56 57
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_N	56 57
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	
	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	37 45
	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	37 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	
	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	8 45
	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	8 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	45 55
	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	45 55
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N	
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	36 45
	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	36 45
	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_N	
	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_P	

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1832 SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 39 50 73
1833	DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 39 50 73
1834 MAX98300_R	DIFFPAIR	AUDIO	MAX98300_R_P	50
1835	DIFFPAIR	AUDIO	MAX98300_R_N	50

K21/K78 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	
	1TO1_DIFFPAIR		CHGR_CSI_R_P	52
	1TO1_DIFFPAIR		CHGR_CSI_R_N	52
	1TO1_DIFFPAIR		CHGR_CSO_R_P	45 52
	1TO1_DIFFPAIR		CHGR_CSO_R_N	45 52
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	38
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	38
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	38
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	38
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
	USB_85D	USB	USB_LT2_P	
	USB_85D	USB	USB_LT2_N	
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P	
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT	6 50 51
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT	6 50 51
1899 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_N	
1900 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_P	
1901 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_N	
1902 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_P	
1903 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_N	
1904 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_P	
1905 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_R	
1906 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_R	
1907 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_N_R	
1908 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_P_R	
1909 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_L	
1910 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_L	
1911 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_P	
1912 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_N	
1913 SPKRAMP_INR	DIFFPAIR	AUDIO	SPKRAMP_INR_P	6 39 50 73
1914 AUD_DIFF	DIFFPAIR	AUDIO	SPKRAMP_INR_N	6 39 50 73
1915 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_P	
1916 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_N	
	USB_85D	USB	USB_TPAD_R_P	
	USB_85D	USB	USB_TPAD_R_N	
		SB_POWER	PP3V3_S5	6 7
		SB_POWER	PP3V3_S0	6 7
		GND	GND	

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1917 (USB_EXTA)	USB_85D	USB	USB_EXTA_MUXED_P	
1918 (USB_EXTA)	USB_85D	USB	USB_EXTA_MUXED_N	
1919 (USB_EXTA)	USB_85D	USB	USB_LT1_P	
1920 (USB_EXTA)	USB_85D	USB	USB_LT1_N	
1921 (USB_TPAD)	USB_85D	USB	USB_TPAD_CONN_P	6 48
1922 (USB_TPAD)	USB_85D	USB	USB_TPAD_CONN_N	6 48
1923 SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	I2C_SMC_SMS_SDA_R	
1924 SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	I2C_SMC_SMS_SCL_R	
1925	SMB_55S	SMB	I2C_TCON_SCL	
1926	SMB_55S	SMB	I2C_TCON_SDA	
1927	SMB_55S	SMB	I2C_TCON_SCL_CONN	
1928	SMB_55S	SMB	I2C_TCON_SDA_CONN	

SYNC_MASTER=CONSTRAINTS SYNC_DATE=04/06/2011

PAGE TITLE

Project Specific Constraints

Apple Inc.

DRAWING NUMBER 051-8871 SIZE D

REVISION 2.5.0

BRANCH

PAGE 108 OF 109

SHEET 73 OF 74

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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.1 MM			
37_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.160 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.155MM	0.155 MM		0.130 MM	0.130 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL10	Y	0.095 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.115 MM	0.115 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.195 MM	0.195 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL10	Y	0.074 MM	0.074 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL10	N	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL4,ISL9	Y	0.071 MM	0.071 MM		0.300 MM	0.300 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.280 MM	0.280 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.120 MM	0.165 MM			
48_OHM_SE	*	Y	0.097 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL10	Y	0.110 MM	0.110 MM		0.170 MM	0.170 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.129 MM	0.129 MM		0.170 MM	0.170 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.180 MM	0.180 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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PAGE TITLE: PCB Rule Definitions

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REVISION: 2.5.0

BRANCH

PAGE: 109 OF 109

SHEET: 74 OF 74

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