NBQAA

Bordeaux 10G

LA-6072P REV 1.0 Schematic

Intel Arrandale CPU / Intel 5 Series Chipset
2010-03-22 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Title: **Cover Page**

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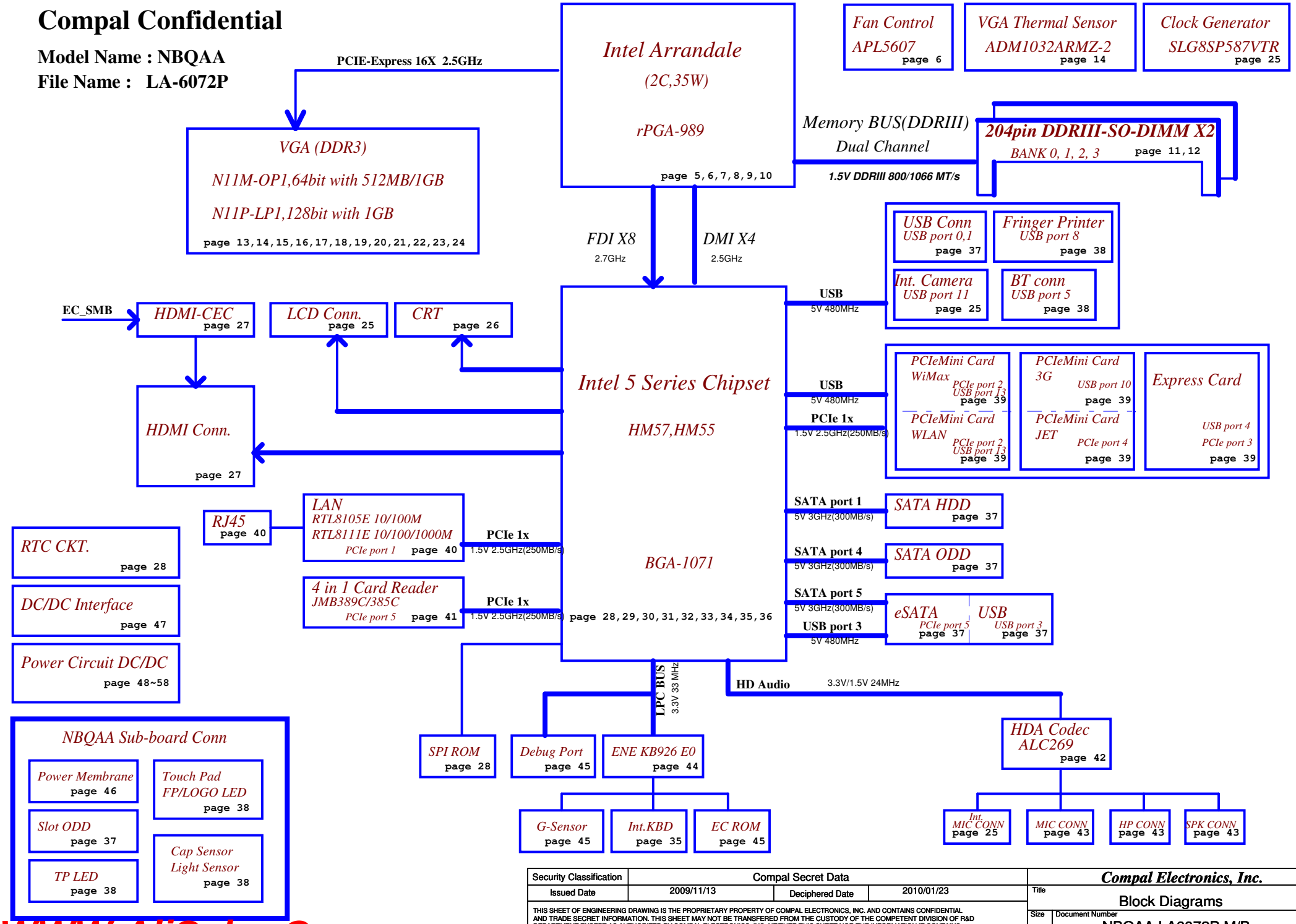
Model Name : NBQAA
File Name : LA-6072P



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Title: Block Diagrams

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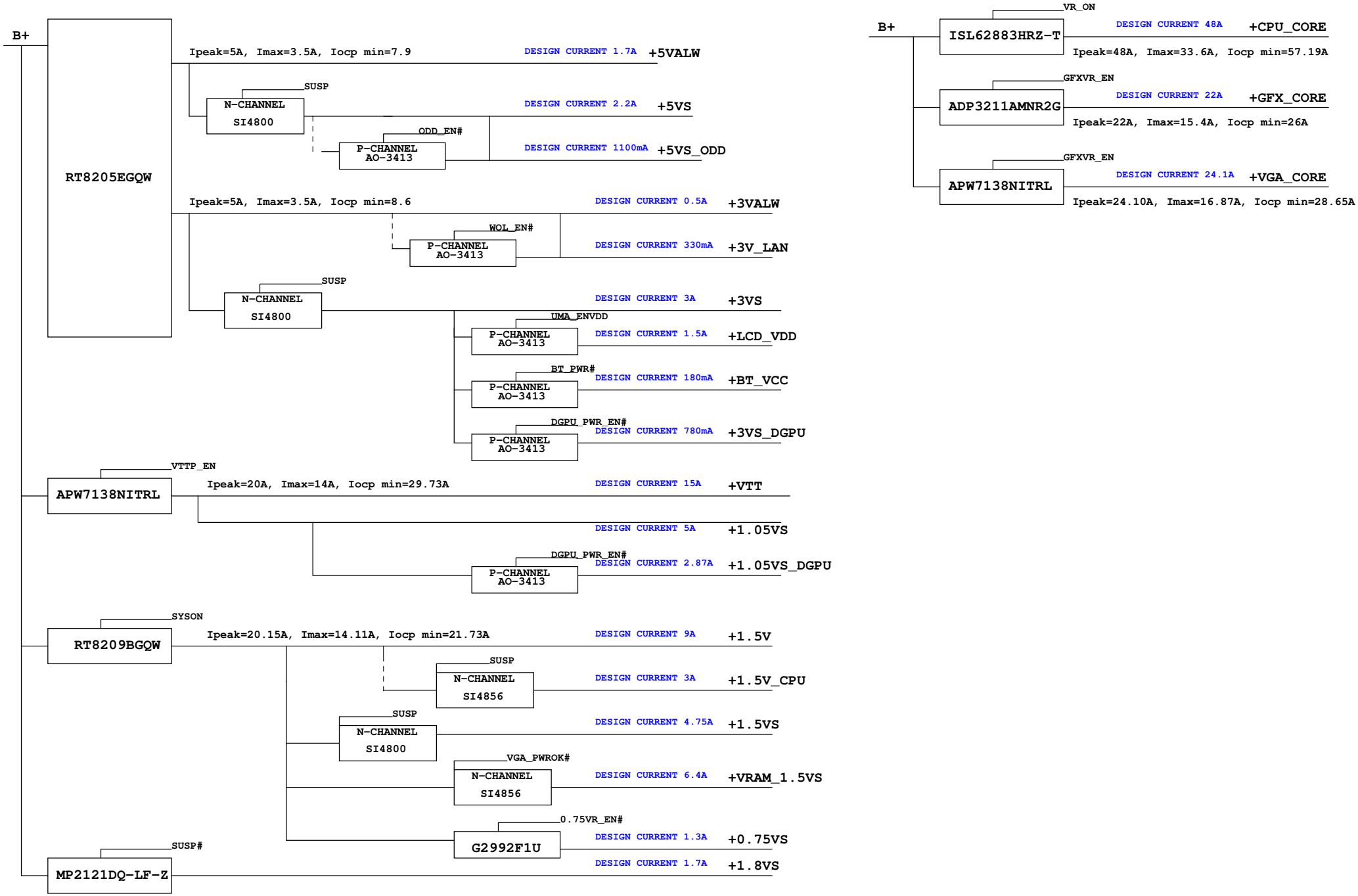
NBQAA Bordeaux Intel Arrandale (Discrete)



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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	Card Reader		HDMI-CEC		LAN		CAM+MIC
description	B				Y	U	V	X
explain	Bluetooth	JMB389	JMB385	HDMI	HDMI+CEC	10/100	10/100/1000	CAM
BTO	BT@	JMB389@	JMB385@	IHDMI@	IHDMI@+CEC@	8105E@	8111E@	CAM@

Function	ODD		KB LED	Mini Card				GPU	
description		T	K	G	J		W	P	M
explain	Normal	Slot	KB LED	3G	JET	3G/JFT	WiMAX	N11P-LP1	N11M-OP1
BTO	ODD0@	ODD1@	KBL@	3G@	JET@	3GJFT@	WiMAX@	N11P@	N11P@

Function	PCH		VRAM	
description	H5	H7	512	1G
explain	HM55	HM57	512M	1G
BTO	HM55@	HM57@	4pcs@	4pcs@+8pcs@

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

Power	Device	Address
+3VL	EC KB926 D3	
+3VL	HDMI-CEC	
+3VL	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 D3	
+3VS	AMD GPU Thermal Sensor	
+3VS	Ambient Ligh Sensor	
+3VALW	PCH	
+3VS	G-Sensor	

PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Express	
+3VS	Slot#1--WLAN/Wimax	
+3VS	Slot#2--JET/3G	

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Title: **Notes List**

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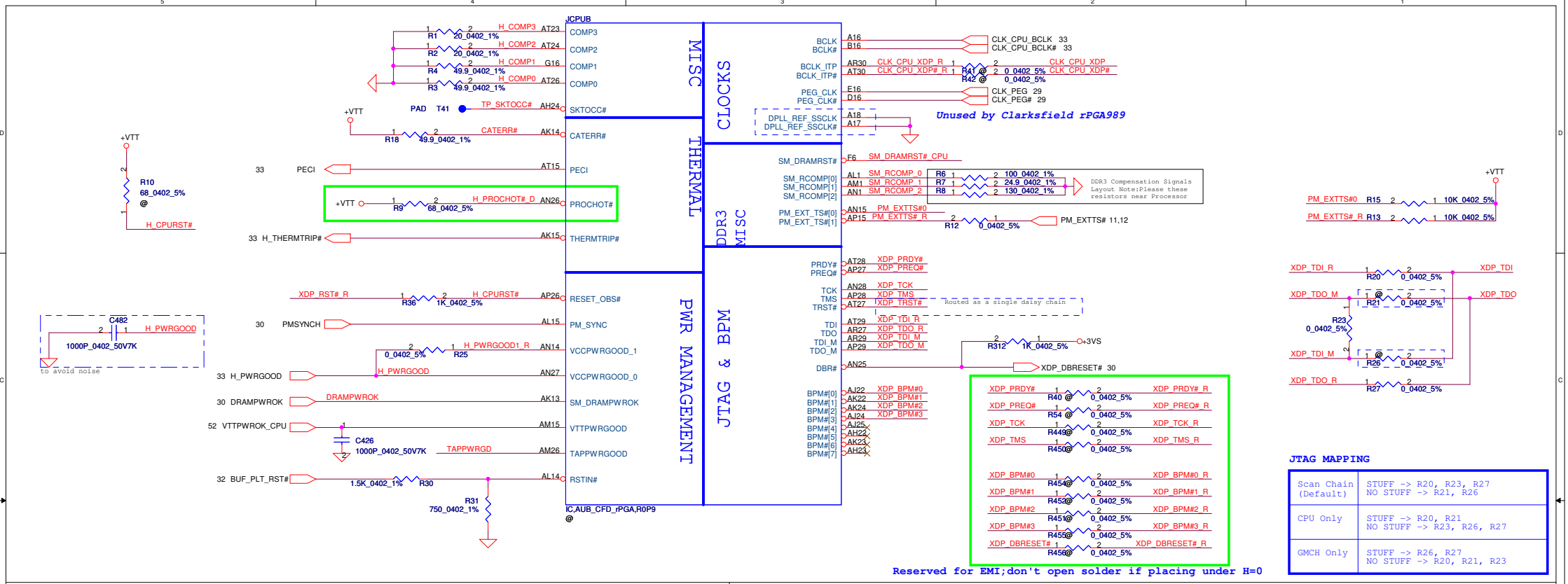

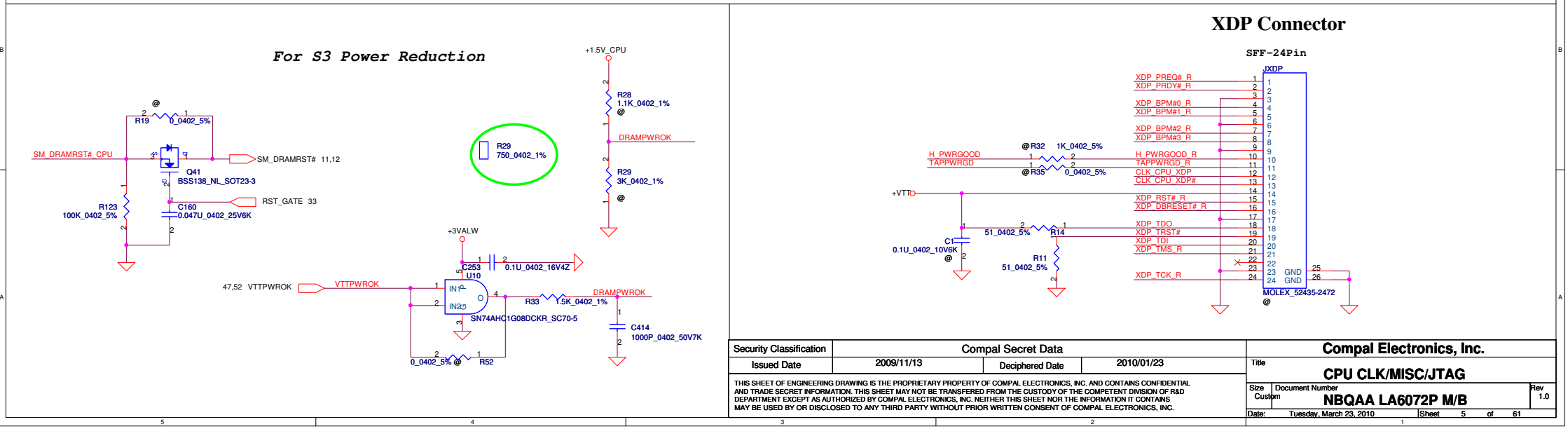

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Title: **CPU CLK/MISC/JTAG**

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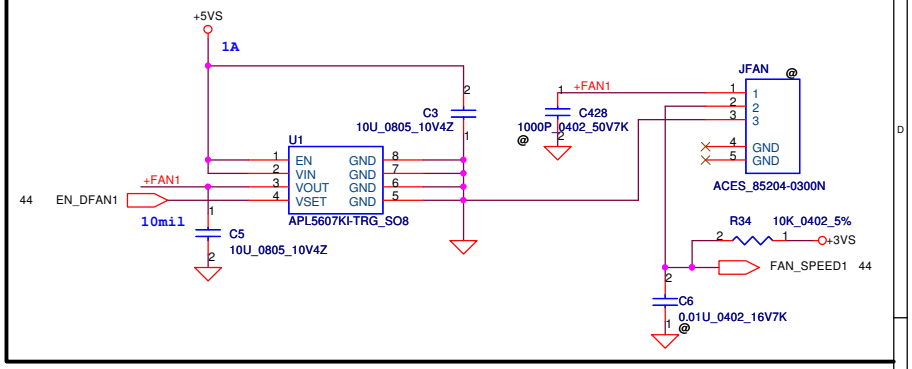
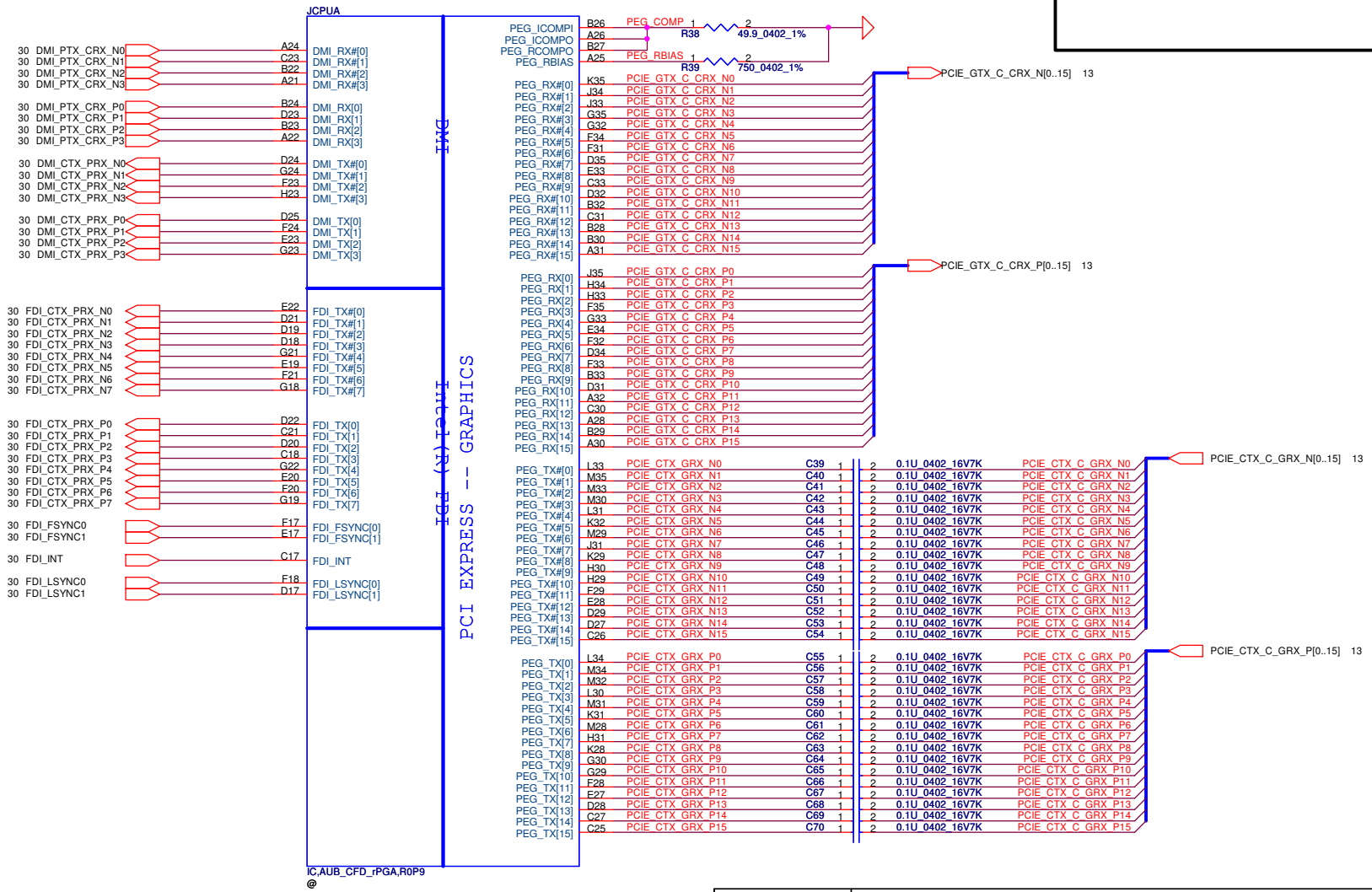
FAN Control Circuit





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Compal Electronics, Inc.

Title: **CPU DMI/FDI/PEG**

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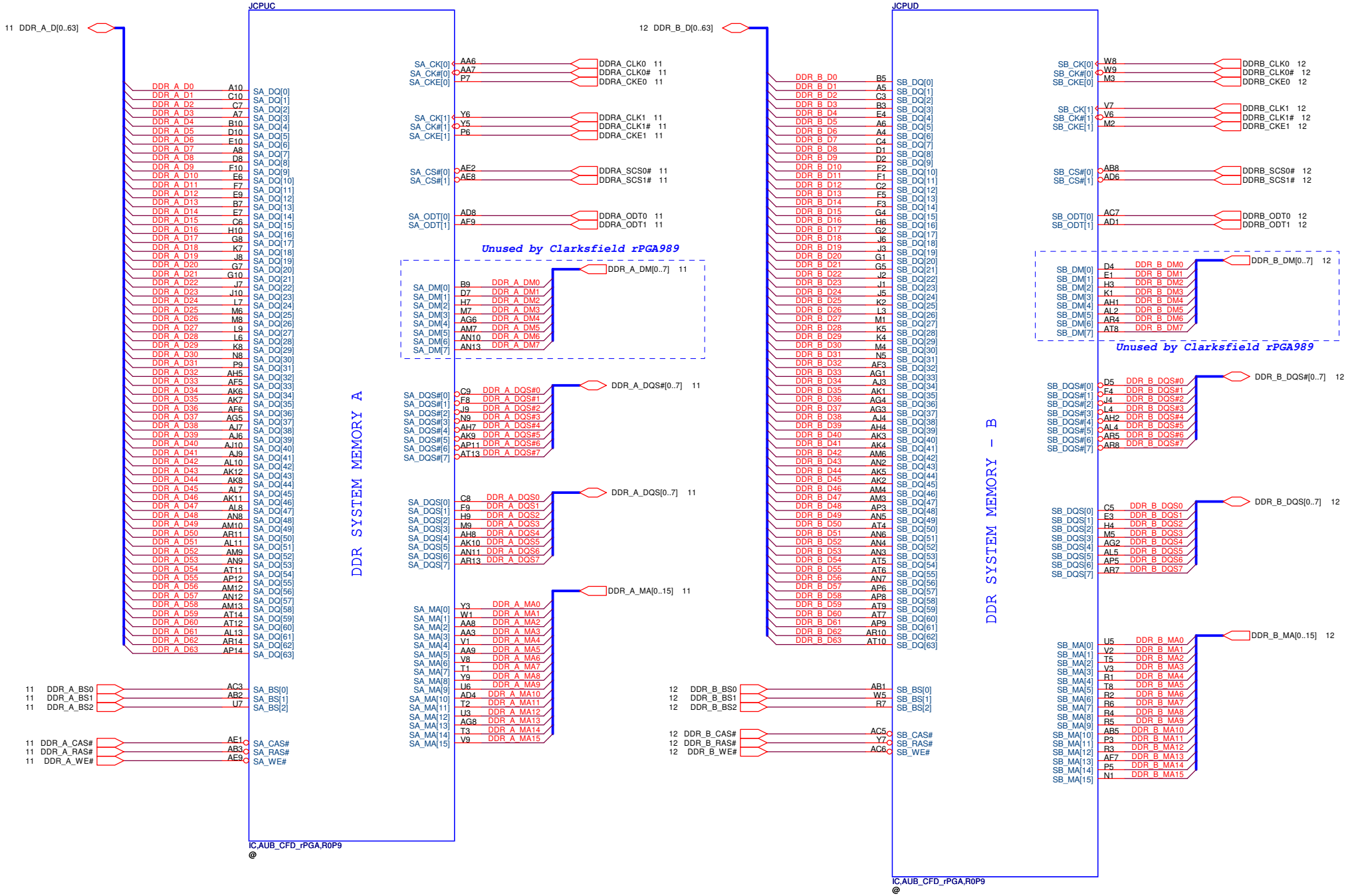

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Compal Electronics, Inc.

Title: **CPU DDRIII**

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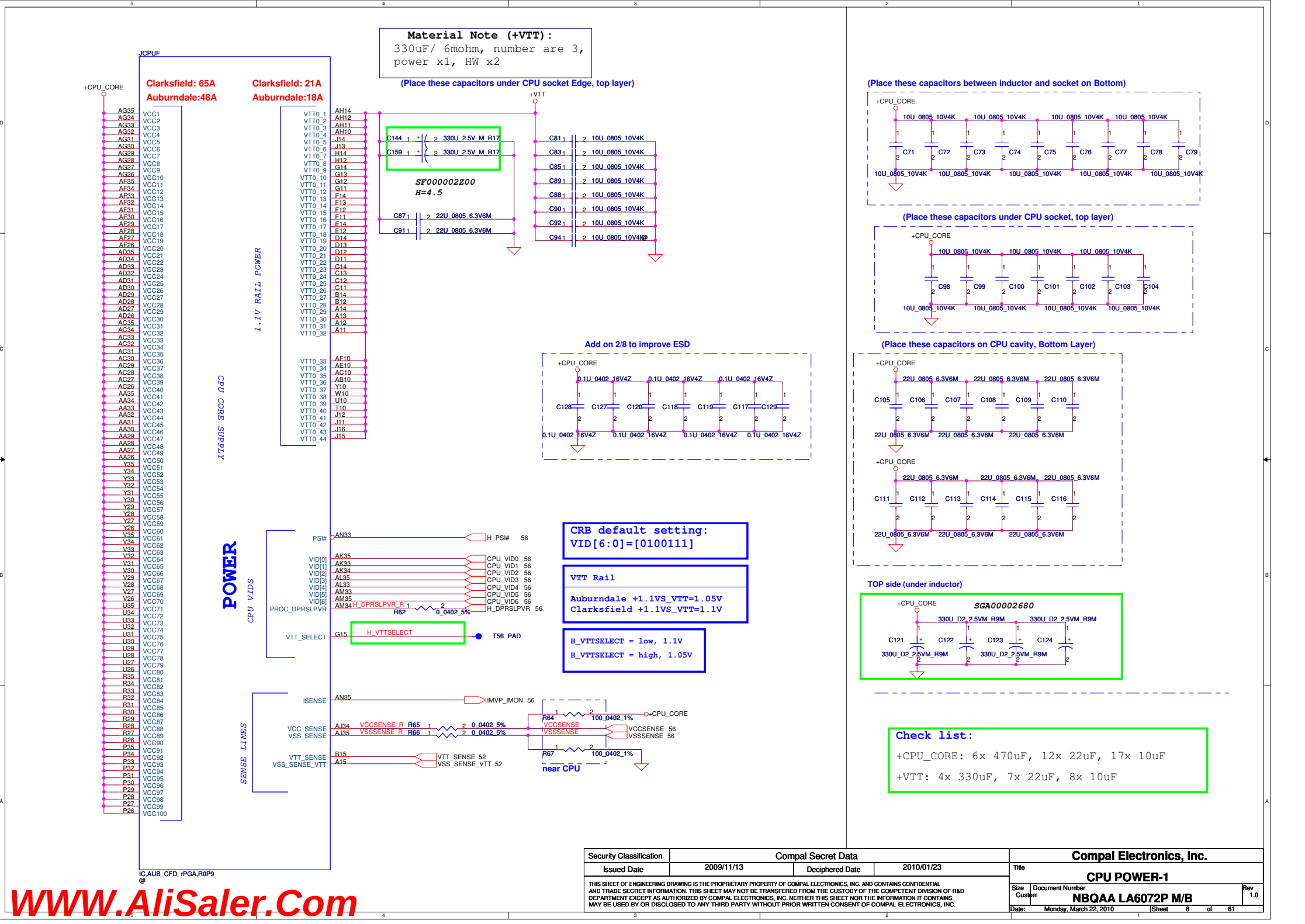

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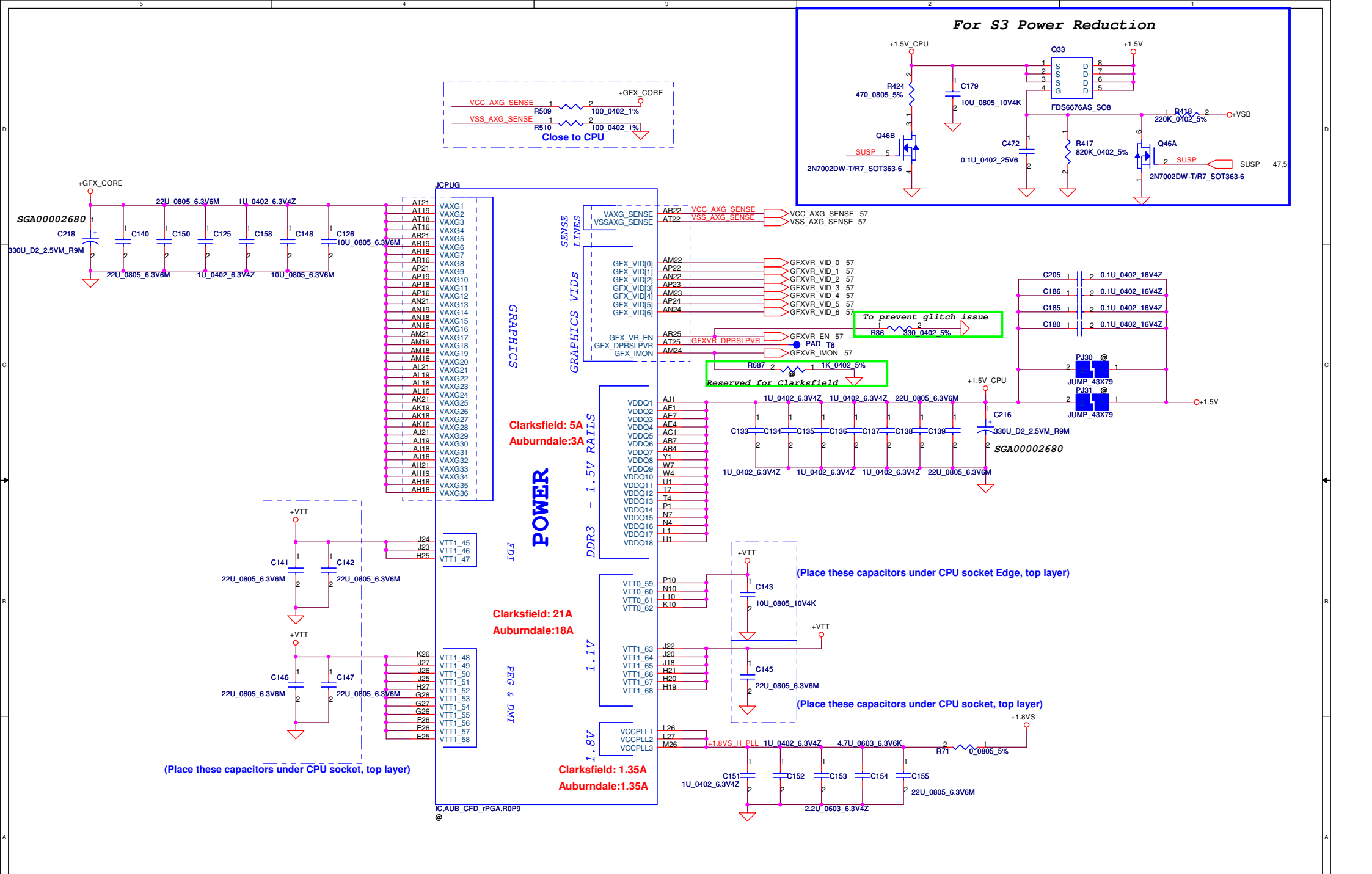

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Compal Electronics, Inc.

Title: **CPU POWER-2**

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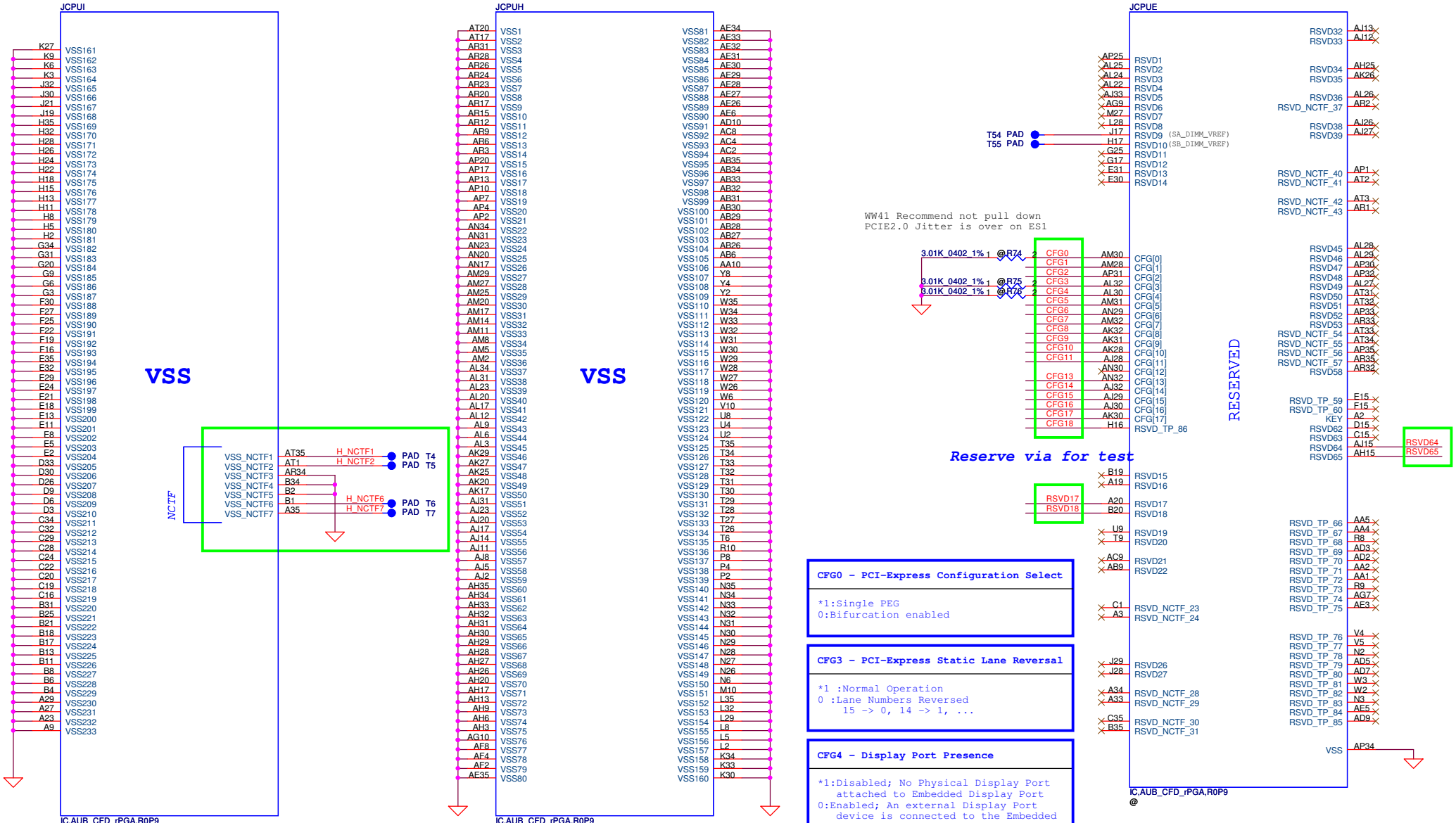

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Compal Electronics, Inc.

Title: **CPU GND/RESERVED/XDP**

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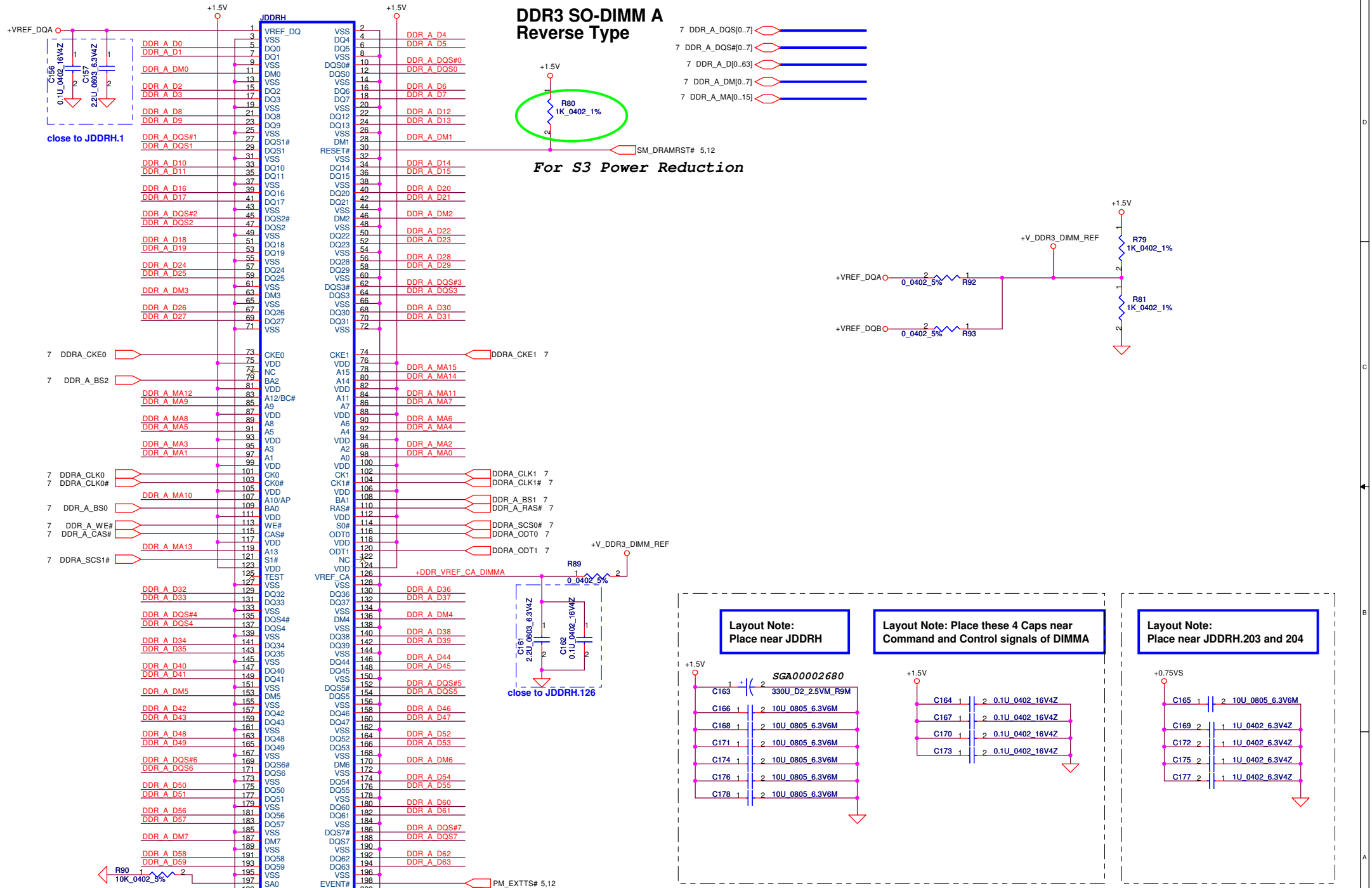
DDR3 SO-DIMM A
Reverse Type



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Title: **DDRIII-SODIMM0**

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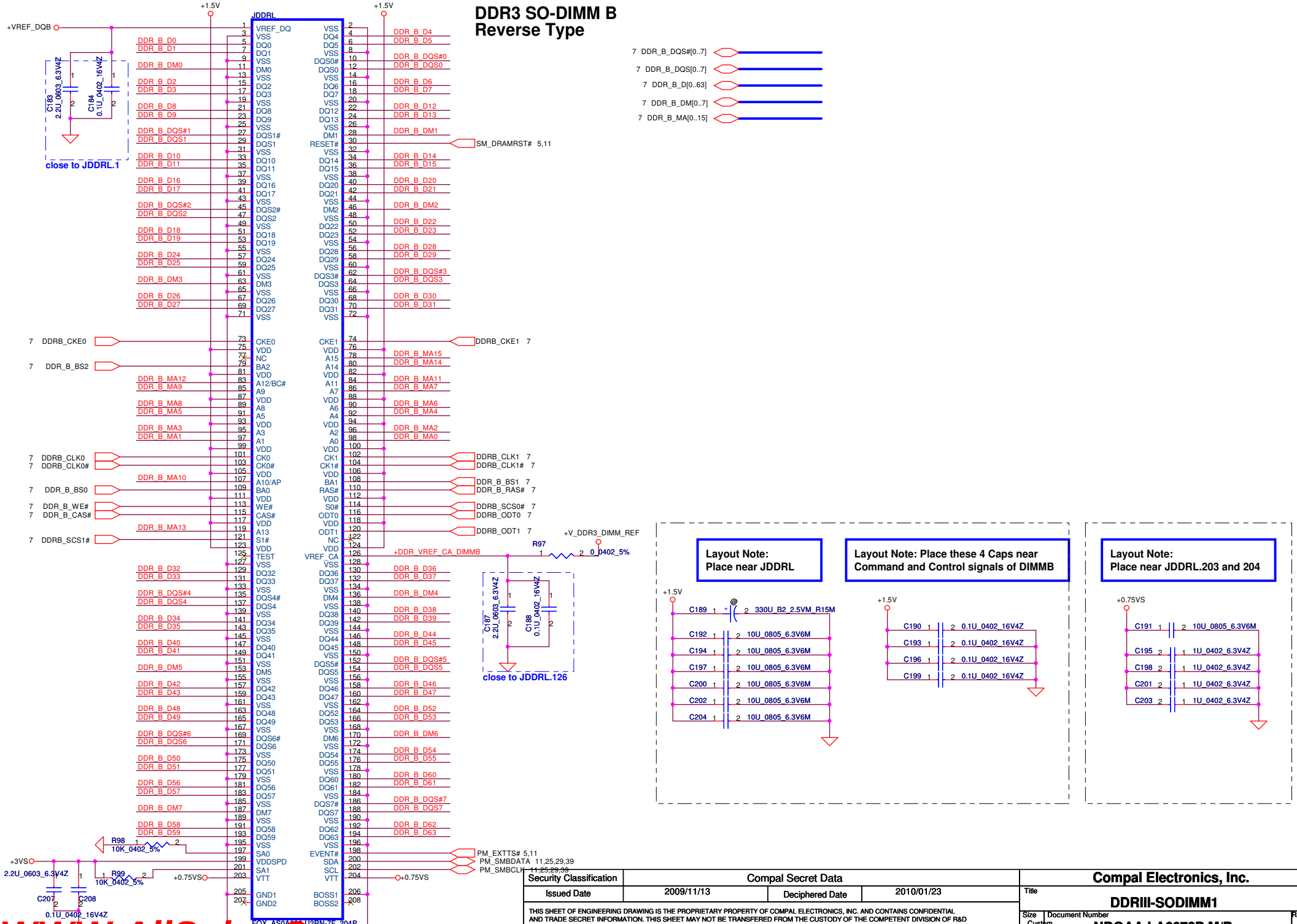
DDR3 SO-DIMM B
Reverse Type



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Compal Electronics, Inc.

Title: **DDRIII-SODIMM1**

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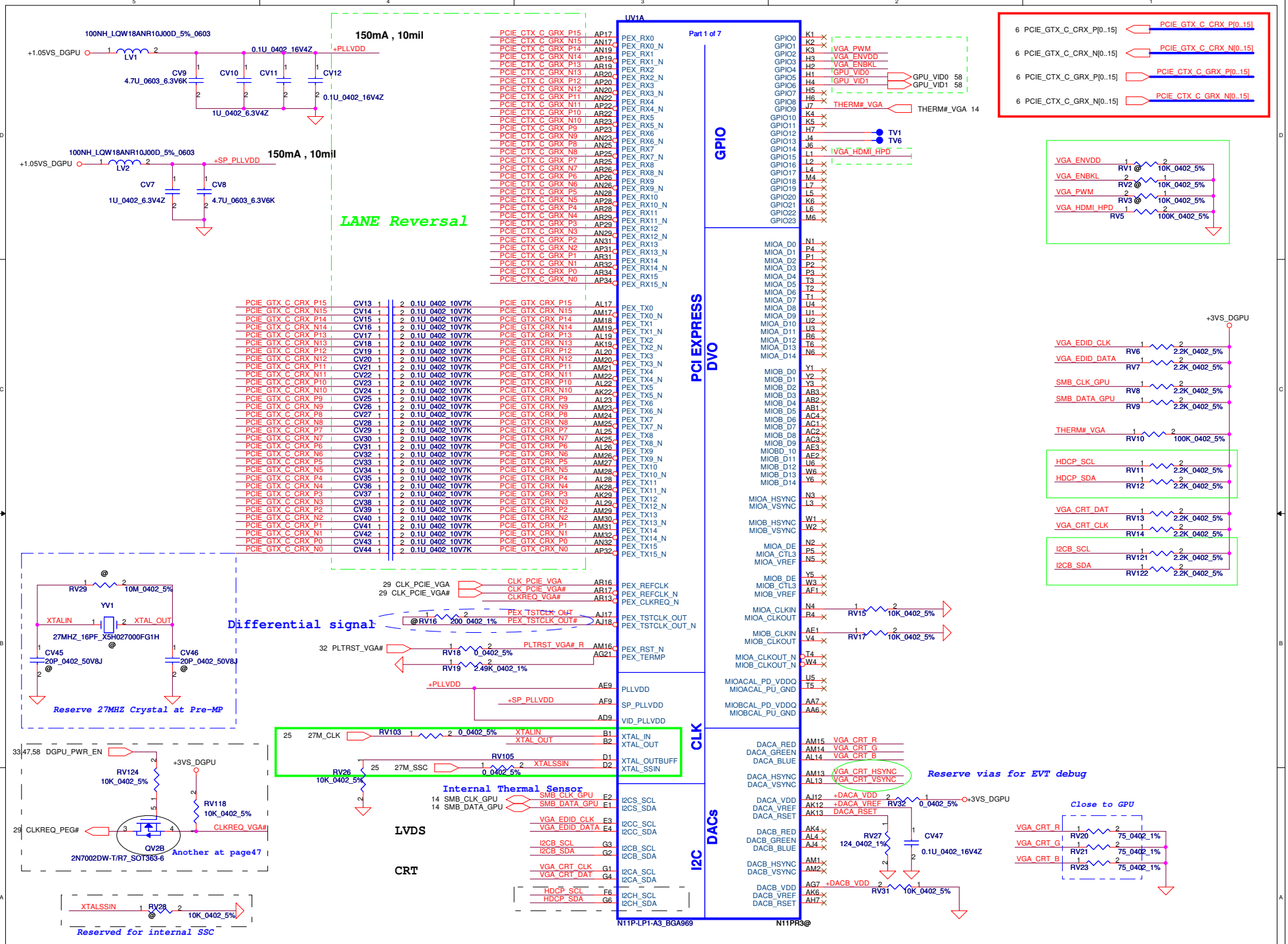

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Compal Electronics, Inc.

Title: **PCIE/DAC/GPIO**

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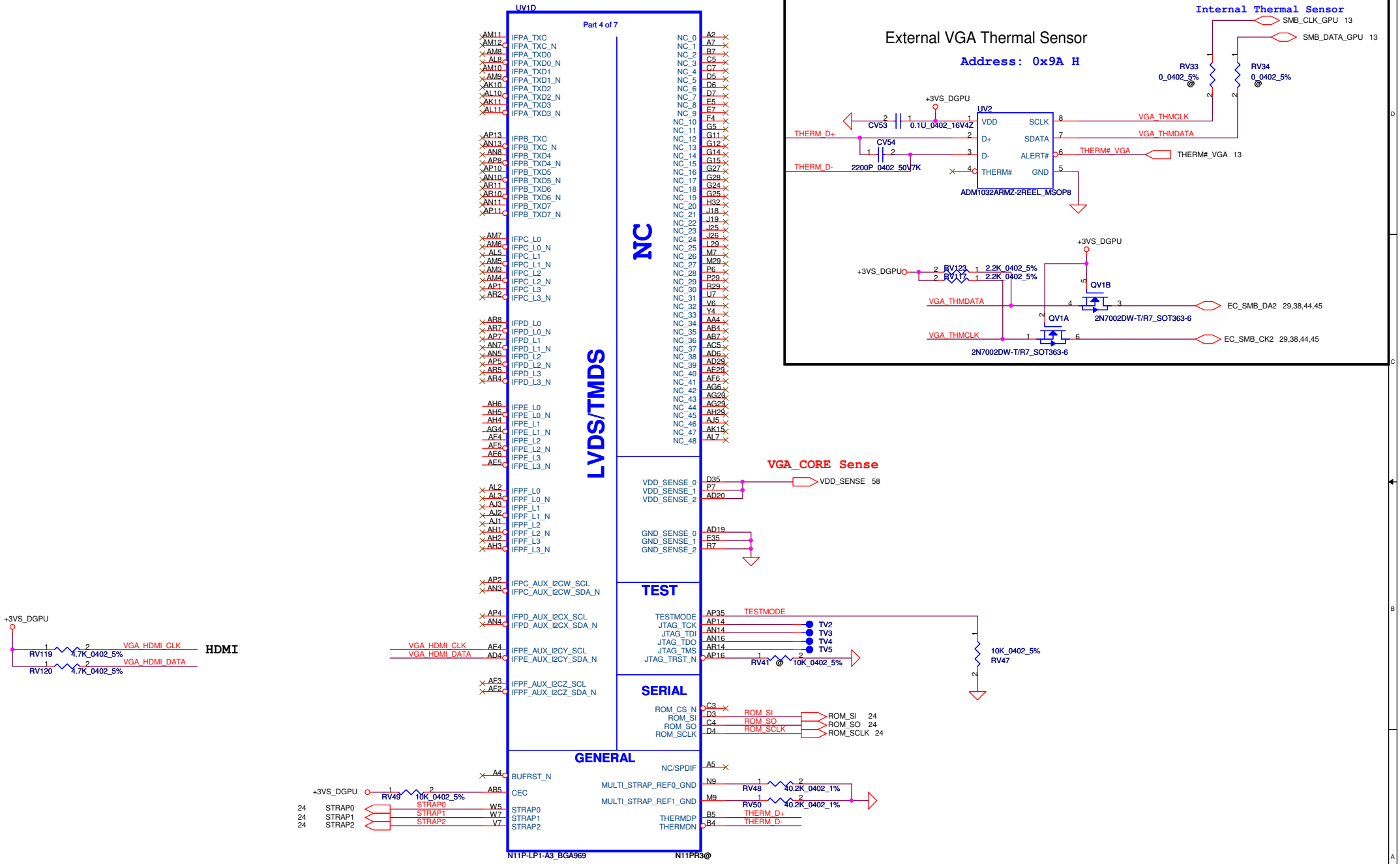

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Title: **LVDS/HDMI/DP/THM**

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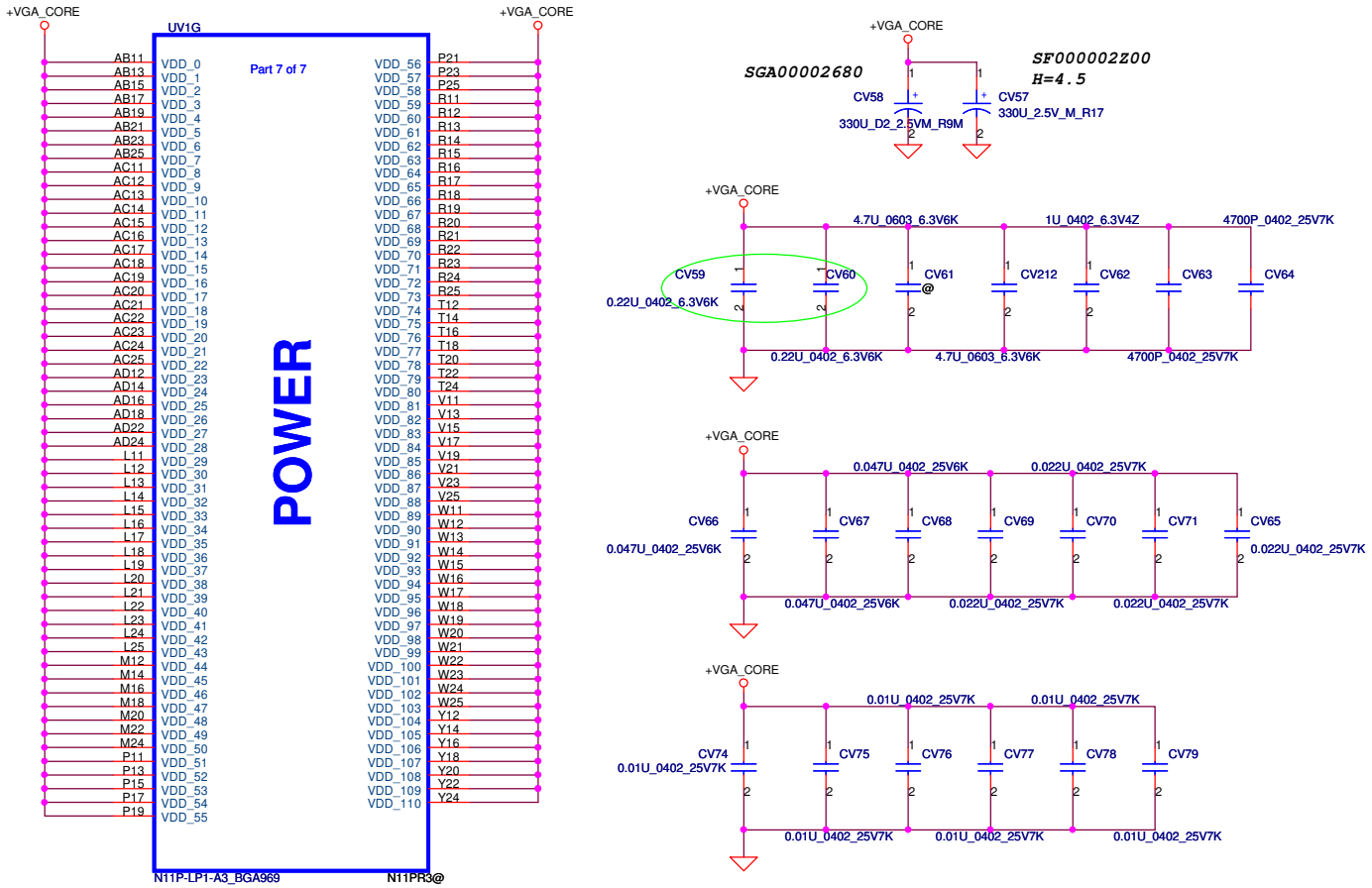

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Title: **VGA CORE**

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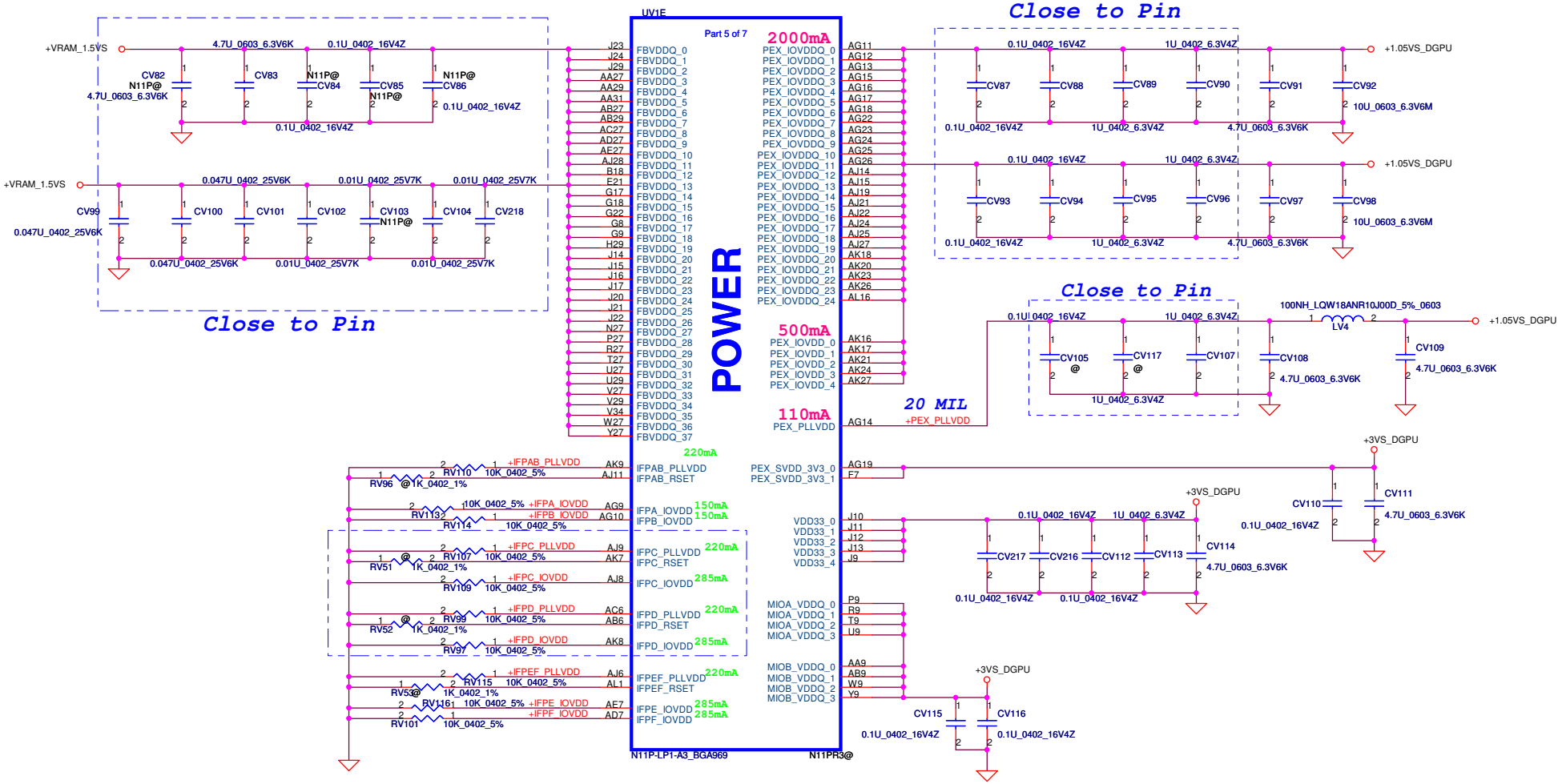

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Title: **POWER**

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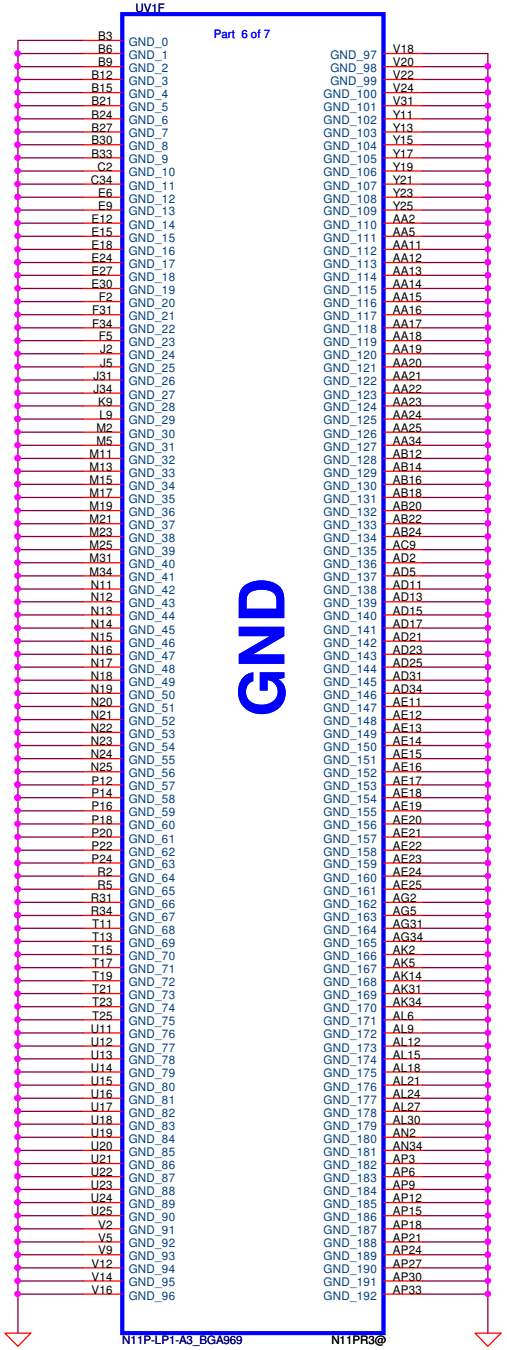

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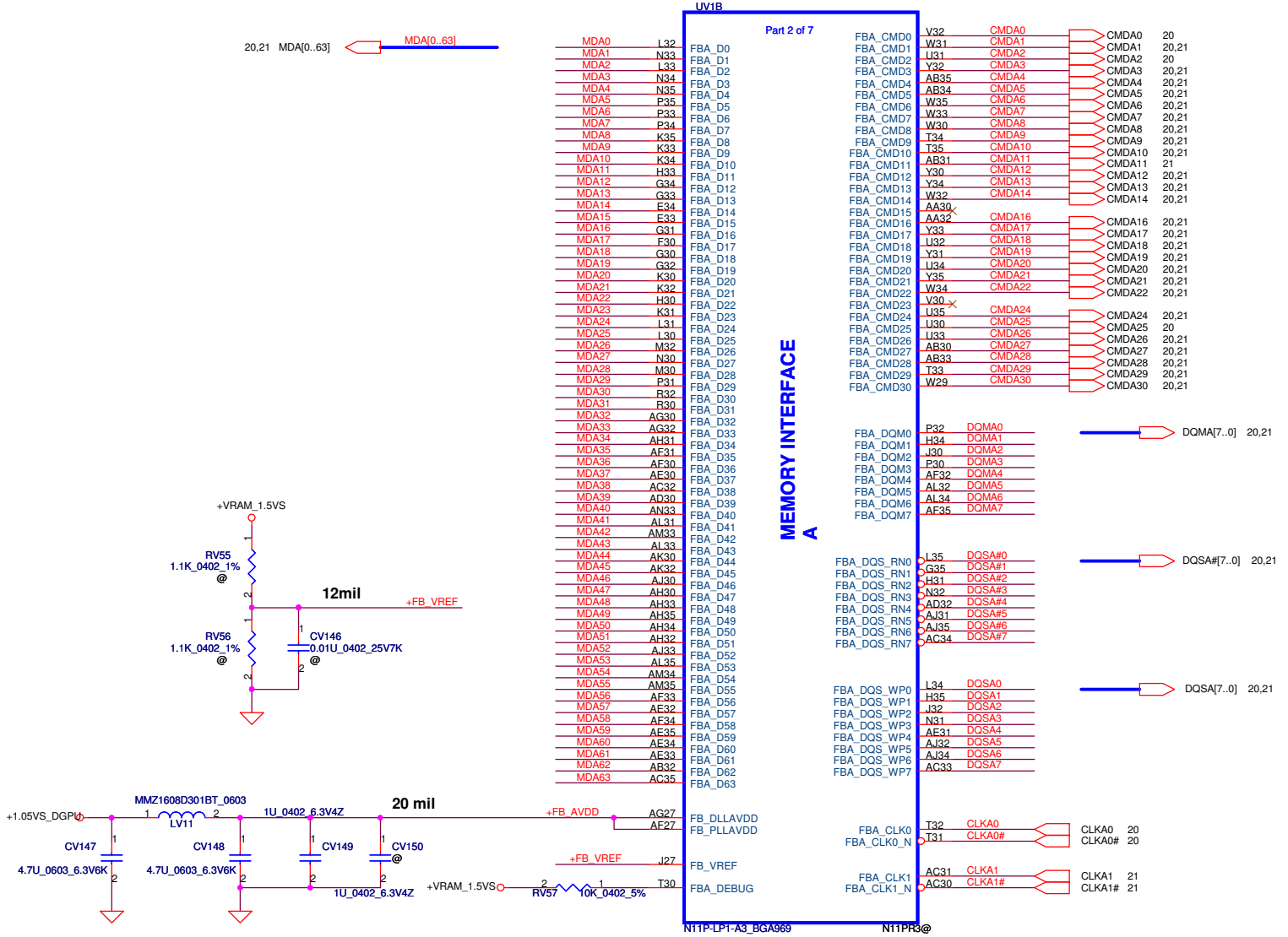

Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

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Compal Electronics, Inc.

Title: **MEM Interface A**

Size | Document Number: NBQAA LA6072P M/B | Rev 1.0

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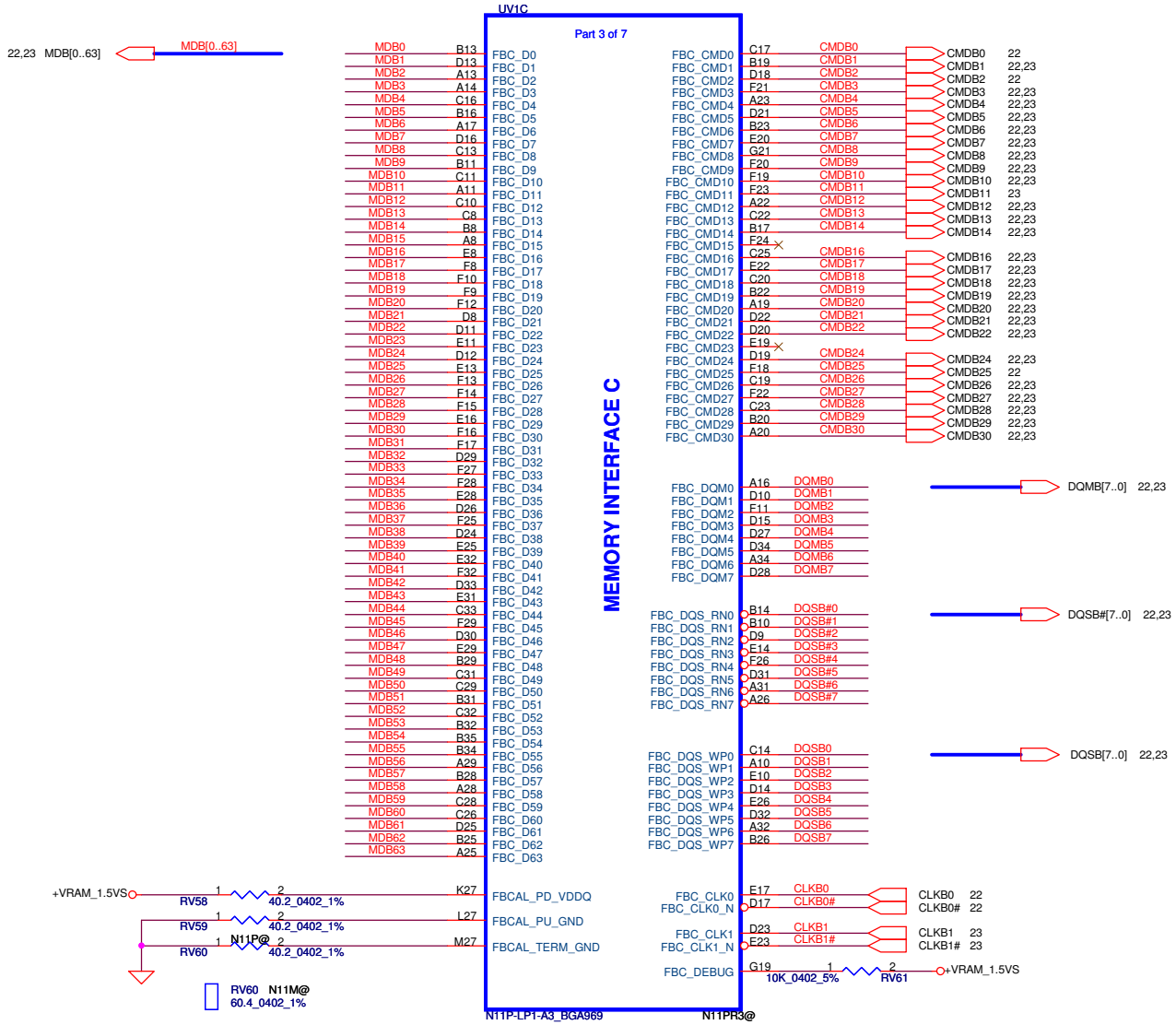

Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

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Compal Electronics, Inc.

Title: **MEM Interface C**

Size | Document Number: NBQAA LA6072P M/B | Rev 1.0

Date: Monday, March 22, 2010 | Sheet 19 of 61

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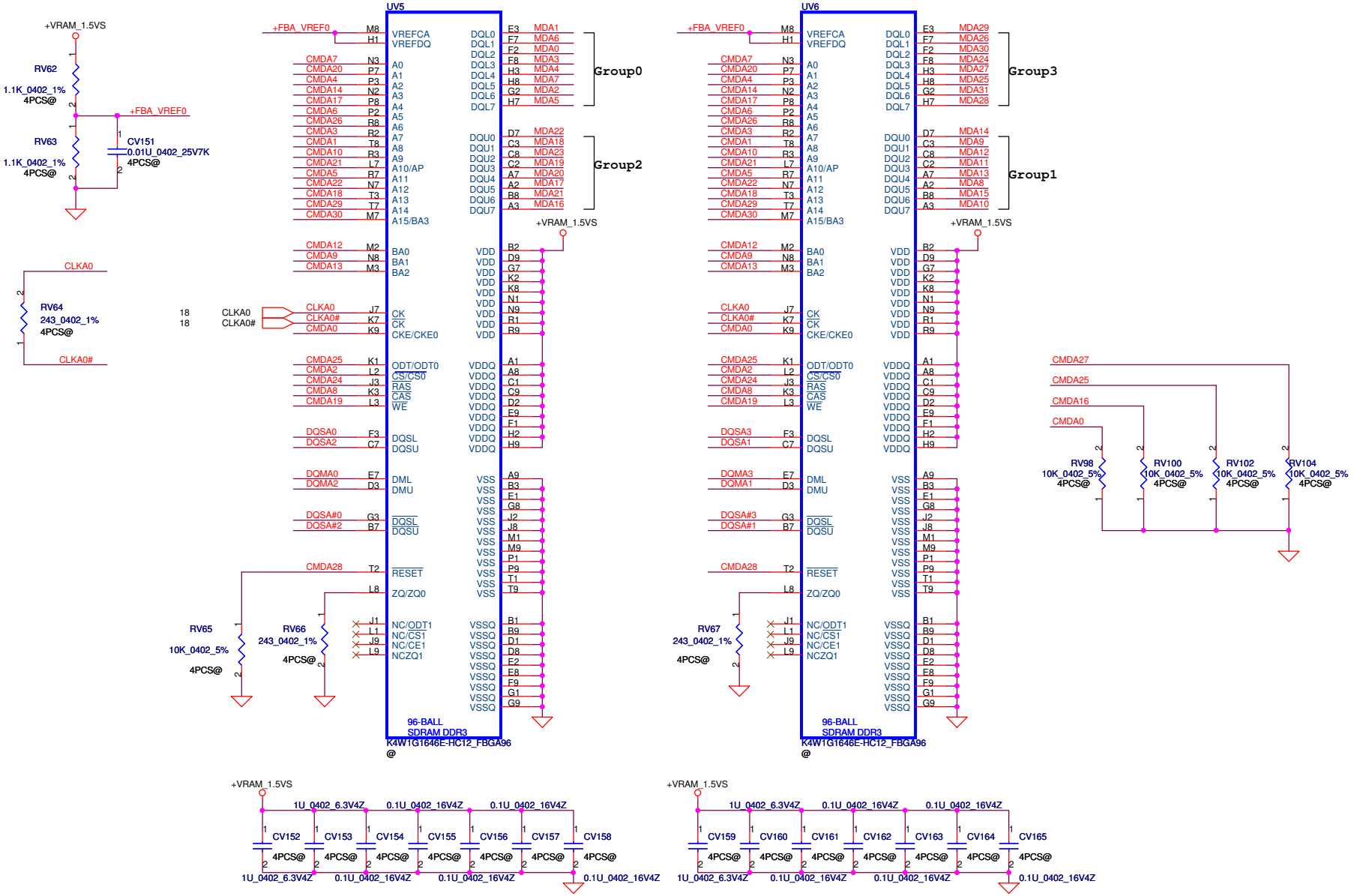
Memory Partition A - Lower 32 bits



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

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Compal Electronics, Inc.

Title: **VRAM A Lower**

Size | Document Number: **NBQAA LA6072P M/B** | Rev 1.0

Date: Monday, March 22, 2010 | Sheet 20 of 61

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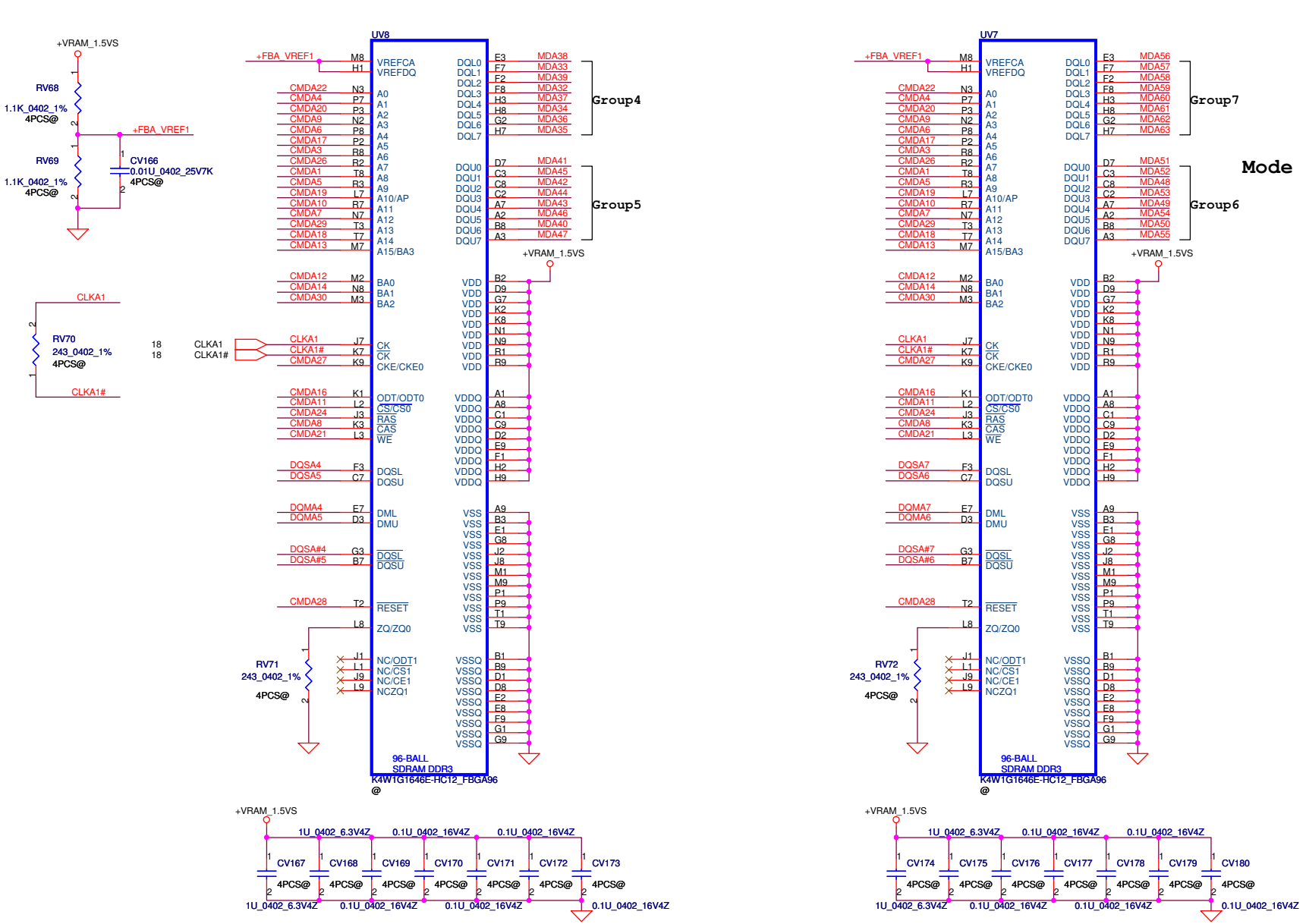
Memory Partition A - Upper 32 bits



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

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Compal Electronics, Inc.

Title: **VRAM A Upper**

Size | Document Number: **NBQAA LA6072P M/B** | Rev 1.0

Date: Monday, March 22, 2010 | Sheet 21 of 61

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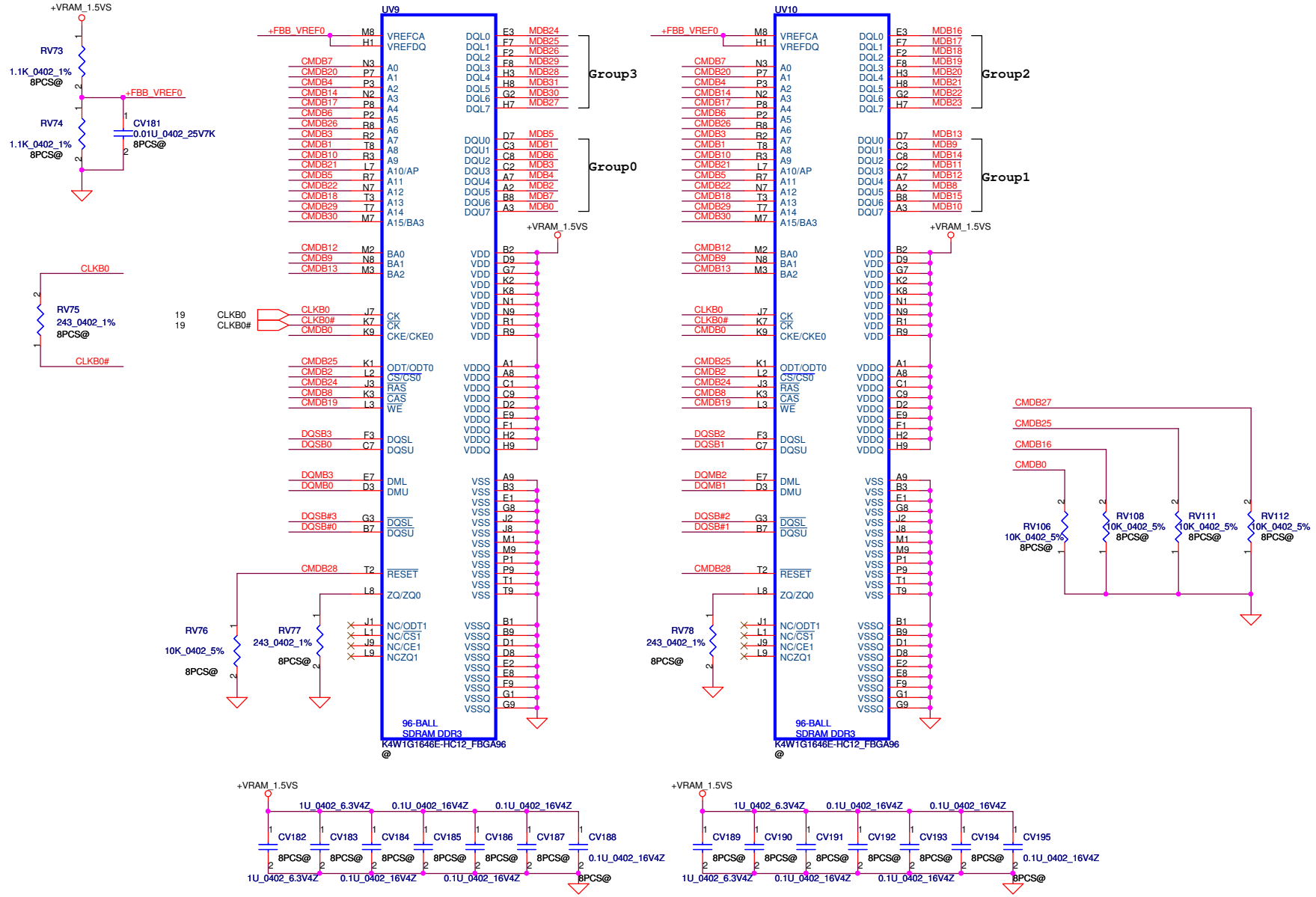
Memory Partition C - Lower 32 bits



Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

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Compal Electronics, Inc.

Title: **VRAM C Lower**

Size: Custom | Document Number: NBQAA LA6072P M/B | Rev: 1.0

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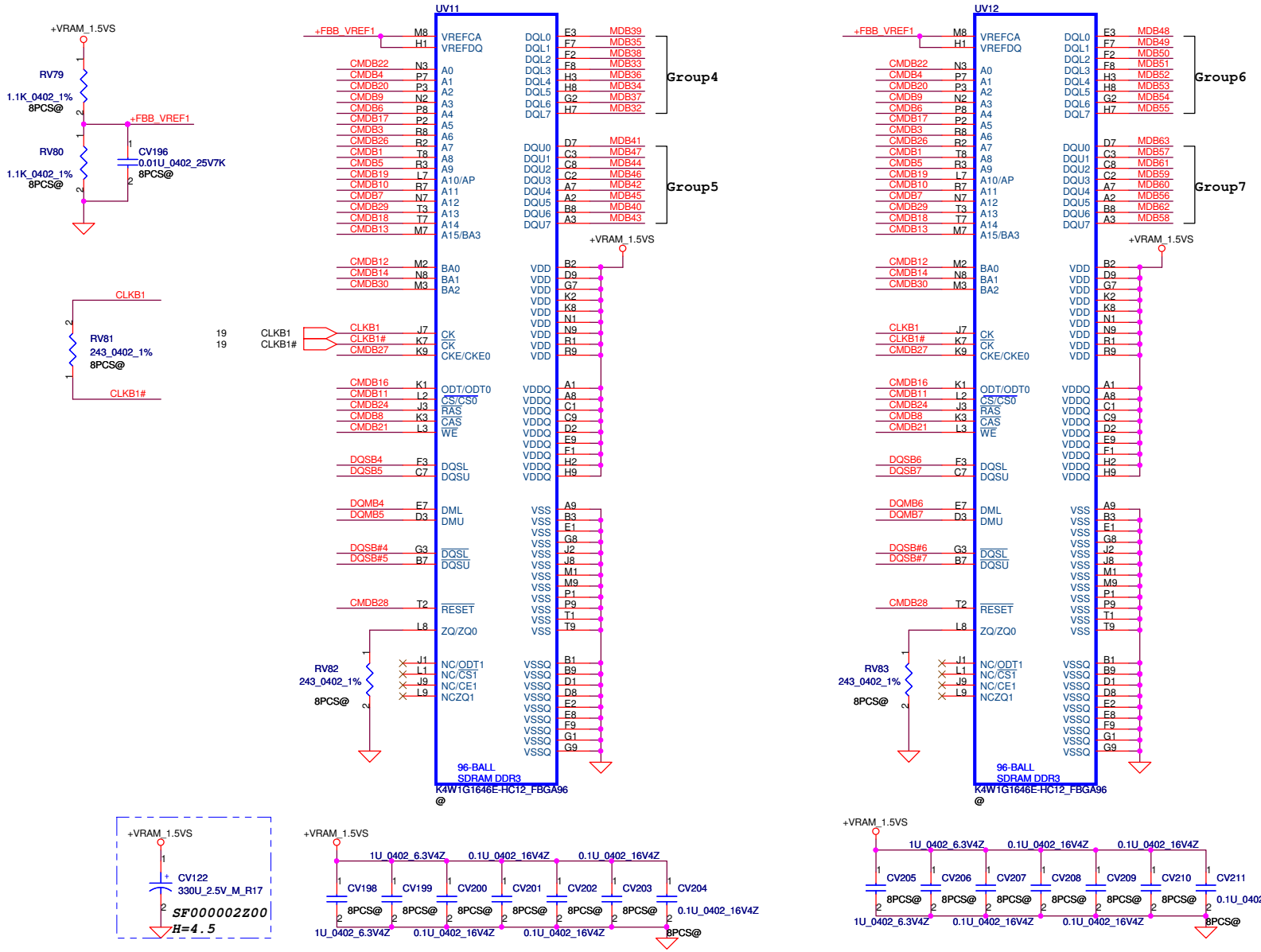
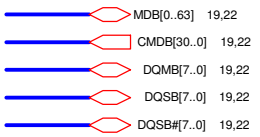
Memory Partition C - Upper 32 bits





Mode C - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/01

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Compal Electronics, Inc.

Title: **VRAM C Upper**

Size: Custom | Document Number: NBQAA LA6072P M/B | Rev: 1.0

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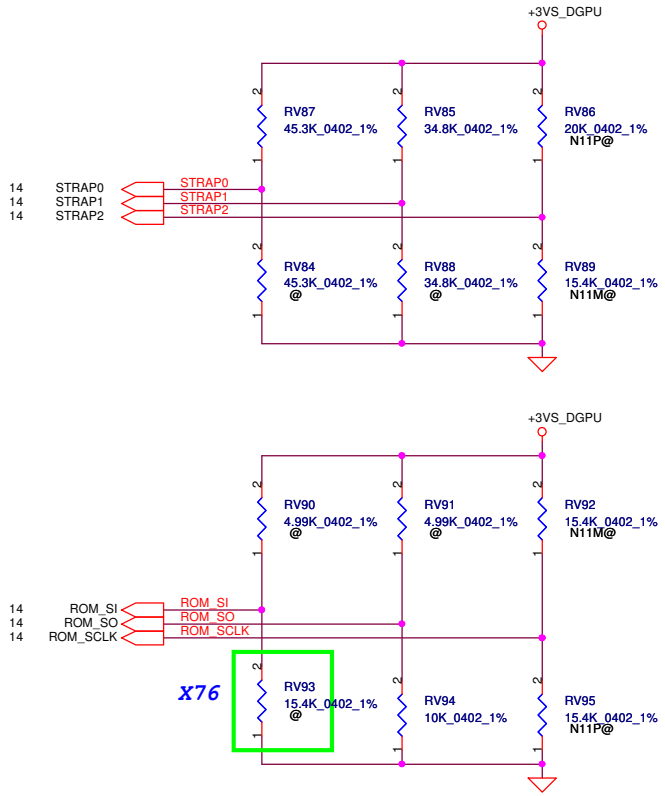

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	VDD33	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	VDD33	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM
ROM_SI	VDD33	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	VDD33	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	VDD33	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	VDD33	USER[3]	USER[2]	USER[1]	USER[0]

Device ID straps

	DeviceID	PCI_DEVID[4..0]	ROM_SCLK	STRAP2
N11P-LP1	0xA2B	[01011]	Pull down 15K	Pull up 20K
N11M-GE1	0xA75	[10101]	Pull up 15K	Pull down 30K
N11M-OP1	0xA72	[10010]	Pull up 15K	Pull down 15K

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	1110=EDID
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
1110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

	VRAM		RAMCFG[3..0]		RV93
DDR3 64M16	Hynix H5TQ1G63BFR-12C SA000032400	512MB	0010	PD 15K	SD034154280
		1GB	0010	PD 15K	SD034154280
	Samsung K4W1G1646E-HC12 SA000035700	512MB	0011	PD 20K	SD034200280
		1GB	0011	PD 20K	SD034200280
DDR3 128M16	Reserved for 128M16				

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Issued Date	2009/11/13	Deciphered Date	2010/01/01

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Compal Electronics, Inc.

Title: MSIC

Size: Custom | Document Number: NBQAA LA6072P M/B | Rev: 1.0

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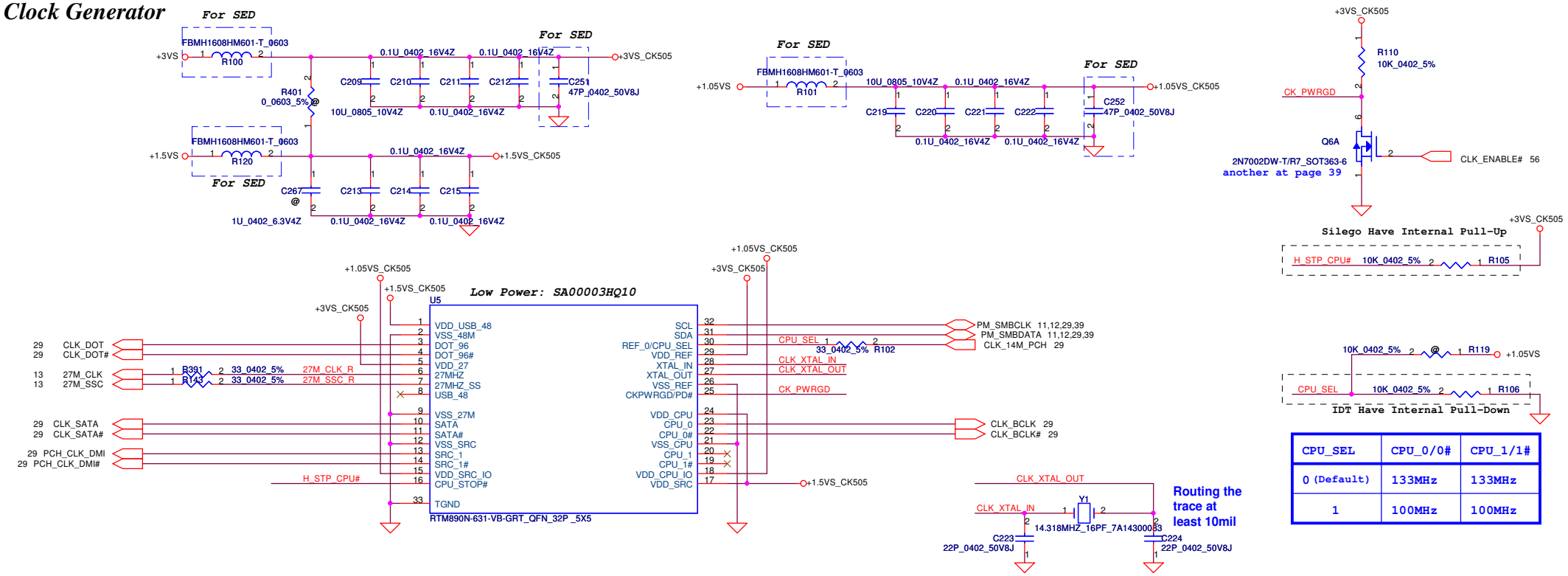
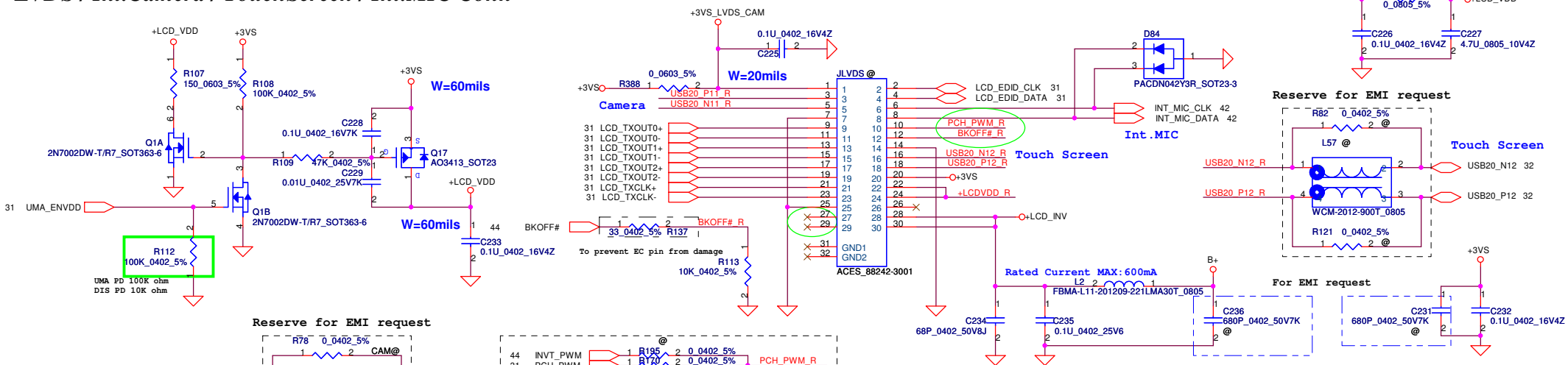
Clock Generator



CPU_SEL	CPU_0/0#	CPU_1/1#
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

LVDS / Int.Camera / TouchScreen / Int.MIC Conn



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Compal Electronics, Inc.

Title: **Clock Generator (CK505)/ LVDS CONN**

Size: Custom | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

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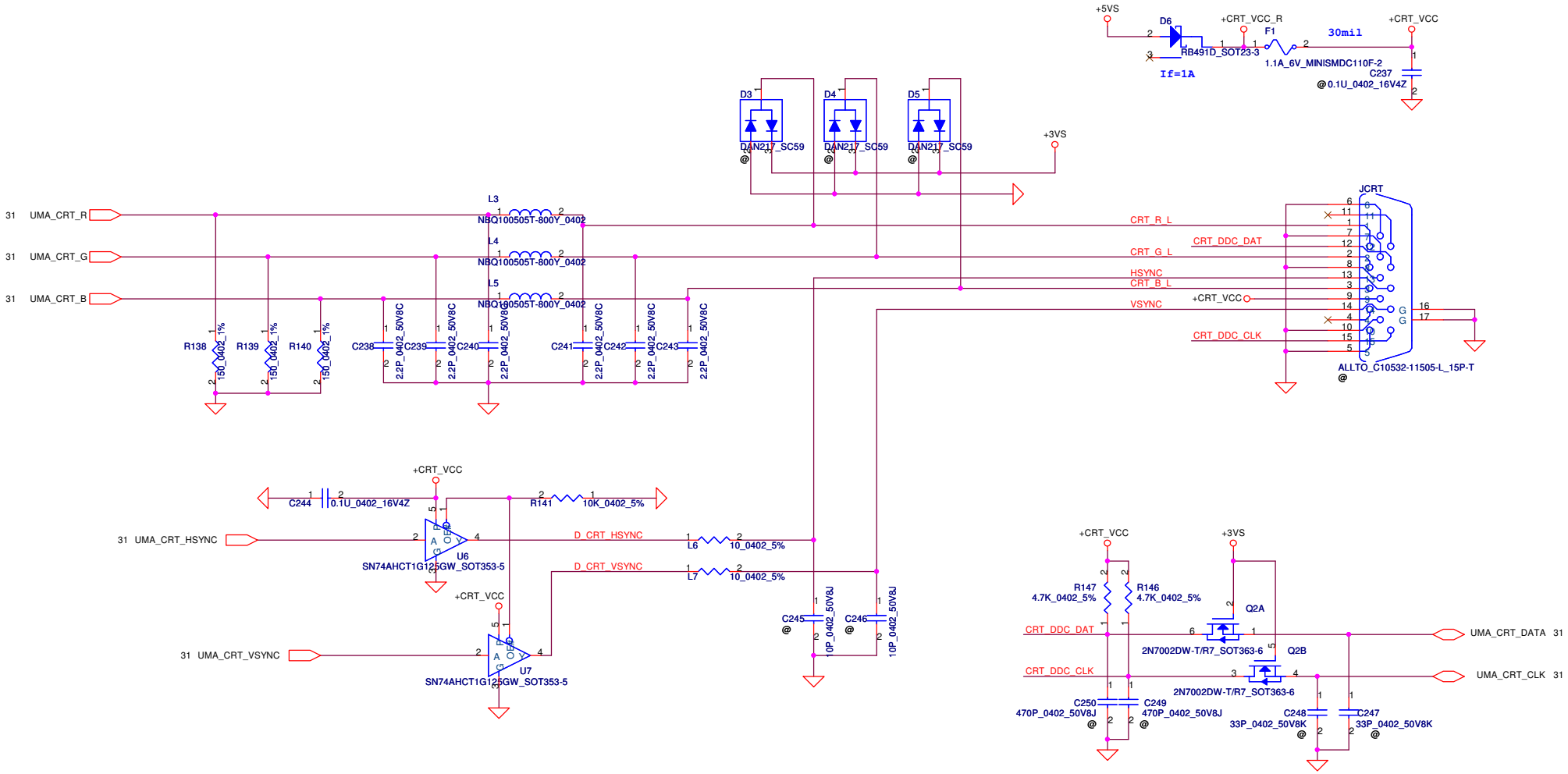
CRT CONNECTOR



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Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title	CRT\TV\LVDS	
Size	Document Number: NBQAA LA6072P M/B	Rev 1.0
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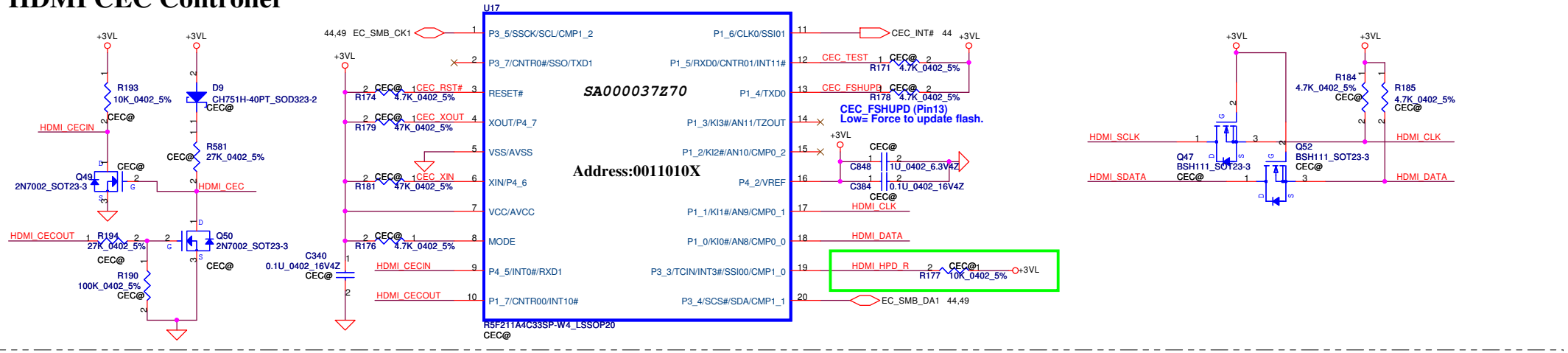
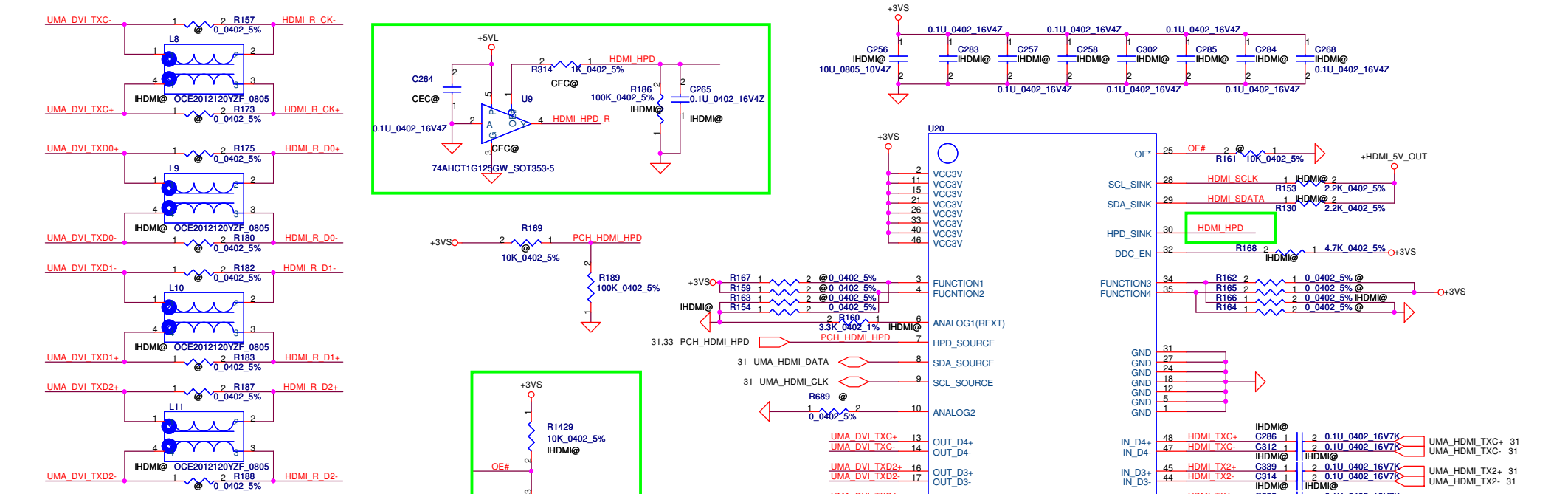
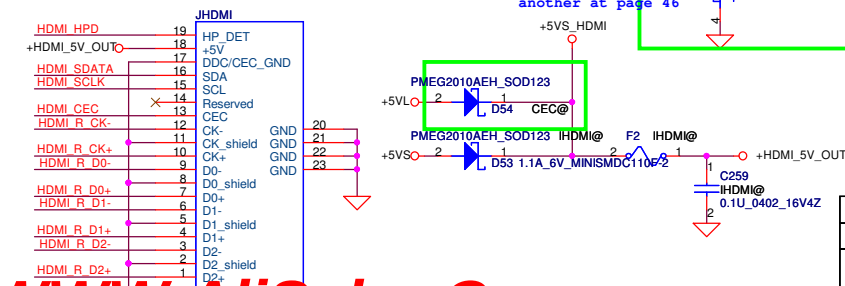
HDMI CEC Controller





HDMI Connector



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Compal Electronics, Inc.

Title: HDMI Connector

Size | Document Number: NBQAA LA6072P M/B | Rev 1.0

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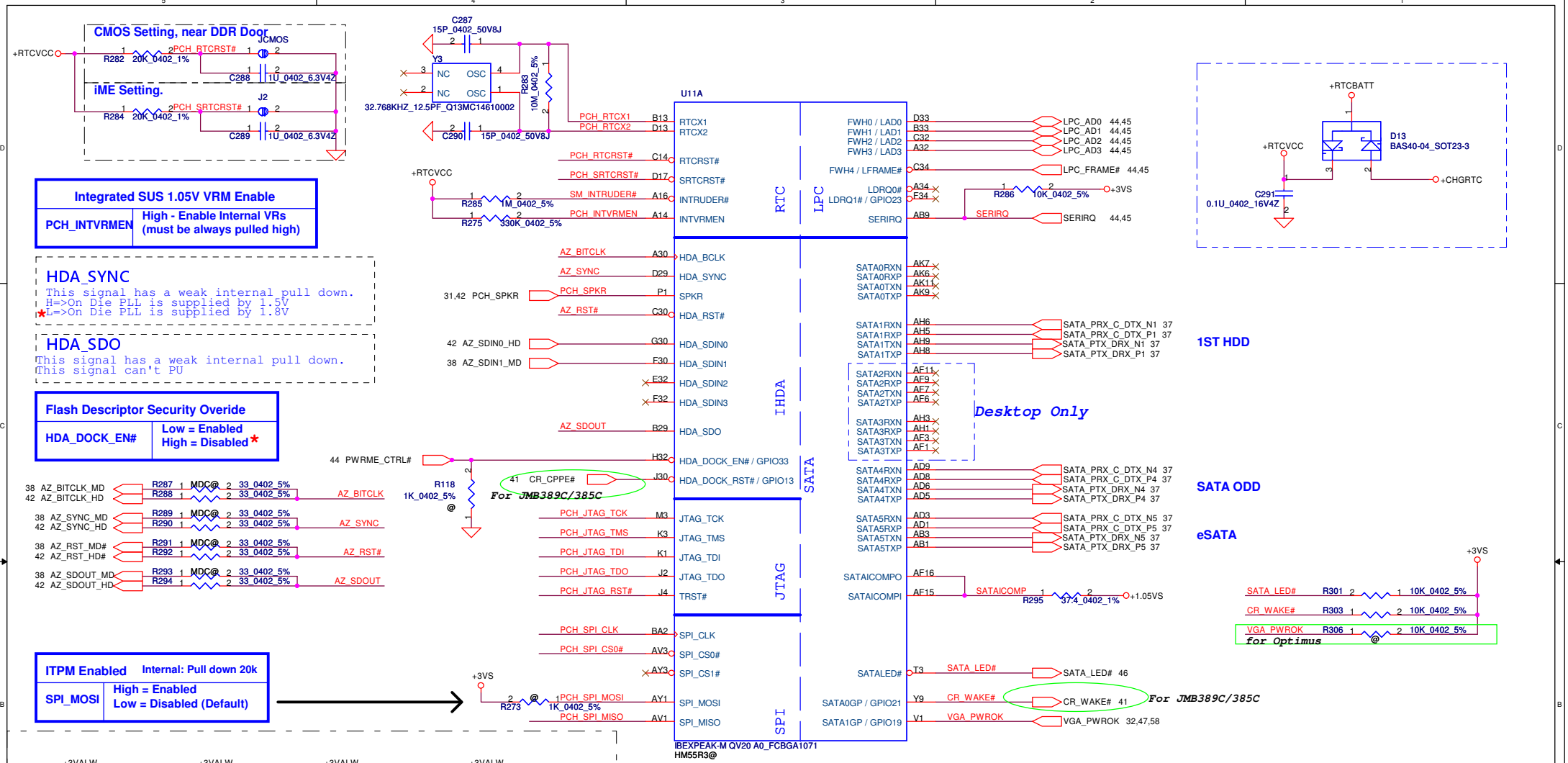

PCH Pin	RefDes	PCH JTAG Enable ES1	PCH JTAG Enable ES2	PCH JTAG Disable (Default) ES1	PCH JTAG Disable (Default) ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
	R535	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20Kohm	No Install
	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R364	20Kohm	20Kohm	No Install	No Install
	R643	10Kohm	10Kohm	No Install	No Install

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Compal Electronics, Inc.

Title: **PCH-SPI/SATA/LPC/RTC/HDA**

Size: B | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

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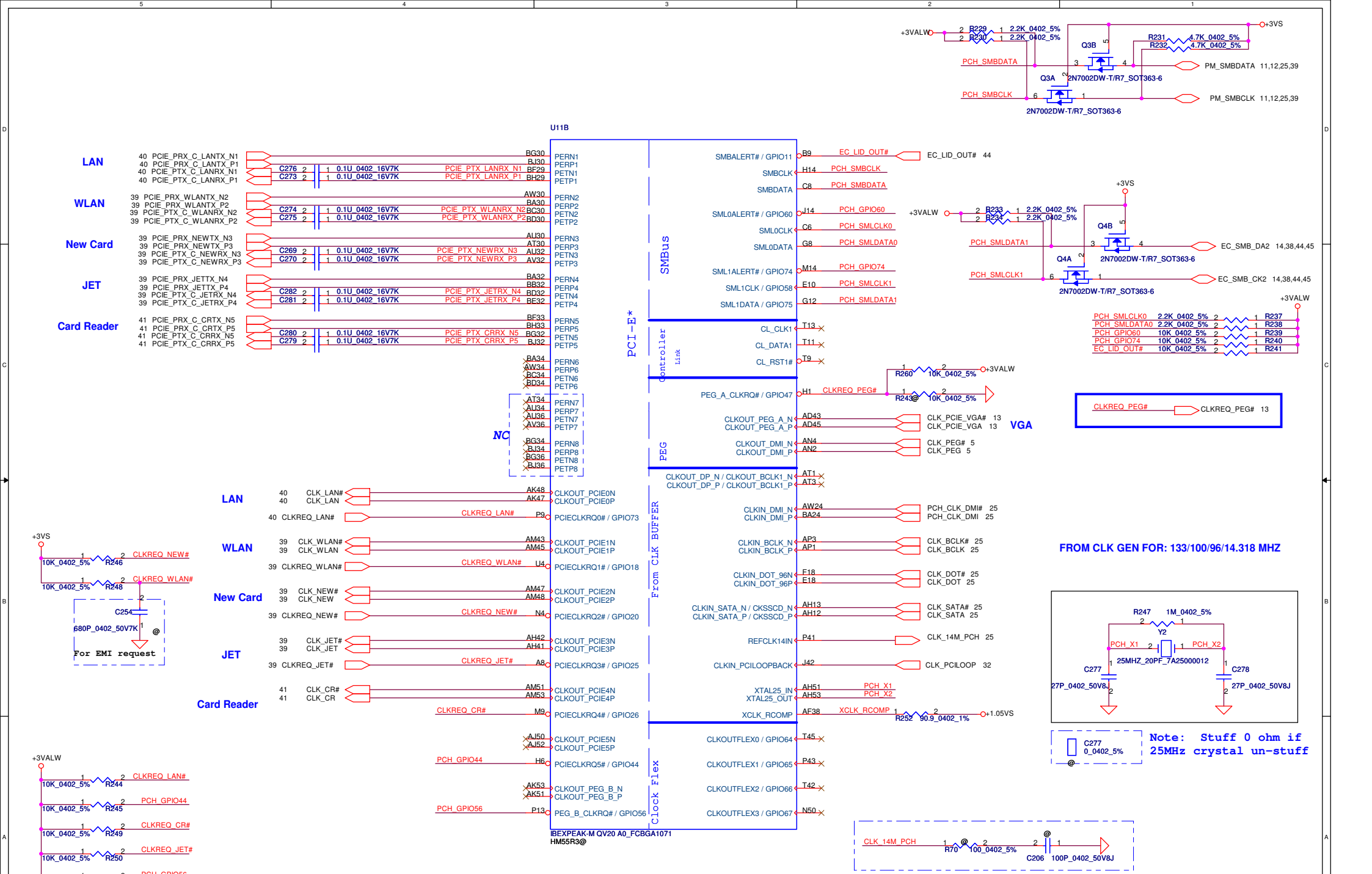

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Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **CLK/PCIE/SMBUS**

Size: B | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

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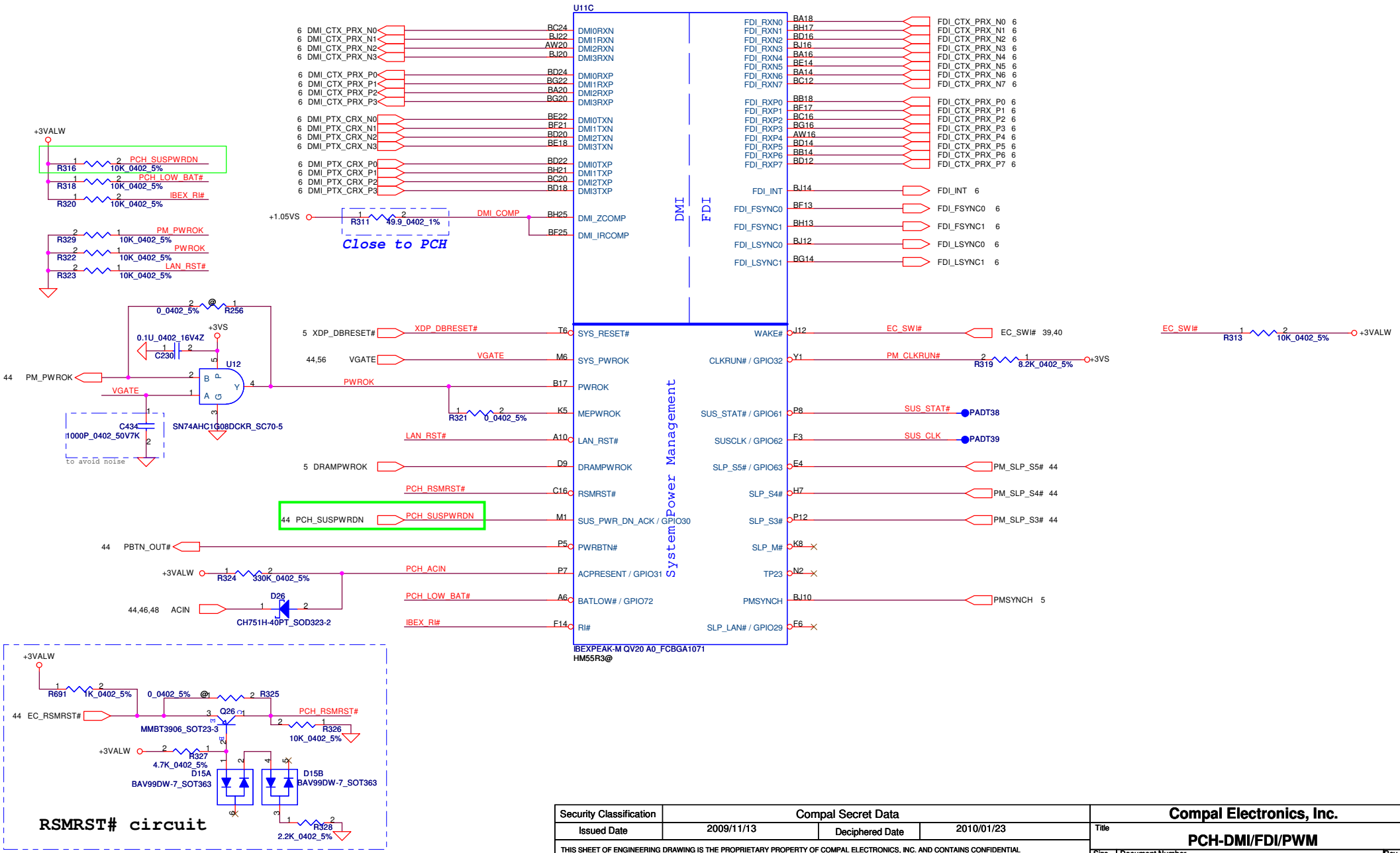

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Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **PCH-DMI/FDI/PWM**

Size: B | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

Date: Tuesday, March 23, 2010 | Sheet 30 of 61

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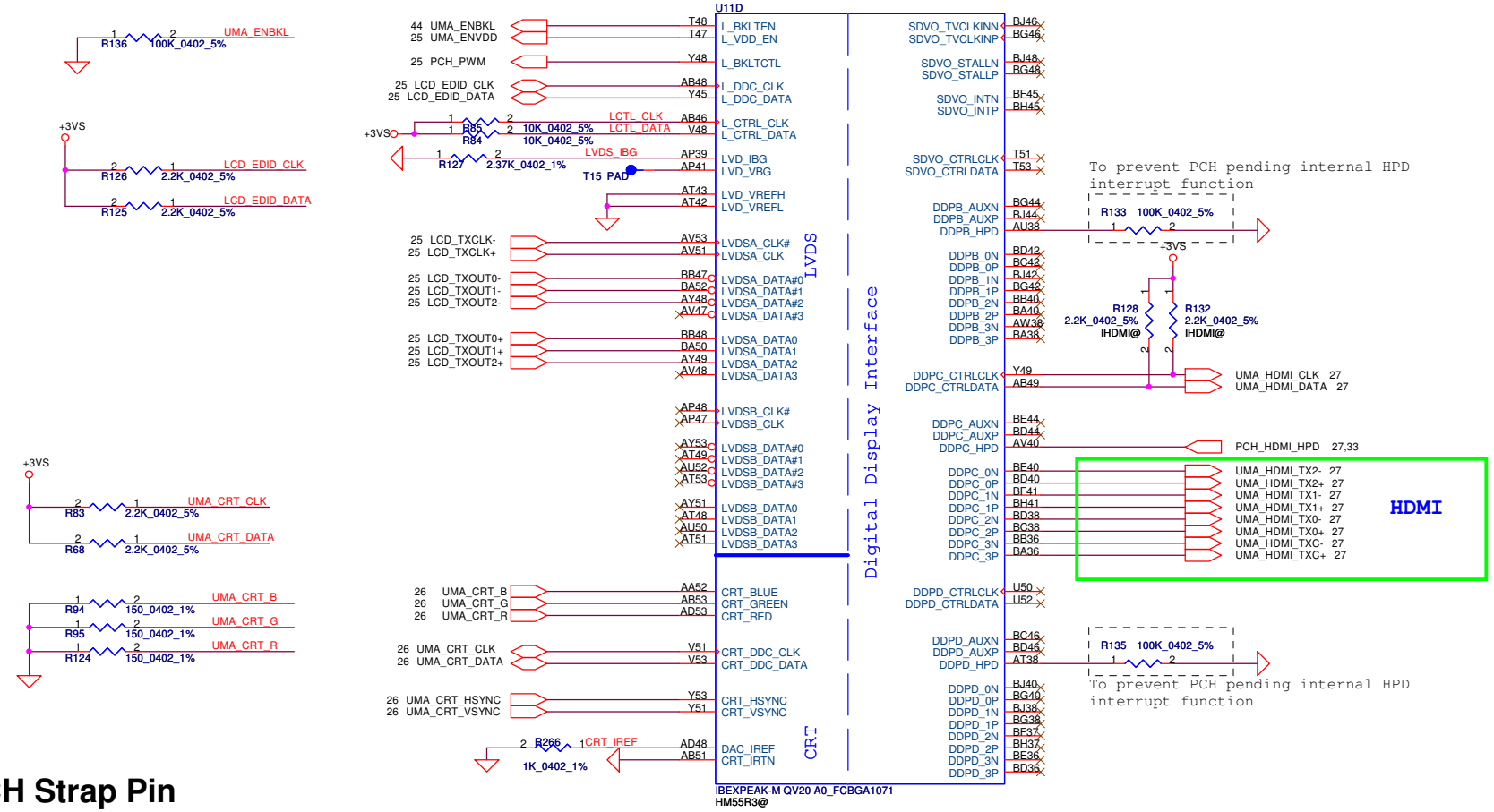
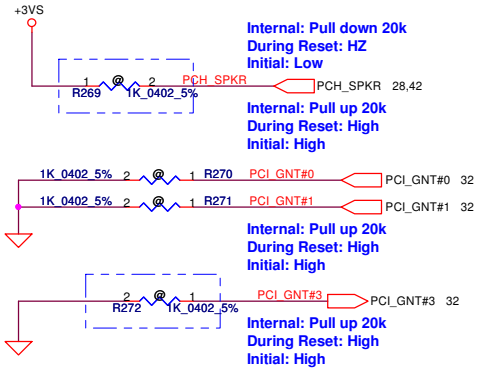


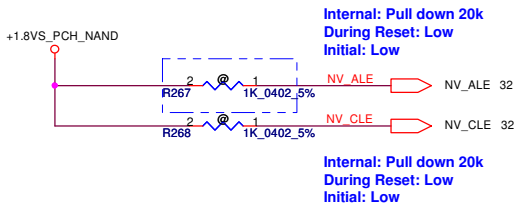
PCH Strap Pin



NO REBOOT Strap	
PCH_SPKR	Low= Disable High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable



Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **PCH-VGA/LVDS/TV**

Size: Custom | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 31 of 61

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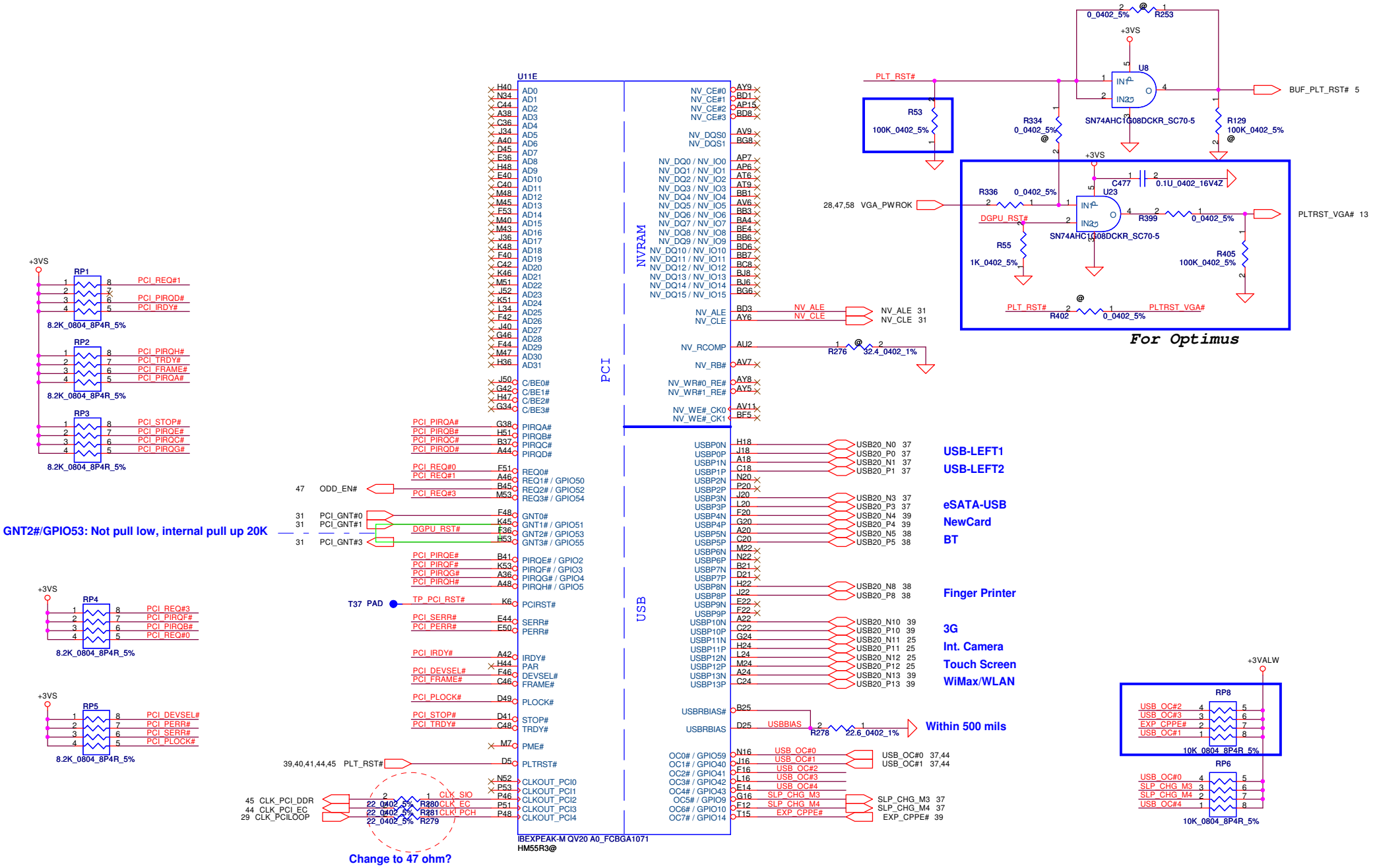

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **PCH USB/PCI/NAND**

Size: B | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 32 of 61

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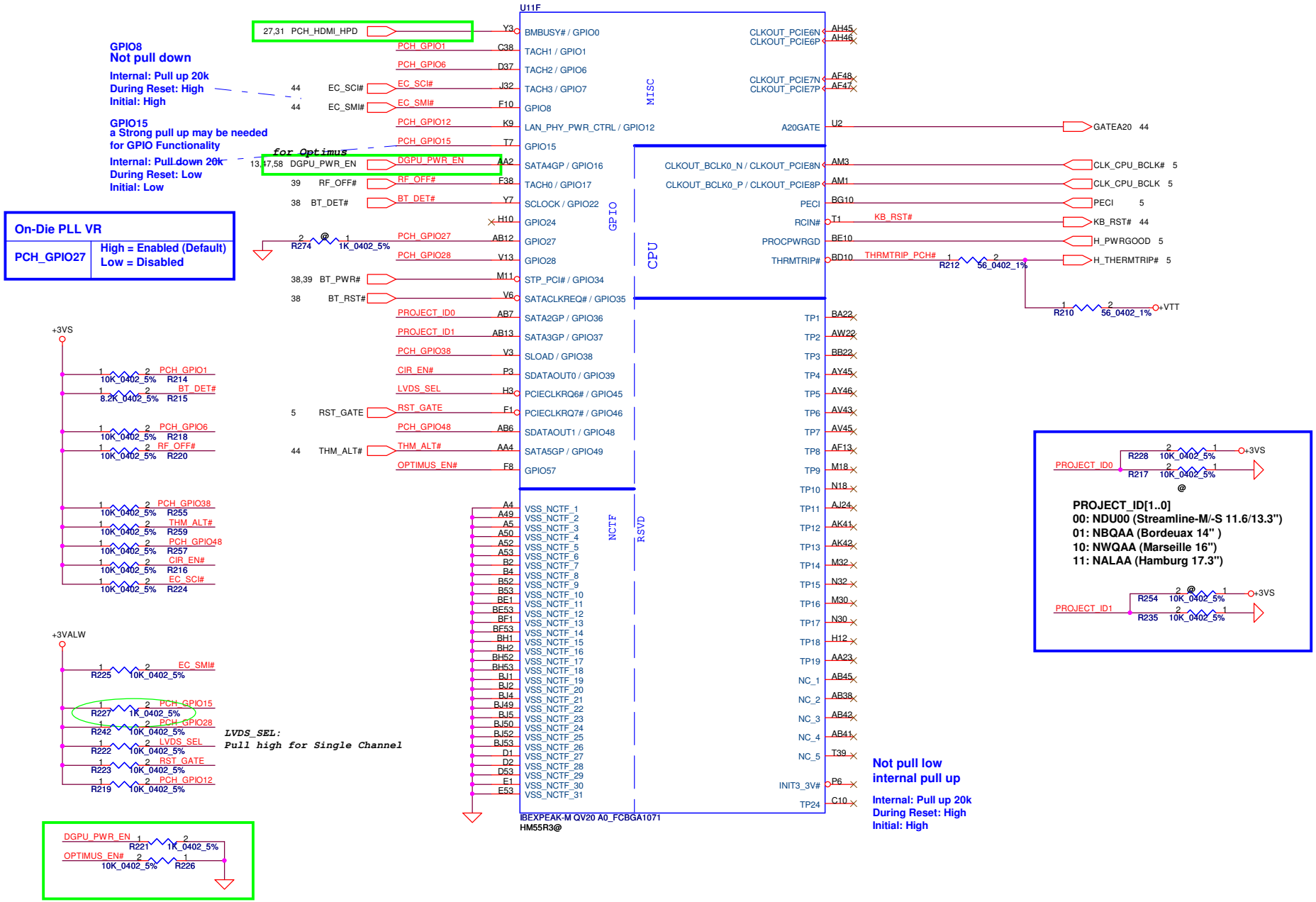

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **PCH CPU/GPIO**

Size: B | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 33 of 61

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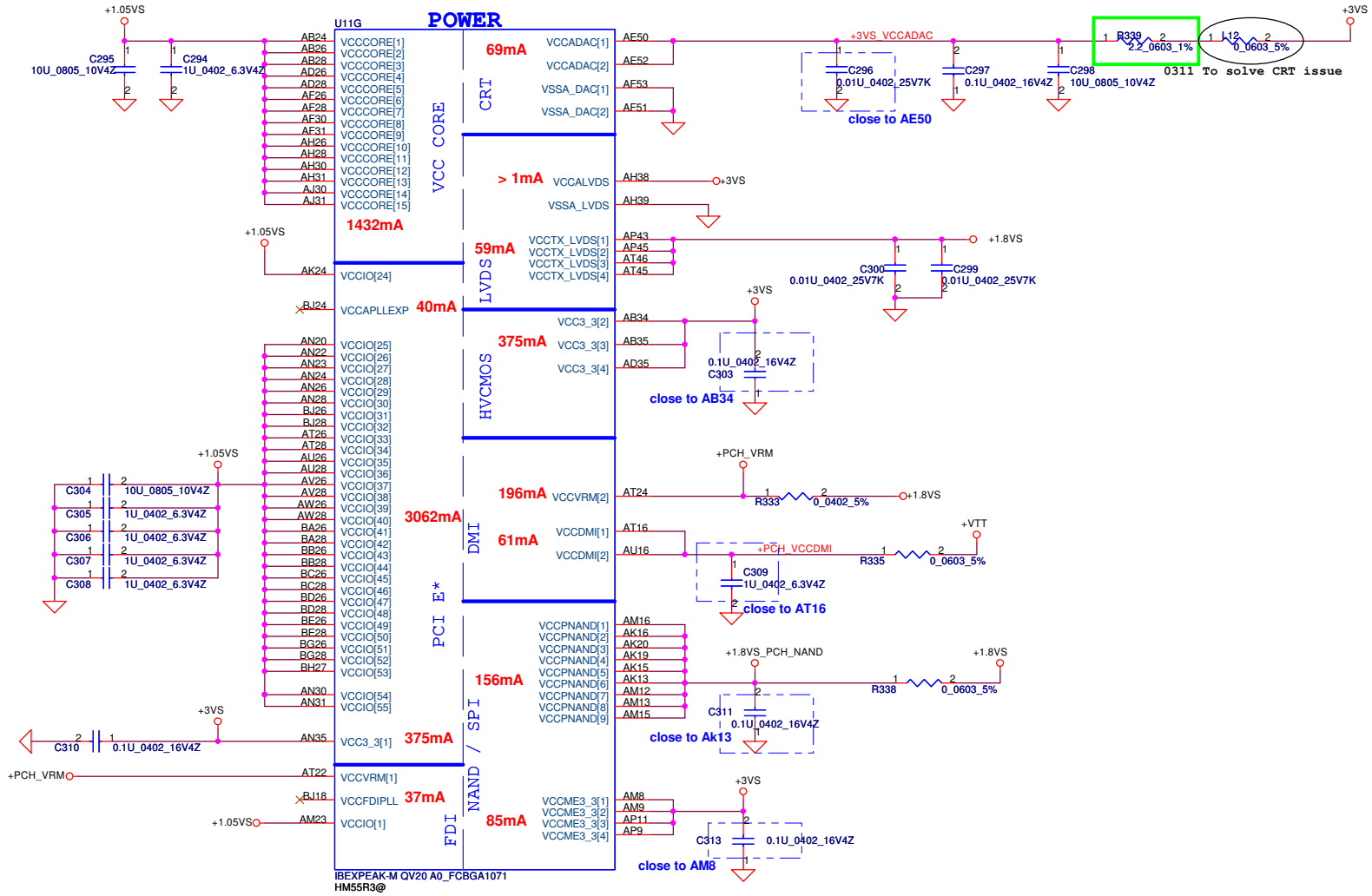

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **PCH POWER-1**

Size: B | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 34 of 61

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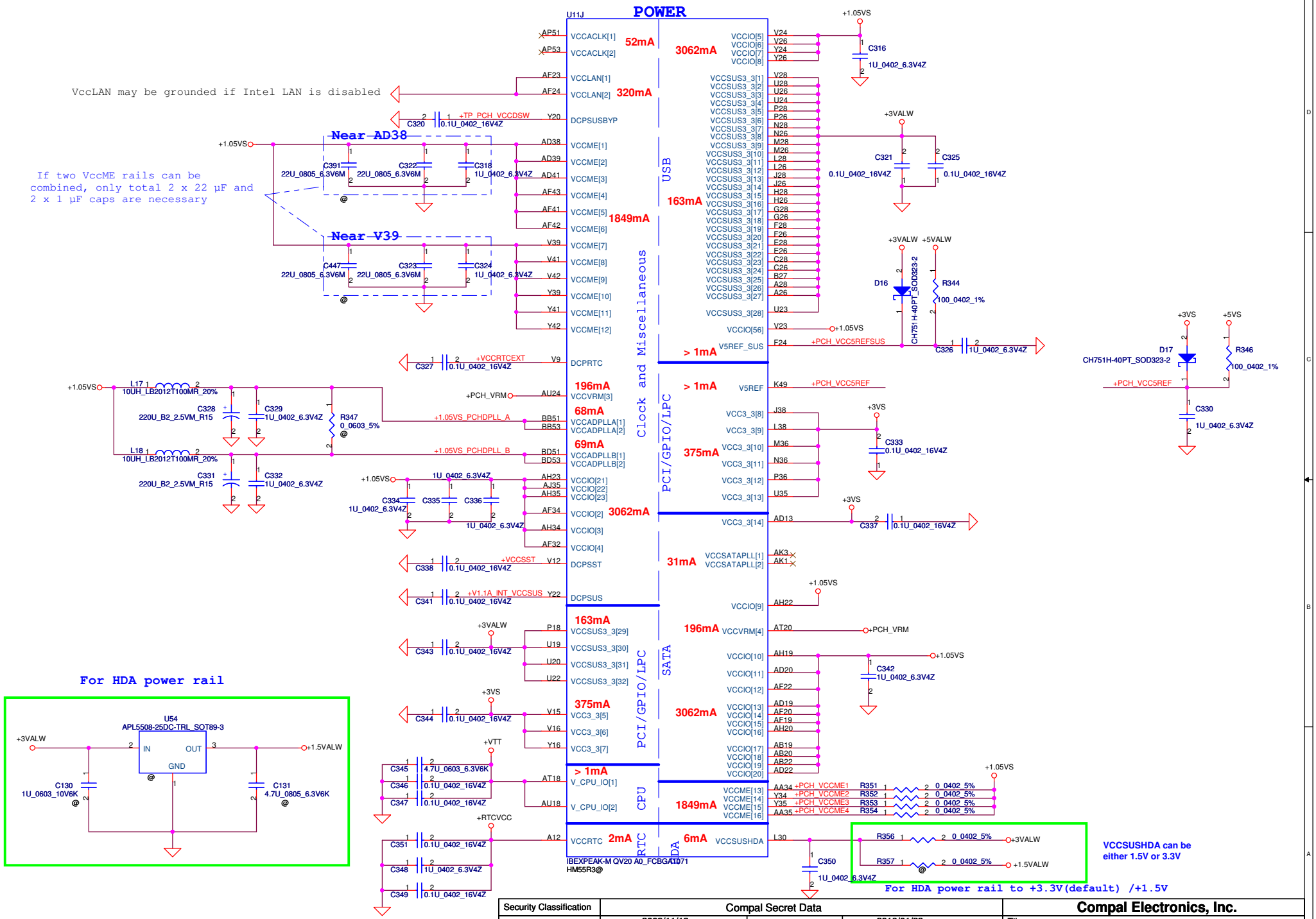

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **PCH POWER-2**

Size: Custom | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 35 of 61

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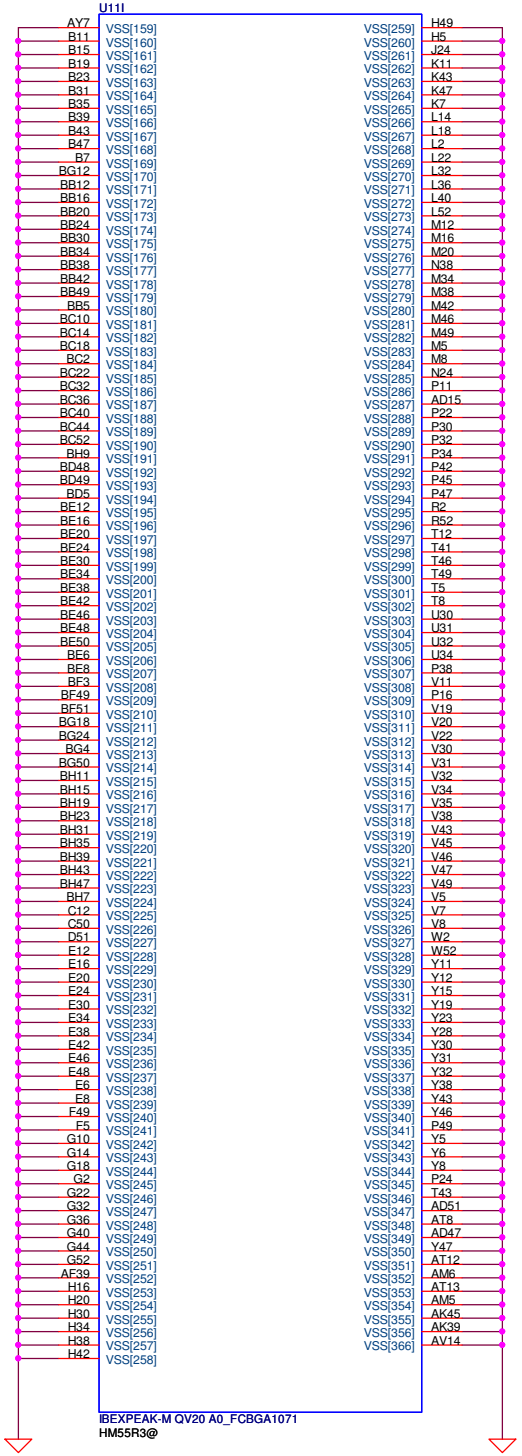

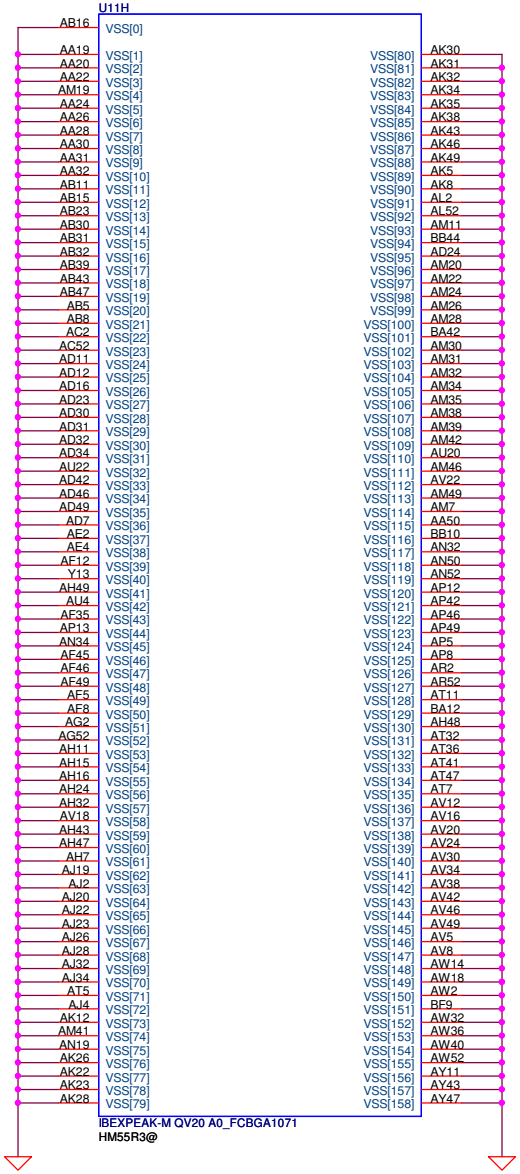

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Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: **PCH-GND**

Size: Custom | Document Number: **NBQAA LA6072P M/B** | Rev: 1.0

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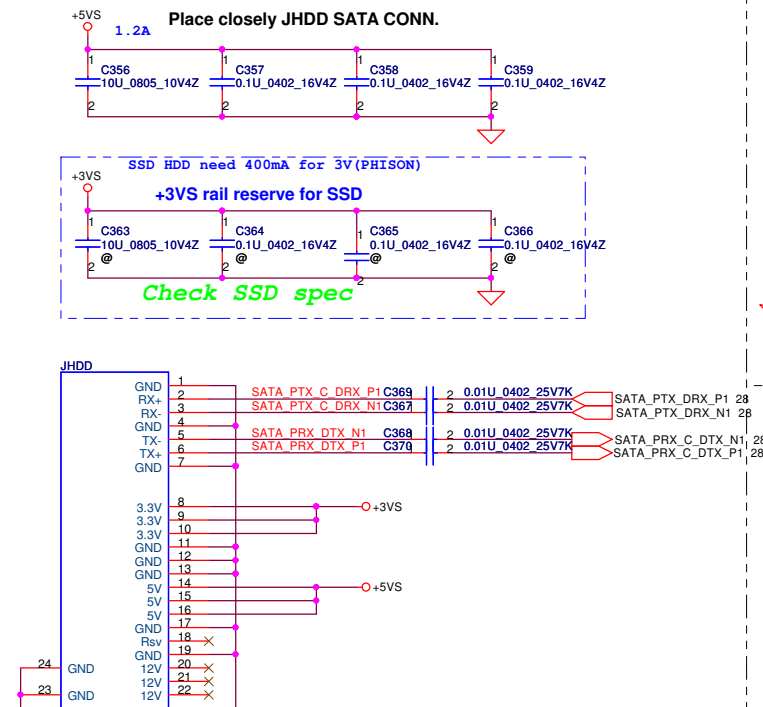
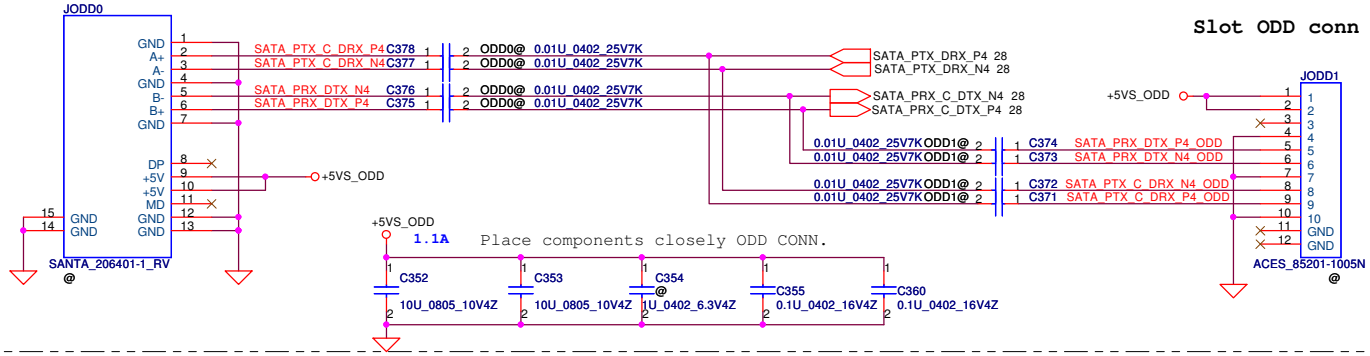
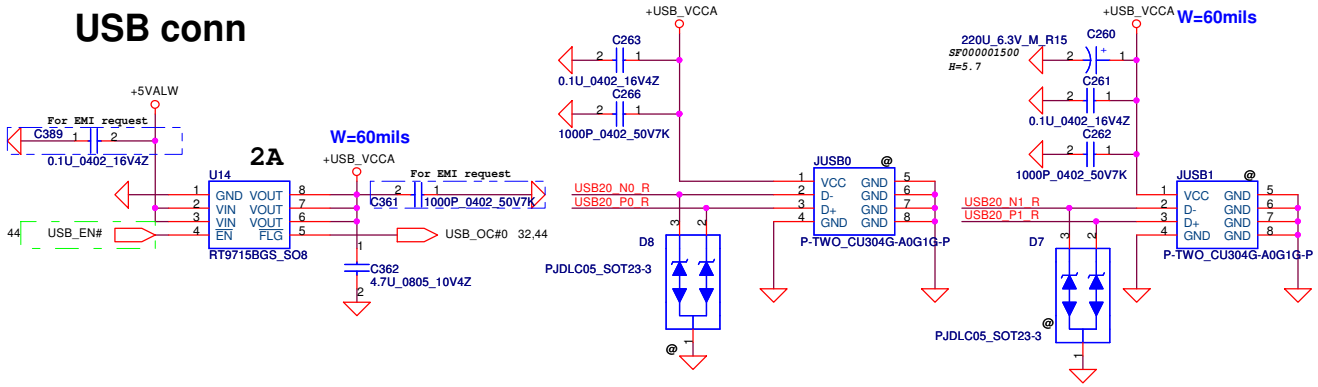
SATA HDD Conn.



SATA ODD Conn



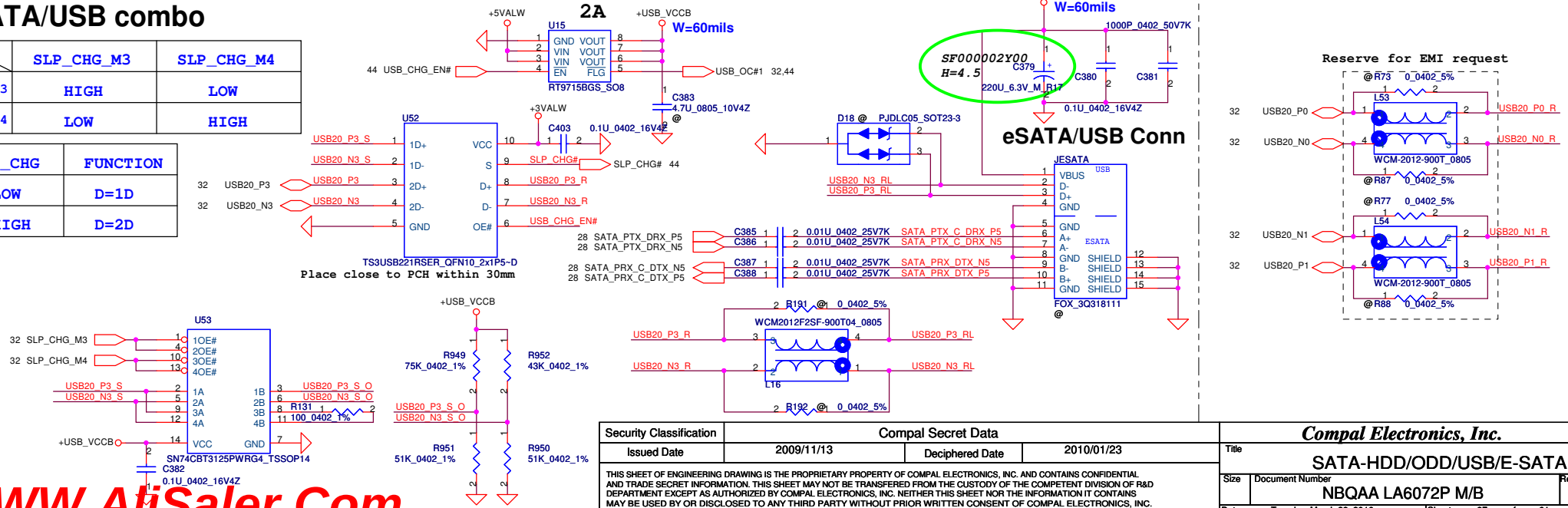
USB conn



eSATA/USB combo

	SLP_CHG_M3	SLP_CHG_M4
Mode 3	HIGH	LOW
Mode 4	LOW	HIGH

SLP_CHG	FUNCTION
LOW	D=1D
HIGH	D=2D



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Compal Electronics, Inc.

Title: SATA-HDD/ODD/USB/E-SATA

Size: | Document Number: NBQAA LA6072P M/B | Rev: 1.0

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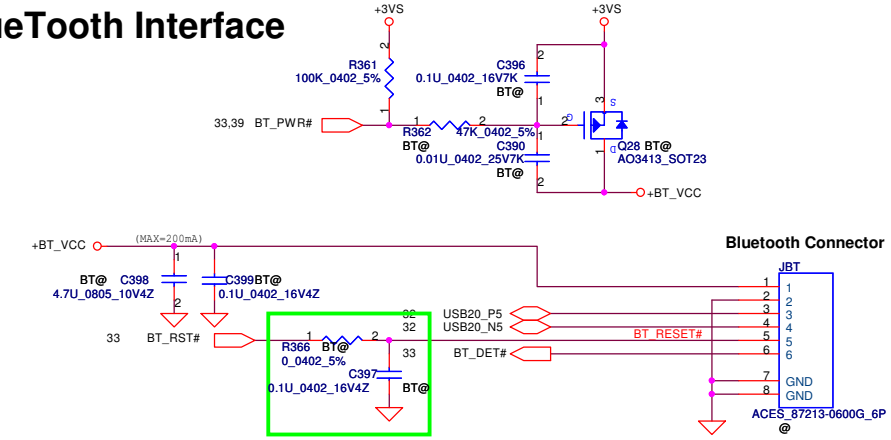
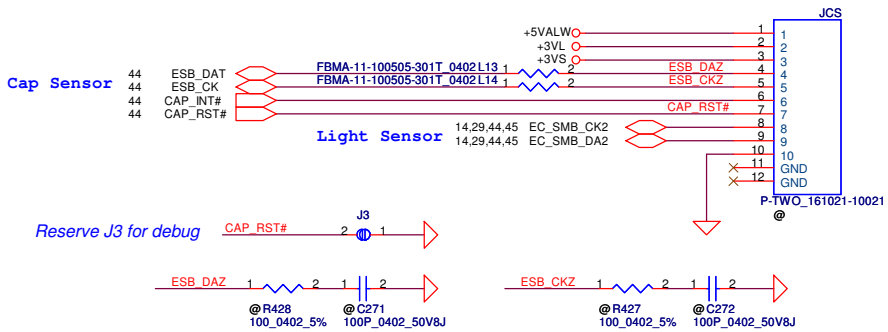
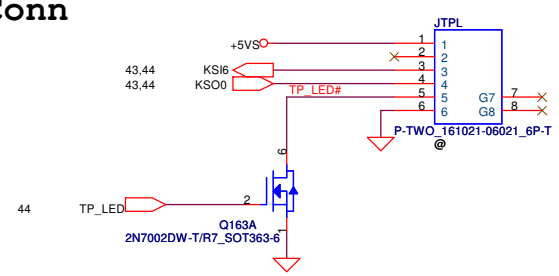
BlueTooth Interface



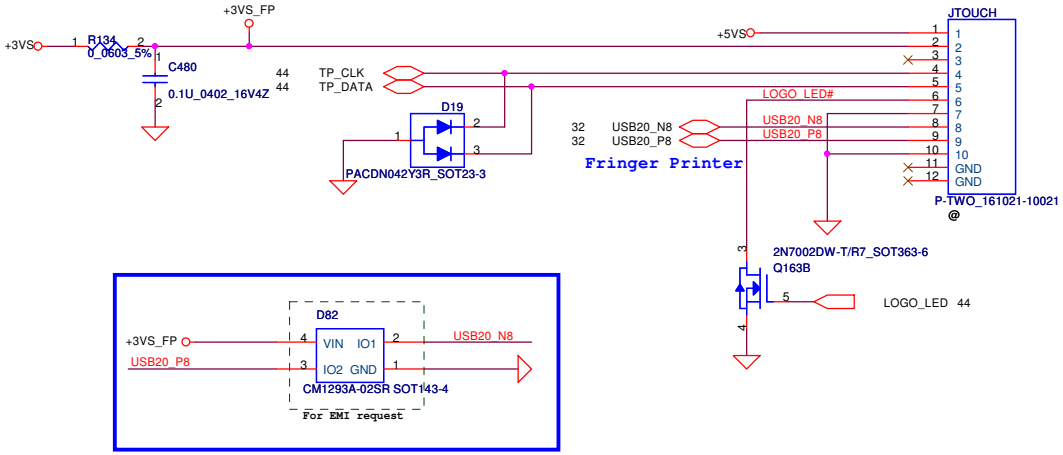
Cap Sensor / Light Sensor Conn



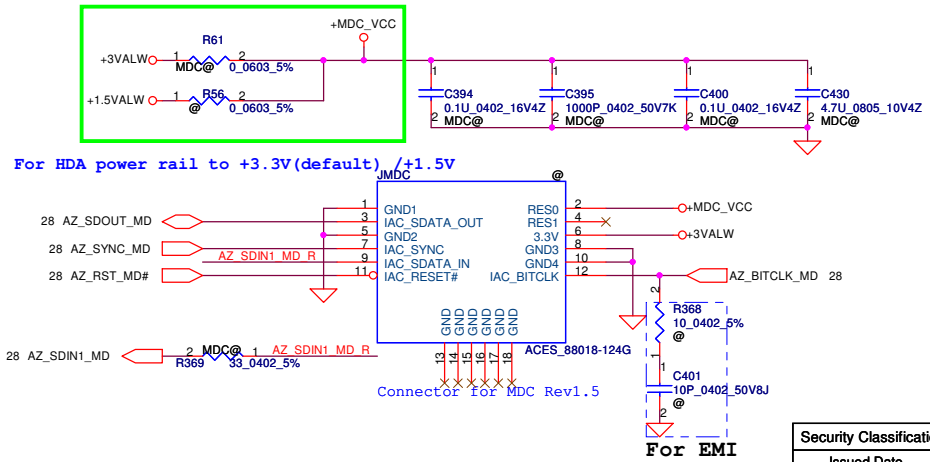
TP LED Conn



TP/B LED/B FP/B Conn



MDC 1.5 Conn



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Compal Electronics, Inc.

Title: USB/BT/FP/MDC/TP/CAP

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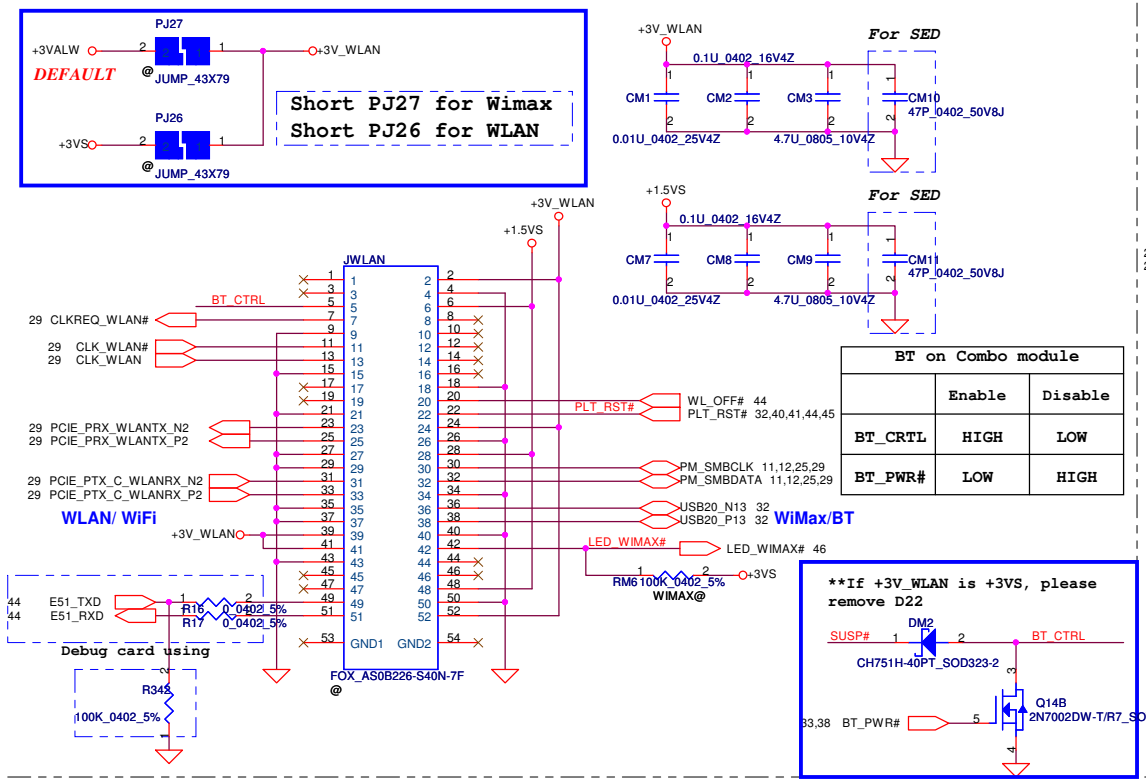
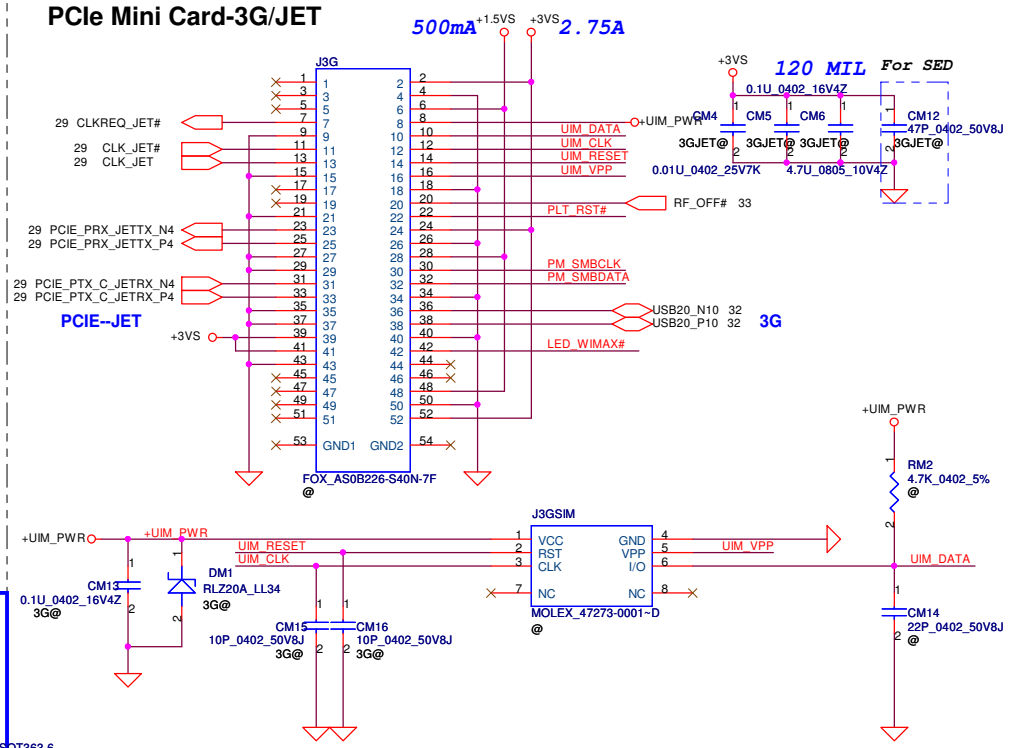
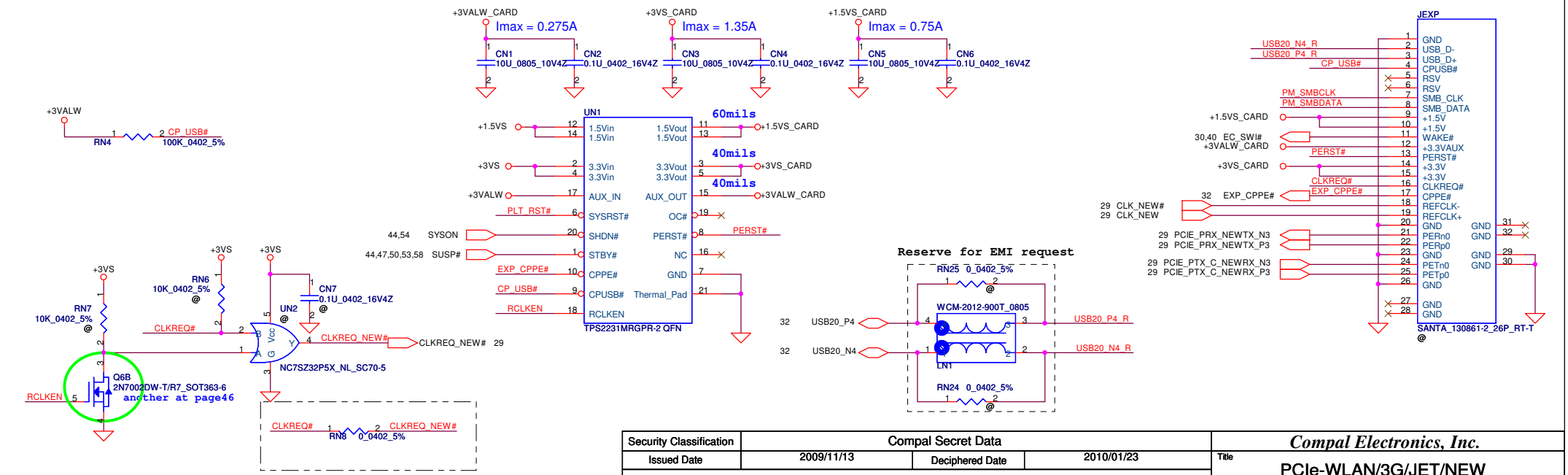
PCIe Mini Card-WLAN/WiMax



PCIe Mini Card-3G/JET





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Compal Electronics, Inc.

Title: PCIe-WLAN/3G/JET/NEW

Size | Document Number: NBQAA LA6072P M/B | Rev 1.0

Date: Tuesday, March 23, 2010 | Sheet 39 of 61

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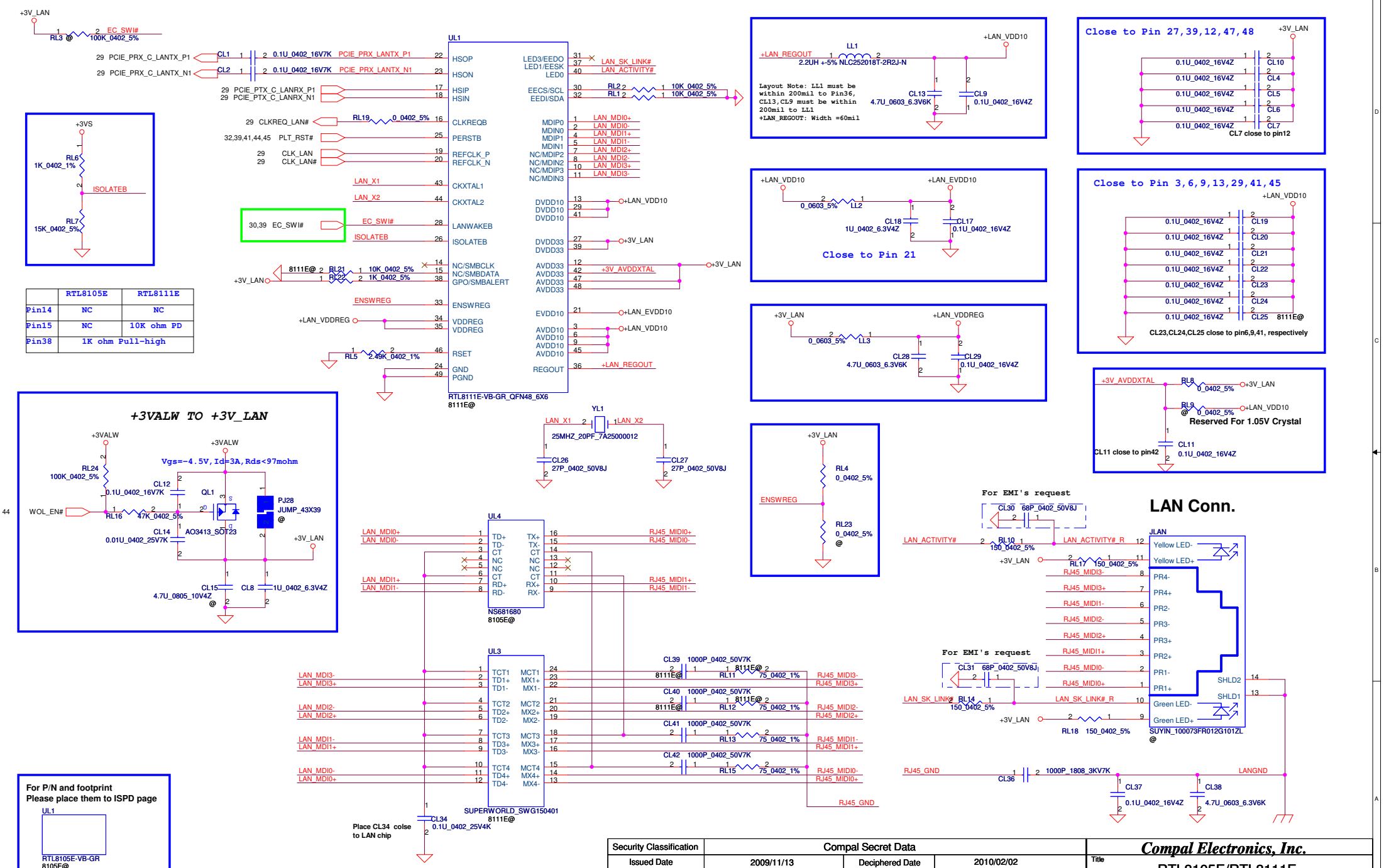

	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	

For P/N and footprint
Please place them to ISPD page
UL1
RTL8105E-VB-GR
8105E@

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/02/02

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Compal Electronics, Inc.

Title: RTL8105E/RTL8111E

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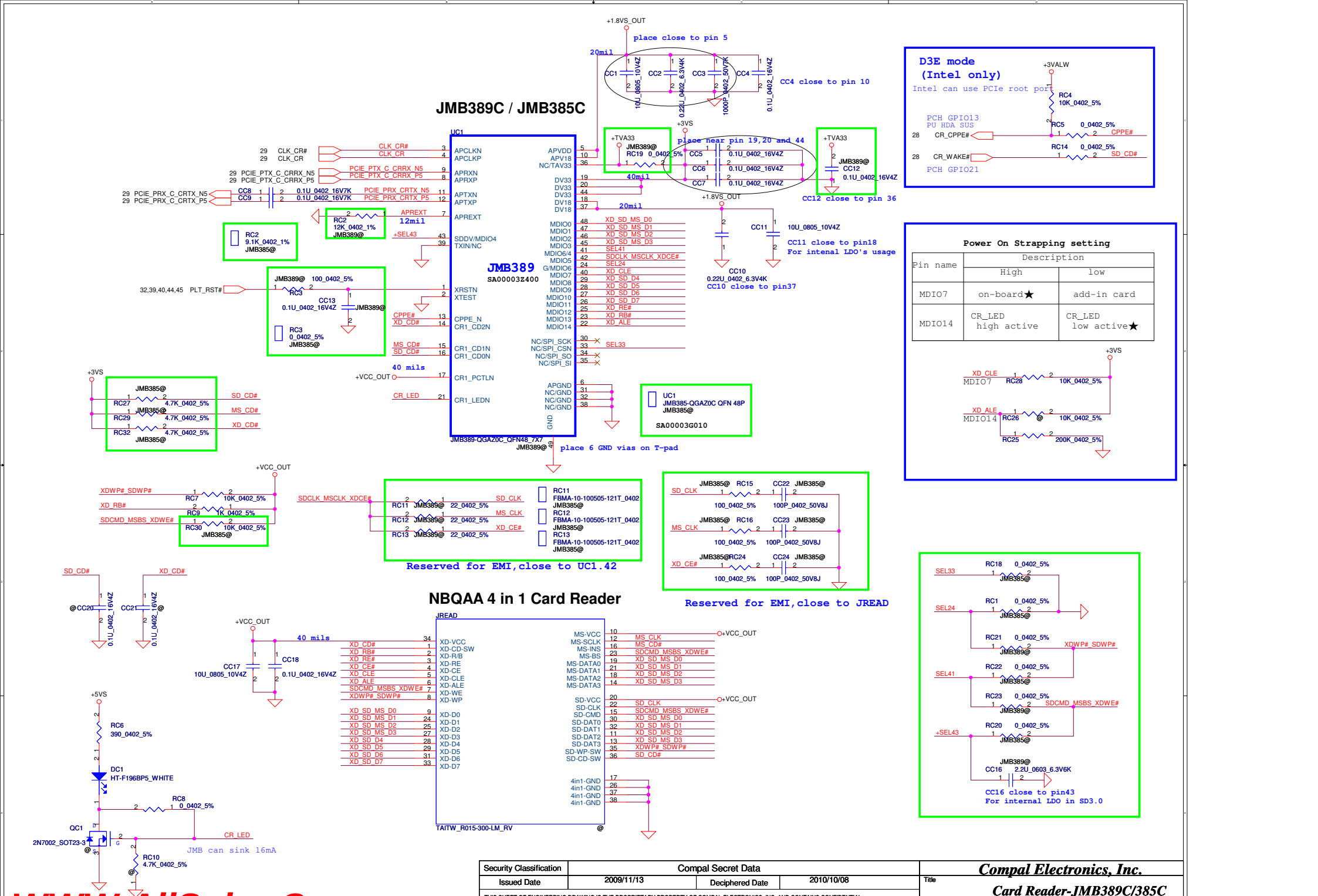

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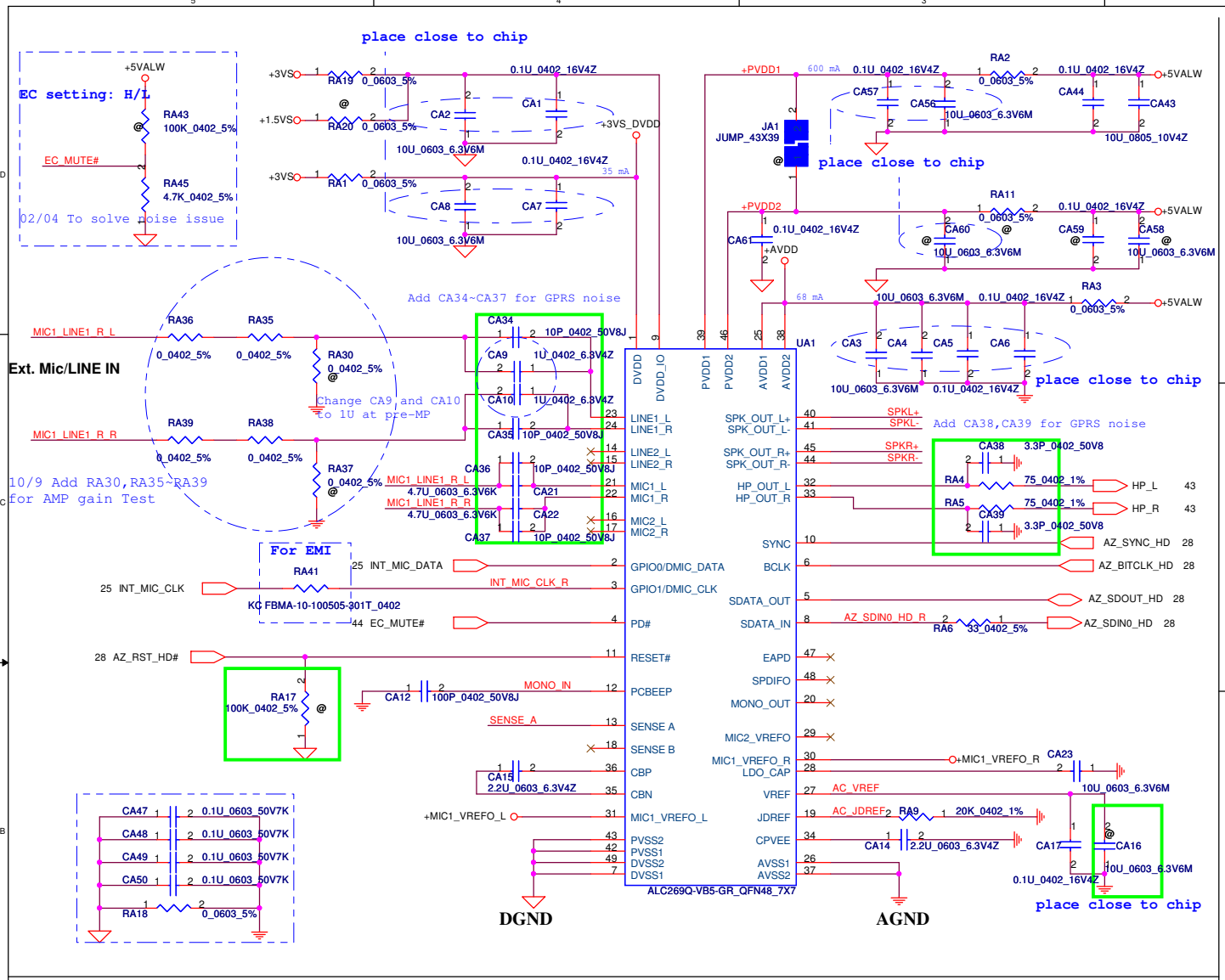
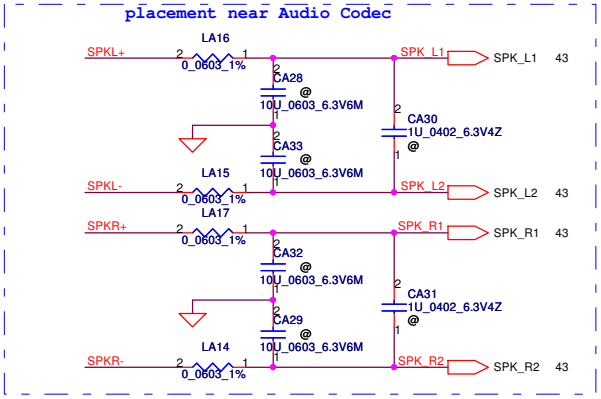
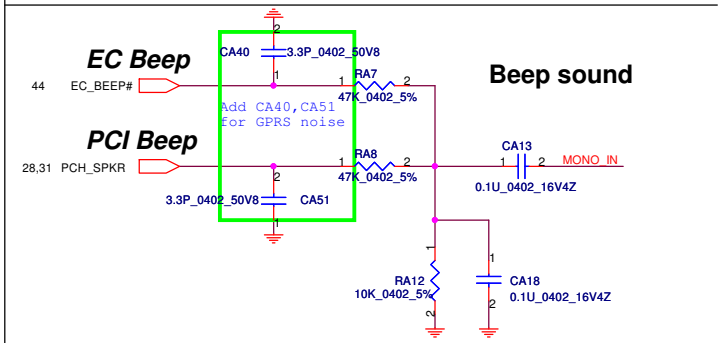
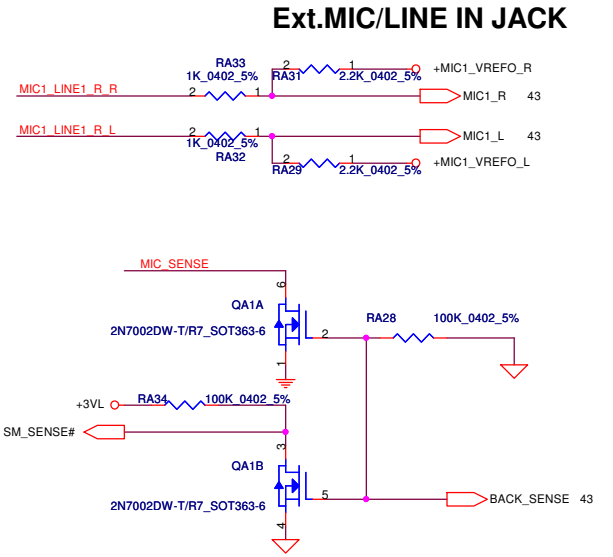
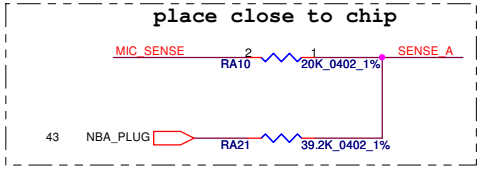








Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	



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Compal Electronics, Inc.

Title: HDA CODEC ALC269

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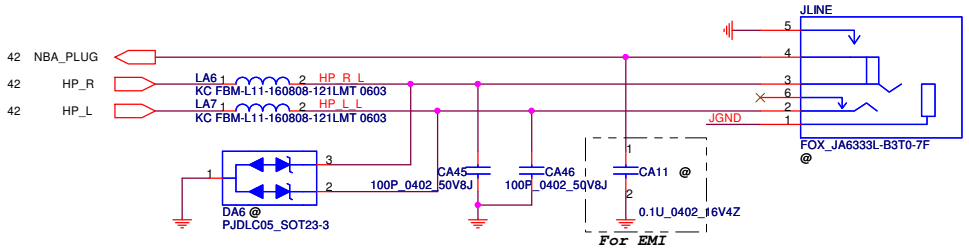
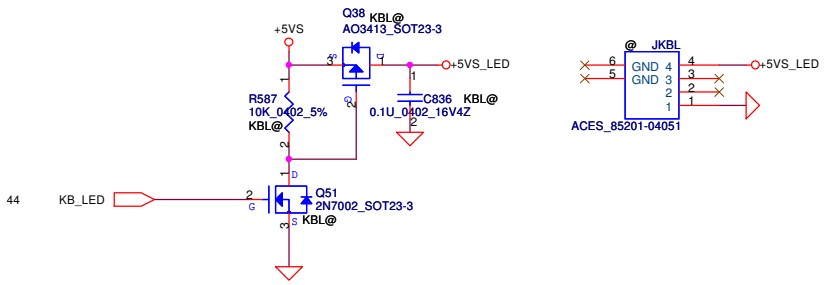
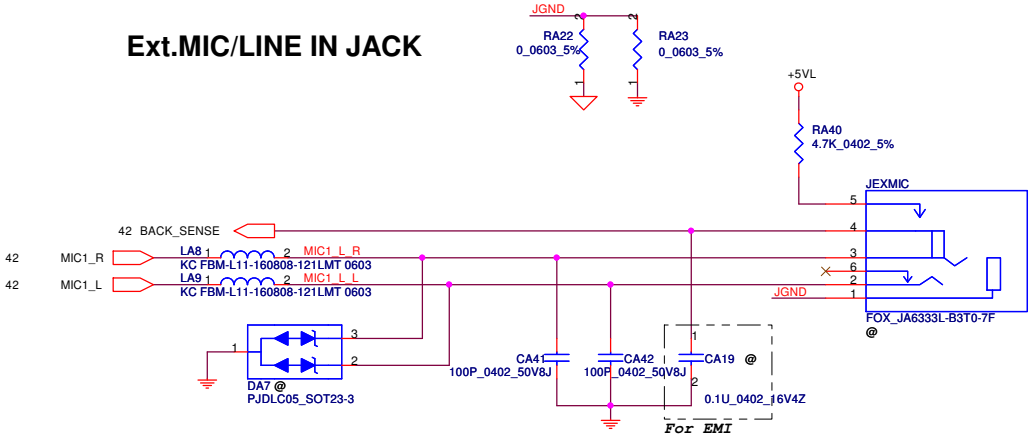
HeadPhone/LINE Out JACK



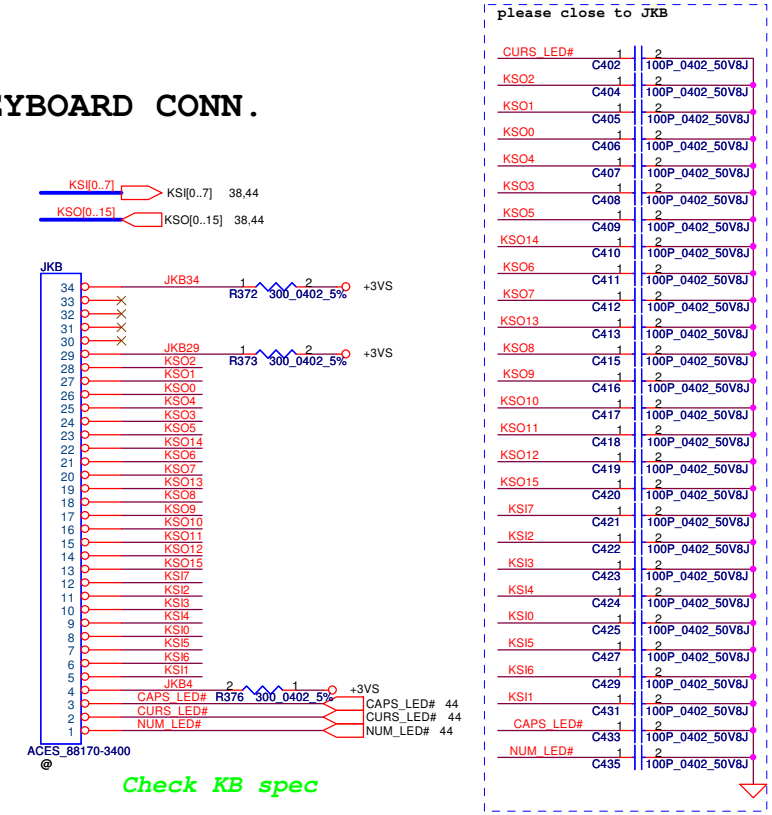
Keyboard LED



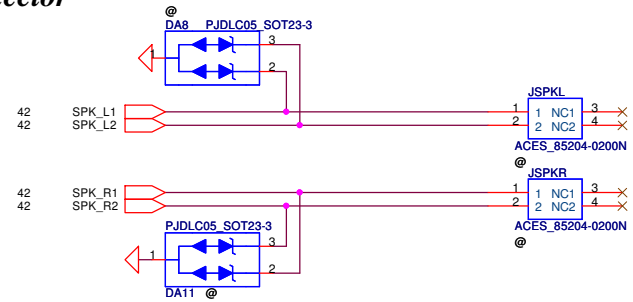
Ext.MIC/LINE IN JACK



KEYBOARD CONN.



Speaker Connector



Need to update symbol

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Compal Electronics, Inc.

Title: AUDIO/KB CONN

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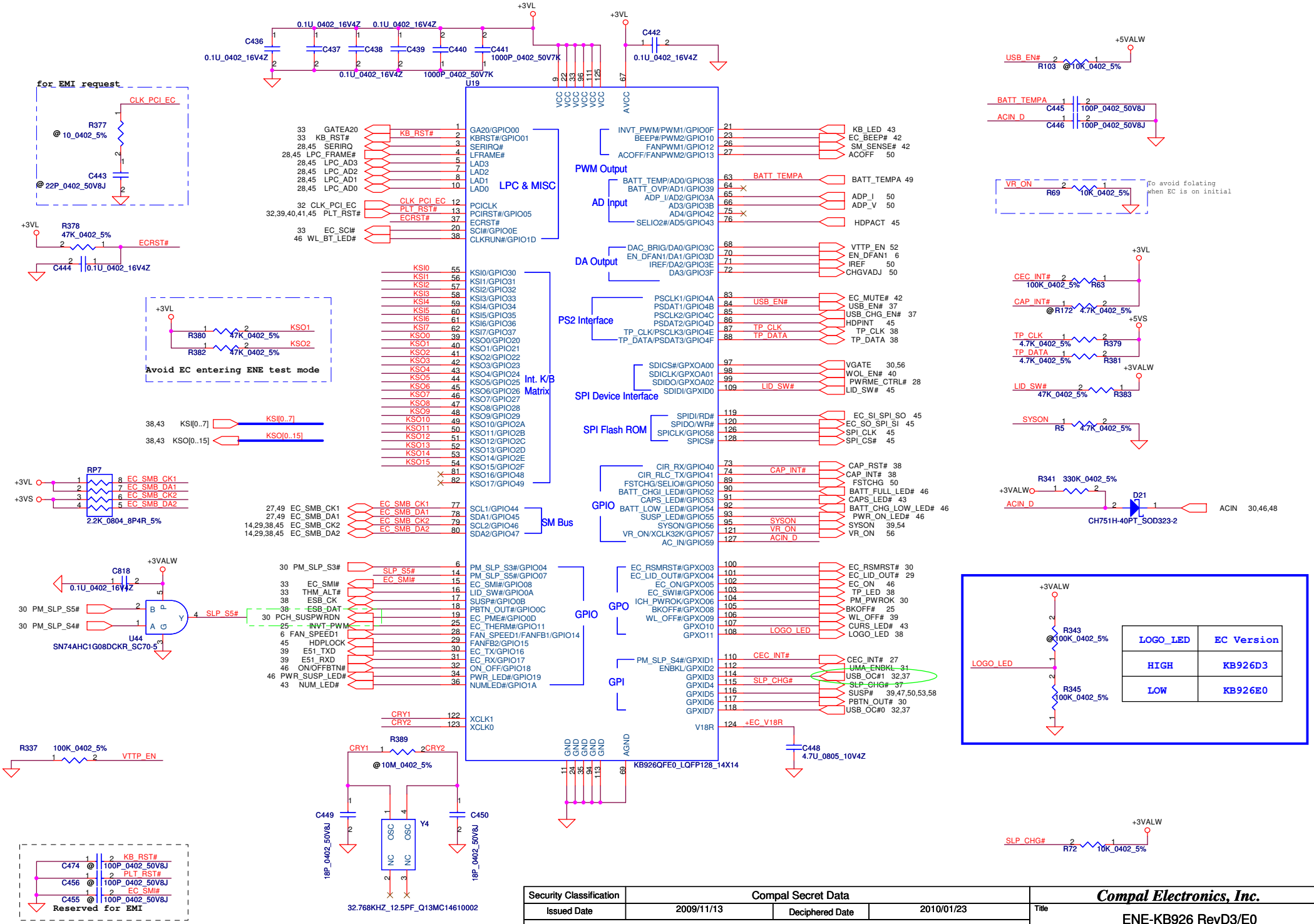

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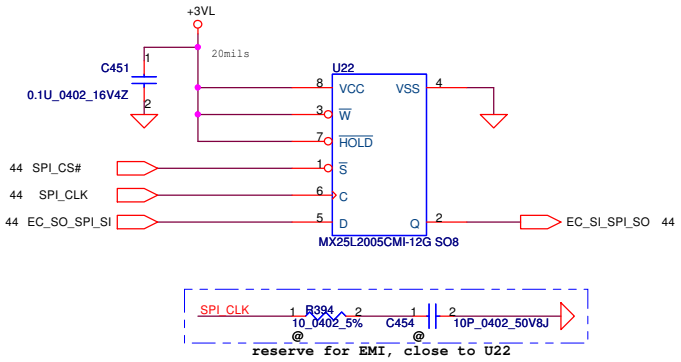
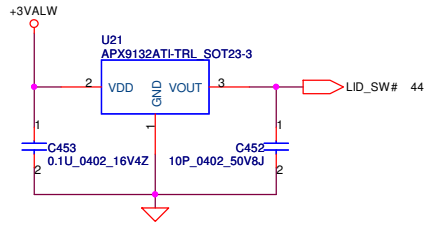
SPI Flash (256KB)

Socket: SP07000F500 & SP07000H900

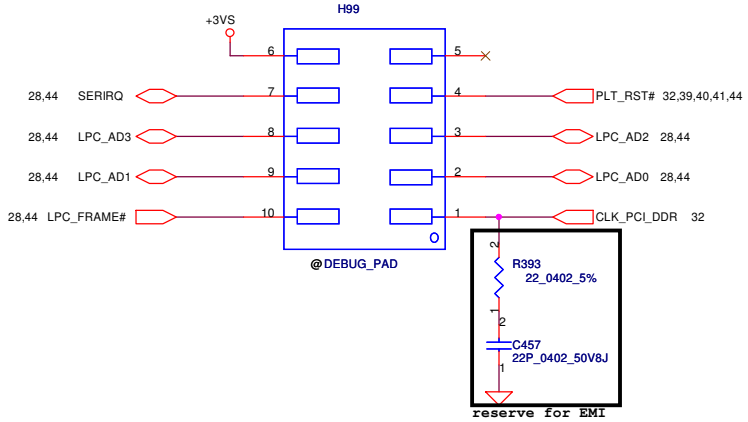


Lid SW

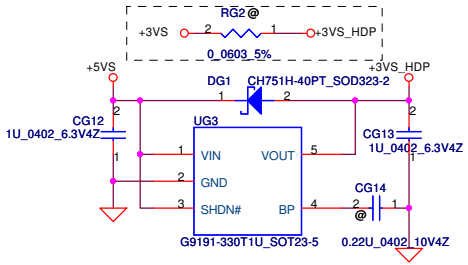


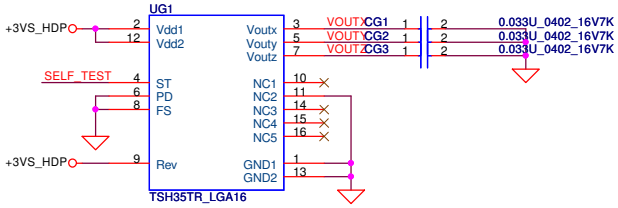
LPC Debug Port

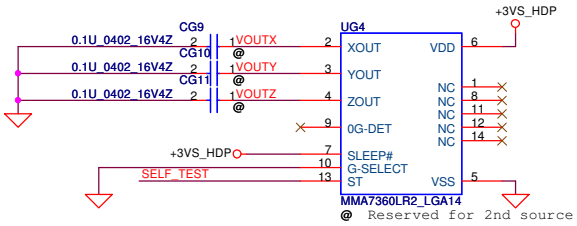
Please place the PAD under DDR DIMM.



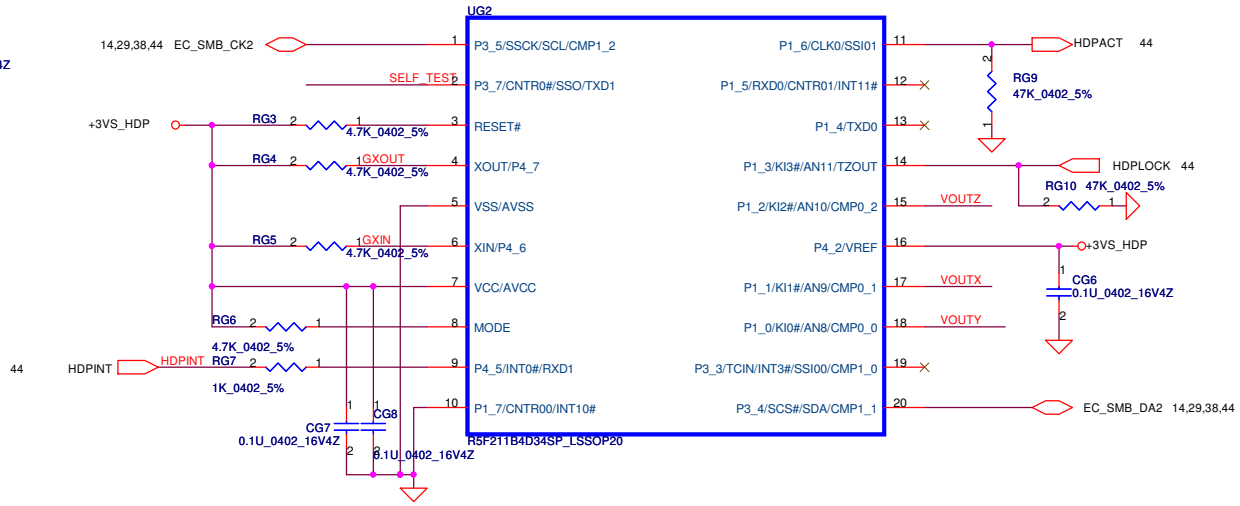
G-Sensor







SA00003A600 Supports ODD unexpected tray eject prevention



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Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: SPI ROM/G-SENSOR/Debug

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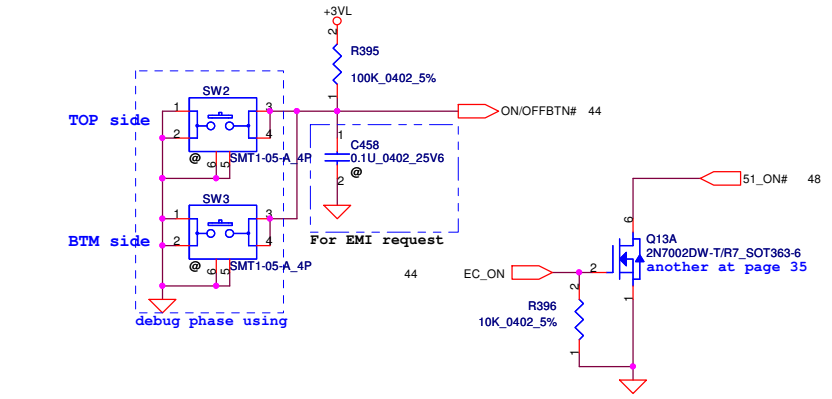
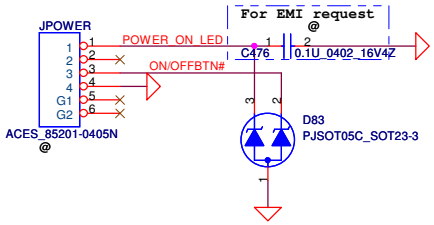
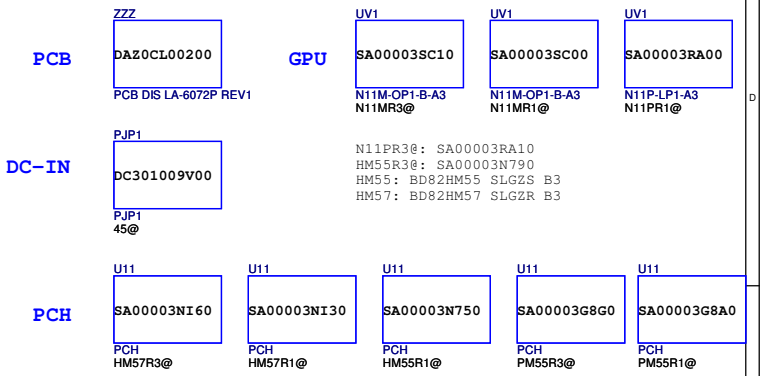
Power Button



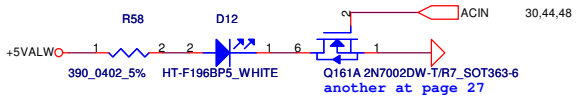
PWR/B Conn



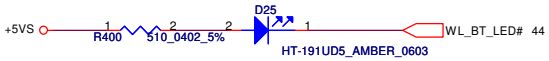
ISPD



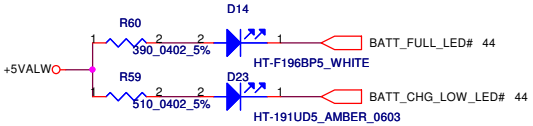
DC-IN LED



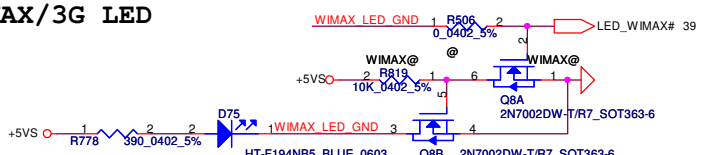
WL/BT LED



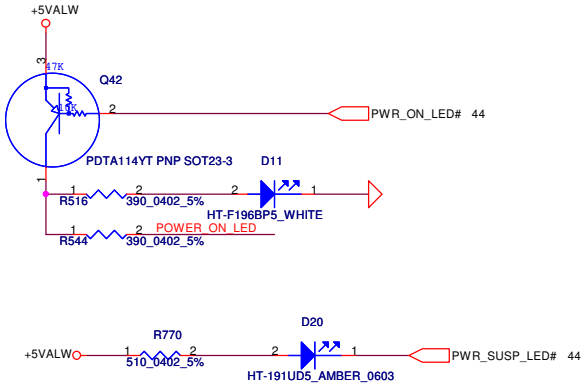
BATT CHARGE/FULL LED



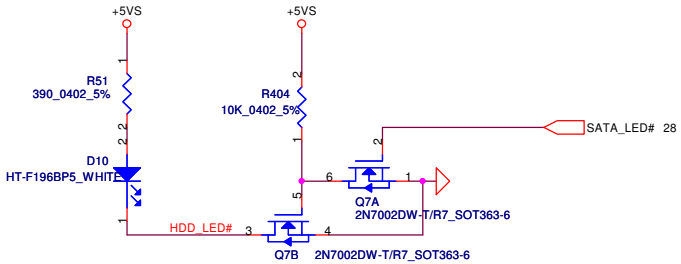
WiMAX/3G LED



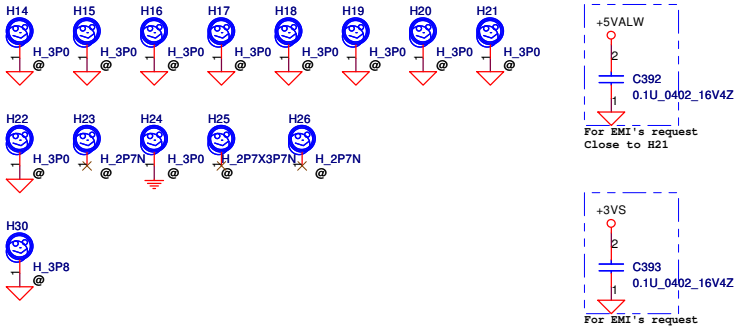
POWER/SUSPEND LED

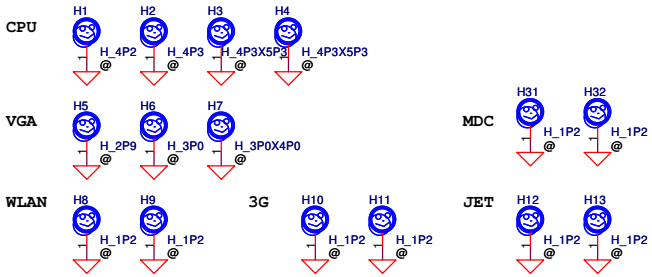


HDD LED

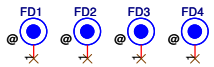


Screw Hole





PCB Fedical Mark PAD



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Compal Electronics, Inc.

Title: Comm. SW/ Sub Conn./LEDS

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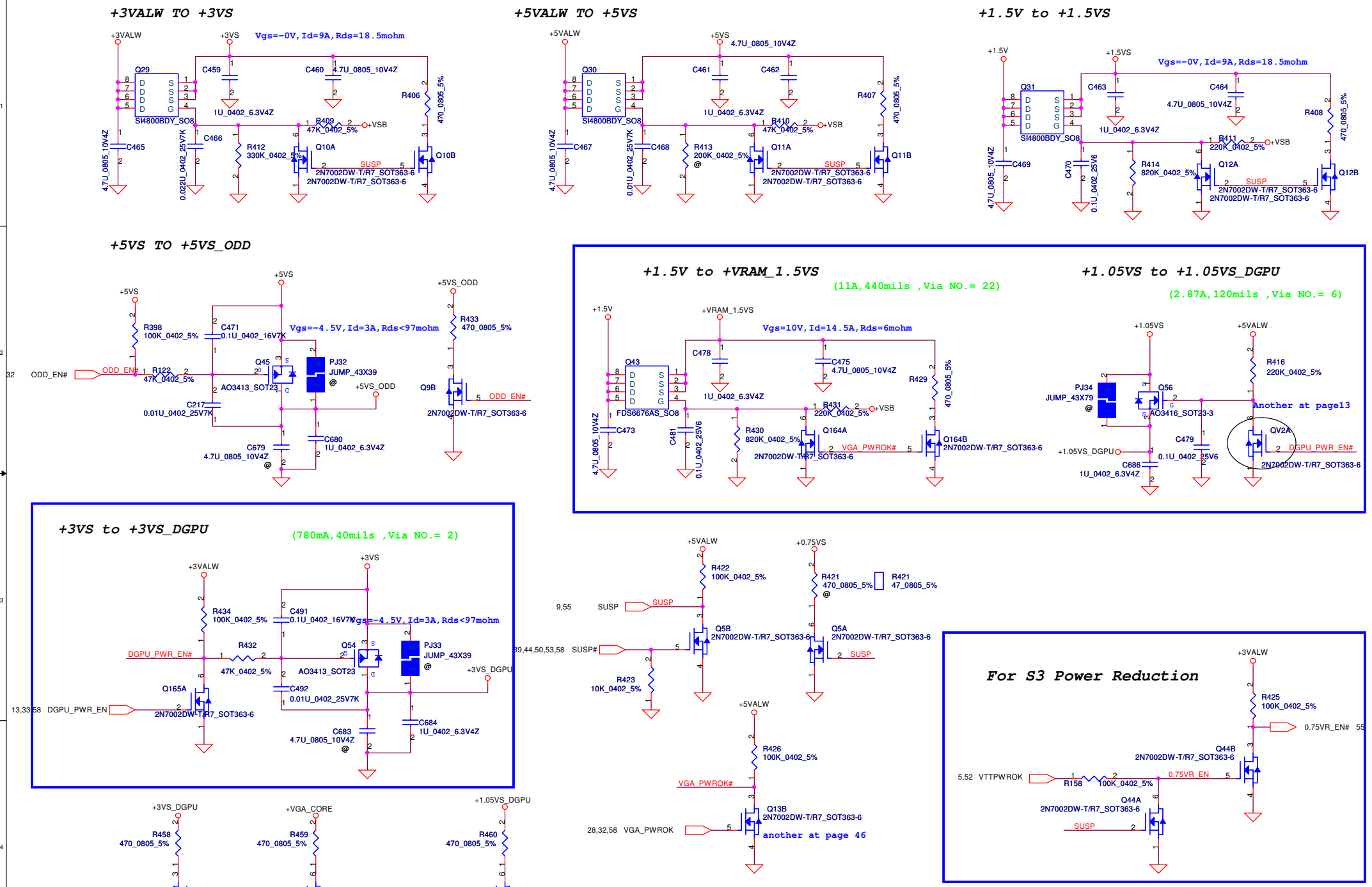

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Issued Date	2009/11/13	Deciphered Date	2010/01/23

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Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size | Document Number: NBQAA LA6072P M/B | Rev: 1.0

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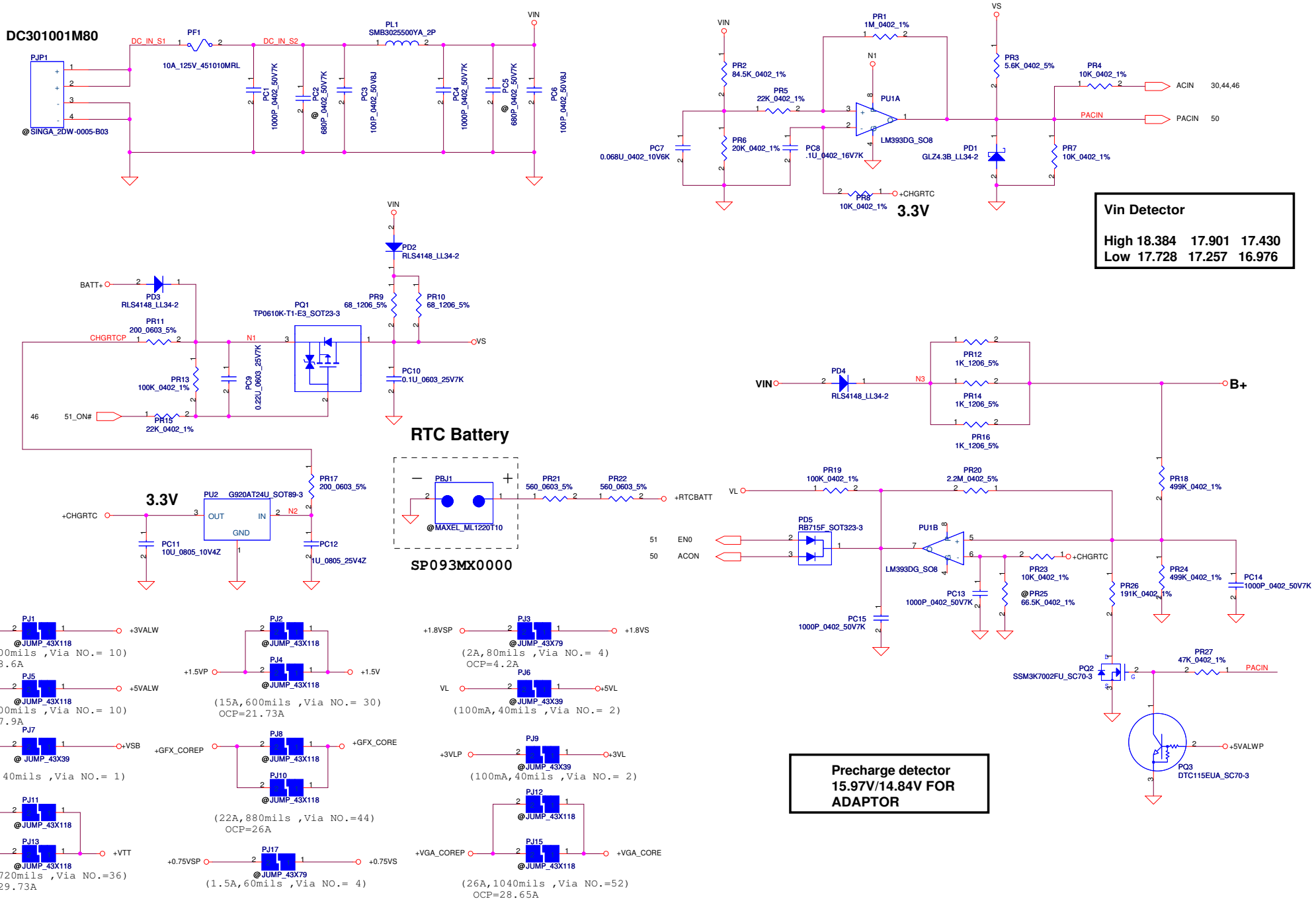

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Issued Date	2009/11/13	Deciphered Date	2010/10/21

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Compal Electronics, Inc.

Title: DCIN / DETECTOR

Size | Document Number: NBQAA DIS | Rev 1.0

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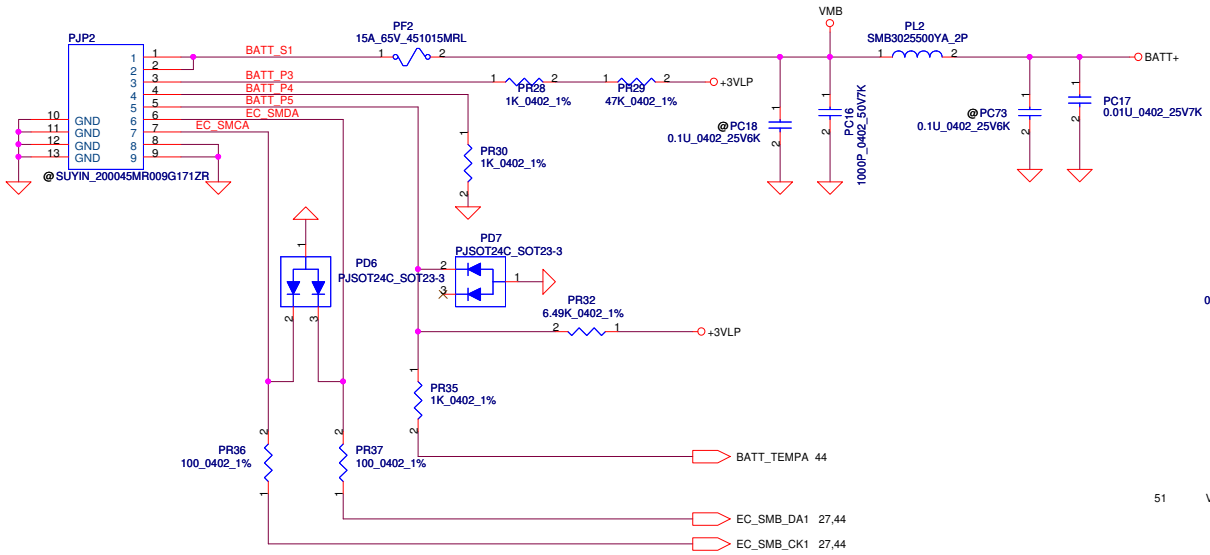


PH1 under CPU botten side :

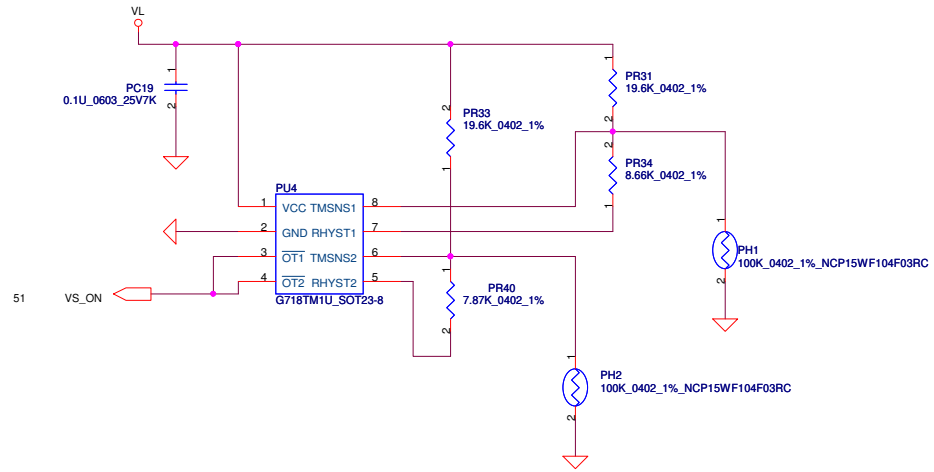
CPU thermal protection at 95 degree C

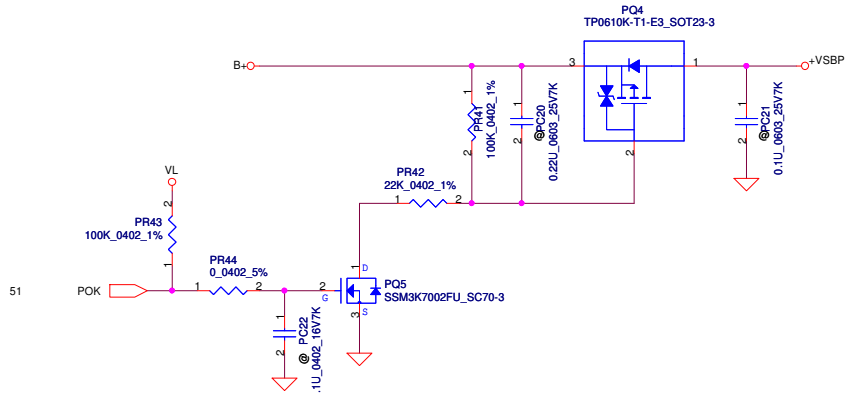
Recovery at 56 degree C

PH2 near main Battery CONN :

BAT. thermal protection at 95 degree C

Recovery at 48 degree C





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Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size | Document Number: NBQAA | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 49 of 61

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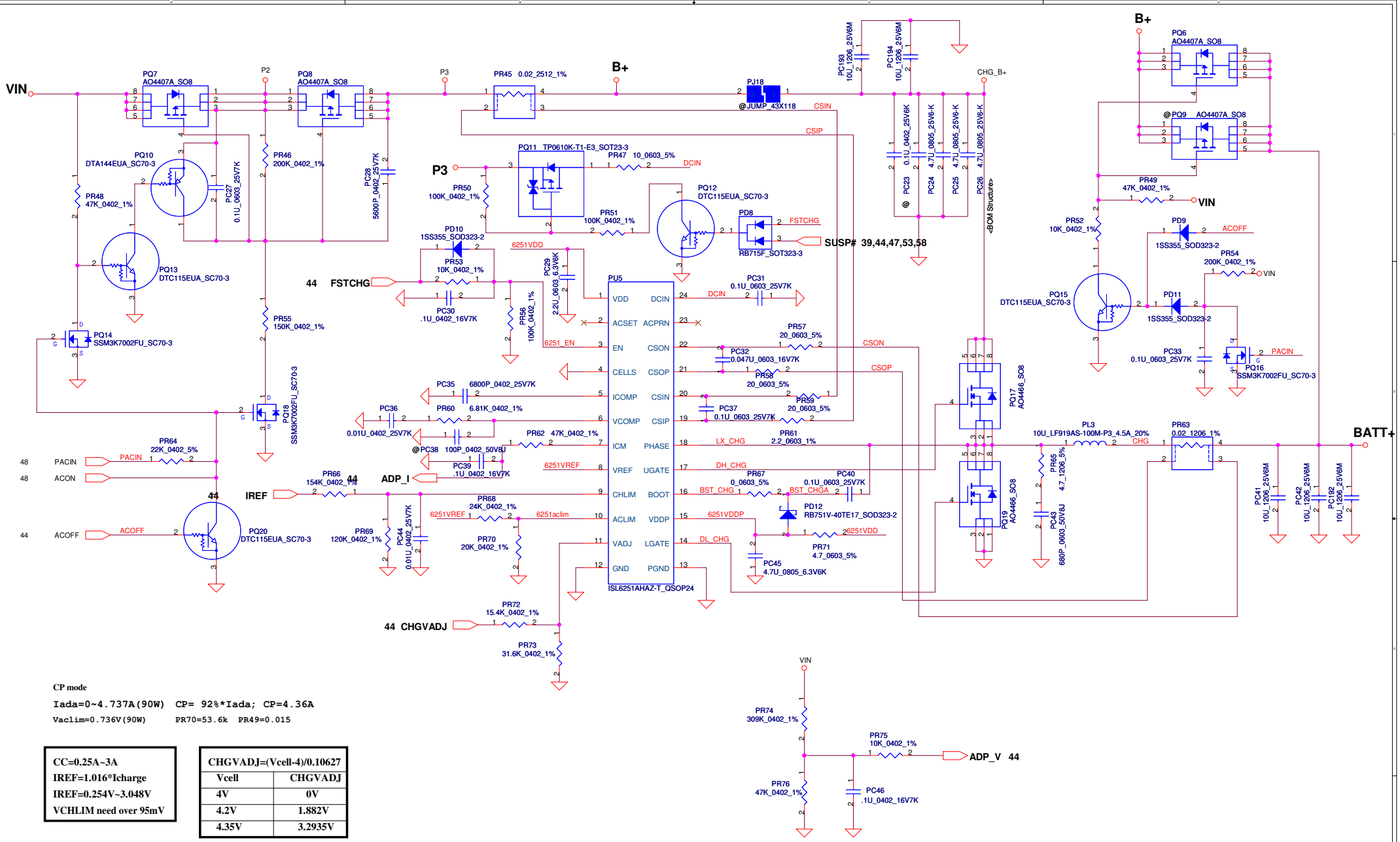

CP mode

Iada=0~4.737A(90W) CP= 92%*Iada; CP=4.36A

Vaclim=0.736V(90W) PR70=53.6k PR49=0.015

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

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Compal Electronics, Inc.

Title: CHARGER

Size: | Document Number: NBQAA | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 50 of 61

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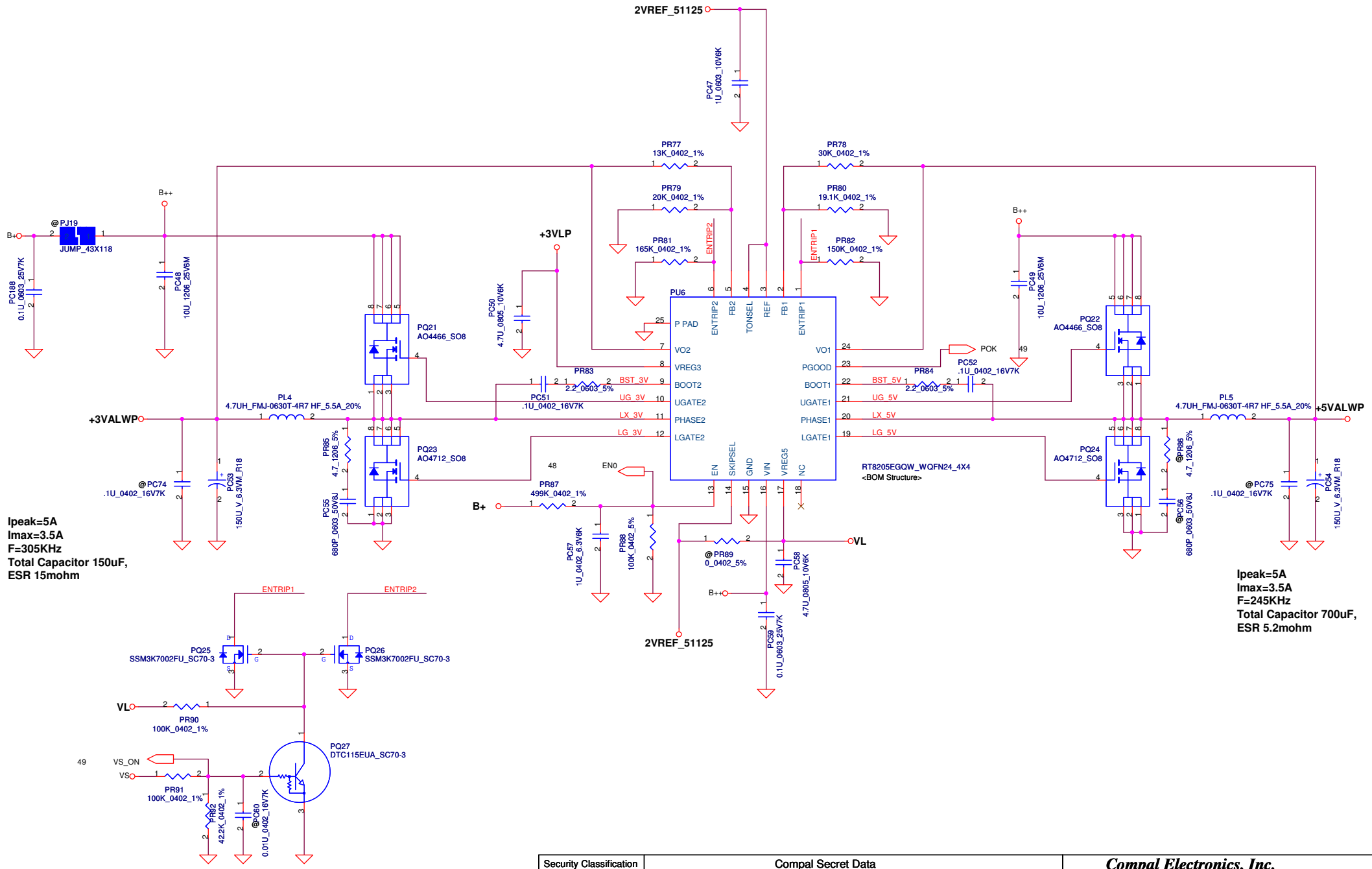

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

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Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size | Document Number: NBQAA | Rev: 1.0

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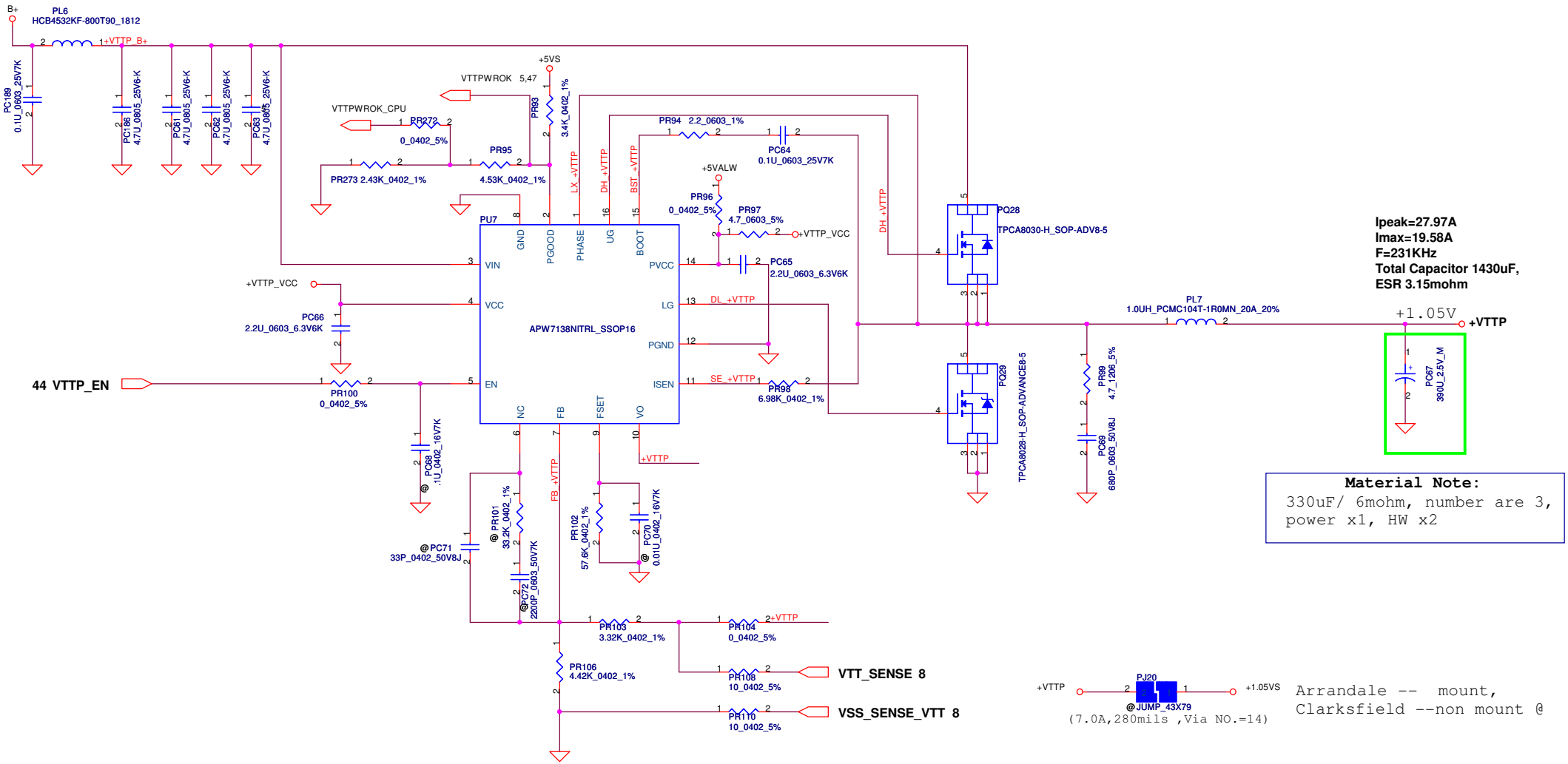

Security Classification	Compal Secret Data		
Issued Date	2009/11/13	Deciphered Date	2010/10/21

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Compal Electronics, Inc.

Title: +VTTP

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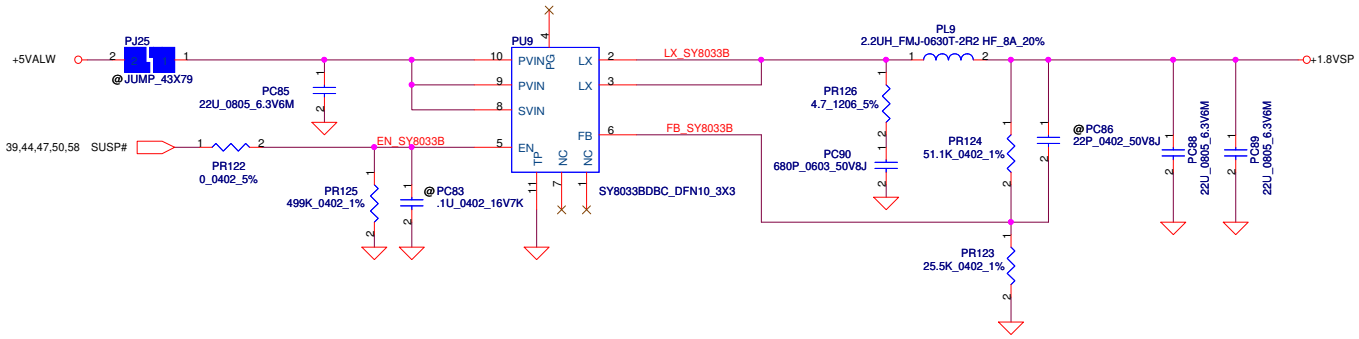

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: +1.8VSP

Size | Document Number: NBQAA | Rev: 1.0

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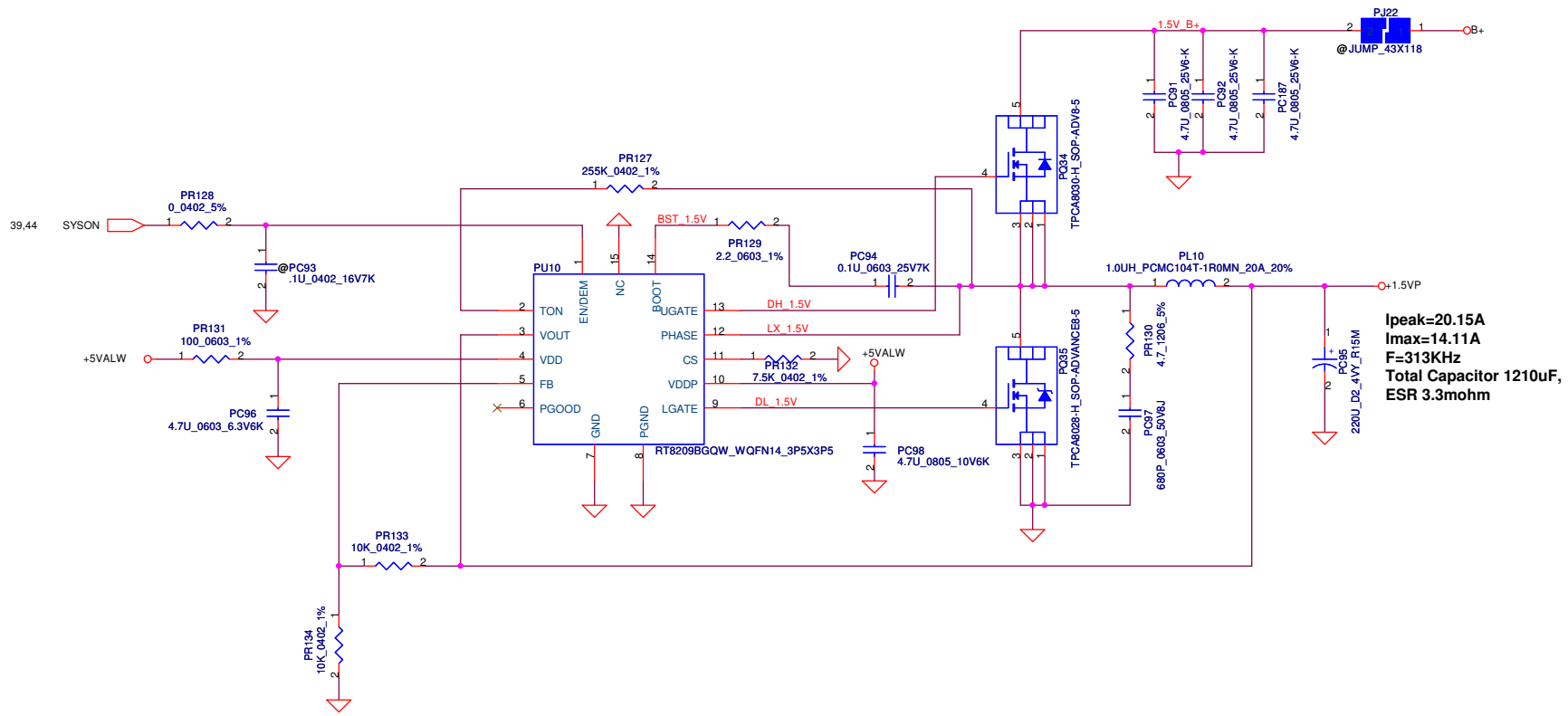

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Issued Date	2009/11/13	Deciphered Date	2010/10/21

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Compal Electronics, Inc.

Title: **+1.5VP**

Size: Custom | Document Number: NBQAA LA6072P M/B | Rev: 1.0

Date: Monday, March 22, 2010 | Sheet 54 of 61

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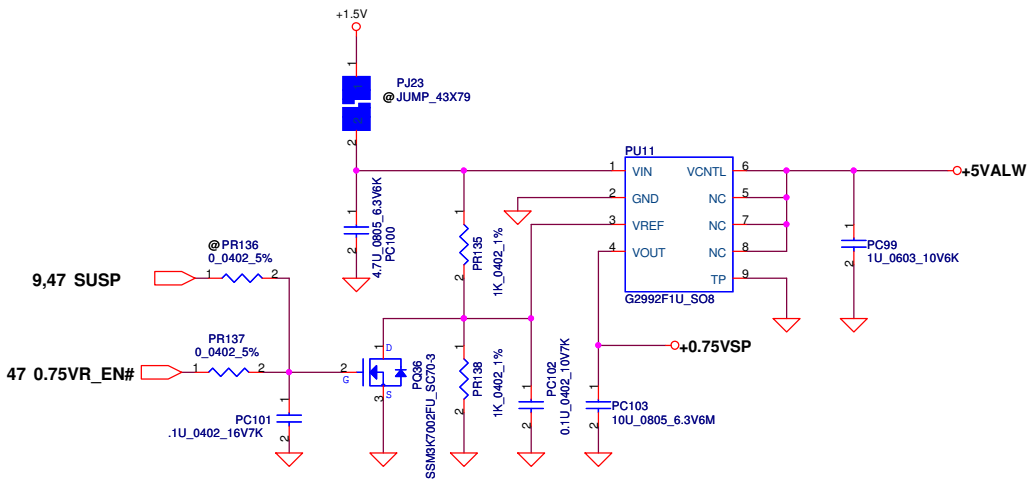

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Compal Electronics, Inc.

Title: 0.75VSP/

Size | Document Number: NBQAA LA6072P M/B | Rev: 1.0

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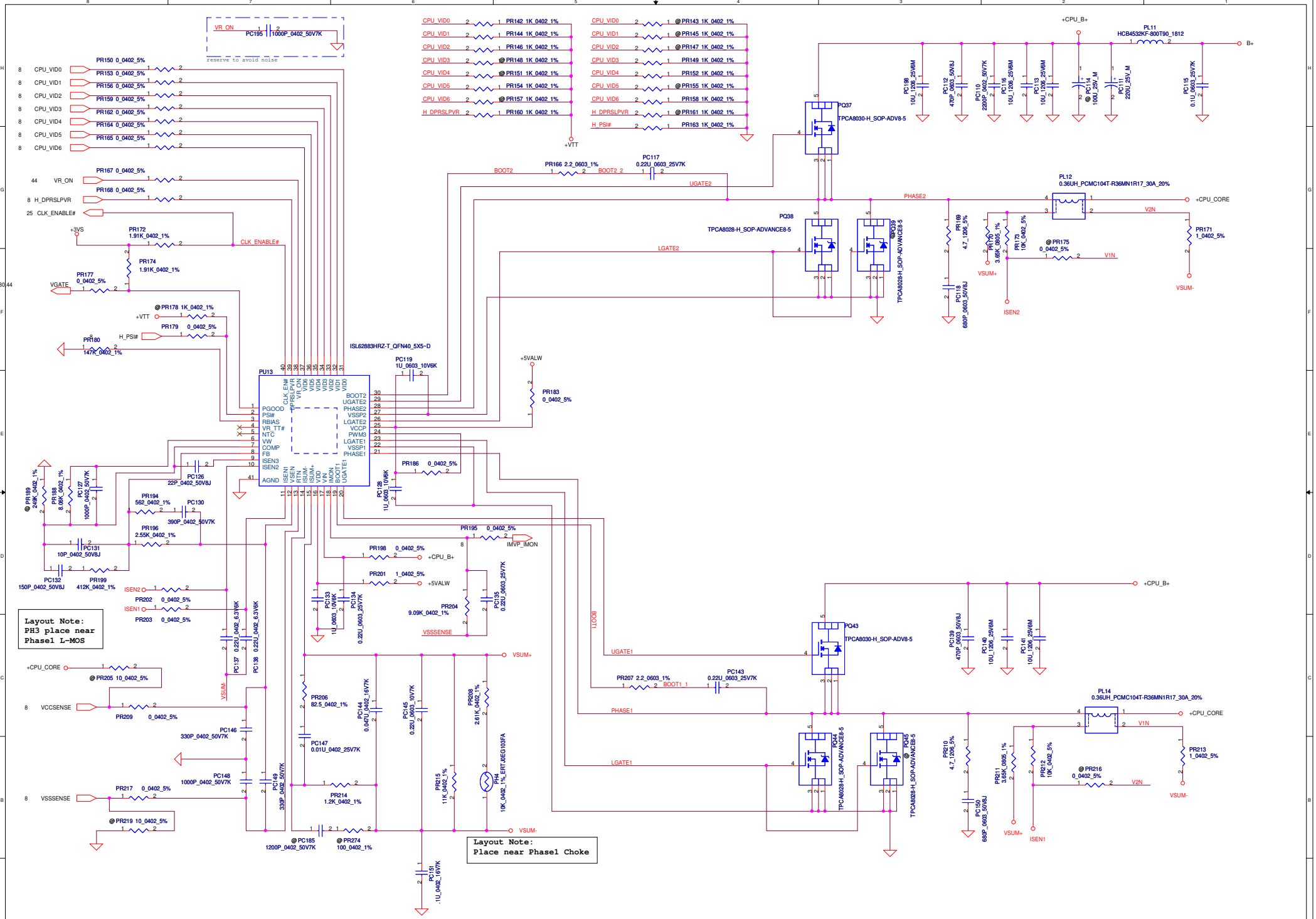

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Issued Date	2009/11/13	Deciphered Date	2010/10/21

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Compal Electronics, Inc.

Title: +CPU_CORE

Size: C | Document Number: NBQAA LA6072P M/B | Rev: 1.0

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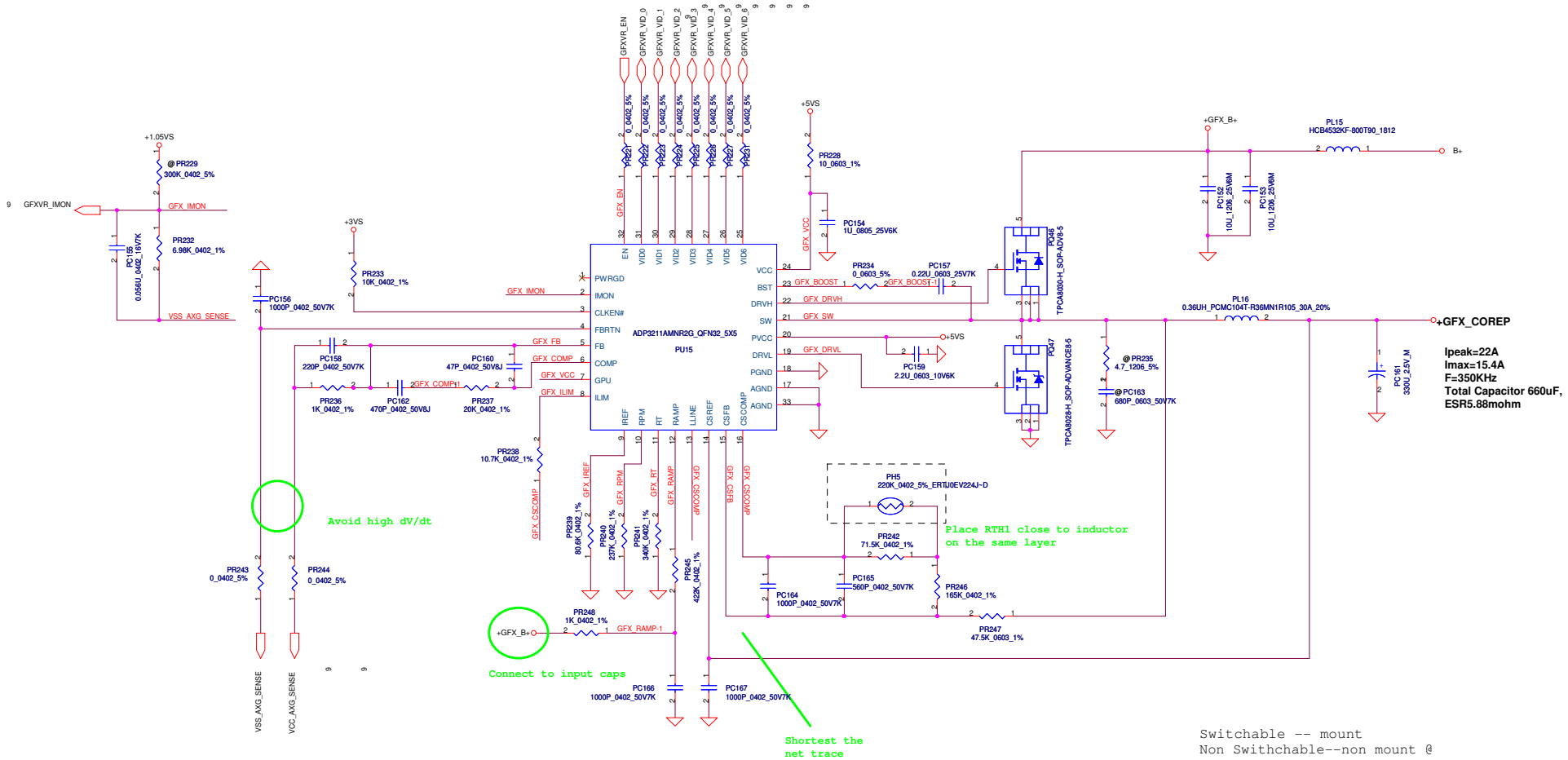

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/11/13	Deciphered Date	2010/10/21	Title: +GFX_COREP
				Size / Document Number: NBQAA LA6072P M/B — Rev 1.0
				Date: Monday, March 22, 2010 — Sheet 57 of 61

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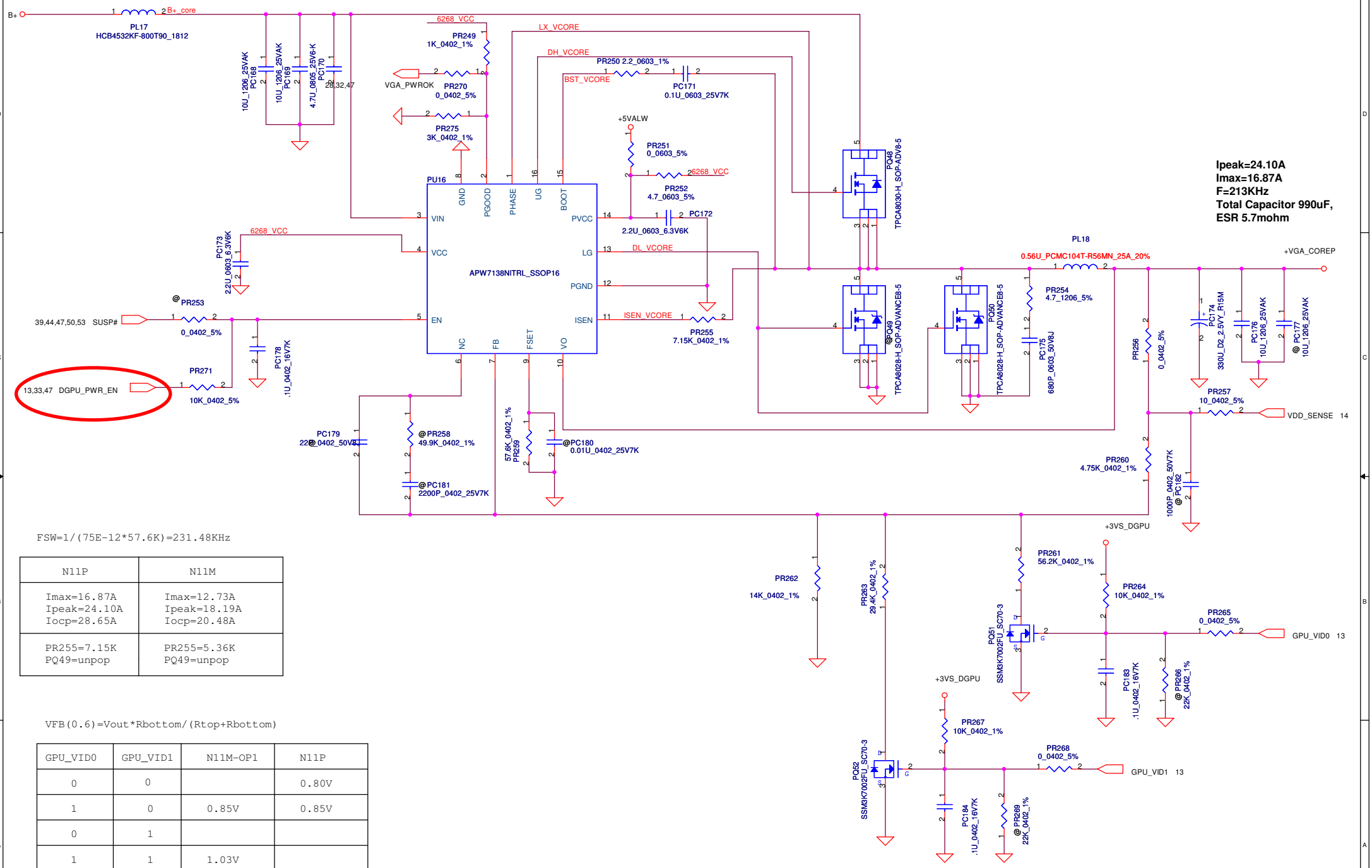

Ipeak=24.10A
Imax=16.87A
F=213KHz
Total Capacitor 990uF,
ESR 5.7mohm

FSW=1/(75E-12*57.6K)=231.48KHz

N11P	N11M
Imax=16.87A Ipeak=24.10A Iocp=28.65A	Imax=12.73A Ipeak=18.19A Iocp=20.48A
PR255=7.15K PQ49=unpop	PR255=5.36K PQ49=unpop

VFB(0.6)=Vout*Rbottom/(Rtop+Rbottom)

GPU_VID0	GPU_VID1	N11M-OP1	N11P
0	0		0.80V
1	0	0.85V	0.85V
0	1		
1	1	1.03V	
		PR260= 4.75K PR262 =14K PR261 =56.2K PR263=16.2K	PR260= 4.75K PR262 =14K PR261 =56.2K PR263=29.4K

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Compal Electronics, Inc.

Title: +VGA_COREP

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NO DATE	PAGE	MODIFICATION LIST	PURPOSE
2009/12/06	P48-59	Release	
2009/12/18	P49	PR31,PR33,PR34,PR40	PH1,PH2 setting point change
2009/12/18	P52	PR98	VTT adjust OCP
2009/12/18	P55	Remove PR136,Add PR137,PC101	0.75VSP Enable signal (EVT added by memo)
2009/12/18	P58	Add PR254,PC175	VGA add snubber (EVT added by memo)
2009/12/18	P58	PC174	VGA output cap change to lower
2009/12/28	P51,P52	Add PC188,PC189,PC115	Add EMC,EMI solution.
2009/12/28	P51	change PR83,PR84,Add PR85,PC55	For EMI,EMC solution
2010/01/06	P51	PR81,PR132,PR255	OCP setting.
2010/01/06	P58	change PR249,PR271,PC178	HW request
2010/02/05	P53	change PU9 solution	change 1.8V Solution
2010/02/05	P51	change PL4,PL5	Change to lower height to solve ME request
2010/01/28	P43	PC197	Reserve 10uF at B+ shape for ripple improvement.
2010/02/08	P50	Add PD6,PD7	ESD solution.
2010/02/08	P57	Change PR247	GFX load-line
2010/02/08	P50	Add PC192,PC193,PC194	ISN issue
2010/03/16	P50	Change PR45,PR68	CP setting
2010/03/16	P50	Change PL3	ME issue
2010/03/16	P51	Change PC53,PC54	ME issue
2010/03/16	P53	PR122,PC83 unmount	1.8V enable signal adjust
2010/03/16	P56	Add PC195	VR_ON prevent noise,same as UMA
2010/03/16	P58	Change PC174	ME issue
2010/03/16	P58	Change PR264,PR265,PR267,PR268,PR263,PC184,PQ52	GPU voltage adjust
2010/03/18	P57	Add PC198	High frequency noise
2010/03/22	P58	Add PR275	Adjust VGA POK voltage level for HW request

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Title: **Power PIR**

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PIR (Product Improve Record)

NBQAA LA-6072P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	12/22	25	Change JLVDS routing	To prevent workmanship and burn issue
2.	12/22	09	Change Q33 routing	For common design
3.	12/22	47	Change Q43 routing	For common design
4.	12/22	39	Change JEXP footprint to SANTA_130861-2_26P_RT-T	Modify footprint
5.	12/22	38	Change JTPL footprint to P-TWO_161021-06021_6P-T	For ME's request
6.	12/22	43	Change JKBL footprint to ACES_85201-04051_4P-T	For ME's request
7.	12/22	13	Delete DV2, Add RV124, QV2 for CLKREQ_VGA#	CLKREQ_VGA# circuit for NV's Optimus
8.	12/23	38	Change JCS footprint to P-TWO_161021-10021_10P-T	For ME's request
9.	12/23	38	Change JTOUCH footprint to P-TWO_161021-10021_10P-T	For ME's request
10.	12/23	33	Change PCH's GPIO57 netname to OPTIMUS_EN# and pull down to GND	For BIOS recognizing Optimus
11.	12/23	33	Change PCH's GPIO45 netname to LVDS_SEL	For Common design
12.	12/23	33	Change PCH's GPIO39 netname to CIR_EN#	For Common design
13.	12/24	39	Add DM2, QM1, BT_CTRL on JWLAN.5	For WLAN/BT combo module
14.	12/24	42	Add RA43 on EC_MUTE#	For Audio issue
15.	12/24	43	Detele JEXMIC.5 from GND	For Audio issue
16.	12/24	44	Change PWRME_CTRL to PWRME_CTRL#	Active low signal
17.	12/24	33	Delete GND guide pins of JTOUCH, JCS, JTPL, JODD1	For common design
18.	12/29	29	Add C254 on CLKREQ_WLAN#	For EMI's Request
19.	12/29	43	Exchange JKBL pin1 and pin4	To meet correct footprint
20.	12/29	37	Add C389 on U14	For EMI's Request
21.	12/29	46	Add C392 on H21 for +5VALW	For EMI's Request
22.	12/29	40	Stuff CL7, CL23, CL24	For EMI's Request
23.	12/29	46	Add C393, close to C7 for +3VS	For EMI's Request
24.	12/29	32	Add R55 on DGPU_RST#	For common design
25.	12/29	27	Add R314 on HDMI_HPD and U9	To prevent ESD damage to U9
26.	01/03	47	change +1.05VS_DGPU routing	To turn on/off normally

REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	02/01	31	Change RA40 to pull up +5VL	Support S/M function in battery mode
2.	02/01	30	Change RA34 to pull up +3VL	Support S/M function in battery mode
3.	02/01	44	Add R103 to USB_EN# and pull up +5VALW	For common code with NWQAA
4.	02/01	44	Add R69 to VR_ON and pull low to GND	To avoid folating when EC is on initial
5.	02/01	30	Add C434 to VGATE	Reserve to avoid noise
6.	02/01	05	Add C482 to H_PWRGOOD	Reserve to avoid noise
7.	02/01	40	Add UL4	for 10/100/1000 transformer co-layout
8.	02/01	38	Add MDC circuits	For A51's request, Add MDC in DIS SKU
9.	02/01	35	Reserve U54 for +1.5VALW LDO and change VCCSUSHDA power rail	For MDC design change
10.	02/01	28	Add R287, R289, R291, R293 for Azalia bus to MDC	For MDC design change
11.	02/02	46	Add H31, H32	For MDC design change
12.	02/02	44	Add CAP_RST# on EC pin73 and link to JCS	For Cap sensor design change
13.	02/04	31	Stuff R133, R135 to 100Kohm PD GND	To prevent PCH pending internal HPD
14.	02/04	14	Reserve UV4,RV54,CV56,RV44	Reserved for VBIOS
15.	02/04	42	Add RA45, un-stuff RA43	To solve audio issue
16.	02/06	32	Exchange USB port 4&8	Design change, for A51's request
17.	02/08	08	Change C117,C118,C119,C120,C127,C128,C129	To improve ESD
18.	02/08	40	Change LL1, CL13	For design change
19.	02/09	41	Change RC7, RC8, RC9, RC12, RC13, RC14 from 0 ohm to 22 ohm	For EMI's request

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PIR (Product Improve Record)

NBQAA LA-6072P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	03/11	27	Add R148	To solve display compatibility issue
3.	03/11	15	Change CV58 from OSCON to POLY type	Due to the keyboard stress test is fail
4.	03/11	09	Change C216 from OSCON to POLY type	Due to the keyboard stress test is fail
5.	03/11	11	Change C163 from OSCON to POLY type	Due to the keyboard stress test is fail
6.	03/11	14	Delete UV4,RV54,CV56,RV44	Design change, no need extra BIOS ROM
7.	03/11	25	Stuff D84,D82,D19,D83	For ESD's request
8.	03/11	34	Change L12 from bead to R389 2.2 ohm+- 1%	For CRT issue
9.	03/14	13	Reserve YV1,RV29,CV45,CV46	Reserved for design change
10.	03/14	33	Change R221 to 1K ohm	For NV's Optimus sequence
11.	03/14	32	Change R55 to 1K ohm	For NV's Optimus sequence
12.	03/14	32	Reserve R334, add R336	For NV's Optimus sequence
13.	03/14	39	Change QM1 to Q14B	For cost down
14.	03/15	42	Un-mount CA16	For audio noise issue
15.	03/15	46	Un-mound SW2,SW3	Power button is no need after pre-MP
16.	03/16	42	Change CA12.1, RA12.2, CA18.2 from GND to AGND	For audio noise issue
17.	03/16	42	Change CA9 and CA10 to from 4700pF tp 1uF	For audio noise issue
18.	03/16	42	Add CA34~CA40 and CA51	For audio noise issue
19.	03/18	41	Change Card reader solution from O2 to JMB389C/385C	For design change
20.	03/19	27	Add D54	For HDMI CEC
21.	03/19	34	Add L12 that reserved 0 ohm for EMI	For CRT issue
22.	03/19	46	H22 from 6.0 to 3.0	For ME's request
23.	03/20	20	Change BIOS ROM footprint to M25P80-VMW6TP_SO8	No need the debug connector in MP phase
24.	03/22	13	Stuff RV28, un-stuff RV105	Reserved for 27M_SSC from clock gen
25.	03/22	43	Add RA22,RA23	Reserved to solve GPRS noise
26.	03/22	05	Stuff C482	To avoid noise
27.	03/22	30	Stuff C434	To avoid noise

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