

8. Block Diagram and Schematic

SAMSUNG PROPRIETARY THIS DOCUMENT CONTAINS CONFIDENTIAL PROPRIETARY INFORMATION THAT IS SAMSUNG ELECTRONICS CO.'S PROPERTY. DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS EXCEPT AS AUTHORIZED BY SAMSUNG.																					
<h1>Bremen-L</h1>																					
CPU : Intel Penryn																					
Chip Set : Intel Cantiga & ICH9M																					
Remarks : Montevina Platform																					
<div>Model Name : Bremen-L PBA Name : MAIN PCB Code : GCE : NAN : HAN : Dev. Step : PV Revision : 1.0 T.R. Date : 2009.10.27</div>																					
<table border="1"><thead><tr><th>Design</th><th>CHECK</th><th>APPROVAL</th></tr></thead><tbody><tr><td> </td><td> </td><td> </td></tr><tr><td> </td><td> </td><td> </td></tr></tbody></table>				Design	CHECK	APPROVAL															
Design	CHECK	APPROVAL																			
Owner : SEC Mobile R & D Signature : X																					
<table border="1"><thead><tr><th>DESIGN</th><th>DATE</th><th>TITLE</th><th>SAMSUNG ELECTRONICS</th></tr></thead><tbody><tr><td>Jun PARK</td><td>10/10/2008</td><td>Bremen-L</td><td rowspan="3">PART NO. BA41-xxxxxA</td></tr><tr><td>YMAHN</td><td>DEV. STEP PV</td><td>MAIN</td></tr><tr><td>HJKIM</td><td>REV 1.0</td><td>COVER</td></tr><tr><td colspan="2">LAST EDIT</td><td>October 27, 2009 14:27:43 PM</td><td>PAGE 1 OF 59</td></tr></tbody></table>				DESIGN	DATE	TITLE	SAMSUNG ELECTRONICS	Jun PARK	10/10/2008	Bremen-L	PART NO. BA41-xxxxxA	YMAHN	DEV. STEP PV	MAIN	HJKIM	REV 1.0	COVER	LAST EDIT		October 27, 2009 14:27:43 PM	PAGE 1 OF 59
DESIGN	DATE	TITLE	SAMSUNG ELECTRONICS																		
Jun PARK	10/10/2008	Bremen-L	PART NO. BA41-xxxxxA																		
YMAHN	DEV. STEP PV	MAIN																			
HJKIM	REV 1.0	COVER																			
LAST EDIT		October 27, 2009 14:27:43 PM	PAGE 1 OF 59																		

COM-220-015(1996.6.5) REV. 3

D:\users\mobile24\mentor\Bremen-LPV\Bremen-L_MAIN

8. Block Diagram and Schematic



8. Block Diagram and Schematic

4

SAMSUNG PROPRIETARY
THIS DOCUMENT CONTAINS CONFIDENTIAL
PROPRIETARY INFORMATION THAT IS
SAMSUNG ELECTRONICS CO.'S PROPERTY.
DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS
EXCEPT AS AUTHORIZED BY SAMSUNG.

3

2

1

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9M	Master		SMBUS Master
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	
SODIMM1	1010 001X	A4h	
MICOM	Master		
BATTERY EMC2102	0001 011X	16h	
	0111 101X	7Ah	

USB PORT Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0	0 USB PORT (RIGHT, SUB)	UHCI_3	6 USB PORT (RIGHT, SUB)
UHCL_1	2 USB PORT (LEFT)	UHCI_4	8 CAMERA(17')
	3		9 CAMERA(15')
UHCL_2	4 CARD READER(AU6336)	UHCI_5	11
	5 BLUETOOTH(TBD)		

SATA Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
SATA0	HDD	SATA1	ODD
SATA2	-	SATA3	-

PCI EXPRESS Assignment

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
PCle1	WLAN	PCle2	Wired LAN
PCle3	-	PCle4	-

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	
Crystal	10MHz	MICOM	
Crystal	14.318MHz	CLOCK-Generator	
Crystal	25MHz	LAN	

Voltage Rails

Power Rail	Descriptions	Power Rail	Descriptions
VDC_ADPT	Primary DC system power supply (9 to 19V)	P1.05V_PEG	P1.05V (Direct Media Interface Compensation)
VDC	Charger Reference Voltage Source	P5.0V	5.0V Power Rail (off in S3-S5)
VDC_CHG	3.3V supply for the RTC well.	P3.3V	3.3V Power Rail (off in S3-S5)
PRTC_BAT	5.0V always power well	P1.05	1.05V Power Rail (off in S3-S5)
P5.0V_ALW	12.0V always power well	P0.9V	DDR2 Termination
P1.7V_VREF	Power Chip Reference	P5.0V_AUX	5.0V Power Rail (off in S4-S5)
P2.0V_VREF	Power Chip Reference	P3.3V_AUX	3.3V Power Rail (off in S4-S5)
P5.0V_VREF_FILT	Power Chip Reference	P1.8 AUX	1.8V Power Rail (off in S4-S5)
		CPU_CORE	Core Voltage for CPU
P3.3V_MICOM	Output voltage of RT8205AGQW (if VDC is removed, it will be off)	AUD_P5V	5.0V supply for Audio
LCD_VDD3V	3.3V (LED LCD)	P4.75V_AUD	Audio Analog Voltage
KBC3_CHG4.2V	To charge battery	P5.0V_STB	To charge USB device at sleep status
		P5.0V_ODD	5.0V supply at SUB_ODD Board
P1.2V_LAN	Internal Regulator's Power of LAN Controller	EGFK_CORE	nVidia Graphic Chip power
P2.5V_LAN		P1.5V	1.5V Power Rail (off in S3-S5)
P3.3V_MCD	3.3V (3-in-1 Socket)	P1.5 AUX	1.5V Power Rail (off in S4-S5)
		P1.8V	1.8V Power Rail (off in S3-S5)

REVISION HISTORY

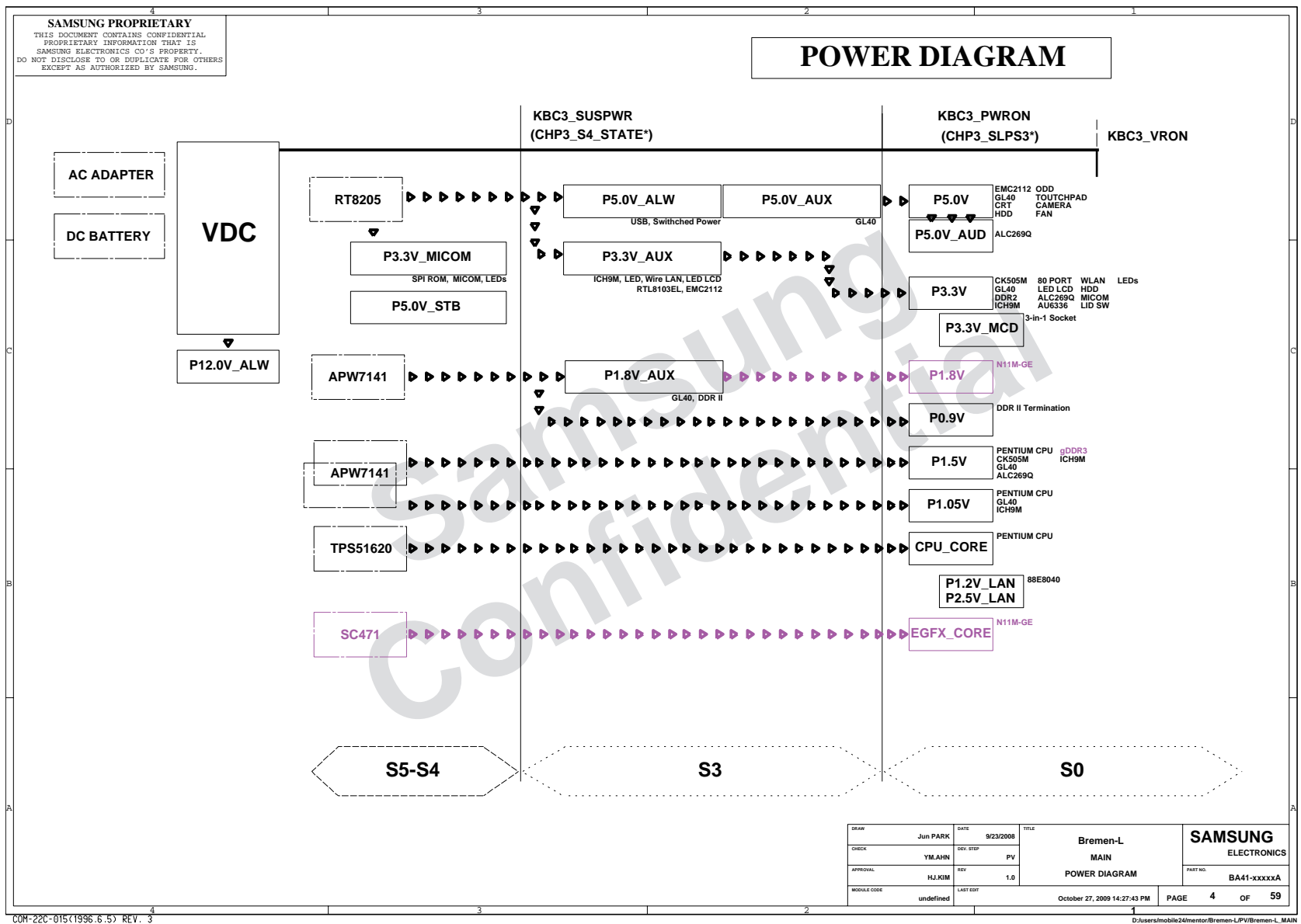
See rev notes for more information.

DRAW	Jun PARK	DATE	9/23/2008	TITLE	Bremen-L	PART NO. SAMSUNG ELECTRONICS BA41-xxxxxA
CHECK	YMLAHN	DEV STEP	PV	MAIN		
APPROVAL	HJ.KIM	REV	1.0	BOARD INFO		
MODULE CODE	undefined	LAST EDIT				
				October 27, 2009 14:27:43 PM		PAGE 3 OF 59

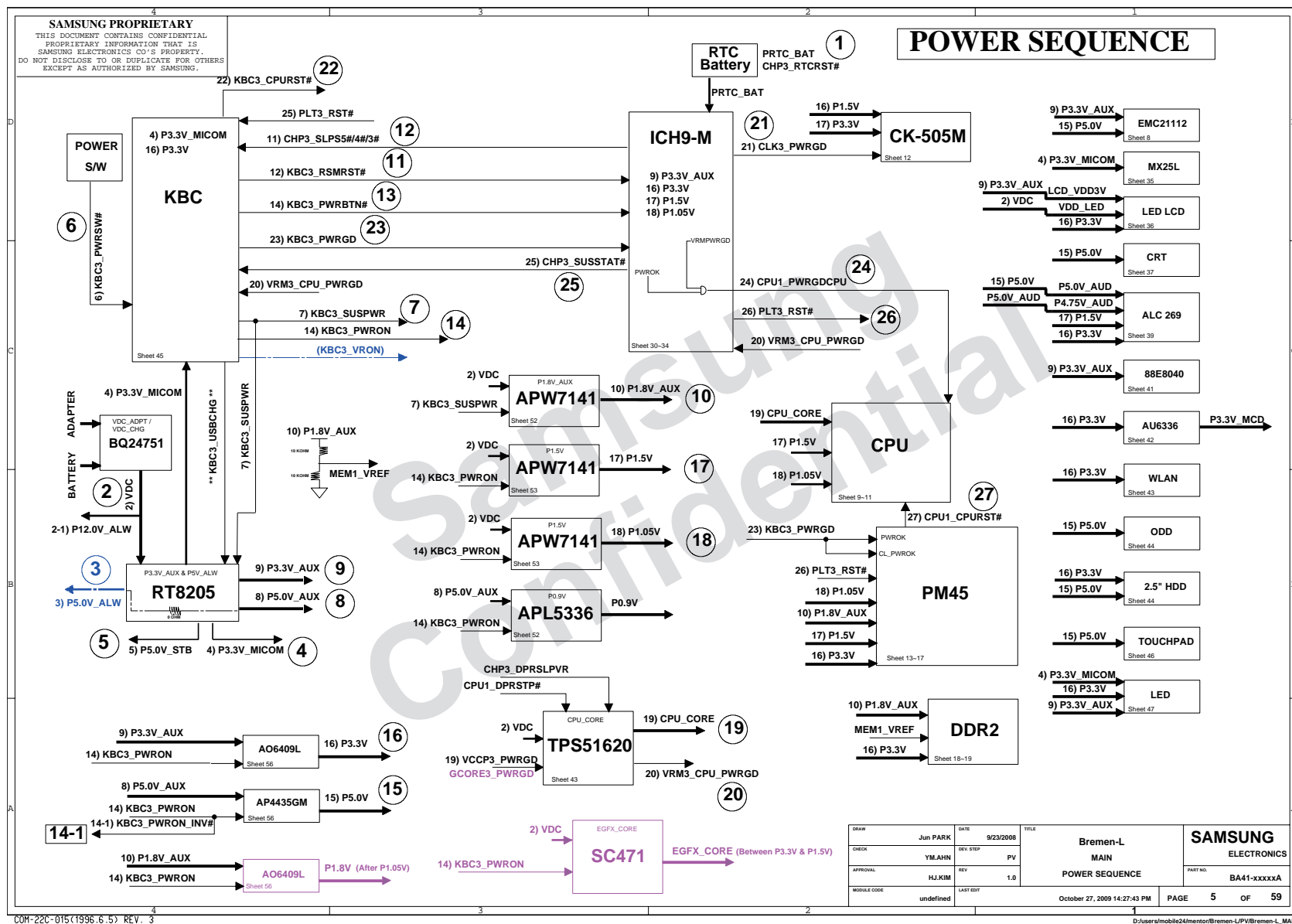
COM-22C-015(1996.6.5) REV. 3

D:\Users\mchiba\Documents\Bremen.L (PV)\Bremen.L

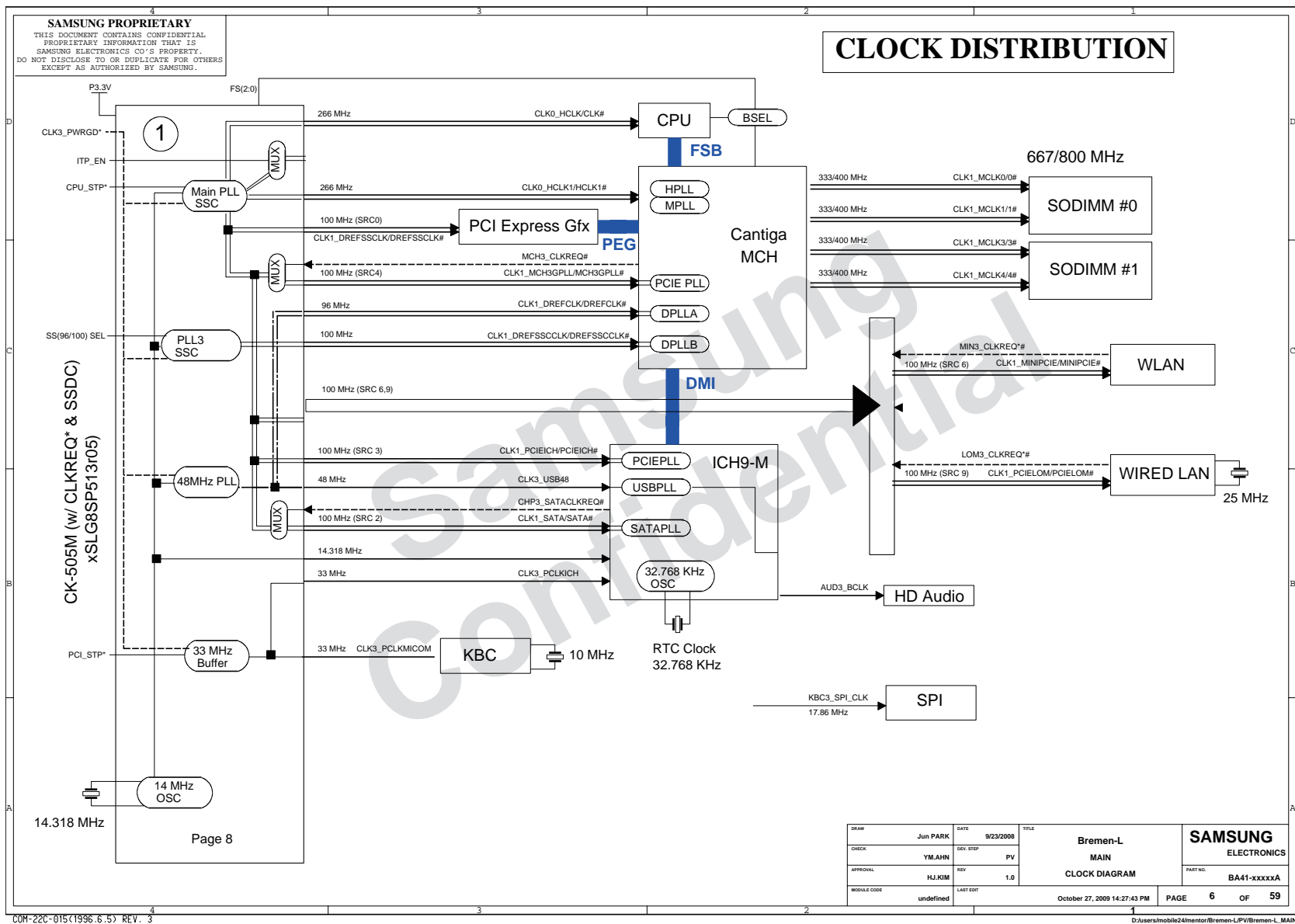
8. Block Diagram and Schematic



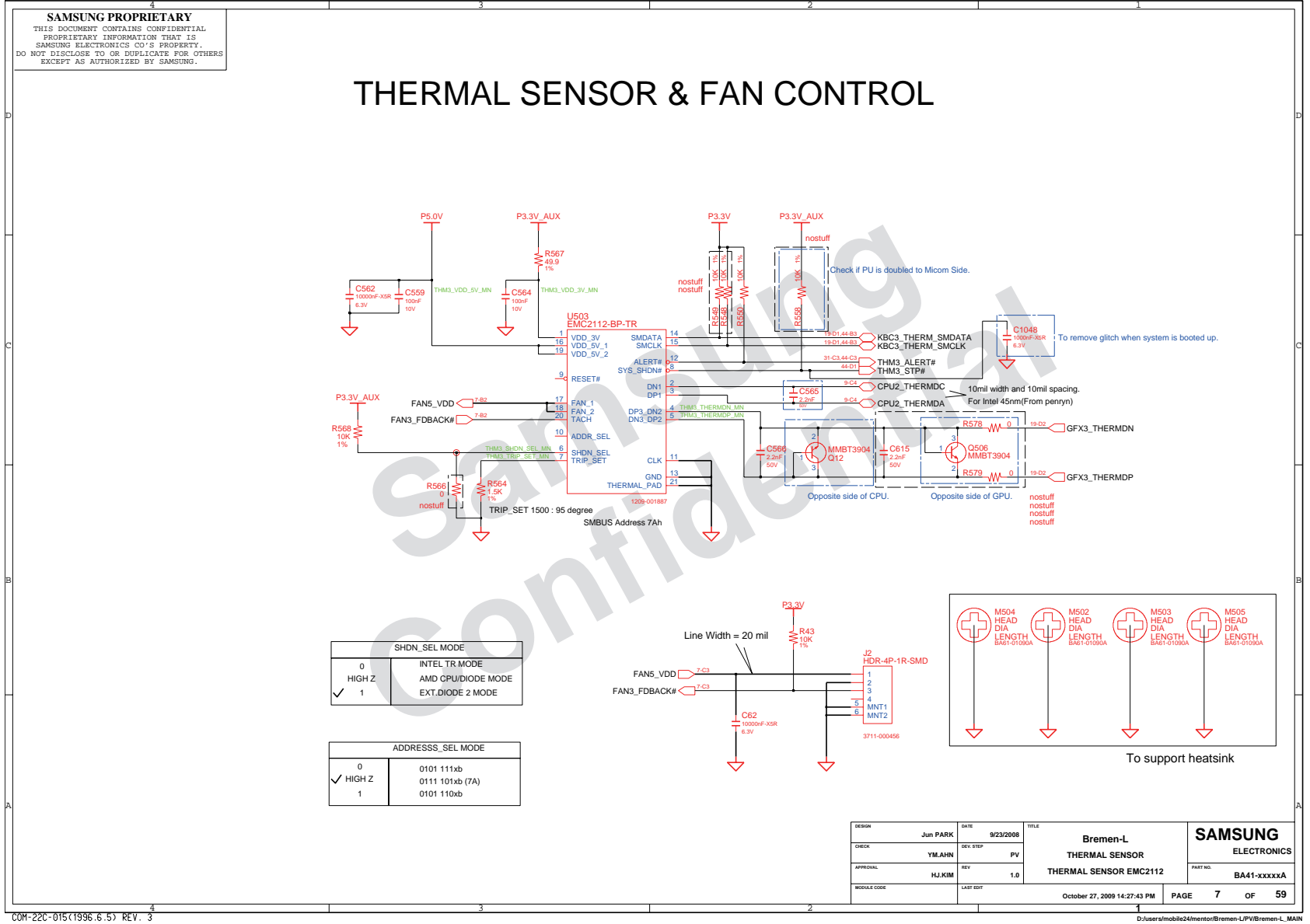
8. Block Diagram and Schematic



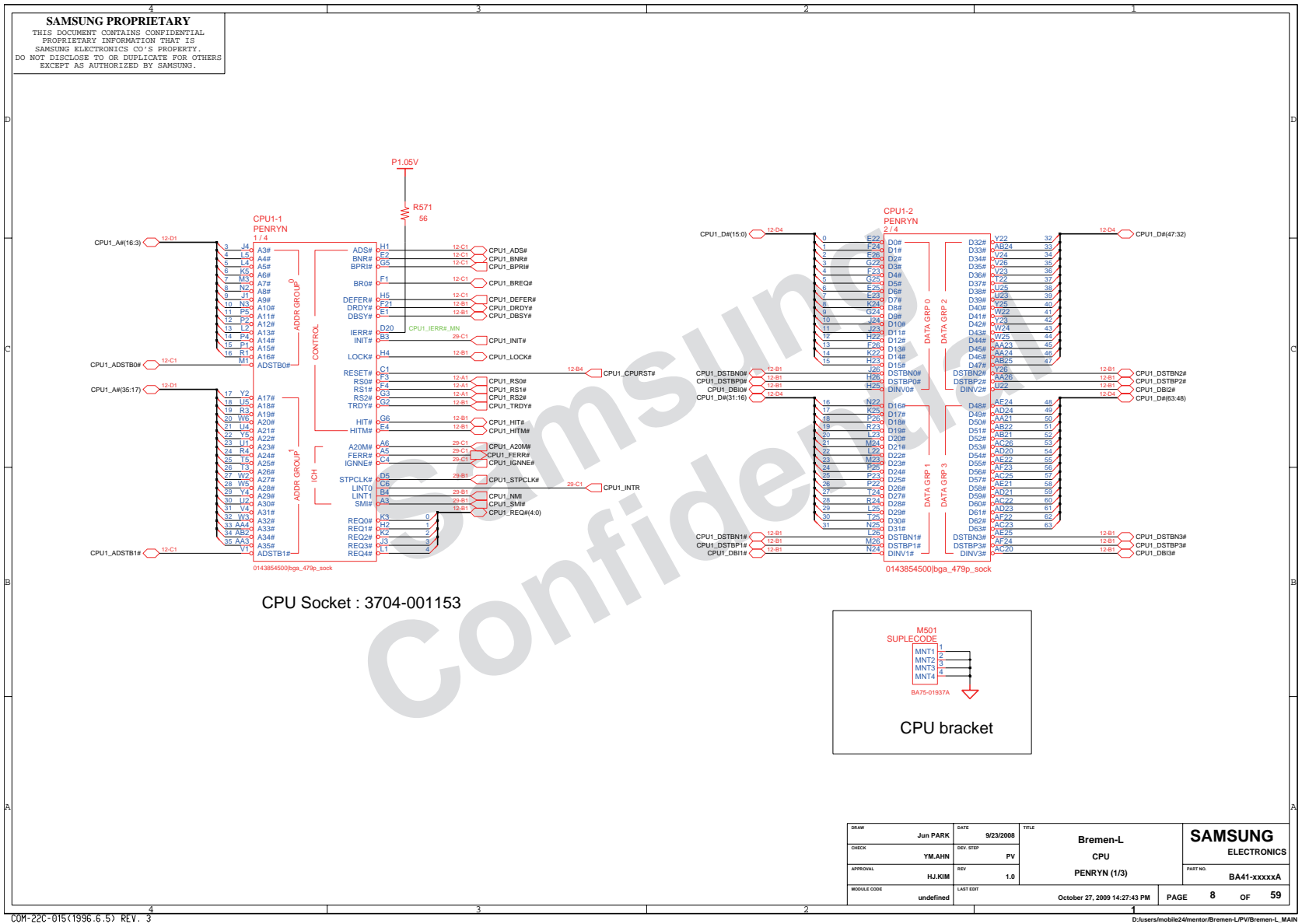
8. Block Diagram and Schematic



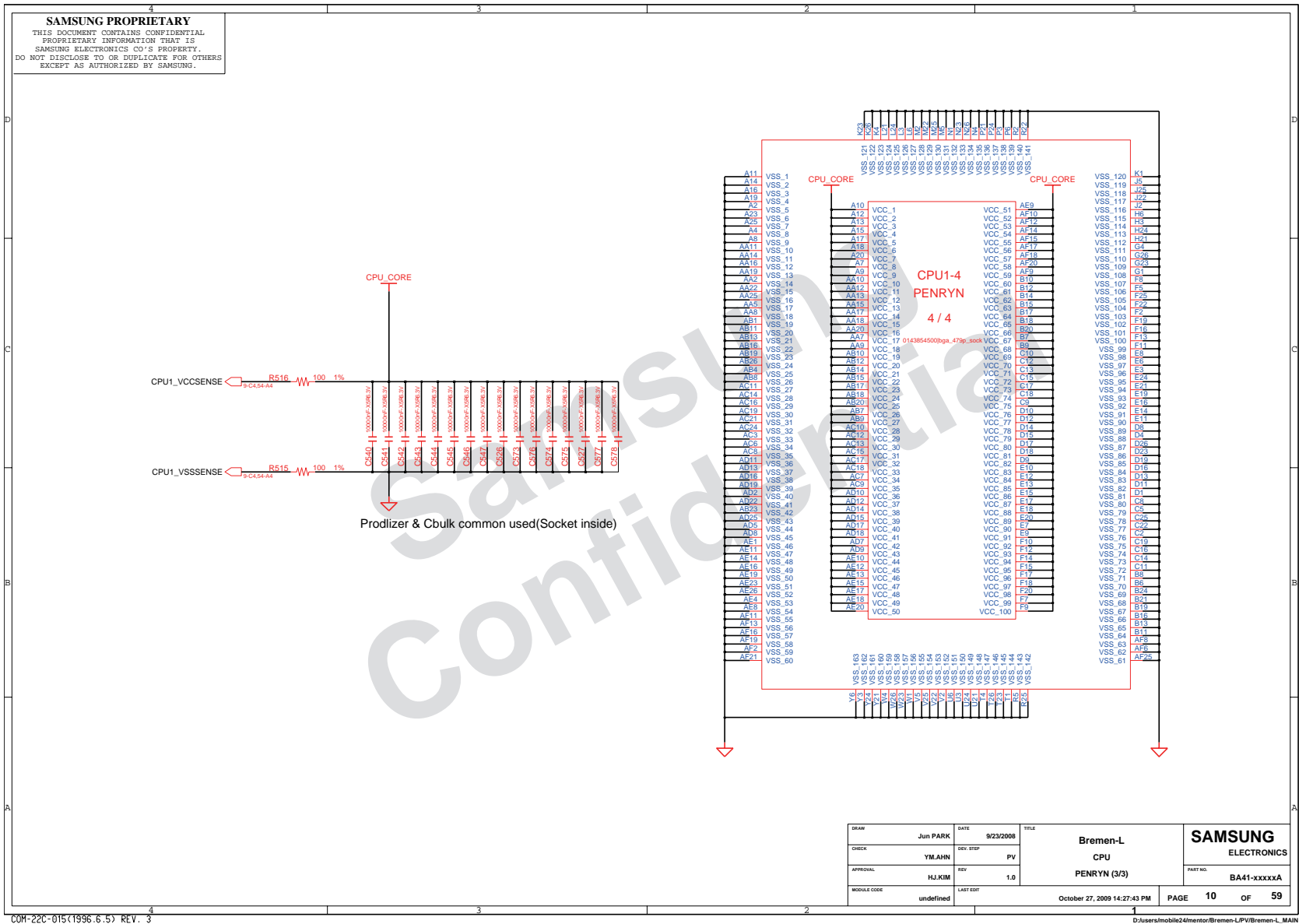
8. Block Diagram and Schematic



8. Block Diagram and Schematic



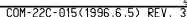
8. Block Diagram and Schematic



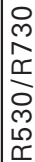
8. Block Diagram and Schematic



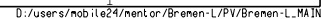
8. Block Diagram and Schematic



D:/users/mobile24/mentor/Bremen-L/PV/Bremen-L MAIN

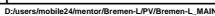


8. Block Diagram and Schematic



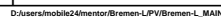


8. Block Diagram and Schematic

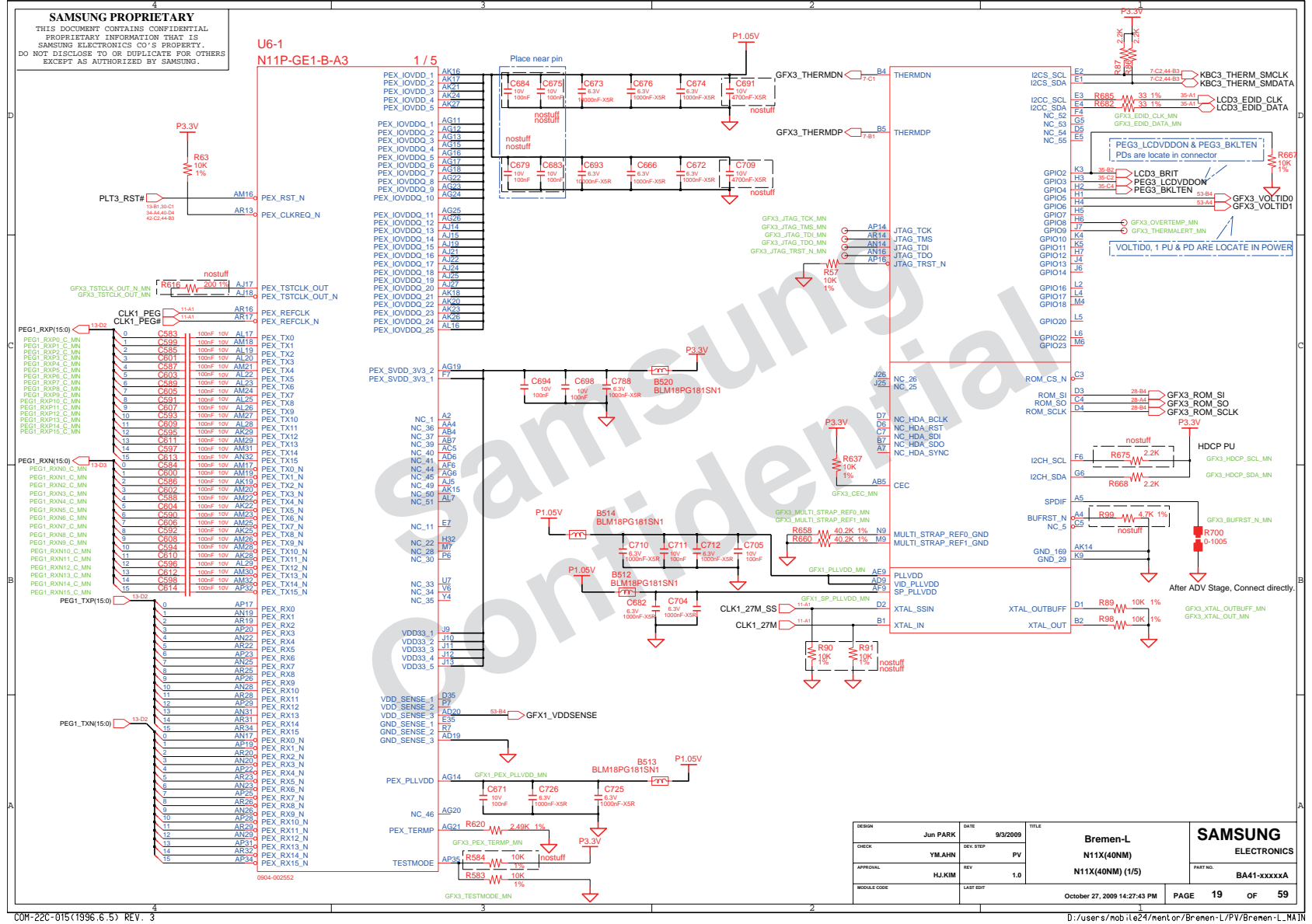




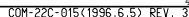
8. Block Diagram and Schematic



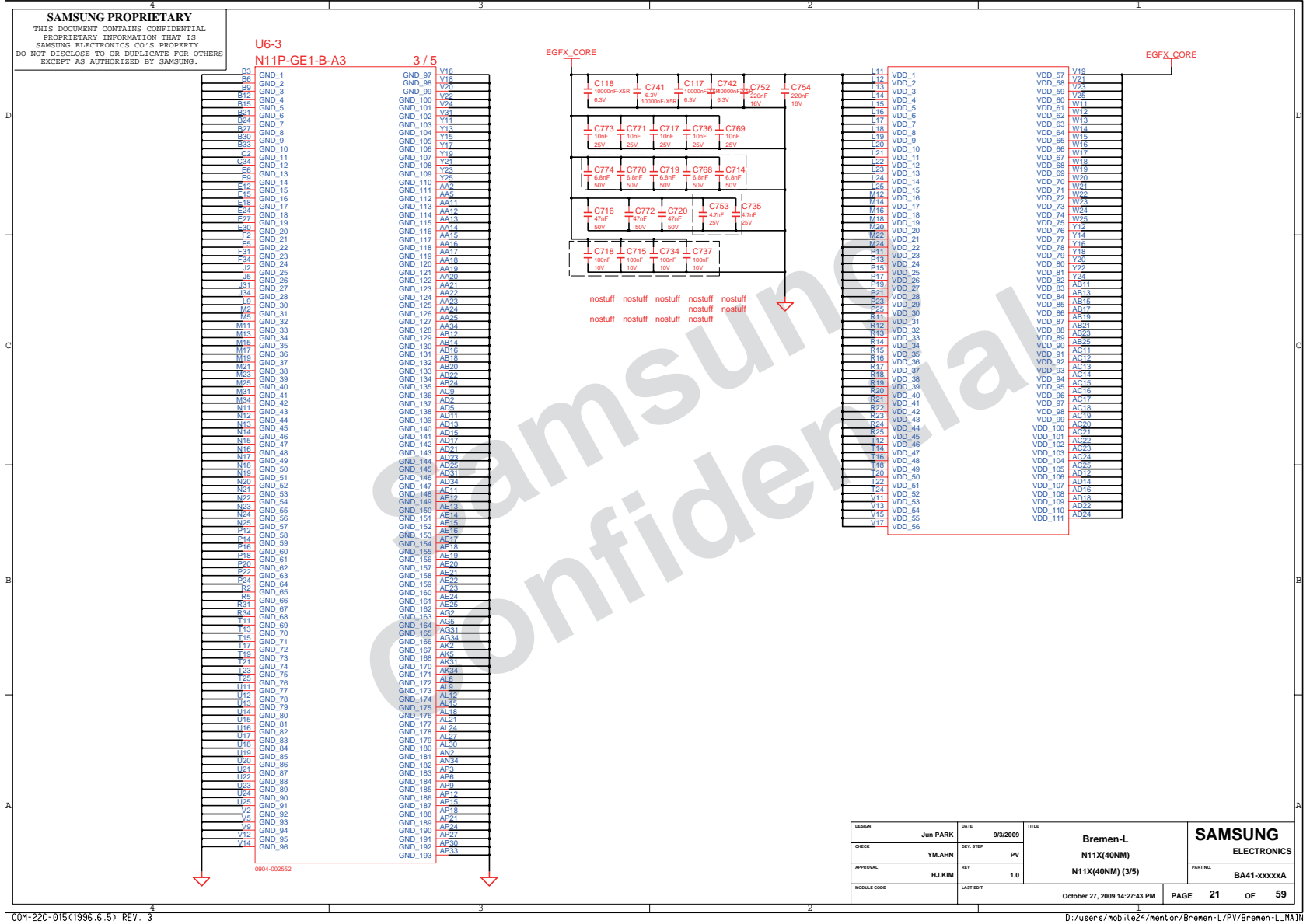
8. Block Diagram and Schematic



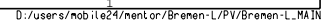
8. Block Diagram and Schematic



8. Block Diagram and Schematic

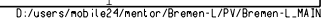


8. Block Diagram and Schematic

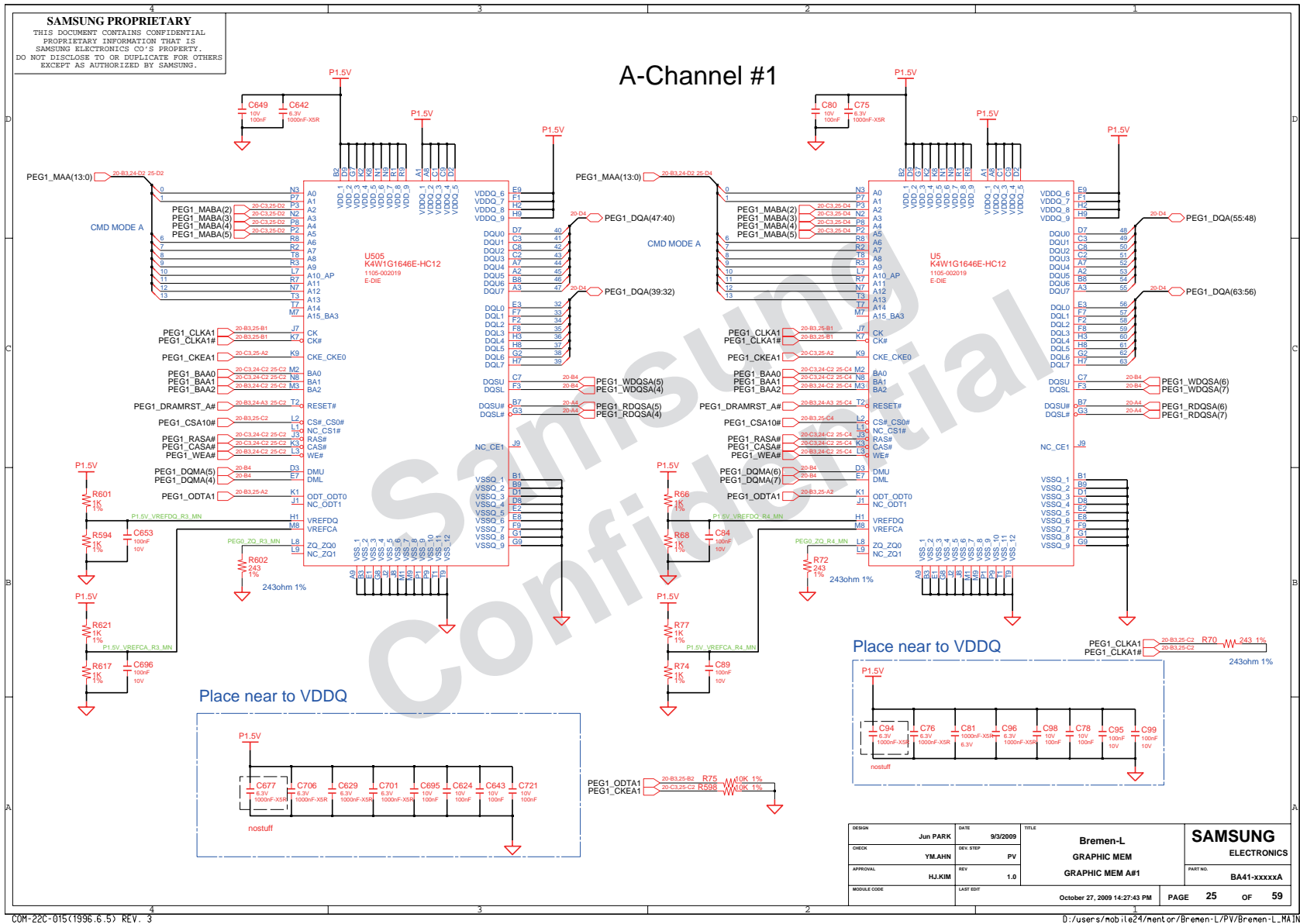




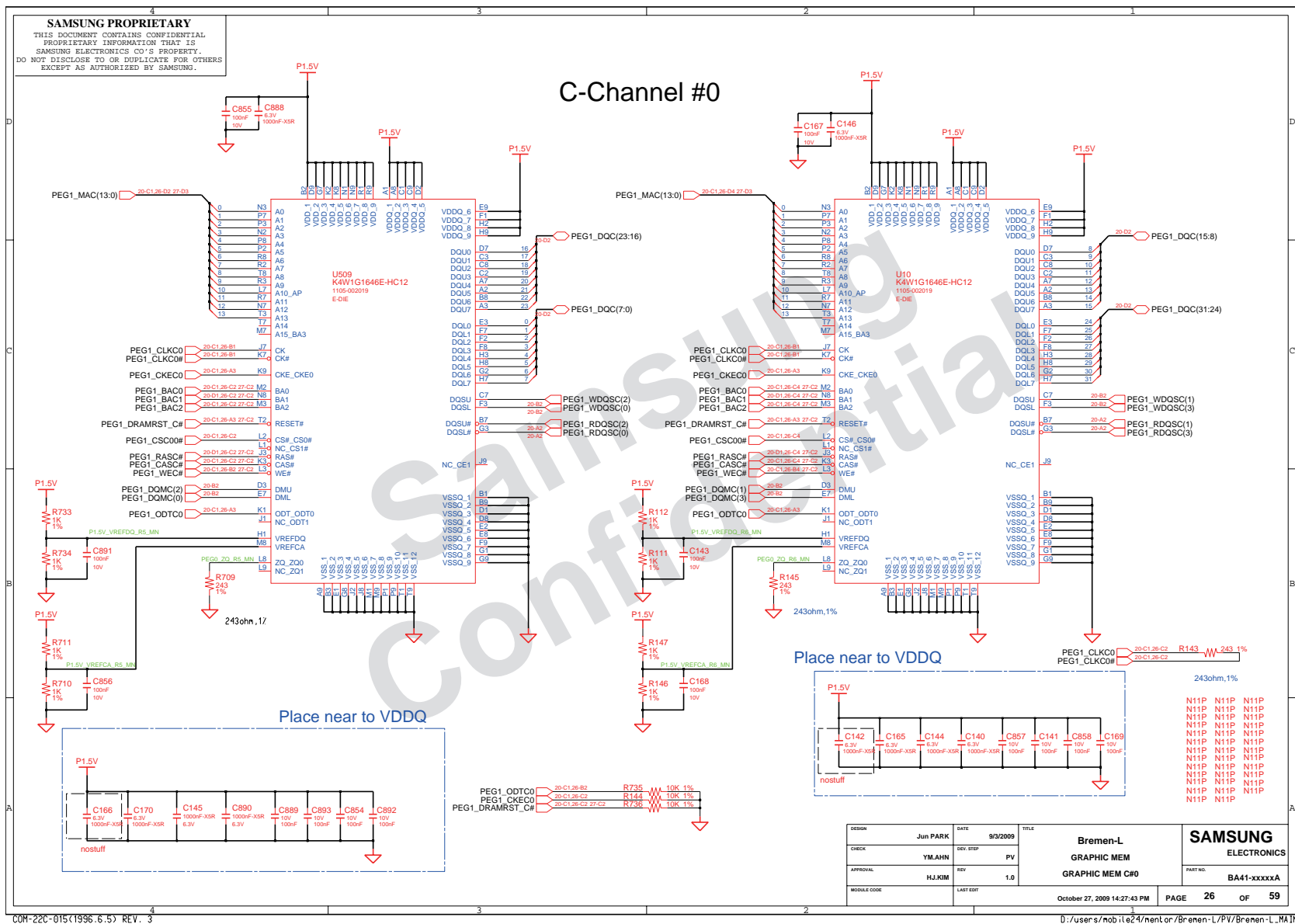
8. Block Diagram and Schematic



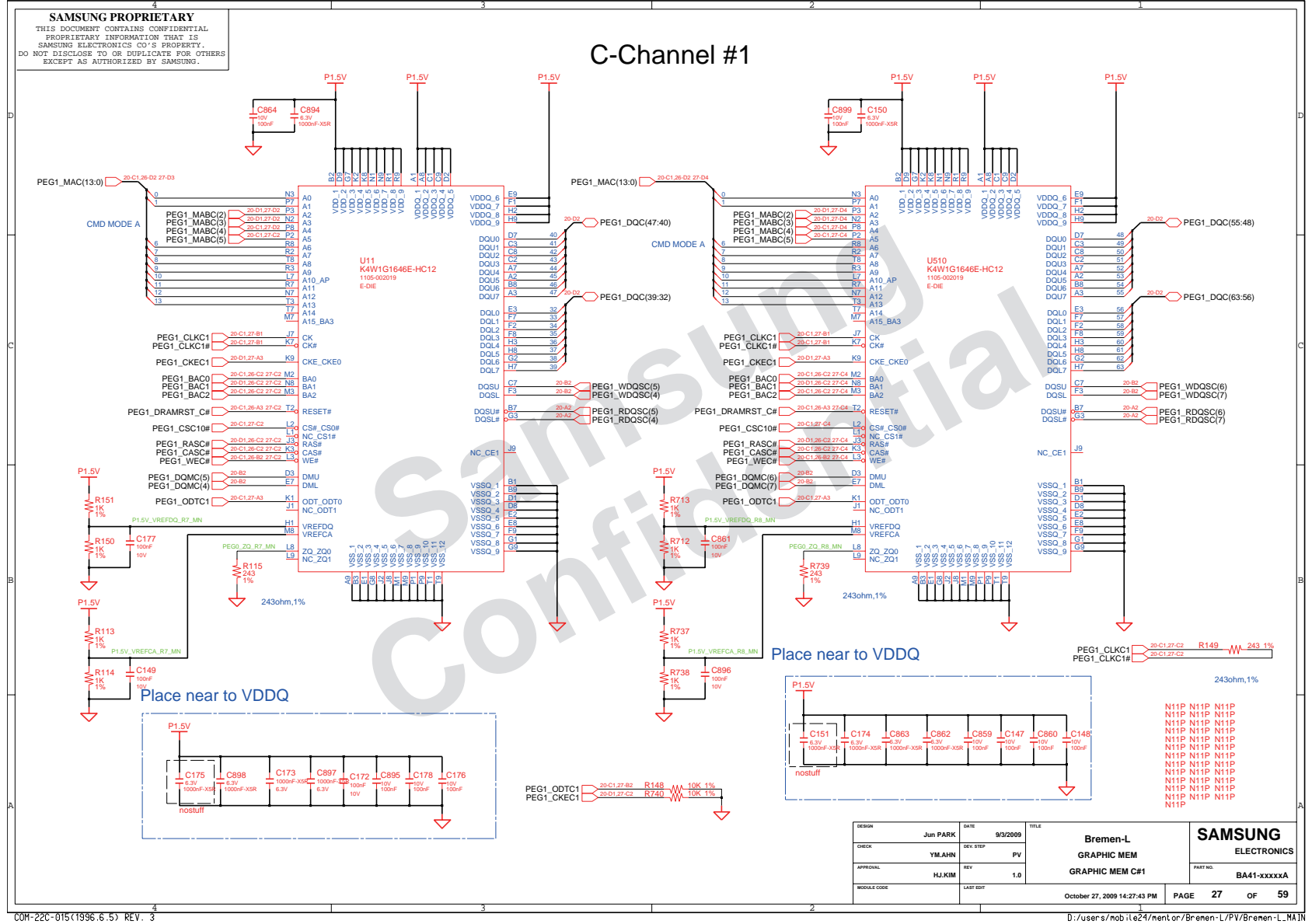
8. Block Diagram and Schematic



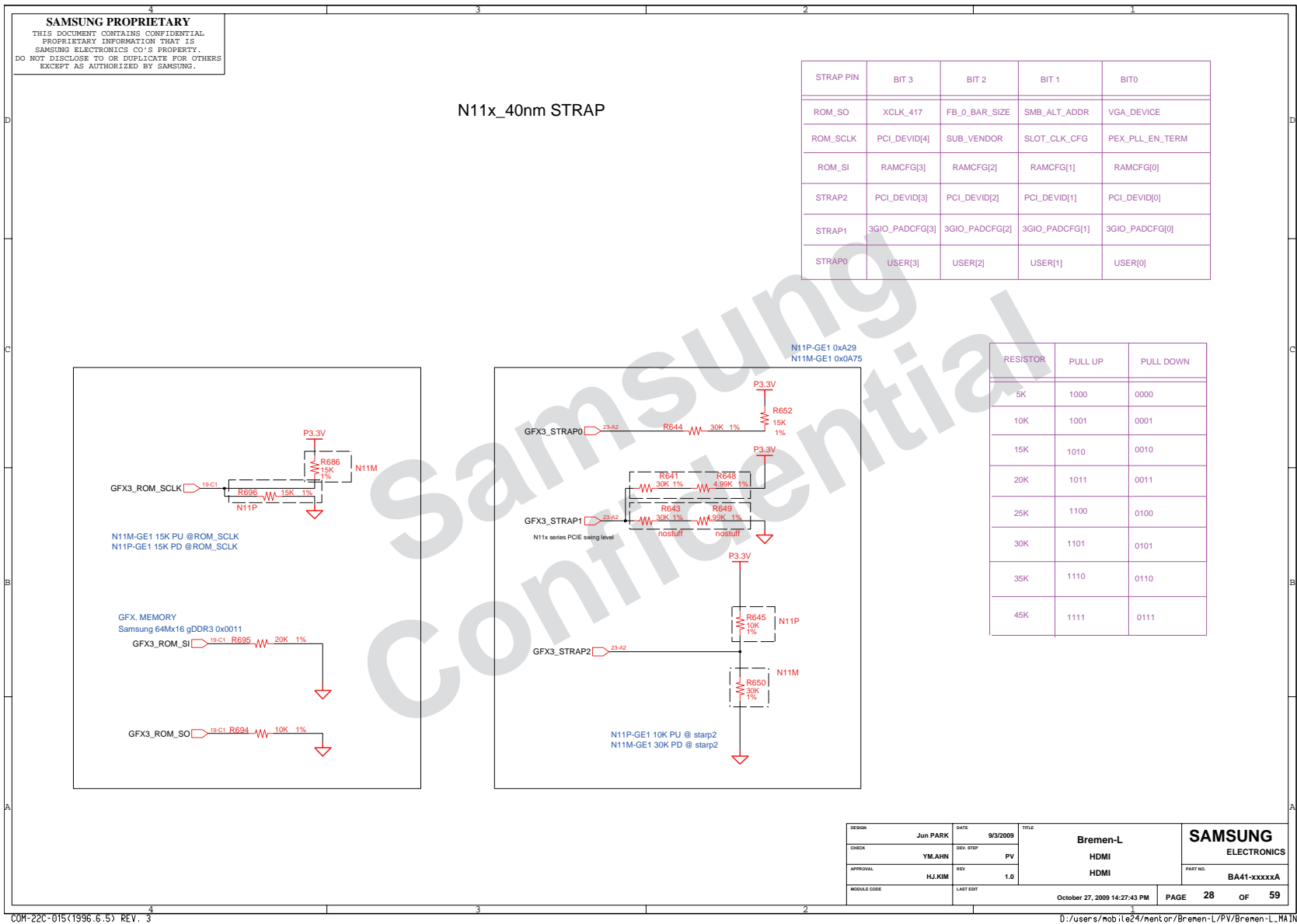
8. Block Diagram and Schematic

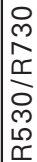


8. Block Diagram and Schematic

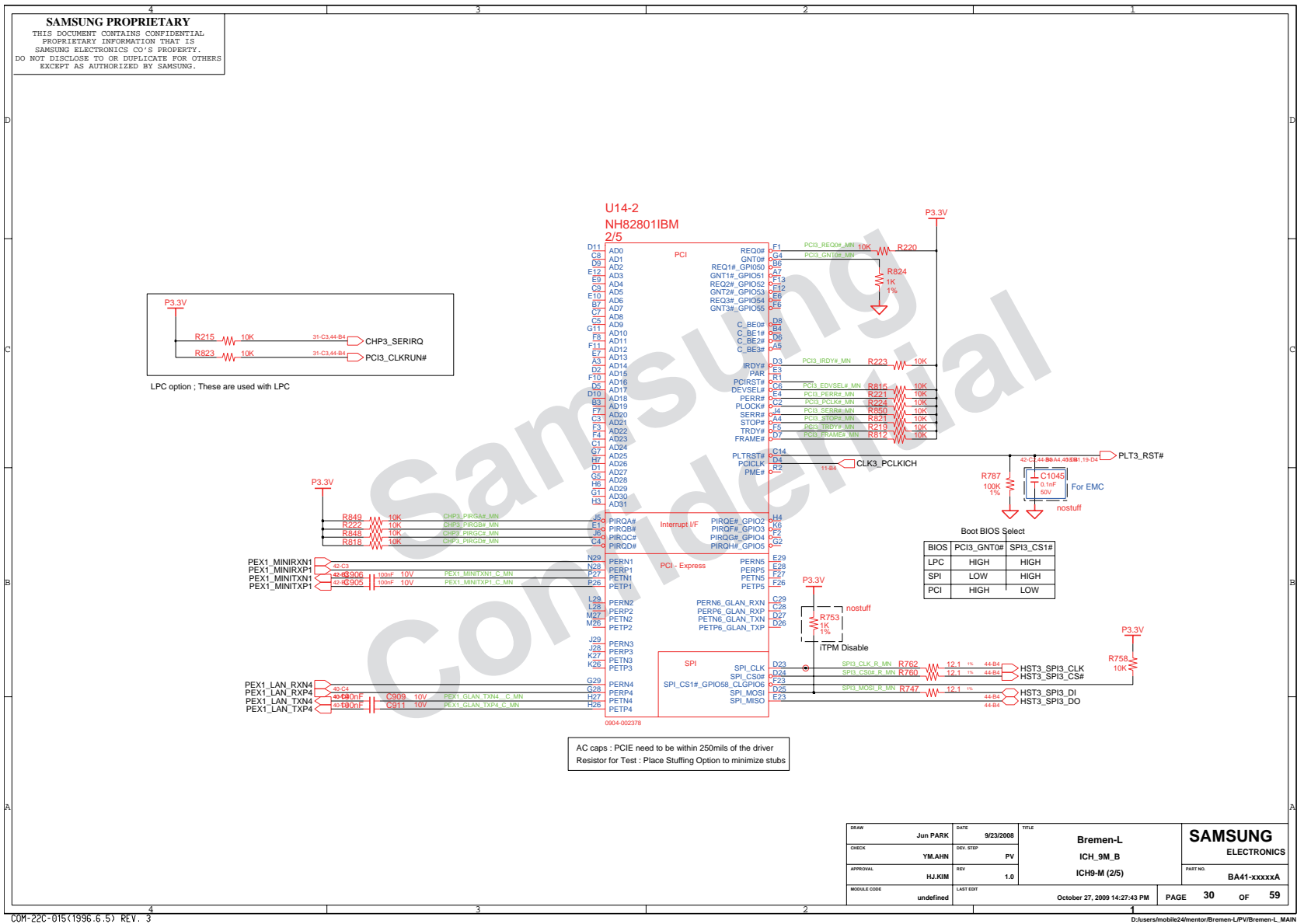


8. Block Diagram and Schematic



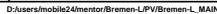


8. Block Diagram and Schematic

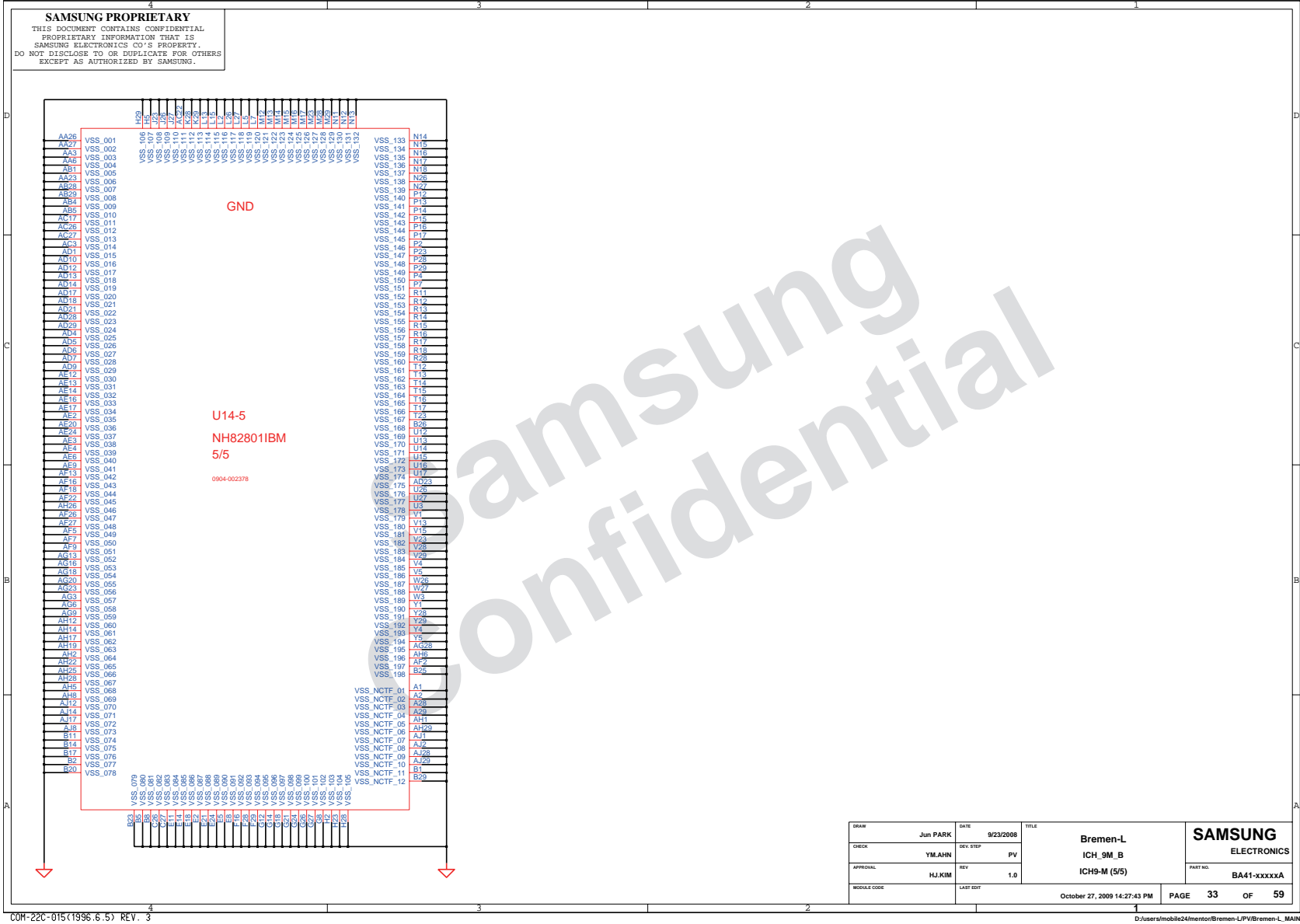




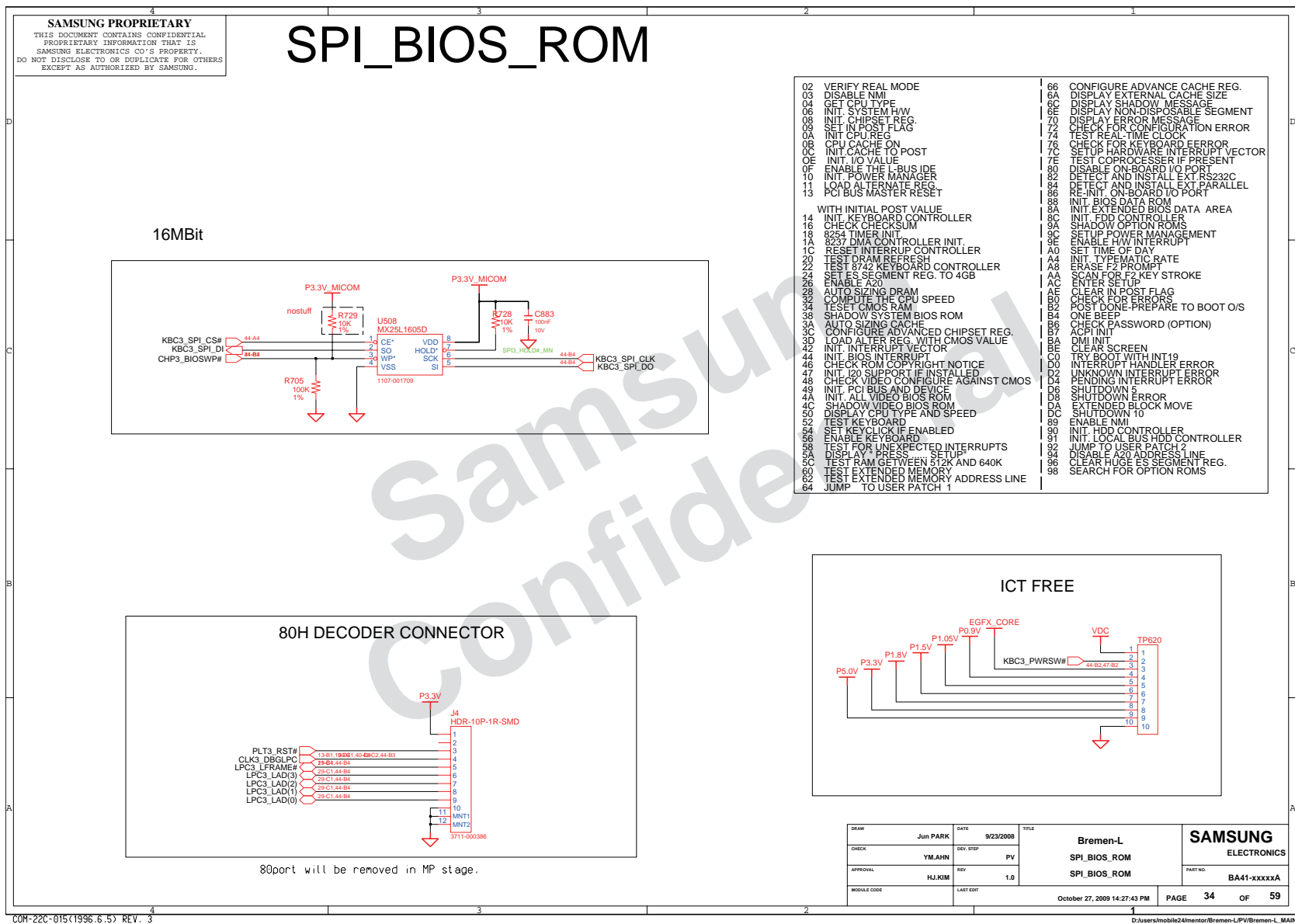
8. Block Diagram and Schematic



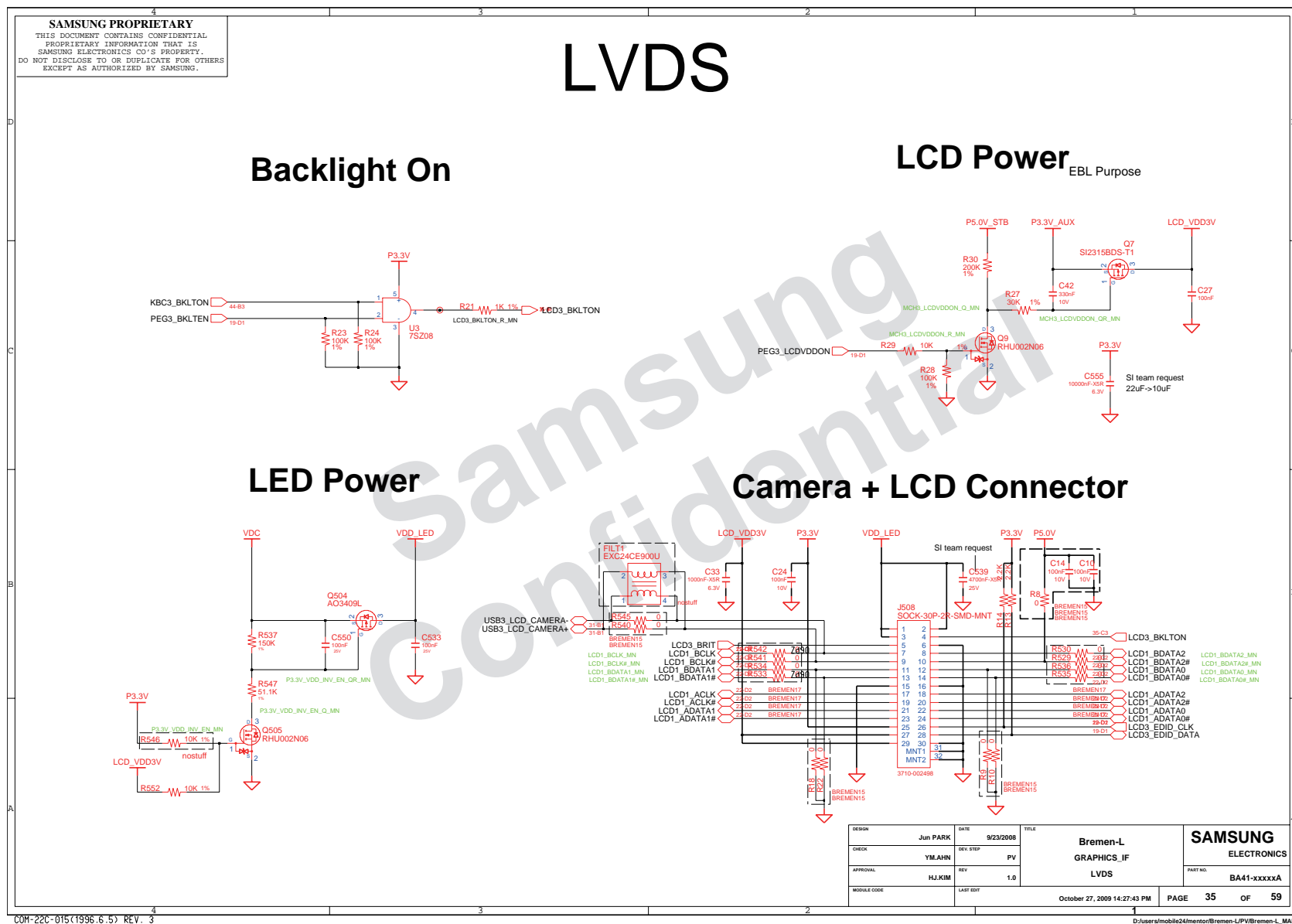
8. Block Diagram and Schematic



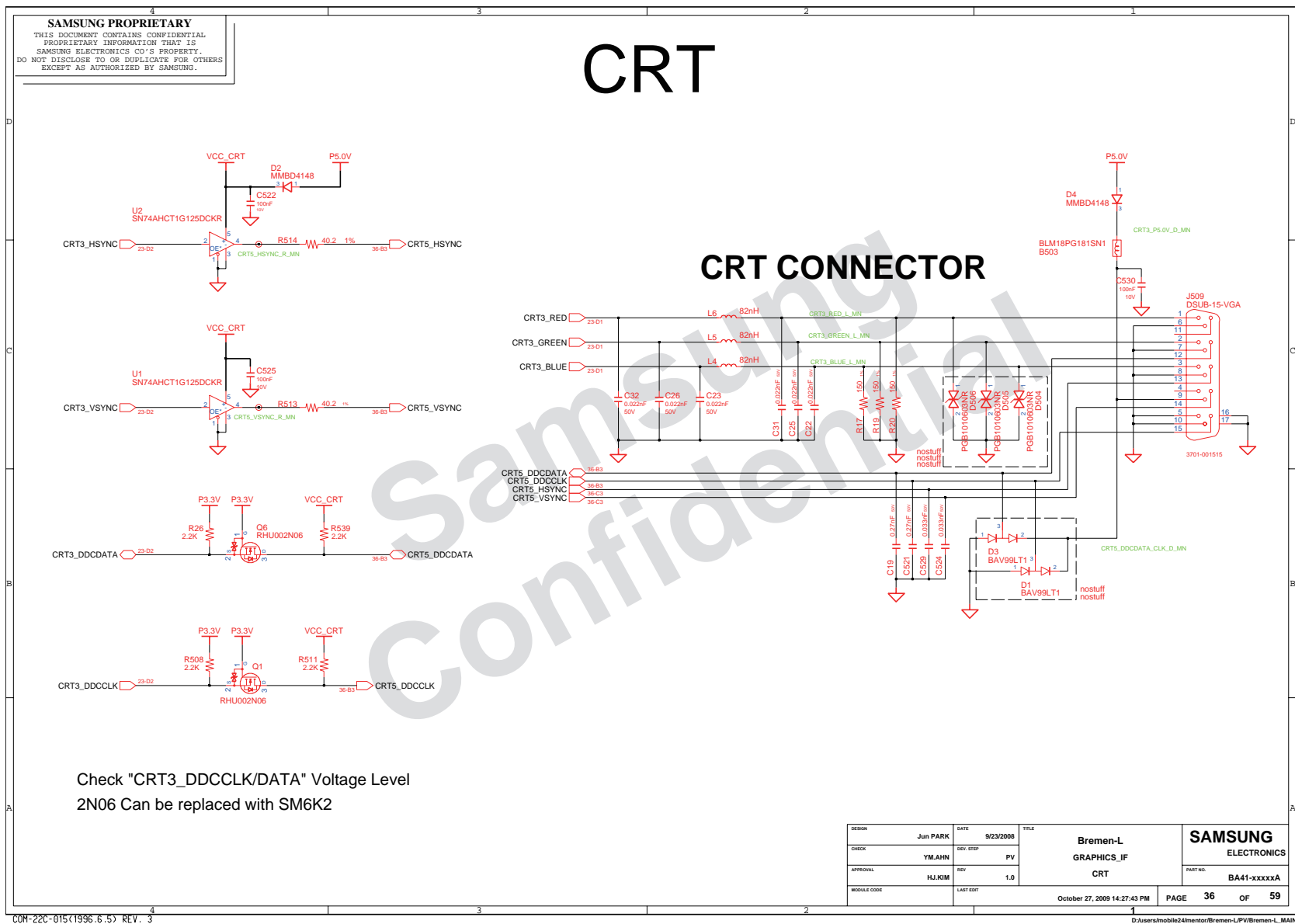
8. Block Diagram and Schematic



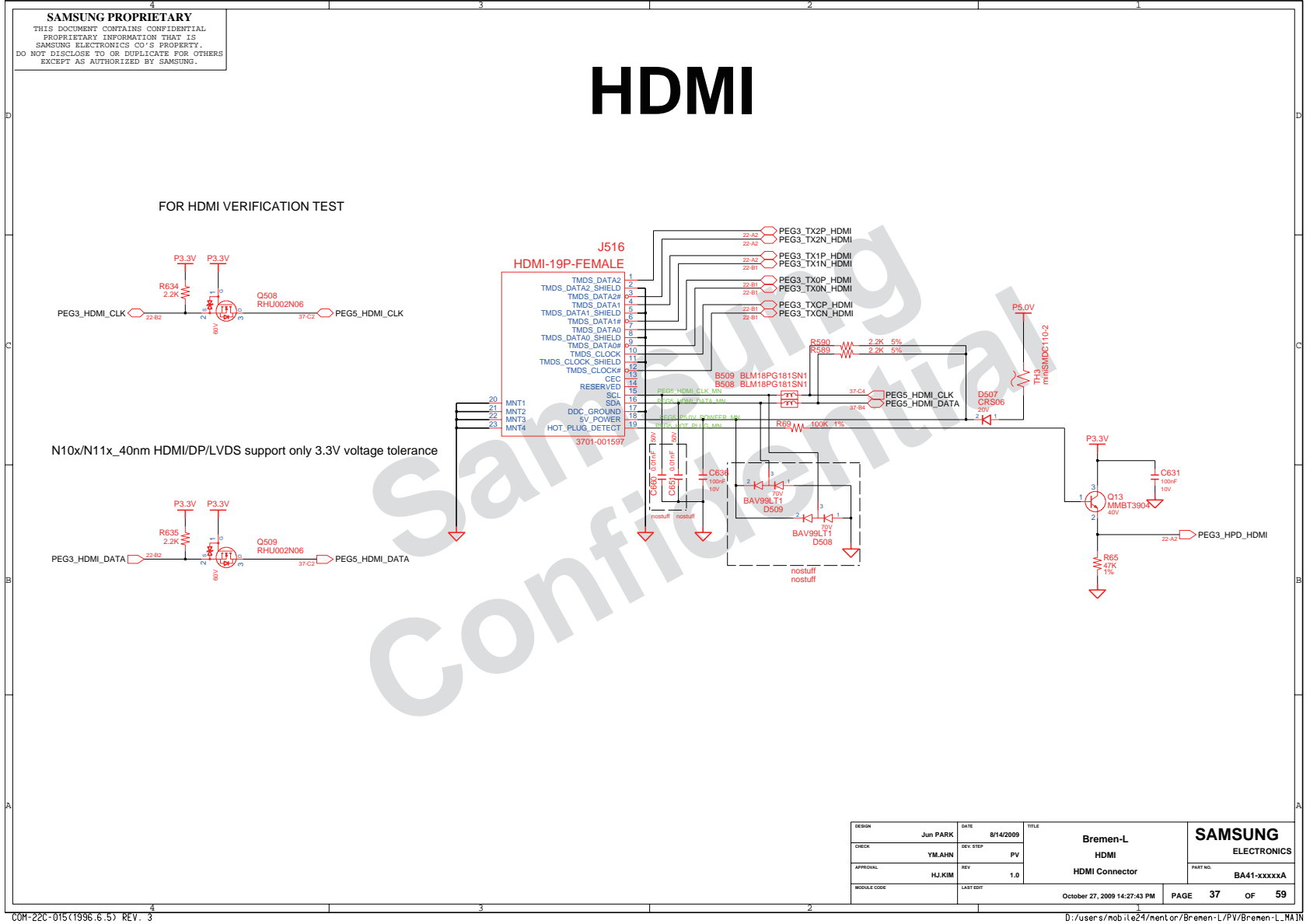
8. Block Diagram and Schematic



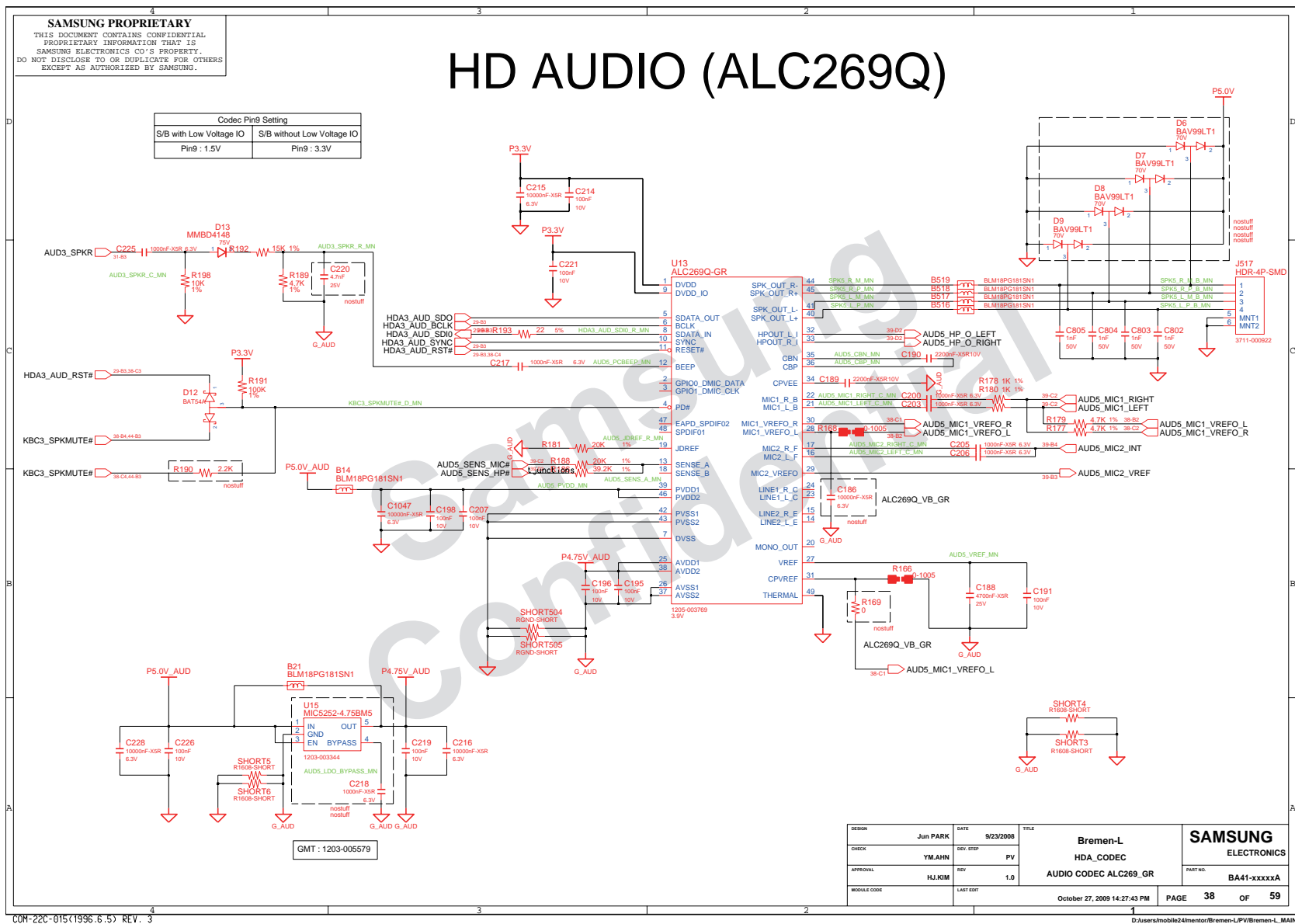
8. Block Diagram and Schematic



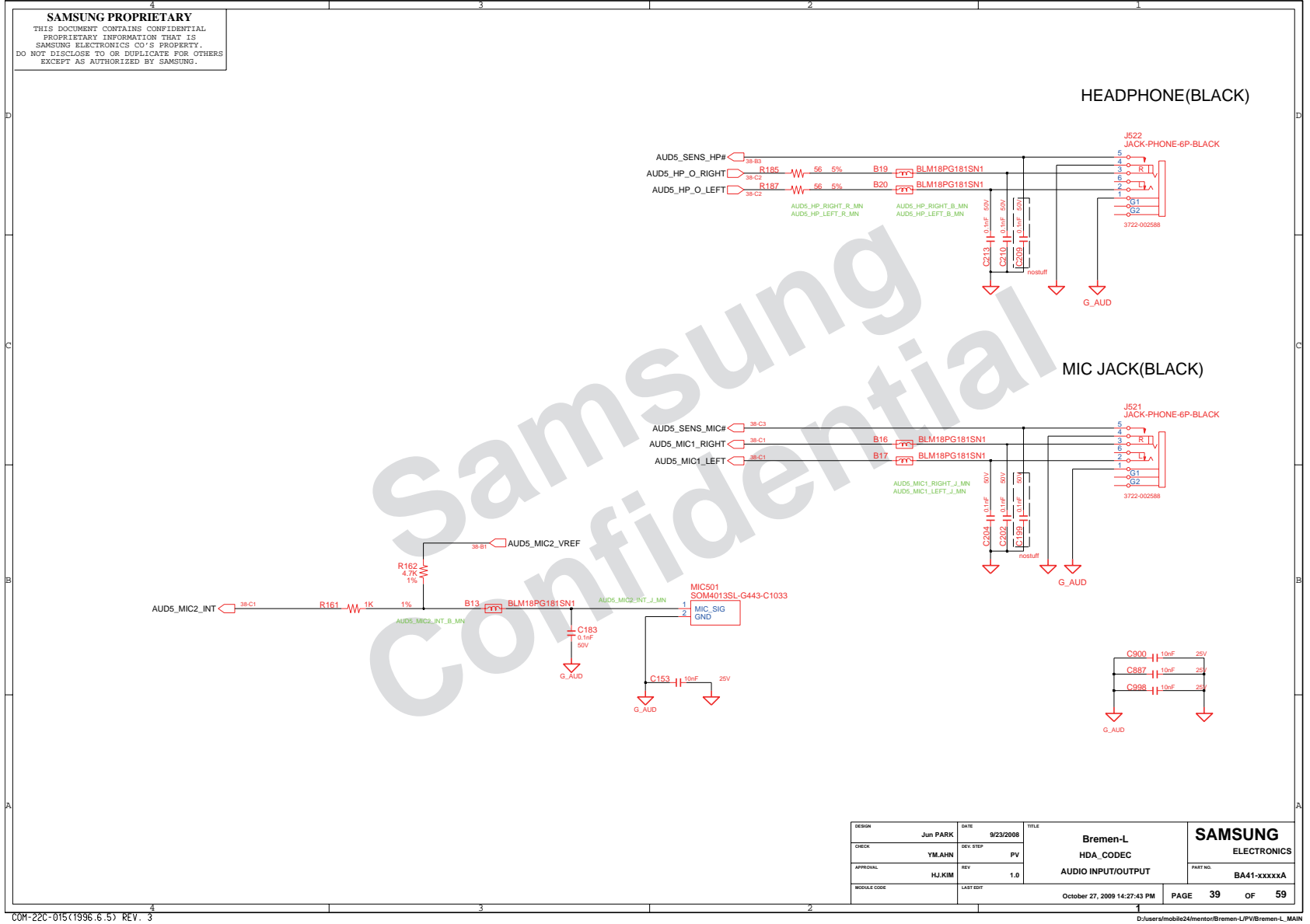
8. Block Diagram and Schematic



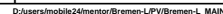
8. Block Diagram and Schematic



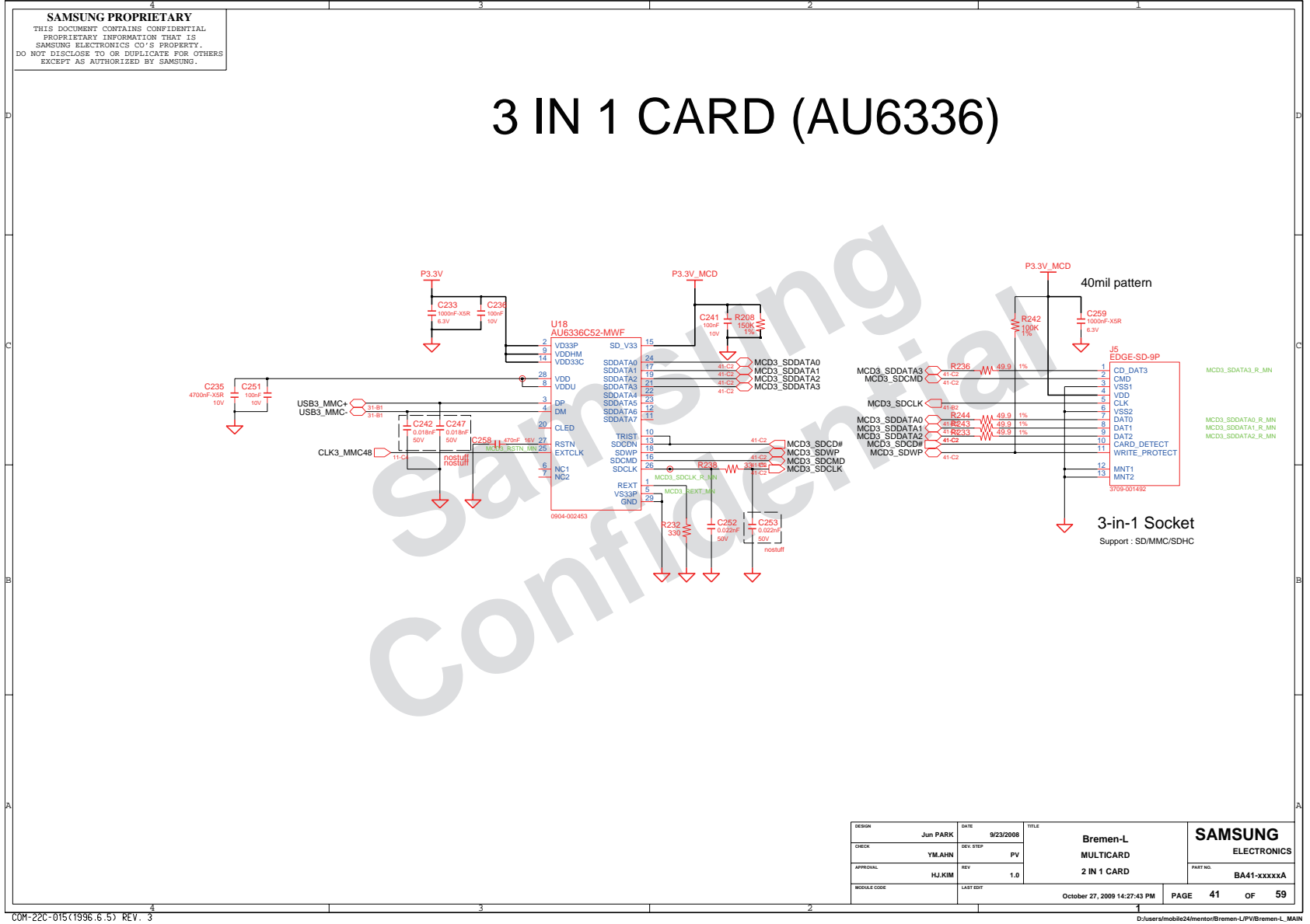
8. Block Diagram and Schematic



8. Block Diagram and Schematic



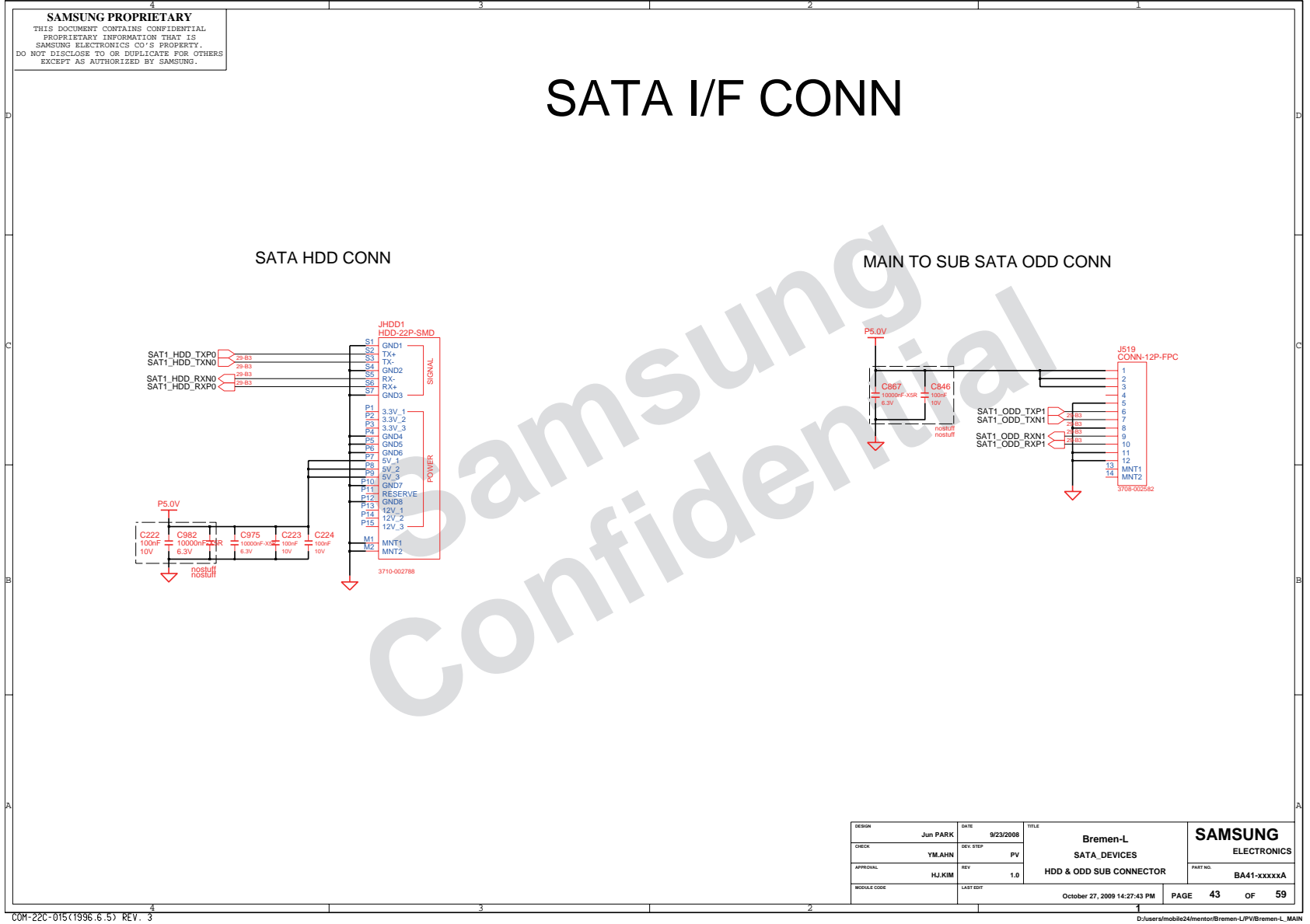
8. Block Diagram and Schematic



8. Block Diagram and Schematic



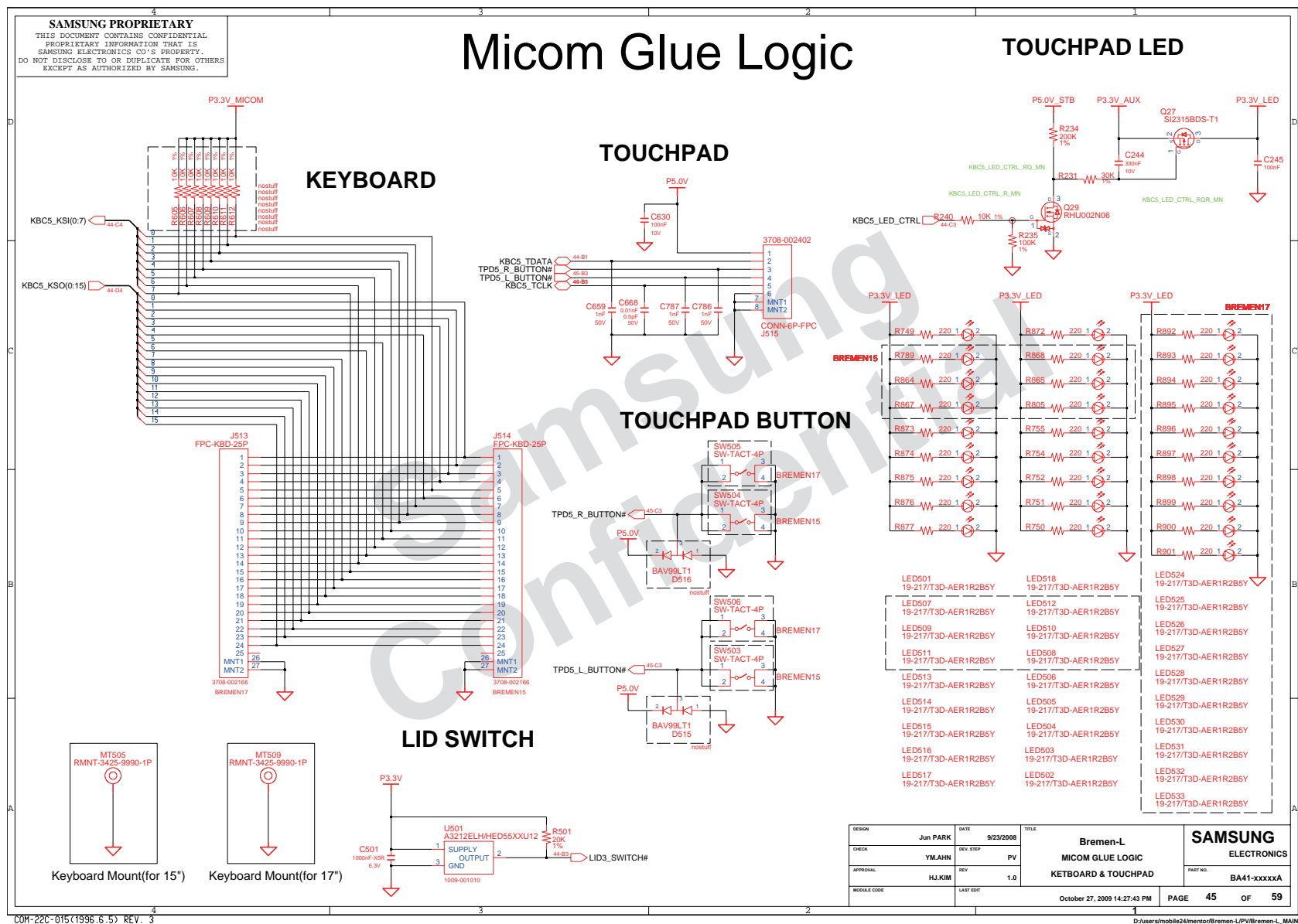
8. Block Diagram and Schematic



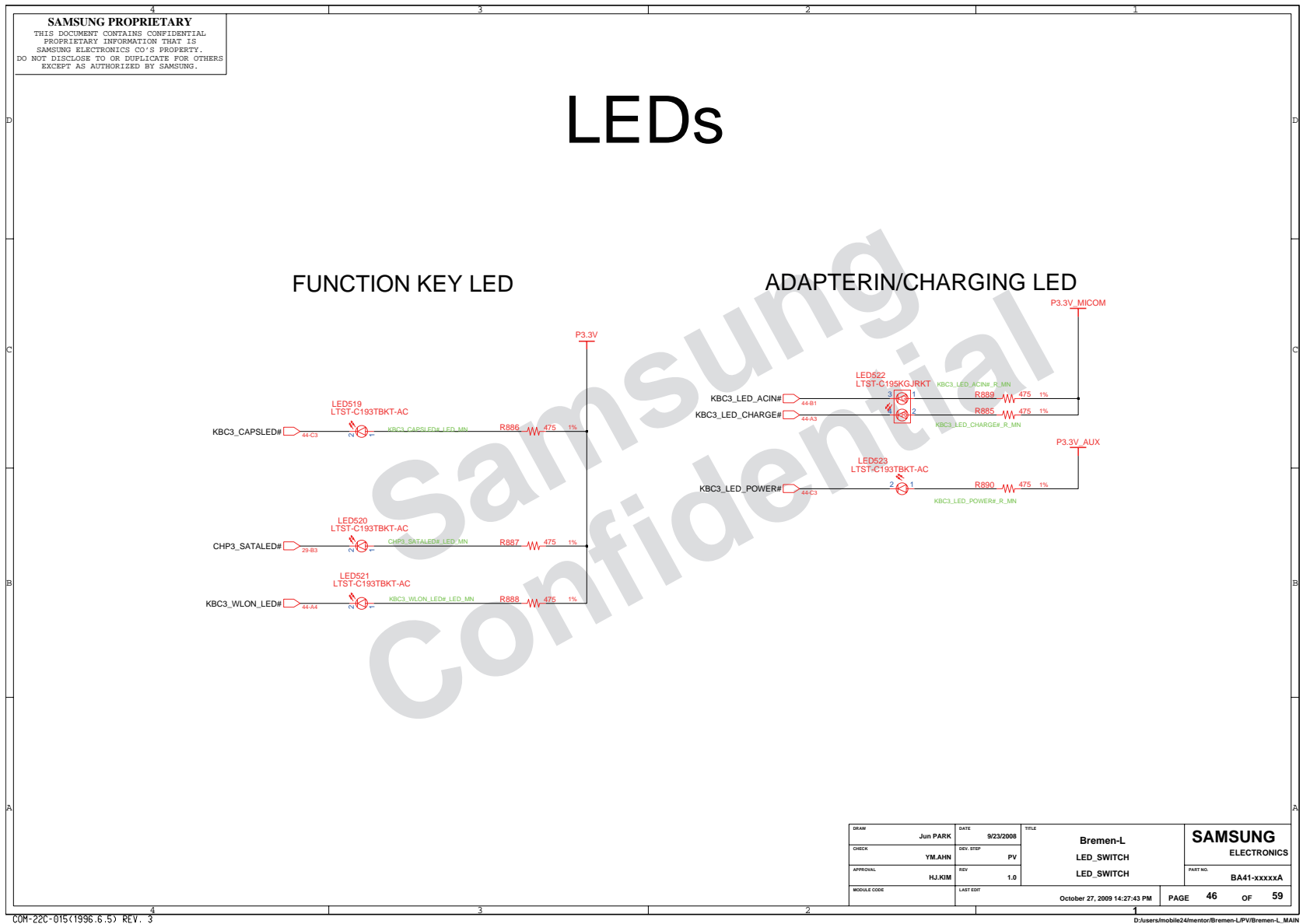
8. Block Diagram and Schematic



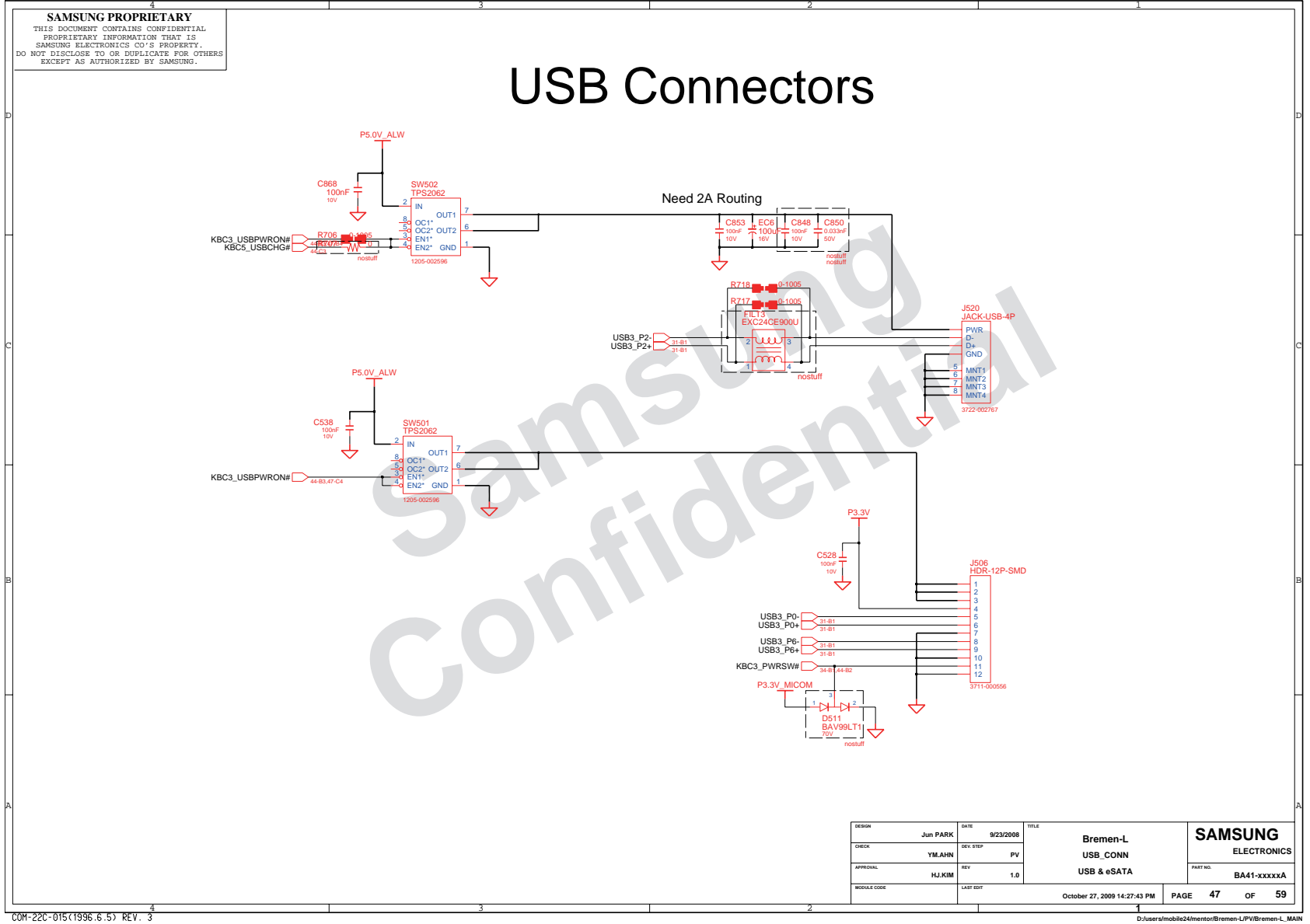
8. Block Diagram and Schematic



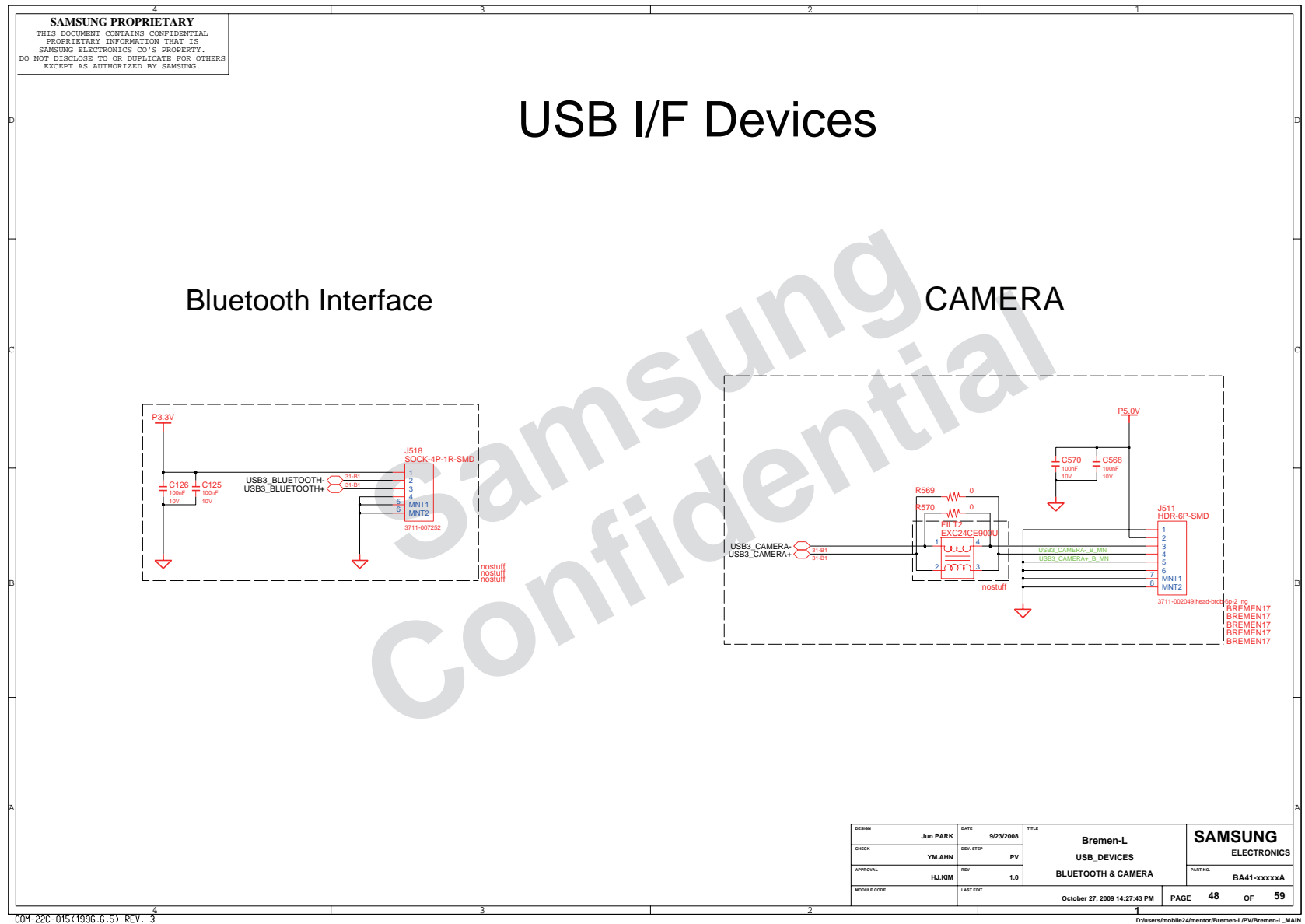
8. Block Diagram and Schematic



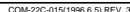
8. Block Diagram and Schematic



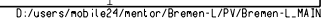
8. Block Diagram and Schematic



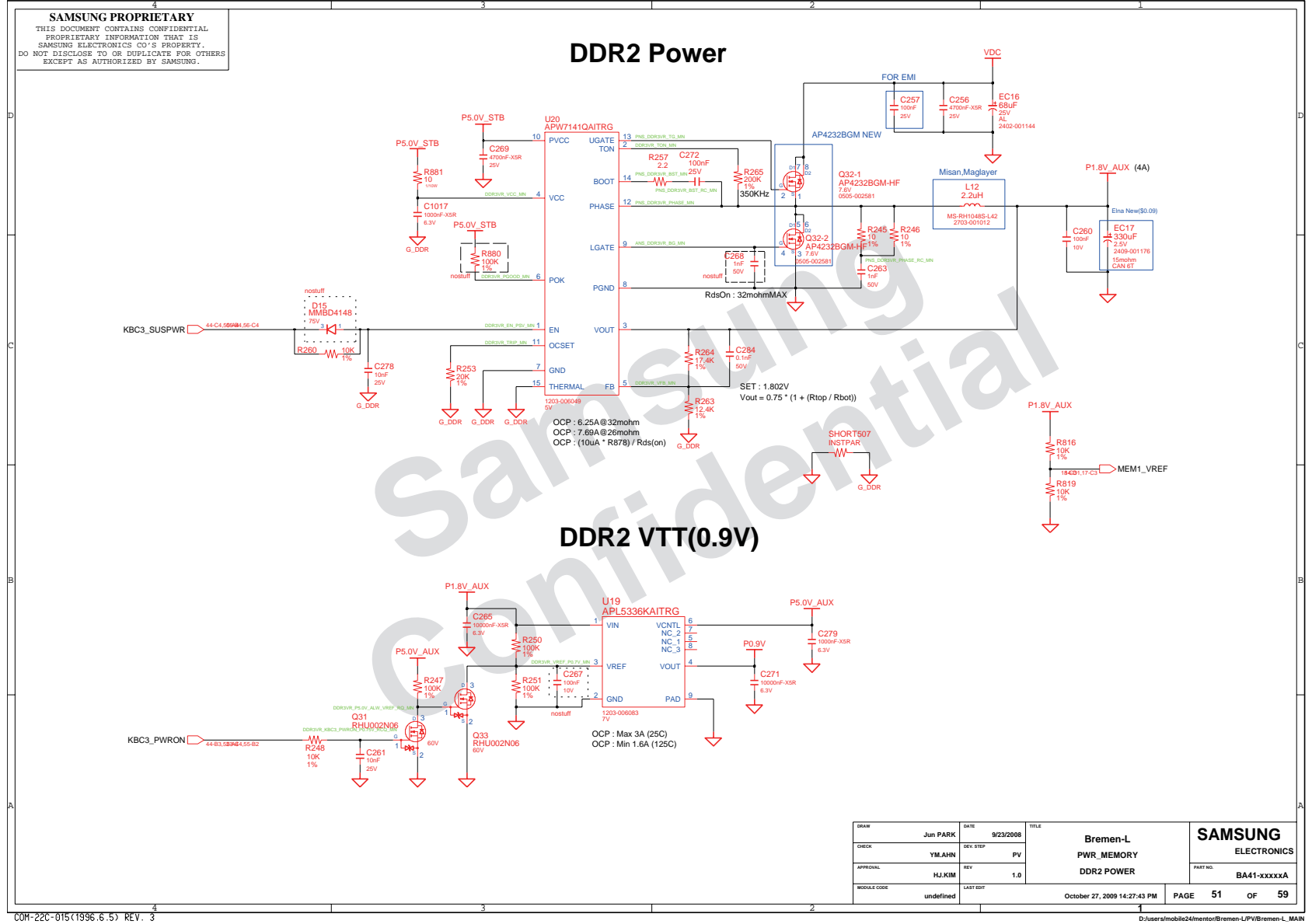
8. Block Diagram and Schematic



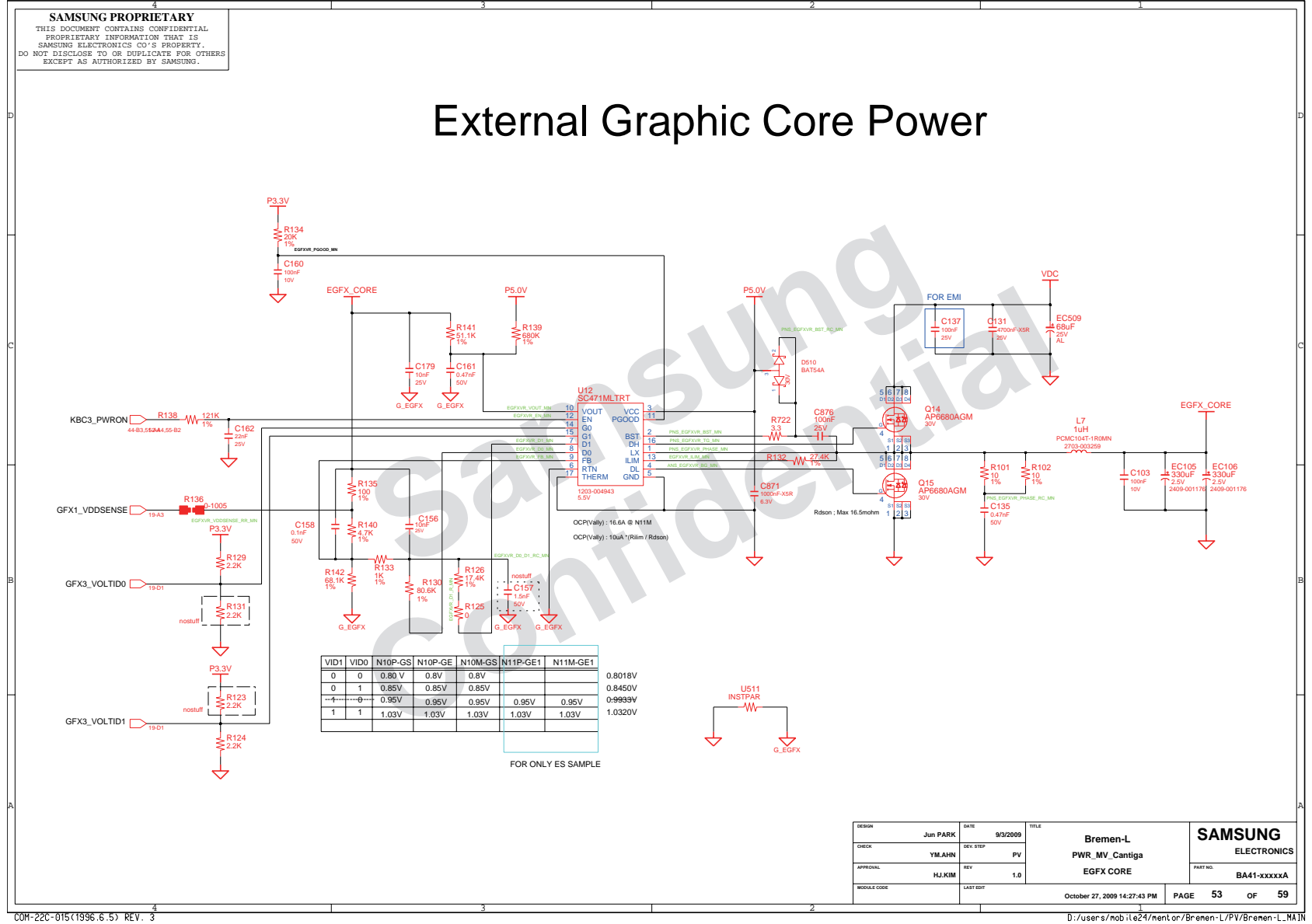
8. Block Diagram and Schematic



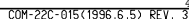
8. Block Diagram and Schematic



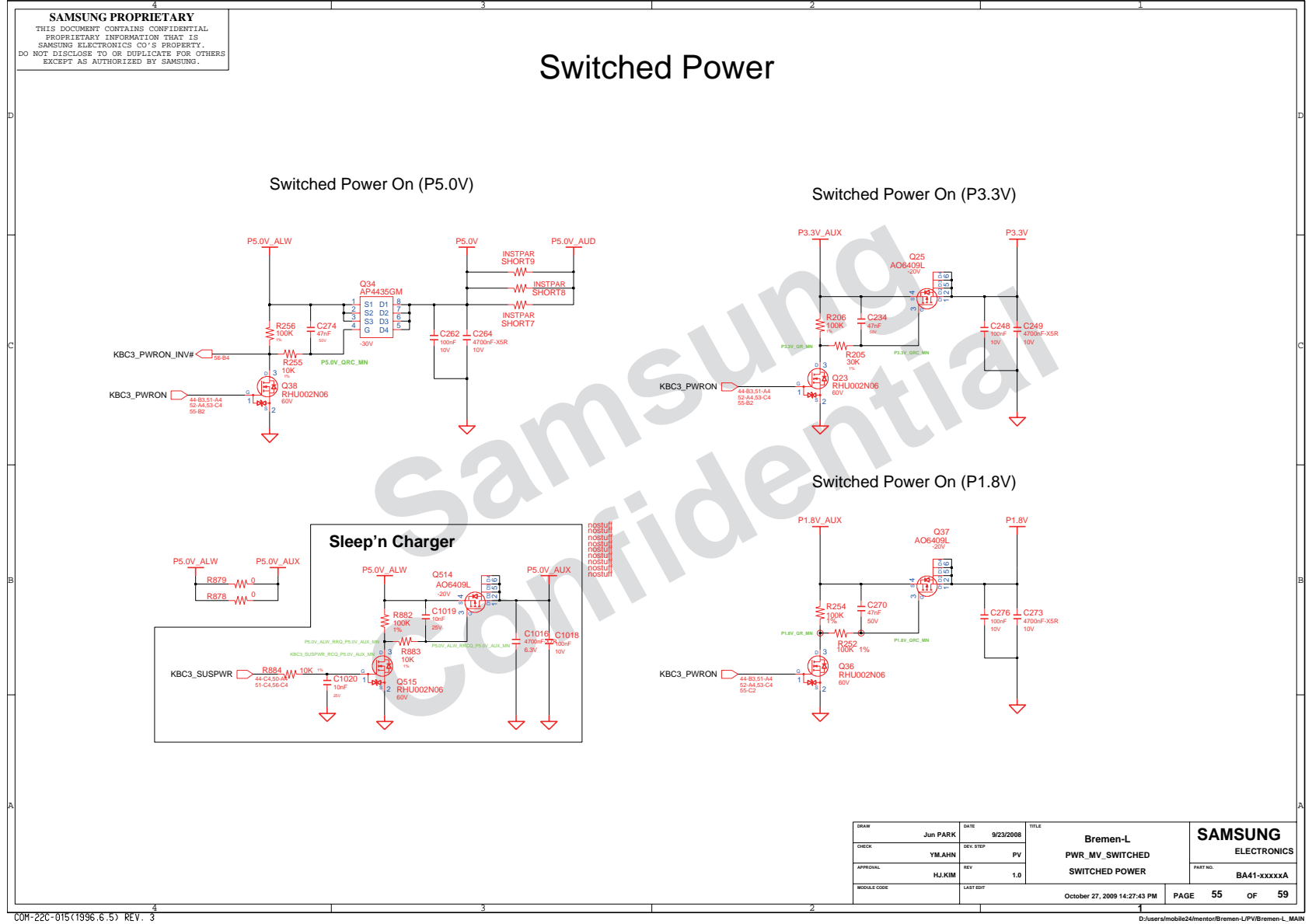
8. Block Diagram and Schematic



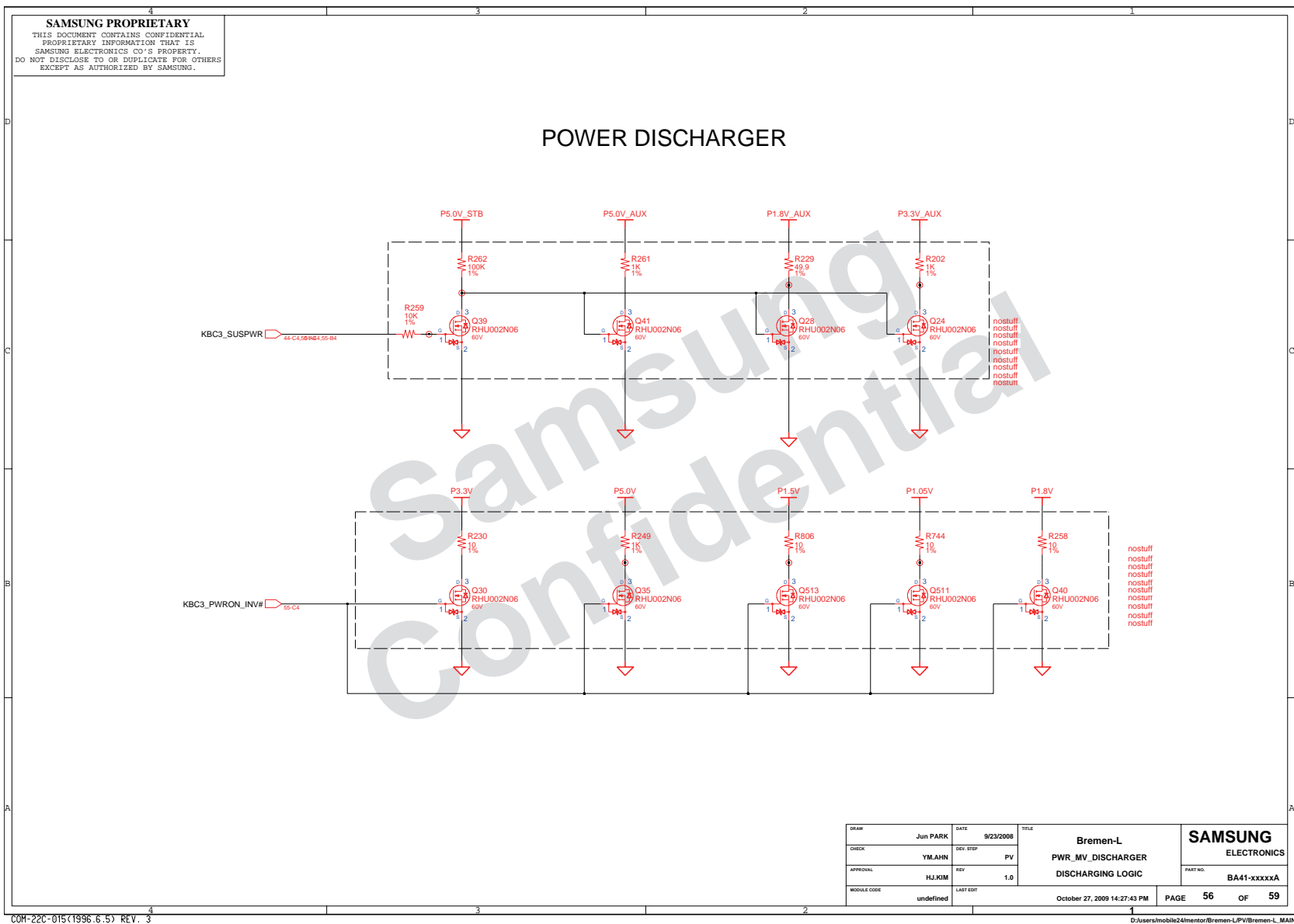
8. Block Diagram and Schematic



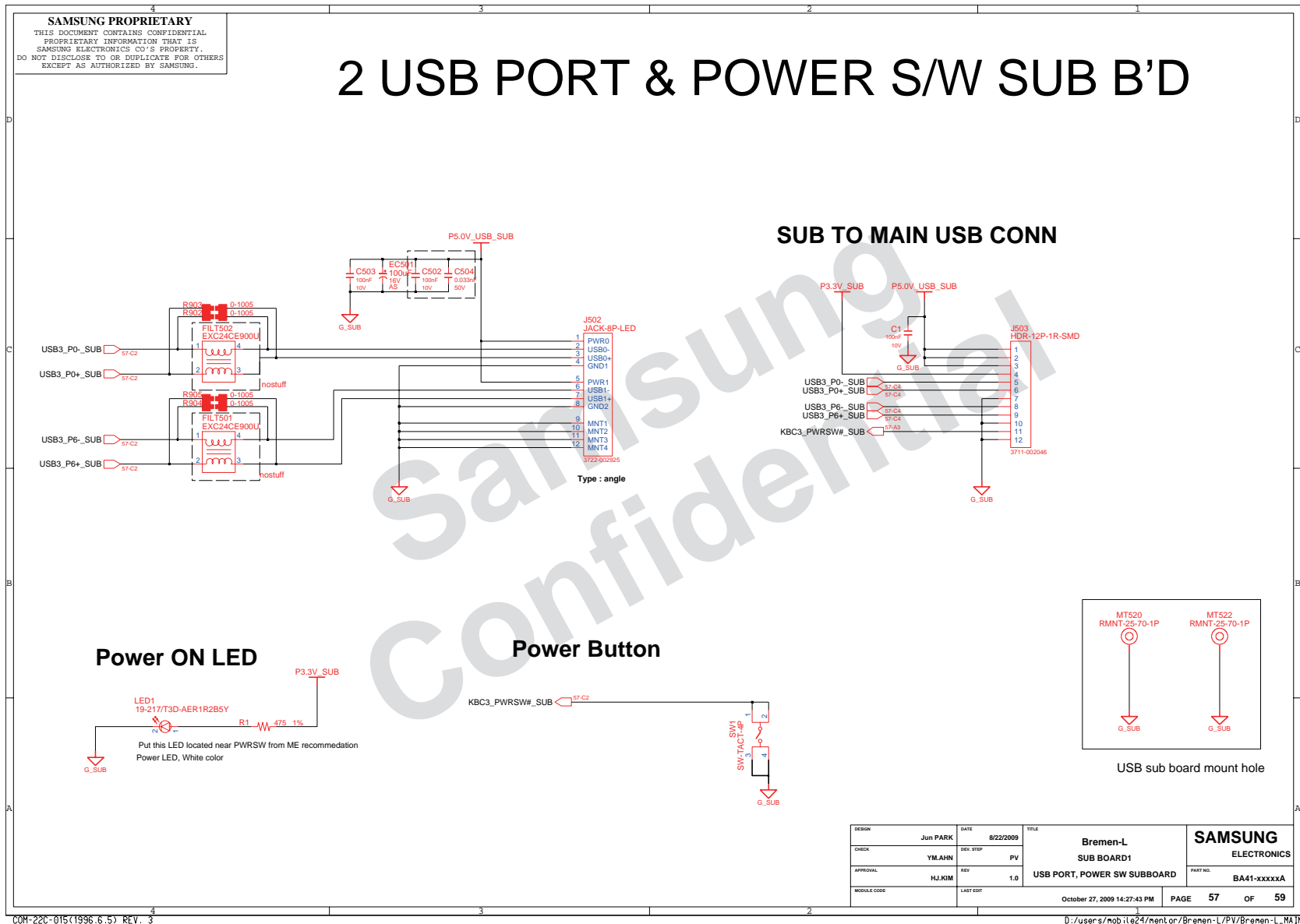
8. Block Diagram and Schematic



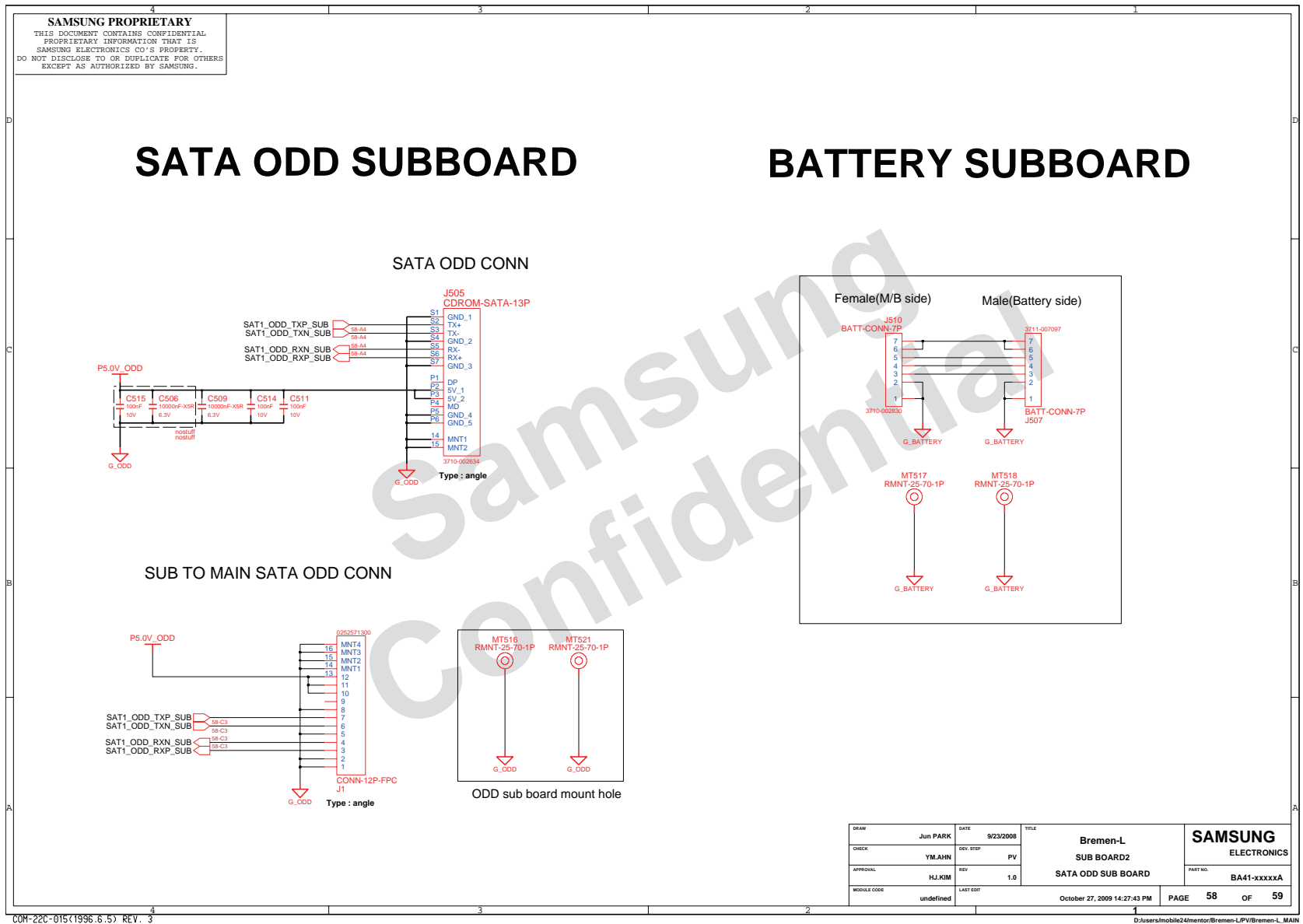
8. Block Diagram and Schematic



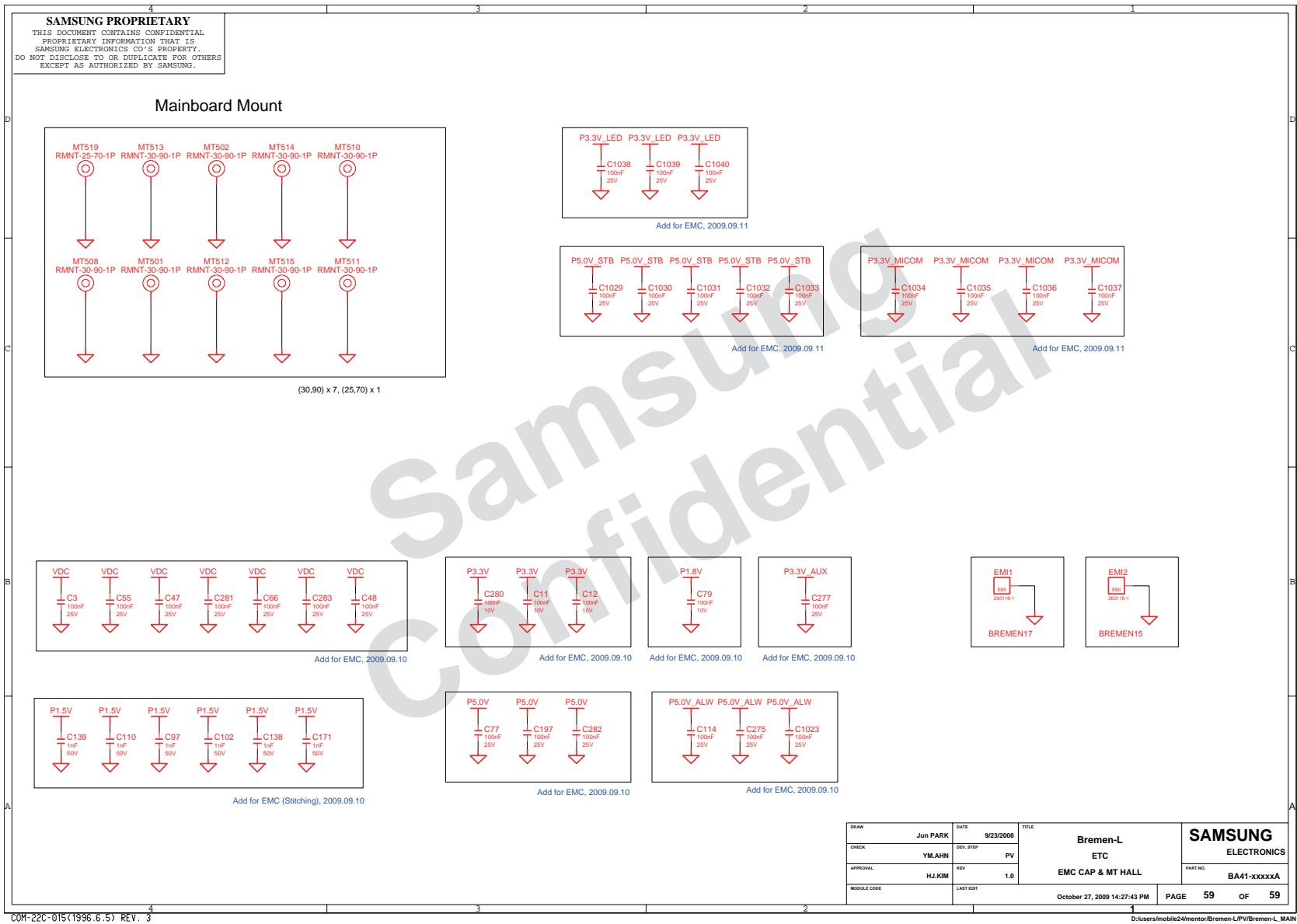
8. Block Diagram and Schematic



8. Block Diagram and Schematic



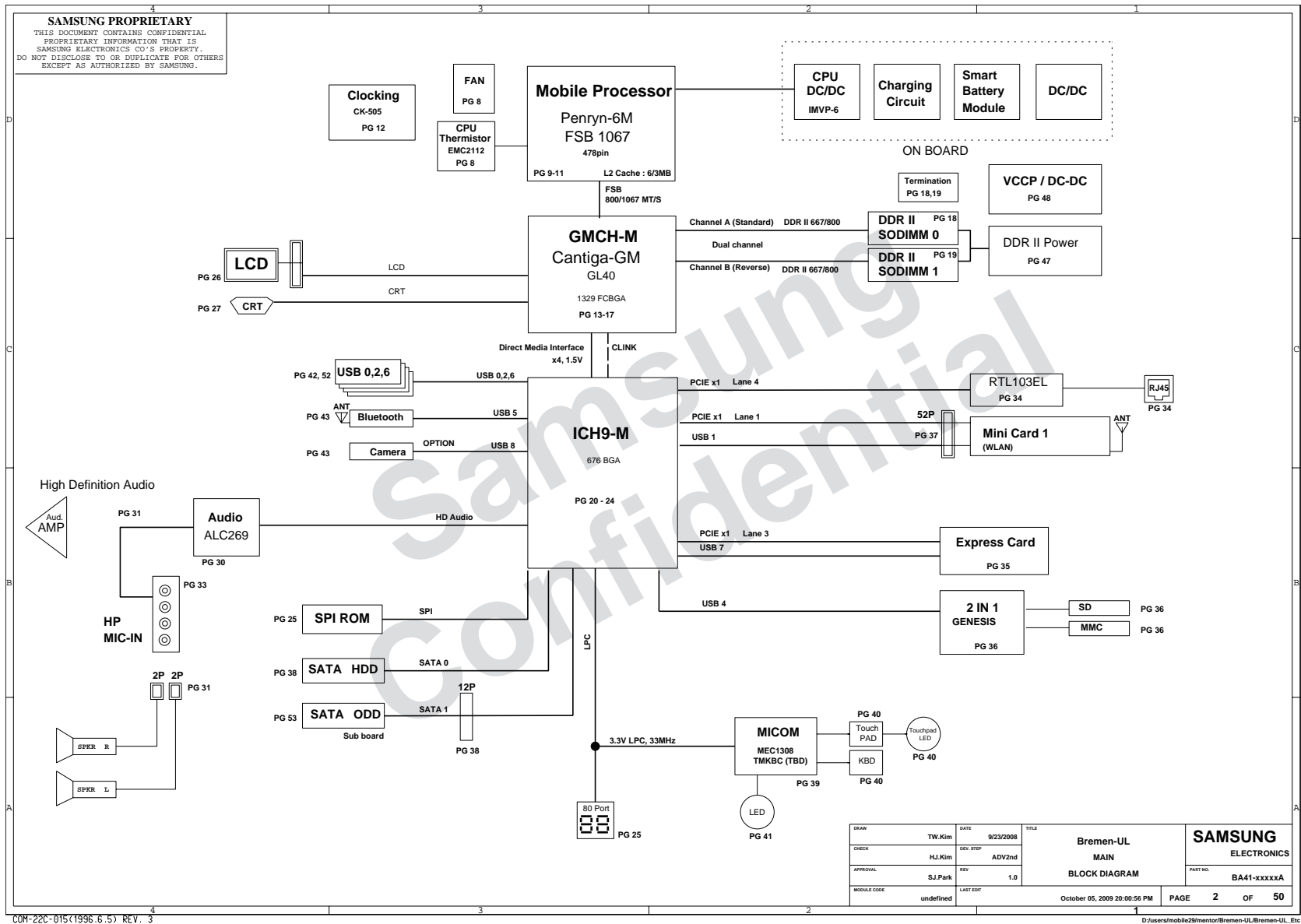
8. Block Diagram and Schematic



8. Block Diagram and Schematic

SAMSUNG PROPRIETARY <small>THIS DOCUMENT CONTAINS CONFIDENTIAL PROPRIETARY INFORMATION THAT IS SAMSUNG ELECTRONICS CO.'S PROPERTY. DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS EXCEPT AS AUTHORIZED BY SAMSUNG.</small>																							
<h1>Bremen-UL</h1>																							
CPU : Intel Penryn Chip Set : Intel Cantiga & ICH9M Remarks : Montevina Platform																							
<table border="1"> <tr> <td>Model Name</td> <td>: Bremen-UL</td> </tr> <tr> <td>PBA Name</td> <td>: MAIN</td> </tr> <tr> <td>PCB Code</td> <td>: GCE : BA41-01177A : NAN : BA41-01178A : HAN : BA41-01179A</td> </tr> <tr> <td>Dev. Step</td> <td>: PV</td> </tr> <tr> <td>Revision</td> <td>: 1.0</td> </tr> <tr> <td>T.R. Date</td> <td>: 2009.10.19</td> </tr> </table>				Model Name	: Bremen-UL	PBA Name	: MAIN	PCB Code	: GCE : BA41-01177A : NAN : BA41-01178A : HAN : BA41-01179A	Dev. Step	: PV	Revision	: 1.0	T.R. Date	: 2009.10.19								
Model Name	: Bremen-UL																						
PBA Name	: MAIN																						
PCB Code	: GCE : BA41-01177A : NAN : BA41-01178A : HAN : BA41-01179A																						
Dev. Step	: PV																						
Revision	: 1.0																						
T.R. Date	: 2009.10.19																						
<table border="1"> <tr> <th>Design</th> <th>CHECK</th> <th>APPROVAL</th> </tr> <tr> <td> </td> <td> </td> <td> </td> </tr> <tr> <td> </td> <td> </td> <td> </td> </tr> </table>				Design	CHECK	APPROVAL																	
Design	CHECK	APPROVAL																					
Owner : SEC Mobile R & D		Signature : X																					
<table border="1"> <tr> <td>DRAW</td> <td>TW.Kim</td> <td>DATE</td> <td>10/10/2009</td> <td rowspan="3"> TITLE Bremen-UL MAIN COVER </td> <td rowspan="3"> SAMSUNG ELECTRONICS PART NO. BA41-xxxxxxA </td> </tr> <tr> <td>CHECK</td> <td>HJ.Kim</td> <td>REV. STEP</td> <td>ADV2nd</td> </tr> <tr> <td>APPROVAL</td> <td>S.J.Park</td> <td>REV</td> <td>1.0</td> </tr> <tr> <td colspan="2">MODULE CODE</td> <td colspan="2">LAST EDIT</td> <td>October 05, 2009 20:00:56 PM</td> <td>PAGE 1 OF 50</td> </tr> </table>		DRAW	TW.Kim	DATE	10/10/2009	TITLE Bremen-UL MAIN COVER	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxxA	CHECK	HJ.Kim	REV. STEP	ADV2nd	APPROVAL	S.J.Park	REV	1.0	MODULE CODE		LAST EDIT		October 05, 2009 20:00:56 PM	PAGE 1 OF 50	1 <small>D:\users\mobile29\mentor\Bremen-UL\Bremen-UL_Etc</small>	
DRAW	TW.Kim	DATE	10/10/2009	TITLE Bremen-UL MAIN COVER	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxxA																		
CHECK	HJ.Kim	REV. STEP	ADV2nd																				
APPROVAL	S.J.Park	REV	1.0																				
MODULE CODE		LAST EDIT		October 05, 2009 20:00:56 PM	PAGE 1 OF 50																		

8. Block Diagram and Schematic



8. Block Diagram and Schematic

SAMSUNG PROPRIETARY
THIS DOCUMENT CONTAINS CONFIDENTIAL
PROPRIETARY INFORMATION THAT IS
SAMSUNG ELECTRONICS CO.'S PROPERTY.
DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS
EXCEPT AS AUTHORIZED BY SAMSUNG.

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	0	NC
1	SYSTEM PORT 1	1	Mini Card 1 (WLAN)
2	SYSTEM PORT 2	2	NC
3	NC	3	LOM
4	NC	4	Mini Card 2 (ROBSON or DVB-T)
5	Bluetooth	5	NC
6	Mini PCI Express 2		
7	Camera		
8	NC		
9	NC		

(This table will be update.)

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	RealTek 88E8057

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0
---------	------------	-----------------

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

REVISION HISTORY

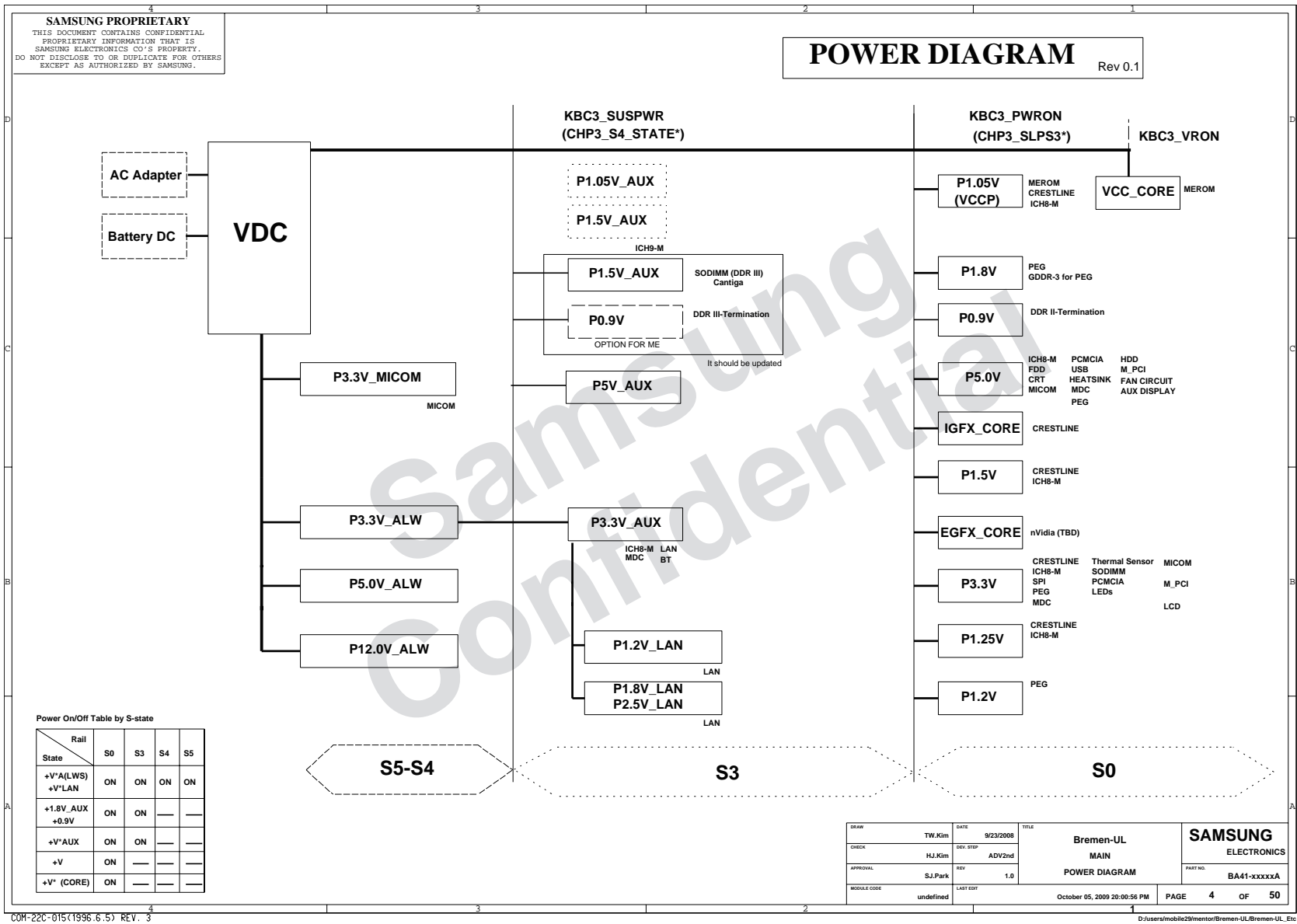
See rev notes for more information.

DRAW	TW.Kim	DATE	9/23/2008	TITLE	Bremen-UL		SAMSUNG ELECTRONICS
CHECK	HJ.Kim	REV. STEP	ADV2nd		MAIN		
APPROVAL	S.J.Park	REV	1.0		BOARD INFO		PART NO. BA41-xxxxxA
MODULE CODE	undefined	LAST EDIT			October 05, 2009 20:00:56 PM	PAGE	3 OF 50

COM-22C-015(1996.6.5) REV. 3

D:\users\mobile29\mentor\Bremen-UL\Bremen-UL_Etc

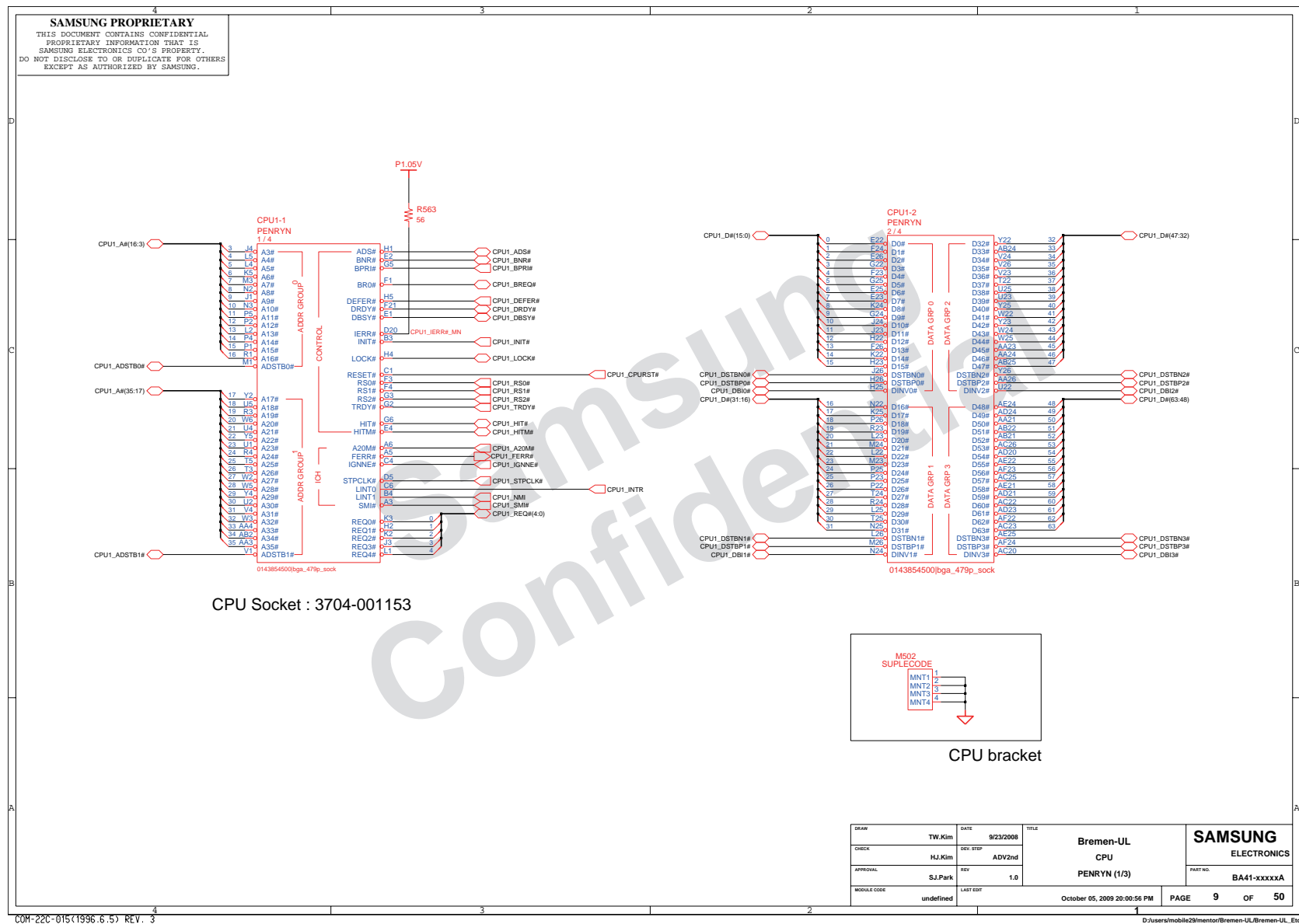
8. Block Diagram and Schematic



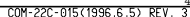
8. Block Diagram and Schematic



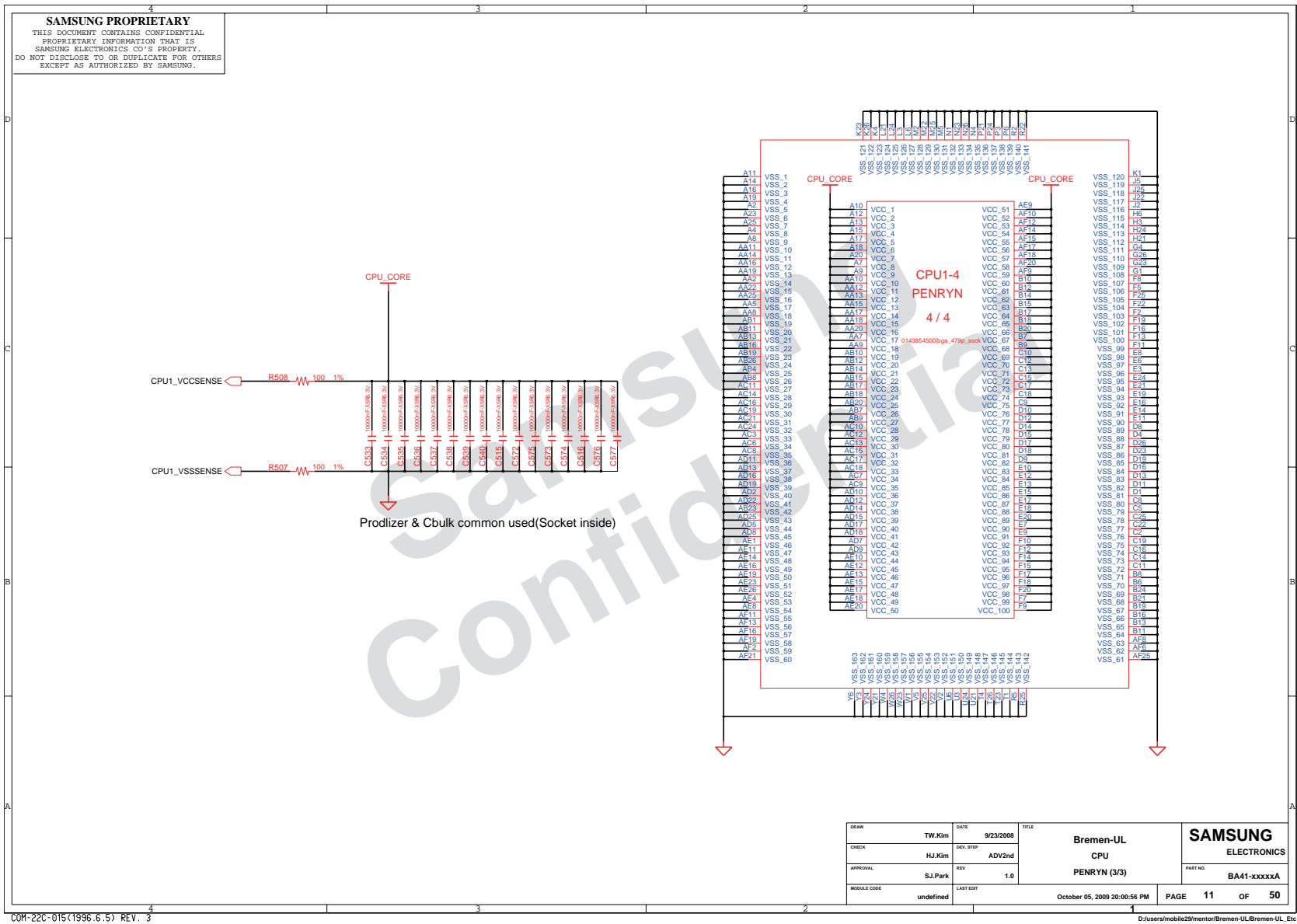
8. Block Diagram and Schematic



8. Block Diagram and Schematic



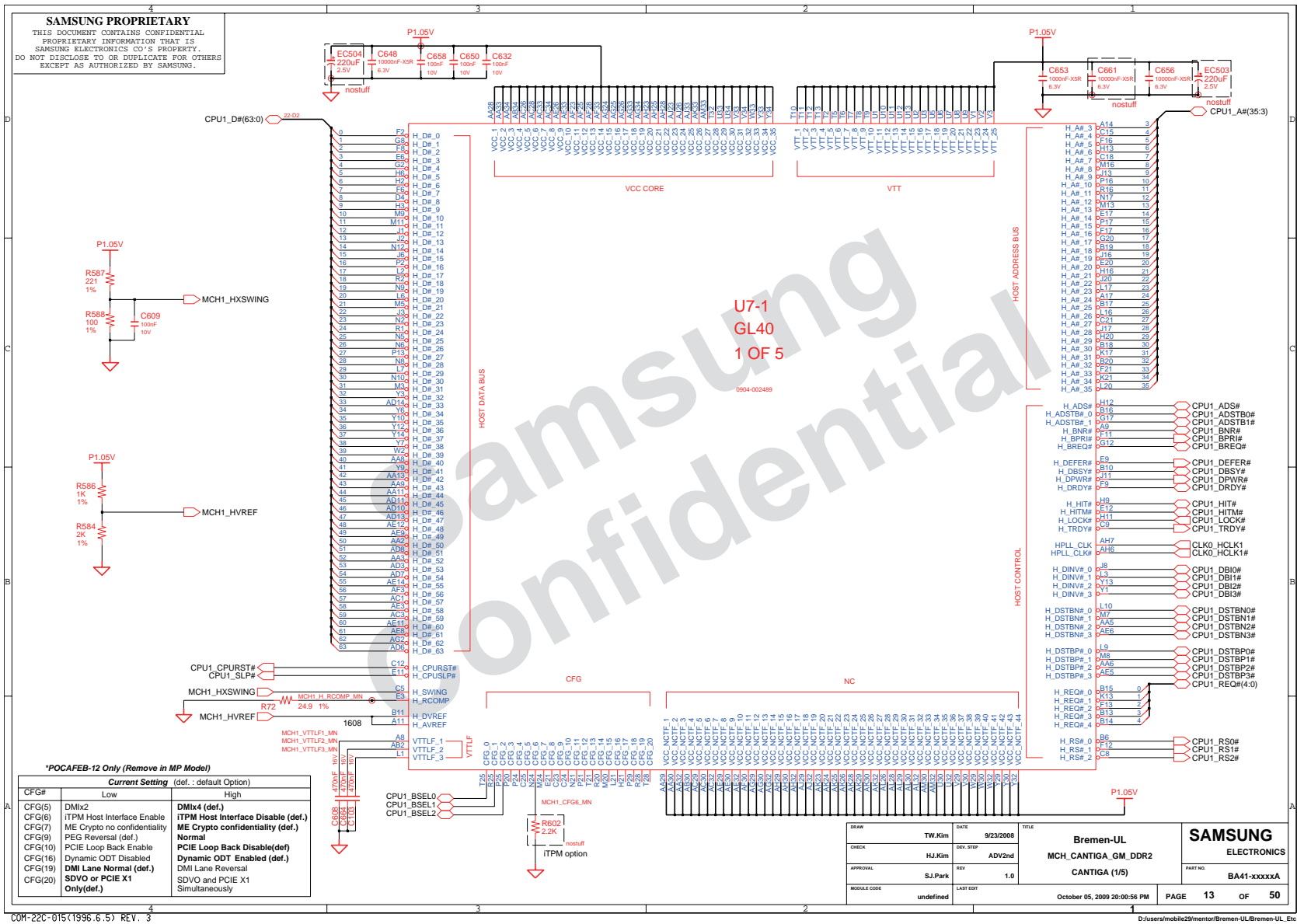
8. Block Diagram and Schematic



8. Block Diagram and Schematic



8. Block Diagram and Schematic



8. Block Diagram and Schematic





8. Block Diagram and Schematic



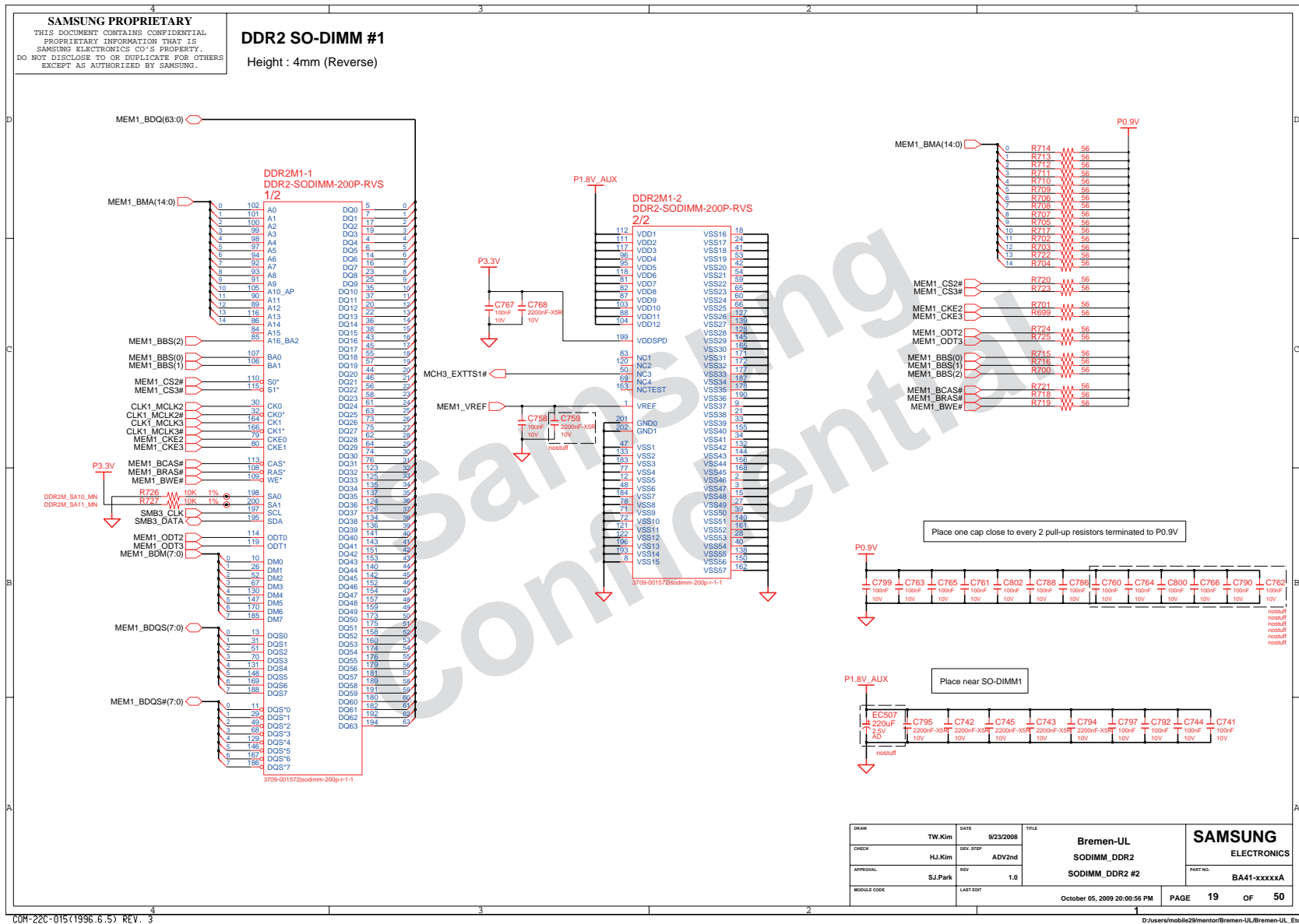
- ## 8. Block Diagram and Schematic



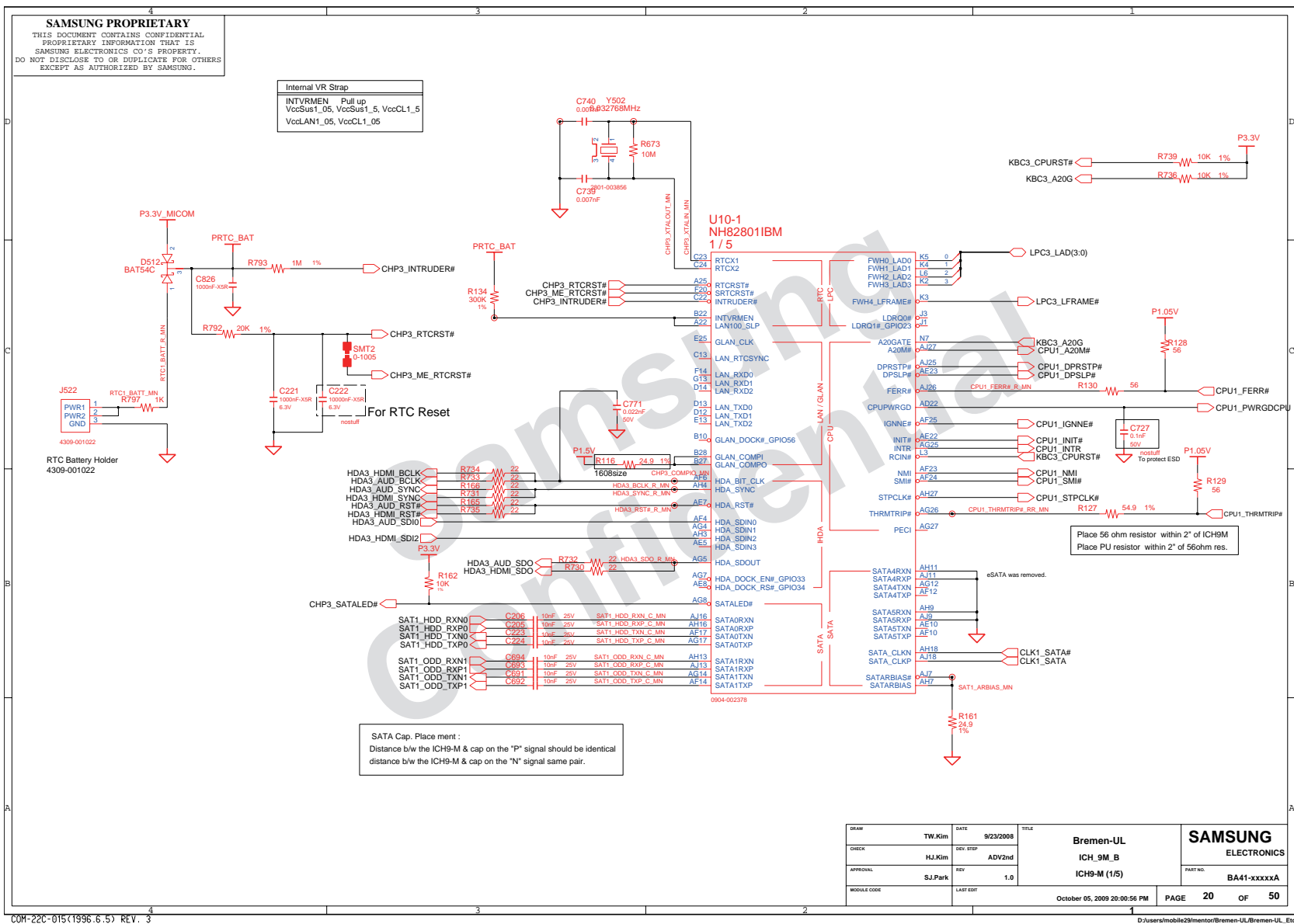
8. Block Diagram and Schematic

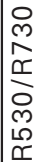


8. Block Diagram and Schematic

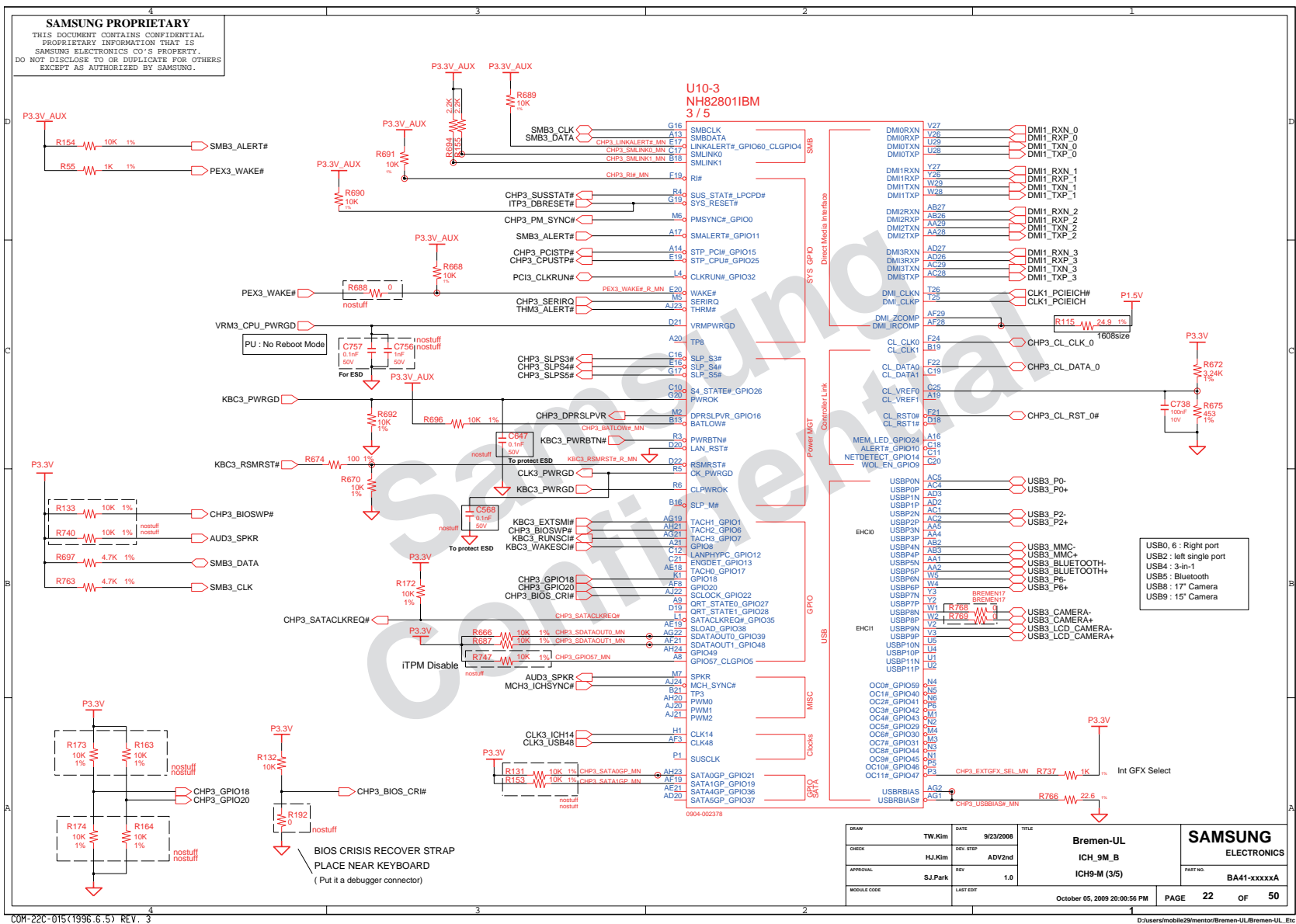


8. Block Diagram and Schematic

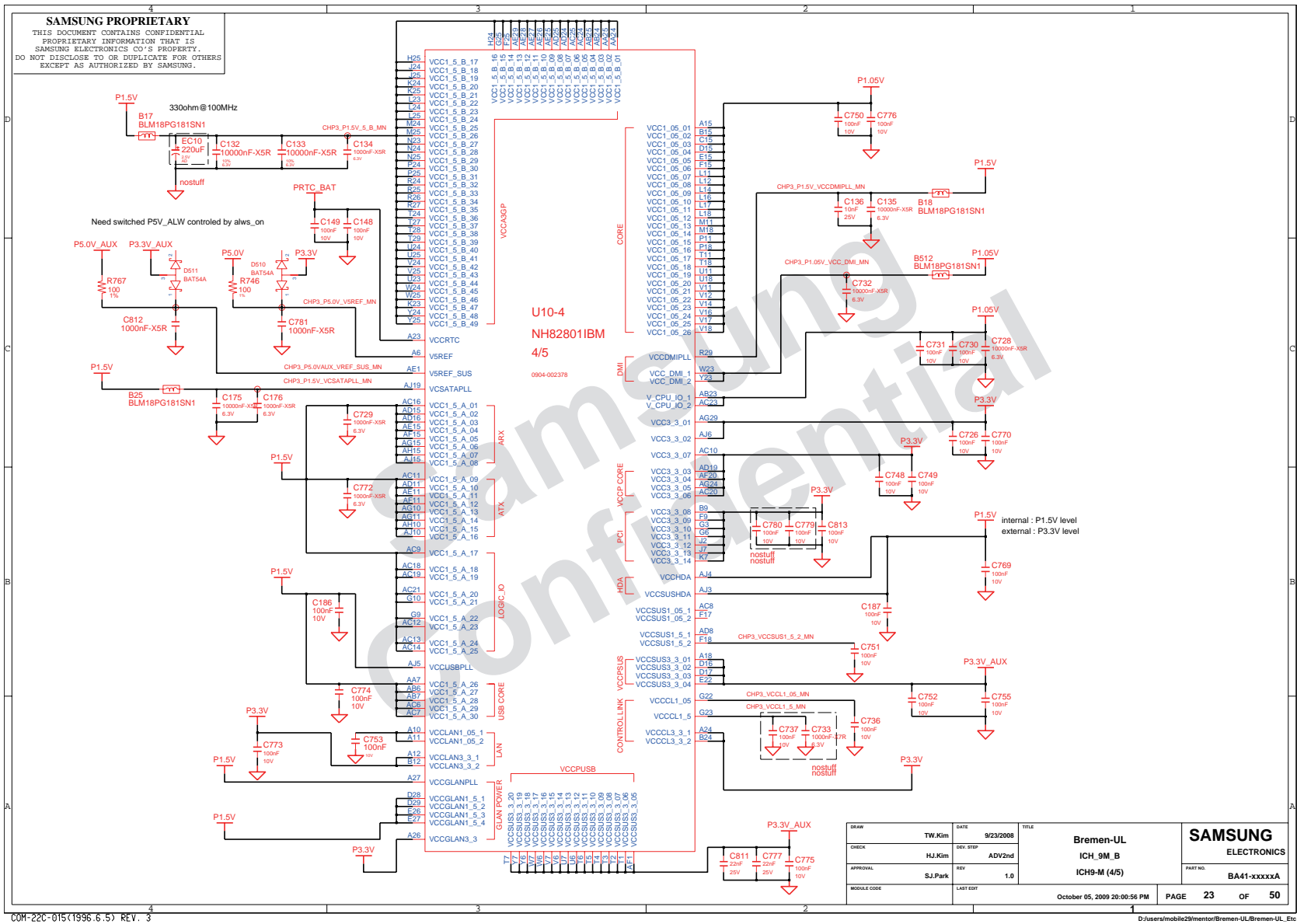




8. Block Diagram and Schematic

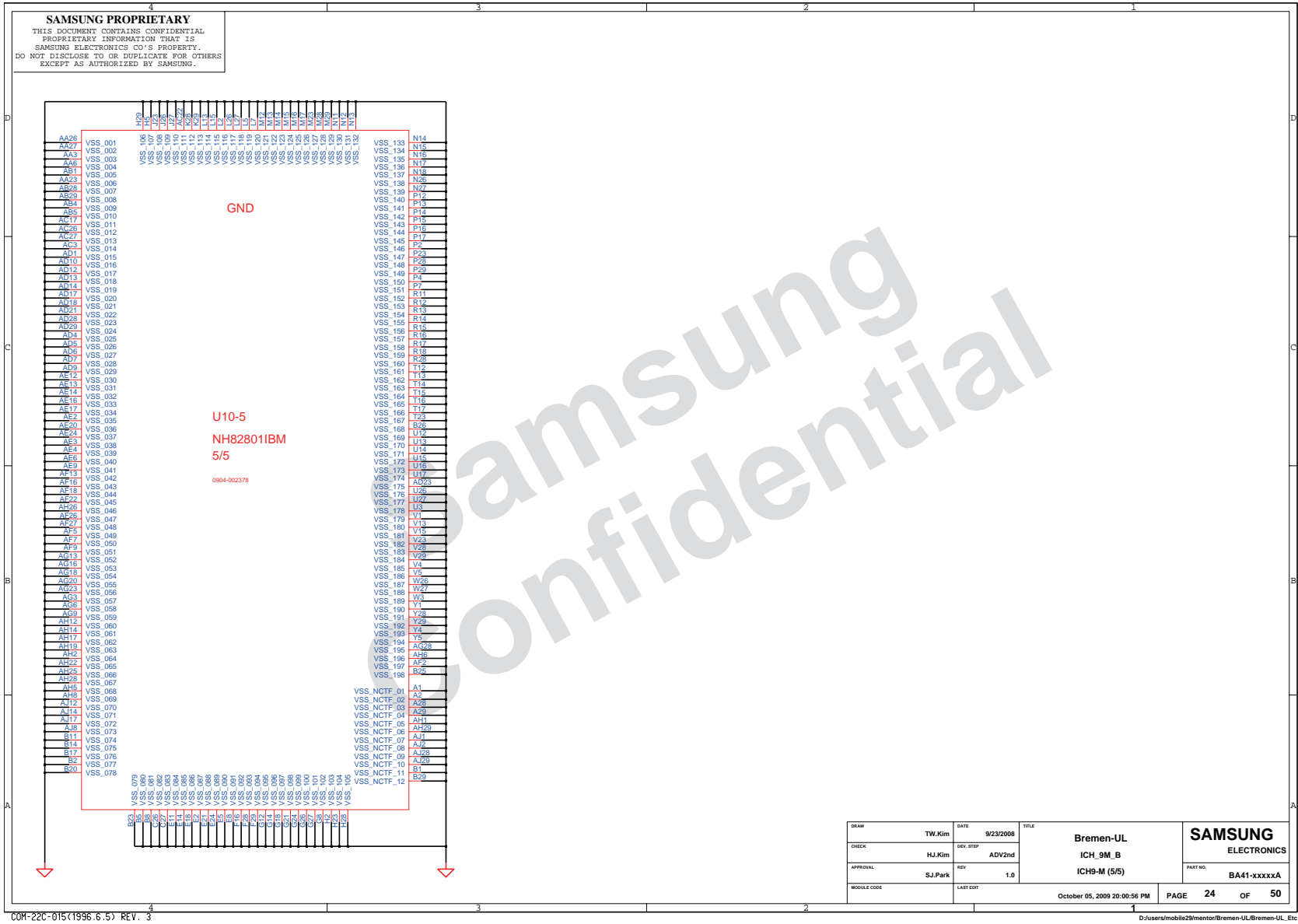


8. Block Diagram and Schematic



- 이 문서는 삼성전자의 기술 자산으로 승인자만이 사용할 수 있습니다 -
- This Document can not be used without Samsung's authorization -

8. Block Diagram and Schematic

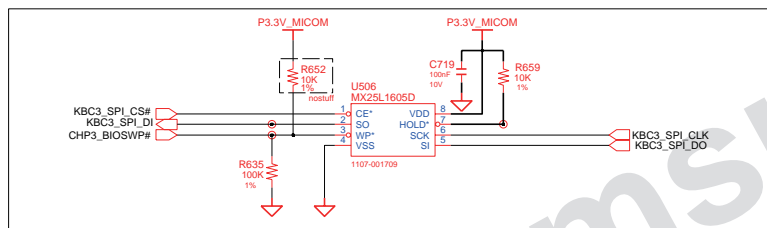


8. Block Diagram and Schematic

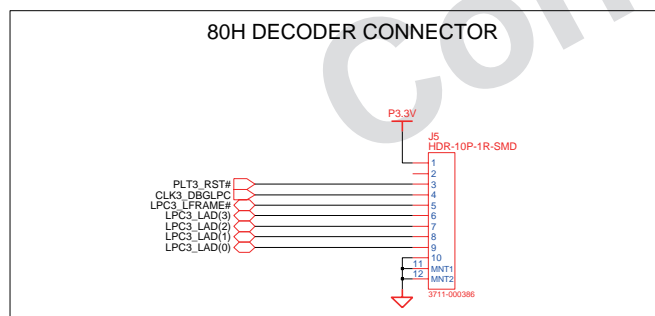
SAMSUNG PROPRIETARY
THIS DOCUMENT CONTAINS CONFIDENTIAL
PROPRIETARY INFORMATION THAT IS
SAMSUNG ELECTRONICS CO'S PROPERTY.
DO NOT DISCLOSE TO OR DUPLICATE FOR OTHERS
EXCEPT AS AUTHORIZED BY SAMSUNG.

SPI_BIOS_ROM

16MBit

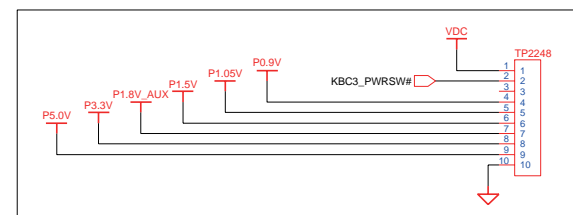


80H DECODER CONNECTOR



80port will be removed in MP stage.

02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	67	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	68	DISPLAY SHADOW MESSAGE
05	INIT STATHW	69	PLAYBACK DISPOSABLE SEGMENT
06	INIT CHIPSET REG.	70	DISPLAY ERROR MESSAGE
07	SET IN POST FLAG	71	CHECK FOR CONFIGURATION ERROR
08	INIT CPU	72	TEST READY
09	CPU CACHE ON	73	CHECK FOR KEYBOARD ERROR
0A	INIT CACHE TO POST	74	SETUP HARDWARE INTERRUPT VECTOR
0B	POST MESSAGE	75	TEST GOOD POST PRESENT
0C	ENABLE THE L-BUS IDE	76	DISABLE ON-BOARD I/O PORT
0D	INIT POWER MANAGER	77	DETECT AND INSTALL EXT RS232C
0E	POST MESSAGE	78	TEST FOR PARALLEL
0F	POST BUS MASTER RESET	79	RE-INIT ON-BOARD TO PORT
		80	INIT BIOS DATA ROM
	WITH INITIAL POST VALUE	81	INIT EXTENDED DATA AREA
14	INIT KEYBOARD CONTROLLER	82	INIT FDD CONTROLLER
16	CHECK CHECKSUM	83	SHADOW OPTION ROMS
18	256K TIMER	84	SETUP POST PROMPT
1A	8237 DMA CONTROLLER INIT	85	ENABLE HW INTERRUPT
1C	RESET INTERRUPT CONTROLLER	86	SET TIME OF DAY
1D	TEST DRABUS	A0	INIT TYPEMATH RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	RAISE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AB	ENTER S3
28	AUTO SIZING DRAM	AC	CLEAR IN POST FLAG
32	COMPUTE THE CPU SPEED	B0	CHECK FOR ERRORS
34	SHADOW SYSTEM BIOS ROM	B4	TEST DONE-PREPARE TO BOOT O/S
3A	AUTO SIZING CACHE	B6	ONE BY ONE
3C	CONFIGURE ADVANCED CHIPSET REG.	BA	CHECK PASSWORD (OPTION)
40	LOAD ALL L-BUS WITH CMOS VALUE	BE	INIT INIT
42	INIT INTERRUPT VECTOR	BE	CLEAR SCREEN
44	INIT BIOS INIT	BF	INIT INIT
46	CHECK ROM COPYRIGHT NOTICE	D0	INITERRUPT HANDLER ERROR
48	INIT I20 SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
4C	CHECK CMOS CONFIGURE AGAINST CMOS	D4	ENDING INTERRUPT ERROR
4E	INIT PCI BUS AND SLICE	D6	UNKNOWN INTERRUPT ERROR
4A	INIT ALL VIDEO BIOS ROM	D8	SHUTDOWN ERROR
50	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
52	DISPLAY (C) TYPE AND SPEED	DB	SHUTDOWN 1H
54	TEST KEYBOARD	DE	ENABLE NMI
56	SET KEYLOCK IF ENABLED	DF	INIT HDD CONTROLLER
58	ENABLE KEYBOARD	E0	LOCKDOWN HDD CONTROLLER
5A	TEST FOR UNEXPECTED INTERRUPTS	92	JUMP TO USER PATCH 2
5C	DISPLAY PRESS F2 SETUP	94	DISABLE A20 ADDRESS LINE
5E	SET TEST RAM WHEN 572K AND 640K	96	TEST FOR HIGH REG.
60	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
62	TEST EXTENDED MEMORY ADDRESS LINE		

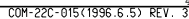


TP for ICT free

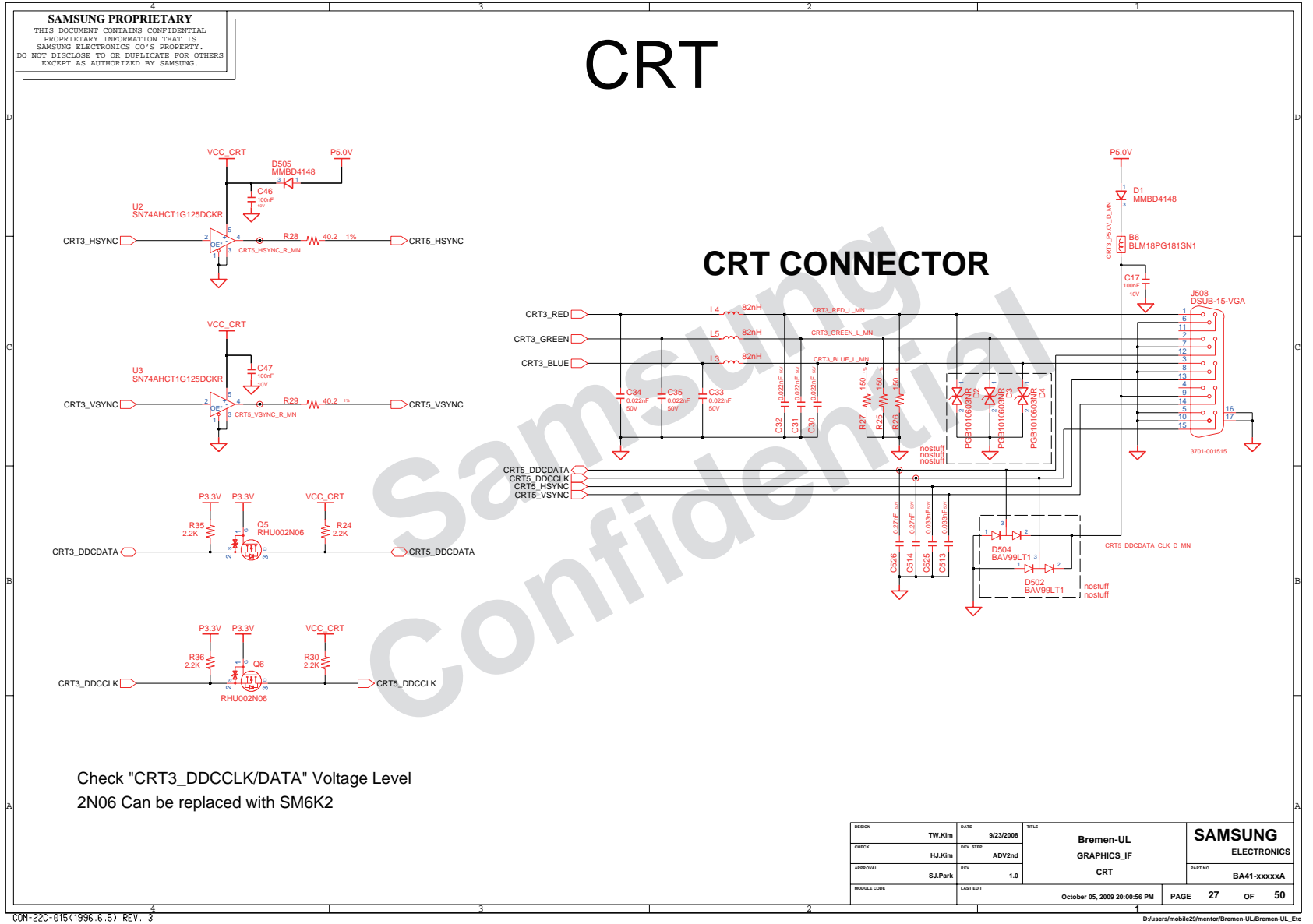
DATE	TW.Kim	DATE	9/23/2008	TITLE Bremen-UL SPI_BIOS_ROM SPI_BIOS_ROM & ICT FREE TP		SAMSUNG ELECTRONICS			
CHECK	HJ.Kim	DEV. STEP	ADV2nd						
APPROVAL	SJ.Park	REV	1.0						
PART NO.			BA41-xxxxxxA						
MODULE CODE		LAST COST		October 05, 2009 20:00:56 PM		PAGE	25	OF	50

8. Block Diagram and Schematic

8. Block Diagram and Schematic



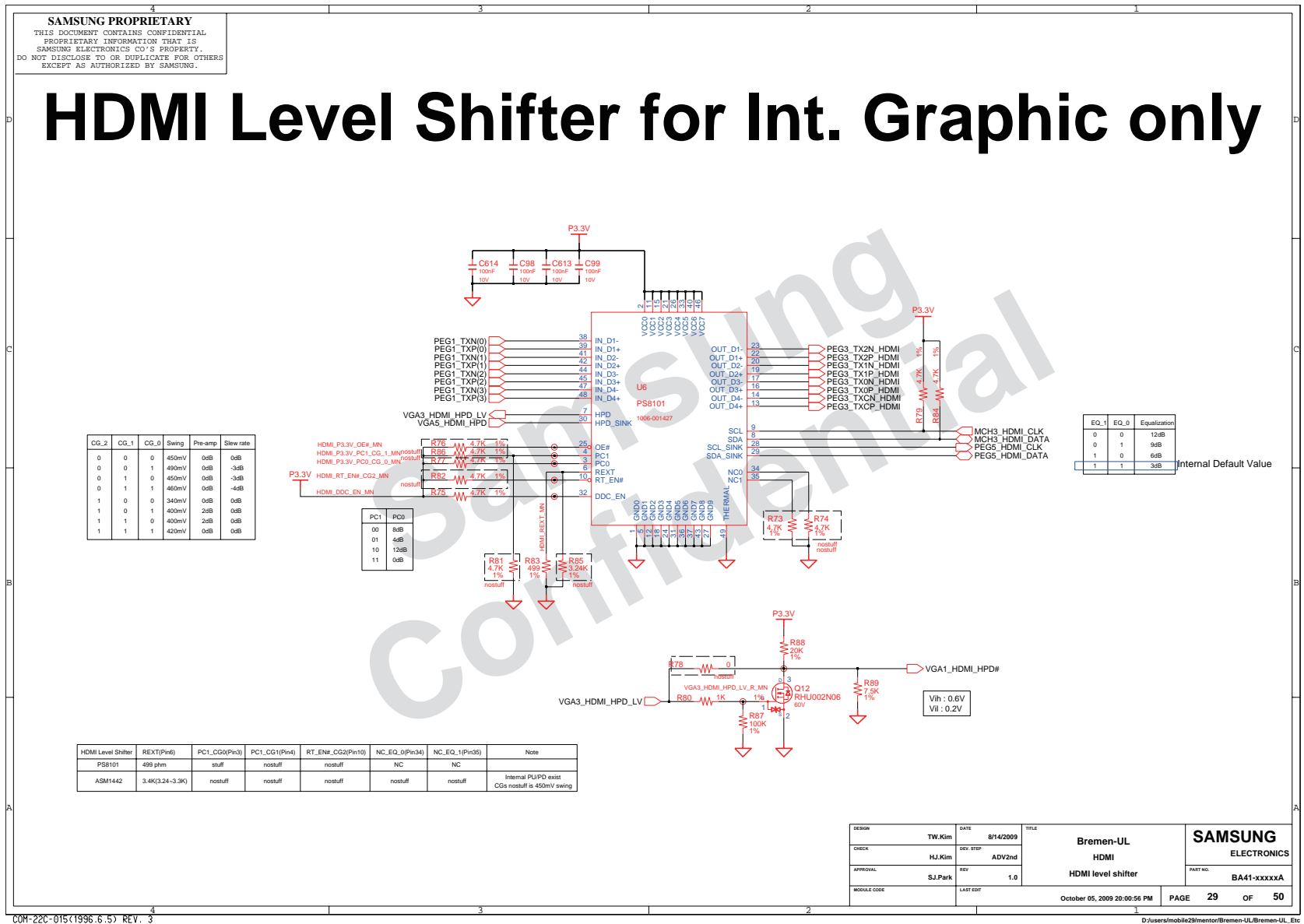
8. Block Diagram and Schematic



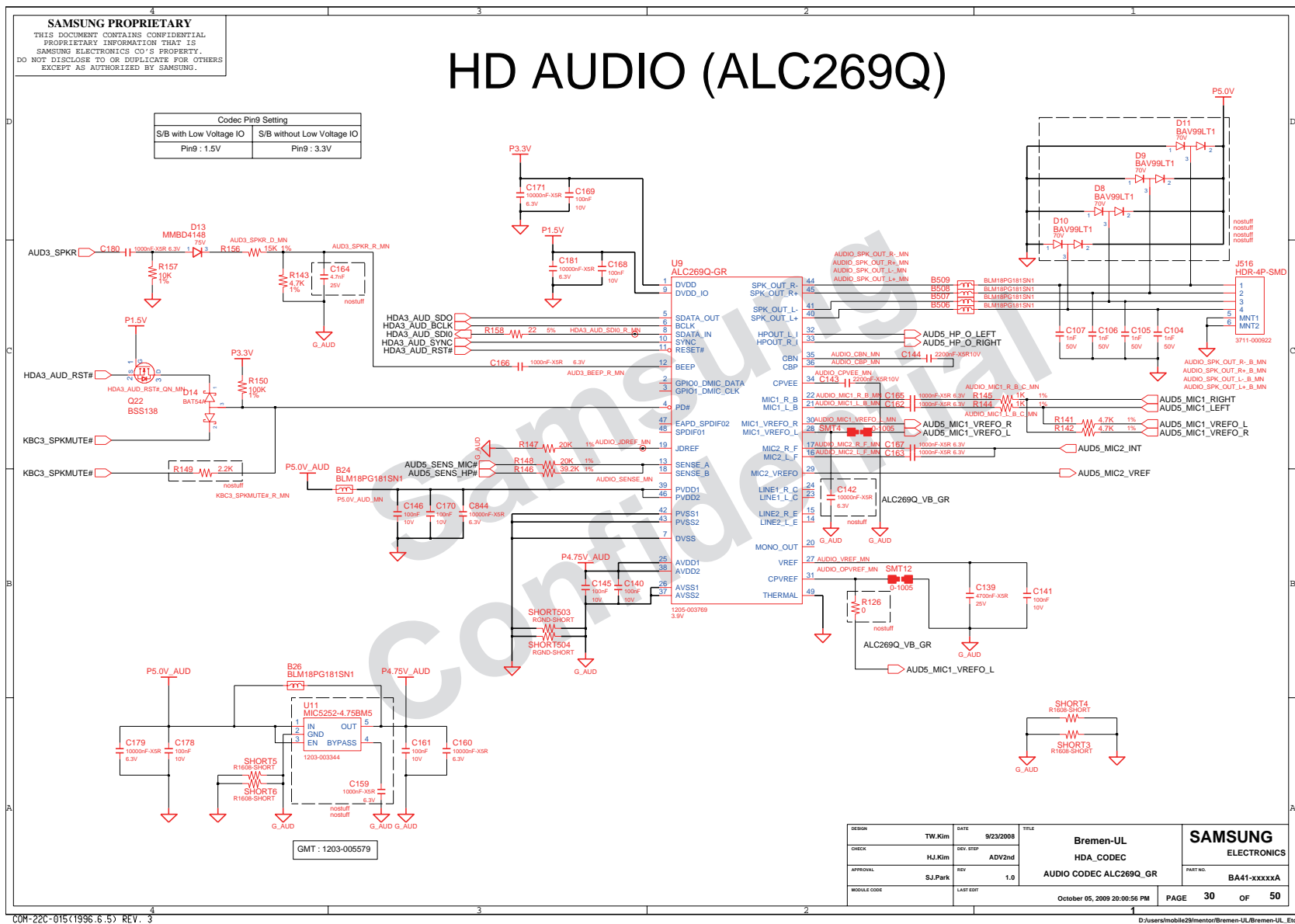
8. Block Diagram and Schematic



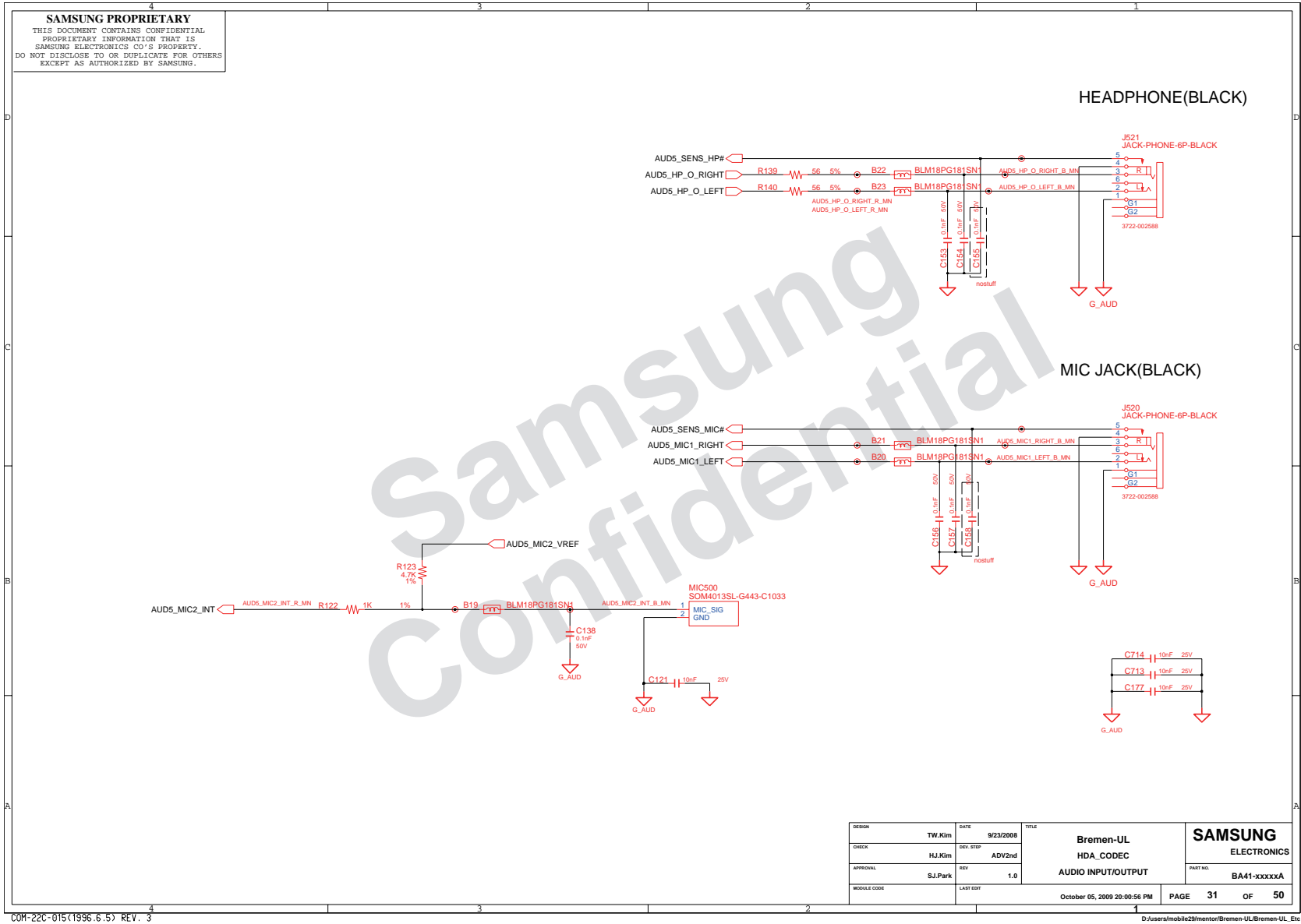
8. Block Diagram and Schematic



8. Block Diagram and Schematic



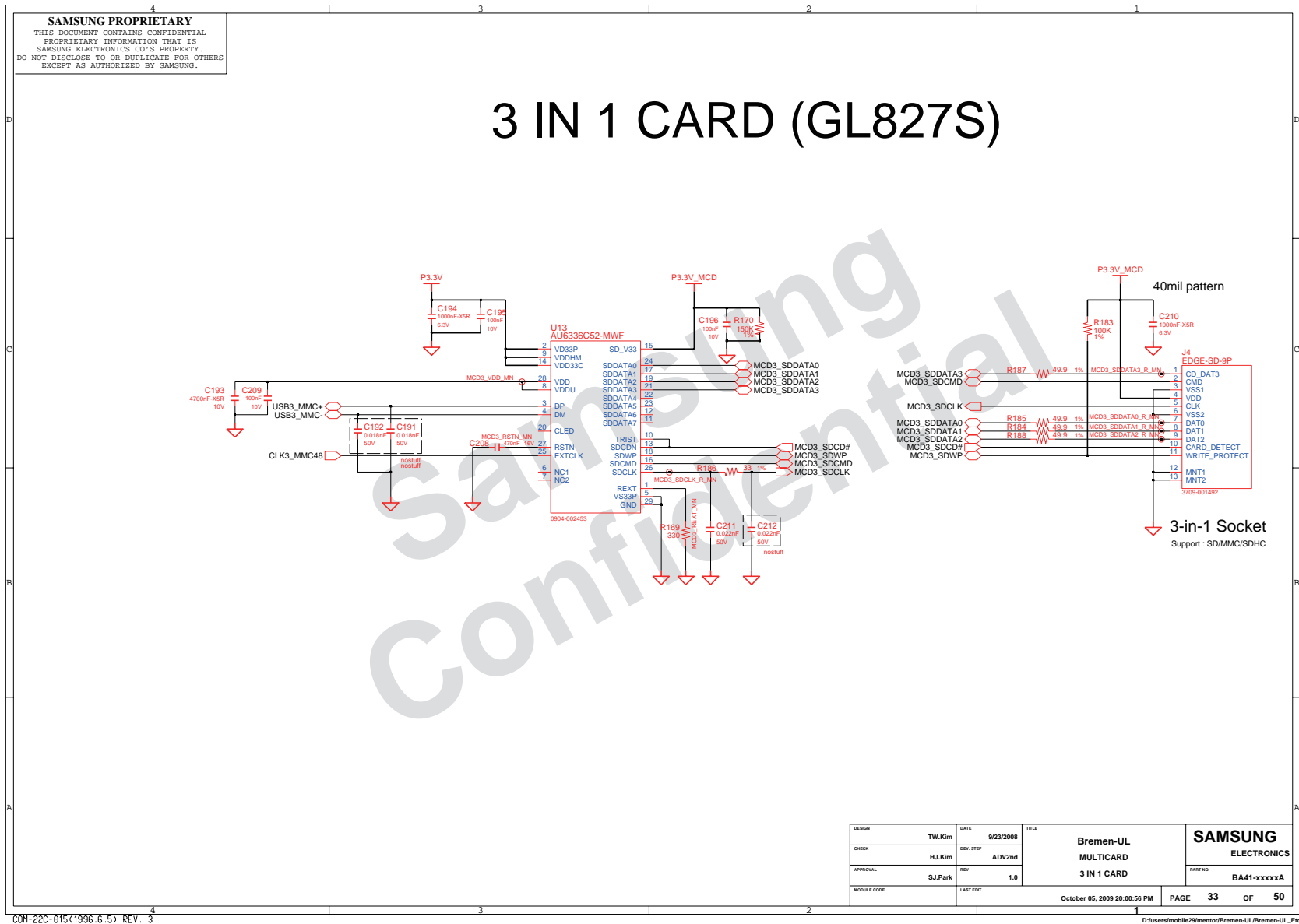
8. Block Diagram and Schematic



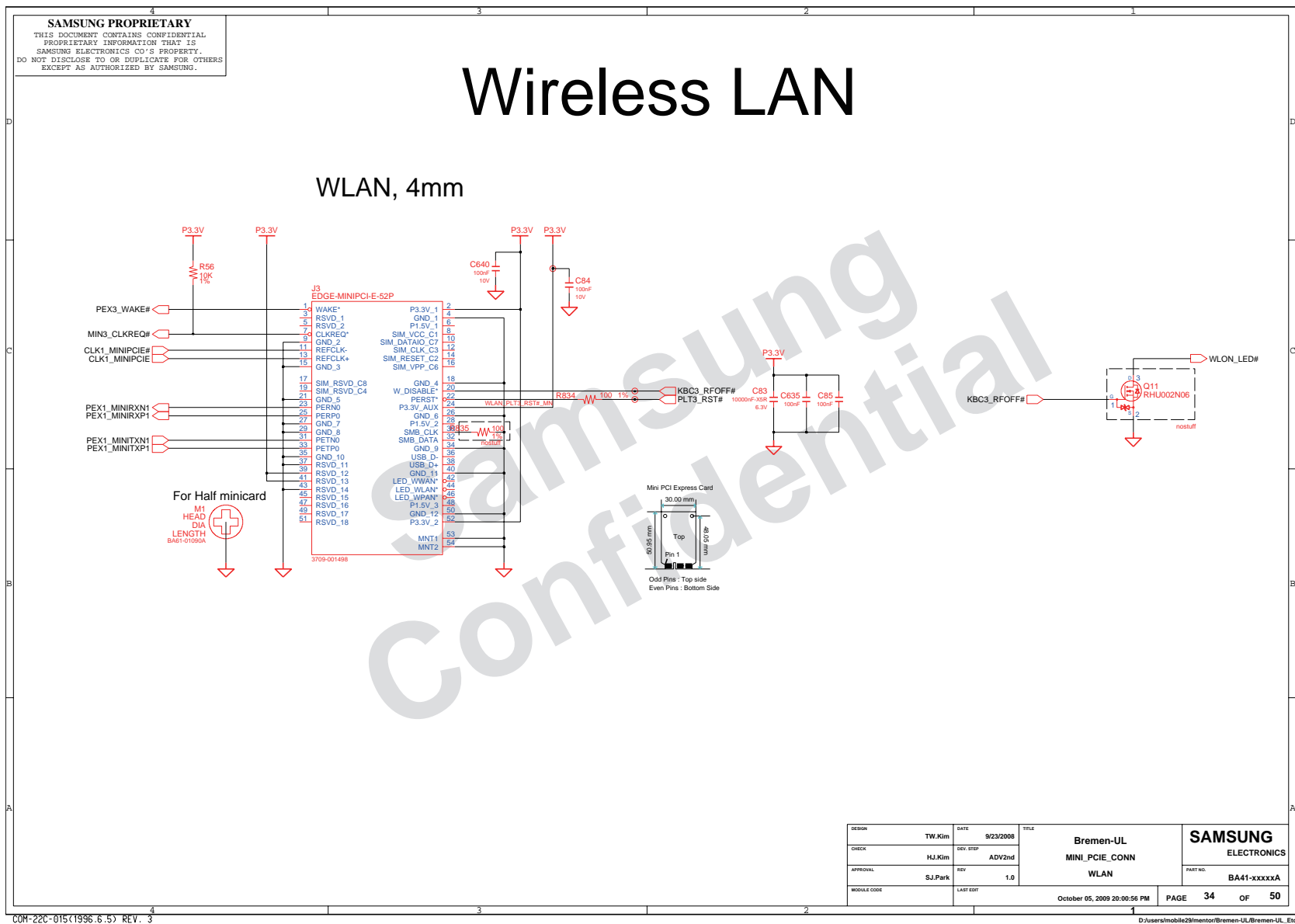
8. Block Diagram and Schematic



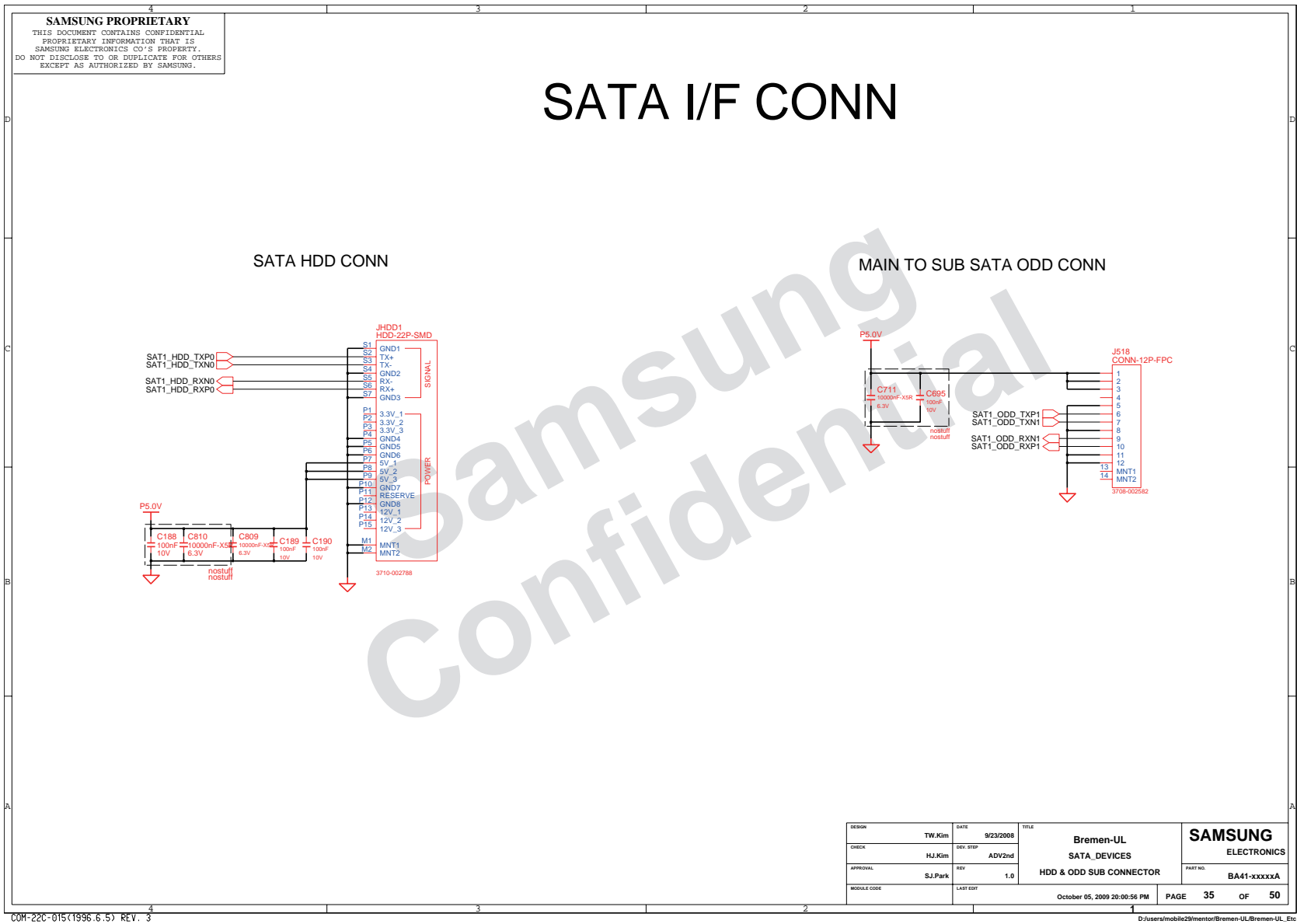
8. Block Diagram and Schematic



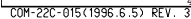
8. Block Diagram and Schematic



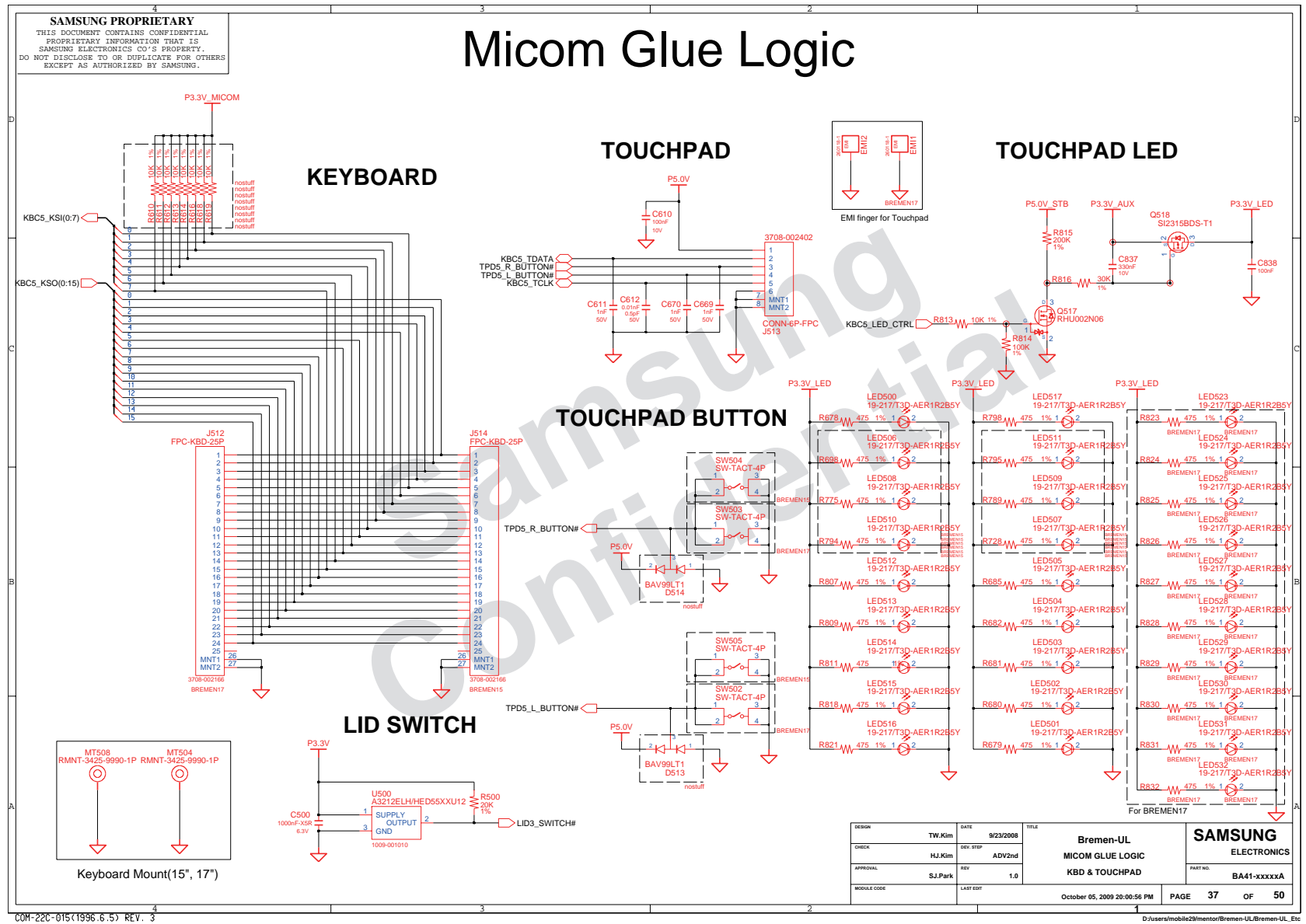
8. Block Diagram and Schematic



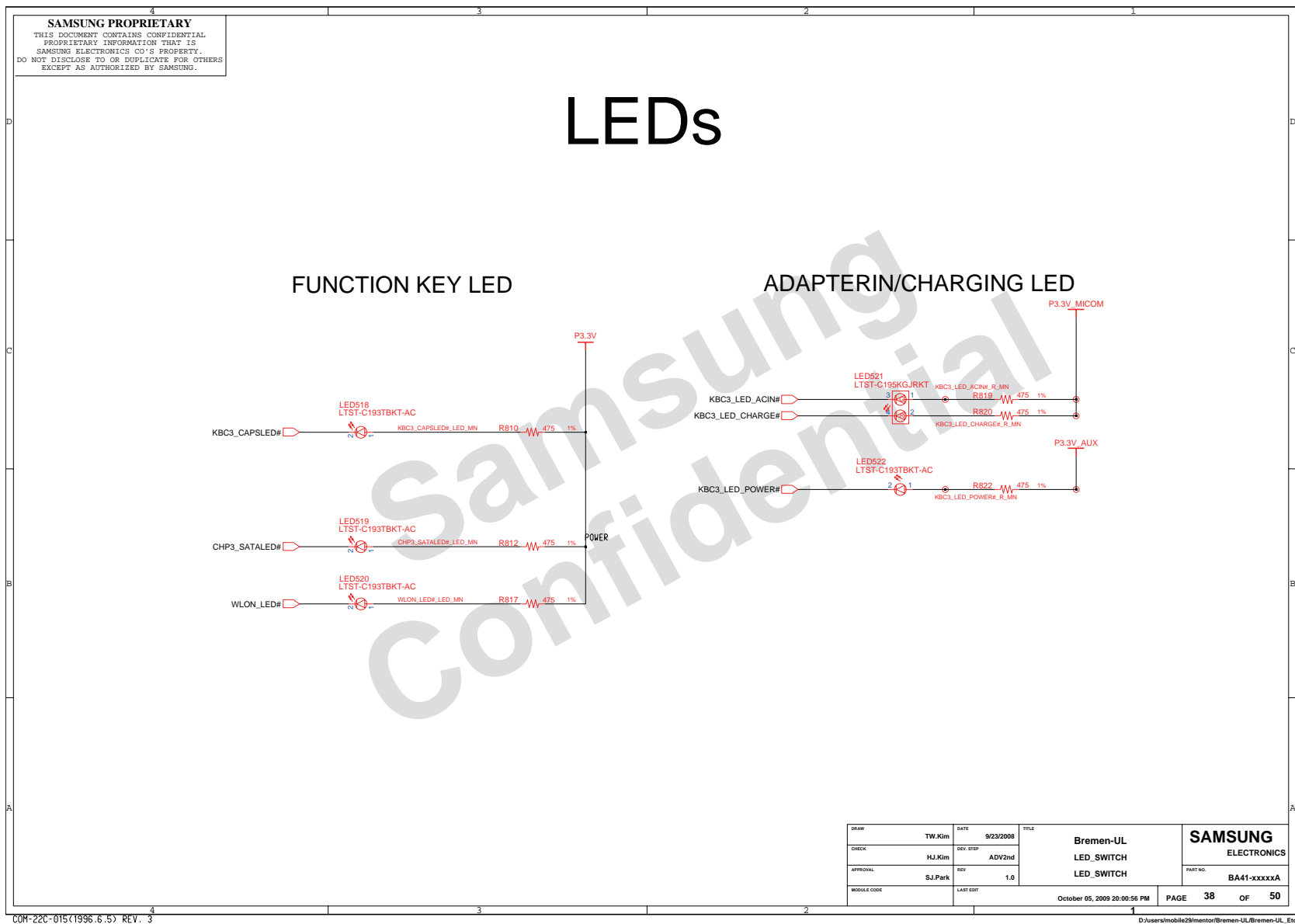
8. Block Diagram and Schematic



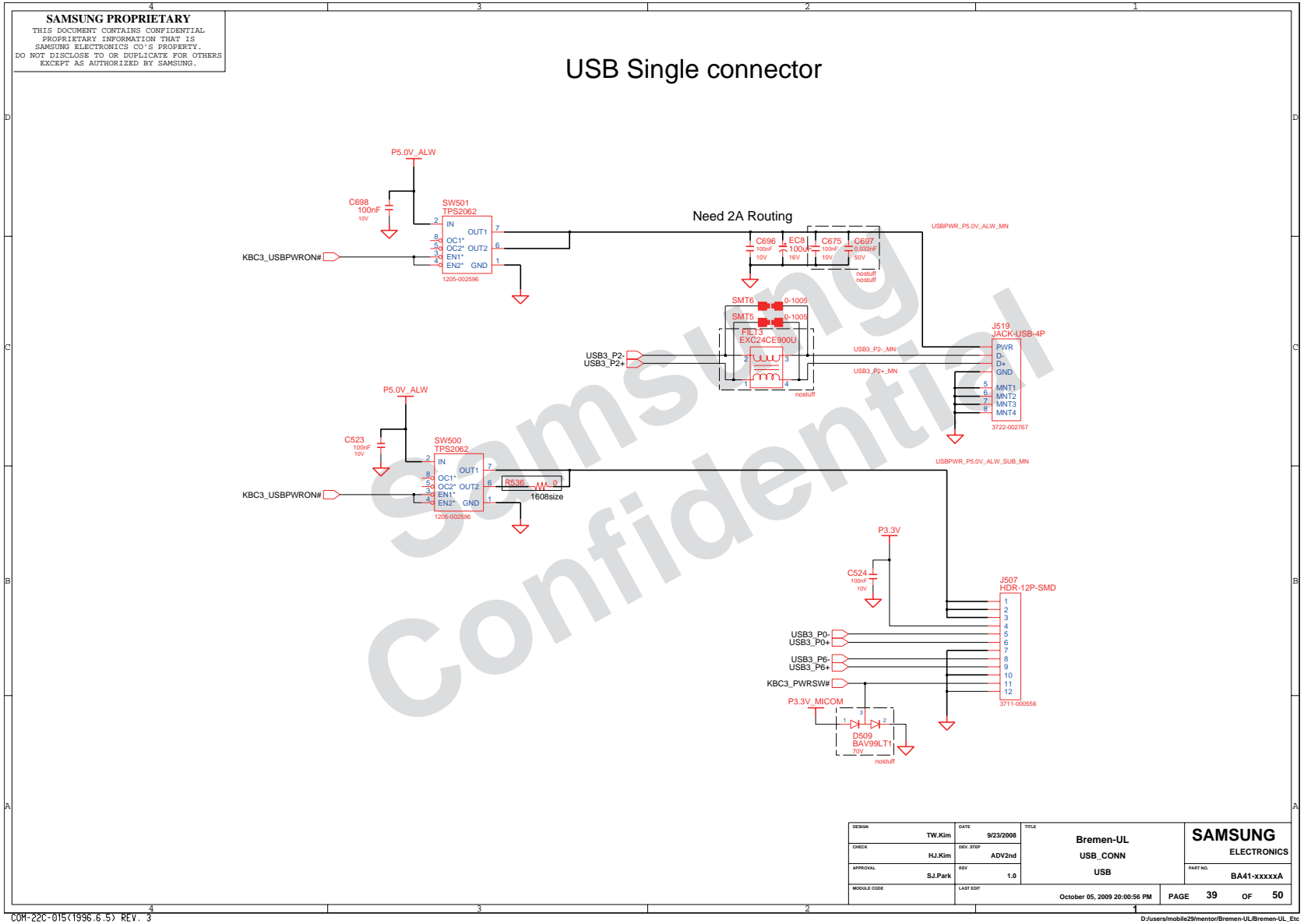
8. Block Diagram and Schematic



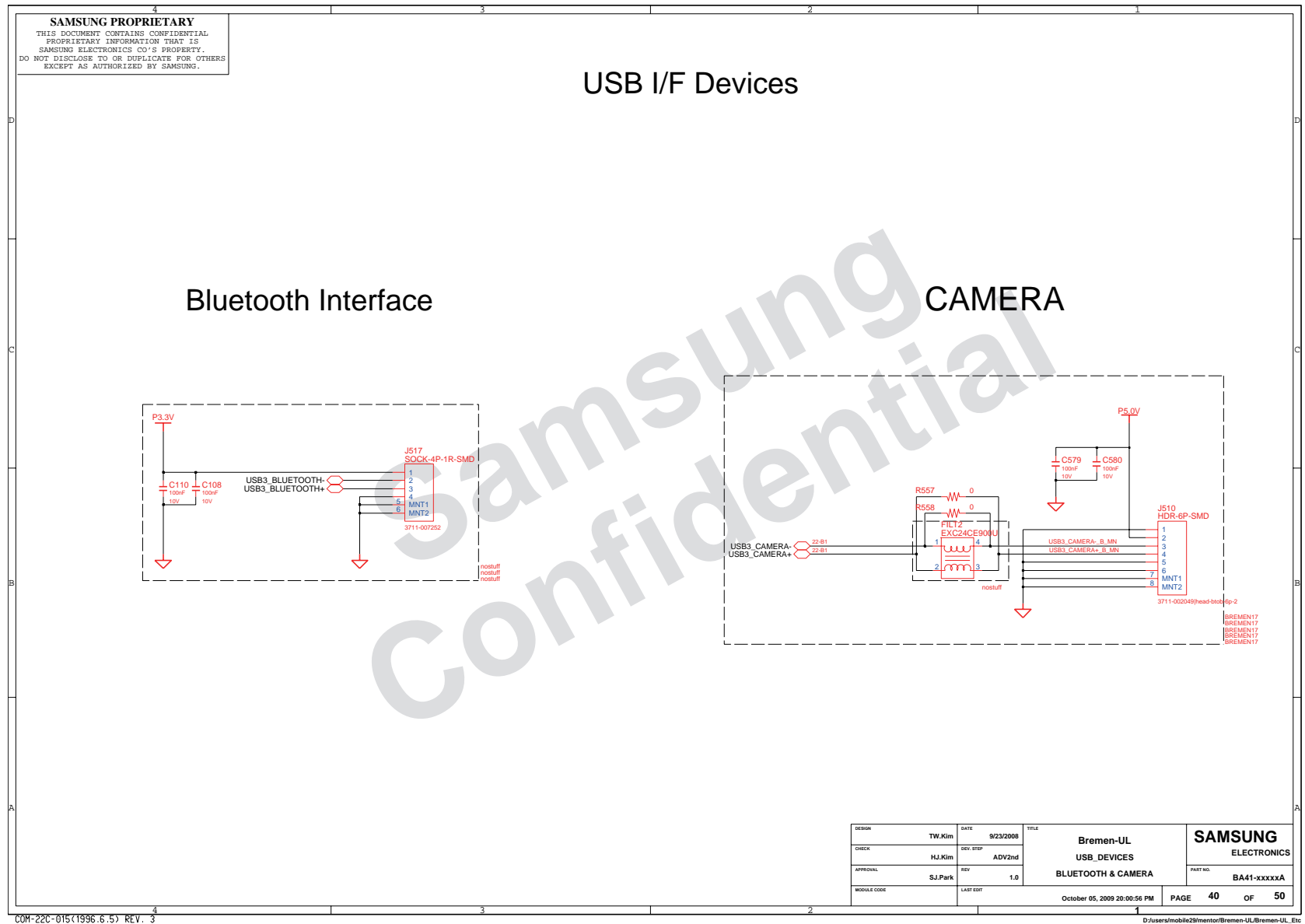
8. Block Diagram and Schematic



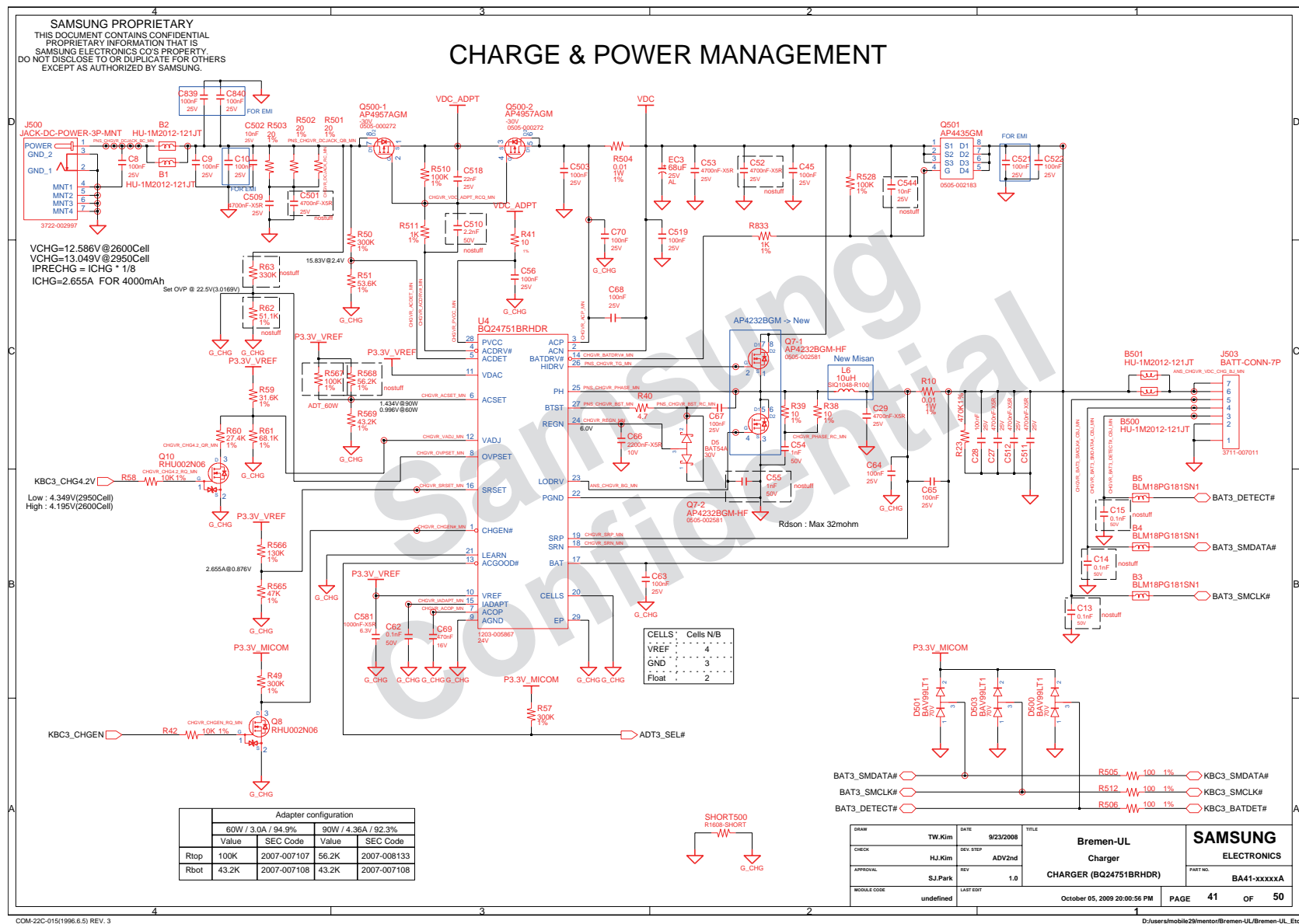
8. Block Diagram and Schematic



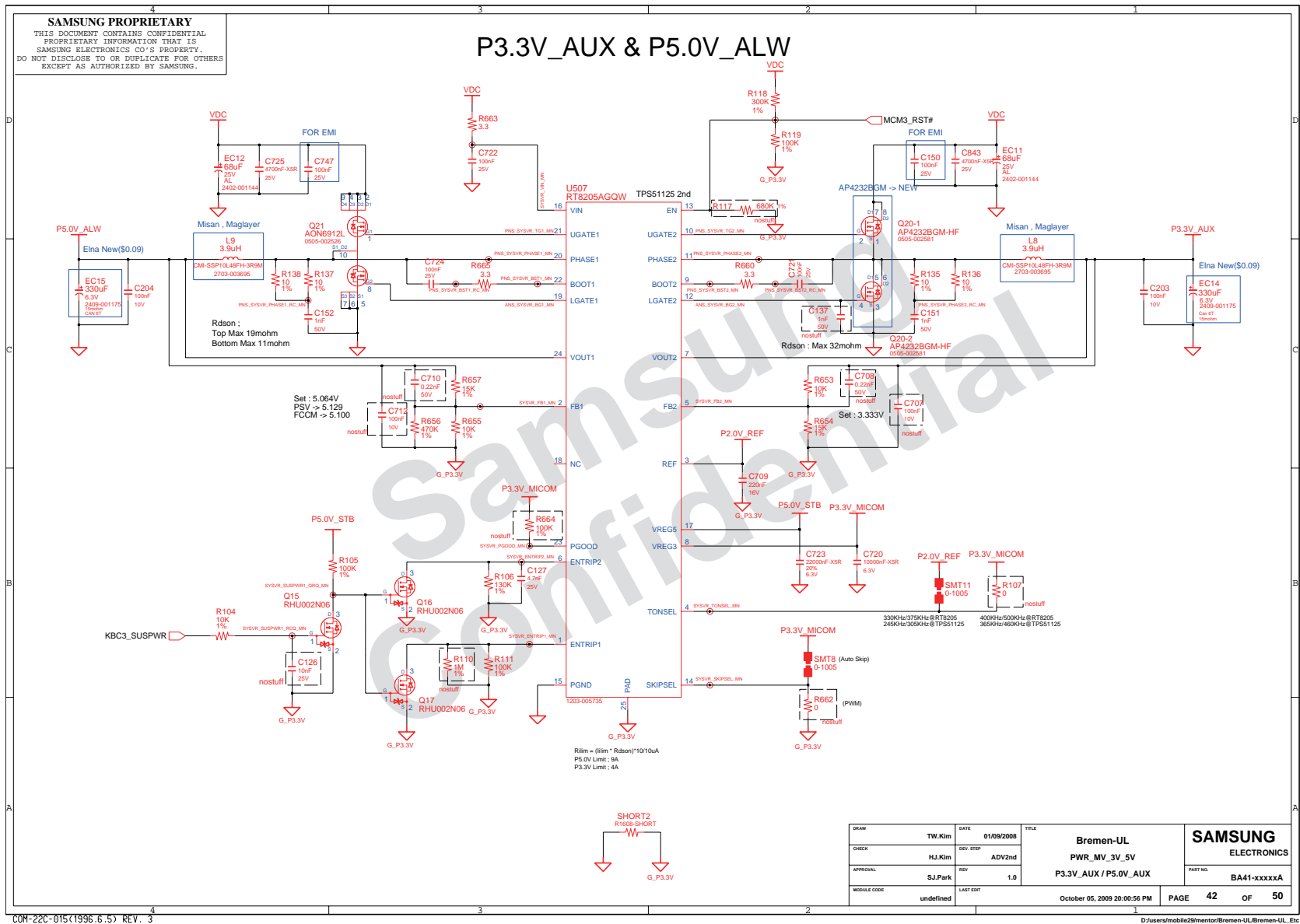
8. Block Diagram and Schematic



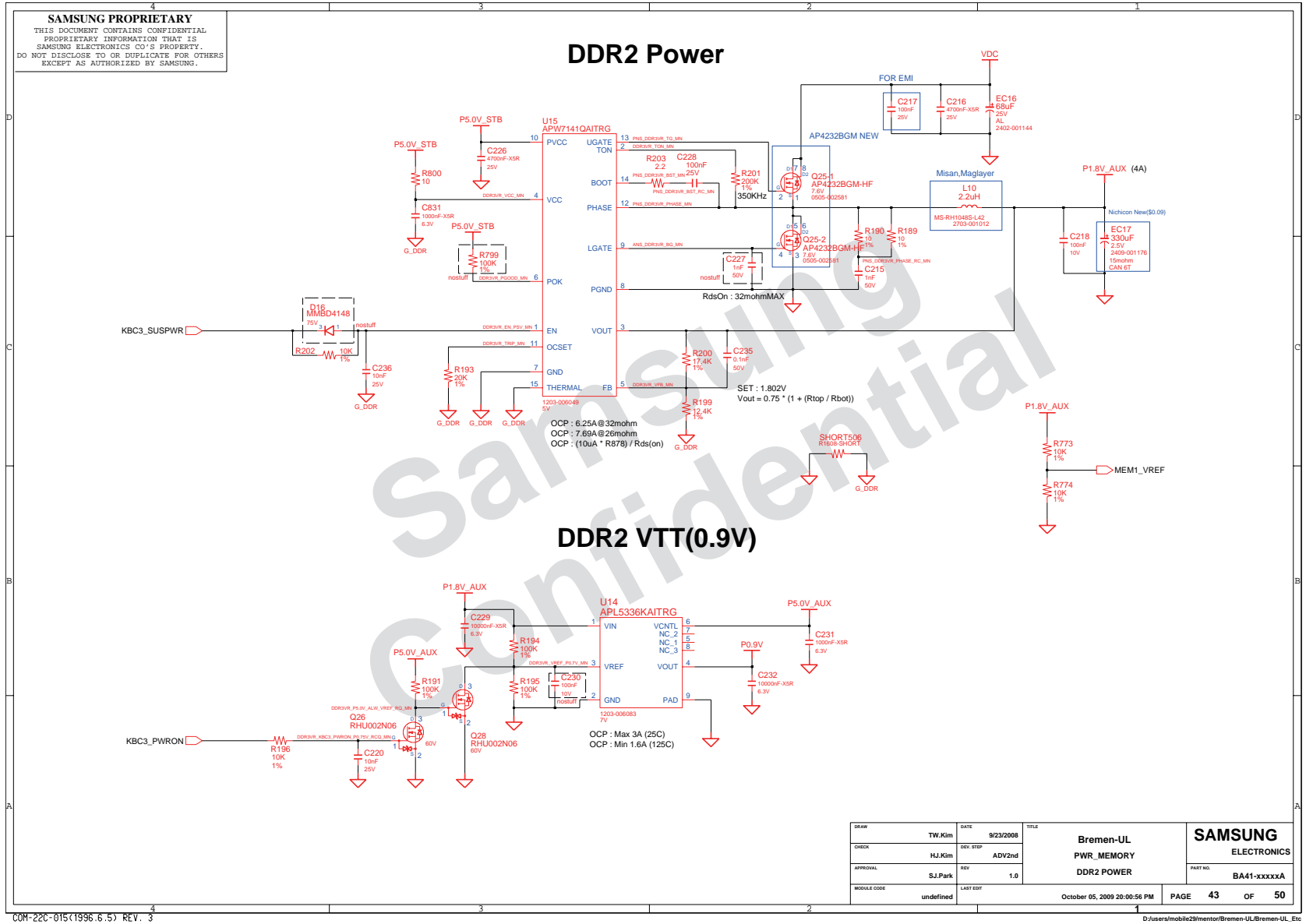
8. Block Diagram and Schematic



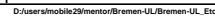
8. Block Diagram and Schematic



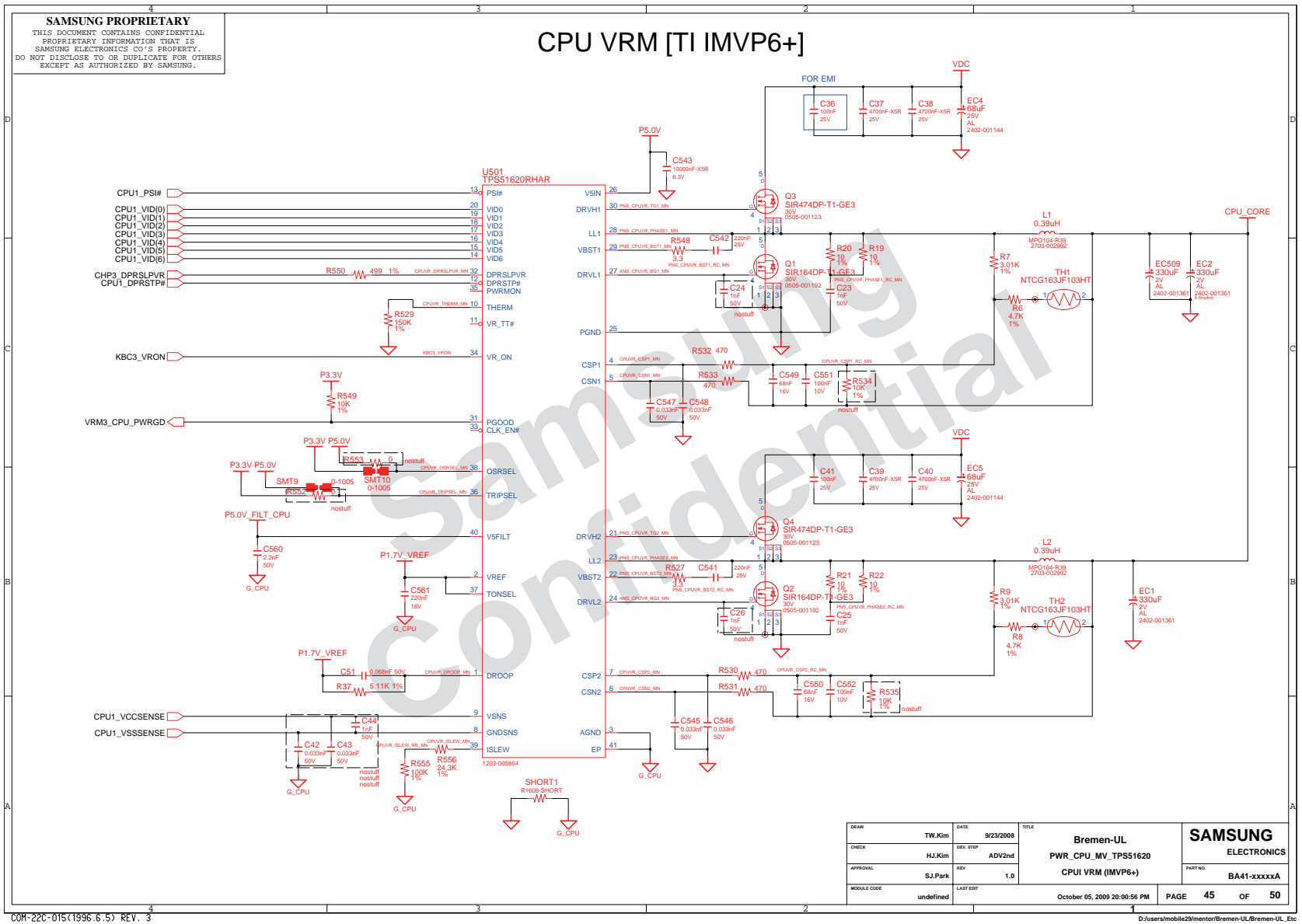
8. Block Diagram and Schematic



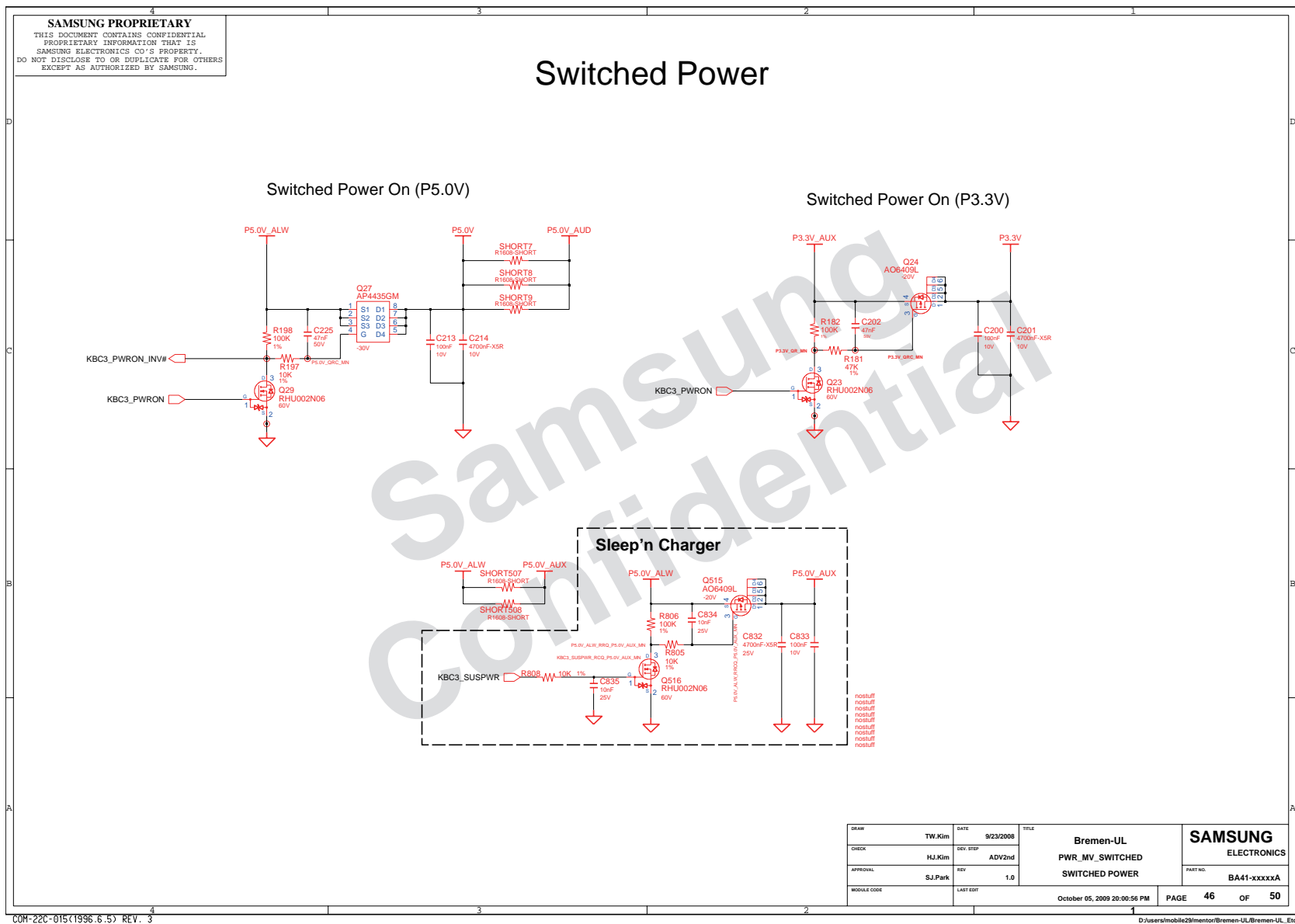
8. Block Diagram and Schematic



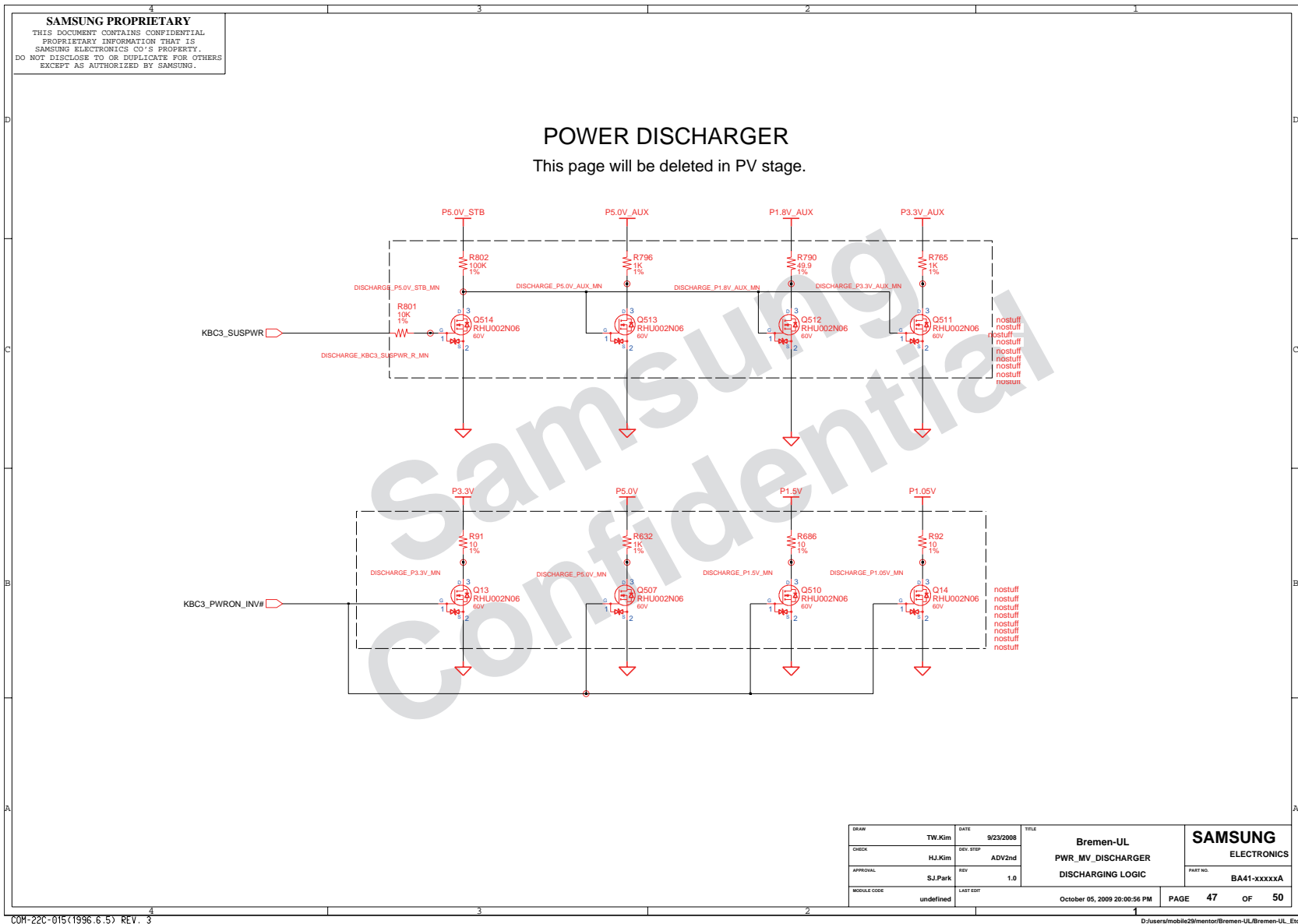
8. Block Diagram and Schematic



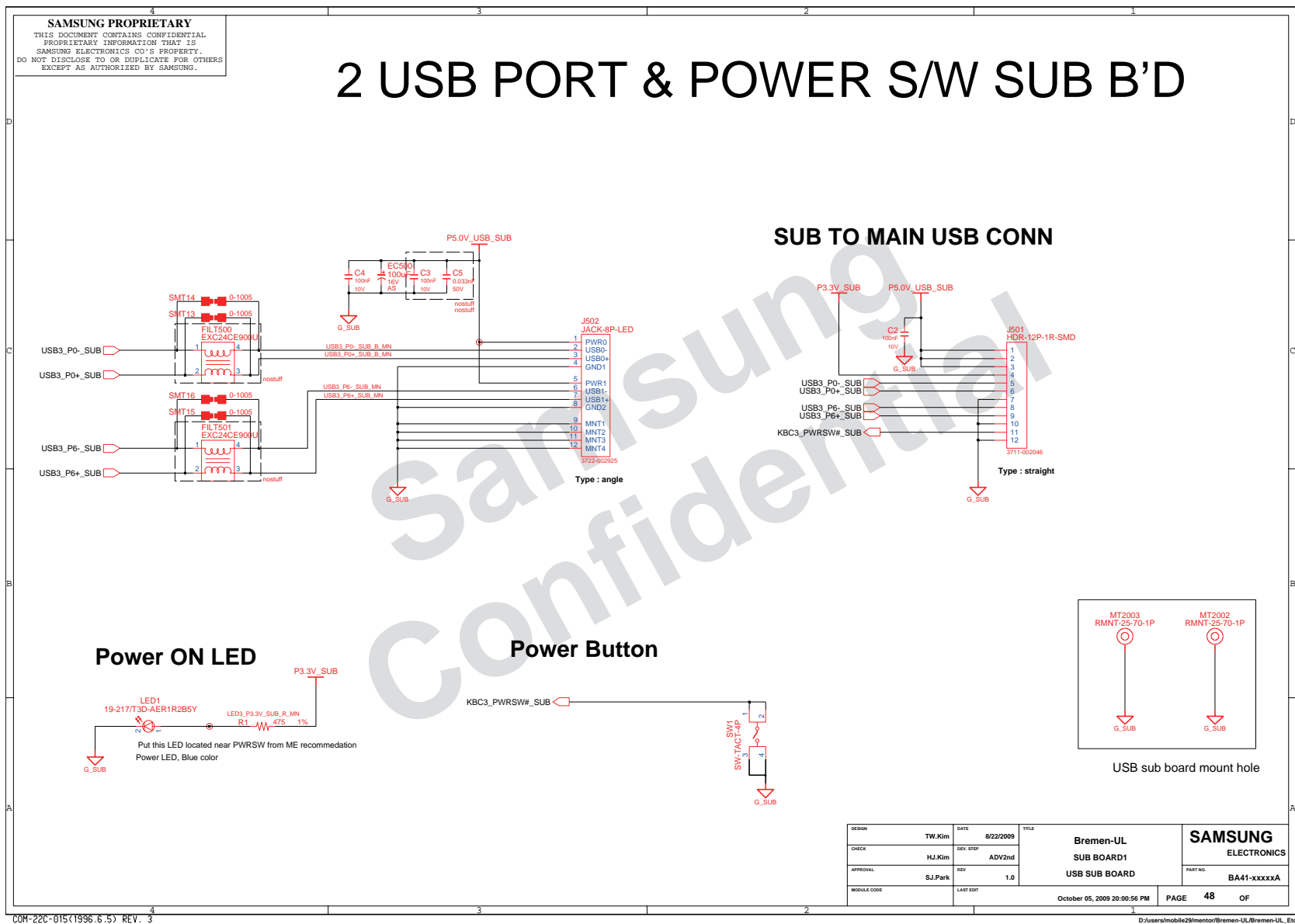
8. Block Diagram and Schematic



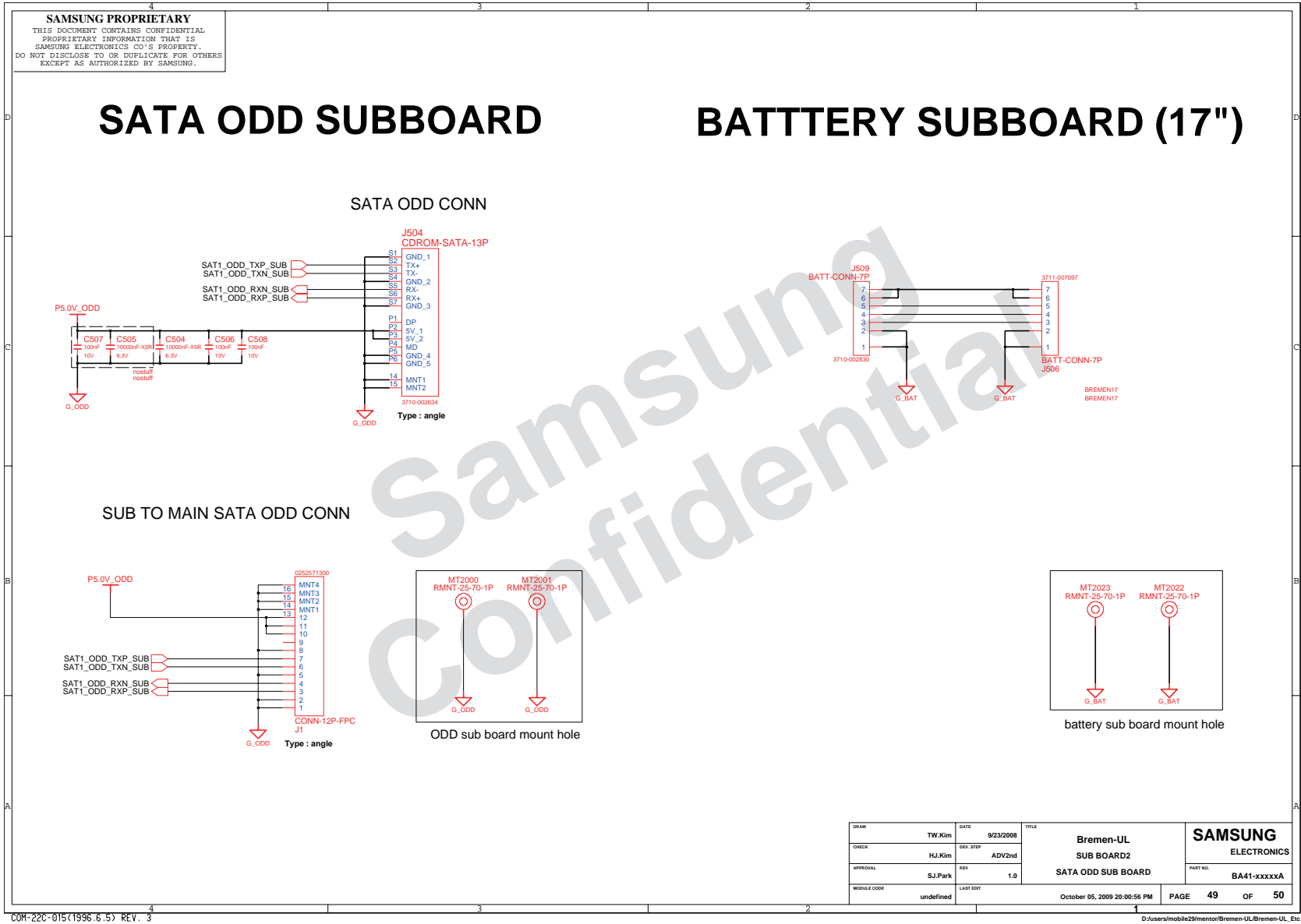
8. Block Diagram and Schematic



8. Block Diagram and Schematic



8. Block Diagram and Schematic



8. Block Diagram and Schematic

