Lenovo IdeaPad B570 Z570 V570

Sandy Bridge

Intel PCH Cougar Point

2011-01-19

REV : XXX

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX

BOM

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 1 of 102	

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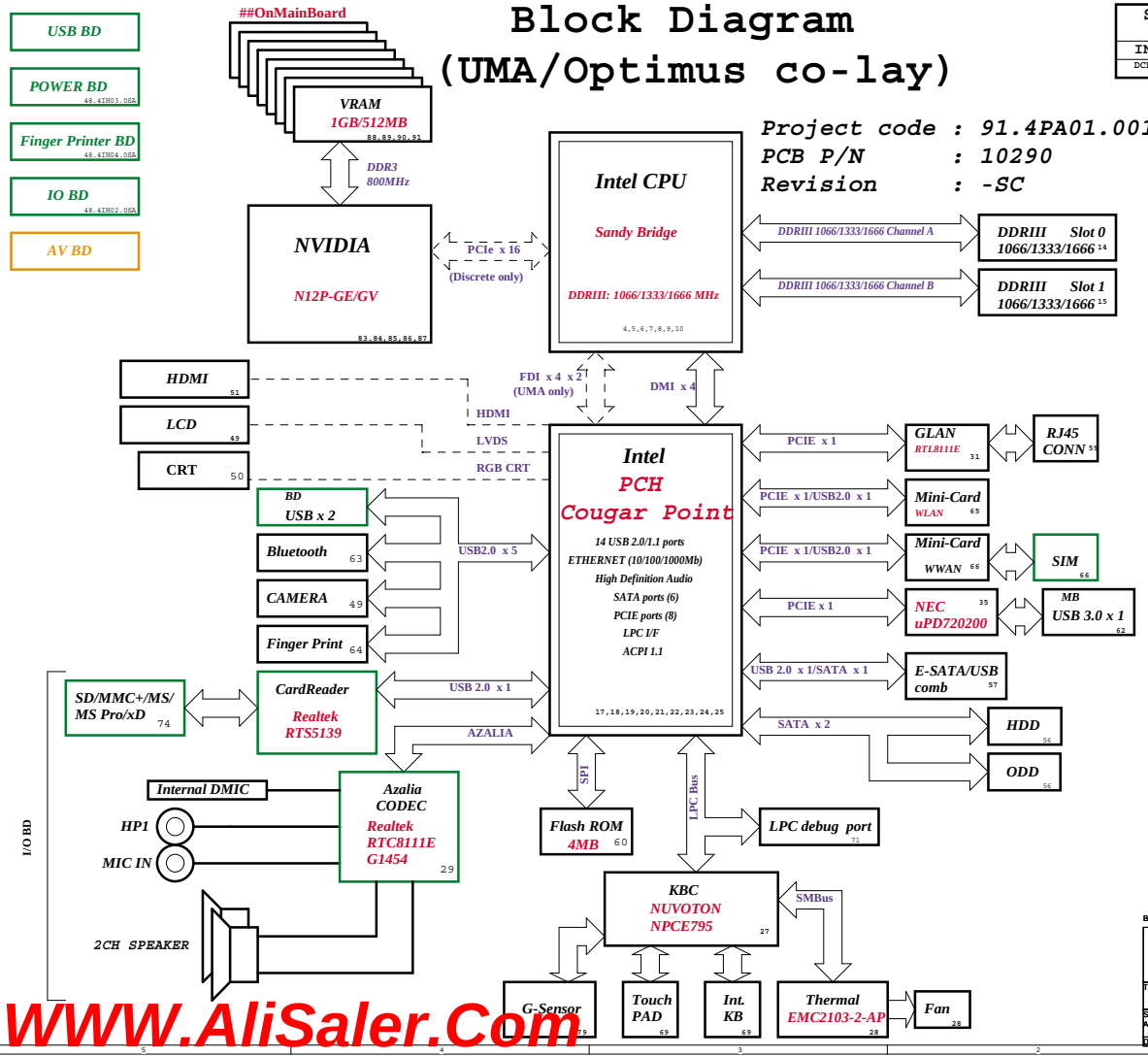
Block Diagram (UMA/Optimus co-lay)

Project code : 91.4PA01.001
PCB P/N : 10290
Revision : -SC



SYSTEM DC/DC RT8208B 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6111CQHC 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183AQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6111C 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

LDO RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5 3D3V_S0	1D5V_S5 1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

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Title: Block Diagram

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 2 of 102

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ ~~10 kΩ weak pull-up resistor~~
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	Dock Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	E-SATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	[illegible]
13	Mini Card1

SMBus ADDRESSES

I2 C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex	Bus
EC SMBus 1 Battery CHARGER			BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP			SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Title: Table of Content

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 3 of 102

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

CPU1A — SANDY — 1 OF 9

DMI: DMI_TXN[3:0] (B27, B25, A25, B24), DMI_TXP[3:0] (B28, B26, A24, B23), DMI_RXN[3:0] (G21, E22, F21, D21), DMI_RXP[3:0] (G22, D22, E20, C21)

FDI: FDI_TXN[7:0] (A21, H19, E19, F18, B21, C20, D18, E17), FDI_TXP[7:0] (A22, G19, E20, G18, B20, C19, D19, F17)

FDI_FSYNC0 J18, FDI_FSYNC1 J17, FDI_INT H20, FDI_LSYNC0 J19, FDI_LSYNC1 H17

eDP: DP_COMP A18, eDP_HPD B16, EDP_AUX C15, EDP_AUX# D15, EDP_TX0 C17, EDP_TX1 E16, EDP_TX2 C16, EDP_TX3 G15, EDP_TX#0 C18, EDP_TX#1 E16, EDP_TX#2 D16, EDP_TX#3 E15

PCI EXPRESS* - GRAPHICS: PEG_ICOMPI J22, PEG_ICOMPO J21, PEG_RCOMPO H22

PEG_RCOMP_R — R401 — 24D9R2F-L-GP — 1D05V_VTT

PEG_RXN[0..15] 83: PEG_RX#0 K33, PEG_RX#1 M35, PEG_RX#2 L34, PEG_RX#3 J35, PEG_RX#4 J32, PEG_RX#5 H34, PEG_RX#6 H31, PEG_RX#7 G33, PEG_RX#8 G30, PEG_RX#9 F35, PEG_RX#10 E34, PEG_RX#11 E32, PEG_RX#12 D33, PEG_RX#13 D31, PEG_RX#14 B33, PEG_RX#15 C32

PEG_RXP[0..15] 83: PEG_RX0 J33, PEG_RX1 L35, PEG_RX2 K34, PEG_RX3 H35, PEG_RX4 H32, PEG_RX5 G34, PEG_RX6 G31, PEG_RX7 F33, PEG_RX8 F30, PEG_RX9 E35, PEG_RX10 E33, PEG_RX11 E32, PEG_RX12 D34, PEG_RX13 E31, PEG_RX14 C33, PEG_RX15 B32

PEG_TXN[0..15] 83: PEG_TX#0 M29, PEG_TX#1 M32, PEG_TX#2 M31, PEG_TX#3 L32, PEG_TX#4 L29, PEG_TX#5 K31, PEG_TX#6 K28, PEG_TX#7 J30, PEG_TX#8 J28, PEG_TX#9 H29, PEG_TX#10 G27, PEG_TX#11 E29, PEG_TX#12 F27, PEG_TX#13 D28, PEG_TX#14 F26, PEG_TX#15 E25

PEG_TXP[0..15] 83: PEG_TX0 M28, PEG_TX1 M33, PEG_TX2 M30, PEG_TX3 L31, PEG_TX4 L28, PEG_TX5 K30, PEG_TX6 K27, PEG_TX7 J29, PEG_TX8 J27, PEG_TX9 H28, PEG_TX10 G28, PEG_TX11 E28, PEG_TX12 F28, PEG_TX13 D27, PEG_TX14 E26, PEG_TX15 D25

C401	SCD1U10V2KX-5GP	PEG_TXN15	PEG_TXN15
C402	SCD1U10V2KX-5GP	PEG_TXN14	PEG_TXN14
C403	SCD1U10V2KX-5GP	PEG_TXN13	PEG_TXN13
C404	SCD1U10V2KX-5GP	PEG_TXN12	PEG_TXN12
C405	SCD1U10V2KX-5GP	PEG_TXN11	PEG_TXN11
C406	SCD1U10V2KX-5GP	PEG_TXN10	PEG_TXN10
C407	SCD1U10V2KX-5GP	PEG_TXN9	PEG_TXN9
C408	SCD1U10V2KX-5GP	PEG_TXN8	PEG_TXN8
C409	SCD1U10V2KX-5GP	PEG_TXN7	PEG_TXN7
C410	SCD1U10V2KX-5GP	PEG_TXN6	PEG_TXN6
C411	SCD1U10V2KX-5GP	PEG_TXN5	PEG_TXN5
C412	SCD1U10V2KX-5GP	PEG_TXN4	PEG_TXN4
C413	SCD1U10V2KX-5GP	PEG_TXN3	PEG_TXN3
C414	SCD1U10V2KX-5GP	PEG_TXN2	PEG_TXN2
C415	SCD1U10V2KX-5GP	PEG_TXN1	PEG_TXN1
C416	SCD1U10V2KX-5GP	PEG_TXN0	PEG_TXN0
C417	SCD1U10V2KX-5GP	PEG_TXP15	PEG_TXP15
C418	SCD1U10V2KX-5GP	PEG_TXP14	PEG_TXP14
C419	SCD1U10V2KX-5GP	PEG_TXP13	PEG_TXP13
C420	SCD1U10V2KX-5GP	PEG_TXP12	PEG_TXP12
C421	SCD1U10V2KX-5GP	PEG_TXP11	PEG_TXP11
C422	SCD1U10V2KX-5GP	PEG_TXP10	PEG_TXP10
C423	SCD1U10V2KX-5GP	PEG_TXP9	PEG_TXP9
C424	SCD1U10V2KX-5GP	PEG_TXP8	PEG_TXP8
C425	SCD1U10V2KX-5GP	PEG_TXP7	PEG_TXP7
C426	SCD1U10V2KX-5GP	PEG_TXP6	PEG_TXP6
C427	SCD1U10V2KX-5GP	PEG_TXP5	PEG_TXP5
C428	SCD1U10V2KX-5GP	PEG_TXP4	PEG_TXP4
C429	SCD1U10V2KX-5GP	PEG_TXP3	PEG_TXP3
C430	SCD1U10V2KX-5GP	PEG_TXP2	PEG_TXP2
C431	SCD1U10V2KX-5GP	PEG_TXP1	PEG_TXP1
C432	SCD1U10V2KX-5GP	PEG_TXP0	PEG_TXP0

1D05V_VTT — R402 — 24D9R2F-L-GP — DY; R403 — Do Not Stuff

62.10055.321

delete R404&RN 401 @20100630

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Title	CPU (PCIE/DMI/FDI)	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 4 of 102	

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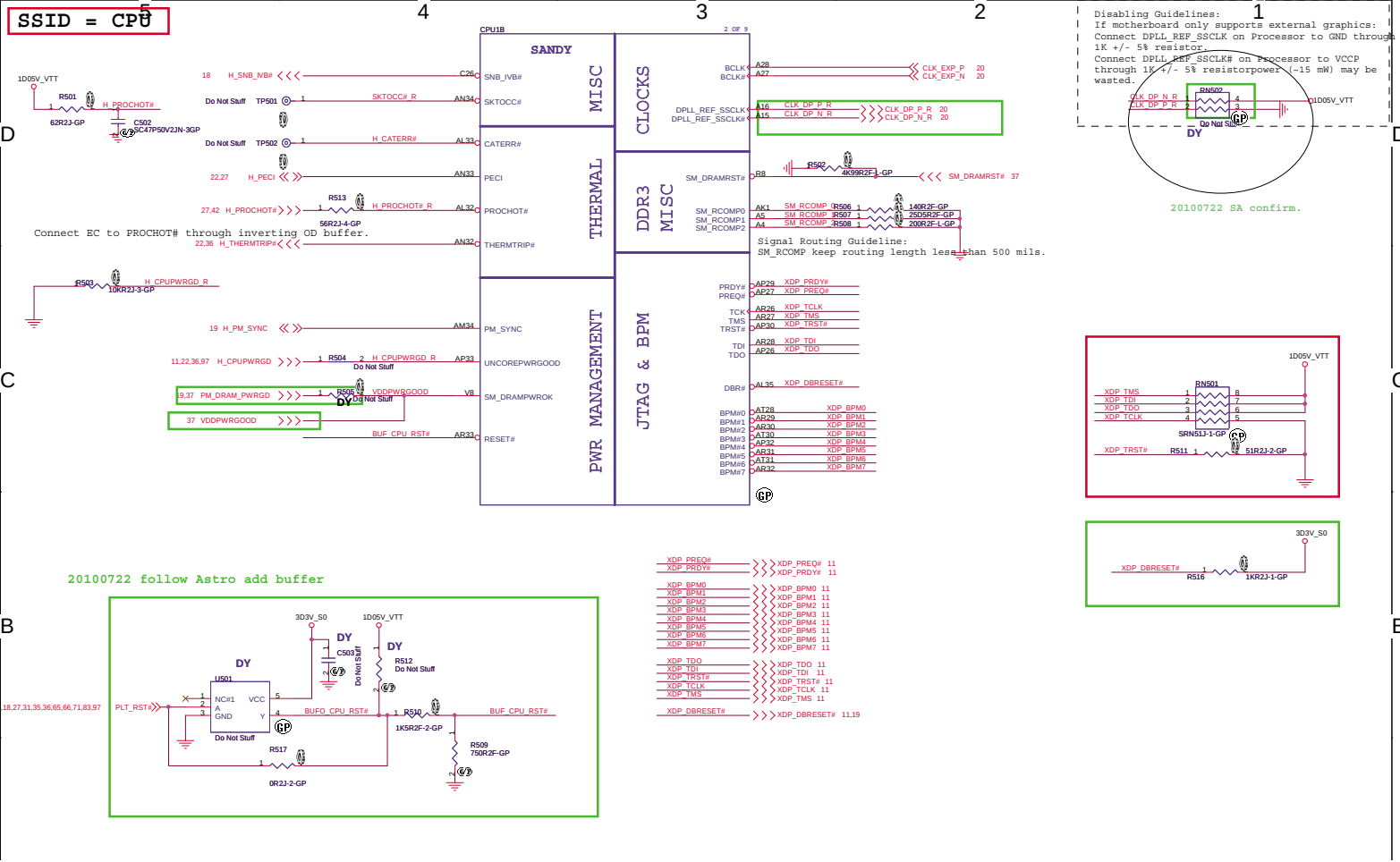
SSID = CPU



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Title	CPU (THERMAL/CLOCK/PM)
Size A3	Document Number LZ57 Rev -1
Date: Tuesday, March 29, 2011	Sheet 5 of 102

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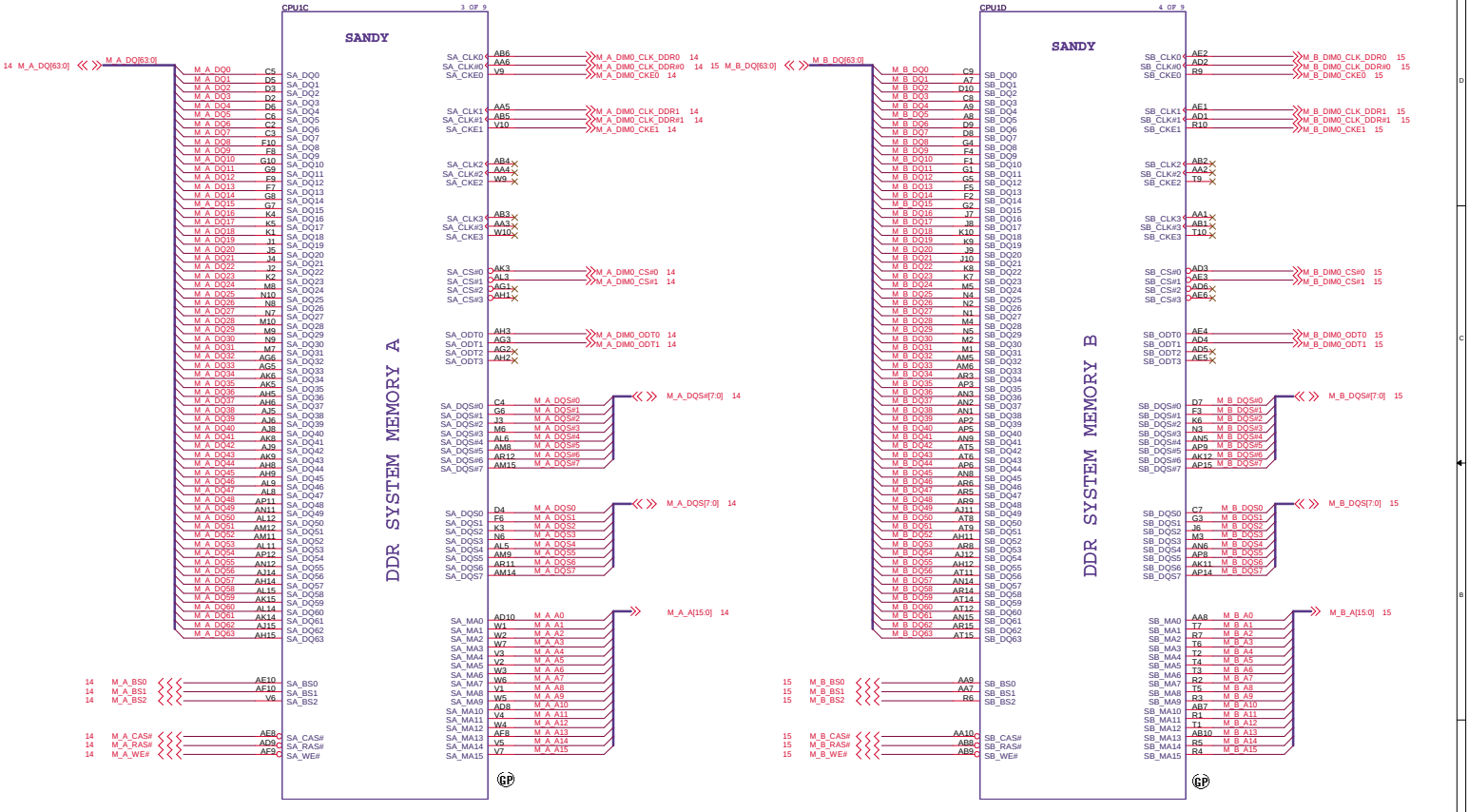
SSID = CPU



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Title	CPU (DDR)	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 6 of 102	

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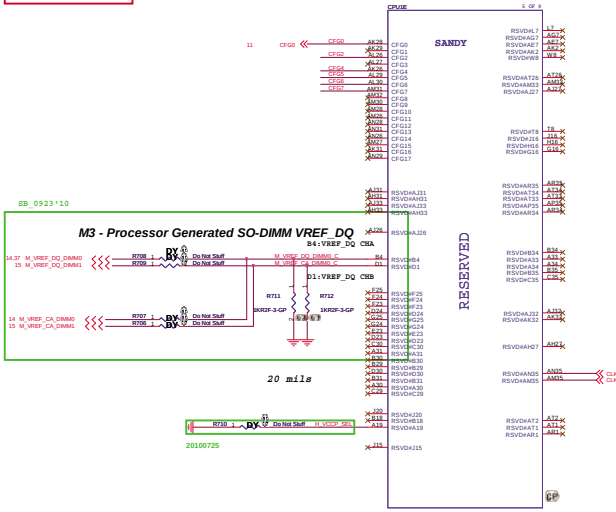
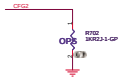
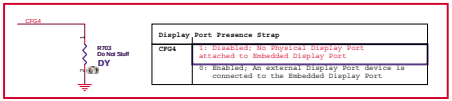
SSID = CPU

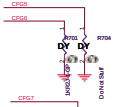




PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled , function 2 disabled
	01: Reserved - (Device 1 function 1 disabled , function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

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Title: CPU (RESERVED)

Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 26, 2013 Sheet 7 of 180

SSID = CPU

POWER

CPU1F — 6 OF 9 — SANDY

PROCESSOR CORE POWER

53A

VCC_CORE

C801 C802 C803 C804 C811 — SC10U6D3V5K-1GP

C815 C817 C818 C819 C820 — SC10U6D3V5K-1GP

C816 C821 C822 C823 C824 C825 C826 C827 — SC10U6D3V5K-1GP

C837 C836 C835 C834 C833 C832 C831 C828 — SC10U6D3V5K-1GP

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AE35 AE34 AE33 AE32 AE31 AE30 AE29 AE28 AE27 AE26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26 — VCC

CORE SUPPLY

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

C805 C806 C807 C808 C809 C810 C838 C839 C840 C841 — SC10U6D3V5K-1GP; C806, C808, C810, C839 DY; C808 Do Not Stuff

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

C812 C813 C814 C829 C830 C842 C843 C844 C845 — SC10U6D3V5K-1GP; C812, C845 DY; C812, C845 Do Not Stuff

PEG AND DDR

R804 need to close to CPU

1D05V_VTT

H_CPU_SVIDDAT — R804 — 130R2F-1-GP

S-HS_20100610 V1.0

SVID

VIDALERT# — AJ29 — H_CPU_SVIDALRT# — R803 — 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK — AJ30 — H_CPU_SVIDCLK — H_CPU_SVIDCLK 42
VIDSOUT — AJ28 — H_CPU_SVIDDAT — H_CPU_SVIDDAT 42

SENSE LINES

VCC_CORE

R801, R802 need to close to CPU

R801 100R2F-L1-GP-U

VCC_SENSE — AJ35 — VCCSENSE 42
VSS_SENSE — AJ34 — VSSSENSE 42

R802 100R2F-L1-GP-U

VCCIO_SENSE — B10 — VCCIO_SENSE 45
VSSIO_SENSE — A10 — VSSIO_SENSE 45

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Title: CPU (VCC_CORE)

Size: Custom | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 8 of 102

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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

POWER

CPU1G — 7 OF 9

SANDY GRAPHICS

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 Do Not Stuff, C902 SC10U6D3V5KX-1GP, C903 Do Not Stuff, C904 SC10U6D3V5KX-1GP, C905 SC10U6D3V5KX-1GP, C906 SC10U6D3V5KX-1GP, C907 SC10U6D3V5KX-1GP, C908 SC10U6D3V5KX-1GP, C918 SC10U6D3V5KX-1GP, C919 SC10U6D3V5KX-1GP, C920 SC10U6D3V5KX-1GP, C921 SC10U6D3V5KX-1GP

VAXG: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17

SENSE LINES

VAXG_SENSE AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37

Close to CPU

VCC_GFXCORE — R906 100R2F-L1-GP-U — VCC_AXG_SENSE — R907 100R2F-L1-GP-U — VSS_AXG_SENSE

S-HR_20100609 V1.0

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

VDDQ: AF7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

C909 SC10U6D3V5KX-1GP, C910 SC10U6D3V5KX-1GP, C911 SC10U6D3V5KX-1GP, C912 Do Not Stuff, C913 Do Not Stuff, C914 SC10U6D3V5KX-1GP

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

C916 Do Not Stuff, C915 SC10U6D3V5KX-1GP, C917 SC10U6D3V5KX-1GP, TC903 ST330U2VDM-4-GP

VCCSA: M27, M26, L26, J26, J25, J24, H26, H25

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

TC902 ST330U2VDM-4-GP, C923 SC10U6D3V5KX-1GP, C922 SC1U3D3V5KX-1GP, C924 Do Not Stuff

VCCPLL: B6, A6, A2

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

MISC

0D85V_S0

R902 100R2F-L1-GP-U — Notice:pull-high 100k or 10k

VCCSA_SENSE H23 — VCCSA_SENSE — VCCSA_SENSE 48

FC_C22 C22 — H_FC_C22 — H_FC_C22 48
VCCSA_VID1 C24 — VCCSA_SEL — VCCSA_SEL 48

RN901 SRN1KJ-7-GP

20100721 standard schematic update

BOM

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Title: CPU (VCC_GFXCORE)

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 9 of 102

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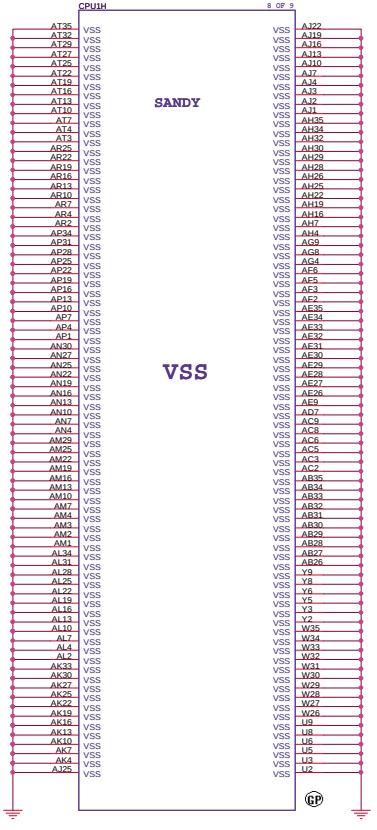
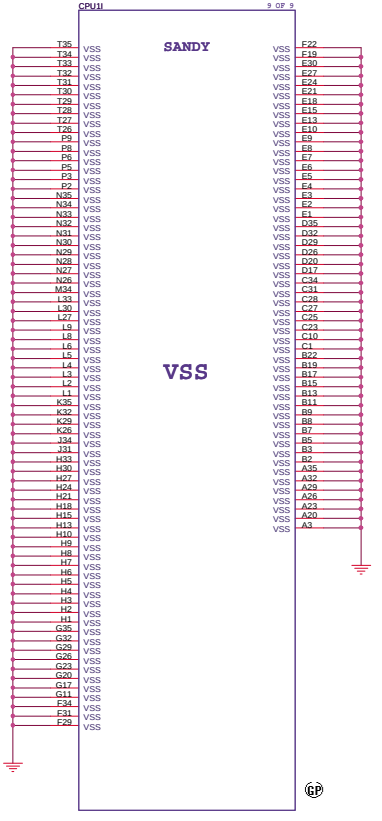
SSID = CPU





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Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VSS)	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 10 of 102	

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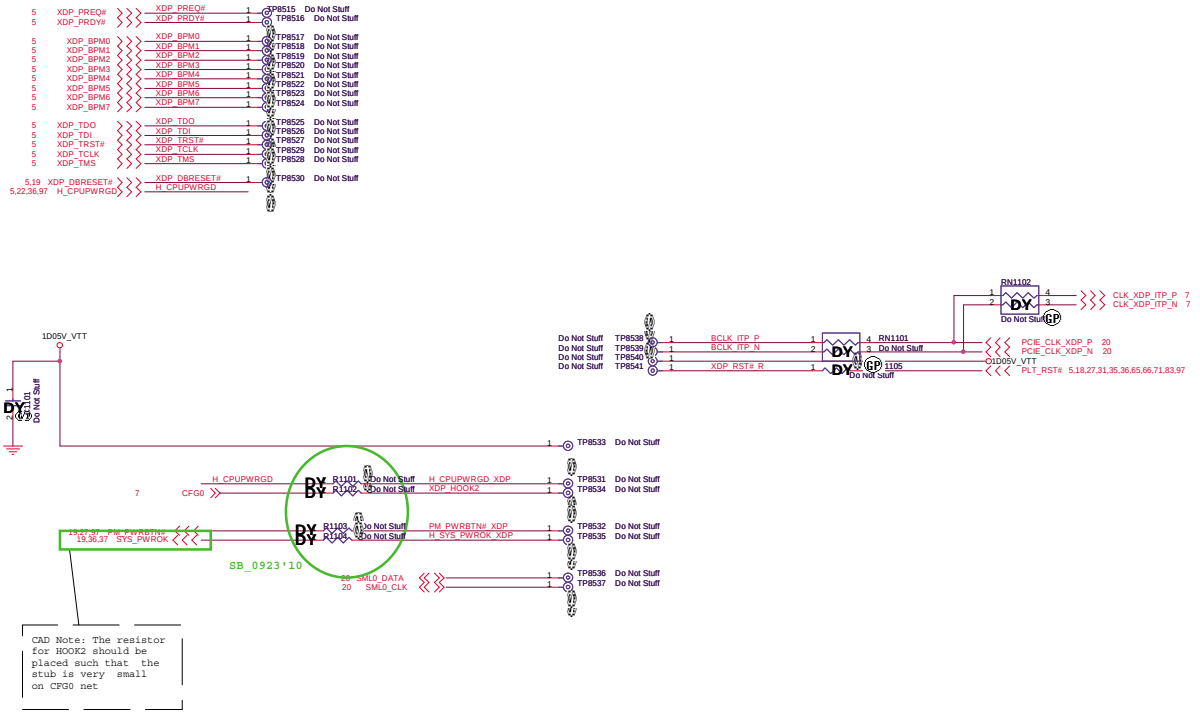

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Title	XDP	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 11 of 102	

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Title	***Reserved***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 12 of 102	

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Title	***Reserved***
Size A4	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 13 of 102

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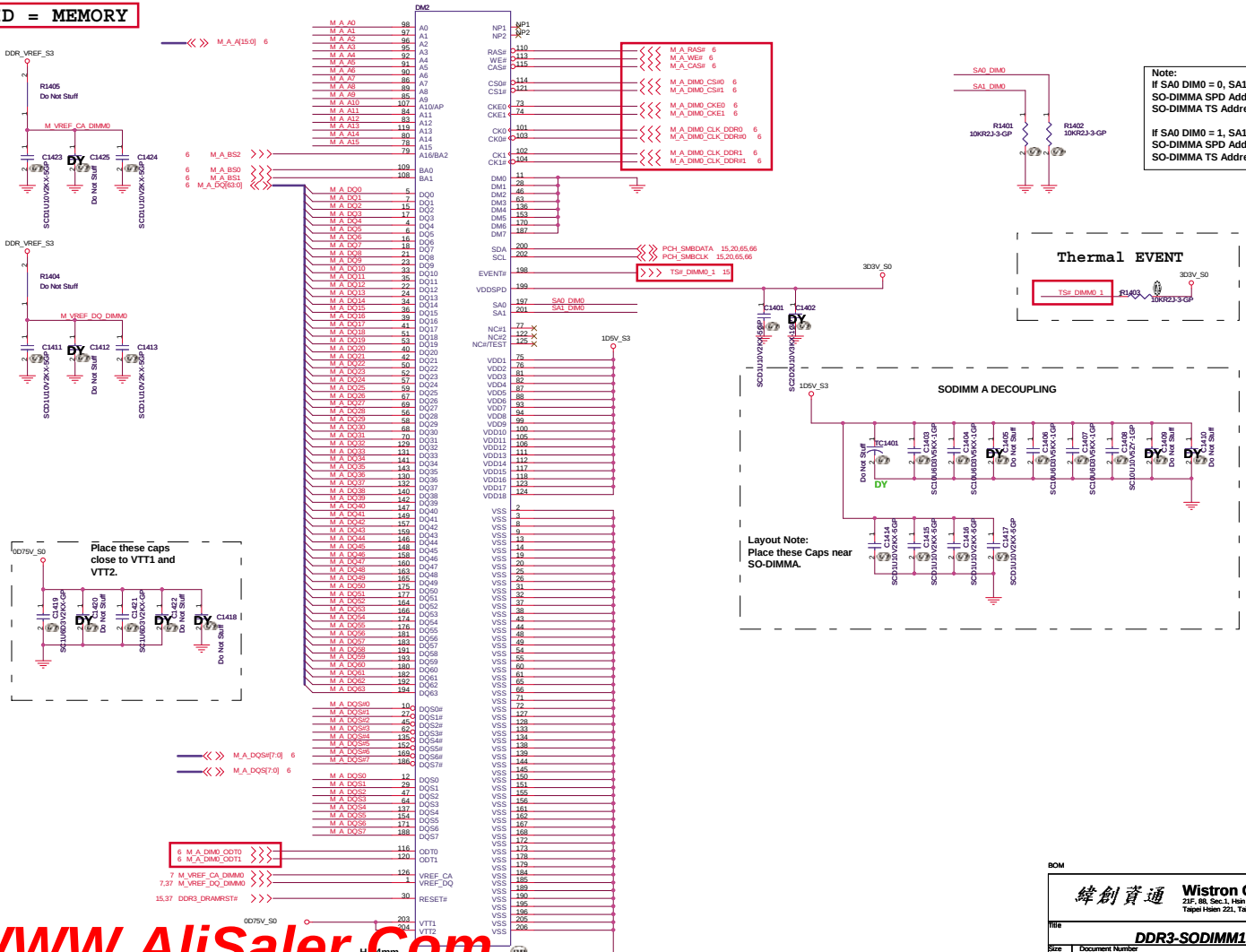
SSID = MEMORY



BOM

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Title: DDR3-SODIMM1

Size: Custom | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 14 of 102

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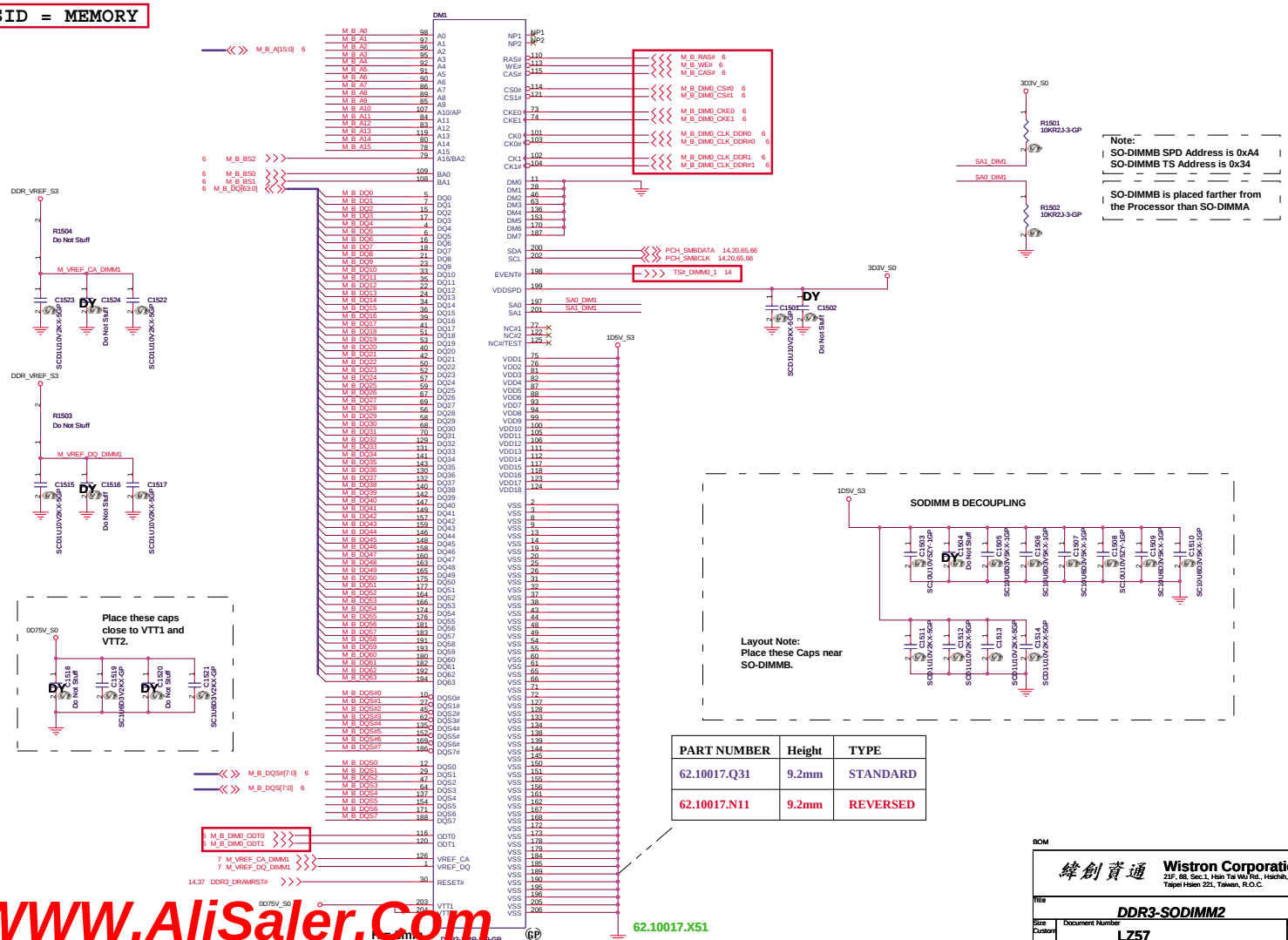
SSID = MEMORY



PART NUMBER	Height	TYPE
62.10017.Q31	9.2mm	STANDARD
62.10017.N11	9.2mm	REVERSED

BOM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 15 of 102

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Title: DDR3-SODIMM2

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 16 of 102

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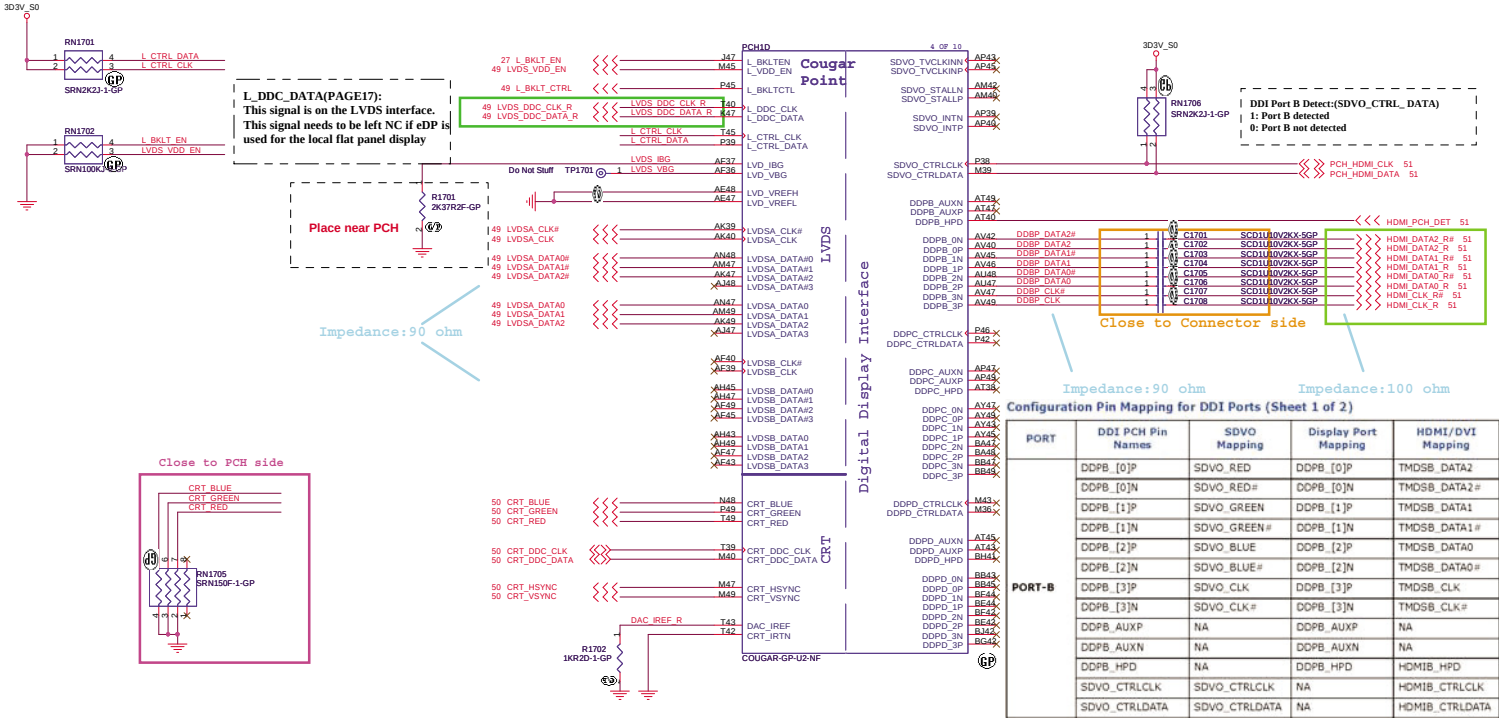

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

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Title: **PCH (LVDS/CRT/DDI)**

Size: A3 | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 17 of 102

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SSID = PCH

20100725 Annie modify

CRB : 2.2K
CEKLT: 1K

+V_NVRAM_VCCQ
R1808 2K2R2J-2-GP
NV_CLE 1 R1809 1K2R2J-1-GP H_SNB_IVB# 5

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

RN1801 SRN8K2J-2-GP
INT_PIRQA# 1 10 3D3V_S0
INT_PIRQE# 2 9 INT_PIRQH#
INT_PIRQC# 3 8 INT_PIRQG#
INT_PIRQB# 4 7 INT_PIRQD#
3D3V_S0 5 6 INT_PIRQF#

R1801 DY 1 Do Not Stuff PCI_GNT3#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

RN1803 SRN10KJ-5-GP
DGPU_HOLD_RST# 1 4
DGPU_PWR_EN# 2 3

C1802 DY Do Not Stuff
C1803 DY Do Not Stuff
BBS_BIT1
BBS_BIT0 21

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

3D3V_S0
R1814 DY Do Not Stuff
INT_PIRQA# INT_PIRQB# INT_PIRQC# INT_PIRQD#
93 DGPU_HOLD_RST# Do Not Stuff TP1805
93 DGPU_PWR_EN# Do Not Stuff TP1804
DGPU_SELECT#
DGPU_PWR_EN#
DGPU_PWM_SELECT# BBS_BIT1
Do Not Stuff TP1801 1 PCI_GNT3#

SC_1026'10
78 dGPU_LED 1 R1818 Do Not Stuff
27,56 SATA_ODD_DAA_SMI# 1 R1813 Do Not Stuff
35 USB30_SMI# 1 R1815 0R2J-2-GP
49 DCR_EN# Do Not Stuff
Do Not Stuff
R1817 Do Not Stuff
Do Not Stuff TP1802 1 PCI_PME#
PCI_PLTRST#
INT_PIRQE# INT_PIRQF# INT_PIRQG# INT_PIRQH#

SC_1025'10
65,71 CLK_PCI_LPC R1804 1 22R2J-2-GP CLK_PCI_LPC_R
20 CLK_PCI_FB R1805 1 22R2J-2-GP CLK_PCI_FB_R
27 CLK_PCI_KBC R1806 1 22R2J-2-GP CLK_PCI_KBC_R
EC1802 DY Do Not Stuff
EC1801 DY Do Not Stuff
KBC CLK EMI

3D3V_S0
U1801 VCC B A Y GND
DY Do Not Stuff
Do Not Stuff
27,31,35,36,65,66,71,83,97 PLT_RST#
PCI_PLTRST#
R1807 0R2J-2-GP
C1802 DY Do Not Stuff
R1816 DY Do Not Stuff
C1801 DY Do Not Stuff
20100629

PCH1E 5 OF 10
Cougar Point
RSVD
NVRAM
PCI
USB
COUGAR-GP-U2-NF

RSVD#AV5 NV_ALE
DF_TVS AY1 NV_CLE
RSVD#AV10 AV10 NV_RCOMP 1 TP1803 Do Not Stuff

+V_NVRAM_VCCQ
Danbury Technology:
Disabled when Low.
Enable when High.
R1810 DY Do Not Stuff
NV_ALE

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	X
1	USB Ext. port 1 (Left Side)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	E-SATA /USB Ext. port 4
9	USB Ext. port 2(CardReader BD
10	USB Ext. port 3(RJ45_BD)
11	Mini Card1 (WLAN)
12	CAMERA
13	X

USB_PN1 62 USB_PP1 62
USB_PN2 64 USB_PP2 64
USB_PN3 63 USB_PP3 63
USB_PN4 66 USB_PP4 66
USB_PN5 82 USB_PP5 82
USB_PN8 57 USB_PP8 57
USB_PN9 82 USB_PP9 82
USB_PN10 82 USB_PP10 82
USB_PN11 65 USB_PP11 65
USB_PN12 49 USB_PP12 49
USB_RBIAS 1 R1811 22D6R2F-L1-GP

SW programing USB_OC#12_13 for USB 9

USB_OC#0 1 USB_OC#0_1 62
USB_OC#2 3
USB_OC#4 5
USB_OC#6 7
USB_OC#8 9 USB_OC#8_9 62
USB_OC#10 11 USB_OC#10_11 61
USB_OC#12 13 USB_OC#12_13 61
PCH_GPIO14

R1820 0R2J-2-GP LZ57 6L -1_1209'10

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

RN1802 SRN10KJ-L3-GP
USB_OC#2 3 1 10 3D3V_S5
USB_OC#4 5 2 9 USB_OC#12 13
USB_OC#6 7 3 8 USB_OC#8 9
USB_OC#10 11 4 7 PCH_GPIO14
3D3V_S5 5 6 USB_OC#0 1

BOM

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Title	PCH (PCI/USB/NVRAM)	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 18 of 102	

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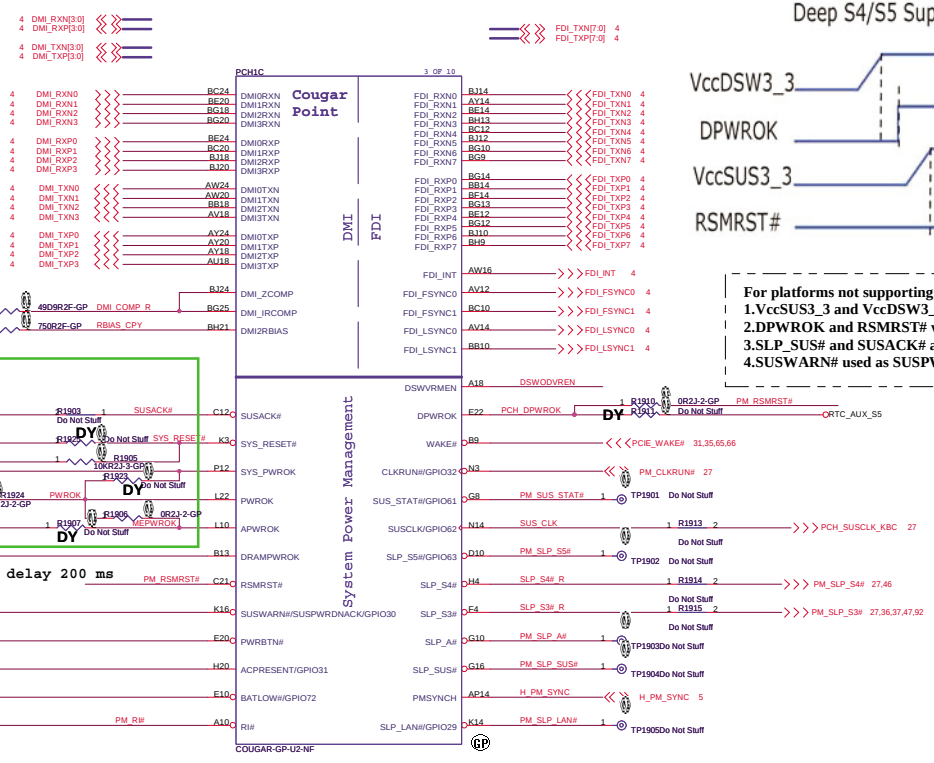
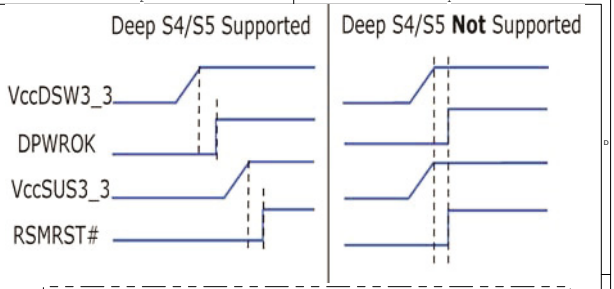
SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

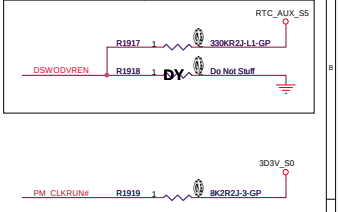


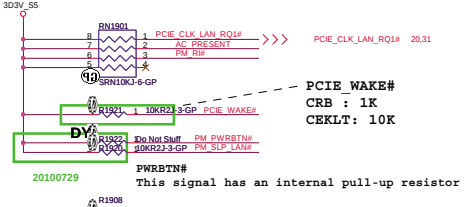
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms



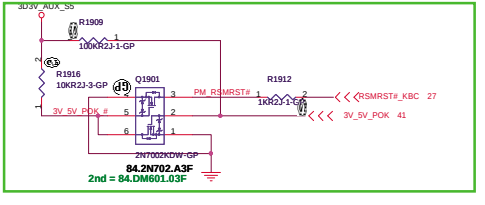
For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled





PCIE_WAKE#
CRB : 1K
CEKLT: 10K



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCH (DM I/FDI/PM)	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 19 of 102	

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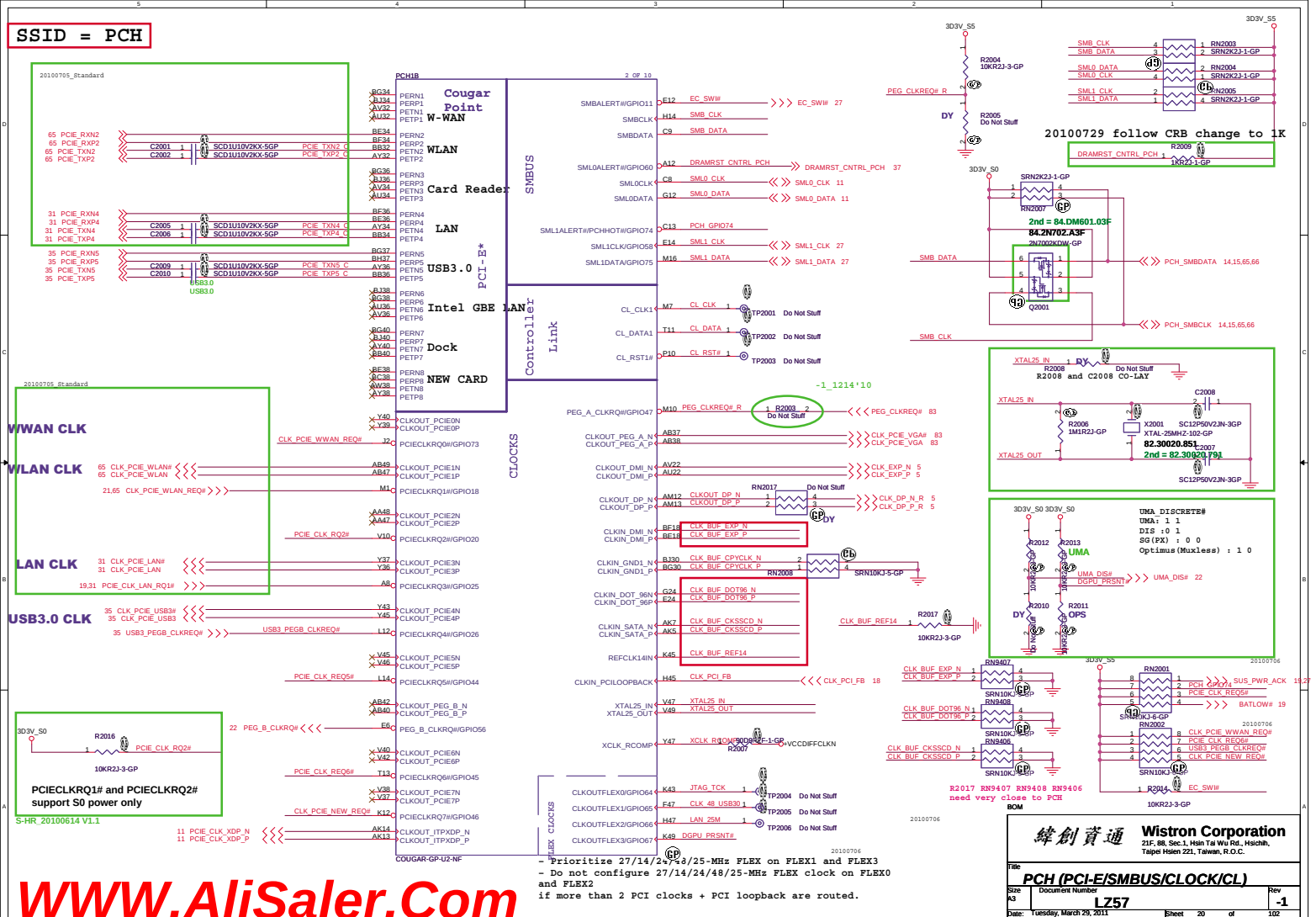
SSID = PCH



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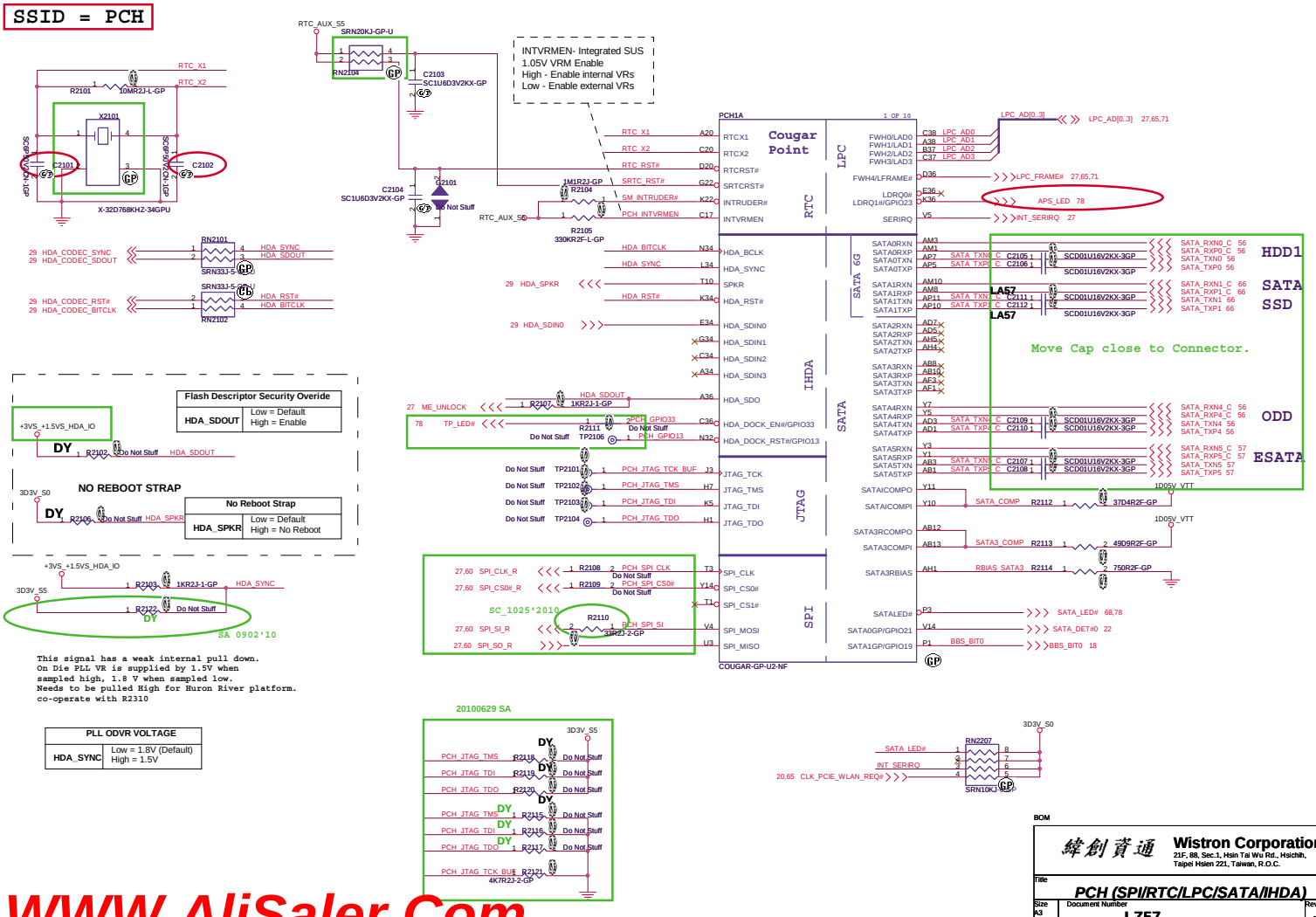
SSID = PCH



BOM

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Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size: A3 | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 21 of 102

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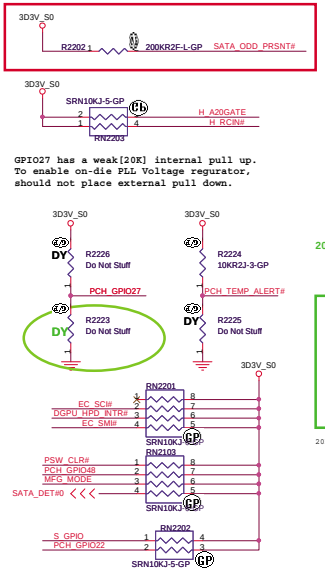
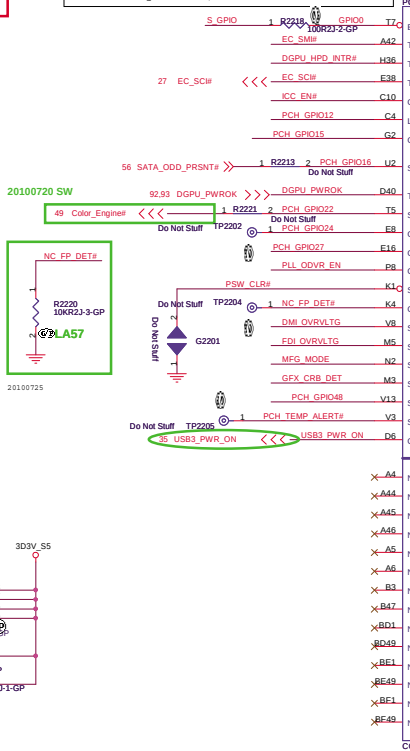
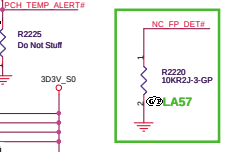
SSID = PCH

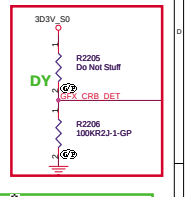
Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY









SB 0923'10

PCH_THERMTRIP_R R2222 1 01D05V_VTT
DY
Do Not Stuff

20100729 follow Annie CRB

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

BOM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 22 of 102

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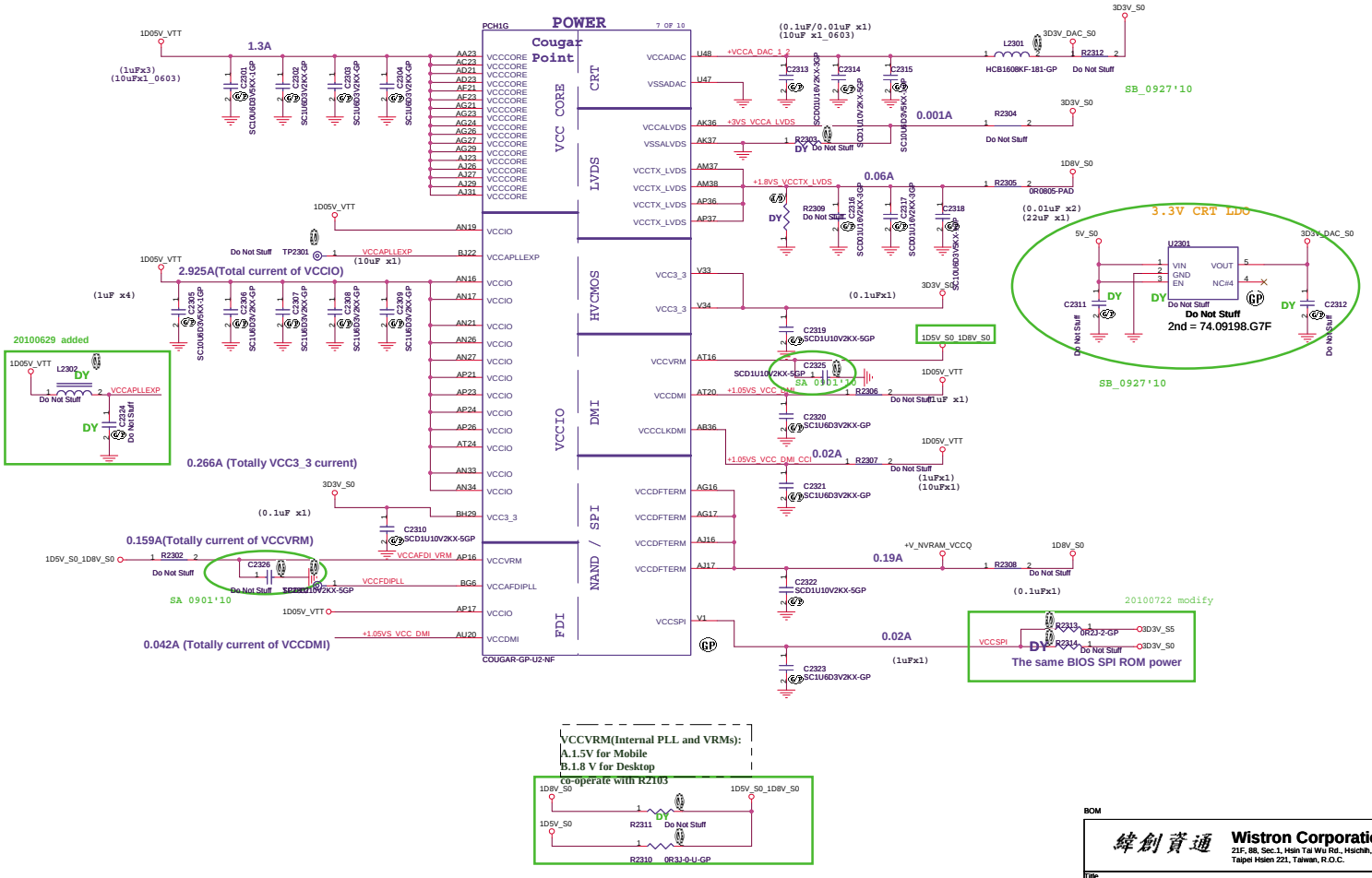
SSID = PCH 6A



BOM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER1)**

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 23 of 102

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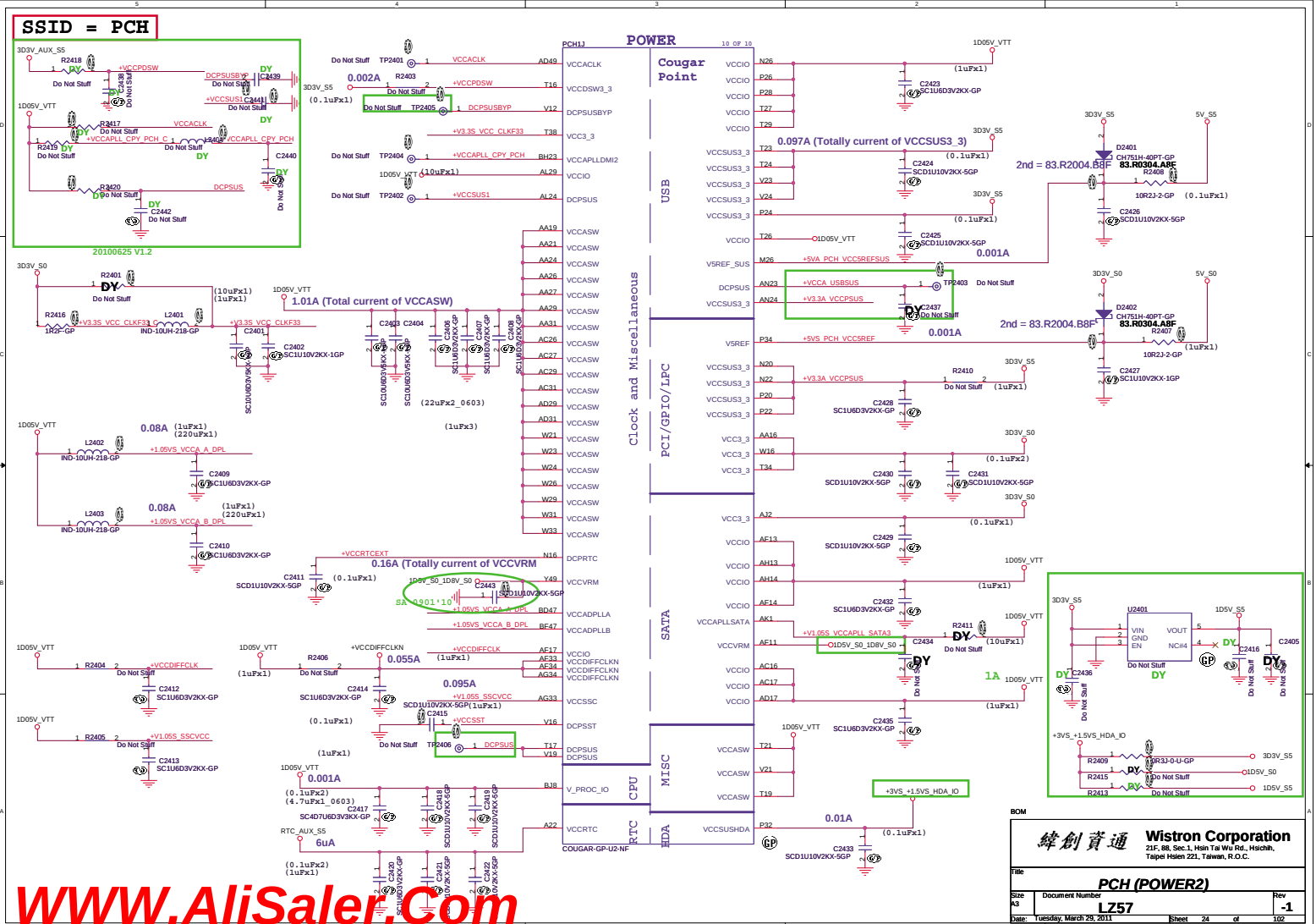


BOM

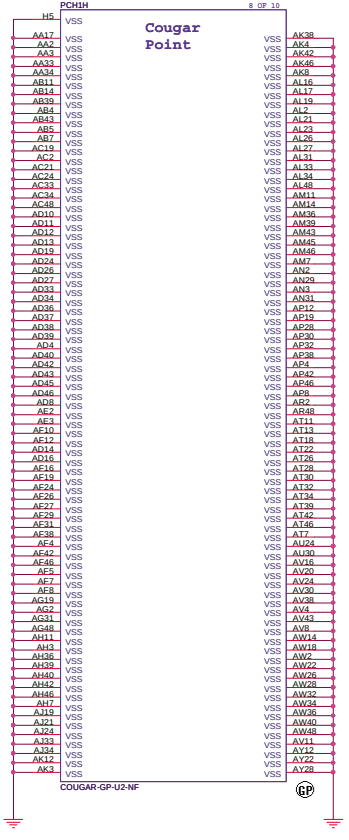
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

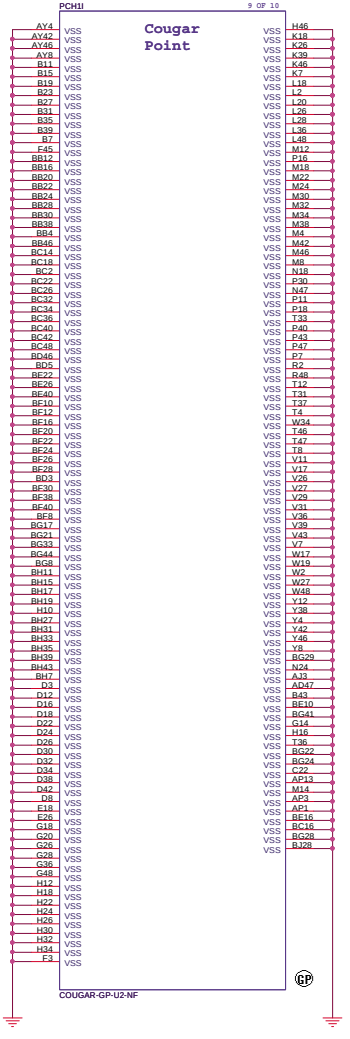
Title: PCH (POWER2)

Size: A3 | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 24 of 102

SSID = PCH





BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PCH (VSS)***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 25 of 102	

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 26 of 102

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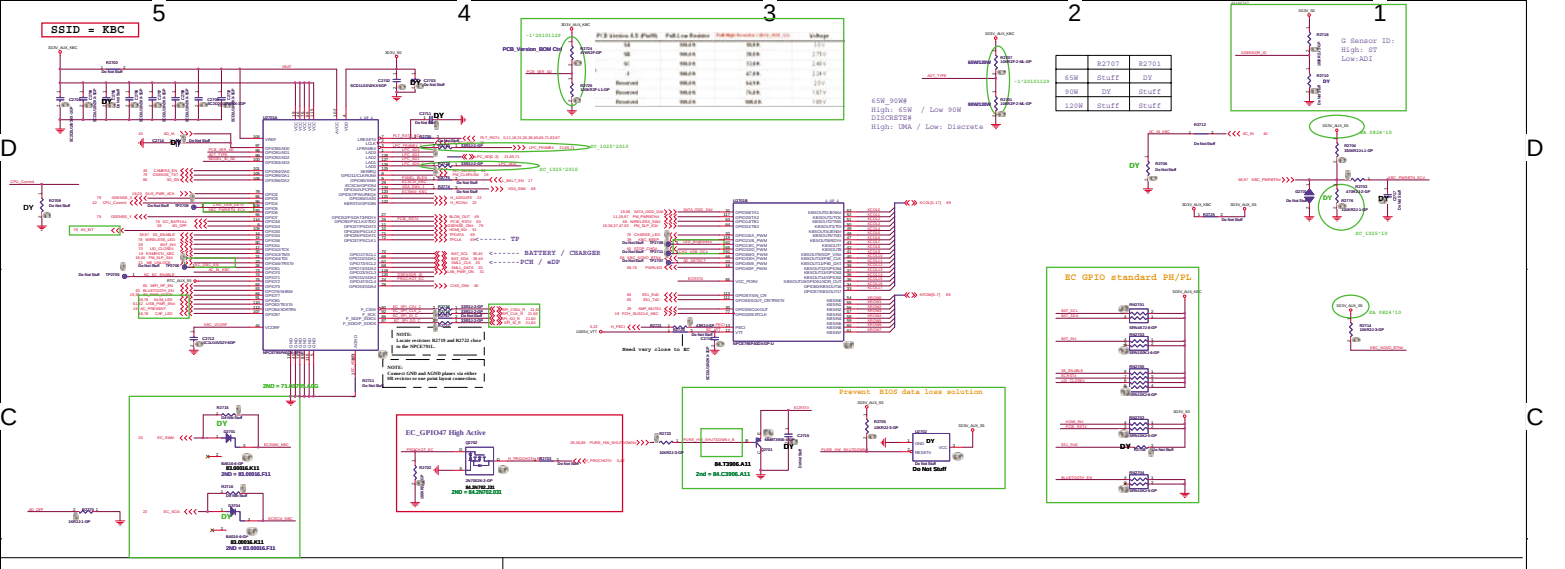

	R2707	R2701
65W	Stuff	DY
90W	DY	Stuff
120W	Stuff	Stuff

LILI Multi GPIO setting

Model_ID_ROM Ctrl OPS: 64.14335.6DL

MODEL_ID_AD(Pin100)	Pull-Low Register	Pull-High Register	Voltage
V/W S7 UMA	100.0 K	64.9 K	2.001 V
V/W S7 OPTIMUS	100.0 K	76.8 K	1.847 V
Z S7 UMA	100.0 K	100.0 K	1.650 V
Z S7 OPTIMUS	100.0 K	143.0 K(64.14335.L0L)	1.32 V

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Taipei Hsien 221, Taiwan, R.O.C.

KBC Nuvoton NPCE785

L257 -1

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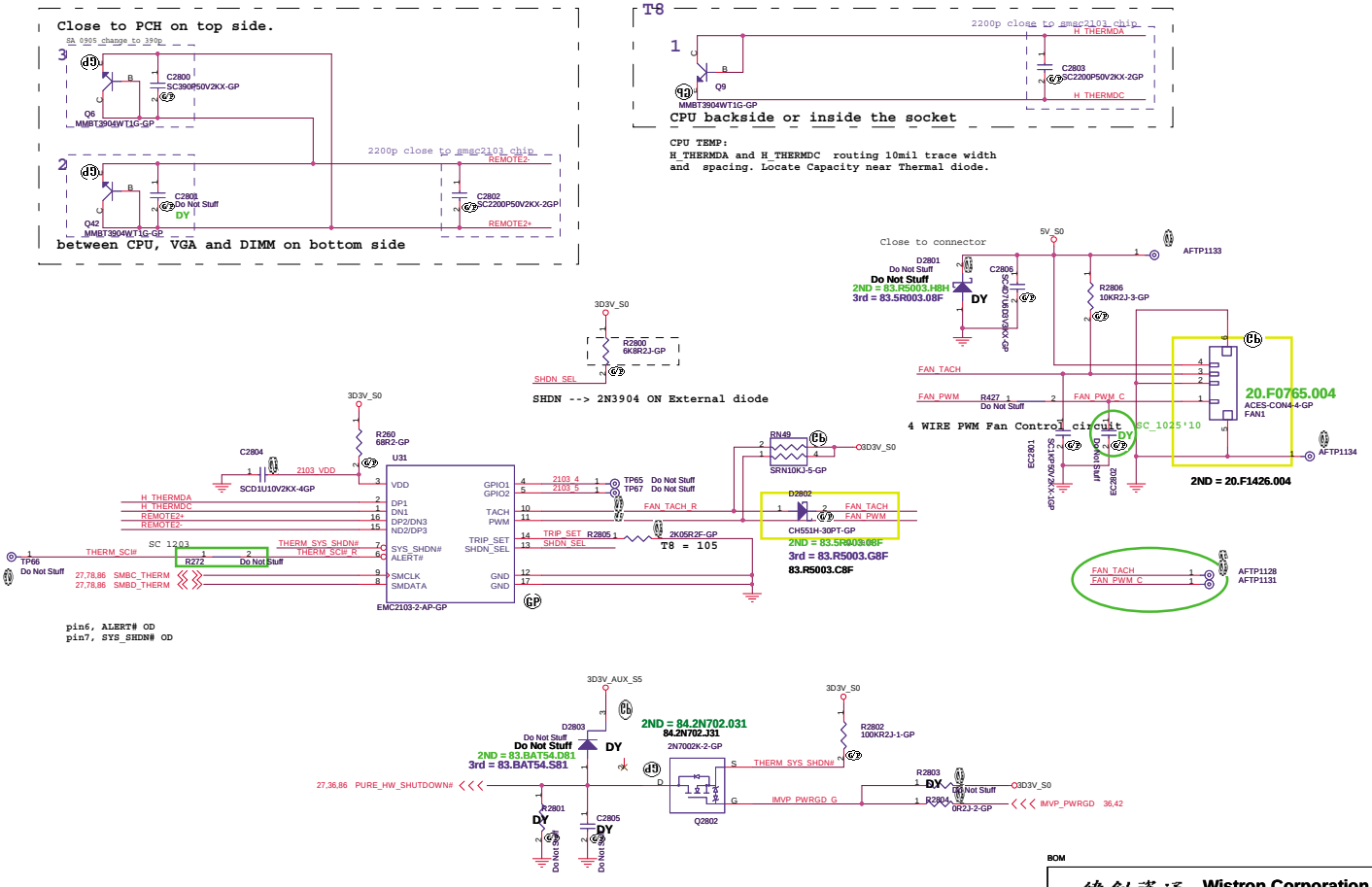
SSID = Thermal

Thermal sensor



BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 28 of 102

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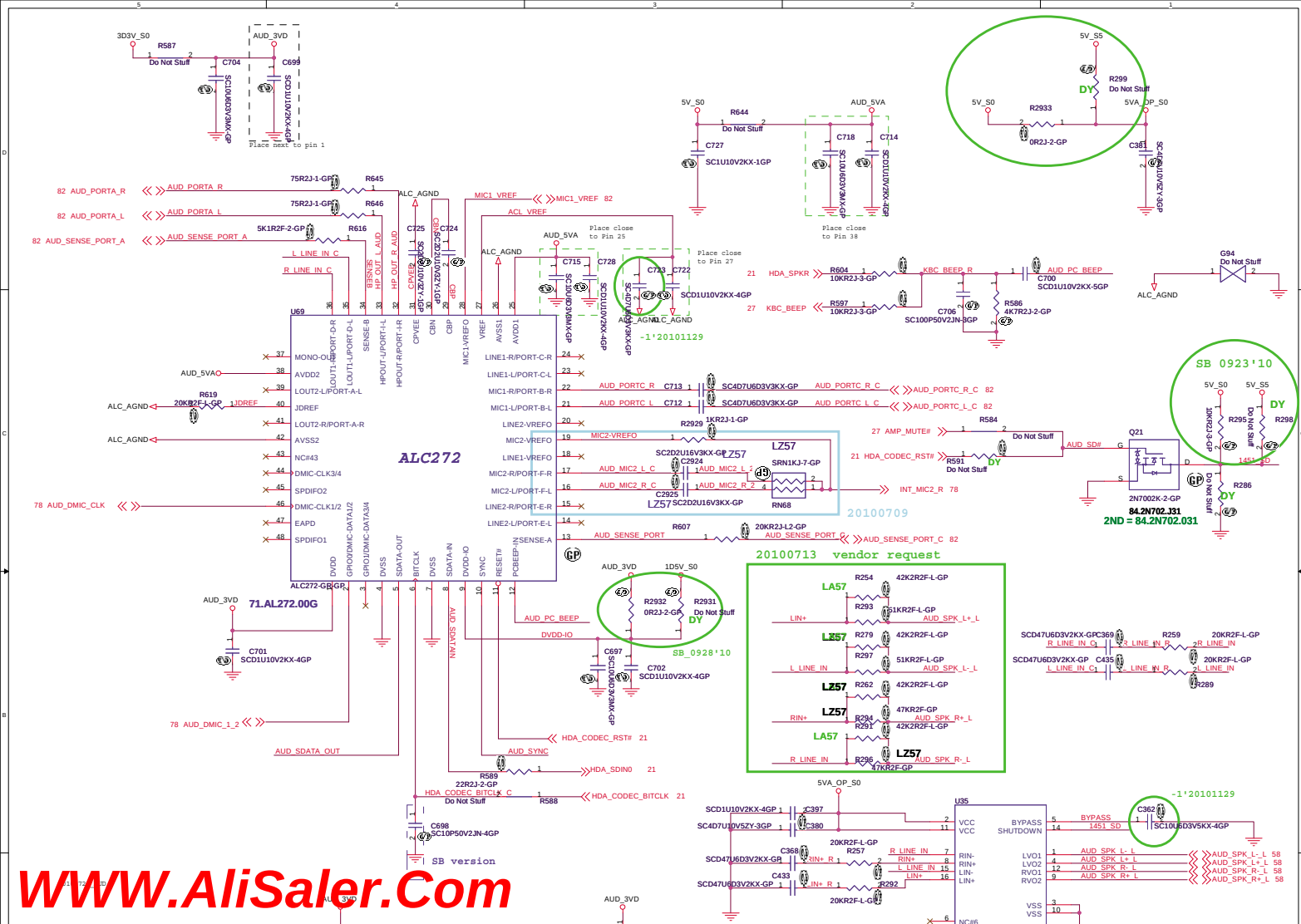
ALC272
U69
ALC272-GR-GP
71.AL272.00G
20100713 vendor request
20100709
SB 0923'10
SB_0928'10
SB version
-1'20101129
84.2N702.J31
2ND = 84.2N702.031
U35
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blanking

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***reserved***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 30 of 102

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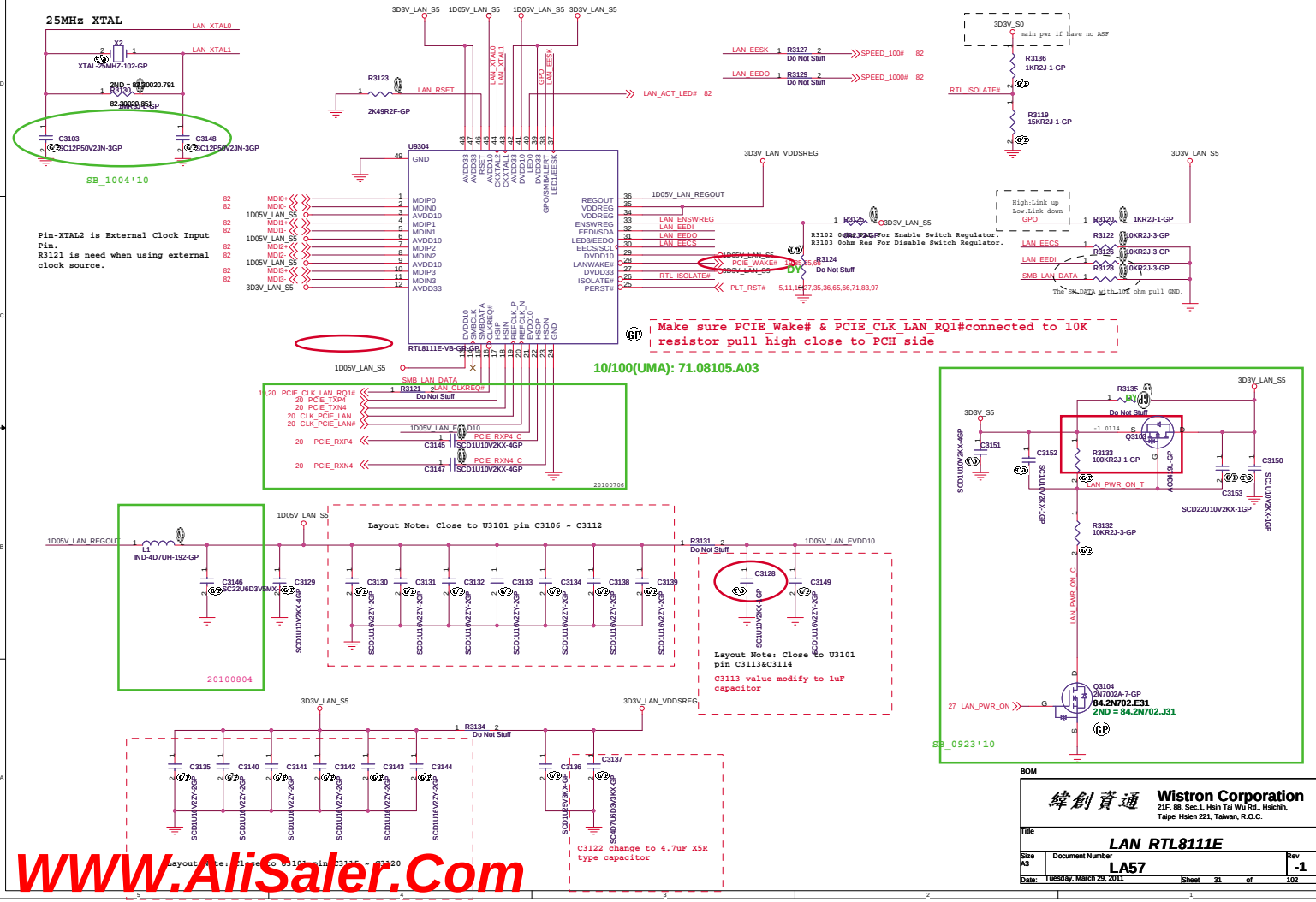

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BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RTS5159 (CARD READER)***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 32 of 102	

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BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **LZ57**
Rev	**-1**
Date: Tuesday, March 29, 2011	Sheet 33 of 102

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BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 34 of 102

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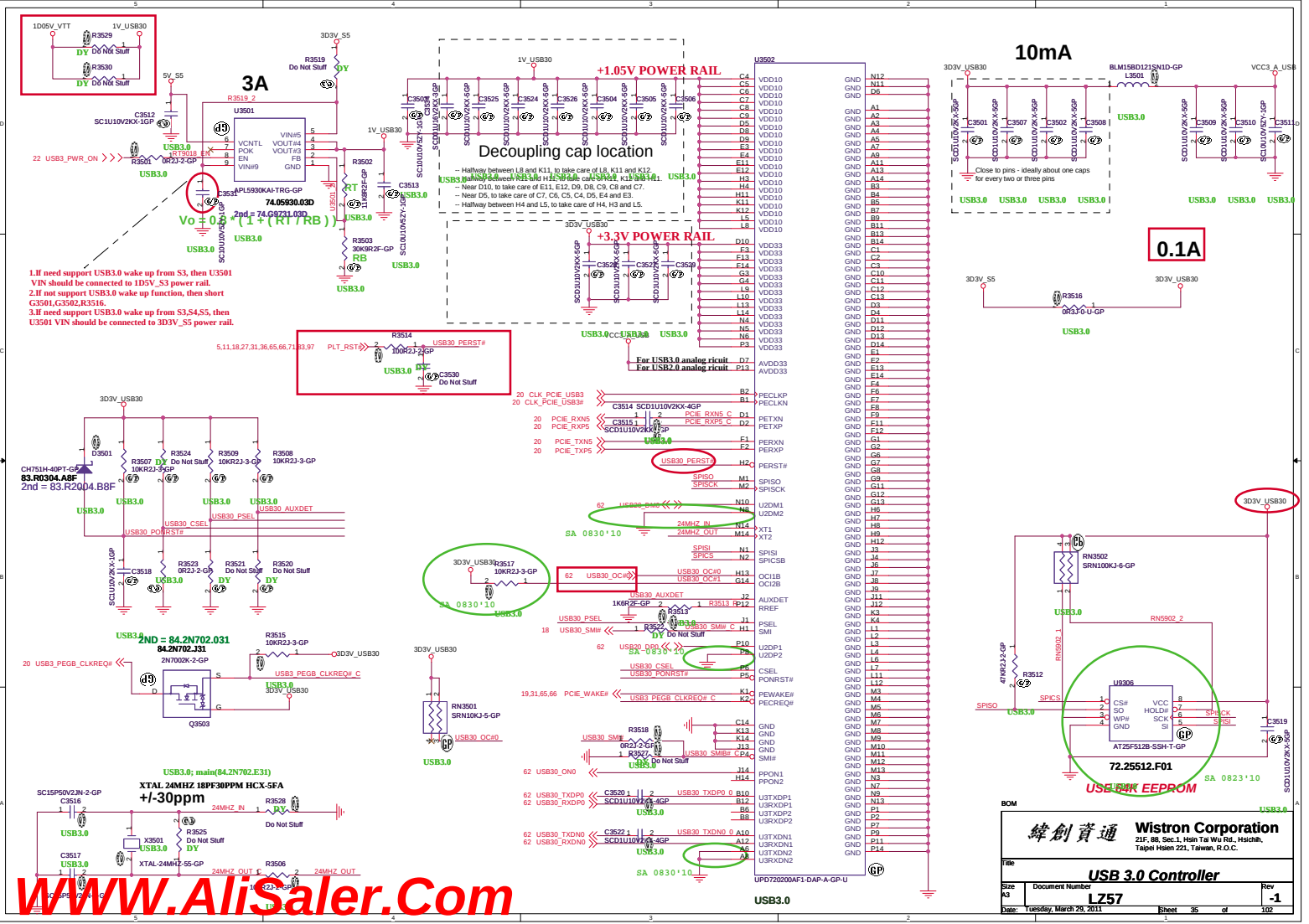
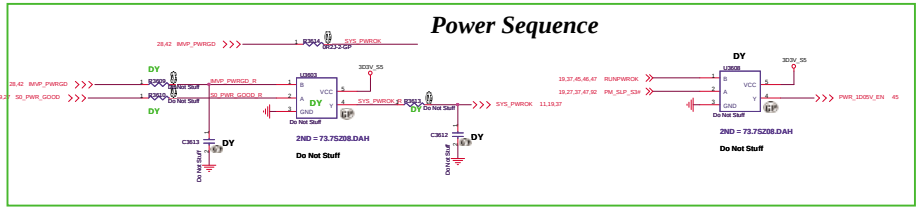
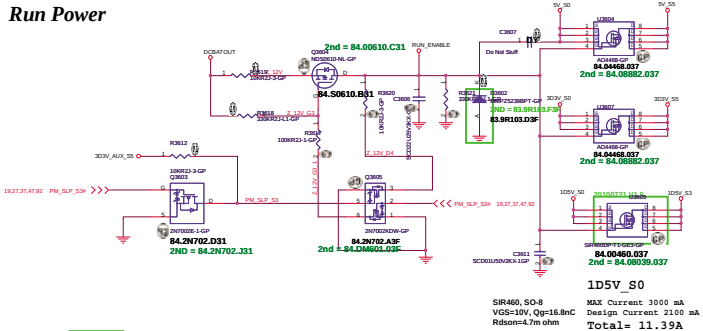
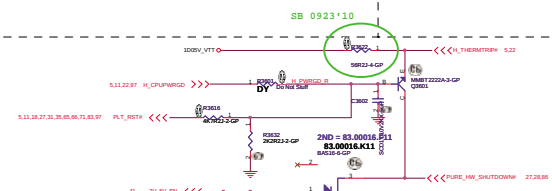


WWW.AliSaler.Com



SSID = Reset.Suspend





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BOM

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 26, 2013 Sheet 36 of 100

Close to CPU
S3 Power Reduction Circuit Processor VREF DQ Implementation

R3707 Do Not Stuff DY
Q3708 2N7002K-2-GP
7,14 M_VREF_DQ_DIMM0
R3708 +V_SM_VREF
Do Not Stuff 84.2N702.J31
+V_SM_VREF_CNT 9
R3705 100KR2J-1-GP
36 PS_S3CNTRL
Q3707 2N7002E-1-GP
DY; main(84.2N702.E31)
PS_S3CNTRL_1.5S
Do Not Stuff
R3721 0R2J-2-GP
R3717 DY
RUN_ENABLE
PM_SLP_S3# 19,27,36,47,92
Do Not Stuff
2ND = 84.2N702.J31
20100725 modify

Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

1D5V_DDR_S0
0D75V_S0
2
R3704 Do Not Stuff DY
R3703 22R2J-2-GP
0D75V_S0_P2
1D5V_DDR_S0_P2
Q3701 2N7002E-1-GP
Q3702 Do Not Stuff
DY; main(84.2N702.E31)
36 PS_S3CNTRL
PS_S3CNTRL
84.2N702.D31
2ND = 84.2N702.J31
Do Not Stuff
2ND = 84.2N702.J31

5 S3 Power Reduction X01 20091111

Q3704 Do Not Stuff
DY; main(84.2N702.E31)
36 PS_S3CNTRL
0D75V_EN
Do Not Stuff
2ND = 84.2N702.J31
5V_S5
R3714 Do Not Stuff DY
1D5V_DDR_S0
R3715 DY Do Not Stuff
Q3706 Do Not Stuff
1.5V_RUN_CPU_EN
1.5V_RUN_CPU_EN#
C3704 Do Not Stuff DY
Do Not Stuff
2ND = 84.03904.P11
3rd = 84.03904.L06
Q3705
DY; main(84.2N702.E31)
0D75V_EN_L
19,27,36,47,92 PM_SLP_S3#
Do Not Stuff
Do Not Stuff
2ND = 84.2N702.J31
3D3V_S0
R3712 Do Not Stuff DY
R3711 Do Not Stuff
R3716 Do Not Stuff DY
SA 0810'10
1.05VTT_PWRGD 45,48
R3710 0R2J-2-GP
0D75V_EN 46
C3705 Do Not Stuff DY

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

1D5V_S3
R3706 1KR2J-1-GP
R3709 Do Not Stuff DY
Q3703 2N7002E-1-GP
5 SM_DRAMRST#
SM_DRAMRST#
R3718 1KR2J-1-GP
DDR3_DRAMRST# 14,15
C3702 SC100P50V2JN-3GP
84.2N702.D31
DRAMRST_CNTRL_PCH 20
2ND = 84.2N702.J31
C3703 SCD047U16V2KX-1-GP
DRAMRST_CNTRL_PCH

Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK

3D3V_S5
R3713 200R2F-L-GP
U3701 74VHC1G09DFT2G-GP
5,19 PM_DRAM_PWRGD
46 0D75V_EN
R3701 Do Not Stuff DY
11,19,36 SYS_PWROK
R3722 Do Not Stuff DY
C3701 SCD1U10V2KX-GP
19,36,45,46,47 RUNPWROK
R3724 0R2J-2-GP DY
3D3V_S5
1D5V_DDR_S0
CEKLT V1.0: PCH to 1K,CUP to 200R
R3702 200R2F-L-GP
VDDPWRGOOD_R
R3719 130R2F-1-GP
VDDPWRGOOD 5
R3720 Do Not Stuff DY
Q3709 Do Not Stuff
DY; main(84.2N702.E31)
2ND = 84.2N702.J31
R3723 Do Not Stuff DY
5,19 PM_DRAM_PWRGD
VDDPWRGOOD_R
20100725 modify
PS_DRAMPWROK must have a maximum of 5ns rise or fall time
PS_DRAMPWROK 1.5V 250mV and the signal shall be monotonic

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ADAPTER
Size A3 / Document Number	LZ57
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 37 of 102

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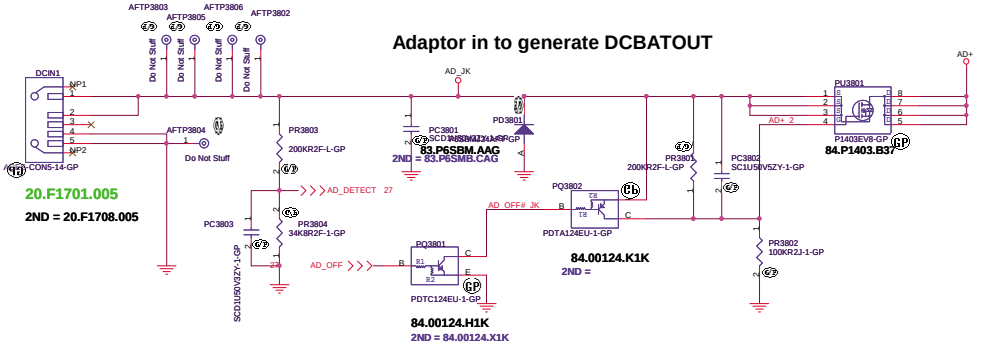

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DCIN_JACK***	
Size	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 38 of 102	

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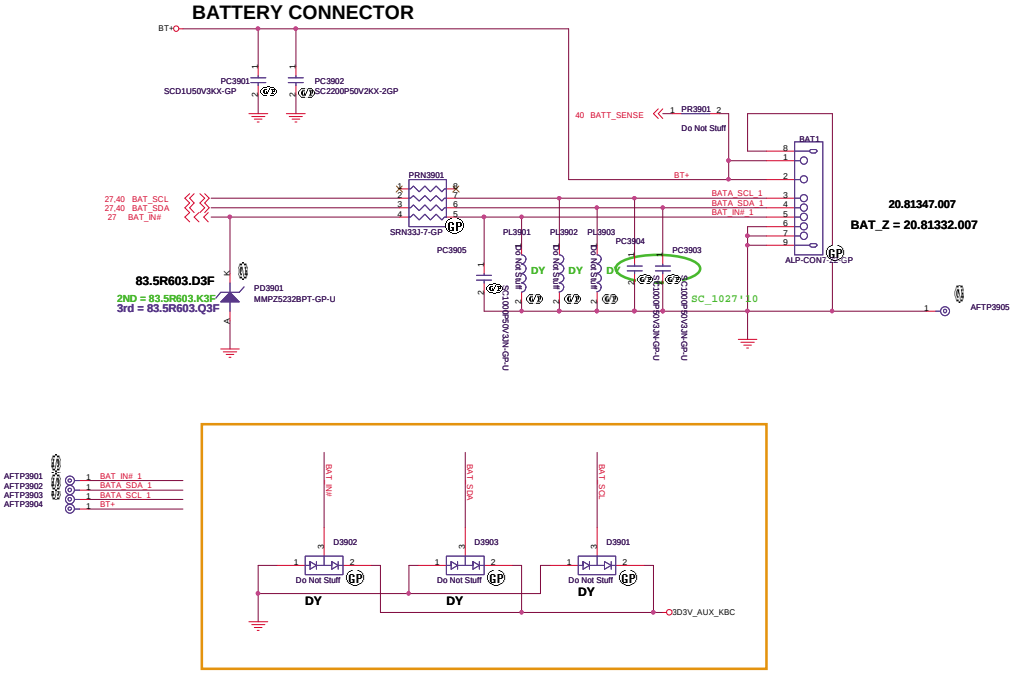

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BATT_CONN	
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 39 of 102	

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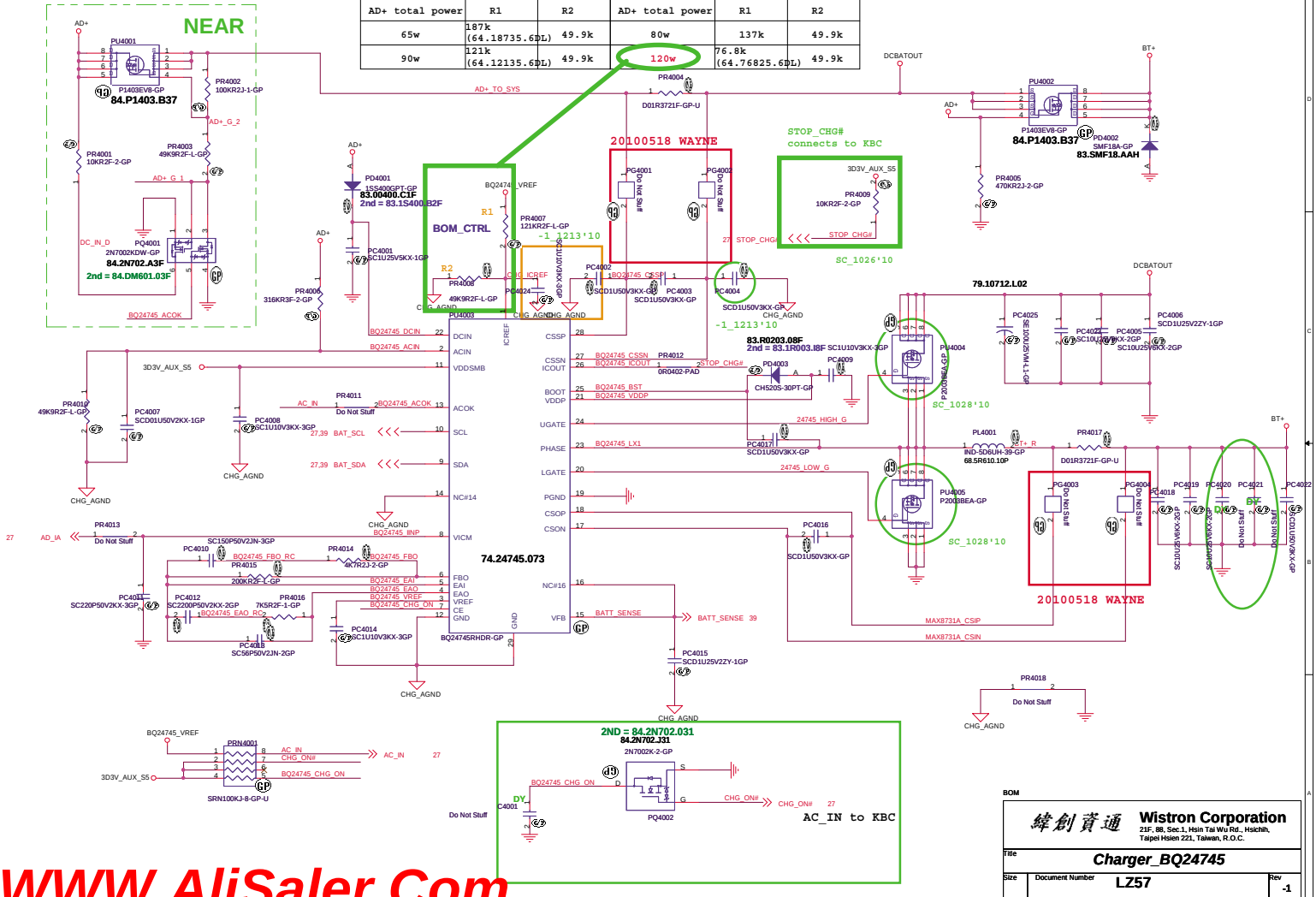
AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k (64.18735.6DL)	49.9k	80w	137k	49.9k
90w	121k (64.12135.6DL)	49.9k	120w	76.8k (64.76825.6DL)	49.9k



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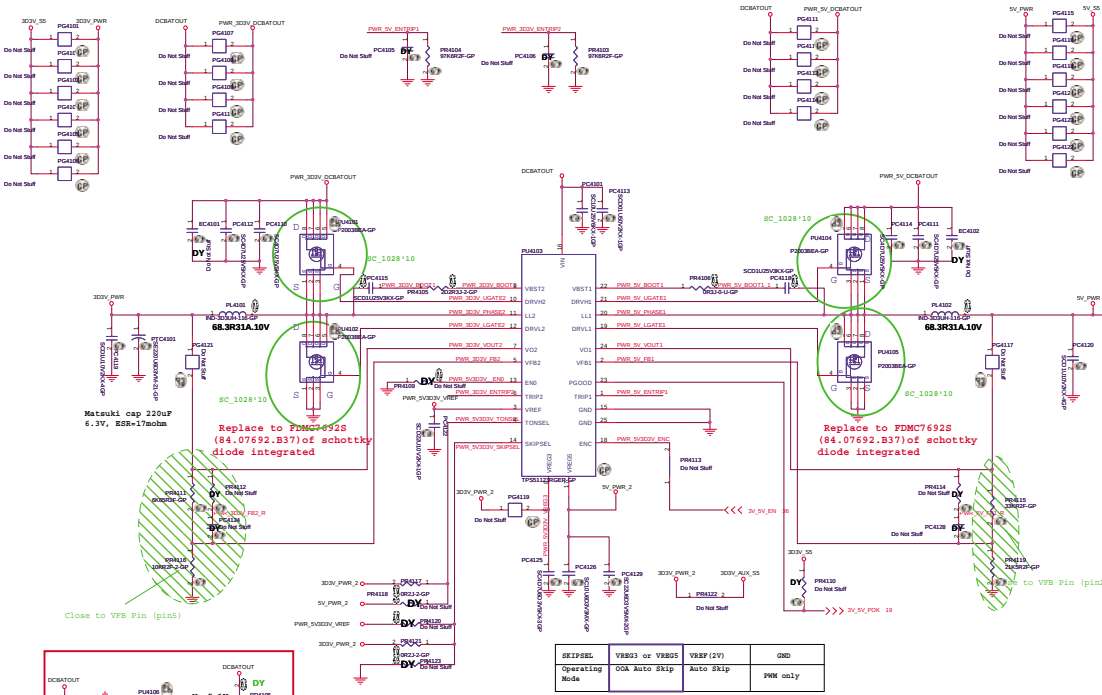
SSID = PWR.Plane.Regulator_5v3p3v



SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

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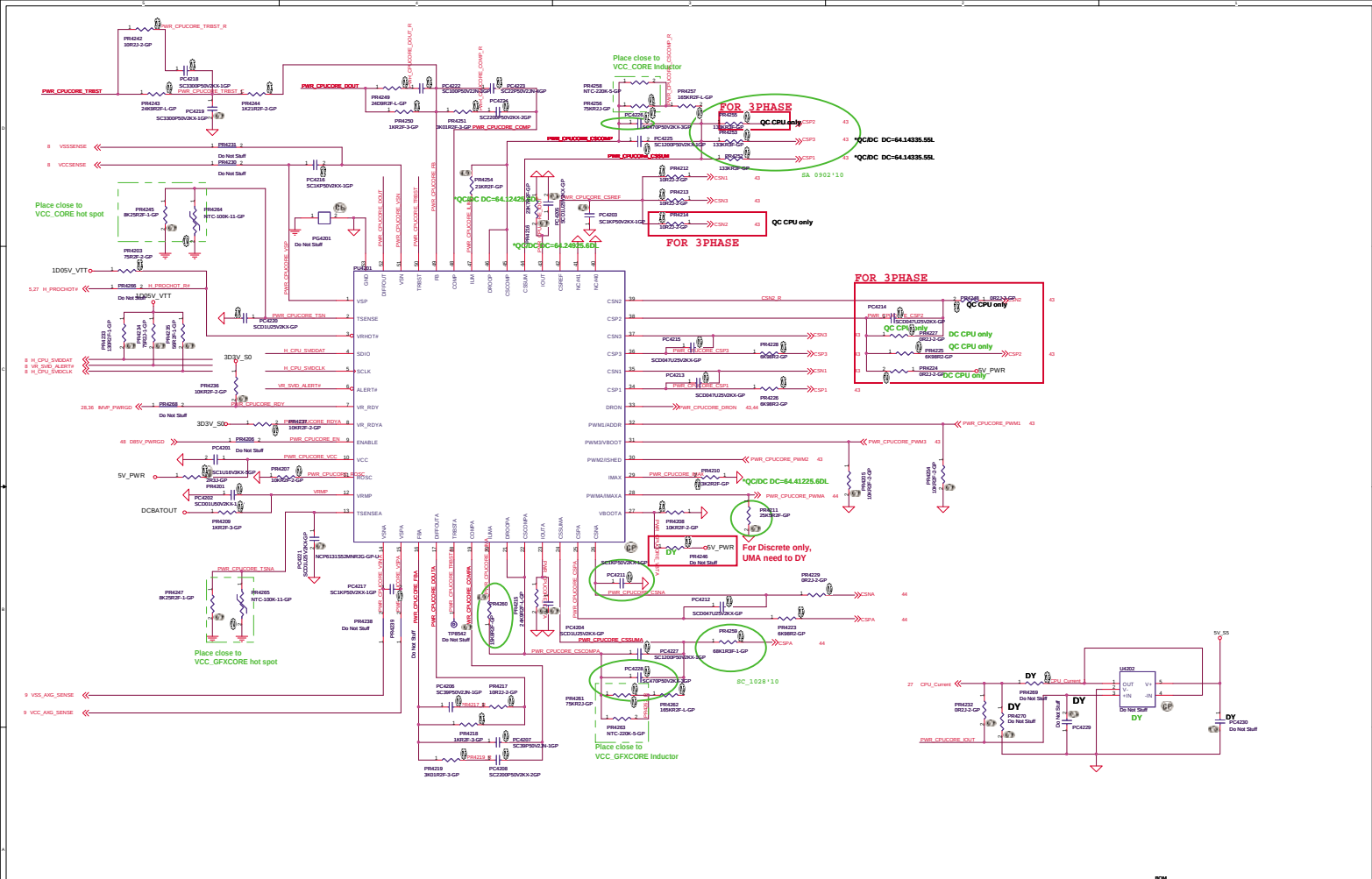
Title: DC/DC 3D3V5V

Size	Document Number	Rev
	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 41 of 100



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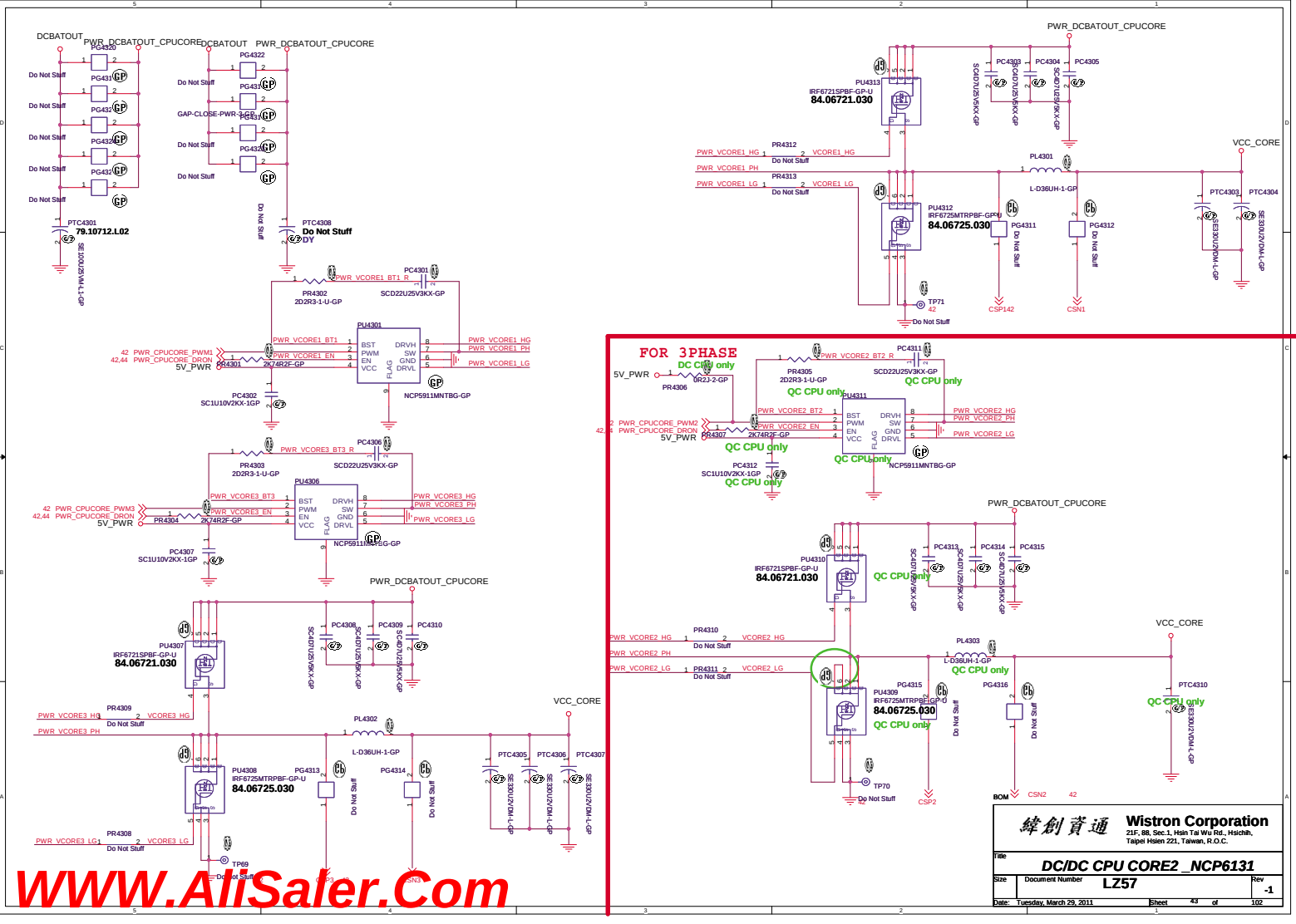

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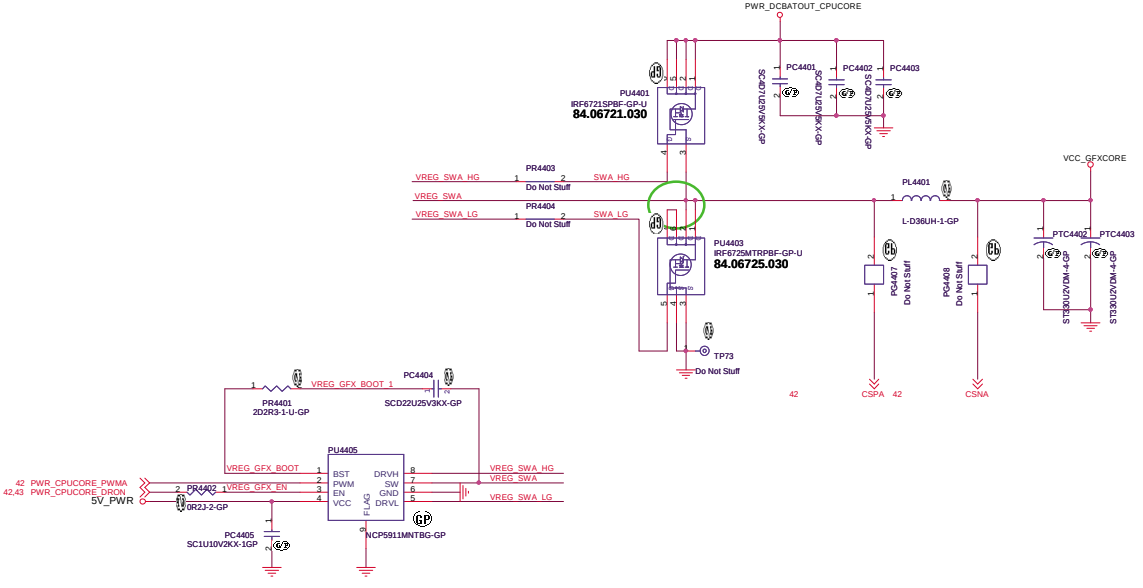

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DC/DC CPU CORE3 _NCP6131***	
Size	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 44 of 102	

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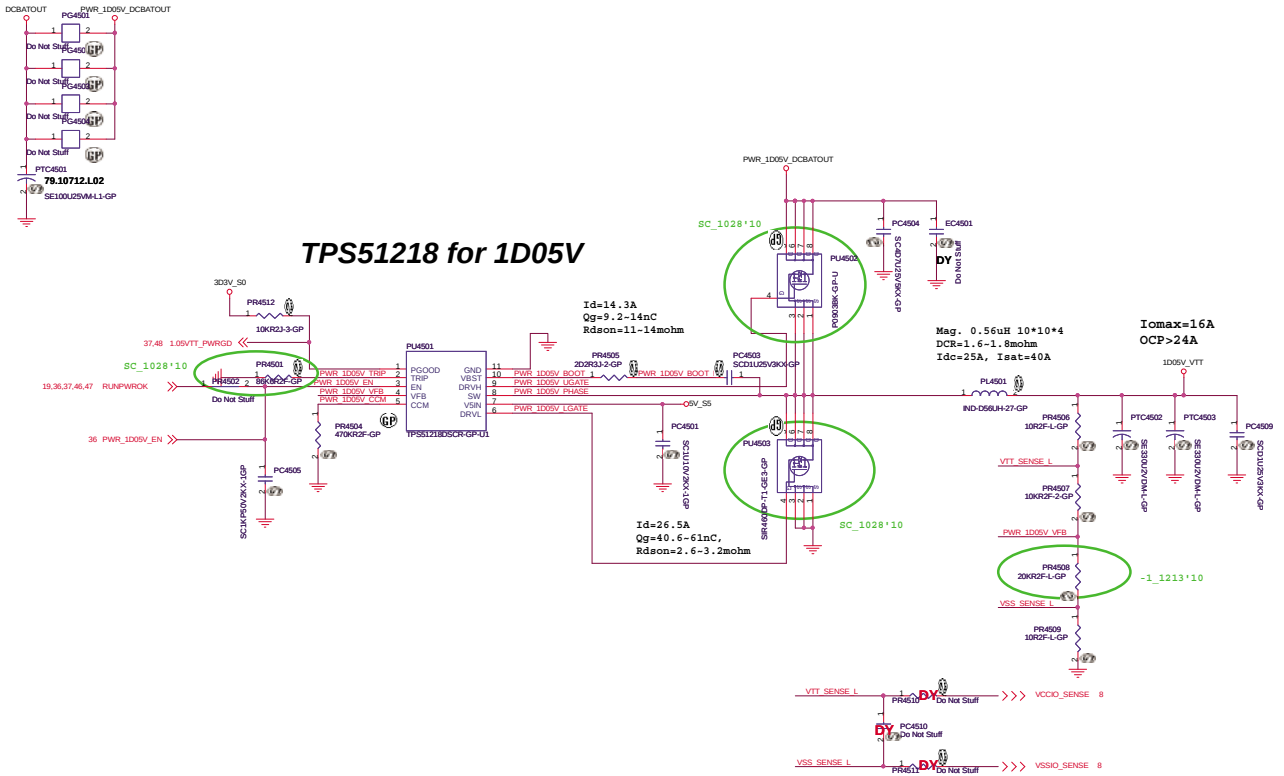

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	TPS51218_1D05V	
Size	Document Number	Rev -1
Date: Tuesday, March 29, 2011	Sheet 45 of 102	

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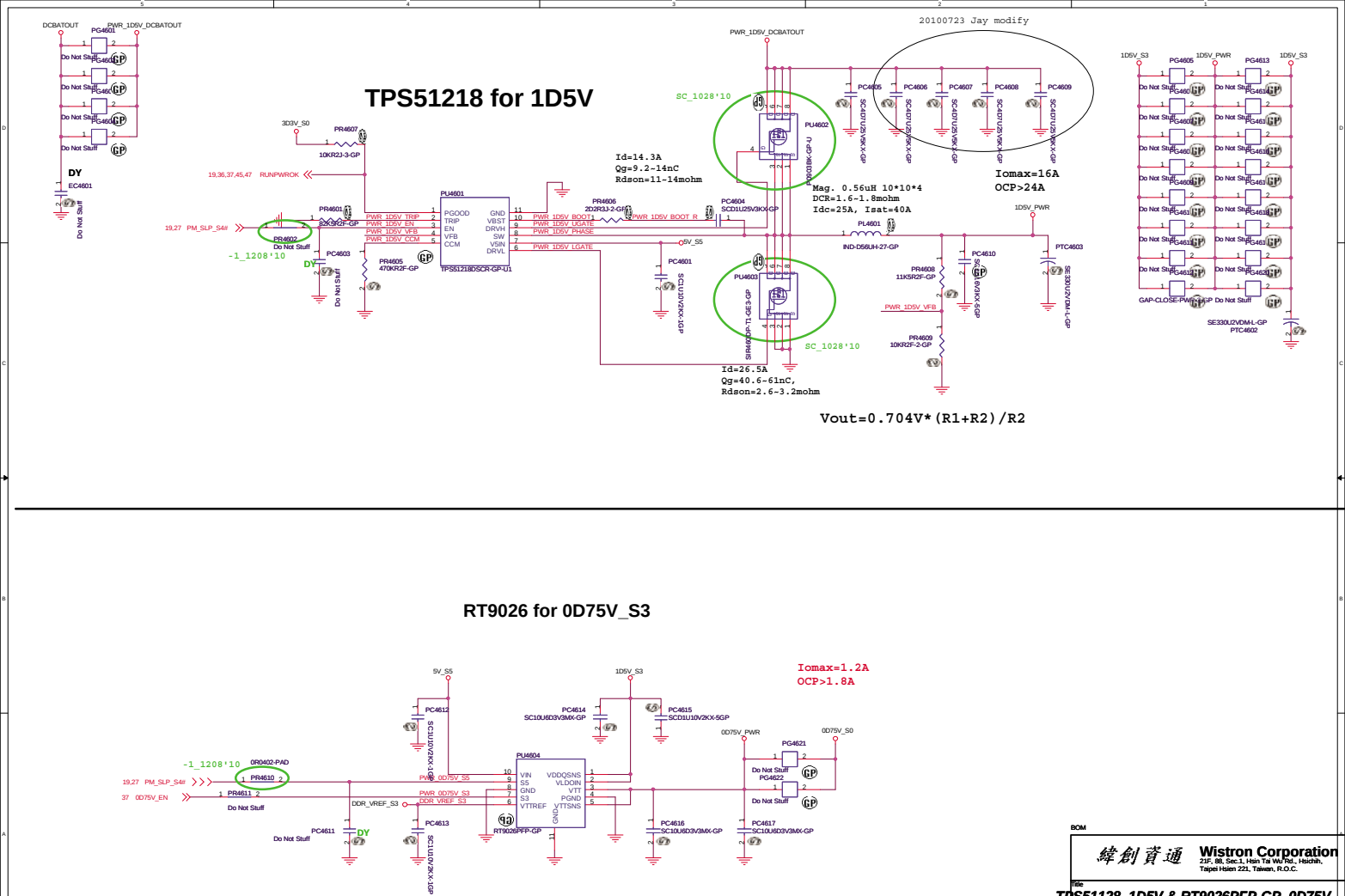

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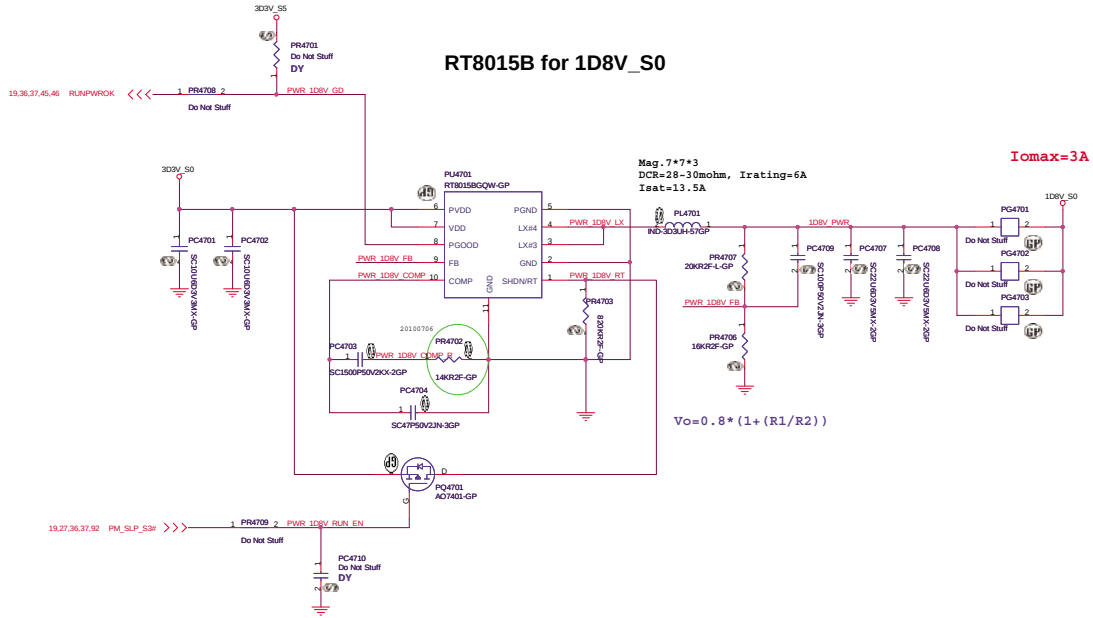
RT9025 for 1D8V_S0



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***1D8V_RT9025***	
Size	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 47 of 102	

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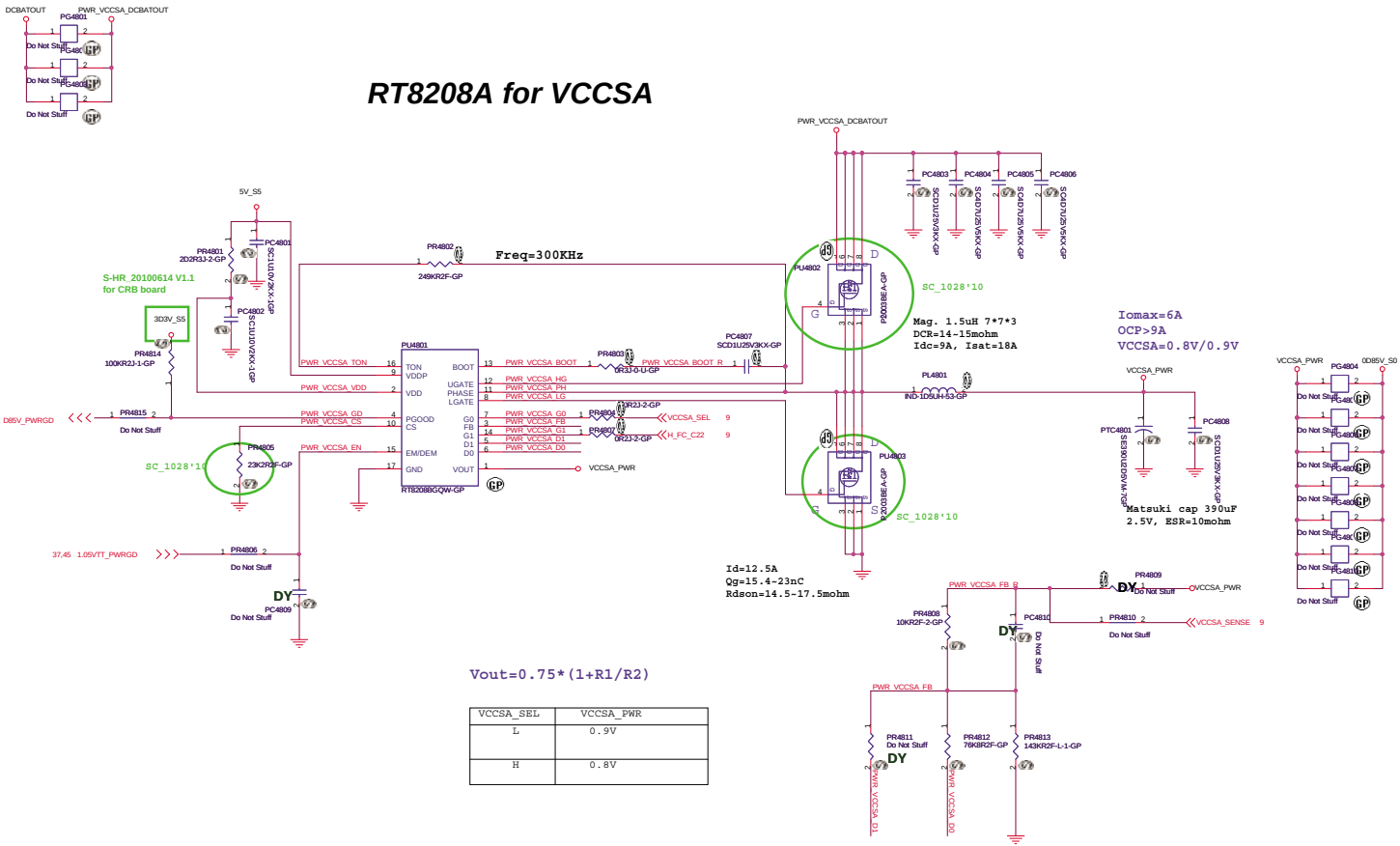
RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RT8208B_VCCSA*

Size	Document Number	Rev
	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 48 of 102

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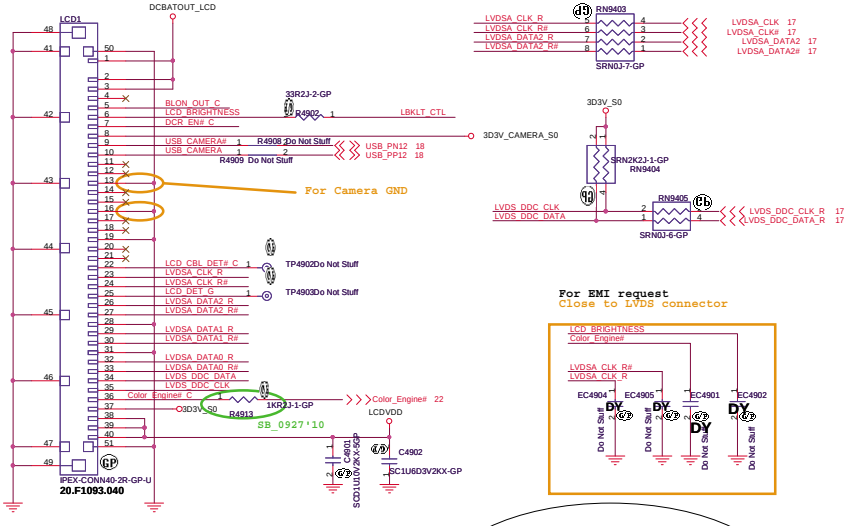
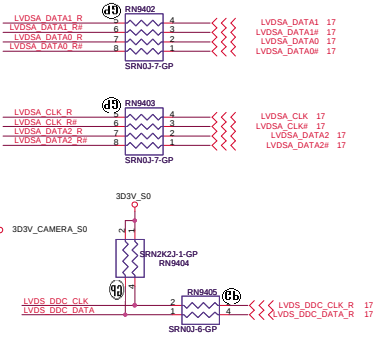
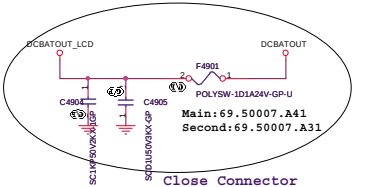
SSID = VIDEO

LVDS CONNECTOR

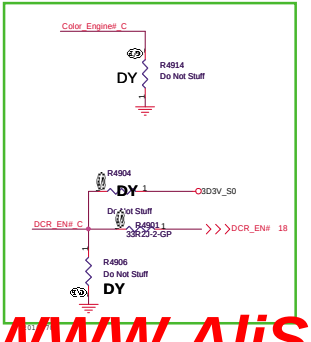




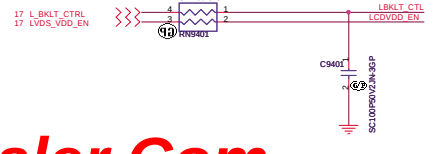
For EMI request
Close to LVDS connector



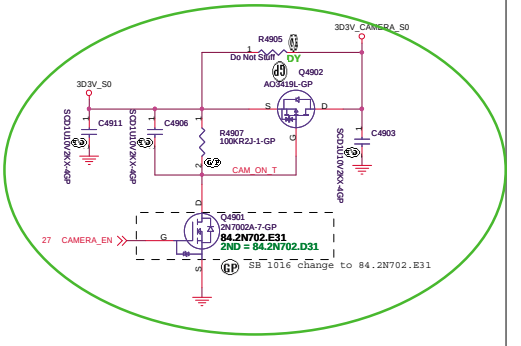
Close Connector



Panel BL brightness/Power En/BL En



CAMERA POWER



SB 0923'10

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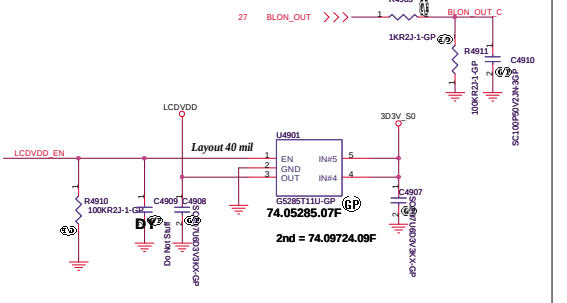

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 49 of 102

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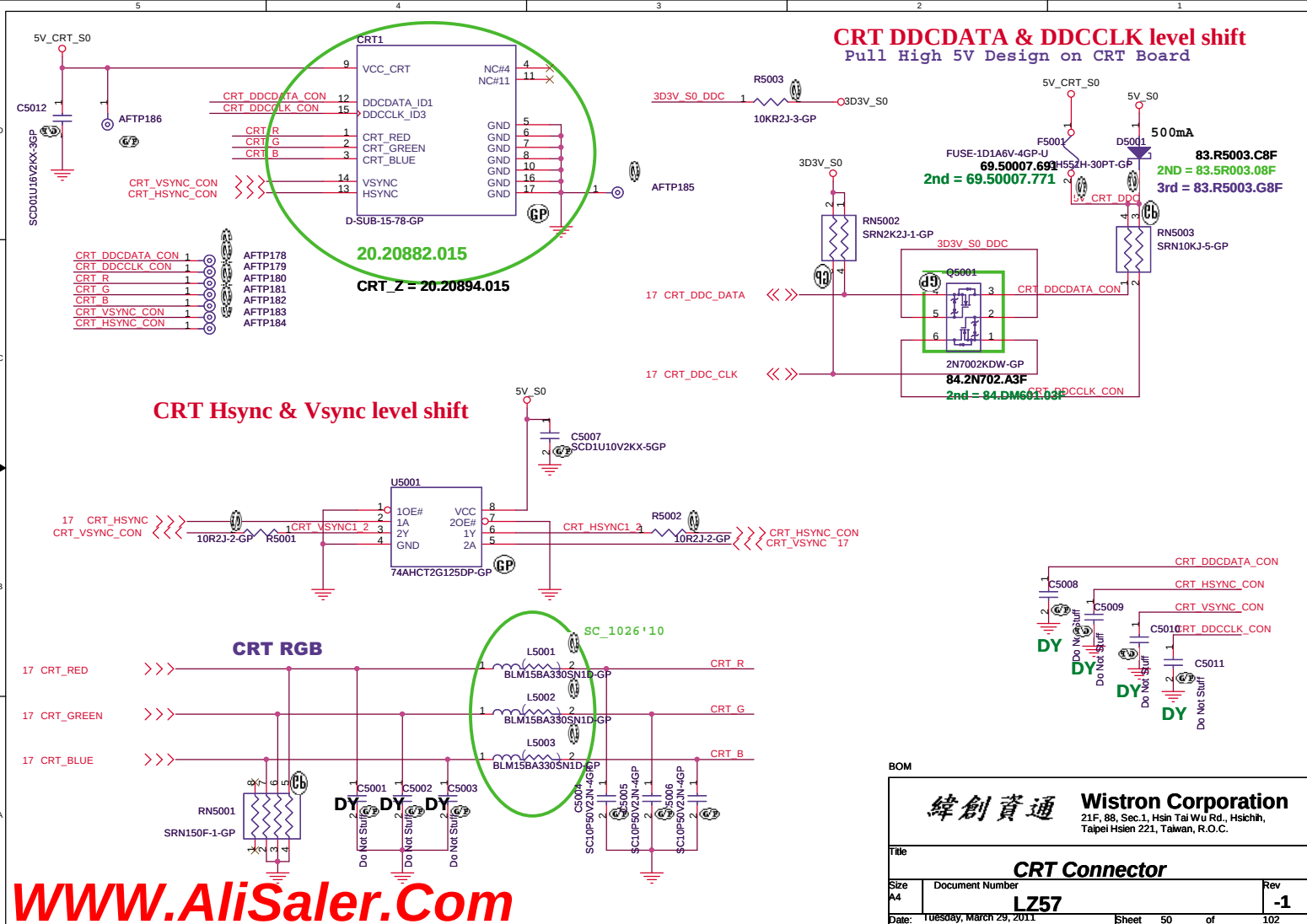

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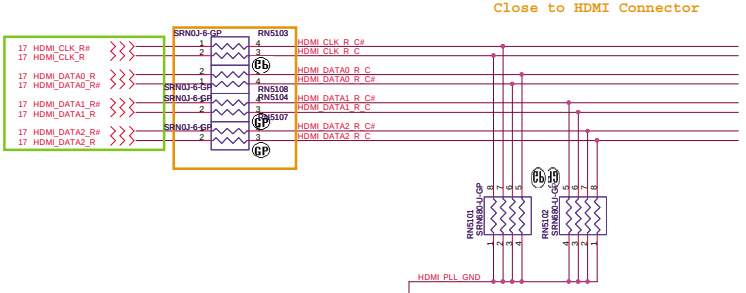
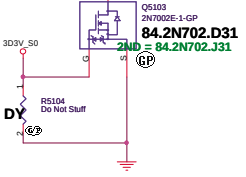
SSID = VIDEO

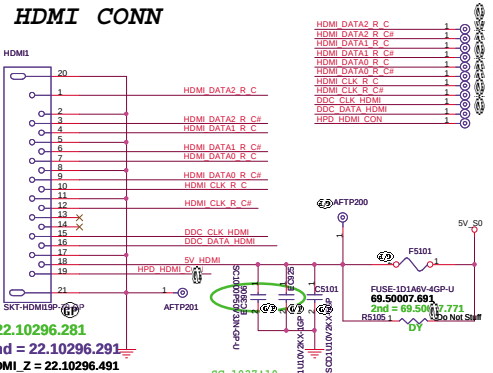
HDMI CONNECTOR

HDMI Passive Level Shifter

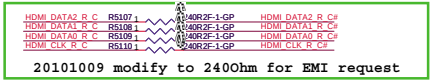


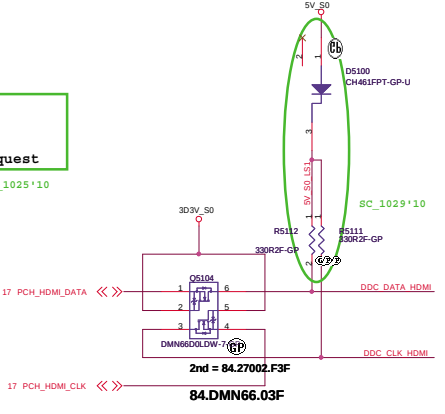


HDMI CONN

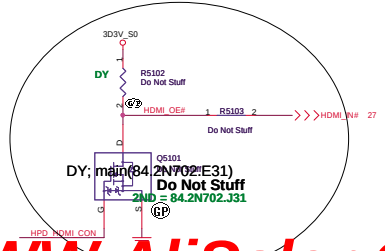


HDMI DDC Passive Level Shifter

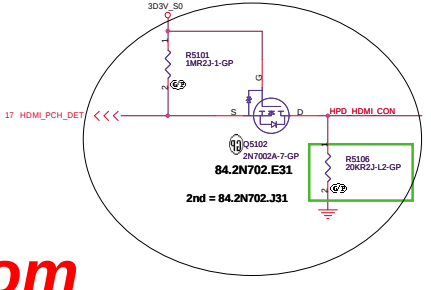




20100727 modify, KBC isn't use.



20100727 follow intel design guide



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI Level Shifter/Connector	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 51 of 102	

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: S-VIDEO

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 53 of 102

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(Blanking)

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 54 of 102

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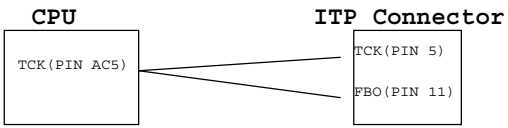
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ITP	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 55 of 102	

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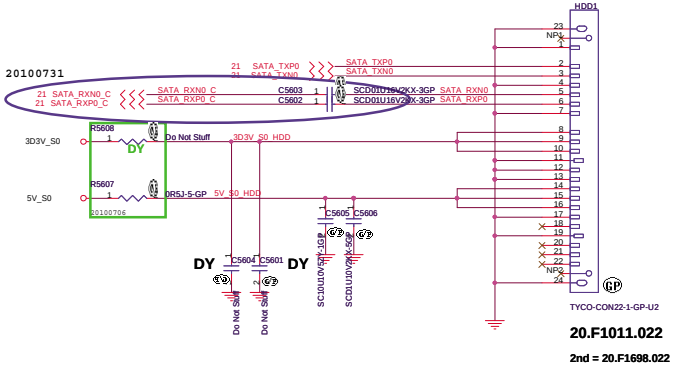
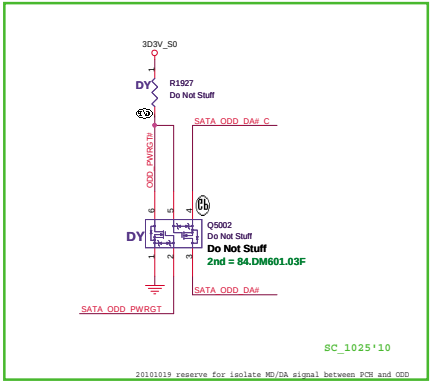
SSID = SATA

SATA HDD Connector



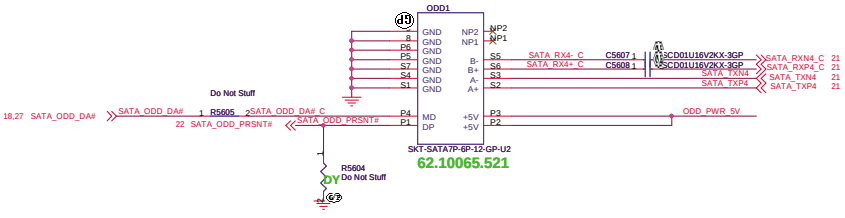


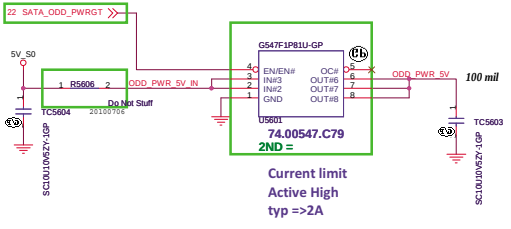
ODD Connector

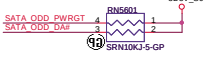
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

SATA Zero Power ODD







SUPPORT ZERO SATA ODD

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD/ODD	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 56 of 102	

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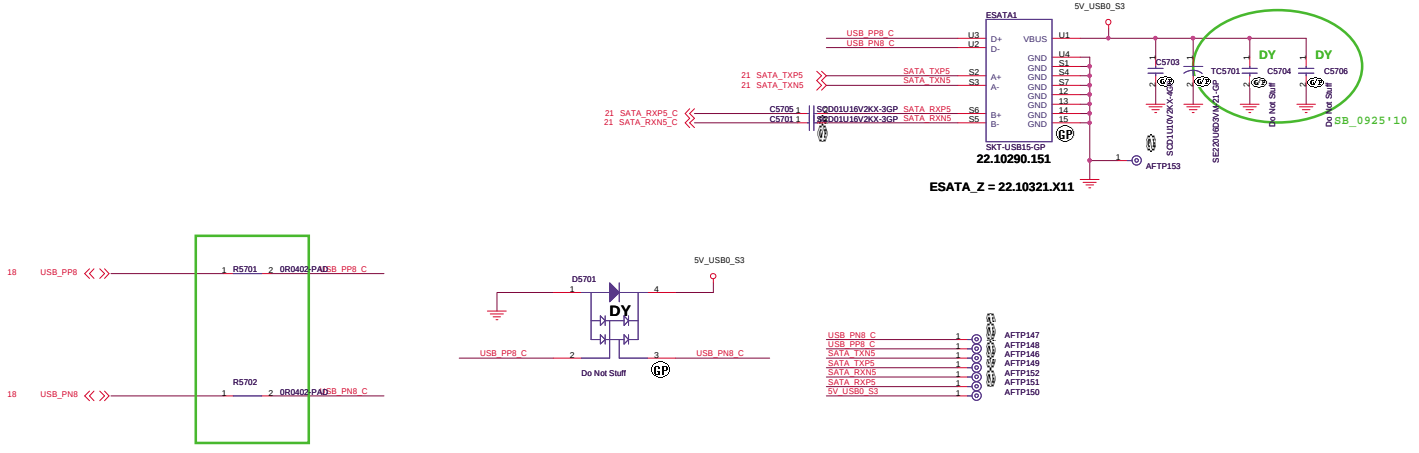

BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: E-SATA/LUSB

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 57 of 102

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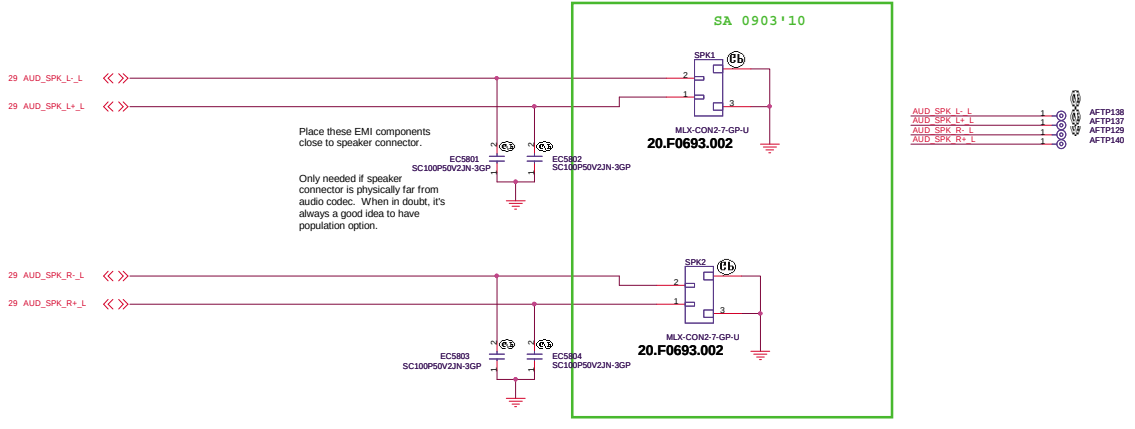
INTERNAL STEREO SPEAKERS



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MIC/SPEAKER/AUDIO JACK***
Size A3 / Document Number	**LZ57** / Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 58 of 102

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Reserved

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Reserved	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 59 of 102	

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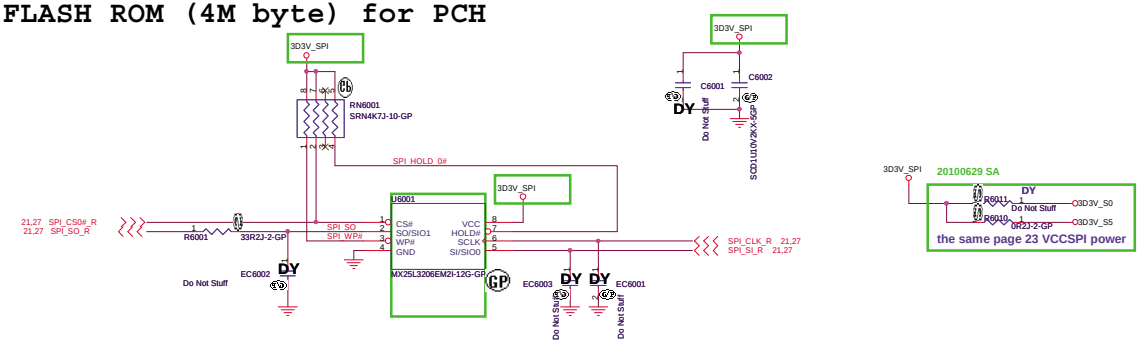
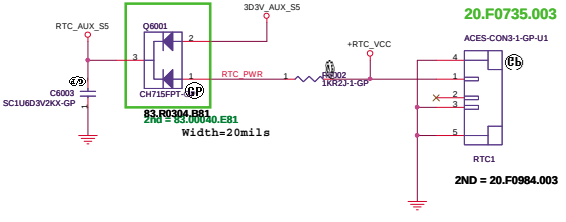
SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Flash/RTC
Size A3	Document Number LZ57
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 60 of 102

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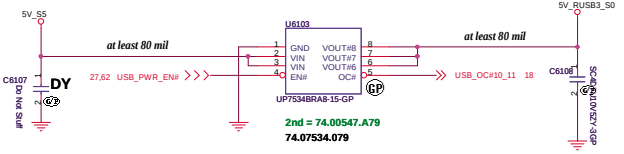
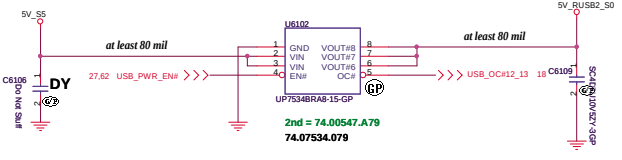
SSID = USB

RJ45_USB Board USB Power



I/O Board USB Power



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	USB Power SW	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 61 of 102	

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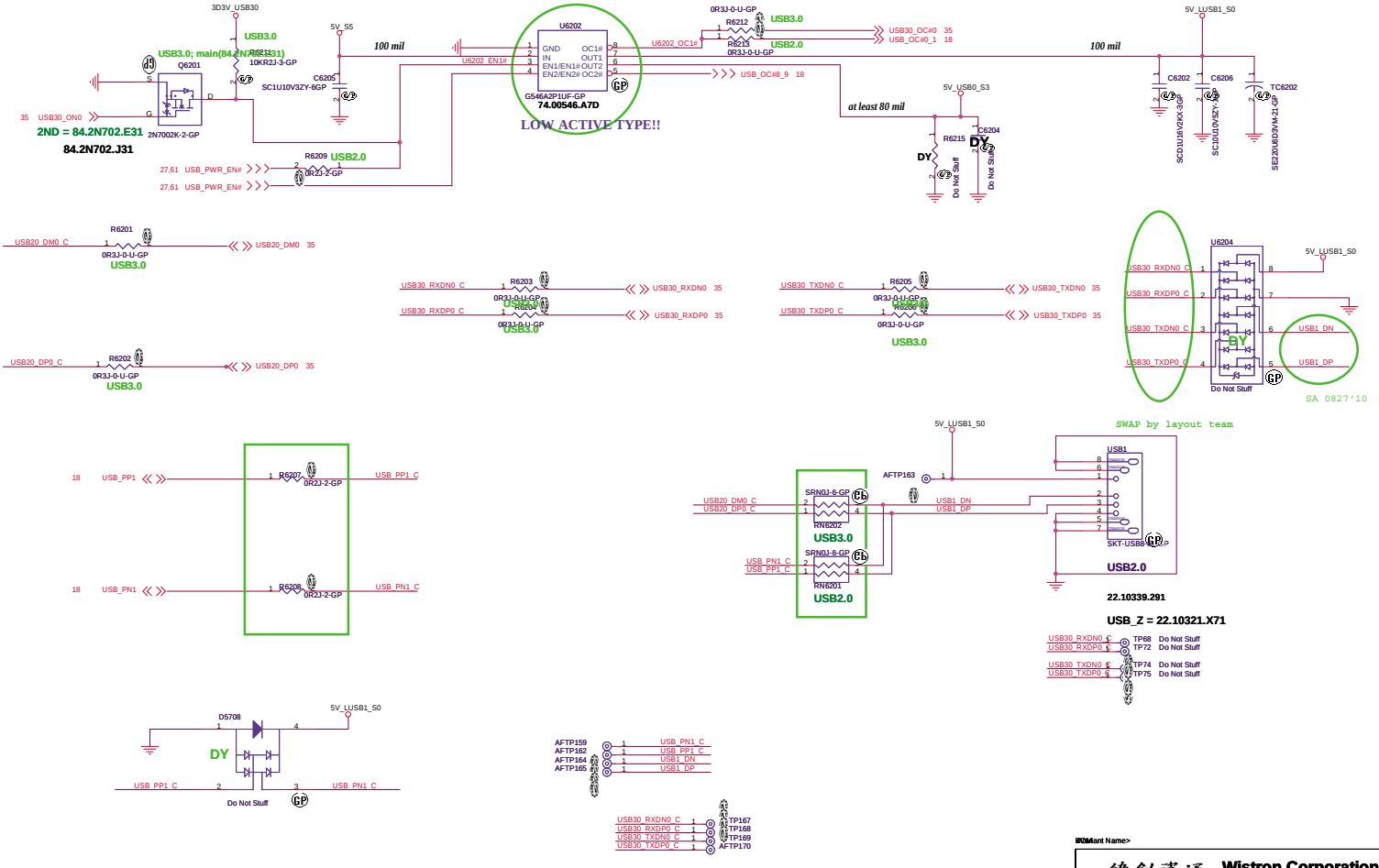
Left Side USB Power Switch



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BOM Plant Name:

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 2.0/3.0 Port

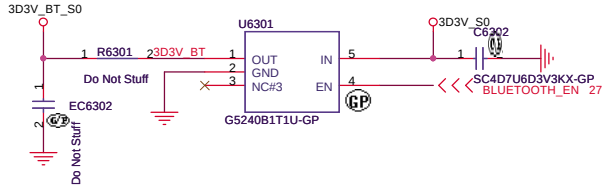
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 62 of 102

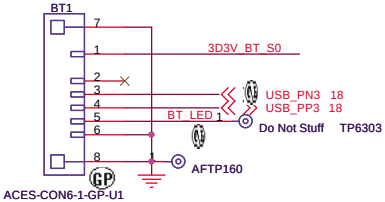
SSID = User.Interface

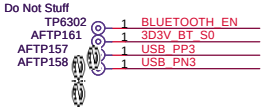
Bluetooth Module conn.

Bluetooth Module



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request





20.F0772.006

2ND = 20.F1804.006

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Bluetooth	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 63 of 102	

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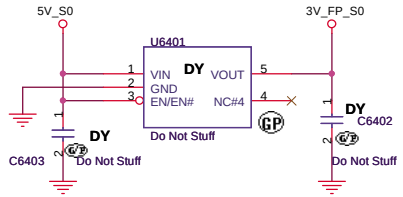
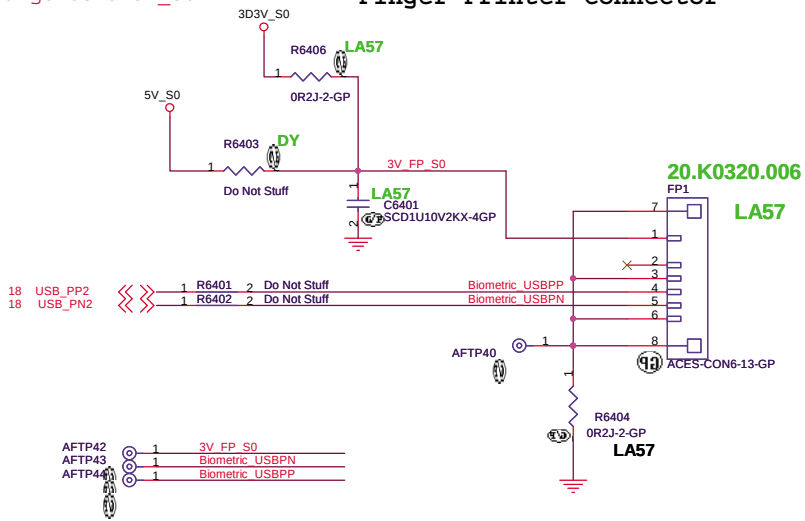


LA47 change to 3D3V_S0

Finger Printer Connector



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RESERVED***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 64 of 102	

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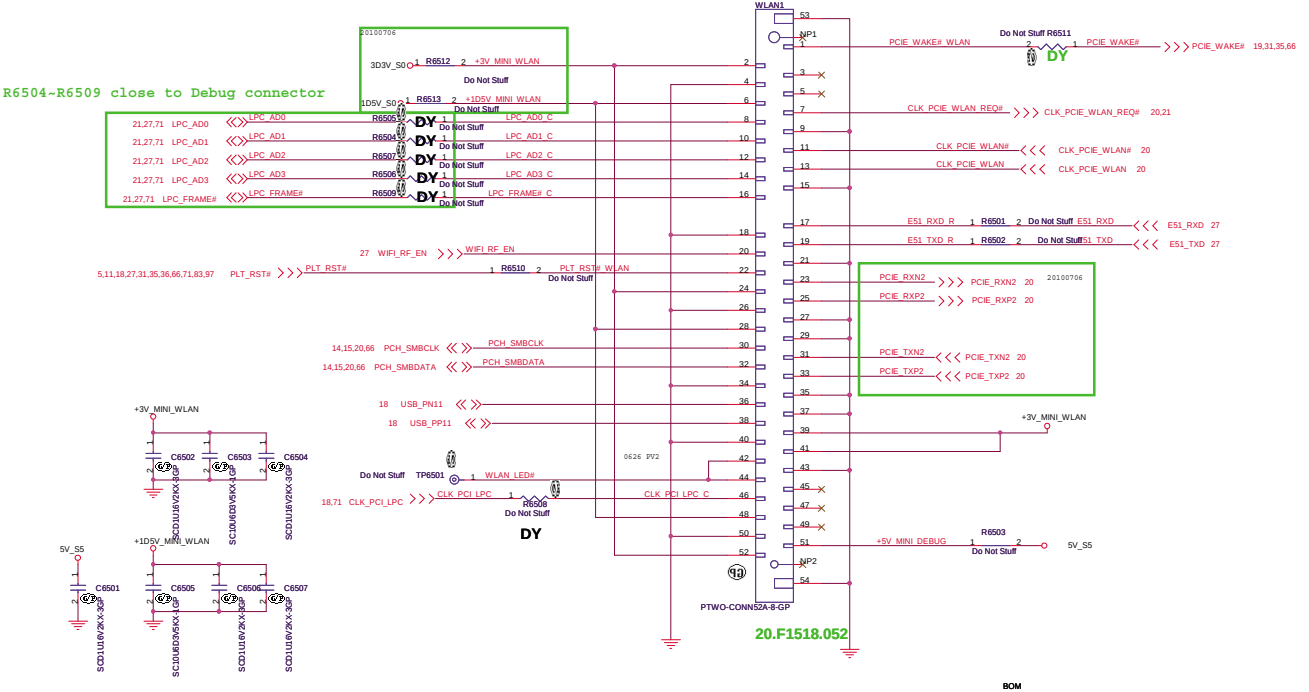
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



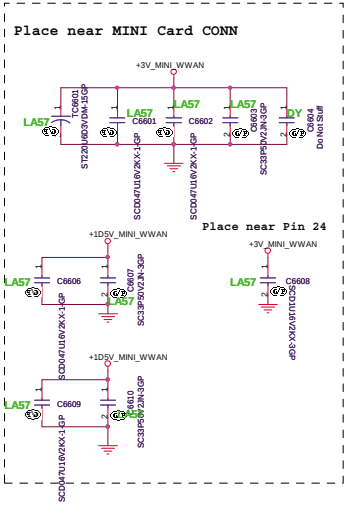
BOM

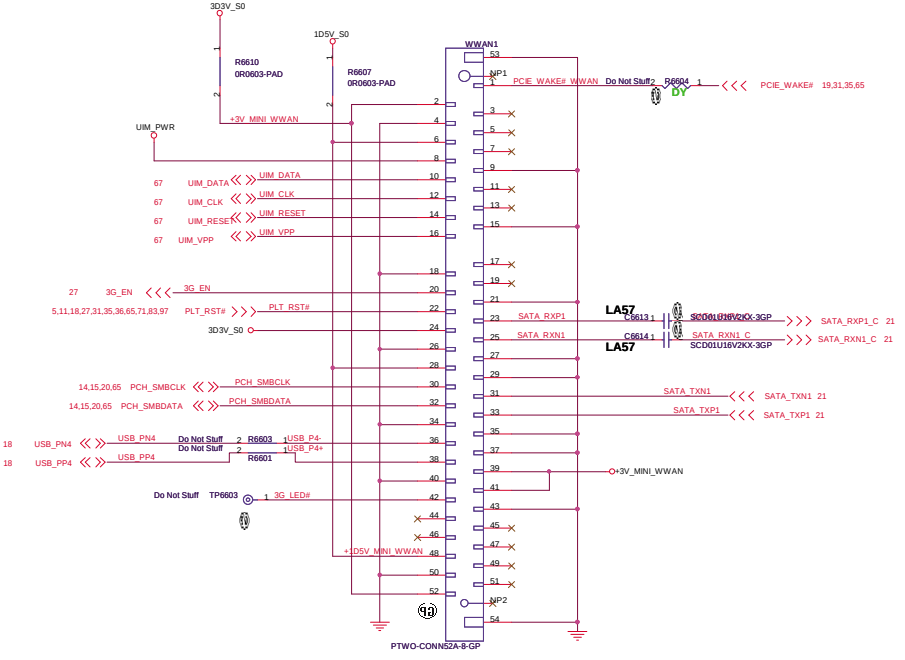
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	MINICARD(WLAN)/ITP CONN
Size A3	Document Number LZ57
	Rev -1
Date: Tuesday, March 29, 2011	Sheet 65 of 102

WWW.AliSaler.Com

SSID = Wireless

Mini Card Connector(WWAN)





BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	WWAN Connector	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 66 of 102	

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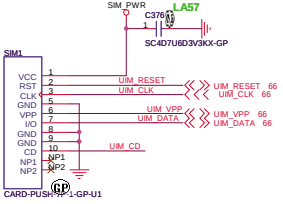
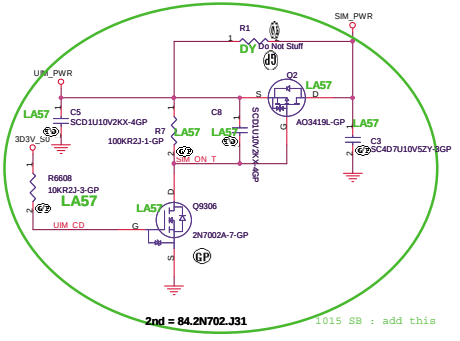


LA57

20.I0073.001



84.2N702.E31

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SIM CARD***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 67 of 102	

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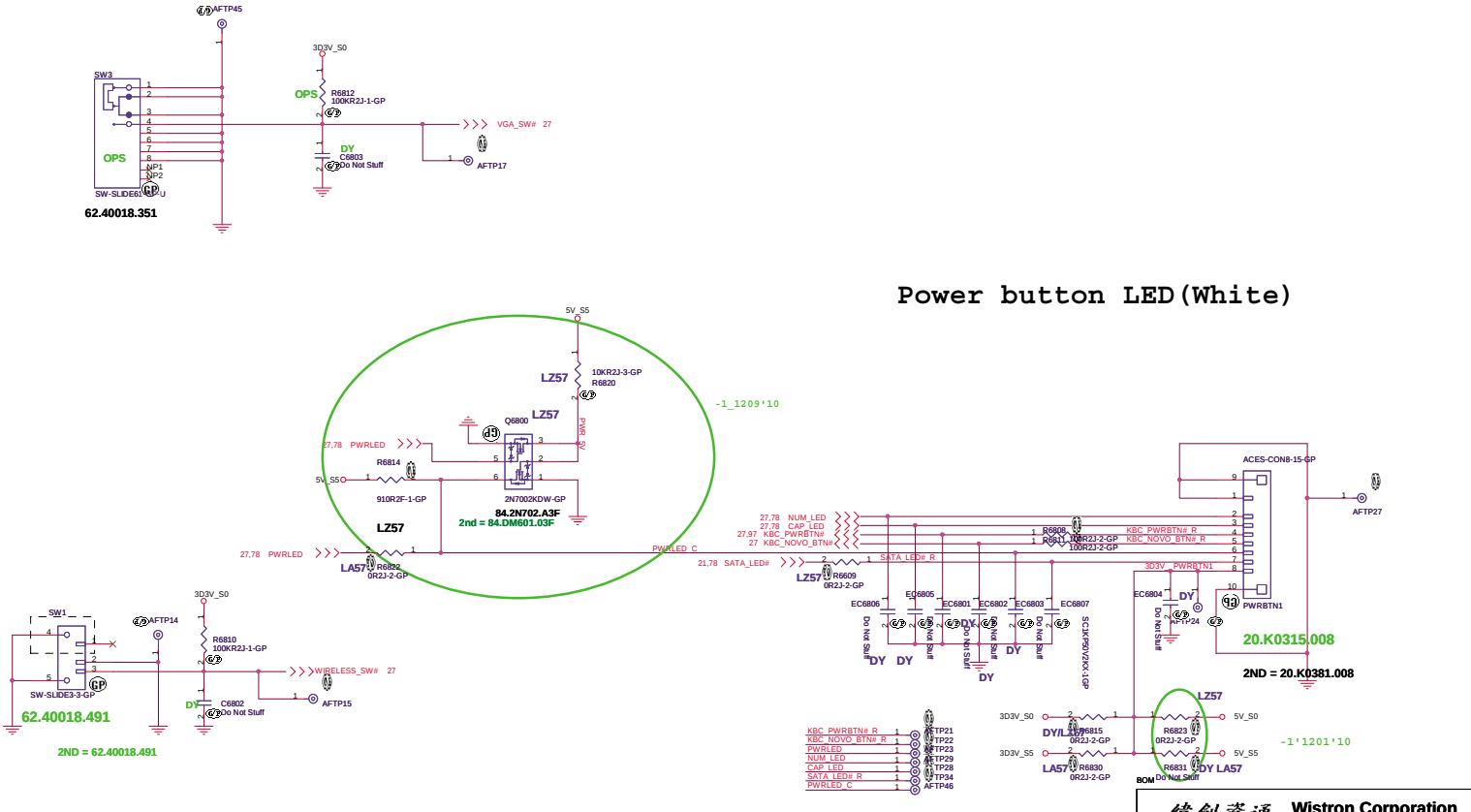
SSID = User.Interface



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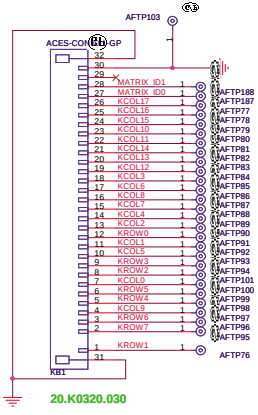
SSID = KBC

Internal KeyBoard Connector

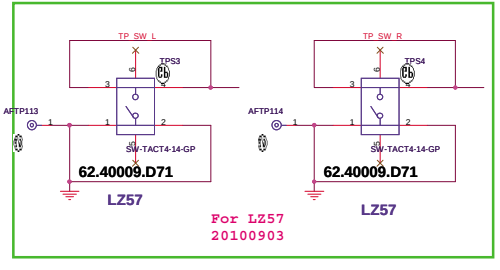


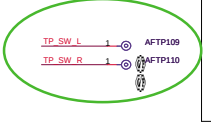
20.K0320.030

ID KEY MATRIX	SENSE			
	27	28	29	30
	ID0	ID1	ID2	GND
US	GND	GND	X	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

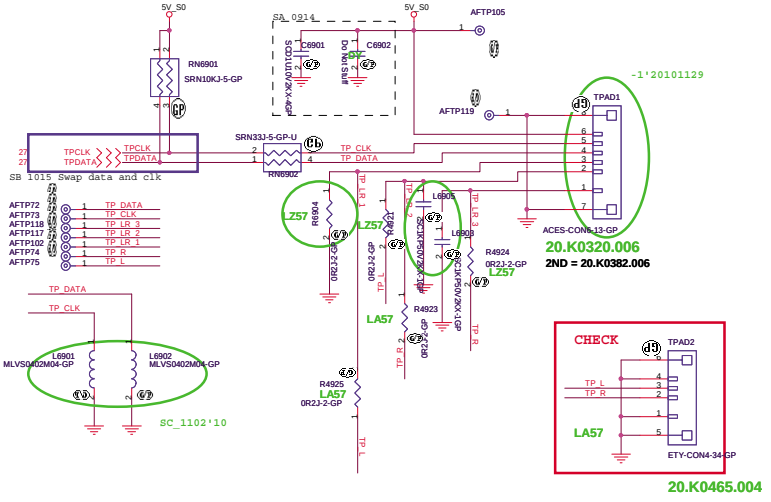
KROW[0..7] 27

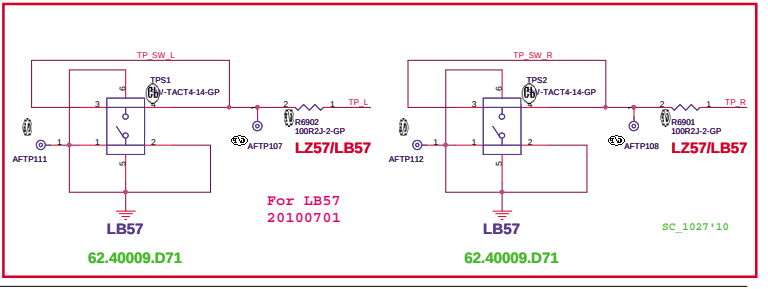
KCOL[0..17] 27





SSID = Touch.Pad





BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Key Board/Touch Pad	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 69 of 102	

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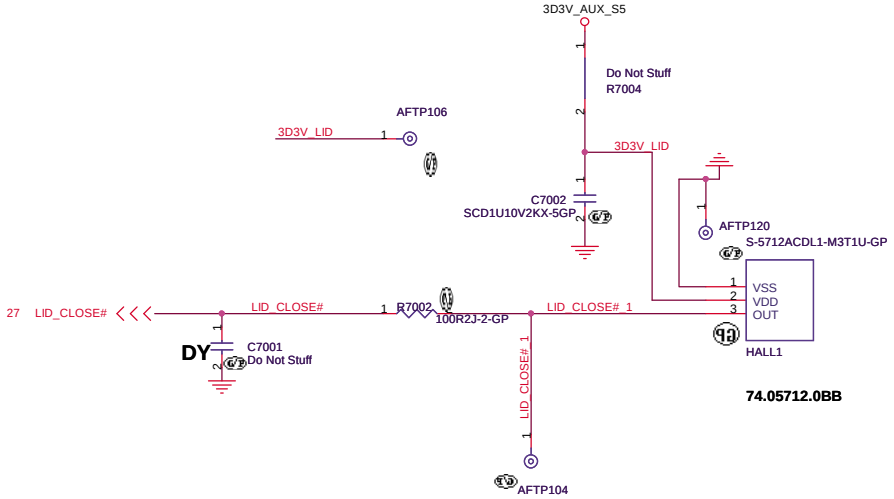

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 70 of 102

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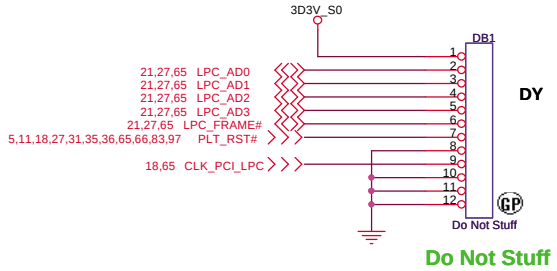

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 71 of 102

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緯創資通 Wistron Corporation
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Title

Reserved

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 72 of 102

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Title: **Reserved**

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 73 of 102

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Title	***CARD Reader CONN***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 74 of 102	

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Title	***New Card***
Size A4	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 75 of 102

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Title	***Reserved***
Size A4	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 76 of 102

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Title: **Reserved**

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 77 of 102

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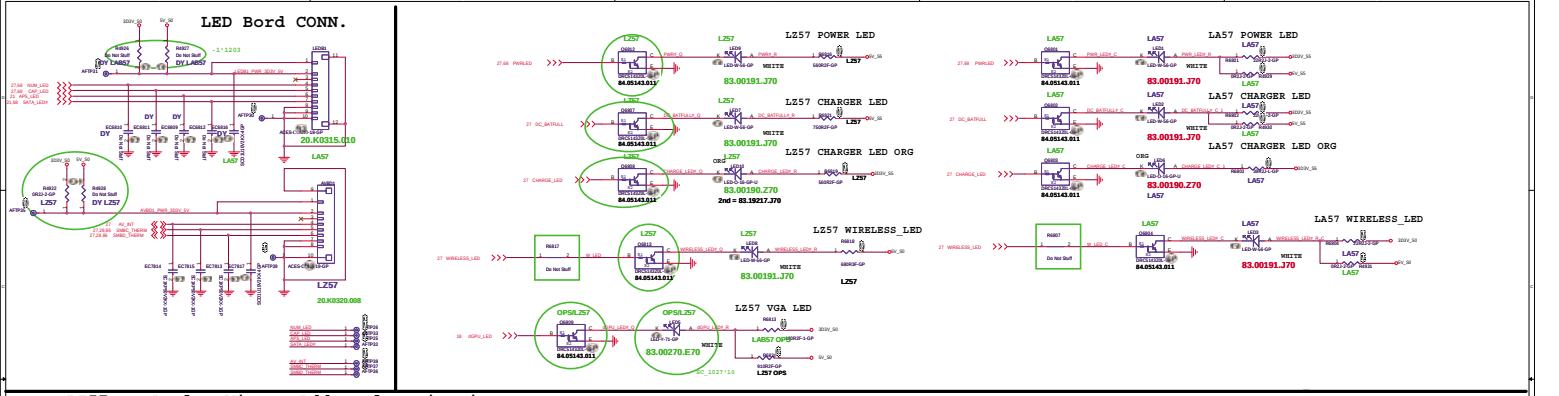
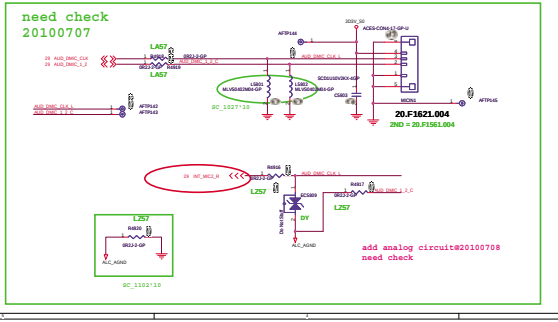
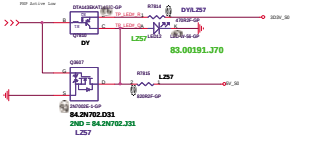


LZ57 => Analog Mic => Add analog circuit.
LA57 => Digital Mic



LZ57 Touch Pad LED



Wistron Corporation
LED8/LED
LZ57
-1

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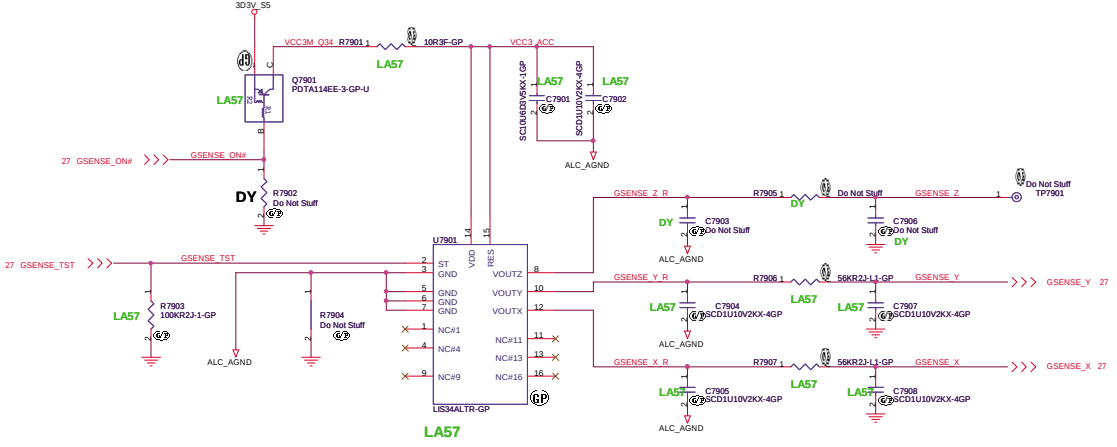
G-Sensor



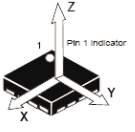
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCBC switching area.



BOM

緯創資通 **Wistron Corporation**
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Title	G-Sensor	
Size Custom	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 79 of 102	

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Title	***Reserved***
Size A4	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 80 of 102

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Title	***Reserved***
Size A4	Document Number **LZ57**
Rev	**-1**
Date: Tuesday, March 29, 2011	Sheet 81 of 102

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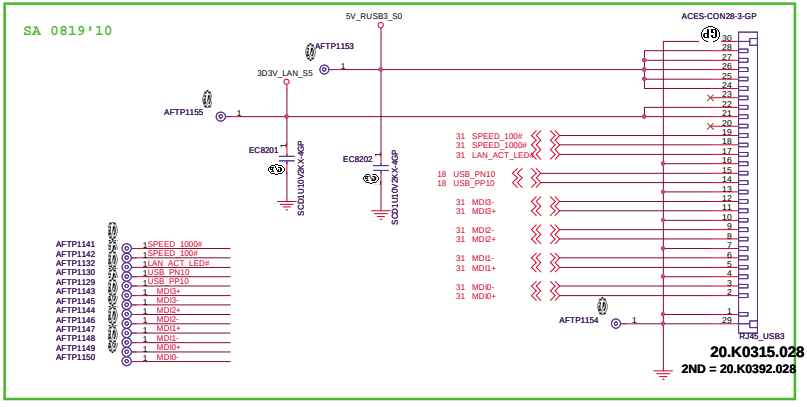
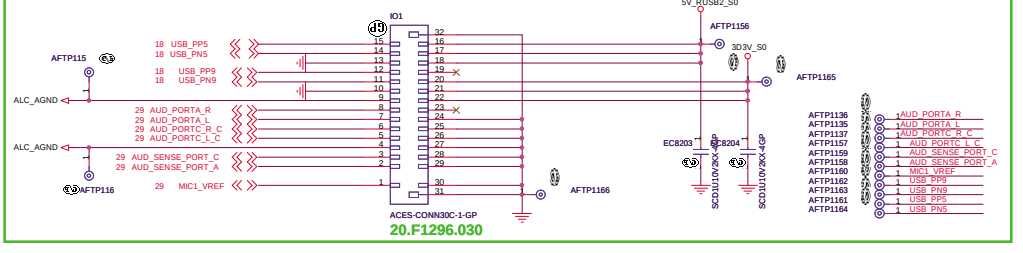
RJ45_USB CONN.



Card Reader Board CONN.



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***IO Board Connector***
Size A3 / Document Number	LZ57
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 82 of 102

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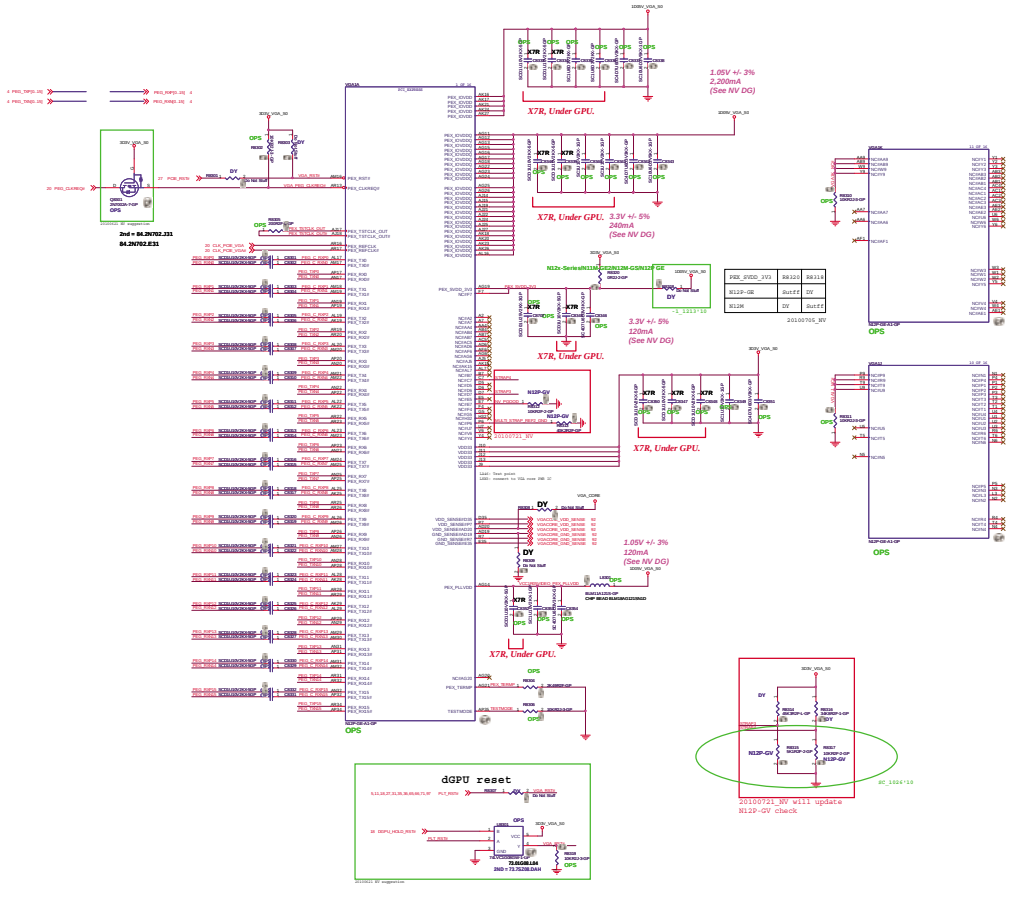

Wistron Corporation	
N12P-GE(1/6): PEG I/F	
L257	-3

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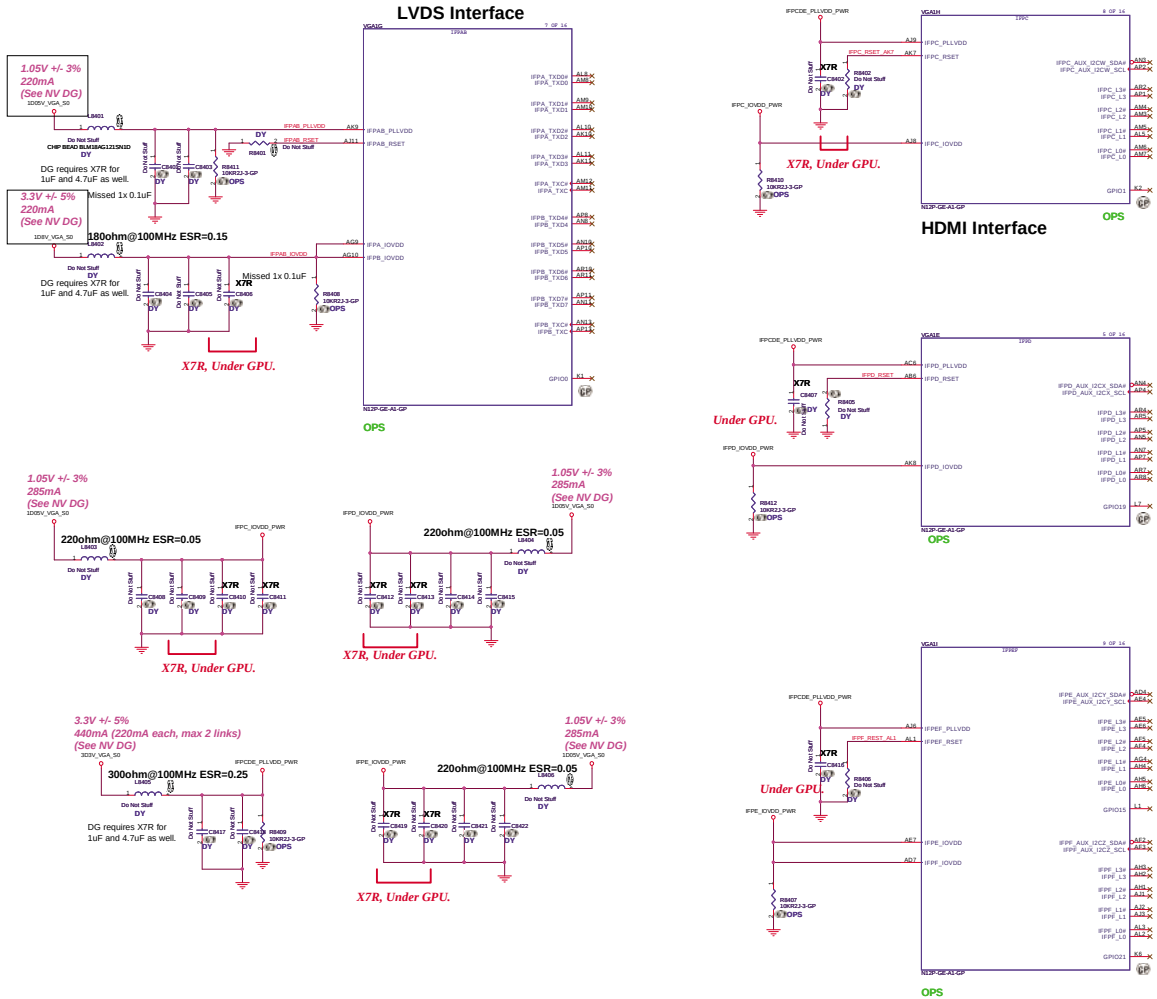

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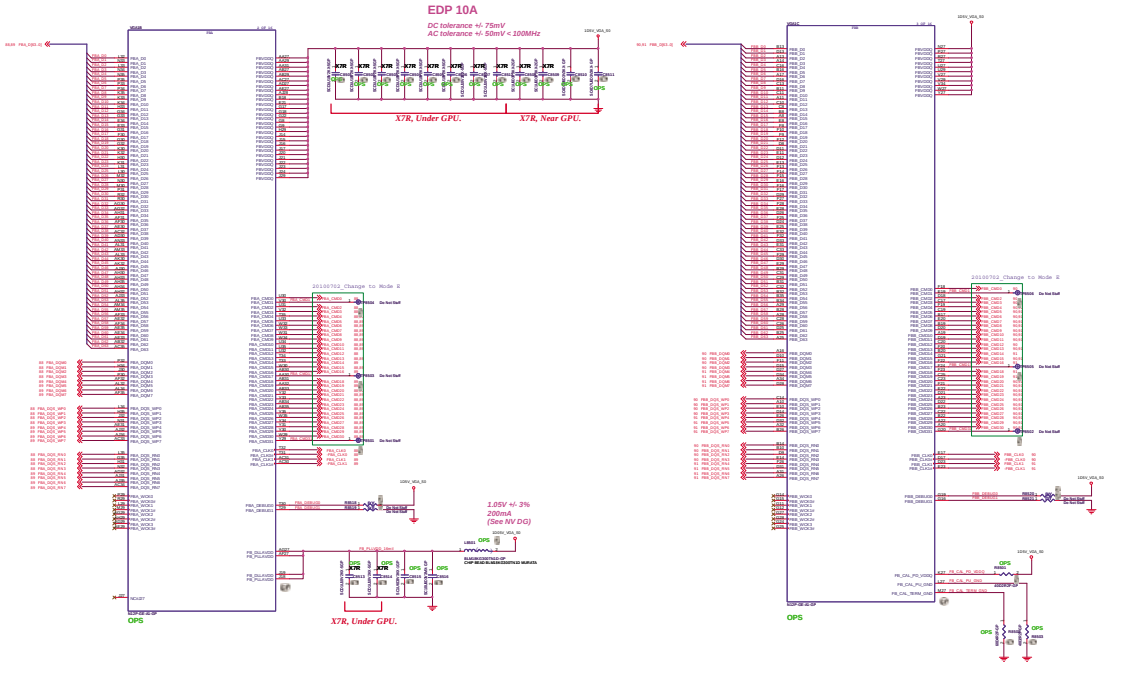
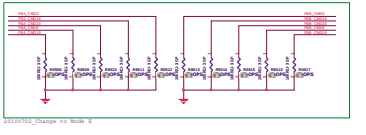
Title: N12P-Q1/Q3 (2/6): DIGITAL OUT

Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 84 of 102



FBCLK Termination place on VRAM side



FBCLK Termination place on VRAM side

倉制資訊	Wistron Corporation 21F, No. 88, Hsin Tai Wu Road, Hsichih Taipei Hsien 221, Taiwan, R.O.C.
N12P-Q1/Q3 (3/8): VRAM I/F	
LZ57	3

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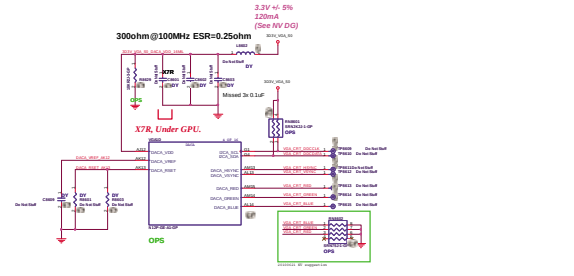
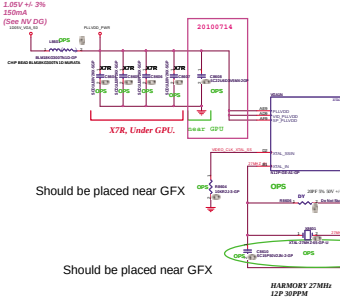
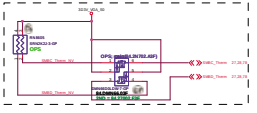
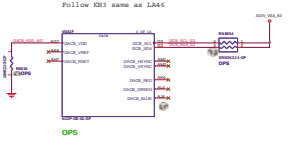








I2CA=>CRT, I2CC=>LVDS.

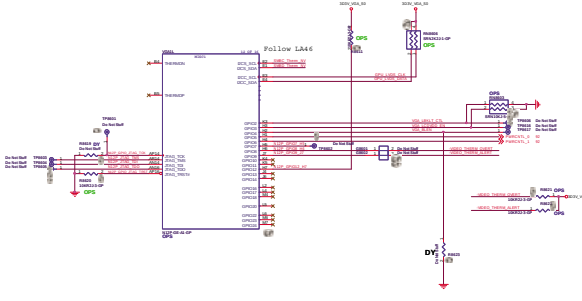
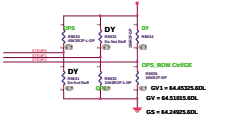


TABLE
VIDEO MEMORY

	HYNIX 128Mx16 0110 72.52G63.00U ~~72.52G63.A0U~~	SAMSUNG 128Mx16 0111 72.42164.C0U ~~72.42164.D0U~~	HYNIX 64Mx16 0010 72.51G63.C0U	Samsung 64Mx16 0011 72.41164.H0U
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

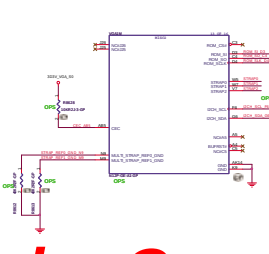


LOGIC

TABLE
NVIDIA

	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: TBD	N12P-GV1 DEV ID: 0xDF7	N11P-GS DEV ID: 0xDF0	N12M-GE DEV ID: 0xA7A 1010	N11M-GE2 DEV ID: 0xA70
STRAP2	PD R8635 30Kohm 64.30025.6DL	TBD	PD R8635 45Kohm 64.45325.6DL	PD R8635 5Kohm 64.51015.6DL	PU R8634 15Kohm 64.15025.6DL	PD R8635 5Kohm 64.51015.6DL

LOGIC



	N12P-GE	N12P-GV	N12P-GV1	N12M-GE	N11P-GS
ROM_SO	Pull-Low	Pull-high	Pull-Low	Pull-Low	Pull-Low
Stuff	R8617	R8625	R8617	R8617	R8617

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N12P-Q1/Q3 (4/6): GPIO
LZ57

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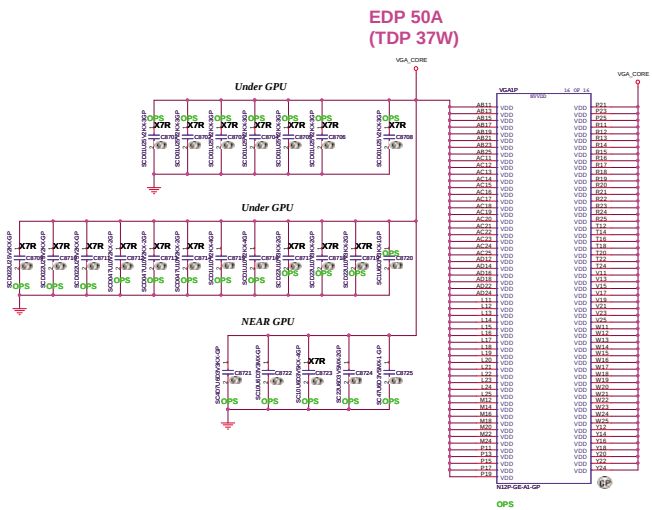

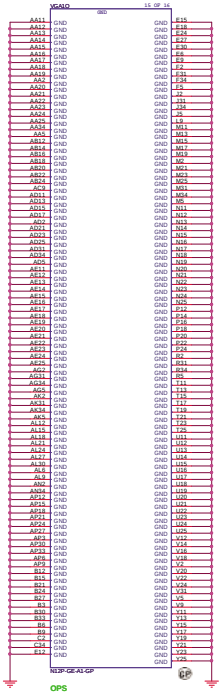

BOM

蜂創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	N12P-Q1/Q3 (5/6): POWER
Size: A2	Document Number: LZ57
Rev: -1	
Date: Tuesday, March 29, 2011	Sheet 87 of 100

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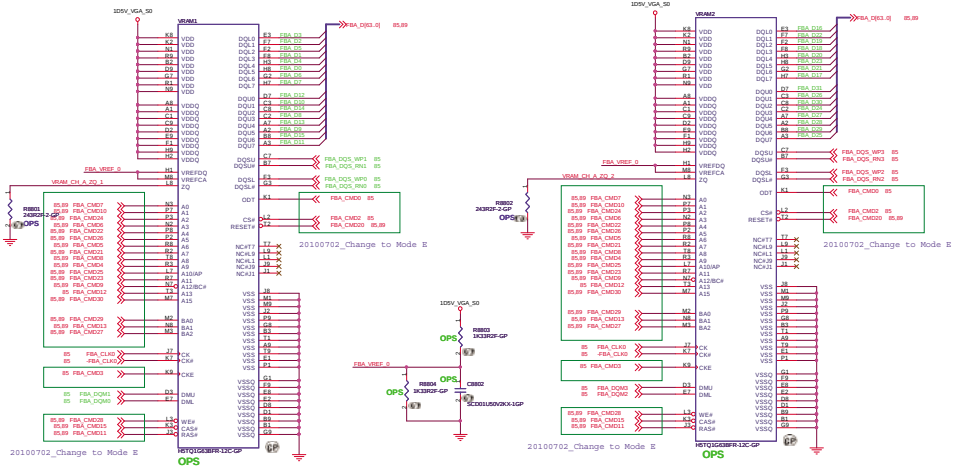
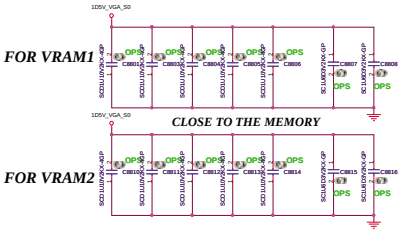


FB CMD mapping Mode D-N12x

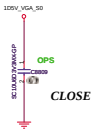
FOR VRAM1

FOR VRAM2



CLOSE TO THE MEMORY

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

BOM

蜂創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VRAM CHANNEL-A	
Size A2	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 88 of 102	

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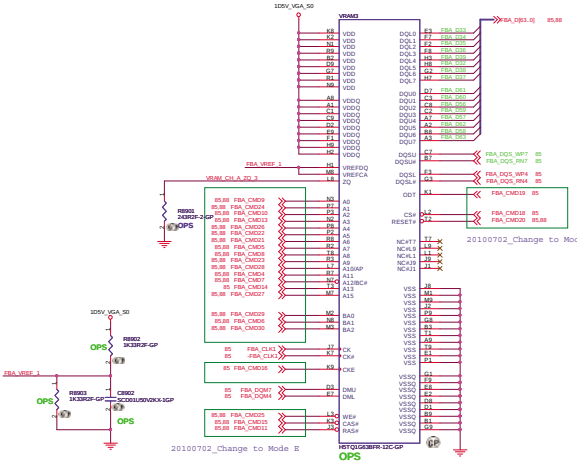
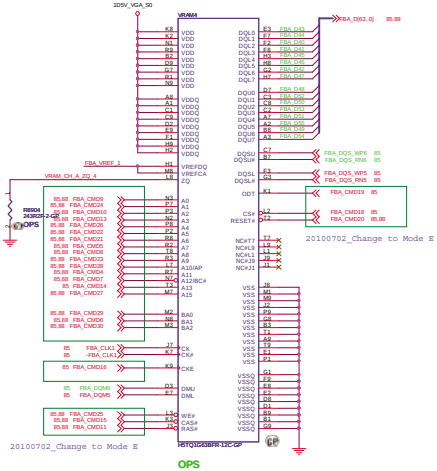
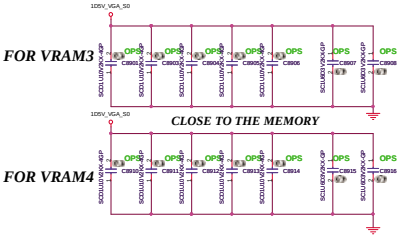




FB CMD mapping Mode D-N12x



CLOSE TO THE MEMORY

CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
File	**VRAM CHANNEL-A**
Size A2 / Document Number	LZ57 / Rev -1
Date: Tuesday, March 29, 2011	Sheet 89 of 102

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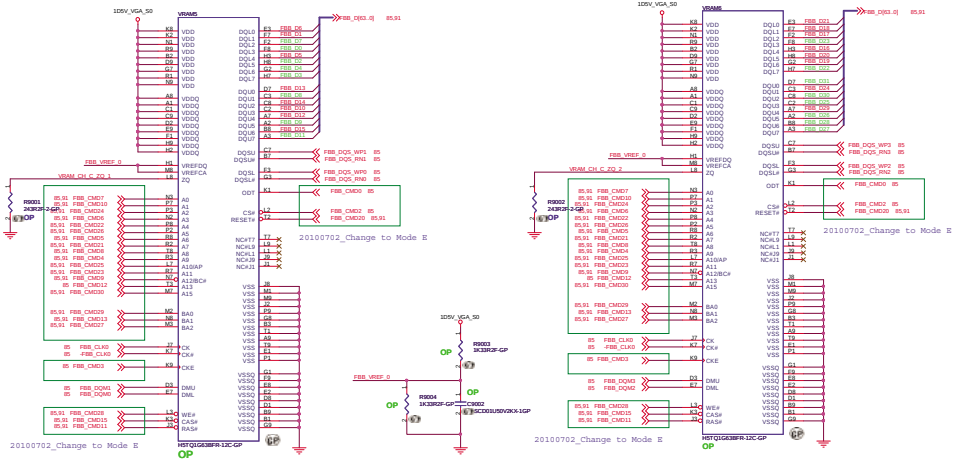
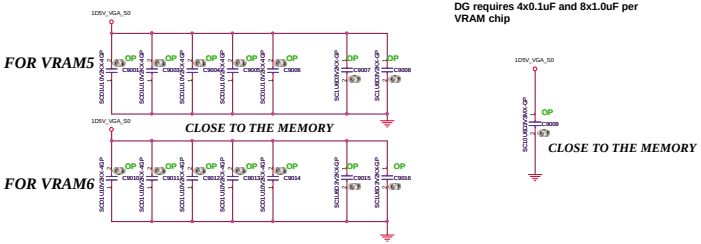


DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT C

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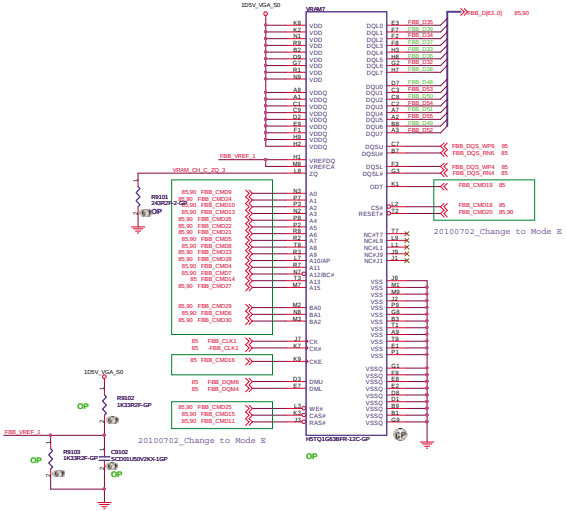
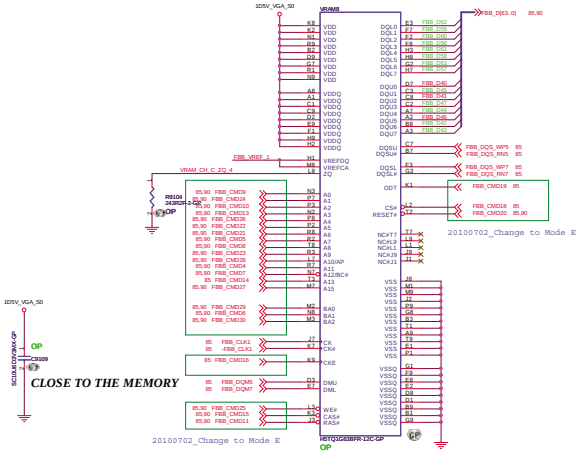
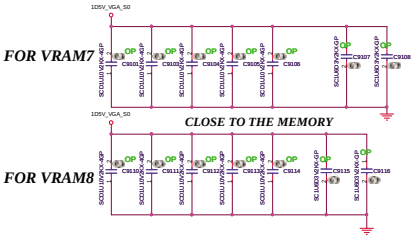
Title: VRAM CHANNEL-C

Size | Document Number | Rev







VIDEO FRAME BUFFER PORT C

BOM

緯創資通	Wistron Corporation 22F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VRAM CHANNEL-C	
Size A2	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 91 of 102	

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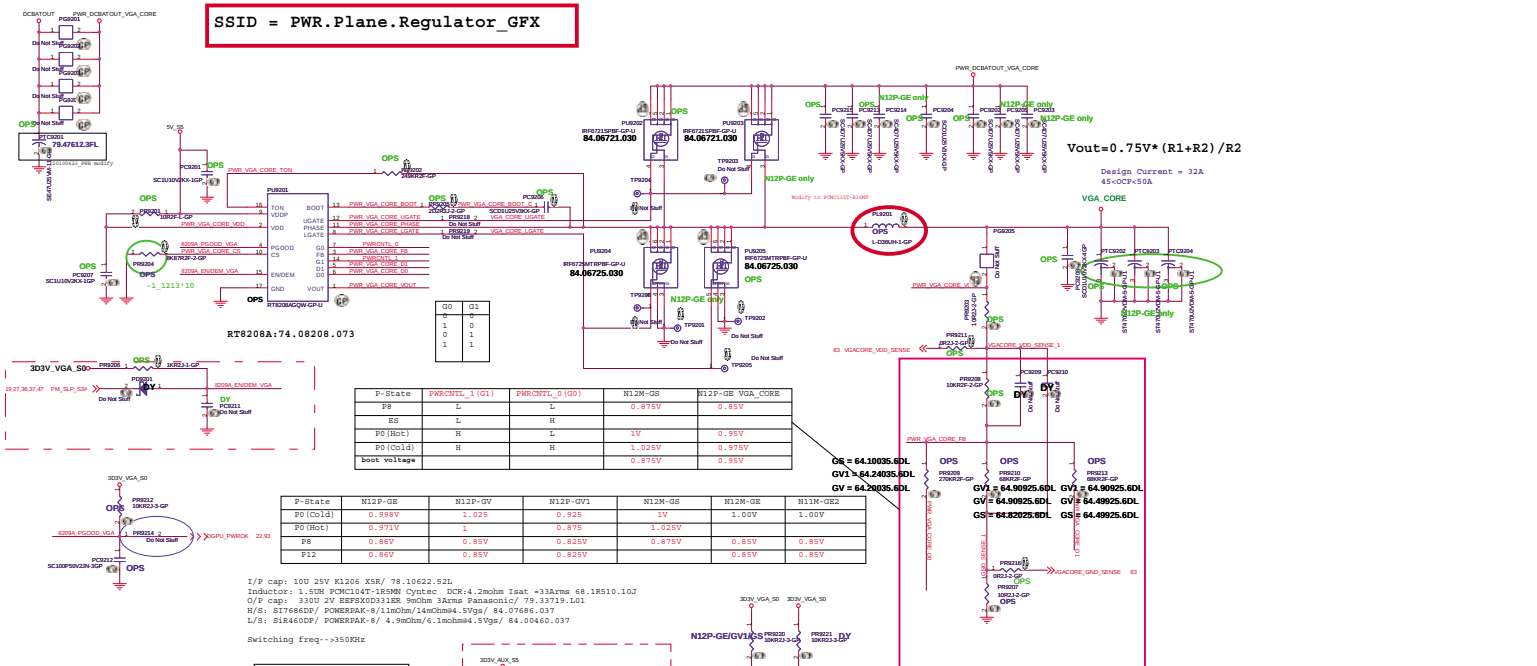
SSID = PWR.Plane.Regulator_GFX



G0	G1
0	0
1	0
0	1
1	1

P-State	PWRCNTL_1(G1)	PWRCNTL_0(G0)	N12M-GS	N12P-GE VGA_CORE
P8	L	L	0.875V	0.85V
KS	L	H		
P0(Hot)	H	L	1V	0.95V
P0(Cold)	H	H	1.025V	0.975V
boot voltage			0.875V	0.95V

P-State	N12P-GE	N12P-GV	N12P-GV1	N12M-GS	N12M-GE	N11M-GE2
P0(Cold)	0.998V	1.025	0.925	1V	1.00V	1.00V
P0(Hot)	0.971V	1	0.875	1.025V		
P8	0.86V	0.85V	0.825V	0.875V	0.85V	0.85V
P12	0.86V	0.85V	0.825V		0.85V	0.85V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: S17686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: S1R460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

	N12P-GE	N12P-GV1	N12P-GV	N12P-GS
P0(Cold)	0.998V	0.946V	1.048V	
P0(Hot)	0.971V	0.915V	1.011V	
P8/P12	0.86V	0.833V	0.86V	
Boot Voltage	0.971V	0.915V	0.86V	
PR9209	270k(64.27035.6DL)	240k(64.24035.6DL)	200k(64.20035.6DL)	
PR9210	68k(64.68025.6DL)	90.9k(64.90925.6DL)	68k(64.68025.6DL)	
PR9213	68k(64.68025.6DL)	90.9k(64.90925.6DL)	49.9k(64.49925.6DL)	

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Title: DC/DC_VGA CORE_RT8208B

Size: | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 52 of 102

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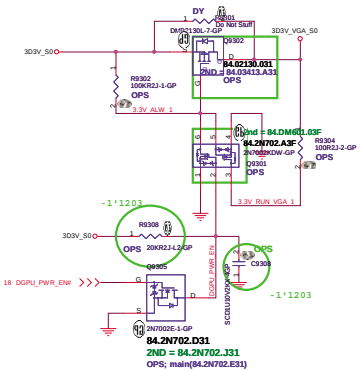
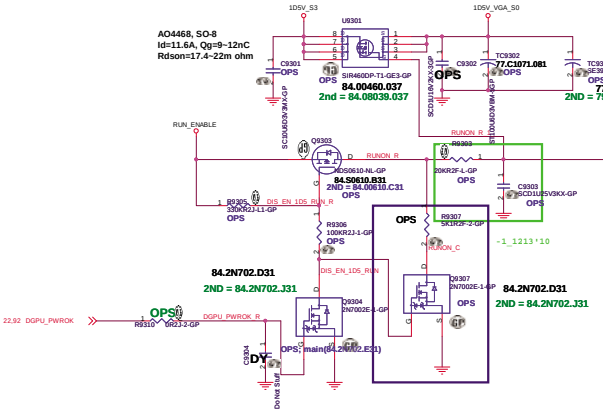
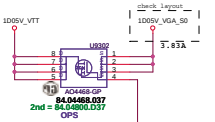
+3VS to 3.3V_DELAY Transfer



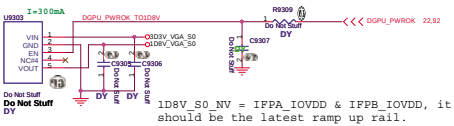
1D5V_VGA_S0



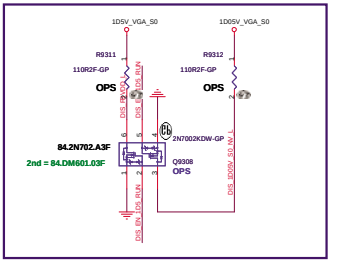
1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.



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Title: PCB PETT VGA POWER

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 26, 2013 Sheet 54 of 102

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Title	CRT Switch	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 95 of 102	

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緯創資通 **Wistron Corporation**

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Title	***TOUCH PANEL***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 96 of 102	

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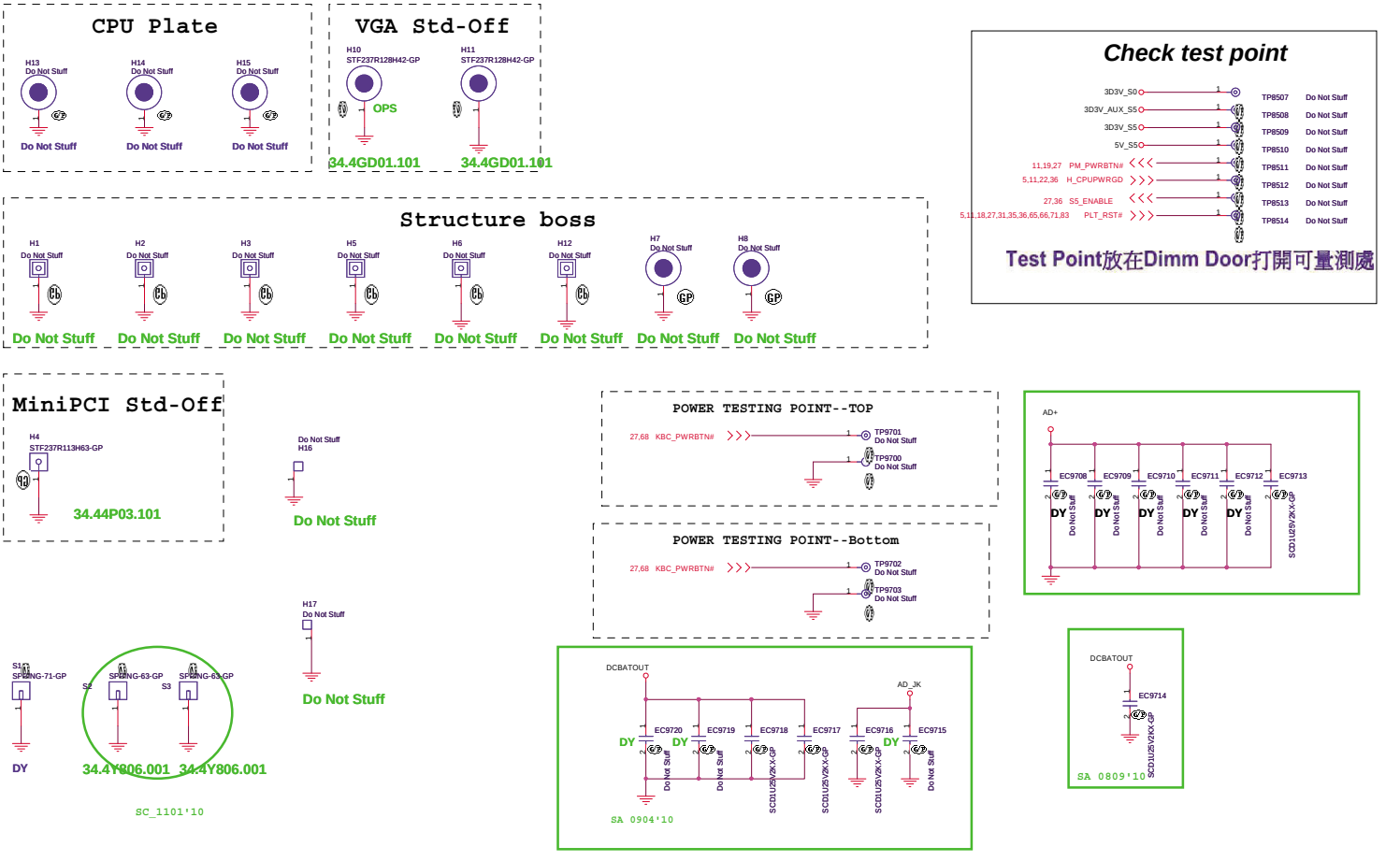

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Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 97 of 102

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Title	***Change History***
Size A4	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 98 of 102

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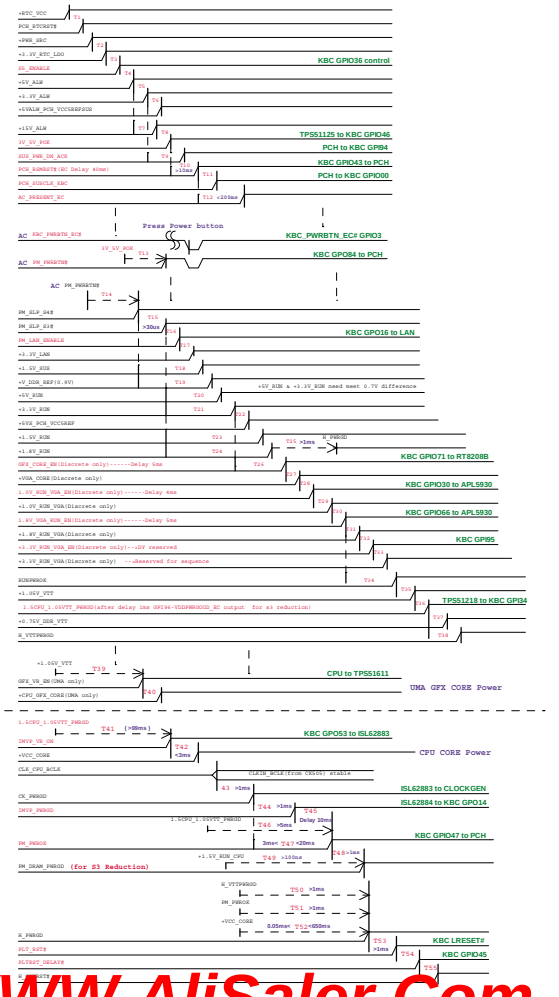
Intel-Power Up Sequence

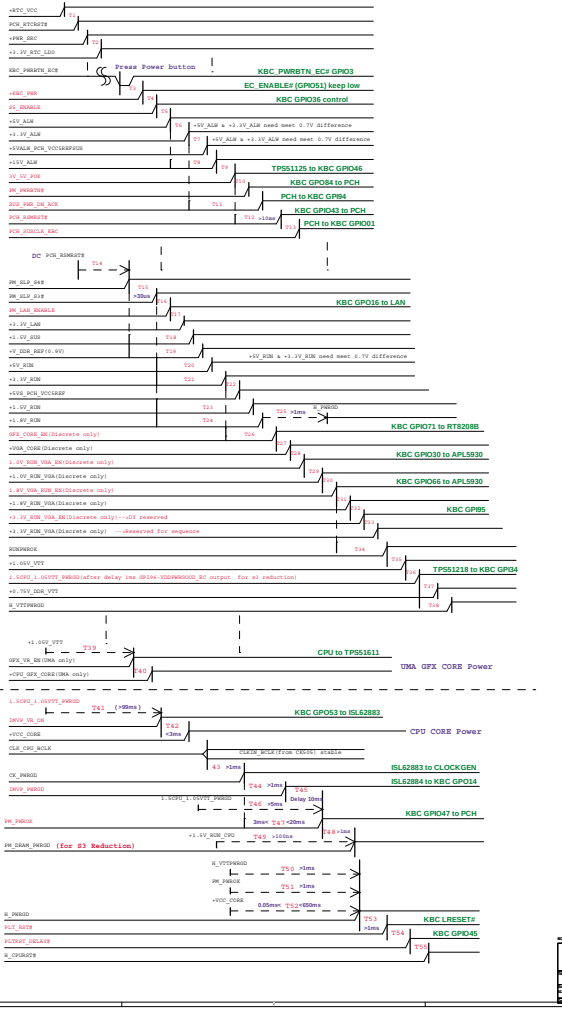
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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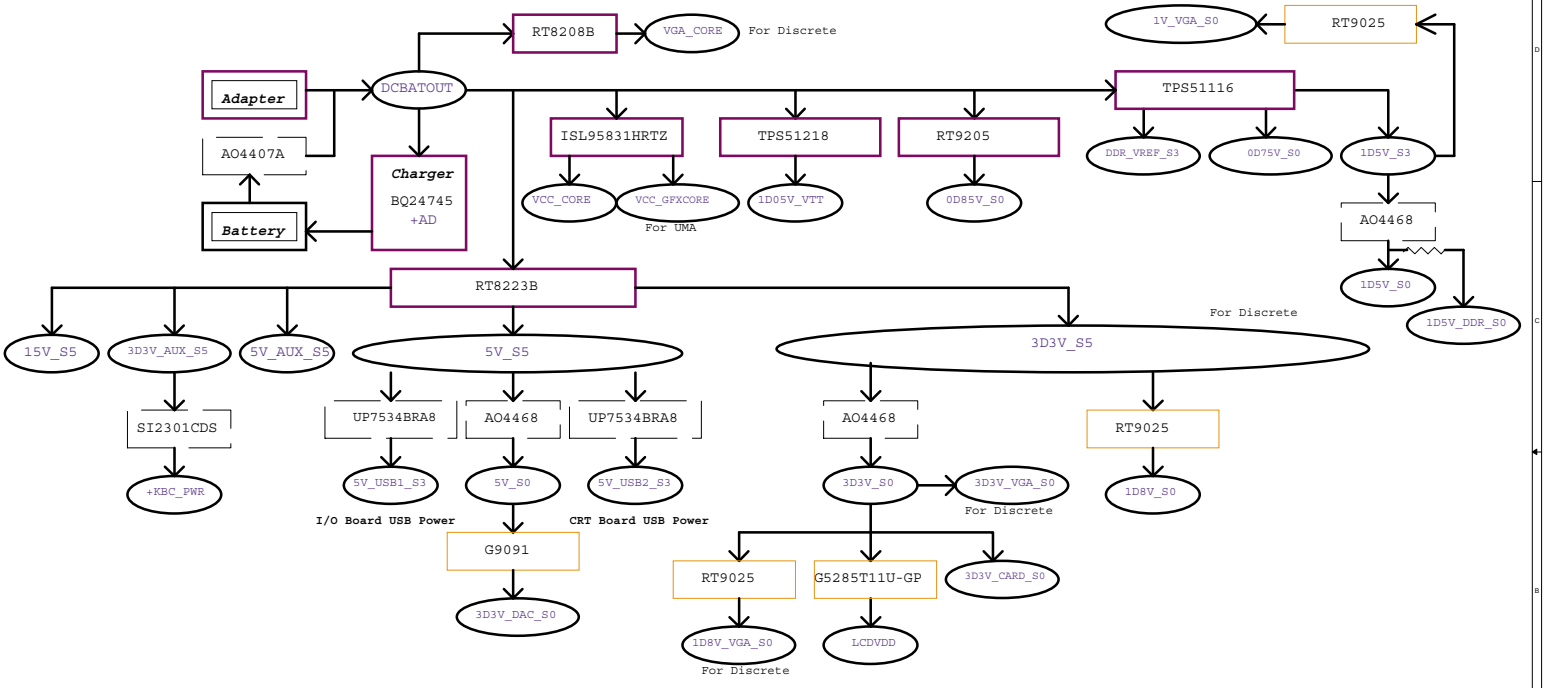
Power Sequence

LZ57

-3



Power Shape

Regulator	LDO	Switch

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Title: **Power Block Diagram**

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 100 of 102

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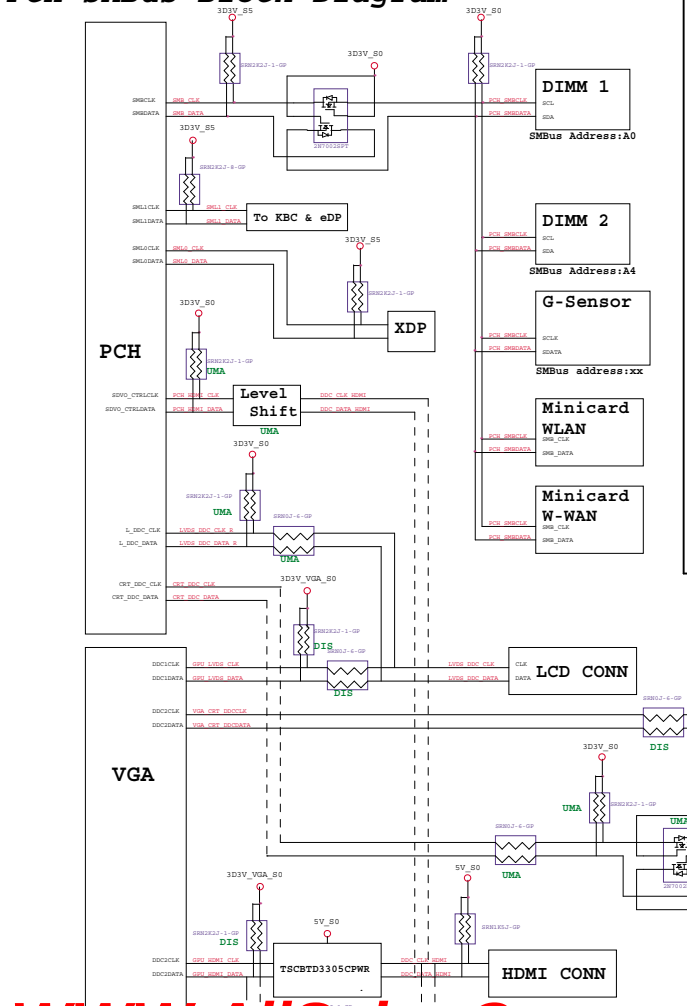
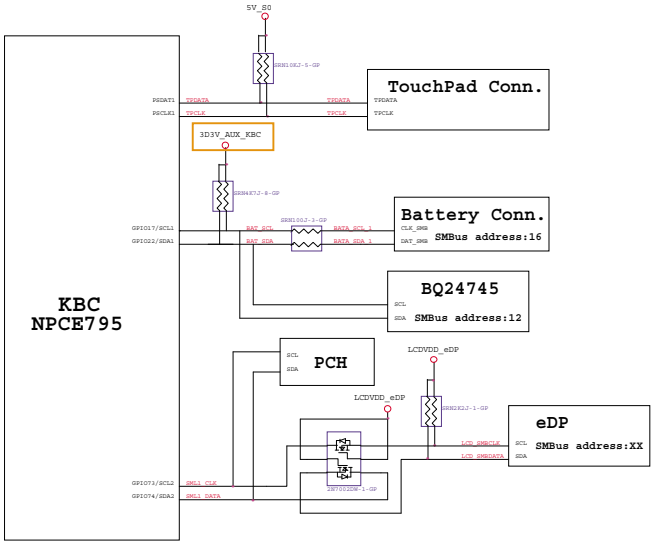
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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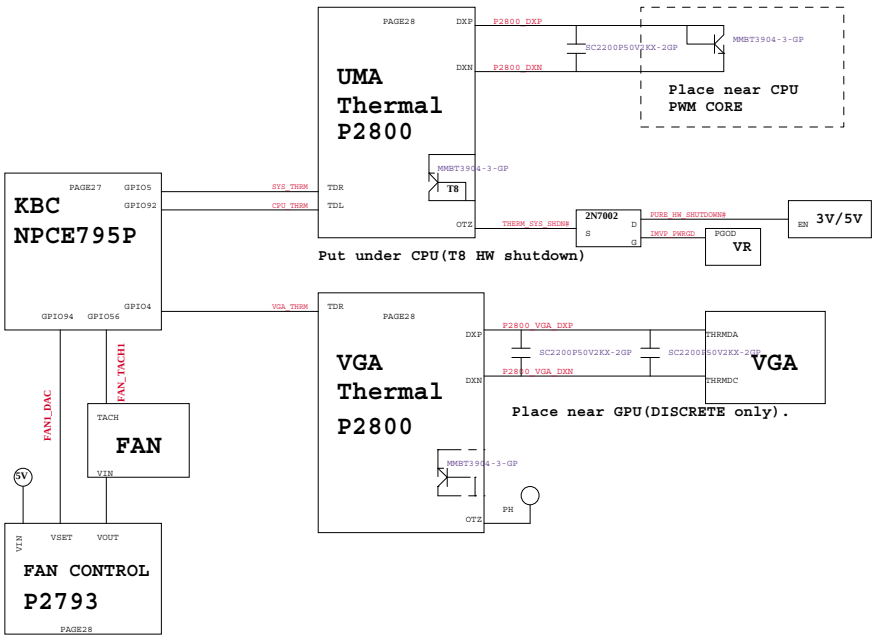
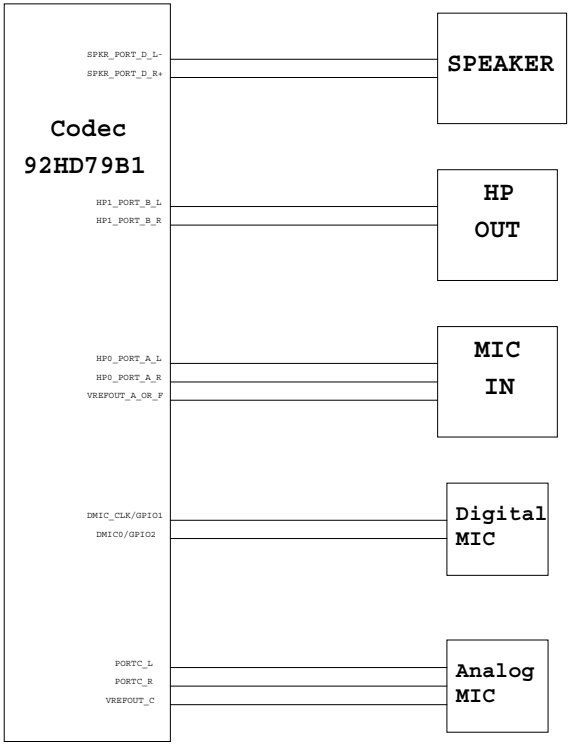
File	SMBUS Block Diagram		
Size A2	Document Number LZ57		Rev -1
Date: Tuesday, March 26, 2013	Sheet 3/31	of	100

Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
Size: Custom	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 102 of 102	

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