Compal Confidential

Schematic Document

Crestline_GM/PM+NB8M-GS & ICH8M

2007 / 1 / 2 Rev:0.4

Security Classification	Compal Secret Data		
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Title: *Cover Sheet*

Size: Custom | Document Number: *LA-4121P* | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 1 of 51

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Project Code: ANRJAL3000 (JAL30)

File Name : LA-4121P

JAL30 UMA/Discrete

Thermal Sensor ADM1032ARMZ P4

Mobile Merom uFCPGA-478 CPU P4, 5, 6

CK505 TSSOP-64 Clock Generator ICS 9LPRS365 P16

CRT & HDMI P15 , P39

Fan conn P4

LVDS Panel Interface P15

H_A#(3..35) H_D#(0..63) FSB 667/800MHz 1.05V

nVidia NB8M-GS P33 ~ 36

VRAM x 4 P37 , 38

Intel Crestline MCH FCBGA 1299 P7, 8, 9, 10, 11, 12

DDR2 667MHz 1.8V Dual Channel

DDR2-SO-DIMM X2 BANK 0, 1, 2, 3 P13, 14

CardBus Controller OZ129TN P25

PCI

DMI X4

C-Link

Media Card

1394

Express Card P26

PCIE2

PCI-E BUS

Intel ICH8M mBGA-676 P17, 18, 19, 20

USB0 USB conn x 1 P30

USB2.0

USB2,3 USB Conn x 2 On IO/B P30

Azalia

SATA0

PATA Slave

PCIE5 10/100/1000 LAN REALTEK RTL8111C-GR P22

PCIE4 Mini Card-1 (WLAN) P27

PCIE1 Mini Card-2 (Robson) P27

RJ45 CONN P22

LPC BUS

Option TPM1.2 P28

USB5 Express Card P26

USB6 Finger Printer P30

USB7 BT P27

USB8 Camera P30

USB9 Felica Conn P30

ENE KB926C0 P28

Touch Pad CONN. P29

Int.KBD P29

BIOS(System/EC) P28

Audio CKT ALC268 P23

AMP & Audio Jack P24

SATA HDD Connector P21

CDROM Conn. P21

Power On/Off CKT. P29

DC/DC Interface CKT. P31

RTC CKT. P18

Power Circuit DC/DC P40~47

Power OK CKT. P29

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Issued Date	2007/1/15	Deciphered Date	2008/1/15

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Title: **Block Diagram**

Size: Custom | Document Number: **LA-4121P** | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 2 of 51

Voltage Rails

O MEANS ON X MEANS OFF

State \ Power plane	+B	+3VALW		+5VS +3VS +1.8VS +1.25VS +CPU_CORE +VCCP	CLOCK
	0	0	0	0	0
S3	0	0		X	0
	0		X	X	0
S5 S4/ Battery only	0	X	X	X	X
	X	X	X	X	X

O MEANS ON
X MEANS OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra / Rc	100K +/- 5%

Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD21	0	PIRQE/PIRQF/PIRQG

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b?
EEPROM(24C16/02)	1010 000X b?
(24C04)	1011 000Xb?

EC SM Bus2 address

Device	Address
ADM1032	4D

ICH7 SM Bus address

Device	Address
Clock Generator (ICS ICS9LPR310)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM2	1001 010Xb?

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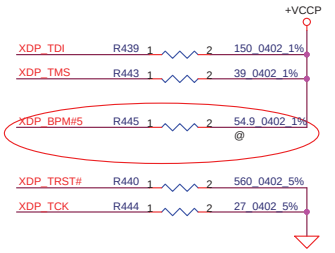
Issued Date	2007/1/15	Deciphered Date	2008/1/15

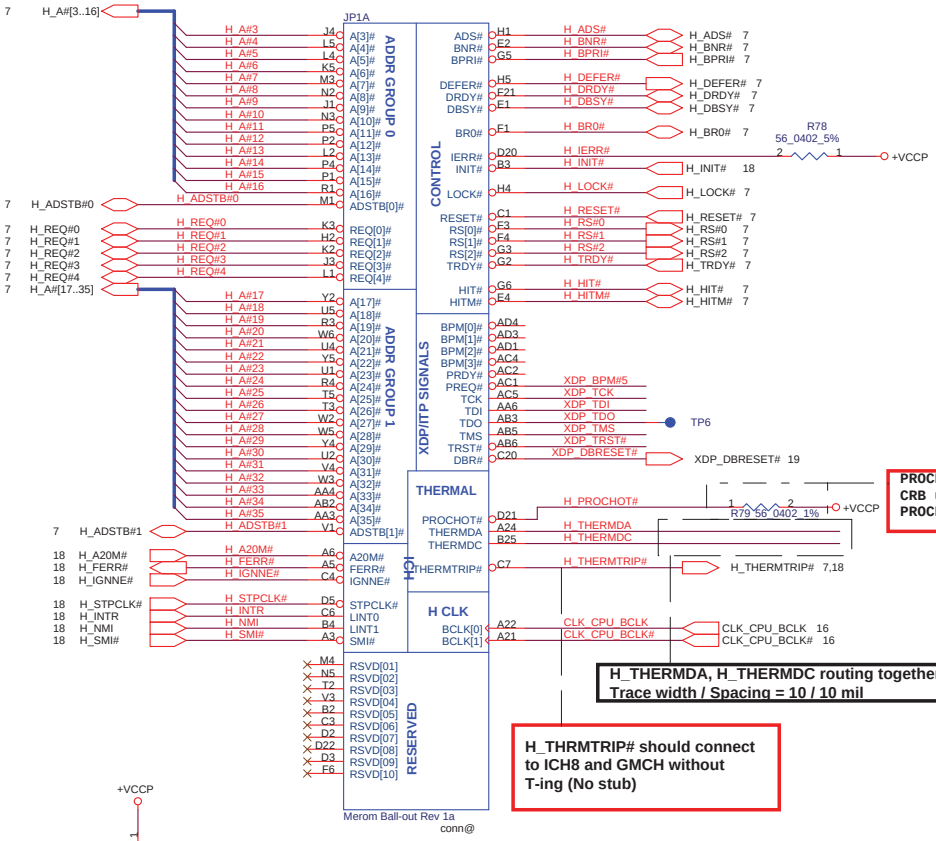
Title: Notes

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 3 of 51

XDP Reserve

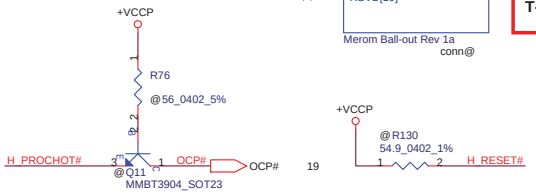




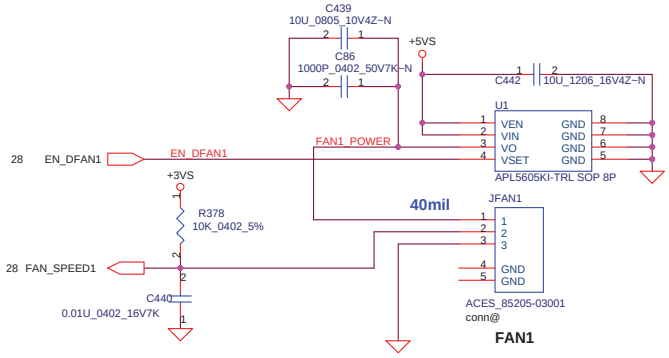
PROCHOT# is not used ---> 56 ohms pull-up
CRB uses 1K ohms pull-up resistor to fix
PROCHOT# failure when driven by a thermal sensor.

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

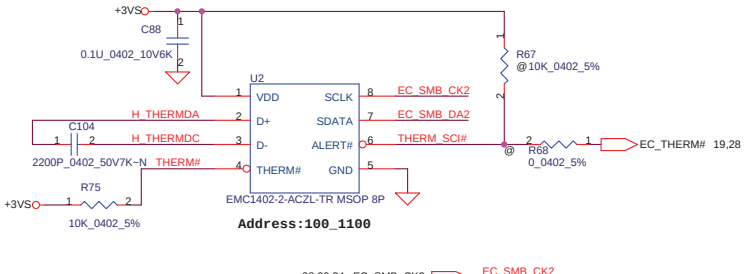
H_THRMTRIP# should connect to ICH8 and GMCH without T-ing (No stub)



FAN1 Control and Tachometer



Thermal Sensor EMC1402-2-ACZL-TR



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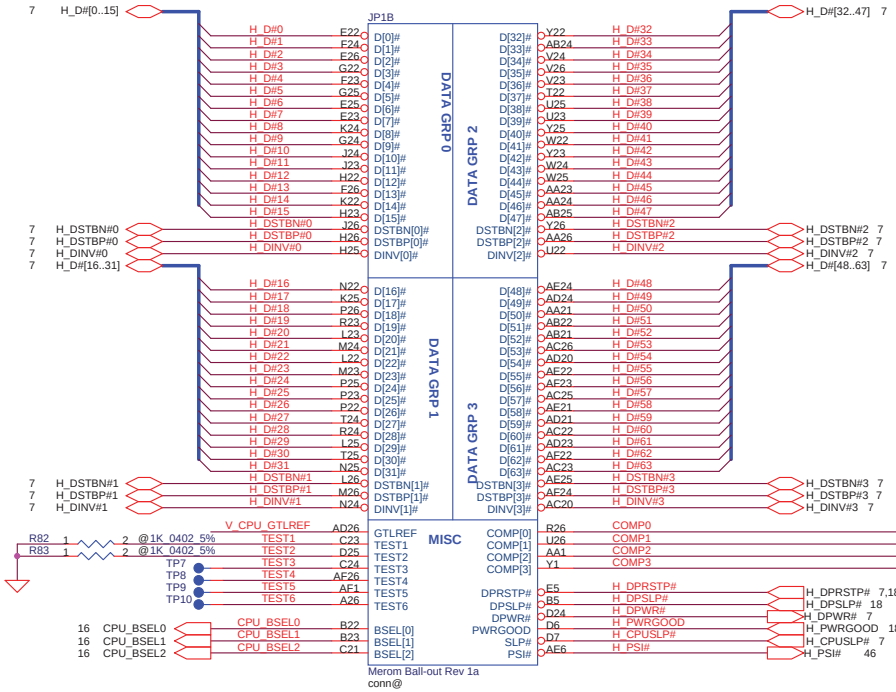
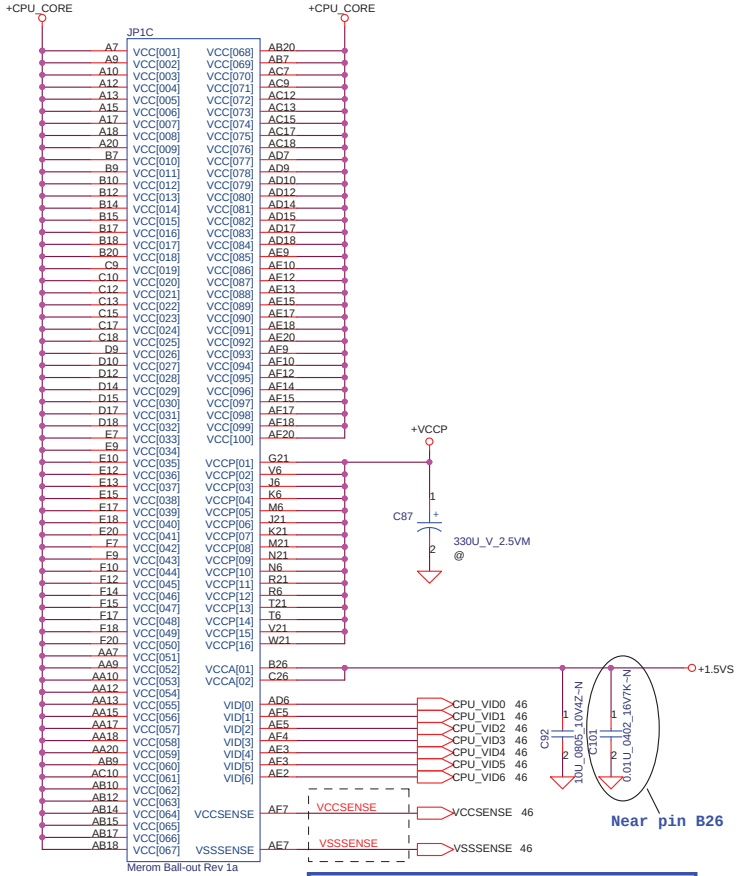
Title: Merom(1/3)-AGTL+/XDP

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 4 of 51



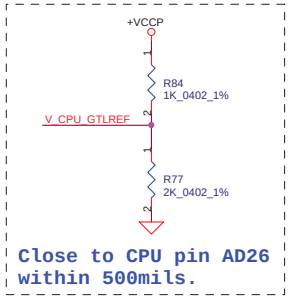


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

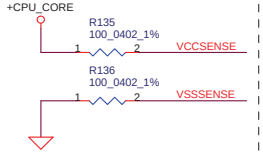
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.



Close to CPU pin AD26 within 500mils.



Close to CPU pin within 500mils.

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Compal Electronics, Inc.

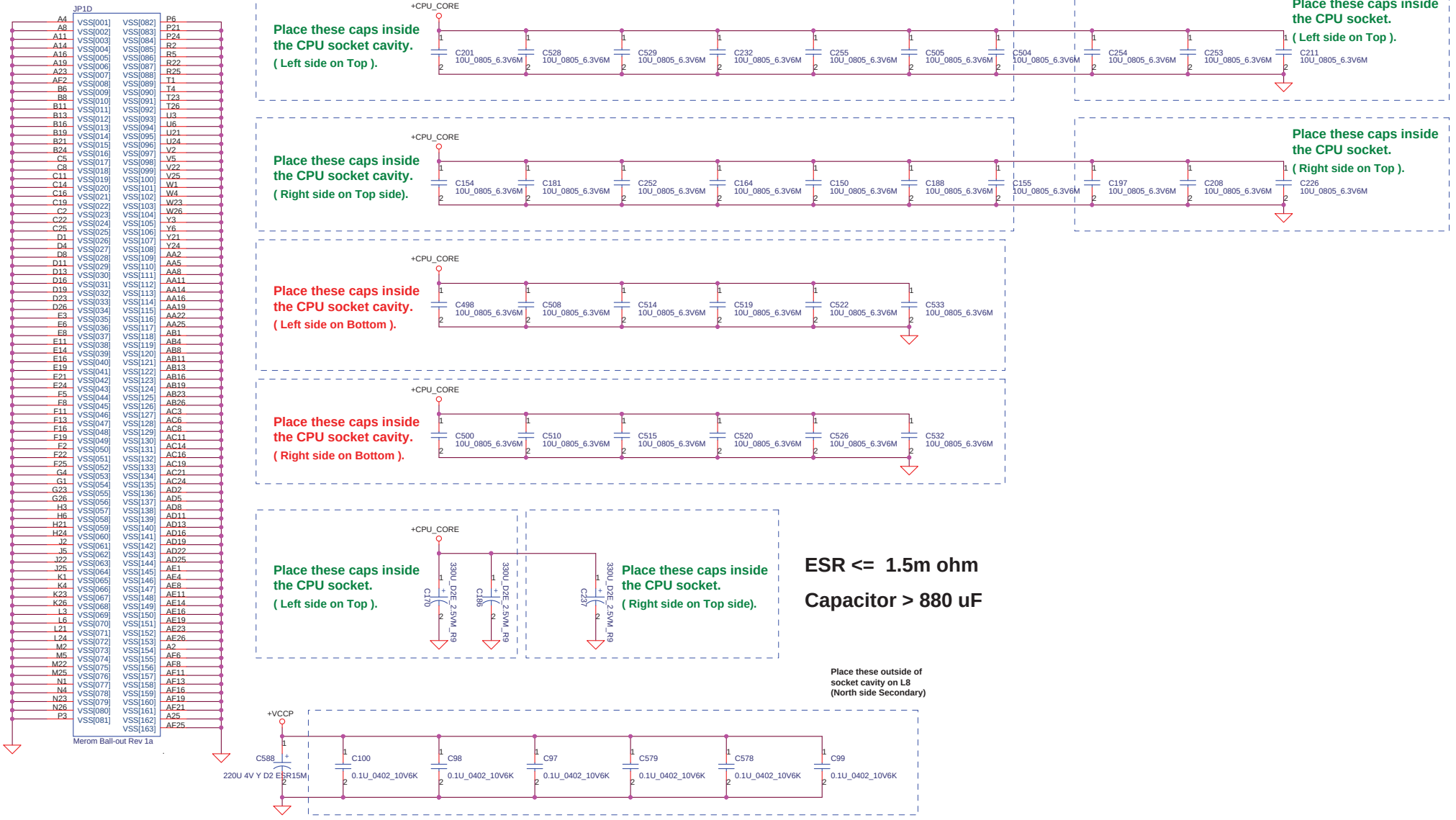
Title: Merom(2/3)-AGTL+/PWR

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 5 of 51

High Frequence Decoupling

10uF 0805 X5R -> 85 degree.



Security Classification	Compal Secret Data		
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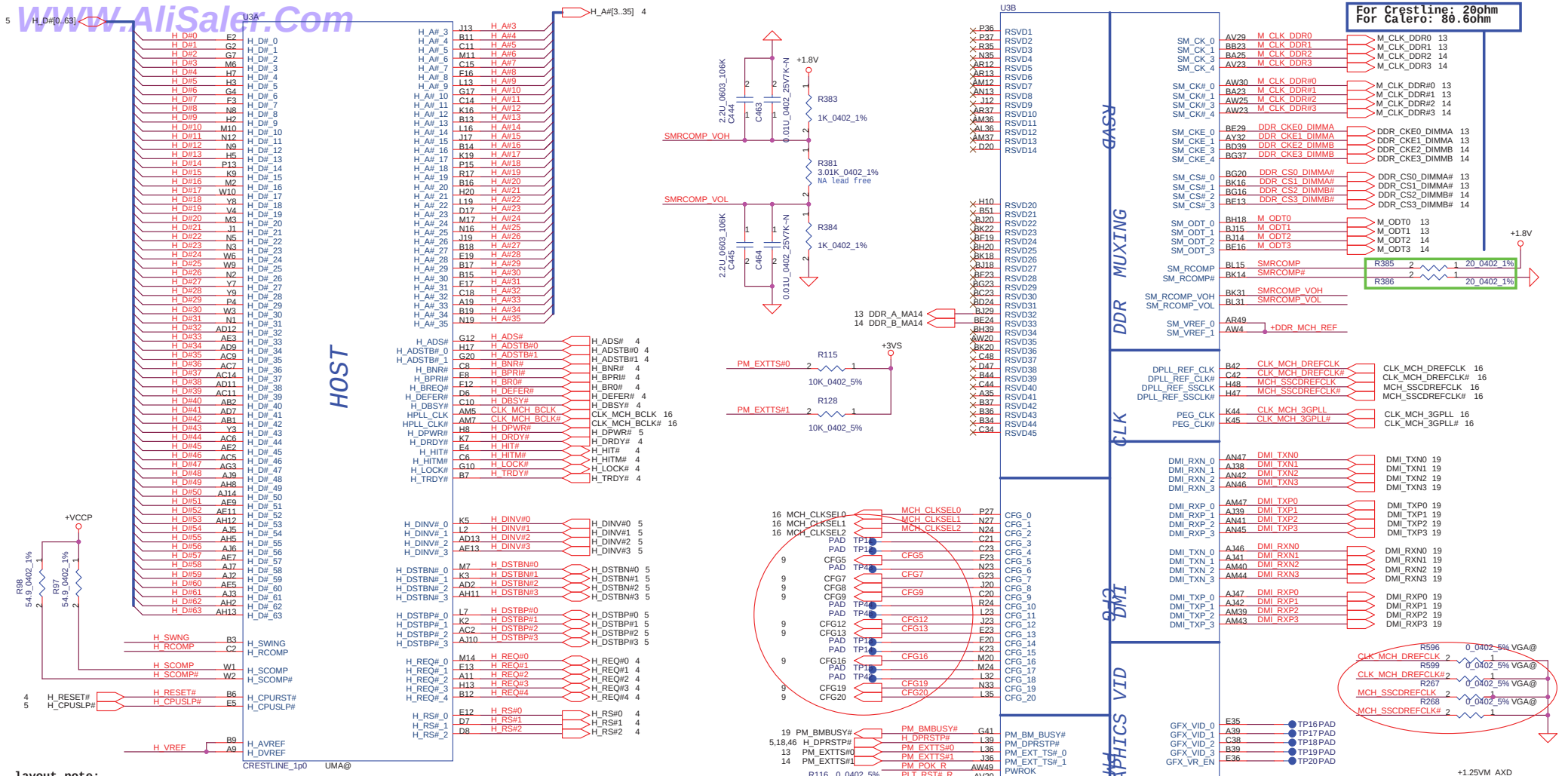
Compal Electronics, Inc.			
Title: Merom(3/3)-GND&Bypass			
Size: Custom	Document Number: LA-4121P		Rev: 0.4
Date: Thursday, January 10, 2008	Sheet 6 of 51		



Security Classification	Compal Secret Data		
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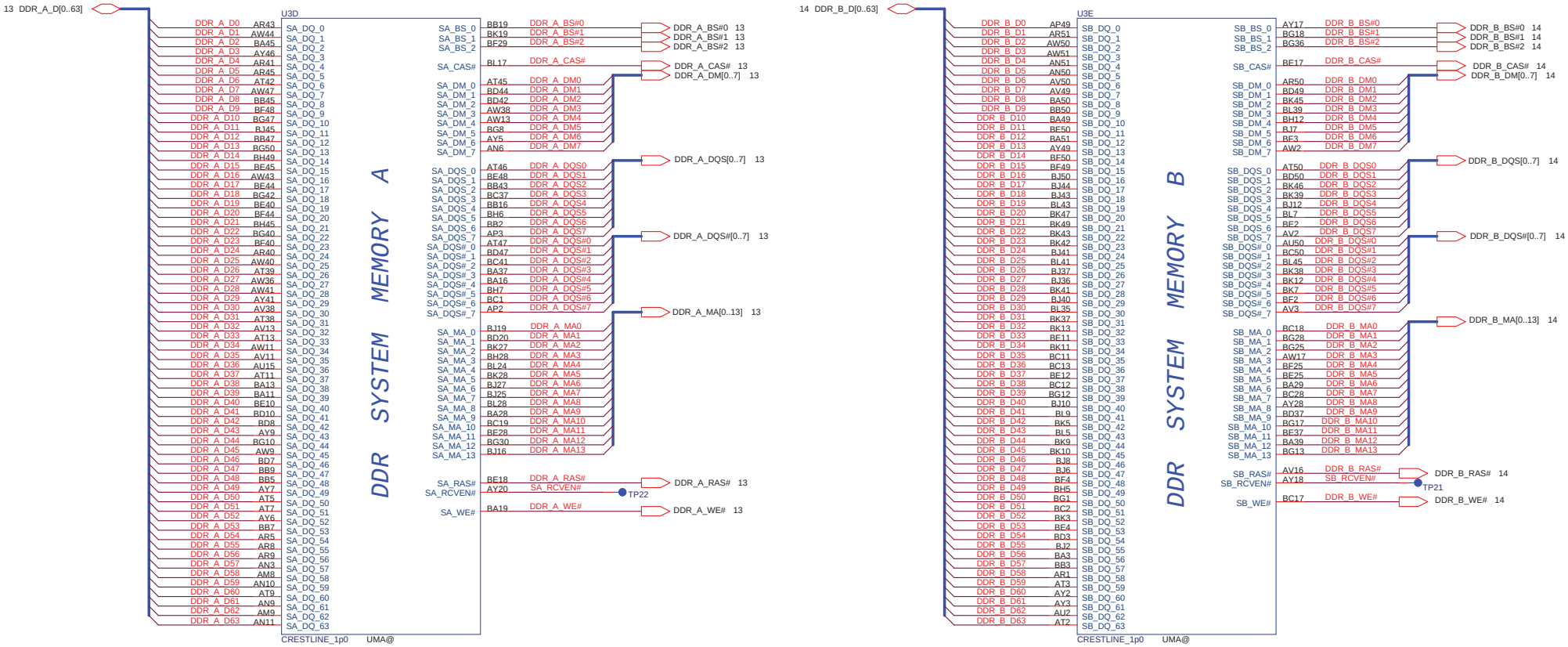
Compal Electronics, Inc.

Title: CRESTLINE(1/6)-AGTL+/DMI/DDR2

Size	Document Number	Rev
Custom	LA-4121P	0.4

Date: Thursday, January 10, 2008 Sheet 7 of 51



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: CRESTLINE(2/6)-DDR2 A/B CH

Size	Document Number	Rev
Custom	LA-4121P	0.4

Date: Thursday, January 10, 2008 Sheet 8 of 51

For Crestline:2.4kohm
For Calero: 1.5Kohm

PEGCOMP trace width
and spacing is 20/25 mils.

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational. * 1 = PCIE/SDVO are operating simu.

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

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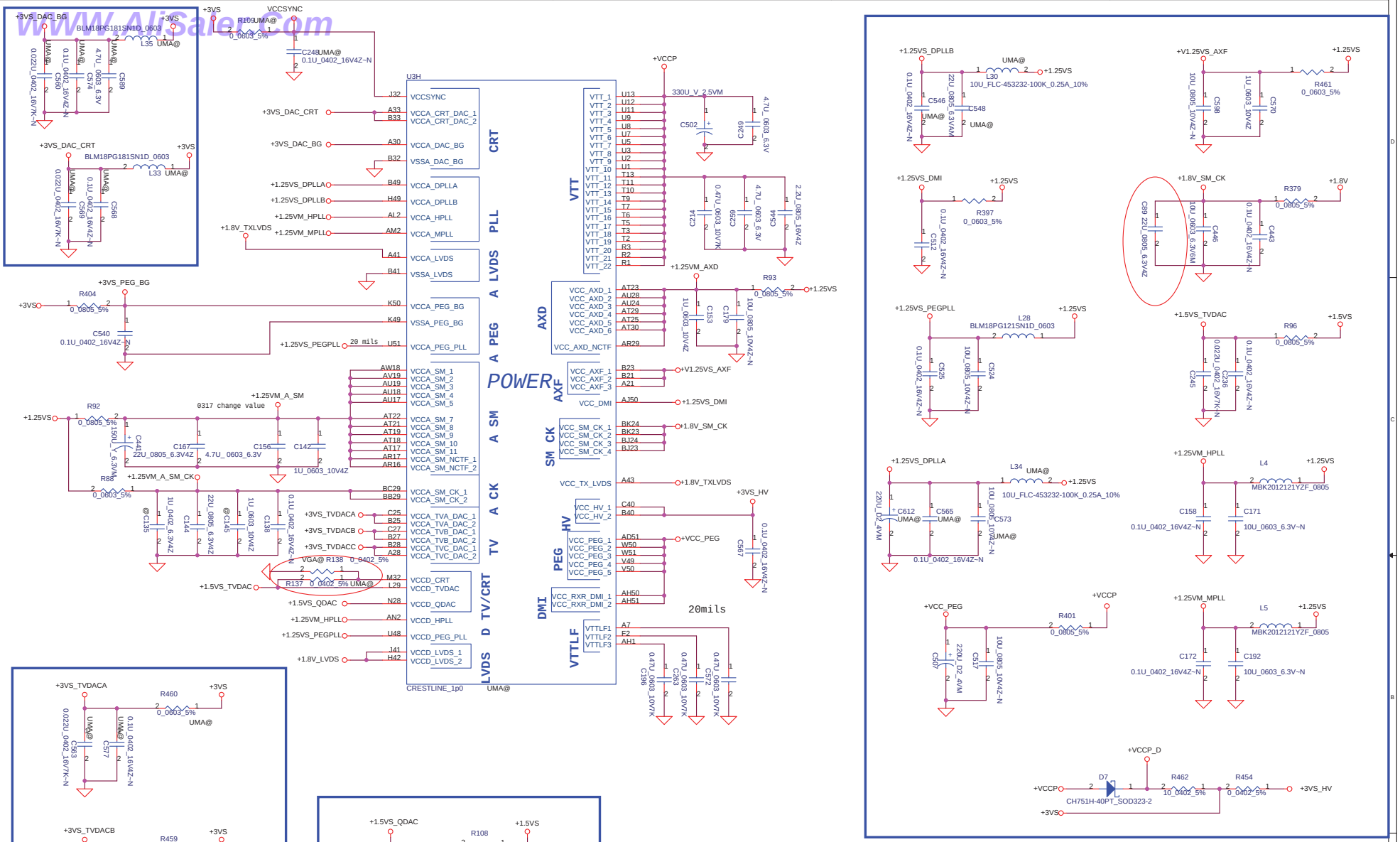
Title: CRESTLINE(3/6)-VGA/LVDS/TV

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 9 of 51



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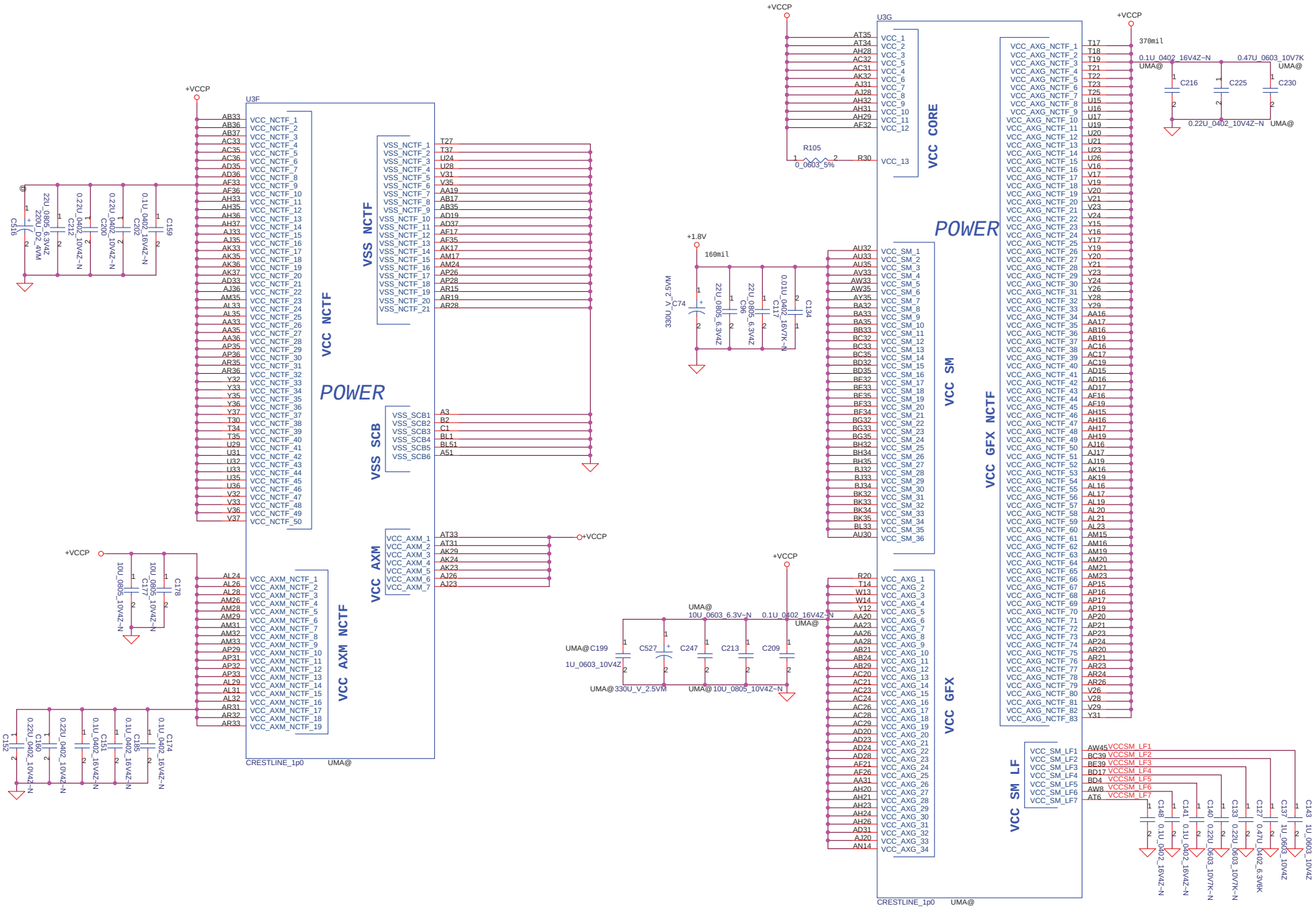
Title	CRESTLINE(4/6)-PWR		
Size: Custom	Document Number: LA-4121P		Rev: 0.4
Date: Thursday, January 10, 2008	Sheet 10 of 51		



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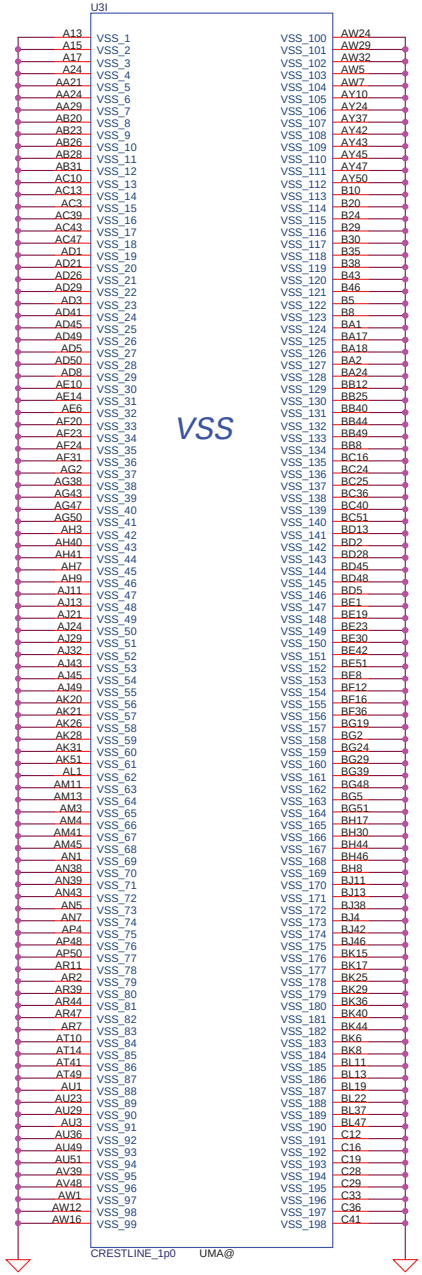
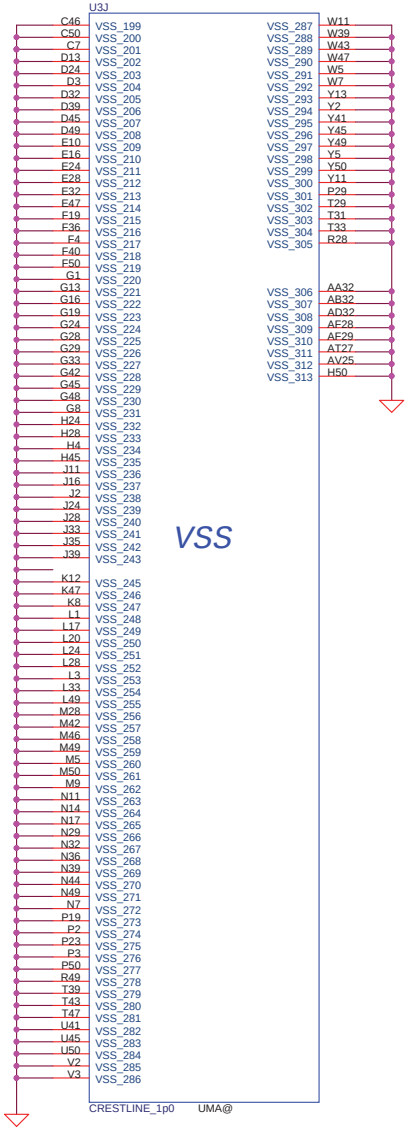
Compal Electronics, Inc.			
Title: CRESTLINE(5/6)-PWR/GND			
Size: Custom	Document Number: LA-4121P		Rev: 0.4
Date: Thursday, January 10, 2008	Sheet 11 of 51		





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Title: CRESTLINE(6/6)-PWR/GND

Size	Document Number	Rev
Custom	LA-4121P	0.4

Date: Thursday, January 10, 2008 Sheet 12 of 51

8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]

Layout Note:
+DDR_MCH_REF trace width and spacing is 20/20.

14 +DDR_MCH_REF1 → +DDR_MCH_REF1 → N-ZV6V1_20P_0.1U_85C → close to connector

+1.8V → R58 1K_0402_1% → +DDR_MCH_REF1 → R59 1K_0402_1%

Layout Note:
Place near JDIM1

+1.8V
C50 2.2U_0603_6.3V6K
C436 2.2U_0603_6.3V6K
C435 2.2U_0603_6.3V6K
C437 2.2U_0603_6.3V6K
C51 2.2U_0603_6.3V6K
C54 0.1U_0402_16V4Z
C434 0.1U_0402_16V4Z
C433 0.1U_0402_16V4Z
C55 0.1U_0402_16V4Z
C75 330U_D2E_2.5VM_R7

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

+0.9VS
DDR_A_V
C70 C68 C52 C69 C71 C59 C65 C62 C64 C53 C60 C63 C66 — 0.1U_0402_16V4Z

Layout Note:
Place these resistor closely JP41,all trace length Max=1.5"

DDR_A_V
RP27 56_0404_4P2R_5%: DDR_A_MA8, DDR_A_MA5
RP26 56_0404_4P2R_5%: DDR_CKE0_DIMMA, DDR_A_MA12
RP24 56_0404_4P2R_5%: DDR_A_MA1, DDR_A_MA3
RP19 56_0404_4P2R_5%: DDR_A_MA7, DDR_A_MA6
RP16 56_0404_4P2R_5%: DDR_A_RAS#, DDR_CS0_DIMMA#
RP25 56_0404_4P2R_5%: DDR_A_BS#2, DDR_A_MA9
RP23 56_0404_4P2R_5%: DDR_A_BS#0, DDR_A_MA10
RP18 56_0404_4P2R_5%: DDR_A_MA2, DDR_A_MA4
RP22 56_0404_4P2R_5%: DDR_A_CAS#, DDR_A_WE#
RP17 56_0404_4P2R_5%: DDR_A_BS#1, DDR_A_MA0
RP21 56_0404_4P2R_5%: DDR_CS1_DIMMA#, M_ODT1
RP15 56_0404_4P2R_5%: M_ODT0, DDR_A_MA13
RP20 56_0404_4P2R_5%: DDR_CKE1_DIMMA, DDR_A_MA11, DDR_A_MA14
R55 56_0402_5%

Close to VREF pins of SO-DIMM

+DDR_MCH_REF1 → C72 2.2U_0805_16V4Z, C67 0.1U_0402_16V4Z

+1.8V → JDIM1

	1	VREF	VSS	2	
DDR_A_D4	3	VSS	DQ4	4	DDR_A_D6
DDR_A_D1	5	DQ0	DQ5	6	DDR_A_D0
	7	DQ1	VSS	8	
DDR_A_DQS#0	9	VSS	DM0	10	DDR_A_DM0
DDR_A_DQS0	11	DQS0#	VSS	12	
	13	DQS0	DQ6	14	DDR_A_D5
	15	VSS	DQ7	16	DDR_A_D7
DDR_A_D2	17	DQ2	VSS	18	
DDR_A_D3	19	VSS	DQ12	20	DDR_A_D13
	21	DQ3	DQ13	22	DDR_A_D12
DDR_A_D8	23	VSS	VSS	24	
DDR_A_D14	25	DQ8	DM1	26	DDR_A_DM1
	27	DQ9	VSS	28	
DDR_A_DQS#1	29	VSS	CK0	30	M_CLK_DDR0 7
DDR_A_DQS1	31	DQS1#	CK0#	32	M_CLK_DDR#0 7
	33	DQS1	VSS	34	
DDR_A_D9	35	VSS	DQ14	36	DDR_A_D11
DDR_A_D15	37	DQ10	DQ15	38	DDR_A_D10
	39	DQ11	VSS	40	
	41	VSS	VSS	42	
DDR_A_D16	43	DQ16	DQ20	44	DDR_A_D20
DDR_A_D17	45	DQ17	DQ21	46	DDR_A_D21
	47	VSS	VSS	48	
DDR_A_DQS#2	49	DQS2#	NC	50	PM_EXTTS#0 7
DDR_A_DQS2	51	DQS2	DM2	52	DDR_A_DM2
	53	VSS	VSS	54	
DDR_A_D18	55	DQ18	DQ22	56	DDR_A_D23
DDR_A_D19	57	DQ19	DQ23	58	DDR_A_D22
	59	VSS	VSS	60	
DDR_A_D29	61	DQ24	DQ28	62	DDR_A_D28
DDR_A_D24	63	DQ25	DQ29	64	DDR_A_D25
	65	VSS	VSS	66	
DDR_A_DM3	67	DM3	DQS3#	68	DDR_A_DQS#3
	69	NC	DQS3	70	DDR_A_DQS3
	71	VSS	VSS	72	
DDR_A_D26	73	DQ26	DQ30	74	DDR_A_D31
DDR_A_D27	75	DQ27	DQ31	76	DDR_A_D30
	77	VSS	VSS	78	
7 DDR_CKE0_DIMMA	79	CKE0	NC/CKE1	80	DDR_CKE1_DIMMA → DDR_CKE1_DIMMA 7
	81	VDD	VDD	82	
	83	NC	NC/A15	84	
8 DDR_A_BS#2	85	BA2	NC/A14	86	DDR_A_MA14 → DDR_A_MA14 7
	87	VDD	VDD	88	
DDR_A_MA12	89	A12	A11	90	DDR_A_MA11
DDR_A_MA9	91	A9	A7	92	DDR_A_MA7
DDR_A_MA8	93	A8	A6	94	DDR_A_MA6
	95	VDD	VDD	96	
DDR_A_MA5	97	A5	A4	98	DDR_A_MA4
DDR_A_MA3	99	A3	A2	100	DDR_A_MA2
DDR_A_MA1	101	A1	A0	102	DDR_A_MA0
	103	VDD	VDD	104	
DDR_A_MA10	105	A10/AP	BA1	106	DDR_A_BS#1 → DDR_A_BS#1 8
8 DDR_A_BS#0	107	BA0	RAS#	108	DDR_A_RAS# → DDR_A_RAS# 8
8 DDR_A_WE#	109	WE#	S0#	110	DDR_CS0_DIMMA# → DDR_CS0_DIMMA# 7
	111	VDD	VDD	112	
8 DDR_A_CAS#	113	CAS#	ODT0	114	M_ODT0 → M_ODT0 7
7 DDR_CS1_DIMMA#	115	NC/S1#	NC/A13	116	DDR_A_MA13
	117	VDD	VDD	118	
7 M_ODT1	119	NC/ODT1	NC	120	
	121	VSS	VSS	122	
DDR_A_D37	123	DQ32	DQ36	124	DDR_A_D32
DDR_A_D36	125	DQ33	DQ37	126	DDR_A_D33
	127	VSS	VSS	128	
DDR_A_DQS#4	129	DQS4#	DM4	130	DDR_A_DM4
DDR_A_DQS4	131	DQS4	VSS	132	
	133	VSS	DQ38	134	DDR_A_D39
DDR_A_D35	135	DQ34	DQ39	136	DDR_A_D38
DDR_A_D34	137	DQ35	VSS	138	
	139	VSS	DQ44	140	DDR_A_D45
DDR_A_D40	141	DQ40	DQ45	142	DDR_A_D43
DDR_A_D44	143	DQ41	VSS	144	
	145	VSS	DQS5#	146	DDR_A_DQS#5
DDR_A_DM5	147	DM5	DQS5	148	DDR_A_DQS5
	149	VSS	VSS	150	
DDR_A_D41	151	DQ42	DQ46	152	DDR_A_D47
DDR_A_D46	153	DQ43	DQ47	154	DDR_A_D42
	155	VSS	VSS	156	
DDR_A_D49	157	DQ48	DQ52	158	DDR_A_D52
DDR_A_D48	159	DQ49	DQ53	160	DDR_A_D53
	161	VSS	VSS	162	
	163	NC,TEST	CK1	164	M_CLK_DDR1 → M_CLK_DDR1 7
DDR_A_DQS#6	165	VSS	CK1#	166	M_CLK_DDR#1 → M_CLK_DDR#1 7
DDR_A_DQS6	167	DQS6#	VSS	168	
	169	DQS6	DM6	170	DDR_A_DM6
DDR_A_D54	171	VSS	VSS	172	
DDR_A_D50	173	DQ50	DQ54	174	DDR_A_D51
	175	DQ51	DQ55	176	DDR_A_D55
DDR_A_D61	177	VSS	VSS	178	
DDR_A_D60	179	DQ56	DQ60	180	DDR_A_D57
	181	DQ57	DQ61	182	DDR_A_D56
DDR_A_DM7	183	VSS	VSS	184	
	185	DM7	DQS7#	186	DDR_A_DQS#7
	187	VSS	DQS7	188	DDR_A_DQS7
DDR_A_D59	189	DQ58	VSS	190	
DDR_A_D58	191	DQ59	DQ62	192	DDR_A_D62
	193	VSS	DQ63	194	DDR_A_D63
14,16,19 ICH_SM_DA	195	SDA	VSS	196	
14,16,19 ICH_SM_CLK	197	SCL	SA0	198	
+3VS	199	VDDSPD	SA1	200	

FOX_ASOA426-M2RN-7F

C61 0.1U_0402_16V4Z, C73 2.2U_0603_6.3V6K

R56 10K_0402_5%, R57 10K_0402_5%

SO-DIMM A
REVERSE
Bottom side

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.			
Title: DDR2 SO-DIMM I			
Size: Custom	Document Number: LA-4121P		Rev: 0.4
Date: Thursday, January 10, 2008	Sheet 13 of 51		

8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]

Layout Note:
Place near JDIM2

+1.8V
2.2U_0603_6.3V6K: C25, C28, C29, C27, C24
0.1U_0402_16V4Z: C57, C42, C26, C56
330U_D2E_2.5VM_R7: C79 @

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS
DDR_B_V
0.1U_0402_16V4Z: C33, C32, C30, C44, C36, C46, C31, C37, C45, C41, C40, C34, C35

Layout Note:
Place these resistor closely JP42,all trace length Max=1.5"

DDR_B_V
RP14: DDR_B_MA14, DDR_B_MA11 — RP6: DDR_B_MA7, DDR_B_MA9
RP12: DDR_B_MA8, DDR_B_MA5 — RP5: DDR_B_MA3, DDR_B_MA1
RP3: DDR_B_RAS#, DDR_B_BS#1 — RP13: DDR_B_MA12, DDR_B_MA6
RP9: DDR_B_CAS#, DDR_CS2_DIMMB# — RP4: DDR_B_MA0, DDR_B_MA4
RP10: DDR_B_WE#, DDR_B_BS#0 — RP11: DDR_B_MA2, DDR_B_MA10
RP8: DDR_CS3_DIMMB#, M_ODT3 — RP2: M_ODT2, DDR_B_MA13
RP7: DDR_CKE3_DIMMB, R49 10K_0402_5% — DDR_CKE2_DIMMB, DDR_B_BS#2
All: 56_0404_4P2R_5%

Close to VREF pins of SO-DIMM

+1.8V
+DDR_MCH_REF1 — +DDR_MCH_REF1 13
2.2U_0805_16V4Z: C39
0.1U_0402_16V4Z: C49

JDIM2 — FOX_AS0A426-NARN-7F-N

1	VREF	VSS	2		
3	VSS	DQ4	4	DDR_B_D0	DDR_B_D5
5	DQ0	DQ5	6	DDR_B_D1	DDR_B_D4
7	DQ1	VSS	8		
9	VSS	DM0	10	DDR_B_DQS#0	DDR_B_DM0
11	DQS0#	VSS	12	DDR_B_DQS0	
13	DQS0	DQ6	14		DDR_B_D6
15	VSS	DQ7	16	DDR_B_D2	DDR_B_D7
17	DQ2	VSS	18	DDR_B_D3	
19	DQ3	DQ12	20		DDR_B_D12
21	VSS	DQ13	22	DDR_B_D8	DDR_B_D13
23	DQ8	VSS	24	DDR_B_D9	
25	DQ9	DM1	26		DDR_B_DM1
27	VSS	VSS	28		
29	DQS1#	CK0	30	DDR_B_DQS#1	M_CLK_DDR2 7
31	DQS1	CK0#	32	DDR_B_DQS1	M_CLK_DDR#2 7
33	VSS	VSS	34		
35	DQ10	DQ14	36	DDR_B_D10	DDR_B_D14
37	DQ11	DQ15	38	DDR_B_D11	DDR_B_D15
39	VSS	VSS	40		
41	VSS	VSS	42		
43	DQ16	DQ20	44	DDR_B_D17	DDR_B_D21
45	DQ17	DQ21	46	DDR_B_D20	DDR_B_D16
47	VSS	VSS	48		
49	DQS2#	NC	50	DDR_B_DQS#2	PM_EXTTS#1 7
51	DQS2	DM2	52	DDR_B_DQS2	DDR_B_DM2
53	VSS	VSS	54		
55	DQ18	DQ22	56	DDR_B_D18	DDR_B_D22
57	DQ19	DQ23	58	DDR_B_D19	DDR_B_D23
59	VSS	VSS	60		
61	DQ24	DQ28	62	DDR_B_D28	DDR_B_D26
63	DQ25	DQ29	64	DDR_B_D25	DDR_B_D24
65	VSS	VSS	66		
67	DM3	DQS3#	68	DDR_B_DM3	DDR_B_DQS#3
69	NC	DQS3	70		DDR_B_DQS3
71	VSS	VSS	72		
73	DQ26	DQ30	74	DDR_B_D30	DDR_B_D29
75	DQ27	DQ31	76	DDR_B_D31	DDR_B_D27
77	VSS	VSS	78		
79	CKE0	NC/CKE1	80	7 DDR_CKE2_DIMMB DDR_CKE2_DIMMB	DDR_CKE3_DIMMB DDR_CKE3_DIMMB 7
81	VDD	VDD	82		
83	NC	NC/A15	84		
85	BA2	NC/A14	86	8 DDR_B_BS#2	DDR_B_MA14 DDR_B_MA14 7
87	VDD	VDD	88		
89	A12	A11	90	DDR_B_MA12	DDR_B_MA11
91	A9	A7	92	DDR_B_MA9	DDR_B_MA7
93	A8	A6	94	DDR_B_MA8	DDR_B_MA6
95	VDD	VDD	96		
97	A5	A4	98	DDR_B_MA5	DDR_B_MA4
99	A3	A2	100	DDR_B_MA3	DDR_B_MA2
101	A1	A0	102	DDR_B_MA1	DDR_B_MA0
103	VDD	VDD	104		
105	A10/AP	BA1	106	DDR_B_MA10	DDR_B_BS#1 8
107	BA0	RAS#	108	8 DDR_B_BS#0 DDR_B_BS#0	DDR_B_RAS# 8
109	WE#	S0#	110	8 DDR_B_WE# DDR_B_WE#	DDR_CS2_DIMMB# 7
111	VDD	VDD	112		
113	CAS#	ODT0	114	8 DDR_B_CAS# DDR_B_CAS#	M_ODT2 7
115	NC/S1#	NC/A13	116	7 DDR_CS3_DIMMB# DDR_CS3_DIMMB#	DDR_B_MA13
117	VDD	VDD	118		
119	NC/ODT1	NC	120	7 M_ODT3 M_ODT3	
121	VSS	VSS	122		
123	DQ32	DQ36	124	DDR_B_D32	DDR_B_D36
125	DQ33	DQ37	126	DDR_B_D33	DDR_B_D37
127	VSS	VSS	128		
129	DQS4#	DM4	130	DDR_B_DQS#4	DDR_B_DM4
131	DQS4	VSS	132	DDR_B_DQS4	
133	VSS	DQ38	134		DDR_B_D39
135	DQ34	DQ39	136	DDR_B_D34	DDR_B_D38
137	DQ35	VSS	138	DDR_B_D35	
139	VSS	DQ44	140		DDR_B_D44
141	DQ40	DQ45	142	DDR_B_D40	DDR_B_D45
143	DQ41	VSS	144	DDR_B_D41	
145	VSS	DQS5#	146		DDR_B_DQS#5
147	DM5	DQS5	148	DDR_B_DM5	DDR_B_DQS5
149	VSS	VSS	150		
151	DQ42	DQ46	152	DDR_B_D42	DDR_B_D46
153	DQ43	DQ47	154	DDR_B_D43	DDR_B_D47
155	VSS	VSS	156		
157	DQ48	DQ52	158	DDR_B_D48	DDR_B_D52
159	DQ49	DQ53	160	DDR_B_D49	DDR_B_D53
161	VSS	VSS	162		
163	NC,TEST	CK1	164		M_CLK_DDR3 7
165	VSS	CK1#	166		M_CLK_DDR#3 7
167	DQS6#	VSS	168	DDR_B_DQS#6	
169	DQS6	DM6	170	DDR_B_DQS6	DDR_B_DM6
171	VSS	VSS	172		
173	DQ50	DQ54	174	DDR_B_D51	DDR_B_D54
175	DQ51	DQ55	176	DDR_B_D50	DDR_B_D55
177	VSS	VSS	178		
179	DQ56	DQ60	180	DDR_B_D56	DDR_B_D60
181	DQ57	DQ61	182	DDR_B_D61	DDR_B_D57
183	VSS	VSS	184		
185	DM7	DQS7#	186	DDR_B_DM7	DDR_B_DQS#7
187	VSS	DQS7	188		DDR_B_DQS7
189	DQ58	VSS	190	DDR_B_D59	
191	DQ59	DQ62	192	DDR_B_D58	DDR_B_D62
193	VSS	DQ63	194		DDR_B_D63
195	SDA	VSS	196	13,16,19 ICH_SM_DA ICH_SM_DA	
197	SCL	SA0	198	13,16,19 ICH_SM_CLK ICH_SM_CLK	
199	VDDSPD	SA1	200	+3VS	

+3VS
C43: 0.1U_0402_16V4Z
C38: 2.2U_0603_6.3V6K
R44: 10K_0402_5% — +3VS
R45: 10K_0402_5%

SO-DIMM B
REVERSE
Bottom side

Security Classification	Compal Secret Data		
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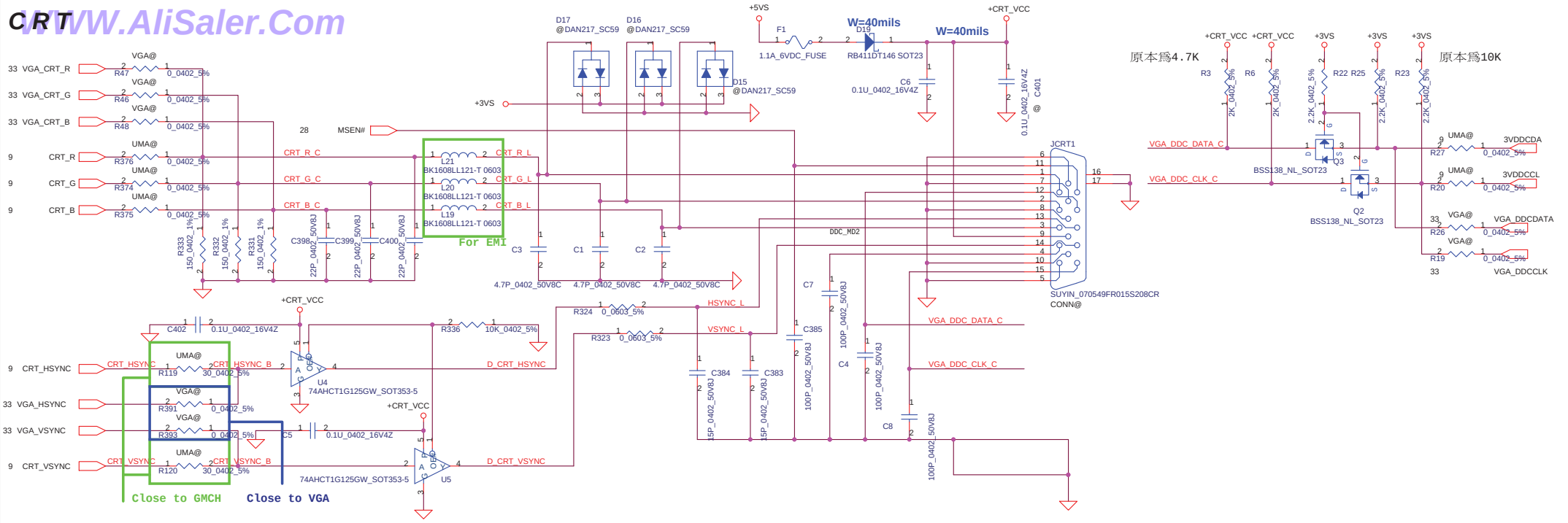
Compal Electronics, Inc.

Title: **DDR2 SO-DIMM II**

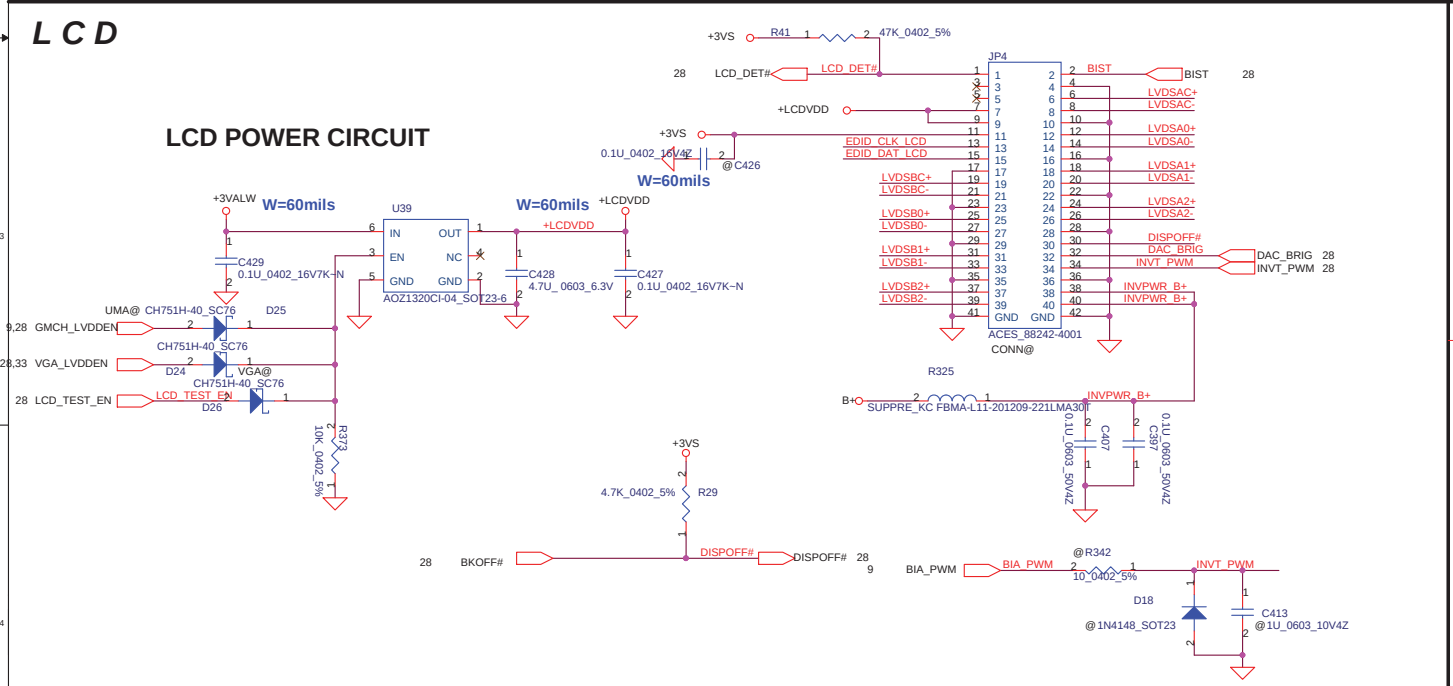
Size: Custom	Document Number: LA-4121P	Rev: 0.4
Date: Thursday, January 10, 2008	Sheet 14 of 51	

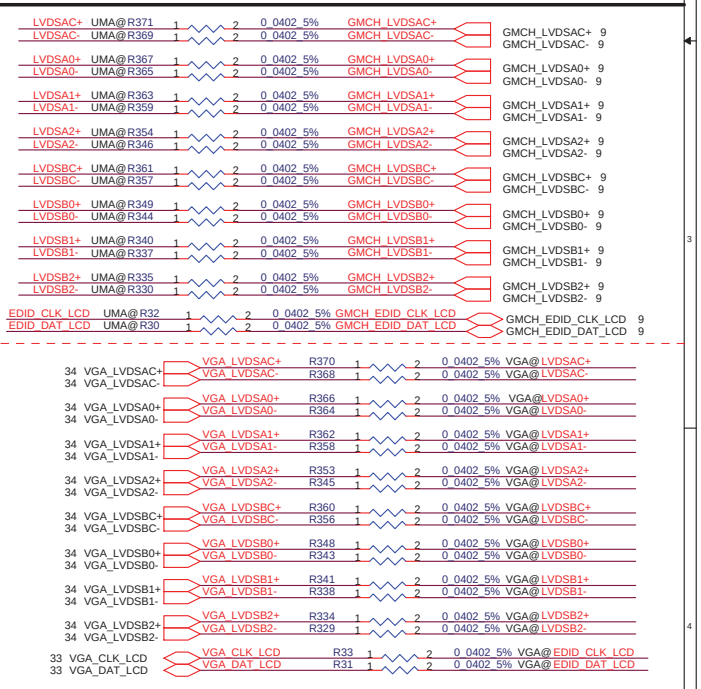
CRT



LCD

LCD POWER CIRCUIT





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Compal Electronics, Inc.

Title: CRT CONN/LCD CONN

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 15 of 51

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff	R1107	R1135	R1083			
*(Default)	No Stuff	R1074	R1086	R1098	R1113	R1128	R1139
667MHz	Stuff	R1086	R1139	R1135	R1074	R1139	R1135
	No Stuff	R1083	R1107	R1128			
		R1113	R1098				
800MHz	Stuff	R1135	R1139				
	No Stuff	R1083	R1086	R1098	R1128		
		R1074	R1107	R1113			

+3VM_CK505 — +3VS — R558 0_0805_5% — C657 10U_0805_10V4Z~N — C629 0.1U_0402_16V4Z~N — C665 0.1U_0402_16V4Z~N — C625 0.1U_0402_16V4Z~N — C649 0.1U_0402_16V4Z~N — C626 0.1U_0402_16V4Z~N — C661 0.1U_0402_16V4Z~N

Place close to U6

+1.25VS — R532 0_0805_5% — C631 22U_0805_6.3V4Z — C662 0.1U_0402_16V4Z~N — C664 0.1U_0402_16V4Z~N — C630 22U_0805_6.3V4Z — C663 0.1U_0402_16V4Z~N — C623 0.1U_0402_16V4Z~N — C627 0.1U_0402_16V4Z~N — +1.25VM_CK505

U6 — ICS9LPRS365BGLFT_TSSOP64

+3VM_CK505 — VDDPCI, VDD48, VDDPLL3, VDDREF, VDDSRC, VDDCPU

+1.25VM_CK505 — VDD96_IO, VDDPLL3_IO, VDDSRC_IO, VDDSRC_IO, VDDCPU_IO

NC 48

SCLK 64 — ICH_SM_CLK 13,14,19
SDATA 63 — ICH_SM_DA 13,14,19

PCI_STOP# 38 — H_STP_PCI# 19
CPU_STOP# 37 — H_STP_CPU# 19

CPU0 54 — R_CPU_BCLK — R495 — CLK_CPU_BCLK 4
CPU0# 53 — R_CPU_BCLK# — R496 — CLK_CPU_BCLK# 4

CPU1_F 51 — R_MCH_BCLK — R497 — CLK_MCH_BCLK 7
CPU1#_F 50 — R_MCH_BCLK# — R498 — CLK_MCH_BCLK# 7

SRC8/CPU2_ITP 47 — R_CLK_PCIE_LAN — R499 — CLK_PCIE_LAN 22
SRC8#/CPU2_ITP# 46 — R_CLK_PCIE_LAN# — R500 — CLK_PCIE_LAN# 22

SRC10 34 — R_PCIE_EXPR — R491 — CLK_PCIE_EXPR 26
SRC10# 35 — R_PCIE_EXPR# — R490 — CLK_PCIE_EXPR# 26

SRC11/CR#_H 33 — R_EXPR_CARD_REQ# — R533 — EXPR_CARD_REQ# 26
SRC11#/CR#_G 32 — R_MCARD_REQ# — R538 — MCARD_REQ# 27

SRC9 30 — R_CLK_PCIE_MCard — R566 — CLK_PCIE_MCARD 27
SRC9# 31 — R_CLK_PCIE_MCard# — R567 — CLK_PCIE_MCARD# 27

SRC7/CR#_F 44 — R_PCIE_LAN_REQ# — R489 — PCIE_LAN_REQ# 22
SRC7#/CR#_E 43 — R_ROBSON_REQ# — R501 — ROBSON_REQ# 27
R484 10K_0402_5% +3VS
R485 10K_0402_5% +3VS

SRC6 41 — R_CLK_Rob — R487 — CLK_PCIE_Rob 27
SRC6# 40 — R_CLK_Rob# — R488 — CLK_PCIE_Rob# 27

SRC4 27 — R_MCH_3GPLL — R587 — CLK_MCH_3GPLL 7
SRC4# 28 — R_MCH_3GPLL# — R588 — CLK_MCH_3GPLL# 7

SRC3/CR#_C 24 — R_PCIE_ICH — R585 — CLK_PCIE_ICH 19
SRC3#/CR#_D 25 — R_PCIE_ICH# — R586 — CLK_PCIE_ICH# 19

SRC2/SATA 21 — R_PCIE_SATA — R583 — CLK_PCIE_SATA 18
SRC2#/SATA# 22 — R_PCIE_SATA# — R584 — CLK_PCIE_SATA# 18

SRC1/SE1/27MHz_NonSS 17 — R_SSCDREFCLK — R581 — UMA@0_0402_5% — MCH_SSCDREFCLK 7
SRC1#/SE2/27MHz_SS 18 — R_SSCDREFCLK# — R582 — UMA@0_0402_5% — MCH_SSCDREFCLK# 7

SRC0/DOT96 13 — R_MCH_DREFCLK — R579 — UMA@0_0402_5% — CLK_MCH_DREFCLK 7
SRC0#/DOT96# 14 — R_MCH_DREFCLK# — R580 — UMA@0_0402_5% — CLK_MCH_DREFCLK# 7
R249 — VGA@0_0402_5% — CLK_PCIE_VGA 33
R248 — VGA@0_0402_5% — CLK_PCIE_VGA# 33

CK_PWRGD/PD# 56 — CK_PWRGD — CK_PWRGD 19
@R511 — CLK_EN# — CLK_EN# 46

R263 2.2K_0402_5% — FSA — MCH_CLKSEL0 7 — CPU_BSEL0 5 — R262 0_0402_5% — R264 1K_0402_5%

+VCCP — R197 1K_0402_5% — FSB — MCH_CLKSEL1 7 — CPU_BSEL1 5 — @R196 0_0402_5% — R198 1K_0402_5%

R509 10K_0402_5% — FSC — MCH_CLKSEL2 7 — CPU_BSEL2 5 — @R492 0_0402_5% — R494 1K_0402_5% — R493 0_0402_5%

+3VS — R550 10K_0402_5% — R562 10K_0402_5%

19 CLKSATAREQ# — 475_0402_1% — R556 — SATA_REQ — PCI0/CR#_A 1
7 CLKMCHREQ# — 475_0402_1% — R563 — MCH_REQ — PCI1/CR#_B 3
27 CLK_DEBUG_PORT — 22_0402_5% — R564 — PCI2_TME — PCI2/TME 4
28 CLK_PCI_TPM — 22_0402_5% — R576
25 CLK_PCI_CB — 33_0402_5% — R577 — PCI_CLK3 — PCI3 5
28 CLK_PCI_EC — 33_0402_5% — R578 — 27_SEL — PCI4/27_Select 6
17 CLK_PCI_ICH — 33_0402_5% — R565 — ITP_EN — PCI_F5/ITP_EN 7

CLK_XTAL_IN — X1 60
CLK_XTAL_OUT — X2 59

19 CLK_48M_ICH — 33_0402_5% — R265 — FSA — USB_48MHZ/FSLA 10
FSB — FSLB/TEST_MODE 57
19 CLK_14M_ICH — 33_0402_5% — R510 — FSC — REF0/FSLC/TEST_SEL 62

+1.25VM_CK505 — VDDSRC_IO 45

GNDSRC 42, GNDPCI 8, GND48 11, GND 15, GND 19, GNDCPU 52, GNDSRC 23, GNDSRC 29, GNDREF 58

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1 = Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

CLK_XTAL_OUT — CLK_XTAL_IN — Y1 14.31818MHz_20P_1BX14318BE1A — C640 18P_0402_50V8J~N — C634 18P_0402_50V8J~N

Placed within 500 mils of CK505M

Routing the trace at least 10mil

+3VM_CK505 — ITP_EN — R244 10K_0402_5%
+3VM_CK505 — 27_SEL — R591 10K_0402_5% VGA@ — R592 10K_0402_5% UMA@
+3VM_CK505 — PCI2_TME — R574 10K_0402_5% — R575 10K_0402_5% @

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: Clock Generator

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 16 of 51

+3VS

R223 8.2K_0402_5% PCI_DEVSEL#
R218 8.2K_0402_5% PCI_STOP#
R209 8.2K_0402_5% PCI_TRDY#
R204 8.2K_0402_5% PCI_FRAME#
R212 8.2K_0402_5% PCI_PLOCK#
R210 8.2K_0402_5% PCI_IRDY#
R238 8.2K_0402_5% PCI_SERR#
R211 8.2K_0402_5% PCI_PERR#

+3VS

R239 8.2K_0402_5% PCI_PIRQA#
R213 8.2K_0402_5% PCI_PIRQB#
R208 8.2K_0402_5% PCI_PIRQC#
R206 8.2K_0402_5% PCI_PIRQD#
R240 8.2K_0402_5% PCI_PIRQE#
R237 8.2K_0402_5% PCI_PIRQF#
R236 8.2K_0402_5% PCI_PIRQG#
R216 8.2K_0402_5% PCI_PIRQH#

R215 8.2K_0402_5% PCI_REQ0#
R226 8.2K_0402_5% PCI_REQ1#
R205 8.2K_0402_5% PCI_REQ2#
R207 8.2K_0402_5% PCI_REQ3#

25 PCI_AD[0..31]

U7B

PCI_AD0 D20 AD0
PCI_AD1 E19 AD1
PCI_AD2 D19 AD2
PCI_AD3 A20 AD3
PCI_AD4 D17 AD4
PCI_AD5 A21 AD5
PCI_AD6 A19 AD6
PCI_AD7 C19 AD7
PCI_AD8 A18 AD8
PCI_AD9 B16 AD9
PCI_AD10 A12 AD10
PCI_AD11 E16 AD11
PCI_AD12 A14 AD12
PCI_AD13 G16 AD13
PCI_AD14 A15 AD14
PCI_AD15 B6 AD15
PCI_AD16 C11 AD16
PCI_AD17 A9 AD17
PCI_AD18 D11 AD18
PCI_AD19 B12 AD19
PCI_AD20 C12 AD20
PCI_AD21 D10 AD21
PCI_AD22 C7 AD22
PCI_AD23 F13 AD23
PCI_AD24 E11 AD24
PCI_AD25 E13 AD25
PCI_AD26 E12 AD26
PCI_AD27 D8 AD27
PCI_AD28 A6 AD28
PCI_AD29 E8 AD29
PCI_AD30 D6 AD30
PCI_AD31 A3 AD31

PCI

REQ0# A4 PCI_REQ0# → PCI_REQ0# 25
GNT0# D7 PCI_GNT0# → PCI_GNT0# 25
REQ1#/GPIO50 E18 PCI_REQ1#
GNT1#/GPIO51 C18
REQ2#/GPIO52 B19 PCI_REQ2#
GNT2#/GPIO53 E18
REQ3#/GPIO54 A11 PCI_REQ3#
GNT3#/GPIO55 C10 PCI_GNT3#

C/BE0# C17 PCI_CBE#0 → PCI_CBE#0 25
C/BE1# E15 PCI_CBE#1 → PCI_CBE#1 25
C/BE2# E16 PCI_CBE#2 → PCI_CBE#2 25
C/BE3# E17 PCI_CBE#3 → PCI_CBE#3 25

IRDY# C8 PCI_IRDY# → PCI_IRDY# 25
PAR D9 PCI_PAR → PCI_PAR 25
PCIRST# G6 PCI_PCIRST#
DEVSEL# D16 PCI_DEVSEL# → PCI_DEVSEL# 25
PERR# A7 PCI_PERR#
PLOCK# B7 PCI_PLOCK#
SERR# F10 PCI_SERR# → PCI_SERR#
STOP# C16 PCI_STOP# → PCI_STOP# 25
TRDY# C9 PCI_TRDY# → PCI_TRDY# 25
FRAME# A17 PCI_FRAME# → PCI_FRAME# 25

PLTRST# AG24 PCI_PLTRST#
PCICLK B10 CLK_PCI_ICH → CLK_PCI_ICH 16
PME# G7 PCI_PME# — 10K_0402_5% — R202 — +3V_SB

Interrupt I/F

PCI_PIRQA# F9 PIRQA#
PCI_PIRQB# B5 PIRQB#
PCI_PIRQC# C5 PIRQC#
PCI_PIRQD# A10 PIRQD#

PIRQE#/GPIO2 F8 PCI_PIRQE#
PIRQF#/GPIO3 G11 PCI_PIRQF#
PIRQG#/GPIO4 F12 PCI_PIRQG# → PCI_PIRQG# 25
PIRQH#/GPIO5 B3 PCI_PIRQH#

ICH8M REV 1.0

PCI_GNT3# — R201 @ 1K_0402_5%

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default*

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS
0	1	SPI
1	1	LPC *(Defaul)

PCI_GNT0# — @R219 1K_0402_5%

Place closely pin B10

CLK_PCI_ICH — R203 @ 10_0402_5% — C314 @8.2P_0402_50V

+3VS — @U8 — PCI_PCIRST# — R246 0_0402_5% — NC7SZ08P5X_NL_SC70-5 — PCI_RST# — R245 100K_0402_5% @ — PCI_RST# 21,25

+3VS — @U9 — PCI_PLTRST# — R307 0_0402_5% — NC7SZ08P5X_NL_SC70-5 — PLT_RST# — R308 100K_0402_5% @ — PLT_RST# 7,19,22,26,27,28,33

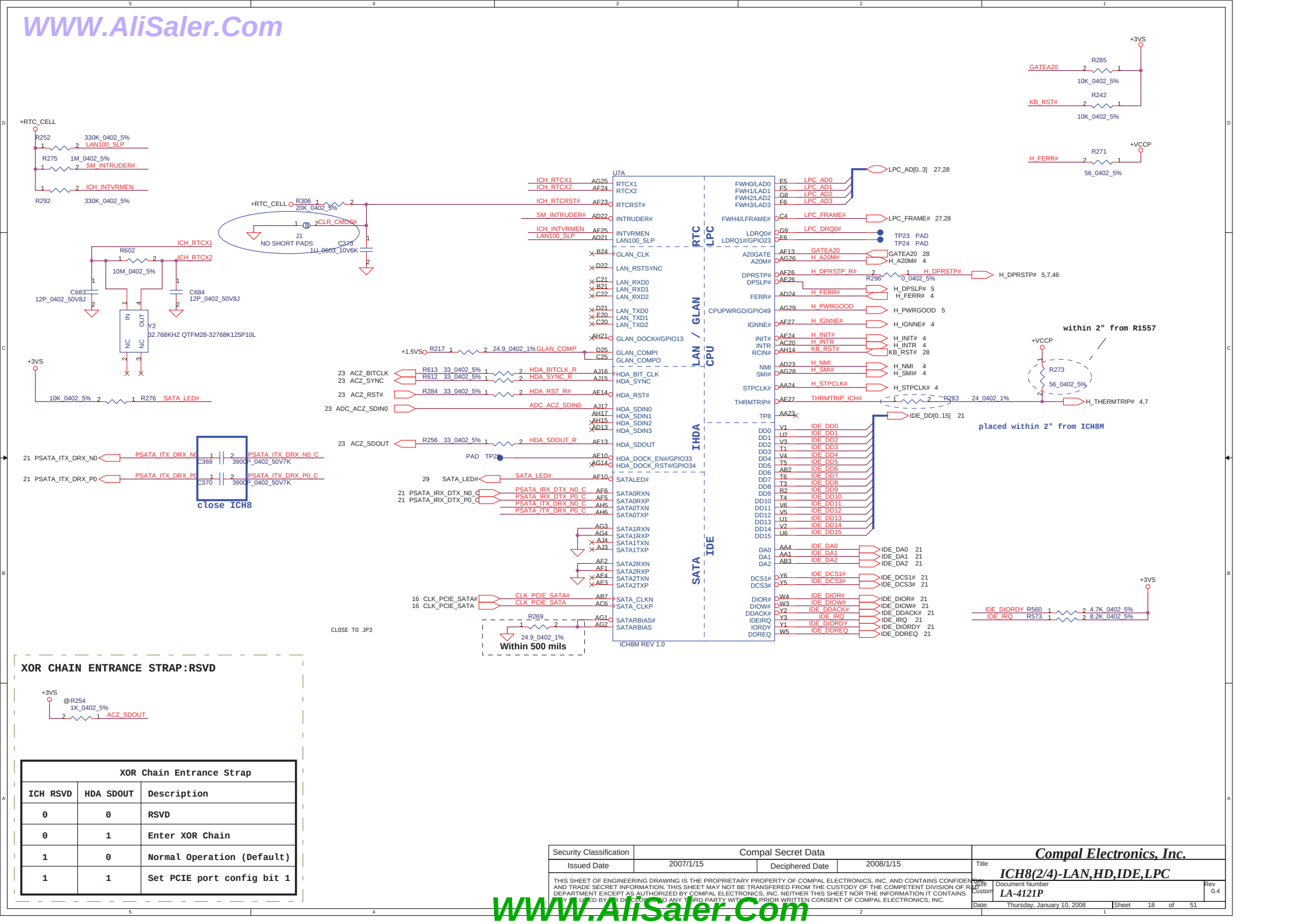
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: ICH8(1/4)-PCI/INT

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 17 of 51



XOR CHAIN ENTRANCE STRAP:RSVD

XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: ICH8(2/4)-LAN,HD,IDE,LPC

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 18 of 51

Place closely pin G5

CLK_48M_ICH
R235
@10_0402_5%
C331
@4.7P_0402_50V8C

Place closely pin AG9

CLK_14M_ICH
R303
@10_0402_5%
C371
@4.7P_0402_50V8C

U7C

ICH8M REV 1.0

RSMRST# -> CLPWROK -> PWROK

modify follow intel check list-1003

U7D

ICH8M REV 1.0

Within 500 mils

Within 500 mils

RSMRST circuit

For(DDR/CLKGEN/G-sensor/WWAN)

For(WLAN/EXP-Card/LAN)

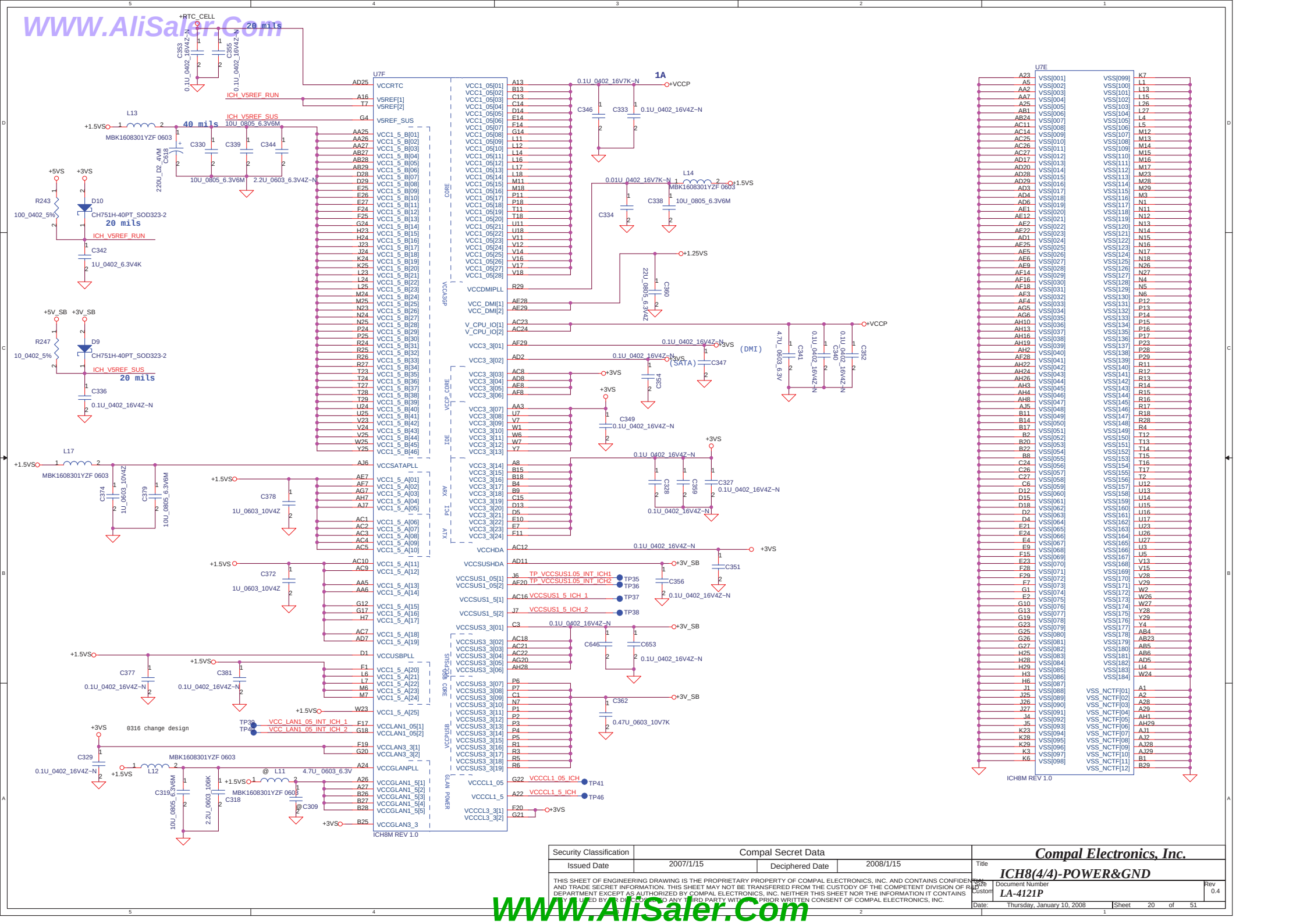
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

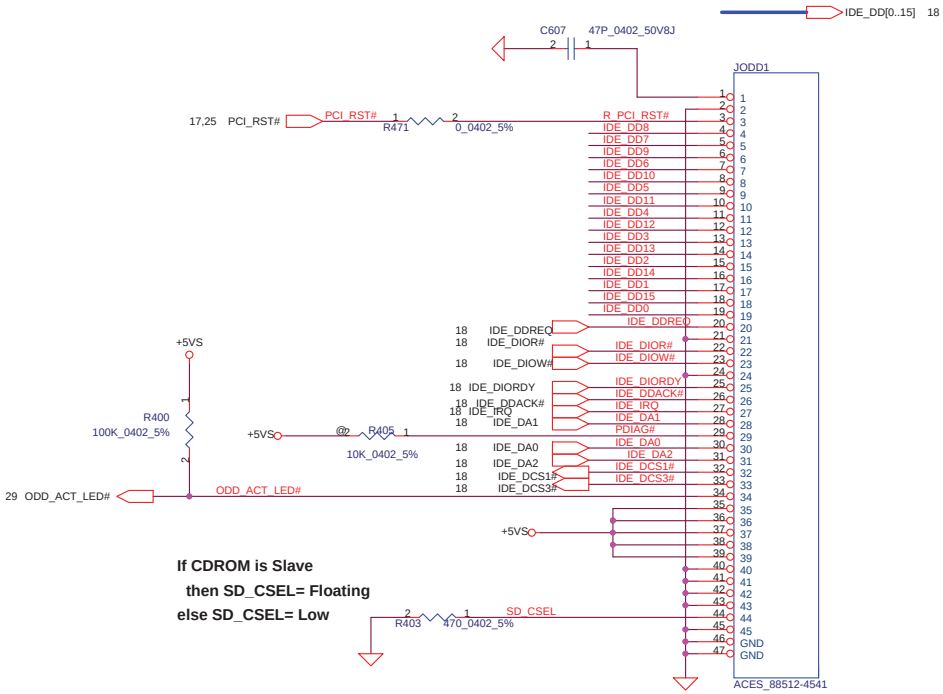
Title: ICH8(3/4)-PM,USB,GPIO

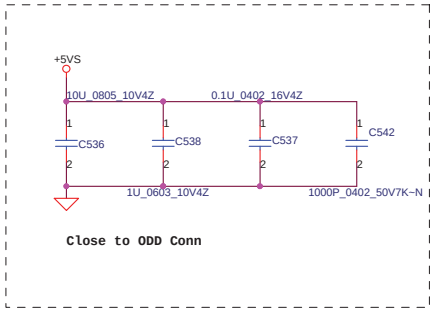
Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 19 of 51

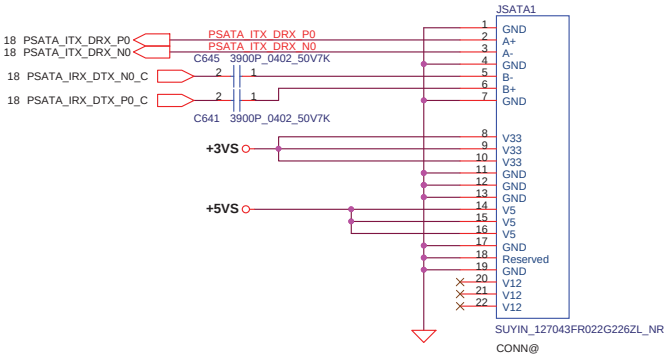


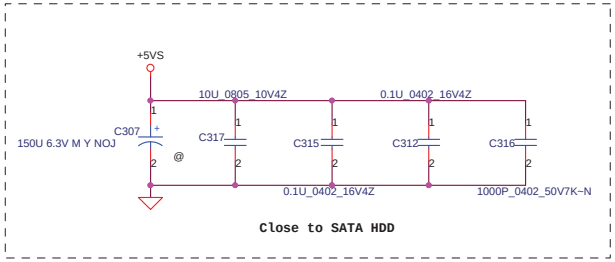
CDROM CONN





SATA HDD CONN





then SD_CSEL= Floating
else SD_CSEL= Low

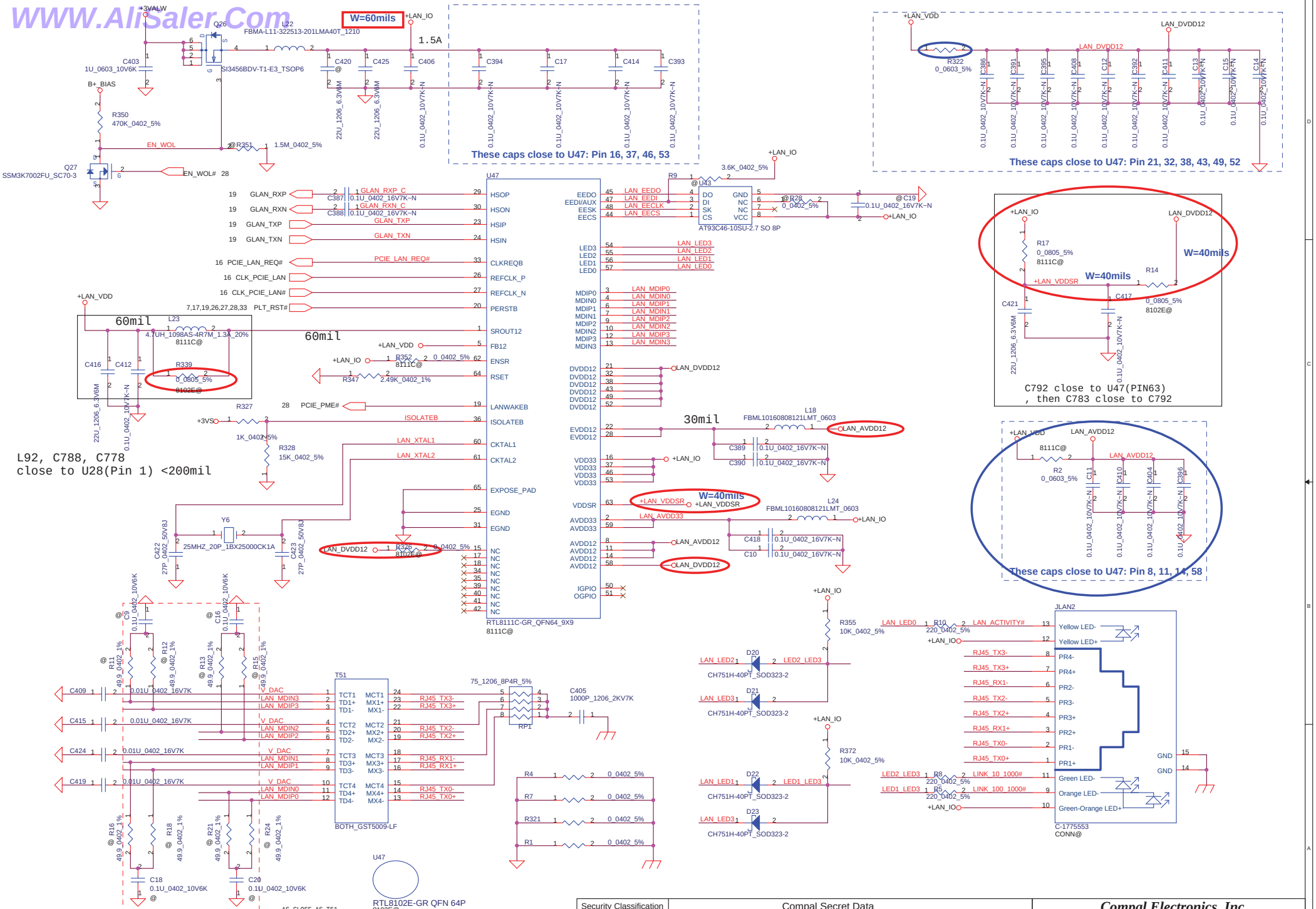
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: HDD/CDROM

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 21 of 51



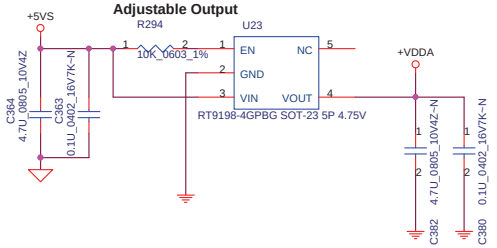
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

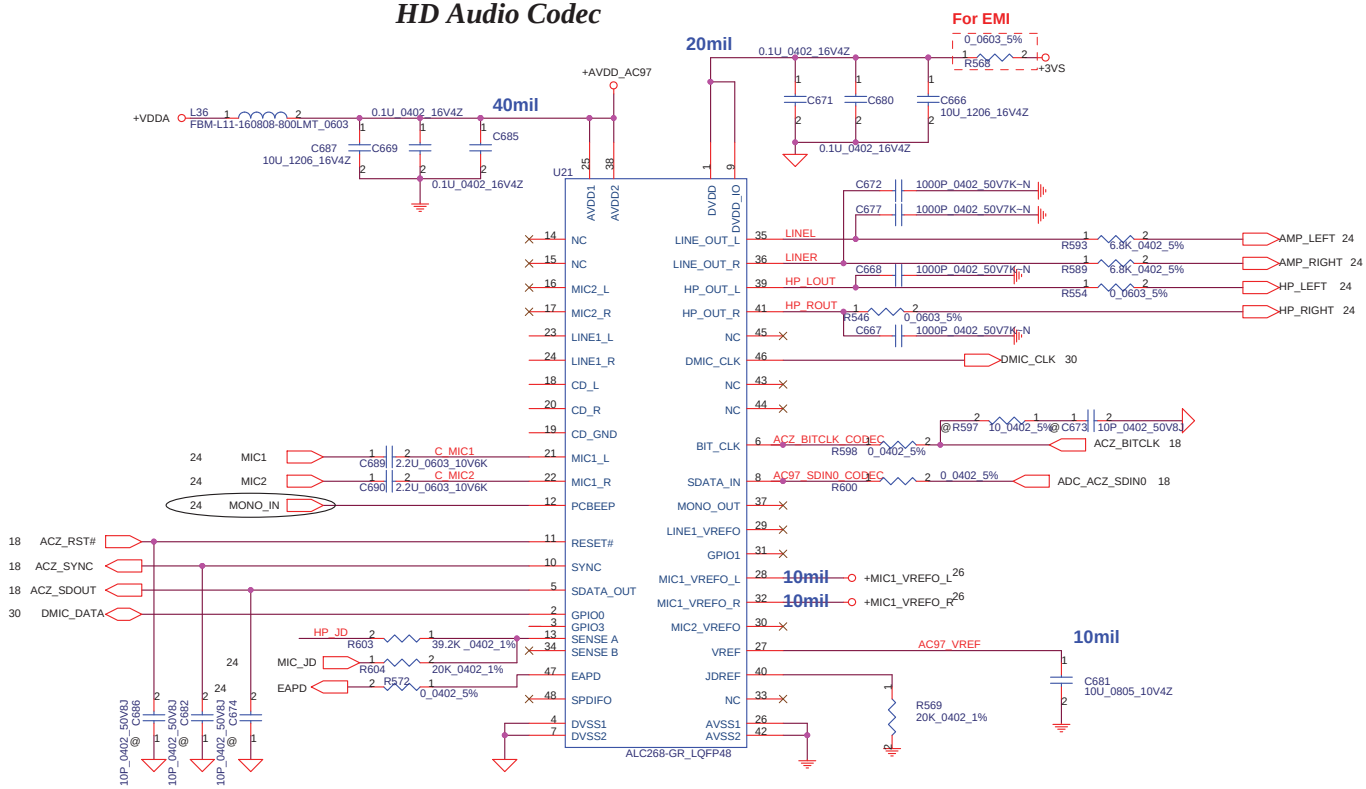
Title: Broadcom BCM5787M

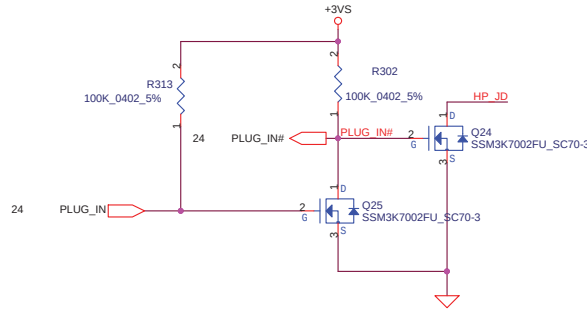
Size	Document Number	Rev
Custom	LA-4121P	0.4

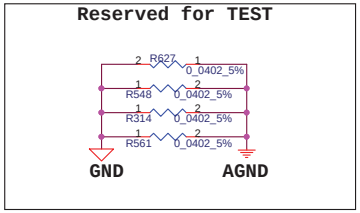
Date: Thursday, January 10, 2008 | Sheet 22 of 51



HD Audio Codec







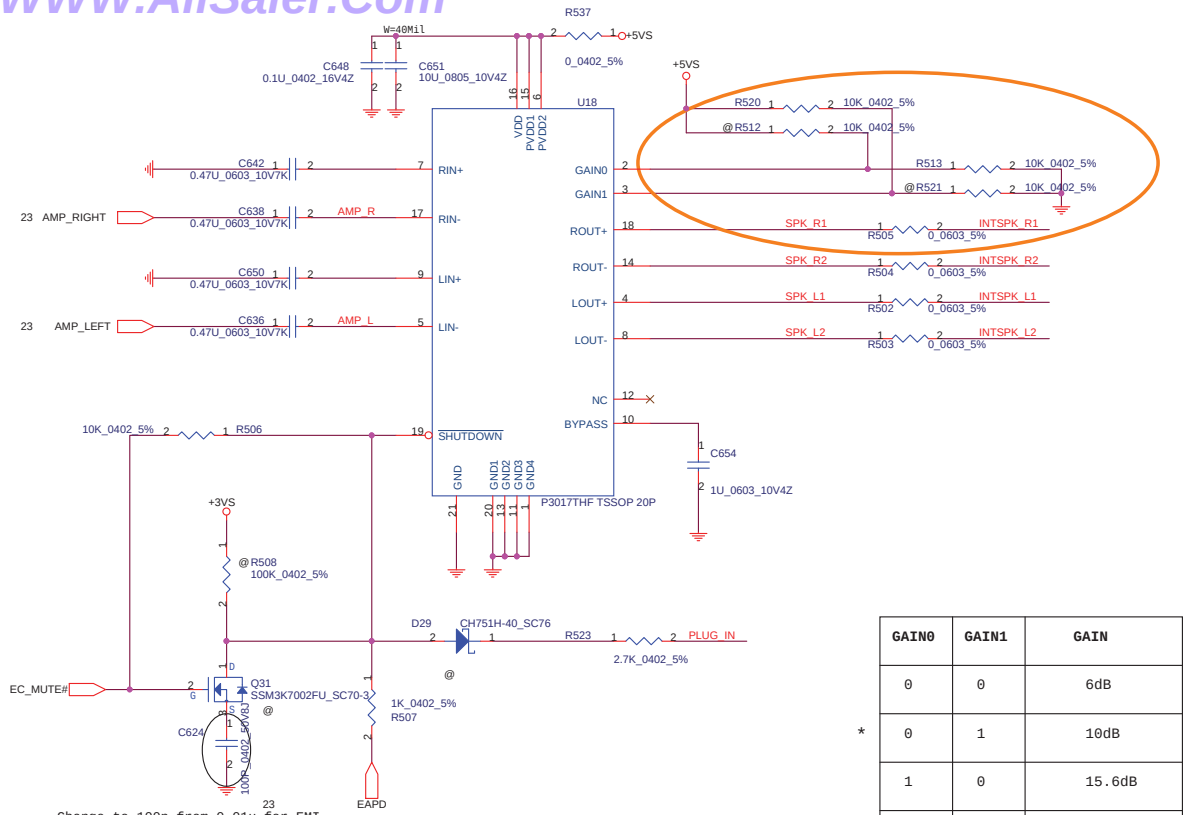
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: Codec ALC268

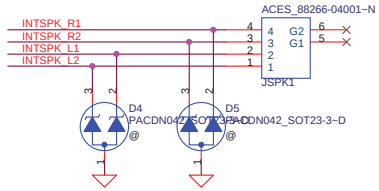
Size	Document Number	Rev
Custom	LA-4121P	0.4

Date: Thursday, January 10, 2008 Sheet 23 of 51

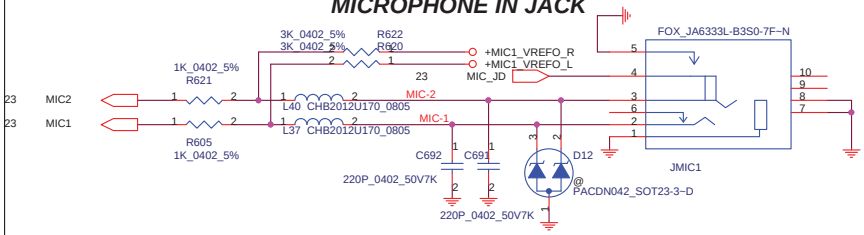


	GAIN0	GAIN1	GAIN
	0	0	6dB
*	0	1	10dB
	1	0	15.6dB
	1	1	21.6dB

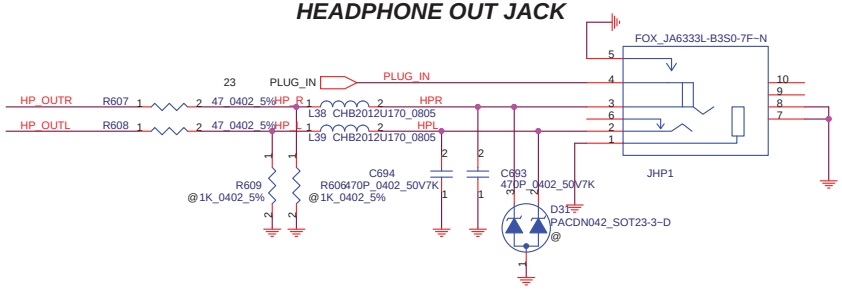
Speaker Connector

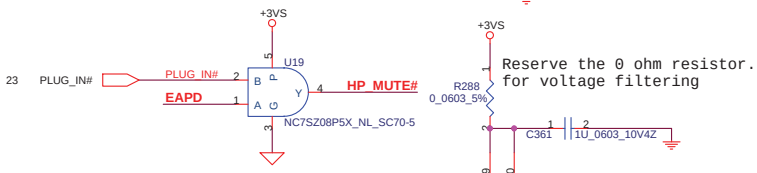


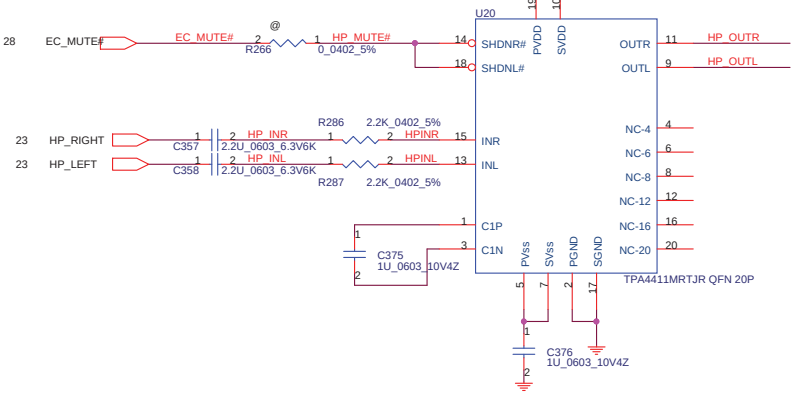
MICROPHONE IN JACK



HEADPHONE OUT JACK

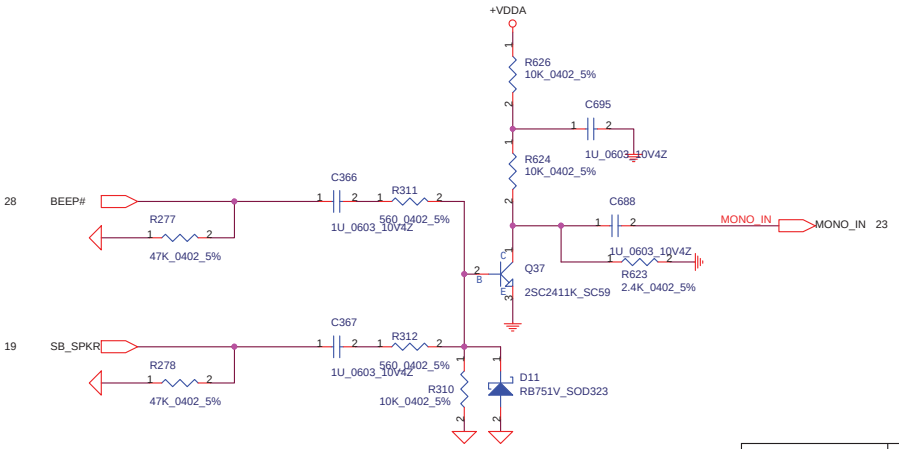






EC Beep

ICH Beep



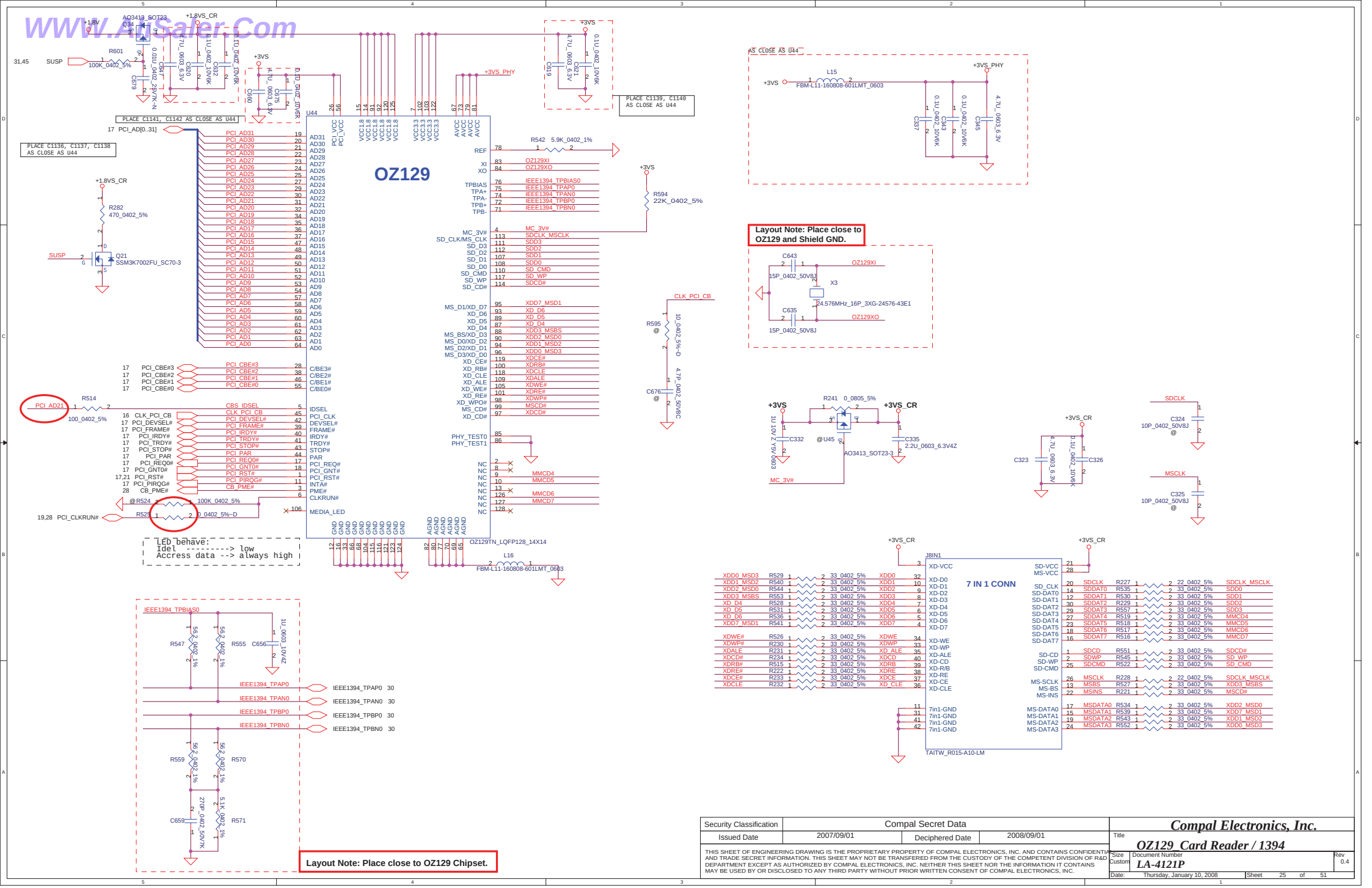
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: AMP/Audio Jack

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 24 of 51



Security Classification	Compal Secret Data		
Issued Date	2007/09/01	Deciphered Date	2008/09/01

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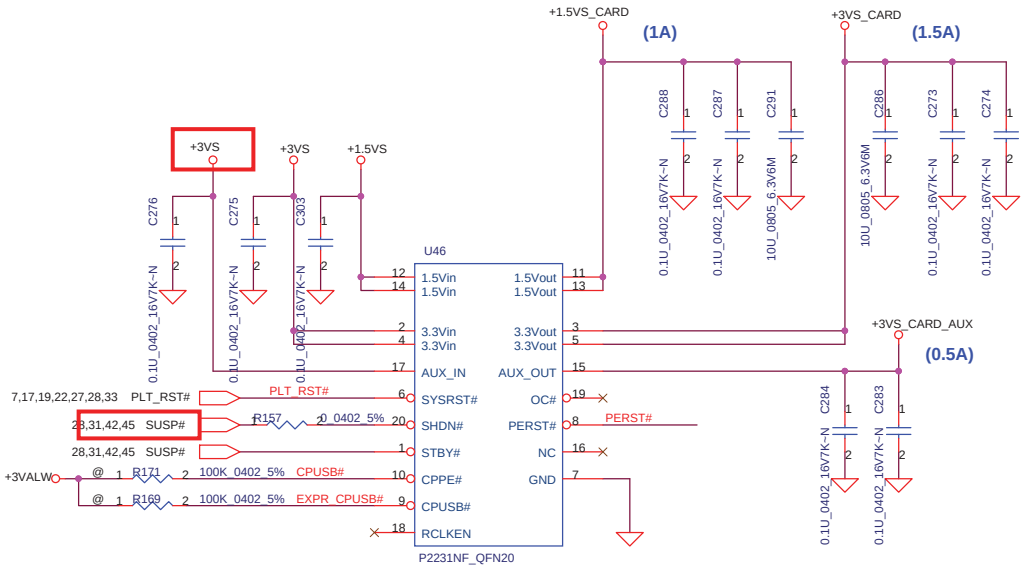
Compal Electronics, Inc.

Title: *OZ129_Card Reader / 1394*

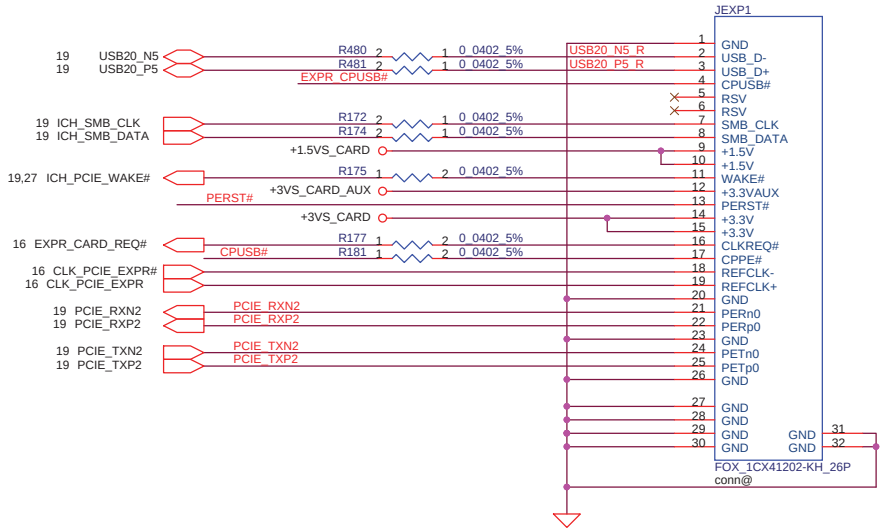
Size	Document Number	Rev
Custom	LA-4121P	0.4

Date: Thursday, January 10, 2008 Sheet 25 of 51

Express Card Power Switch



Express Card



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

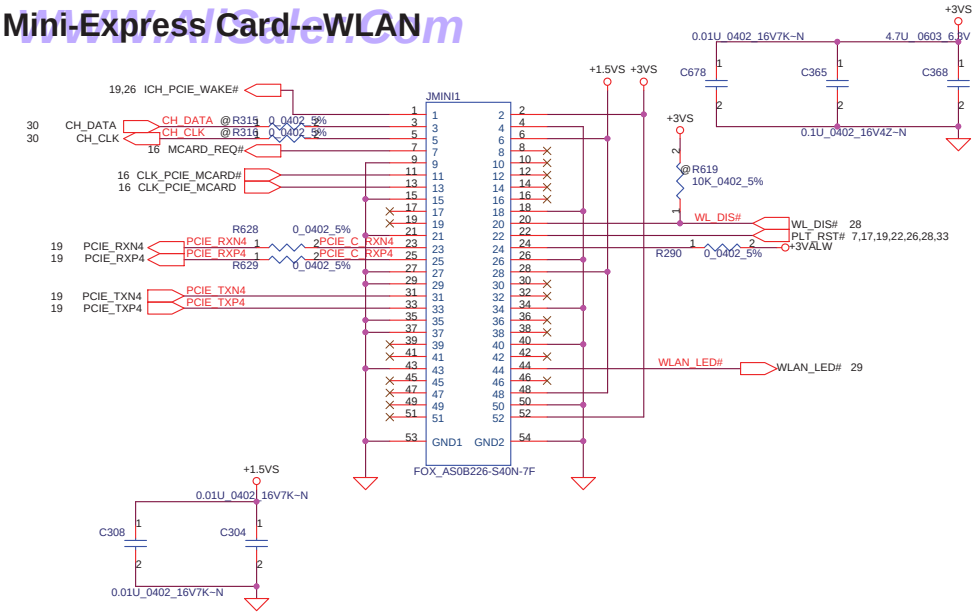
Compal Electronics, Inc.

Title: **Express Card**

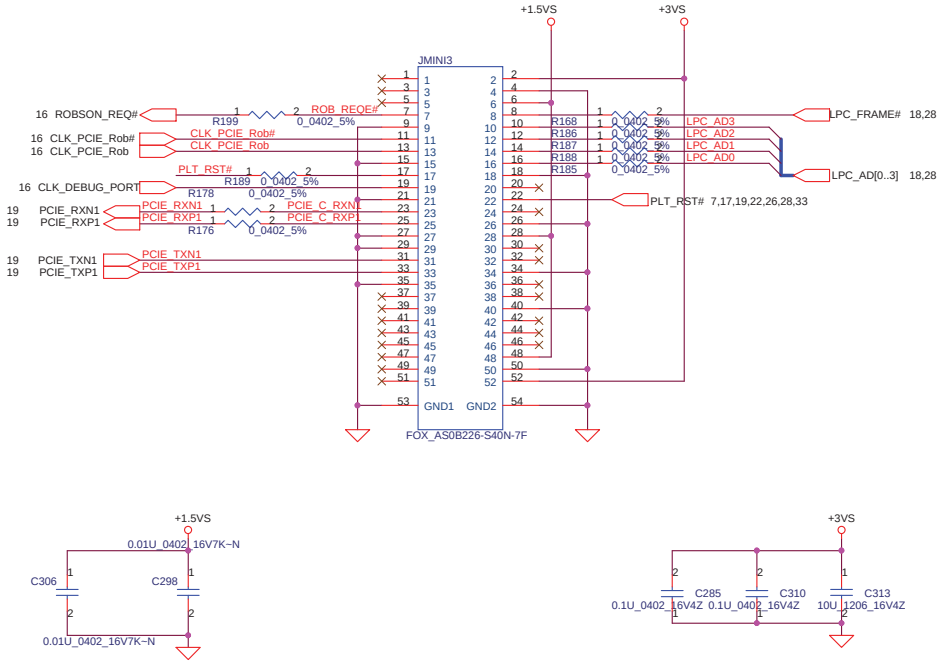
Size	Document Number	Rev
Custom	LA-4121P	0.4

Date: Thursday, January 10, 2008 Sheet 26 of 51

Mini-Express Card---WLAN



Robson



Mini-Express Card---WWAN

Mini-Express Card---Bluetooth

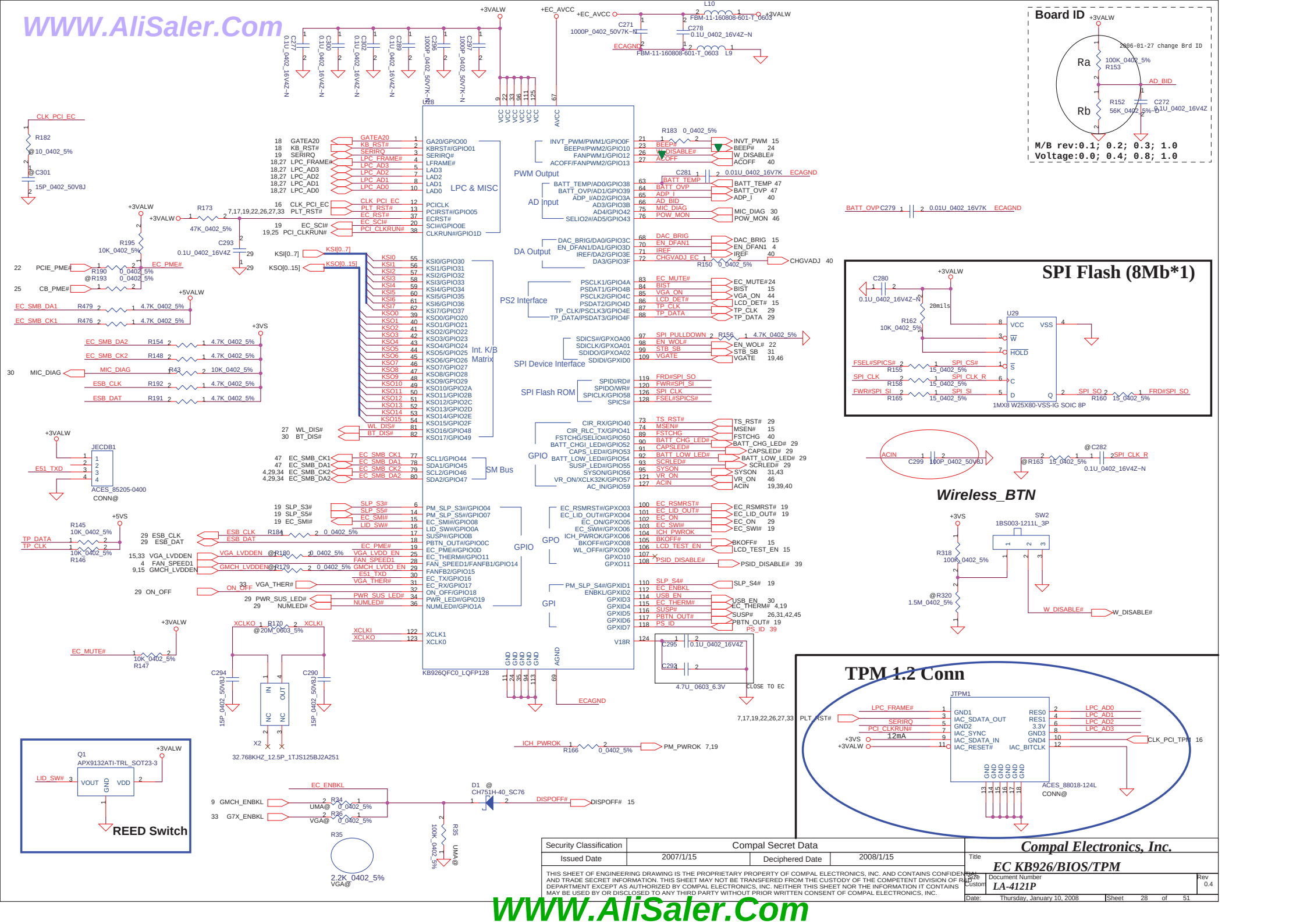
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: Mini Card

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 27 of 51



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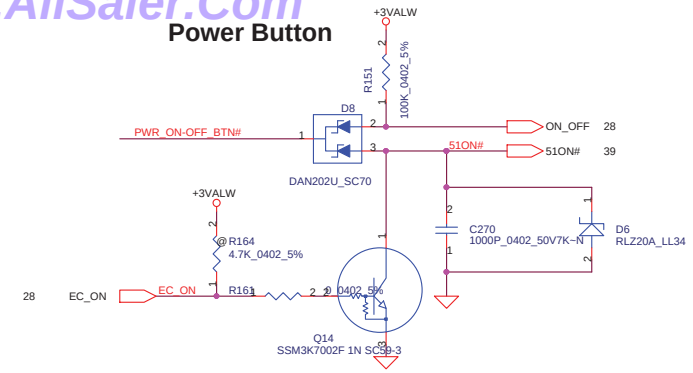
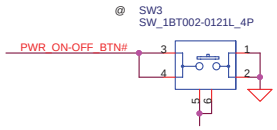
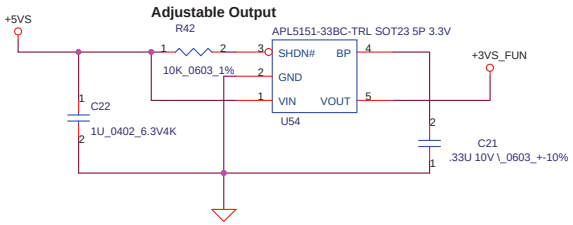
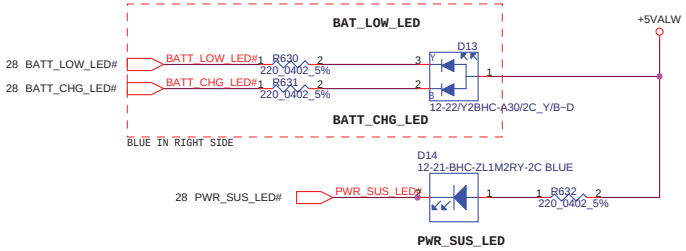
Power Button



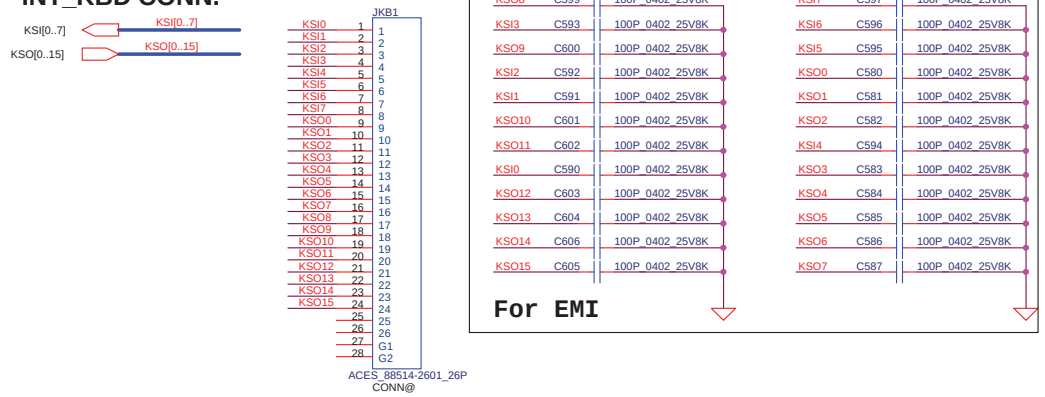


Regulator for ENE sensor

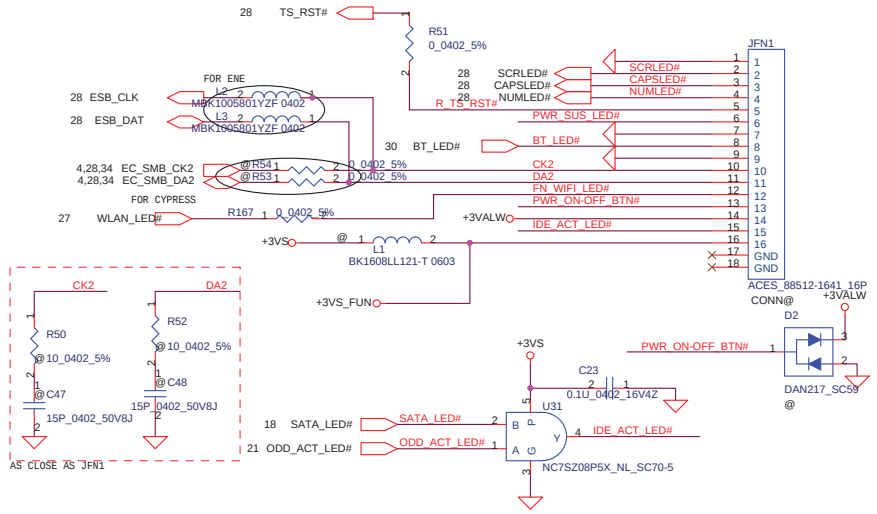




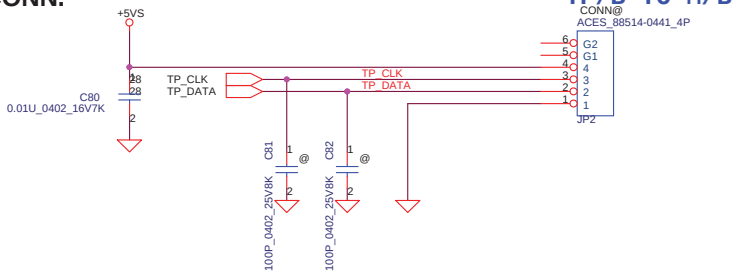
INT_KBD CONN.



Function/B CONN.



Touch PAD/B CONN.



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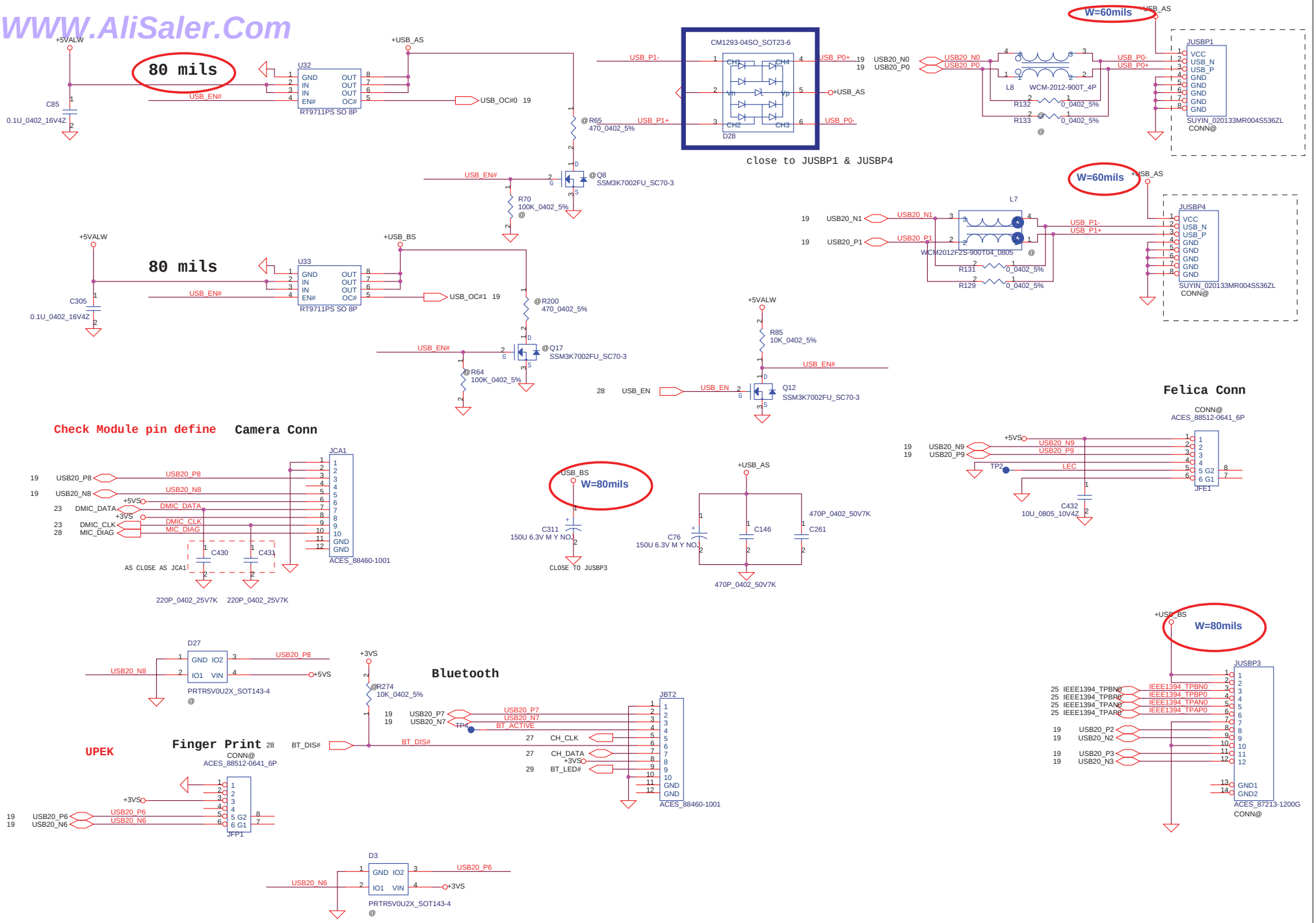
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: PWR_OK/BTN/KB/TP

Size: Custom | Document Number: LA-4121P | Rev: 0.4

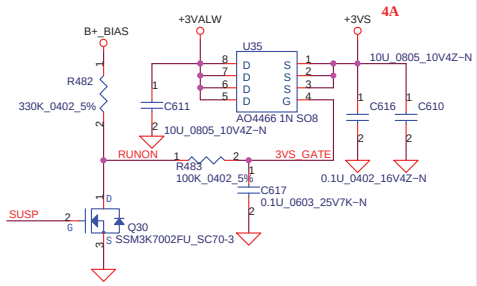
Date: Thursday, January 10, 2008 | Sheet 29 of 51



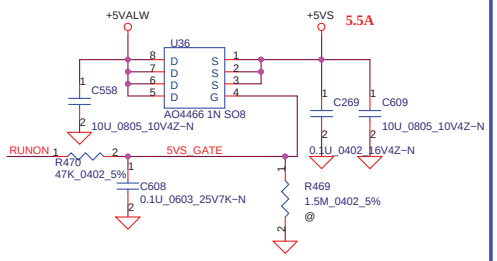
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.			
Title: USB/BlueTooth/FP/Felcia/Camera			
Size: Custom	Document Number: LA-4121P		Rev: 0.4
Date: Thursday, January 10, 2008		Sheet 30 of 51	

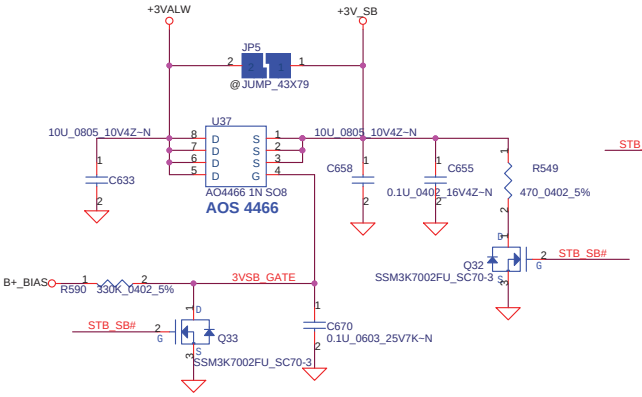
+3VALW to +3VS Transfer



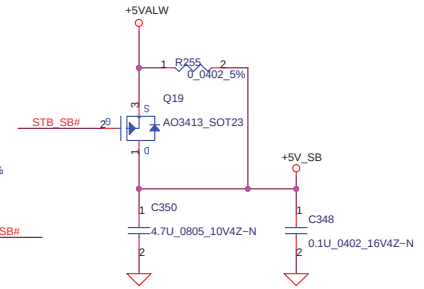
+5VALW to +5VS Transfer

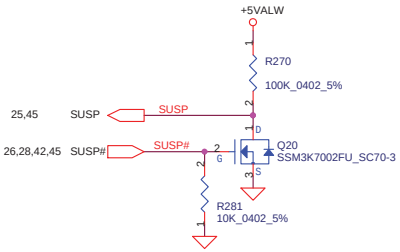


+3VALW TO +3V_SB

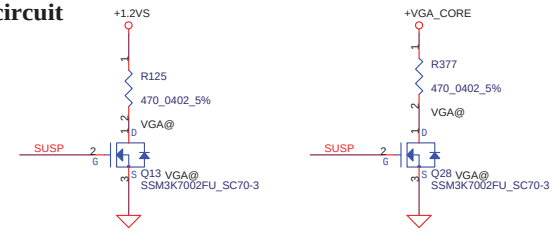


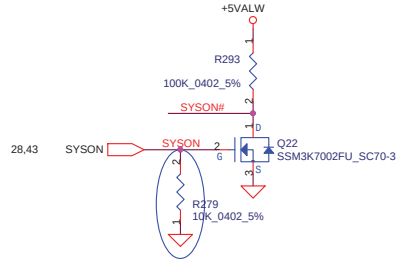
+5VALW TO +5V_SB



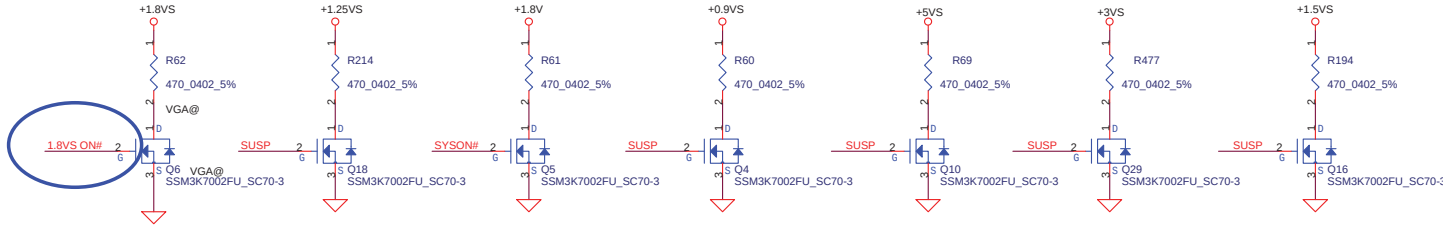


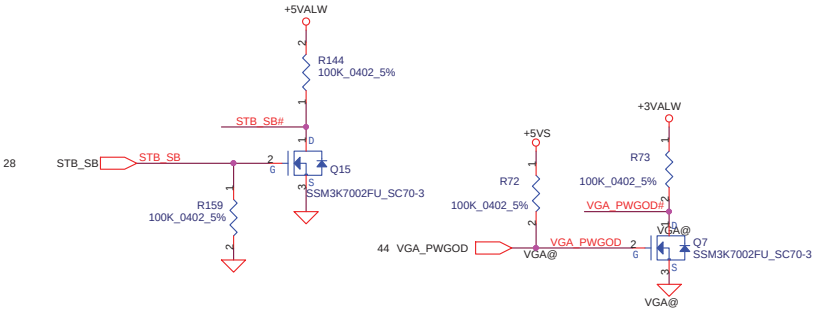
VGA Discharge circuit



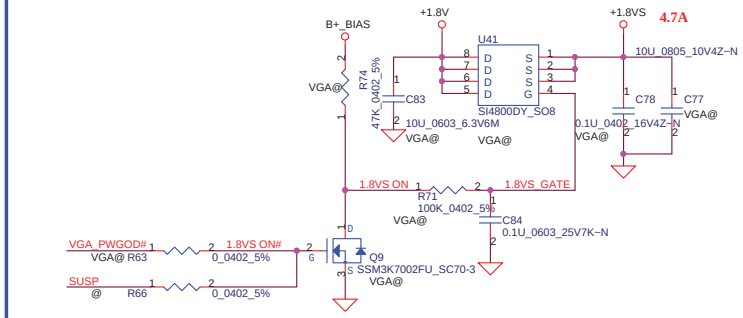


Discharge circuit -1





+1.8V to +1.8VS Transfer



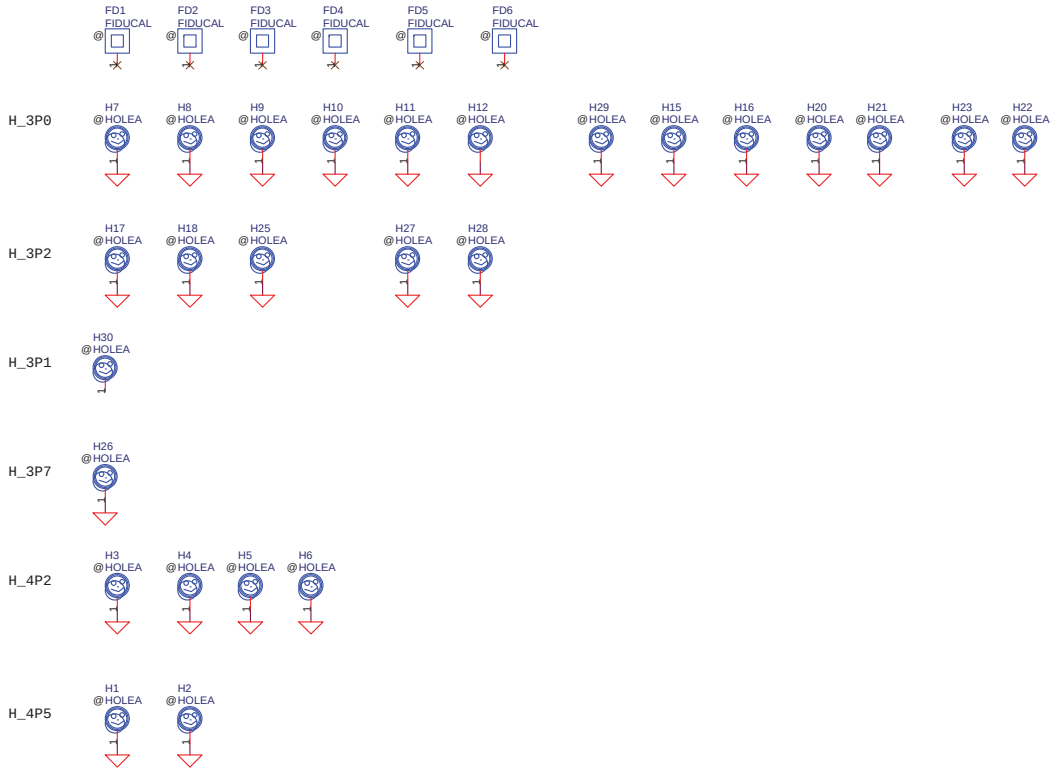
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: DC/DC Circuits

Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 31 of 51



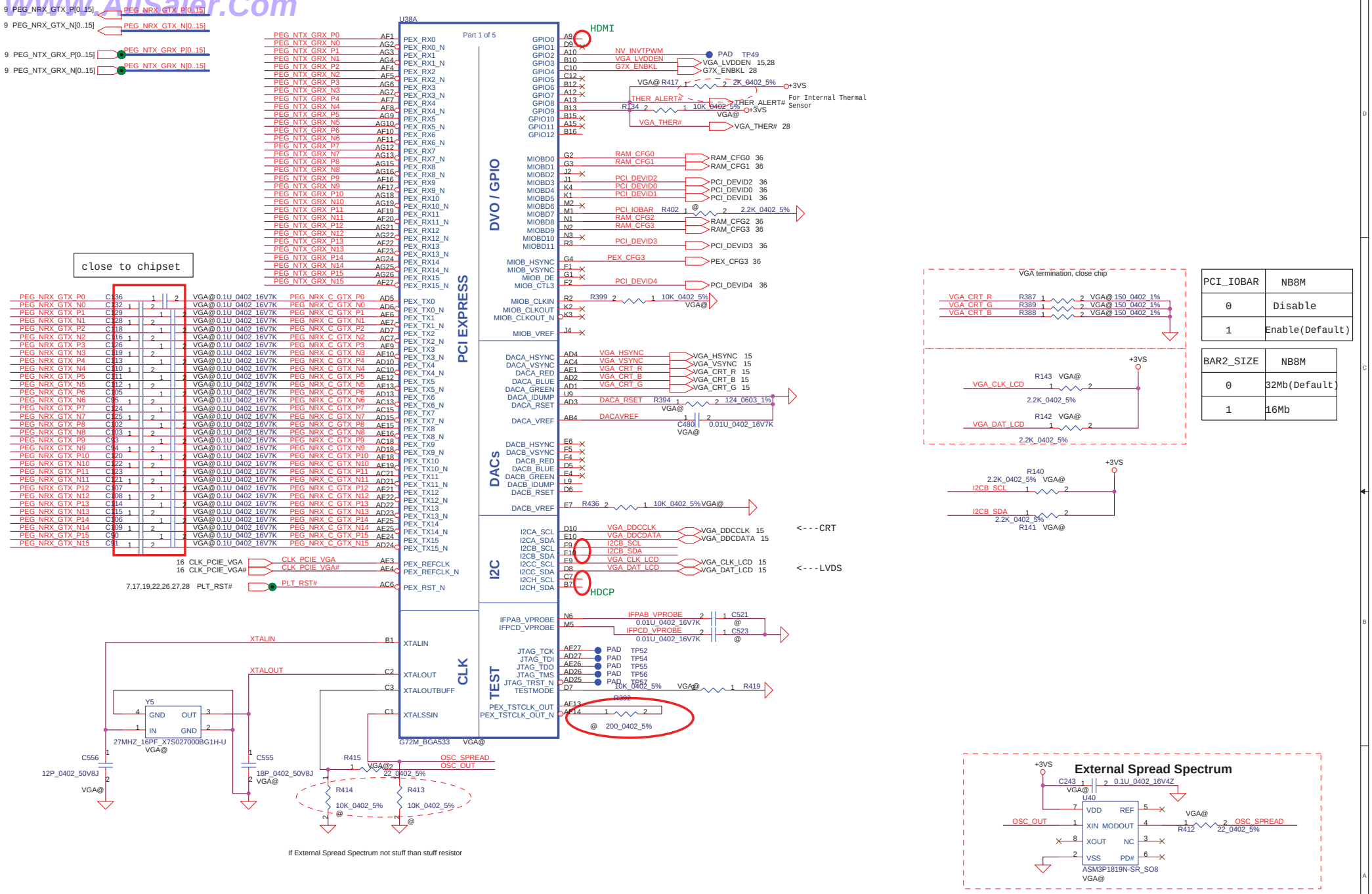
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Compal Electronics, Inc.

Title: **Screws**

Size	Document Number	Rev
Custom	LA-4121P	0.4

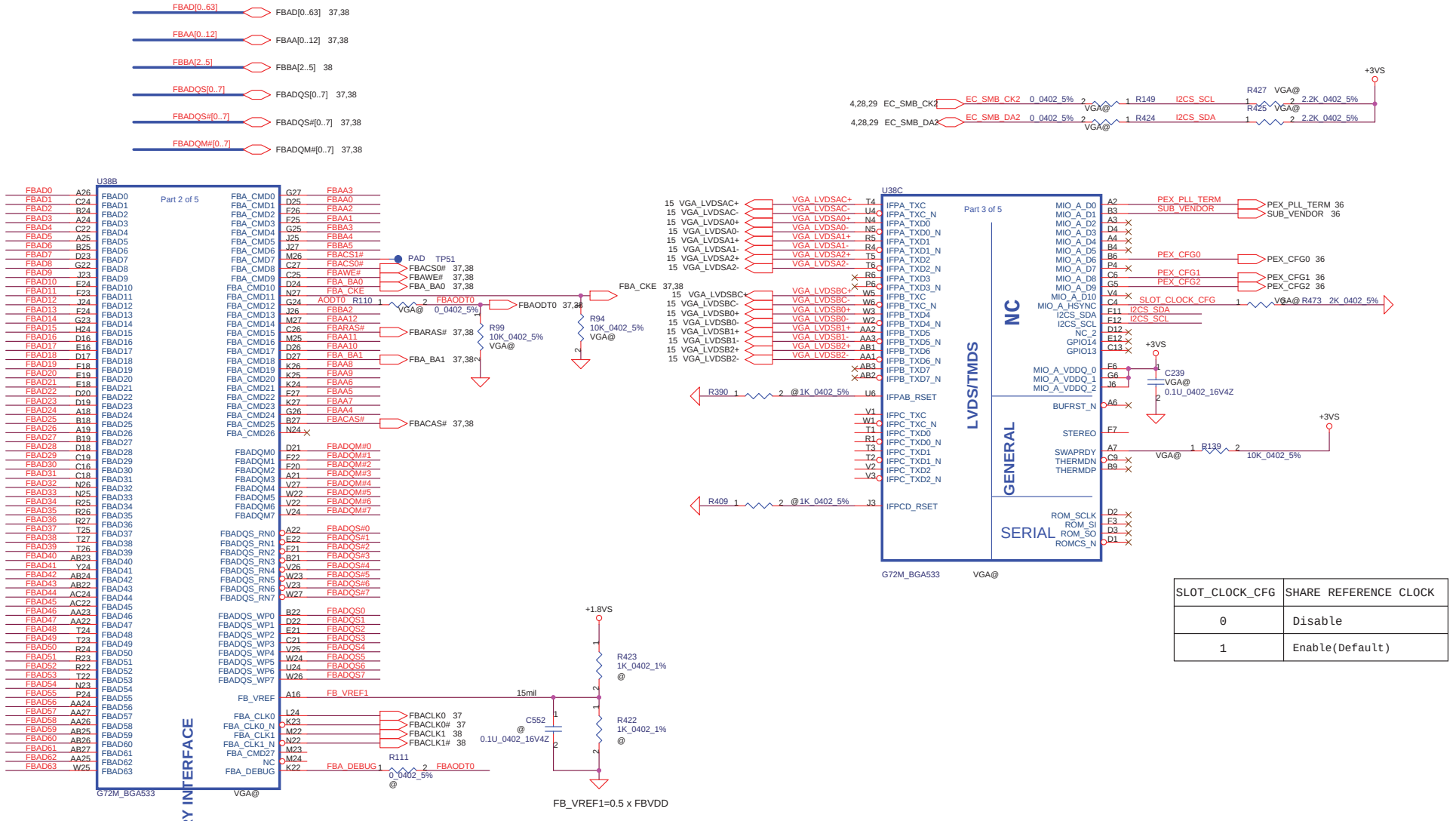
Date: Thursday, January 10, 2008 Sheet 32 of 51



PCI_IOBAR	NB8M
0	Disable
1	Enable(Default)

BAR2_SIZE	NB8M
0	32Mb(Default)
1	16Mb

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/07/10	Deciphered Date	2007/07/10
			Title: NB8M-GS Main
			Size: Custom; Document Number; Rev: 0.4
			Date: Thursday, January 10, 2008; Sheet 33 of 51



SLOT_CLOCK_CFG	SHARE REFERENCE CLOCK
0	Disable
1	Enable(Default)

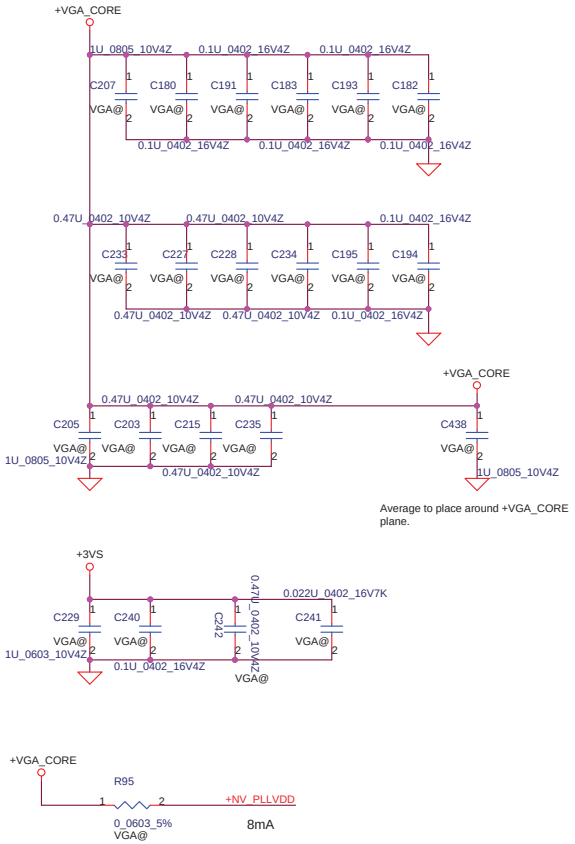
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

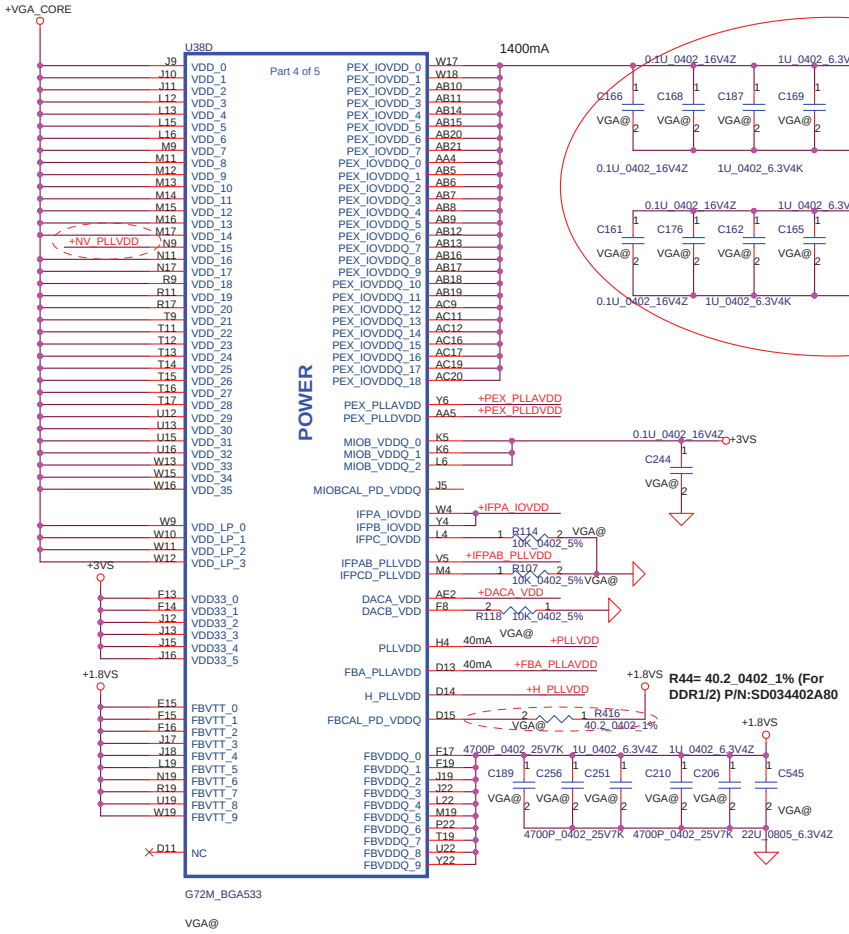
Compal Electronics, Inc.

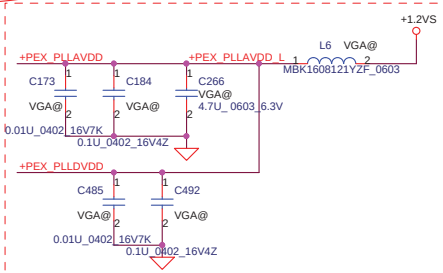
Title: NB8M-GS Memory

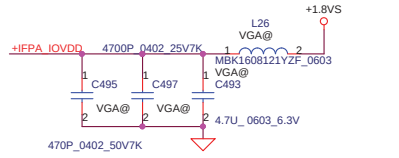
Size	Document Number	Rev
Custom		0.4

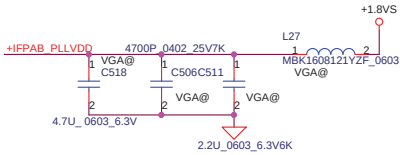
Date: Thursday, January 10, 2008 | Sheet 34 of 51

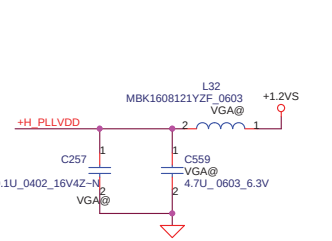


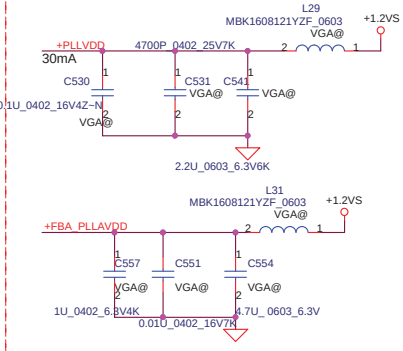


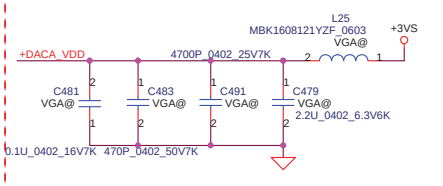






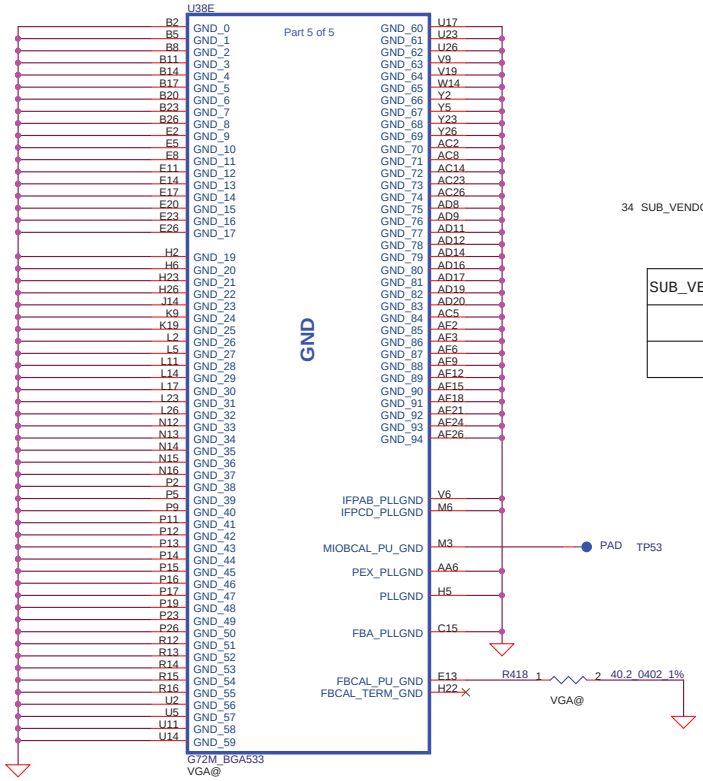






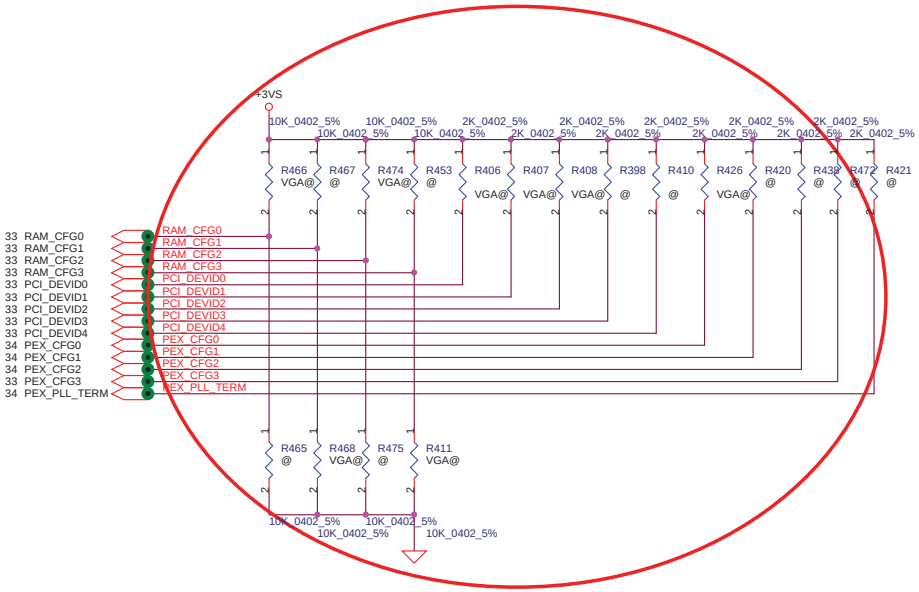
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.	
Title	NB8M-GS Power
Size: Custom	Document Number
Rev	0.4
Date: Thursday, January 10, 2008	Sheet 35 of 51



SUB_VENDOR	
0	N0 VIDEO BIOS ROM
1	BIOS ROM is present(Default)

STRAPS	PIN	DESCRIPTION	Value	Value
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9,8,6]	Recommended for G7x	001	
RAM_CFG[3:0]	MIOAD[5:2]	**RAM_CFG[3] (Bandwidth 0=Full, 1=Half)**		
		RAM_CFG[2] (0=16M or 1=32M)		
		RAM_CFG[1:0] **(Manufacture)** **(01=Sam, 10=Inf, 11=Hyn)**		
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxx8 G72M-0x01D8 NB8M-GS : 0X0427 NB8M-SE : 0X0428	0111 1000	
		G72MV-0x01D7 TBD/TBD	0111	



Bandwidth	RAM Type	Vendor	
FULL R17	32M R11	Samsung	**R20, R19**
HALF R12	16M R16	Hynix	**R18, R19**
		Infineon	**R18, R21**

Package		
(10*12.5)	**Infineon GDDR2(400): SA00000S800 (HYB18T256161AFL-25)**	**Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)**
(11*13)	**Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)**	**Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)**
(8*13)	**Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)**	**Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)**

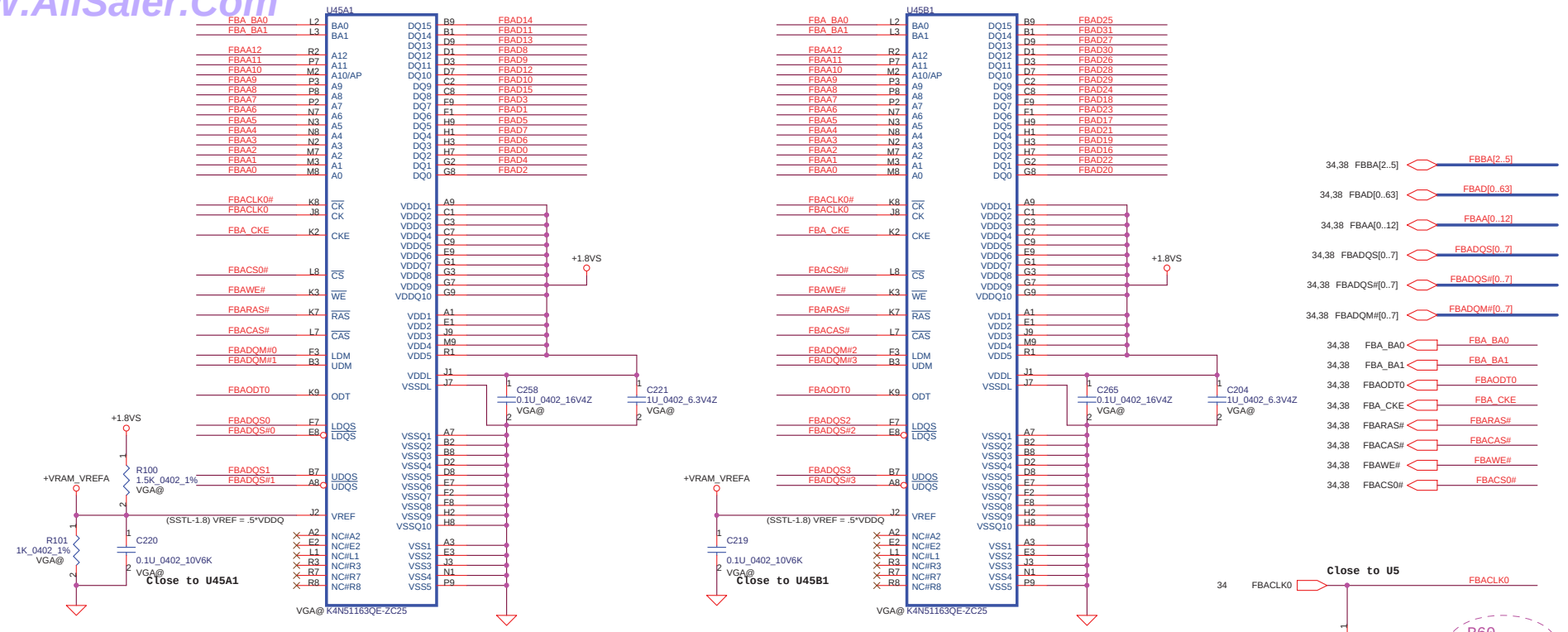
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

Compal Electronics, Inc.

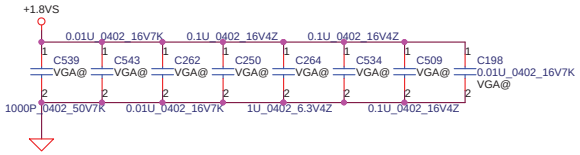
Title: NB8M-GS GND & STRAP

Size: Custom | Document Number | Rev: 0.4

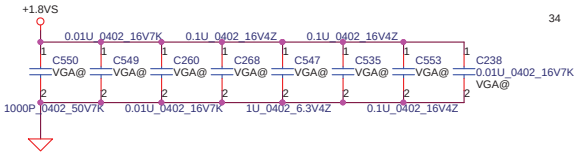
Date: Thursday, January 10, 2008 | Sheet 36 of 51



DDR2 BGA MEMORY

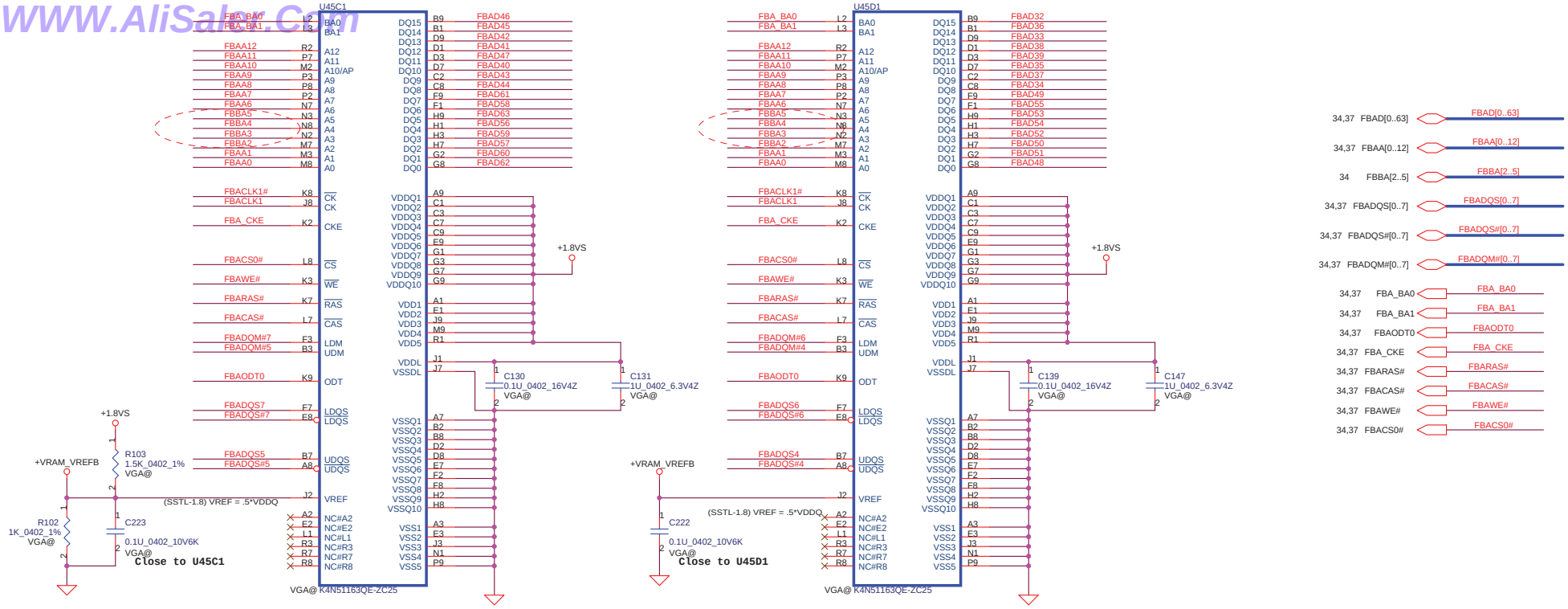


DDR2 BGA MEMORY



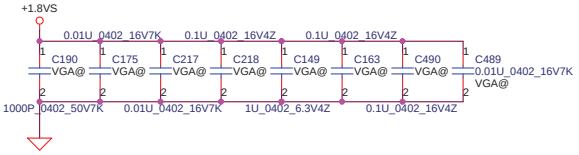
Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

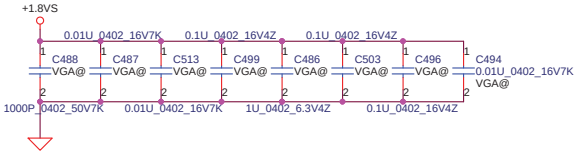
Compal Electronics, Inc.			
Title: VRAM DDRA			
Size: Custom	Document Number		Rev: 0.4
Date: Thursday, January 10, 2008	Sheet 37 of 51		

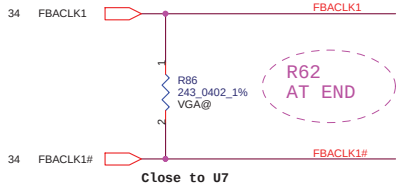


DDR2 BGA MEMORY

DDR2 BGA MEMORY

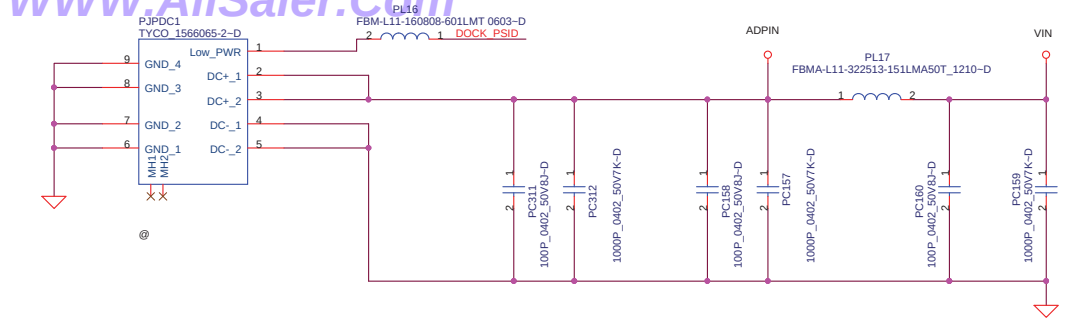


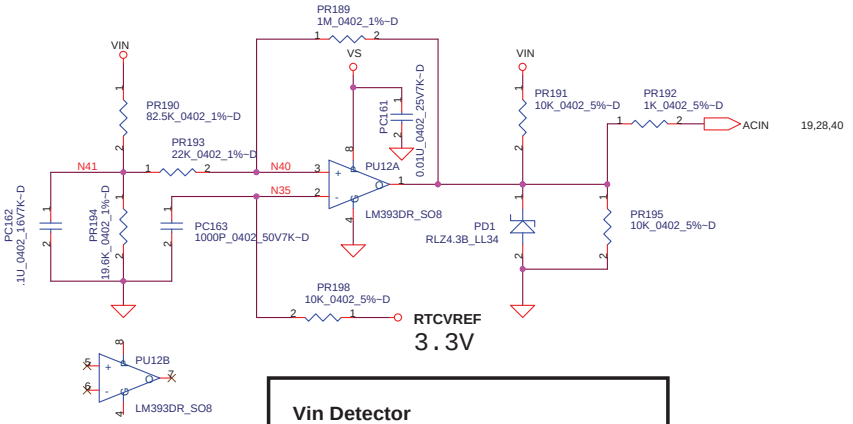




Security Classification	Compal Secret Data		
Issued Date	2006/07/10	Deciphered Date	2007/07/10

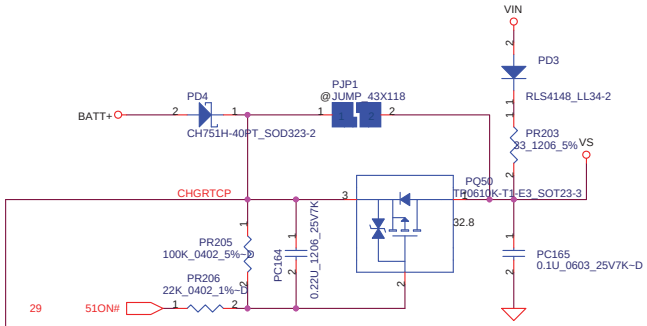
Compal Electronics, Inc.			
Title: VRAM DDRB			
Size: Custom	Document Number		Rev: 0.4
Date: Thursday, January 10, 2008	Sheet 38 of 51		

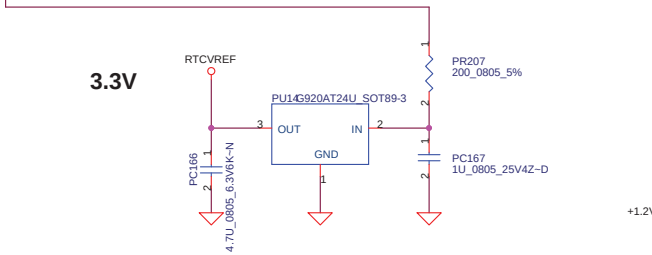


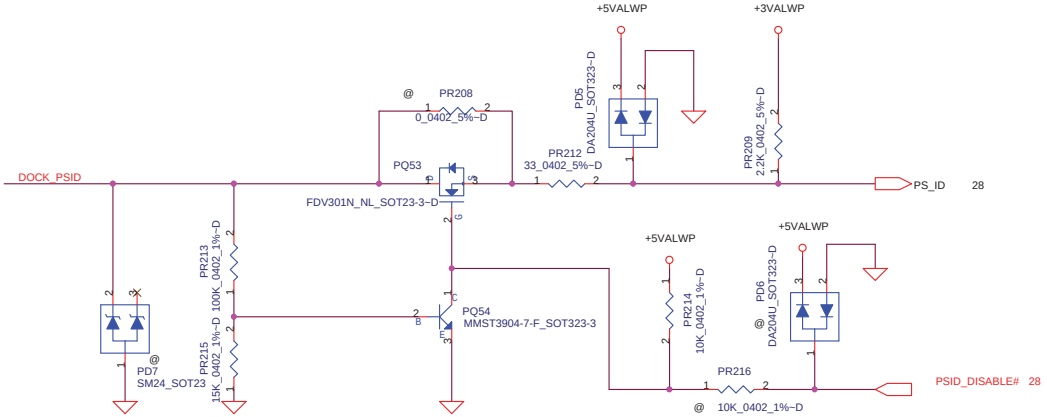


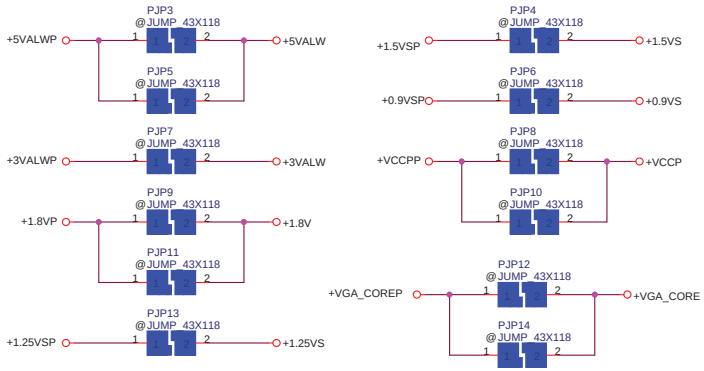
Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813







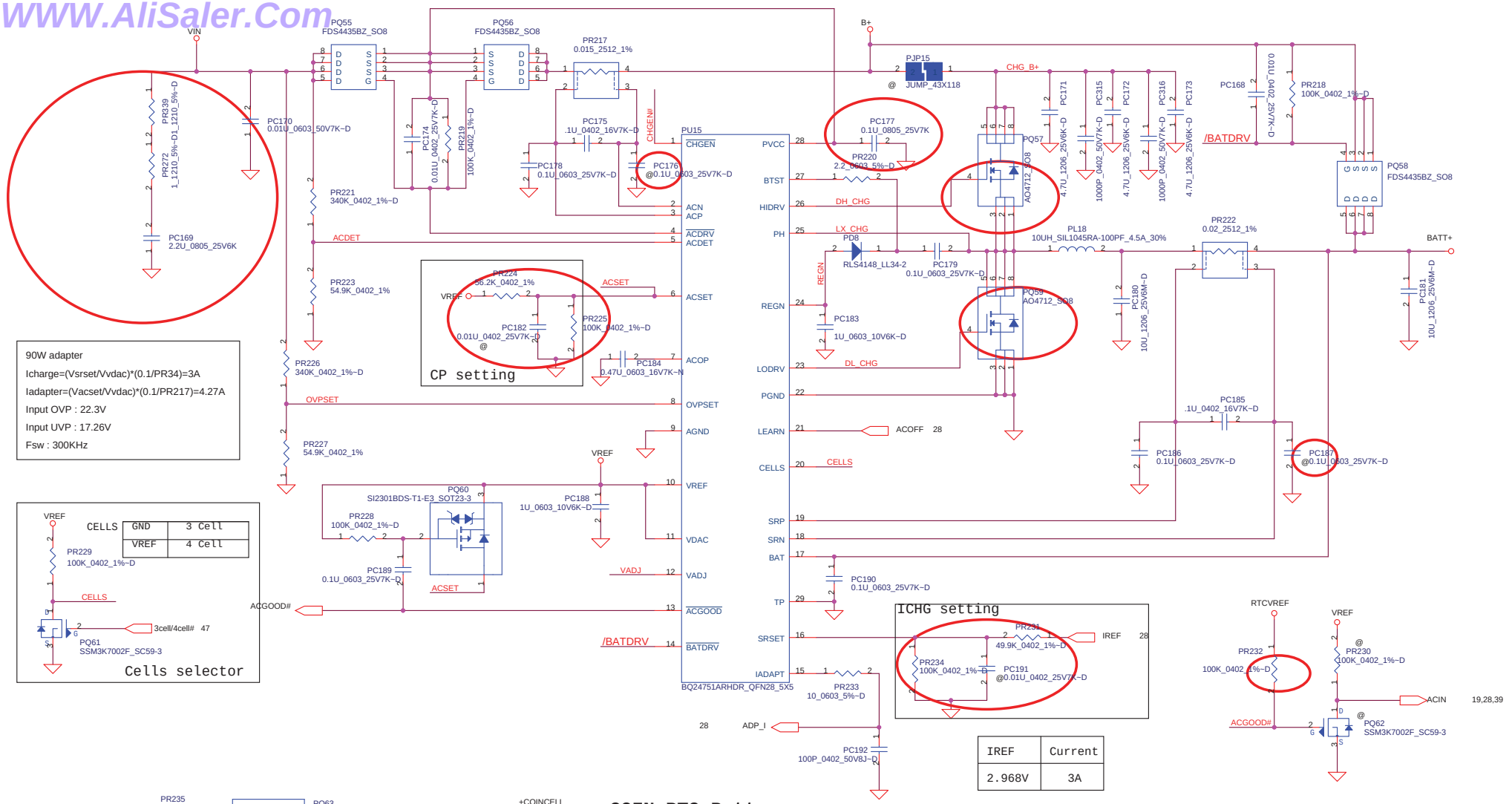


Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title: **DCIN / Precharge**

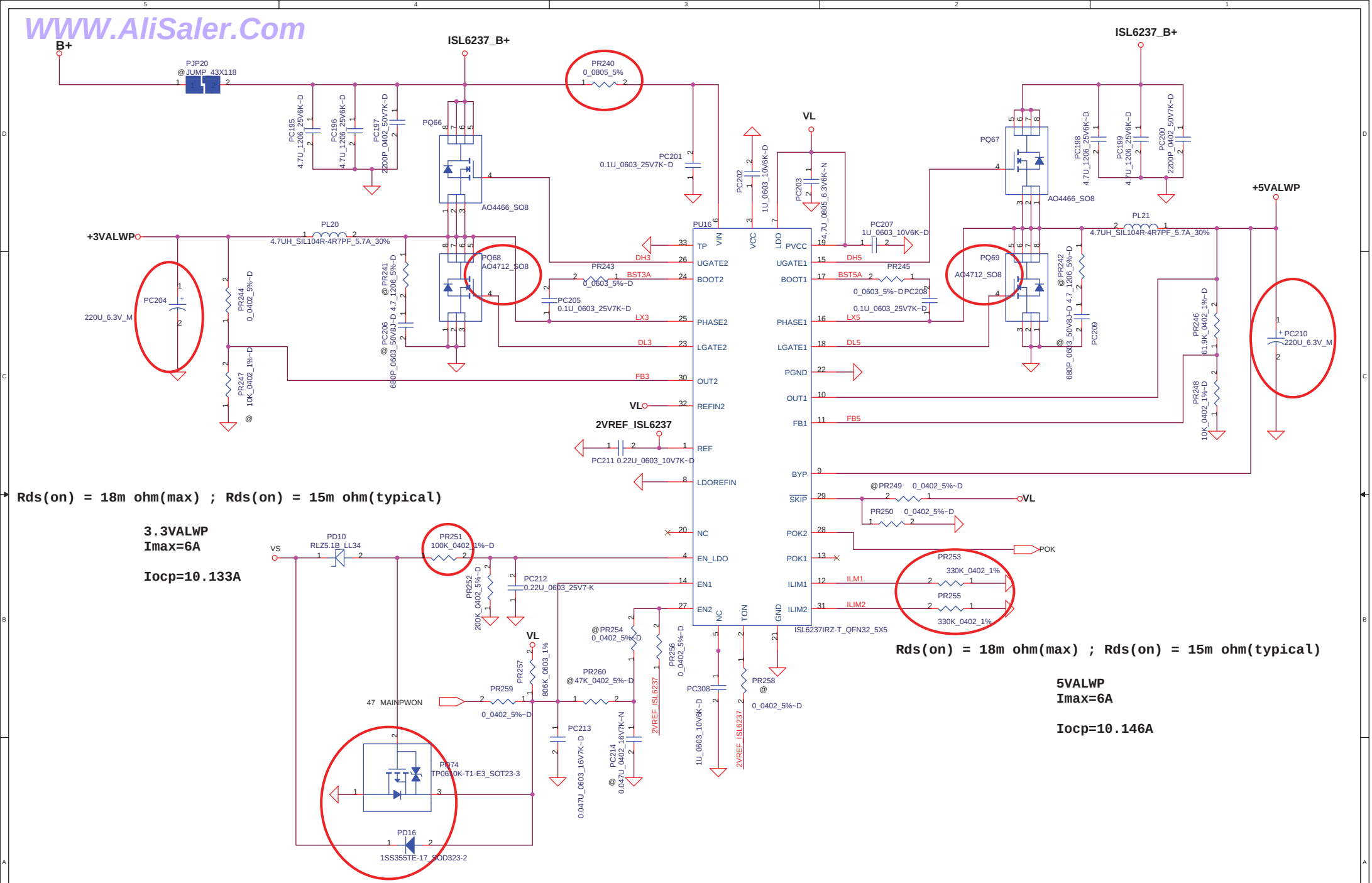
Size	Document Number	Rev
Custom	JAL30	0.2

Date: Thursday, January 10, 2008 | Sheet 39 of 51

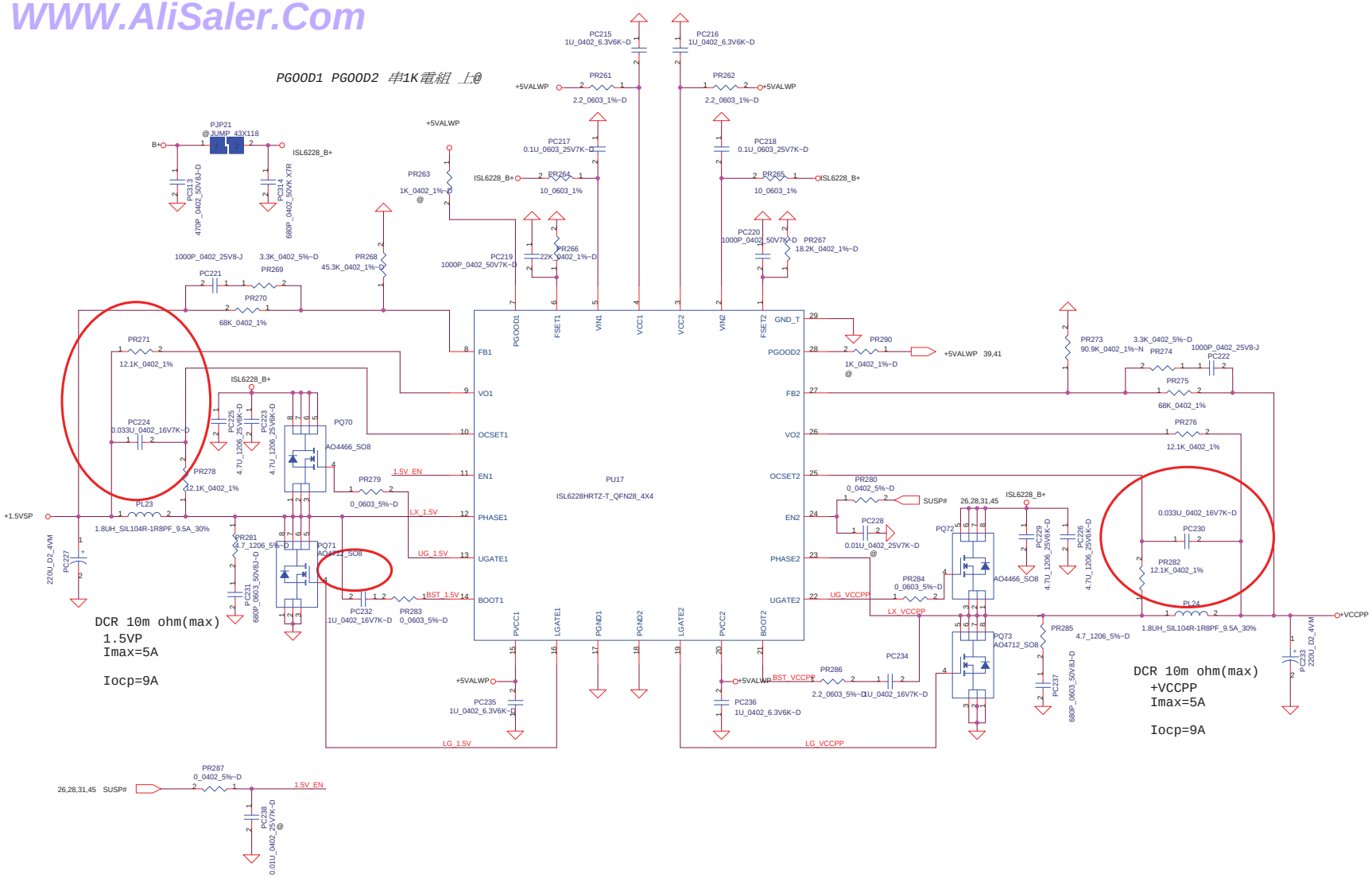


Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Compal Electronics, Inc.	
Title	Charger/RTC BATTERY
Size: B	Document Number: JAL30
Rev	0.2
Date: Thursday, January 10, 2008	Sheet 40 of 51

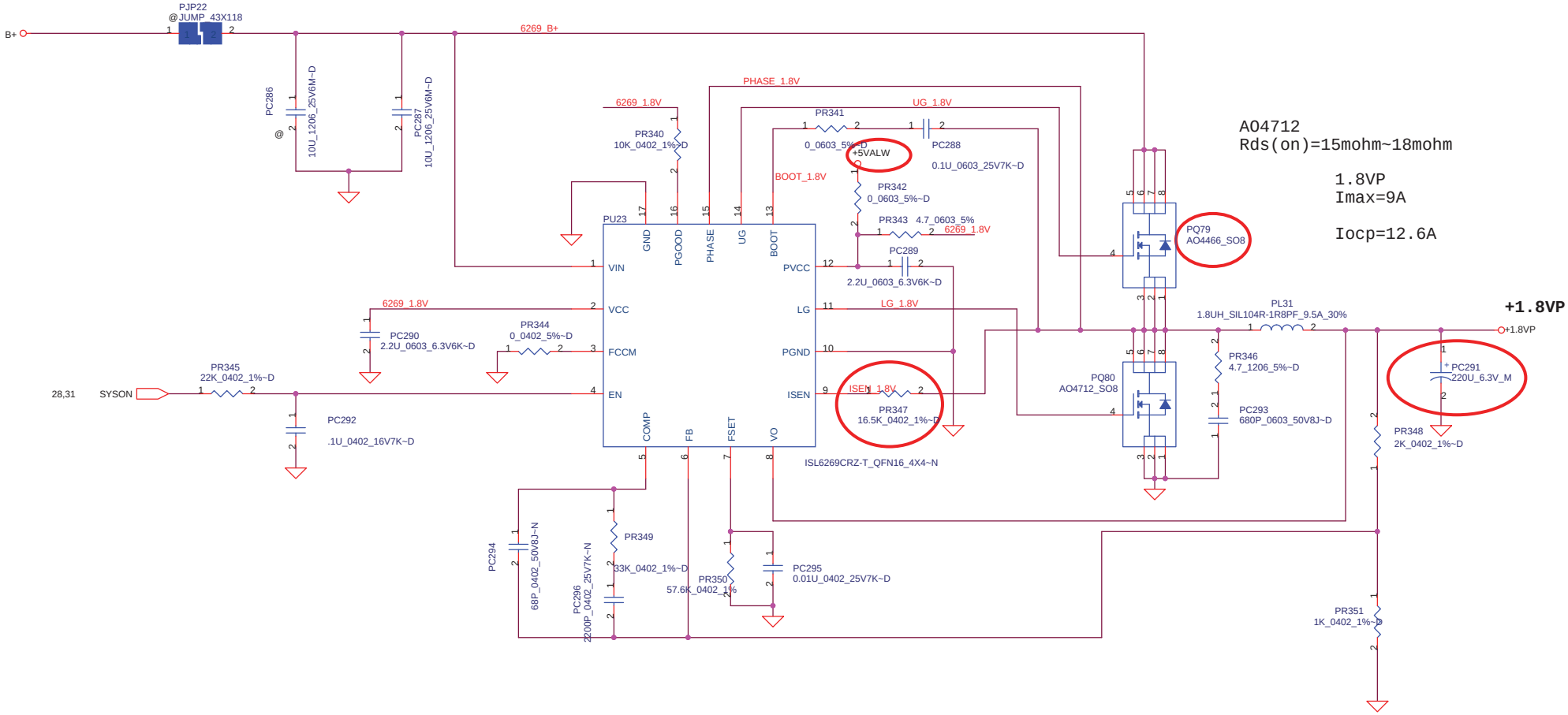


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/10/1	Deciphered Date	2007/05/30
Title	+3VALWP, +5VALWP		
Size: Custom	Document Number: JAL30		Rev: 0.2
Date: Thursday, January 10, 2008	Sheet 41 of 51		



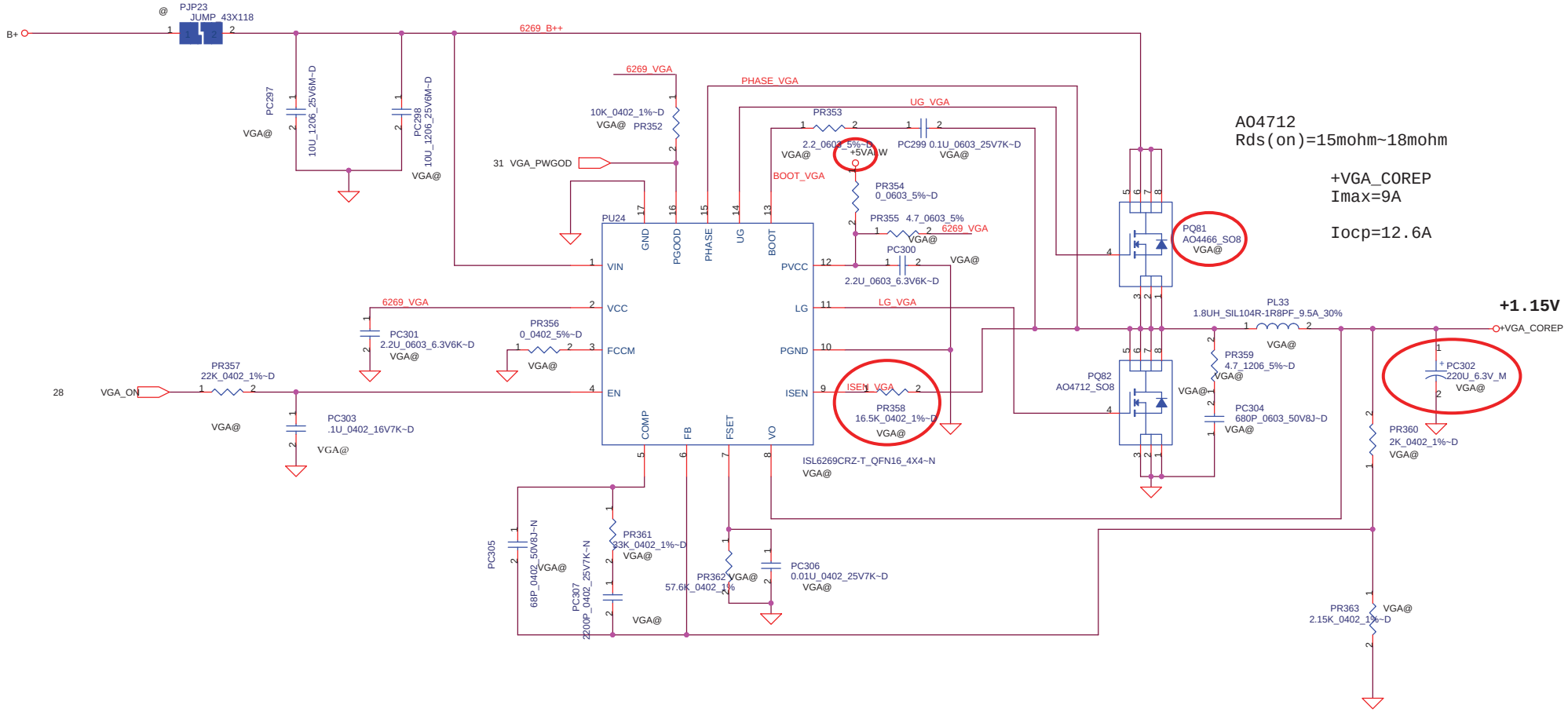
Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/5/01

Title	+1.5VP/VCCPP		
Size	Document Number	JAL30	Rev 0.2
Date: Thursday, January 10, 2008	Sheet 42 of 51		



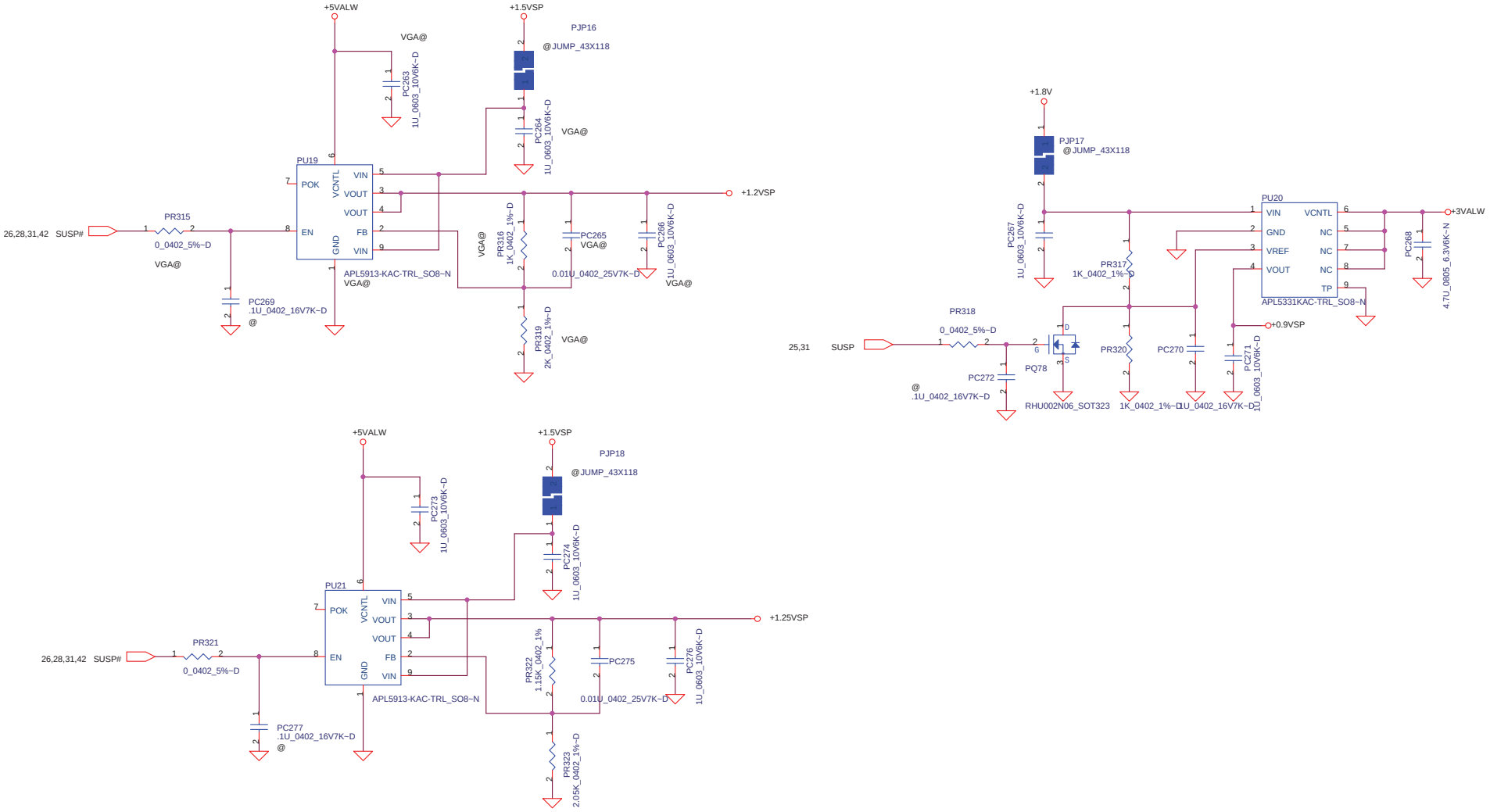
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2006/10/1	Deciphered Date	2007/05/30

Title	NB_CORE		
Size	Document Number	JAL30	Rev 0.11
Date:	Thursday, January 10, 2008	Sheet 43 of 51	



Security Classification	Compal Secret Data		
Issued Date	2006/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.			
Title	+VGA_COREP		
Size	Document Number	JAL60	Rev 0.11
Date: Thursday, January 10, 2008	Sheet 44 of 51		



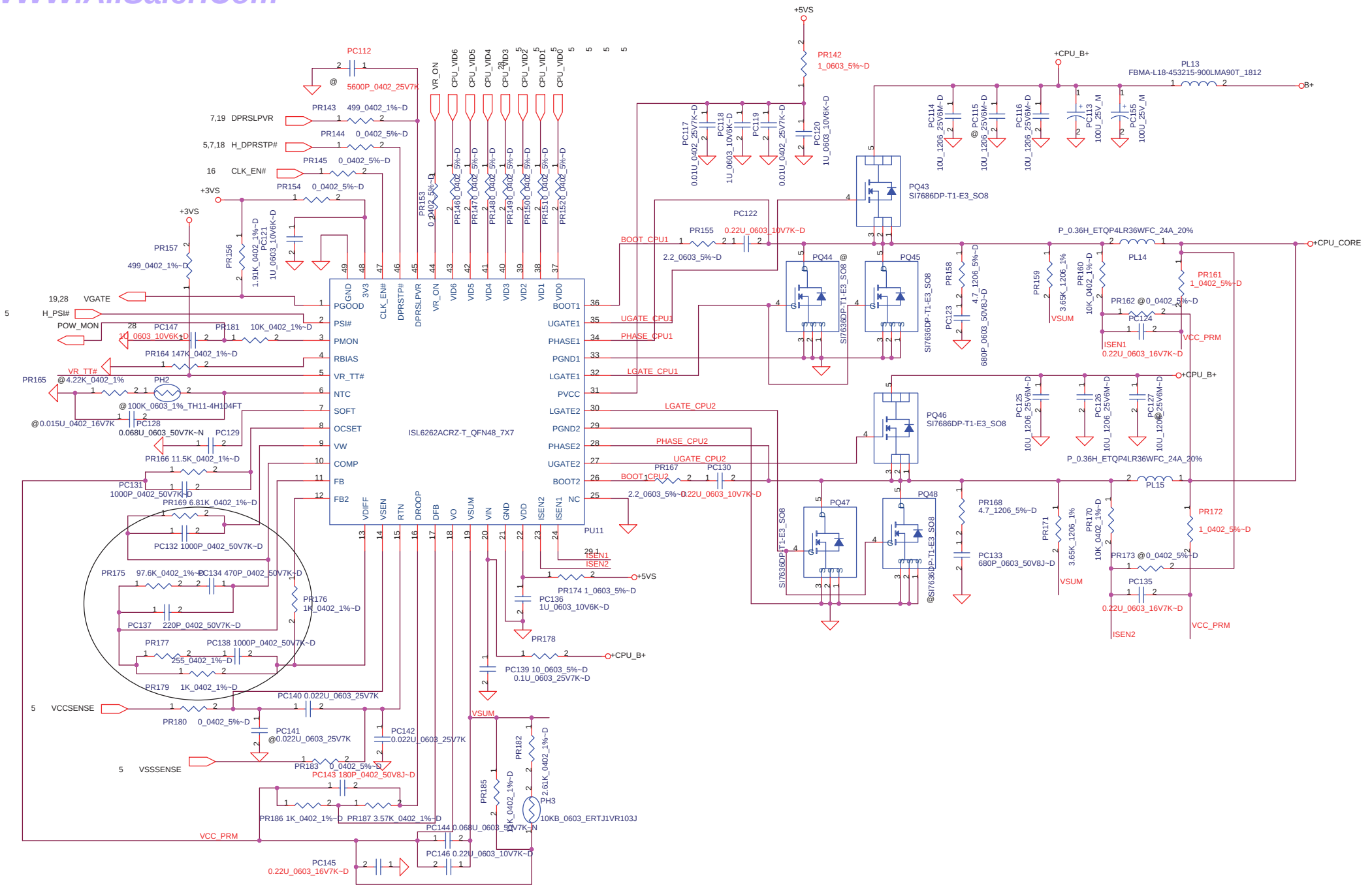
Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.

Title: **+1.25VSP / +0.9VSP/ +1.2VSP**

Size	Document Number	Rev
Custom	JAL30	0.2

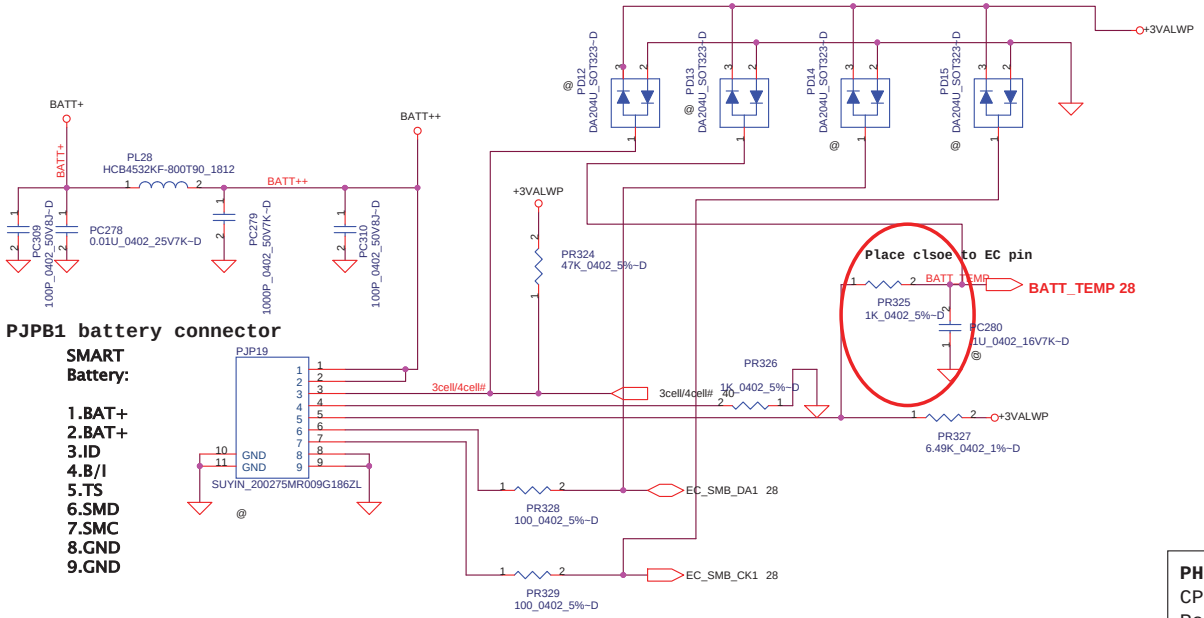
Date: Thursday, January 10, 2008 Sheet 45 of 51



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

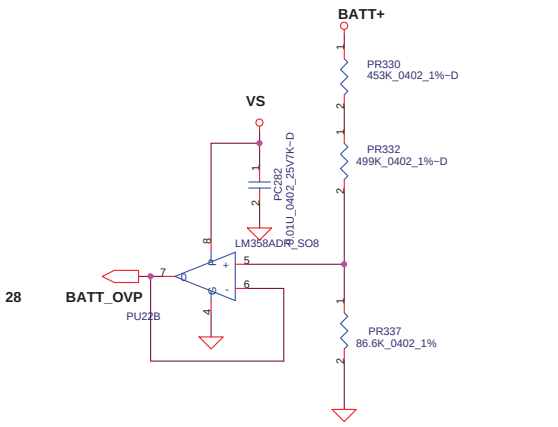
Compal Electronics, Inc.			
Title: +CPU_CORE			
Size: Custom	Document Number: JAL30		Rev: 0.1
Date: Thursday, January 10, 2008	Sheet 46 of 51		

Battery Connect/OTP

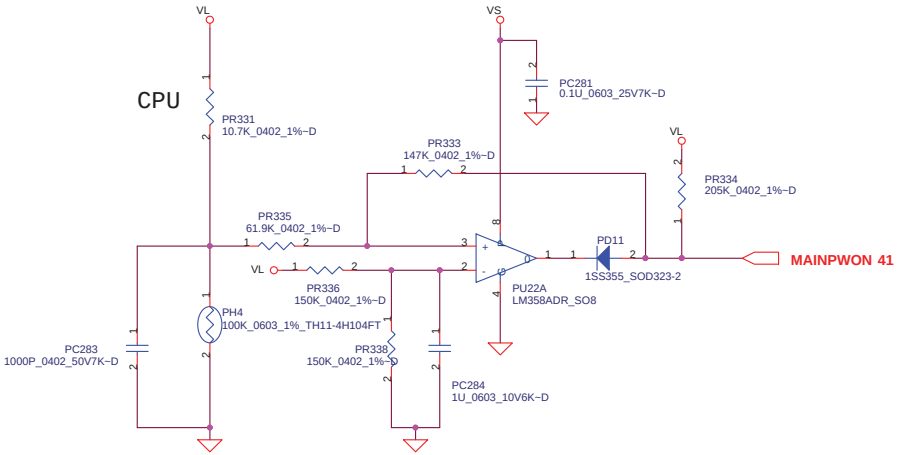


CPU

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+



Security Classification	Compal Secret Data		
Issued Date	2005/10/1	Deciphered Date	2007/05/30

Compal Electronics, Inc.			
Title	BATTERY CONN		
Size: Custom	Document Number: JAL30		Rev: 0.2
Date: Thursday, January 10, 2008	Sheet 47 of 51		

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	+3VALWP/+5VALWP	07/11/19	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PQ76 to turn off 5VALWP wehn shut down the system in the DC-mode	
2	40	Charge	07/11/25	COMPAL	Change RTC circuitry part	del PD16 PC285 PL29 JRTC1	
3	40	Charge	07/11/25	COMPAL	change charge voltage can to adjust	ADD PR53 PR54	
4	40	Charge	07/11/25	COMPAL	increase Coin RTC battery circuitry	ADD PD2 PR1 PC1	
5	40	Charge	07/11/25	COMPAL	increase BQ24751 Vin Detector function	increase PR232	
6	40	Charge	07/12/26	COMPAL	change charge voltage can to adjust	Change PR53 from 15K to 4.3K	
7	42	1.5VSP/+VCCPP	07/12/26	COMPAL	adjust 1.5VSP/+VCCPP OCP set	Change PR271 PR276 PR278 PR282 from 9.09K to 12.1K	
8	43	1.8VP	07/12/26	COMPAL	adjust 1.8VP OCP set	Change PR347 from 12.1K to 16.5K	
9	44	VGA_CORE	07/12/26	COMPAL	adjust VGA_CORE OCP set	Change PR358 from 12.1K to 16.5K	
10	41	+3VALWP/+5VALWP	07/12/26	COMPAL	The schematic location doesn't correspond to PCBA	Change location from PQ76 to PQ74	
11	43	1.8VP	07/12/26	COMPAL	delete resistor 0ohm for HW request	DEL PR342	
12	44	VGA_CORE	07/12/26	COMPAL	delete resistor 0ohm for HW request	DEL PR354	
13	46	CPU_CORE	07/12/26	COMPAL	modify MOS type SO8 to Power Pack for height limit	DEL PQ44 PQ48	
14	43	1.8VP	08/01/04	COMPAL	In order to replace IC for system request	ADD PU23 PR342	
15	44	VGA_CORE	08/01/04	COMPAL	In order to replace IC for system request	ADD PU24 PR354	
16	41	+3VALWP/+5VALWP	08/01/04	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PD16 to turn off 5VALWP wehn shut down the system in the DC-mode	
17	40	Charge	08/01/04	COMPAL	adjust battery charge voltage set	CHANGE PR53 from 15K to 4.3K	
18	40	Charge	08/01/04	COMPAL	VIN Detector has the same function	DEL PR230 PQ62	
19							
20			08/01/04	COMPAL	Increase Resistor on charge boot for EMI request	CHANGE PR220 PR286from 0 to 2.2 ohm	
21			08/01/04	COMPAL	Increase Capacitor on charge boot for EMI request	ADD PC123 PC133 PC231 PC237 PC309 PC310 PC311 PC313 PC312 PC314 PC293	
22			08/01/04	COMPAL	Increase Resistor on charge boot for EMI request	ADD PR158 PR168 PR285 PR281 PR346	
23			08/01/04	COMPAL	Increase Bead on charge boot for EMI request	ADD PL17 PL28	
24							
25							
26							
27							
28							
29							
30							
31							
32							

Compal Electronics, Inc.

Title: PW PIR-1

Size: Custom | Document Number: LA-3682P | Rev: 0.1

Date: Thursday, January 10, 2008 | Sheet 48 of 51

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	24	P24-Mini-Card/WWAN/Roboson	2007/2/3	Compal HW	LED1 Pin3 and Pin4 swap cause BATT_LOW_LED# no function.	Correct LED1 footprint to LED_HT-297UD-CB_4P	0.2 (SW1-13.3")
2	22	P22-Gigabit LAN(BCM5787M)	2007/2/3	Compal HW	+3VLAN voltage abnormally	Add Q46 for B+_BIAS turn on	0.2 (SW1-13.3")
3	19	P19-ICH8(3/4)_DMI,USB,GPIO,PCIE	2007/2/3	Compal HW	R121 no need for INTEL no reserve	Un mount R121	0.2 (SW1-13.3")
4	19	P22-Gigabit LAN(BCM5787M)	2007/2/13	Compal HW	Can't install MAC to EEPROM due to VCC 2.04V only	Change R4 to 0ohm or short R4.	0.2 (SW1-13.3")
5	29	P29-EC KB926/REED SW/TPM1.2	2007/3/1	Compal HW	KB matrix error by use AK1 KB circuit	Modify to SW1 KB pin define	0.2 (SW1-13.3")
6	27	P27-CardBus/R5C803	2007/3/1	Compal HW	CB_PME# pull high of two kind power plan (+3V & +3V_SB)	Un-mount R419	0.2 (SW1-13.3")
7	32	P32-DC/DC Interface	2007/5/11	Compal HW	No VGAPOWERGOOD for turn on +1.8VS	Add pull hish +3VS for VGA_PWGOD	0.2
8	11	P11-CRESTLINE(5/6)-PWR/GND	2007/5/11	Compal HW	VCCP no power	Remove C140(0 ohm in VGA BOM)	
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Compal Electronics, Inc.

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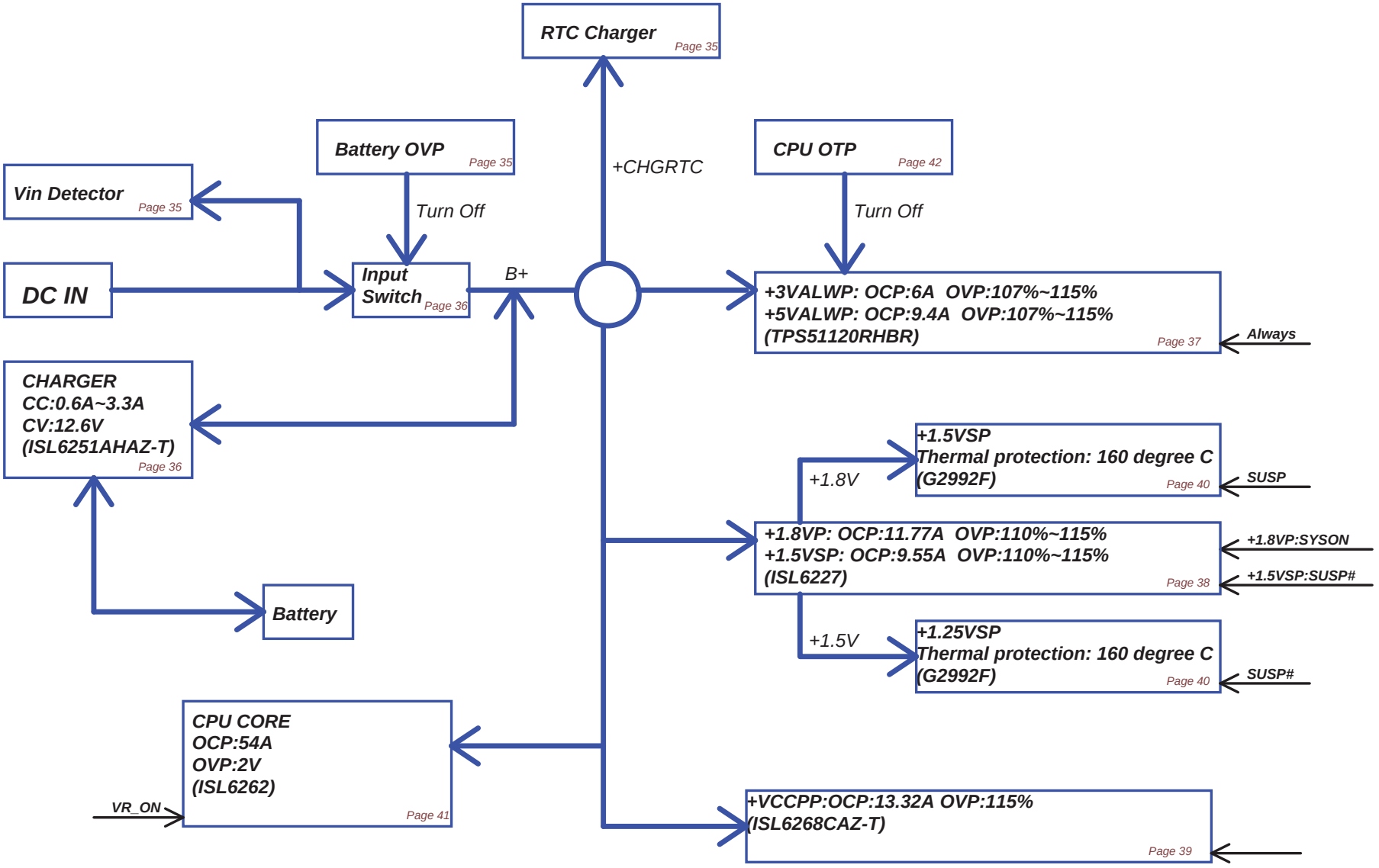
Size: Custom | Document Number: LA-4121P | Rev: 0.4

Date: Thursday, January 10, 2008 | Sheet 49 of 51

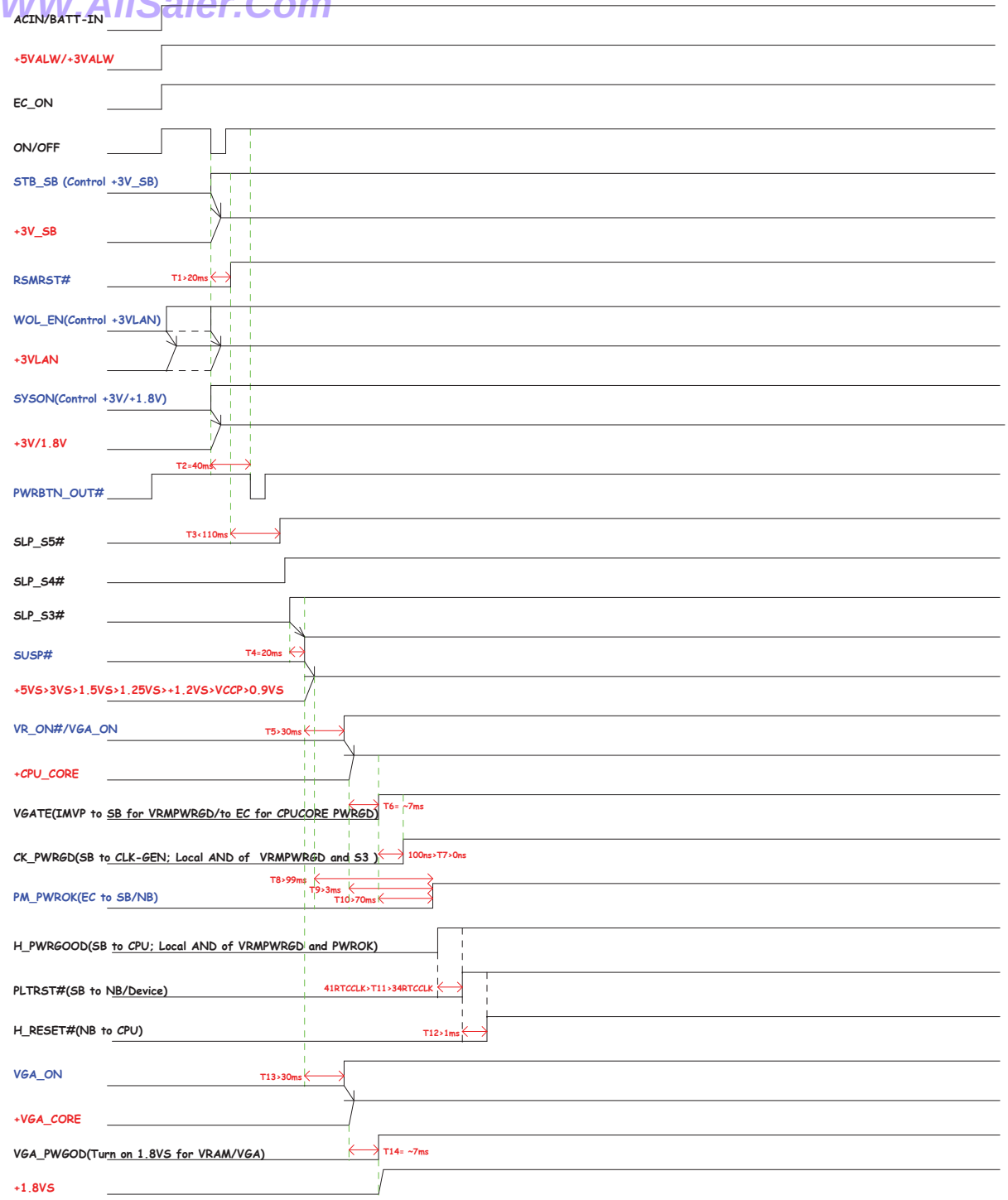
JAL30 Power Bock



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

Title: Power Block

Size: Custom	Document Number: LA-4121P	Rev: 0.4
Date: Thursday, January 10, 2008	Sheet 50 of 51	



Security Classification	Compal Secret Data		
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Title: *Power On Sequence*

Size	Document Number	Rev
Custom	*LA-4121P*	0.4
Date: Thursday, January 10, 2008	Sheet 51 of 61	