

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	APPD DATE
			2010-07-23

SCHEN, MLB, K16


07/23/2010

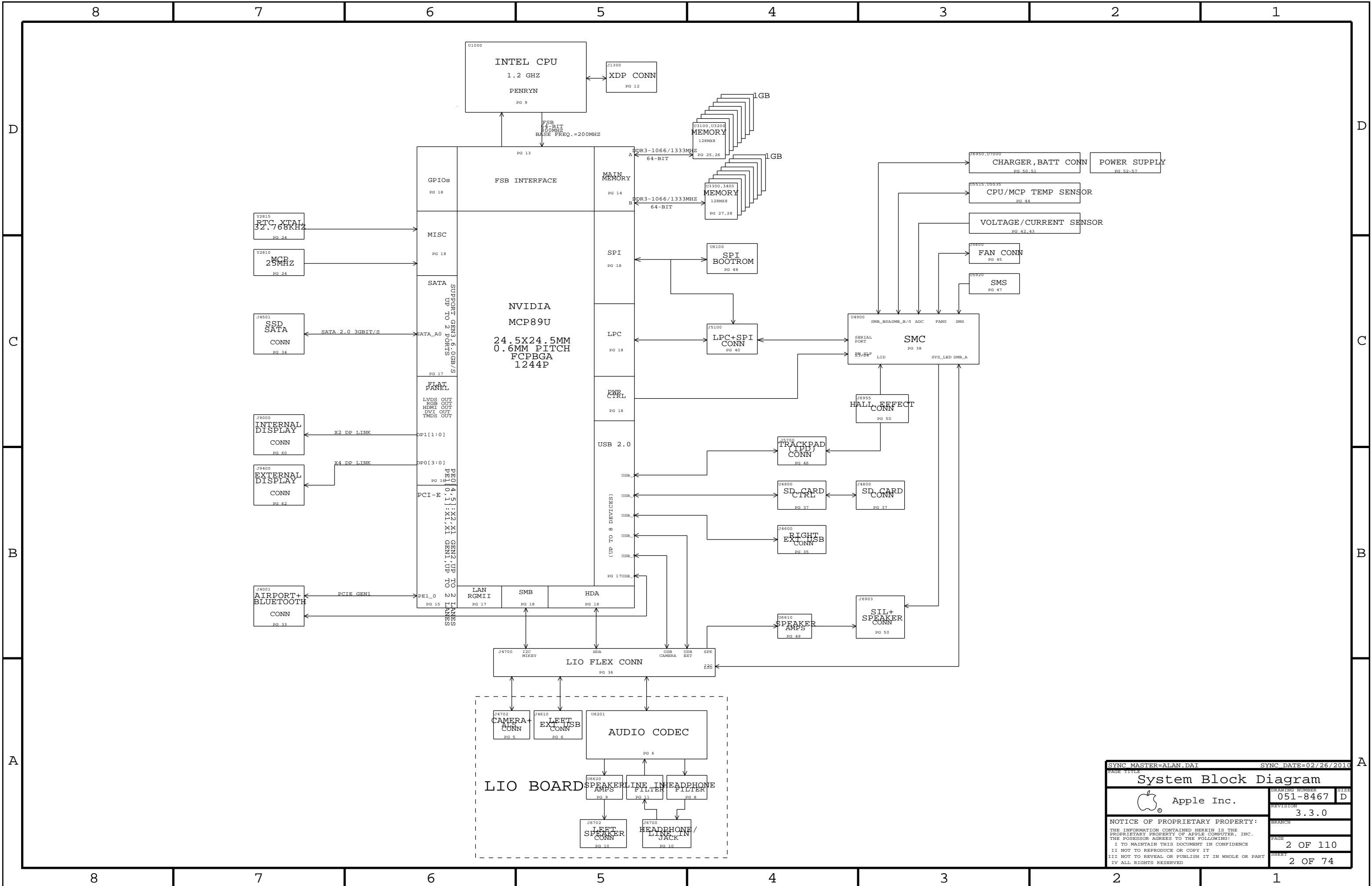
Page	Contents	Sync	Date
1	Table of Contents	N/A	N/A
2	System Block Diagram		02/26/2010
3	Power Block Diagram		2/25/2010
4	BOM Configuration		12/11/2009
5	K16 BOM Variants	N/A	N/A
6	Revision History	N/A	N/A
7	Functional Test / No Test	(K99_MLB)	(02/16/2010)
8	Power Aliases	(K99_MLB)	(02/11/2010)
9	Signal Aliases	(MASTER)	(MASTER)
10	CPU FSB	K99_MLB	04/08/2010
11	CPU Power & Ground	K99_MLB	04/08/2010
12	CPU Decoupling & VID	(K99_MLB)	(02/11/2010)
13	eXtended Debug Port (Micro-XDP)	K99_MLB	03/01/2010
14	MCP CPU Interface	K99_MLB	04/08/2010
15	MCP Memory Interface	K99_MLB	04/08/2010
16	MCP PCIe Interfaces	K99_MLB	04/08/2010
17	MCP Graphics	K99_MLB	04/08/2010
18	MCP SATA, USB & Ethernet	K99_MLB	04/08/2010
19	MCP HDA, LPC & MISC	K99_MLB	04/08/2010
20	MCP Power & Ground	K99_MLB	04/08/2010
21	MCP89 Memory Rail Gating	K99_MLB	04/08/2010
22	MCP89 GFX Core Rail Gating	K99_MLB	04/08/2010
23	MCP Standard Decoupling	K99_MLB	04/08/2010
24	MCP Graphics Support	K99_MLB	04/08/2010
25	SB Misc	(K99_MLB)	(02/11/2010)
26	DDR3 DRAM Channel A (0-31)	K99_MLB	04/08/2010
27	DDR3 DRAM Channel A (32-63)	K99_MLB	04/08/2010
28	DDR3 DRAM Channel B (0-31)	K99_MLB	04/08/2010
29	DDR3 DRAM Channel B (32-63)	K99_MLB	04/08/2010
30	DDR BYPASSING 1	K99_MLB	04/08/2010
31	DDR BYPASSING 2	K99_MLB	04/08/2010
32	Memory Active Termination	K99_MLB	04/08/2010
33	FSB/DDR3 Vref Margining	K99_MLB	04/08/2010
34	X21 WIRELESS CONNECTOR	K99_MLB	04/08/2010
35	SATA CONNECTOR	K99_MLB	04/08/2010
36	External USB Connectors	K99_MLB	03/01/2010
37	Left I/O (LIO) Connector	(MASTER)	(MASTER)
38	SecureDigital Card Reader	(MASTER)	(MASTER)


Page	Contents	Sync	Date
39	SMC	K16_MLB	06/01/2010
40	SMC Support	(K99_MLB)	(03/01/2010)
41	LPC+SPI Debug Connector	K99_MLB	04/08/2010
42	K16/K99 SMUS Connections	K99_MLB	07/23/2010
43	Voltage & Current Sensing	K99_MLB	04/08/2010
44	Current Sensing	K99_MLB	04/08/2010
45	Thermal Sensors	K99_MLB	04/08/2010
46	Fan	K99_MLB	04/08/2010
47	WELLSPRING 1	K99_MLB	04/08/2010
48	SPI ROM	K99_MLB	04/08/2010
49	AUDIO0: SPEAKER AMP	K99_MLB	04/08/2010
50	DC-In & Battery Connectors	(MASTER)	(MASTER)
51	PBus Supply & Battery Charger	(K99_MLB)	(02/16/2010)
52	5V / 3.3V Power Supply	K99_MLB	04/08/2010
53	1.5V/1.35V LVDDR3 Supply	K16_MLB	06/01/2010
54	IMVP6 CPU VCore Regulator	(K99_MLB)	(02/16/2010)
55	MCP VCore Regulator	(K99_MLB)	(02/11/2010)
56	CPUVTT (1.05V) Power Supply	(K99_MLB)	(03/01/2010)
57	Misc Power Supplies	K99_MLB	04/08/2010
58	Power Sequencing	K99_MLB	04/08/2010
59	Power FETs	K99_MLB	04/08/2010
60	Internal DisplayPort Connector	K99_MLB	07/23/2010
61	External DisplayPort Support	K99_MLB	04/08/2010
62	DisplayPort Connector	K16_MLB	06/01/2010
63	LCD Backlight Driver	(K99_MLB)	(03/01/2010)
64	LCD Backlight Support	K99_MLB	04/08/2010
65	Additional CPU/GPU Decoupling	K99_MLB	05/18/2010
66	CPU/FSB Constraints	K99_MLB	04/08/2010
67	Memory Constraints	K99_MLB	04/08/2010
68	MCP Constraints 1	K99_MLB	04/08/2010
69	MCP Constraints 2	K99_MLB	04/08/2010
70	Ethernet Constraints	K99_MLB	04/08/2010
71	SMC Constraints	K99_MLB	04/08/2010
72	K16/K99 Specific Constraints	T27_MLB	09/08/2009
73	K99 RULE DEFINITIONS	K99_MLB	04/08/2010
74	Acoustic Cap BOM Config Tables	K16_MLB	06/01/2010

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8467	1	SCHEM,MLB,K16	SCH	CRITICAL	
820-2838	1	PCBF,MLB,K16	PCB	CRITICAL	

DRAWING TITLE		SCHEM, MLB, K16	
 Apple Inc.	DRAWING NUMBER	051-8467	SIZE
	REVISION	D	
	3.3.0		
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		PAGE	1 OF 110
		SHEET	1 OF 74



SYNC MASTER=ALAN.DAI		SYNC DATE=02/26/2010	
PAGE TITLE			
System Block Diagram			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	2 OF 110
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	2 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

[illegible]

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B

A

D

C

B


	8	7	6	5	4	3	2	1									
BOM Variants				Bar Code Labels / EEE #'s													
D	BOM NUMBER	BOM NAME	BOM OPTIONS		PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION							
	639-1070	PCBA,MLB,1.86GHZ HY 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWQ,CAPS:MU,DDR3:HYNIX_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWM]	CRITICAL	EEEE:DCWM							
	639-0837	PCBA,MLB,1.86GHZ,HY 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXW,CAPS:SS,DDR3:HYNIX_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWN]	CRITICAL	EEEE:DCWN							
	639-1096	PCBA,MLB,1.86GHZ HY 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXN,CAPS:TY,DDR3:HYNIX_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWP]	CRITICAL	EEEE:DCWP							
	639-1101	PCBA,MLB,1.86GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXV,CAPS:MU,DDR3:HYNIX_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWQ]	CRITICAL	EEEE:DCWQ							
	639-1098	PCBA,MLB,1.86GHZ HY 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXQ,CAPS:SS,DDR3:HYNIX_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWR]	CRITICAL	EEEE:DCWR							
	639-1068	PCBA,MLB,1.86GHZ HY 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWN,CAPS:TY,DDR3:HYNIX_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWT]	CRITICAL	EEEE:DCWT							
	639-1083	PCBA,MLB,1.86GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX6,CAPS:MU,DDR3:MICRON_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWV]	CRITICAL	EEEE:DCWV							
	639-1078	PCBA,MLB,1.86GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX1,CAPS:SS,DDR3:MICRON_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWW]	CRITICAL	EEEE:DCWW							
	639-1090	PCBA,MLB,1.86GHZ MI 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXG,CAPS:TY,DDR3:MICRON_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWX]	CRITICAL	EEEE:DCWX							
C	639-1088	PCBA,MLB,1.86GHZ MI 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXD,CAPS:MU,DDR3:MICRON_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCWY]	CRITICAL	EEEE:DCWY							
	639-1067	PCBA,MLB,1.86GHZ MI 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWM,CAPS:SS,DDR3:MICRON_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX0]	CRITICAL	EEEE:DCX0							
	639-1077	PCBA,MLB,1.86GHZ MI 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX0,CAPS:TY,DDR3:MICRON_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX1]	CRITICAL	EEEE:DCX1							
	639-1080	PCBA,MLB,1.86GHZ SA 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX2,CAPS:MU,DDR3:SAMSUNG_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX2]	CRITICAL	EEEE:DCX2							
	639-1095	PCBA,MLB,1.86GHZ SA 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXM,CAPS:SS,DDR3:SAMSUNG_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX3]	CRITICAL	EEEE:DCX3							
	639-1071	PCBA,MLB,1.86GHZ SA 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCWR,CAPS:TY,DDR3:SAMSUNG_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX4]	CRITICAL	EEEE:DCX4							
	639-1097	PCBA,MLB,1.86GHZ SA 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXP,CAPS:MU,DDR3:SAMSUNG_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX5]	CRITICAL	EEEE:DCX5							
	639-1084	PCBA,MLB,1.86GHZ SA 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCX7,CAPS:SS,DDR3:SAMSUNG_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX6]	CRITICAL	EEEE:DCX6							
	639-1091	PCBA,MLB,1.86GHZ SA 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DCXH,CAPS:TY,DDR3:SAMSUNG_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX7]	CRITICAL	EEEE:DCX7							
	639-1092	PCBA,MLB,2.13GHZ HY 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXJ,CAPS:MU,DDR3:HYNIX_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX8]	CRITICAL	EEEE:DCX8							
B	639-1082	PCBA,MLB,2.13GHZ,HY 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX5,CAPS:SS,DDR3:HYNIX_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCX9]	CRITICAL	EEEE:DCX9							
	639-1085	PCBA,MLB,2.13GHZ HY 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX8,CAPS:TY,DDR3:HYNIX_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXC]	CRITICAL	EEEE:DCXC							
	639-1089	PCBA,MLB,2.13GHZ HY 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXF,CAPS:MU,DDR3:HYNIX_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXD]	CRITICAL	EEEE:DCXD							
	639-1075	PCBA,MLB,2.13GHZ HY 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWX,CAPS:SS,DDR3:HYNIX_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXF]	CRITICAL	EEEE:DCXF							
	639-1079	PCBA,MLB,2.13GHZ HY 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX2,CAPS:TY,DDR3:HYNIX_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXG]	CRITICAL	EEEE:DCXG							
	639-1099	PCBA,MLB,2.13GHZ MI 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXR,CAPS:MU,DDR3:MICRON_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXH]	CRITICAL	EEEE:DCXH							
	639-1087	PCBA,MLB,2.13GHZ MI 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXC,CAPS:SS,DDR3:MICRON_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXJ]	CRITICAL	EEEE:DCXJ							
	639-1069	PCBA,MLB,2.13GHZ MI 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWP,CAPS:TY,DDR3:MICRON_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXK]	CRITICAL	EEEE:DCXK							
	639-1100	PCBA,MLB,2.13GHZ MI 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXT,CAPS:MU,DDR3:MICRON_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXL]	CRITICAL	EEEE:DCXL							
	639-1093	PCBA,MLB,2.13GHZ MI 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXK,CAPS:SS,DDR3:MICRON_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXM]	CRITICAL	EEEE:DCXM							
A	639-1076	PCBA,MLB,2.13GHZ MI 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWY,CAPS:TY,DDR3:MICRON_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXN]	CRITICAL	EEEE:DCXN							
	639-1074	PCBA,MLB,2.13GHZ SA 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWW,CAPS:MU,DDR3:SAMSUNG_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXP]	CRITICAL	EEEE:DCXP							
	639-1072	PCBA,MLB,2.13GHZ SA 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWT,CAPS:SS,DDR3:SAMSUNG_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXQ]	CRITICAL	EEEE:DCXQ							
	639-1086	PCBA,MLB,2.13GHZ SA 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX9,CAPS:TY,DDR3:SAMSUNG_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXR]	CRITICAL	EEEE:DCXR							
	639-1073	PCBA,MLB,2.13GHZ SA 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCWV,CAPS:MU,DDR3:SAMSUNG_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXT]	CRITICAL	EEEE:DCXT							
	639-1081	PCBA,MLB,2.13GHZ SA 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCX4,CAPS:SS,DDR3:SAMSUNG_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXV]	CRITICAL	EEEE:DCXV							
	639-1094	PCBA,MLB,2.13GHZ SA 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DCXL,CAPS:TY,DDR3:SAMSUNG_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DCXW]	CRITICAL	EEEE:DCXW							
	639-1450	PCBA,MLB,1.86GHZ EL 2GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG4W,CAPS:MU,DDR3:ELPIDA_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG4W]	CRITICAL	EEEE:DG4W							
	639-1451	PCBA,MLB,1.86GHZ EL 2GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG4Y,CAPS:SS,DDR3:ELPIDA_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG4Y]	CRITICAL	EEEE:DG4Y							
	639-1455	PCBA,MLB,1.86GHZ EL 2GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG53,CAPS:TY,DDR3:ELPIDA_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG53]	CRITICAL	EEEE:DG53							
	639-1453	PCBA,MLB,2.13GHZ EL 2GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG51,CAPS:MU,DDR3:ELPIDA_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG51]	CRITICAL	EEEE:DG51							
	639-1454	PCBA,MLB,2.13GHZ EL 2GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG52,CAPS:SS,DDR3:ELPIDA_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG52]	CRITICAL	EEEE:DG52							
	639-1452	PCBA,MLB,2.13GHZ EL 2GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG50,CAPS:TY,DDR3:ELPIDA_2GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG50]	CRITICAL	EEEE:DG50							
	639-1458	PCBA,MLB,1.86GHZ EL 4GB,MU CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5P,CAPS:MU,DDR3:ELPIDA_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5P]	CRITICAL	EEEE:DG5P							
	639-1463	PCBA,MLB,1.86GHZ EL 4GB,SS CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5W,CAPS:SS,DDR3:ELPIDA_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5W]	CRITICAL	EEEE:DG5W							
	639-1460	PCBA,MLB,1.86GHZ EL 4GB,TY CAP,K16	K16_CMNPTS,CPU:1.86GHZ,EEEE:DG5T,CAPS:TY,DDR3:ELPIDA_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5T]	CRITICAL	EEEE:DG5T							
	639-1462	PCBA,MLB,2.13GHZ EL 4GB,MU CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5Q,CAPS:MU,DDR3:ELPIDA_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5Q]	CRITICAL	EEEE:DG5Q							
	639-1459	PCBA,MLB,2.13GHZ EL 4GB,SS CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5V,CAPS:SS,DDR3:ELPIDA_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5V]	CRITICAL	EEEE:DG5V							
	639-1461	PCBA,MLB,2.13GHZ EL 4GB,TY CAP,K16	K16_CMNPTS,CPU:2.13GHZ,EEEE:DG5R,CAPS:TY,DDR3:ELPIDA_4GB		825-7557	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE_DG5R]	CRITICAL	EEEE:DG5R							
	607-6915	CMN PTS,PCBA,MLB,K16	K16_COMMON														
085-1327	K16 MLB DEVELOPMENT BOM	K16_DEVEL:ENG															
SAMSUNG				MURATA				TAIYO YUDEN									
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	SS_CAP_2_2UF	138S0633	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	MU_CAP_2_2UF	138S0634	1	CAP, 2.2UF, 6.3V, 20%, 0402	C4807	CRITICAL	TY_CAP_2_2UF
K16-Specific BOM Tables																	
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION												
337S3751	1	PDC,SLGAB,PRQ,1.86,17W,1066,ED,6M,BGA	U1000	CRITICAL	CPU:1.86GHZ												
337S3758	1	PDC,SLGEQ,PRQ,2.13,17W,1066,ED,6M,BGA	U1000	CRITICAL	CPU:2.13GHZ												
341T0276	1	IC ASSY,SMC EXTERNAL,K16	U4900	CRITICAL	SMC:PROG												
341T0275	1	IC ASSY,EFI UNLOCKED,K16	U6100	CRITICAL	BOOTROM:UNLOCKED												
341S2785	1	IC EFI ROM,PVT,LOCKED,K16	U6100	CRITICAL	BOOTROM:LOCKED												
Sub-BOMs																	
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION												
085-1327	1	K16 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM												
607-6915	1	CMN PTS,PCBA,MLB,K16	CMNPTS	CRITICAL	K16_CMNPTS												
8	7	6	5	4	3	2	1										
A																	
SYNC MASTER=N/A SYNC DATE=N/A																	
PAGE TITLE																	
K16 BOM Variants																	
DRAWING NUMBER 051-8467 SIZE D																	
REVISION 3.3.0																	
BRANCH																	
PAGE 5 OF 110																	
SHEET 5 OF 74																	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED																	
8	7	6	5	4	3	2	1										

SYNC MASTER=N/A

SYNC DATE=N/A

PAGE TITLE

K16 BOM Variants

 Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

051-8467

REVISION

3.3.0

BRANCH

PAGE

5 OF 110

SHEET

5 OF 74

	8	7	6	5	4	3	2	1	
D	<div>Revision History</div> <div>Proto 0 (ECO #0000876215, v1.0.0, P4 change #210266, 03/16/2010)</div> <div><div>v1.1.0 (P4 change #211399, 03/24/2010)</div><div>MCP: 7742015 - Added RC to DDC pass FETs to avoid glitch (pp. 7, 93). 7788138 - Added feedback divider and BOM tables for more HVDD LDOs (pp. 4, 25). SMC: 7761747 - Added resistors to connect TCON to SMC or MCP SMBus (pp. 4, 52, 90). 7787883 - Added support for DP HPD wake / S4 state (pp. 4, 7, 8, 19, 49, 50, 78, 94). SMS: 7765466 - Added S3 pull-up to SMS_INT_L to prevent leakage path (pp. 50, 59). 7769139 - Unstuffed SMS circuit (pg. 4). General: 7787897 - Property/page fixes to reduce CheckPlus warnings/errors (pp. 7, 8, 12, 17, 74, 93, 108).</div><div>v1.2.0 (P4 change #211839, 03/26/2010)</div><div>USB: 7796626 - Changed port switch from TPS2052B to TPS2069 (pg. 46). SMC: 7787883 - Added PLACE_NEAR property on R5022 to avoid stub (pg. 50). SMBus: 7761747 - Added TCON I2C nets to FUNC_TEST list for J9000 (pg. 7). Power: 7796648 - Changed DP and LCD power from PP3V3_S3 to PP3V3_S5 (pp. 8, 90). 7796658 - Changed backlight driver to E00 version (pg. 97). BOM: 7796661 - Set up primary & alternate for power supply FET (pp. 4, 72). 7796654 - Consolidated SSM6N15FE to SSM6N37FE (pg. 48). 7796658 - Changed RCs on some SMC analog inputs (pg. 54). 7796683 - Stuffed RC on backlight driver PWM input (pg. 97). General: 7796631 - Sorted BOM variants for easier verification (pg. 5). 7796631 - Cosmetic clean-up (pg. 76).</div><div>v1.3.0 (P4 change #212050, 03/26/2010)</div><div>SMBus: 7761747 - Added isolation FET and unstuffed series R's on TCON I2C for now (pp. 4, 90, 108). Power Supply: 7796661 - Removed alternate FET, made some FETs primary to other APN (pp. 4, 72, 73, 76). 7798425 - R/C value changes for 3.42V G3Hot power supply (pg. 69). 7798399 - R/C value changes for 5V/3.3V power supply (pg. 72). 7800179 - R value changes for CPU VCore power supply (pg. 74). 7798445 - R value changes for 0.9V S5 power supply (pg. 77). 7796658 - Changed backlight driver back to non-E00 version (pp. 4, 97). BOM: 7796658 - Added alternates for two caps per GSM and removed unused alternates (pg. 4). 7798399 - Consolidated 100pF caps (pp. 74, 75).</div><div>v1.4.0 (P4 change #212757, 03/31/2010)</div><div>MCP SPI: 7809733 - Changed strapping to select 62.5MHz SPI bus frequency (pg. 4). SMBus: 7796631 - Added XDP connection to SMBus aliases page (pp. 13, 52). 7808530 - Changed SMC 'MGMT' SMBus pull-ups from 4.7K to 2K (pg. 52). 7761747 - Documented SMBus addresses for panel (pg. 52). SD Card: 7800415 - Changed SD Card discharge R to more standard value (pg. 48). Power Supplies: 7803283 - Changed 5V S3 regulator output from 5.02V to 5.12V nominal (pg. 72). 7809760 - Stuffed C9799 and clarified tables/BOMOPTIONS around these parts (pg. 97).</div></div> <div>Proto 1 (ECO #0000884508, v2.0.0, P4 change #212783, 03/31/2010)</div> <div><div>v2.1.0 (P4 change #??????, ??/??/2010)</div><div>BOM: 7796658 - Changed OMITs to OMIT_TABLES (pp. 10-11, 14-20, 26, 31-36, 49, 61).</div></div>								D
C									C
B									B
A									A
	8	7	6	5	4	3	2	1	


NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

SYNC MASTER=N/A

SYNC DATE=N/A

PAGE TITLE

Revision History

 Apple Inc.

051-8467

D

REVISION

3.3.0

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BRANCH


PAGE

SHEET

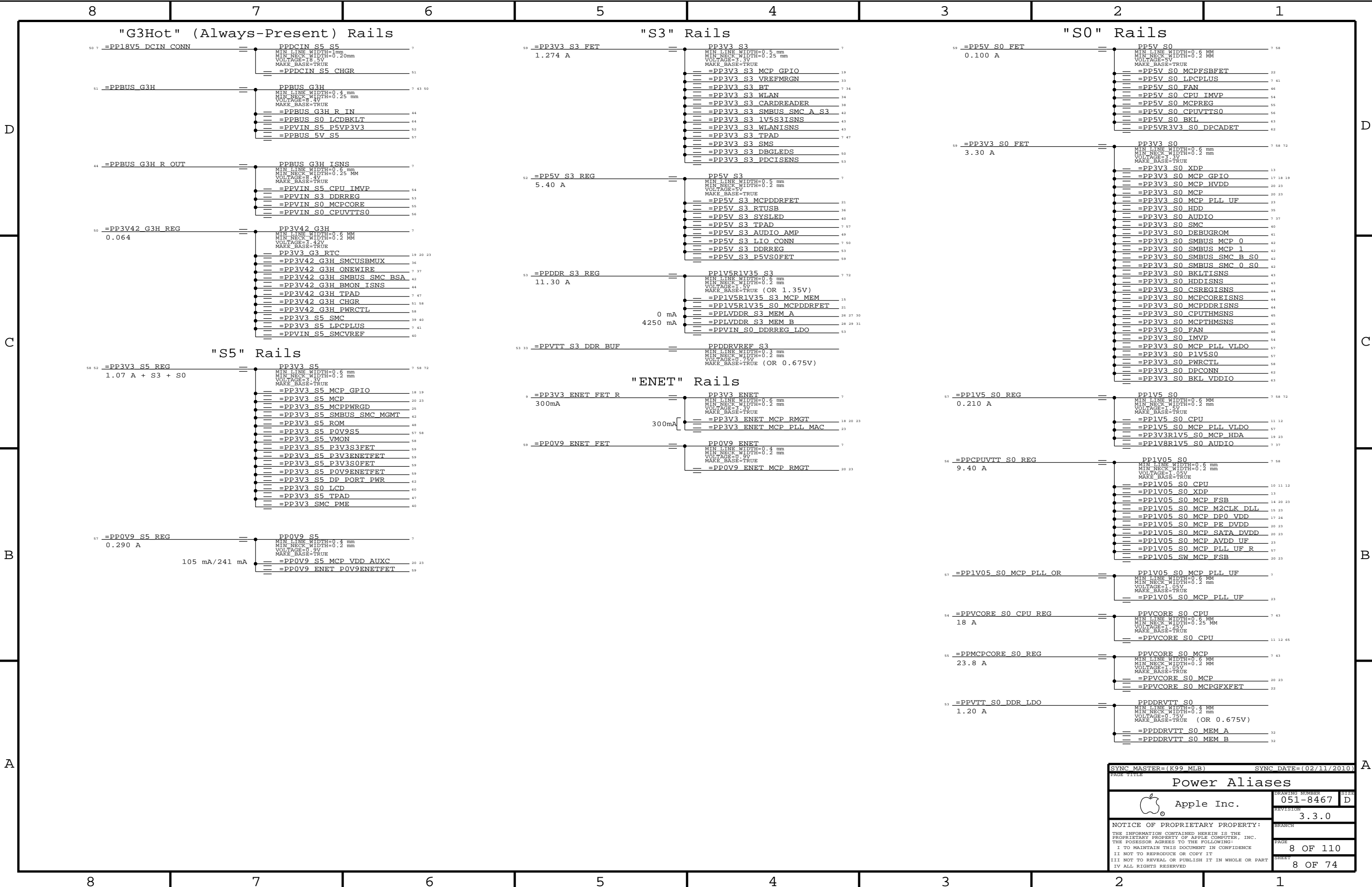
6 OF 110

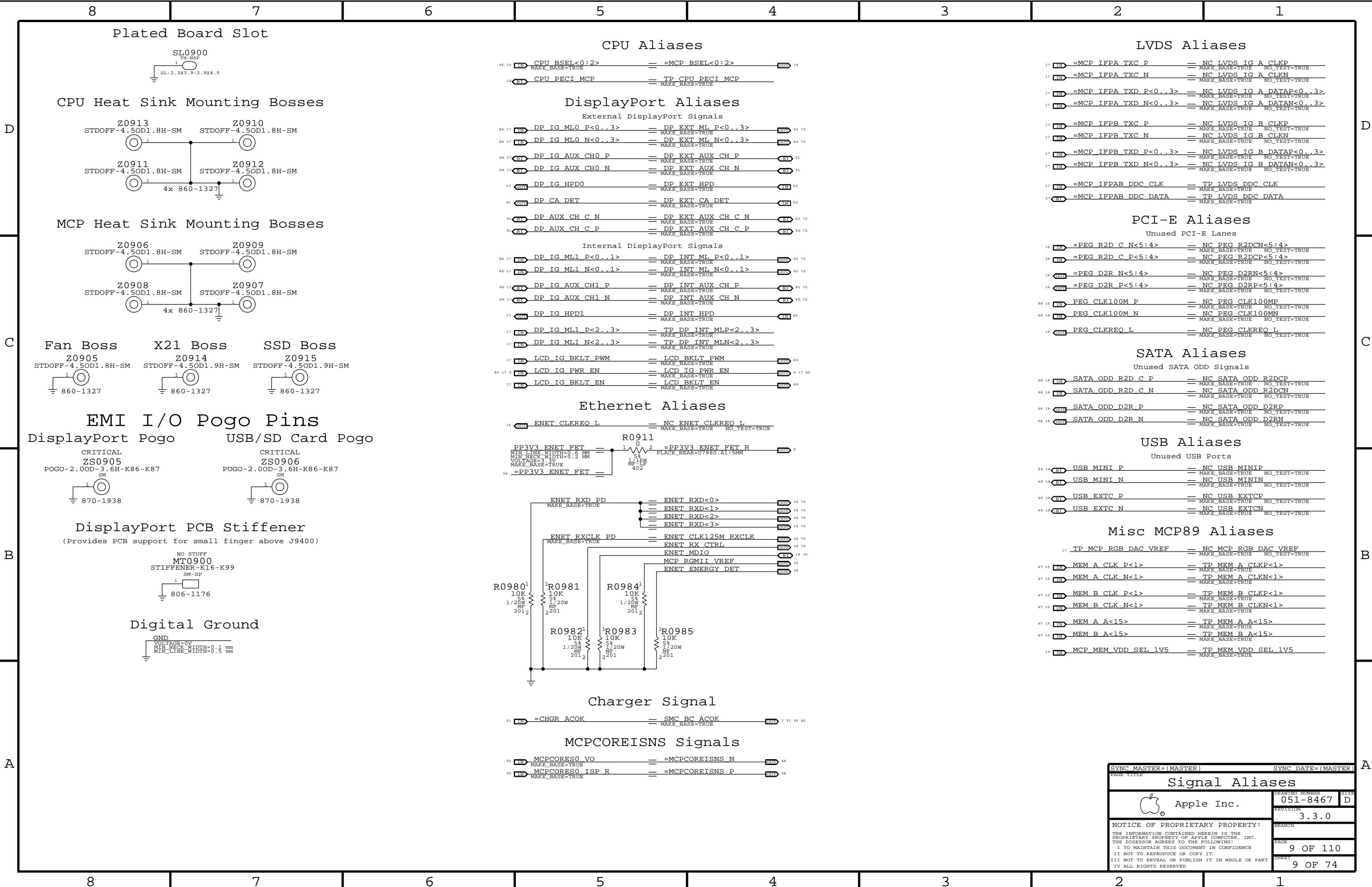
6 OF 74

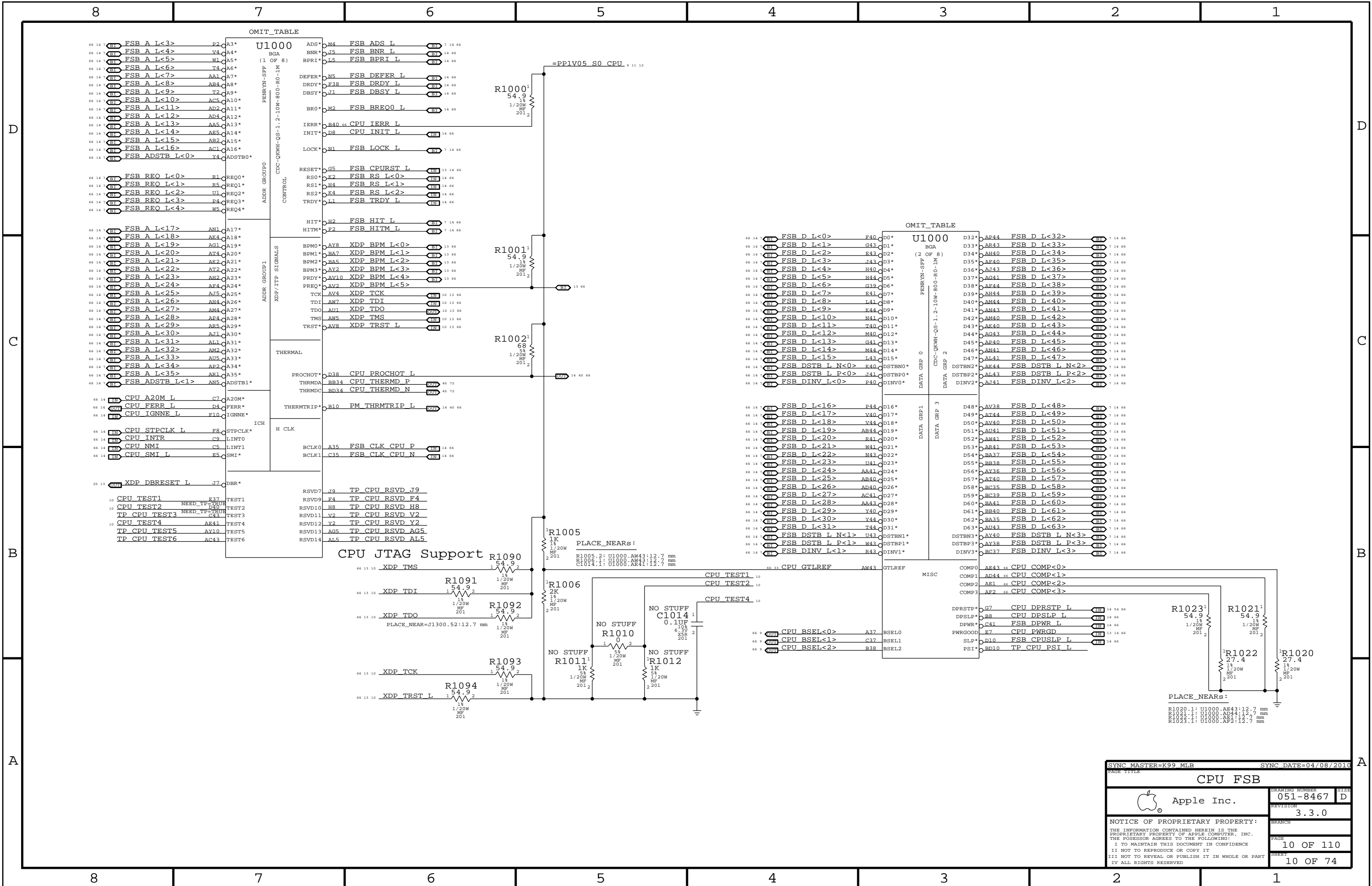
NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

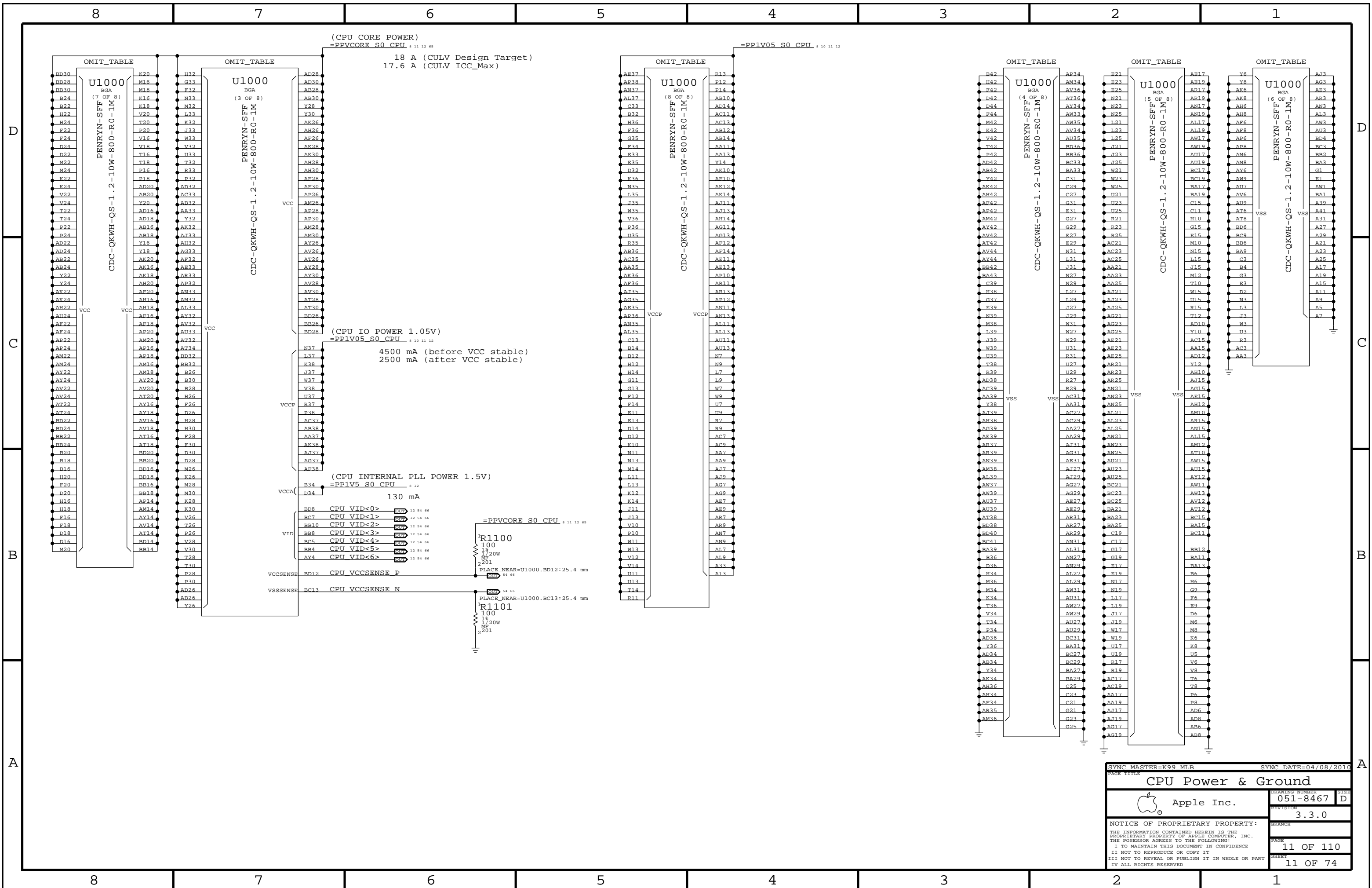
SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
Revision History			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	6 OF 110
		SHEET	6 OF 74

8	7	6	5	4	3	2	1
Functional Test Points				NO_TEST Nets			
J4001: AirPort / BT Connector				FSB Signals (Covered via CPU/MCP JTAG)			
FUNC_TEST				NO_TEST			
TRUE PP3V3 WLAN_F 7 34 40 (Need 5 TPs)				TRUE FSB A L<35..3> 10 14 66			
TRUE WIFI_EVENT_L 34 39 40				TRUE FSB ADS_L 10 14 66			
TRUE PCIE AP R2D_N 34 68				TRUE FSB ADSTB_L<1..0> 10 14 66			
TRUE PCIE AP R2D_P 34 68				TRUE FSB D L<63..0> 10 14 66			
TRUE PCIE CLK100M AP_N 16 34 68				TRUE FSB DINV_L<3..0> 10 14 66			
TRUE PCIE CLK100M AP_P 16 34 68				TRUE FSB DSTB_L N<3..0> 10 14 66			
TRUE USB_BT_P 18 34 69				TRUE FSB DSTB_L P<3..0> 10 14 66			
TRUE USB_BT_N 18 34 69				TRUE FSB HIT_L 10 14 66			
TRUE PCIE AP D2R_P 16 34 68				TRUE FSB HITM_L 10 14 66			
TRUE PCIE AP D2R_N 16 34 68				TRUE FSB LOCK_L 10 14 66			
TRUE PCIE_WAKE_L 16 34				TRUE FSB REQ_L<4..0> 10 14 66			
TRUE AP_RESET_CONN_L 34							
TRUE AP_CLKREQ_O_L 34							
TRUE PP3V3_S3_BT 8 34							
(Need to add 6 GND TPs)							
J4501: SATA SSD Connector							
FUNC_TEST							
TRUE PP3V3_S0_HDD_R 7 35 (Need 5 TPs)							
TRUE SATA_HDD_D2R_C_P 35 68							
TRUE SATA_HDD_D2R_C_N 35 68							
TRUE SATA_HDD_R2D_N 35 68							
TRUE SATA_HDD_R2D_P 35 68							
TRUE SMC_HDD_QOB_TEMP 35 39							
TRUE SMC_HDD_TEMP_CTL 35 39							
(Need to add 6 GND TPs)							
J4700: LIO Connector							
FUNC_TEST							
TRUE PP3V42_G3H_ONEWIRE 8 37 (Need 2 TPs)							
TRUE PP3V3_S0_AUDIO 8 37							
TRUE PP1V8R1V5_S0_AUDIO 8 37							
TRUE SYS_ONEWIRE 37 39							
TRUE SMC_BC_ACOK 9 37 39 40							
TRUE USB_PWR_EN 36 37 58							
TRUE SMC_LID 7 37 39 40 47							
TRUE I2C_LIO_SDA 37 42							
TRUE I2C_LIO_SCL 37 42							
TRUE I2C_MIKEY_SCL 37 42							
TRUE I2C_MIKEY_SDA 37 42							
TRUE AUD_IPHS_SWITCH_EN 19 37							
TRUE AUD_IP_PERIPHERAL_DET 17 37							
TRUE AUD_I2C_INT_L 19 37							
TRUE AUD_GPIO_3 37 49							
TRUE SPKRAMP_INR_N 37 49 72							
TRUE SPKRAMP_INR_P 37 49 72							
TRUE USB_EXTD_N 18 37 69							
TRUE USB_EXTD_P 18 37 69							
TRUE USB_CAMERA_N 18 37 69							
TRUE USB_CAMERA_P 18 37 69							
TRUE HDA_SDOUT 19 37 69							
TRUE HDA_BIT_CLK 19 37 69							
TRUE HDA_SDIN0 19 37 69							
TRUE USB_EXTD_OC_L 18 37							
TRUE HDA_RST_L 19 37 69							
TRUE HDA_SYNC 19 37 69							
(Need to add 5 GND TPs)							
J4800: SD Card Connector							
FUNC_TEST							
TRUE PP3V3_SW_SD_PWR 38							
TRUE SD_CLK 38 70							
TRUE SD_CMD 38 70							
TRUE SD_D<7..0> 38 70							
TRUE SD_CD_L 38							
TRUE SD_WP 38							
(Need to add 2 GND TPs)							
J5100: LPC+SPI Connector							
FUNC_TEST							
TRUE PP3V3_S5_LPCPLUS 8 41							
TRUE PP5V_S0_LPCPLUS 8 41							
TRUE LPC_AD<3..0> 19 39 41 69							
TRUE SPI_ALT_MOSI 41 69							
TRUE SPI_ALT_MISO 41 69							
TRUE LPC_FRAME_L 19 39 41 69							
TRUE PM_CLKRUN_L 19 39 41							
TRUE SMC_TMS 39 40 41							
TRUE LPCPLUS_RESET_L 25 41							
TRUE SMC_TDO 39 40 41							
TRUE SMC_TRST_L 39 41							
TRUE SMC_MD1 39 41							
TRUE SMC_TX_L 36 39 40 41							
TRUE LPC_CLK33M_LPCPLUS 25 41 69							
TRUE SPIROM_USE_MLB 19 41 48							
TRUE SPI_ALT_CLK 41 69							
TRUE SPI_ALT_CS_L 41 69							
TRUE LPC_SERIRQ 19 39 41							
TRUE LPC_PWRDWN_L 19 39 41							
TRUE SMC_TDI 39 40 41							
TRUE SMC_TCK 39 40 41							
TRUE SMC_RESET_L 39 40 41 51							
TRUE SMC_NMI 39 41							
TRUE SMC_RX_L 36 39 40 41							
TRUE LPCPLUS_GPIO 19 41							
(Need to add 6 GND TPs)							
J5600: Fan Connector							
FUNC_TEST							
TRUE PP5V_S0 7 8 58							
TRUE FAN_RT_TACH 46							
TRUE FAN_RT_PWM 46							
(Need to add 1 GND TP)							
J5700: IPD Flex Connector							
FUNC_TEST							
TRUE PP5V_S3_TPAD 8 57							
TRUE PP3V42_G3H_TPAD 8 47							
TRUE PP3V3_S3_TPAD 8 47							
TRUE USB_TPAD_CONN_P 47 72							
TRUE USB_TPAD_CONN_N 47 72							
TRUE I2C_TPAD_SDA 42 47							
TRUE I2C_TPAD_SCL 42 47							
TRUE SMC_ONOFF_L 39 40 47							
TRUE SMC_LID 7 37 39 40 47							
TRUE SMC_TPAD_RST_L 40 47							
(Need to add 5 GND TPs)							
J6900: DC-In Connector							
FUNC_TEST							
TRUE PP18V5_DCIN_CONN 8 50 (Need 6 TPs)							
TRUE PP5V_S3_LIO_CONN 8 50							
(Need to add 6 GND TPs)							
J6903: Speaker Connector							
FUNC_TEST							
TRUE SPKRAMP_R_P_OUT 49 50							
TRUE SPKRAMP_R_N_OUT 49 50							
J6950: Battery Connector							
FUNC_TEST							
TRUE PPVBAT_G3H_CONN 50 51 (Need 4 TPs)							
TRUE SMBUS_SMC_BSA_SCL 42 71							
TRUE SMBUS_SMC_BSA_SDA 42 71							
TRUE SYS_DETECT_L 50							
(Need to add 4 GND TPs near J6950 and 1 for shield)							
J9000: Internal DP Connector							
FUNC_TEST							
TRUE PPVOUT_SW_LCDCLKLT 7 43 60 63 (Need 2 TPs)							
TRUE PP3V3_SW_LCD 60 (Need 2 TPs)							
TRUE I2C_TCON_SDA 42 60							
TRUE LED_RETURN_6 50 63							
TRUE LED_RETURN_5 50 63							
TRUE LED_RETURN_4 50 63							
TRUE LED_RETURN_3 50 63							
TRUE LED_RETURN_2 50 63							
TRUE LED_RETURN_1 50 63							
TRUE DP_INT_HPD_CONN 60							
TRUE DP_INT_AUX_CH_C_N 60 72							
TRUE DP_INT_AUX_CH_C_P 60 72							
TRUE DP_INT_ML_F_P<0> 60 72							
TRUE DP_INT_ML_F_N<0> 60 72							
TRUE DP_INT_ML_F_P<1> 60 72							
TRUE DP_INT_ML_F_N<1> 60 72							
TRUE I2C_TCON_SCL 42 60							
(Need to add 5 GND TPs)							
Misc Voltages & Control Signals							
FUNC_TEST							
TRUE PPVOUT_SW_LCDCLKLT 7 43 60 63							
TRUE PPDCIN_S5_S5 8							
TRUE PPBUS_G3H 8 43 50							
TRUE PPBUS_G3H_ISNS 8							
TRUE PP5V_S3 8							
TRUE PP5V_S3_RTUSB_A_F 36							
TRUE PP5V_S0 7 8 58							
TRUE PP3V42_G3H 8							
TRUE PP3V3_S5 8 58 72							
TRUE PP3V3_SW_DPPWR 62							
TRUE PP3V3_S3 8							
TRUE PP3V3_WLAN_F 7 34 40							
TRUE PP3V3_S0 8 58 72							
TRUE PP3V3_S0_HDD_R 7 35							
TRUE PP3V3_ENET 8							
TRUE PP1V5R1V35_S3 8 72							
TRUE PP1V5_S0 8 58 72							
TRUE PP1V05_S0 8 58							
TRUE PP1V05_S0_MCP_PLL_UF 8							
TRUE PP0V9_S5 8							
TRUE PP0V9_ENET 8							
TRUE PPVCORE_S0_CPU 8 43							
TRUE PPVCORE_S0_MCP 8 43							
(Need to add 27 GND TPs)							
TRUE SMC_PM_G2_EN 39 58							
TRUE PM_SLP_S4_L 19 39 58							
TRUE PM_SLP_S3_L 19 39 40 58							









4x 270uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

[illegible][illegible][illegible]

Part	Value	Part	Value
CRITICAL	CRITICAL	CRITICAL	CRITICAL
OMIT TABLE	NO STUFF	OMIT TABLE	NO STUFF
1 C1230	1 C1231	1 C1230	1 C1231
10UF	10UF	10UF	10UF
20%	20%	20%	20%
6.3V	6.3V	6.3V	6.3V
X5R	X5R	X5R	X5R
603	603	603	603

[illegible][illegible]

CRITICAL OMIT TABLE 1 C1260 2 2.2UF 208 3.3V 2 CERM 402-LF	CRITICAL OMIT TABLE 1 C1261 2 2.2UF 208 3.3V 2 CERM 402-LF	CRITICAL OMIT TABLE 1 C1262 2 2.2UF 208 3.3V 2 CERM 402-LF	CRITICAL OMIT TABLE 1 C1263 2 2.2UF 208 3.3V 2 CERM 402-LF	CRITICAL OMIT TABLE 1 C1264 2 2.2UF 208 3.3V 2 CERM 402-LF	CRITICAL OMIT TABLE 1 C1265 2 2.2UF 208 3.3V 2 CERM 402-LF	CRITICAL OMIT TABLE 1 C1266 2 2.2UF 208 3.3V 2 CERM 402-LF	CRITICAL OMIT TABLE 1 C1267 2 2.2UF 208 3.3V 2 CERM 402-LF
--	--	--	--	--	--	--	--

Four critical capacitor locations are identified on the PCB:

- C1270**: 270uF 20V TANT CASE-B4-SM
- C1271**: 270uF 20V TANT CASE-B4-SM
- C1272**: 270uF 20V TANT CASE-B4-SM
- C1273**: 270uF 20V TANT CASE-B4-SM

```
66 54 11 IN CPU VID<0..6> == IMVP6 VID<0..6> OUT 66
      MAKE_BASE=TRUE
```

11 8 =PP1V5_S0_CPU 1x 10uF, 1x 0.01uF

OMIT_TABLE

C1280 10uF

6.3V X5R 603

C1281 0.01uF

10V X5R 201

LAYOUT NOTE:

PLACE C1281 NEAR PIN B34 OF U1000

11 10 8 =PP1V05 S0 CPU 1x 270uF, 12x 2.2uF

CRITICAL C1290 270uF

CASE-B4-SM

LAYOUT NOTE:
 PLACE C1290 CLOSE TO CPU
 PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
 PLACE C1291-C1296 CLOSE TO FSB DATA PINS

D

C

B

A

D

C

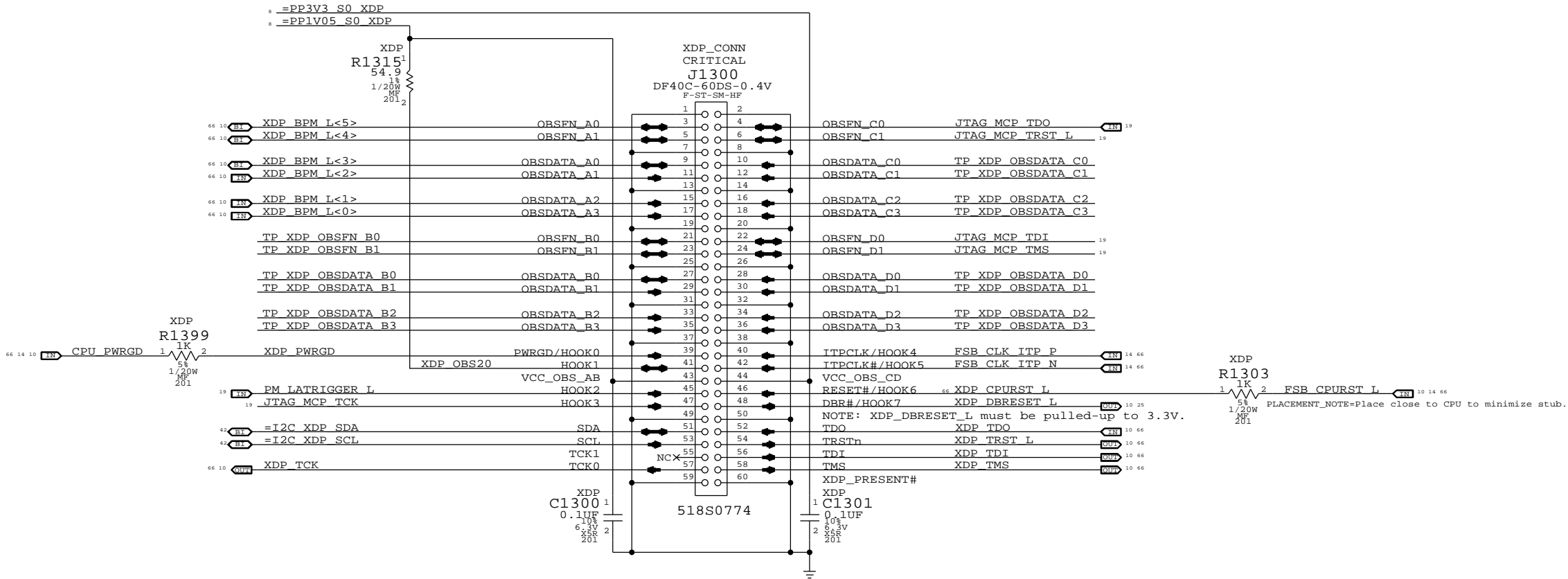
B

A

Micro2-XDP Connector


NOTE: This is not the standard XDP pinout.

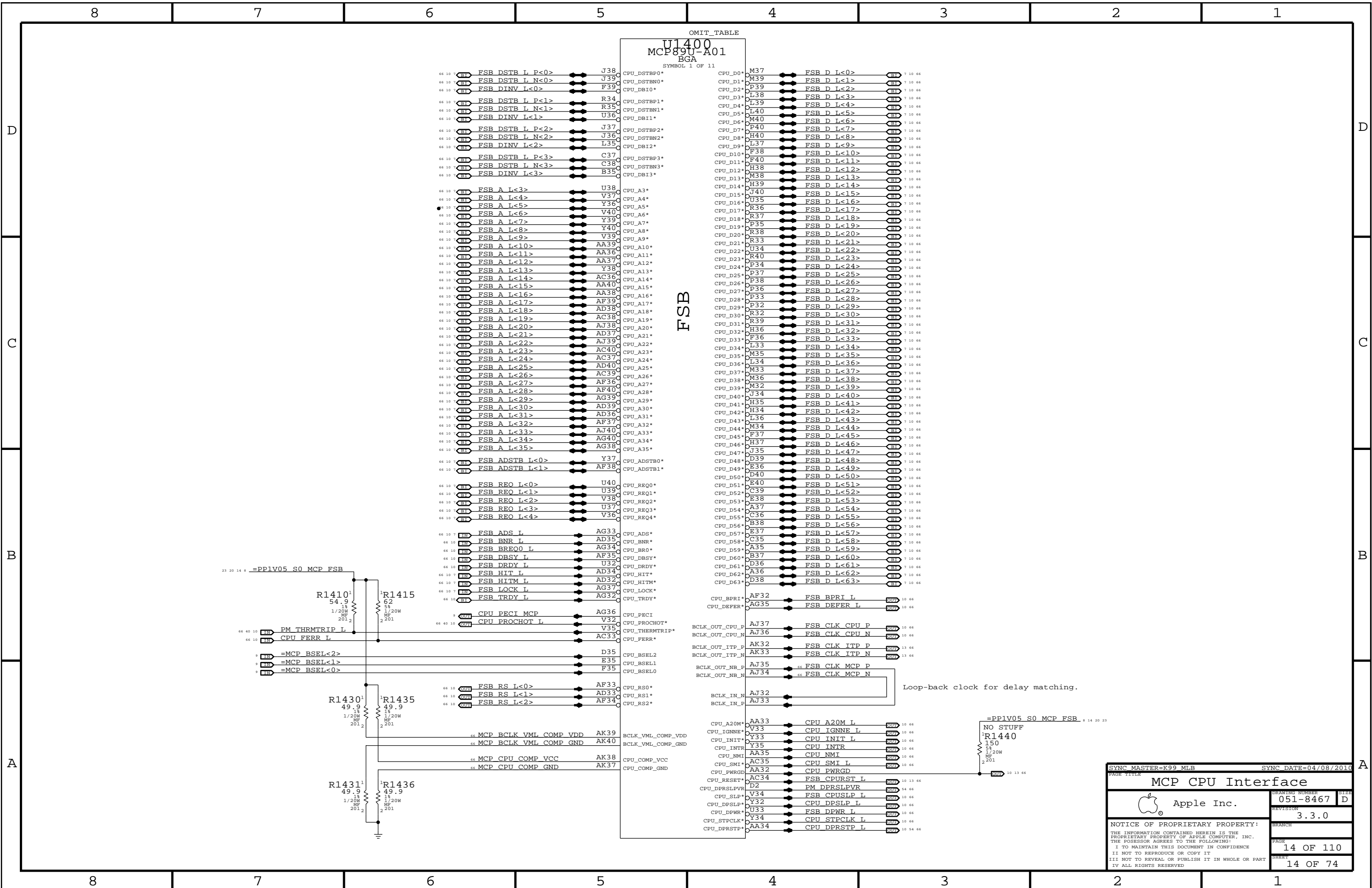
Use with 920-0782 Adapter Flex to support chipset debug.



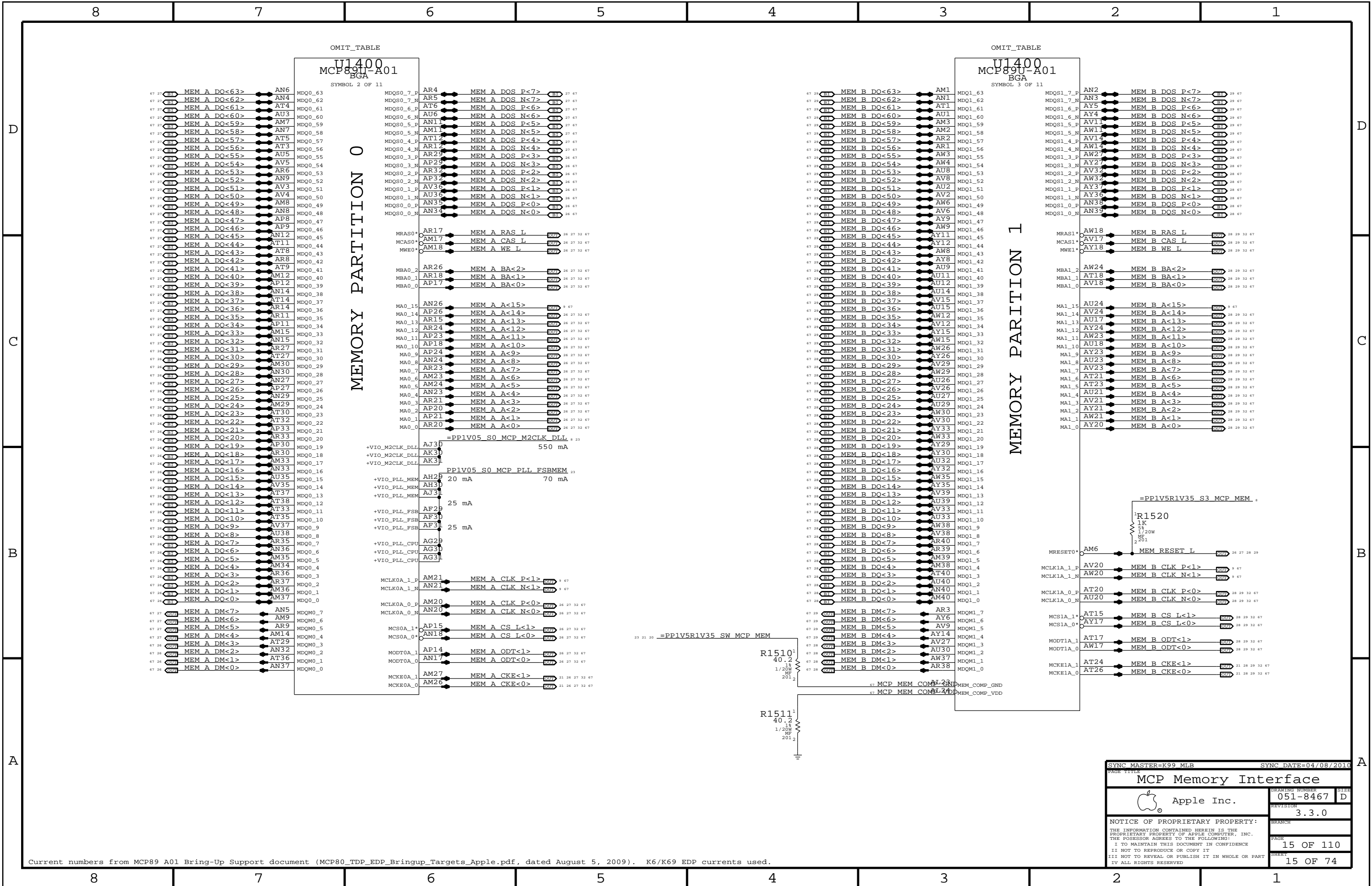
Direction of XDP adapter flex

Please place J1300 within 1" of board edge with odd-numbered pins facing edge. Avoid any tall components between J1300 and edge.

SYNC MASTER=K99 MLB		SYNC DATE=03/01/2010	
PAGE TITLE			
eXtended Debug Port		(Micro-XDP)	
	Apple Inc.	DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	13 OF 110
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	13 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE		MCP CPU Interface	
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	14 OF 110
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	14 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

MCP Memory Interface

Apple Inc.

DRAWING NUMBER051-8467

REVISION3.3.0

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

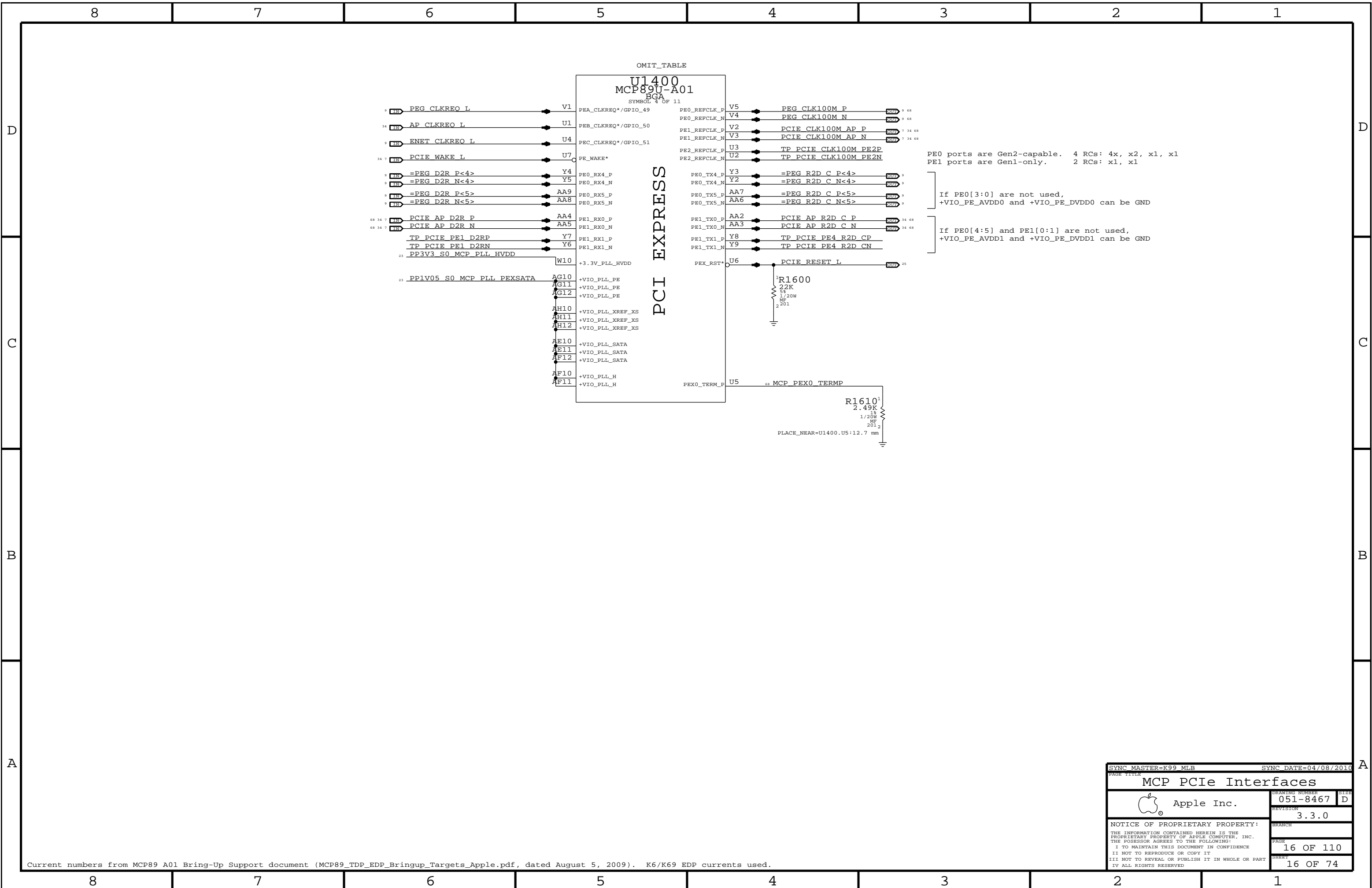
II NOT TO REPRODUCE OR COPY IT

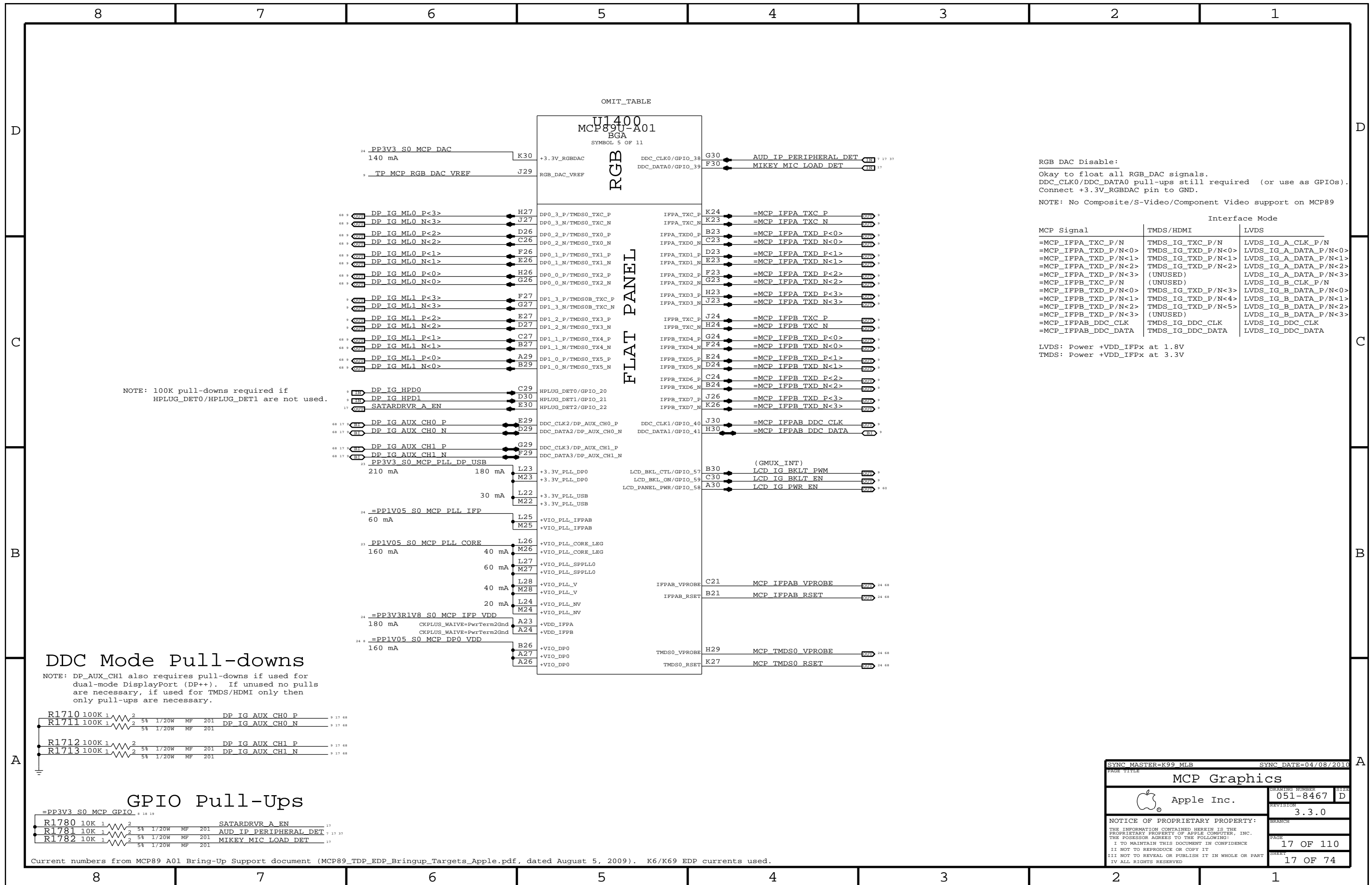
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

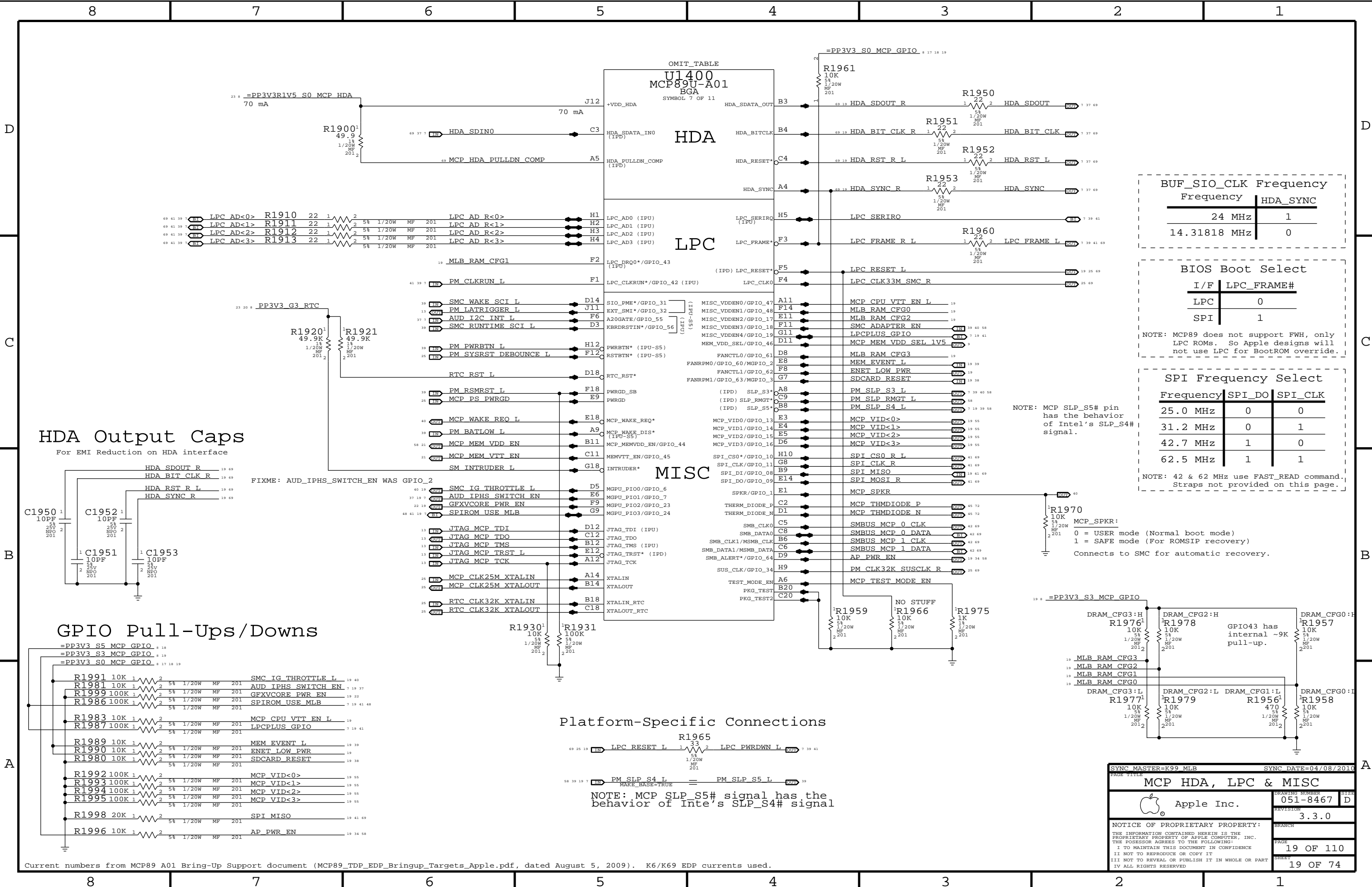
IV ALL RIGHTS RESERVED

PAGE15 OF 110

SHEET15 OF 74

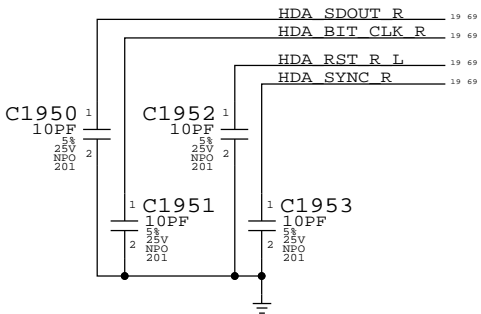




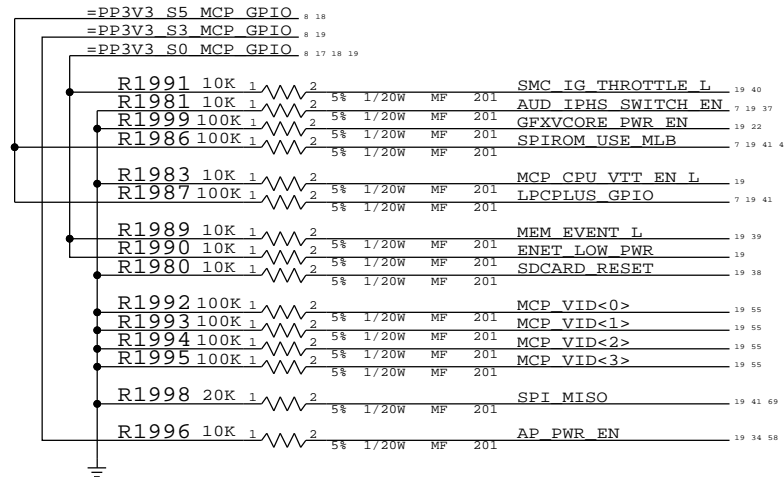


HDA Output Caps

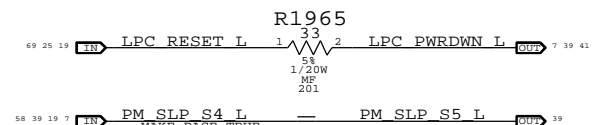
For EMI Reduction on HDA interface



GPIO Pull-Ups/Downs



Platform-Specific Connections



NOTE: MCP SLP_S5# signal has the behavior of Inte's SLP_S4# signal

BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select

I/F	LPC_FRAME#
LPC	0
SPI	1

NOTE: MCP89 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

SPI Frequency Select

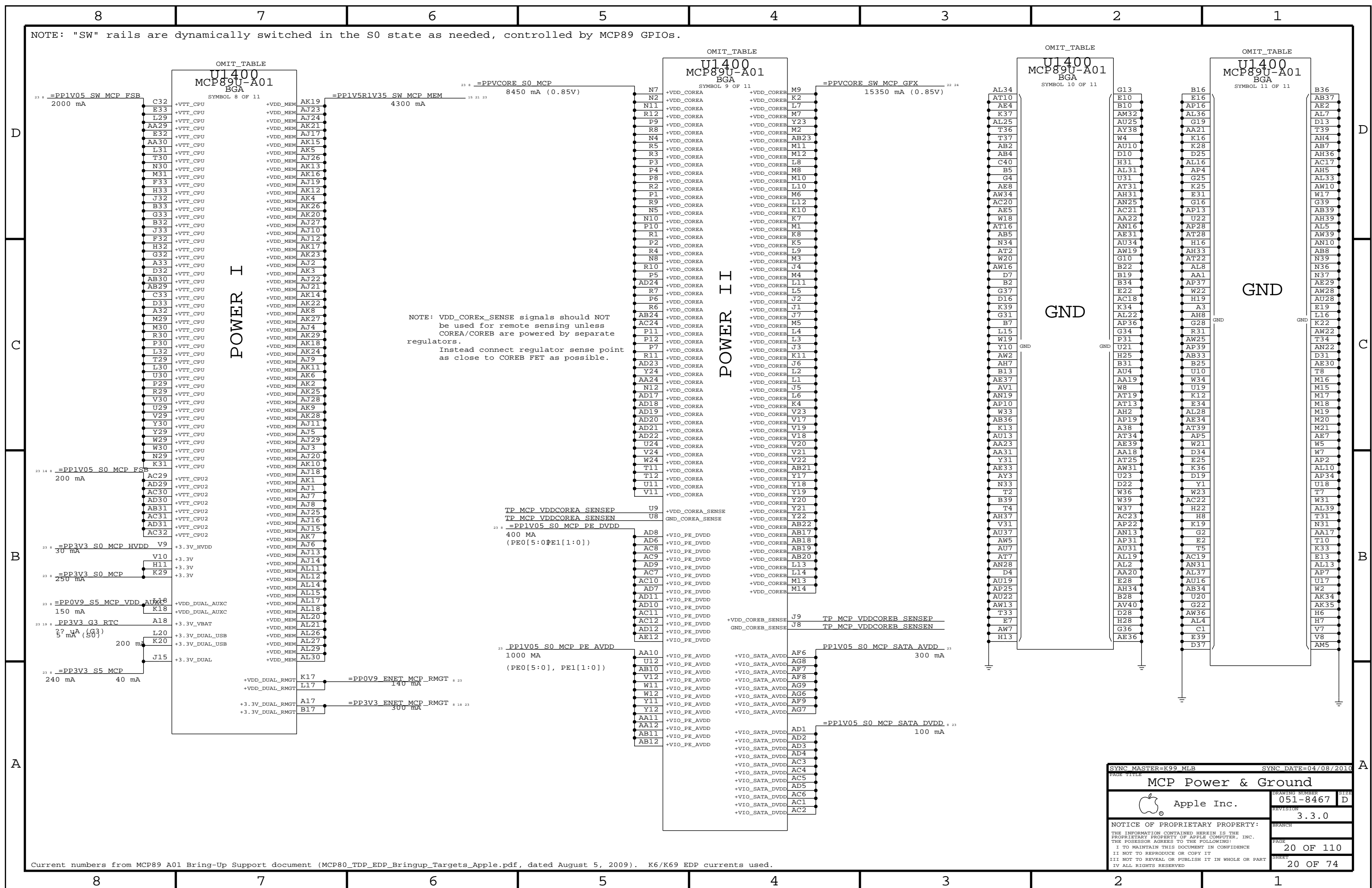
Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

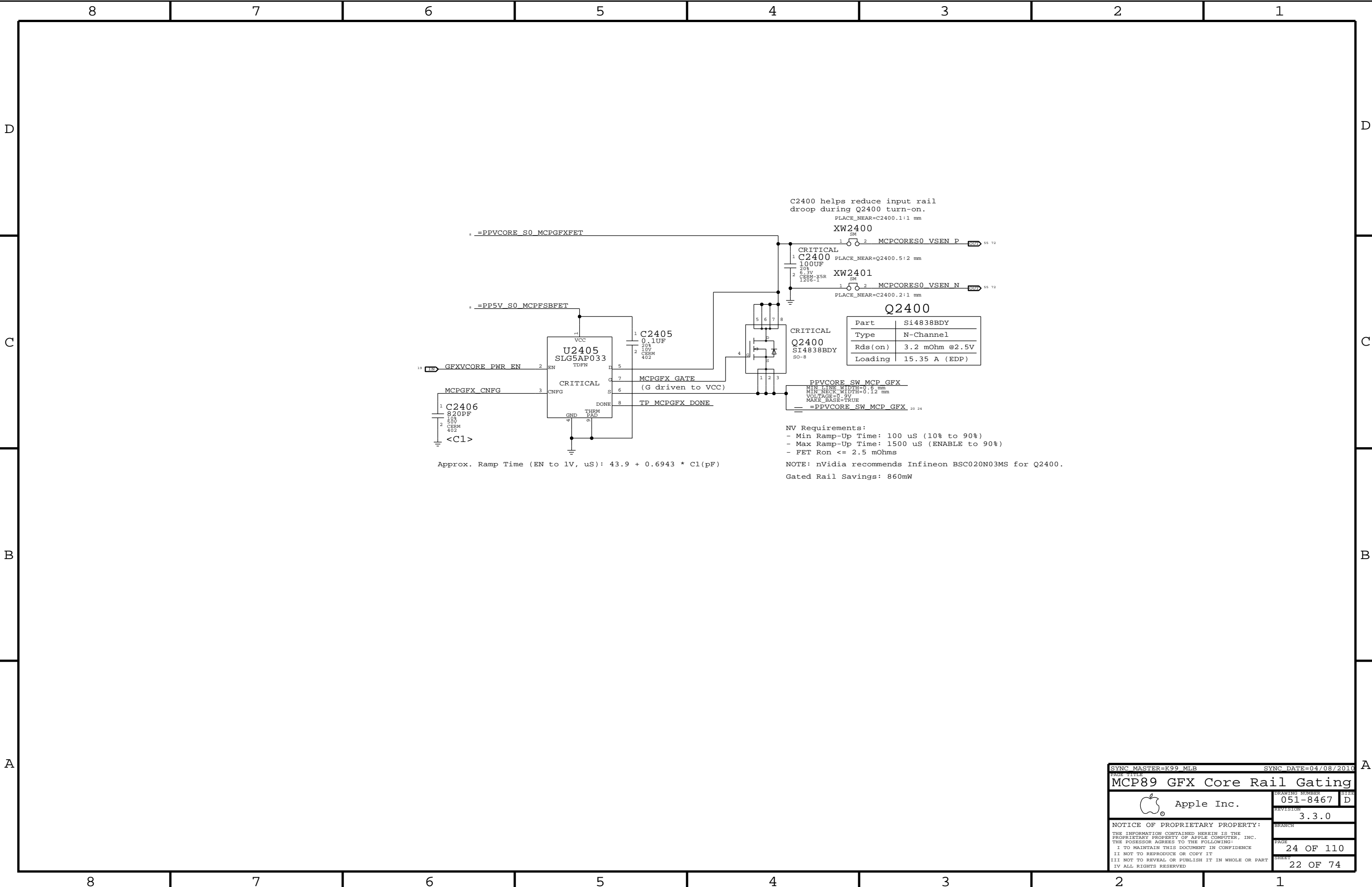
NOTE: 42 & 62 Mhz use FAST_READ command. Straps not provided on this page.

NOTE: MCP SLP_S5# pin has the behavior of Intel's SLP_S4# signal.

MCP_SPKR:
0 = USER mode (Normal boot mode)
1 = SAFE mode (For ROMSIP recovery)
Connects to SMC for automatic recovery.

PAGE TITLE		SYNC DATE=04/08/2010	
MCP HDA, LPC & MISC		DRAWING NUMBER	051-8467
Apple Inc.		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	19 OF 110
		SHEET	19 OF 74





C2400 helps reduce input rail droop during Q2400 turn-on.
PLACE_NEAR=C2400.1:1 mm

XW2400

CRITICAL
C2400
100UF
20%
6.3V
X5R
1206-1

PLACE_NEAR=Q2400.5:2 mm

XW2401

CRITICAL
Q2400
Si4838BDY
SO-8

Part	Si4838BDY
Type	N-Channel
Rds(on)	3.2 mOhm @2.5V
Loading	15.35 A (EDP)

PPVCORE SW MCP GFX
MIN LINE WIDTH=0.6 mm
MIN NECK WIDTH=0.12 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

NV Requirements:
- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.
Gated Rail Savings: 860mW

Approx. Ramp Time (EN to 1V, uS): $43.9 + 0.6943 * C1(pF)$

SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

MCP89 GFX Core Rail Gating

Apple Inc.

051-8467

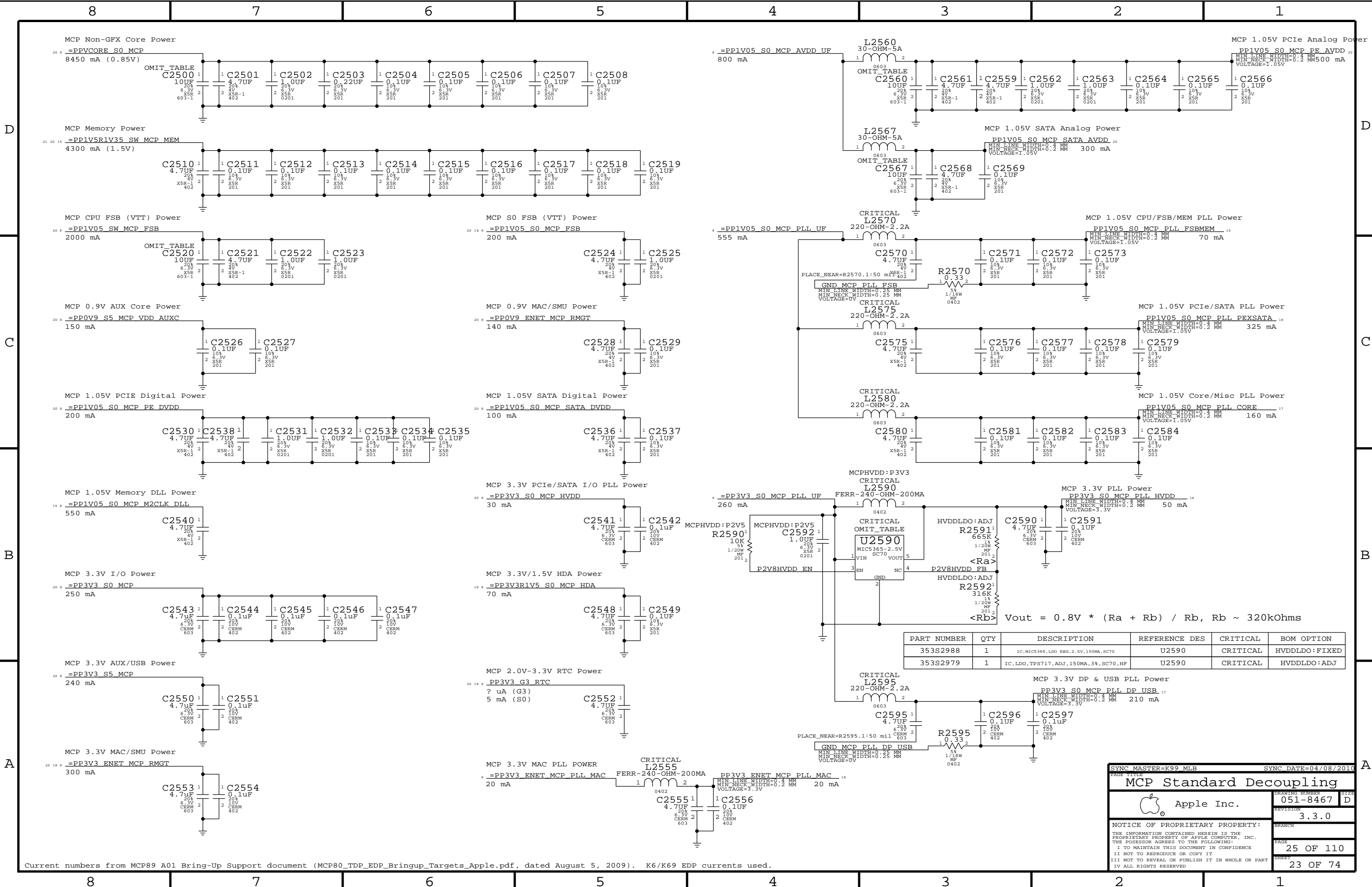
3.3.0

24 OF 110

22 OF 74

NOTICE OF PROPRIETARY PROPERTY:

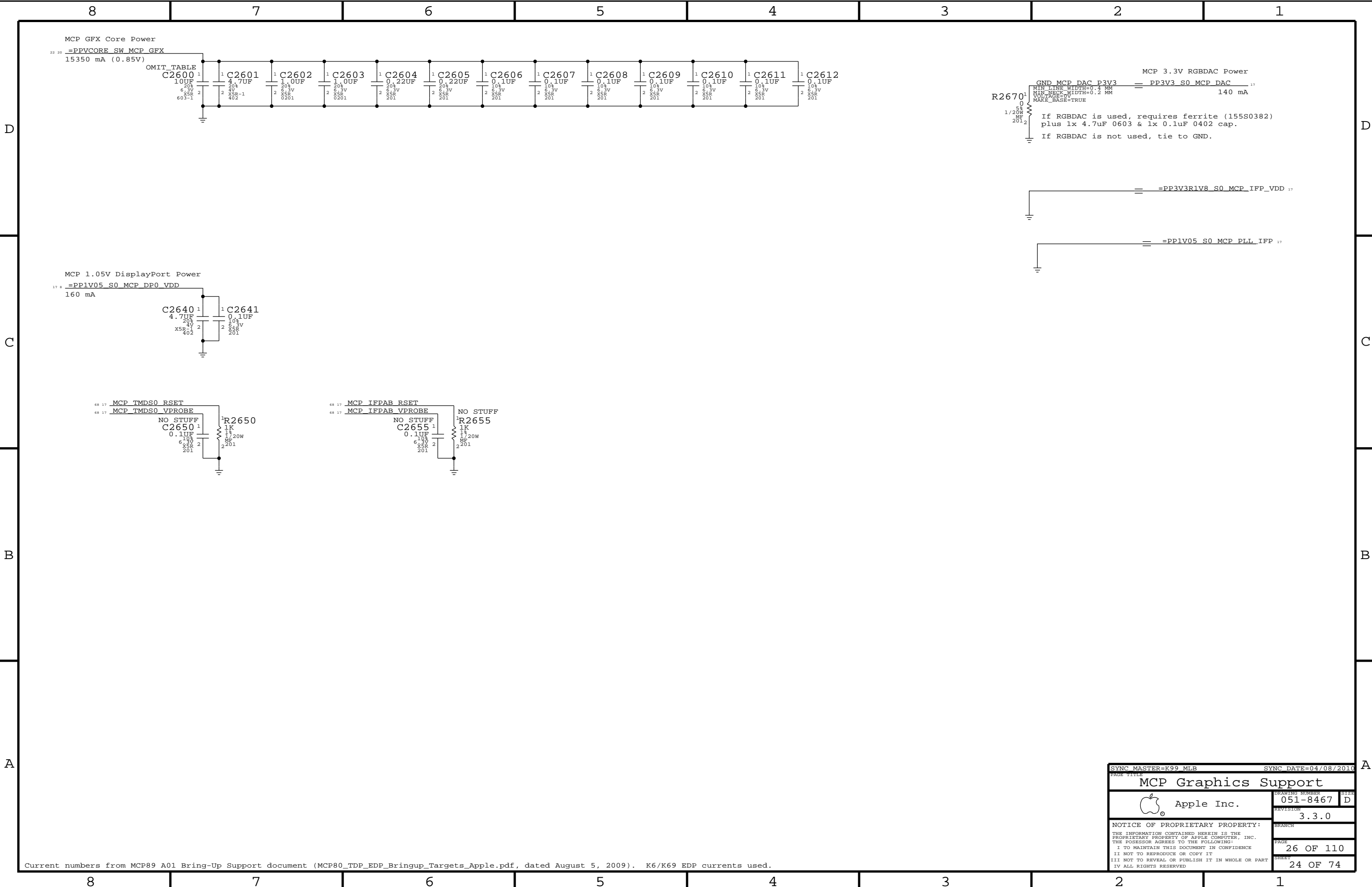
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED




Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

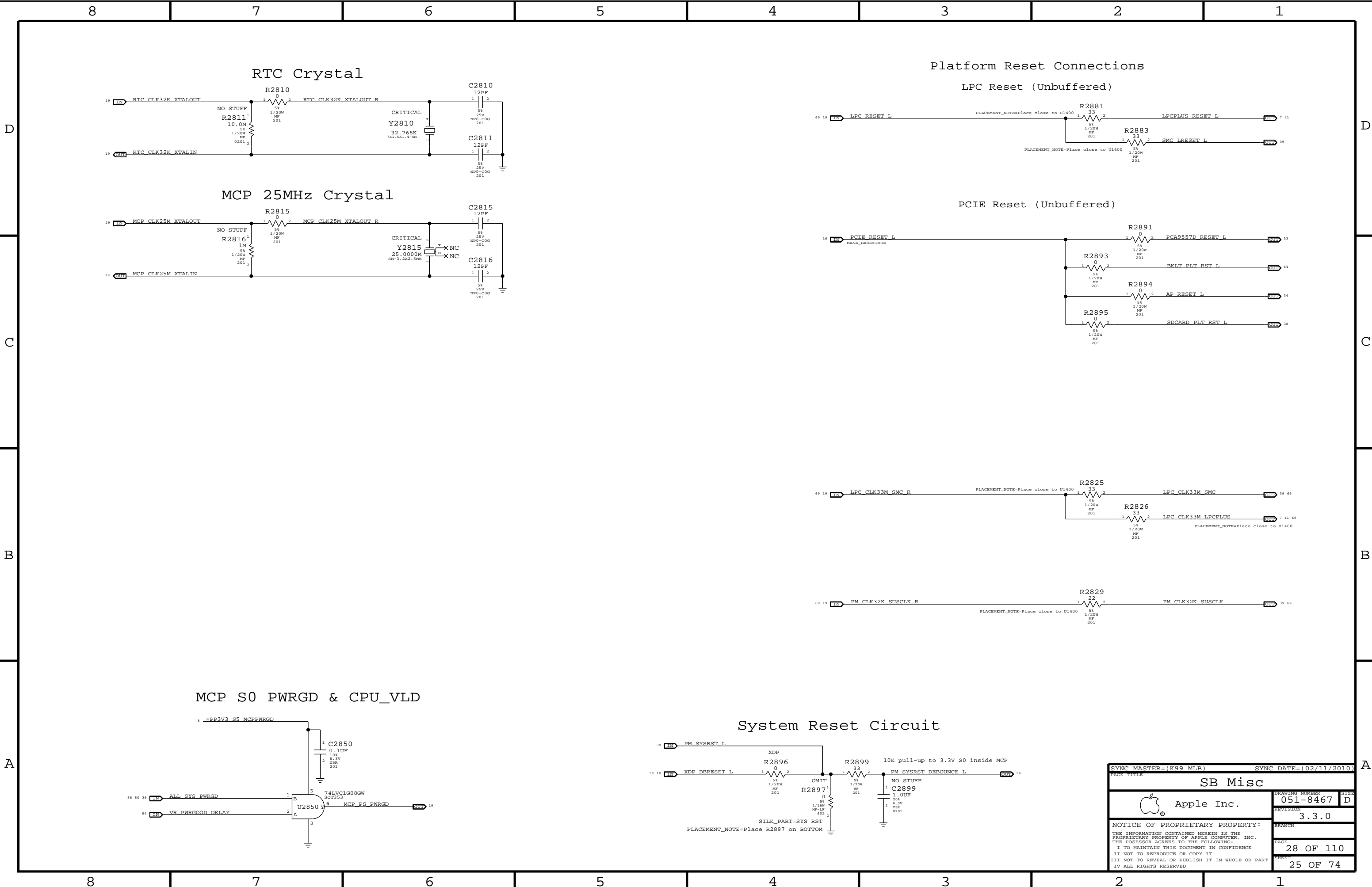
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2988	1	IC, MIC5366, LDO REG, 2.5V, 150mA, SC70	U2590	CRITICAL	HVDDLDO: FIXED
353S2979	1	IC, LDO, TPS717, ADJ, 150mA, 3%, SC70, HF	U2590	CRITICAL	HVDDLDO: ADJ

PAGE TITLE		SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
MCP Standard Decoupling		Apple Inc.		DRAWING NUMBER	
				051-8467	
				REVISION	
				3.3.0	
				BRANCH	
				PAGE	
				25 OF 110	
				SHEET	
				23 OF 74	

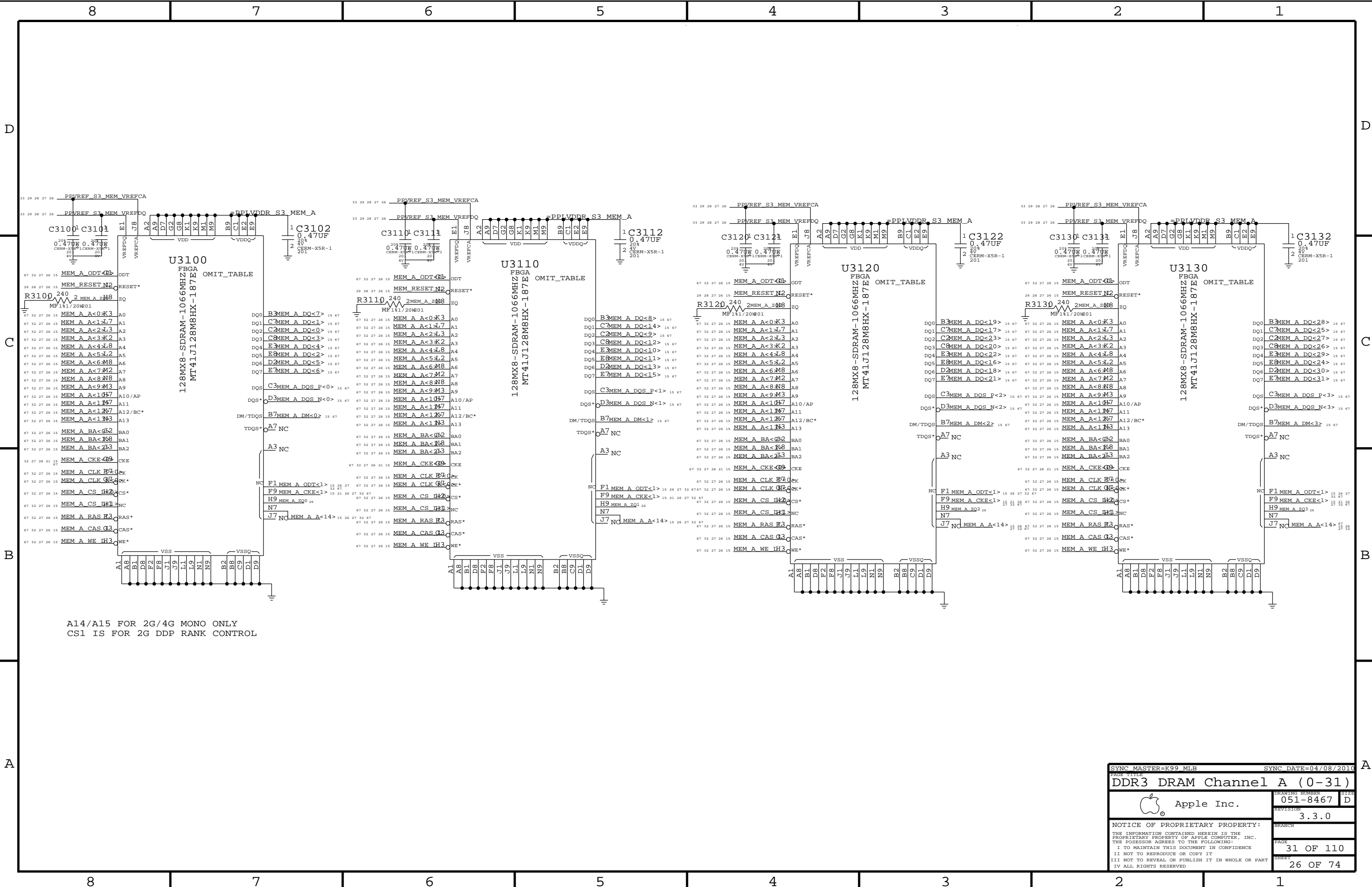


Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.


SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
MCP Graphics Support		DRAWING NUMBER	
 Apple Inc.		051-8467	D
		REVISION	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		3.3.0	
		BRANCH	
		PAGE	
		SHEET	
		26 OF 110	
		24 OF 74	

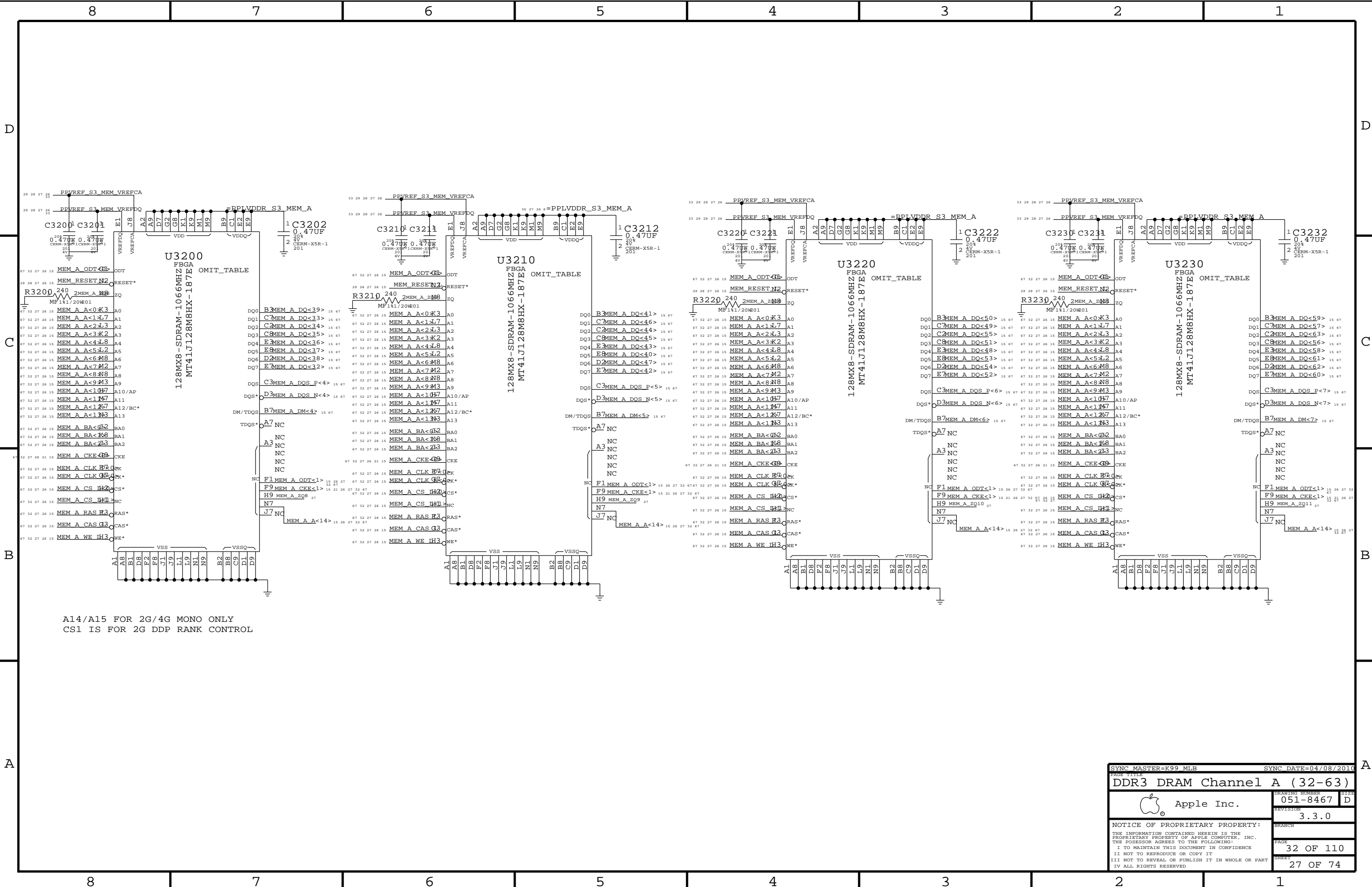


PAGE TITLE		SYNC MASTER=(K99 MLB)		SYNC DATE=(02/11/2010)	
SB Misc		DRAWING NUMBER		SIZE	
Apple Inc.		051-8467		D	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION		BRANCH	
		3.3.0			
		PAGE		SHEET	
		28 OF 110		25 OF 74	




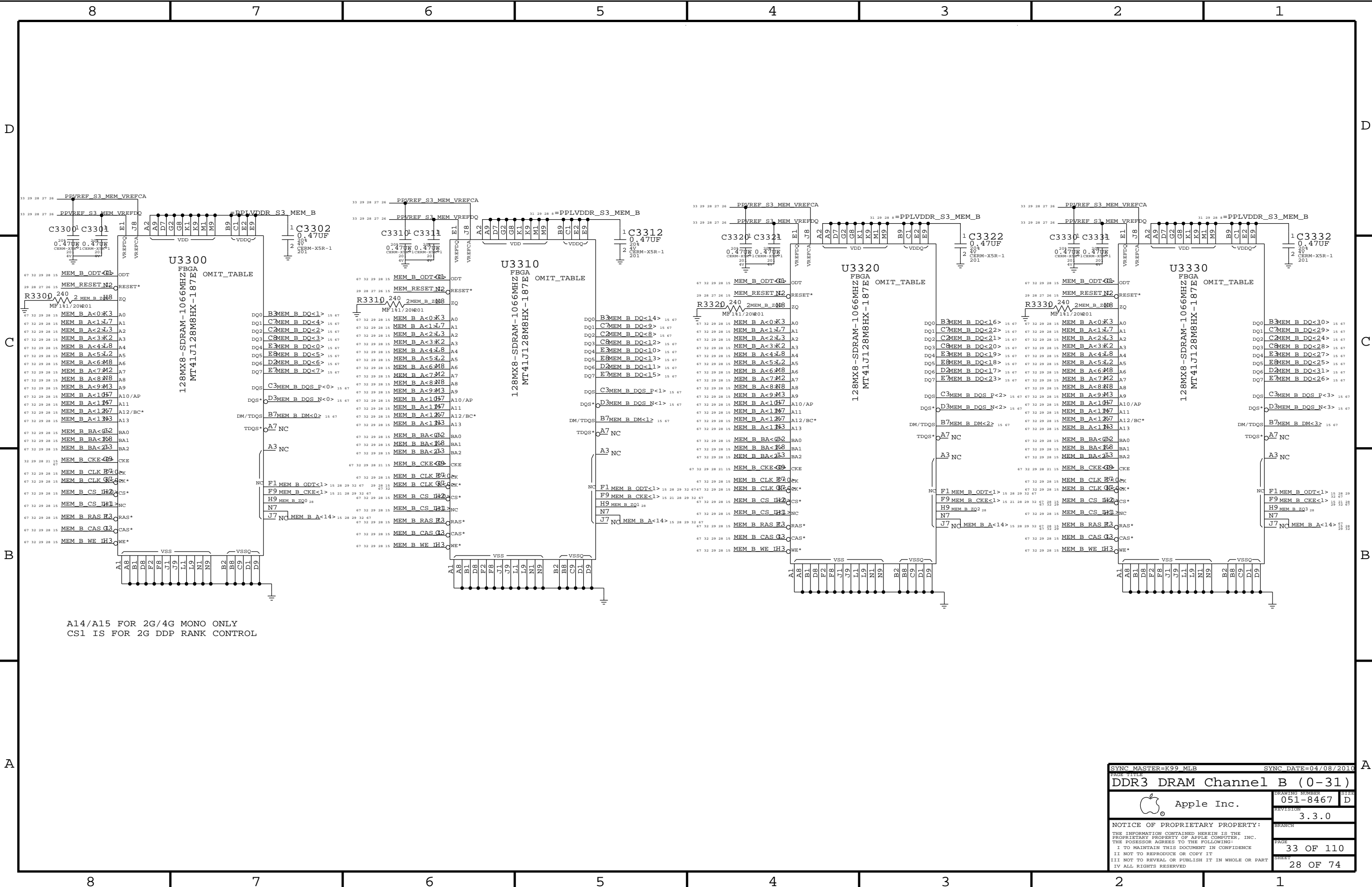
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
DDR3 DRAM Channel A		(0-31)	
	Apple Inc.	DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	31 OF 110
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	26 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			




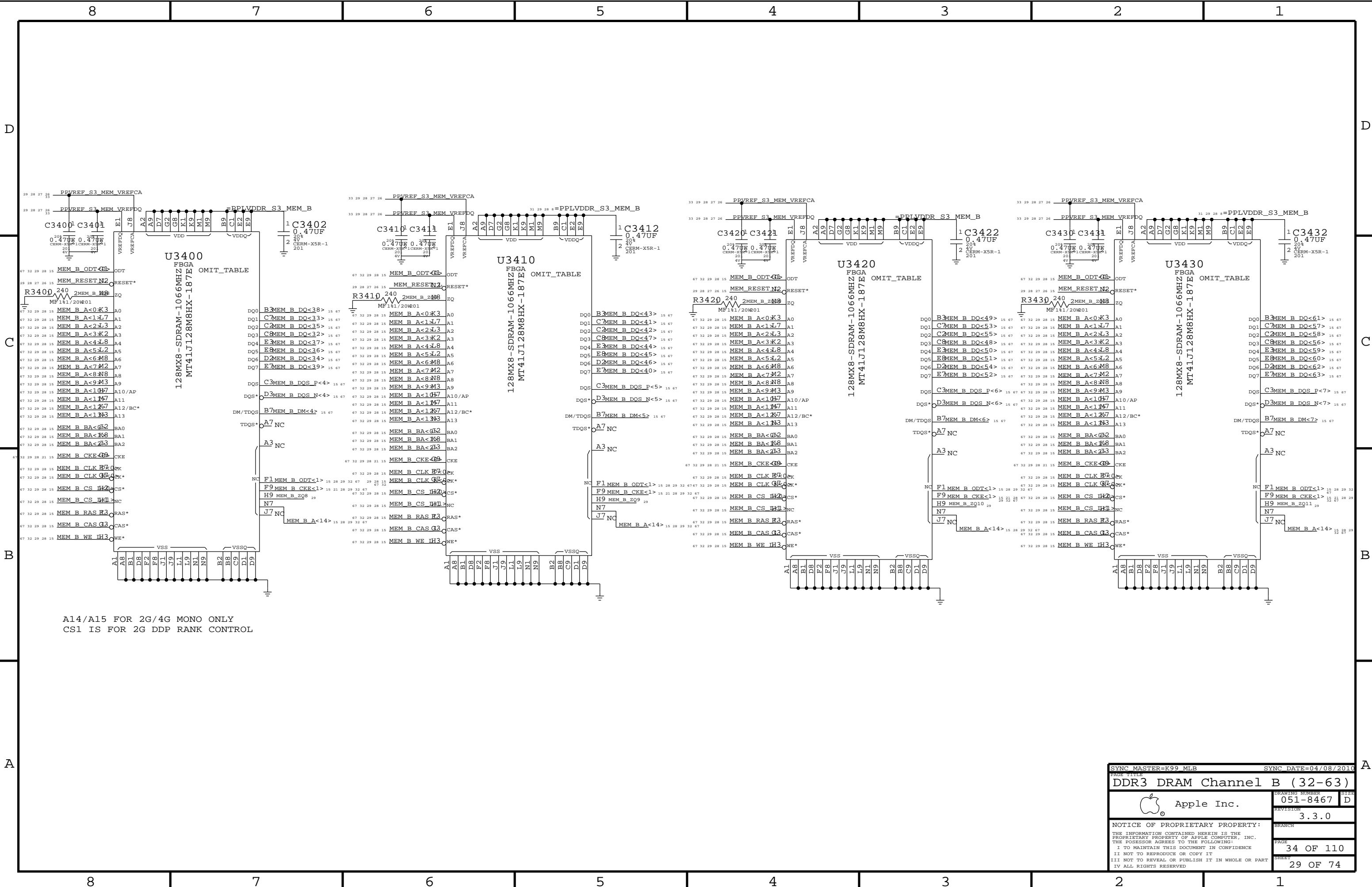
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
DDR3 DRAM Channel A		A (32-63)	
 Apple Inc.	DRAWING NUMBER		051-8467
	REVISION		3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		32 OF 110	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		27 OF 74	
IV ALL RIGHTS RESERVED			




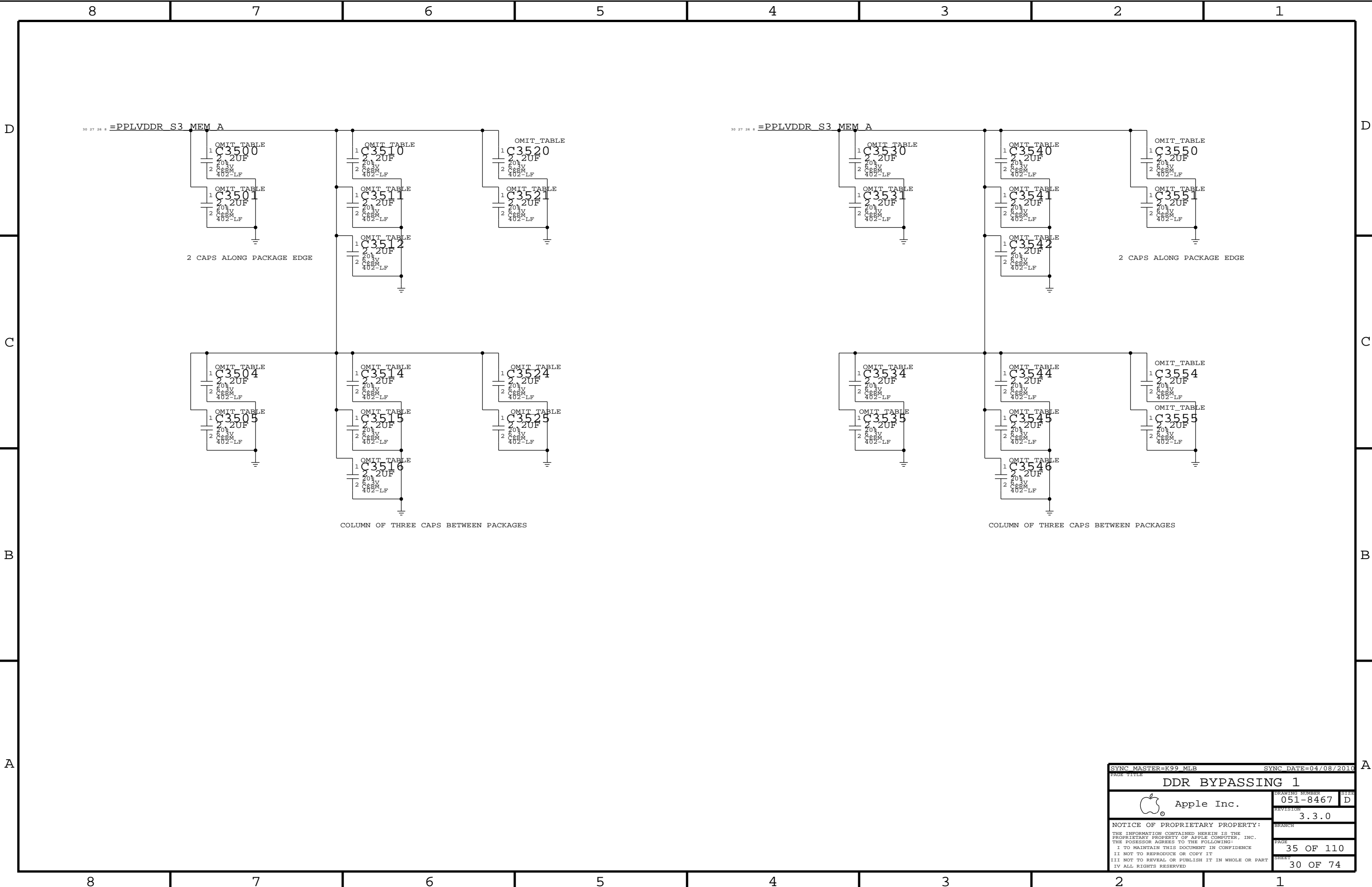
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

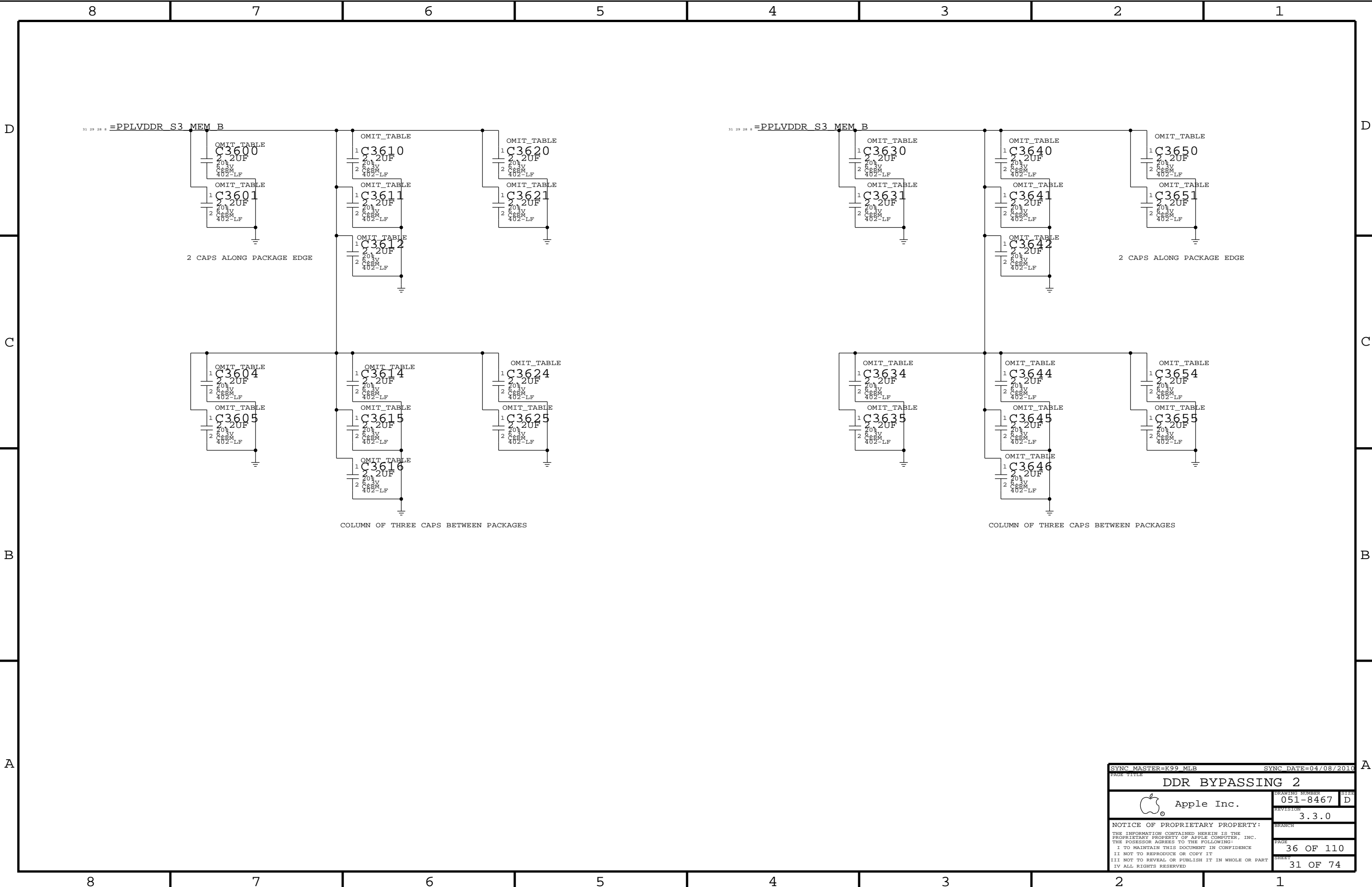
SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
DDR3 DRAM Channel B		(0-31)	
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	33 OF 110
		SHEET	28 OF 74

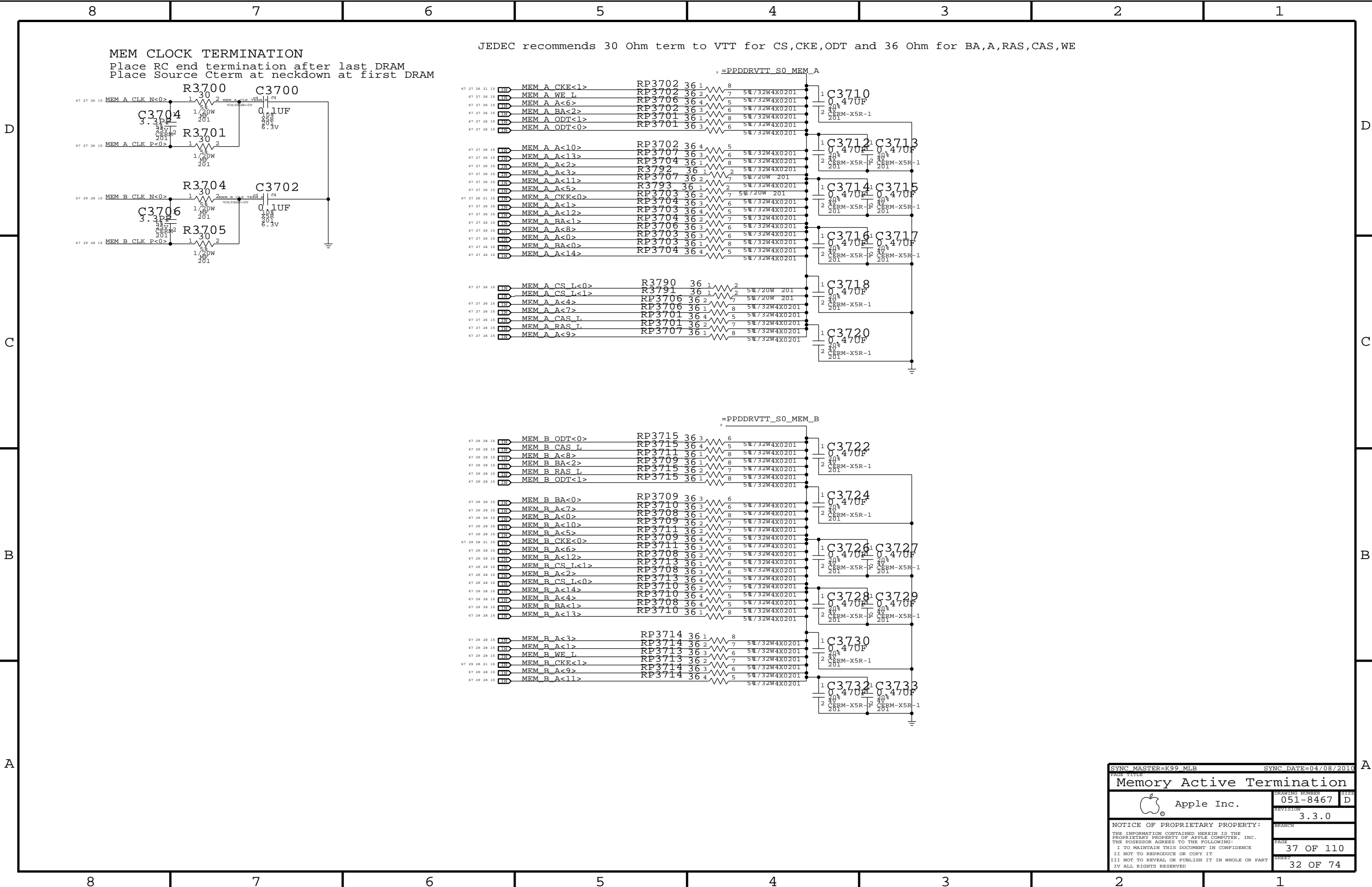


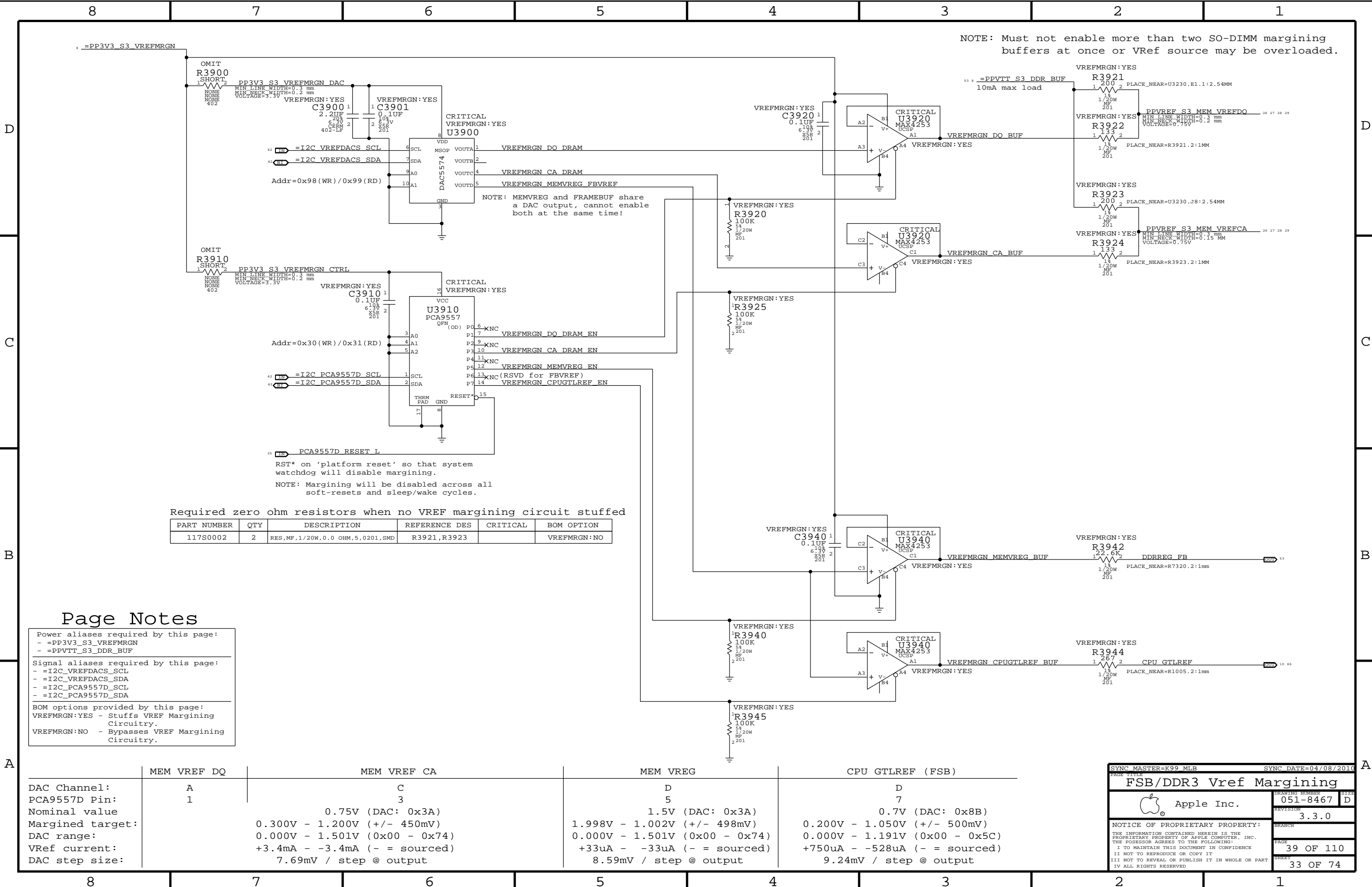
A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
DDR3 DRAM Channel B		B (32-63)	
	Apple Inc.	DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	34 OF 110
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	29 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			









Page Notes

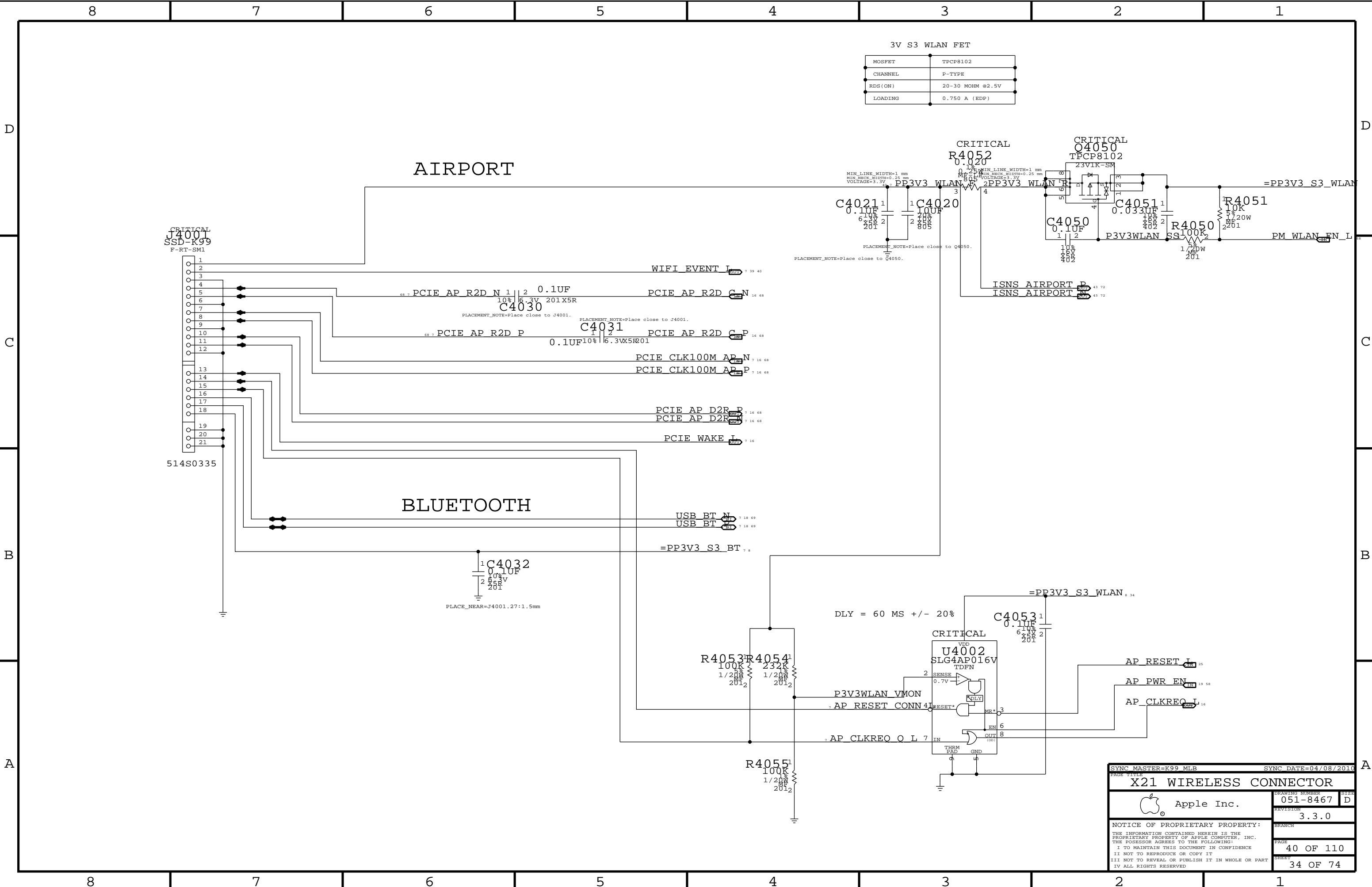
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN:YES - Stuffs VREF Margining Circuitry.
VREFMRGN:NO - Bypasses VREF Margining Circuitry.

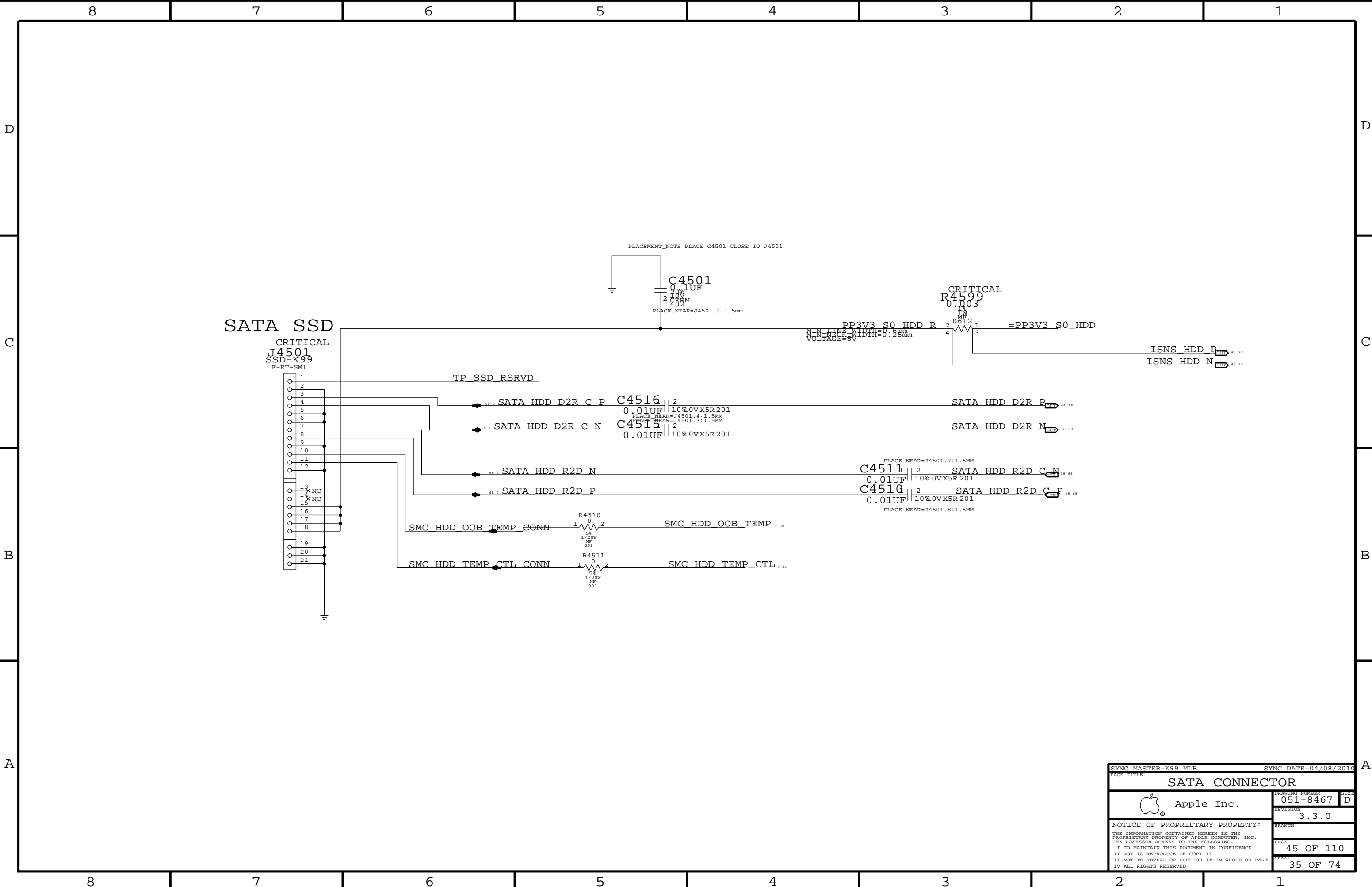
	MEM VREF DQ	MEM VREF CA	MEM VREG	CPU GTLREF (FSB)
DAC Channel:	A	C	D	D
PCA9557D Pin:	1	3	5	7
Nominal value		0.75V (DAC: 0x3A)	1.5V (DAC: 0x3A)	0.7V (DAC: 0x8B)
Margined target:		0.300V - 1.200V (+/- 450mV)	1.998V - 1.002V (+/- 498mV)	0.200V - 1.050V (+/- 500mV)
DAC range:		0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.501V (0x00 - 0x74)	0.000V - 1.191V (0x00 - 0x5C)
Vref current:		+3.4mA - -3.4mA (- = sourced)	+33uA - -33uA (- = sourced)	+750uA - -528uA (- = sourced)
DAC step size:		7.69mV / step @ output	8.59mV / step @ output	9.24mV / step @ output


PAGE TITLE		DRAWING NUMBER	
FSB/DDR3 Vref Margining		051-8467	
Apple Inc.		REVISION	
		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		39 OF 110	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		33 OF 74	
IV ALL RIGHTS RESERVED			



3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS (ON)	20-30 MOHM @2.5V
LOADING	0.750 A (EDP)

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE		X21 WIRELESS CONNECTOR	
Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	40 OF 110
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	34 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
SATA CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	45 OF 110
		SHEET	35 OF 74

D

C

B

A

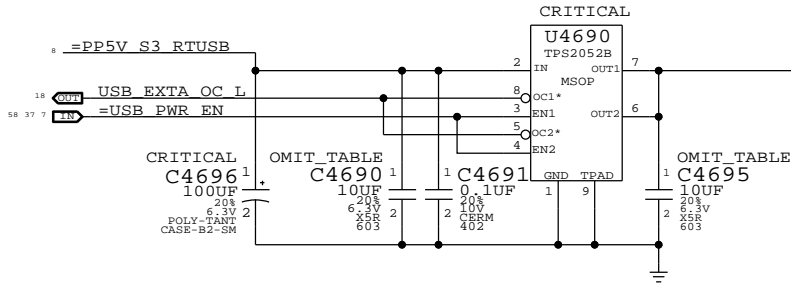
D

C

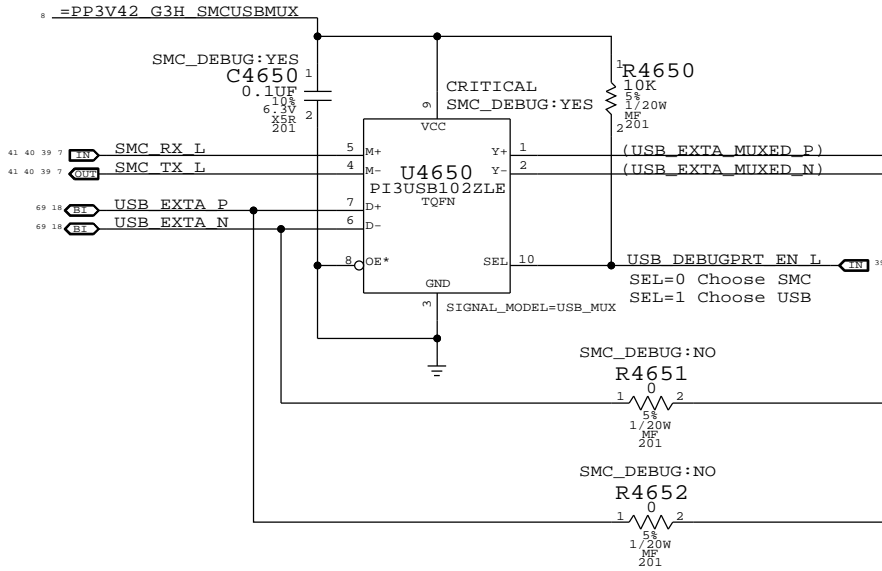
B

A

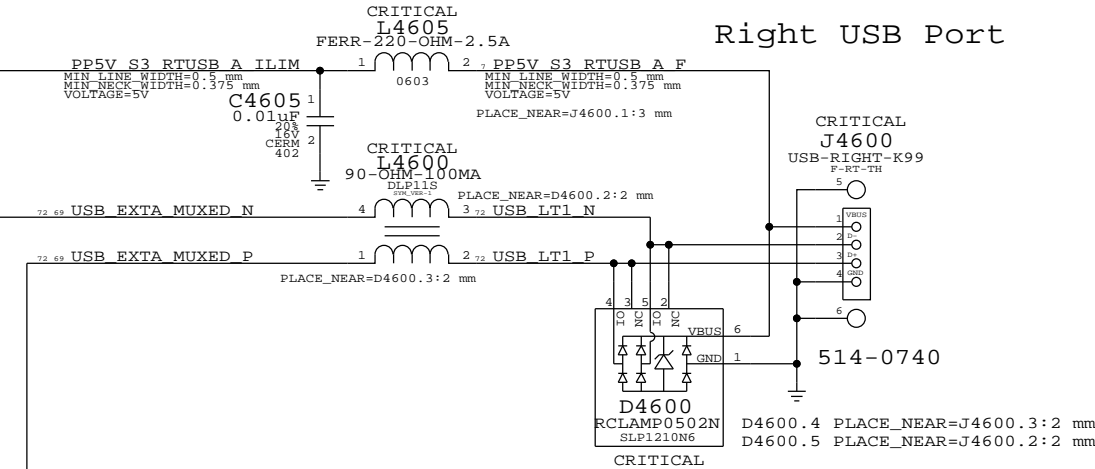
Port Power Switch




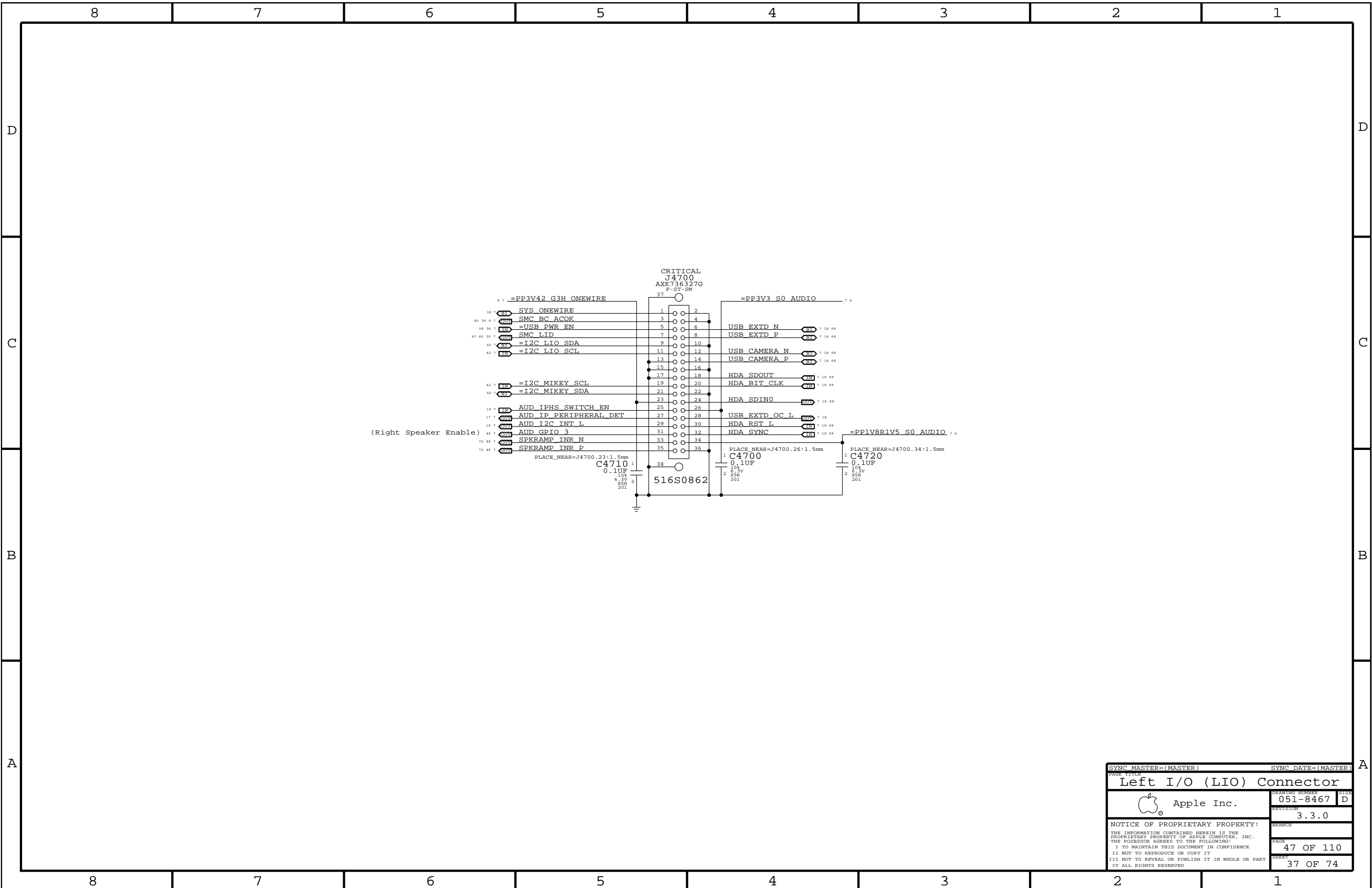
USB/SMC Debug Mux




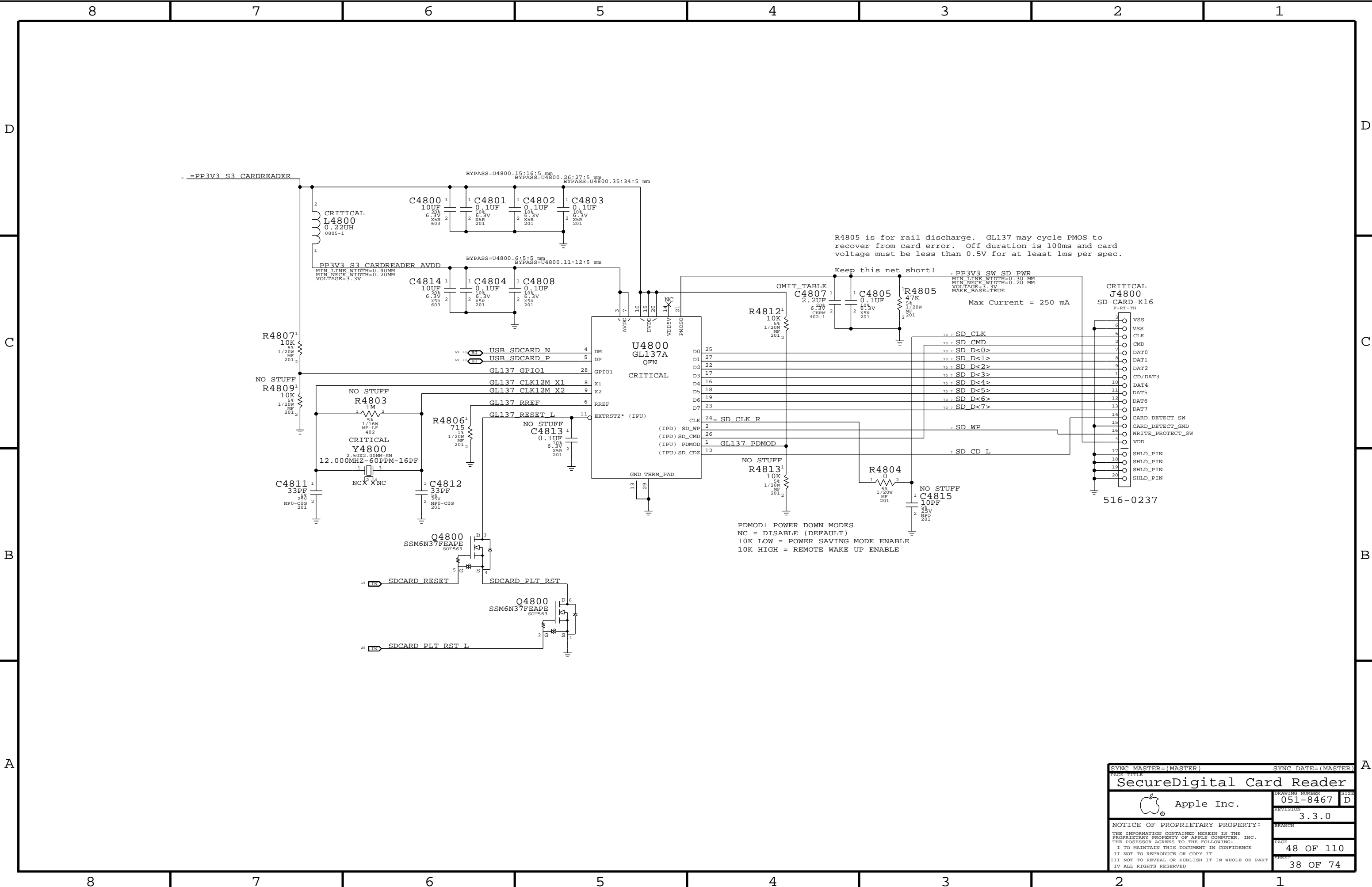
Right USB Port



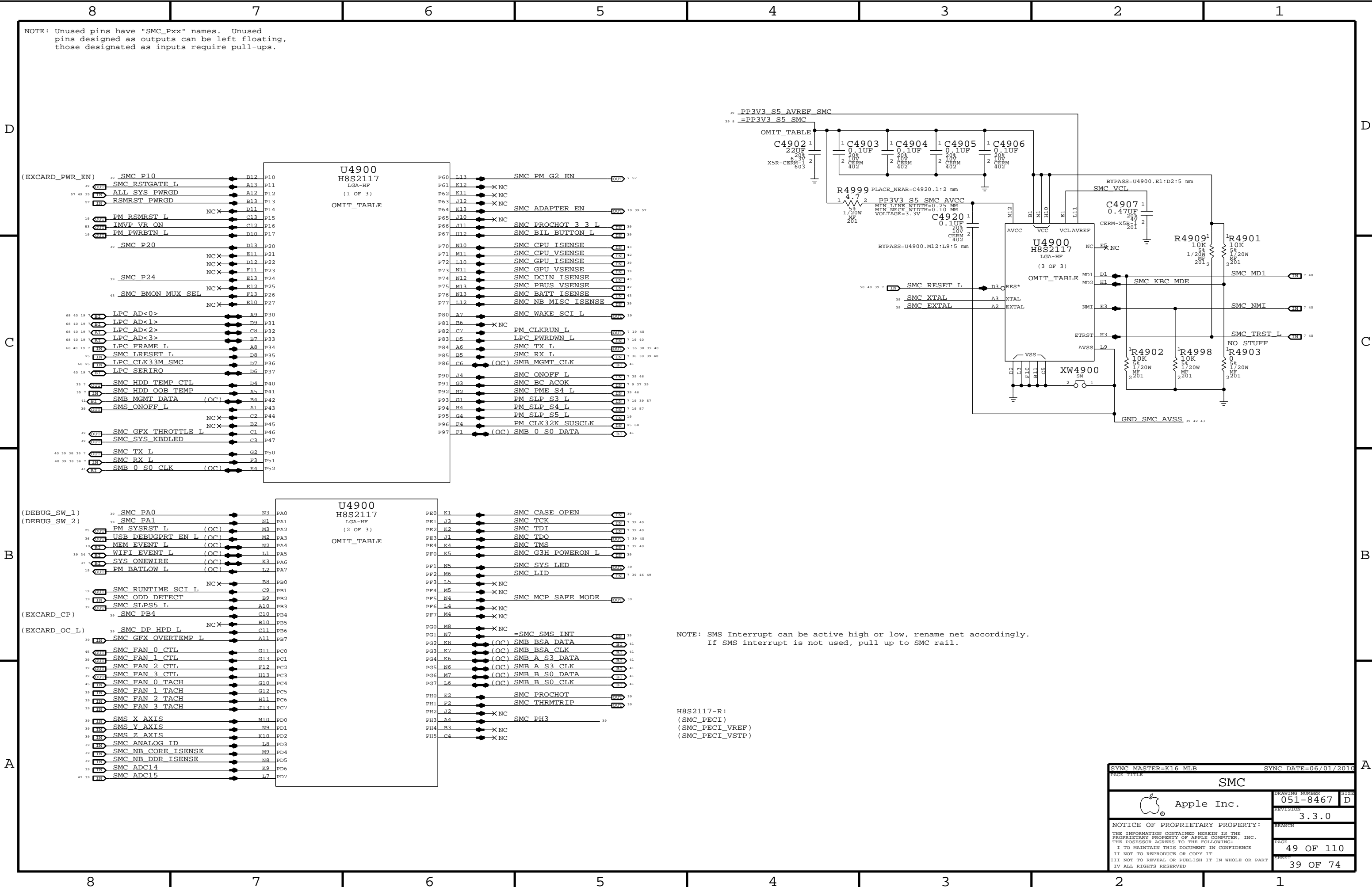
SYNC MASTER=K99 MLB		SYNC DATE=03/01/2010	
PAGE TITLE			
External USB Connectors			
 Apple Inc.		DRAWING NUMBER	051-8467
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	3.3.0
		BRANCH	
		PAGE	46 OF 110
		SHEET	36 OF 74



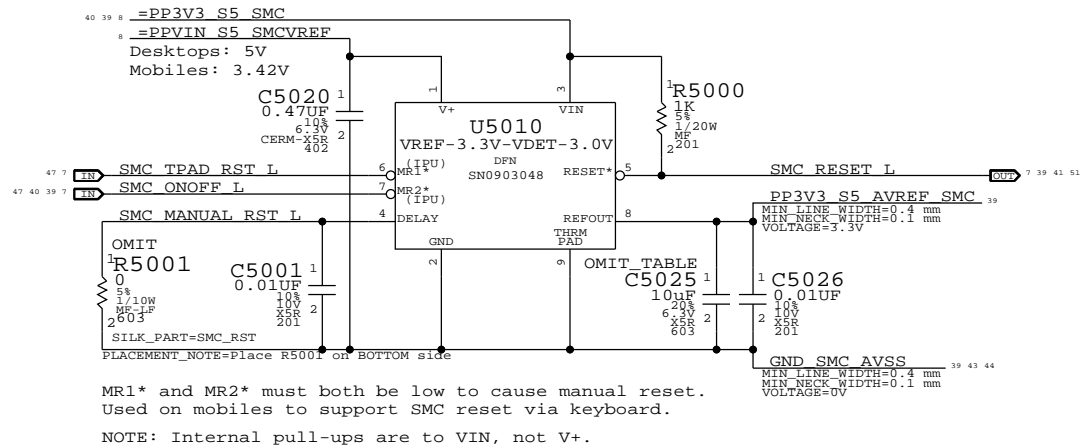
SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
PAGE TITLE			
Left I/O (LIO) Connector			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	47 OF 110
		SHEET	37 OF 74



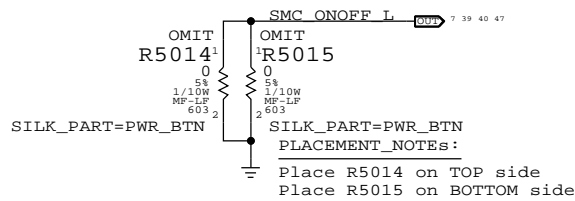
PAGE TITLE		PAGE NUMBER	
SecureDigital Card Reader		051-8467	
Apple Inc.		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		48 OF 110	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		38 OF 74	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



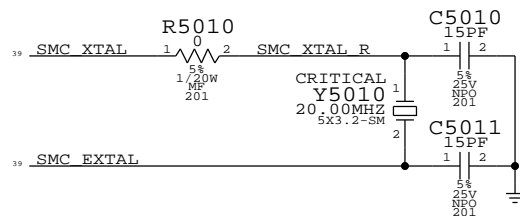
SMC Reset "Button", Supervisor & AVREF Supply



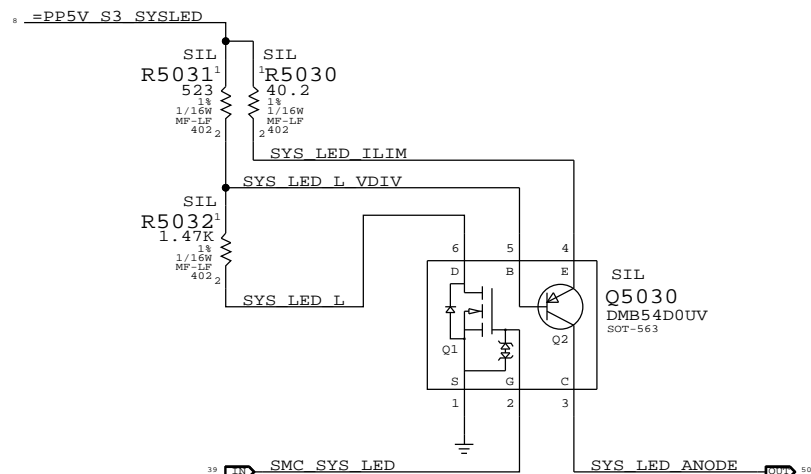
Debug Power "Buttons"



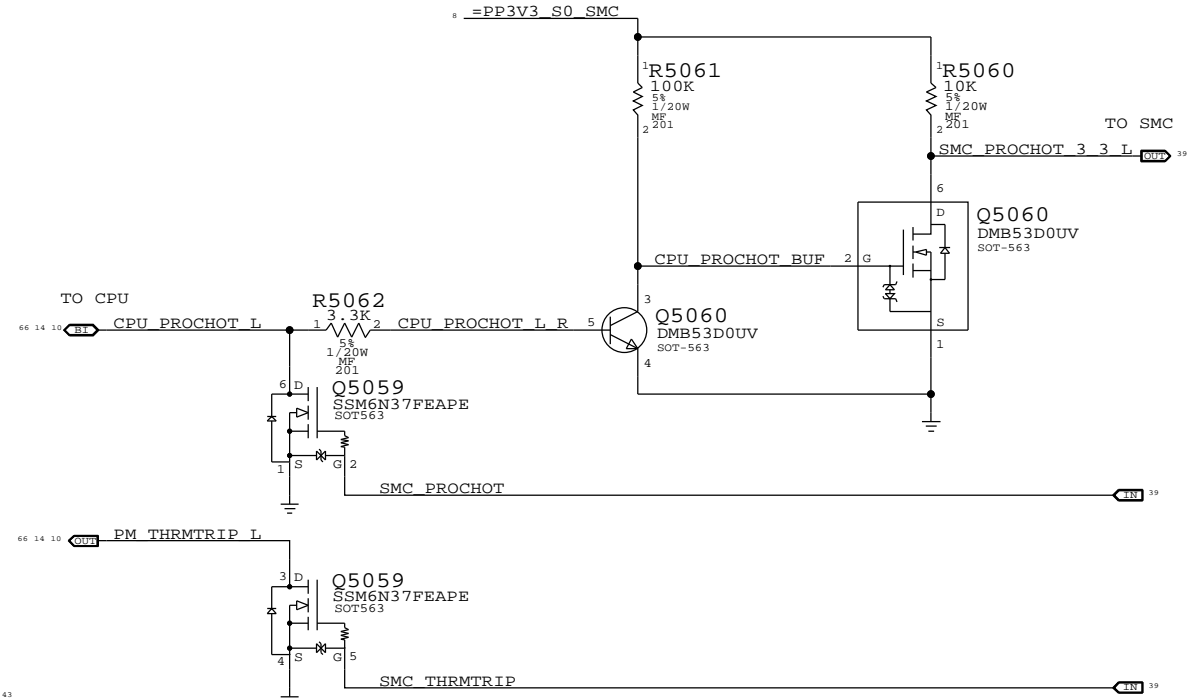
SMC Crystal Circuit



System (Sleep) LED Circuit

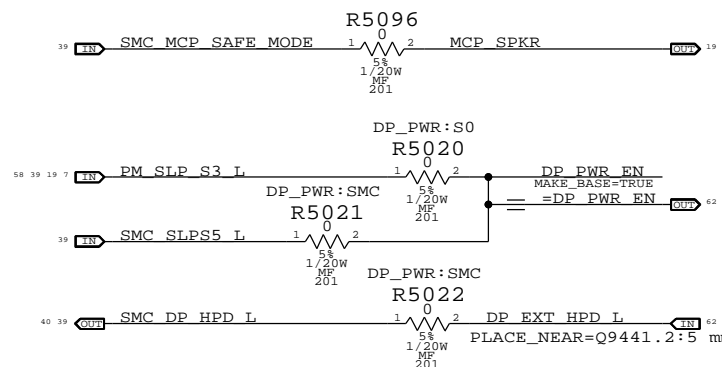


SMC FSB to 3.3V Level Shifting



SMC Aliases

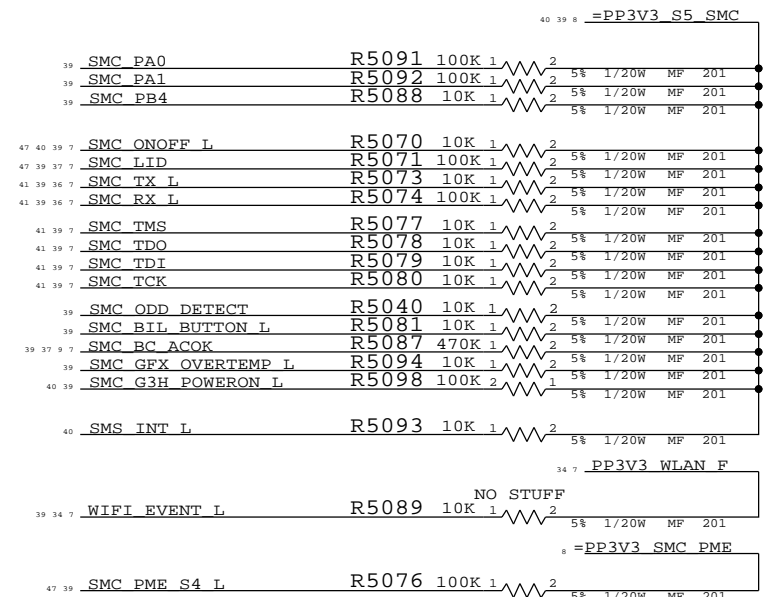
SMC LCDCLK ISENSE	=	SMS X AXIS	MAKE_BASE=TRUE
SMC WLAN ISENSE	=	SMS Y AXIS	MAKE_BASE=TRUE
SMC HDD ISENSE	=	SMS Z AXIS	MAKE_BASE=TRUE
SMC CSREG ISENSE	=	SMC ADC14	MAKE_BASE=TRUE
SMC LCDCLK VSENSE	=	SMC ADC15	MAKE_BASE=TRUE
SMC MCP CORE ISENSE	=	SMC NB CORE ISENSE	MAKE_BASE=TRUE
SMC MCP DDR ISENSE	=	SMC NB DDR ISENSE	MAKE_BASE=TRUE
SMC 1V5S3 ISENSE	=	SMC NB MISC ISENSE	MAKE_BASE=TRUE
TP SMC ANALOG ID	=	SMC ANALOG ID	MAKE_BASE=TRUE
TP SMC GPU ISENSE	=	SMC GPU ISENSE	MAKE_BASE=TRUE
SMC MCP VSENSE	=	SMC GPU VSENSE	MAKE_BASE=TRUE
SMC GFX THROTTLE L	=	SMC IG THROTTLE L	MAKE_BASE=TRUE
SMS INT L	=	=SMC SMS INT	MAKE_BASE=TRUE
MCP WAKE REO L	=	SMC G3H POWERON L	MAKE_BASE=TRUE



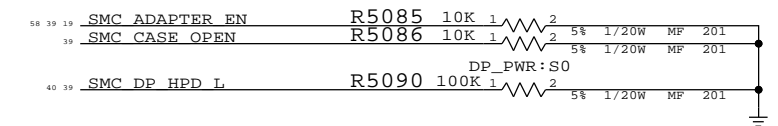
Unused Pins

SMS ONOFF L	=	TP SMS ONOFF L	MAKE_BASE=TRUE
SMC SYS KBDLED	=	TP SMC SYS KBDLED	MAKE_BASE=TRUE
SMC FAN 1 CTL	=	TP SMC FAN 1 CTL	MAKE_BASE=TRUE
TP SMC FAN 1 TACH	=	SMC FAN 1 TACH	MAKE_BASE=TRUE
SMC FAN 2 CTL	=	NC SMC FAN 2 CTL	MAKE_BASE=TRUE NO_TEST=TRUE
NC SMC FAN 2 TACH	=	SMC FAN 2 TACH	MAKE_BASE=TRUE NO_TEST=TRUE
SMC FAN 3 CTL	=	NC SMC FAN 3 CTL	MAKE_BASE=TRUE NO_TEST=TRUE
NC SMC FAN 3 TACH	=	SMC FAN 3 TACH	MAKE_BASE=TRUE NO_TEST=TRUE
SMC RSTGATE L	=	TP SMC RSTGATE L	MAKE_BASE=TRUE
SMC P10	=	TP SMC P10	MAKE_BASE=TRUE
SMC P20	=	TP SMC P20	MAKE_BASE=TRUE
SMC P24	=	TP SMC P24	MAKE_BASE=TRUE
SMC PH3	=	TP SMC PH3	MAKE_BASE=TRUE

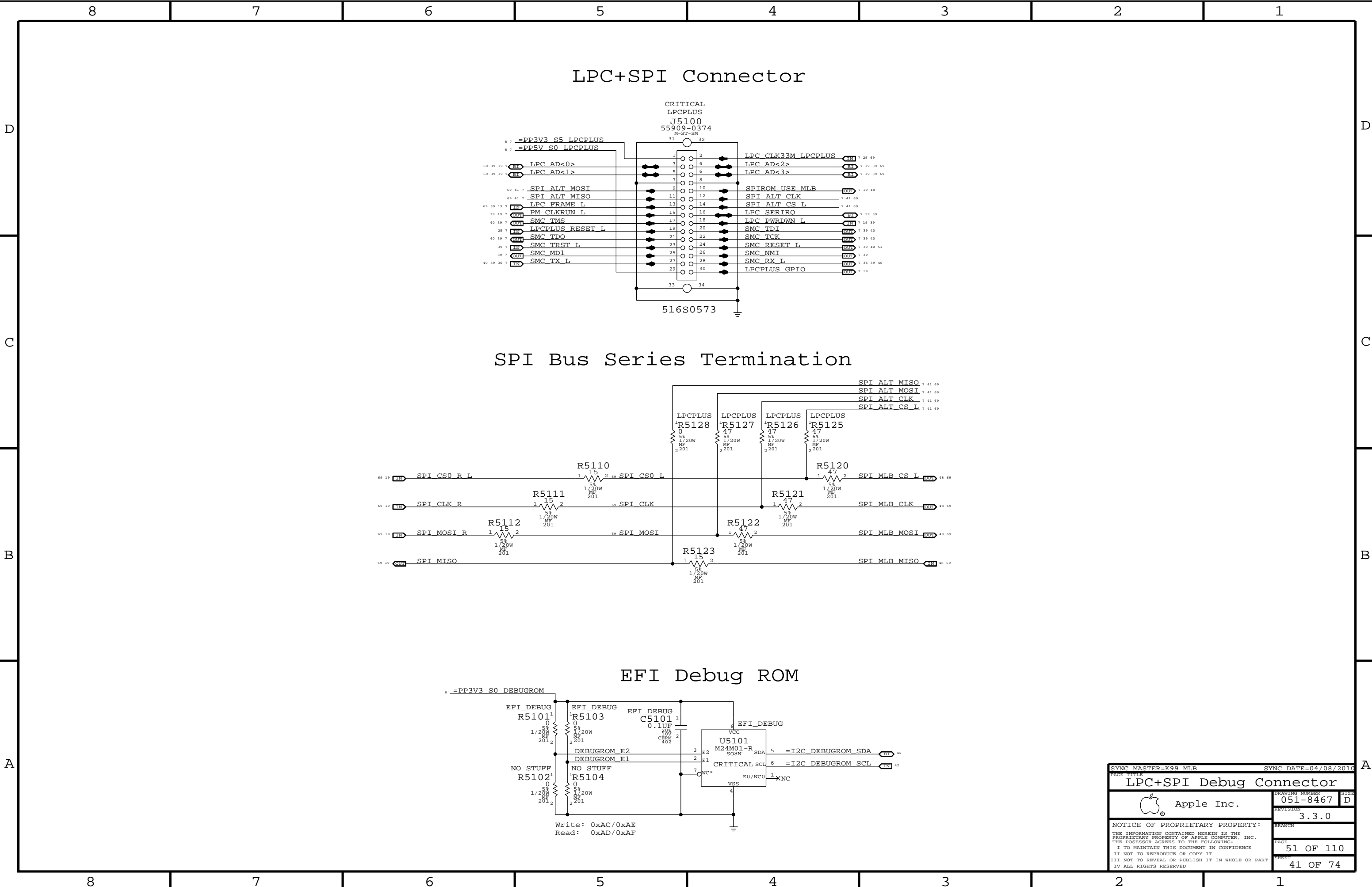
SMC Pull-ups



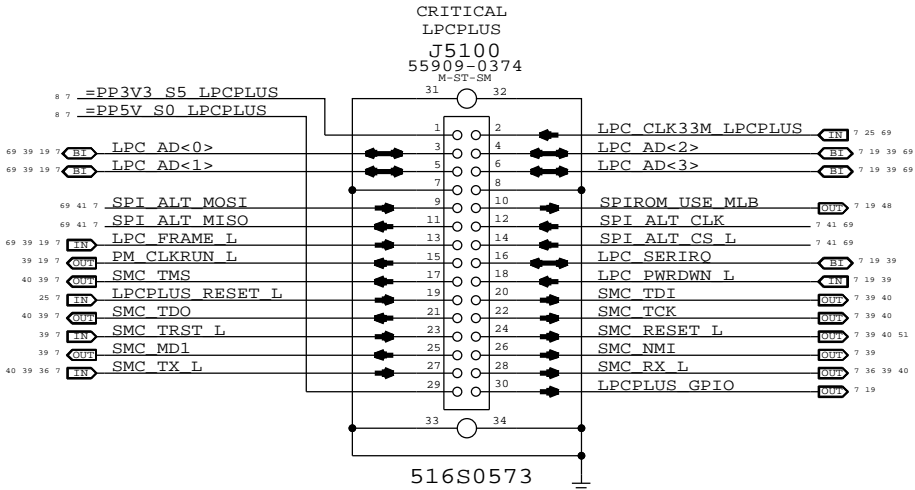
SMC Pull-downs



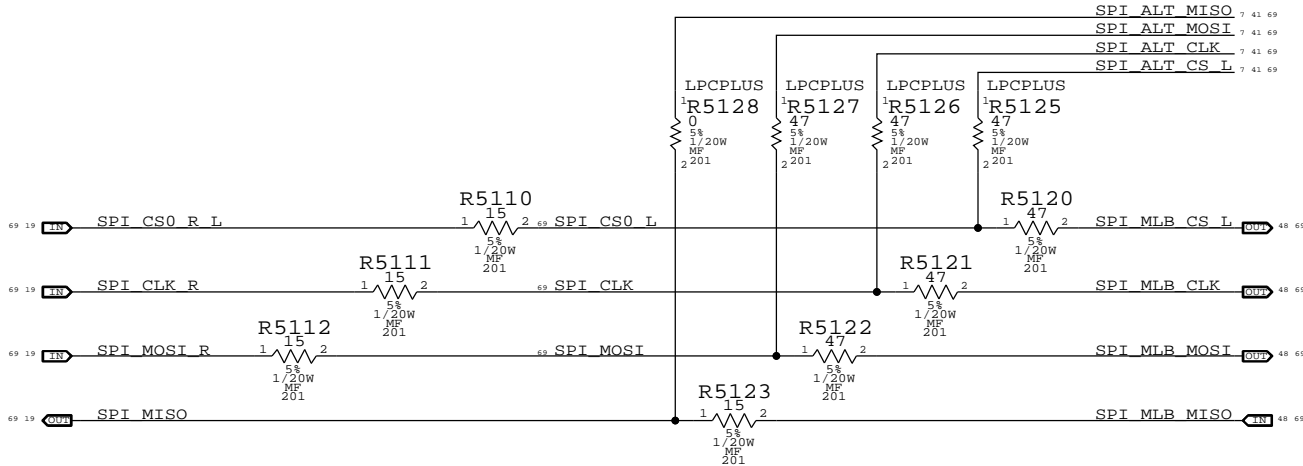
SYNC MASTER=(K99 MLB)		SYNC DATE=(03/01/2010)	
PAGE TITLE			
SMC Support		DRAWING NUMBER	SIZE
Apple Inc.		051-8467	D
REVISION		3.3.0	
BRANCH		PAGE	
NOTICE OF PROPRIETARY PROPERTY:		50 OF 110	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		SHEET	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		40 OF 74	
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



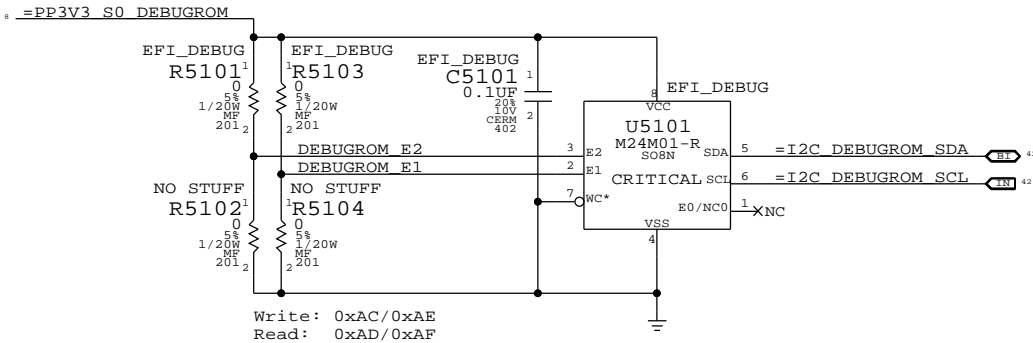
LPC+SPI Connector




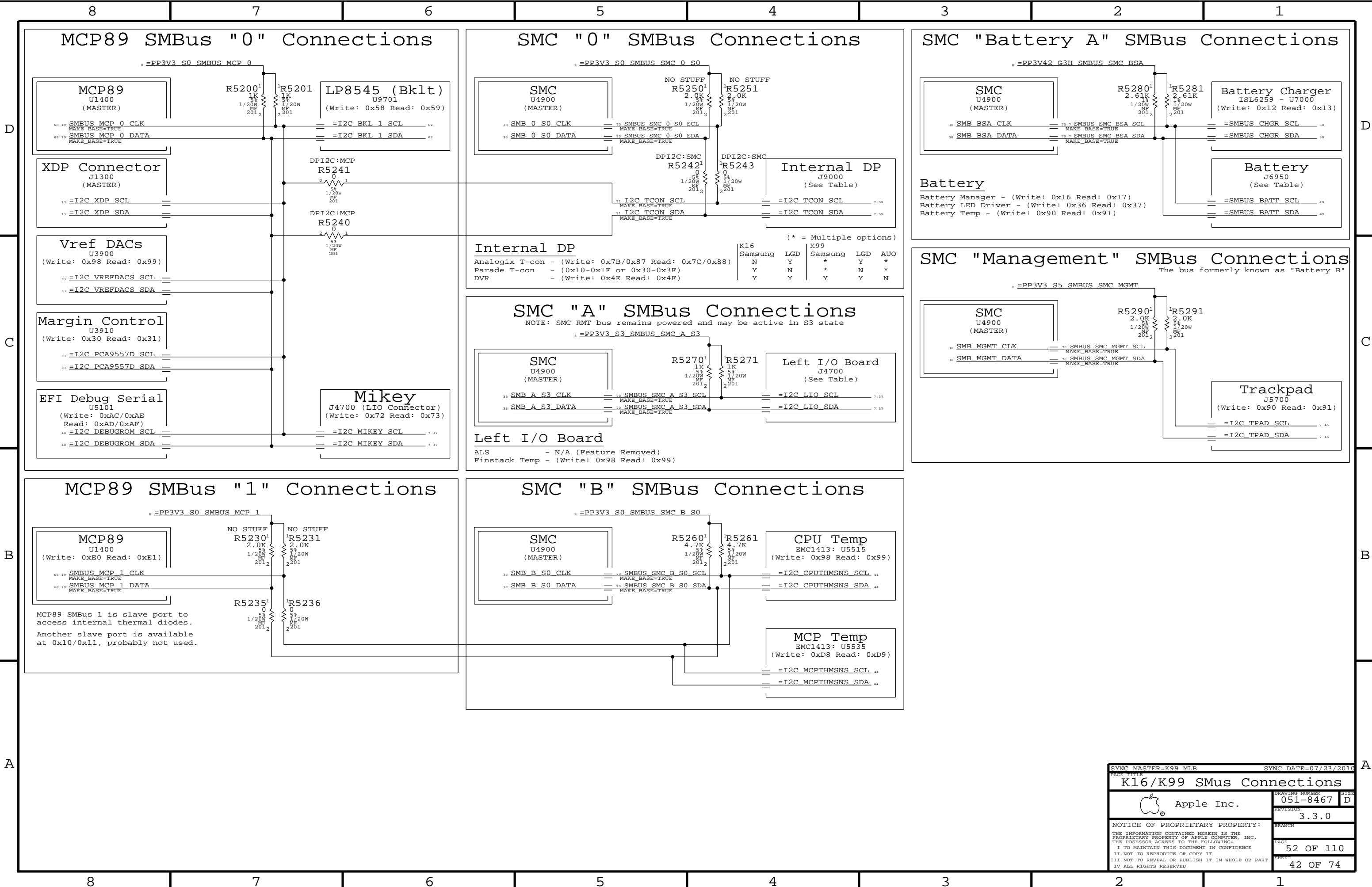
SPI Bus Series Termination

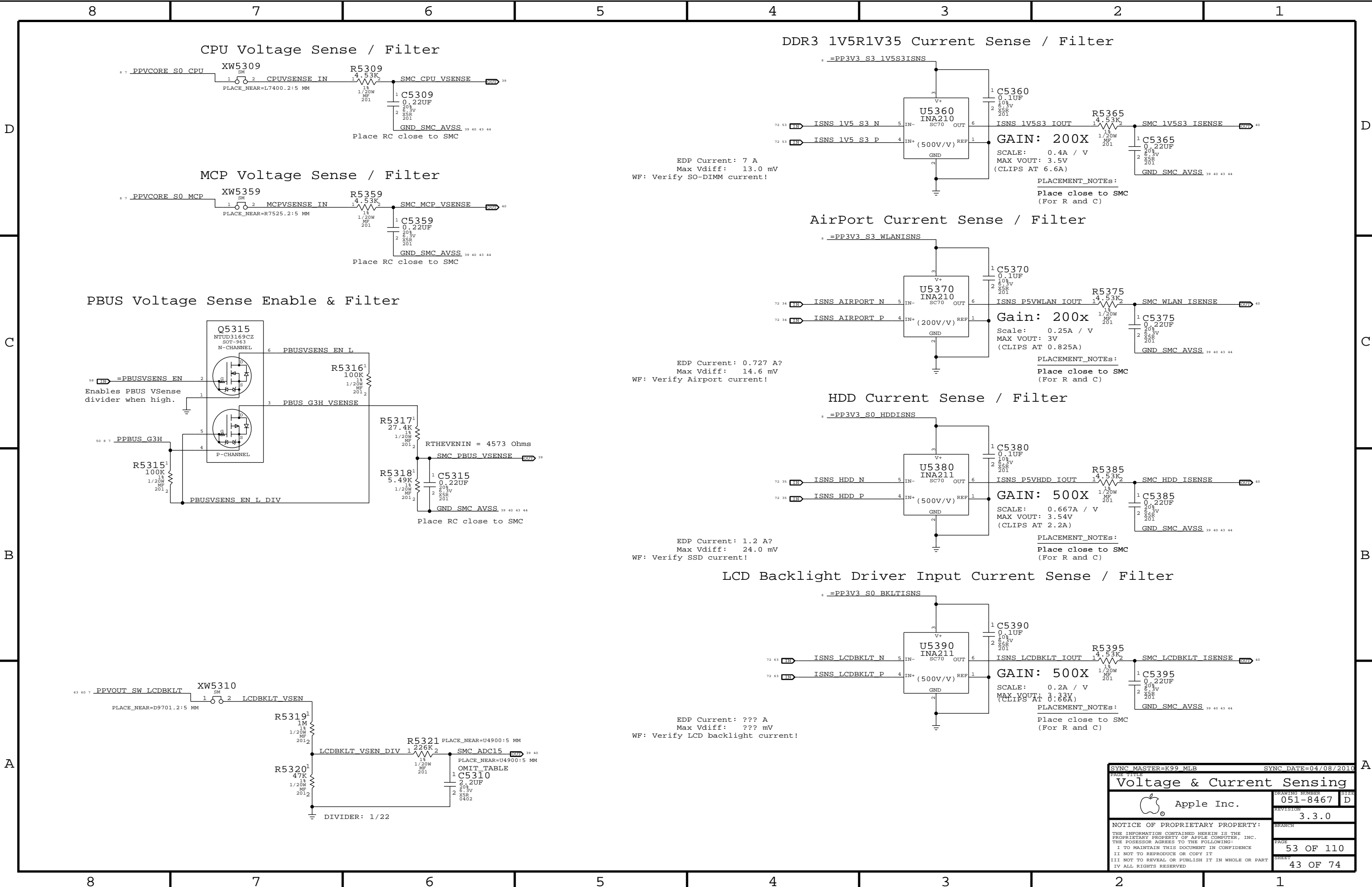


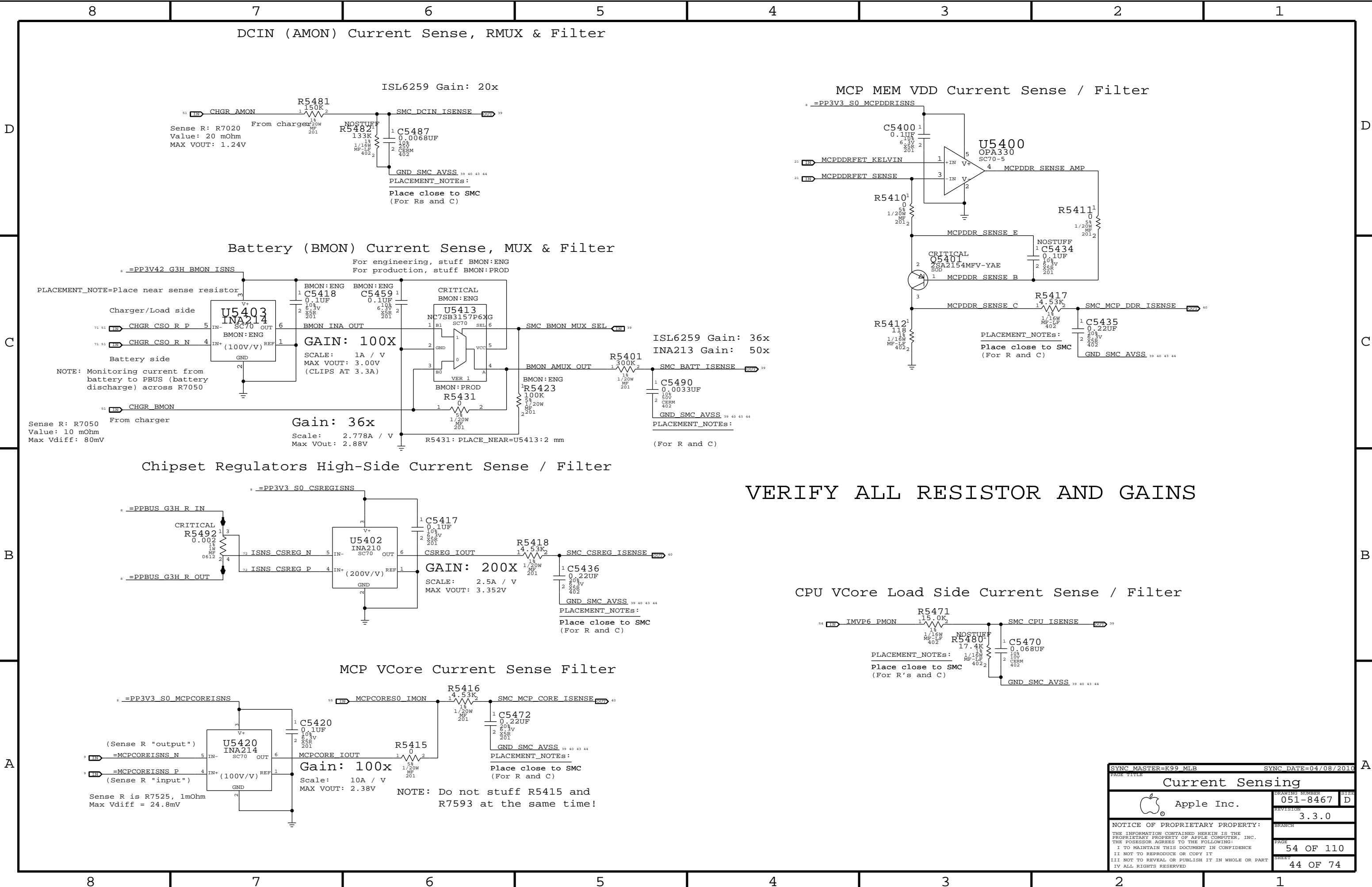
EFI Debug ROM




SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
LPC+SPI Debug Connector			
 Apple Inc.		DRAWING NUMBER	051-8467
		SIZE	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	3.3.0
		BRANCH	
		PAGE	51 OF 110
		SHEET	41 OF 74







VERIFY ALL RESISTOR AND GAINS

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
Current Sensing			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	54 OF 110
		SHEET	44 OF 74

D

C

B

A

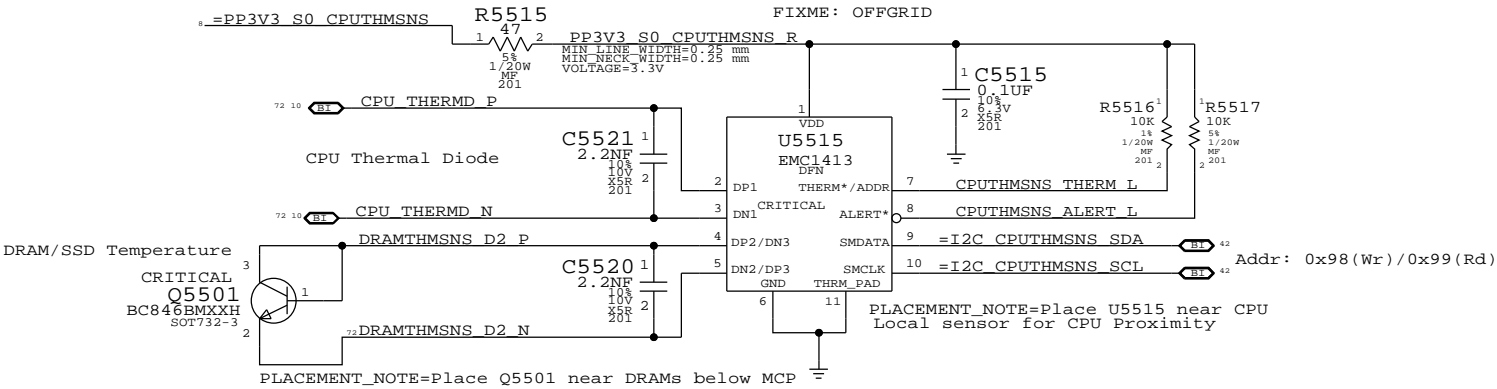
D

C

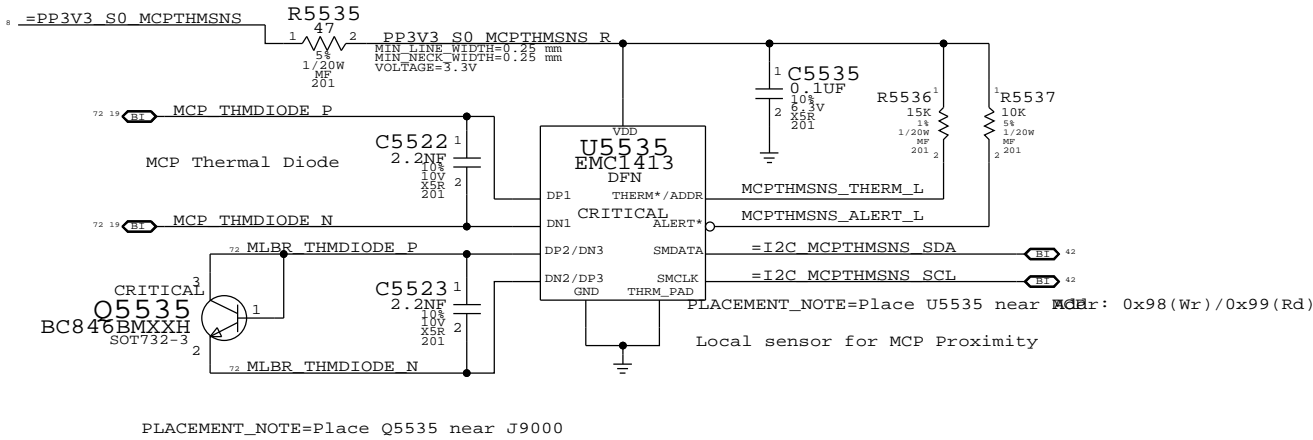
B


A

CPU T-Diode Thermal Sensor

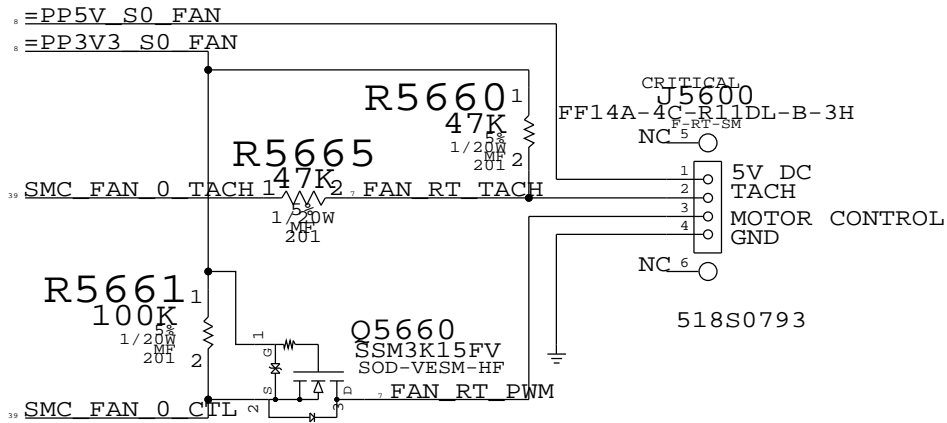


MCP T-Diode Thermal Sensor



SYNC MASTER=K99_MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
Thermal Sensors			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	55 OF 110
		SHEET	45 OF 74

FAN CONNECTOR



SYNC_MASTER=K99_MLB		SYNC_DATE=04/08/2010	
PAGE_TITLE		Fan	
Apple Inc.		DRAWING_NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	56 OF 110
		SHEET	46 OF 74

D

C

B

A

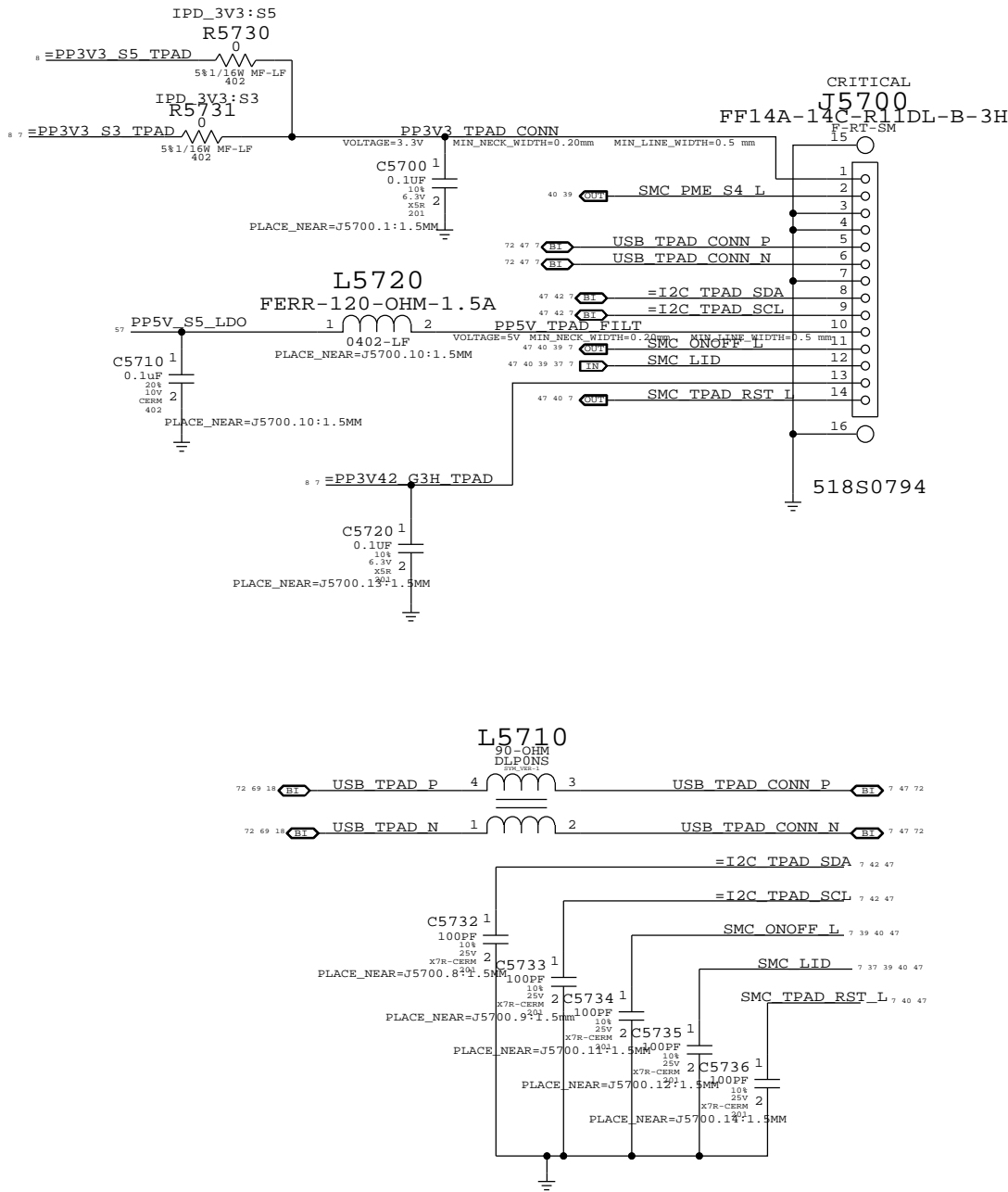
D


C

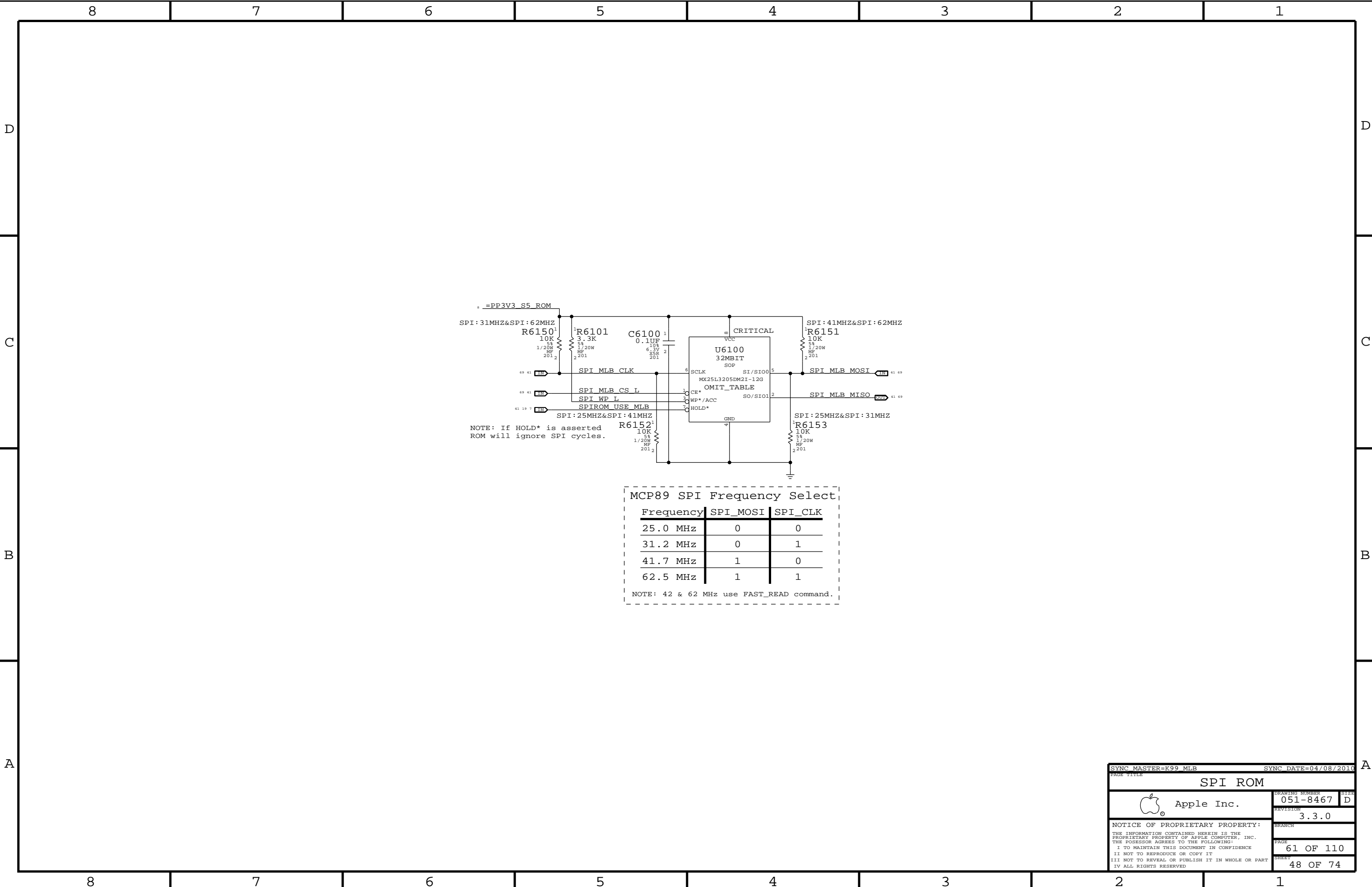
B

A

IPD Flex Connector

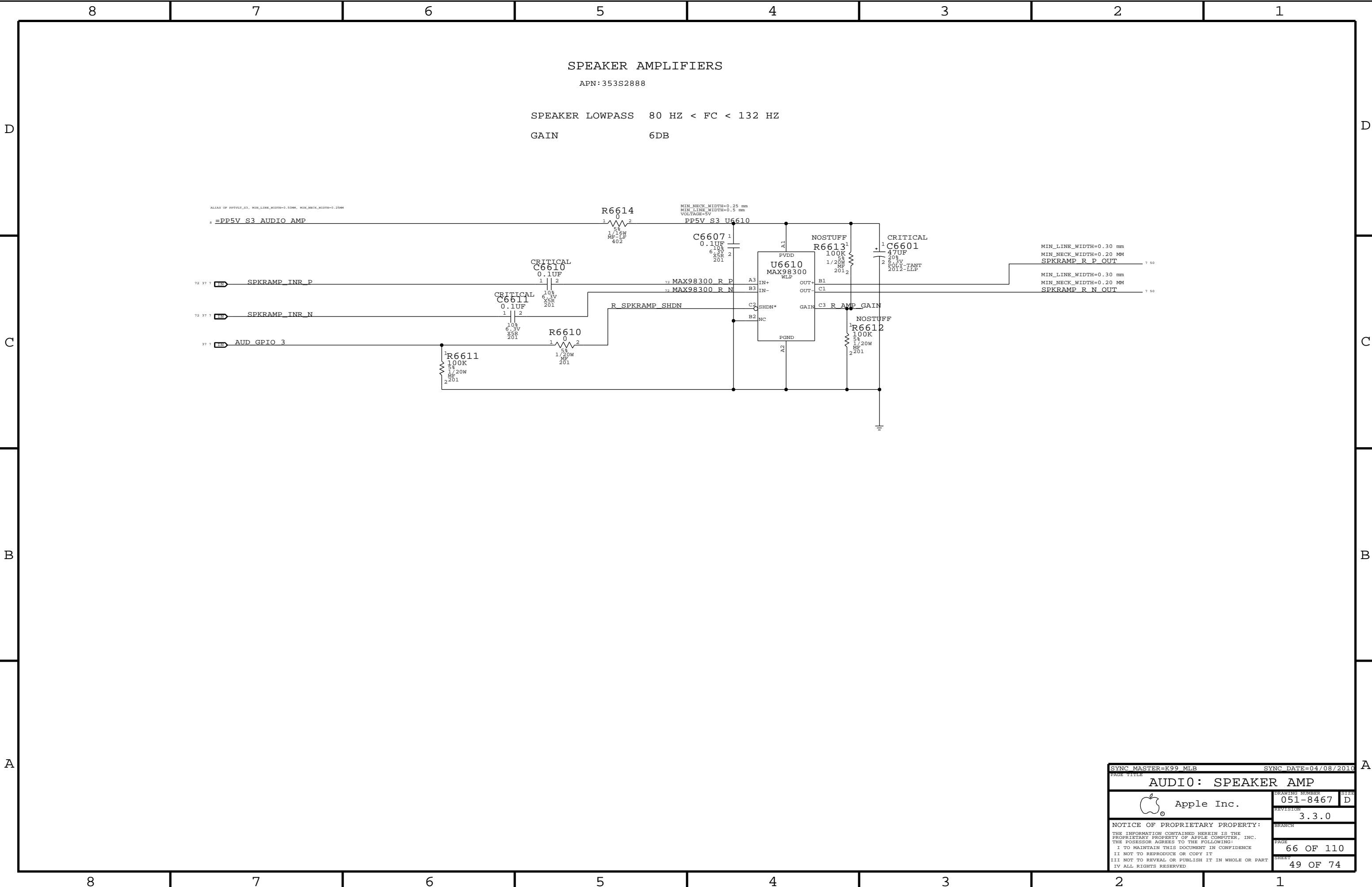


SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
WELLSPRING 1			
 Apple Inc.	DRAWING NUMBER		SHEET
	051-8467		D
	REVISION		
		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:			
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			
BRANCH		PAGE	
		57 OF 110	
SHEET			
		47 OF 74	



MCP89 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1


NOTE: 42 & 62 MHz use FAST_READ command.



SYNC_MASTER=K99_MLB

SYNC_DATE=04/08/2010

AUDIO0: SPEAKER AMP



Apple Inc.

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

051-8467

SIZE

D

REVISION

3.3.0

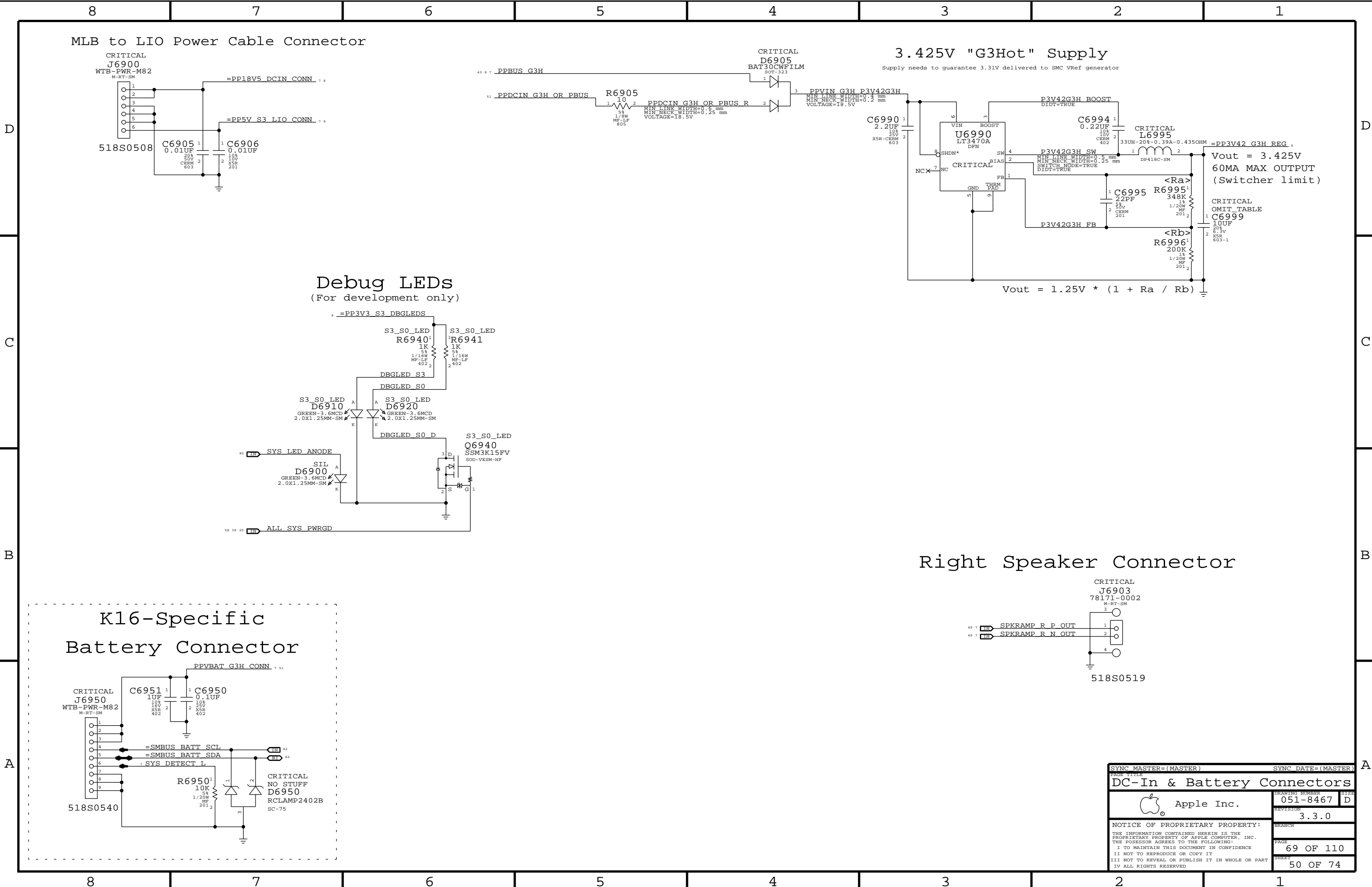
BRANCH

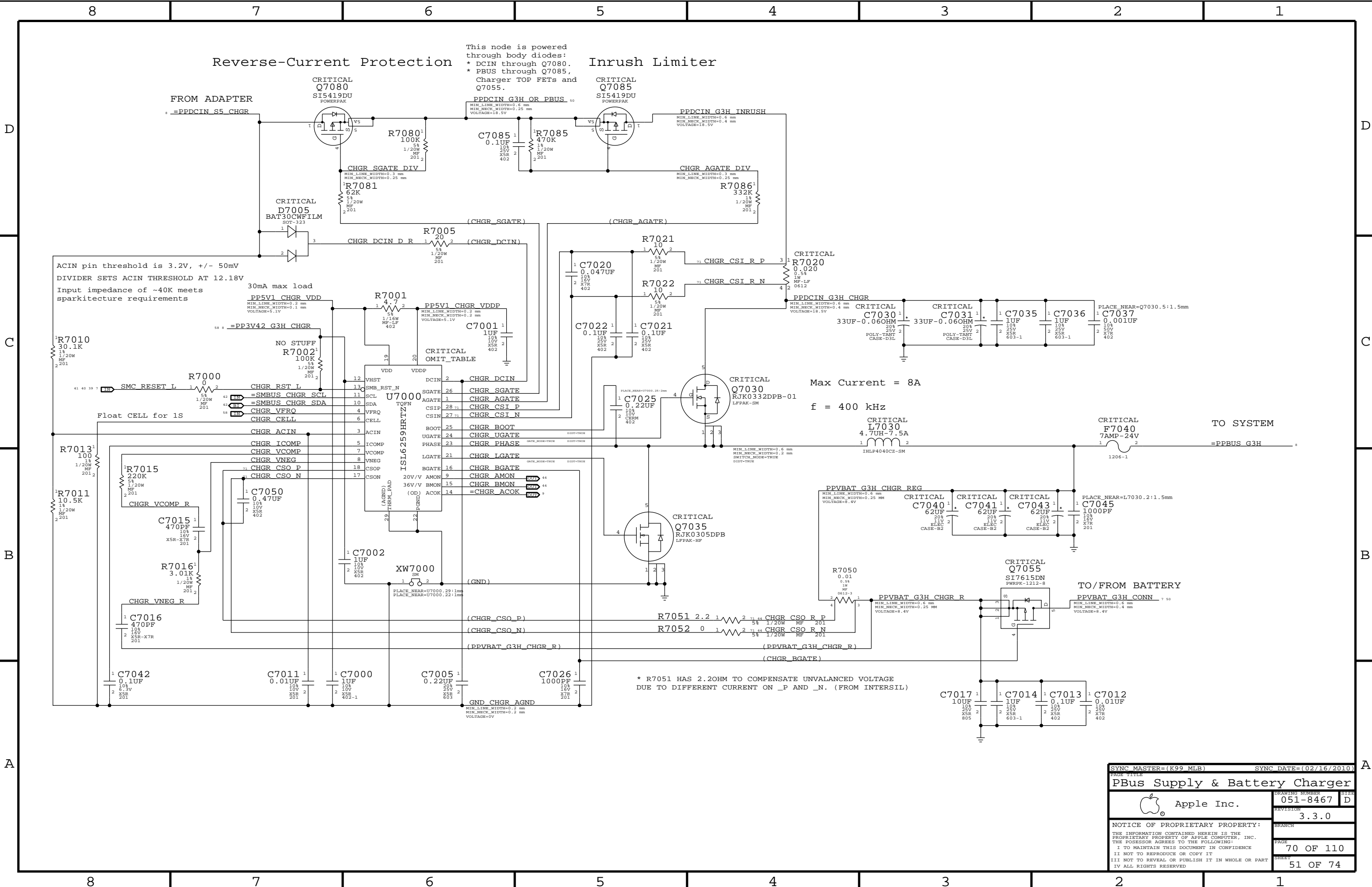
PAGE


66 OF 110

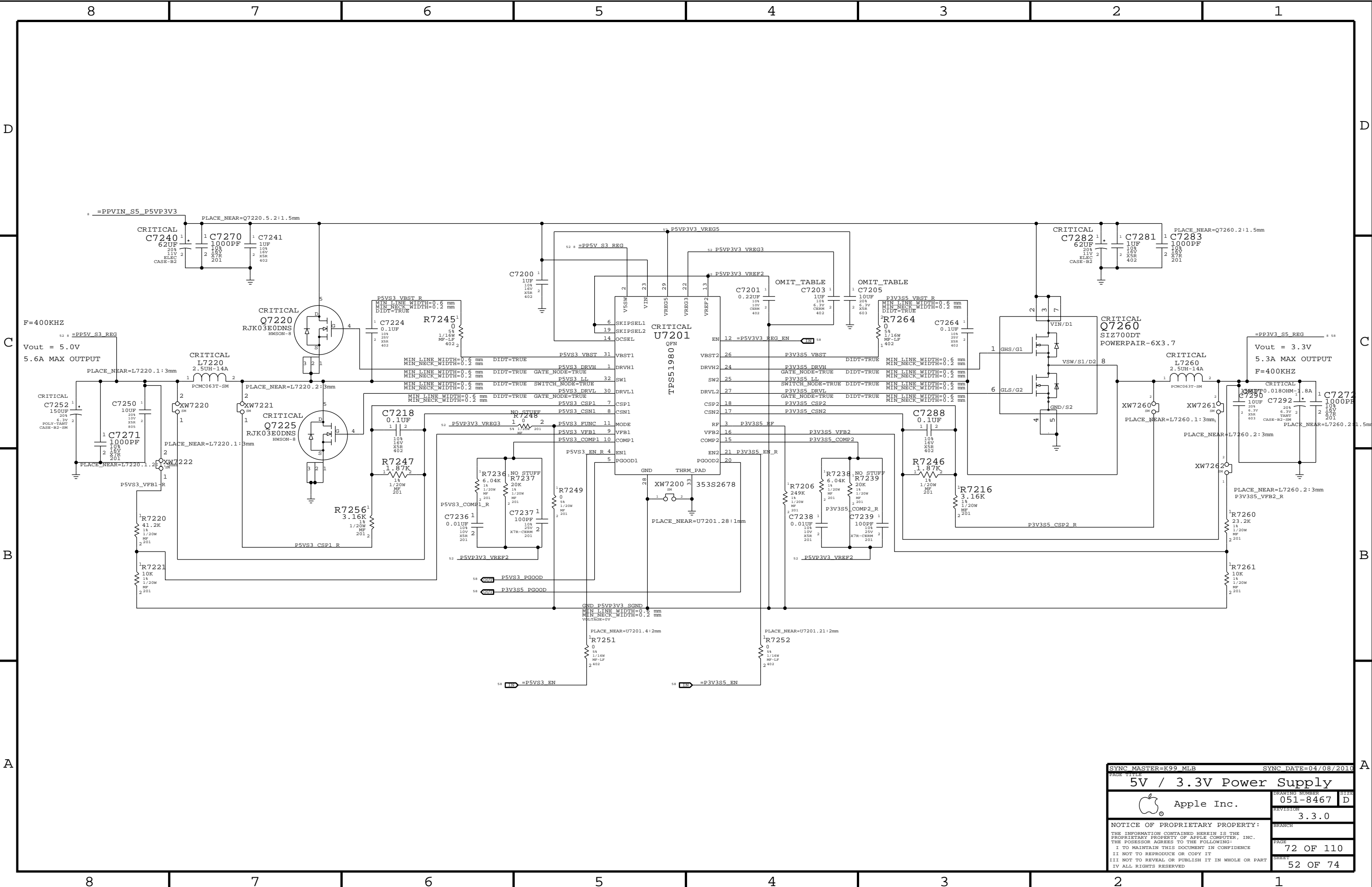
SHEET


49 OF 74





SYNC MASTER=(K99 MLB)		SYNC DATE=(02/16/2010)	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		BRANCH	
		PAGE	70 OF 110
		SHEET	51 OF 74



SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
5V / 3.3V Power Supply			
 Apple Inc.		DRAWING NUMBER	051-8467
		SIZE	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	3.3.0
		BRANCH	
PAGE		72	OF 110
SHEET		52	OF 74

D

C

B

A

D

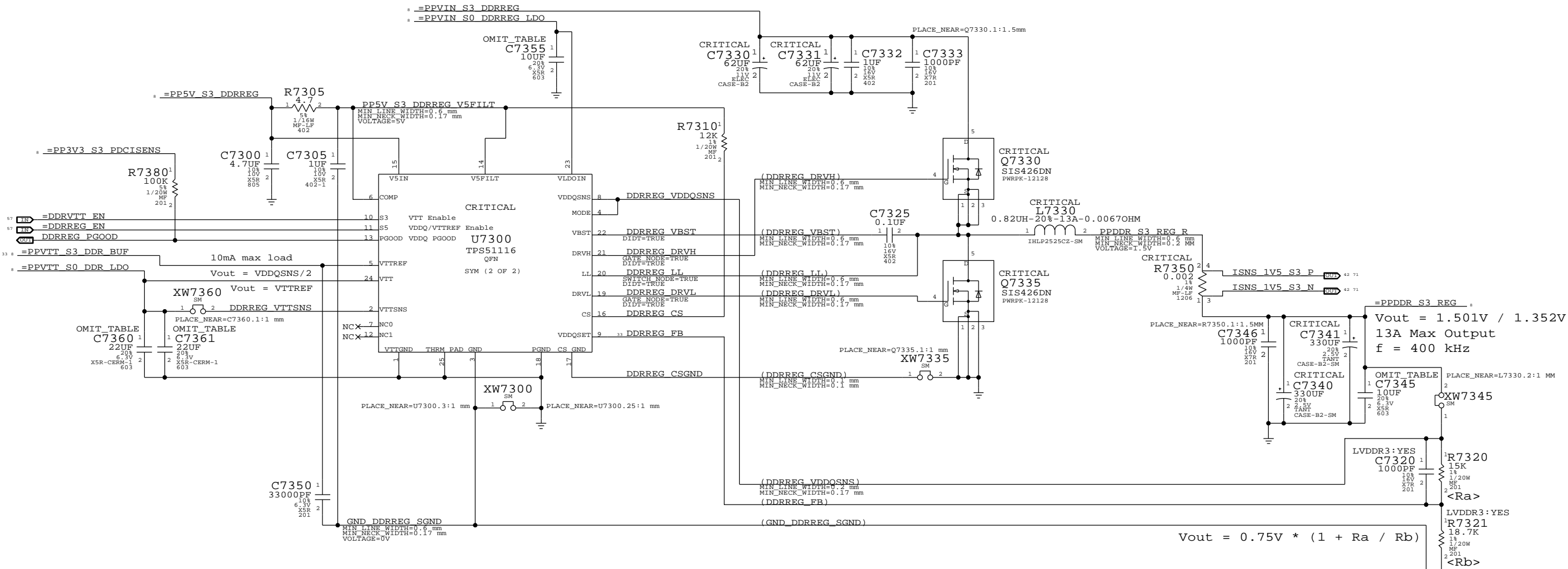
C

B

A

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1




Use LVDDR3:YES for fixed 1.35V operation or LVDDR3:NO for fixed 1.5V operation.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0331	1	RES,15K,1%,1/16W,MF-LF,0402	R7321		LVDDR3:NO

SYNC MASTER=K16 MLB

SYNC DATE=06/01/2010

1.5V/1.35V LVDDR3 Supply

 Apple Inc.

051-8467

3.3.0

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

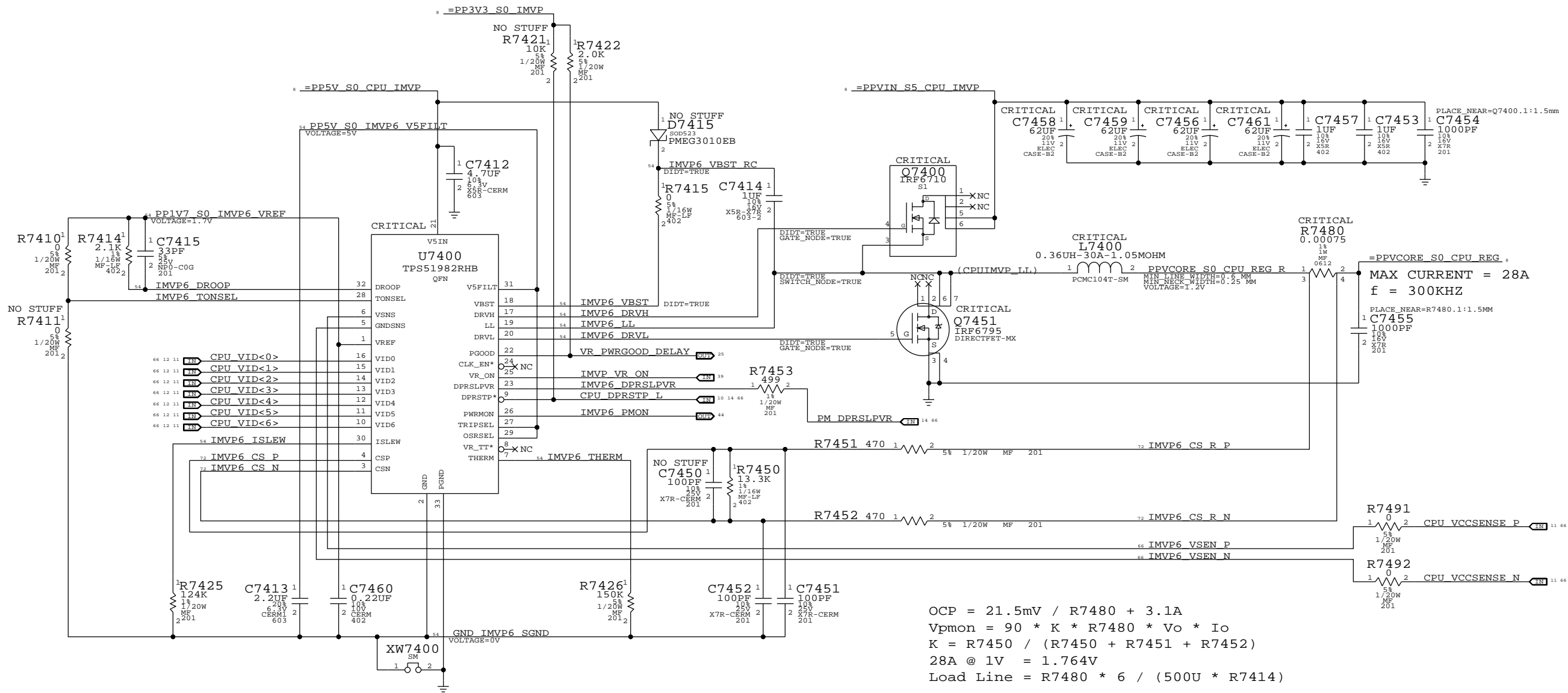
IV ALL RIGHTS RESERVED

PAGE

73 OF 110

SHEET

53 OF 74



OCp = 21.5mV / R7480 + 3.1A
Vpmon = 90 * K * R7480 * Vo * Io
K = R7450 / (R7450 + R7451 + R7452)
28A @ 1V = 1.764V
Load Line = R7480 * 6 / (500U * R7414)

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
54 GND IMVP6 SGND	0.50 MM	0.20 MM
54 IMVP6 DROOP	0.25 MM	0.20 MM
54 IMVP6 THERM	0.25 MM	0.20 MM
54 IMVP6 ISLEW	0.25 MM	0.20 MM
54 PP1V7 S0 IMVP6 VREF	0.25 MM	0.20 MM
54 PP5V S0 IMVP6 V5FILT	0.25 MM	0.20 MM
54 IMVP6 LL	1.5 MM	0.20 MM
54 IMVP6 VBST	0.25 MM	0.20 MM
54 IMVP6 DRVH	1.5 MM	0.20 MM
54 IMVP6 DRVL	1.5 MM	0.20 MM
54 IMVP6 VBST RC	1.5 MM	0.20 MM

SYNC MASTER=(K99 MLB) SYNC DATE=(02/16/2010)

PAGE TITLE

IMVP6 CPU VCore Regulator

Apple Inc.

051-8467

REVISION

3.3.0

NOTICE OF PROPRIETARY PROPERTY:

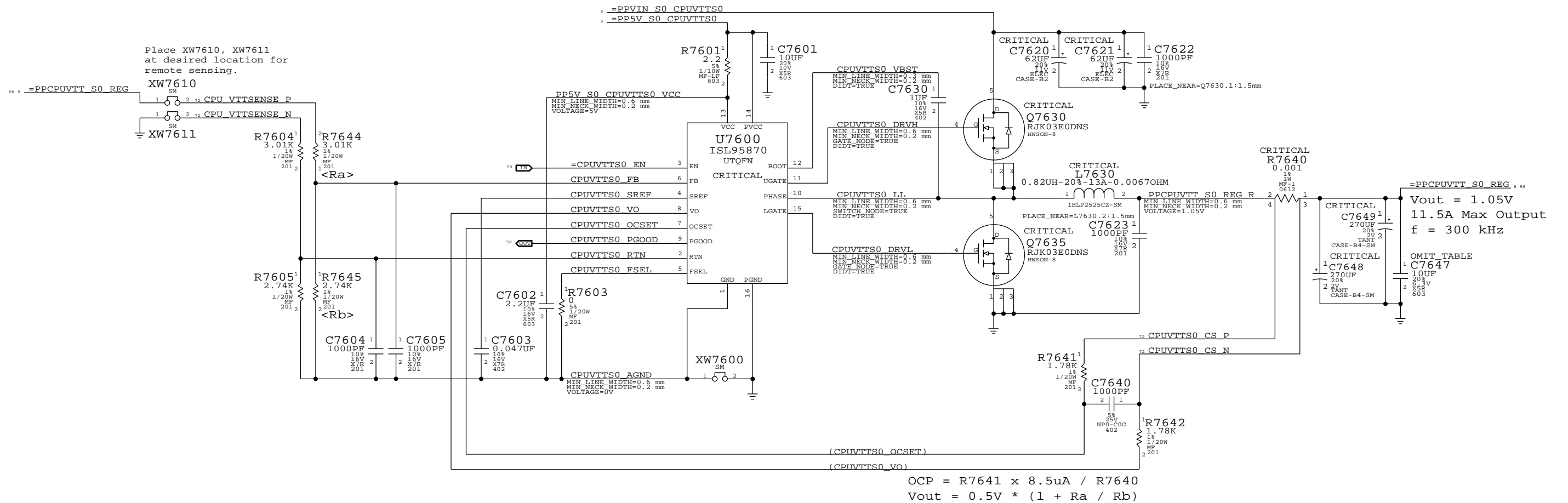
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER

74 OF 110

SIZE

54 OF 74




SYNC MASTER=(K99 MLB)

SYNC DATE=(03/01/2010)

PAGE TITLE

CPUVTT (1.05V) Power Supply

 Apple Inc.

DRAWING NUMBER

051-8467

SIZE

D

REVISION

3.3.0

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BRANCH

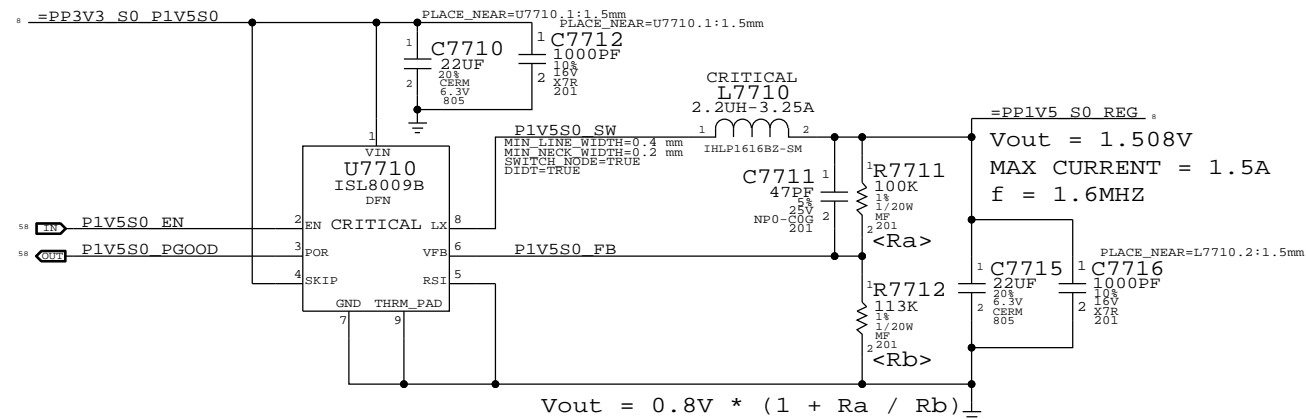
PAGE

SHEET

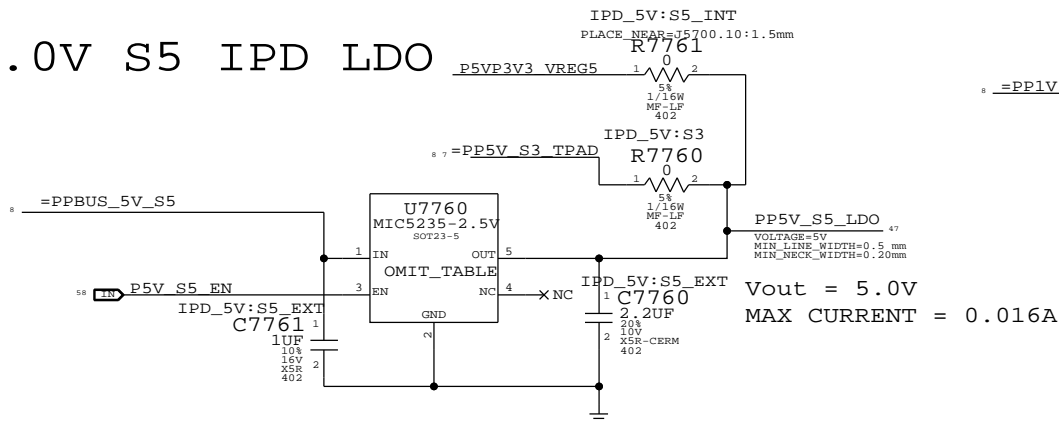
76 OF 110

56 OF 74

1.5V S0 Regulator

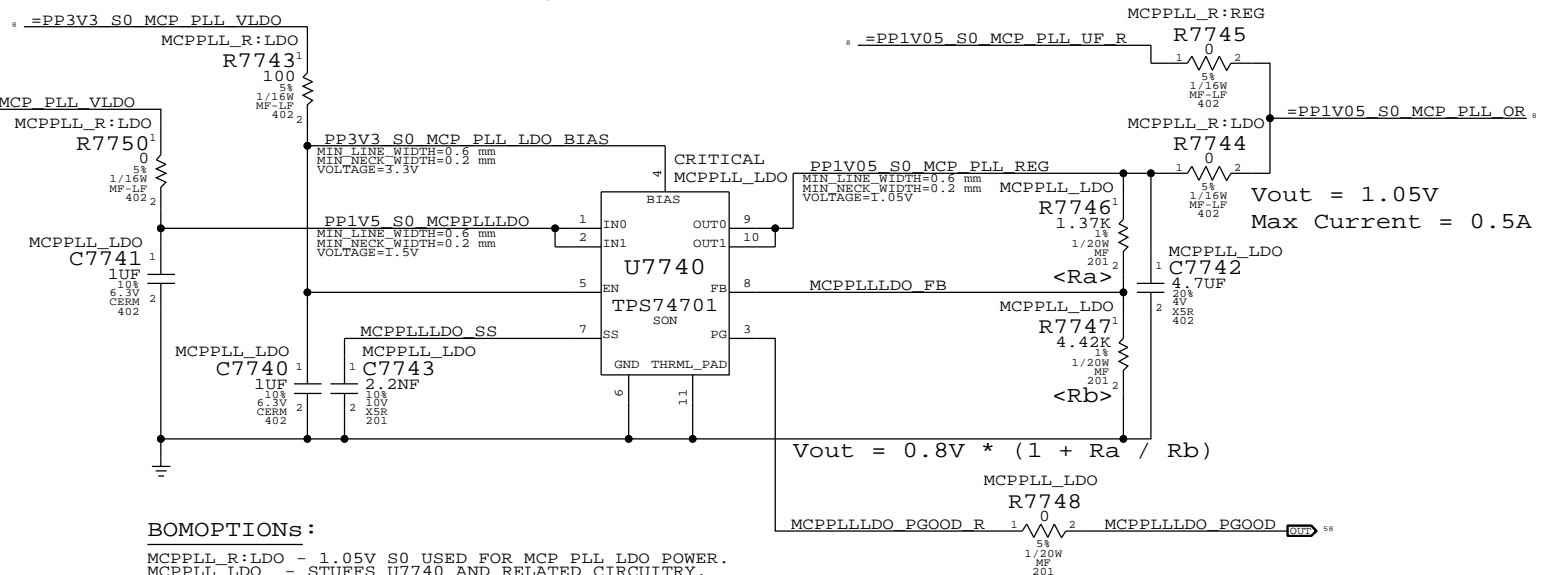


5.0V S5 IPD LDO



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3034	1	IC,LDO,MIC5235,5V,1A,150MA,SOT23-5	U7760		IPD_5V:S5_EXT

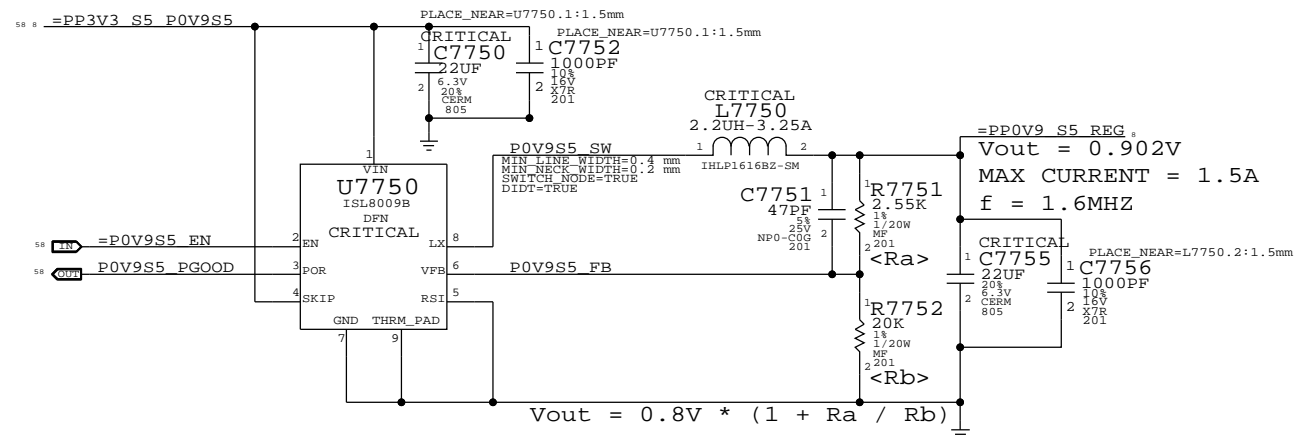
1.05V S0 MCP PLL LDO




BOMOPTIONS:

MCPPLL_R:LDO - 1.05V S0 USED FOR MCP PLL LDO POWER.
MCPPLL_LDO - STUFFS U7740 AND RELATED CIRCUITRY.
TO USE U7740, MCPPLL_R:LDO AND MCPPLL_LDO MUST BE ACTIVE.
TO USE 1.05V S0, MCPPLL_R:REG MUST BE ACTIVE, MCPPLL_LDO CAN BE ACTIVE, MCPPLL_R:LDO MUST BE INACTIVE.

MCP 0.9V S5 (AUXC) Switcher



SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
Misc Power Supplies			
 Apple Inc.		DRAWING NUMBER	051-8467
		SIZE	D
NOTICE OF PROPRIETARY PROPERTY:		REVISION	3.3.0
		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	77 OF 110
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	57 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



C

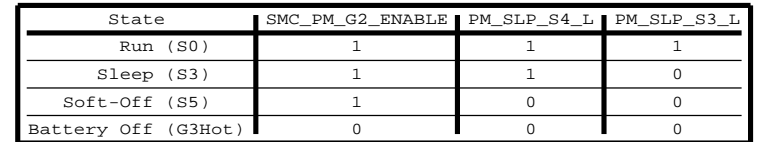
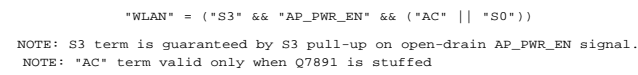
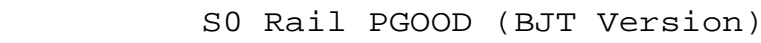


A

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).



S0 Rail PGOOD (ISL Version)



PM_SLP_S4_L 1 2 0 5K 1/20W 5% MF 201

VFRQ:SLP4

R7864

VFRQ:SLP3 1 2 0 5K 1/20W 5% MF 201

R7863

CHGR_VFRQ_GATE

CHGR_VFRQ

Q7860

SSM3K15FV

SOD-VESM-HF

D1

1N4148

SOD-56

R7861

10K

5K

1/20W

5%

MF

201

R7860

10K

5K

1/20W

5%

MF

201

M3

1/2HP

115V

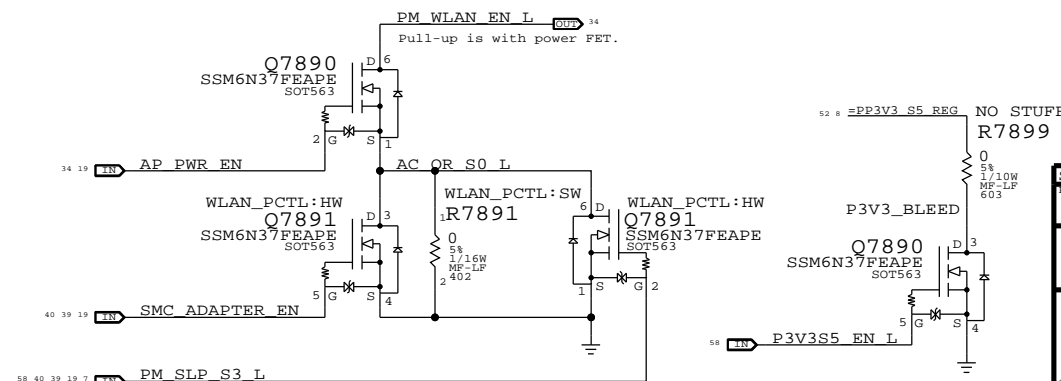
60Hz


3-Phase

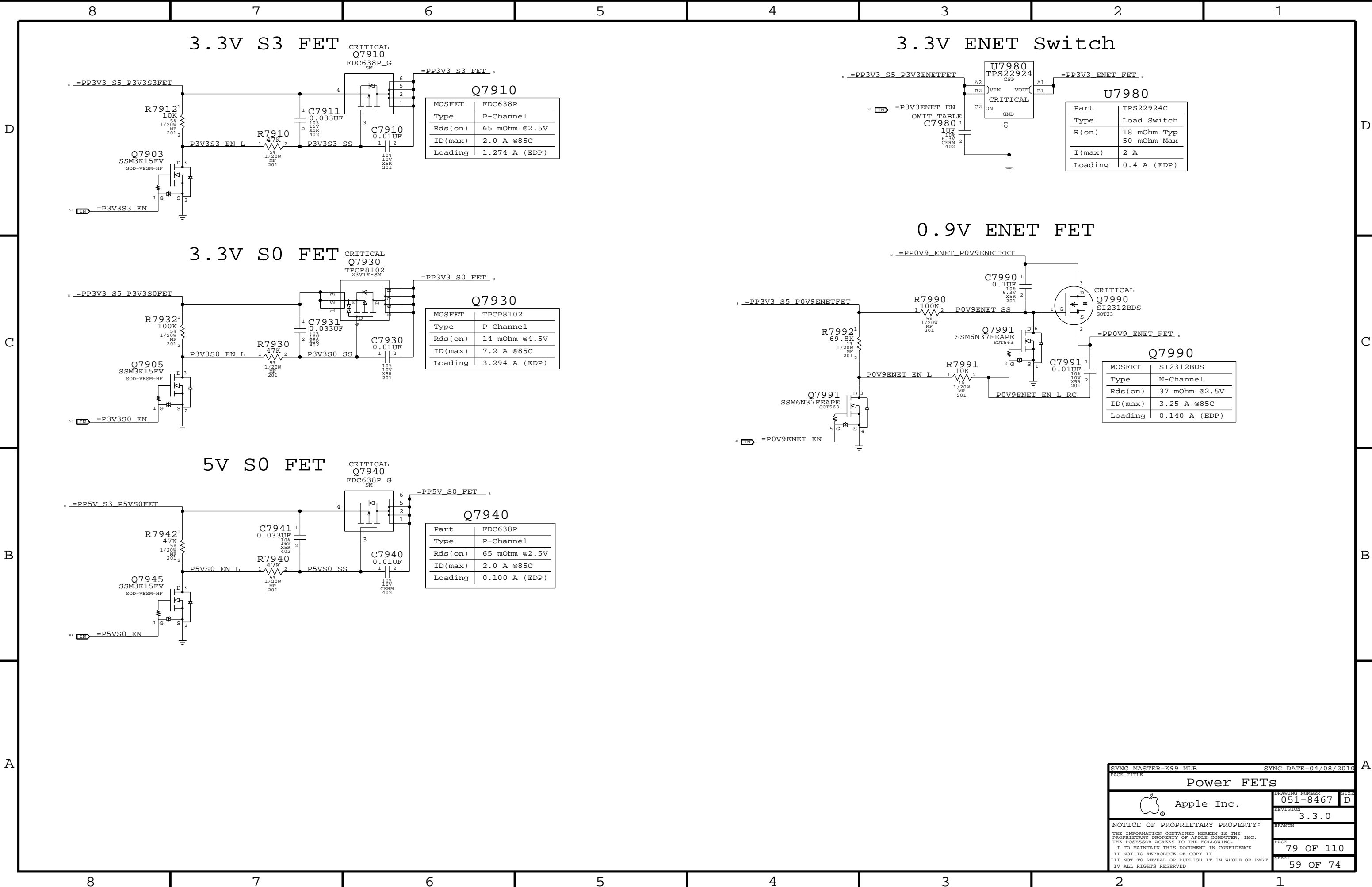
```
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
```

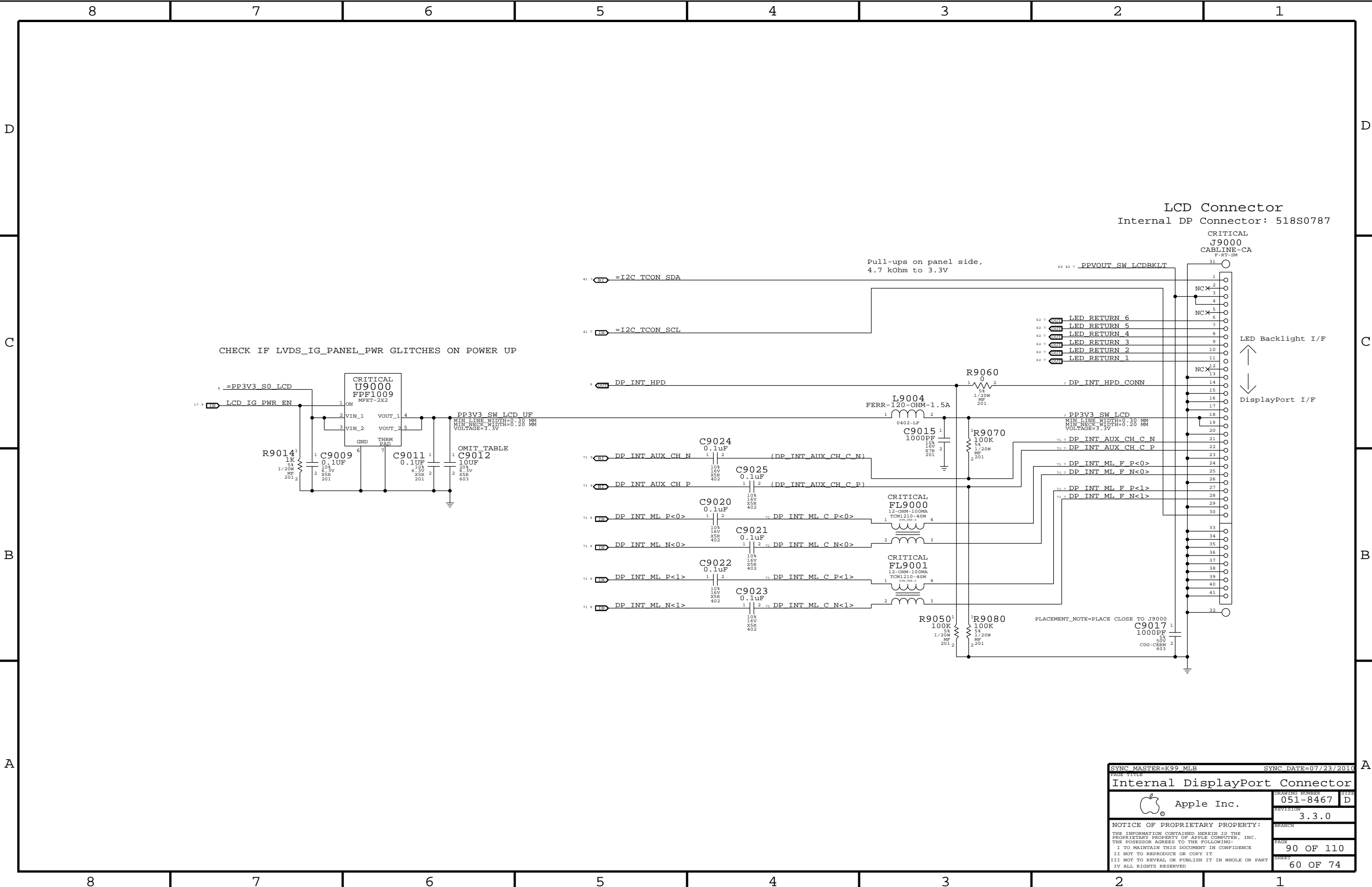
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

NOTE: "AC" term valid only when Q7891 is stuffed



SYNCH MASTER=K99 MLB		SYNCH DATE=04/08/2010	
PAGE TITLE			
Power Sequencing			
 Apple Inc.		DRAWING NUMBER	SIZE
		051-8467	D
		REVISION	
		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		78 OF 110	
		SHEET	
		58 OF 74	






LCD Connector
Internal DP Connector: 518S0787

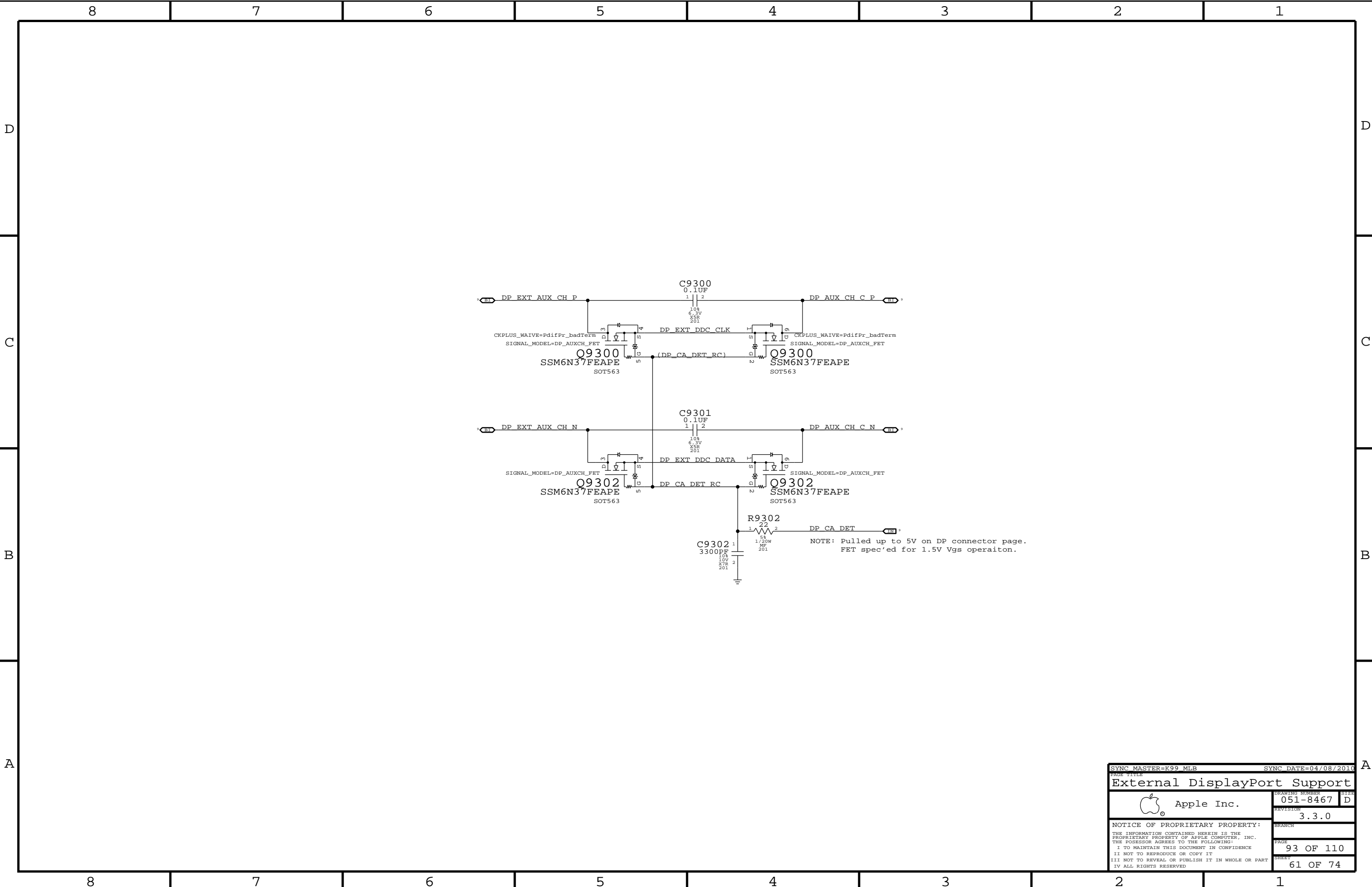
CRITICAL
J9000
CABLINE-CA
P-RT-SM

Pull-ups on panel side,
4.7 kOhm to 3.3V

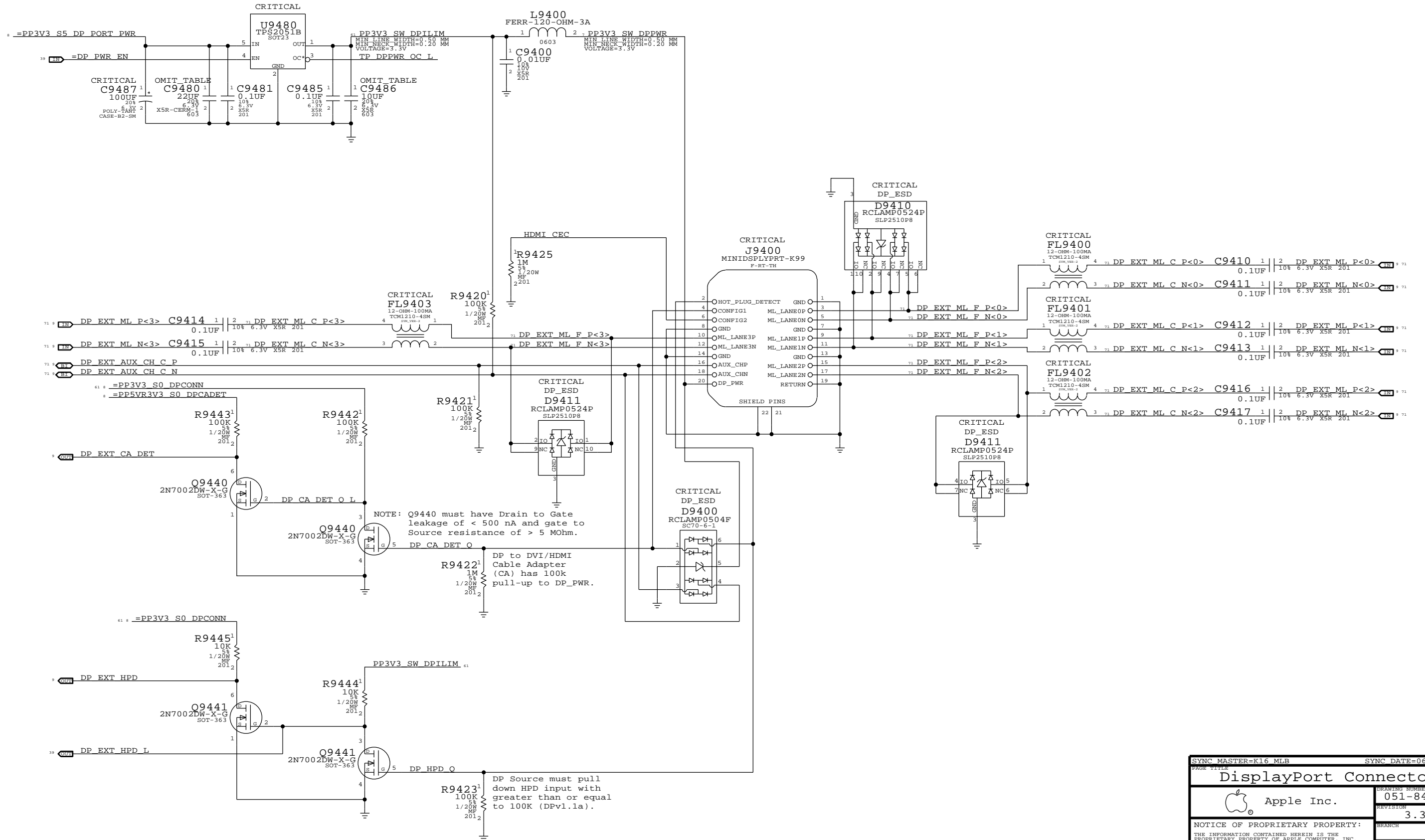
CHECK IF LVDS_IG_PANEL_PWR GLITCHES ON POWER UP


LED Backlight I/F
↑
↓
DisplayPort I/F

SYNC MASTER=K99 MLB		SYNC DATE=07/23/2010	
PAGE TITLE			
Internal DisplayPort Connector			
 Apple Inc.		DRAWING NUMBER	051-8467
		REVISION	3.3.0
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	90 OF 110
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	60 OF 74
II NOT TO REPRODUCE OR COPY IT			
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART			
IV ALL RIGHTS RESERVED			



Port Power Switch



SYNC MASTER=K16 MLB		SYNC DATE=06/01/2010	
PAGE TITLE			
DisplayPort Connector			
 Apple Inc.		DRAWING NUMBER	051-8467
		SIZE	D
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED		REVISION	3.3.0
		BRANCH	
		PAGE	94 OF 110
		SHEET	62 OF 74

D

C

B

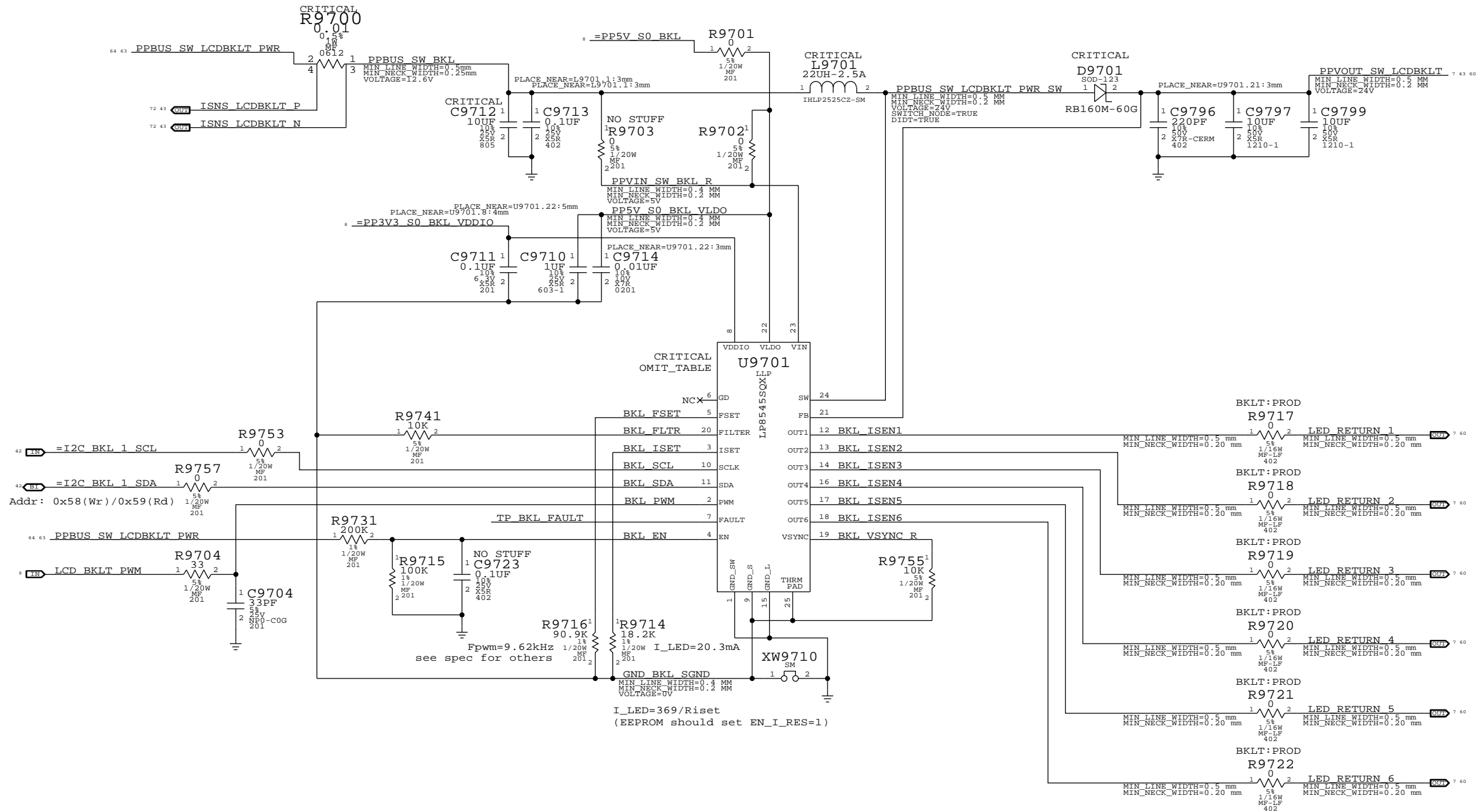
A

D

C

B


A

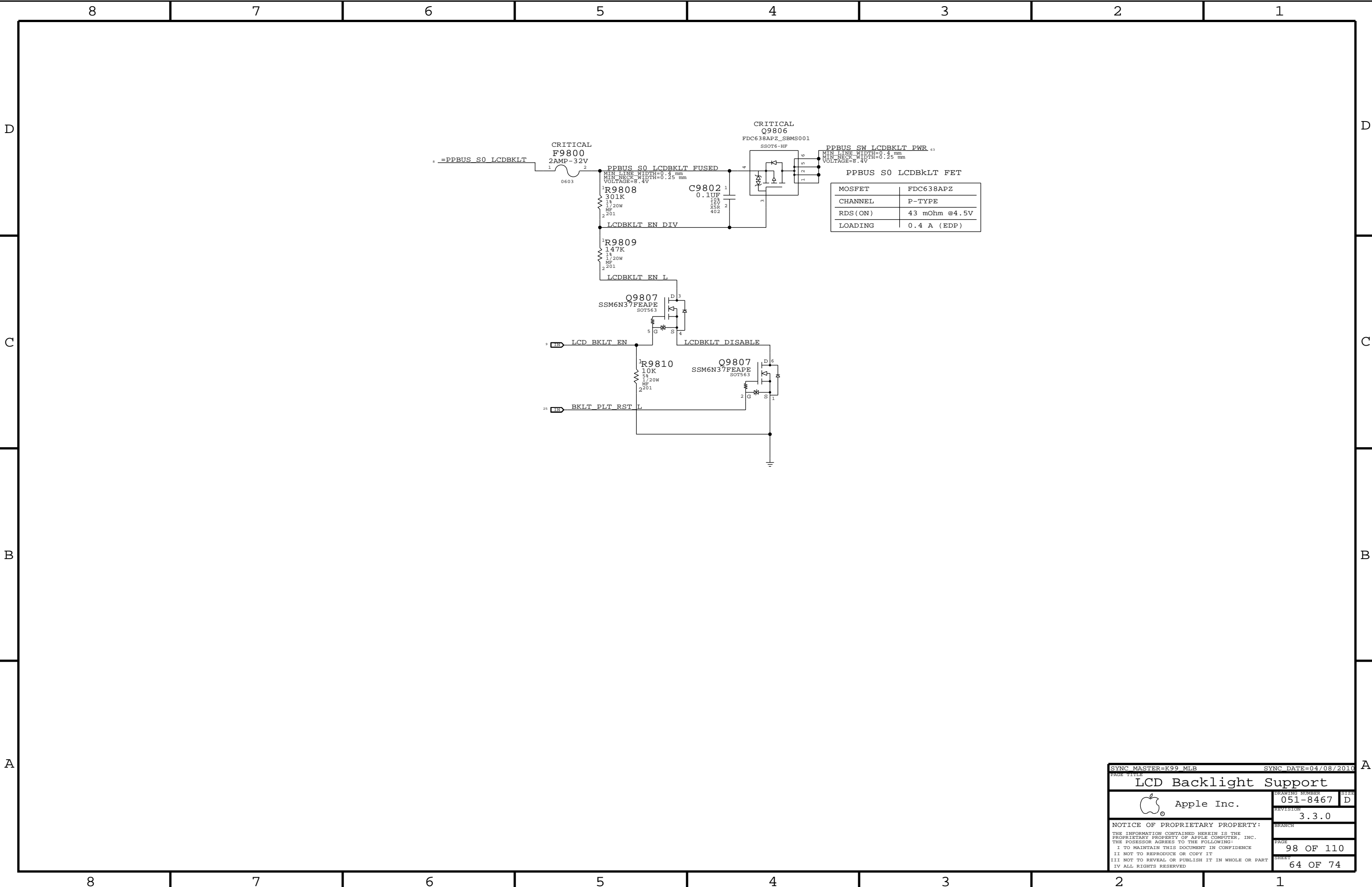


FOR LP8543:
STUFF R9741
NO STUFF R9740, C9740, C9741, R9754

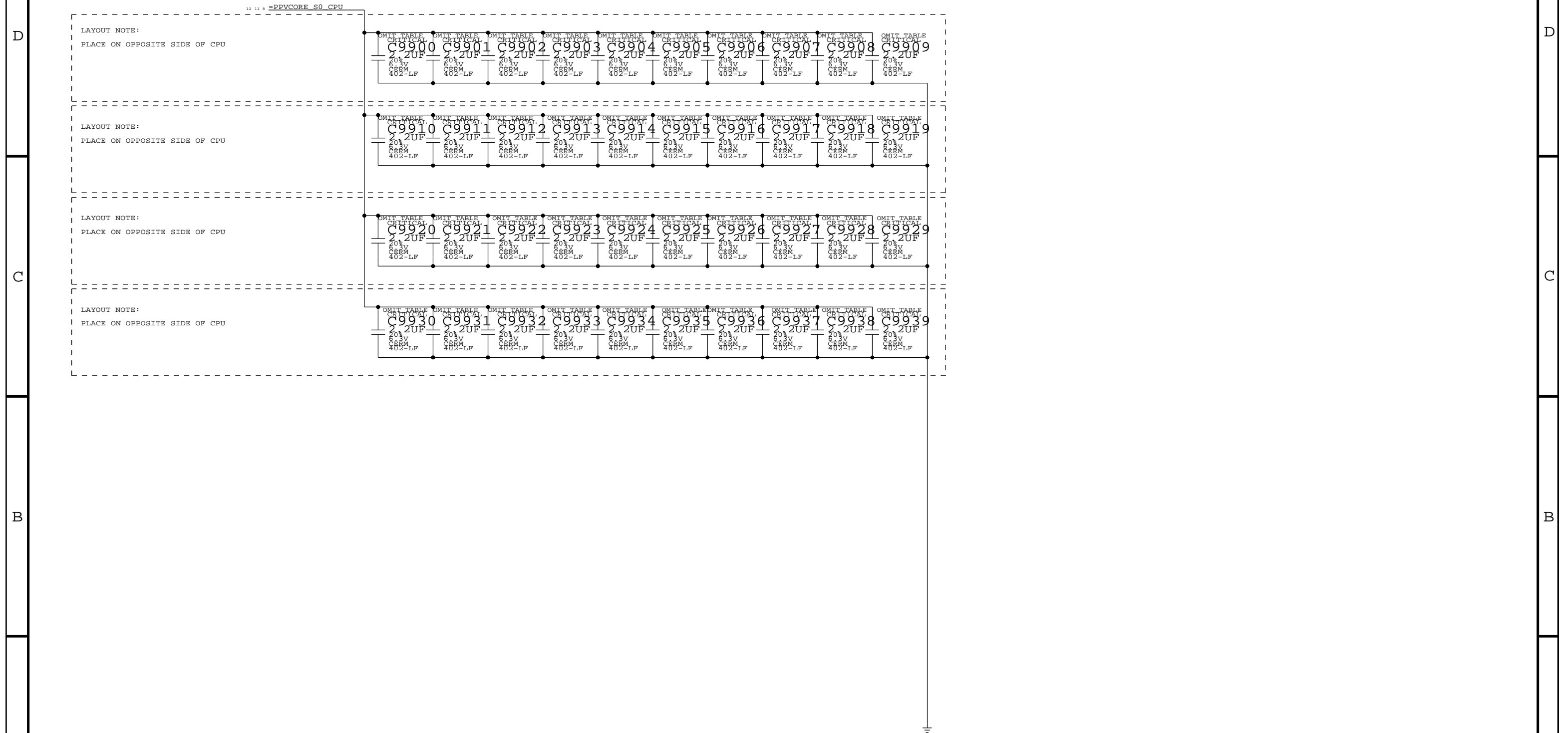
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
353S2896	1	IC,LP8545,LED BKLT CTRLR,PRODUCTIO,LLP24	U9701	CRITICAL	PROJ:K16
353S2967	1	IC,LP8545,LED BKLT CTRLR,LLP24,K99 VER	U9701	CRITICAL	PROJ:K99


10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=(K99 MLB)		SYNC DATE=(03/01/2010)	
PAGE TITLE			
LCD Backlight Driver		DRAWING NUMBER	
	Apple Inc.	051-8467	D
		REVISION	
		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		97 OF 110	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		63 OF 74	
IV ALL RIGHTS RESERVED			



ADDITIONAL CPU VCORE HF DECOUPLING
40x 1uF 0402



SYNC MASTER=K99 MLB PAGE 1 OF 1		SYNC DATE=05/18/2010 PAGE 1 OF 1	
Additional CPU/GPU Decoupling			
 Apple Inc.		DRAWING NUMBER 051-8467	SIZE D
		REVISION 3.3.0	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE I NOT TO REPRODUCE OR COPY IT I NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART I ALL RIGHTS RESERVED		BRANCH	PAGE 99 OF 110
		SHEET 65 OF 74	

D

B

A

WWW.AliSaler.Com

A

A

A

A

D

C

B

A

A

D

CB

B

D

CB

B

D

A

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_QS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_QDS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_QDS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_QDS	MEM_CLK	*	MEM_QDS2MEM
MEM_QDS	MEM_CTRL	*	MEM_QDS2MEM
MEM_QDS	MEM_CMD	*	MEM_QDS2MEM
MEM_QDS	MEM_DATA	*	MEM_QDS2MEM
MEM_QDS	MEM_QDS	*	MEM_QDS2MEM

DDR3:

DQ signals should be matched within 5 ps of associated QDS pair.
QDS intra-pair matching should be within 1 ps, inter-pair matching should be within 360 ps
No QDS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
CMD/CTRL signals should be matched within 150 ps.
All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD


SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

MEM_A/B_CKE EC SET NAME IS CHANGED ON K6, CANNOT SYNC THIS PAGE FROM T27

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>	9 15 26 27 32
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>	9 15 26 27 32
MEM_A_CKE	MEM_50S	MEM_CTRL	MEM A CKE<3..0>	15 21 26 27 32
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A CS L<3..0>	15 26 27 32
MEM_A_CNTRL	MEM_50S	MEM_CTRL	MEM A ODT<3..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A A<15..0>	9 15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A BA<2..0>	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A RAS L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A CAS L	15 26 27 32
MEM_A_CMD	MEM_50S	MEM_CMD	MEM A WE L	15 26 27 32
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>	15 27
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DM<0>	15 26
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DM<1>	15 26
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DM<2>	15 26
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DM<3>	15 26
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DM<4>	15 27
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DM<5>	15 27
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DM<6>	15 27
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DM<7>	15 27
MEM_A_QDS0	MEM_70D	MEM_QDS	MEM A QDS P<0>	15 26
MEM_A_QDS0	MEM_70D	MEM_QDS	MEM A QDS N<0>	15 26
MEM_A_QDS1	MEM_70D	MEM_QDS	MEM A QDS P<1>	15 26
MEM_A_QDS1	MEM_70D	MEM_QDS	MEM A QDS N<1>	15 26
MEM_A_QDS2	MEM_70D	MEM_QDS	MEM A QDS P<2>	15 26
MEM_A_QDS2	MEM_70D	MEM_QDS	MEM A QDS N<2>	15 26
MEM_A_QDS3	MEM_70D	MEM_QDS	MEM A QDS P<3>	15 26
MEM_A_QDS3	MEM_70D	MEM_QDS	MEM A QDS N<3>	15 26
MEM_A_QDS4	MEM_70D	MEM_QDS	MEM A QDS P<4>	15 27
MEM_A_QDS4	MEM_70D	MEM_QDS	MEM A QDS N<4>	15 27
MEM_A_QDS5	MEM_70D	MEM_QDS	MEM A QDS P<5>	15 27
MEM_A_QDS5	MEM_70D	MEM_QDS	MEM A QDS N<5>	15 27
MEM_A_QDS6	MEM_70D	MEM_QDS	MEM A QDS P<6>	15 27
MEM_A_QDS6	MEM_70D	MEM_QDS	MEM A QDS N<6>	15 27
MEM_A_QDS7	MEM_70D	MEM_QDS	MEM A QDS P<7>	15 27
MEM_A_QDS7	MEM_70D	MEM_QDS	MEM A QDS N<7>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>	9 15 28 29 32
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>	9 15 28 29 32
MEM_B_CKE	MEM_50S	MEM_CTRL	MEM B CKE<3..0>	15 21 28 29 32
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B CS L<3..0>	15 28 29 32
MEM_B_CNTRL	MEM_50S	MEM_CTRL	MEM B ODT<3..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B A<15..0>	9 15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B BA<2..0>	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B RAS L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B CAS L	15 28 29 32
MEM_B_CMD	MEM_50S	MEM_CMD	MEM B WE L	15 28 29 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DM<7>	15 29
MEM_B_QDS0	MEM_70D	MEM_QDS	MEM B QDS P<0>	15 28
MEM_B_QDS0	MEM_70D	MEM_QDS	MEM B QDS N<0>	15 28
MEM_B_QDS1	MEM_70D	MEM_QDS	MEM B QDS P<1>	15 28
MEM_B_QDS1	MEM_70D	MEM_QDS	MEM B QDS N<1>	15 28
MEM_B_QDS2	MEM_70D	MEM_QDS	MEM B QDS P<2>	15 28
MEM_B_QDS2	MEM_70D	MEM_QDS	MEM B QDS N<2>	15 28
MEM_B_QDS3	MEM_70D	MEM_QDS	MEM B QDS P<3>	15 28
MEM_B_QDS3	MEM_70D	MEM_QDS	MEM B QDS N<3>	15 28
MEM_B_QDS4	MEM_70D	MEM_QDS	MEM B QDS P<4>	15 29
MEM_B_QDS4	MEM_70D	MEM_QDS	MEM B QDS N<4>	15 29
MEM_B_QDS5	MEM_70D	MEM_QDS	MEM B QDS P<5>	15 29
MEM_B_QDS5	MEM_70D	MEM_QDS	MEM B QDS N<5>	15 29
MEM_B_QDS6	MEM_70D	MEM_QDS	MEM B QDS P<6>	15 29
MEM_B_QDS6	MEM_70D	MEM_QDS	MEM B QDS N<6>	15 29
MEM_B_QDS7	MEM_70D	MEM_QDS	MEM B QDS P<7>	15 29
MEM_B_QDS7	MEM_70D	MEM_QDS	MEM B QDS N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	15

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
Memory Constraints			
 Apple Inc.	DRAWING NUMBER	051-8467	SIZE D
	REVISION	3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		101 OF 110	
II NOT TO REPRODUCE OR COPY IT		SHEET	
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART		67 OF 74	
IV ALL RIGHTS RESERVED			

8

7

6

5

4

3

2

1

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_90D	PCIE	PEG R2D P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C P<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R C N<15..0>
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D P
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D P
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R C P
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R C N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D P
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R C P
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R C N
MCP_PE0_BECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
MCP_PE0_BECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PE1_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
MCP_PE1_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PE2_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
MCP_PE2_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PE3_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
MCP_PE3_BECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP	MCP_PEX_COMP	MCP_PEX_COMP	MCP PEX0 TERMP
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET	MCP_DAC_COMP	MCP_DAC_COMP	MCP TV_DAC RSET
MCP_DAC_VREF	MCP_DAC_COMP	MCP_DAC_COMP	MCP TV_DAC VREF
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 P<1..0>
DP_INT_ML	DP_90D	DISPLAYPORT	DP IG ML1 N<1..0>
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 P
DP_INT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH1 N
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML0 N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH0 N
MCP_TMDS0_RSET	MCP_DV_COMP		MCP TMDS0 RSET
MCP_TMDS0_VPROBE			MCP TMDS0 VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP IFPAB RSET
MCP_IFPAB_VPROBE			MCP IFPAB VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C N
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D P
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R C P
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D P
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C P
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERM		SATA_TERM	MCP SATA TERMP

8

7

6

5

4

3

2

1

WWW.AliSaler.Com

SYNC MASTER=K99 MLB

SYNC DATE=04/08/2010

MCP Constraints 1

Apple Inc.

DRAWING NUMBER

051-8467

SIZE

D

REVISION

3.3.0

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

- I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
- II NOT TO REPRODUCE OR COPY IT
- III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
- IV ALL RIGHTS RESERVED

BRANCH

PAGE

102 OF 110

SHEET

68 OF 74

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5x_DIELECTRIC	?
CLK_LPC	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.7

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIA5	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.8

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.10

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=1.5x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.11

SPI Interface Constraints


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

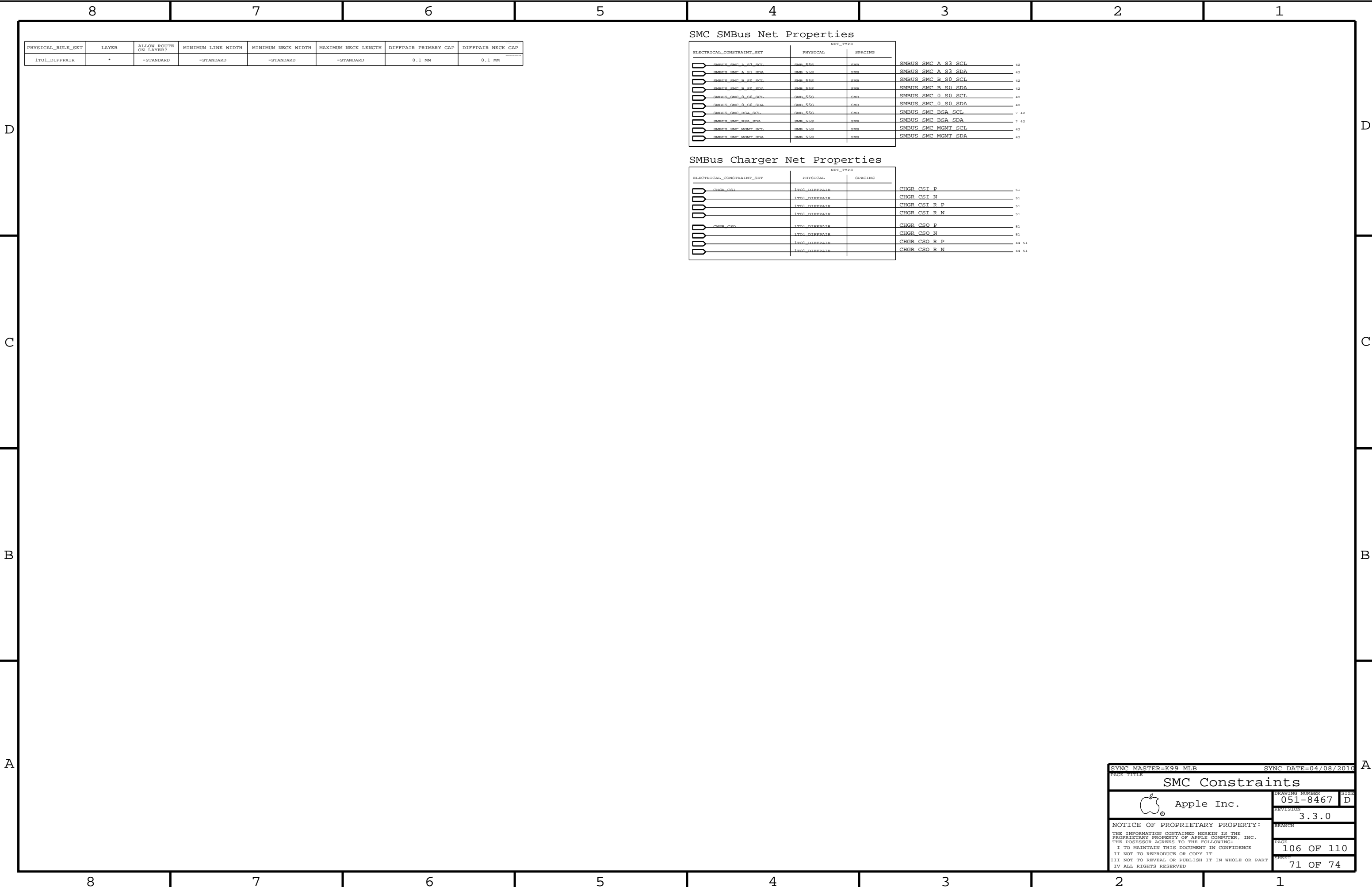
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	= 1.5x_DIELECTRIC	?


SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.12

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	LPC_AD	LPC_55S	LPC	LPC AD<3...0>	7 19 39 41
	LPC_FRAME_L	LPC_55S	LPC	LPC FRAME_L	7 19 39 41
	LPC_RESET_L	LPC_55S	LPC	LPC RESET_L	19 25
	MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC_R	19 25
		CLK_LPC_55S	CLK_LPC	LPC CLK33M SMC	25 39
		CLK_LPC_55S	CLK_LPC	LPC CLK33M LPCPLUS	7 25 41
	USB_EXT_A	USB_90D	USB	USB EXT_A_P	18 36
		USB_90D	USB	USB EXT_A_N	18 36
		USB_90D	USB	USB EXT_A_MUXED_P	16 72
		USB_90D	USB	USB EXT_A_MUXED_N	16 72
	USB_MINI	USB_90D	USB	USB MINI_P	6 18
		USB_90D	USB	USB MINI_N	6 18
	USB_EXTD	USB_90D	USB	USB EXT_D_P	7 18 37
		USB_90D	USB	USB EXT_D_N	7 18 37
	USB_CAMERA	USB_90D	USB	USB CAMERA_P	7 18 37
		USB_90D	USB	USB CAMERA_N	7 18 37
	USB_RT	USB_90D	USB	USB BT_P	7 18 34
		USB_90D	USB	USB BT_N	7 18 34
	USB_TPAD	USB_90D	USB	USB TPAD_P	18 47 72
		USB_90D	USB	USB TPAD_N	18 47 72
	USB_IR	USB_90D	USB	USB IR_P	
		USB_90D	USB	USB IR_N	
	USB_EXTB	USB_90D	USB	USB EXT_B_P	
		USB_90D	USB	USB EXT_B_N	
	USB_T57	USB_90D	USB	USB T57_P	
		USB_90D	USB	USB T57_N	
	USB_EXTC	USB_90D	USB	USB EXT_C_P	9 18
		USB_90D	USB	USB EXT_C_N	9 18
	USB_SDCARD	USB_90D	USB	USB SDCARD_P	18 38
		USB_90D	USB	USB SDCARD_N	18 38
	USB_WM	USB_90D	USB	USB WM_P	
		USB_90D	USB	USB WM_N	
	MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	18
	SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS MCP_0_CLK	19 42
	SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS MCP_0_DATA	19 42
	(SMBUS_SMC_MGMT_SCL)	SMB_55S	SMB	SMBUS MCP_1_CLK	19 42
	(SMBUS_SMC_MGMT_SDA)	SMB_55S	SMB	SMBUS MCP_1_DATA	19 42
	HDA_BIT_CLK	HDA_55S	HDA	HDA BIT_CLK	7 19 37
		HDA_55S	HDA	HDA BIT_CLK_R	19
	HDA_SYNC	HDA_55S	HDA	HDA SYNC	7 19 37
		HDA_55S	HDA	HDA SYNC_R	19
	HDA_RST_L	HDA_55S	HDA	HDA RST_R_L	19
		HDA_55S	HDA	HDA RST_L	7 19 37
	HDA_SDIN0	HDA_55S	HDA	HDA SDIN0	7 19 37
		HDA_55S	HDA	HDA SDIN_CODEC	
	HDA_SDOIT	HDA_55S	HDA	HDA SDOUT	7 19 37
		HDA_55S	HDA	HDA SDOUT_R	19
	MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	19
	MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	19 25
		CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	25 39
	SPI_CLK	SPI_55S	SPI	SPI_CLK_R	19 41
		SPI_55S	SPI	SPI_CLK	41
	SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	19 41
		SPI_55S	SPI	SPI_MOSI	41
	SPI_MISO	SPI_55S	SPI	SPI_MISO	19 41
	SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	19 41
		SPI_55S	SPI	SPI_CS0_L	41
		SPI_55S	SPI	SPI_MLB_CLK	41 48
		SPI_55S	SPI	SPI_MLB_MOSI	41 48
		SPI_55S	SPI	SPI_MLB_MISO	41 48
		SPI_55S	SPI	SPI_MLB_CS_L	41 48
		SPI_55S	SPI	SPI_ALT_CLK	7 41
		SPI_55S	SPI	SPI_ALT_MOSI	7 41
		SPI_55S	SPI	SPI_ALT_MISO	7 41
		SPI_55S	SPI	SPI_ALT_CS_L	7 41

SYNC MASTER=K99 MLB		SYNC DATE=04/08/2010	
PAGE TITLE			
MCP Constraints 2			
	DRAWING NUMBER		SIZE
	051-8467		D
	REVISION		
Apple Inc.		3.3.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			
		PAGE	103 OF 110
		SHEET	69 OF 74



8	7	6	5	4	3	2	1
K99 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM				NO_TYPE,BGA		MM	15.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.100 MM	0.076 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
27P4_OHM_SE	ISL3,ISL10	Y	0.250 MM	0.250 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.250 MM	0.250 MM			
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.140 MM	0.140 MM			
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.090 MM	0.090 MM			
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	ISL3,ISL4,ISL9,ISL10	Y	0.076 MM	0.076 MM			
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.135 MM	0.135 MM		0.130 MM	0.130 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.155 MM	0.155 MM		0.130 MM	0.130 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.160 MM	0.160 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.125 MM	0.125 MM		0.160 MM	0.160 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
75_OHM_DIFF	TOP,BOTTOM	Y	0.160 MM	0.160 MM		0.160 MM	0.160 MM
75_OHM_DIFF	ISL3,ISL10	Y	0.120 MM	0.120 MM		0.140 MM	0.140 MM
75_OHM_DIFF	ISL4,ISL9	Y	0.140 MM	0.140 MM		0.140 MM	0.140 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
95_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
95_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL3,ISL10	Y	0.089 MM	0.089 MM		0.210 MM	0.210 MM
95_OHM_DIFF	ISL4,ISL9	Y	0.105 MM	0.105 MM		0.210 MM	0.210 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL3,ISL10	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM
100_OHM_DIFF	ISL4,ISL9	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	
DEFAULT				*	0.1 MM	?	
STANDARD				*	=DEFAULT	?	
BGA_P1MM				*	0.1 MM	?	
BGA_P2MM				*	0.2 MM	?	
BGA_P3MM				*	0.3 MM	?	
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	
1:1_SPACING				*	0.1 MM	?	
1.5:1_SPACING				*	0.15 MM	?	
1.8:1_SPACING				*	0.18 MM	?	
2:1_SPACING				*	0.2 MM	?	
2.28:1_SPACING				*	0.228 MM	?	
2.5:1_SPACING				*	0.25 MM	?	
3:1_SPACING				*	0.3 MM	?	
4:1_SPACING				*	0.4 MM	?	
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	
GND				*	=STANDARD	?	
PPIV5_MEM				*	=STANDARD	?	
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	
GND_P2MM				*	0.2 MM	1000	
PWR_P2MM				*	0.2 MM	1000	
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	
NB_STATIC				*	=STANDARD	?	
SPACING_RULE_SET				LAYER	LINE-TO-LINE SPACING	WEIGHT	
2X_DIELECTRIC				*	0.140 MM	?	
3X_DIELECTRIC				*	0.210 MM	?	
4X_DIELECTRIC				*	0.280 MM	?	
1.5X_DIELECTRIC				*	0.105 MM	?	
5X_DIELECTRIC				*	0.350 MM	?	
SYNC MASTER=K99_MLB SYNC DATE=04/08/2010							
K99 RULE DEFINITIONS							
 Apple Inc.				DRAWING NUMBER		SIZE	
				051-8467		D	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED				REVISION		BRANCH	
				3.3.0			
				PAGE		SHEET	
				109 OF 110		73 OF 74	

8

7

6

5

4

3

2

1

1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7460	CRITICAL	SS_CAP_1UF	138S0628	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7460	CRITICAL	MU_CAP_1UF	138S0630	2	CAP, 1UF, 6.3V, 10%, 0402	C7203,C7460	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1268,C1269,C1270,C1271,C1272,C1273,C1274,C1275	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1268,C1269,C1270,C1271,C1272,C1273,C1274,C1275	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1268,C1269,C1270,C1271,C1272,C1273,C1274,C1275	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1276,C1277,C1278,C1279,C1280,C1281,C1282,C1283	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1276,C1277,C1278,C1279,C1280,C1281,C1282,C1283	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1276,C1277,C1278,C1279,C1280,C1281,C1282,C1283	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1284,C1285,C1286,C1287,C1288,C1289,C1290,C1291	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1284,C1285,C1286,C1287,C1288,C1289,C1290,C1291	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1284,C1285,C1286,C1287,C1288,C1289,C1290,C1291	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1292,C1293,C1294,C1295,C1296,C1297,C1298,C1299	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1292,C1293,C1294,C1295,C1296,C1297,C1298,C1299	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1292,C1293,C1294,C1295,C1296,C1297,C1298,C1299	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1300,C1301,C1302,C1303,C1304,C1305,C1306,C1307	CRITICAL	TY_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1308,C1309,C1310,C1311,C1312,C1313,C1314,C1315	CRITICAL	SS_CAP_2_2UF	138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1308,C1309,C1310,C1311,C1312,C1313,C1314,C1315	CRITICAL	MU_CAP_2_2UF	138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1308,C1309,C1310,C1311,C1312,C1313,C1314,C1315	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1316,C1317,C1318,C1319,C1320,C1321,C1322,C1323	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1316,C1317,C1318,C1319,C1320,C1321,C1322,C1323	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1316,C1317,C1318,C1319,C1320,C1321,C1322,C1323	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1324,C1325,C1326,C1327,C1328,C1329,C1330,C1331	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1324,C1325,C1326,C1327,C1328,C1329,C1330,C1331	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1324,C1325,C1326,C1327,C1328,C1329,C1330,C1331	CRITICAL	TY_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1332,C1333,C1334,C1335,C1336,C1337,C1338,C1339	CRITICAL	SS_CAP_2_2UF	138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1332,C1333,C1334,C1335,C1336,C1337,C1338,C1339	CRITICAL	MU_CAP_2_2UF	138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1332,C1333,C1334,C1335,C1336,C1337,C1338,C1339	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1340,C1341,C1342,C1343,C1344,C1345,C1346,C1347	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1340,C1341,C1342,C1343,C1344,C1345,C1346,C1347	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1340,C1341,C1342,C1343,C1344,C1345,C1346,C1347	CRITICAL	TY_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1348,C1349,C1350,C1351,C1352,C1353,C1354,C1355	CRITICAL	SS_CAP_2_2UF	138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1348,C1349,C1350,C1351,C1352,C1353,C1354,C1355	CRITICAL	MU_CAP_2_2UF	138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1348,C1349,C1350,C1351,C1352,C1353,C1354,C1355	CRITICAL	TY_CAP_2_2UF
138S0632	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1356,C1357,C1358,C1359,C1360,C1361,C1362,C1363	CRITICAL	SS_CAP_2_2UF	138S0633	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1356,C1357,C1358,C1359,C1360,C1361,C1362,C1363	CRITICAL	MU_CAP_2_2UF	138S0634	9	CAP, 2.2UF, 6.3V, 20%, 0402	C1356,C1357,C1358,C1359,C1360,C1361,C1362,C1363	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	SS_CAP_10UF	138S0625	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	MU_CAP_10UF	138S0627	1	CAP, 10UF, 6.3V, 20%, 0603	C1280	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C2600,C2605,C2620,C2625,C2630,C2635,C2640,C2645	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C2600,C2605,C2620,C2625,C2630,C2635,C2640,C2645	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C2600,C2605,C2620,C2625,C2630,C2635,C2640,C2645	CRITICAL	TY_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C2650,C2655,C2660,C2665,C2670,C2675,C2680,C2685	CRITICAL	SS_CAP_10UF	138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C2650,C2655,C2660,C2665,C2670,C2675,C2680,C2685	CRITICAL	MU_CAP_10UF	138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C2650,C2655,C2660,C2665,C2670,C2675,C2680,C2685	CRITICAL	TY_CAP_10UF

22UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

MURATA

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0635	4	CAP, 22UF, 6.3V, 20%, 0603	C1230,C1234,C1237,C1238	CRITICAL	SS_CAP_22UF	138S0676	4	CAP, 22UF, 6.3V, 20%, 0603	C1230,C1234,C1237,C1238	CRITICAL	MU_CAP_22UF	138S0688	4	CAP, 22UF, 6.3V, 20%, 0603	C1230,C1234,C1237,C1238	CRITICAL	TY_CAP_22UF
138S0635	3	CAP, 22UF, 6.3V, 20%, 0603	C1229,C1228,C1227	CRITICAL	SS_CAP_22UF	138S0676	3	CAP, 22UF, 6.3V, 20%, 0603	C1229,C1228,C1227	CRITICAL	MU_CAP_22UF	138S0688	3	CAP, 22UF, 6.3V, 20%, 0603	C1229,C1228,C1227	CRITICAL	TY_CAP_22UF
138S0635	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	SS_CAP_22UF	138S0676	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	MU_CAP_22UF	138S0688	5	CAP, 22UF, 6.3V, 20%, 0603	C1230,C4902,C7360,C7361,C9480	CRITICAL	TY_CAP_22UF

8

7

6

5

4

3

2

1

SYNC MASTER=K16_MLB

SYNC DATE=06/01/2010

PAGE TITLE

Acoustic Cap BOM Config Tables

Apple Inc.

DRAWING NUMBER

051-8467

REVISION

3.3.0

BRANCH

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

PAGE

110 OF 110

SHEET

74 OF 74