1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

| REV | ECN | DESCRIPTION OF REVISION | CK APPD / DATE |
|---|---|---|---|
| | | | 2011-02-08 |

# K60 MLB

LAST_MODIFIED=Tue Feb 8 14:39:56 2011


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DRAWING
TITLE=K22
ABBREV=DRAWING
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DRAWING TITLE: SCH,K60,MLB

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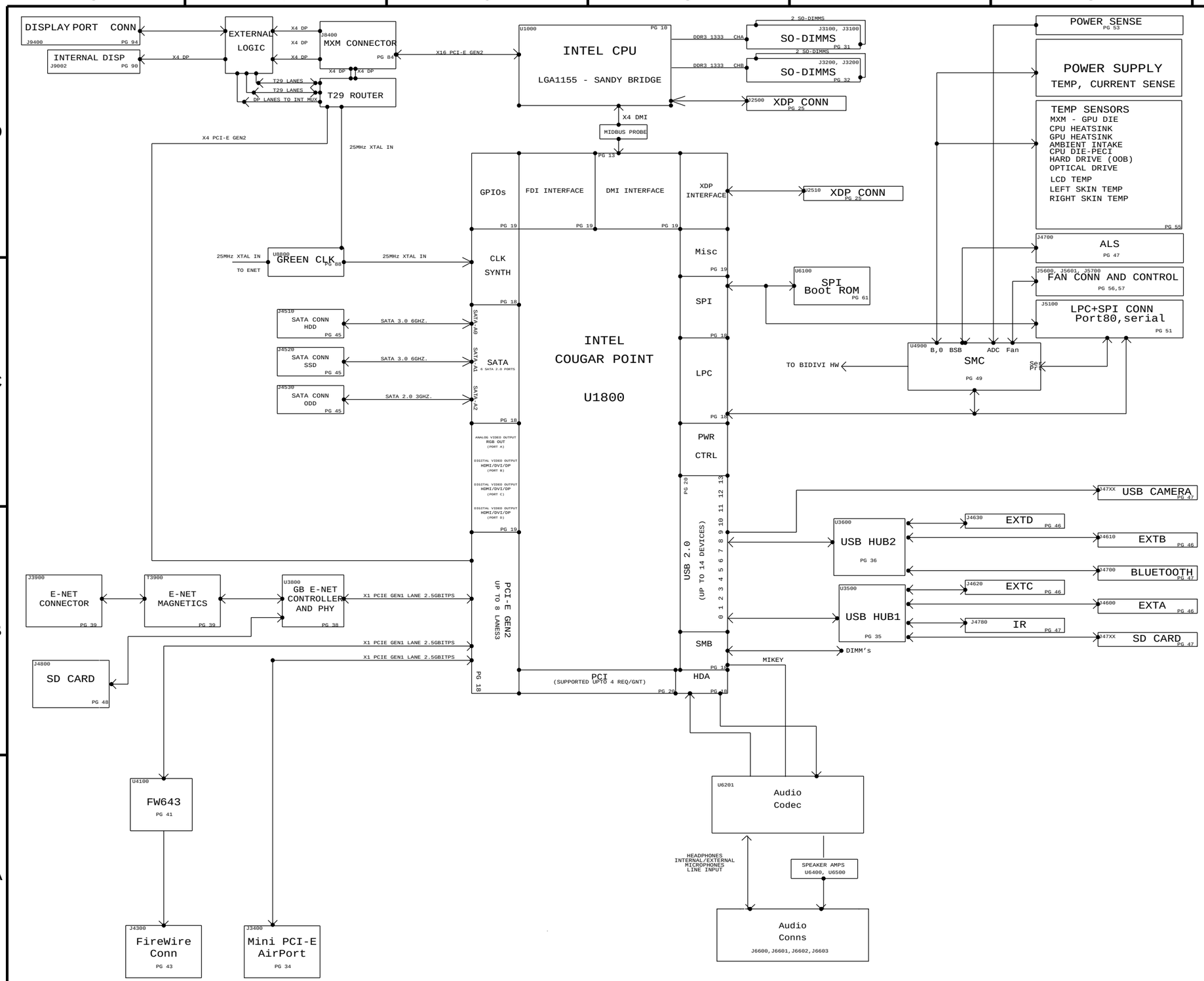


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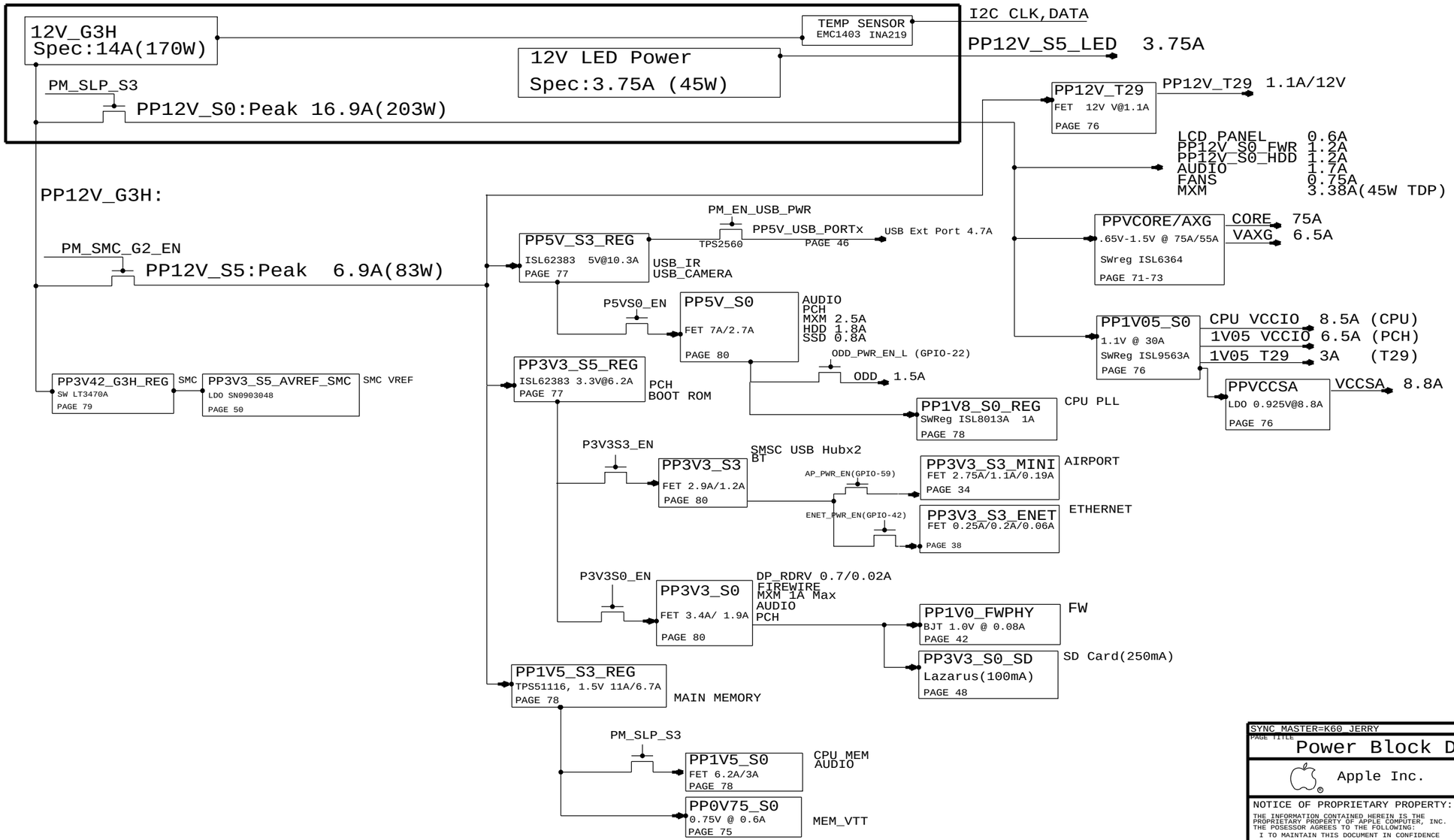
# AC/DC POWER SUPPLY (Spec:215W)

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## BOM Variants

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|---|---|---|
| 085-0801 | PCBA,MLB,DEV,K60 | DEVELOPMENT,DEV_GROUP |
| 639-1767 | PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD | K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG |
| 639-1820 | PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD | K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG |
| 639-1821 | PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD | K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,YES_DBG |
| 639-2160 | PCBA,MLB,K60,2.5G,4C,PRQ,P2_ODD,NO_DBG | K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG |
| 639-2159 | PCBA,MLB,K60,2.7G,4C,PRQ,P2_ODD,NO_DBG | K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG |
| 639-2161 | PCBA,MLB,K60,2.8G,4C,PRQ,P2_ODD,NO_DBG | K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P2,NO_DBG |
| 639-2118 | PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD | K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG |
| 639-2122 | PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD | K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG |
| 639-2119 | PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD | K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,YES_DBG |
| 639-2132 | PCBA,MLB,K60,2.5G,4C,PRQ,P1_ODD,NO_DBG | K60,2P5GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG |
| 639-2133 | PCBA,MLB,K60,2.7G,4C,PRQ,P1_ODD,NO_DBG | K60,2P7GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG |
| 639-2134 | PCBA,MLB,K60,2.8G,4C,PRQ,P1_ODD,NO_DBG | K60,2P8GHZ_SNB_CPU_PRQ,BASIC1,BASIC2,CPUVCORE-3PH,ODD_SATA:P1,NO_DBG |

## BOM GROUPS

| BOM GROUP | BOM OPTIONS |
|---|---|
| BASIC1 | COMMON,ALTERNATE,MXM,FCIM,CPU_1V5_SENSE,CPU_VCCSA_SENSE,1V05_PCH_SENSE,HUB_USX2061,PRODUCTION,VAXG,SSD |
| BASIC2 | AP,BT,IR,T29 |
| DEV_GROUP | VREFMRGN_A,VREFMRGN_B,DIMM_1V5_SENSE |
| YES_DBG | XDP,XDP_CONN,XDP_CPU_BPM,MOJOMUX:YES,LPCPLUS:YES |
| NO_DBG | MOJOMUX:NO,LPCPLUS:NO |

## CPU SOCKET & ILM SUB-BOMS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 511S0071 | 1 | SOCKET,LGA1155,CPU-LF | U1000 | CRITICAL | TYCO_SOCKET |
| 604-1474 | 1 | ASSY,PURCHASED,ILM,TYCO | ILM | CRITICAL | TYCO_SOCKET |
| 511S0073 | 1 | SOCKET,LGA1155,CPU-LF | U1000 | CRITICAL | MOLEX_SOCKET |
| 604-1161 | 1 | ASSY,PURCHASED,ILM,MOLEX | ILM | CRITICAL | MOLEX_SOCKET |

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|---|---|---|
| 085-2452 | SUB ASSY,CPU SOCKET,K60,TYCO | TYCO_SOCKET |
| 085-2453 | SUB ASSY,CPU SOCKET,K60,MOLEX | MOLEX_SOCKET |

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 085-2452 | 1 | TYCO CPU SOCKET AND ILM | SKT_ILM | CRITICAL | |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 085-2453 | 085-2452 | | SKT_ILM | MOLEX ALTERNATE |

## BOARD STACK-UP

| | |
|---|---|
| TOP | SIGNAL |
| 2 | GROUND |
| 3 | SIGNAL |
| 4 | POWER |
| 5 | POWER |
| 6 | SIGNAL |
| 7 | GROUND |
| BOTTOM | SIGNAL |

## COMMON

| | PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|---|
| | 337S4088 | 1 | IC,COUGAR POINT,SLJ4F,BD82Z68,PRQ,B3 | U1800 | CRITICAL | |
| | 353S3055 | 1 | IC,PI3VEDP212,X2 DP MUX,QFN | U9390 | CRITICAL | |
| | 338S0753 | 1 | IC,FW643,1394B_PCIE,PHY/LINK | U4100 | CRITICAL | |
| | 825-7122 | 1 | MLB LABEL,48.0X4.8 | X14 | CRITICAL | |
| | 343S0534 | 1 | IC,BCM57765,ENET&SD,8X8 | U3900 | CRITICAL | |
| RAW: 335S0807 | 341T0184 | 1 | FLASH,EFI BOOTROM,K60/K62 | U6100 | CRITICAL | |
| RAW: 335S0539 | 341T0328 | 1 | SFLASH ENET 2MBIT,CIV | U3990 | CRITICAL | |
| | 338S0945 | 1 | T29 ROUTER, IC ASSP | U9700 | CRITICAL | T29 |
| RAW: 335S0550 | 341T0257 | 1 | IC,T29,SERIAL EEPROM | U9790 | CRITICAL | T29 |
| RAW: 337S3997 | 341T0326 | 1 | IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25 | U9330 | CRITICAL | T29 |
| RAW: 335S0709 | 341T0330 | 1 | IC,MXM SYS ROM,24C02 | U8570 | CRITICAL | |
| RAW: 338S0878 | 341T0185 | 1 | IC,SMC,K60 | U4900 | CRITICAL | K60 |

## CPUS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 337S4043 | 1 | SNB,SR00S,PRQ,D2,2.5,65W,4+1,6M,LGA | CPU | CRITICAL | 2P5GHZ_SNB_CPU_PRQ |
| 337S4062 | 1 | SNB,SR009,PRQ,D2,2.7,65W,4+1,6M,LGA | CPU | CRITICAL | 2P7GHZ_SNB_CPU_PRQ |
| 337S4061 | 1 | SNB,SR00E,PRQ,D2,2.8,65W,4+1,8M,LGA | CPU | CRITICAL | 2P8GHZ_SNB_CPU_PRQ |

## K60 PARTS

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 051-8115 | 1 | SCH,MLB,K60 | SCH1 | | K60 |
| 820-2641 | 1 | PCBF,MLB,K60 | MLB1 | | K60 |

## K60 ALTERNATE PARTS

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 128S0298 | 128S0293 | | | 330UF |
| 371S0679 | 371S0652 | | | PIN DIODE |
| 377S0107 | 377S0066 | | | USB DIODE |
| 376S0972 | 376S0612 | | | ROHM TRA-BJT |

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BOM Configuration

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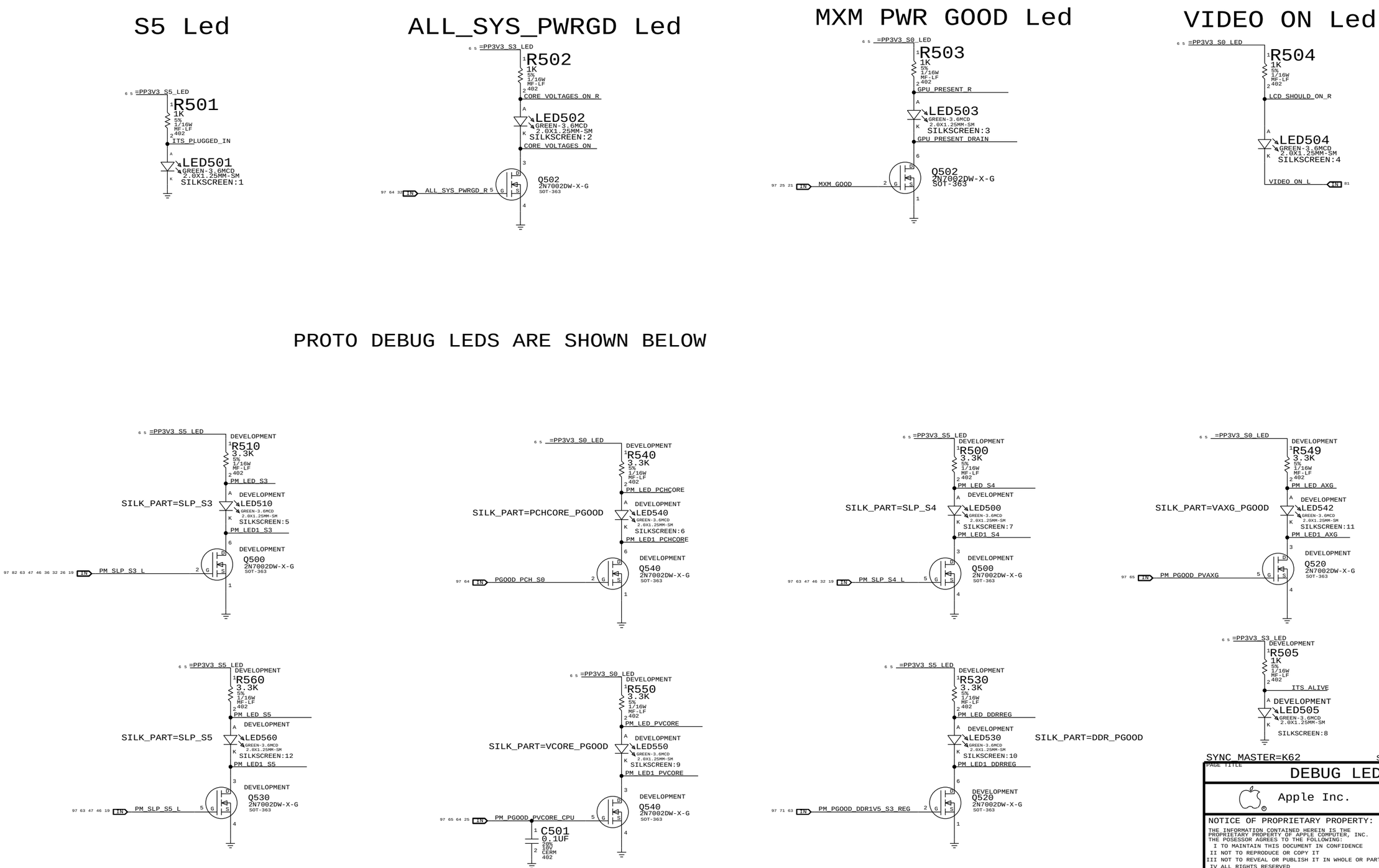
S5 Led
ALL_SYS_PWRGD Led
MXM PWR GOOD Led
VIDEO ON Led
PROTO DEBUG LEDS ARE SHOWN BELOW
=PP3V3_S5_LED
R501
1K
ITS_PLUGGED_IN
LED501
GREEN-3.6MCD
2.0X1.25MM-SM
SILKSCREEN:1
=PP3V3_S3_LED
R502
CORE_VOLTAGES_ON_R
LED502
SILKSCREEN:2
CORE_VOLTAGES_ON
ALL_SYS_PWRGD_R
Q502
2N7002DW-X-G
SOT-363
=PP3V3_S0_LED
R503
GPU_PRESENT_R
LED503
SILKSCREEN:3
GPU_PRESENT_DRAIN
MXM_GOOD
Q502
2N7002DW-X-G
SOT-363
=PP3V3_S0_LED
R504
LCD_SHOULD_ON_R
LED504
SILKSCREEN:4
VIDEO_ON_L
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DEVELOPMENT
R510
3.3K
PM_LED_S3
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LED510
SILKSCREEN:5
PM_LED1_S3
Q500
2N7002DW-X-G
PM_SLP_S3_L
=PP3V3_S0_LED
R540
PM_LED_PCHCORE
SILK_PART=PCHCORE_PGOOD
LED540
SILKSCREEN:6
PM_LED1_PCHCORE
Q540
PGOOD_PCH_S0
=PP3V3_S5_LED
R500
PM_LED_S4
SILK_PART=SLP_S4
LED500
SILKSCREEN:7
PM_LED1_S4
Q500
PM_SLP_S4_L
=PP3V3_S0_LED
R549
PM_LED_AXG
SILK_PART=VAXG_PGOOD
LED542
SILKSCREEN:11
PM_LED1_AXG
Q520
PM_PGOOD_PVAXG
=PP3V3_S5_LED
R560
PM_LED_S5
SILK_PART=SLP_S5
LED560
SILKSCREEN:12
PM_LED1_S5
Q530
PM_SLP_S5_L
=PP3V3_S0_LED
R550
PM_LED_PVCORE
SILK_PART=VCORE_PGOOD
LED550
SILKSCREEN:9
PM_LED1_PVCORE
Q540
PM_PGOOD_PVCORE_CPU
C501
0.1UF
=PP3V3_S5_LED
R530
PM_LED_DDRREG
LED530
SILKSCREEN:10
PM_LED1_DDRREG
SILK_PART=DDR_PGOOD
Q520
PM_PGOOD_DDR1V5_S3_REG
=PP3V3_S3_LED
R505
ITS_ALIVE
LED505
SILKSCREEN:8
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SYNC_DATE=01/06/2011
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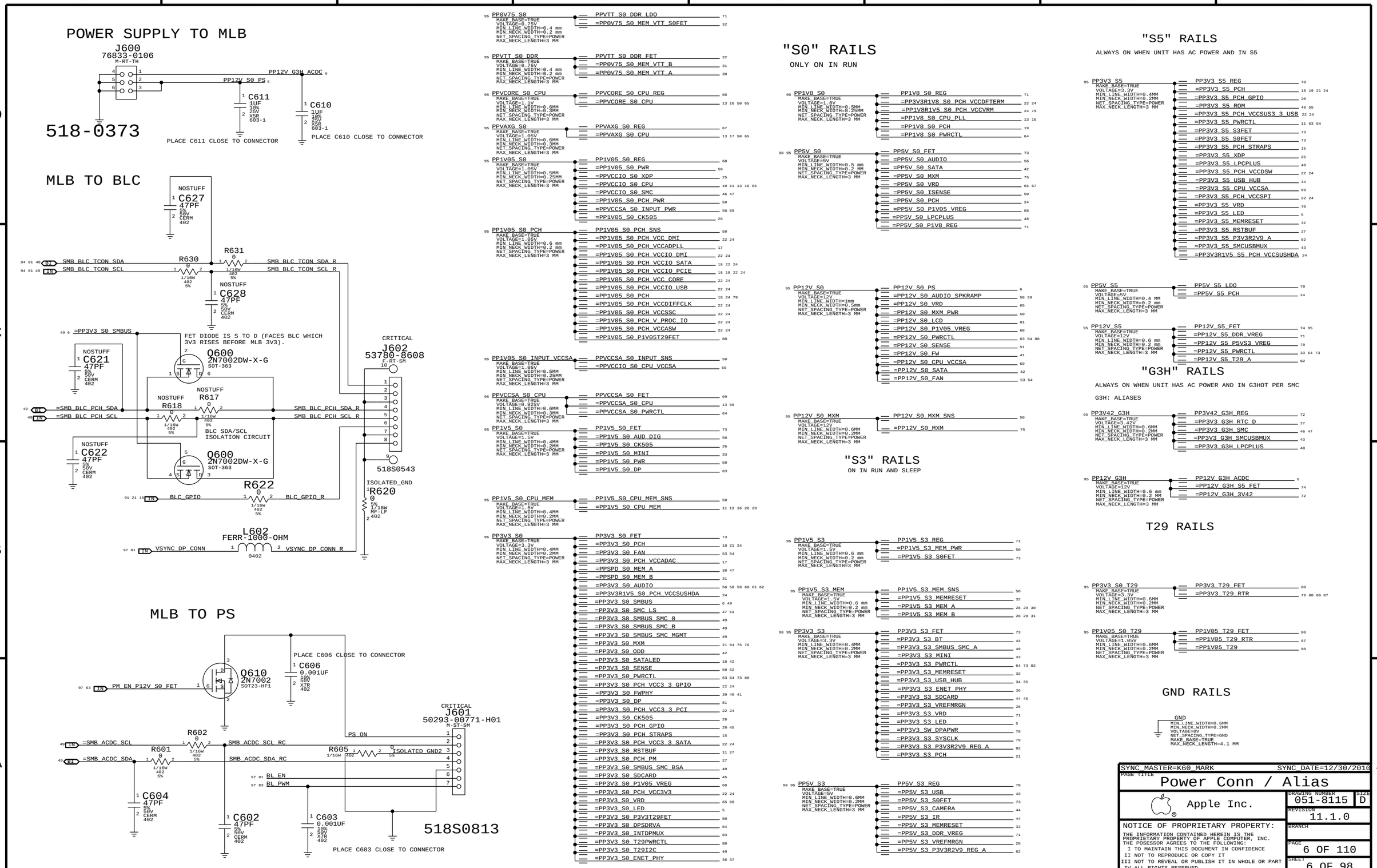


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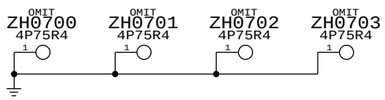
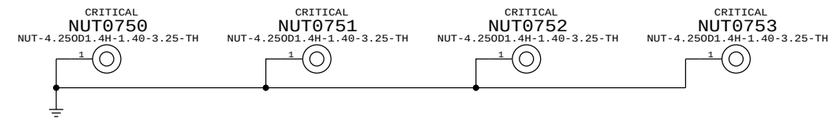
## CPU Heatsink

4mm Plated Holes (998-0850)



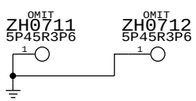

## DIMM CONNECTOR NUTS

Nuts (805-9582)



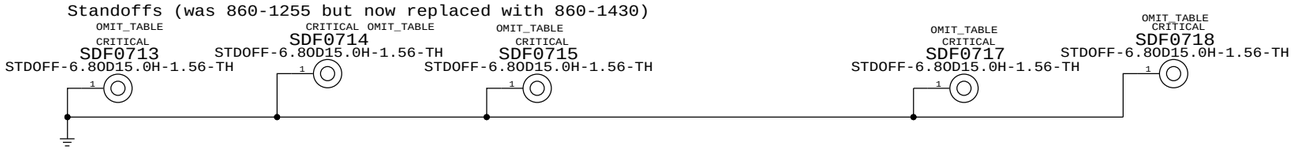

## PCH HEATSINK

MOUNTING HOLES (998-0873, 998-0976)




## Rear Cover

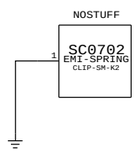
Standoffs (was 860-1255 but now replaced with 860-1430)



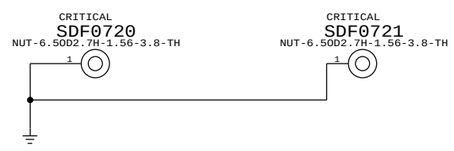

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 860-1430 | 5 | STANDOFF,MLB,K60/K62 | SDF0713,SDF0714,SDF0715,SDF0717,SDF0718 | |

## For EMC

EMC Spring (870-1577); Near DIMMs




MXM STANDOFFS (835-0272)




SYNC_MASTER=K74_MASTER SYNC_DATE=N/A

PAGE TITLE: Holes

Apple Inc.

DRAWING NUMBER: 051-8115 SIZE: D

REVISION: 11.1.0

BRANCH:

PAGE: 7 OF 110

SHEET: 7 OF 98

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## UNUSED CPU SIGNALS

| | | | |
|---|---|---|---|
| 10 | TP_CPU_RSVD<16..1> | NC_CPU_RSVD<16..1> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_CPU_RSVD<46..19> | NC_CPU_RSVD<46..19> | MAKE_BASE=TRUE NO_TEST=TRUE |

## NC ON UNUSED PCI ALIASES

| | | | |
|---|---|---|---|
| 20 | TP_PCI_AD<31..0> | NC_PCI_AD<31..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_PCI_C_BE_L<3..0> | NC_PCI_C_BE_L<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_PCI_PAR | NC_PCI_PAR | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_PCI_RESET_L | NC_PCI_RESET_L | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_LPC_DREQ0_L | NC_LPC_DREQ0_L | MAKE_BASE=TRUE NO_TEST=TRUE |

## NC ON UNUSED MEM ALIASES

| | | | |
|---|---|---|---|
| 12 | TP_MEM_A_DQ_CB<7..0> | NC_MEM_A_DQ_CB<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 12 | TP_MEM_A_DQS_N<8> | NC_MEM_A_DQSN<8> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 12 | TP_MEM_A_DQS_P<8> | NC_MEM_A_DQSP<8> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 12 | TP_MEM_B_DQ_CB<7..0> | NC_MEM_B_DQ_CB<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 12 | TP_MEM_B_DQS_N<8> | NC_MEM_B_DQSN<8> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 12 | TP_MEM_B_DQS_P<8> | NC_MEM_B_DQSP<8> | MAKE_BASE=TRUE NO_TEST=TRUE |

## NC ON UNUSED MISC ALIASES

| | | | |
|---|---|---|---|
| 18 | TP_HDA_SDIN1 | NC_HDA_SDIN1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_HDA_SDIN2 | NC_HDA_SDIN2 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_HDA_SDIN3 | NC_HDA_SDIN3 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_PWM0 | NC_PCH_PWM0 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_PWM1 | NC_PCH_PWM1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_PWM2 | NC_PCH_PWM2 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_PWM3 | NC_PCH_PWM3 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_SST | NC_PCH_SST | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_CL_CLK1 | NC_PCH_CL_CLK1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_CL_DATA1 | NC_PCH_CL_DATA1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_CL_RST1 | NC_PCH_CL_RST1 | MAKE_BASE=TRUE NO_TEST=TRUE |

## NC ON UNUSED PCIE ALIASES

| | | | |
|---|---|---|---|
| 18 | TP_PCIE_CLK100M_PE5P | NC_PCIE_CLK100M_PE5P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_CLK100M_PE5N | NC_PCIE_CLK100M_PE5N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCIE_CLK100M_PE6P | NC_PCIE_CLK100M_PE6P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCIE_CLK100M_PE6N | NC_PCIE_CLK100M_PE6N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCIE_CLK100M_PE7P | NC_PCIE_CLK100M_PE7P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCIE_CLK100M_PE7N | NC_PCIE_CLK100M_PE7N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_PE_RX_N<3..0> | NC_PE_RXN<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_PE_RX_P<3..0> | NC_PE_RXP<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_PE_TX_N<3..0> | NC_PE_TXN<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_PE_TX_P<3..0> | NC_PE_TXP<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_D2R_PERN4 | NC_PCIE_D2R_PERN4 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_D2R_PERP4 | NC_PCIE_D2R_PERP4 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_R2D_PETN4 | NC_PCIE_R2D_PETN4 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_R2D_PETP4 | NC_PCIE_R2D_PETP4 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_CLK100M_PE4P | NC_PCIE_CLK100M_PE4P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_CLK100M_PE4N | NC_PCIE_CLK100M_PE4N | MAKE_BASE=TRUE NO_TEST=TRUE |

## NC ON UNUSED USB ALIASES

| | | | |
|---|---|---|---|
| 20 | TP_USB_1N | NC_USB_1N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_1P | NC_USB_1P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_2N | NC_USB_2N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_2P | NC_USB_2P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_3N | NC_USB_3N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_3P | NC_USB_3P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_4N | NC_USB_4N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_4P | NC_USB_4P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_5N | NC_USB_5N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_5P | NC_USB_5P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_6N | NC_USB_6N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_6P | NC_USB_6P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_7N | NC_USB_7N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_7P | NC_USB_7P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_10N | NC_USB_10N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_10P | NC_USB_10P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_11N | NC_USB_11N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_11P | NC_USB_11P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_12N | NC_USB_12N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_12P | NC_USB_12P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_13N | NC_USB_13N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_USB_13P | NC_USB_13P | MAKE_BASE=TRUE NO_TEST=TRUE |

## NC ON UNUSED DISPLAY ALIASES

| | | | |
|---|---|---|---|
| 19 | TP_CRT_IG_DDC_CLK | NC_CRT_IG_DDC_CLK | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_DDC_DATA | NC_CRT_IG_DDC_DATA | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_RED | NC_CRT_IG_RED | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_GREEN | NC_CRT_IG_GREEN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_BLUE | NC_CRT_IG_BLUE | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_HSYNC | NC_CRT_IG_HSYNC | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_VSYNC | NC_CRT_IG_VSYNC | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_B_MLN<3..0> | NC_DP_IG_B_MLN<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_B_MLP<3..0> | NC_DP_IG_B_MLP<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_B_AUX_N | NC_DP_IG_B_AUXN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_B_AUX_P | NC_DP_IG_B_AUXP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_B_HPD | NC_DP_IG_B_HPD | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_B_DDC_CLK | NC_DP_IG_B_CTRL_CLK | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_B_DDC_DATA | NC_DP_IG_B_CTRL_DATA | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_C_MLN<3..0> | NC_DP_IG_C_MLN<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_C_MLP<3..0> | NC_DP_IG_C_MLP<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_C_AUX_N | NC_DP_IG_C_AUXN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_C_AUX_P | NC_DP_IG_C_AUXP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_C_HPD | NC_DP_IG_C_HPD | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_C_CTRL_CLK | NC_DP_IG_C_CTRL_CLK | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_C_CTRL_DATA | NC_DP_IG_C_CTRL_DATA | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_D_MLN<3..0> | NC_DP_IG_D_MLN<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_D_MLP<3..0> | NC_DP_IG_D_MLP<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_D_AUXN | NC_DP_IG_D_AUXN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_D_AUXP | NC_DP_IG_D_AUXP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_D_HPD | NC_DP_IG_D_HPD | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_D_CTRL_CLK | NC_DP_IG_D_CTRL_CLK | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_DP_IG_D_CTRL_DATA | NC_DP_IG_D_CTRL_DATA | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_TVCLKINN | NC_SDVO_TVCLKINN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_TVCLKINP | NC_SDVO_TVCLKINP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_STALLN | NC_SDVO_STALLN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_STALLP | NC_SDVO_STALLP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_INTN | NC_SDVO_INTN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_INTP | NC_SDVO_INTP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_L_BKLTCTL | NC_PCH_L_BKLTCTL | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_L_BKLTEN | NC_PCH_L_BKLTEN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_L_VDD_EN | NC_PCH_L_VDD_EN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_CLKOUT_DPN | NC_PCH_CLKOUT_DPN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_CLKOUT_DPP | NC_PCH_CLKOUT_DPP | MAKE_BASE=TRUE NO_TEST=TRUE |

## NC ON UNUSED FDI ALIASES

| | | | |
|---|---|---|---|
| 10 | TP_CPU_FDI_TX_N<7..0> | NC_CPU_FDI_TXN<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_CPU_FDI_TX_P<7..0> | NC_CPU_FDI_TXP<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_FDI_RX_N<7..0> | NC_PCH_FDI_RXN<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_FDI_RX_P<7..0> | NC_PCH_FDI_RXP<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |

## NC ON UNUSED SATA ALIASES

| | | | |
|---|---|---|---|
| 19 | TP_SATA_D_D2RN | NC_SATA_D_D2RN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_D_D2RP | NC_SATA_D_D2RP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_D_R2D_CN | NC_SATA_D_R2D_CN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_D_R2D_CP | NC_SATA_D_R2D_CP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_E_D2RN | NC_SATA_E_D2RN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_E_D2RP | NC_SATA_E_D2RP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_E_R2D_CN | NC_SATA_E_R2D_CN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_E_R2D_CP | NC_SATA_E_R2D_CP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_F_D2RN | NC_SATA_F_D2RN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_F_D2RP | NC_SATA_F_D2RP | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_F_R2D_CN | NC_SATA_F_R2D_CN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SATA_F_R2D_CP | NC_SATA_F_R2D_CP | MAKE_BASE=TRUE NO_TEST=TRUE |

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
# UNUSED SIGNAL ALIAS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

BRANCH

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## PEG Slot Support

THIS SIGNAL NAME IS CONNECTED TO MXM

| | | | | | |
|---|---|---|---|---|---|
| 18 IN | PEG_CLK100M_P | 90 | GPU_CLK100M_PCIE_P (MAKE_BASE=TRUE) | CLK_100M_MXM_P | OUT 75 |
| 18 IN | PEG_CLK100M_N | 90 | GPU_CLK100M_PCIE_N (MAKE_BASE=TRUE) | CLK_100M_MXM_N | OUT 75 |
| 19 IN | =PEG_R2D_C_P<0..15> | | PEG_R2D_C_P<0..15> (MAKE_BASE=TRUE) | | OUT 77 90 |
| 19 IN | =PEG_R2D_C_N<0..15> | | PEG_R2D_C_N<0..15> (MAKE_BASE=TRUE) | | OUT 77 90 |
| 19 OUT | =PEG_D2R_P<0..15> | | PEG_D2R_P<0..15> (MAKE_BASE=TRUE) | | IN 77 90 |
| 19 OUT | =PEG_D2R_N<0..15> | | PEG_D2R_N<0..15> (MAKE_BASE=TRUE) | | IN 77 90 |
| 21 IN | PEG_CLKREQ_L | | MXM_CLKREQ_L (MAKE_BASE=TRUE) | | OUT 75 97 |
| 75 | MXM_RESET_L | | PEG_RESET_L (MAKE_BASE=TRUE) | | 27 97 |

97 91 19 IN PM_CLK32K_SUSCLK_R — R929 22 5% 1/16W MF-LF 402 (1, 2) — PM_CLK32K_SUSCLK OUT 46 91 97

PLACEMENT_NOTE=PLACE CLOSE TO U1800

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
# Signal Aliases

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SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R1010.1
ROUTE B5 TO R1010.1 AS A SEPERATE 10 MIL TRACE.

OMIT
U1000
SANDY_BRIDGE
LGA1155-SKT
(1 OF 10)

DMI

| | | |
|---|---|---|
| DMI_S2N_N<0> | W4 | DMI_RX_0* |
| DMI_S2N_N<1> | V4 | DMI_RX_1* |
| DMI_S2N_N<2> | Y4 | DMI_RX_2* |
| DMI_S2N_N<3> | AA5 | DMI_RX_3* |
| DMI_S2N_P<0> | W5 | DMI_RX_0 |
| DMI_S2N_P<1> | V3 | DMI_RX_1 |
| DMI_S2N_P<2> | Y3 | DMI_RX_2 |
| DMI_S2N_P<3> | AA4 | DMI_RX_3 |
| DMI_N2S_N<0> | V6 | DMI_TX_0* |
| DMI_N2S_N<1> | W8 | DMI_TX_1* |
| DMI_N2S_N<2> | Y7 | DMI_TX_2* |
| DMI_N2S_N<3> | AA8 | DMI_TX_3* |
| DMI_N2S_P<0> | V7 | DMI_TX_0 |
| DMI_N2S_P<1> | W7 | DMI_TX_1 |
| DMI_N2S_P<2> | Y6 | DMI_TX_2 |
| DMI_N2S_P<3> | AA7 | DMI_TX_3 |

FLEXIBLE DISPLAY INTERFACE (Unused)

| | | |
|---|---|---|
| TP_CPU_FDI_TX_N<0> | AC7 | FDI_TX_0* |
| TP_CPU_FDI_TX_N<1> | AC3 | FDI_TX_1* |
| TP_CPU_FDI_TX_N<2> | AD1 | FDI_TX_2* |
| TP_CPU_FDI_TX_N<3> | AD3 | FDI_TX_3* |
| TP_CPU_FDI_TX_N<4> | AD6 | FDI_TX_4* |
| TP_CPU_FDI_TX_N<5> | AE8 | FDI_TX_5* |
| TP_CPU_FDI_TX_N<6> | AF2 | FDI_TX_6* |
| TP_CPU_FDI_TX_N<7> | AG1 | FDI_TX_7* |
| TP_CPU_FDI_TX_P<0> | AC8 | FDI_TX_0 |
| TP_CPU_FDI_TX_P<1> | AC2 | FDI_TX_1 |
| TP_CPU_FDI_TX_P<2> | AD2 | FDI_TX_2 |
| TP_CPU_FDI_TX_P<3> | AD4 | FDI_TX_3 |
| TP_CPU_FDI_TX_P<4> | AD7 | FDI_TX_4 |
| TP_CPU_FDI_TX_P<5> | AE7 | FDI_TX_5 |
| TP_CPU_FDI_TX_P<6> | AF3 | FDI_TX_6 |
| TP_CPU_FDI_TX_P<7> | AG2 | FDI_TX_7 |
| CPU_FDI_FSYNC<0> | AC5 | FDI_FSYNC_0 |
| CPU_FDI_FSYNC<1> | AE5 | FDI_FSYNC_1 |
| CPU_FDI_INT | AG3 | FDI_INT |
| CPU_FDI_LSYNC<0> | AC4 | FDI_LSYNC_0 |
| CPU_FDI_LSYNC<1> | AE4 | FDI_LSYNC_1 |
| CPU_FDI_COMPIO | AE2 | FDI_COMPIO |
| | AE1 | FDI_ICOMPO |

PLACEMENT_NOTE=Place within 12.7MM of CPU
R1011 0 5% 1/10W MF-LF 402
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=CPU_RCOMP

PCI EXPRESS (Available for Workstation only)

| | | |
|---|---|---|
| TP_PE_RX_N<0> | P4 | PE_RX_0* |
| TP_PE_RX_N<1> | R1 | PE_RX_1* |
| TP_PE_RX_N<2> | T3 | PE_RX_2* |
| TP_PE_RX_N<3> | U1 | PE_RX_3* |
| TP_PE_RX_P<0> | P3 | PE_RX_0 |
| TP_PE_RX_P<1> | R2 | PE_RX_1 |
| TP_PE_RX_P<2> | T4 | PE_RX_2 |
| TP_PE_RX_P<3> | U2 | PE_RX_3 |
| TP_PE_TX_N<0> | P7 | PE_TX_0* |
| TP_PE_TX_N<1> | T8 | PE_TX_1* |
| TP_PE_TX_N<2> | R5 | PE_TX_2* |
| TP_PE_TX_N<3> | U6 | PE_TX_3* |
| TP_PE_TX_P<0> | P8 | PE_TX_0 |
| TP_PE_TX_P<1> | T7 | PE_TX_1 |
| TP_PE_TX_P<2> | R6 | PE_TX_2 |
| TP_PE_TX_P<3> | U5 | PE_TX_3 |

PCI EXPRESS -- GRAPHICS

| | | |
|---|---|---|
| PEG_COMPI | B4 | |
| PEG_ICOMPO | B5 | |
| PEG_RCOMPO | C4 | CPU_PEG_COMP |
| PEG_RX_0* | B12 | =PEG_D2R_N<0> |
| PEG_RX_1* | D11 | =PEG_D2R_N<1> |
| PEG_RX_2* | C9 | =PEG_D2R_N<2> |
| PEG_RX_3* | E9 | =PEG_D2R_N<3> |
| PEG_RX_4* | B7 | =PEG_D2R_N<4> |
| PEG_RX_5* | C5 | =PEG_D2R_N<5> |
| PEG_RX_6* | A6 | =PEG_D2R_N<6> |
| PEG_RX_7* | E1 | =PEG_D2R_N<7> |
| PEG_RX_8* | F3 | =PEG_D2R_N<8> |
| PEG_RX_9* | G1 | =PEG_D2R_N<9> |
| PEG_RX_10* | H4 | =PEG_D2R_N<10> |
| PEG_RX_11* | J2 | =PEG_D2R_N<11> |
| PEG_RX_12* | K4 | =PEG_D2R_N<12> |
| PEG_RX_13* | L2 | =PEG_D2R_N<13> |
| PEG_RX_14* | M4 | =PEG_D2R_N<14> |
| PEG_RX_15* | N2 | =PEG_D2R_N<15> |
| PEG_RX_0 | B11 | =PEG_D2R_P<0> |
| PEG_RX_1 | D12 | =PEG_D2R_P<1> |
| PEG_RX_2 | C10 | =PEG_D2R_P<2> |
| PEG_RX_3 | E10 | =PEG_D2R_P<3> |
| PEG_RX_4 | B8 | =PEG_D2R_P<4> |
| PEG_RX_5 | C6 | =PEG_D2R_P<5> |
| PEG_RX_6 | A5 | =PEG_D2R_P<6> |
| PEG_RX_7 | E2 | =PEG_D2R_P<7> |
| PEG_RX_8 | F4 | =PEG_D2R_P<8> |
| PEG_RX_9 | G2 | =PEG_D2R_P<9> |
| PEG_RX_10 | H3 | =PEG_D2R_P<10> |
| PEG_RX_11 | J1 | =PEG_D2R_P<11> |
| PEG_RX_12 | K3 | =PEG_D2R_P<12> |
| PEG_RX_13 | L1 | =PEG_D2R_P<13> |
| PEG_RX_14 | M3 | =PEG_D2R_P<14> |
| PEG_RX_15 | N1 | =PEG_D2R_P<15> |
| PEG_TX_0* | C14 | =PEG_R2D_C_N<0> |
| PEG_TX_1* | E13 | =PEG_R2D_C_N<1> |
| PEG_TX_2* | G13 | =PEG_R2D_C_N<2> |
| PEG_TX_3* | F11 | =PEG_R2D_C_N<3> |
| PEG_TX_4* | J13 | =PEG_R2D_C_N<4> |
| PEG_TX_5* | D7 | =PEG_R2D_C_N<5> |
| PEG_TX_6* | C3 | =PEG_R2D_C_N<6> |
| PEG_TX_7* | E5 | =PEG_R2D_C_N<7> |
| PEG_TX_8* | F7 | =PEG_R2D_C_N<8> |
| PEG_TX_9* | G9 | =PEG_R2D_C_N<9> |
| PEG_TX_10* | G6 | =PEG_R2D_C_N<10> |
| PEG_TX_11* | K8 | =PEG_R2D_C_N<11> |
| PEG_TX_12* | J6 | =PEG_R2D_C_N<12> |
| PEG_TX_13* | M7 | =PEG_R2D_C_N<13> |
| PEG_TX_14* | L5 | =PEG_R2D_C_N<14> |
| PEG_TX_15* | N6 | =PEG_R2D_C_N<15> |
| PEG_TX_0 | C13 | =PEG_R2D_C_P<0> |
| PEG_TX_1 | E14 | =PEG_R2D_C_P<1> |
| PEG_TX_2 | G14 | =PEG_R2D_C_P<2> |
| PEG_TX_3 | F12 | =PEG_R2D_C_P<3> |
| PEG_TX_4 | J14 | =PEG_R2D_C_P<4> |
| PEG_TX_5 | D8 | =PEG_R2D_C_P<5> |
| PEG_TX_6 | D3 | =PEG_R2D_C_P<6> |
| PEG_TX_7 | E6 | =PEG_R2D_C_P<7> |
| PEG_TX_8 | F8 | =PEG_R2D_C_P<8> |
| PEG_TX_9 | G10 | =PEG_R2D_C_P<9> |
| PEG_TX_10 | G5 | =PEG_R2D_C_P<10> |
| PEG_TX_11 | K7 | =PEG_R2D_C_P<11> |
| PEG_TX_12 | J5 | =PEG_R2D_C_P<12> |
| PEG_TX_13 | M8 | =PEG_R2D_C_P<13> |
| PEG_TX_14 | L6 | =PEG_R2D_C_P<14> |
| PEG_TX_15 | N5 | =PEG_R2D_C_P<15> |

PLACEMENT_NOTE=Place within 12.7MM of CPU
R1010 24.9 1% 1/10W MF-LF 402
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=CPU_RCOMP
=PPVCCIO_S0_CPU

OMIT
U1000
SANDY_BRIDGE
LGA1155-SKT
(5 OF 10)

RESERVED

| | | |
|---|---|---|
| TP_CPU_RSVD<1> | C38 | RSVD_C38 |
| TP_CPU_RSVD<2> | C39 | RSVD_C39 |
| TP_CPU_RSVD<3> | D38 | RSVD_D38 |
| TP_CPU_RSVD<4> | H7 | RSVD_H7 |
| TP_CPU_RSVD<5> | H8 | RSVD_H8 |
| TP_CPU_RSVD<6> | J9 | RSVD_J9 |
| TP_CPU_RSVD<7> | J31 | RSVD_J31 |
| TP_CPU_RSVD<8> | J33 | RSVD_J33 |
| TP_CPU_RSVD<9> | J34 | RSVD_J34 |
| TP_CPU_RSVD<10> | K9 | RSVD_K9 |
| TP_CPU_RSVD<11> | K31 | RSVD_K31 |
| TP_CPU_RSVD<12> | K34 | RSVD_K34 |
| TP_CPU_RSVD<13> | L9 | RSVD_L9 |
| TP_CPU_RSVD<14> | L31 | RSVD_L31 |
| TP_CPU_RSVD<15> | L33 | RSVD_L33 |
| TP_CPU_RSVD<16> | L34 | RSVD_L34 |
| SNS_CPU_THERMD_N | M34 | RSVD_M34 ThermDC |
| SNS_CPU_THERMD_P | N33 | RSVD_N33 ThermDA |
| TP_CPU_RSVD<19> | N34 | RSVD_N34 |
| CPU_CFG<0> | H36 | CFG_0 |
| CPU_CFG<1> | J36 | CFG_1 |
| CPU_CFG<2> | J37 | CFG_2 |
| CPU_CFG<3> | K36 | CFG_3 |
| CPU_CFG<4> | L36 | CFG_4 |
| CPU_CFG<5> | N35 | CFG_5 |
| CPU_CFG<6> | L37 | CFG_6 |
| CPU_CFG<7> | M36 | CFG_7 |
| CPU_CFG<8> | J38 | CFG_8 |
| CPU_CFG<9> | L35 | CFG_9 |
| CPU_CFG<10> | M38 | CFG_10 |
| CPU_CFG<11> | N36 | CFG_11 |
| CPU_CFG<12> | N38 | CFG_12 |
| CPU_CFG<13> | N39 | CFG_13 |
| CPU_CFG<14> | N37 | CFG_14 |
| CPU_CFG<15> | N40 | CFG_15 |
| CPU_CFG<16> | G37 | CFG_16 |
| CPU_CFG<17> | G36 | CFG_17 |

| | | |
|---|---|---|
| RSVD_P35 | P35 | TP_CPU_RSVD<20> |
| RSVD_P37 | P37 | TP_CPU_RSVD<21> |
| RSVD_P39 | P39 | TP_CPU_RSVD<22> |
| RSVD_R34 | R34 | TP_CPU_RSVD<23> |
| RSVD_R36 | R36 | TP_CPU_RSVD<24> |
| RSVD_R38 | R38 | TP_CPU_RSVD<25> |
| RSVD_R40 | R40 | TP_CPU_RSVD<26> |
| RSVD_AB6 | AB6 | TP_CPU_RSVD<27> |
| RSVD_AB7 | AB7 | TP_CPU_RSVD<28> |
| RSVD_AD34 | AD34 | TP_CPU_RSVD<29> |
| RSVD_AD35 | AD35 | TP_CPU_RSVD<30> |
| RSVD_AD37 | AD37 | TP_CPU_RSVD<31> |
| RSVD_AE6 | AE6 | TP_CPU_RSVD<32> |
| RSVD_AF4 | AF4 | TP_CPU_RSVD<33> |
| RSVD_AG4 | AG4 | TP_CPU_RSVD<34> |
| RSVD_AJ11 | AJ11 | TP_CPU_RSVD<35> |
| RSVD_AJ29 | AJ29 | TP_CPU_RSVD<36> |
| RSVD_AJ30 | AJ30 | TP_CPU_RSVD<37> |
| RSVD_AJ31 | AJ31 | TP_CPU_RSVD<38> |
| RSVD_AN20 | AN20 | TP_CPU_RSVD<39> |
| RSVD_AP20 | AP20 | TP_CPU_RSVD<40> |
| RSVD_AT11 | AT11 | TP_CPU_RSVD<41> |
| RSVD_AT14 | AT14 | TP_CPU_RSVD<42> |
| RSVD_AU10 | AU10 | TP_CPU_RSVD<43> |
| RSVD_AV34 | AV34 | TP_CPU_RSVD<44> |
| RSVD_AW34 | AW34 | TP_CPU_RSVD<45> |
| RSVD_AY10 | AY10 | TP_CPU_RSVD<46> |
| RSVD_NCTF_AV1 | AV1 | TP_CPU_RSVD_NCTF<1> |
| RSVD_NCTF_AW2 | AW2 | TP_CPU_RSVD_NCTF<2> |
| RSVD_NCTF_AY3 | AY3 | TP_CPU_RSVD_NCTF<3> |
| RSVD_NCTF_B39 | B39 | TP_CPU_RSVD_NCTF<4> |
| NCTF_A38 | A38 | TP_CPU_NCTF<1> |
| NCTF_C2 | C2 | TP_CPU_NCTF<2> |
| NCTF_D1 | D1 | TP_CPU_NCTF<3> |
| NCTF_AU40 | AU40 | TP_CPU_NCTF<4> |
| NCTF_AW38 | AW38 | TP_CPU_NCTF<5> |

INTEL SUGGESTS TO KEEP THESE TPS

FOR SANDYBRIDGE PROCESSOR

CFG [6:5] :PCIE CONFIGURATION SELECT 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [2] :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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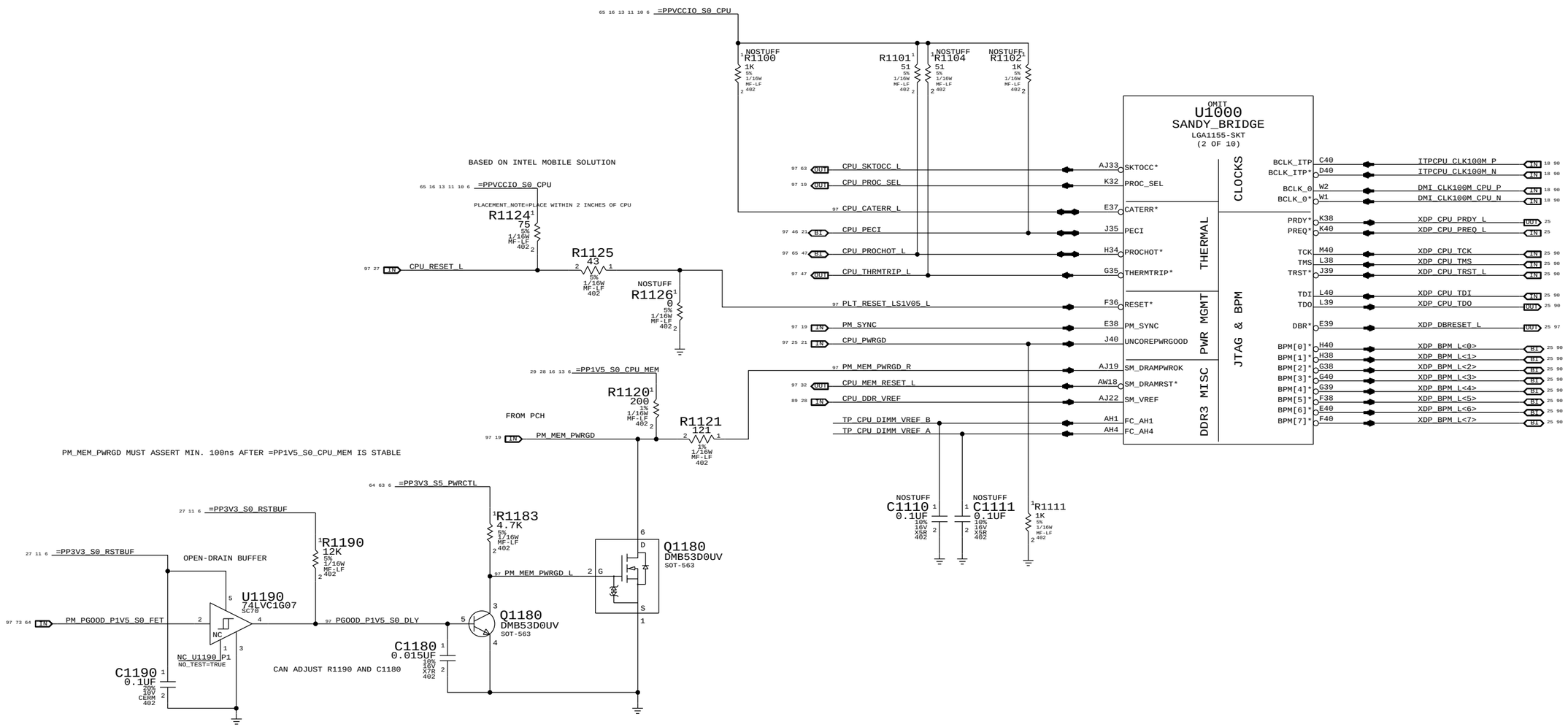


PAGE TITLE
# CPU CLOCK/MISC/JTAG

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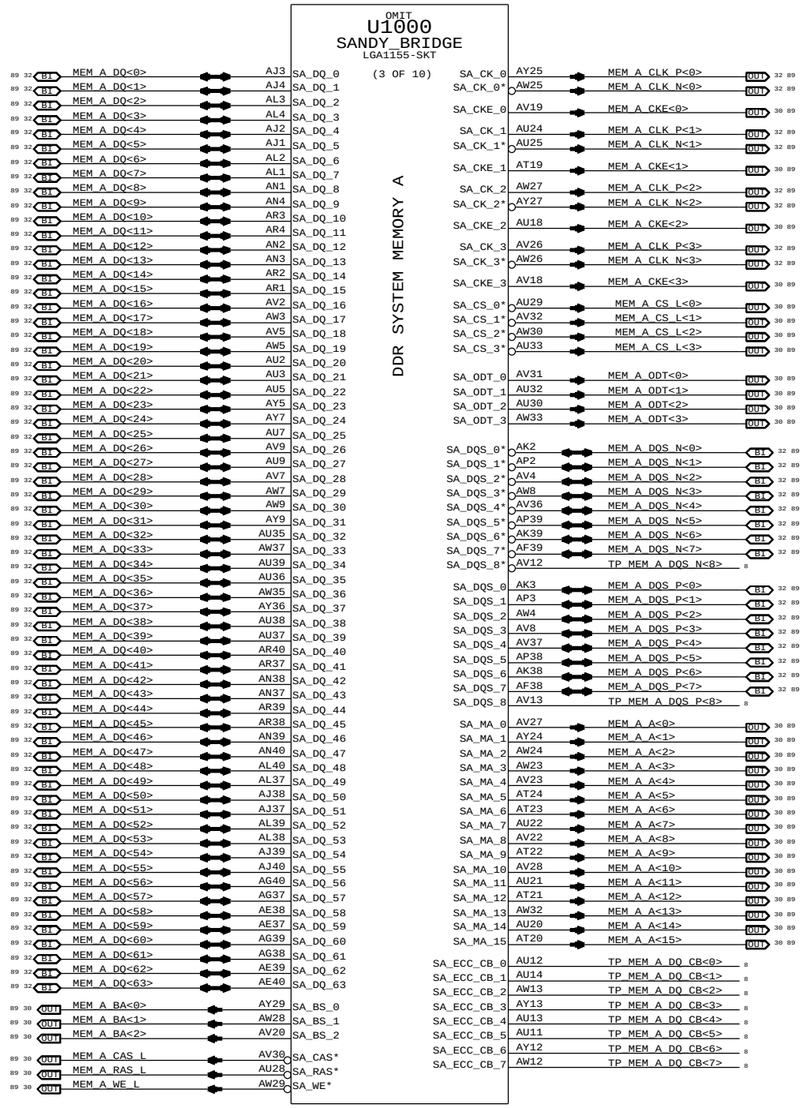


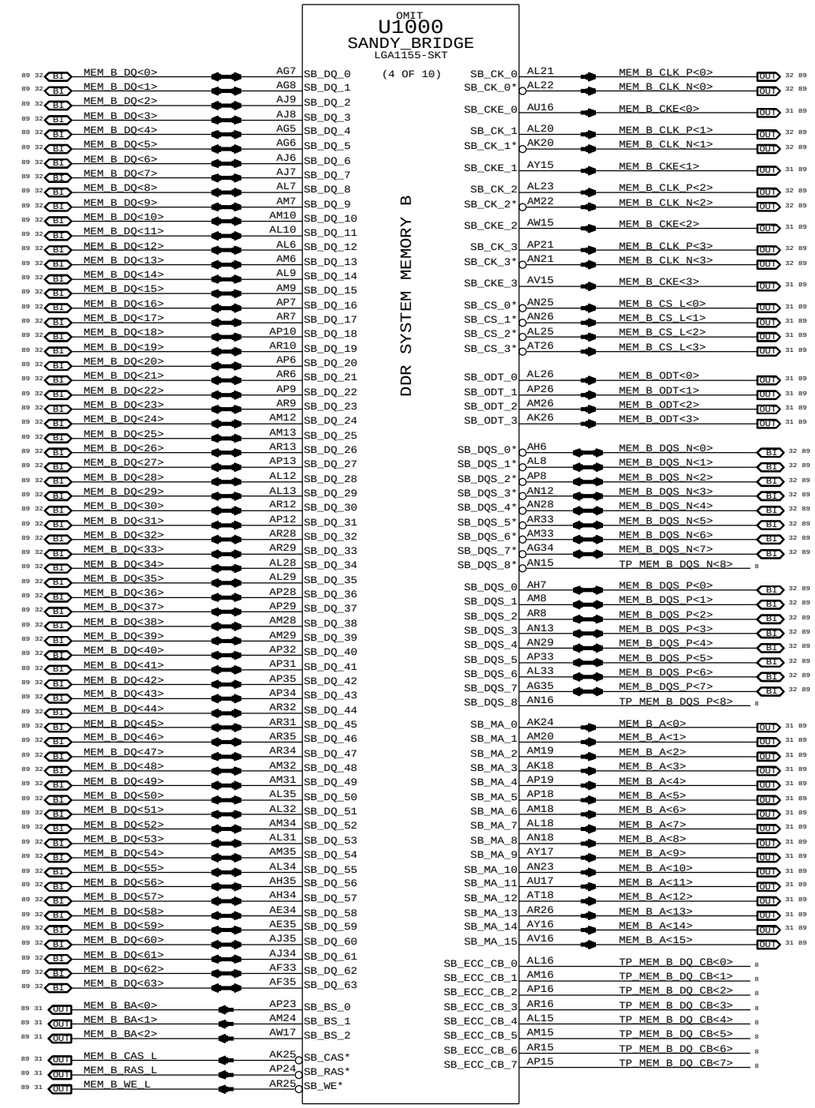


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PAGE TITLE
# CPU DDR3 INTERFACES

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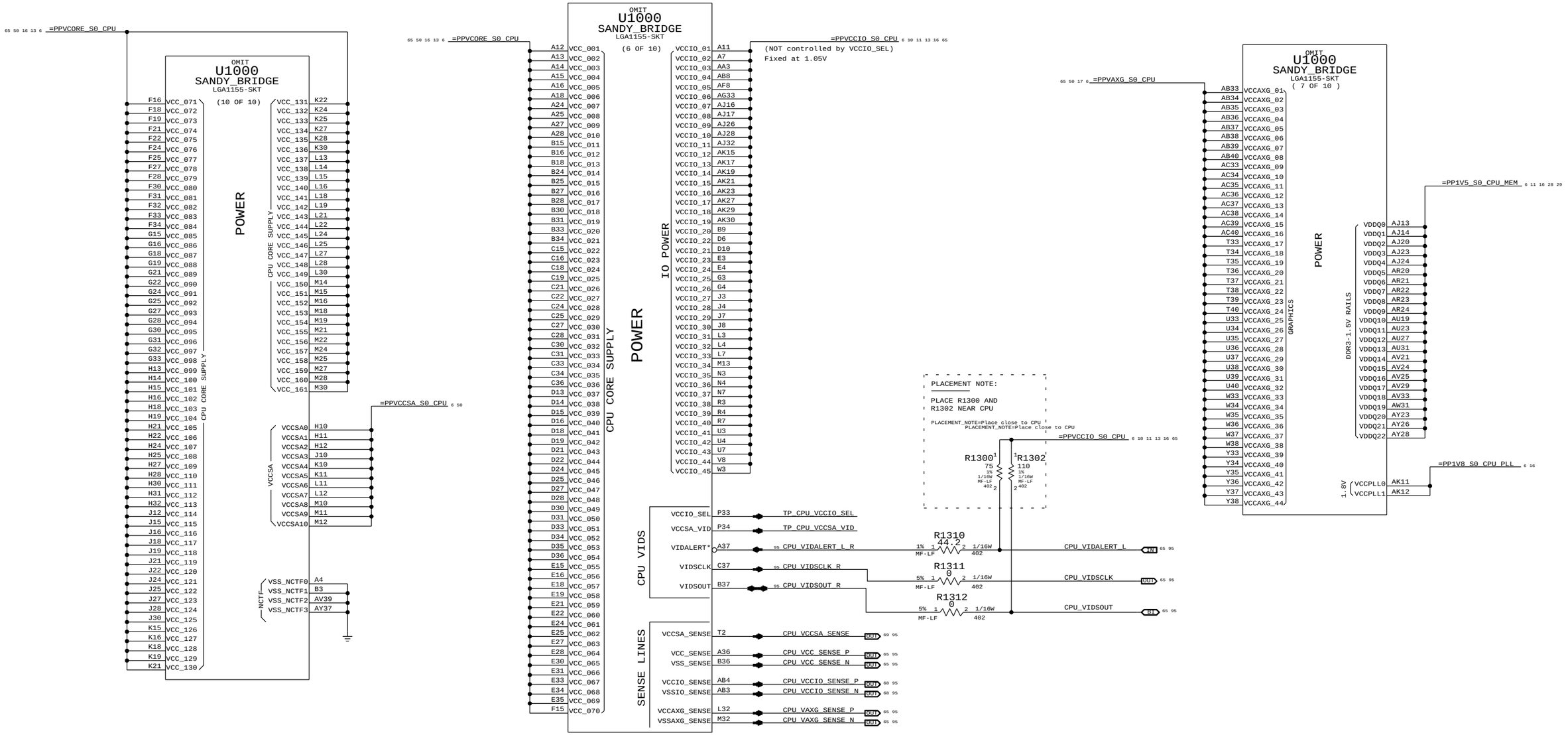


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PAGE TITLE
# CPU POWER

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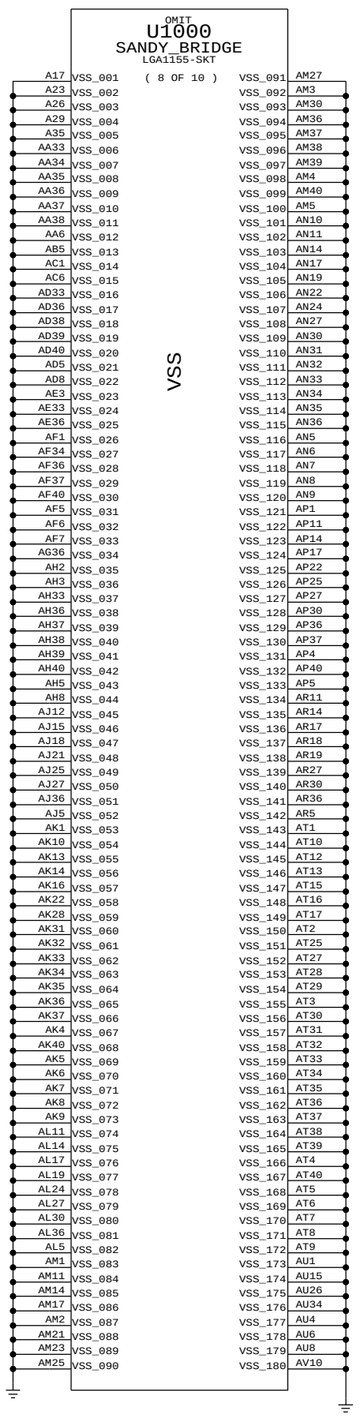


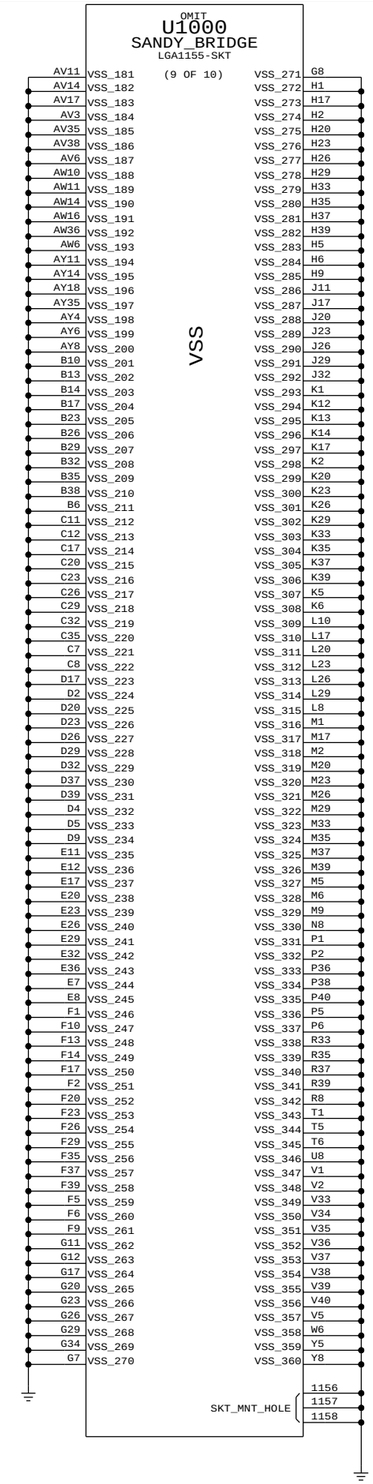


PAGE TITLE

# CPU GROUNDS

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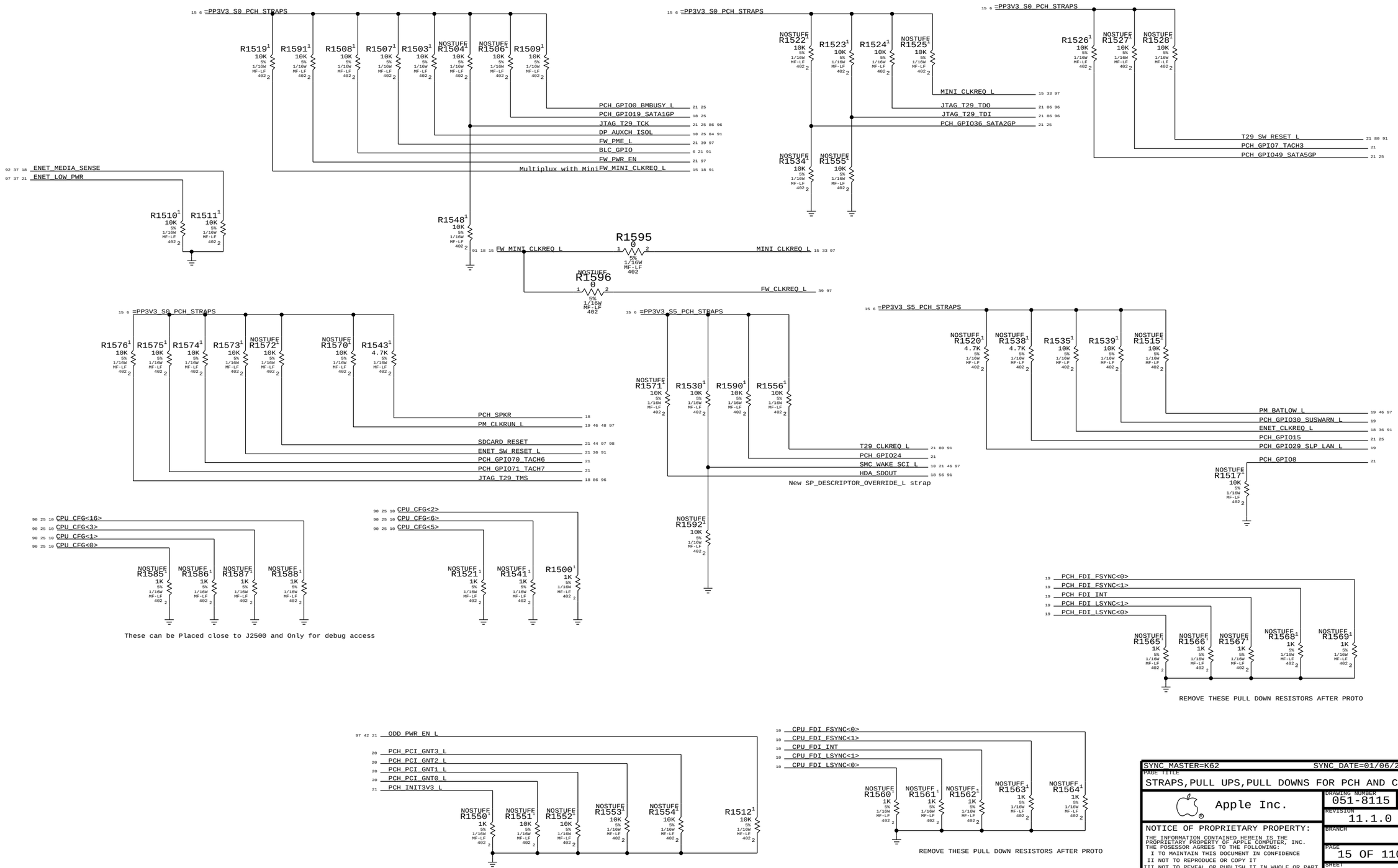


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PAGE TITLE
STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU

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# CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT_NOTE (C1600-C1613):

**Place inside socket cavity**

16 13 6 65 50 =PPVCORE_S0_CPU

C1600 22UF 20% 6.3V CERM-X5R 805-3
C1601 22UF 20% 6.3V CERM-X5R 805-3
C1602 22UF 20% 6.3V CERM-X5R 805-3
C1603 22UF 20% 6.3V CERM-X5R 805-3
C1604 22UF 20% 6.3V CERM-X5R 805-3
C1605 22UF 20% 6.3V CERM-X5R 805-3
C1606 22UF 20% 6.3V CERM-X5R 805-3
C1607 22UF 20% 6.3V CERM-X5R 805-3
C1608 22UF 20% 6.3V CERM-X5R 805-3
C1609 22UF 20% 6.3V CERM-X5R 805-3

C1610 22UF 20% 6.3V CERM-X5R 805-3
C1611 22UF 20% 6.3V CERM-X5R 805-3
C1612 22UF 20% 6.3V CERM-X5R 805-3
C1613 22UF 20% 6.3V CERM-X5R 805-3

BULK CAPS ON CPU VREG PAGE 72

10x 10UF and 10x 1UF CAPACITORS

**Place inside socket cavity**

65 50 16 13 6 =PPVCORE_S0_CPU

C1620 10UF 20% 16V X5R 603
C1621 10UF 20% 16V X5R 603
C1622 10UF 20% 16V X5R 603
C1623 10UF 20% 16V X5R 603
C1624 10UF 20% 16V X5R 603
C1625 10UF 20% 16V X5R 603
C1626 10UF 20% 16V X5R 603
C1627 10UF 20% 16V X5R 603
C1628 10UF 20% 16V X5R 603
C1629 10UF 20% 16V X5R 603

C1630 1UF 10% 16V X5R 402
C1631 1UF 10% 16V X5R 402
C1632 1UF 10% 16V X5R 402
C1633 1UF 10% 16V X5R 402
C1634 1UF 10% 16V X5R 402
C1635 1UF 10% 16V X5R 402
C1636 1UF 10% 16V X5R 402
C1637 1UF 10% 16V X5R 402
C1638 1UF 10% 16V X5R 402
C1639 1UF 10% 16V X5R 402

# CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

PLACEMENT_NOTE (C1650-C1657):

**Place under socket cavity on secondary side.**

13 11 10 6 65 =PPVCCIO_S0_CPU

C1650 22UF 20% 6.3V CERM-X5R 805
C1651 22UF 20% 6.3V CERM-X5R 805
C1652 22UF 20% 6.3V CERM-X5R 805
C1653 22UF 20% 6.3V CERM-X5R 805
C1654 22UF 20% 6.3V CERM-X5R 805
C1655 22UF 20% 6.3V CERM-X5R 805
C1656 22UF 20% 6.3V CERM-X5R 805
C1657 22UF 20% 6.3V CERM-X5R 805

PLACEMENT_NOTE (C1660-C1665):

**Place at edge of socket.**

BULK CAPS ON CPU VREG PAGE 72

C1660 10uF 20% 6.3V X5R 603
C1661 10uF 20% 6.3V X5R 603
C1662 10uF 20% 6.3V X5R 603
C1663 10uF 20% 6.3V X5R 603
C1664 10uF 20% 6.3V X5R 603
C1665 10uF 20% 6.3V X5R 603

C1670 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

# Memory (CPU VCCDDR) DECOUPLING

6x 22uF 0805, 5x 1uF 0402. INTEL RECOMMENDATION 9X 22uF 0805

28 13 11 6 29 =PP1V5_S0_CPU_MEM

C1676 22uF 20% 6.3V CERM-X5R 805
C1677 22uF 20% 6.3V CERM-X5R 805
C1678 22uF 20% 6.3V CERM-X5R 805
C1679 22uF 20% 6.3V CERM-X5R 805
C1680 22uF 20% 6.3V CERM-X5R 805
C1681 22uF 20% 6.3V CERM-X5R 805
C1682 1UF 10% 10V X5R 402
C1683 1UF 10% 10V X5R 402
C1684 1UF 10% 10V X5R 402
C1685 1UF 10% 10V X5R 402
C1686 1UF 10% 10V X5R 402

Note: VCCSA decoupling is on regulator page

# PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 10x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402
C1692 2.2UF 10% 6.3V X5R 402
C1691 4.7UF 10% 6.3V X5R-CERM 603
C1695 10UF 20% 6.3V X5R 603
C1690 22uF 20% 6.3V CERM-X5R 805
C1696 47UF 20% 6.3V X5R 0805
C1697 47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 78

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
CPU NON-GFX DECOUPLING

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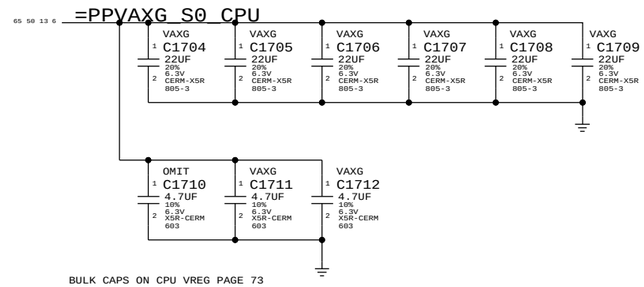
# VAXG DECOUPLING

INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

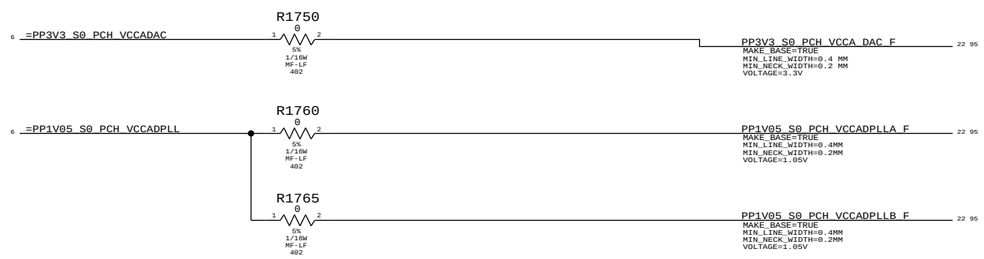
PLACEMENT_NOTE (C1704-C1709):

**Place inside socket cavity**




BULK CAPS ON CPU VREG PAGE 73

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 138S0586 | 1 | CAP,4.7UF,10%,6.3V,0603 | C1710 | VAXG |
| 113S0022 | 1 | RES,0 OHM,5%,0603 | C1710 | NO_VAXG |

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PAGE TITLE
GFX DECOUPLING & PCH PWR ALIAS

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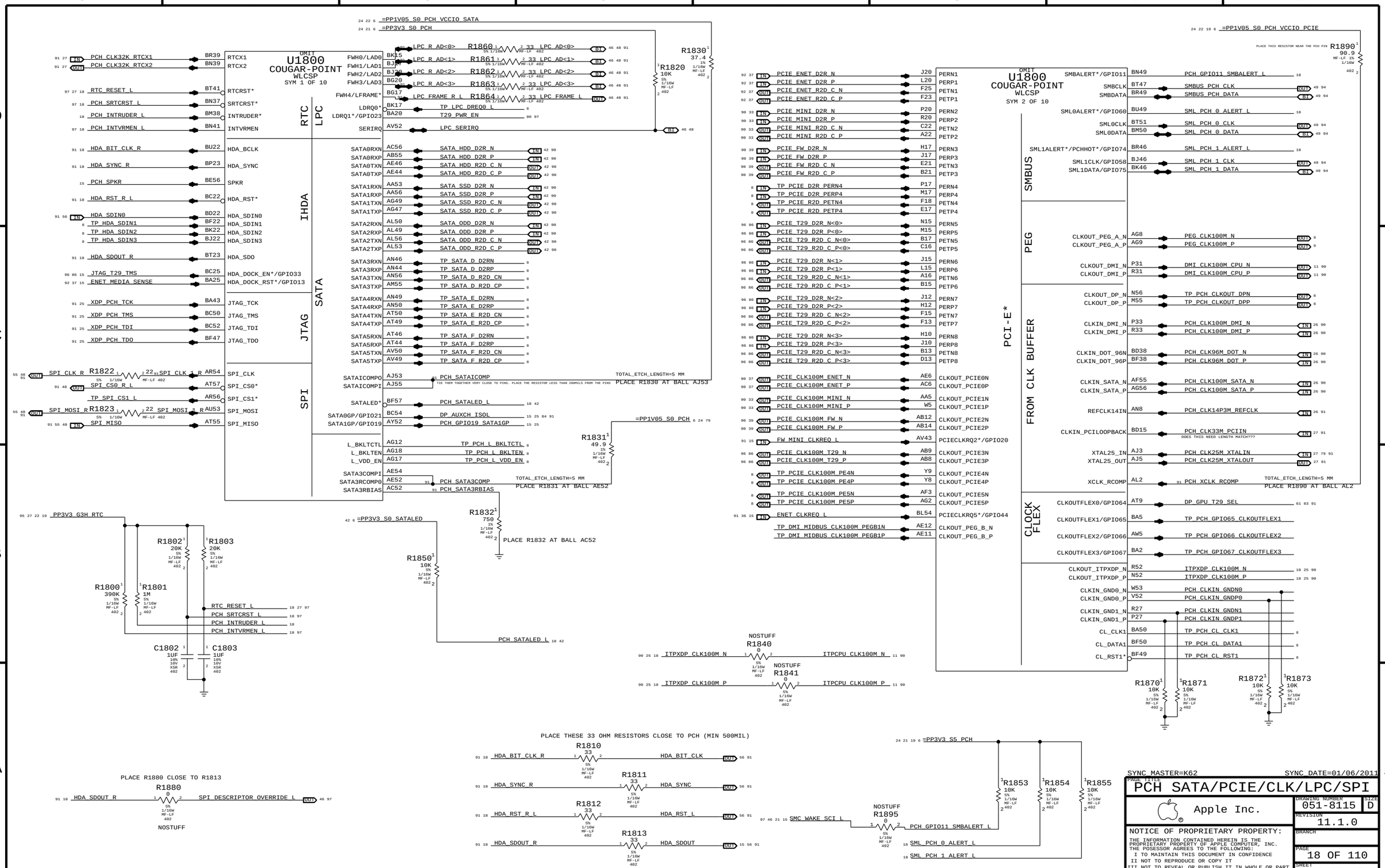


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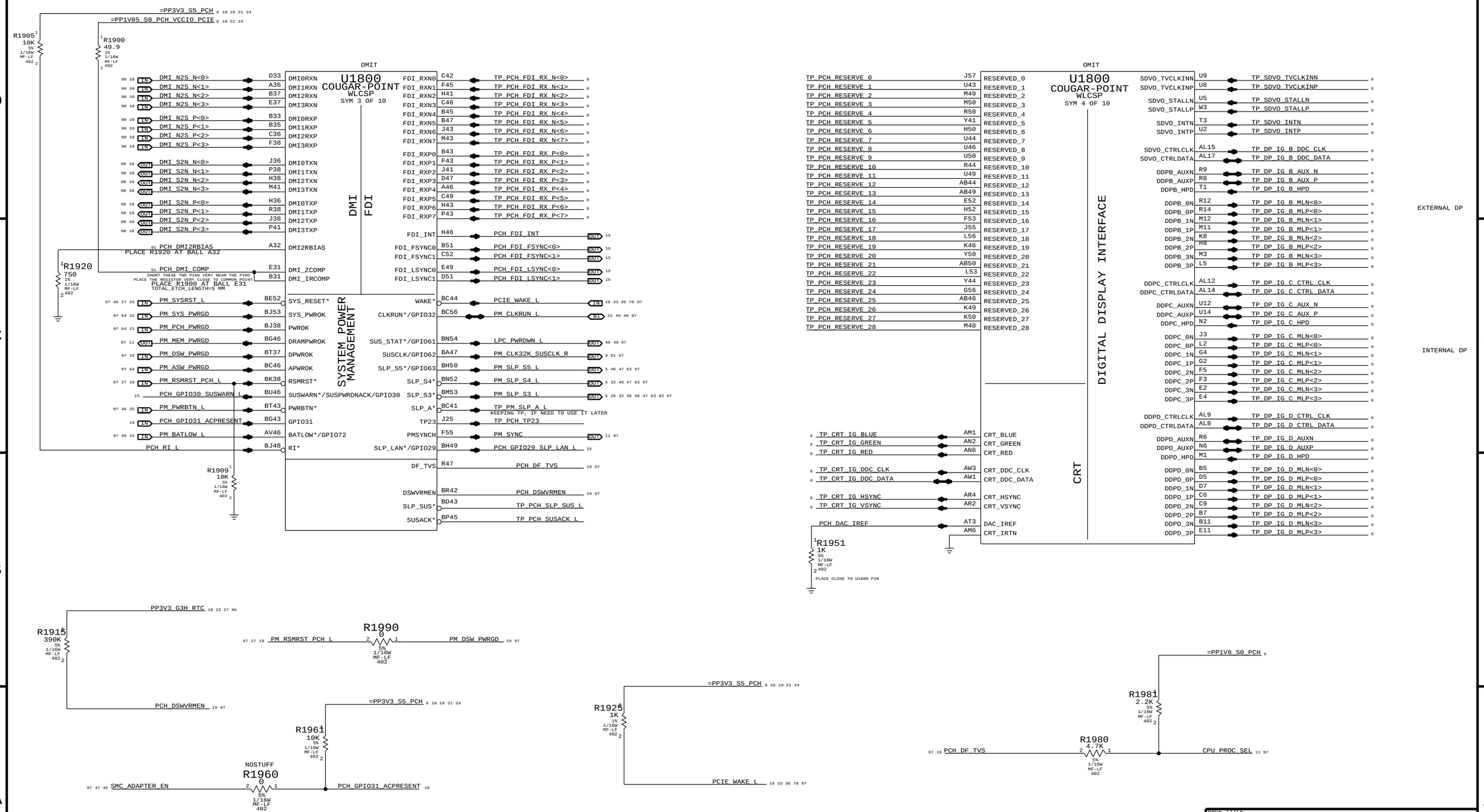


PAGE TITLE
# PCH DMI/FDI/GRAPHICS

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DRAWING NUMBER 051-8115 SIZE D

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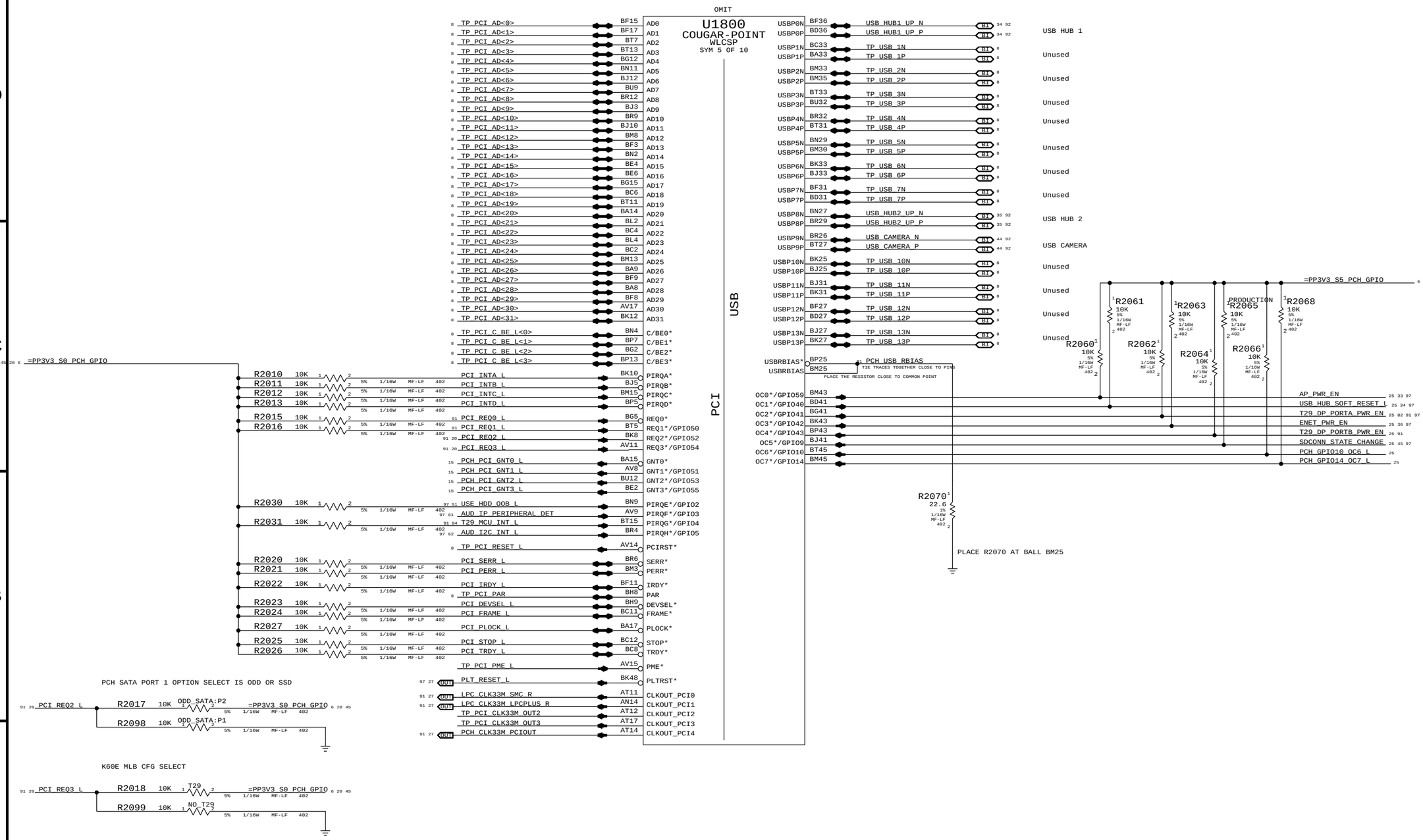


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PAGE TITLE
PCH PCI/FLASHCACHE/USB

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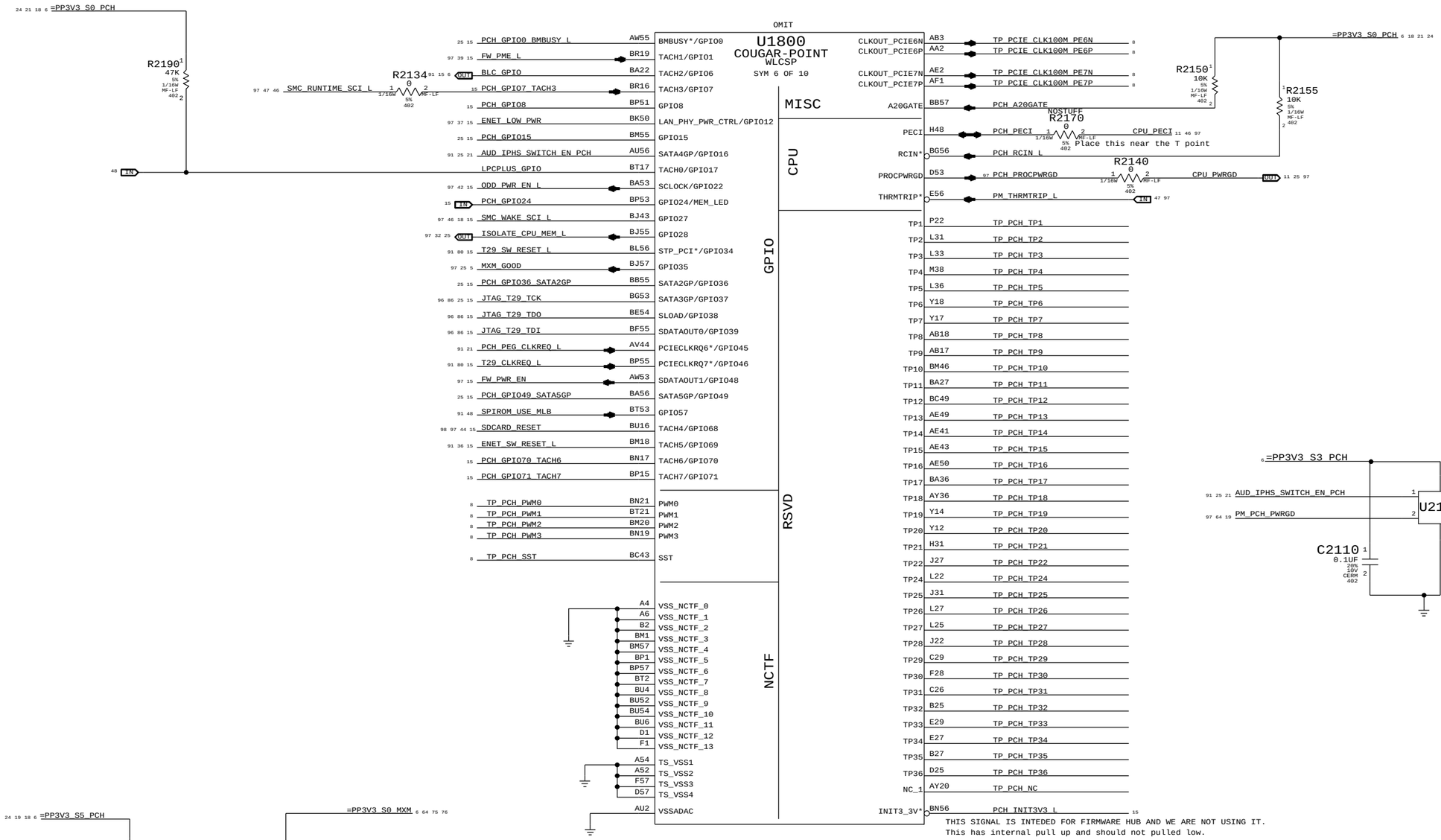


MXM CLKREQ ISOLATION

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
# PCH MISC

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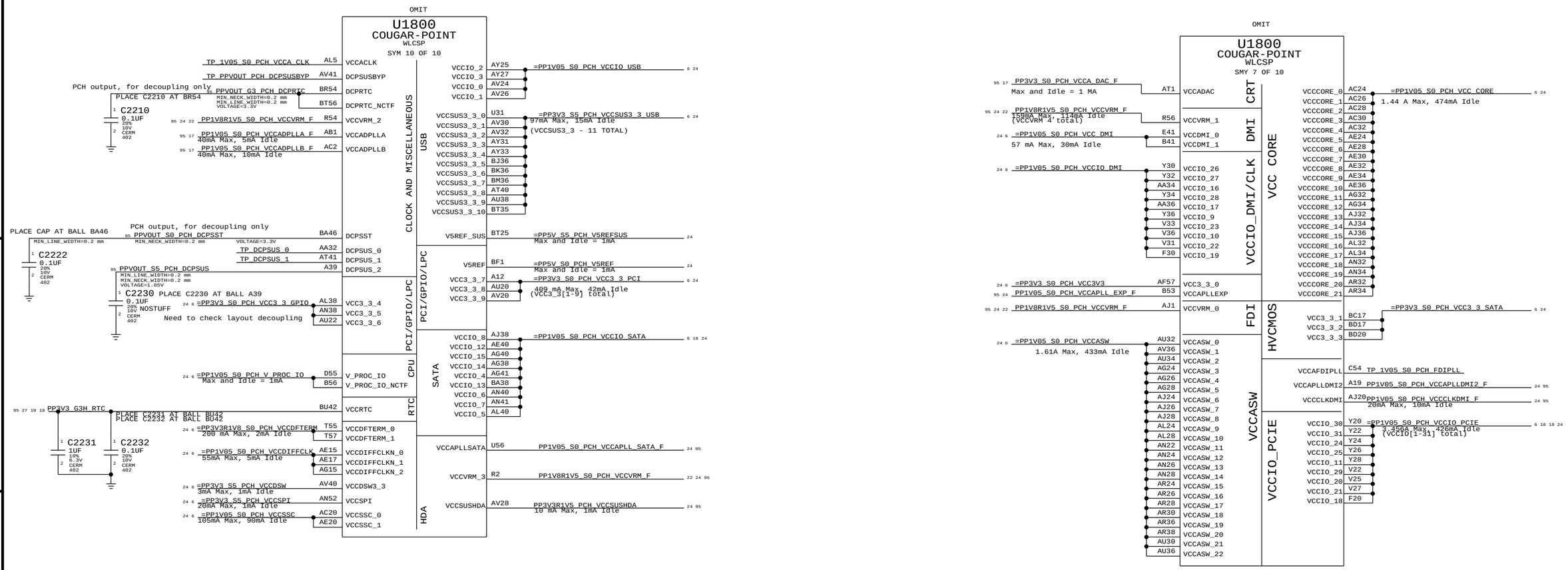


PAGE TITLE
# PCH POWER

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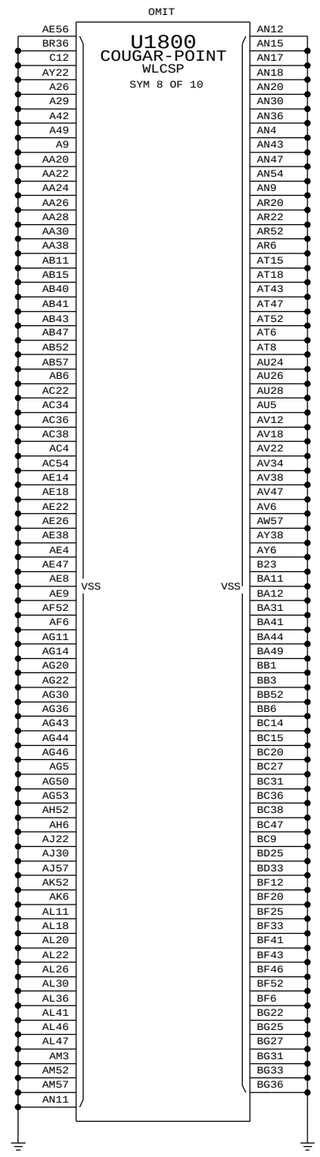


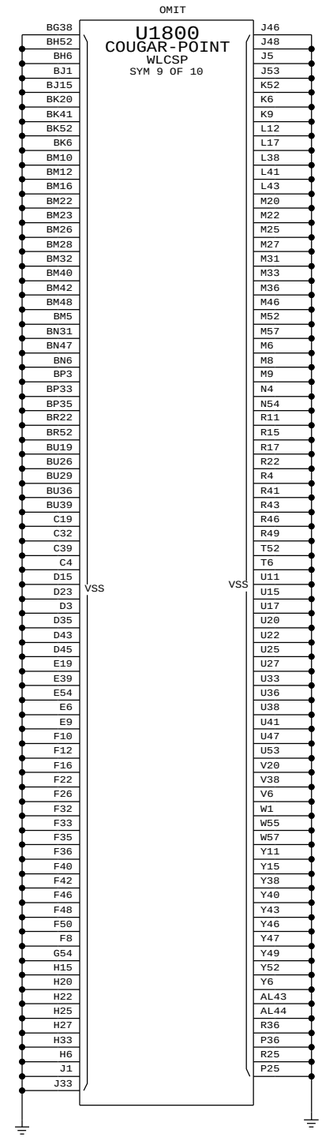


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PAGE TITLE
# PCH GROUNDS

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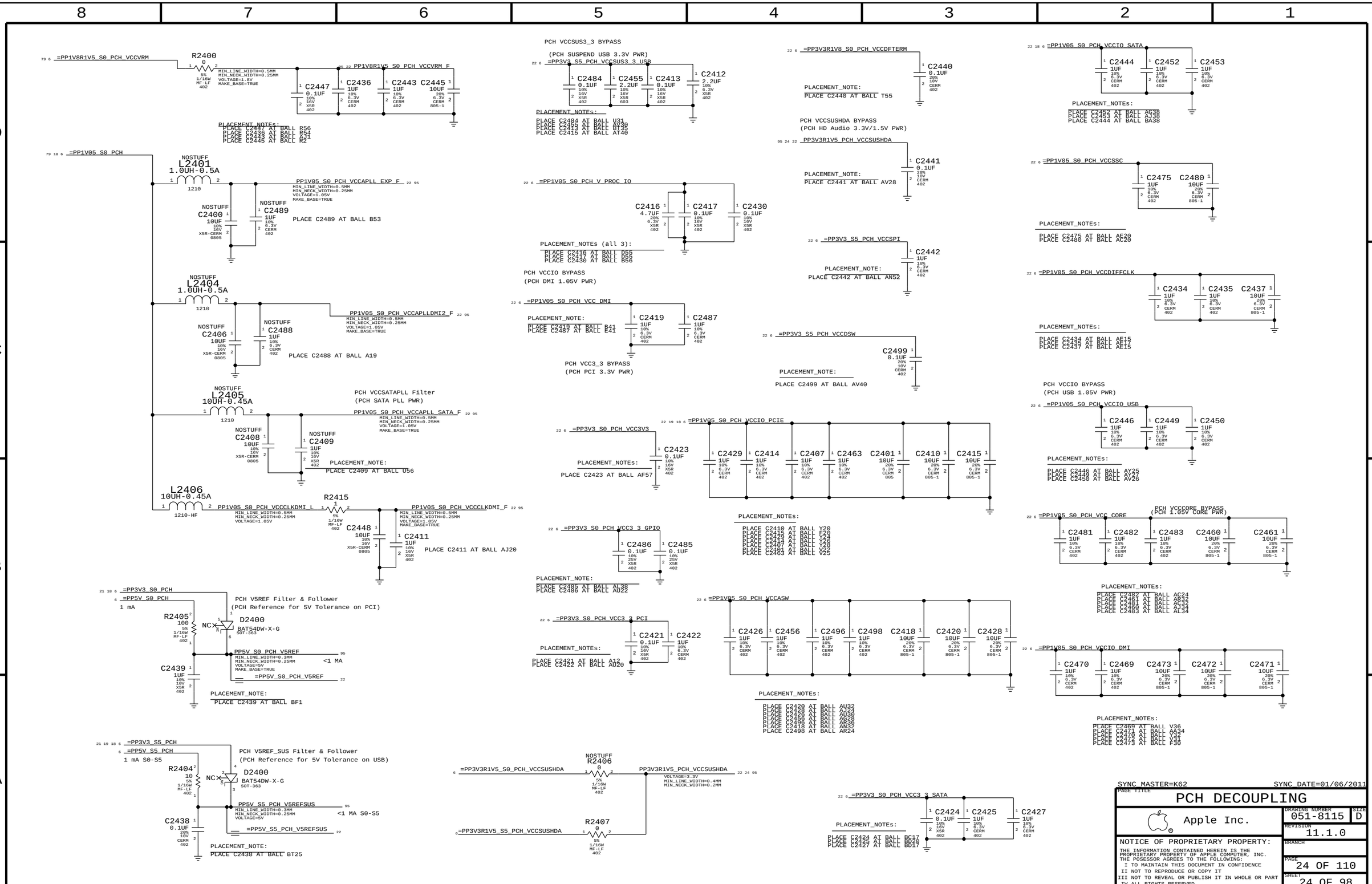


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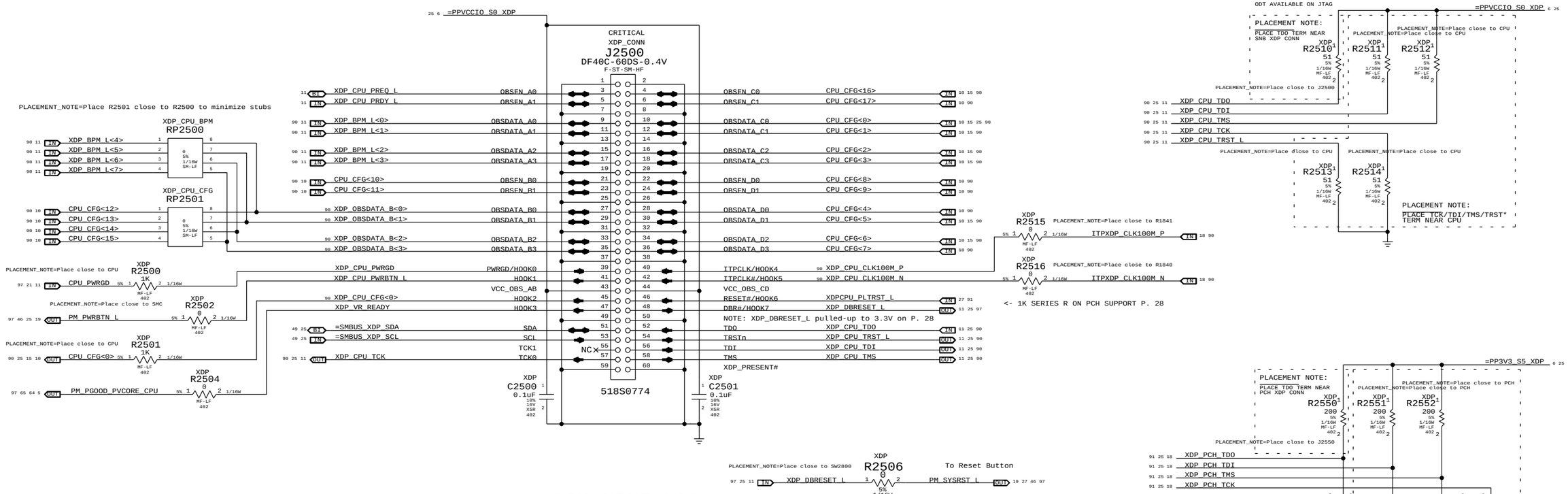
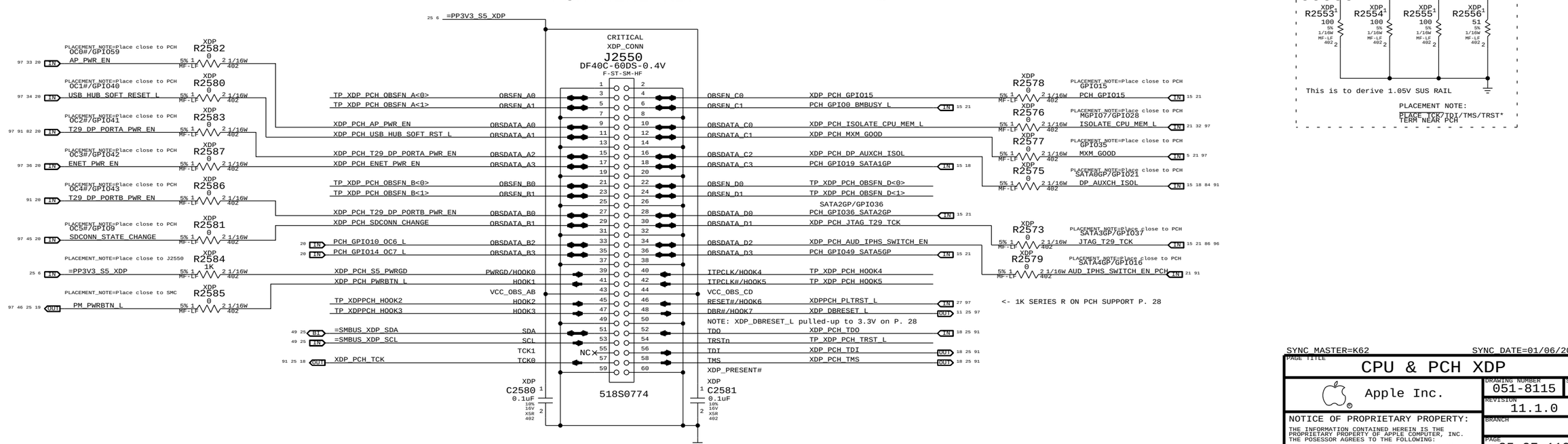
# PROCESSOR MINI XDP




# PCH MINI XDP

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| | |
|---|---|
| PAGE TITLE | CPU & PCH XDP |
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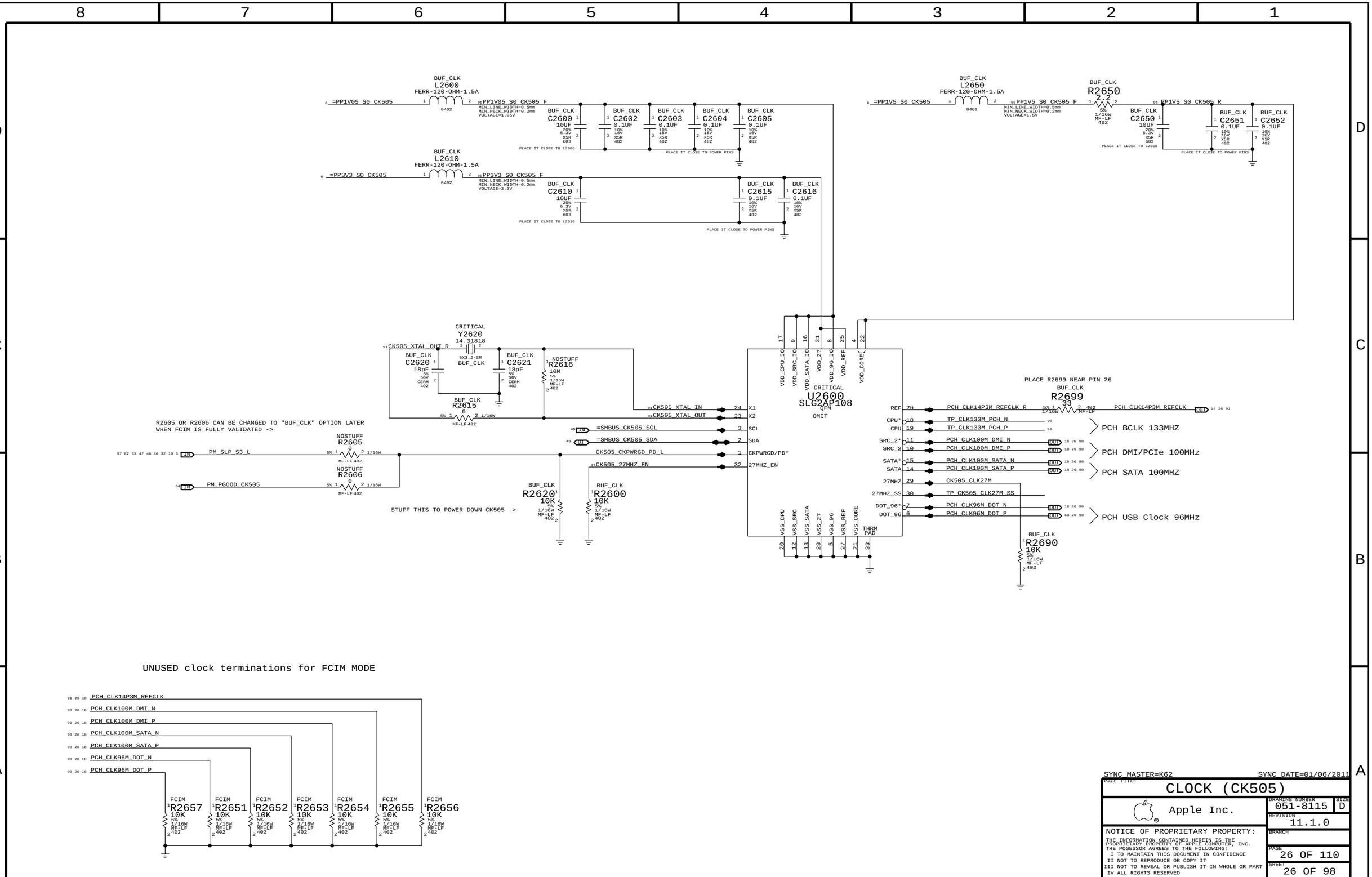


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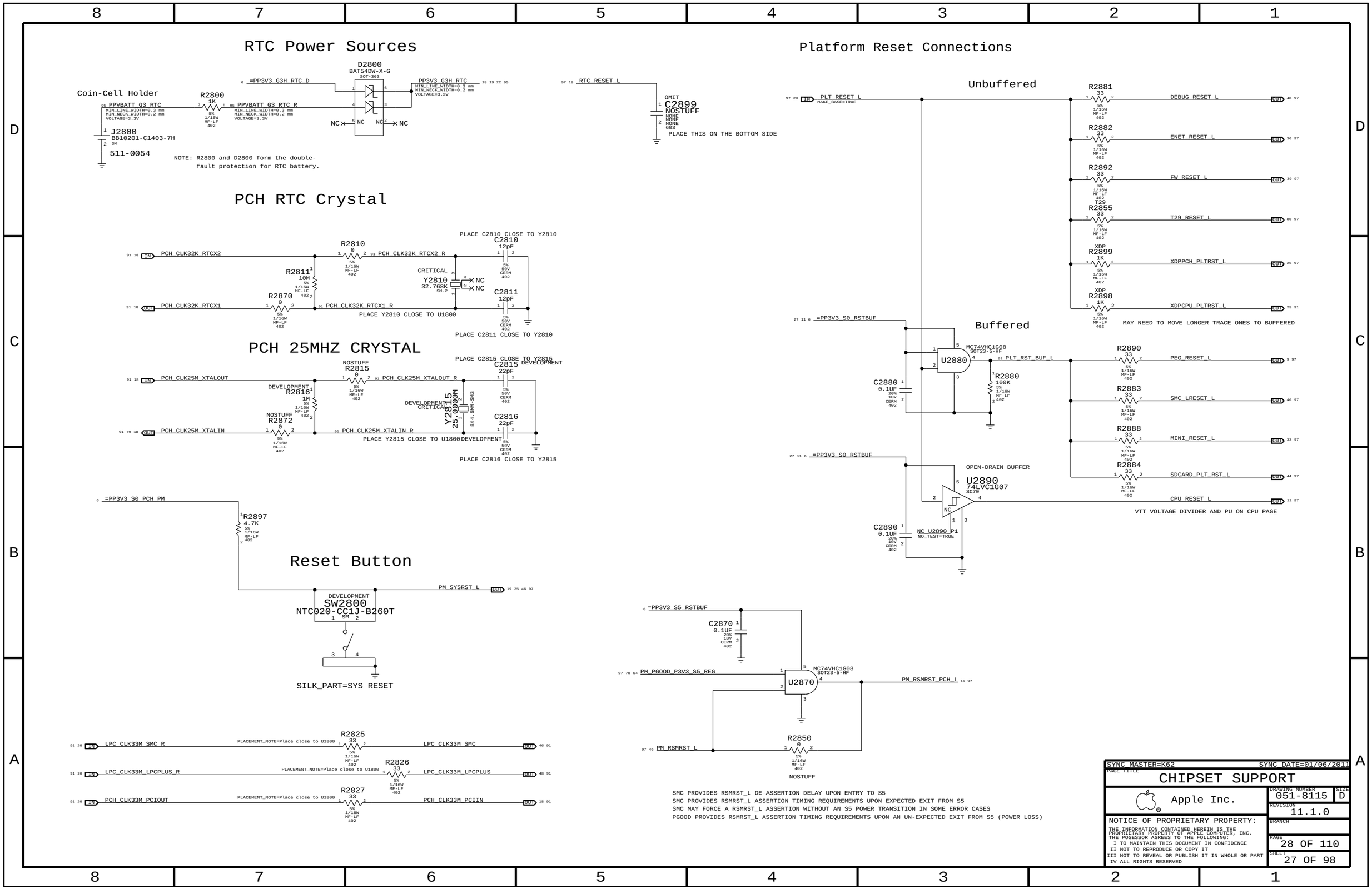
RTC Power Sources
Coin-Cell Holder
J2800
BB10201-C1403-7H
511-0054
PPVBATT_G3_RTC
R2800
1K
PPVBATT_G3_RTC_R
D2800
BAT54DW-X-G
SOT-363
=PP3V3_G3H_RTC_D
PP3V3_G3H_RTC
NC
RTC_RESET_L
OMIT
C2899
NOSTUFF
PLACE THIS ON THE BOTTOM SIDE
NOTE: R2800 and D2800 form the double-fault protection for RTC battery.
PCH RTC Crystal
PCH_CLK32K_RTCX2
PCH_CLK32K_RTCX1
R2810
R2811
10M
R2870
PCH_CLK32K_RTCX2_R
PCH_CLK32K_RTCX1_R
CRITICAL
Y2810
32.768K
C2810
12pF
C2811
12pF
PLACE C2810 CLOSE TO Y2810
PLACE Y2810 CLOSE TO U1800
PLACE C2811 CLOSE TO Y2810
PCH 25MHZ CRYSTAL
PCH_CLK25M_XTALOUT
PCH_CLK25M_XTALIN
NOSTUFF
R2815
DEVELOPMENT
R2816
1M
R2872
PCH_CLK25M_XTALOUT_R
PCH_CLK25M_XTALIN_R
Y2815
25.0000M
C2815
22pF
C2816
22pF
PLACE C2815 CLOSE TO Y2815
PLACE Y2815 CLOSE TO U1800
PLACE C2816 CLOSE TO Y2815
Platform Reset Connections
Unbuffered
PLT_RESET_L
MAKE_BASE=TRUE
R2881
33
DEBUG_RESET_L
R2882
ENET_RESET_L
R2892
FW_RESET_L
T29
R2855
T29_RESET_L
XDP
R2899
1K
XDPPCH_PLTRST_L
R2898
XDPCPU_PLTRST_L
MAY NEED TO MOVE LONGER TRACE ONES TO BUFFERED
Buffered
=PP3V3_S0_RSTBUF
U2880
MC74VHC1G08
SOT23-5-HF
PLT_RST_BUF_L
C2880
0.1UF
R2880
100K
R2890
PEG_RESET_L
R2883
SMC_LRESET_L
R2888
MINI_RESET_L
R2884
SDCARD_PLT_RST_L
OPEN-DRAIN BUFFER
U2890
74LVC1G07
SC70
CPU_RESET_L
VTT VOLTAGE DIVIDER AND PU ON CPU PAGE
C2890
0.1UF
NC_U2890_P1
NO_TEST=TRUE
=PP3V3_S0_PCH_PM
R2897
4.7K
Reset Button
PM_SYSRST_L
DEVELOPMENT
SW2800
NTC020-CC1J-B260T
SILK_PART=SYS RESET
=PP3V3_S5_RSTBUF
C2870
0.1UF
PM_PGOOD_P3V3_S5_REG
U2870
PM_RSMRST_PCH_L
R2850
PM_RSMRST_L
NOSTUFF
LPC_CLK33M_SMC_R
LPC_CLK33M_SMC
R2825
33
LPC_CLK33M_LPCPLUS_R
LPC_CLK33M_LPCPLUS
R2826
PCH_CLK33M_PCIOUT
PCH_CLK33M_PCIIN
R2827
PLACEMENT_NOTE=Place close to U1800
SMC PROVIDES RSMRST_L DE-ASSERTION DELAY UPON ENTRY TO S5
SMC PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON EXPECTED EXIT FROM S5
SMC MAY FORCE A RSMRST_L ASSERTION WITHOUT AN S5 POWER TRANSITION IN SOME ERROR CASES
PGOOD PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON AN UN-EXPECTED EXIT FROM S5 (POWER LOSS)
SYNC_MASTER=K62
SYNC_DATE=01/06/2011
PAGE TITLE
CHIPSET SUPPORT
Apple Inc.
DRAWING NUMBER
051-8115
SIZE
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REVISION
11.1.0
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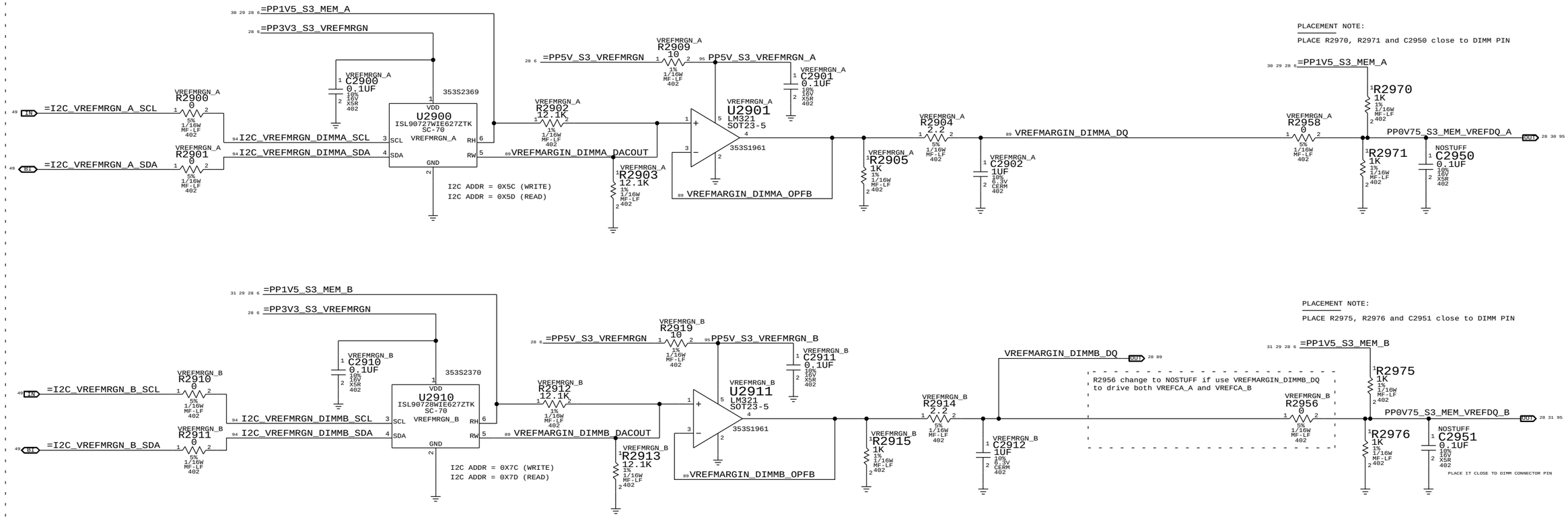


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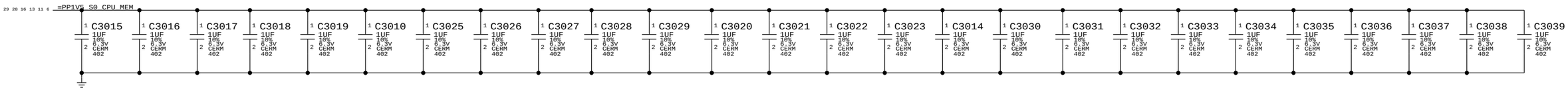
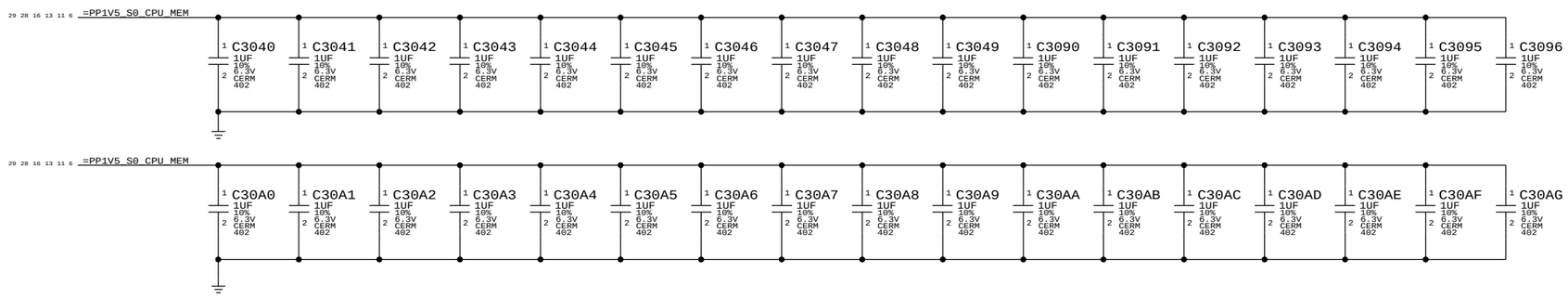
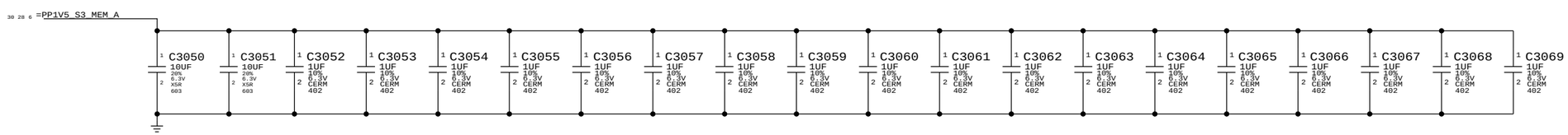
DIMM A (CLOSER TO CPU) CAPS TO STITCH 1V5_CPU_MEM TO GND NEAR DIMM DIMM B (FURTHER FROM CPU)



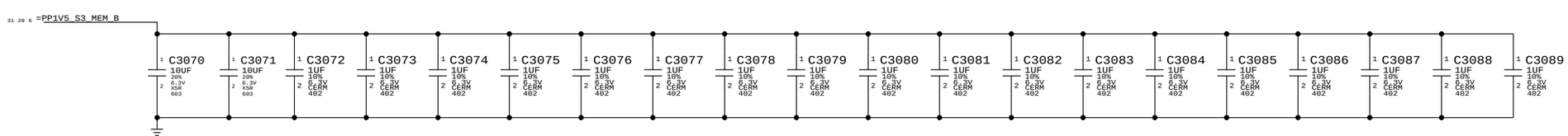

EXTRA DECOUPLING CAPS FOR 1V5_CPU_MEM RAIL




DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL A DIMM CONNECTOR




DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL B DIMM CONNECTOR

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PAGE TITLE
MEMORY CAPS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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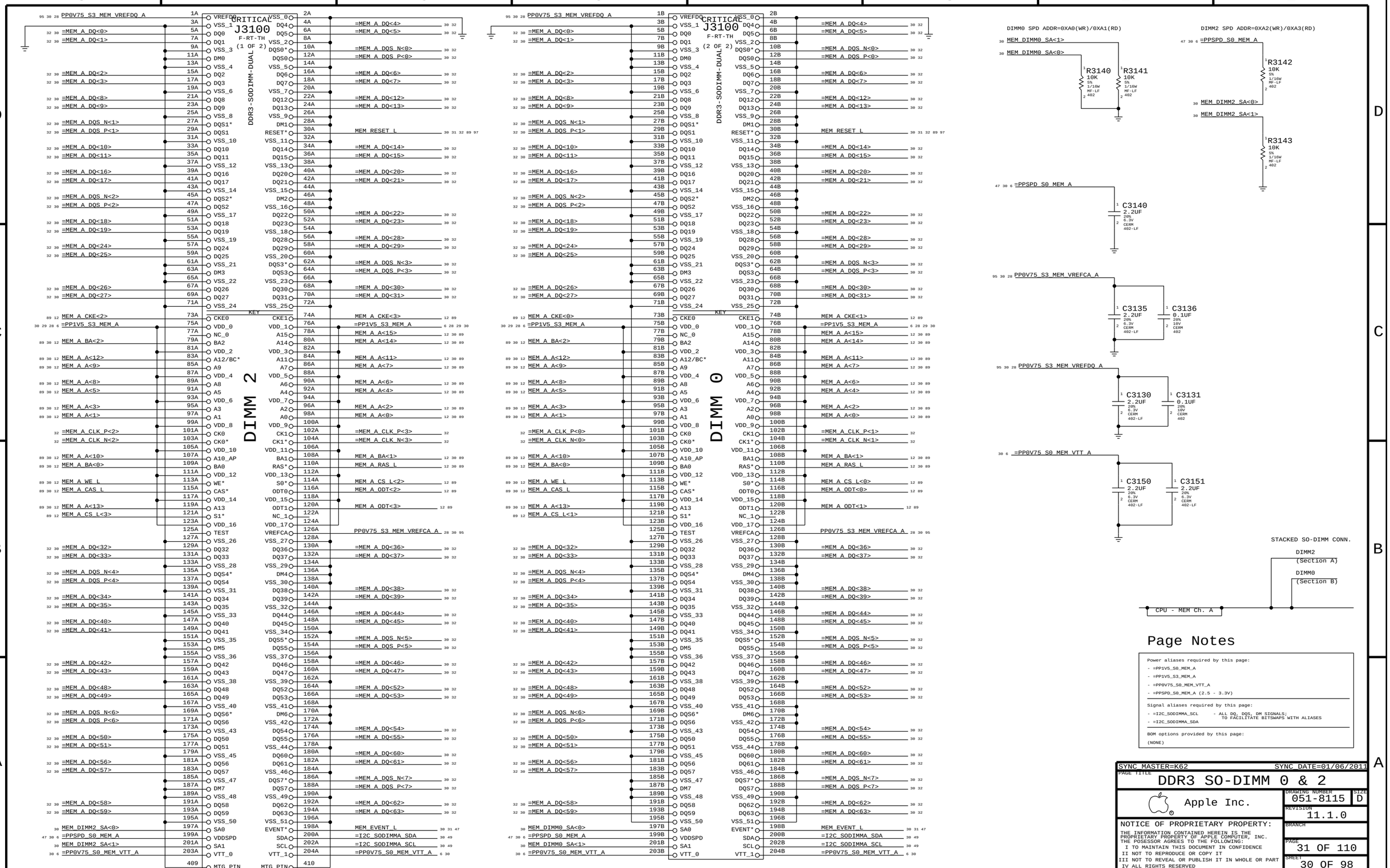


## Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

| | |
|---|---|
| SYNC_MASTER=K62 | SYNC_DATE=01/06/2011 |
| PAGE TITLE: DDR3 SO-DIMM 0 & 2 | |
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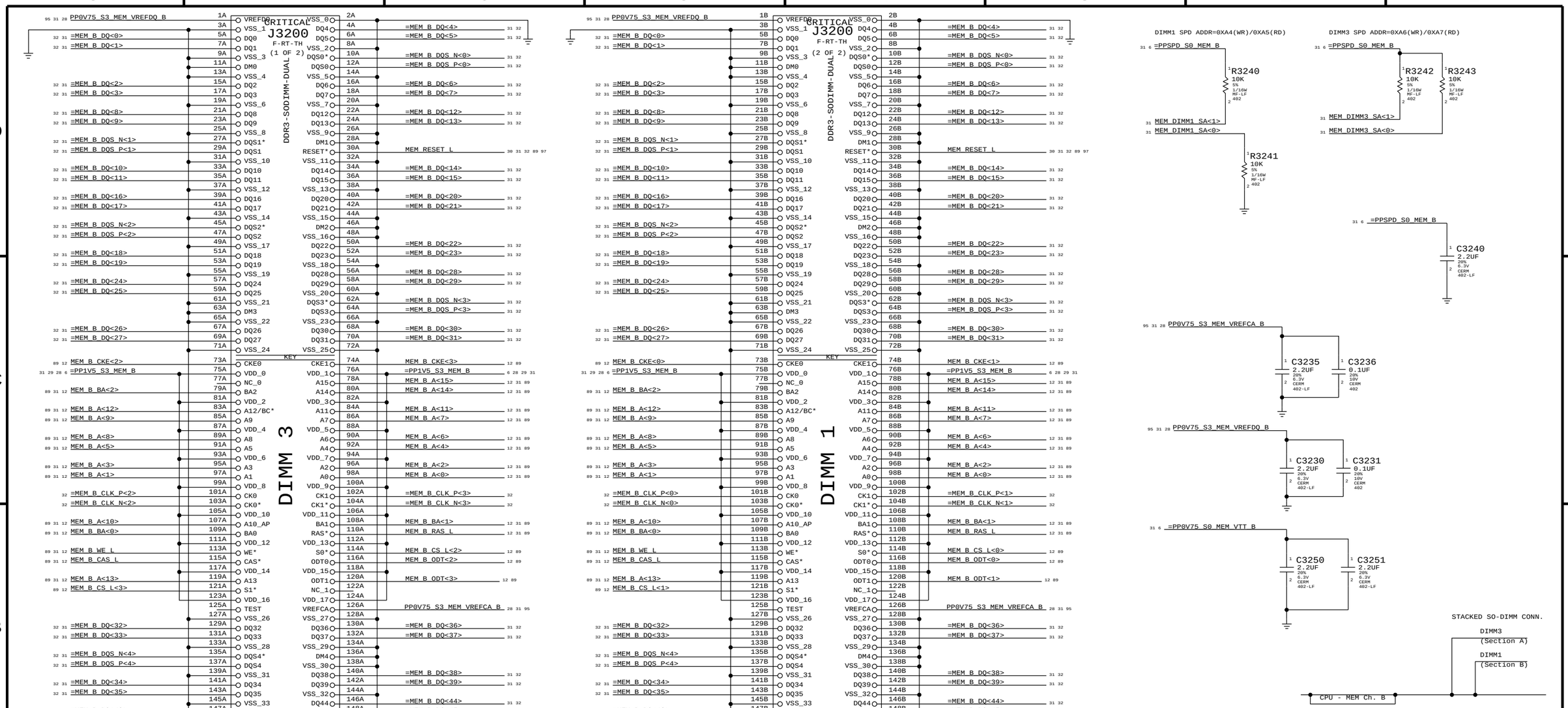


## Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

- ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

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|---|---|
| SYNC_MASTER=K62 | SYNC_DATE=01/06/2011 |
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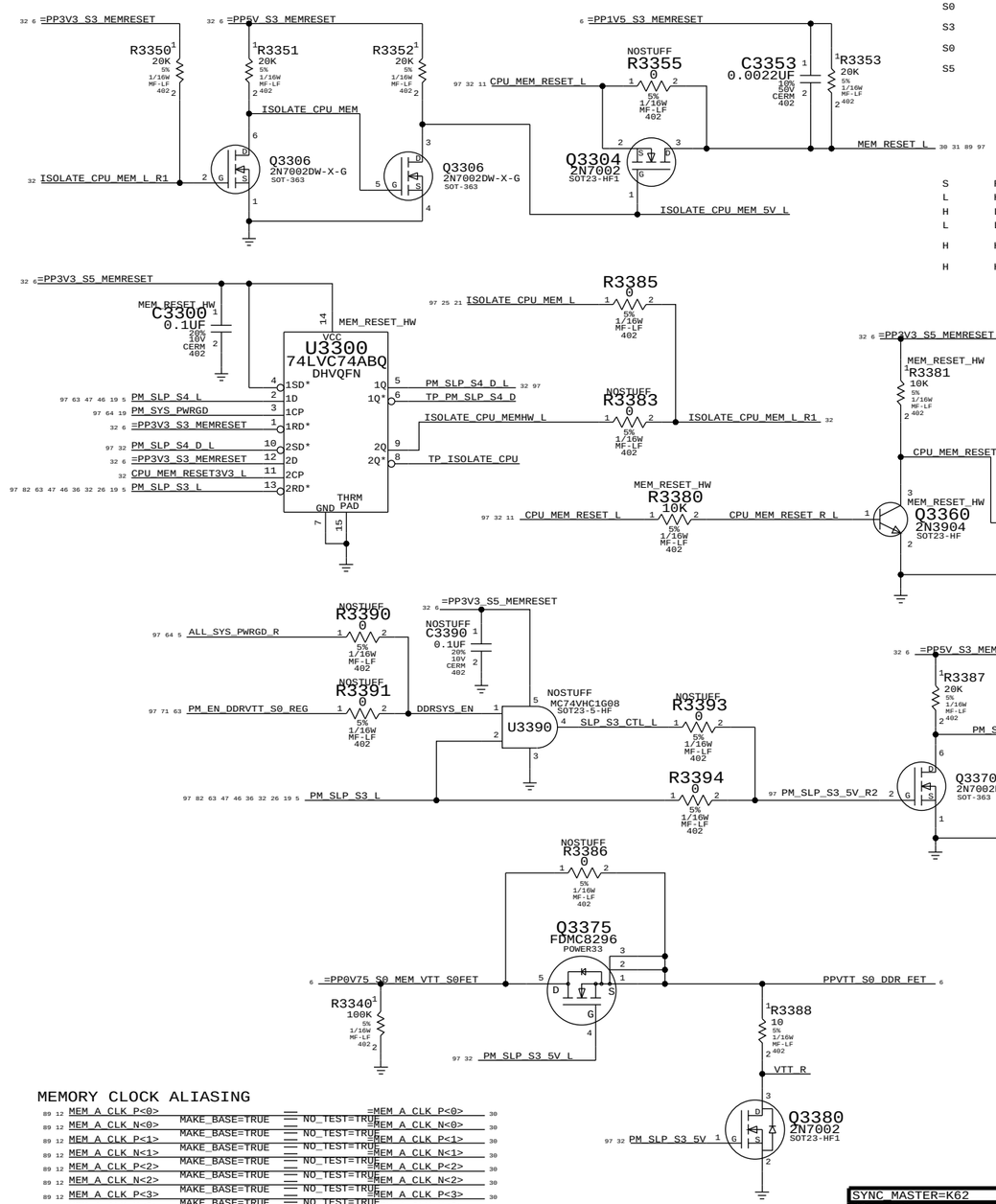
| | SHEET: 31 OF 98 |

# DDR3 RESET SUPPORT

SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

| | CPU_RESET_L | ISOLATE_L | MEM_RESET_L |
|---|---|---|---|
| S5 | 0 | 3.3V | 0 |
| S0 | 0 | 3.3V | 0 |
| S0 | 1.5V | 3.3V | 1.5V |
| S3 | 0 | 0 | 1.5V |
| S0 | 1.5V | 3.3V | 1.5V |
| S5 | 0 | 3.3V | 0 |

| S | R | CLK | D | Q | QB |
|---|---|---|---|---|---|
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | POSEDGE | L | L | H |
| H | H | POSEDGE | H | H | L |




## MEMORY CLOCK ALIASING

| | | | |
|---|---|---|---|
| MEM_A_CLK_P<0> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_CLK_P<0> |
| MEM_A_CLK_N<0> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_CLK_N<0> |
| MEM_A_CLK_P<1> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_CLK_P<1> |
| MEM_A_CLK_N<1> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_CLK_N<1> |
| MEM_A_CLK_P<2> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_CLK_P<2> |
| MEM_A_CLK_N<2> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_CLK_N<2> |
| MEM_A_CLK_P<3> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_CLK_P<3> |
| MEM_A_CLK_N<3> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_CLK_N<3> |
| MEM_B_CLK_P<0> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_CLK_P<0> |
| MEM_B_CLK_N<0> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_CLK_N<0> |
| MEM_B_CLK_P<1> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_CLK_P<1> |
| MEM_B_CLK_N<1> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_CLK_N<1> |
| MEM_B_CLK_P<2> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_CLK_P<2> |
| MEM_B_CLK_N<2> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_CLK_N<2> |
| MEM_B_CLK_P<3> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_CLK_P<3> |
| MEM_B_CLK_N<3> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_CLK_N<3> |

## CPU CHANNEL A DQS 0 -> DIMM A DQS 7

| | | | |
|---|---|---|---|
| MEM_A_DQS_N<0> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_N<7> |
| MEM_A_DQS_P<0> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_P<7> |
| MEM_A_DQ<7> | MAKE_BASE=TRUE | | =MEM_A_DQ<57> |
| MEM_A_DQ<6> | MAKE_BASE=TRUE | | =MEM_A_DQ<56> |
| MEM_A_DQ<5> | MAKE_BASE=TRUE | | =MEM_A_DQ<58> |
| MEM_A_DQ<4> | MAKE_BASE=TRUE | | =MEM_A_DQ<59> |
| MEM_A_DQ<3> | MAKE_BASE=TRUE | | =MEM_A_DQ<60> |
| MEM_A_DQ<2> | MAKE_BASE=TRUE | | =MEM_A_DQ<61> |
| MEM_A_DQ<1> | MAKE_BASE=TRUE | | =MEM_A_DQ<62> |
| MEM_A_DQ<0> | MAKE_BASE=TRUE | | =MEM_A_DQ<63> |

## CPU CHANNEL A DQS 1 -> DIMM A DQS 6

| | | | |
|---|---|---|---|
| MEM_A_DQS_N<1> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_N<6> |
| MEM_A_DQS_P<1> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_P<6> |
| MEM_A_DQ<15> | MAKE_BASE=TRUE | | =MEM_A_DQ<49> |
| MEM_A_DQ<14> | MAKE_BASE=TRUE | | =MEM_A_DQ<52> |
| MEM_A_DQ<13> | MAKE_BASE=TRUE | | =MEM_A_DQ<51> |
| MEM_A_DQ<12> | MAKE_BASE=TRUE | | =MEM_A_DQ<50> |
| MEM_A_DQ<11> | MAKE_BASE=TRUE | | =MEM_A_DQ<48> |
| MEM_A_DQ<10> | MAKE_BASE=TRUE | | =MEM_A_DQ<53> |
| MEM_A_DQ<9> | MAKE_BASE=TRUE | | =MEM_A_DQ<55> |
| MEM_A_DQ<8> | MAKE_BASE=TRUE | | =MEM_A_DQ<54> |

## CPU CHANNEL A DQS 2 -> DIMM A DQS 5

| | | | |
|---|---|---|---|
| MEM_A_DQS_N<2> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_N<5> |
| MEM_A_DQS_P<2> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_P<5> |
| MEM_A_DQ<23> | MAKE_BASE=TRUE | | =MEM_A_DQ<40> |
| MEM_A_DQ<22> | MAKE_BASE=TRUE | | =MEM_A_DQ<45> |
| MEM_A_DQ<21> | MAKE_BASE=TRUE | | =MEM_A_DQ<46> |
| MEM_A_DQ<20> | MAKE_BASE=TRUE | | =MEM_A_DQ<47> |
| MEM_A_DQ<19> | MAKE_BASE=TRUE | | =MEM_A_DQ<41> |
| MEM_A_DQ<18> | MAKE_BASE=TRUE | | =MEM_A_DQ<44> |
| MEM_A_DQ<17> | MAKE_BASE=TRUE | | =MEM_A_DQ<43> |
| MEM_A_DQ<16> | MAKE_BASE=TRUE | | =MEM_A_DQ<42> |

## CPU CHANNEL A DQS 3 -> DIMM A DQS 4

| | | | |
|---|---|---|---|
| MEM_A_DQS_N<3> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_N<4> |
| MEM_A_DQS_P<3> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_P<4> |
| MEM_A_DQ<31> | MAKE_BASE=TRUE | | =MEM_A_DQ<37> |
| MEM_A_DQ<30> | MAKE_BASE=TRUE | | =MEM_A_DQ<33> |
| MEM_A_DQ<29> | MAKE_BASE=TRUE | | =MEM_A_DQ<35> |
| MEM_A_DQ<28> | MAKE_BASE=TRUE | | =MEM_A_DQ<34> |
| MEM_A_DQ<27> | MAKE_BASE=TRUE | | =MEM_A_DQ<36> |
| MEM_A_DQ<26> | MAKE_BASE=TRUE | | =MEM_A_DQ<32> |
| MEM_A_DQ<25> | MAKE_BASE=TRUE | | =MEM_A_DQ<38> |
| MEM_A_DQ<24> | MAKE_BASE=TRUE | | =MEM_A_DQ<39> |

## CPU CHANNEL A DQS 4 -> DIMM A DQS 3

| | | | |
|---|---|---|---|
| MEM_A_DQS_N<4> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_N<3> |
| MEM_A_DQS_P<4> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_P<3> |
| MEM_A_DQ<39> | MAKE_BASE=TRUE | | =MEM_A_DQ<28> |
| MEM_A_DQ<38> | MAKE_BASE=TRUE | | =MEM_A_DQ<29> |
| MEM_A_DQ<37> | MAKE_BASE=TRUE | | =MEM_A_DQ<27> |
| MEM_A_DQ<36> | MAKE_BASE=TRUE | | =MEM_A_DQ<31> |
| MEM_A_DQ<35> | MAKE_BASE=TRUE | | =MEM_A_DQ<25> |
| MEM_A_DQ<34> | MAKE_BASE=TRUE | | =MEM_A_DQ<24> |
| MEM_A_DQ<33> | MAKE_BASE=TRUE | | =MEM_A_DQ<26> |
| MEM_A_DQ<32> | MAKE_BASE=TRUE | | =MEM_A_DQ<30> |

## CPU CHANNEL A DQS 5 -> DIMM A DQS 2

| | | | |
|---|---|---|---|
| MEM_A_DQS_N<5> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_N<2> |
| MEM_A_DQS_P<5> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_P<2> |
| MEM_A_DQ<47> | MAKE_BASE=TRUE | | =MEM_A_DQ<17> |
| MEM_A_DQ<46> | MAKE_BASE=TRUE | | =MEM_A_DQ<16> |
| MEM_A_DQ<45> | MAKE_BASE=TRUE | | =MEM_A_DQ<22> |
| MEM_A_DQ<44> | MAKE_BASE=TRUE | | =MEM_A_DQ<23> |
| MEM_A_DQ<43> | MAKE_BASE=TRUE | | =MEM_A_DQ<21> |
| MEM_A_DQ<42> | MAKE_BASE=TRUE | | =MEM_A_DQ<20> |
| MEM_A_DQ<41> | MAKE_BASE=TRUE | | =MEM_A_DQ<18> |
| MEM_A_DQ<40> | MAKE_BASE=TRUE | | =MEM_A_DQ<19> |

## CPU CHANNEL A DQS 6 -> DIMM A DQS 1

| | | | |
|---|---|---|---|
| MEM_A_DQS_N<6> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_N<1> |
| MEM_A_DQS_P<6> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_P<1> |
| MEM_A_DQ<55> | MAKE_BASE=TRUE | | =MEM_A_DQ<12> |
| MEM_A_DQ<54> | MAKE_BASE=TRUE | | =MEM_A_DQ<13> |
| MEM_A_DQ<53> | MAKE_BASE=TRUE | | =MEM_A_DQ<10> |
| MEM_A_DQ<52> | MAKE_BASE=TRUE | | =MEM_A_DQ<15> |
| MEM_A_DQ<51> | MAKE_BASE=TRUE | | =MEM_A_DQ<8> |
| MEM_A_DQ<50> | MAKE_BASE=TRUE | | =MEM_A_DQ<9> |
| MEM_A_DQ<49> | MAKE_BASE=TRUE | | =MEM_A_DQ<11> |
| MEM_A_DQ<48> | MAKE_BASE=TRUE | | =MEM_A_DQ<14> |

## CPU CHANNEL A DQS 7 -> DIMM A DQS 0

| | | | |
|---|---|---|---|
| MEM_A_DQS_N<7> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_N<0> |
| MEM_A_DQS_P<7> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_A_DQS_P<0> |
| MEM_A_DQ<63> | MAKE_BASE=TRUE | | =MEM_A_DQ<5> |
| MEM_A_DQ<62> | MAKE_BASE=TRUE | | =MEM_A_DQ<4> |
| MEM_A_DQ<61> | MAKE_BASE=TRUE | | =MEM_A_DQ<3> |
| MEM_A_DQ<60> | MAKE_BASE=TRUE | | =MEM_A_DQ<2> |
| MEM_A_DQ<59> | MAKE_BASE=TRUE | | =MEM_A_DQ<1> |
| MEM_A_DQ<58> | MAKE_BASE=TRUE | | =MEM_A_DQ<0> |
| MEM_A_DQ<57> | MAKE_BASE=TRUE | | =MEM_A_DQ<7> |
| MEM_A_DQ<56> | MAKE_BASE=TRUE | | =MEM_A_DQ<6> |

## CPU CHANNEL B DQS 0 -> DIMM B DQS 7

| | | | |
|---|---|---|---|
| MEM_B_DQS_N<0> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_N<7> |
| MEM_B_DQS_P<0> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_P<7> |
| MEM_B_DQ<7> | MAKE_BASE=TRUE | | =MEM_B_DQ<61> |
| MEM_B_DQ<6> | MAKE_BASE=TRUE | | =MEM_B_DQ<60> |
| MEM_B_DQ<5> | MAKE_BASE=TRUE | | =MEM_B_DQ<62> |
| MEM_B_DQ<4> | MAKE_BASE=TRUE | | =MEM_B_DQ<63> |
| MEM_B_DQ<3> | MAKE_BASE=TRUE | | =MEM_B_DQ<56> |
| MEM_B_DQ<2> | MAKE_BASE=TRUE | | =MEM_B_DQ<57> |
| MEM_B_DQ<1> | MAKE_BASE=TRUE | | =MEM_B_DQ<58> |
| MEM_B_DQ<0> | MAKE_BASE=TRUE | | =MEM_B_DQ<59> |

## CPU CHANNEL B DQS 1 -> DIMM B DQS 6

| | | | |
|---|---|---|---|
| MEM_B_DQS_N<1> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_N<6> |
| MEM_B_DQS_P<1> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_P<6> |
| MEM_B_DQ<15> | MAKE_BASE=TRUE | | =MEM_B_DQ<51> |
| MEM_B_DQ<14> | MAKE_BASE=TRUE | | =MEM_B_DQ<54> |
| MEM_B_DQ<13> | MAKE_BASE=TRUE | | =MEM_B_DQ<53> |
| MEM_B_DQ<12> | MAKE_BASE=TRUE | | =MEM_B_DQ<52> |
| MEM_B_DQ<11> | MAKE_BASE=TRUE | | =MEM_B_DQ<48> |
| MEM_B_DQ<10> | MAKE_BASE=TRUE | | =MEM_B_DQ<49> |
| MEM_B_DQ<9> | MAKE_BASE=TRUE | | =MEM_B_DQ<50> |
| MEM_B_DQ<8> | MAKE_BASE=TRUE | | =MEM_B_DQ<55> |

## CPU CHANNEL B DQS 2 -> DIMM B DQS 5

| | | | |
|---|---|---|---|
| MEM_B_DQS_N<2> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_N<5> |
| MEM_B_DQS_P<2> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_P<5> |
| MEM_B_DQ<23> | MAKE_BASE=TRUE | | =MEM_B_DQ<45> |
| MEM_B_DQ<22> | MAKE_BASE=TRUE | | =MEM_B_DQ<40> |
| MEM_B_DQ<21> | MAKE_BASE=TRUE | | =MEM_B_DQ<42> |
| MEM_B_DQ<20> | MAKE_BASE=TRUE | | =MEM_B_DQ<47> |
| MEM_B_DQ<19> | MAKE_BASE=TRUE | | =MEM_B_DQ<44> |
| MEM_B_DQ<18> | MAKE_BASE=TRUE | | =MEM_B_DQ<41> |
| MEM_B_DQ<17> | MAKE_BASE=TRUE | | =MEM_B_DQ<46> |
| MEM_B_DQ<16> | MAKE_BASE=TRUE | | =MEM_B_DQ<43> |

## CPU CHANNEL B DQS 3 -> DIMM B DQS 4

| | | | |
|---|---|---|---|
| MEM_B_DQS_N<3> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_N<4> |
| MEM_B_DQS_P<3> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_P<4> |
| MEM_B_DQ<31> | MAKE_BASE=TRUE | | =MEM_B_DQ<32> |
| MEM_B_DQ<30> | MAKE_BASE=TRUE | | =MEM_B_DQ<39> |
| MEM_B_DQ<29> | MAKE_BASE=TRUE | | =MEM_B_DQ<37> |
| MEM_B_DQ<28> | MAKE_BASE=TRUE | | =MEM_B_DQ<38> |
| MEM_B_DQ<27> | MAKE_BASE=TRUE | | =MEM_B_DQ<35> |
| MEM_B_DQ<26> | MAKE_BASE=TRUE | | =MEM_B_DQ<34> |
| MEM_B_DQ<25> | MAKE_BASE=TRUE | | =MEM_B_DQ<36> |
| MEM_B_DQ<24> | MAKE_BASE=TRUE | | =MEM_B_DQ<33> |

## CPU CHANNEL B DQS 4 -> DIMM B DQS 3

| | | | |
|---|---|---|---|
| MEM_B_DQS_N<4> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_N<3> |
| MEM_B_DQS_P<4> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_P<3> |
| MEM_B_DQ<39> | MAKE_BASE=TRUE | | =MEM_B_DQ<28> |
| MEM_B_DQ<38> | MAKE_BASE=TRUE | | =MEM_B_DQ<24> |
| MEM_B_DQ<37> | MAKE_BASE=TRUE | | =MEM_B_DQ<31> |
| MEM_B_DQ<36> | MAKE_BASE=TRUE | | =MEM_B_DQ<30> |
| MEM_B_DQ<35> | MAKE_BASE=TRUE | | =MEM_B_DQ<29> |
| MEM_B_DQ<34> | MAKE_BASE=TRUE | | =MEM_B_DQ<25> |
| MEM_B_DQ<33> | MAKE_BASE=TRUE | | =MEM_B_DQ<27> |
| MEM_B_DQ<32> | MAKE_BASE=TRUE | | =MEM_B_DQ<26> |

## CPU CHANNEL B DQS 5 -> DIMM B DQS 2

| | | | |
|---|---|---|---|
| MEM_B_DQS_N<5> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_N<2> |
| MEM_B_DQS_P<5> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_P<2> |
| MEM_B_DQ<47> | MAKE_BASE=TRUE | | =MEM_B_DQ<18> |
| MEM_B_DQ<46> | MAKE_BASE=TRUE | | =MEM_B_DQ<20> |
| MEM_B_DQ<45> | MAKE_BASE=TRUE | | =MEM_B_DQ<23> |
| MEM_B_DQ<44> | MAKE_BASE=TRUE | | =MEM_B_DQ<22> |
| MEM_B_DQ<43> | MAKE_BASE=TRUE | | =MEM_B_DQ<19> |
| MEM_B_DQ<42> | MAKE_BASE=TRUE | | =MEM_B_DQ<21> |
| MEM_B_DQ<41> | MAKE_BASE=TRUE | | =MEM_B_DQ<17> |
| MEM_B_DQ<40> | MAKE_BASE=TRUE | | =MEM_B_DQ<16> |

## CPU CHANNEL B DQS 6 -> DIMM B DQS 1

| | | | |
|---|---|---|---|
| MEM_B_DQS_N<6> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_N<1> |
| MEM_B_DQS_P<6> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_P<1> |
| MEM_B_DQ<55> | MAKE_BASE=TRUE | | =MEM_B_DQ<8> |
| MEM_B_DQ<54> | MAKE_BASE=TRUE | | =MEM_B_DQ<14> |
| MEM_B_DQ<53> | MAKE_BASE=TRUE | | =MEM_B_DQ<10> |
| MEM_B_DQ<52> | MAKE_BASE=TRUE | | =MEM_B_DQ<11> |
| MEM_B_DQ<51> | MAKE_BASE=TRUE | | =MEM_B_DQ<9> |
| MEM_B_DQ<50> | MAKE_BASE=TRUE | | =MEM_B_DQ<15> |
| MEM_B_DQ<49> | MAKE_BASE=TRUE | | =MEM_B_DQ<12> |
| MEM_B_DQ<48> | MAKE_BASE=TRUE | | =MEM_B_DQ<13> |

## CPU CHANNEL B DQS 7 -> DIMM B DQS 0

| | | | |
|---|---|---|---|
| MEM_B_DQS_N<7> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_N<0> |
| MEM_B_DQS_P<7> | MAKE_BASE=TRUE | NO_TEST=TRUE | =MEM_B_DQS_P<0> |
| MEM_B_DQ<63> | MAKE_BASE=TRUE | | =MEM_B_DQ<2> |
| MEM_B_DQ<62> | MAKE_BASE=TRUE | | =MEM_B_DQ<1> |
| MEM_B_DQ<61> | MAKE_BASE=TRUE | | =MEM_B_DQ<3> |
| MEM_B_DQ<60> | MAKE_BASE=TRUE | | =MEM_B_DQ<7> |
| MEM_B_DQ<59> | MAKE_BASE=TRUE | | =MEM_B_DQ<4> |
| MEM_B_DQ<58> | MAKE_BASE=TRUE | | =MEM_B_DQ<5> |
| MEM_B_DQ<57> | MAKE_BASE=TRUE | | =MEM_B_DQ<6> |
| MEM_B_DQ<56> | MAKE_BASE=TRUE | | =MEM_B_DQ<0> |

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PAGE TITLE
DDR3 SUPPORT AND BITSWAPS

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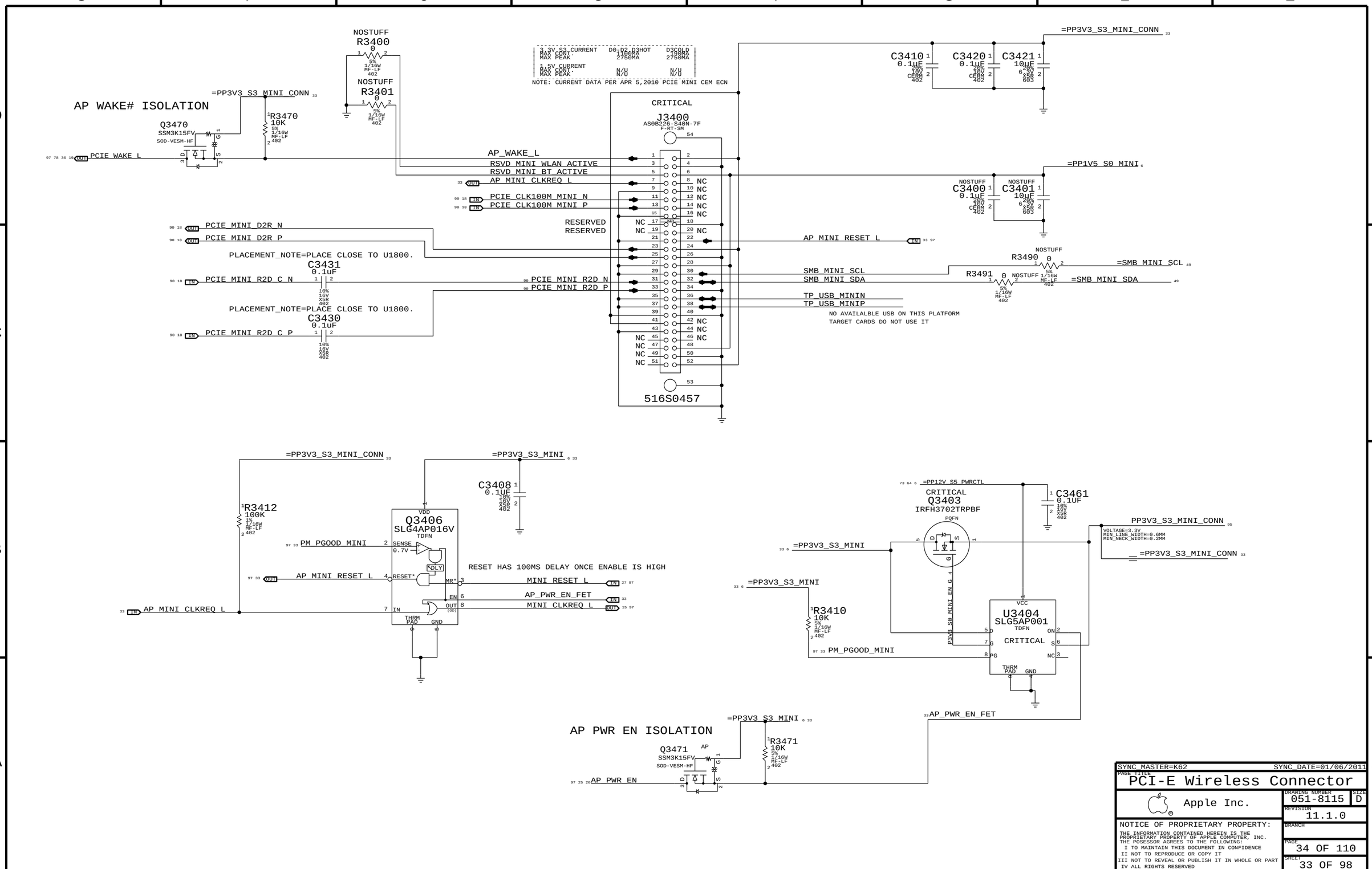


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PAGE TITLE
# PCI-E Wireless Connector

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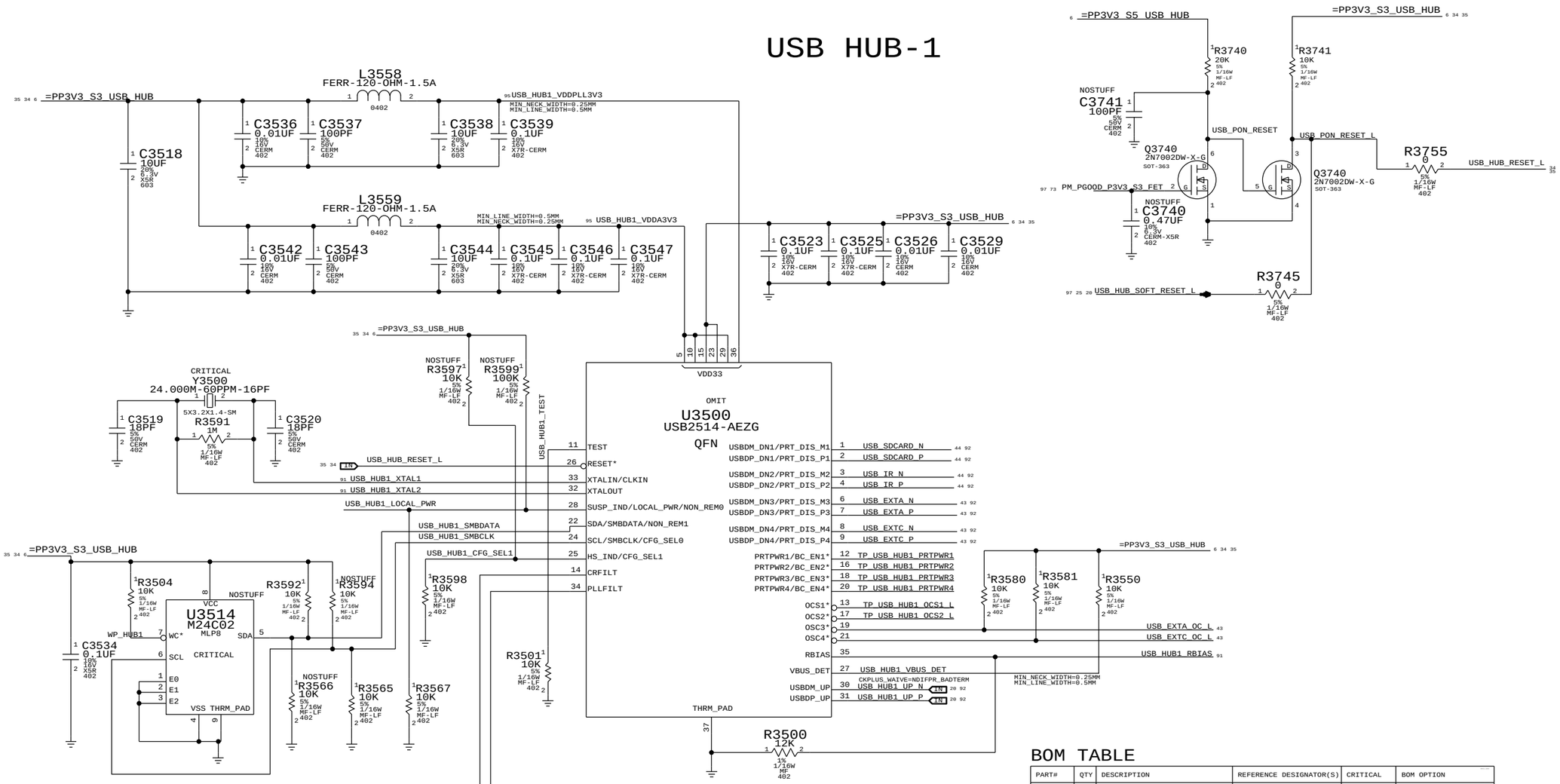
# USB HUB-1




| | SEL1 | SEL0 | DESCRIPTION |
|---|---|---|---|
| DEFAULT K23F ==> | 0 | 0 | Internal Default with Self powered Operation |
| | 0 | 1 | SMBUS Slave Config |
| | 1 | 0 | Internal Default with Bus powered Operation |
| | 1 | 1 | EEPROM Supported |

| | NON_REM1 | NON_REM0 | DESCRIPTION |
|---|---|---|---|
| | 0 | 0 | All ports are Non removable |
| | 0 | 1 | Port1 is non removable |
| DEFAULT K23F ==> | 1 | 0 | Port 1 and 2 are non removable |
| | 1 | 1 | Port1,2 and 3 are non Removable |

## BOM TABLE

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 338S0721 | 2 | SMSC USX2061-AEZG | U3500,U3600 | CRITICAL | HUB_USX2061 |
| 338S0824 | 2 | SMSC USB2514B | U3500,U3600 | CRITICAL | HUB_USB2514B |

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USB HUB 1

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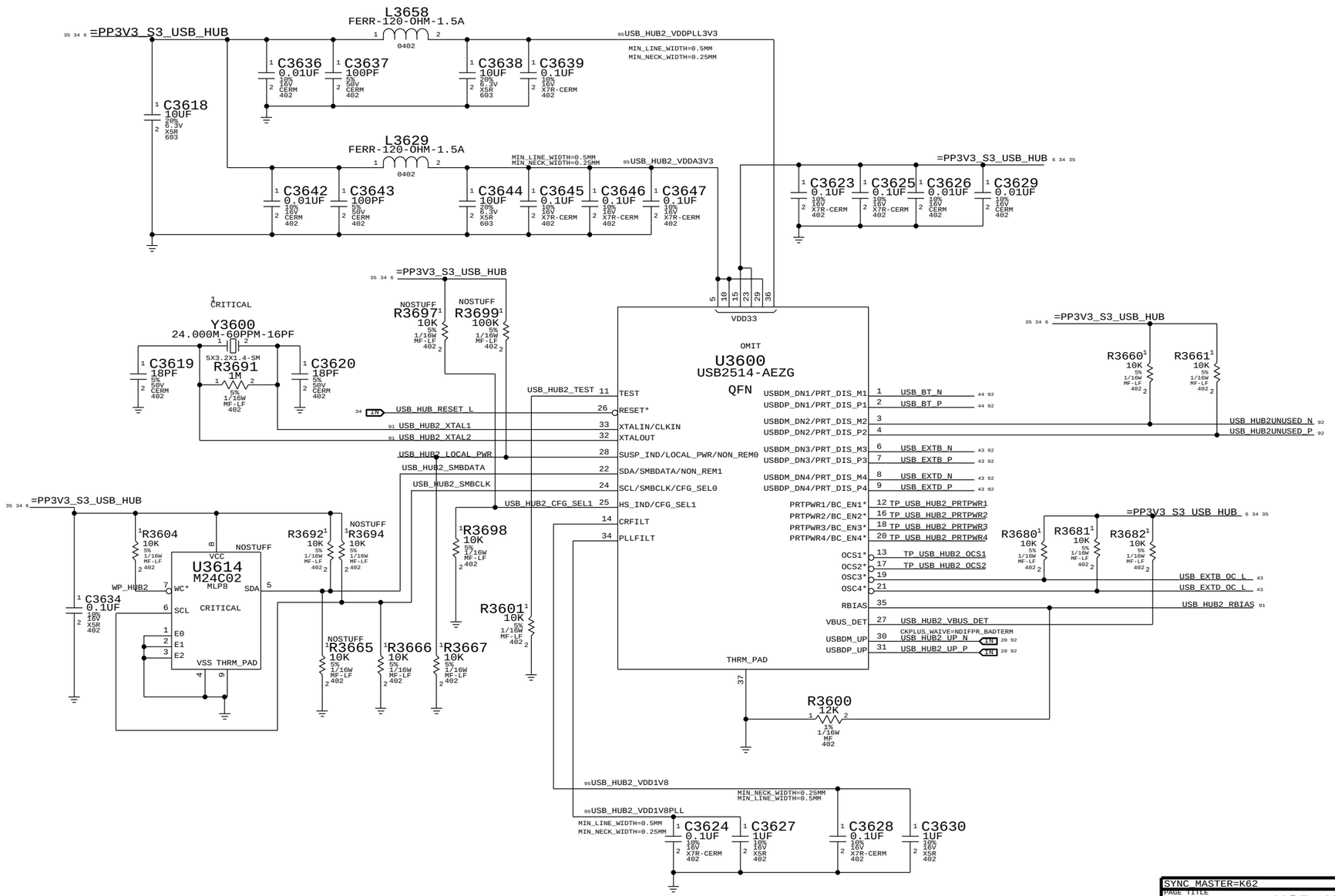
# USB HUB-2

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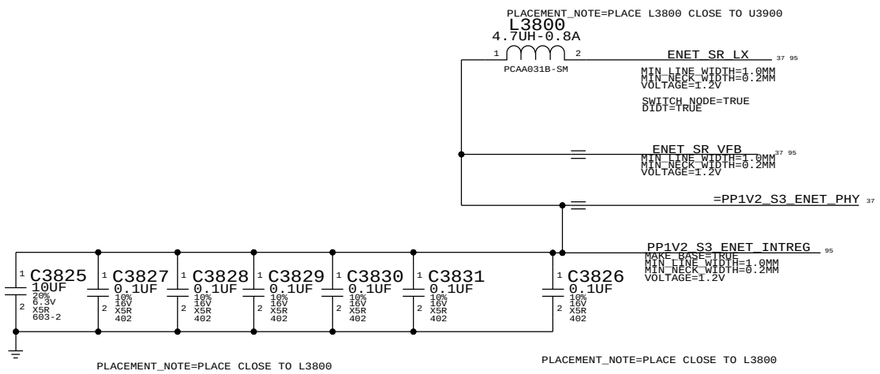
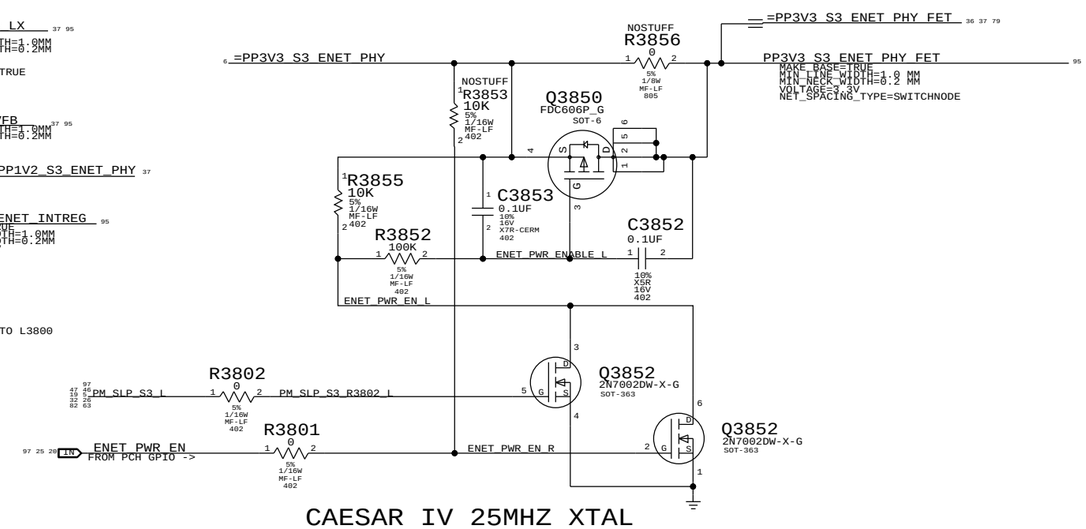
## CAESAR IV 1.2V INT.VR CMPTS

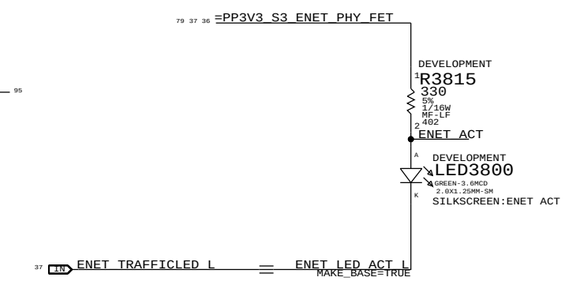



## CAESAR IV POWER ENABLE CIRCUIT

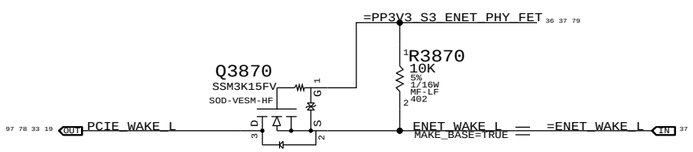
3V3_ENET_PHY_FET = S0 || (S3 POWER && ENET_PWR_EN)



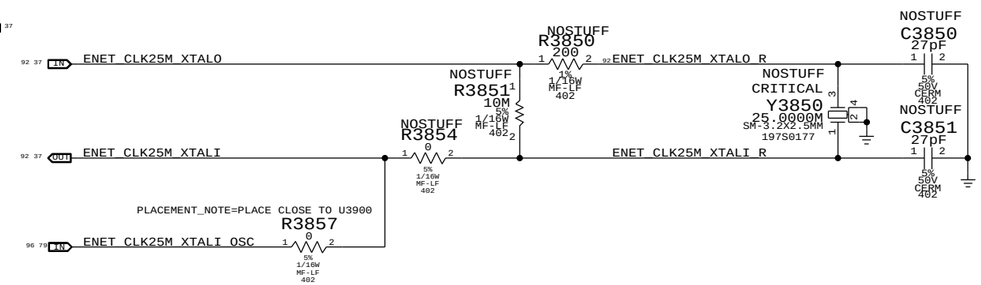

## CAESAR IV ACTIVITY LED



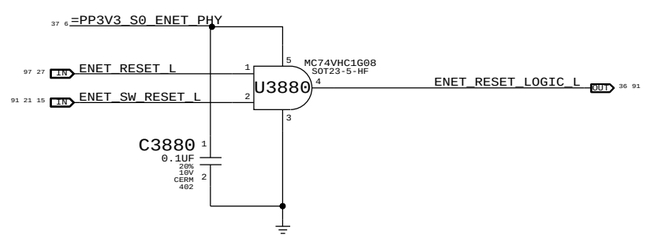

## CAESAR IV WAKE# ISOLATION



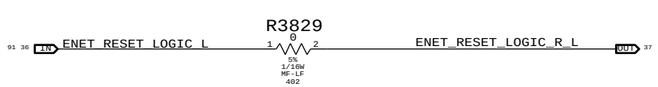

## CAESAR IV 25MHZ XTAL




## CAESAR IV SW RESET GATING

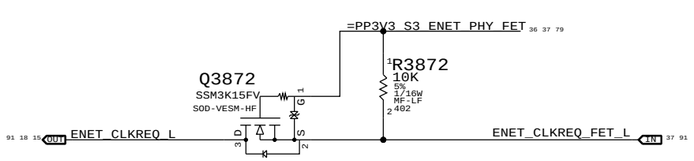



## CAESAR IV RESET CONNECTION




## CAESAR IV STRAPS (NONE)

## CAESAR IV CLKREQ ISOLATION

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PAGE TITLE
# CAESAR IV SUPPORT

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

281mA (1000base-T max power, Caesar IV)

=PP3V3_S3_ENET_PHY_FET

R3901 0 5% 1/16W MF-LF 402 — ENET_3V3_S3_SR_IN (SWITCH_NODE=TRUE, DIDT=TRUE, NET_SPACING_TYPE=SWITCHNODE, MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V)

C3979 4.7UF 20% 6.3V CERM 603

C3980 0.1UF 10% 16V X5R 402

C3981 0.1UF 10% 16V X5R 402

CRITICAL L3900 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_XTALVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

R3900 0 5% 1/16W MF-LF 402 — ENET_XTALVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C3900 0.1UF 10% 16V X7R-CERM 402

VDD for Card Reader I/O — =PP3V3R1V8_ENET_LR_OUT

CRITICAL L3905 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_BIASVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3910 FERR-600-OHM-0.5A SM — PP3V3_S3_ENET_PHY_AVDDH (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

R3910 4.7K 5% 1/16W MF-LF 402

C3910 0.1UF 10% 16V X7R-CERM 402

C3911 0.1UF 10% 16V X7R-CERM 402

R3940 4.7K 5% 1/16W MF-LF 402

R3941 4.7K 5% 1/16W MF-LF 402

C3917 0.1UF 10% 16V X7R-CERM 402

C3918 0.1UF 10% 16V X7R-CERM 402

C3915 4.7UF 10% 6.3V X5R-CERM 603

C3916 0.1UF 10% 16V X7R-CERM 402

=PP3V3_S0_ENET_PHY

R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

C3950 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_N

C3951 0.1uF 10% 16V X5R 402 — PCIE_ENET_D2R_P

C3955 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_C_P

C3956 0.1uF 10% 16V X5R 402 — PCIE_ENET_R2D_C_N

R3943 0 5% 1/16W MF-LF 402 — =ENET_WAKE_L (See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_SR_LX — ENET_SR_VFB

Internal 1.2V Switching Regulator pins.

=PP1V2_S3_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_AVDDL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V)

C3921 0.1UF 10% 16V X7R-CERM 402

C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_PCIEPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V)

C3926 0.1UF 10% 16V X7R-CERM 402

C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A SM — PP1V2_S3_ENET_PHY_GPHYPLL (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V)

C3931 0.1UF 10% 16V X7R-CERM 402

C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402

C3935 10UF 10% 6.3V X5R 805

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O. Connect only to U3900 pin 20.

=PP3V3R1V8_ENET_LR_OUT

PP3V3R1V8_ENET_LR_OUT_REG (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V)

DEVELOPMENT C3970 4.7UF 10% 6.3V X5R-CERM 603 — DEVELOPMENT C3971 0.1UF 10% 16V X7R-CERM 402 — C3972 0.1UF 10% 16V X7R-CERM 402 — DEVELOPMENT

NOSTUFF R3959 150 5% 1/16W MF-LF 402 — NOSTUFF C3959 10PF 5% 50V CERM 402

MUST DO: REMOVE C/R3959 AFTER PROTO 2

OMIT
U3900
BCM57765
QFN-8X8

| Pin | Signal | Net |
|---|---|---|
| 42, 48 | AVDDH | |
| 37 | BIASVDDH | |
| 17 | XTALVDDH | |
| 7 | VDDO | |
| 20, 56, 62 | | |
| 14 | SR_VDD | |
| 15 | SR_VDDP | |
| 16 | SR_LX | |
| 13 | SR_VFB | |
| 39, 45, 51 | AVDDL | |
| 29 | PCIE_PLLVDDL | |
| 32 | GPHY_PLLVDDL | |
| 36 | | |
| 35, 61 | VDDC | |
| 58 | VMAIN_PRSNT (IPD-ENET) | ENET_VMAIN_PRSNT |
| 27 | PCIE_TXD_N | PCIE_ENET_D2R_C_N |
| 28 | PCIE_TXD_P | PCIE_ENET_D2R_C_P |
| 33 | PCIE_RXD_P | PCIE_ENET_R2D_P |
| 34 | PCIE_RXD_N | PCIE_ENET_R2D_N |
| 31 | PCIE_REFCLK_P | PCIE_CLK100M_ENET_P |
| 30 | PCIE_REFCLK_N | PCIE_CLK100M_ENET_N |
| 11 | PERST* (IPD) | ENET_RESET_LOGIC_R_L |
| 12 | CLKREQ* (OD) | ENET_CLKREQ_FET_L |
| 3 | WAKE* (OD) | ENET_WAKE_R_L |
| 4 | LOW_PWR (IPD) | ENET_LOW_PWR |
| 6 | SMB_CLK | ENET_SMB_CLK |
| 10 | SMD_DATA (IPD-ENETM) | ENET_SMB_DATA |
| 66 | SCLK | ENET_SCLK |
| 64 | SI/LINKLED* | ENET_MISO |
| 65 | SO | ENET_MOSI |
| 63 | CS* | ENET_CS_L |
| 2 | SPD100LED*/SERIAL_DO (OD) | TP_ENET_SPD100LED_L |
| 67 | TRAFFICLED*/SERIAL_DI (OD) | ENET_TRAFFICLED_L |
| 18 | XTALI | ENET_CLK25M_XTALI |
| 19 | XTALO | ENET_CLK25M_XTALO |
| 38 | RDAC | ENET_RDAC |
| 69 | THRM_PAD (NO IPU OR IPD-ENET) | |
| 40 | TRD0_P | ENETCONN_MDI_P<0> |
| 41 | TRD0_N | ENETCONN_MDI_N<0> |
| 44 | TRD1_P | ENETCONN_MDI_P<1> |
| 43 | TRD1_N | ENETCONN_MDI_N<1> |
| 46 | TRD2_P | ENETCONN_MDI_P<2> |
| 47 | TRD2_N | ENETCONN_MDI_N<2> |
| 50 | TRD3_P | ENETCONN_MDI_P<3> |
| 49 | TRD3_N | ENETCONN_MDI_N<3> |
| 5 | GPIO_0 (IPD) | NC |
| 8 | GPIO_1/CR_BUS_PWR (IPD) | |
| 9 | RE*/GPIO_2 | ENET_MEDIA_SENSE |
| 1 | SD_DETECT/WE* (IPx-ENET) | ENET_SD_DETECT_L |
| 26 | CR_CMD/CLE (IPU-ENET) | ENET_SD_CMD |
| 21 | CR_CLK/RY_BY* | ENET_SD_CLK |
| 25 | CR_DATA0 (IPU-ENET) | ENET_CR_DATA<0> |
| 24 | CR_DATA1 | ENET_CR_DATA<1> |
| 23 | CR_DATA2 | ENET_CR_DATA<2> |
| 22 | CR_DATA3 | ENET_CR_DATA<3> |
| 52 | CR_DATA4 | ENET_CR_DATA<4> |
| 53 | CR_DATA5 | ENET_CR_DATA<5> |
| 54 | CR_DATA6 | ENET_CR_DATA<6> |
| 55 | CR_DATA7 | ENET_CR_DATA<7> |
| 59 | CE*/MS_INS* (IPU-ENET) | NC_ENET_CE_L_MS_INS_L |
| 60 | CR_LED/ALE (IPU-ENET) | ENET_CR_PWREN |
| 57 | CR_WP*/XD_WP* (IPU-ENET) | |
| 68 | XD_DETECT (IPU-ENET) | ENET_SR_DISABLE |

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

| Net | Resistor | Value | Placement |
|---|---|---|---|
| ENET_SD_DETECT_L | R3960 | 0 | DEVELOPMENT |
| ENET_SD_CMD | R3961 | 33 | DEVELOPMENT, PLACEMENT_NOTE=PLACE NEAR U3900 |
| ENET_SD_CLK | R3979 | 33 | DEVELOPMENT, PLACEMENT_NOTE=PLACE NEAR U3900 |
| ENET_CR_DATA<0> | R3971 | 33 | DEVELOPMENT |
| ENET_CR_DATA<1> | R3972 | 33 | DEVELOPMENT |
| ENET_CR_DATA<2> | R3973 | 33 | DEVELOPMENT |
| ENET_CR_DATA<3> | R3974 | 33 | DEVELOPMENT |
| ENET_CR_DATA<4> | R3975 | 33 | DEVELOPMENT |
| ENET_CR_DATA<5> | R3976 | 33 | DEVELOPMENT |
| ENET_CR_DATA<6> | R3977 | 33 | DEVELOPMENT |
| ENET_CR_DATA<7> | R3978 | 33 | DEVELOPMENT |

5% 1/16W MF-LF 402

SDCONN_DETECT_L — SDCONN_CMD — SDCONN_CLK — SDCONN_DATA<0> — SDCONN_DATA<1> — SDCONN_DATA<2> — SDCONN_DATA<3> — SDCONN_DATA<4> — SDCONN_DATA<5> — SDCONN_DATA<6> — SDCONN_DATA<7>

NO_TEST=TRUE

No MS (Memory Stick) Insert feature needed. Control signal to light LED or control SD bus power.

SDCONN_WP

R3980 1K 5% 1/16W MF-LF 402 NOSTUFF — =PP3V3_S3_ENET_PHY_FET

R3981 1K 5% 1/16W MF-LF 402

(See note)

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET supports both active-levels for WP.

PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900
PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

R3965 1.24K 1% 1/16W MF-LF 402

## PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup. (Required ROM size 1 Mbit)

=PP3V3_S3_ENET_PHY_FET

R3993 4.7K 5% 1/16W MF-LF 402 — R3992 4.7K 5% 1/16W MF-LF 402

R3904 0 5% 402 1/16W MF-LF

U3990
AT45DB021D
SOIC-8S1
OMIT_TABLE

| Pin | Signal | Net |
|---|---|---|
| 8 | VCC | |
| 2 | SCK | ENET_SCLK_R |
| 4 | CS* | ENET_CS_L |
| 5 | WP* | ENET_SWP_L |
| 3 | RESET* | ENET_SRESET_L |
| 1 | SI | ENET_MOSI |
| 8 | SO | ENET_MISO |
| | GND | |

C3990 0.1UF 10% 16V X7R-CERM 402

NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402 — R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K62 SYNC_DATE=01/06/2013

PAGE TITLE
# ETHERNET PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
REVISION 11.1.0
BRANCH
PAGE 39 OF 110
SHEET 37 OF 98

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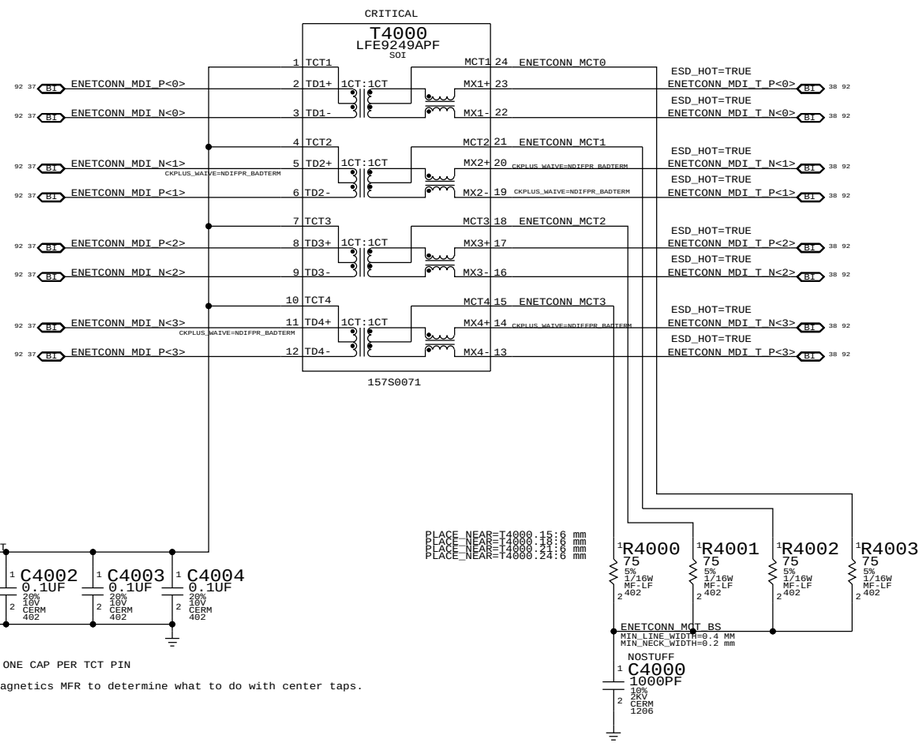
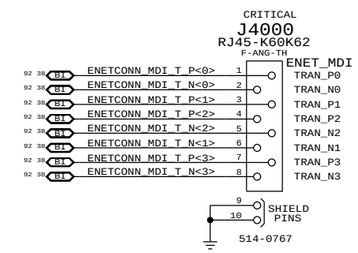
# THIS PAGE DIFFERENT BETWEEN K60 and K62.




NOTE: Check with PHY and Magnetics MFR to determine what to do with center taps.

NOTE: BOB SMITH TERMINATION FOR EMC.

NO PAIR AND PIN POLARITY SWAPS




SYNC_MASTER=K60_MARK SYNC_DATE=01/06/2011

PAGE TITLE
Ethernet Connector

Apple Inc.

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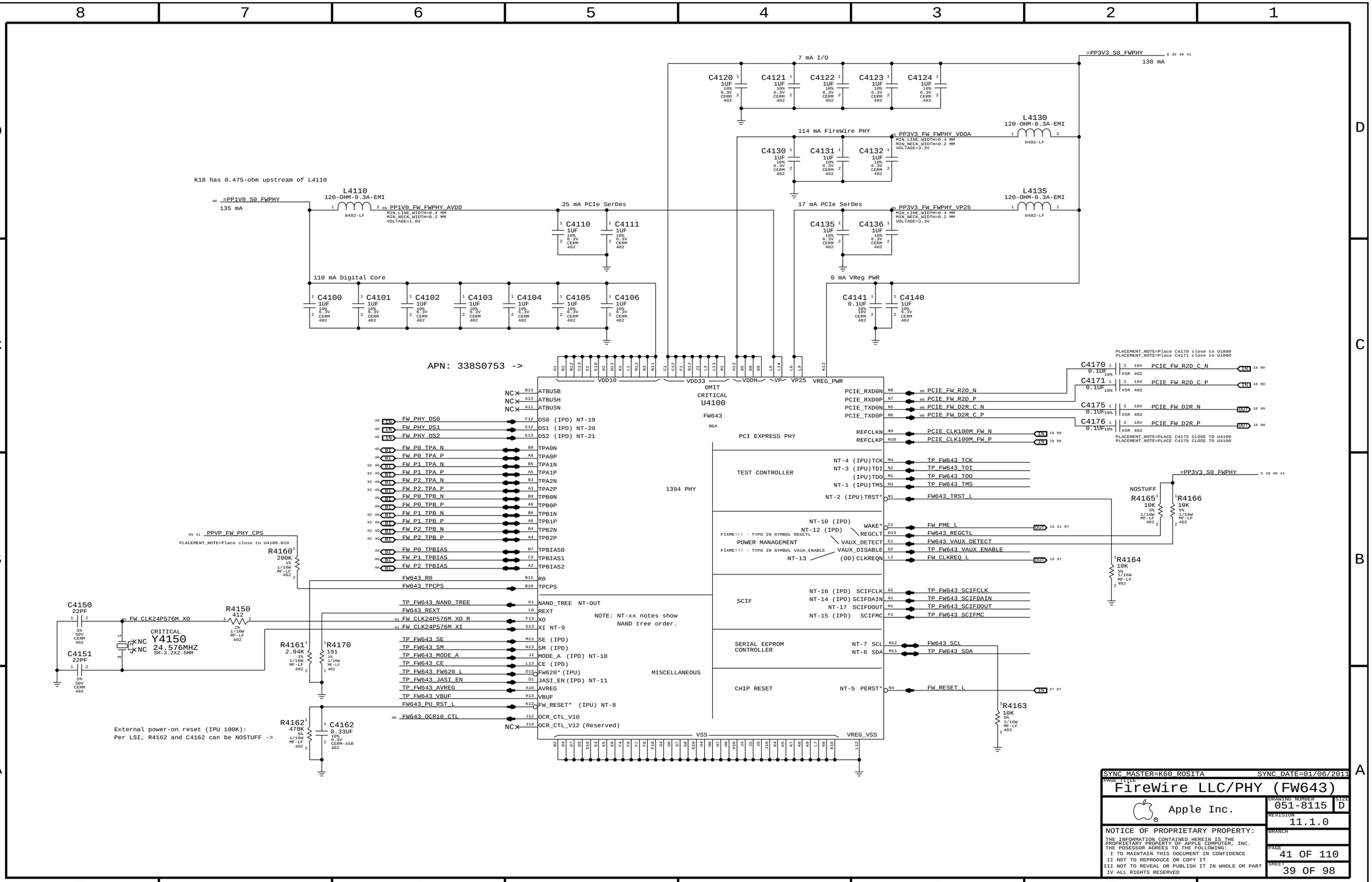


SYNC_MASTER=K60_ROSITA SYNC_DATE=01/06/2011

PAGE TITLE
# FireWire LLC/PHY (FW643)

Apple Inc.

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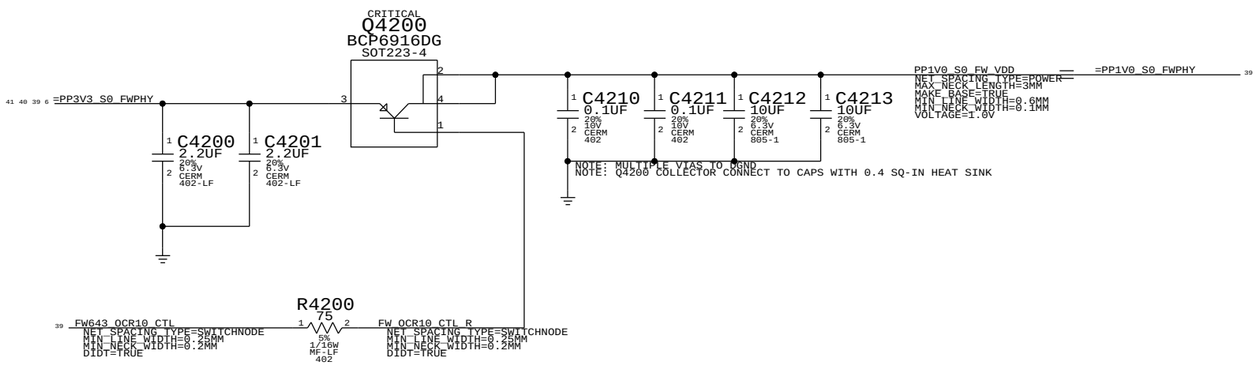
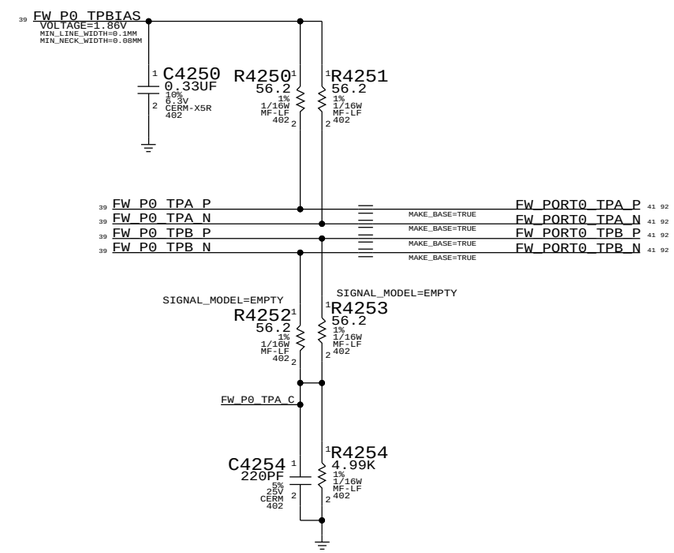
## FW643 1.0V GENERATION

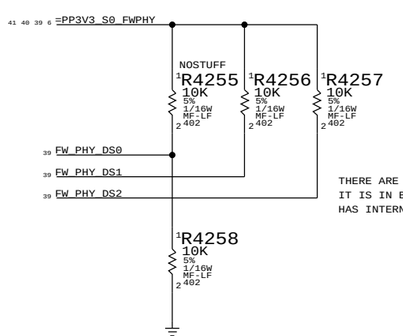



## Termination

Place close to FireWire PHY




## 1394 PHY DATA/STROBE OPTIONS




THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

## 2ND & 3RD TPA/TPB PAIR UNUSED

| | | | |
|---|---|---|---|
| 39 | FW_P1_TPBIAS | NC_FW_PORT1_TPBIAS | MAKE_BASE=TRUE NO_TEST=TRUE |
| 92 39 | FW_P1_TPA_P | NC_FW_PORT1_TPA_P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 92 39 | FW_P1_TPA_N | NC_FW_PORT1_TPA_N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 92 39 | FW_P1_TPB_P | NC_FW_PORT1_TPB_P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 92 39 | FW_P1_TPB_N | NC_FW_PORT1_TPB_N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 39 | FW_P2_TPBIAS | NC_FW_PORT2_TPBIAS | MAKE_BASE=TRUE NO_TEST=TRUE |
| 92 39 | FW_P2_TPA_P | NC_FW_PORT2_TPA_P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 92 39 | FW_P2_TPA_N | NC_FW_PORT2_TPA_N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 92 39 | FW_P2_TPB_P | NC_FW_PORT2_TPB_P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 92 39 | FW_P2_TPB_N | NC_FW_PORT2_TPB_N | MAKE_BASE=TRUE NO_TEST=TRUE |

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
FireWire: 1394B MISC

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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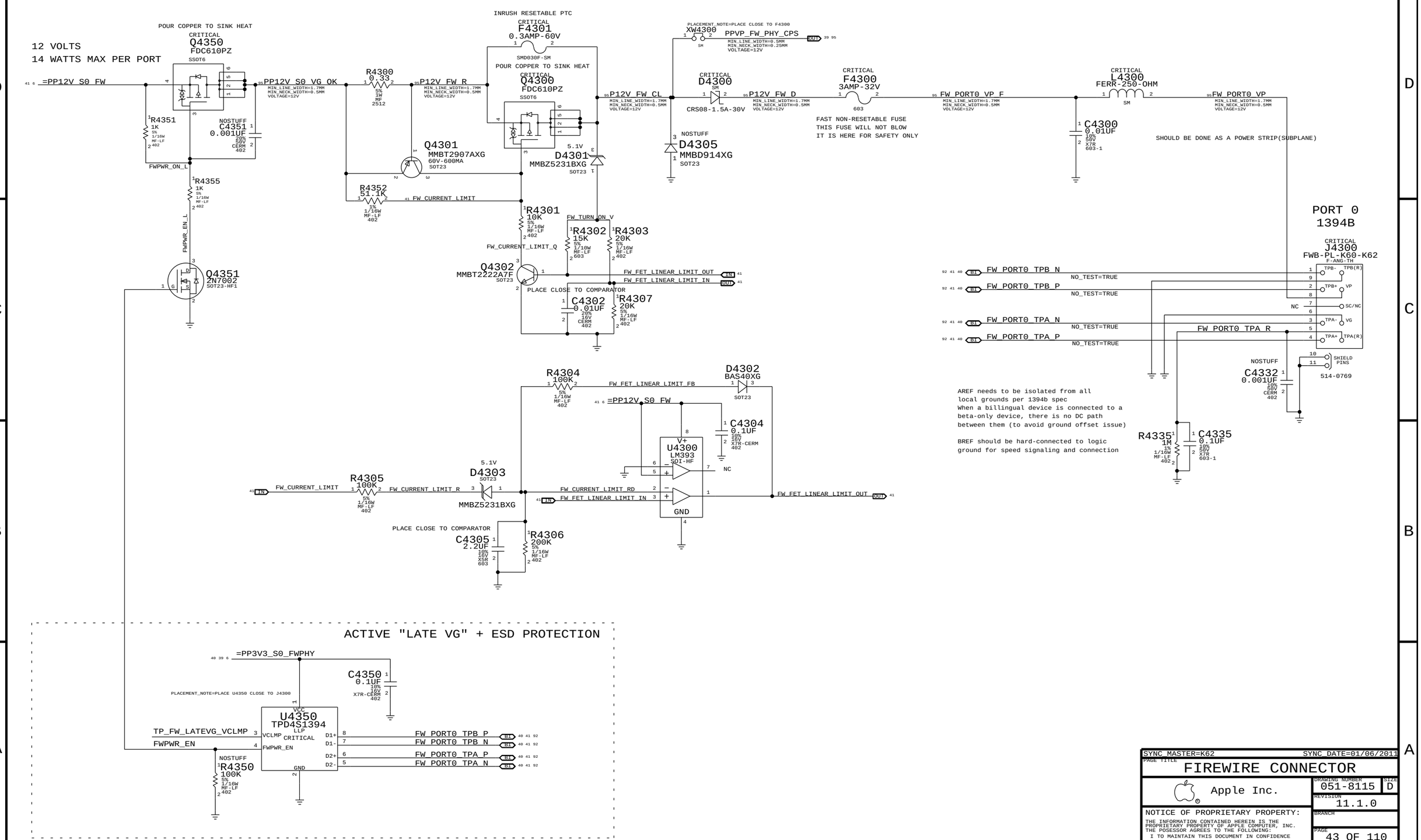


SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

# FIREWIRE CONNECTOR

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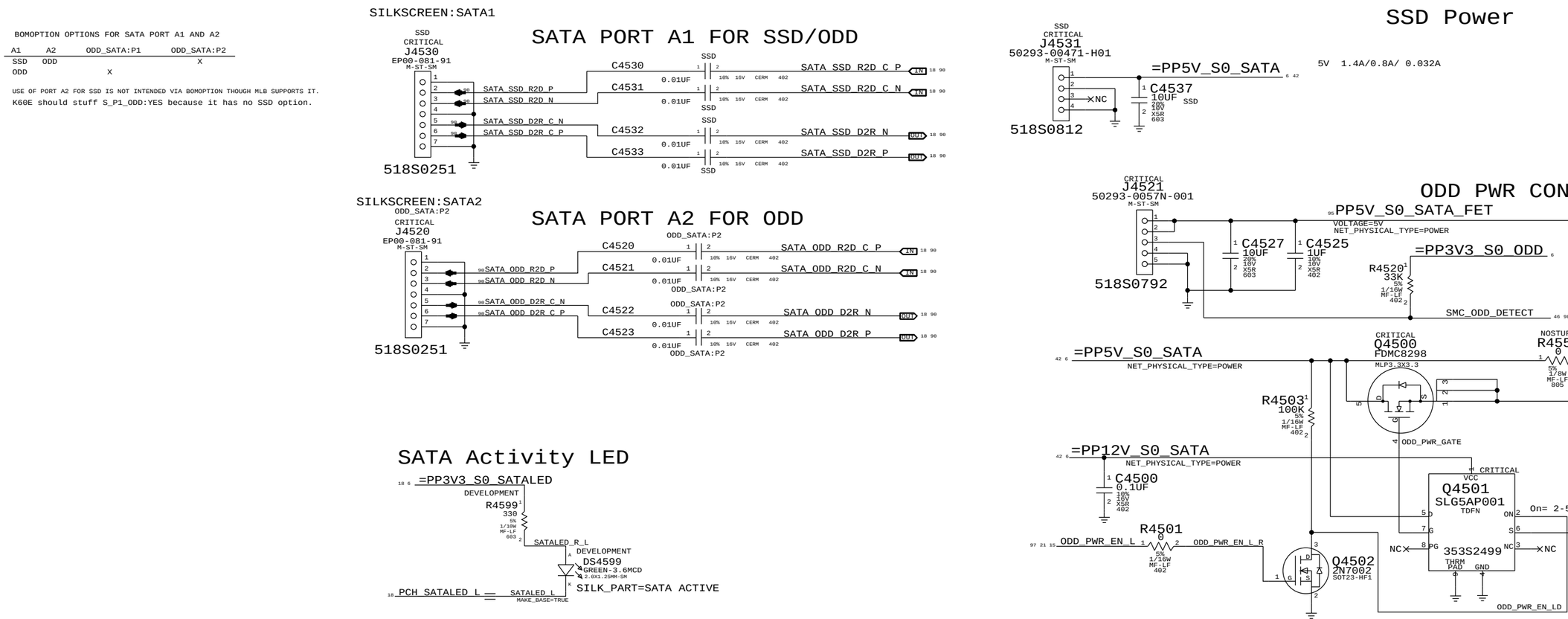
BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

| A1 | A2 | ODD_SATA:P1 | ODD_SATA:P2 |
|---|---|---|---|
| SSD | ODD | | X |
| ODD | | X | |

USE OF PORT A2 FOR SSD IS NOT INTENDED VIA BOMOPTION THOUGH MLB SUPPORTS IT.
K60E should stuff S_P1_ODD:YES because it has no SSD option.




| | |
|---|---|
| SYNC_MASTER=K60_JERRY | SYNC_DATE=01/06/2011 |
| PAGE TITLE: SATA Connectors | |
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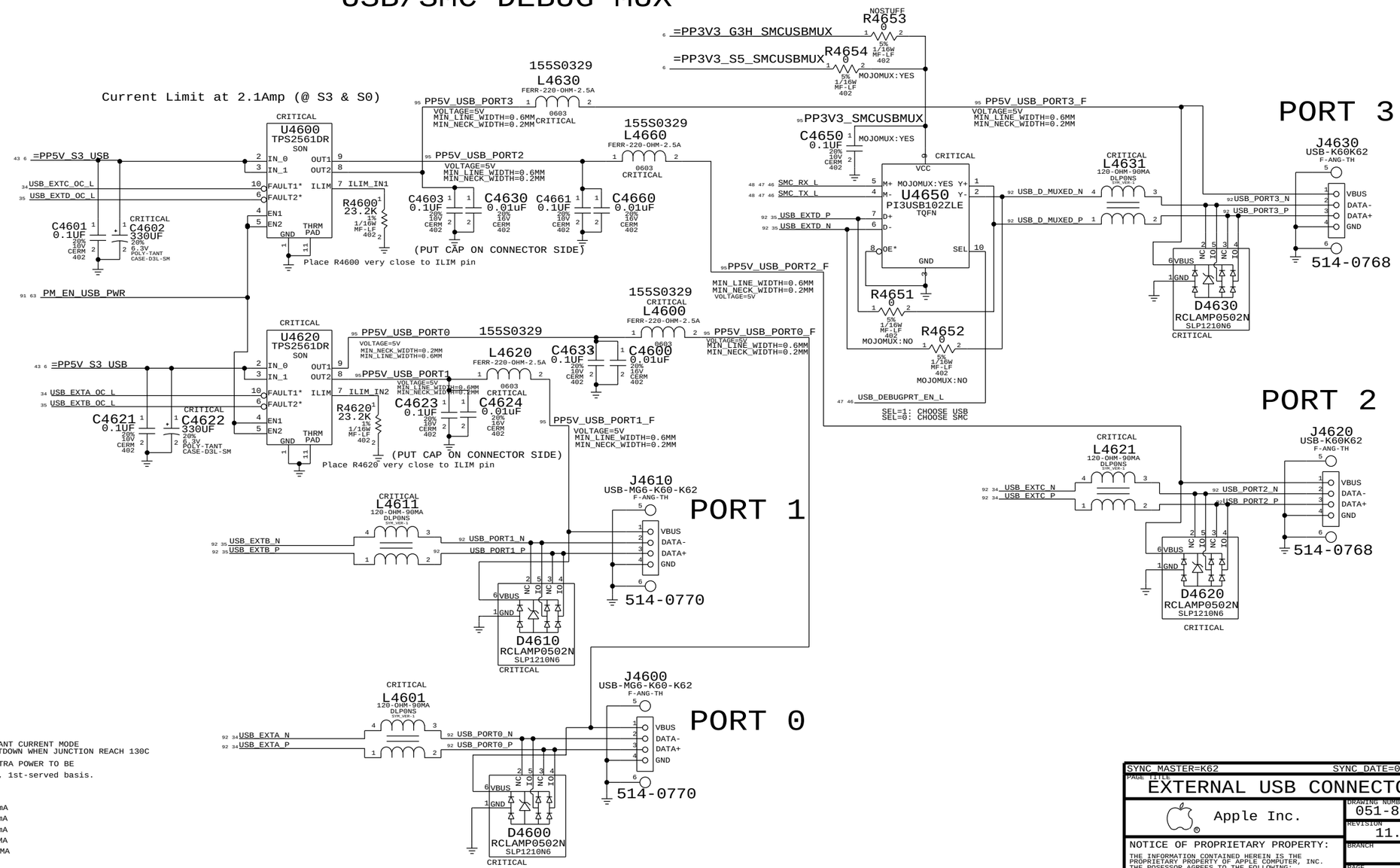
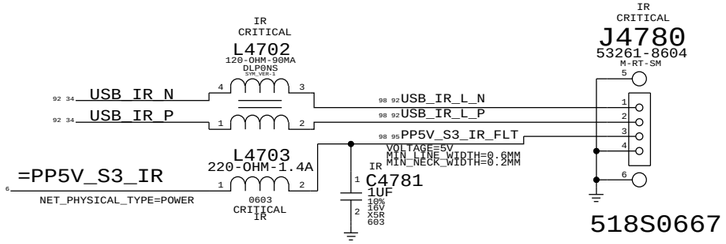
# USB/SMC DEBUG MUX

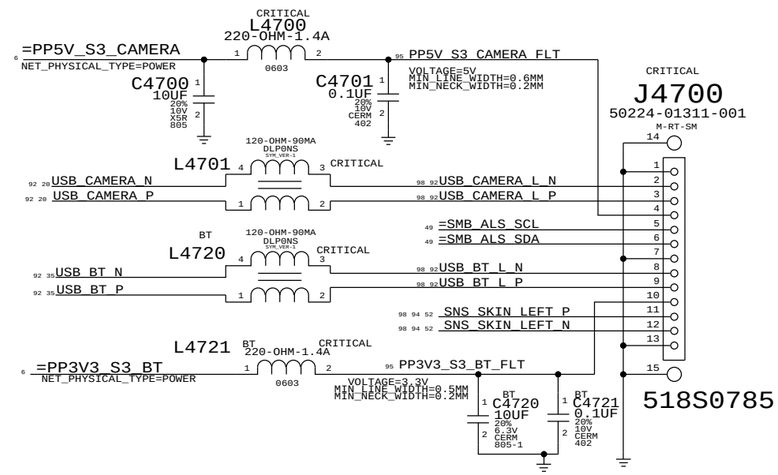
ADDED AT EVT & SWITCH TO S5 RAIL



## IR RECEIVER CONNECTOR

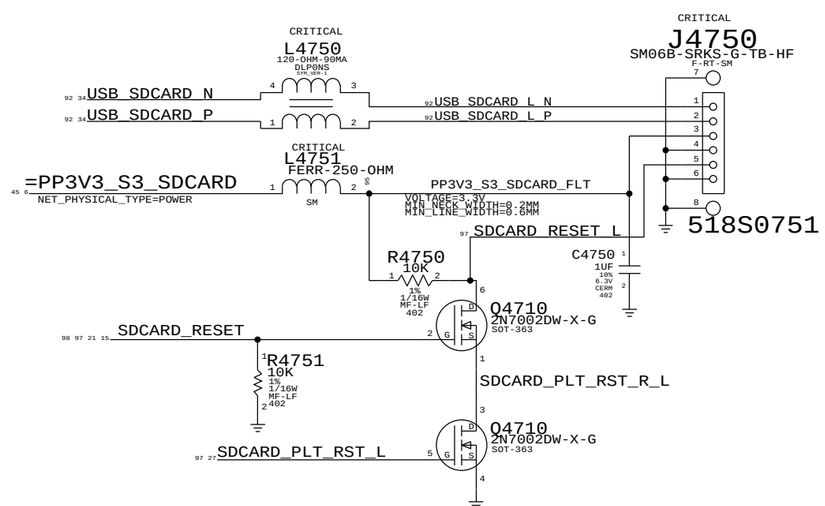



## CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR




Skin Temp sense at upper Left Screen corner

## SD Card Reader Board ( Lazarus )




SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

# Internal USB Connections

Apple Inc.

| | |
|---|---|
| DRAWING NUMBER | 051-8115 |
| SIZE | D |
| REVISION | 11.1.0 |
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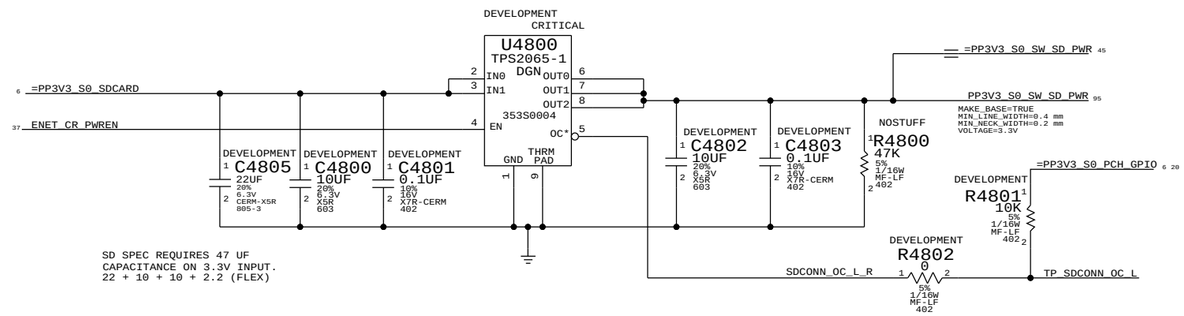
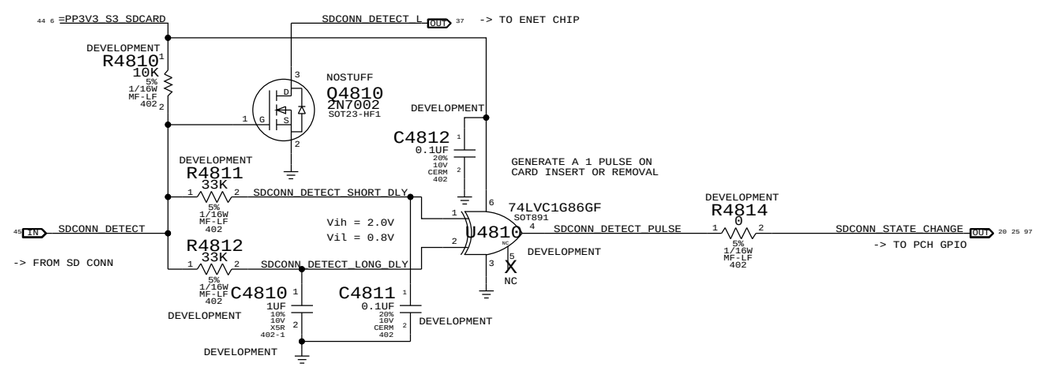
## SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

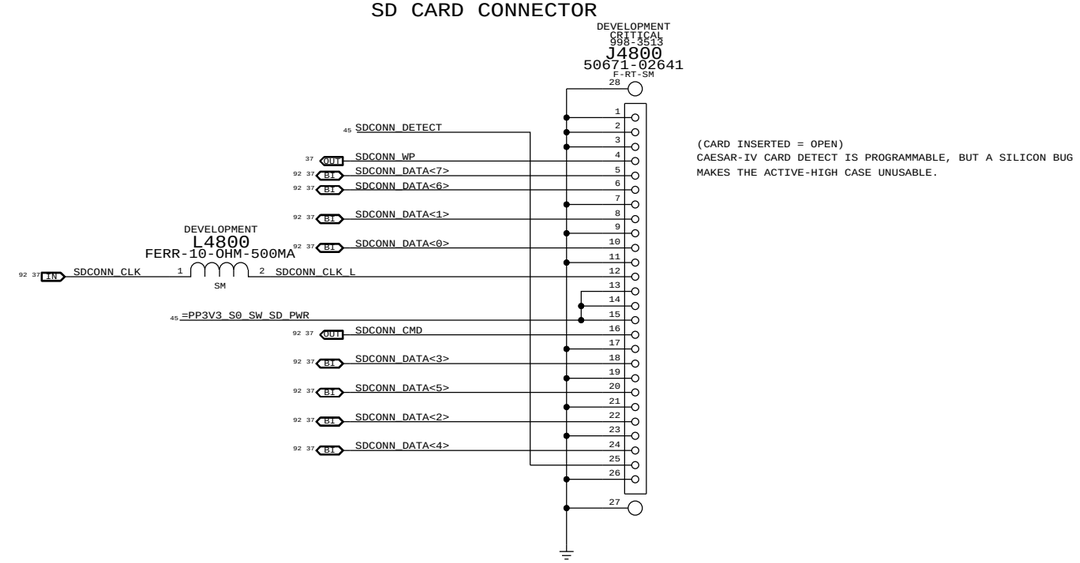
TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R4800 IS NOSTUFF.




## SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT




## SD CARD CONNECTOR




SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
# SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

338S0878

U4900
H8S2117
LFBGA
(1 OF 4)
OMIT

| Pin | Net | Dir | Note |
|---|---|---|---|
| B12 P10 | SMC_EXCARD_PWR_EN | OUT | 47 |
| C13 P11 | SMC_RSTGATE_L | OUT | 47 |
| A15 P12 | ALL_SYS_PWRGD_SMC | IN | 97 64 |
| B14 P13 | RSMRST_PWRGD | IN | 97 64 |
| B15 P14 | NC | | |
| C14 P15 | PM_RSMRST_L | OUT | 97 27 |
| D12 P16 | CPUIMVP_VR_ON | OUT | 47 |
| C15 P17 | PM_PWRBTN_L | OUT | 97 25 19 |
| D13 P20 | NC | | K62 NEW:NOT USE |
| D14 P21 | NC | | |
| D15 P22 | NC | | |
| F12 P23 | NC | | |
| E14 P24 | NC | | K62 NEW:NOT USE |
| E15 P25 | NC | | |
| E13 P26 | NC | | K62 NEW:NOT USE |
| F14 P27 | NC | | |
| D9 P30 | LPC_AD<0> | BI | 91 48 18 |
| C9 P31 | LPC_AD<1> | BI | 91 48 18 |
| A9 P32 | LPC_AD<2> | BI | 91 48 18 |
| B9 P33 | LPC_AD<3> | BI | 91 48 18 |
| D8 P34 | LPC_FRAME_L | IN | 91 48 18 |
| C8 P35 | SMC_LRESET_L | IN | 97 27 |
| A8 P36 | LPC_CLK33M_SMC | IN | 91 27 |
| D7 P37 | LPC_SERIRQ | BI | 48 18 |
| A5 P40 | NC | | |
| B5 P41 | NC | | K62 P1 NOT USED, WAS OOB_TEMP |
| D5 P42 (OC) | SMB_MGMT_DATA | BI | 49 |
| C3 P43 | SMS_ONOFF_L | OUT | 47 |
| B1 P44 | NC | | |
| C2 P45 | NC | | |
| D3 P46 | SMC_GFX_THROTTLE_L | OUT | 47 |
| C1 P47 | NC | | |
| G1 P50 | SMC_TX_L | OUT | 48 47 46 43 |
| G4 P51 | SMC_RX_L | IN | 48 47 46 43 |
| F2 P52 (OC) | SMB_0_S0_CLK | BI | 49 |
| P60 L13 | SMC_PM_G2_EN | OUT | 74 97 |
| P61 L14 | NC | | |
| P62 L15 | NC | | |
| P63 K12 | NC | | |
| P64 K13 | SMC_ADAPTER_EN | OUT | 19 47 97 |
| P65 K14 | NC | | |
| P66 J12 | SMC_PROCHOT_3_3_L | IN | 47 97 |
| P67 J13 | SMC_BIL_BUTTON_L | IN | 47 |
| P70 N12 | SMC_VCORE_ISENSE | IN | 50 94 (IMON) |
| P71 R13 | SMC_VCORE_VSENSE | IN | 50 94 (IMON) |
| P72 P13 | SMC_CPU_1V5_ISENSE | IN | 50 94 |
| P73 R14 | SMC_CPU_1V5_VSENSE | IN | 50 94 |
| P74 P14 | SMC_VCCSA_ISENSE | IN | 50 94 |
| P75 R15 | SMC_VCCSA_VSENSE | IN | 50 94 |
| P76 N13 | SMC_VAXG_ISENSE | IN | 50 94 (IMON) |
| P77 P15 | SMC_VAXG_VSENSE | IN | 50 94 (IMON) |
| P80 C7 | SMC_WAKE_SCI_L | OUT | 15 18 21 97 PROTO-3, Change back to WAKE_SCI_L |
| P81 A7 | NC | | |
| P82 B7 | PM_CLKRUN_L | OUT | 15 19 48 97 |
| P83 D6 | LPC_PWRDWN_L | IN | 19 48 97 |
| P84 C6 | SMC_TX_L | OUT | 43 46 47 48 |
| P85 A6 | SMC_RX_L | IN | 43 46 47 48 |
| P86 B6 | SMB_MGMT_CLK (OC) | BI | 49 |
| P90 K4 | SMC_ONOFF_L | IN | 47 97 |
| P91 J2 | SMC_BC_ACOK | IN | 47 |
| P92 J1 | NC | | |
| P93 J3 | PM_SLP_S3_L | IN | 5 19 26 32 36 47 63 82 97 |
| P94 J4 | PM_SLP_S4_L | IN | 5 19 32 47 63 97 K60 New Change |
| P95 H2 | PM_SLP_S5_L | IN | 5 19 47 63 97 K60 New Change |
| P96 H1 | PM_CLK32K_SUSCLK | IN | 9 91 97 |
| P97 G2 | SMB_0_S0_DATA (OC) | BI | 49 |

U4900
H8S2117
LFBGA
(2 OF 4)
OMIT

| Pin | Net | Dir | Note |
|---|---|---|---|
| R3 PA0 | SMC_PA0 | IN | 47 K62 NEW:NOT USE,PULLED UP |
| P3 PA1 | SPI_DESCRIPTOR_OVERRIDE_L (OC) | OUT | 97 18 |
| R2 PA2 | PM_SYSRST_L (OC) | OUT | 97 27 25 19 |
| N3 PA3 | USB_DEBUGPRT_EN_L (OC) | OUT | 47 43 |
| R1 PA4 | MEM_EVENT_A_L (OC) | IN | 47 |
| N2 PA5 | MEM_EVENT_B_L (OC) | IN | 47 |
| M4 PA6 | SYS_ONEWIRE (OC) | BI | 47 |
| N1 PA7 | PM_BATLOW_L (OC) | OUT | 97 19 15 |
| B10 PB0 | NC | | |
| A10 PB1 | SMC_RUNTIME_SCI_L | OUT | 97 47 23 PROTO-3:back to K75F |
| D10 PB2 | SMC_ODD_DETECT | IN | 98 42 |
| A11 PB3 | SMC_PB3 (See below) | IN | 47 K62 NEW:NOT USE,PULLED UP |
| B11 PB4 | SMC_HDD_OOB_TEMP | IN | 94 51 |
| C11 PB5 | NC | | |
| A12 PB6 | SMC_PB6 | IN | K62 NEW:NOT USE,PULLED UP |
| D11 PB7 | SMC_GFX_OVERTEMP_L | IN | 47 |
| G14 PC0 | SMC_FAN_0_CTL | OUT | 53 |
| G15 PC1 | SMC_FAN_1_CTL | OUT | 53 |
| G13 PC2 | NC | | |
| G12 PC3 | SMC_FAN_3_CTL | OUT | 54 |
| H14 PC4 | SMC_FAN_0_TACH | IN | 53 |
| H15 PC5 | SMC_FAN_1_TACH | IN | 53 |
| H13 PC6 | NC | | |
| H12 PC7 | SMC_FAN_3_TACH | IN | 54 |
| M11 PD0 | SMC_1V05_ISENSE | IN | (IMON) 94 50 |
| P11 PD1 | SMC_1V05_VSENSE | IN | (IMON) 94 50 |
| R11 PD2 | SMC_PCH_1V05_ISENSE | IN | 94 50 |
| N11 PD3 | SMC_PCH_1V05_VSENSE | IN | 94 50 |
| P10 PD4 | SMC_GPU_ISENSE | IN | 94 50 |
| R10 PD5 | SMC_GPU_VSENSE | IN | 94 50 |
| N10 PD6 | SMC_DIMM_ISENSE | IN | 94 50 |
| M10 PD7 | SMC_DIMM_VSENSE | IN | 94 50 |
| M3 PE0 | SMC_PE0 | IN | 47 K62 NEW:NOT USE,PULLED UP |
| M2 PE1* | SMC_TCK | IN | 47 48 |
| M1 PE2* | SMC_TDI | IN | 47 48 |
| L4 PE3* | SMC_TDO | OUT | 47 48 |
| L2 PE4* | SMC_TMS | IN | 47 48 |
| M7 PF0 | G3_POWERON_L | IN | 47 |
| P6 PF1 | SMC_SYS_LED | OUT | 47 |
| R6 PF2 | SMC_LID | | 47 |
| N6 PF3 | NC | | |
| M6 PF4 | NC | | |
| R5 PF5 | BDV_BKL_PWM | OUT | 83 97 K62 PROTO-2:NEW |
| P5 PF6 | NC | | |
| N5 PF7 | NC | | |
| P9 PG0 | NC | | |
| R9 PG1 | SMC_SMS_INT | IN | 47 |
| N9 PG2 | SMB_BSA_DATA (OC) | BI | 49 |
| P8 PG3 | SMB_BSA_CLK (OC) | BI | 49 |
| R8 PG4 | SMB_A_S3_DATA (OC) | BI | 49 |
| M8 PG5 | SMB_A_S3_CLK (OC) | BI | 49 |
| P7 PG6 | SMB_B_S0_DATA (OC) | BI | 49 |
| R7 PG7 | SMB_B_S0_CLK (OC) | BI | 49 |
| E1 PH0 | SMC_PROCHOT | OUT | 47 97 |
| F3 PH1 | SMC_THRMTRIP | OUT | |
| K2 PH2 | NC | | |
| C4 PH3 | CPU_PECI_R | | 97 PECI |
| D4 PH4 | PVCCIO_S0_SMC_R | | PEVref |
| B3 PH5 | PM_PECI_PWRGD_R | | 97 PEVSTP |

R4910 0 MF-LF 5% 402 1/16W — CPU_PECI 11 21 97

R4911 0 MF-LF 5% 402 1/16W — =PPVCCIO_S0_SMC 6 47

R4912 0 MF-LF 5% 402 1/16W — PM_PECI_PWRGD 64 97

C4910 0.1UF 20% 10V CERM 402

SMC PB3: SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

SMC PG1: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

95 47 46 PP3V3_G3H_AVREF_SMC Peak/Ave/Standby = 2mA/1mA/5uA
47 46 6 =PP3V3_G3H_SMC Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA

C4902 22UF 20% 6.3V CERM 805
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place C4907 close to U4900 pin 13

R4999 4.7 5% 1/16W MF-LF 402 — Peak/Ave/Standby= 2mA/1mA/5uA
95 48 PP3V3_G3H_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.4V

C4920 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place R4999 close to U4900 pin 76
PLACEMENT_NOTE=Place C4920 close to U4900 pin 76

SMC_VCL
C4907 0.47UF 10% 6.3V CERM-X5R 402

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(3 OF 4)
OMIT

| Pin | Net | Dir | Note |
|---|---|---|---|
| N14 | AVCC | | |
| A1 | VCC | | |
| P1 | VCL | | |
| J15 | AVREF | | |
| F1 | | | |
| M14 | | | |
| E3 | RES* | | 97 48 47 SMC_RESET_L IN |
| A2 | XTAL | | 94 47 SMC_XTAL |
| B2 | EXTAL | | 94 47 SMC_EXTAL |
| E2 | MD1 | | SMC_MD1 IN 48 |
| K1 | MD2 | | SMC_KBC_MDE |
| F4 | NMI | | SMC_NMI IN 48 |
| L1 | ETRST* | | SMC_TRST_L IN 48 |
| R12 | AVSS | | NOSTUFF |
| D2, P4, F12, B13, A4 | VSS | | |

R4909 10K 5% 1/16W MF-LF 402
R4901 10K 5% 1/16W MF-LF 402
R4902 10K 5% 1/16W MF-LF 402
R4998 10K 5% 1/16W MF-LF 402
R4903 0 5% 1/16W MF-LF 402

XW4900 SM

GND_SMC_AVSS 46 47 50 94

95 47 46 PP3V3_G3H_AVREF_SMC
47 46 6 =PP3V3_G3H_SMC
95 46 PP3V3_G3H_SMC_AVCC

U4900
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LFBGA
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OMIT

| Pin | Net | Note |
|---|---|---|
| M15 | AVCC1 | |
| P2 | VCC3 | |
| M15 | AVREF1 | |
| E4, N4, M9, M12, M13, L12, A3 | NC | |
| C5 | NC | PJ0 |
| B8 | NC | PJ1 |
| C10 | NC | PJ2 |
| C12 | NC | PJ3 |
| A14 | NC | PJ4 |
| F15 | NC | PJ5 |
| J14 | NC | PJ6 |
| K15 | NC | PJ7 |
| N8 | NC | PI0 |
| N7 | NC | PI1 |
| M5 | NC | PI2 |
| L3 | NC | PI3 |
| K3 | NC | PI4 |
| H3 | NC | PI5 |
| H4 | NC | PI6 |
| G3 | NC | PI7 |
| P12 | AVSS1 | |
| R4, F13, A13, B4, D1 | VSS | |

94 50 47 46 GND_SMC_AVSS

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
# SMC

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DRAWING NUMBER 051-8115 SIZE D
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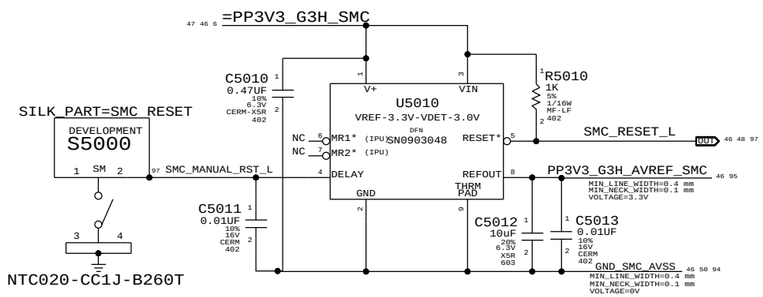
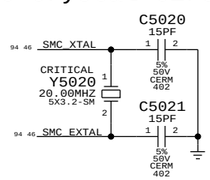
## SMC Reset "Button", Supervisor & AVREF Supply



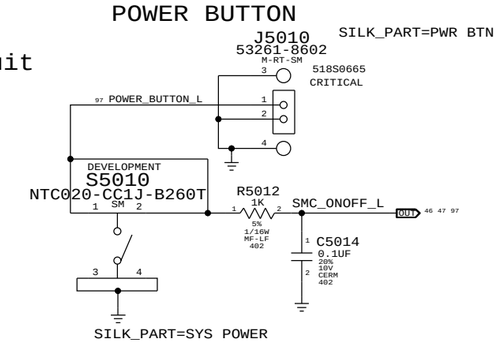

MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

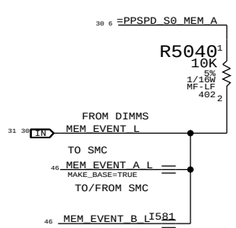
## SMC Crystal Circuit




## POWER BUTTON




## MEM_EVENT




## MISC. SIGNAL ALIASES

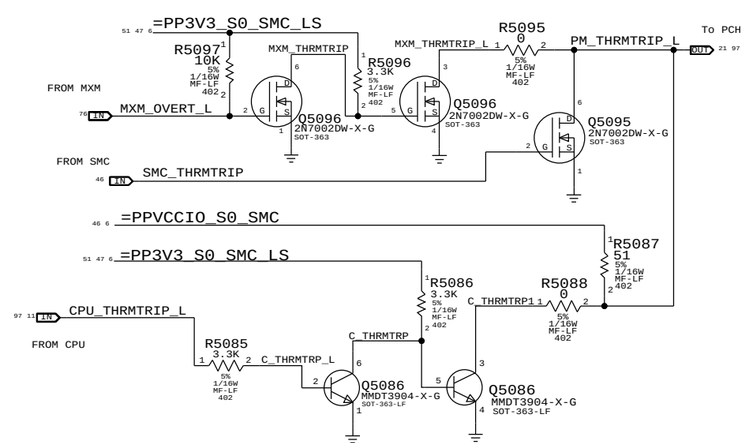
| | | |
|---|---|---|
| SMC_GFX_OVERTEMP_L | MXM_ALERT_L | MAKE_BASE=TRUE |
| SMC_GFX_THROTTLE_L | MXM_PWR_LEVEL | MAKE_BASE=TRUE |
| CPUIMVP_VR_ON | SMC_DELAYED_PWRGD | MAKE_BASE=TRUE |

UNUSED PORT 7 ANALOG SENSORS

## UNUSED TP/NC ALIASES

| | | |
|---|---|---|
| SMC_EXCARD_PWR_EN | TP_SMC_EXCARD_PWR_EN | MAKE_BASE=TRUE |
| SMS_ONOFF_L | TP_SMS_ONOFF_L | MAKE_BASE=TRUE |
| SMC_RSTGATE_L | TP_SMC_RSTGATE_L | MAKE_BASE=TRUE |
| SMC_SYS_LED | TP_SMC_SYS_LED | MAKE_BASE=TRUE |
| SMC_PB3 | TP_SMC_PB3 | MAKE_BASE=TRUE |

## SMC & MXM THERMTRIP LEVEL SHIFTING



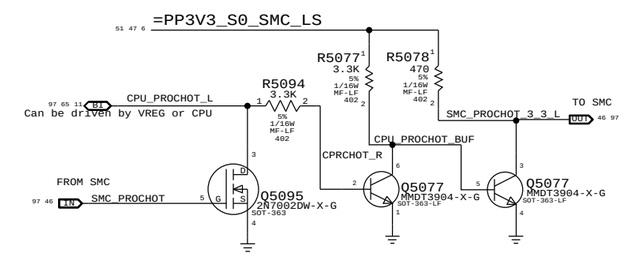

## =PP3V3_G3H_SMC

| | | | | |
|---|---|---|---|---|
| SMC_ONOFF_L | R5020 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_TX_L | R5021 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_RX_L | R5022 | 100K | 5% | 1/16W MF-LF 402 |
| SYS_ONEWIRE | R5023 | 2.0K | 5% | 1/16W MF-LF 402 |
| SMC_TMS | R5024 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_TDO | R5025 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_TDI | R5026 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_TCK | R5027 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_BIL_BUTTON_L | R5028 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_BC_ACOK | R5029 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_ADAPTER_EN | R5030 | 10K | 5% | 1/16W MF-LF 402 |
| USB_DEBUGPRT_EN_L | R5031 | 10K | 5% | 1/16W MF-LF 402 |
| G3_POWERON_L | R5034 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_SMS_INT | R5032 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_LID | R5033 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_PA0 | R5037 | 100K | 5% | 1/16W MF-LF 402 |
| SMC_PB6 | R5038 | 100K | 5% | 1/16W MF-LF 402 |
| SMC_PE0 | R5036 | 100K | 5% | 1/16W MF-LF 402 |

## =PP3V3_S0_SMC_LS

| | | | | |
|---|---|---|---|---|
| SMC_GFX_OVERTEMP_L | R5035 | 10K | 5% | 1/16W MF-LF 402 |
| SMC_RUNTIME_SCI_L | R5044 | 10K | 5% | 1/16W MF-LF 402 |
| PM_SLP_S3_L | R5041 | 100K | 5% | 1/16W MF-LF 402 |
| PM_SLP_S5_L | R5042 | 100K | 5% | 1/16W MF-LF 402 |
| PM_SLP_S4_L | R5043 | 100K | 5% | 1/16W MF-LF 402 |

## SMC PROCHOT 3.3V LEVEL SHIFTING




| | |
|---|---|
| SYNC_MASTER=K62 | SYNC_DATE=01/06/2011 |
| PAGE TITLE | SMC Support |
| Apple Inc. | DRAWING NUMBER 051-8115 SIZE D |
| | REVISION 11.1.0 |
| | BRANCH |
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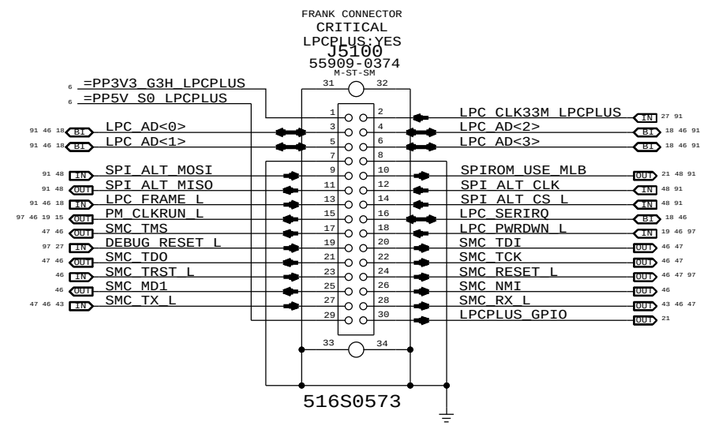
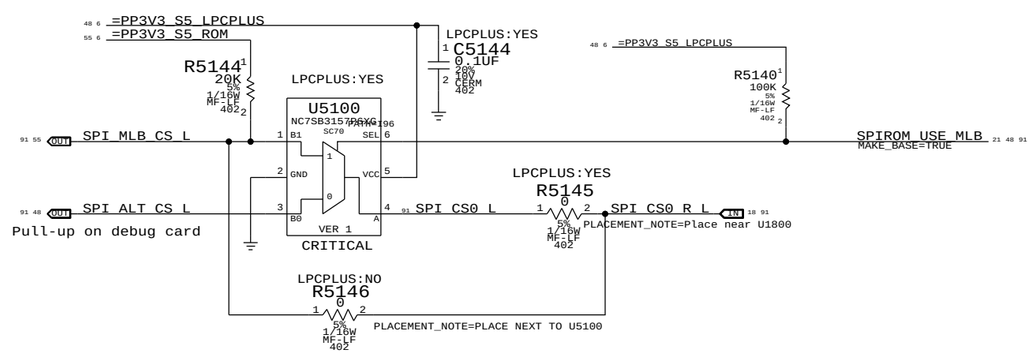
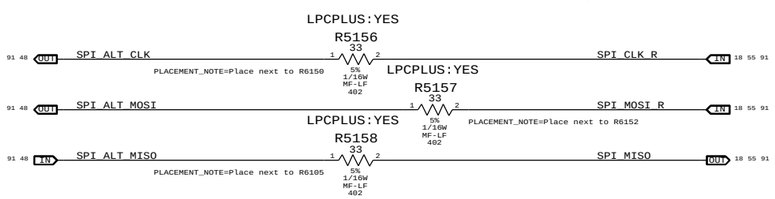
# LPC+SPI Connector




# Alternate SPI ROM Support




## SPI Bus Series Resistance Option




SYNC_MASTER=K62_AARON SYNC_DATE=11/30/2009

PAGE TITLE
LPC+SPI Debug Connector

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## PCH "SMBUS" CONNECTIONS

49 6 =PP3V3_S0_SMBUS

**PCH**
U1800
(MASTER)
94 18 SMBUS_PCH_CLK MAKE_BASE=TRUE
94 18 SMBUS_PCH_DATA MAKE_BASE=TRUE

R5208[1] 2.2K 5% 1/16W MF-LF 402 2
[1]R5209 2.2K 5% 1/16W MF-LF 402 2

**MEMORY A DIMMS**
J3100-A/B
(DIMM0: WRITE: 0XA0 READ: 0XA1)
(DIMM2: WRITE: 0XA2 READ: 0XA3)
=I2C_SODIMMA_SCL 30
=I2C_SODIMMA_SDA 30

**MEMORY B DIMMS**
J3200-A/B
(DIMM1: WRITE: 0XA4 READ: 0XA5)
(DIMM3: WRITE: 0XA6 READ: 0XA7)
=I2C_SODIMMB_SCL 31
=I2C_SODIMMB_SDA 31

**XDP (PCH)**
J2550
49 25 =SMBUS_XDP_SCL
49 25 =SMBUS_XDP_SDA

**MIKEY**
U6806
(WRITE: 0X72 READ: 0X73)
=I2C_AUDIO_SCL 62
=I2C_AUDIO_SDA 62

**XDP (CPU)**
J2500
49 25 =SMBUS_XDP_SCL
49 25 =SMBUS_XDP_SDA

**CK505**
U2600
(WRITE: 0XD2 READ: 0XD3)
=SMBUS_CK505_SCL 26
=SMBUS_CK505_SDA 26

**MEM VREF MARGIN A**
U2900
(WRITE: 0X5C READ: 0X5D)
=I2C_VREFMRGN_A_SCL 28
=I2C_VREFMRGN_A_SDA 28

**SPTX BLC MICRO**
VIA J602
(WRITE: 0X6E READ: 0X6F)
6 =SMB_BLC_PCH_SCL
6 =SMB_BLC_PCH_SDA

**MEM VREF MARGIN B**
U2910
(WRITE: 0X7C READ: 0X7D)
=I2C_VREFMRGN_B_SCL 28
=I2C_VREFMRGN_B_SDA 28

**DP SDRV "A"**
U9310, PS8301
(WRITE: 0X94, READ: 0X95)
=I2C_DPSDRVA_SCL 84
=I2C_DPSDRVA_SDA 84

## PCH "SML 0" CONNECTIONS

49 6 =PP3V3_S0_SMBUS

**PCH**
U1800
(MASTER)
94 18 SML_PCH_0_CLK MAKE_BASE=TRUE
94 18 SML_PCH_0_DATA MAKE_BASE=TRUE

R5202[1] 8.2K 5% 1/16W MF-LF 402 2
[1]R5203 8.2K 5% 1/16W MF-LF 402 2

THIS PAGE DIFFERENT BETWEEN K60 AND K62.

## SMC SLAVE SMBUS "2" CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 2 ONLY (NO CONNECTIONS, JUST PULLUP)

6 =PP3V3_S0_SMBUS_SMC_BSA

**SMC**
U4900
(SLAVE)
46 SMB_BSA_CLK — 94 SMBUS_SMC_BSA_SCL MAKE_BASE=TRUE
46 SMB_BSA_DATA — 94 SMBUS_SMC_BSA_SDA MAKE_BASE=TRUE

R5280[1] 100K 5% 1/16W MF-LF 402 2
[1]R5281 100K 5% 1/16W MF-LF 402 2

## SMC "B" SMBUS CONNECTIONS

BUS B CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K60/62 CHOOSES 0

6 =PP3V3_S0_SMBUS_SMC_B

**SMC**
U4900
(MASTER)
46 SMB_B_S0_CLK — 94 SMBUS_SMC_B_S0_SCL MAKE_BASE=TRUE
46 SMB_B_S0_DATA — 94 SMBUS_SMC_B_S0_SDA MAKE_BASE=TRUE

R5260[1] 2.0K 5% 1/16W MF-LF 402 2
[1]R5261 2.0K 5% 1/16W MF-LF 402 2

**AC/DC PS TEMPS**
EMC1403-[1,2] : ACDC THRU J600
(WRITE: 0X98 OR 0X9A, READ: 0X99 OR 0X9B)
3 SENSE POINTS - PRIMARY, SECONDARY, AMB
=SMB_ACDC_SCL 6
=SMB_ACDC_SDA 6

**AC/DC PS POWER**
INA219: ACDC THRU J600
(WRITE: 0X80, READ: 0X81)
OUTPUT VOLTAGE, CURRENT, POWER

## SMC "0" SMBUS CONNECTIONS

USES INTERNAL SMC CONTROLLER CHANNEL 0 ONLY

6 =PP3V3_S0_SMBUS_SMC_0

**SMC**
U4900
(MASTER)
46 SMB_0_S0_CLK — 94 SMBUS_SMC_0_S0_SCL MAKE_BASE=TRUE
46 SMB_0_S0_DATA — 94 SMBUS_SMC_0_S0_SDA MAKE_BASE=TRUE

R5250[1] 2.2K 5% 1/16W MF-LF 402 2
[1]R5251 2.2K 5% 1/16W MF-LF 402 2

Also reserve 0x56 and 0x32 per spec

**MXM TEMP**
GPU ON CARD - J8400
NV INSIDE (WRITE: 0X9E READ: 0X9F)
EMC1402 ON AMD MXM CARD (WRITE: 0X98 READ: 0X99)
=SMB_MXM_THRM_SCL 76
=SMB_MXM_THRM_SDA 76

**EMC1414: U5520**
DEV: CPU D,CPU HTSK
(WRITE: 0X78 READ: 0X79)
**EMC1428: U5500**
PROD: AMB,L-SKIN,R-SKIN,ODD, LCD,CPU PROX,MXM TEMPS
(WRITE: 0x92 READ:0x93)
=SMB_SNS1_SCL 52
=SMB_SNS1_SDA 52

**PCIE MINI-CARD X18 WI-FI MODULE**
TMP106: J3400
(WRITE: 0X90 READ: 0X91)
=SMB_MINI_SCL 33
=SMB_MINI_SDA 33

## PCH "SML 1" CONNECTIONS

49 6 =PP3V3_S0_SMBUS

**PCH (FOR TEMP)**
U1800
(SLAVE)
(WRITE: 0X86 READ: 0X89)
94 18 SML_PCH_1_CLK MAKE_BASE=TRUE
94 18 SML_PCH_1_DATA MAKE_BASE=TRUE

NOSTUFF R5204[1] 8.2K 5% 1/16W MF-LF 402 2
NOSTUFF [1]R5205 8.2K 5% 1/16W MF-LF 402 2

R5206 0 5% 1/10W MF-LF 402 1 2
R5207 0 5% 1/10W MF-LF 402 1 2

THE PCH address is user programmable by SPI ROM

## SMC "A" SMBUS CONNECTIONS

NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S3 STATE
BUS A CAN USE EITHER INTERNAL SMC CHANNEL 0 OR 1, K74 CHOOSES 1

6 =PP3V3_S3_SMBUS_SMC_A

**SMC**
U4900
(MASTER)
46 SMB_A_S3_CLK — 94 SMBUS_SMC_A_S3_SCL MAKE_BASE=TRUE
46 SMB_A_S3_DATA — 94 SMBUS_SMC_A_S3_SDA MAKE_BASE=TRUE

R5270[1] 4.7K 5% 1/16W MF-LF 402 2
[1]R5271 4.7K 5% 1/16W MF-LF 402 2

**ALS**
(WRITE: 0X52 READ: 0X53)
=SMB_ALS_SCL 44
=SMB_ALS_SDA 44

## SMC "MANAGEMENT" SMBUS (BUS 1)

USES INTERNAL SMC CONTROLLER CHANNEL 1 ONLY

6 =PP3V3_S0_SMBUS_SMC_MGMT

**SMC**
U4900
(MASTER)
46 SMB_MGMT_CLK — 94 SMBUS_SMC_MGMT_SCL MAKE_BASE=TRUE
46 SMB_MGMT_DATA — 94 SMBUS_SMC_MGMT_SDA MAKE_BASE=TRUE

R5290[1] 2.2K 5% 1/16W MF-LF 402 2
[1]R5291 2.2K 5% 1/16W MF-LF 402 2

**PANEL TEMP SENSOR**
TMP421 ON TCON BOARD VIA J9002
(SLAVE)
(WRITE: 0X9E READ: 0X9F)
SMB_DP_TCON_SLA_SCL 81
SMB_DP_TCON_SLA_SDA 81

**DISPLAY TCON**
PARADE ON TCON BOARD VIA J9002
(SLAVE)
(TBD WRITE: 0X1A READ: 0X1B)
(TO READ VENDOR ID AND PANEL ID)
TCON ALSO HAS MASTER BUS TO LUT ROM AND EDID ROM.

## DISPLAY TCON TO SPTX OR O2M BLC

49 6 =PP3V3_S0_SMBUS

**DISPLAY TCON**
VIA J9002
(MASTER)
=SMB_DP_TCON_SDA — MAKE_BASE=TRUE
=SMB_DP_TCON_SCL — MAKE_BASE=TRUE

R5210[1] 2.2K 5% 1/16W MF-LF 402 2
[1]R5211 2.2K 5% 1/16W MF-LF 402 2

**BLC MICRO**
VIA J602
(SLAVE)
(WRITE: 0X6E READ: 0X6F)
SMB_BLC_TCON_SDA 84 81 6 MUX
SMB_BLC_TCON_SCL 84 81 BS

NOTE: DISPLAY TCON HAS 4.7K PU.
NOTE: SPTX BLC HAS 4.7K PU.
NOTE: O2Micro BLC HAS NO PU.

## T29 I2C CONNECTIONS

6 =PP3V3_S0_T29I2C

I2C BUS PULL-UP RAIL MUST REFLECT WHEN USB POWER (VBUS) IS VALID.

**T29 IC**
U9700
(MASTER)
96 86 I2C_T29_SCL MAKE_BASE=TRUE
96 86 I2C_T29_SDA MAKE_BASE=TRUE

T29 R5230[1] 4.7K 5% 1/16W MF-LF 402 2
T29 [1]R5231 4.7K 5% 1/16W MF-LF 402 2

**T29 PORT A MCU**
U9330
(WRITE: 0X26 READ: 0X27)
=I2C_T29AMCU_SCL 84
=I2C_T29AMCU_SDA 84

SYNC_MASTER=K60_MARK SYNC_DATE=01/06/2011

PAGE TITLE
# SMBUS CONNECTIONS

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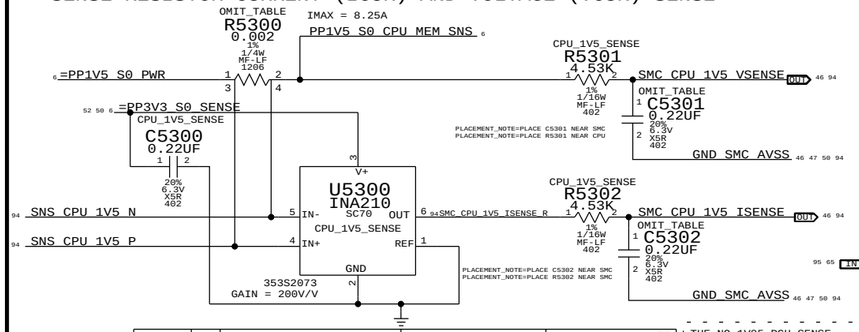
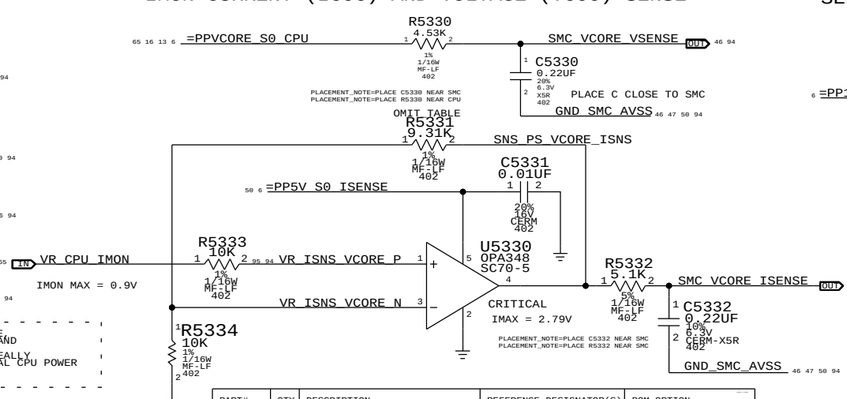
## CPU VDD 1.5V
### SENSE RESISTOR CURRENT (IC5R) AND VOLTAGE (VC5R) SENSE




| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 104S0018 | 1 | RES,2 MILLIOHM,1206 | R5300 | CPU_1V5_SENSE |
| 101S0414 | 1 | RES,0 OHM,1206,20 MILLIOHM MAX | R5300 | NO_CPU_1V5_SENSE |
| 132S0080 | 2 | CAP,0.22UF,402 | C5301,C5302 | CPU_1V5_SENSE |
| 116S0004 | 2 | RES,0 OHM,402 | C5301,C5302 | NO_CPU_1V5_SENSE |

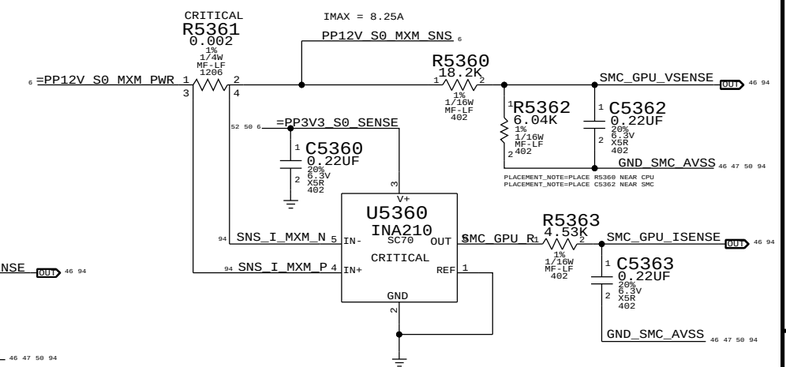
THE NO_1V05_PCH_SENSE, NO_CPU_VCCSA_SENSE, AND NO_CPU_1V5_SENSE BOMOPTIONS SHOULD IDEALLY NEVER BE USED AS TOTAL CPU POWER SENSING REQUIRES ALL 3 SENSORS.

## CPU VCC (VCORE)
### IMON CURRENT (IC0C) AND VOLTAGE (VC0C) SENSE

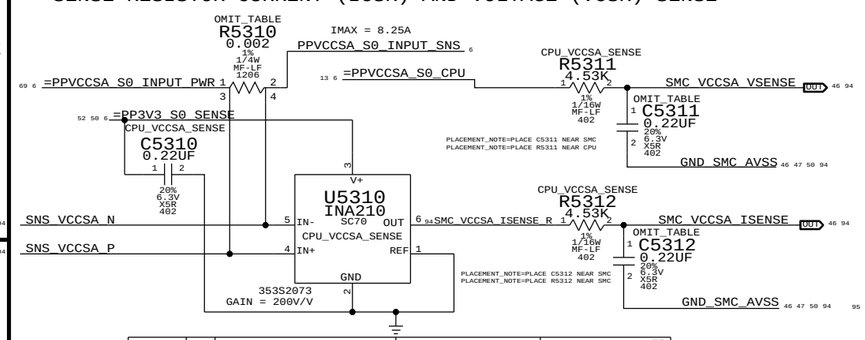



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 114S0312 | 1 | RES,MTL FILM,1/16W,9.31K,0402 | R5331 | CPUVCORE-3PH |
| 114S0345 | 1 | RES,MTL FILM,1/16W,21K,0402 | R5331 | CPUVCORE-4PH |

## GPU MXM
### SENSE RESISTOR CURRENT (IG0R) AND VOLTAGE (VG0R) SENSE

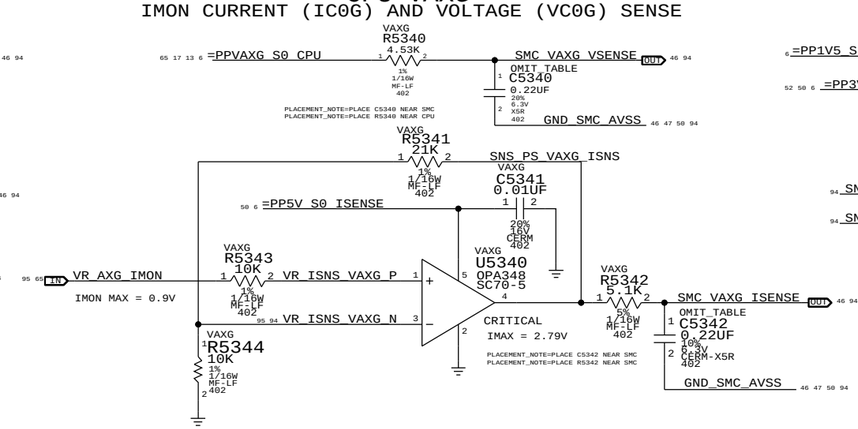



## CPU VCCSA
### SENSE RESISTOR CURRENT (ICSR) AND VOLTAGE (VCSR) SENSE



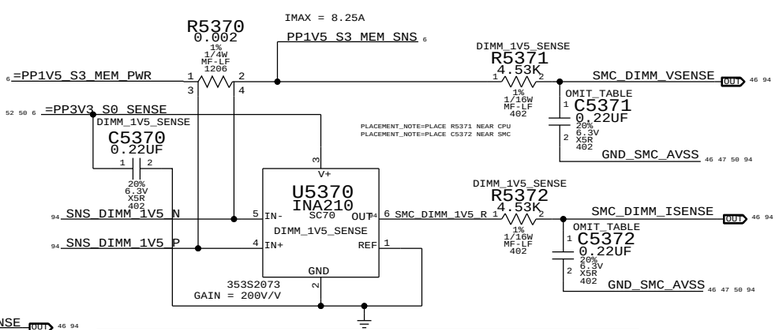

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 104S0018 | 1 | RES,2 MILLIOHM,1206 | R5310 | CPU_VCCSA_SENSE |
| 101S0414 | 1 | RES,0 OHM,1206,20 MILLIOHM MAX | R5310 | NO_CPU_VCCSA_SENSE |
| 132S0080 | 2 | CAP,0.22UF,402 | C5311,C5312 | CPU_VCCSA_SENSE |
| 116S0004 | 2 | RES,0 OHM,402 | C5311,C5312 | NO_CPU_VCCSA_SENSE |

## CPU VAXG
### IMON CURRENT (IC0G) AND VOLTAGE (VC0G) SENSE



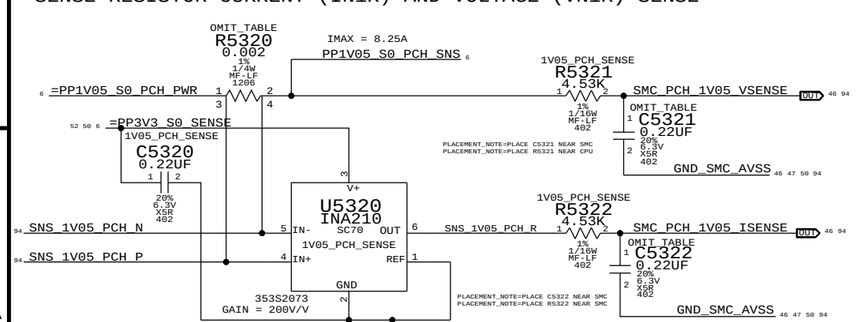

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 132S0080 | 2 | CAP,0.22UF,402 | C5340,C5342 | VAXG |
| 116S0004 | 2 | RES,0 OHM,402 | C5340,C5342 | NO_VAXG |

## DIMM VDD 1.5V (LIKELY DEVELOPMENT ONLY)
### SENSE RESISTOR CURRENT (IM0R) AND VOLTAGE (VM0R) SENSE



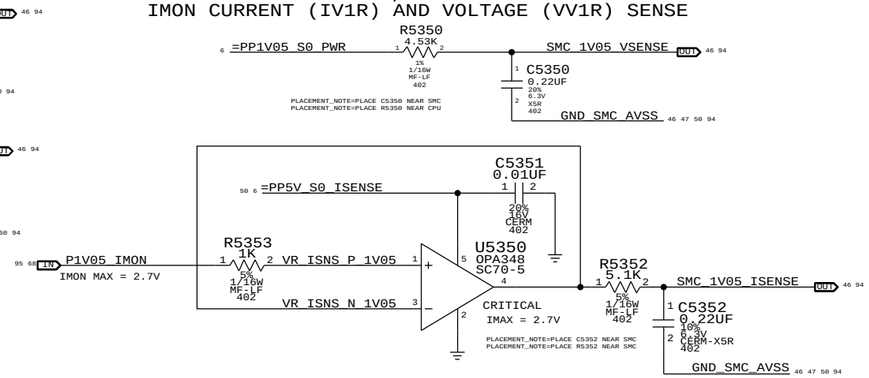

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 132S0080 | 2 | CAP,0.22UF,402 | C5371,C5372 | DIMM_1V5_SENSE |
| 116S0004 | 2 | RES,0 OHM,402 | C5371,C5372 | PRODUCTION |

## PCH 1.05V
### SENSE RESISTOR CURRENT (IN1R) AND VOLTAGE (VN1R) SENSE




| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 104S0018 | 1 | RES,2 MILLIOHM,1206 | R5320 | 1V05_PCH_SENSE |
| 101S0414 | 1 | RES,0 OHM,1206,20 MILLIOHM MAX | R5320 | NO_1V05_PCH_SENSE |
| 132S0080 | 2 | CAP,0.22UF,402 | C5321,C5322 | 1V05_PCH_SENSE |
| 116S0004 | 2 | RES,0 OHM,402 | C5321,C5322 | NO_1V05_PCH_SENSE |

## 1.05V FOR CPU VCCIO, CPU VCCSA & PCH 1.05V
### IMON CURRENT (IV1R) AND VOLTAGE (VV1R) SENSE




NOTE: TOTAL CPU POWER = VC0C*IC0C + VC5R*IC5R + VCSR*ICSR + VC0G*IC0G + VV1R*ICIR

where ICIR = IV1R - IN1R - ICSR

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
# CPU/PCH/GPU POWER SENSE

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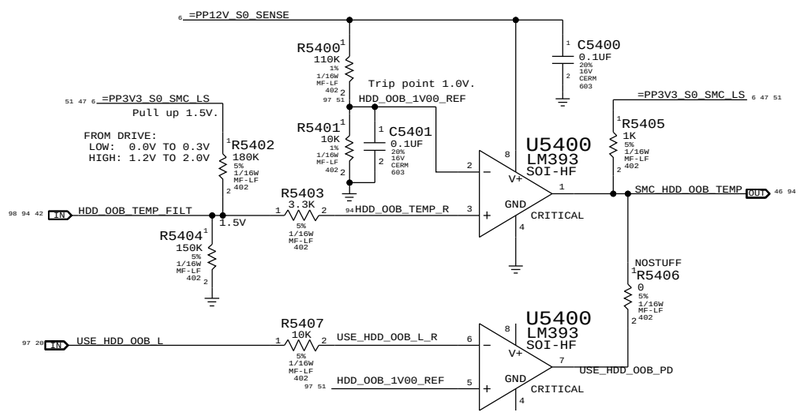
# HDD OOB TEMPERATURE SENSING




DRIVE ACTIVE = VALID SIGNAL PROTOCOL BETWEEN 0-2.0V.
DRIVE ASLEEP = HDD DRIVES HDD_OOB_TEMP LOW
DRIVE ABSENT = OOB IS PULLED HIGH UNLESS PCH DETERMINES SSD PRESENT AND DRIVES USE_HDD_OOB_L LOW WHICH THEN PULLS HDD_OOB_TEMP LOW.

NOTE: WILL BE CONNECTED TO SATA PWR CONNECTOR PIN 11
THIS PIN IS ORIGINALLY INTENDED FOR HDD LED OUTPUT,
AND ALSO FOR HDD STAGGERED PIN UP (FLOATING) OR IMMEDIATE SPIN-UP (GROUND).
BOTH FUNCTIONS NOT USED.

SYNC MASTER=K62 SYNC DATE=01/06/2011

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HDD OOB SENSE

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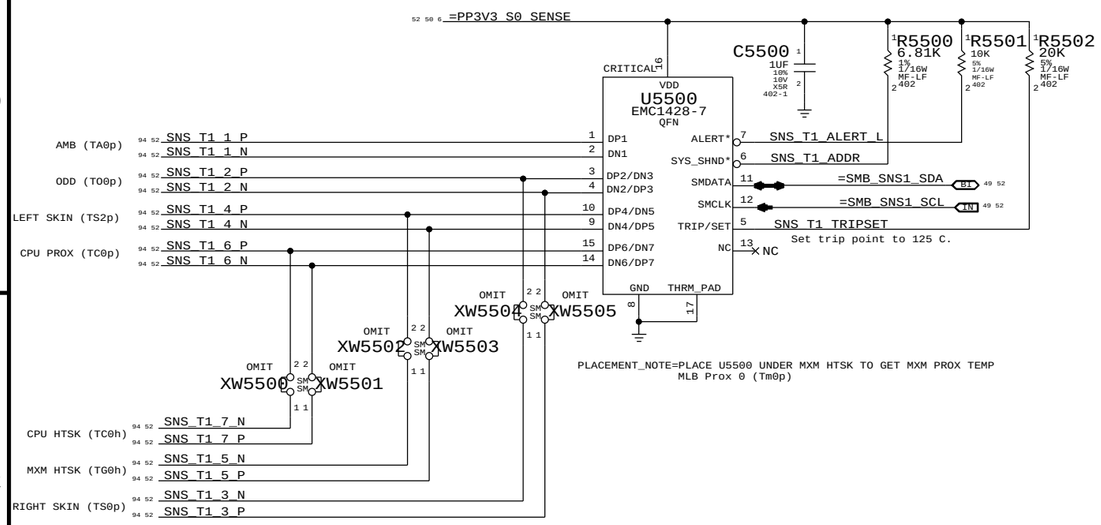
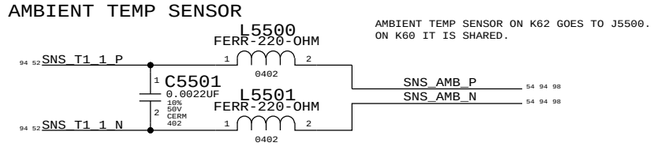
# SNS T1: PRODUCTION TEMP SENSOR IC



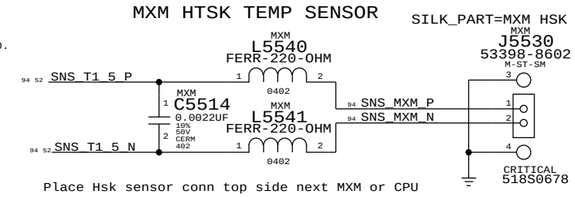

EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

## AMBIENT TEMP SENSOR



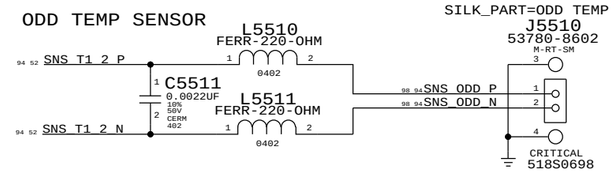

AMBIENT TEMP SENSOR ON K62 GOES TO J5500.
ON K60 IT IS SHARED.

## MXM HTSK TEMP SENSOR

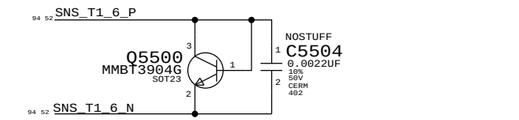



Place Hsk sensor conn top side next MXM or CPU

## ODD TEMP SENSOR

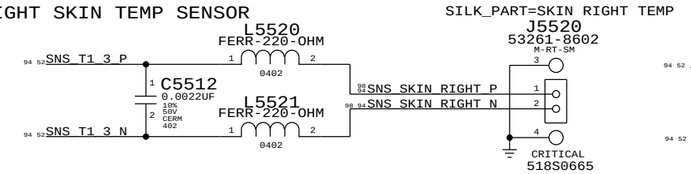



## CPU PROXIMITY TEMP SENSOR

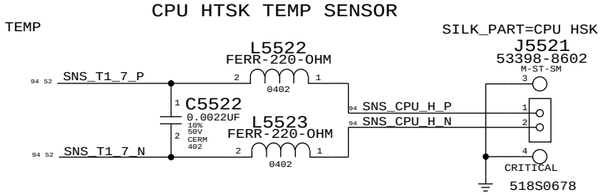



Place Q5500 (CPU Proximity Sensor) at the solder side
at edge near backer plate of CPU to replace HeatSink Temp Sensor

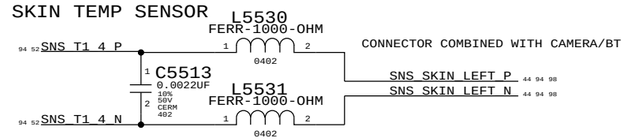
## RIGHT SKIN TEMP SENSOR




## CPU HTSK TEMP SENSOR

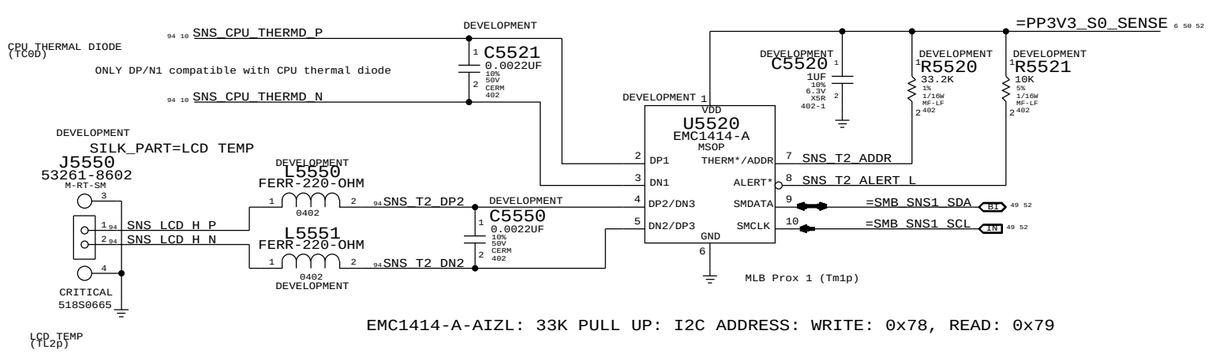



## LEFT SKIN TEMP SENSOR




THIS PAGE DIFFERENT BETWEEN K60 AND K62.

# SNS T2: DEVELOPMENT TEMP SENSOR IC




EMC1414-A-AIZL: 33K PULL UP: I2C ADDRESS: WRITE: 0x78, READ: 0x79

| | |
|---|---|
| SYNC MASTER=K60 MARK | SYNC DATE=01/06/2011 |
| PAGE TITLE: TEMP SENSORS | |
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| | REVISION: 11.1.0 |
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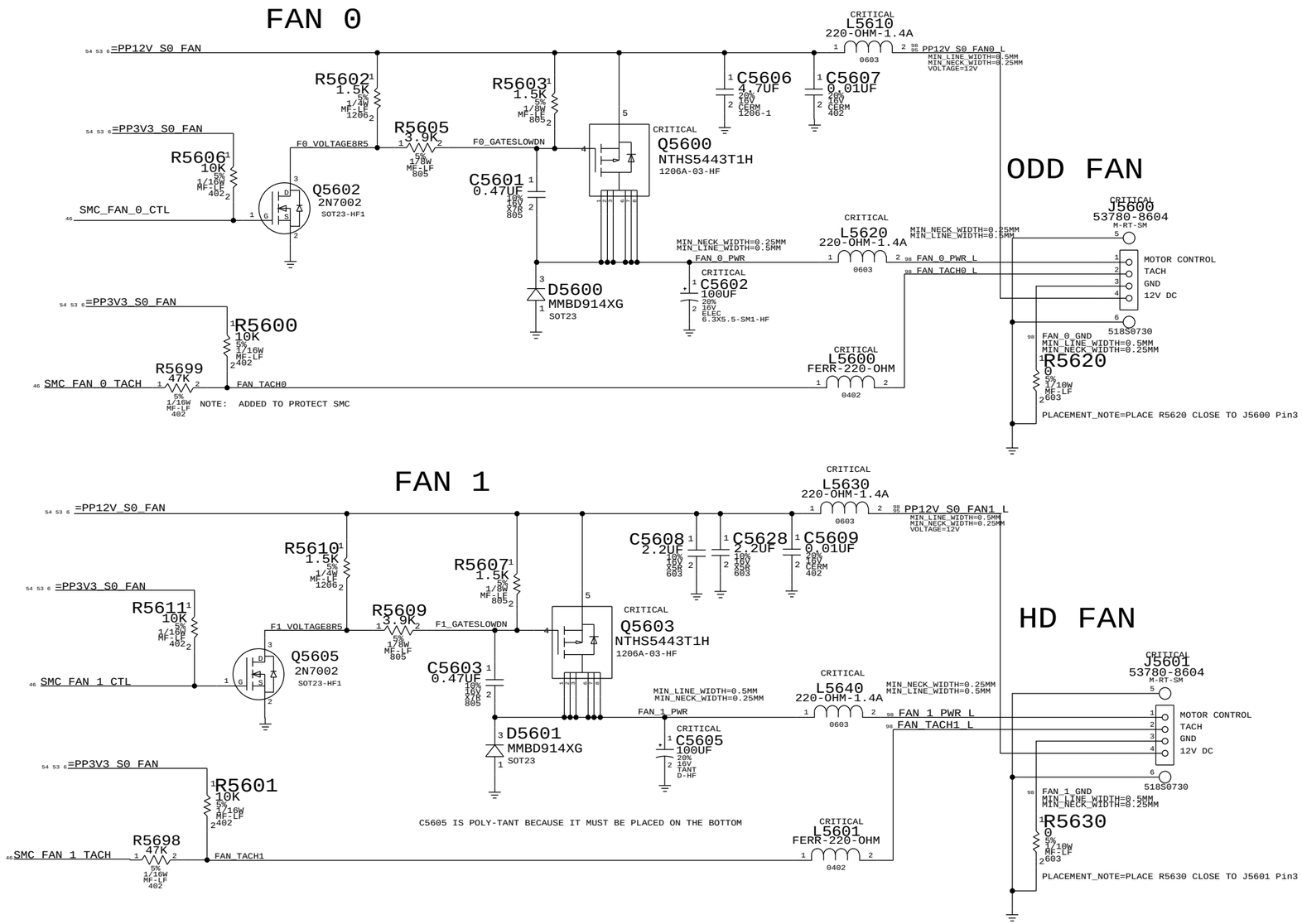


SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

# HD AND OD FAN

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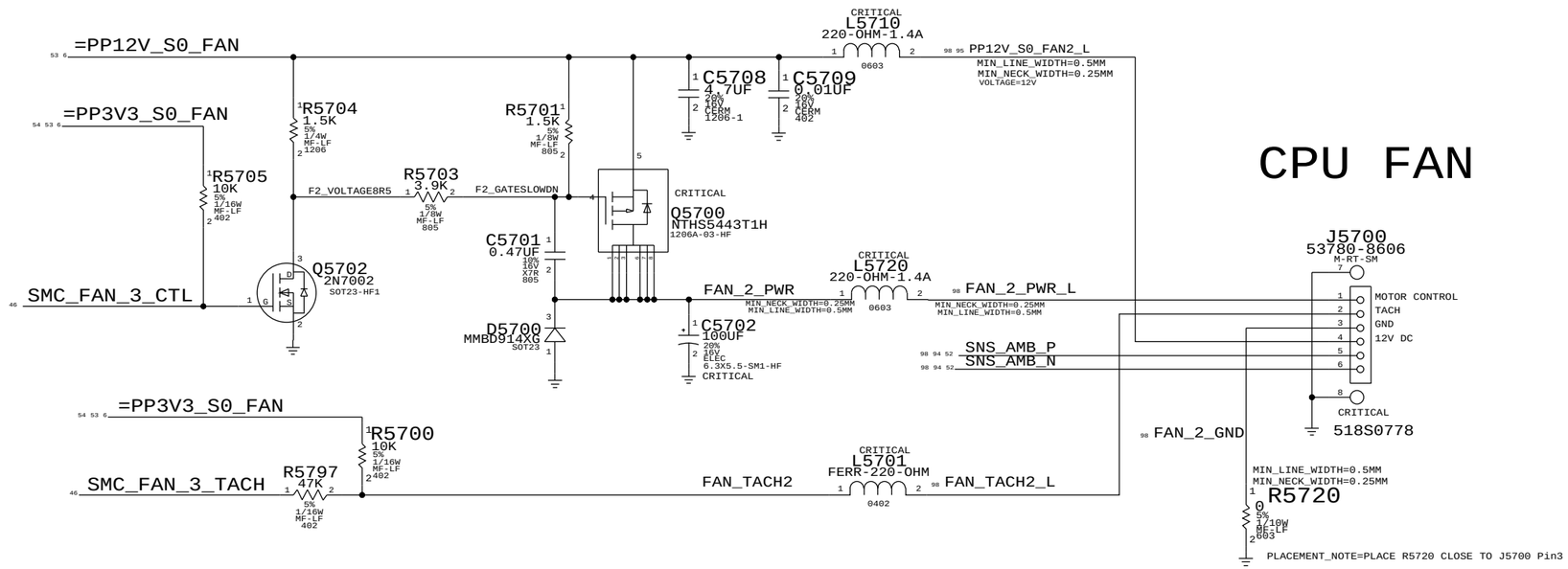
## SMC'S FAN3 OUTPUT CONTROL FAN 2




CPU FAN

## FAN 3 SMC CONTROL (UNUSED)

| | |
|---|---|
| SYNC_MASTER=K60_JERRY | SYNC_DATE=01/06/2011 |
| PAGE TITLE: CPU FAN | |
| Apple Inc. | DRAWING NUMBER: 051-8115 SIZE: D |
| | REVISION: 11.1.0 |
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| | PAGE: 57 OF 110 |
| | SHEET: 54 OF 98 |

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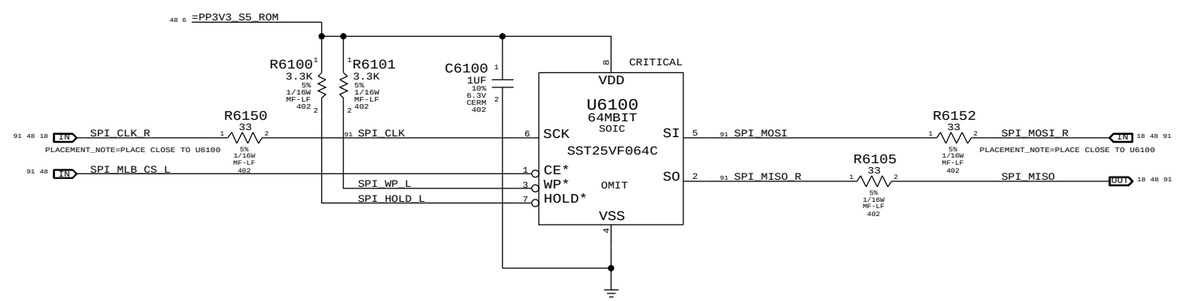


SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

# SPI ROM

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

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# AUDIO CODEC

APPLE P/N 353S2592

PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6201 4.7UF 20% 4V X5R-1 402

C6200 0.47UF 10% 10V X5R 402

C6208 10UF 20% 10V POLY-TANT CASE-B2-SM

GND_AUDIO_HPAMP

PP4V5_AUDIO_ANALOG

R6200 2.67K 1% 1/16W MF-LF 402

C6209 2.2UF 20% 6.3V CERM 402-LF

C6210 2.2UF 20% 6.3V CERM 402-LF

VBIAS_DAC

CS4206_FP

CS4206_FN

C6202 0.47UF 10% 10V X5R 402

C6203 10UF 20% 10V POLY-TANT CASE-B2-SM

C6205 1UF 10% 10V X5R 402-1

C6204 0.47UF 10% 10V X5R 402

C6206 0.47UF 10% 10V X5R 402

CRITICAL C6207 10UF 20% 6.3V CERM-X5R 0402-1

GND_AUDIO_CODEC

PP5V_AUDIO_HPAMP

=PP3V3_S0_AUDIO

PP4V5_AUDIO_ANALOG

GND_AUDIO_HPAMP

R6205 0 5% 1/16W MF-LF 402

CRITICAL U6201 CS4206B QFN

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 29 | VBIAS_DAC | | |
| 44 | VHP_FILT+ | 38 | HPOUT_L |
| 41 | VHP_FILT- | 40 | HPOUT_R |
| | | 39 | HPREF |
| 2 | GPIO0/DMIC_SDA1 | 35 | LINEOUT_L1+ |
| 12 | GPIO1/DMIC_SDA2/SPDIF_OUT2 | 34 | LINEOUT_L1- |
| 14 | GPIO2 | 36 | LINEOUT_R1+ |
| 15 | GPIO3 | 37 | LINEOUT_R1- |
| 13 | SENSE_A | 31 | LINEOUT_L2+ |
| | | 30 | LINEOUT_L2- |
| | | 32 | LINEOUT_R2+ |
| | | 33 | LINEOUT_R2- |
| 45 | FLYP | | |
| 43 | FLYC | | |
| 42 | FLYN | | |
| 3 | VL_HD | | |
| 1 | VL_IF | | |
| 6 | BITCLK | | |
| 10 | SYNC | | |
| 8 | SDI | | |
| 5 | SDO | | |
| 11 | RESET* | | |
| 47 | SPDIF_IN | | |
| 48 | SPDIF_OUT | | |
| | | 16 | MICBIAS |
| | | 28 | VCOM |
| | | 21 | LINEIN_L+ |
| | | 22 | LINEIN_C- |
| | | 23 | LINEIN_R+ |
| | | 18 | MICIN_L+ |
| | | 17 | MICIN_L- |
| | | 19 | MICIN_R+ |
| | | 20 | MICIN_R- |
| | | 27 | VREF+_ADC |
| | | 4 | DMIC_SCL |

VD VA_REF VA_HP VA

DGND THRM PAD AGND

MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM

MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM

TWEETERS

AUD_HP_L_P

AUD_HP_R_P

AUD_HP_PORT_REF

AUD_LO1_L_P

AUD_LO1_L_N

AUD_LO1_R_P

AUD_LO1_R_N

AUD_LO2_L_P

TP_AUD_LO2_N_L NC

AUD_LO2_R_P

TP_AUD_LO2_N_R NC

WOOFERS

AUD_CODEC_MICBIAS

CS4206_VCOM MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

AUD_LI_P_L

AUD_LI_COM

AUD_LI_P_R

AUD_MIC_INP_L

AUD_MIC_INN_L

AUD_MIC_INR_P

AUD_MIC_INR_N

CS4206_VREF_ADC NC MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

TP_CS4206_DMIC_SCL NC

HP AMP SPEAKERS

NC TP_AUD_DMIC_SDA1

NC TP_AUD_GPIO_1

AUD_GPIO_2

AUD_GPIO_3

AUD_SENSE_A

CS4206_FLYP

CS4206_FLYC

CS4206_FLYN

C6211 2.2UF 20% 6.3V CERM 402-LF

C6212 2.2UF 20% 6.3V CERM 402-LF

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK

HDA_SYNC

HDA_SDIN0

R6201 22 5% 1/16W MF-LF 402

AUD_SDI_R

HDA_SDOUT

HDA_RST_L

AUD_SPDIF_IN_CODEC

AUD_SPDIF_OUT

R6202 22 5% 1/16W MF-LF 402

AUD_SPDIF_CHIP

R6203 100K 1% 1/16W MF-LF 402

GND_AUDIO_HPAMP

GND_AUDIO_CODEC

CRITICAL C6213 10UF 10% 20% TANT CASE-P3-HF

CRITICAL C6214 10UF 20% 10% POLY-TANT CASE-B2-SM

XW6200 AUD_HP_L_N

XW6201 AUD_HP_R_N

HP AMP/LINE OUT

PLACE XWS 6200 & 6201 NEAR PINS 38 & 40

XW6202 AUD_LO2_L_N

XW6203 AUD_LO2_R_N

PLACE XWS 6202 & 6203 NEAR PINS 35 & 36

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 353S2592 | 353S3199 | | U6201 | CS4206A |

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

## APPLE P/N 353S2456
## 4.5V POWER SUPPLY FOR CODEC

XW6212 PP5V_AUDIO_HPAMP

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=4.5V

NOSTUFF L6212 FERR-220-OHM 0402

PP5V_LAMP_VREG

L6210 FERR-220-OHM 0402

=PP5V_S0_AUDIO

R6220 0 5% 1/16W MF-LF 402

VR6201 TPS71745 SON CRITICAL

4V5_REG_IN 4V5_REG_EN 4V5_OUT 4V5_NR

R6213 0 5% 1/16W MF-LF 603

PP4V5_AUDIO_ANALOG

NOSTUFF C6221 1UF 10% 10V X5R 402-1

C6222 1UF 10% 10V X5R 402-1

C6223 0.1UF 10% 10V X7R-CERM 402

C6224 1UF 10% 10V X5R 402-1

GND_AUDIO_CODEC MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

NOSTUFF R6212 0 5% 1/16W MF-LF 402

R6210 0 5% 1/16W MF-LF 603

XW6211 GND_AUDIO_HPAMP MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM VOLTAGE=0V

## ISOLATED 5 V POWER SUPPLY FOR HP AMP

APN 152S1314

CRITICAL T6250 1.8UH-1.6A-243MOHM LPD3015-SM

AUD_XFRMR_SEC

D6252 DO222-SM STPS1L30MF

PP5V_AUDIO_ISO MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V

=PP5V_S0_AUDIO

C6250 10UF 20% 10V X5R 603

CRITICAL Q6250 DMMT3906W-7-F SOT-363

NOSTUFF R6258 1K 1% 1/16W MF-LF 402

CRITICAL C6256 1UF 10% 25V X5R 402

R6255 1.0K 1% 1/10W MF-LF 603

SC4503_SW

SC4503_SW_SNBR MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

CRITICAL C6258 150UF-.025-OHM 20% 6.3V TANT CASE-B2-SM APN 128S0271

C6259 10UF 20% 10V X5R 603

R6257 4.99K 1% 1/10W MF-LF 603

GND_AUDIO_ISO MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

SC4503_FB_DDROP

C6257 0.1UF 10% 16V X7R-CERM 402

R6256 49.9K 1% 1/16W MF-LF 402

D6250 SOD-523 BAT54XV2T1

R6260 10 1% 1/10W MF-LF 603

GND_AUDIO_ISO

R6254 20 1% 1/16W MF-LF 603

APN 353S3080

DMMT3906W-7-F SOT-363 CRITICAL Q6250

SC4503_SW MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM

SC4503_FB_RDIV SC4503_FB_PNP

R6253 43.2K 1% 1/16W MF-LF 402

SC4503_FB_FILT

D6251 SOD-523 BAT54XV2T1

SC4503_SW_D

R6250 40.2K 1% 1/16W MF-LF 402

U6250 SC4503 TSOT-23 SYM VER 2 CRITICAL

IN SW SHDN*/SS FB GND

SC4503_SHDN

MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM SC4503_FB

R6251 3.40K 1% 1/16W MF-LF 402

R6252 12.4K 1% 1/16W MF-LF 402

C6252 0.1UF 10% 16V X7R-CERM 402

C6251 0.1UF 10% 16V X7R-CERM 402

NOSTUFF C6253 1UF 10% 16V X5R 402-1

C6254 0.01UF 10% 16V CERM 402

NOSTUFF C6261 0.001UF 10% 50V X7R 402

NOSTUFF R6259 100K 1% 1/16W MF-LF 402

C6255 0.001UF 10% 50V X7R 402

SYNC MASTER=K60_DAVID SYNC DATE=01/06/2011

PAGE TITLE

# AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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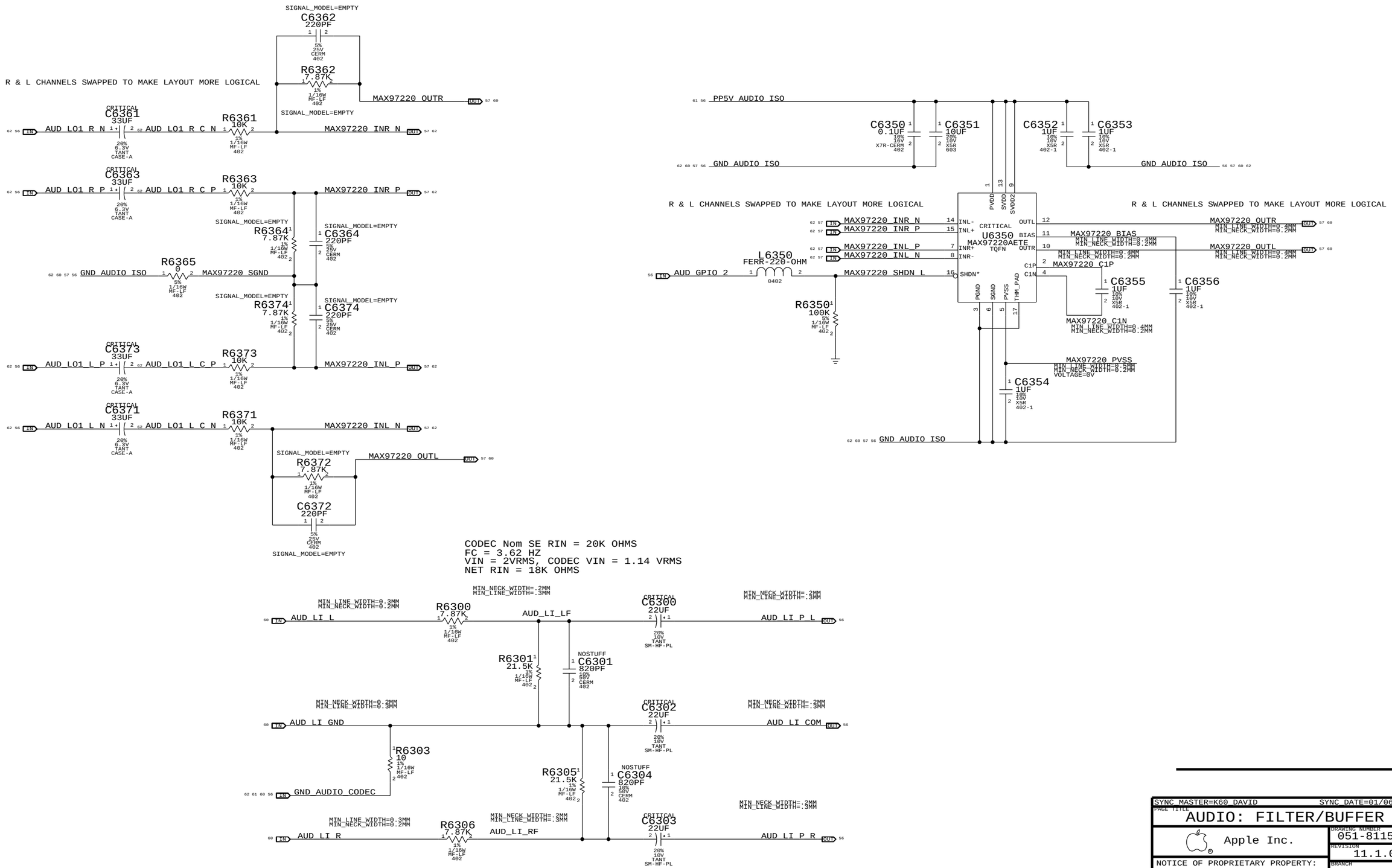


SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
# AUDIO: FILTER/BUFFER

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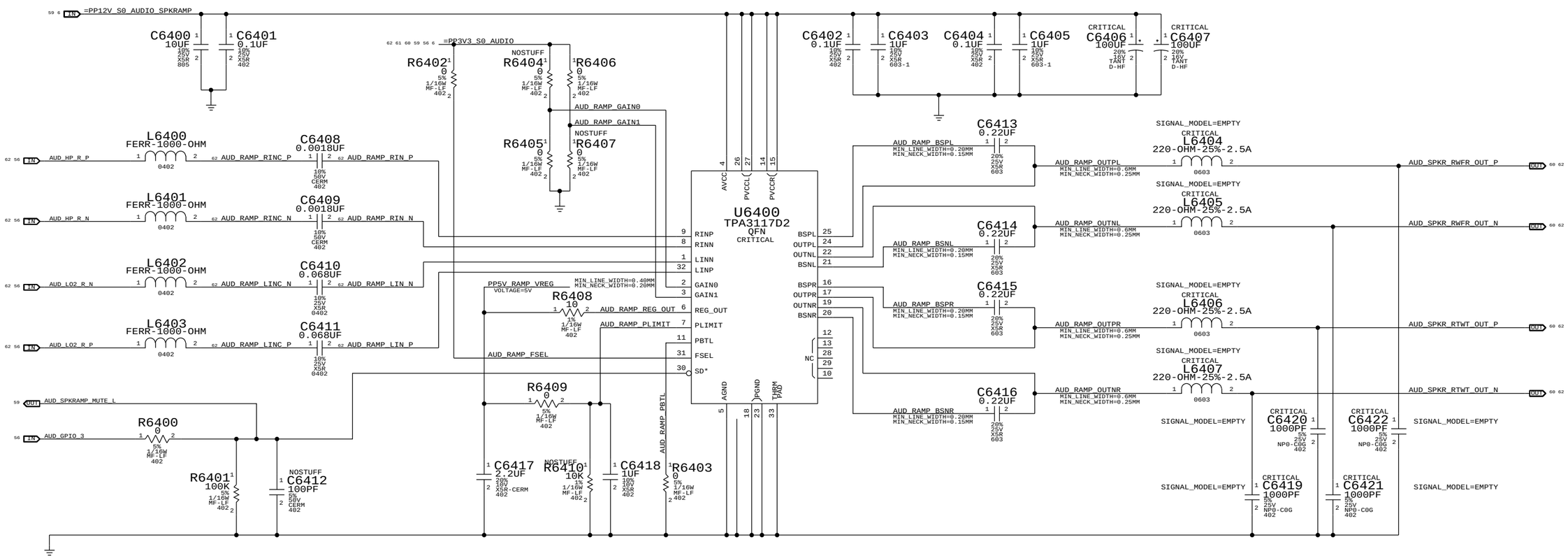
# RIGHT CH SPEAKER AMP

APPLE P/N 353S3069

R6402 = HIGH = 400 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)




SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
AUDIO: SPEAKER AMP_1

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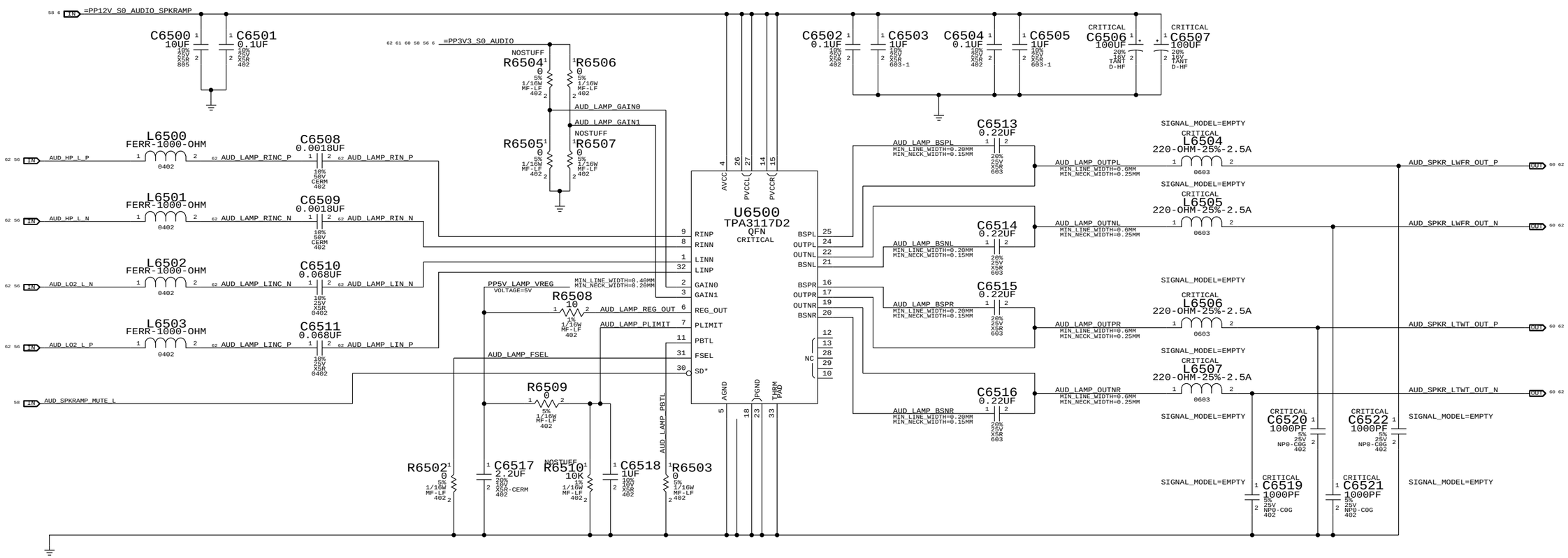
# LEFT CH SPEAKER AMP
APPLE P/N 353S3069

R6502 = LOW = 300 KHZ
SPEAKER AMP GAIN = +15.2 DB
SPEAKER AMP RIN = 104K NOMINAL W/ +15.2 DB GAIN
FC_HPF, TWEETERS = ~850 HZ (0.0018 UF)
FC_HPF, WOOFERS = ~22.5 HZ (0.068 UF)




SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D
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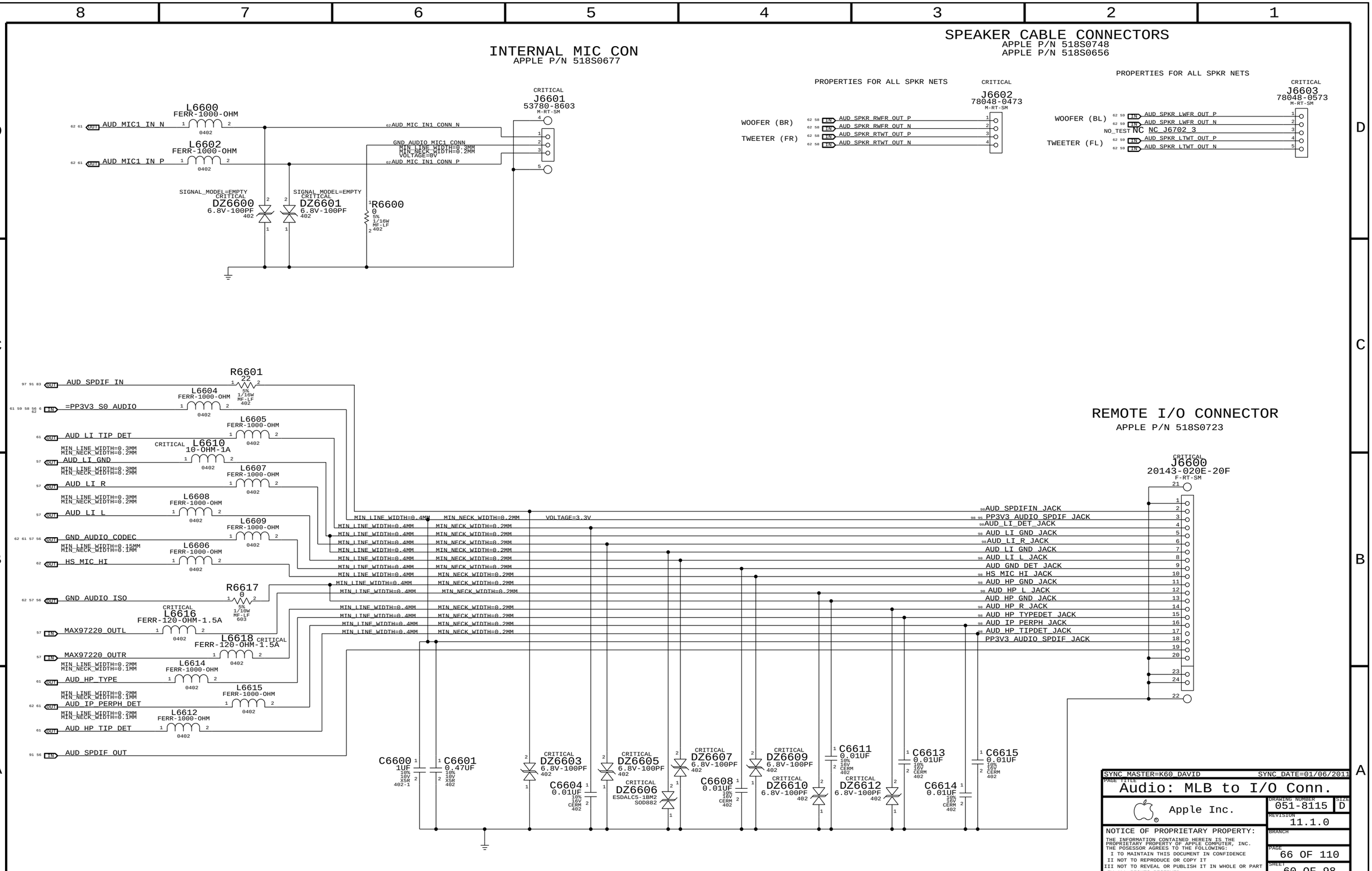


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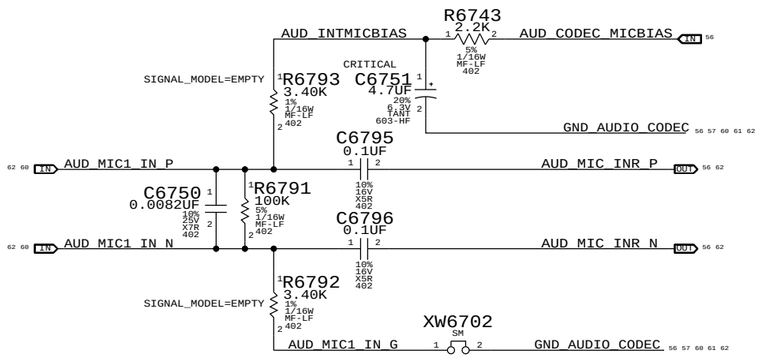
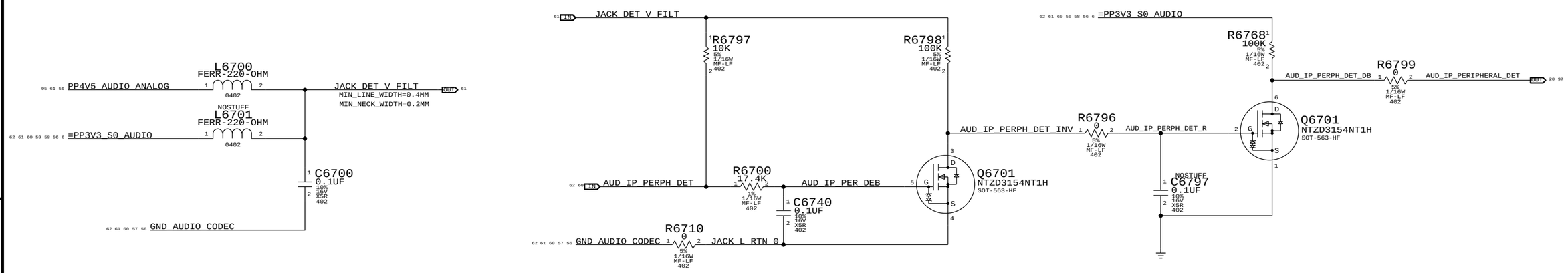
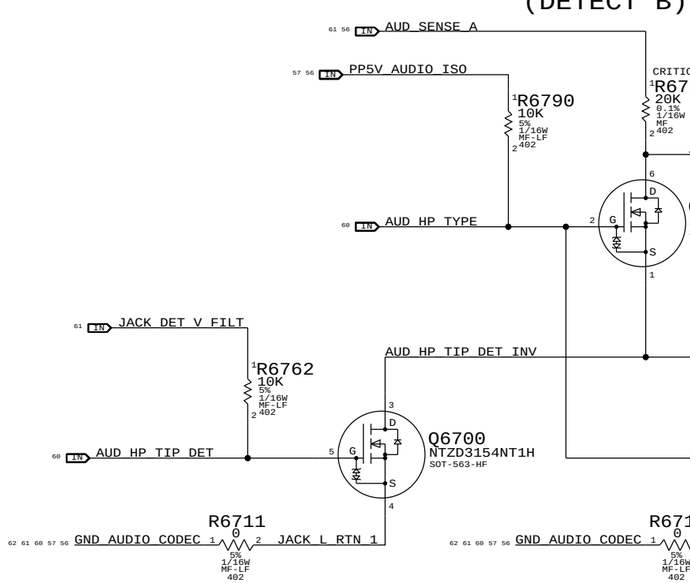
## Internal Microphone Impedance Matching



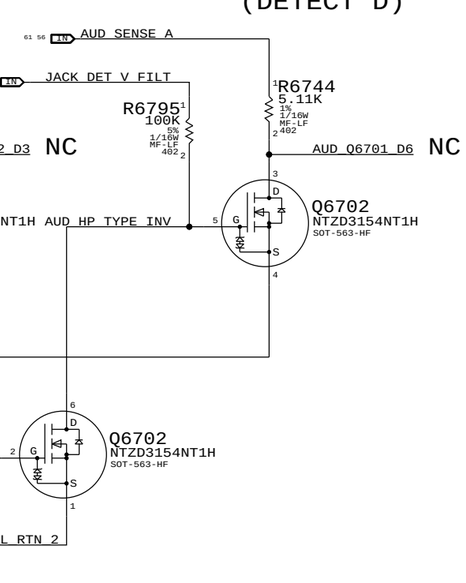

## IPHS HS Detect Debounce CKT



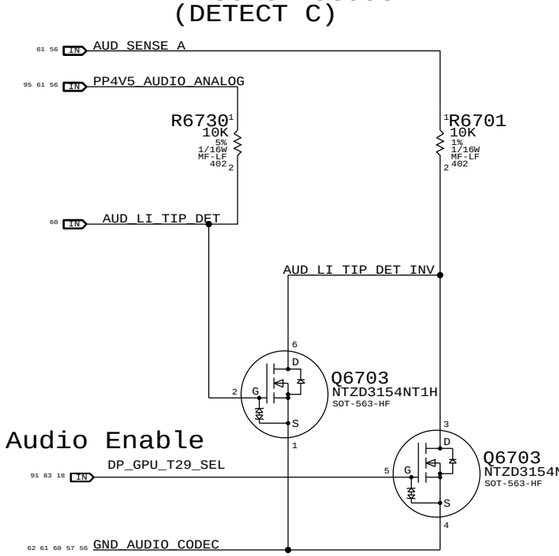

## Digital Out (DETECT B)




## Headphone Out (DETECT D)




## LI Insert Detect (DETECT C)




## DP Audio Enable

DP_GPU_T29_SEL

SYNC MASTER=K60 DAVID SYNC DATE=11/24/2010

PAGE TITLE
# AUDIO: Detects/Grounding

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

| FUNCTION | VOLUME/MUTE | CONVERTER | PIN COMPLEX | SHDN | DET ASSIGNMENT |
|---|---|---|---|---|---|
| HP/LINE OUT | 0X03 (3) | 0X03 (3) | 0X0A (10,D) | GPIO_2 | 0X0A (D) |
| PRIMARY SPKRS (WFR) | 0X04 (4) | 0X04 (4) | 0X0B (11) | GPIO_3 | N/A |
| SECONDARY SPKRS (TWT) | 0X02 (2) | 0X02 (2) | 0X09 (09) | GPIO_3 | N/A |
| SPDIF OUT | N/A | 0X08 (8) | 0x10 (16) | N/A | 0X0D (B) |

CODEC INPUT SIGNAL PATHS

| FUNCTION | CONVERTER | PIN COMPLEX | ENABLE/CONTROL | DET ASSIGNMENT |
|---|---|---|---|---|
| LINE IN | 0X05 (5) | 0X12 (12,C) | N/A | 0X12 (C) |
| SPDIF IN | 0X07 (7) | 0x0F (15) | N/A | N/A |
| INTERNAL MIC | 0X06 (6) | 0X0E (14,LEFT & RIGHT) | N/A | N/A |
| EXTERNAL MIC | 0X06 (6) | 0X0D (13,V22,B,LEFT) | COUGAR POINT GPIO 16 | COUGAR POINT GPIO 5 (RCVR INT)<br>COUGAR POINT GPIO 3 (PERIPH DET) |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| AUDIO | * | 0.1 MM | ? |
| SPKROUT | * | 0.2 MM | ? |

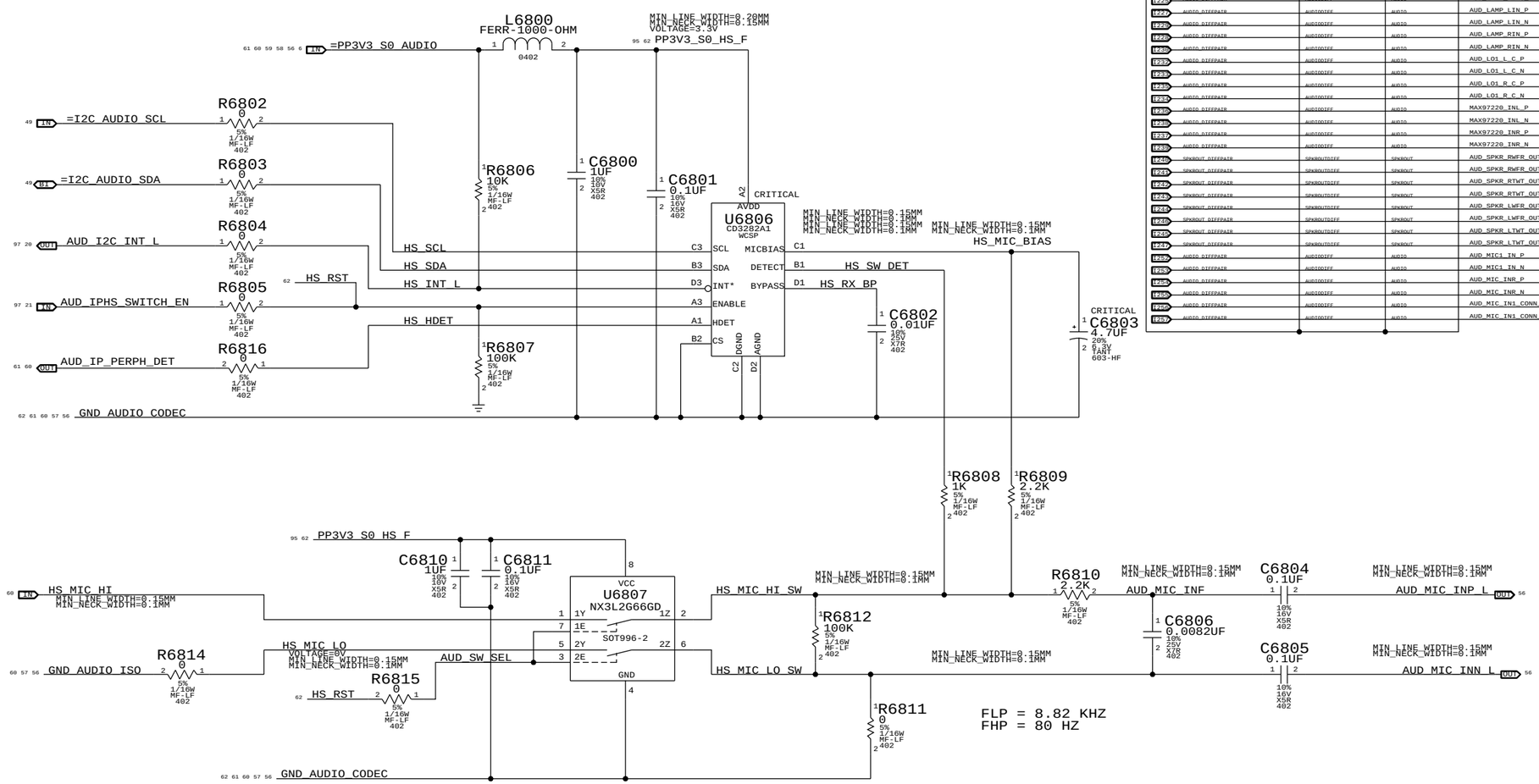
| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| AUDIODIFF | * | AUDIODIFF |
| SPKROUTDIFF | * | SPKROUTDIFF |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| AUDIODIFF | * | Y | 0.1 MM | 0.1 MM | 10 MM | 0.1 MM | 0.1 MM |
| SPKROUTDIFF | * | Y | 0.6 MM | 0.25 MM | 10 MM | 0.2 MM | 0.2 MM |

| | ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|---|
| IPD8 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HP_L_P | 56 59 |
| IPD9 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HP_L_N | 56 59 |
| IPD10 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HP_R_P | 56 58 |
| IPD11 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HP_R_N | 56 58 |
| IPD17 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_P | 56 57 |
| IPD18 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_N | 56 57 |
| IPD19 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_P | 56 57 |
| IPD20 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_N | 56 57 |
| IPD21 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_L_P | 56 59 |
| IPD22 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_L_N | 56 59 |
| IPD23 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_R_P | 56 58 |
| IPD24 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_R_N | 56 58 |
| IPD27 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LINC_P | 58 |
| IPD28 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LINC_N | 58 |
| IPD29 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RINC_P | 58 |
| IPD30 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RINC_N | 58 |
| IPD31 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LIN_P | 58 |
| IPD32 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LIN_N | 58 |
| IPD33 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RIN_P | 58 |
| IPD34 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RIN_N | 58 |
| IPD35 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LINC_P | 59 |
| IPD36 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LINC_N | 59 |
| IPD37 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RINC_P | 59 |
| IPD38 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RINC_N | 59 |
| IPD39 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LIN_P | 59 |
| IPD40 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LIN_N | 59 |
| IPD41 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RIN_P | 59 |
| IPD42 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RIN_N | 59 |
| IPD43 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_C_P | 57 |
| IPD44 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_C_N | 57 |
| IPD45 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_C_P | 57 |
| IPD46 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_C_N | 57 |
| IPD47 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX97220_INL_P | 57 |
| IPD48 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX97220_INL_N | 57 |
| IPD49 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX97220_INR_P | 57 |
| IPD50 | AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX97220_INR_N | 57 |
| IPD51 | SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RWFR_OUT_P | 58 60 |
| IPD52 | SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RWFR_OUT_N | 58 60 |
| IPD53 | SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RTWT_OUT_P | 58 60 |
| IPD54 | SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RTWT_OUT_N | 58 60 |
| IPD55 | SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LWFR_OUT_P | 59 60 |
| IPD56 | SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LWFR_OUT_N | 59 60 |
| IPD57 | SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LTWT_OUT_P | 59 60 |
| IPD58 | SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LTWT_OUT_N | 59 60 |
| IPD59 | AUDIODIFF_DIFFPAIR | AUDIODIFF | AUDIO | AUD_MIC1_IN_P | 60 61 |
| IPD60 | AUDIODIFF_DIFFPAIR | AUDIODIFF | AUDIO | AUD_MIC1_IN_N | 60 61 |
| IPD61 | AUDIODIFF_DIFFPAIR | AUDIODIFF | AUDIO | AUD_MIC_INR_P | 56 61 |
| IPD62 | AUDIODIFF_DIFFPAIR | AUDIODIFF | AUDIO | AUD_MIC_INR_N | 56 61 |
| IPD63 | AUDIODIFF_DIFFPAIR | AUDIODIFF | AUDIO | AUD_MIC_IN1_CONN_P | 60 |
| IPD64 | AUDIODIFF_DIFFPAIR | AUDIODIFF | AUDIO | AUD_MIC_IN1_CONN_N | 60 |

# MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640




SYNC_MASTER=K60_DAVID SYNC_DATE=01/06/2011

PAGE TITLE

AUDIO: Mikey

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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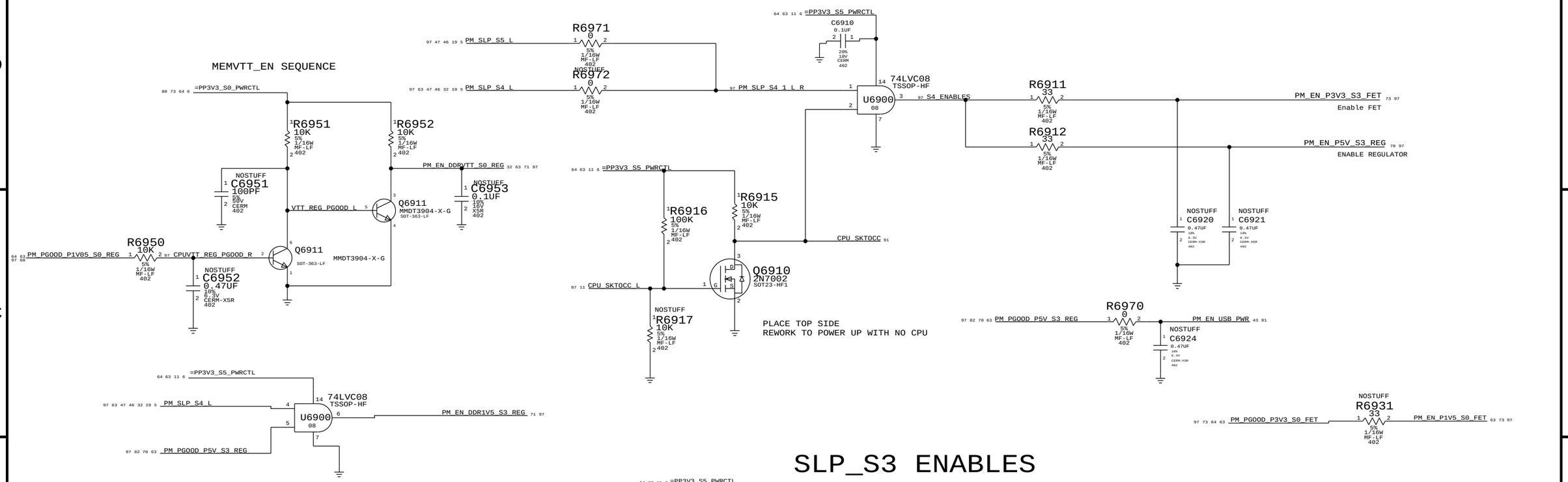
# SLP_S4 ENABLES

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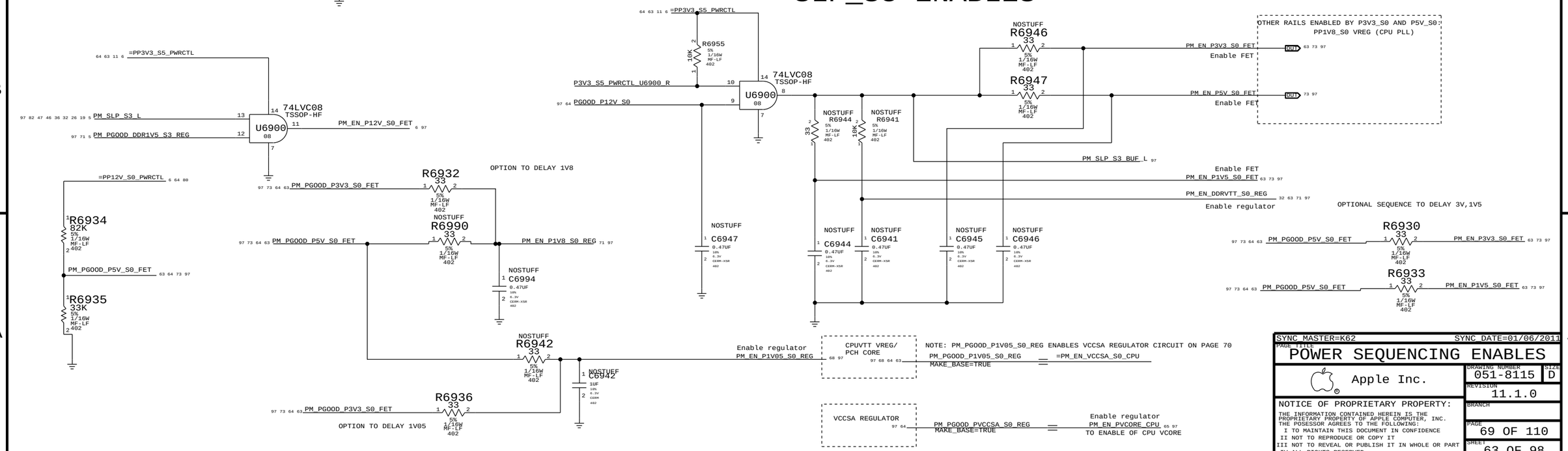


SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

# POWER SEQUENCING ENABLES

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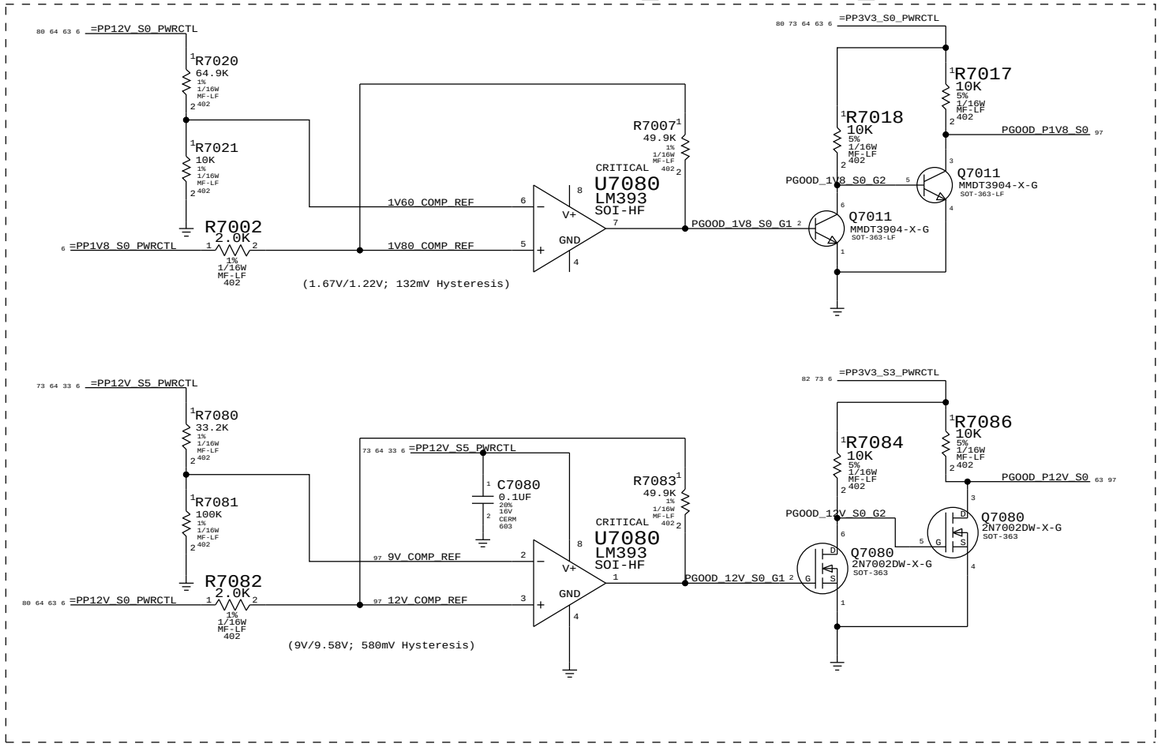
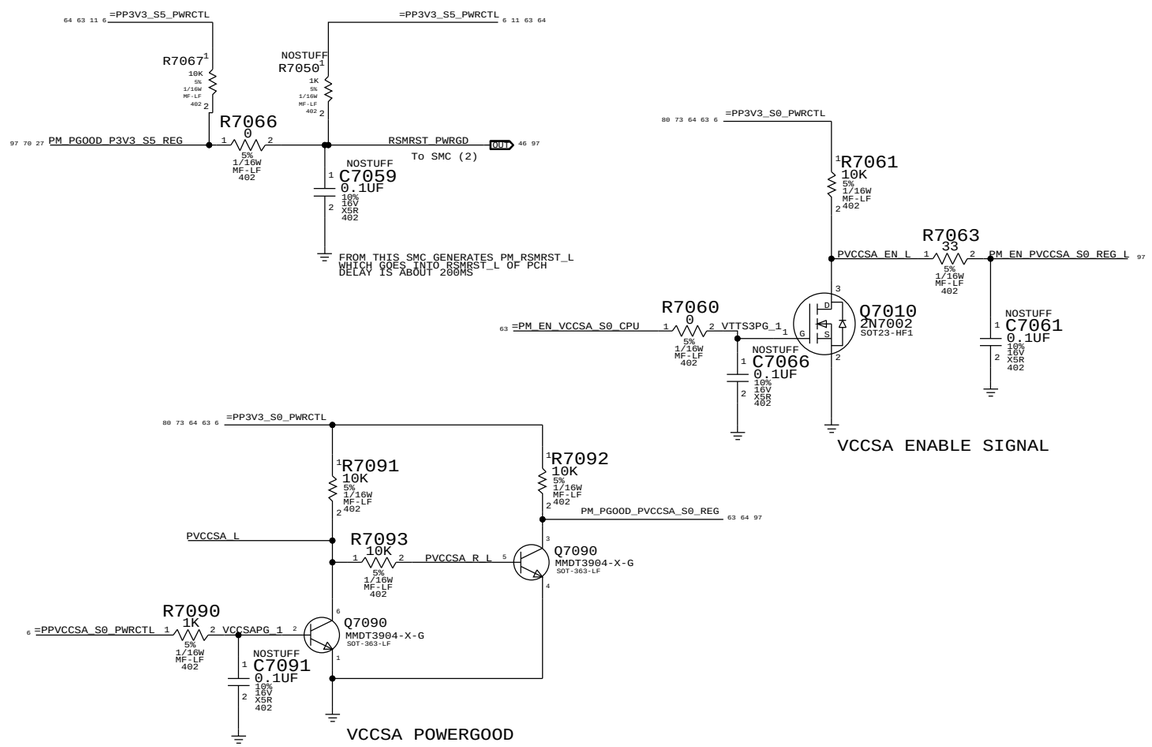
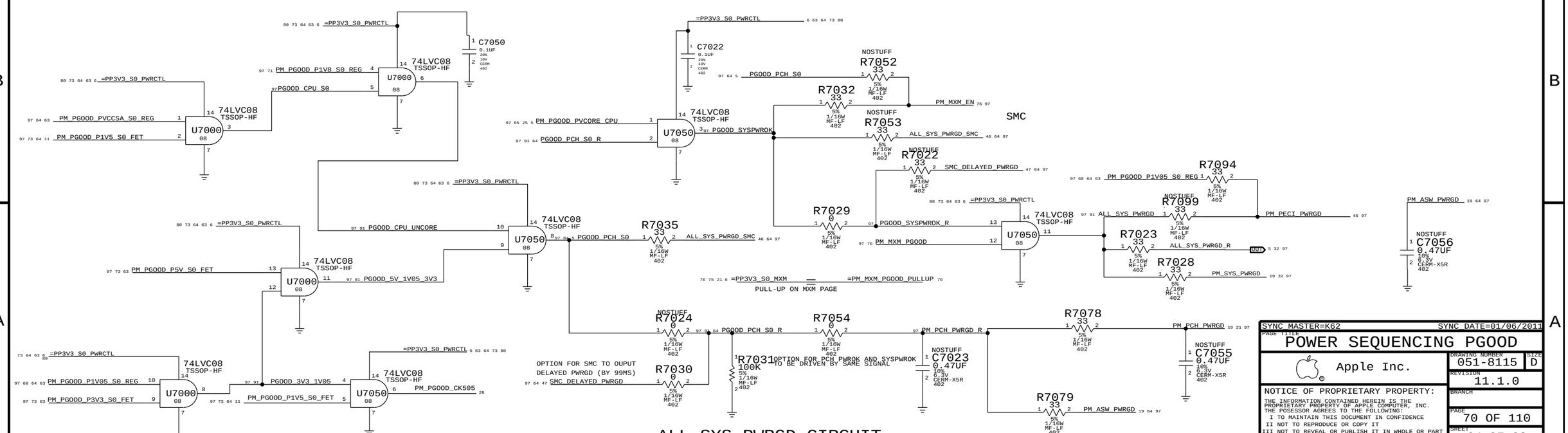
# PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0




S0 RAILS PGOOD




ALL_SYS_PWRGD CIRCUIT

| | |
|---|---|
| SYNC_MASTER=K62 | SYNC_DATE=01/06/2011 |
| PAGE TITLE | POWER SEQUENCING PGOOD |
| Apple Inc. | DRAWING NUMBER 051-8115 |
| | SIZE D |
| | REVISION 11.1.0 |
| | BRANCH |
| | PAGE 70 OF 110 |
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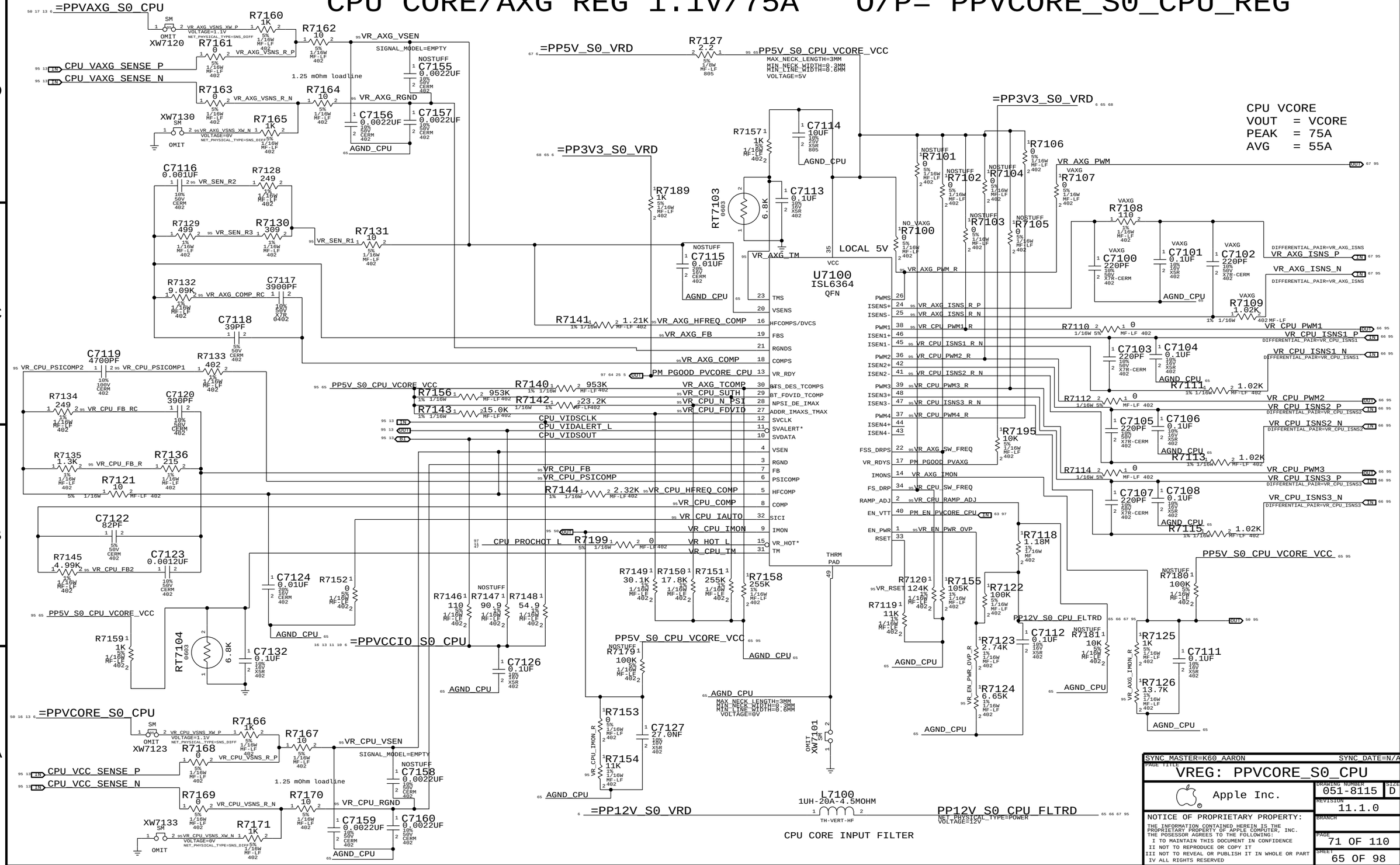
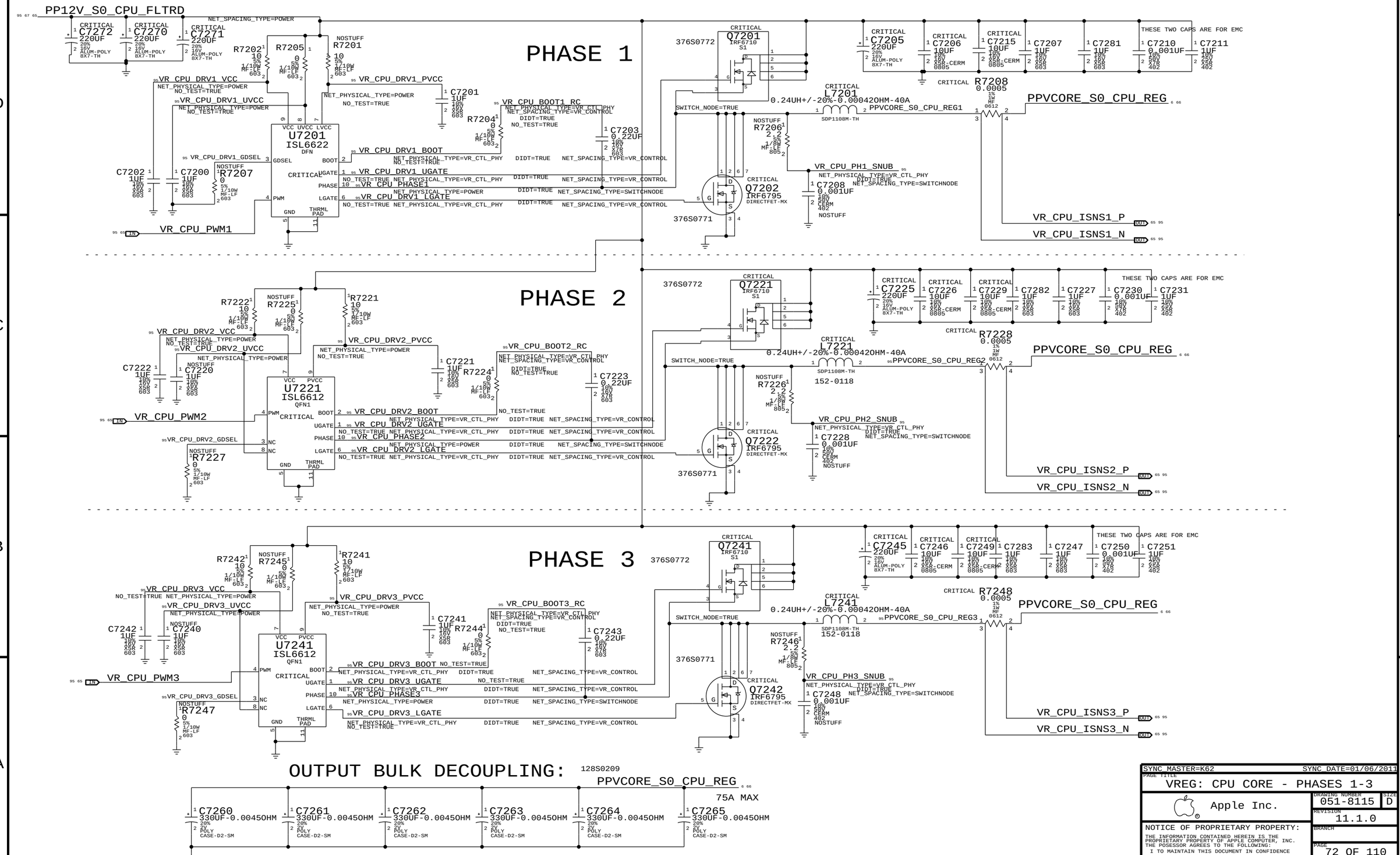
# CPU CORE/AXG REG 1.1V/75A O/P= PPVCORE_S0_CPU_REG






SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
VREG: CPU CORE - PHASES 1-3

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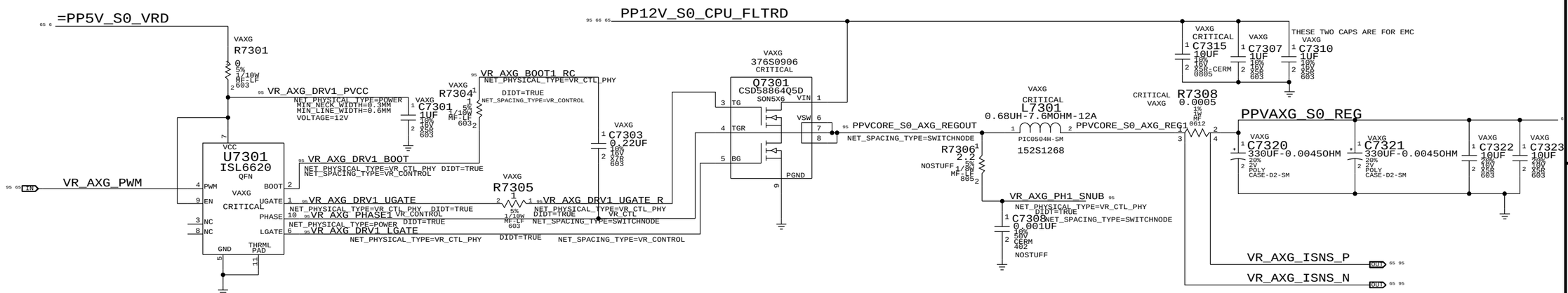
# AXG PHASE (MAX 15A)




SYNC_MASTER=K60_AARON SYNC_DATE=N/A

PAGE TITLE
VREG:AXG PHASE/CORE - CAPS

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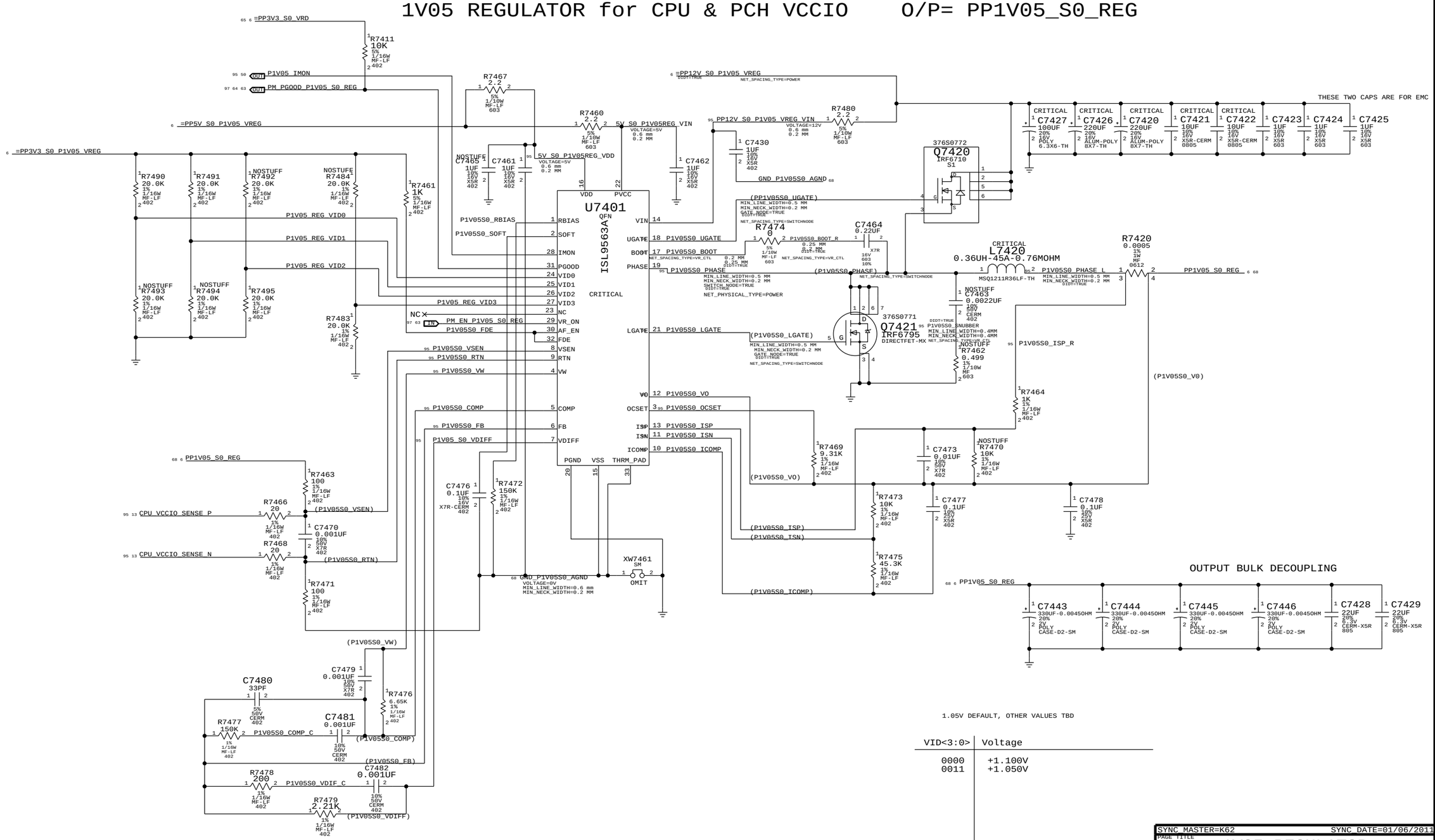
# 1V05 REGULATOR for CPU & PCH VCCIO  O/P= PP1V05_S0_REG




1.05V DEFAULT, OTHER VALUES TBD

| VID<3:0> | Voltage |
|---|---|
| 0000 | +1.100V |
| 0011 | +1.050V |

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: 1V05 REGULATOR

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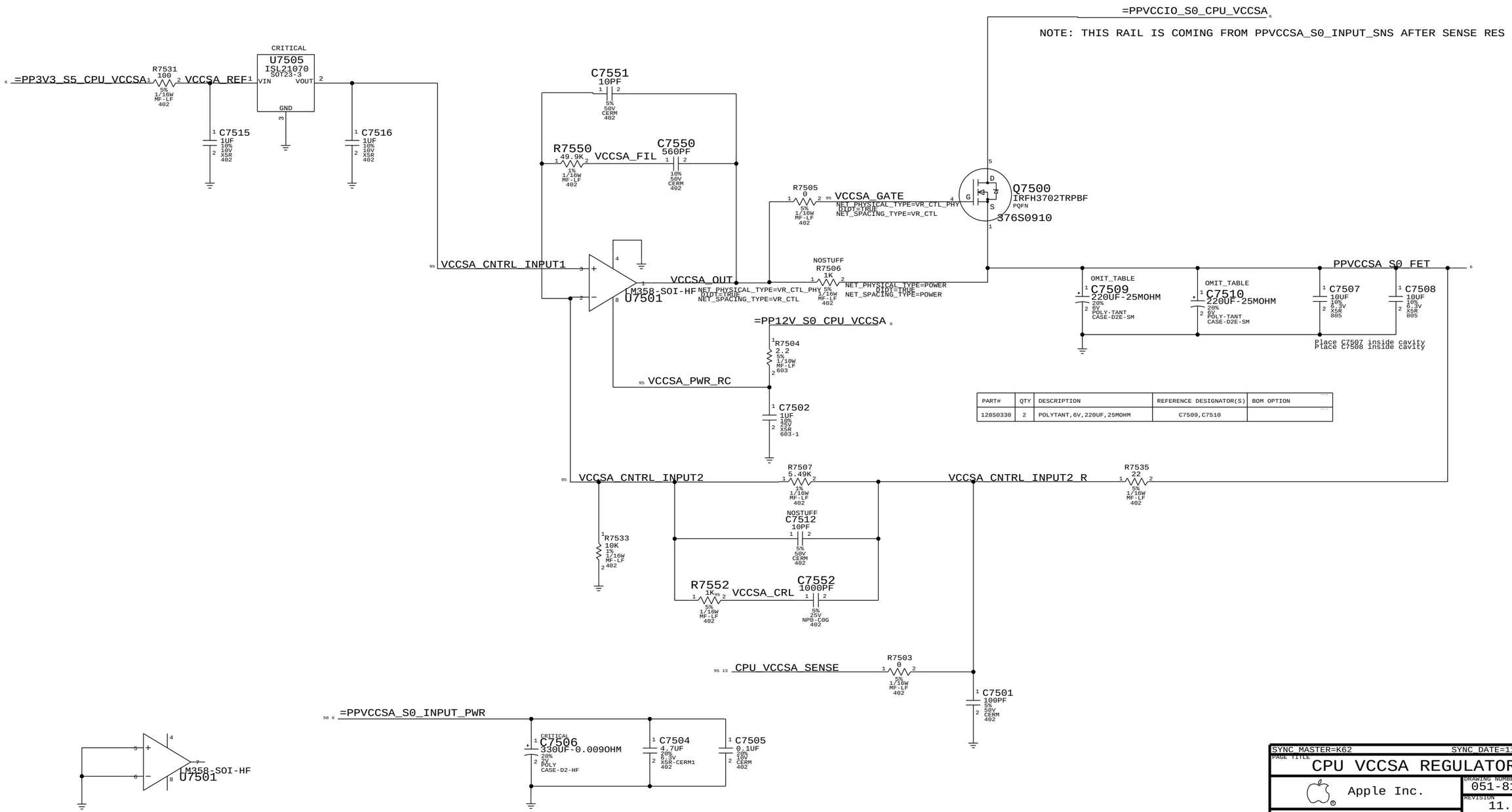
# CPU VCCSA 0.925V (8.8A MAX)




| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 128S0330 | 2 | POLYTANT,6V,220UF,25MOHM | C7509,C7510 | |

SYNC MASTER=K62 SYNC DATE=11/15/2010

PAGE TITLE
CPU VCCSA REGULATOR

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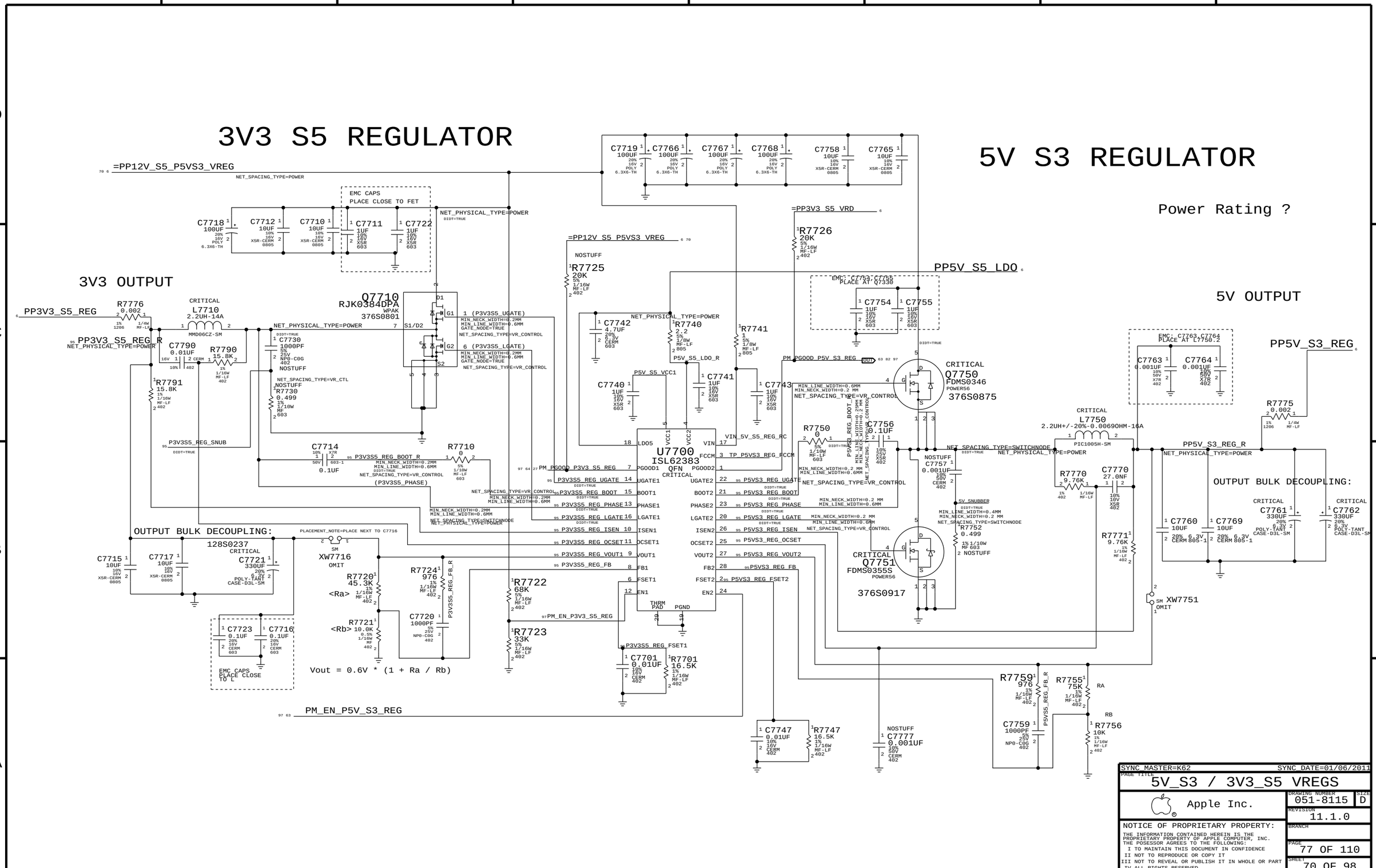


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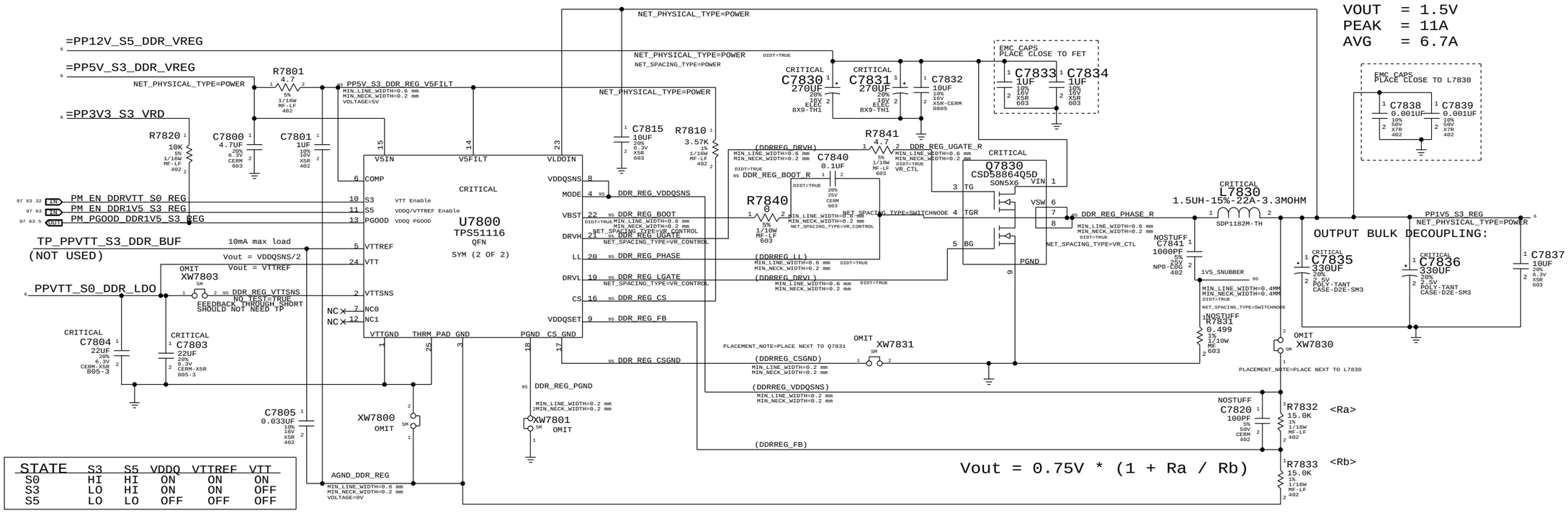
# 1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11A
AVG = 6.7A



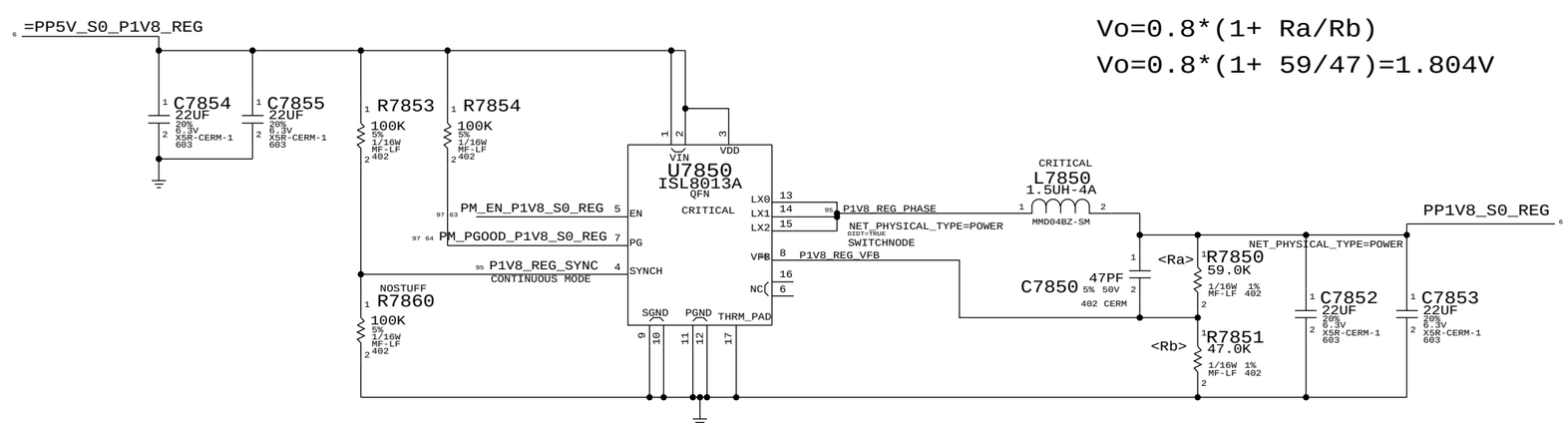

| STATE | S3 | S5 | VDDQ | VTTREF | VTT |
|---|---|---|---|---|---|
| S0 | HI | HI | ON | ON | ON |
| S3 | LO | HI | ON | ON | OFF |
| S5 | LO | LO | OFF | OFF | OFF |

Vout = 0.75V * (1 + Ra / Rb)

# 1.8 V SUPPLY

## 1A Average current

Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V




SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE: 1.5V / 1.8V VREGS

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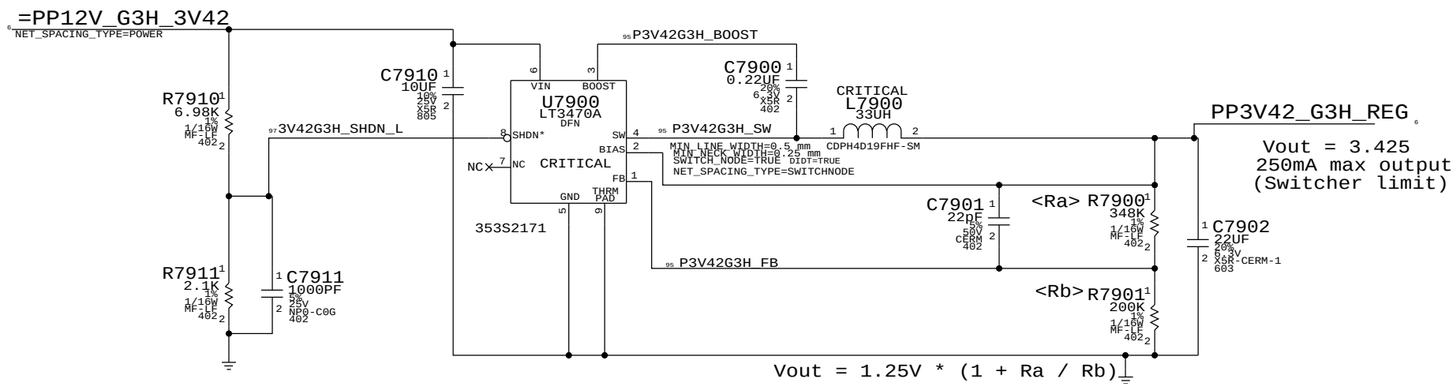
# 3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator




SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
3.42 G3HOT SUPPLY

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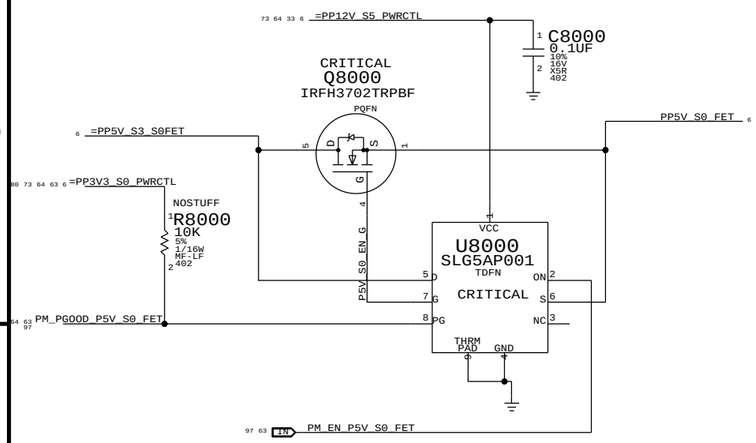
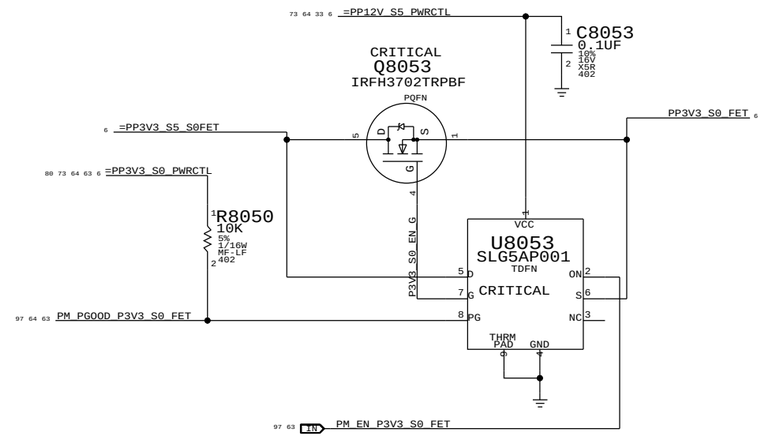
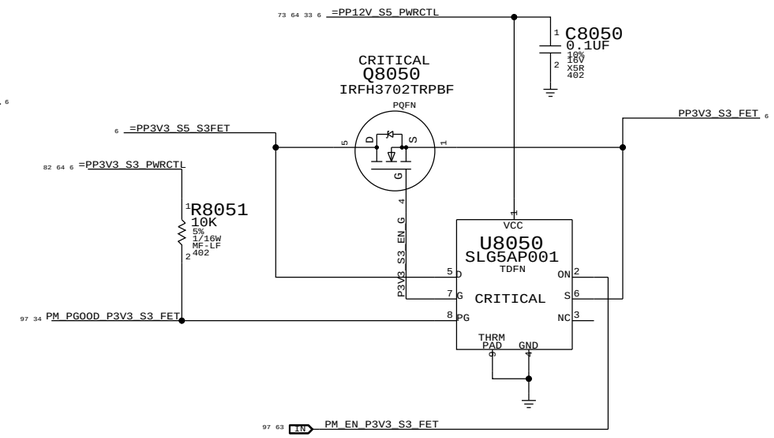
## 5V S0 FET (6.6A PK/3.1A AVG)



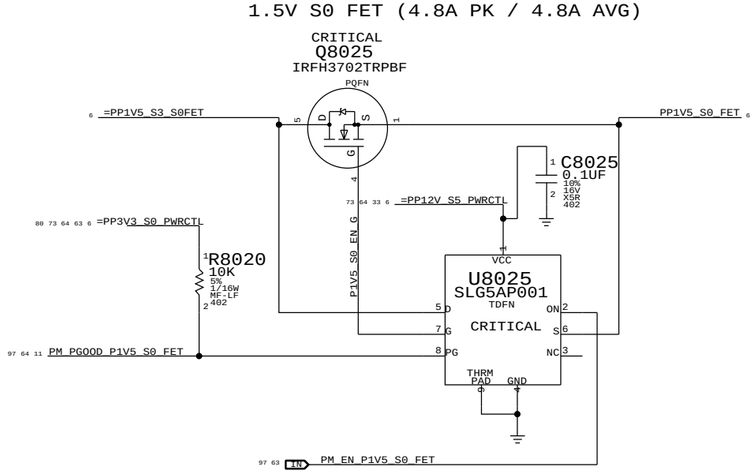

## 3.3V S0 FET (2.9APK / 2.0A AVG)




## 3.3V S3 FET (3.4A PK / 1.6A AVG)




## 1.5V S0 FET (4.8A PK / 4.8A AVG)




SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE

# S3+S0 FETS

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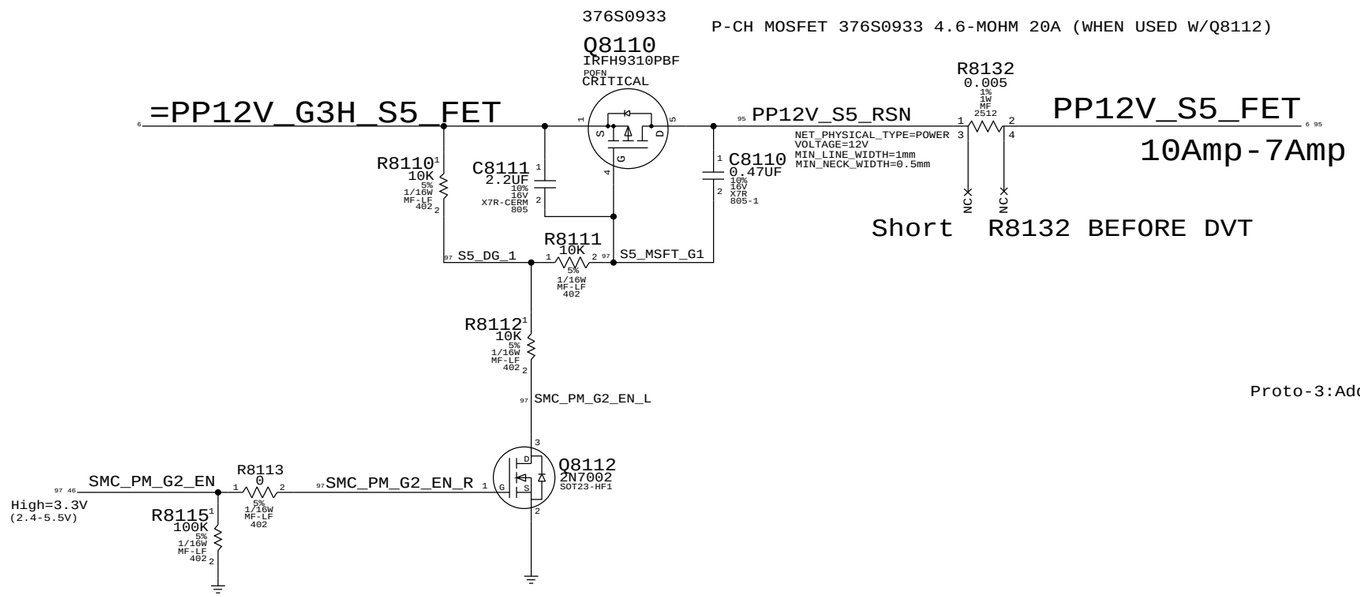


SYNC_MASTER=K60_JERRY SYNC_DATE=01/06/2011

PAGE TITLE
12V_S0 & 12V_S5 switch

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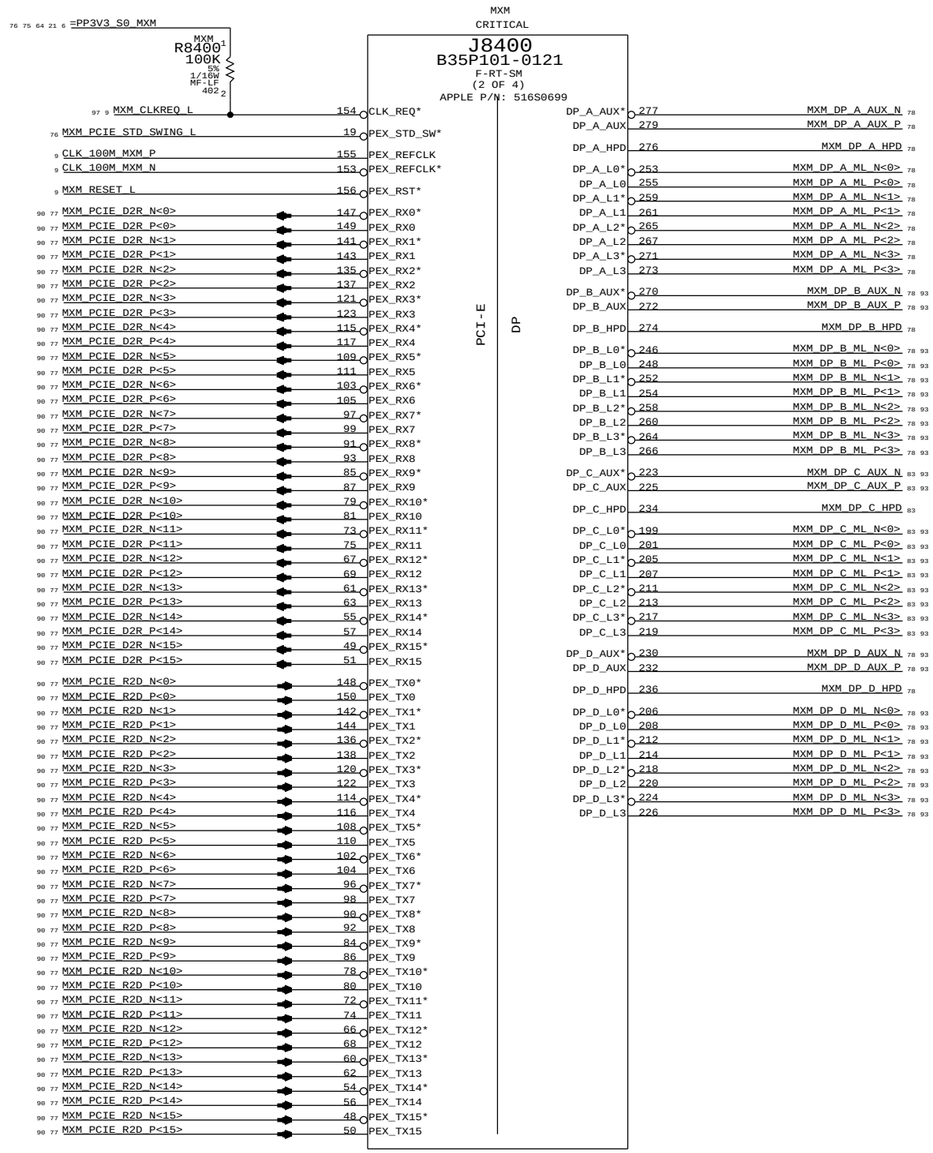
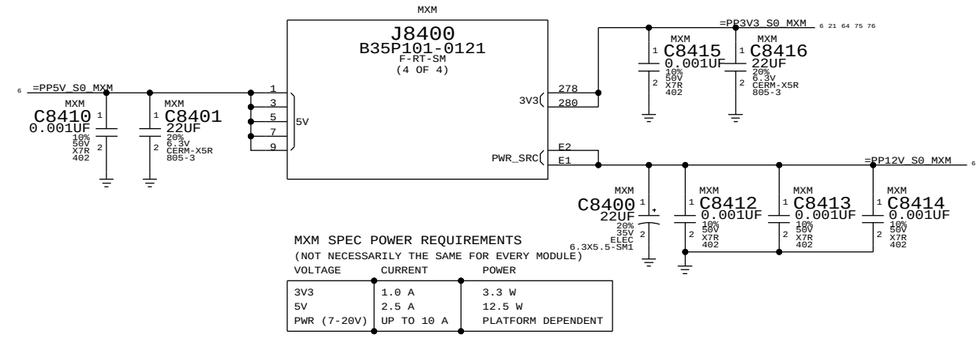
# Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM




MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

| VOLTAGE | CURRENT | POWER |
|---|---|---|
| 3V3 | 1.0 A | 3.3 W |
| 5V | 2.5 A | 12.5 W |
| PWR (7-20V) | UP TO 10 A | PLATFORM DEPENDENT |

## MXM DP PORT ROUTING

| | K62 | K60 |
|---|---|---|
| DP A | EXT DP1 | EXT DP1 |
| DP B | T29 DP2 | T29 DP2 |
| DP C | INT DP | INT DP |
| DP D | T29 DP1 | T29 DP1 |
| DP E | EXT DP2 | |

SYNC MASTER=K62 SYNC DATE=01/06/2011

PAGE TITLE
MXM PCIe, DP & Power

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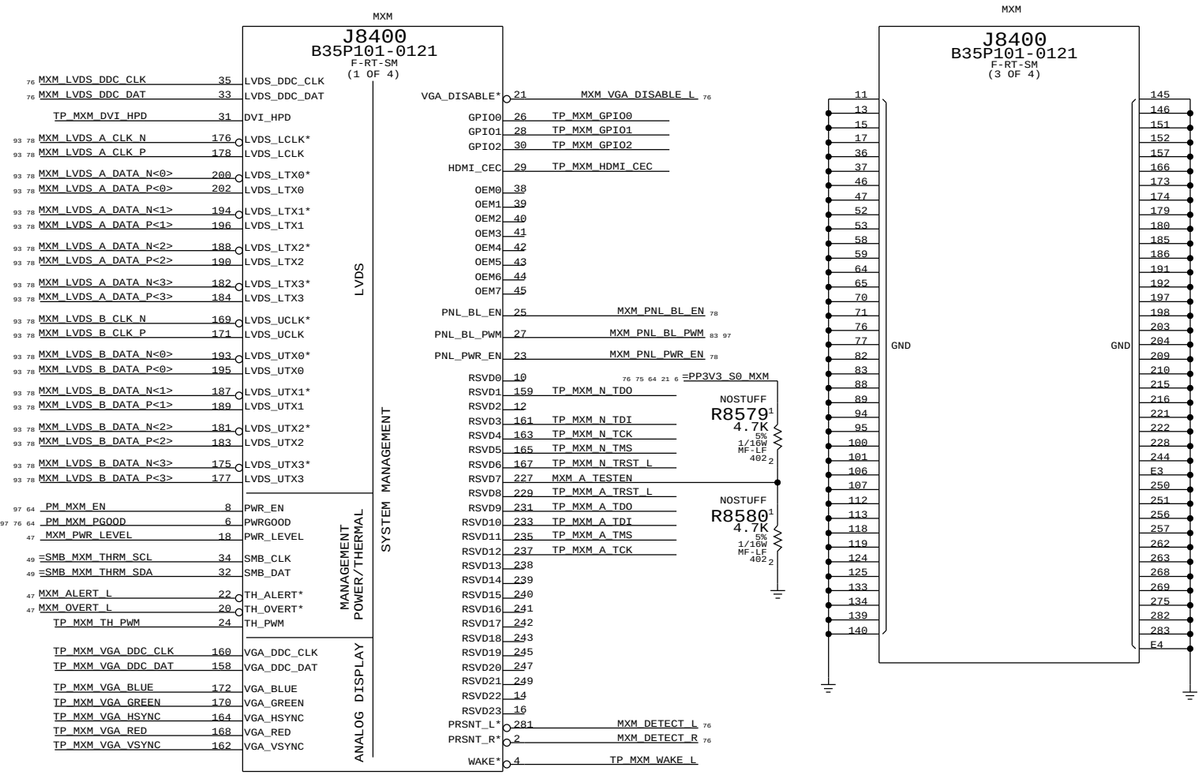
# Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM

Signal aliases required by this page:
- =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

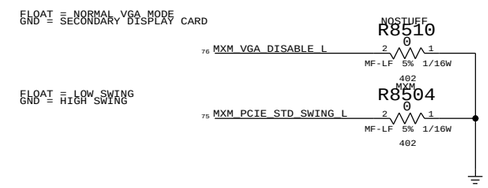
BOM options provided by this page:

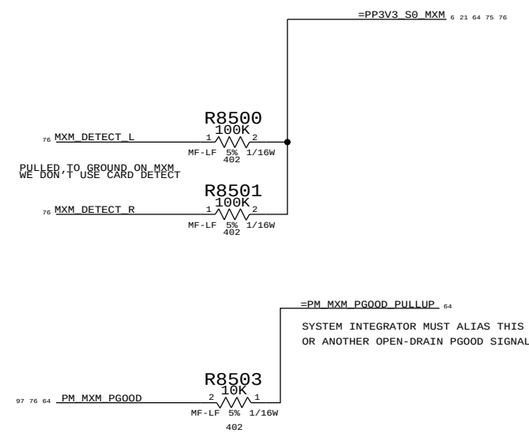
## PULLUPS & PULLDOWNS AT MXM CONNECTOR





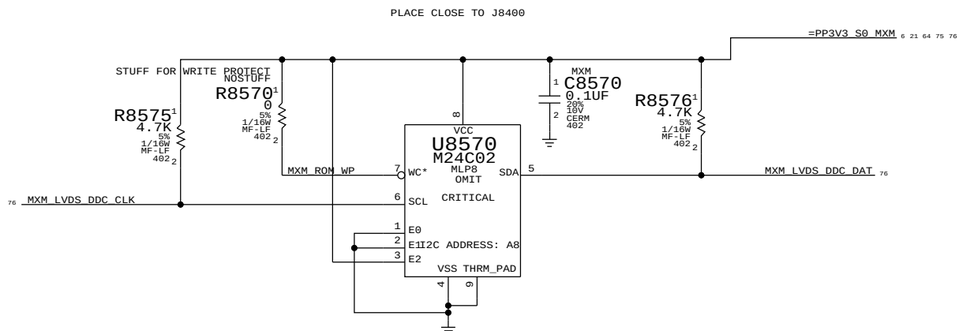





## MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400




| | |
|---|---|
| SYNC_MASTER=K60_MASTER | SYNC_DATE=N/A |
| PAGE TITLE: MXM I/O | |
| Apple Inc. | DRAWING NUMBER: 051-8115 SIZE: D |
| | REVISION: 11.1.0 |
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| | PAGE: 85 OF 110 |
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# MXM TX CAPS

| | | | | | |
|---|---|---|---|---|---|
| PEG_R2D_C_P<0> | MXM C8600 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<15> | |
| PEG_R2D_C_N<0> | MXM C8601 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<15> | |
| PEG_R2D_C_N<1> | MXM C8602 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<14> | |
| PEG_R2D_C_P<1> | MXM C8603 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<14> | |
| PEG_R2D_C_N<2> | MXM C8604 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<13> | |
| PEG_R2D_C_P<2> | MXM C8605 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<13> | |
| PEG_R2D_C_P<3> | MXM C8606 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<12> | |
| PEG_R2D_C_N<3> | MXM C8607 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<12> | |
| PEG_R2D_C_N<4> | MXM C8608 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<11> | |
| PEG_R2D_C_P<4> | MXM C8609 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<11> | |
| PEG_R2D_C_N<5> | MXM C8610 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<10> | |
| PEG_R2D_C_P<5> | MXM C8611 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<10> | |
| PEG_R2D_C_P<6> | MXM C8612 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<9> | |
| PEG_R2D_C_N<6> | MXM C8613 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<9> | |
| PEG_R2D_C_N<7> | MXM C8614 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<8> | |
| PEG_R2D_C_P<7> | MXM C8615 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<8> | |
| PEG_R2D_C_P<8> | MXM C8616 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<7> | |
| PEG_R2D_C_N<8> | MXM C8617 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<7> | |
| PEG_R2D_C_P<9> | MXM C8618 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<6> | |
| PEG_R2D_C_N<9> | MXM C8619 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<6> | |
| PEG_R2D_C_N<10> | MXM C8620 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<5> | |
| PEG_R2D_C_P<10> | MXM C8621 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<5> | |
| PEG_R2D_C_N<11> | MXM C8622 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<4> | |
| PEG_R2D_C_P<11> | MXM C8623 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<4> | |
| PEG_R2D_C_P<12> | MXM C8624 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<3> | |
| PEG_R2D_C_N<12> | MXM C8625 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<3> | |
| PEG_R2D_C_N<13> | MXM C8626 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<2> | |
| PEG_R2D_C_P<13> | MXM C8627 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<2> | |
| PEG_R2D_C_P<14> | MXM C8628 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<1> | |
| PEG_R2D_C_N<14> | MXM C8629 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<1> | |
| PEG_R2D_C_N<15> | MXM C8630 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_P<0> | |
| PEG_R2D_C_P<15> | MXM C8631 | 0.1UF | 2 10% 16V X5R 402 | MXM_PCIE_R2D_N<0> | |

# MXM RX CAPS

| | | | | | |
|---|---|---|---|---|---|
| MXM_PCIE_D2R_P<15> | MXM C8632 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<0> | |
| MXM_PCIE_D2R_N<15> | MXM C8633 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<0> | |
| MXM_PCIE_D2R_P<14> | MXM C8634 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<1> | |
| MXM_PCIE_D2R_N<14> | MXM C8635 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<1> | |
| MXM_PCIE_D2R_P<13> | MXM C8636 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<2> | |
| MXM_PCIE_D2R_N<13> | MXM C8637 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<2> | |
| MXM_PCIE_D2R_P<12> | MXM C8638 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<3> | |
| MXM_PCIE_D2R_N<12> | MXM C8639 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<3> | |
| MXM_PCIE_D2R_P<11> | MXM C8640 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<4> | |
| MXM_PCIE_D2R_N<11> | MXM C8641 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<4> | |
| MXM_PCIE_D2R_P<10> | MXM C8642 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<5> | |
| MXM_PCIE_D2R_N<10> | MXM C8643 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<5> | |
| MXM_PCIE_D2R_P<9> | MXM C8644 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<6> | |
| MXM_PCIE_D2R_N<9> | MXM C8645 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<6> | |
| MXM_PCIE_D2R_P<8> | MXM C8646 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<7> | |
| MXM_PCIE_D2R_N<8> | MXM C8647 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<7> | |
| MXM_PCIE_D2R_P<7> | MXM C8648 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<8> | |
| MXM_PCIE_D2R_N<7> | MXM C8649 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<8> | |
| MXM_PCIE_D2R_P<6> | MXM C8650 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<9> | |
| MXM_PCIE_D2R_N<6> | MXM C8651 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<9> | |
| MXM_PCIE_D2R_P<5> | MXM C8652 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<10> | |
| MXM_PCIE_D2R_N<5> | MXM C8653 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<10> | |
| MXM_PCIE_D2R_P<4> | MXM C8654 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<11> | |
| MXM_PCIE_D2R_N<4> | MXM C8655 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<11> | |
| MXM_PCIE_D2R_P<3> | MXM C8656 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<12> | |
| MXM_PCIE_D2R_N<3> | MXM C8657 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<12> | |
| MXM_PCIE_D2R_P<2> | MXM C8658 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<13> | |
| MXM_PCIE_D2R_N<2> | MXM C8659 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<13> | |
| MXM_PCIE_D2R_P<1> | MXM C8662 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<14> | |
| MXM_PCIE_D2R_N<1> | MXM C8663 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<14> | |
| MXM_PCIE_D2R_P<0> | MXM C8660 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_N<15> | |
| MXM_PCIE_D2R_N<0> | MXM C8661 | 0.1UF | 2 10% 16V X5R 402 | PEG_D2R_P<15> | |

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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# Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

## MXM ALIAS

| | | | | |
|---|---|---|---|---|
| 75 | MXM_DP_A_ML_P<0..3> | DP_EXTA_ML_C_P<0..3> | MAKE_BASE=TRUE NO_TEST=TRUE | 84 93 |
| 75 | MXM_DP_A_ML_N<0..3> | DP_EXTA_ML_C_N<0..3> | MAKE_BASE=TRUE NO_TEST=TRUE | 84 93 |
| 75 | MXM_DP_A_AUX_P | DP_EXTA_AUXCH_C_P | MAKE_BASE=TRUE NO_TEST=TRUE | 78 84 93 |
| 75 | MXM_DP_A_AUX_N | DP_EXTA_AUXCH_C_N | MAKE_BASE=TRUE NO_TEST=TRUE | 78 84 93 |
| 75 | MXM_DP_A_HPD | DP_EXTA_HPD | MAKE_BASE=TRUE NO_TEST=TRUE | 84 |

## T29 CONN POWER CONTROL ALIAS

| | | | |
|---|---|---|---|
| 95 84 | PP3V3_SW_DPAPWR | =PP3V3_SW_DPAPWR | 6 |
| 97 36 33 19 | PCIE_WAKE_L | =T29_WAKE_L | 84 |

## Unused MXM Interfaces

| | | | |
|---|---|---|---|
| 93 76 | MXM_LVDS_A_CLK_N | NC_MXM_LVDS_A_CLK_N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 93 76 | MXM_LVDS_A_CLK_P | NC_MXM_LVDS_A_CLK_P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 93 76 | MXM_LVDS_A_DATA_N<3..0> | NC_MXM_LVDS_A_DATA_N<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 93 76 | MXM_LVDS_A_DATA_P<3..0> | NC_MXM_LVDS_A_DATA_P<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 93 76 | MXM_LVDS_B_CLK_N | NC_MXM_LVDS_B_CLK_N | MAKE_BASE=TRUE NO_TEST=TRUE |
| 93 76 | MXM_LVDS_B_CLK_P | NC_MXM_LVDS_B_CLK_P | MAKE_BASE=TRUE NO_TEST=TRUE |
| 93 76 | MXM_LVDS_B_DATA_N<3..0> | NC_MXM_LVDS_B_DATA_N<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 93 76 | MXM_LVDS_B_DATA_P<3..0> | NC_MXM_LVDS_B_DATA_P<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |

## T29 MXM DP ALIAS

| | | | | |
|---|---|---|---|---|
| 93 75 | MXM_DP_D_ML_P<0..3> | DP_T29SNK0_ML_C_P<0..3> | MAKE_BASE=TRUE NO_TEST=TRUE | 86 96 |
| 93 75 | MXM_DP_D_ML_N<0..3> | DP_T29SNK0_ML_C_N<0..3> | MAKE_BASE=TRUE NO_TEST=TRUE | 86 96 |
| 93 75 | MXM_DP_D_AUX_P | DP_T29SNK0_AUXCH_C_P | MAKE_BASE=TRUE NO_TEST=TRUE | 86 96 |
| 93 75 | MXM_DP_D_AUX_N | DP_T29SNK0_AUXCH_C_N | MAKE_BASE=TRUE NO_TEST=TRUE | 86 96 |
| 75 | MXM_DP_D_HPD | DP_T29SNK0_HPD | MAKE_BASE=TRUE NO_TEST=TRUE | 86 |
| 93 75 | MXM_DP_B_ML_P<0..3> | DP_T29SNK1_ML_C_P<0..3> | MAKE_BASE=TRUE NO_TEST=TRUE | 86 96 |
| 93 75 | MXM_DP_B_ML_N<0..3> | DP_T29SNK1_ML_C_N<0..3> | MAKE_BASE=TRUE NO_TEST=TRUE | 86 96 |
| 93 75 | MXM_DP_B_AUX_P | DP_T29SNK1_AUXCH_C_P | MAKE_BASE=TRUE NO_TEST=TRUE | 86 96 |
| 93 75 | MXM_DP_B_AUX_N | DP_T29SNK1_AUXCH_C_N | MAKE_BASE=TRUE NO_TEST=TRUE | 86 96 |
| 75 | MXM_DP_B_HPD | DP_T29SNK1_HPD | MAKE_BASE=TRUE NO_TEST=TRUE | 86 |

## Unused T29 Interfaces

| | | | | | |
|---|---|---|---|---|---|
| 96 86 | T29_D2R_N<2..3> | NC_T29_D2R_N<2..3> | MAKE_BASE=TRUE NO_TEST=TRUE | | |
| 96 86 | T29_D2R_P<2..3> | NC_T29_D2R_P<2..3> | MAKE_BASE=TRUE NO_TEST=TRUE | | |
| 96 86 | T29_R2D_C_N<2..3> | NC_T29_R2D_C_N<2..3> | MAKE_BASE=TRUE NO_TEST=TRUE | | |
| 96 86 | T29_R2D_C_P<2..3> | NC_T29_R2D_C_P<2..3> | MAKE_BASE=TRUE NO_TEST=TRUE | | |
| 86 | T29_LSEO<3> | T29_LSEO_LSOE3 | MAKE_BASE=TRUE NO_TEST=TRUE | T29_LSOE<3> | 86 |
| 86 | T29_LSEO<2> | T29_LSEO_LSEO2 | MAKE_BASE=TRUE NO_TEST=TRUE | T29_LSOE<2> | 86 |

## UNUSED MXM CONTROL SIGNALS

| | | | |
|---|---|---|---|
| 76 | MXM_PNL_BL_EN | NC_MXM_PNL_BL_EN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 76 | MXM_PNL_PWR_EN | NC_MXM_PNL_PWR_EN | MAKE_BASE=TRUE NO_TEST=TRUE |

## DDC/AUX ALIAS

| | | | | |
|---|---|---|---|---|
| 93 84 78 | DP_EXTA_AUXCH_C_P | DP_EXTA_DDC_CLK | MAKE_BASE=TRUE | 84 |
| 93 84 78 | DP_EXTA_AUXCH_C_N | DP_EXTA_DDC_DATA | MAKE_BASE=TRUE | 84 |

SYNC_MASTER=K60_AARON SYNC_DATE=07/18/2010

PAGE TITLE
DP ALIAS AND CONTROL

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

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# System RTC Power Source & 32kHz / 25MHz Clock Generator

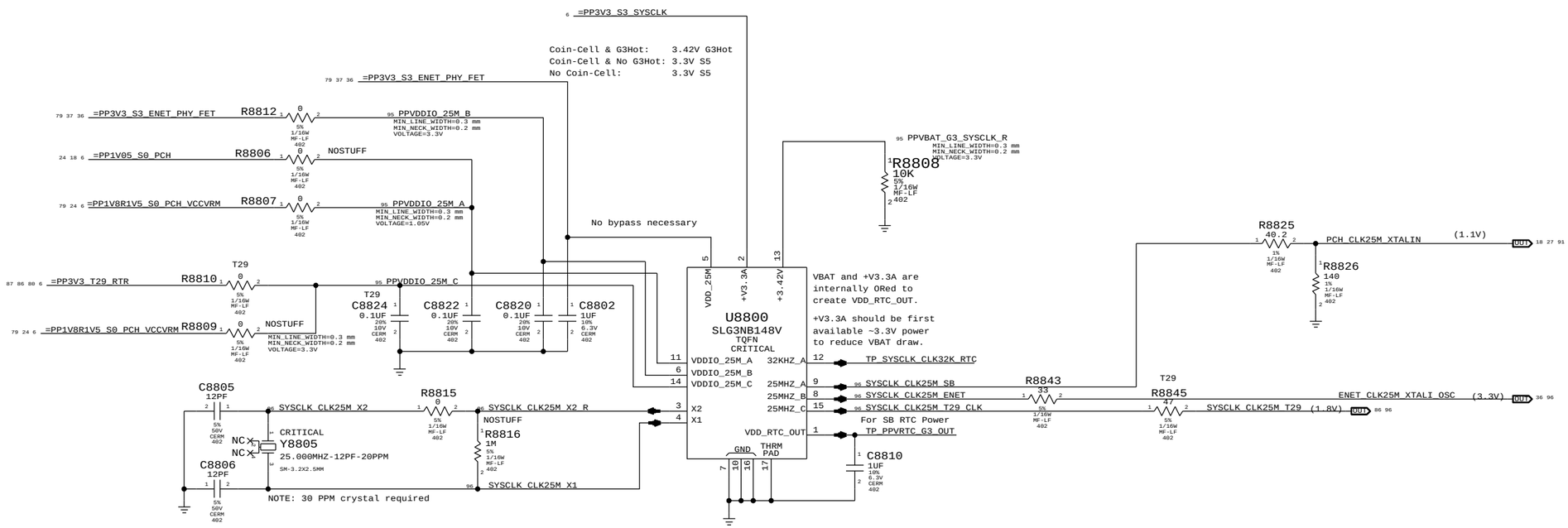
## GreenCLK Implementation Notes:

VBAT: Alias as appropriate (see note below & Desktop Example)
+V3.3A: Alias as appropriate (see note below)
VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000
For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000
For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary

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|---|---|
| SYNC MASTER=K62 | SYNC DATE=01/06/2013 |
| PAGE TITLE: GREEN CLOCK | |
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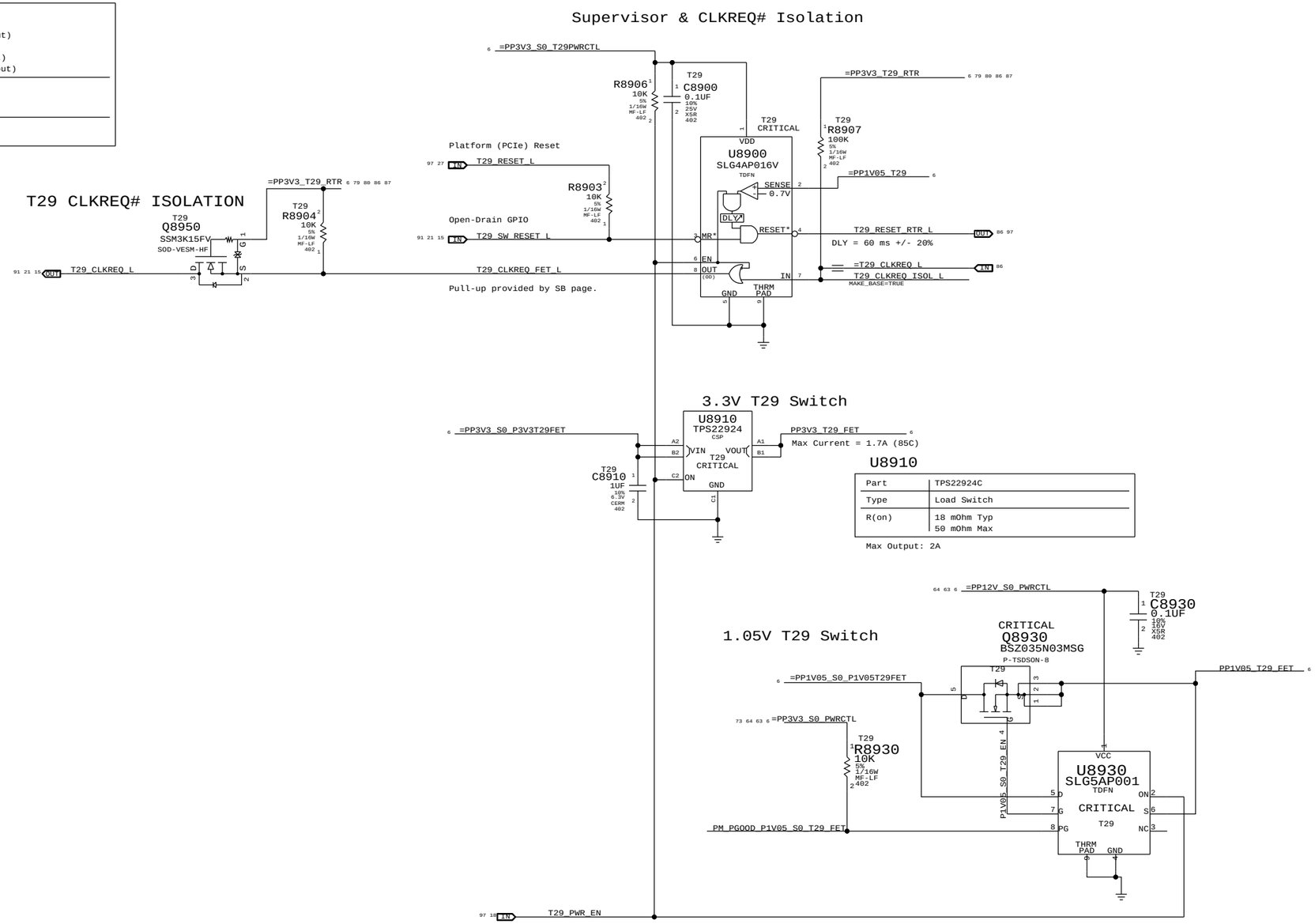
# Page Notes

Power aliases required by this page:
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:
- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:
(NONE)




| | |
|---|---|
| SYNC_MASTER=K62 | SYNC_DATE=01/06/2011 |
| PAGE TITLE | T29 POWER |
| Apple Inc. | DRAWING NUMBER 051-8115 SIZE D |
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## Page Notes

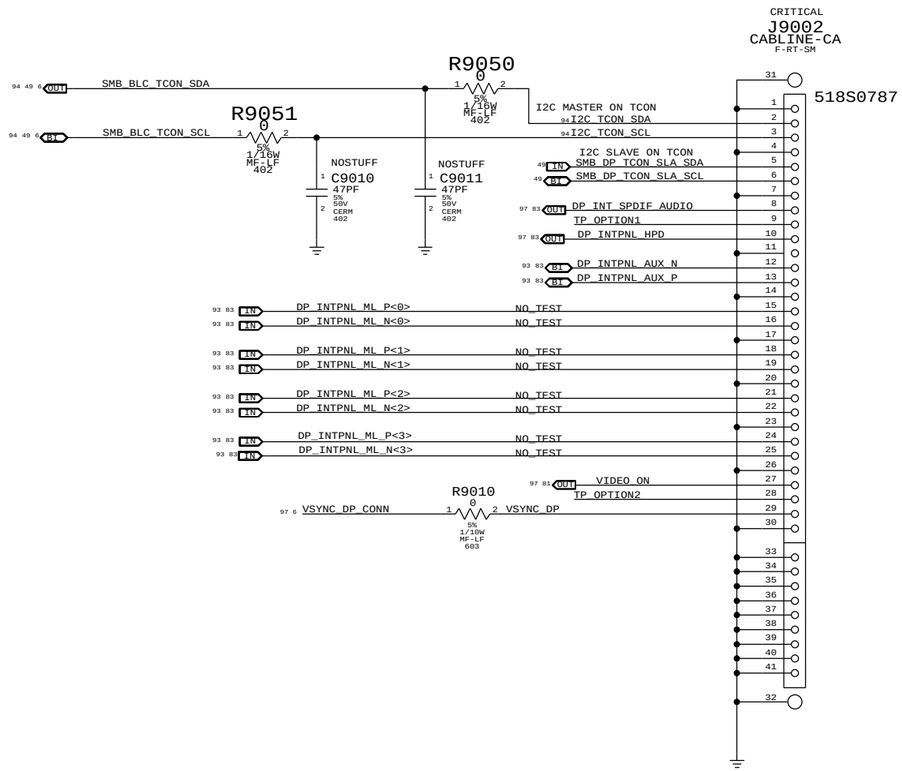
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

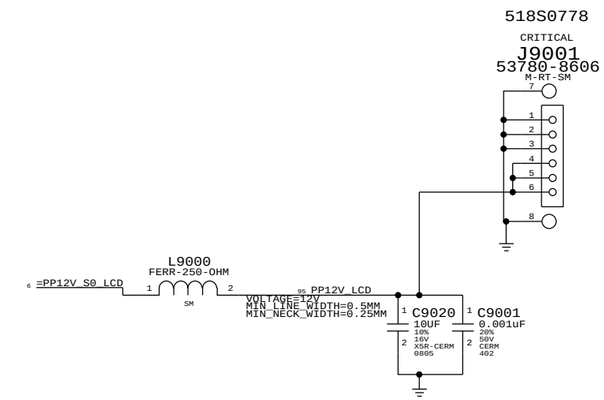
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

## INTERNAL DP INTERFACE

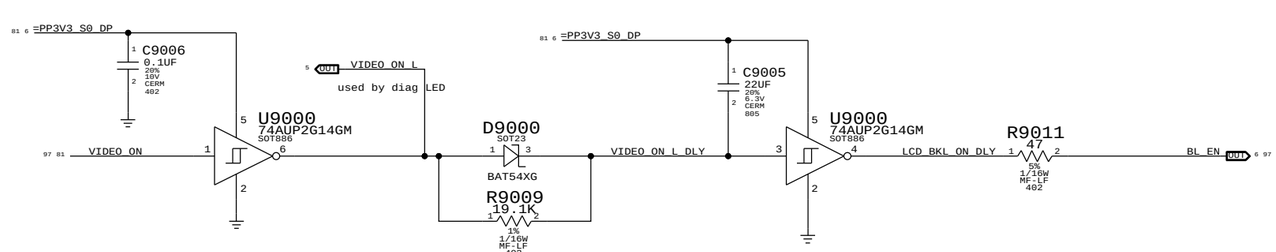



## INTERNAL DP POWER




## BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video




SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
# Display: Int DP Connector

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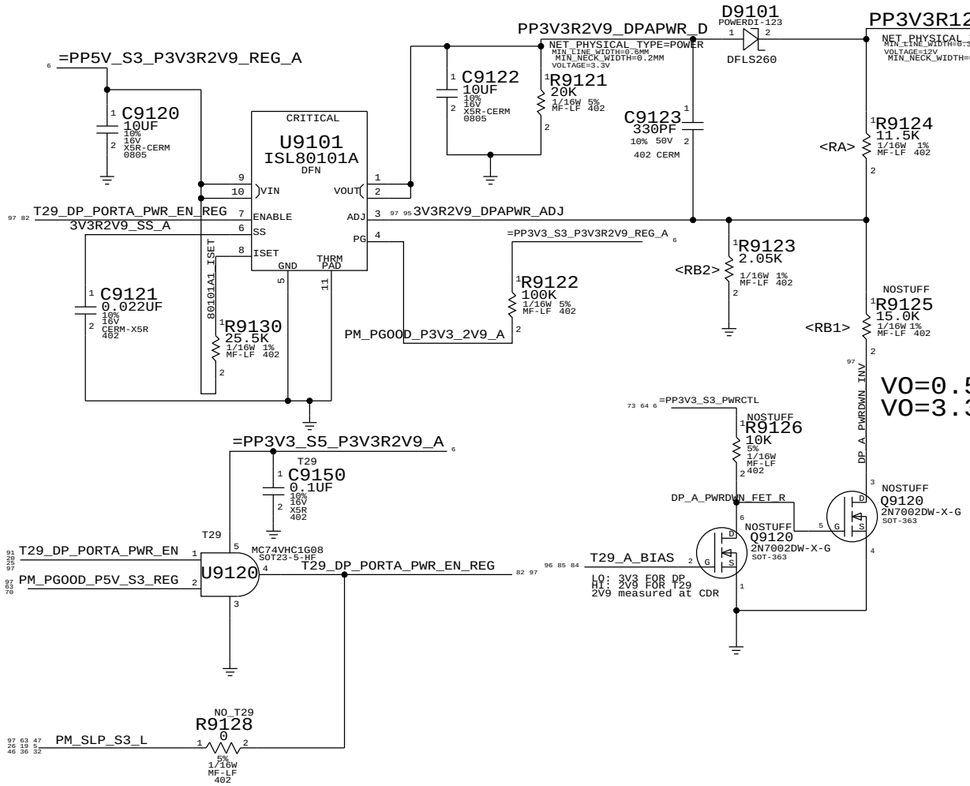
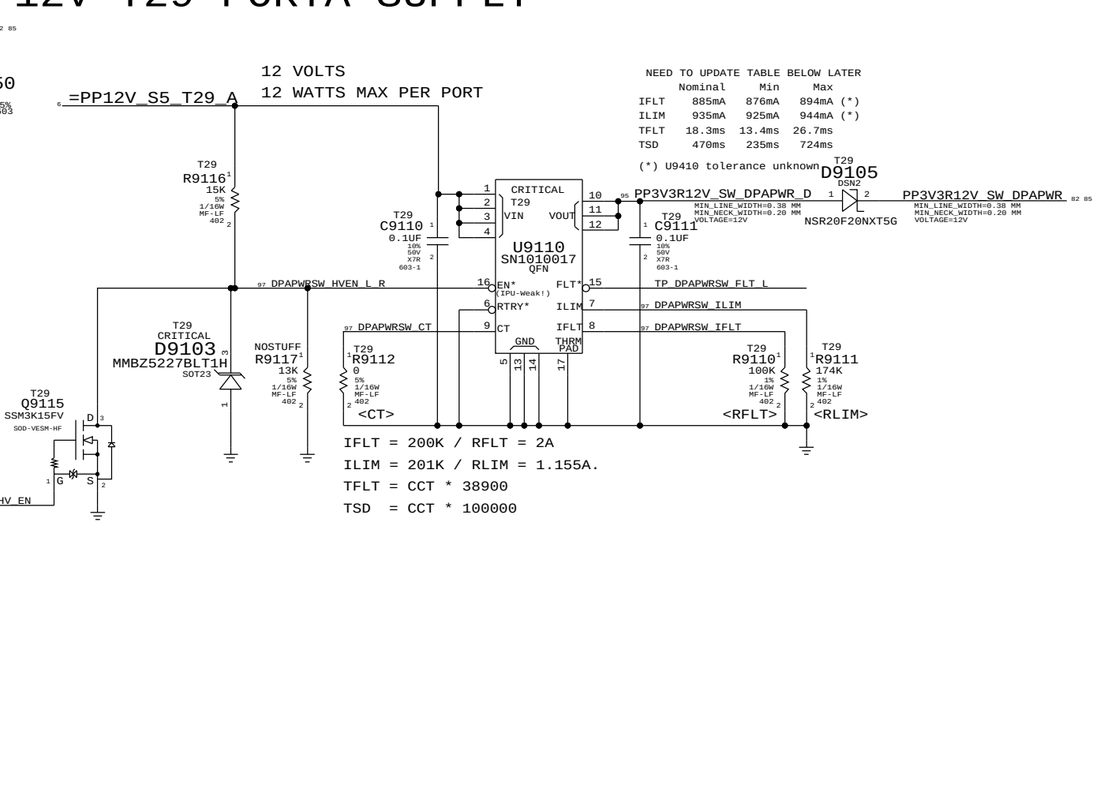
# 3V3(DP)/2V9(T29) PORTA SUPPLY




# 12V T29 PORTA SUPPLY




SYNC_MASTER=K62 SYNC_DATE=11/14/2010

PAGE TITLE
2V9/3V3/12V POWER SWITCH

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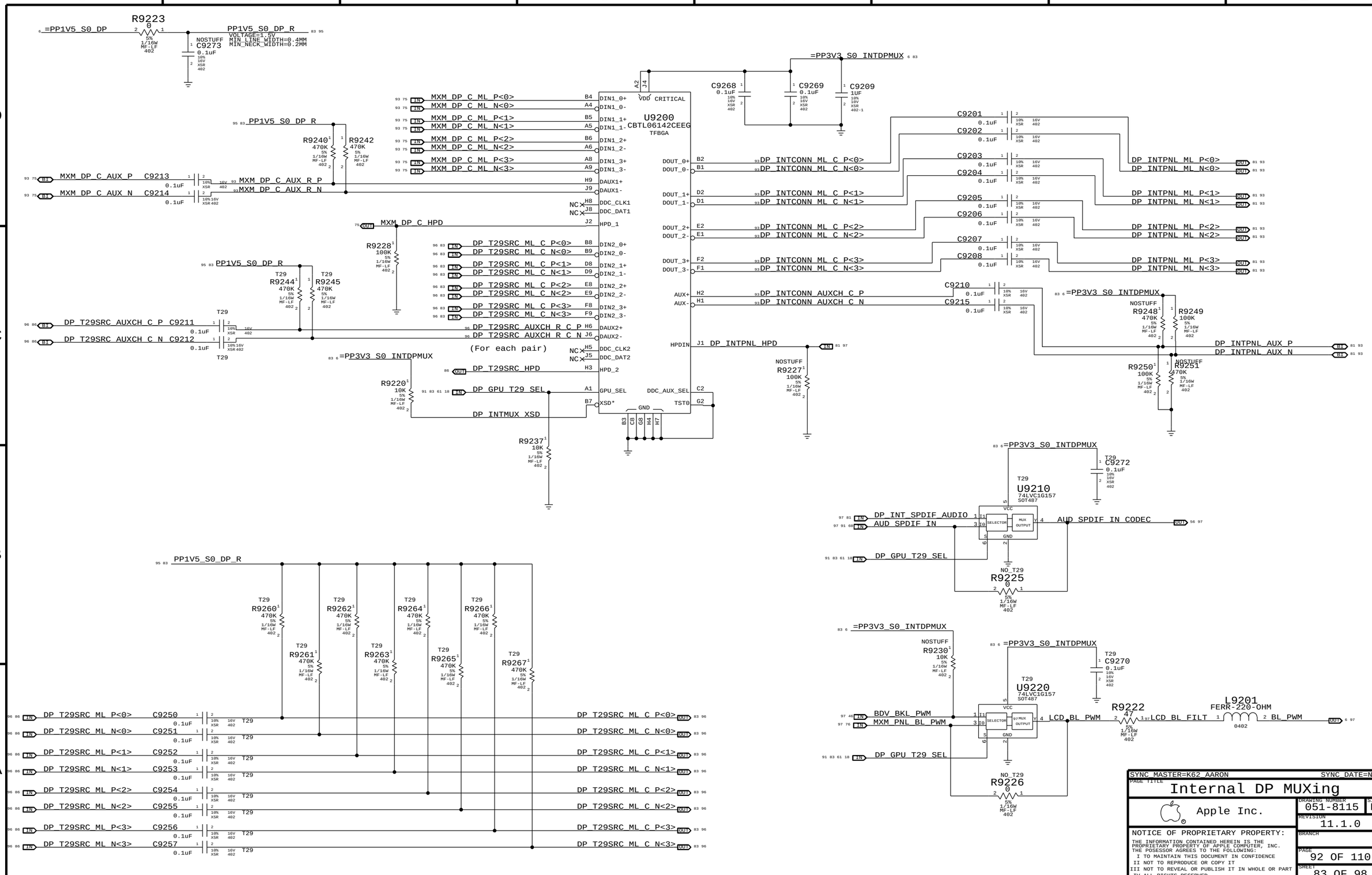
R9223 0
=PP1V5_S0_DP
PP1V5_S0_DP_R
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NOSTUFF C9273 0.1uF
U9200 CBTL06142CEEG TFBGA
VDD CRITICAL
=PP3V3_S0_INTDPMUX
C9268 0.1uF
C9269 0.1uF
C9209 1UF
MXM_DP_C_ML_P<0>
MXM_DP_C_ML_N<0>
MXM_DP_C_ML_P<1>
MXM_DP_C_ML_N<1>
MXM_DP_C_ML_P<2>
MXM_DP_C_ML_N<2>
MXM_DP_C_ML_P<3>
MXM_DP_C_ML_N<3>
R9240 470K
R9242 470K
MXM_DP_C_AUX_P C9213 0.1uF
MXM_DP_C_AUX_N C9214 0.1uF
MXM_DP_C_AUX_R_P
MXM_DP_C_AUX_R_N
MXM_DP_C_HPD
R9228 100K
DP_T29SRC_ML_C_P<0>
DP_T29SRC_ML_C_N<0>
DP_T29SRC_ML_C_P<1>
DP_T29SRC_ML_C_N<1>
DP_T29SRC_ML_C_P<2>
DP_T29SRC_ML_C_N<2>
DP_T29SRC_ML_C_P<3>
DP_T29SRC_ML_C_N<3>
R9244 470K
R9245 470K
DP_T29SRC_AUXCH_C_P C9211 0.1uF
DP_T29SRC_AUXCH_C_N C9212 0.1uF
DP_T29SRC_AUXCH_R_C_P
DP_T29SRC_AUXCH_R_C_N
(For each pair)
=PP3V3_S0_INTDPMUX
DP_T29SRC_HPD
R9220 10K
DP_GPU_T29_SEL
DP_INTMUX_XSD
R9237 10K
GND
DOUT_0+
DOUT_0-
DOUT_1+
DOUT_1-
DOUT_2+
DOUT_2-
DOUT_3+
DOUT_3-
AUX+
AUX-
HPDIN
DDC_AUX_SEL
TST0
DP_INTCONN_ML_C_P<0>
DP_INTCONN_ML_C_N<0>
DP_INTCONN_ML_C_P<1>
DP_INTCONN_ML_C_N<1>
DP_INTCONN_ML_C_P<2>
DP_INTCONN_ML_C_N<2>
DP_INTCONN_ML_C_P<3>
DP_INTCONN_ML_C_N<3>
DP_INTCONN_AUXCH_C_P
DP_INTCONN_AUXCH_C_N
DP_INTPNL_HPD
NOSTUFF R9227 100K
C9201 0.1uF
C9202 0.1uF
C9203 0.1uF
C9204 0.1uF
C9205 0.1uF
C9206 0.1uF
C9207 0.1uF
C9208 0.1uF
DP_INTPNL_ML_P<0>
DP_INTPNL_ML_N<0>
DP_INTPNL_ML_P<1>
DP_INTPNL_ML_N<1>
DP_INTPNL_ML_P<2>
DP_INTPNL_ML_N<2>
DP_INTPNL_ML_P<3>
DP_INTPNL_ML_N<3>
C9210 0.1uF
C9215 0.1uF
=PP3V3_S0_INTDPMUX
NOSTUFF R9248 470K
R9249 100K
DP_INTPNL_AUX_P
DP_INTPNL_AUX_N
R9250 100K
NOSTUFF R9251 470K
=PP3V3_S0_INTDPMUX
C9272 0.1uF
U9210 74LVC1G157 SOT487
DP_INT_SPDIF_AUDIO
AUD_SPDIF_IN
AUD_SPDIF_IN_CODEC
DP_GPU_T29_SEL
NO_T29 R9225 0
=PP3V3_S0_INTDPMUX
NOSTUFF R9230 10K
=PP3V3_S0_INTDPMUX
C9270 0.1uF
U9220 74LVC1G157 SOT487
BDV_BKL_PWM
MXM_PNL_BL_PWM
LCD_BL_PWM
R9222 47
LCD_BL_FILT
L9201 FERR-220-OHM
BL_PWM
DP_GPU_T29_SEL
NO_T29 R9226 0
R9260 470K
R9261 470K
R9262 470K
R9263 470K
R9264 470K
R9265 470K
R9266 470K
R9267 470K
DP_T29SRC_ML_P<0> C9250 0.1uF
DP_T29SRC_ML_N<0> C9251 0.1uF
DP_T29SRC_ML_P<1> C9252 0.1uF
DP_T29SRC_ML_N<1> C9253 0.1uF
DP_T29SRC_ML_P<2> C9254 0.1uF
DP_T29SRC_ML_N<2> C9255 0.1uF
DP_T29SRC_ML_P<3> C9256 0.1uF
DP_T29SRC_ML_N<3> C9257 0.1uF
DP_T29SRC_ML_C_P<0>
DP_T29SRC_ML_C_N<0>
DP_T29SRC_ML_C_P<1>
DP_T29SRC_ML_C_N<1>
DP_T29SRC_ML_C_P<2>
DP_T29SRC_ML_C_N<2>
DP_T29SRC_ML_C_P<3>
DP_T29SRC_ML_C_N<3>
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SYNC_DATE=N/A
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Internal DP MUXing
Apple Inc.
DRAWING NUMBER 051-8115
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# T29 A High-Speed Signals

DP EXTA ML C P<0> C9300 0.1uF → DP EXTA ML P<0>
DP EXTA ML C N<0> C9301 0.1uF → DP EXTA ML N<0>
DP EXTA ML C P<1> C9302 0.1uF → DP EXTA ML P<1>
DP EXTA ML C N<1> C9303 0.1uF → DP EXTA ML N<1>
DP EXTA ML C P<2> C9304 0.1uF → DP EXTA ML P<2>
DP EXTA ML C N<2> C9305 0.1uF → DP EXTA ML N<2>
DP EXTA ML C P<3> C9306 0.1uF → DP EXTA ML P<3>
DP EXTA ML C N<3> C9307 0.1uF → DP EXTA ML N<3>
DP EXTA AUXCH C P C9308 0.1uF → DP EXTA AUXCH P
DP EXTA AUXCH C N C9309 0.1uF → DP EXTA AUXCH N

R9309 1M 5% MF-LF 1/16W 402 =PP3V3_S0_DPSDRVA
R9308 1M 5% MF-LF 1/16W 402

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

T29 signals are P/N-swapped after AC caps to improve layout.

T29 D2R N<0> / T29 D2R P<0> → T29 D2R C P<0> / T29 D2R C N<0>
OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9372 1.0NH+/-0.1NH 0201-1 T29 — T29 R2D C P<0> → T29 R2D C F N<0>
L9373 1.0NH+/-0.1NH 0201-1 T29 — T29 R2D C N<0> → T29 R2D C F P<0>
(All 4 L's)

T29 A BIAS R2D P0 VOLTAGE=3.3V
GND_VOID=TRUE (C9370/C9371)
C9370 0.47uF CERM-X5R-1 201 T29
C9371 0.47uF CERM-X5R-1 201 T29
(C9372.2) GND_VOID=TRUE C9372 0.47uF CERM-X5R-1 201 T29
(C9373.2) GND_VOID=TRUE C9373 0.47uF CERM-X5R-1 201 T29
T29 A BIAS R2D N0 VOLTAGE=3.3V

R9372 1.5K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY — T29 R2D P<0>
R9373 1.5K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY — T29 R2D N<0>
GND_VOID=TRUE T29

T29 A BIAS R2D P1 VOLTAGE=3.3V
GND_VOID=TRUE (C9380/C9381)
C9380 0.47uF CERM-X5R-1 201 T29
C9381 0.47uF CERM-X5R-1 201 T29
T29 D2R P<1> / T29 D2R N<1> → T29 D2R C P<1> / T29 D2R C N<1>
OVERSIZE_PAD=0.875 mm^2 (Both L's)
L9382 1.0NH+/-0.1NH 0201-1 T29 — T29 R2D C N<1> → T29 R2D C F N<1>
L9383 1.0NH+/-0.1NH 0201-1 T29 — T29 R2D C P<1> → T29 R2D C F P<1>
(C9383.2) GND_VOID=TRUE C9382 0.47uF CERM-X5R-1 201 T29
(C9383.2) GND_VOID=TRUE C9383 0.47uF CERM-X5R-1 201 T29
T29 A BIAS R2D N1 VOLTAGE=3.3V

R9382 1.5K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY — T29 R2D P<1>
R9383 1.5K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY — T29 R2D N<1>
GND_VOID=TRUE T29

T29 Path Biasing

D9364 BAR90-02LRH TSLP-2-7 — GND_VOID=TRUE (D9364.2)
D9372 BAR90-02LRH TSLP-2-7 — T29: TX_0 — T29DPA ML C P<0>
D9373 BAR90-02LRH TSLP-2-7 — T29DPA ML C N<0>
D9365 BAR90-02LRH TSLP-2-7
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY
R9374 1.5K 5% 1/20W MF 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
R9375 1.5K 5% 1/20W MF 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
T29 D2R C P<1> / T29 D2R C N<1>

D9360 BAR90-02LRH TSLP-2-7 — GND_VOID=TRUE (D9360.2)
D9382 BAR90-02LRH TSLP-2-7 — T29: TX_1 — T29DPA ML C P<2>
D9383 BAR90-02LRH TSLP-2-7 — T29DPA ML C N<2>
D9361 BAR90-02LRH TSLP-2-7
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)
R9384 1.5K 5% 1/20W MF 201 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
R9385 1.5K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

# DP A Super-Driver

=PP3V3_S0_DPSDRVA
C9310 2.2UF 20% 6.3V CERM 402-LF; C9311 0.1UF 20% 10V CERM 402; C9312 0.1UF 20% 10V CERM 402

PS8301 I2C Addresses:

| A1 | A0 | Addr (W/R) |
|---|---|---|
| 0 | 0 | 0x96/0x97 |
| 0 | 1 | 0xB6/0xB7 |
| 1 | 0 | 0x94/0x95 |
| 1 | 1 | 0xB4/0xB5 |

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF R9311 1K 5% 1/16W MF-LF 402; R9310 1K 5% 1/16W MF-LF 402; R9312 1K 5% 1/16W MF-LF 402

U9310 PS8301TQFN40GTR-A QFN CRITICAL
DP EXTA ML P<0> → IN_D0P; DP EXTA ML N<0> → IN_D0N
DP EXTA ML P<1> → IN_D1P; DP EXTA ML N<1> → IN_D1N
DP EXTA ML P<2> → IN_D2P; DP EXTA ML N<2> → IN_D2N
DP EXTA ML P<3> → IN_D3P; DP EXTA ML N<3> → IN_D3N
DP EXTA DDC CLK → IN_SCL; DP EXTA DDC DATA → IN_SDA
DP EXTA AUXCH P → IN_AUXP; DP EXTA AUXCH N → IN_AUXN
DP EXTA HPD → IN_HPD
DPSDRVA I2C CTL EN → I2C_CTL_EN (IPU)
DPSDRVA I2C ADDR0 → I2C_ADDR0 (IPD)
DPSDRVA I2C ADDR1 → I2C_ADDR1 (IPD)
=I2C DPSDRVA SCL → SCL_CTL; =I2C DPSDRVA SDA → SDA_CTL
DPSDRVA REXT → REXT
DP AUXCH ISOL → AUXDDC_OFF (IPD)
DP A PWRDWN R → PD (IPD)
OUT_D0P → DP SDRVA ML C P<0>; OUT_D0N → DP SDRVA ML C N<0>
OUT_D1P → DP SDRVA ML C P<1>; OUT_D1N → DP SDRVA ML C N<1>
OUT_D2P → DP SDRVA ML C P<2>; OUT_D2N → DP SDRVA ML C N<2>
OUT_D3P → DP SDRVA ML C P<3>; OUT_D3N → DP SDRVA ML C N<3>
AC_AUXP → DP SDRVA AUXCH C P; AC_AUXN → DP SDRVA AUXCH C N
OUT_AUXP_SCL → (DP_SDRVA_AUXCH_P); OUT_AUXN_SDA → (DP_SDRVA_AUXCH_N)
(IPD) OUT_HPD → (DP_SDRVA_HPD)
CA_DET → DP A CA DET
CEXT → DPSDRVA CEXT
VDD; GND; THMPAD

R9370 390 5% 1/20W MF 201; R9371 390 5% 1/20W MF 201
R9354 22; R9355 22; R9350 22; R9351 22
R9352 390 5% 1/20W MF 201; R9353 390 5% 1/20W MF 201
DP SDRVA ML R P<0> / DP SDRVA ML R N<0> → DP SDRVA ML P<0> / DP SDRVA ML N<0>
DP SDRVA ML R P<2> / DP SDRVA ML R N<2> → DP SDRVA ML P<2> / DP SDRVA ML N<2>
C9363 0.1uF; C9362 0.1uF; C9367 0.1uF; C9366 0.1uF; C9369 0.1uF; C9368 0.1uF 10% 16V X5R-CERM 0201
C9319 2.2UF 20% 6.3V CERM 402-LF

AUXCH Snoop Port, used by PS8301 during training.

SDRV_PD R9318 0 5% 1/16W MF-LF 402; R9319 4.02K 1% 1/16W MF-LF 402

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

# DP/T29 A Low-Speed MUX

C9359 0.1uF; CRITICAL U9359 74LVC1G04DBDCK SC70
DP A PWRDWN → DP A BIAS
IC supports input high while Vcc = 0V.

R9361 1.5K 5% 1/20W MF 201 — DP A BIAS N 2 VOLTAGE=3.3V — R9362 51 5% 1/20W MF 201
R9360 1.5K 5% 1/20W MF 201 — DP A BIAS P 2 VOLTAGE=3.3V — R9363 51 5% 1/20W MF 201
R9365 1.5K 5% 1/20W MF 201 — DP A BIAS N 0 VOLTAGE=3.3V — R9366 51 5% 1/20W MF 201
R9364 1.5K 5% 1/20W MF 201 — DP A BIAS P 0 VOLTAGE=3.3V — R9367 51 5% 1/20W MF 201
Both R's: C9358 0.1uF 10% 16V X5R-CERM 0201

PP3V3_SW_DPAPWR Must be 3.3V DP A port power
C9390 0.1uF; C9391 0.1uF 20% 10V CERM 402
R9399 100K 5% 1/16W MF-LF 402

U9390 CBTL04DP081 HVQFN CRITICAL
DIN1_0+ / DIN1_0- / DIN1_1+ / DIN1_1- / AUX1+ / AUX1- / HPD_1 / DIN2_0+ / DIN2_0- / DIN2_1+ / DIN2_1- / AUX2+ / AUX2- / HPD_2 / GPU_SEL / AUX_SEL / NC
DOUT_0+ / DOUT_0- / DOUT_1+ / DOUT_1- / AUX+ / AUX- / HPD_IN
DP SDRVA ML N<3> / DP SDRVA ML P<3> → T29DPA ML N<3> / T29DPA ML P<3> — T29: Unused
DP SDRVA ML N<1> / DP SDRVA ML P<1> → T29DPA ML N<1> / T29DPA ML P<1> — T29: LSX_A_R2P/P2R (P/N)
DP SDRVA AUXCH P / DP SDRVA AUXCH N → DP A EXT AUXCH P / DP A EXT AUXCH N — T29: RX_1 Bias Sink
DP SDRVA HPD → DP A EXT HPD
DP SDRVA ML N<3> / DP SDRVA ML P<3> / DP SDRVA ML N<1> / DP SDRVA ML P<1> / DP SDRVA AUXCH P / DP SDRVA AUXCH N / DP SDRVA HPD
CKPLUS_WAIVE=NdifPr_badTerm
T29 A RSVD N / T29 A RSVD P
(T29_A_LSX_P2R) / (T29_A_LSX_R2P)
T29 D2R1 BIASP / T29 D2R1 BIASN
NC
LO=Port A HI=Port B
THMPAD GND
SIGNAL_MODEL=T29DP_MUX

T29 R9392 51 5% 1/16W MF-LF 402; T29 R9393 51 5% 1/16W MF-LF 402
T29 R9396 1K 5% 1/16W MF-LF 402; T29 R9397 1K 5% 1/16W MF-LF 402
DP A PWRDWN; T29 A BIAS
R9398 100K 5% 1/16W MF-LF 402

CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

# Port A MCU

PP3V3_SW_DPAPWR Must be 3.3V DP A port power
C9330 0.1uF; C9331 0.1uF 20% 10V CERM 402
R9338 10K 5% 1/16W MF-LF 402

CRITICAL U9330 LPC1112A HVQFN25
RESET#/PIO0_0 → DP A CA DET
PIO0_1/CLKOUT → T29 LSEO<0>
PIO0_2/SSEL/CT16B0_CAP0
PIO0_4/SCL (OD) → =I2C T29AMCU SCL
PIO0_5/SDA (OD) → =I2C T29AMCU SDA
PIO0_6/SCK → T29DPA HPD
PIO0_7/CTS# → T29 A BIAS
PIO0_8/MISO/CT16B0_MAT0 → T29 LSOE<0>
PIO0_9/MOSI/CT16B0_MAT1 → T29 LSOE<1>
SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)
R/PIO0_11/AD0 (OD) → T29 MCU INT L
R/PIO1_0/AD1 → T29DPA CONFIG1 RC
R/PIO1_1/AD2 → T29DPA CONFIG2 RC
R/PIO1_2/AD3 → T29 A HV EN R
(IPU) SWDIO/PIO1_3/AD4 → T29 A UC ADDR
PIO1_4/AD5/WAKEUP → DP A EXT HPD
PIO1_6/RXD → T29 A LSX P2R (P2R = PLUG TO RECEPTACLE)
PIO1_7/TXD → T29 A LSX R2P (R2P = RECEPTACLE TO PLUG)
PIO1_8/CT16B1_CAP0 → T29 LSEO<1>
XTALIN; VSS; THRM PAD

DP A PWRDWN
=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#
=T29 WAKE L
OMIT R9330 0 5% 1/16W MF-LF 402 — SWCLK, SWDIO
T29 A UC ADDR

R9335 1K 5% 1/16W MF-LF 402; R9336 10K 5% 1/16W MF-LF 402
I2C Addr: 0x26/0x27 (Wr/Rd)
T29 R9334 10K 5% 1/16W MF-LF 402 — T29 A HV EN
T29 R9339 1M 5% 1/16W MF-LF 402
NO_T29 R9378 T29 A BIAS 0 5% MF 1/20W 201
NO_T29 R9380 T29DPA CONFIG1 RC 0 5% MF 1/20W 201 DP A CA DET
NO_T29 R9379 T29DPA HPD 0 5% MF 1/20W 201 DP A EXT HPD
NO_T29 R9381 DP A PWRDWN 0 5% MF 1/20W 201

R9330 provides pads for programming/debug of MCU, please make accessible. If project has space for 10-pin programming header it should be used.

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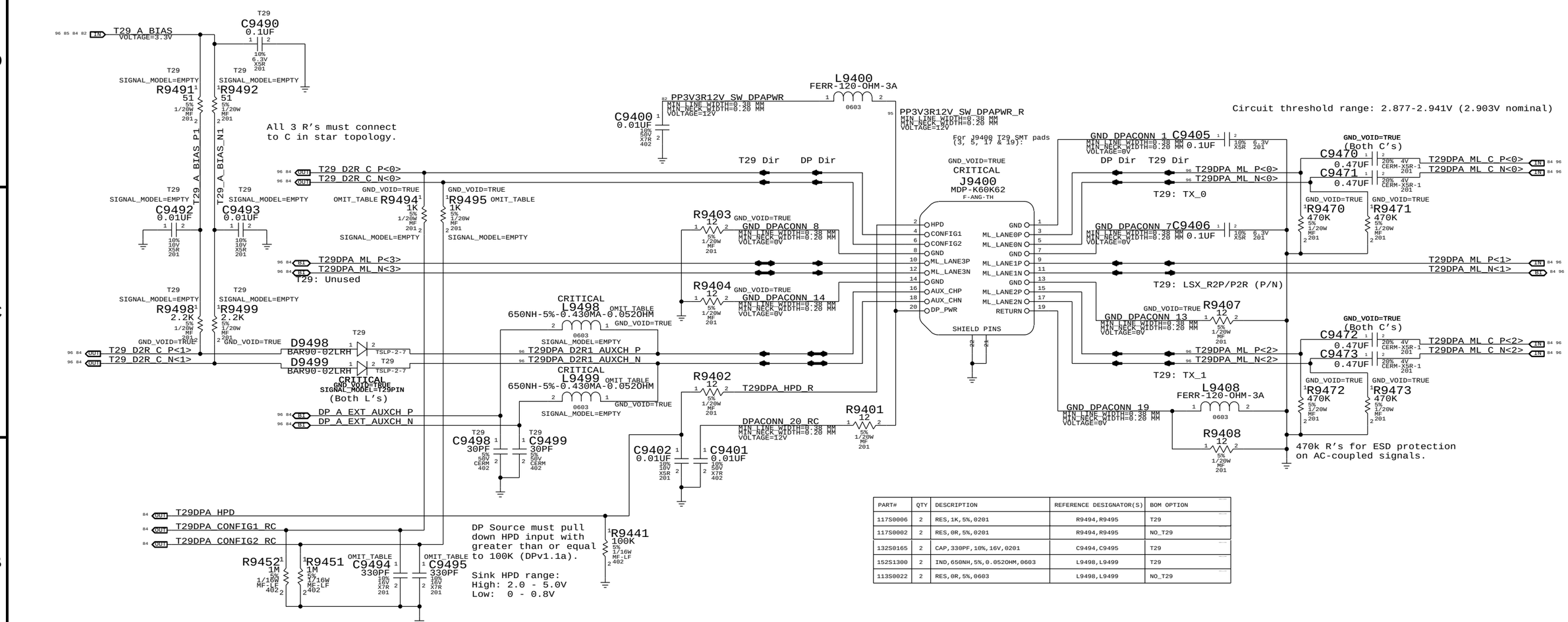
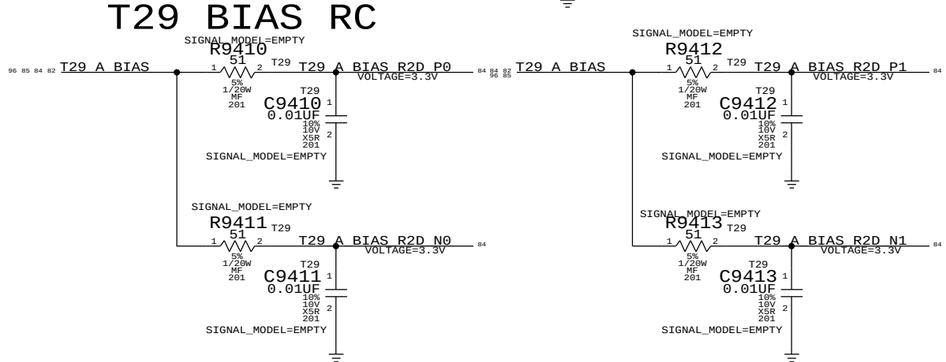
# DisplayPort/T29 A Connector

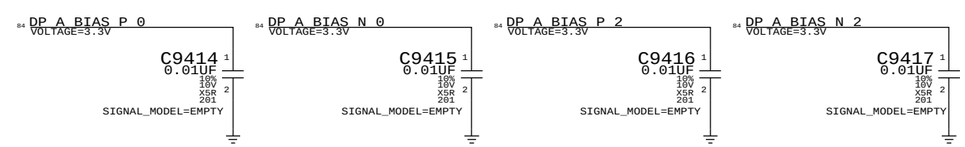



| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION |
|---|---|---|---|---|
| 117S0006 | 2 | RES,1K,5%,0201 | R9494,R9495 | T29 |
| 117S0002 | 2 | RES,0R,5%,0201 | R9494,R9495 | NO_T29 |
| 132S0165 | 2 | CAP,330PF,10%,16V,0201 | C9494,C9495 | T29 |
| 152S1300 | 2 | IND,650NH,5%,0.052OHM,0603 | L9498,L9499 | T29 |
| 113S0022 | 2 | RES,0R,5%,0603 | L9498,L9499 | NO_T29 |

## T29 BIAS RC




## DP BIAS CAPS

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PAGE TITLE: DisplayPort/T29 A Connector

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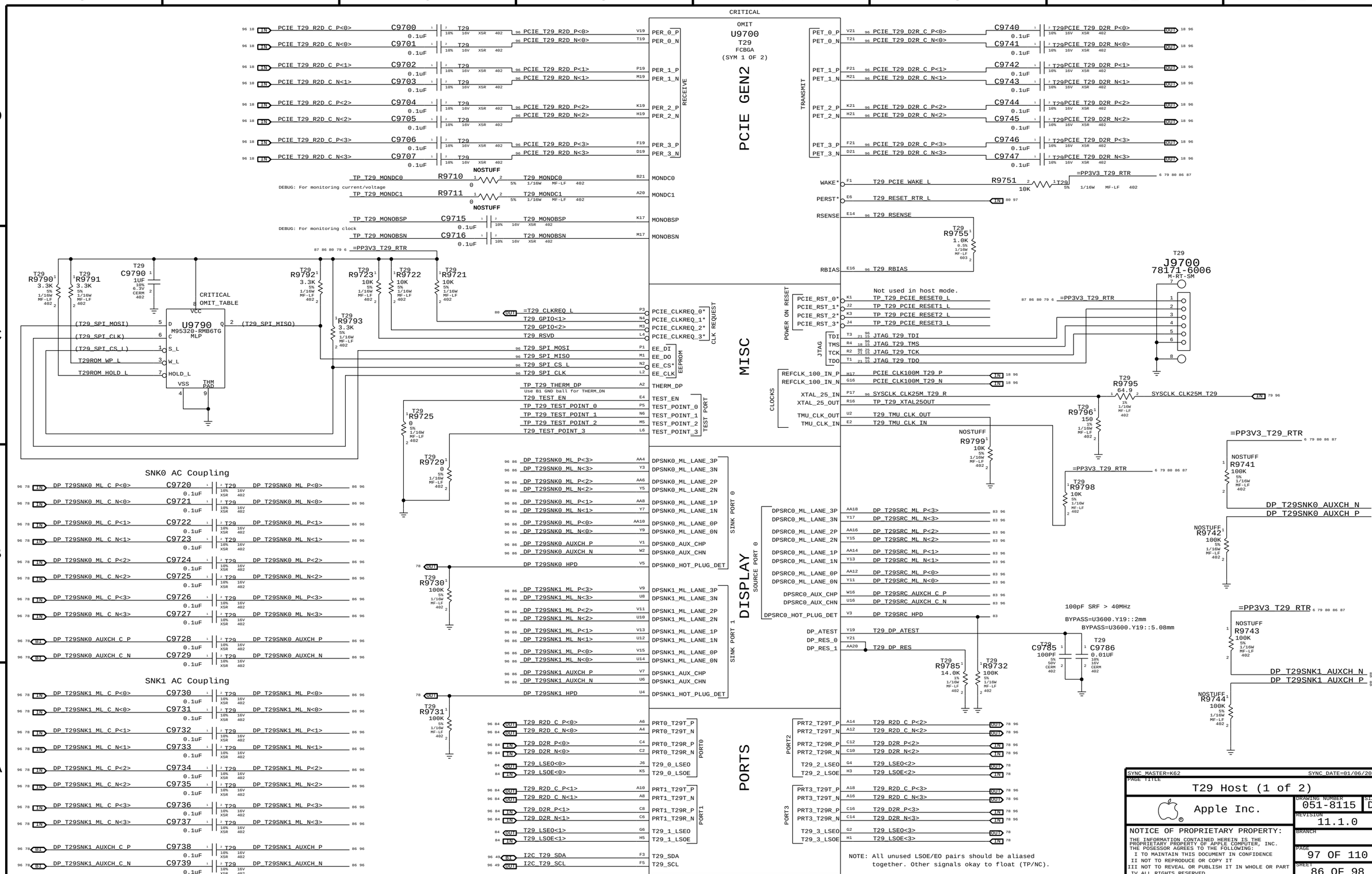


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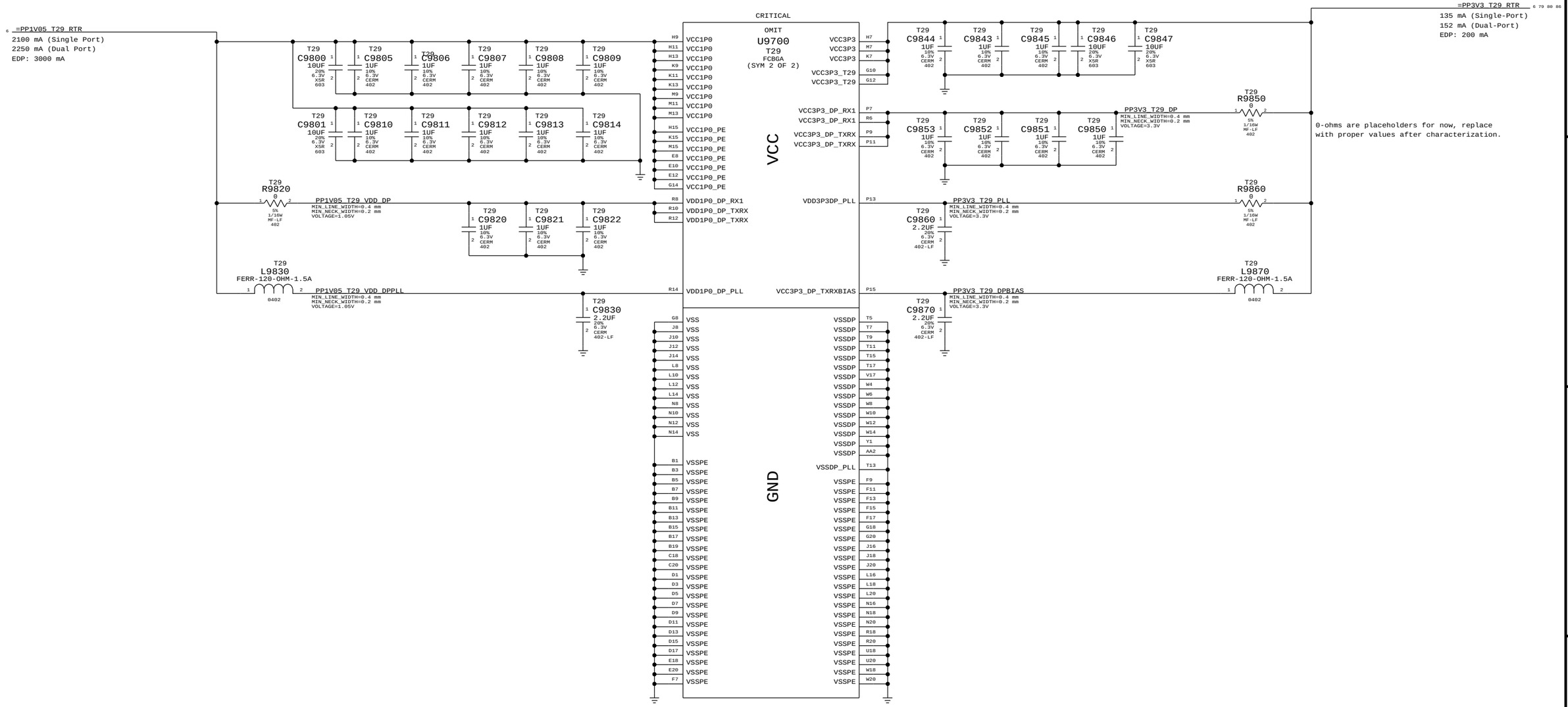


Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

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# K60/62 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

| BOARD LAYERS | BOARD AREAS | BOARD UNITS (MIL or MM) | ALLEGRO VERSION |
|---|---|---|---|
| TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM | NO_TYPE,BGA,BGA_P1MM | MM | 15.5.1 |

## PHYSICAL CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DEFAULT | * | Y | =50_OHM_SE | =50_OHM_SE | 100 MM | 0 MM | 0 MM |
| STANDARD | * | Y | =DEFAULT | =DEFAULT | 12.7 MM | =DEFAULT | =DEFAULT |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 34_OHM_SE | TOP,BOTTOM | Y | 0.21 MM | 0.090 MM | =STANDARD | | |
| 34_OHM_SE | * | Y | 0.19 MM | 0.090 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 39_OHM_SE | TOP,BOTTOM | Y | 0.175 MM | 0.090 MM | =STANDARD | | |
| 39_OHM_SE | * | Y | 0.159 MM | 0.090 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 42_OHM_SE | TOP,BOTTOM | Y | 0.151 MM | 0.090 MM | =STANDARD | | |
| 42_OHM_SE | * | Y | 0.135 MM | 0.090 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 50_OHM_SE | TOP,BOTTOM | Y | 0.1 MM | 0.085 MM | 15 MM | | |
| 50_OHM_SE | * | Y | 0.1 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 55_OHM_SE | TOP,BOTTOM | Y | 0.085 MM | 0.085 MM | =STANDARD | | |
| 55_OHM_SE | * | Y | 0.076 MM | 0.076 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 68_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 68_OHM_DIFF | ISL3,ISL6 | Y | 0.16 MM | 0.090 MM | =STANDARD | 0.13 MM | 0.1 MM |
| 68_OHM_DIFF | TOP,BOTTOM | Y | 0.165 MM | 0.090 MM | =STANDARD | 0.13 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 85_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 85_OHM_DIFF | ISL3,ISL6 | Y | 0.115 MM | 0.085 MM | =STANDARD | 0.2 MM | 0.1 MM |
| 85_OHM_DIFF | TOP,BOTTOM | Y | 0.125 MM | 0.085 MM | =STANDARD | 0.2 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 90_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 90_OHM_DIFF | ISL3,ISL6 | Y | 0.099 MM | 0.085 MM | 12 MM | 0.2 MM | 0.1 MM |
| 90_OHM_DIFF | TOP,BOTTOM | Y | 0.110 MM | 0.085 MM | =STANDARD | 0.2 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 100_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 100_OHM_DIFF | ISL3,ISL6 | Y | 0.081 MM | 0.081 MM | =STANDARD | 0.25 MM | 0.1 MM |
| 100_OHM_DIFF | TOP,BOTTOM | Y | 0.091 MM | 0.085 MM | =STANDARD | 0.25 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 110_OHM_DIFF | * | N | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 110_OHM_DIFF | ISL3,ISL6 | Y | =STANDARD | =STANDARD | =STANDARD | =STANDARD | =STANDARD |
| 110_OHM_DIFF | TOP,BOTTOM | Y | 0.075 MM | 0.075 MM | =STANDARD | 0.320 MM | 0.15 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 1:1_DIFFPAIR | * | Y | =STANDARD | =STANDARD | =STANDARD | 0.1 MM | 0.085 MM |
| POWER_WIDTH | * | Y | 0.600 MM | 0.200 MM | 3.0 MM | =STANDARD | =STANDARD |
| POWER_CTL | * | Y | 0.300 MM | 0.200 MM | 3.0 MM | =STANDARD | =STANDARD |

## SPACING RULE SET

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DEFAULT | * | 0.1 MM | ? |
| STANDARD | * | =DEFAULT | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| 2:1_SPACING | * | 0.2 MM | ? |
| 2.5:1_SPACING | * | 0.25 MM | ? |
| 3:1_SPACING | * | 0.3 MM | ? |
| 3.5:1_SPACING | * | 0.35 MM | ? |
| 4:1_SPACING | * | 0.4 MM | ? |
| 5:1_SPACING | * | 0.5 MM | ? |
| 6:1_SPACING | * | 0.6 MM | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| 2X_DIELECTRIC | * | 0.155 MM | ? |
| 2X_DIELECTRIC | TOP,BOTTOM | 0.145 MM | ? |
| 3X_DIELECTRIC | * | 0.230 MM | ? |
| 3X_DIELECTRIC | TOP,BOTTOM | 0.215 MM | ? |
| 4X_DIELECTRIC | * | 0.305 MM | ? |
| 4X_DIELECTRIC | TOP,BOTTOM | 0.285 MM | ? |
| 5X_DIELECTRIC | * | 0.380 MM | ? |
| 5X_DIELECTRIC | TOP,BOTTOM | 0.355 MM | ? |
| 7X_DIELECTRIC | * | 0.532 MM | ? |
| 7X_DIELECTRIC | TOP,BOTTOM | 0.497 MM | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GND | * | * | STANDARD |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| POWER | * | * | STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| GND | * | =STANDARD | ? |
| GND_P2MM | * | 0.2 MM | 1000 |
| PWR_P2MM | * | 0.2 MM | 1000 |
| SWITCHNODE | * | 0.8 MM | 1000 |

## CONSTRAINTS FOR BGA AREA

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| BGA_P1MM | * | =DEFAULT | ? |
| BGA_P1P5MM | * | 0.15 MM | ? |
| BGA_P2MM | * | 0.2 MM | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| * | * | BGA_P1MM | BGA_P1MM |
| * | * | BGA | BGA_P1MM |
| MEM_CLK | * | BGA | BGA_P1P5MM |
| CLK_PCIE | * | BGA | BGA_P1MM |
| CLK_LPC | * | BGA | BGA_P1MM |
| CLK_PCI | * | BGA | BGA_P1MM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| VR_CONTROL | * | * | SWITCHNODE |
| VR_CONTROL | VR_CONTROL | * | STANDARD |
| VR_CONTROL | SWITCHNODE | * | STANDARD |
| VR_CONTROL | GND | * | STANDARD |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| POWER | BGA_P1MM | POWER_CTL |
| POWER | * | POWER_WIDTH |
| VR_CTL_PHY | BGA_P1MM | DEFAULT |
| VR_CTL_PHY | * | POWER_CTL |

## BOARD STACK-UP

| | | |
|---|---|---|
| TOP | HALF OZ | SIGNAL |
| | 0.071 | PREPREG |
| 2 | TWO OZ | GND |
| | 0.076 | PREPREG |
| 3 | ONE OZ | SIGNAL |
| | 0.370 | PREPREG |
| 4 | TWO OZ | POWER |
| | 0.101 | CORE |
| 5 | TWO OZ | POWER |
| | 0.370 | PREPREG |
| 6 | ONE OZ | SIGNAL |
| | 0.076 | PREPREG |
| 7 | TWO OZ | GND |
| | 0.071 | PREPREG |
| BOTTOM | HALF OZ | SIGNAL |

BOARD THICKNESS = 62 MIL (1.5748 mm)

SYNC MASTER=K62 SYNC DATE=01/06/2011

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## Memory Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| MEM_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| MEM_42S | * | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =STANDARD | =STANDARD |
| MEM_39S | * | =39_OHM_SE | =39_OHM_SE | =39_OHM_SE | =39_OHM_SE | =STANDARD | =STANDARD |
| MEM_34S | * | =34_OHM_SE | =34_OHM_SE | =34_OHM_SE | =34_OHM_SE | =STANDARD | =STANDARD |
| MEM_68D | * | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF |
| MEM_42S_D | * | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | 0.1016 MM | 0.1016 MM |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| MEM_CLK2MEM | * | =4:1_SPACING | ? |
| MEM_CTRL2CTRL | * | =2.5:1_SPACING | ? |
| MEM_CTRL2MEM | * | =3:1_SPACING | ? |
| MEM_CMD2CMD | * | =2:1_SPACING | ? |
| MEM_CMD2MEM | * | =3:1_SPACING | ? |
| MEM_DQ_SAMEBYTE | * | =3:1_SPACING | ? |
| MEM_DQ_DIFFBYTE | * | =5:1_SPACING | ? |
| MEM_DATA2MEM | * | =4:1_SPACING | ? |
| MEM_DQS2MEM | * | =4:1_SPACING | ? |
| MEM_2OTHER | * | =5:1_SPACING | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_CLK | MEM_CLK | * | MEM_CLK2MEM |
| MEM_CLK | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_CMD | MEM_CTRL | * | MEM_CMD2MEM |
| MEM_CMD | MEM_CMD | * | MEM_CMD2CMD |
| MEM_CMD | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_CTRL | MEM_CTRL | * | MEM_CTRL2CTRL |
| MEM_CTRL | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DQS | MEM_CTRL | * | MEM_DQS2MEM |
| MEM_DQS | MEM_CMD | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE0 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE1 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE2 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE3 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE4 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE5 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE6 | * | MEM_DQS2MEM |
| MEM_DQS | MEM_DQ_BYTE7 | * | MEM_DQS2MEM |
| MEM_DQS | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DQ_BYTE5 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE5 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE5 | MEM_DQ_BYTE5 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE5 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE5 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE5 | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DQ_BYTE6 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE6 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE6 | MEM_DQ_BYTE6 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE6 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE6 | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DQ_BYTE7 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE7 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE7 | MEM_DQ_BYTE7 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE7 | * | * | MEM_2OTHER |

## Memory Bus Spacing Group Assignments

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DQ_BYTE0 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE0 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE0 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE1 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE2 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE3 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE4 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE5 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE0 | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DQ_BYTE1 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE1 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE1 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE2 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE3 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE4 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE5 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE1 | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DQ_BYTE2 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE2 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE2 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE3 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE4 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE5 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE2 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE2 | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DQ_BYTE3 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE3 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE3 | MEM_DQ_BYTE3 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE3 | MEM_DQ_BYTE4 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE3 | MEM_DQ_BYTE5 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE3 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE3 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE3 | * | * | MEM_2OTHER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| MEM_DQ_BYTE4 | MEM_CTRL | * | MEM_DATA2MEM |
| MEM_DQ_BYTE4 | MEM_CMD | * | MEM_DATA2MEM |
| MEM_DQ_BYTE4 | MEM_DQ_BYTE4 | * | MEM_DQ_SAMEBYTE |
| MEM_DQ_BYTE4 | MEM_DQ_BYTE5 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE4 | MEM_DQ_BYTE6 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE4 | MEM_DQ_BYTE7 | * | MEM_DQ_DIFFBYTE |
| MEM_DQ_BYTE4 | * | * | MEM_2OTHER |

## Memory Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| | MEM_68D | MEM_CLK | MEM_A_CLK_P<3..0> | 12 32 |
| | MEM_68D | MEM_CLK | MEM_A_CLK_N<3..0> | 12 32 |
| | MEM_39S | MEM_CTRL | MEM_A_CKE<3..0> | 12 30 |
| | MEM_39S | MEM_CTRL | MEM_A_CS_L<3..0> | 12 30 |
| | MEM_39S | MEM_CTRL | MEM_A_ODT<3..0> | 12 30 |
| | MEM_34S | MEM_CMD | MEM_A_A<15..0> | 12 30 |
| | MEM_34S | MEM_CMD | MEM_A_BA<2..0> | 12 30 |
| | MEM_34S | MEM_CMD | MEM_A_RAS_L | 12 30 |
| | MEM_34S | MEM_CMD | MEM_A_CAS_L | 12 30 |
| | MEM_34S | MEM_CMD | MEM_A_WE_L | 12 30 |
| | MEM_42S | MEM_DQ_BYTE0 | MEM_A_DQ<7..0> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE1 | MEM_A_DQ<15..8> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE2 | MEM_A_DQ<23..16> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE3 | MEM_A_DQ<31..24> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE4 | MEM_A_DQ<39..32> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE5 | MEM_A_DQ<47..40> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE6 | MEM_A_DQ<55..48> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE7 | MEM_A_DQ<63..56> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_P<0> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_N<0> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_P<1> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_N<1> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_P<2> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_N<2> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_P<3> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_N<3> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_P<4> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_N<4> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_P<5> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_N<5> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_P<6> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_N<6> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_P<7> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_A_DQS_N<7> | 12 32 |
| H17P | MEM_50S | PM | MEM_RESET_L | 30 31 32 97 |

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| | MEM_68D | MEM_CLK | MEM_B_CLK_P<3..0> | 12 32 |
| | MEM_68D | MEM_CLK | MEM_B_CLK_N<3..0> | 12 32 |
| | MEM_39S | MEM_CTRL | MEM_B_CKE<3..0> | 12 31 |
| | MEM_39S | MEM_CTRL | MEM_B_CS_L<3..0> | 12 31 |
| | MEM_39S | MEM_CTRL | MEM_B_ODT<3..0> | 12 31 |
| | MEM_34S | MEM_CMD | MEM_B_A<15..0> | 12 31 |
| | MEM_34S | MEM_CMD | MEM_B_BA<2..0> | 12 31 |
| | MEM_34S | MEM_CMD | MEM_B_RAS_L | 12 31 |
| | MEM_34S | MEM_CMD | MEM_B_CAS_L | 12 31 |
| | MEM_34S | MEM_CMD | MEM_B_WE_L | 12 31 |
| | MEM_42S | MEM_DQ_BYTE0 | MEM_B_DQ<7..0> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE1 | MEM_B_DQ<15..8> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE2 | MEM_B_DQ<23..16> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE3 | MEM_B_DQ<31..24> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE4 | MEM_B_DQ<39..32> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE5 | MEM_B_DQ<47..40> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE6 | MEM_B_DQ<55..48> | 12 32 |
| | MEM_42S | MEM_DQ_BYTE7 | MEM_B_DQ<63..56> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_P<0> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_N<0> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_P<1> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_N<1> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_P<2> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_N<2> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_P<3> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_N<3> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_P<4> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_N<4> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_P<5> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_N<5> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_P<6> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_N<6> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_P<7> | 12 32 |
| | MEM_42S_D | MEM_DQS | MEM_B_DQS_N<7> | 12 32 |

## MEMORY MISC PROPERTIES

| VOLTAGE | NET_TYPE PHYSICAL | NET_TYPE SPACING | VOLTAGE | | |
|---|---|---|---|---|---|
| | MEM_POWER_PHY | MEM_POWER | | CPU_DIMM_VREF_A | |
| | MEM_POWER_PHY | MEM_POWER | | CPU_DIMM_VREF_B | |
| H16P | MEM_POWER_PHY | MEM_POWER | | CPU_DDR_VREF | 11 28 |
| H16N | MEM_POWER_PHY | MEM_POWER | | VREFMARGIN_DIMMA_DACOUT | 28 |
| H16P | MEM_POWER_PHY | MEM_POWER | | VREFMARGIN_DIMMA_OPFB | 28 |
| H17N | MEM_POWER_PHY | MEM_POWER | | VREFMARGIN_DIMMA_DQ | 28 |
| H17P | MEM_POWER_PHY | MEM_POWER | | CPU_DIMM_VREF_A_SW | |
| H17N | MEM_POWER_PHY | MEM_POWER | | VREFMARGIN_DIMMB_DACOUT | 28 |
| H17P | MEM_POWER_PHY | MEM_POWER | | VREFMARGIN_DIMMB_OPFB | 28 |
| H17N | MEM_POWER_PHY | MEM_POWER | | VREFMARGIN_DIMMB_DQ | 28 |
| H17P | MEM_POWER_PHY | MEM_POWER | | CPU_DIMM_VREF_B_SW | |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| MEM_POWER_WIDTH | * | Y | 0.500 MM | 0.250 MM | =STANDARD | =STANDARD | =STANDARD |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| MEM_POWER_PHY | * | MEM_POWER_WIDTH |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| MEM_POWER | * | =3:1_SPACING | ? |

SYNC_MASTER=K60_ROSITA SYNC_DATE=01/06/2011

PAGE TITLE
# Memory Constraints

Apple Inc.

DRAWING NUMBER 051-8115 SIZE D

REVISION 11.1.0

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## PCI-Express

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| PCIE_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |
| CLK_PCIE_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| PCIE | * | =4X_DIELECTRIC | ? |
| CLK_PCIE | * | 0.5 MM | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| PCIE | TOP,BOTTOM | =4:1_SPACING | ? |

## CPU

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CPU_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| CPU_RCOMP_PHY | * | Y | 0.254 MM | 0.200 MM | 3.0 MM | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CPU_ITP | * | 0.2 MM | ? |
| CPU_RCOMP | * | 0.2 MM | ? |

## SATA Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SATA_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SATA | * | =6:1_SPACING | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SATA | TOP,BOTTOM | =6:1_SPACING | ? |

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| **SATA** | | | | |
| 1B9D | SATA_90D | SATA | SATA_SSD_R2D_C_P | 18 42 |
| 1B9E | SATA_90D | SATA | SATA_SSD_R2D_C_N | 18 42 |
| 1B9F | SATA_90D | SATA | SATA_SSD_R2D_P | 42 |
| 1BA0 | SATA_90D | SATA | SATA_SSD_R2D_N | 42 |
| 1BA1 | SATA_90D | SATA | SATA_SSD_D2R_P | 18 42 |
| 1BA2 | SATA_90D | SATA | SATA_SSD_D2R_N | 18 42 |
| 1BA3 | SATA_90D | SATA | SATA_SSD_D2R_C_P | 42 |
| 1BA4 | SATA_90D | SATA | SATA_SSD_D2R_C_N | 42 |
| **PCIE** | | | | |
| 1B1C | PCIE_85D | PCIE | PCIE_USB3_1_R2D_P | |
| 1B1D | PCIE_85D | PCIE | PCIE_USB3_1_R2D_N | |
| 1B1E | PCIE_85D | PCIE | PCIE_USB3_1_R2D_C_P | |
| 1B1F | PCIE_85D | PCIE | PCIE_USB3_1_R2D_C_N | |
| 1B20 | PCIE_85D | PCIE | PCIE_USB3_1_D2R_P | |
| 1B21 | PCIE_85D | PCIE | PCIE_USB3_1_D2R_N | |
| 1B22 | PCIE_85D | PCIE | PCIE_USB3_1_D2R_C_P | |
| 1B23 | PCIE_85D | PCIE | PCIE_USB3_1_D2R_C_N | |
| 1B2C | PCIE_85D | PCIE | PCIE_USB3_2_R2D_P | |
| 1B2D | PCIE_85D | PCIE | PCIE_USB3_2_R2D_N | |
| 1B2E | PCIE_85D | PCIE | PCIE_USB3_2_R2D_C_P | |
| 1B2F | PCIE_85D | PCIE | PCIE_USB3_2_R2D_C_N | |
| 1B30 | PCIE_85D | PCIE | PCIE_USB3_2_D2R_P | |
| 1B31 | PCIE_85D | PCIE | PCIE_USB3_2_D2R_N | |
| 1B32 | PCIE_85D | PCIE | PCIE_USB3_2_D2R_C_P | |
| 1B33 | PCIE_85D | PCIE | PCIE_USB3_2_D2R_C_N | |
| **CPU ITP** | | | | |
| | CPU_50S | CPU_ITP | XDP_BPM_L<7..0> | 11 25 |
| | CPU_50S | CPU_ITP | CPU_CFG<17..0> | 10 15 25 |
| 1B43 | CPU_50S | CPU_ITP | XDP_OBSDATA_B<3..0> | 25 |
| 1B44 | CPU_50S | CPU_ITP | XDP_CPU_CFG<0> | 25 |
| 1B45 | CPU_50S | CPU_ITP | XDP_CPU_TDO | 11 25 |
| 1B46 | CPU_50S | CPU_ITP | XDP_CPU_TDI | 11 25 |
| 1B47 | CPU_50S | CPU_ITP | XDP_CPU_TMS | 11 25 |
| 1B48 | CPU_50S | CPU_ITP | XDP_CPU_TCK | 11 25 |
| 1B49 | CPU_50S | CPU_ITP | XDP_CPU_TRST_L | 11 25 |
| **CPU_MISC** | | | | |
| | CPU_RCOMP_PHY | CPU_RCOMP | CPU_PEG_COMP | 10 |

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| **PCIE GRAPHICS** | | | | |
| | PCIE_85D | PCIE | PEG_R2D_C_P<15..0> | 9 77 |
| | PCIE_85D | PCIE | PEG_R2D_C_N<15..0> | 9 77 |
| | PCIE_85D | PCIE | PEG_D2R_P<15..0> | 9 77 |
| | PCIE_85D | PCIE | PEG_D2R_N<15..0> | 9 77 |
| | PCIE_85D | PCIE | MXM_PCIE_R2D_P<7..0> | 75 77 |
| | PCIE_85D | PCIE | MXM_PCIE_R2D_N<7..0> | 75 77 |
| | PCIE_85D | PCIE | MXM_PCIE_D2R_P<7..0> | 75 77 |
| | PCIE_85D | PCIE | MXM_PCIE_D2R_N<7..0> | 75 77 |
| **PCIE I/O** | | | | |
| | PCIE_85D | PCIE | PCIE_MINI_R2D_P | 33 |
| | PCIE_85D | PCIE | PCIE_MINI_R2D_N | 33 |
| | PCIE_85D | PCIE | PCIE_MINI_R2D_C_P | 18 33 |
| | PCIE_85D | PCIE | PCIE_MINI_R2D_C_N | 18 33 |
| | PCIE_85D | PCIE | PCIE_MINI_D2R_P | 18 33 |
| | PCIE_85D | PCIE | PCIE_MINI_D2R_N | 18 33 |
| | PCIE_85D | PCIE | PCIE_FW_R2D_P | 39 |
| | PCIE_85D | PCIE | PCIE_FW_R2D_N | 39 |
| | PCIE_85D | PCIE | PCIE_FW_R2D_C_P | 18 39 |
| | PCIE_85D | PCIE | PCIE_FW_R2D_C_N | 18 39 |
| | PCIE_85D | PCIE | PCIE_FW_D2R_P | 18 39 |
| | PCIE_85D | PCIE | PCIE_FW_D2R_N | 18 39 |
| | PCIE_85D | PCIE | PCIE_FW_D2R_C_P | 39 |
| | PCIE_85D | PCIE | PCIE_FW_D2R_C_N | 39 |
| **DMI** | | | | |
| 1B1B | CLK_PCIE_90D | CLK_PCIE | DMI_MIDBUS_CLK100M_N | |
| 1B1C | CLK_PCIE_90D | CLK_PCIE | DMI_MIDBUS_CLK100M_P | |
| 1B1D | CLK_PCIE_90D | CLK_PCIE | DMI_CLK100M_CPU_N | 11 18 |
| 1B1E | CLK_PCIE_90D | CLK_PCIE | DMI_CLK100M_CPU_P | 11 18 |
| | PCIE_85D | PCIE | DMI_S2N_P<3..0> | 10 19 |
| | PCIE_85D | PCIE | DMI_S2N_N<3..0> | 10 19 |
| | PCIE_85D | PCIE | DMI_N2S_P<3..0> | 10 19 |
| | PCIE_85D | PCIE | DMI_N2S_N<3..0> | 10 19 |
| **PCIE REF CLOCKS** | | | | |
| | CLK_PCIE_90D | CLK_PCIE | GPU_CLK100M_PCIE_P | 9 |
| | CLK_PCIE_90D | CLK_PCIE | GPU_CLK100M_PCIE_N | 9 |
| | CLK_PCIE_90D | CLK_PCIE | PCIE_CLK100M_MINI_P | 18 33 |
| | CLK_PCIE_90D | CLK_PCIE | PCIE_CLK100M_MINI_N | 18 33 |
| | CLK_PCIE_90D | CLK_PCIE | PCIE_CLK100M_FW_P | 18 39 |
| | CLK_PCIE_90D | CLK_PCIE | PCIE_CLK100M_FW_N | 18 39 |
| | ENET_100D | ENET_MII | PCIE_CLK100M_ENET_P | 18 37 |
| | ENET_100D | ENET_MII | PCIE_CLK100M_ENET_N | 18 37 |
| **SATA** | | | | |
| | SATA_90D | SATA | SATA_HDD_R2D_C_P | 18 42 |
| | SATA_90D | SATA | SATA_HDD_R2D_C_N | 18 42 |
| | SATA_90D | SATA | SATA_HDD_R2D_P | 42 |
| | SATA_90D | SATA | SATA_HDD_R2D_N | 42 |
| | SATA_90D | SATA | SATA_HDD_D2R_P | 18 42 |
| | SATA_90D | SATA | SATA_HDD_D2R_N | 18 42 |
| | SATA_90D | SATA | SATA_HDD_D2R_C_P | 42 |
| | SATA_90D | SATA | SATA_HDD_D2R_C_N | 42 |
| | SATA_90D | SATA | SATA_ODD_R2D_C_P | 18 42 |
| | SATA_90D | SATA | SATA_ODD_R2D_C_N | 18 42 |
| | SATA_90D | SATA | SATA_ODD_R2D_P | 42 |
| | SATA_90D | SATA | SATA_ODD_R2D_N | 42 |
| | SATA_90D | SATA | SATA_ODD_D2R_P | 18 42 |
| | SATA_90D | SATA | SATA_ODD_D2R_N | 18 42 |
| | SATA_90D | SATA | SATA_ODD_D2R_C_P | 42 |
| | SATA_90D | SATA | SATA_ODD_D2R_C_N | 42 |
| **CLOCKS** | | | | |
| | CLK_PCIE_90D | CLK_PCIE | PCH_CLK100M_DMI_P | 18 26 |
| | CLK_PCIE_90D | CLK_PCIE | PCH_CLK100M_DMI_N | 18 26 |
| | CLK_PCIE_90D | CLK_PCIE | PCH_CLK96M_DOT_P | 18 26 |
| | CLK_PCIE_90D | CLK_PCIE | PCH_CLK96M_DOT_N | 18 26 |
| | CLK_PCIE_90D | CLK_PCIE | PCH_CLK100M_SATA_P | 18 26 |
| | CLK_PCIE_90D | CLK_PCIE | PCH_CLK100M_SATA_N | 18 26 |
| | CLK_PCIE_90D | CLK_PCIE | ITPXDP_CLK100M_N | 18 25 |
| | CLK_PCIE_90D | CLK_PCIE | ITPXDP_CLK100M_P | 18 25 |
| | CLK_PCIE_90D | CLK_PCIE | ITPCPU_CLK100M_N | 11 18 |
| | CLK_PCIE_90D | CLK_PCIE | ITPCPU_CLK100M_P | 11 18 |
| 1B37 | CLK_PCIE_90D | CLK_PCIE | XDP_CPU_CLK100M_P | 25 |
| 1B38 | CLK_PCIE_90D | CLK_PCIE | XDP_CPU_CLK100M_N | 25 |
| **UNUSED CLOCKS** | | | | |
| 1B3B | CLK_PCIE_90D | CLK_PCIE | TP_CLK133M_PCH_N | 26 |
| 1B3C | CLK_PCIE_90D | CLK_PCIE | TP_CLK133M_PCH_P | 26 |
| **UNUSED PCIE** | | | | |
| 1B3D | PCIE_85D | PCIE | MXM_PCIE_R2D_P<8..15> | 75 77 |
| 1B3E | PCIE_85D | PCIE | MXM_PCIE_R2D_N<8..15> | 75 77 |
| 1B3F | PCIE_85D | PCIE | MXM_PCIE_D2R_P<8..15> | 75 77 |
| 1B40 | PCIE_85D | PCIE | MXM_PCIE_D2R_N<8..15> | 75 77 |

SYNC_MASTER=K62 SYNC_DATE=01/06/2011

PAGE TITLE
# PCIE/DMI/FDI/SATA CONSTRAINTS

Apple Inc.

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## PCH CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| PCH_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_PCH_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_PCH | * | =4:1_SPACING | ? |
| COMP_PCH | * | 0.2 MM | ? |
| ITP_PCH | * | 0.2 MM | ? |

## PCI Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| PCI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_PCI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| PCI | * | =STANDARD | ? |
| CLK_PCI | * | 0.2 MM | ? |

## LPC Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| LPC_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| CLK_LPC_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| LPC | * | 0.15 MM | ? |
| CLK_LPC | * | 0.2 MM | ? |

## SMBus Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SMB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SMB | * | =2x_DIELECTRIC | ? |

## HD Audio Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| HDA_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| HDA | * | =2x_DIELECTRIC | ? |

## SPI Interface Constraints

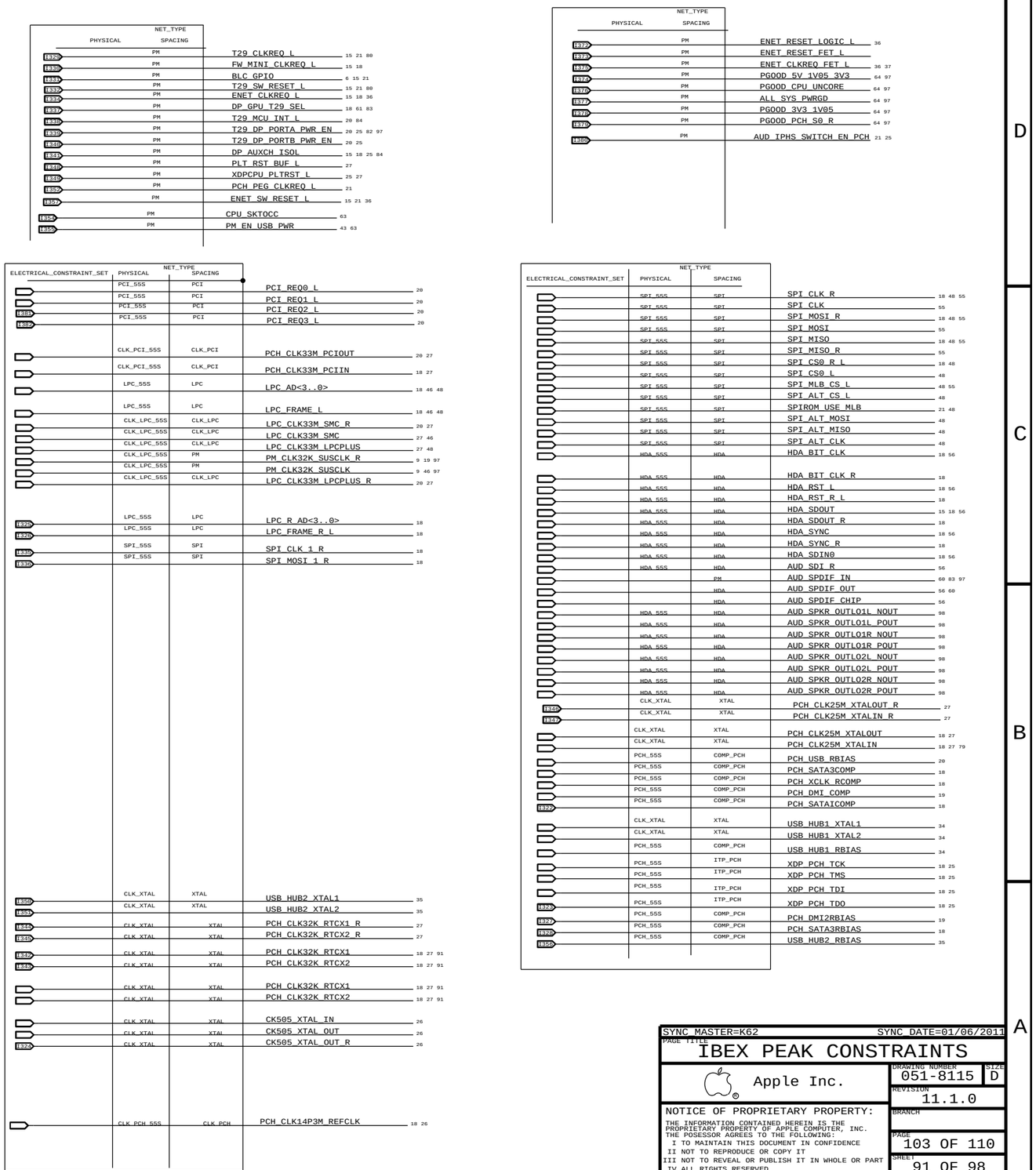
| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SPI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SPI | * | 0.2 MM | ? |

## XTAL Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CLK_XTAL | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| XTAL | * | =4X_DIELECTRIC | ? |

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# IBEX PEAK CONSTRAINTS

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## CAESAR II (ETHERNET) CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| ENET_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| ENET_MII | * | 0.3 MM | ? |
| ENET_SE | * | =STANDARD | ? |

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

## CAESAR II (ETHERNET) CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| ENET_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| ENET_DIFF | * | 0.6 MM | ? |
| ENET_DIFF2DIFF | * | =3:1_SPACING | ? |
| ENET_2OTHER | * | =50MIL_SPACING | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| 50MIL_SPACING | * | 1.27 MM | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| ENET_DIFF | ENET_DIFF | * | ENET_DIFF2DIFF |
| ENET_DIFF_T | * | * | ENET_2OTHER |

## CAESAR IV (SD) CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SD_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SD | * | =3:1_SPACING | ? |

## FireWire Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| FW_110D | * | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF | =110_OHM_DIFF |

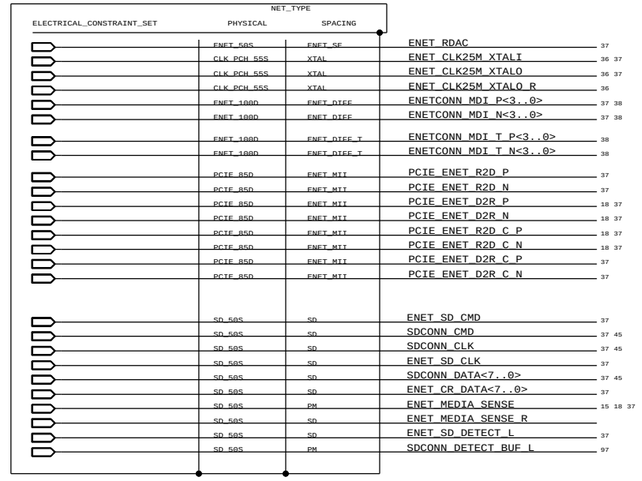
| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| FW_TP | * | =3:1_SPACING | ? |

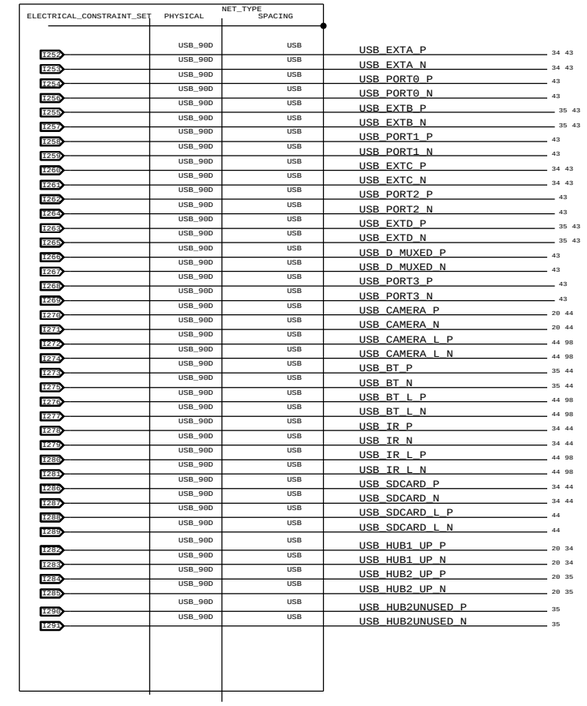
## USB 2.0 Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| USB_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

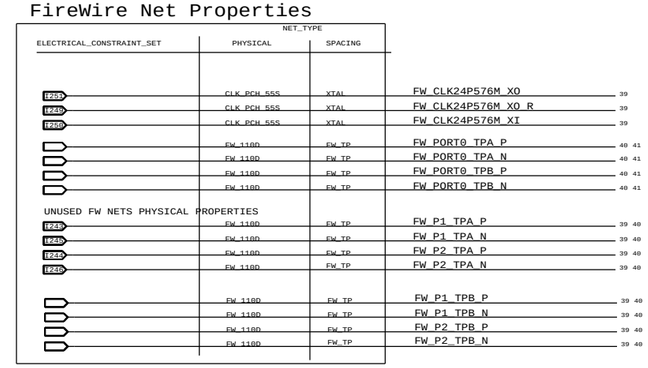
| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| USB | * | =3:1_SPACING | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| USB | TOP,BOTTOM | =4x_DIELECTRIC | ? |




## FireWire Net Properties

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# GRAPHICS CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DP_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | 0.08MM | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DISPLAYPORT | * | =3:1_SPACING | ? |

USE 5X_DIELECTRIC IN K62

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET
ASSINGED IN CONT. MGR.

| | PHYSICAL | SPACING | NET_TYPE | |
|---|---|---|---|---|
| I160 | DP_85D | DISPLAYPORT | DP_INTCONN_ML_C_P<3..0> | 83 |
| I174 | DP_85D | DISPLAYPORT | DP_INTCONN_ML_C_N<3..0> | 83 |
| | DP_85D | DISPLAYPORT | DP_INTCONN_AUXCH_C_P | 83 |
| | DP_85D | DISPLAYPORT | DP_INTCONN_AUXCH_C_N | 83 |
| I152 | DP_85D | DISPLAYPORT | DP_INTPNL_ML_P<3..0> | 81 83 |
| I154 | DP_85D | DISPLAYPORT | DP_INTPNL_ML_N<3..0> | 81 83 |
| | DP_85D | DISPLAYPORT | DP_INTPNL_AUX_P | 81 83 |
| | DP_85D | DISPLAYPORT | DP_INTPNL_AUX_N | 81 83 |
| I181 | DP_85D | DISPLAYPORT | DP_EXTA_ML_P<3..0> | 84 |
| I180 | DP_85D | DISPLAYPORT | DP_EXTA_ML_N<3..0> | 84 |
| I188 | DP_85D | DISPLAYPORT | DP_EXTA_AUXCH_P | 84 |
| I187 | DP_85D | DISPLAYPORT | DP_EXTA_AUXCH_N | 84 |
| I174 | DP_85D | DISPLAYPORT | DP_EXTA_ML_C_P<3..0> | 78 84 |
| I173 | DP_85D | DISPLAYPORT | DP_EXTA_ML_C_N<3..0> | 78 84 |
| I177 | DP_85D | DISPLAYPORT | DP_EXTA_AUXCH_C_P | 78 84 |
| I175 | DP_85D | DISPLAYPORT | DP_EXTA_AUXCH_C_N | 78 84 |
| I193 | DP_85D | DISPLAYPORT | DP_EXTB_ML_P<3..0> | |
| I192 | DP_85D | DISPLAYPORT | DP_EXTB_ML_N<3..0> | |
| I190 | DP_85D | DISPLAYPORT | DP_EXTB_AUXCH_P | |
| I194 | DP_85D | DISPLAYPORT | DP_EXTB_AUXCH_N | |
| I195 | DP_85D | DISPLAYPORT | DP_EXTB_ML_C_P<3..0> | |
| I191 | DP_85D | DISPLAYPORT | DP_EXTB_ML_C_N<3..0> | |
| I189 | DP_85D | DISPLAYPORT | DP_EXTB_AUXCH_C_P | |
| I197 | DP_85D | DISPLAYPORT | DP_EXTB_AUXCH_C_N | |
| I199 | DP_85D | DISPLAYPORT | MXM_DP_B_ML_P<3..0> | 75 78 |
| I200 | DP_85D | DISPLAYPORT | MXM_DP_B_ML_N<3..0> | 75 78 |
| I203 | DP_85D | DISPLAYPORT | MXM_DP_B_AUX_P | 75 78 |
| I202 | DP_85D | DISPLAYPORT | MXM_DP_B_AUX_N | 75 78 |
| I206 | DP_85D | DISPLAYPORT | MXM_DP_C_ML_P<3..0> | 75 83 |
| I204 | DP_85D | DISPLAYPORT | MXM_DP_C_ML_N<3..0> | 75 83 |
| I209 | DP_85D | DISPLAYPORT | MXM_DP_C_AUX_P | 75 83 |
| I208 | DP_85D | DISPLAYPORT | MXM_DP_C_AUX_N | 75 83 |
| I211 | DP_85D | DISPLAYPORT | MXM_DP_C_AUX_R_P | 83 |
| I210 | DP_85D | DISPLAYPORT | MXM_DP_C_AUX_R_N | 83 |
| I207 | DP_85D | DISPLAYPORT | MXM_DP_D_ML_P<3..0> | 75 78 |
| I205 | DP_85D | DISPLAYPORT | MXM_DP_D_ML_N<3..0> | 75 78 |
| I209 | DP_85D | DISPLAYPORT | MXM_DP_D_AUX_P | 75 78 |
| I210 | DP_85D | DISPLAYPORT | MXM_DP_D_AUX_N | 75 78 |

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

| | | | | |
|---|---|---|---|---|
| | DP_85D | DISPLAYPORT | MXM_LVDS_A_CLK_P | 76 78 |
| | DP_85D | DISPLAYPORT | MXM_LVDS_A_CLK_N | 76 78 |
| | DP_85D | DISPLAYPORT | MXM_LVDS_B_CLK_P | 76 78 |
| | DP_85D | DISPLAYPORT | MXM_LVDS_B_CLK_N | 76 78 |
| | DP_85D | DISPLAYPORT | MXM_LVDS_A_DATA_P<3..0> | 76 78 |
| | DP_85D | DISPLAYPORT | MXM_LVDS_A_DATA_N<3..0> | 76 78 |
| | DP_85D | DISPLAYPORT | MXM_LVDS_B_DATA_P<3..0> | 76 78 |
| | DP_85D | DISPLAYPORT | MXM_LVDS_B_DATA_N<3..0> | 76 78 |

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## SMBus Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SMB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SMB | * | =2x_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| THERMAL | * | * | 4:1_SPACING |
| THERMAL | POWER | * | PWR_P2MM |
| THERMAL | GND | * | GND_P2MM |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| THERM_DIFF | * | 1:1_DIFFPAIR |
| SNS_DIFF | * | 1:1_DIFFPAIR |

## SMC SMBus Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| | SMB_55S | SMB | SMBUS_SMC_A_S3_SCL | 49 |
| | SMB_55S | SMB | SMBUS_SMC_A_S3_SDA | 49 |
| | SMB_55S | SMB | SMBUS_SMC_B_S0_SCL | 49 |
| | SMB_55S | SMB | SMBUS_SMC_B_S0_SDA | 49 |
| | SMB_55S | SMB | SMBUS_SMC_0_S0_SCL | 49 |
| | SMB_55S | SMB | SMBUS_SMC_0_S0_SDA | 49 |
| | SMB_55S | SMB | SMBUS_SMC_BSA_SCL | 49 |
| | SMB_55S | SMB | SMBUS_SMC_BSA_SDA | 49 |
| | SMB_55S | SMB | SMBUS_SMC_MGMT_SCL | 49 94 |
| | SMB_55S | SMB | SMBUS_SMC_MGMT_SDA | 49 94 |
| | SMB_55S | SMB | SMBUS_SMC_MGMT_SCL | 49 94 |
| | SMB_55S | SMB | SMBUS_SMC_MGMT_SDA | 49 94 |
| | SMB_55S | SMB | SMBUS_PCH_CLK | 18 49 |
| | SMB_55S | SMB | SMBUS_PCH_DATA | 18 49 |
| | SMB_55S | SMB | SML_PCH_0_CLK | 18 49 |
| | SMB_55S | SMB | SML_PCH_0_DATA | 18 49 |
| | SMB_55S | SMB | SML_PCH_1_CLK | 18 49 |
| | SMB_55S | SMB | SML_PCH_1_DATA | 18 49 |
| | CLK_XTAL | XTAL | SMC_EXTAL | 46 47 |
| | CLK_XTAL | XTAL | SMC_XTAL | 46 47 |
| I254 | SMB_55S | SMB | I2C_VREFMRGN_DIMMA_SCL | 28 |
| I253 | SMB_55S | SMB | I2C_VREFMRGN_DIMMA_SDA | 28 |
| I255 | SMB_55S | SMB | I2C_VREFMRGN_DIMMB_SCL | 28 |
| I256 | SMB_55S | SMB | I2C_VREFMRGN_DIMMB_SDA | 28 |
| I265 | SMB_55S | SMB | SMB_BLC_TCON_SCL | 6 49 81 |
| I264 | SMB_55S | SMB | SMB_BLC_TCON_SDA | 6 49 81 |
| I268 | SMB_55S | SMB | I2C_TCON_SCL | 81 |
| I269 | SMB_55S | SMB | I2C_TCON_SDA | 81 |
| I266 | SMB_55S | SMB | SMB_BLC_PCH_SCL_R | 6 |
| I267 | SMB_55S | SMB | SMB_BLC_PCH_SDA_R | 6 |

## SMC THERMAL NET PROPERTIES

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| | THERM_DIFF | THERMAL | SNS_T1_1_P | 52 |
| | THERM_DIFF | THERMAL | SNS_T1_1_N | 52 |
| | THERM_DIFF | THERMAL | SNS_T2_DP2 | 52 |
| | THERM_DIFF | THERMAL | SNS_T2_DN2 | 52 |
| I208 | THERM_DIFF | THERMAL | SNS_T1_2_P | 52 |
| I209 | THERM_DIFF | THERMAL | SNS_T1_2_N | 52 |
| I207 | THERM_DIFF | THERMAL | SNS_T1_3_P | 52 |
| I206 | THERM_DIFF | THERMAL | SNS_T1_3_N | 52 |
| I211 | THERM_DIFF | THERMAL | SNS_T1_4_P | 52 |
| I212 | THERM_DIFF | THERMAL | SNS_T1_4_N | 52 |
| I213 | THERM_DIFF | THERMAL | SNS_T1_5_P | 52 |
| I214 | THERM_DIFF | THERMAL | SNS_T1_5_N | 52 |
| I215 | THERM_DIFF | THERMAL | SNS_T1_6_P | 52 |
| I216 | THERM_DIFF | THERMAL | SNS_T1_6_N | 52 |
| I217 | THERM_DIFF | THERMAL | SNS_T1_7_P | 52 |
| I218 | THERM_DIFF | THERMAL | SNS_T1_7_N | 52 |
| I220 | THERM_DIFF | THERMAL | SNS_CPU_THERMD_P | 10 52 |
| I221 | THERM_DIFF | THERMAL | SNS_CPU_THERMD_N | 10 52 |
| I219 | THERM_DIFF | THERMAL | SNS_LCD_H_P | 52 |
| I210 | THERM_DIFF | THERMAL | SNS_LCD_H_N | 52 |
| | THERM_DIFF | THERMAL | SNS_ODD_P | 52 98 |
| | THERM_DIFF | THERMAL | SNS_ODD_N | 52 98 |
| | THERM_DIFF | THERMAL | SNS_CPU_H_P | 52 |
| | THERM_DIFF | THERMAL | SNS_CPU_H_N | 52 |
| I222 | THERM_DIFF | THERMAL | SNS_SKIN_RIGHT_P | 52 98 |
| I223 | THERM_DIFF | THERMAL | SNS_SKIN_RIGHT_N | 52 98 |
| | THERM_DIFF | THERMAL | SNS_SKIN_LEFT_P | 44 52 98 |
| | THERM_DIFF | THERMAL | SNS_SKIN_LEFT_N | 44 52 98 |
| | THERM_DIFF | THERMAL | SNS_AMB_P | 52 54 98 |
| | THERM_DIFF | THERMAL | SNS_AMB_N | 52 54 98 |
| | THERM_DIFF | THERMAL | SNS_MXM_P | 52 |
| | THERM_DIFF | THERMAL | SNS_MXM_N | 52 |
| | | THERMAL | HDD_OOB_TEMP_FILT | 42 51 98 |
| | | THERMAL | HDD_OOB_TEMP_FB | 42 |
| | | THERMAL | HDD_OOB_TEMP_R | 51 |
| | | THERMAL | SMC_HDD_OOB_TEMP | 46 51 |

## SMC VOLTAGE/CURRENT NET PROPERTIES

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| | THERM_DIFF | THERMAL | SNS_I_MXM_P | 50 |
| | THERM_DIFF | THERMAL | SNS_I_MXM_N | 50 |
| | THERM_DIFF | THERMAL | SNS_DIMM_1V5_P | 50 |
| | THERM_DIFF | THERMAL | SNS_DIMM_1V5_N | 50 |
| | SNS_DIFF | THERMAL | VR_ISNS_VCORE_P | 50 95 |
| | SNS_DIFF | THERMAL | VR_ISNS_VCORE_N | 50 95 |
| | SNS_DIFF | THERMAL | VR_ISNS_VAXG_P | 50 95 |
| | SNS_DIFF | THERMAL | VR_ISNS_VAXG_N | 50 95 |
| I243 | SNS_DIFF | THERMAL | VR_ISNS_1V05_P | 95 |
| I244 | SNS_DIFF | THERMAL | VR_ISNS_1V05_N | 95 |
| I245 | THERM_DIFF | THERMAL | SNS_CPU_1V5_P | 50 |
| I246 | THERM_DIFF | THERMAL | SNS_CPU_1V5_N | 50 |
| I247 | THERM_DIFF | THERMAL | SNS_VCCSA_P | 50 |
| I248 | THERM_DIFF | THERMAL | SNS_VCCSA_N | 50 |
| I263 | THERM_DIFF | THERMAL | SNS_1V05_PCH_P | 50 |
| I262 | THERM_DIFF | THERMAL | SNS_1V05_PCH_N | 50 |
| I230 | | THERMAL | GND_SMC_AVSS | 46 47 50 94 |
| I241 | | THERMAL | SMC_CPU_1V5_ISENSE | 46 50 |
| I240 | | THERMAL | SMC_CPU_1V5_ISENSE_R | 50 |
| I242 | | THERMAL | SMC_CPU_1V5_VSENSE | 46 50 |
| I229 | | THERMAL | GND_SMC_AVSS | 46 47 50 94 |
| I238 | | THERMAL | SMC_DIMM_ISENSE | 46 50 |
| I239 | | THERMAL | SMC_DIMM_1V5_R | 50 |
| I233 | | THERMAL | SMC_DIMM_VSENSE | 46 50 |
| I228 | | THERMAL | GND_SMC_AVSS | 46 47 50 94 |
| I236 | | THERMAL | SMC_VCCSA_ISENSE | 46 50 |
| I235 | | THERMAL | SMC_VCCSA_ISENSE_R | 50 |
| I237 | | THERMAL | SMC_VCCSA_VSENSE | 46 50 |
| | | THERMAL | GND_SMC_AVSS | 46 47 50 94 |
| | | THERMAL | SMC_PCH_1V05_ISENSE | 46 50 |
| | | THERMAL | SMC_VAXG_VSENSE | 46 50 |
| | | THERMAL | SMC_PCH_1V05_VSENSE | 46 50 |
| I231 | | THERMAL | GND_SMC_AVSS | 46 47 50 94 |
| I232 | | THERMAL | SMC_1V05_ISENSE | 46 50 |
| I227 | | THERMAL | SMC_VAXG_ISENSE | 46 50 |
| I234 | | THERMAL | SMC_1V05_VSENSE | 46 50 |
| I230 | | THERMAL | SMC_GPU_ISENSE | 46 50 |
| | | THERMAL | SMC_GPU_VSENSE | 46 50 |
| | | THERMAL | SMC_VCORE_ISENSE | 46 50 |
| I237 | | THERMAL | SMC_VCORE_VSENSE | 46 50 |
| I235 | | THERMAL | SMC_CPU_VSENSE | |

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| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SWITCHNODE | SWITCHNODE | BGA_P1MM | BGA_P2MM |
| SWITCHNODE | POWER | BGA_P1MM | BGA_P2MM |
| SWITCHNODE | GND | BGA_P1MM | BGA_P2MM |
| SWITCHNODE | * | BGA_P1MM | BGA_P2MM |
| SWITCHNODE | POWER | * | 6:1_SPACING |
| SWITCHNODE | GND | * | 6:1_SPACING |
| SWITCHNODE | * | * | SWITCHNODE |

# POWER NET PROPERTIES

| | NET_TYPE PHYSICAL | SPACING | VOLTAGE | NET | |
|---|---|---|---|---|---|
| I128 | POWER | SWITCHNODE | 1.5V | VR_CPU_PHASE1 | 66 |
| I129 | POWER | SWITCHNODE | 1.5V | VR_CPU_PHASE2 | 66 |
| I130 | POWER | SWITCHNODE | 1.5V | VR_CPU_PHASE3 | 66 |
| I777 | POWER | SWITCHNODE | 1.5V | VR_CPU_PHASE4 | |
| I671 | POWER | SWITCHNODE | 1.5V | VR_AXG_PHASE1 | 67 |
| I132 | POWER | SWITCHNODE | 3.3V | P3V3S5_REG_PHASE | 70 |
| I133 | POWER | SWITCHNODE | 5V | P5VS3_REG_PHASE | 70 |
| I134 | POWER | SWITCHNODE | 1.05V | P1V05S0_PHASE | 68 |
| I742 | POWER | SWITCHNODE | 1.05V | P1V05_REG_PHASE | |
| I136 | POWER | SWITCHNODE | 3.4V | P3V42G3H_SW | 72 |
| I137 | POWER | SWITCHNODE | 3.3V | ENET_3V3_S3_SR_IN | 37 |
| I666 | POWER | SWITCHNODE | 1.2V | ENET_SR_LX | 36 37 |
| I139 | POWER | SWITCHNODE | 1.5V | DDR_REG_PHASE | 71 |
| I140 | POWER | SWITCHNODE | 1.8V | P1V8_REG_PHASE | 71 |
| I141 | POWER | POWER | 0.75V | PP0V75_S3_MEM_VREFCA_A | 28 30 |
| I142 | POWER | POWER | 0.75V | PP0V75_S3_MEM_VREFCA_B | 28 31 |
| I143 | POWER | POWER | 0.75V | PP0V75_S3_MEM_VREFDQ_A | 28 30 |
| I144 | POWER | POWER | 0.75V | PP0V75_S3_MEM_VREFDQ_B | 28 31 |
| I148 | POWER | POWER | 12V | PP12V_S0 | 6 |
| I149 | POWER | POWER | 12V | PP12V_S0_CPU_FLTRD | 65 66 67 |
| I175 | POWER | POWER | 12V | PP12V_S0_FAN0_L | 53 98 |
| I174 | POWER | POWER | 12V | PP12V_S0_FAN1_L | 53 98 |
| I173 | POWER | POWER | 12V | PP12V_S0_FAN2_L | 54 98 |
| I672 | POWER | POWER | 12V | VR_CPU_DRV1_PVCC | 66 |
| I673 | POWER | POWER | 12V | VR_CPU_DRV1_UVCC | 66 |
| I675 | POWER | POWER | 12V | VR_CPU_DRV2_PVCC | 66 |
| I676 | POWER | POWER | 12V | VR_CPU_DRV2_UVCC | 66 |
| I674 | POWER | POWER | 12V | VR_CPU_DRV3_PVCC | 66 |
| I678 | POWER | POWER | 12V | VR_CPU_DRV3_UVCC | 66 |
| I778 | POWER | POWER | 12V | VR_CPU_DRV4_PVCC | |
| I779 | POWER | POWER | 12V | VR_CPU_DRV4_UVCC | |
| I679 | POWER | POWER | 12V | VR_AXG_DRV1_PVCC | 67 |
| I677 | POWER | POWER | 12V | VR_AXG_DRV1_UVCC | |
| I697 | POWER | POWER | 12V | VR_CPU_DRV1_VCC | 66 |
| I698 | POWER | POWER | 12V | VR_CPU_DRV2_VCC | 66 |
| I699 | POWER | POWER | 12V | VR_CPU_DRV3_VCC | 66 |
| I700 | POWER | POWER | 12V | VR_CPU_DRV4_VCC | |
| I654 | POWER | POWER | 12V | PP12V_S0_VG_OK | 41 |
| I653 | POWER | POWER | 12V | P12V_FW_R | 41 |
| I651 | POWER | POWER | 12V | P12V_FW_CL | 41 |
| I652 | POWER | POWER | 12V | P12V_FW_D | 41 |
| I267 | POWER | POWER | 12V | FW_PORT0_VP | 41 |
| I270 | POWER | POWER | 12V | FW_PORT0_VP_F | 41 |
| I544 | POWER | POWER | 12V | PPVP_FW_PHY_CPS | 39 41 |
| I680 | POWER | POWER | 12V | PP12v_S0_P1V05_VREG_VIN | 68 |
| I764 | POWER | POWER | 12V | VCCSA_PWR_RC | 69 |
| I774 | POWER | POWER | 12V | PP12V_S0_BL_R | |
| I775 | POWER | POWER | 12V | PP12V_S5_FET | 6 74 |
| I787 | POWER | POWER | 12V | PP12V_LCD | 81 |
| I604 | POWER | POWER | 12V | PP12V_G3H | 6 |
| I178 | POWER | POWER | 12V | PP12V_S5 | 6 |
| I732 | POWER | POWER | 12V | PP12V_S5_RSN | 74 |
| I268 | POWER | POWER | 0.75V | PPVTT_S0_DDR | 6 |
| I613 | POWER | POWER | 0.75V | PP0V75_S0 | 6 |
| I703 | POWER | POWER | 0.925V | PPVCCSA_S0_CPU | 6 |
| I658 | POWER | POWER | 1.0V | PP1V0_FW_FWPHY_AVDD | 39 |
| I657 | POWER | POWER | 1.0V | PP1V0_S0_FW_VDD | 40 |
| I825 | POWER | POWER | 1.05V | PP1V05_S0_T29 | 6 |
| I746 | POWER | POWER | 1.05V | PP1V05_S0_INPUT_VCCSA | 6 |
| I717 | POWER | POWER | 1.05V | PPVAXG_S0 | 6 |
| I177 | POWER | POWER | 1.05V | PP1V05_S0 | 6 |
| I745 | POWER | POWER | 1.05V | PP1V05_S0_PCH | 6 |
| I179 | POWER | POWER | 1.05V | PP1V05_S0_CK505_F | 26 |
| I715 | POWER | POWER | 1.05V | PPVOUT_S5_PCH_DCPSUS | 22 |
| I182 | POWER | POWER | 1.05V | PP1V05_S0_PCH_VCCADPLLA_F | 17 22 |
| I185 | POWER | POWER | 1.05V | PP1V05_S0_PCH_VCCADPLLB_F | 17 22 |
| I184 | POWER | POWER | 1.05V | PP1V05_S0_PCH_VCCAPLL_EXP_F | 22 24 |
| I737 | POWER | POWER | 1.05V | PP1V05_S0_PCH_VCCAPLLDMI2_F | 22 24 |
| I188 | POWER | POWER | 1.05V | PP1V05_S0_PCH_VCCAPLL_SATA_F | 22 24 |
| I736 | POWER | POWER | 1.05V | PP1V05_S0_PCH_VCCCLKDMI_F | 22 24 |
| I753 | POWER | POWER | 1.1V | PPVCORE_S0_AXG_REG1 | 67 |
| I752 | POWER | POWER | 1.1V | PPVCORE_S0_AXG_REGOUT | 67 |
| I259 | POWER | POWER | 1.1V | PPVCORE_S0_CPU | 6 |
| I258 | POWER | POWER | 1.1V | PPVCORE_S0_CPU_REG1 | 66 |
| I563 | POWER | POWER | 1.1V | PPVCORE_S0_CPU_REG2 | 66 |
| I564 | POWER | POWER | 1.1V | PPVCORE_S0_CPU_REG3 | 66 |
| I786 | POWER | POWER | 1.1V | PPVCORE_S0_CPU_REG4 | |
| I659 | VR_CTL_PHY | VR_CTL | 1.2V | PP1V2_S3_ENET_INTREG | 36 |
| I660 | POWER | POWER | 1.2V | PP1V2_S3_ENET_PHY_AVDDL | 37 |
| I661 | POWER | POWER | 1.2V | PP1V2_S3_ENET_PHY_PCIEPLL | 37 |
| I662 | POWER | POWER | 1.2V | PP1V2_S3_ENET_PHY_GPHYPLL | 37 |
| I194 | POWER | POWER | 1.5V | PP1V5_S0 | 6 |
| I193 | POWER | POWER | 1.5V | PP1V5_S0_CK505_F | 26 |
| I587 | POWER | POWER | 1.5V | PP1V5_S0_CK505_R | 26 |
| I575 | POWER | POWER | 1.5V | PP1V5_S0_CPU_MEM | 6 |
| I754 | POWER | POWER | 1.5V | PP1V5_S0_CPU_SNS | |
| I198 | POWER | POWER | 1.5V | PP1V5_S3 | 6 |
| I704 | POWER | POWER | 1.5V | PP1V5_S3_MEM | 6 |

# POWER NET PROPERTIES

| | NET_TYPE PHYSICAL | SPACING | VOLTAGE | NET | |
|---|---|---|---|---|---|
| I756 | POWER | POWER | 12V | PP12V_S0_MXM | 6 |
| I792 | POWER | POWER | 12V | PP12V_SLG1 | |
| I802 | POWER | POWER | 12V | PP3V3R12V_SW_DPAPWR_1 | |
| I803 | POWER | POWER | 12V | PP3V3R12V_SW_DPBPWR_1 | |
| I797 | POWER | POWER | 1.8V | USB_HUB2_VDD1V8 | 35 |
| I796 | POWER | POWER | 1.8V | USB_HUB2_VDD1V8PLL | 35 |
| I743 | POWER | POWER | 1.8V | PP1V8_S0 | 6 |
| I744 | POWER | POWER | 1.8V | PP1V8R1V5_S0_PCH_VCCVRM_F | 22 24 |
| I758 | POWER | POWER | 1.8V | USB_HUB1_VDD1V8 | 34 |
| I759 | POWER | POWER | 1.8V | USB_HUB1_VDD1V8PLL | 34 |
| I824 | POWER | POWER | 1.8V | PP3V3R1V8_ENET_LR_OUT_REG | 37 |
| I794 | POWER | POWER | 3.3V | PPVBAT_G3_SYSCLK_R | 79 |
| I668 | POWER | POWER | 3.3V | USB_HUB1_VDDPLL3V3 | 34 |
| I667 | POWER | POWER | 3.3V | USB_HUB1_VDDA3V3 | 34 |
| I798 | POWER | POWER | 3.3V | USB_HUB2_VDDPLL3V3 | 35 |
| I799 | POWER | POWER | 3.3V | USB_HUB2_VDDA3V3 | 35 |
| I216 | POWER | POWER | 3.3V | PP3V3R1V5_PCH_VCCSUSHDA | 22 24 |
| I218 | POWER | POWER | 3.3V | PP3V3_S0_CK505_F | 26 |
| I221 | POWER | POWER | 3.3V | PP3V3_S0_HS_F | 62 |
| I655 | POWER | POWER | 3.3V | PP3V3_S0_SW_SD_PWR | 45 |
| I223 | POWER | POWER | 3.3V | PP3V3_S0_PCH_VCCA_DAC_F | 17 22 |
| I839 | POWER | POWER | 3.3V | PP3V3_S0 | 6 |
| I828 | POWER | POWER | 3.3V | PP3V3_SMCUSBMUX | 43 |
| I224 | POWER | POWER | 3.3V | PP3V3_S3 | 6 98 |
| I669 | POWER | POWER | 3.3V | PP3V3_S3_BT_FLT | 44 |
| I557 | POWER | POWER | 3.3V | PP3V3_S3_MINI_CONN | 33 |
| I826 | POWER | POWER | 3.3V | PP3V3_S3_SDCARD_FLT | 44 |
| I748 | POWER | SWITCHNODE | 3.3V | PP3V3_S3_ENET_PHY_FET | 36 |
| I663 | POWER | POWER | 3.3V | PP3V3_S3_ENET_PHY_XTALVDDH | 37 |
| I664 | POWER | POWER | 3.3V | PP3V3_S3_ENET_PHY_BIASVDDH | 37 |
| I665 | POWER | POWER | 3.3V | PP3V3_S3_ENET_PHY_AVDDH | 37 |
| I747 | POWER | POWER | 3.3V | ENET_XTALVDDH | 37 |
| I235 | POWER | POWER | 3.3V | PP3V3_S5 | 6 |
| I766 | POWER | POWER | 3.3V | PP3V3_S5_REG_R | 70 |
| I263 | POWER | POWER | 3.3V | PPVOUT_S0_PCH_DCPSST | 22 |
| I266 | POWER | POWER | 3.3V | PPVOUT_PCH_DCPSUSBYP | |
| I262 | POWER | POWER | 3.3V | PPVOUT_G3_PCH_DCPRTC | 22 |
| I257 | POWER | POWER | 3.3V | PPVBATT_G3_RTC | 27 |
| I260 | POWER | POWER | 3.3V | PPVBATT_G3_RTC_R | 27 |
| I207 | POWER | POWER | 3.3V | PP3V3_AUDIO_SPDIF_JACK | 60 98 |
| I209 | POWER | POWER | 3.3V | PP3V3_FW_FWPHY_VDDA | 39 |
| I212 | POWER | POWER | 3.3V | PP3V3_FW_FWPHY_VP25 | 39 |
| I810 | POWER | POWER | 3.3V | PP3V3_S0_T29 | 6 |
| I816 | POWER | POWER | 3.3V | PP3V3_SW_DPAPWR | 78 84 |
| I821 | POWER | POWER | 3.3V | PP3V3_SW_DPBPWR | |
| I827 | POWER | POWER | 3.3V | PP3V3_G3H_RTC | 18 19 22 27 |
| I231 | POWER | POWER | 3.3V | PP3V3_G3H_AVREF_SMC | 46 47 |
| I236 | POWER | POWER | 3.4V | PP3V3_G3H_SMC_AVCC | 46 |
| I606 | POWER | POWER | 3.42V | PP3V42_G3H | 6 |
| I577 | POWER | POWER | 4.5V | 4V5_REG_IN | 56 |
| I234 | POWER | POWER | 4.5V | PP4V5_AUDIO_ANALOG | 56 61 |
| I670 | POWER | POWER | 4.5V | PP5V_AUDIO_HPAMP | 56 |
| I800 | POWER | POWER | 5V | PP5V_LAMP_VREG | 56 59 |
| I801 | POWER | POWER | 5V | PP5V_RAMP_VREG | 58 |
| I237 | POWER | POWER | 5V | PP5V_S0 | 6 98 |
| I239 | POWER | POWER | 5V | PP5V_S0_CPU_VCORE_VCC | 65 |
| I238 | POWER | POWER | 5V | PP5V_S0_PCH_V5REF | 24 |
| I656 | POWER | POWER | 5V | PP5V_S0_SATA_FET | 42 |
| I681 | POWER | POWER | 5V | 5V_S0_P1V05REG_VIN | 68 |
| I763 | POWER | POWER | 5V | 5V_S0_P1V05REG_VDD | 68 |
| I734 | POWER | POWER | 5V | PP5V_S3 | 6 98 |
| I733 | POWER | POWER | 5V | PP5V_S3_VREFMRGN_A | 28 |
| I245 | POWER | POWER | 5V | PP5V_S3_VREFMRGN_B | 28 |
| I242 | POWER | POWER | 5V | PP5V_S3_DDR_REG_V5FILT | 71 |
| I536 | POWER | POWER | 5V | PP5V_S3_CAMERA_FLT | 44 |
| I243 | POWER | POWER | 5V | PP5V_S3_REG_R | 70 |
| I765 | POWER | POWER | 5V | PP5V_S3_IR_FLT | 44 98 |
| I246 | POWER | POWER | 5V | PP5V_S5 | 6 |
| I244 | POWER | POWER | 5V | PP5V_S5_PCH_V5REFSUS | 24 |
| I247 | POWER | POWER | 5V | PP5V_USB_PORT0 | 43 |
| I250 | POWER | POWER | 5V | PP5V_USB_PORT0_F | 43 |
| I249 | POWER | POWER | 5V | PP5V_USB_PORT1 | 43 |
| I248 | POWER | POWER | 5V | PP5V_USB_PORT1_F | 43 |
| I251 | POWER | POWER | 5V | PP5V_USB_PORT2 | 43 |
| I252 | POWER | POWER | 5V | PP5V_USB_PORT2_F | 43 |
| I253 | POWER | POWER | 5V | PP5V_USB_PORT3 | 43 |
| I255 | POWER | POWER | 5V | PP5V_USB_PORT3_F | 43 |
| I545 | POWER | POWER | | DDR_REG_PGND | 71 |
| I546 | POWER | POWER | | DDR_REG_CSGND | 71 |
| I833 | | POWER | 3.3V | PPVDDIO_25M_B | 79 |
| I834 | | POWER | 1.05V | PPVDDIO_25M_A | 79 |
| I835 | | POWER | 3.3V | PPVDDIO_25M_C | 79 |
| I836 | | POWER | 12V | PP3V3R12V_SW_DPAPWR_R | 85 |
| I837 | | POWER | 12V | PP3V3R12V_SW_DPAPWR_D | 82 |
| I838 | | POWER | 1.5V | PP1V5_S0_DP_R | 83 |

# SENSING NET PROPERTIES

| | NET_TYPE PHYSICAL | SPACING | NET | |
|---|---|---|---|---|
| I155 | SNS_DIFF | THERMAL | VR_CPU_ISNS1_P | 65 66 |
| I156 | SNS_DIFF | THERMAL | VR_CPU_ISNS1_N | 65 66 |
| I158 | SNS_DIFF | THERMAL | VR_CPU_ISNS1_R_N | 65 |
| I160 | SNS_DIFF | THERMAL | VR_CPU_ISNS2_P | 65 66 |
| I159 | SNS_DIFF | THERMAL | VR_CPU_ISNS2_N | 65 66 |
| I163 | SNS_DIFF | THERMAL | VR_CPU_ISNS2_R_N | 65 |
| I162 | SNS_DIFF | THERMAL | VR_CPU_ISNS3_P | 65 66 |
| I164 | SNS_DIFF | THERMAL | VR_CPU_ISNS3_N | 65 66 |
| I166 | SNS_DIFF | THERMAL | VR_CPU_ISNS3_R_N | 65 |
| I788 | SNS_DIFF | THERMAL | VR_CPU_ISNS4_P | |
| I789 | SNS_DIFF | THERMAL | VR_CPU_ISNS4_N | |
| I790 | SNS_DIFF | THERMAL | VR_CPU_ISNS4_R_N | |
| I683 | SNS_DIFF | THERMAL | P1V05S0_ISN | 68 |
| I684 | SNS_DIFF | THERMAL | P1V05S0_ISP | 68 |
| I621 | SNS_DIFF | THERMAL | VR_AXG_ISNS_R_P | 65 |
| I622 | SNS_DIFF | THERMAL | VR_AXG_ISNS_R_N | 65 |
| I623 | SNS_DIFF | THERMAL | VR_AXG_ISNS_N | 65 67 |
| I625 | SNS_DIFF | THERMAL | VR_AXG_ISNS_P | 65 67 |
| I685 | SNS_DIFF | THERMAL | VR_ISNS_1V05_N | 94 |
| I686 | SNS_DIFF | THERMAL | VR_ISNS_1V05_P | 94 |
| I707 | SNS_DIFF | THERMAL | VR_ISNS_VAXG_N | 50 94 |
| I708 | SNS_DIFF | THERMAL | VR_ISNS_VAXG_P | 50 94 |
| I710 | SNS_DIFF | THERMAL | VR_ISNS_VCORE_N | 50 94 |
| I709 | SNS_DIFF | THERMAL | VR_ISNS_VCORE_P | 50 94 |
| I172 | SNS_DIFF | | CPU_VAXG_SENSE_P | 13 65 |
| I171 | SNS_DIFF | | CPU_VAXG_SENSE_N | 13 65 |
| I687 | SNS_DIFF | | VR_AXG_VSNS_R_N | 65 |
| I688 | SNS_DIFF | | VR_AXG_VSNS_R_P | 65 |
| I58 | SNS_DIFF | | VR_AXG_VSEN | 65 |
| I59 | SNS_DIFF | | VR_AXG_RGND | 65 |
| I713 | SNS_DIFF | | VR_AXG_VSNS_XW_N | 65 |
| I714 | SNS_DIFF | | VR_AXG_VSNS_XW_P | 65 |
| I615 | SNS_DIFF | | CPU_VCC_SENSE_N | 13 65 |
| I616 | SNS_DIFF | | CPU_VCC_SENSE_P | 13 65 |
| I711 | SNS_DIFF | | VR_CPU_VSEN | 65 |
| I712 | SNS_DIFF | | VR_CPU_RGND | 65 |
| I151 | SNS_DIFF | | VR_CPU_VSNS_R_N | 65 |
| I152 | SNS_DIFF | | VR_CPU_VSNS_R_P | 65 |
| I153 | SNS_DIFF | | VR_CPU_VSNS_XW_P | 65 |
| I154 | SNS_DIFF | | VR_CPU_VSNS_XW_N | 65 |
| I56 | SNS_DIFF | | CPU_VCCIO_SENSE_P | 13 68 |
| I57 | SNS_DIFF | | CPU_VCCIO_SENSE_N | 13 68 |
| I419 | SNS_DIFF | | P1V05S0_VSEN | 68 |
| I413 | SNS_DIFF | | P1V05S0_RTN | 68 |

# VR CTRL NET PROPERTIES

| | NET_TYPE PHYSICAL | SPACING | NET | |
|---|---|---|---|---|
| I278 | VR_CTL_PHY | SWITCHNODE | VR_CPU_PH1_SNUB | 66 |
| I338 | VR_CTL_PHY | SWITCHNODE | VR_CPU_PH2_SNUB | 66 |
| I339 | VR_CTL_PHY | SWITCHNODE | VR_CPU_PH3_SNUB | 66 |
| I784 | VR_CTL_PHY | SWITCHNODE | VR_CPU_PH4_SNUB | |
| I695 | VR_CTL_PHY | VR_CTL | VR_CPU_COMP | 65 |
| I694 | VR_CTL_PHY | VR_CTL | VR_AXG_TM | 65 |
| I624 | VR_CTL_PHY | VR_CTL | VR_AXG_PWM_R | 65 |
| I619 | VR_CTL_PHY | VR_CTL | VR_AXG_PWM | 65 67 |
| I620 | VR_CTL_PHY | VR_CTL | VR_CPU_PWM2 | 65 66 |
| I626 | VR_CTL_PHY | VR_CTL | VR_CPU_PWM1 | 65 66 |
| I341 | VR_CTL_PHY | VR_CTL | VR_CPU_PWM1_R | 65 |
| I343 | VR_CTL_PHY | VR_CTL | VR_CPU_PWM2_R | 65 |
| I344 | VR_CTL_PHY | VR_CTL | VR_CPU_PWM3 | 65 66 |
| I345 | VR_CTL_PHY | VR_CTL | VR_CPU_PWM3_R | 65 |
| I785 | VR_CTL_PHY | VR_CTL | VR_CPU_PWM4 | |
| I347 | VR_CTL_PHY | VR_CTL | VR_CPU_PWM4_R | 65 |
| I348 | VR_CTL_PHY | VR_CTL | VR_AXG_SW_FREQ | 65 |
| I349 | VR_CTL_PHY | VR_CTL | VR_EN_PWR_OVP | 65 |
| I350 | VR_CTL_PHY | VR_CTL | VR_RSET | 65 |
| I353 | VR_CTL_PHY | VR_CTL | VR_EN_PWR_OVP_R | 65 |
| I352 | VR_CTL_PHY | VR_CONTROL | VR_CPU_BOOT1_RC | 66 |
| I351 | VR_CTL_PHY | VR_CONTROL | VR_CPU_BOOT2_RC | 66 |
| I354 | VR_CTL_PHY | VR_CONTROL | VR_CPU_BOOT3_RC | 66 |
| I696 | VR_CTL_PHY | VR_CONTROL | VR_AXG_BOOT1_RC | 67 |
| I357 | VR_CTL_PHY | VR_CTL | VR_CPU_BOOT4_RC | |
| I359 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV1_BOOT | 66 |
| I360 | VR_CTL_PHY | VR_CTL | VR_CPU_DRV1_GDSEL | 66 |
| I363 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV1_LGATE | 66 |
| I361 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV1_UGATE | 66 |
| I365 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV2_BOOT | 66 |
| I367 | VR_CTL_PHY | VR_CTL | VR_CPU_DRV2_GDSEL | 66 |
| I368 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV2_LGATE | 66 |
| I370 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV2_UGATE | 66 |
| I371 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV3_BOOT | 66 |
| I374 | VR_CTL_PHY | VR_CTL | VR_CPU_DRV3_GDSEL | 66 |
| I376 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV3_LGATE | 66 |
| I377 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV3_UGATE | 66 |
| I780 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV4_BOOT | |
| I781 | VR_CTL_PHY | VR_CTL | VR_CPU_DRV4_GDSEL | |
| I783 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV4_LGATE | |
| I782 | VR_CTL_PHY | VR_CONTROL | VR_CPU_DRV4_UGATE | |
| I690 | VR_CTL_PHY | VR_CONTROL | VR_AXG_DRV1_BOOT | 67 |
| I691 | VR_CTL_PHY | VR_CTL | VR_AXG_DRV1_UGATE_R | 67 |
| I692 | VR_CTL_PHY | VR_CONTROL | VR_AXG_DRV1_LGATE | 67 |
| I693 | VR_CTL_PHY | VR_CONTROL | VR_AXG_DRV1_UGATE | 67 |
| I387 | VR_CTL_PHY | VR_CTL | VR_CPU_SW_FREQ | 65 |
| I388 | VR_CTL_PHY | VR_CTL | VR_CPU_FB | 65 |
| I389 | VR_CTL_PHY | VR_CTL | VR_CPU_FB_R | 65 |
| I390 | VR_CTL_PHY | VR_CTL | VR_CPU_RAMP_ADJ | 65 |
| I393 | VR_CTL_PHY | VR_CTL | VR_CPU_IMON | 50 65 |
| I635 | VR_CTL_PHY | VR_CTL | VR_CPU_SUTH | 65 |
| I637 | VR_CTL_PHY | VR_CTL | VR_CPU_N_PSI | 65 |
| I638 | VR_CTL_PHY | VR_CTL | VR_CPU_FDVID | 65 |
| I641 | VR_CTL_PHY | VR_CTL | VR_CPU_PSICOMP | 65 |
| I639 | VR_CTL_PHY | VR_CTL | VR_CPU_IAUTO | 65 |
| I642 | VR_CTL_PHY | VR_CTL | VR_CPU_PSICOMP1 | 65 |
| I645 | VR_CTL_PHY | VR_CTL | VR_CPU_PSICOMP2 | 65 |
| I644 | VR_CTL_PHY | VR_CTL | VR_CPU_FB_RC | 65 |
| I647 | VR_CTL_PHY | VR_CTL | VR_CPU_FB2 | 65 |
| I646 | VR_CTL_PHY | VR_CTL | VR_CPU_IMON_R | 65 |
| I649 | VR_CTL_PHY | VR_CTL | VR_CPU_HFREQ_COMP | 65 |
| I689 | VR_CTL_PHY | SWITCHNODE | VR_AXG_PH1_SNUB | 67 |
| I627 | VR_CTL_PHY | VR_CTL | VR_AXG_IMON | 50 65 |
| I650 | VR_CTL_PHY | VR_CTL | VR_AXG_IMON_R | 65 |
| I628 | VR_CTL_PHY | VR_CTL | VR_AXG_HFREQ_COMP | 65 |
| I630 | VR_CTL_PHY | VR_CTL | VR_AXG_FB | 65 |
| I629 | VR_CTL_PHY | VR_CTL | VR_SEN_R1 | 65 |
| I631 | VR_CTL_PHY | VR_CTL | VR_SEN_R2 | 65 |
| I634 | VR_CTL_PHY | VR_CTL | VR_SEN_R3 | 65 |
| I632 | VR_CTL_PHY | VR_CTL | VR_AXG_COMP_RC | 65 |
| I633 | VR_CTL_PHY | VR_CTL | VR_AXG_COMP | 65 |
| I636 | VR_CTL_PHY | VR_CTL | VR_AXG_TCOMP | 65 |
| I394 | VR_CTL_PHY | SWITCHNODE | P1V05S0_UGATE | 68 |
| I396 | VR_CTL_PHY | SWITCHNODE | P1V05S0_LGATE | 68 |
| I395 | VR_CTL_PHY | VR_CTL | P1V05S0_BOOT | 68 |
| I682 | VR_CTL_PHY | VR_CTL | P1V05S0_BOOT_R | 68 |
| I716 | VR_CTL_PHY | VR_CTL | P1V05_IMON | 50 68 |
| I398 | VR_CTL_PHY | VR_CTL | P1V05S0_FB | 68 |
| I399 | VR_CTL_PHY | VR_CTL | P1V05S0_PHASE_L | 68 |
| I594 | VR_CTL_PHY | VR_CTL | P1V05S0_VW | 68 |
| I403 | VR_CTL_PHY | VR_CTL | P1V05S0_COMP | 68 |
| I402 | VR_CTL_PHY | VR_CTL | P1V05S0_ICOMP | 68 |
| I401 | VR_CTL_PHY | VR_CTL | P1V05_S0_VDIFF | 68 |
| I404 | VR_CTL_PHY | VR_CTL | P1V05S0_COMP_C | 68 |
| I406 | VR_CTL_PHY | VR_CTL | P1V05S0_VDIF_C | 68 |
| I405 | VR_CTL_PHY | VR_CTL | P1V05S0_VO | 68 |
| I408 | VR_CTL_PHY | VR_CTL | P1V05S0_OCSET | 68 |
| I412 | VR_CTL_PHY | VR_CTL | P1V05S0_SNUBBER | 68 |
| I730 | VR_CTL_PHY | VR_CTL | P1V05_REG_VFB | |
| I760 | VR_CTL_PHY | VR_CTL | ENET_SR_VFB | 36 37 |
| I762 | VR_CTL_PHY | VR_CTL | P1V05S0_ISP_R | 68 |
| I805 | VR_CTL_PHY | VR_CTL | VCCSA_CNTRL_INPUT2_R | 69 95 |
| I808 | VR_CTL_PHY | VR_CTL | T29BST_FBX | |
| I607 | VR_CTL_PHY | VR_CTL | P3V42G3H_BOOST | 72 |
| I608 | VR_CTL_PHY | VR_CTL | P3V42G3H_FB | 72 |

# VR CTRL NET PROPERTIES

| | NET_TYPE PHYSICAL | SPACING | NET | |
|---|---|---|---|---|
| I437 | VR_CTL_PHY | VR_CTL | DDR_REG_CS | 71 |
| I595 | VR_CTL_PHY | VR_CTL | DDR_REG_FB | 71 |
| I439 | VR_CTL_PHY | VR_CONTROL | DDR_REG_LGATE | 71 |
| I596 | VR_CTL_PHY | VR_CONTROL | DDR_REG_UGATE | 71 |
| I443 | VR_CTL_PHY | VR_CONTROL | DDR_REG_BOOT | 71 |
| I442 | VR_CTL_PHY | VR_CONTROL | DDR_REG_BOOT_R | 71 |
| I441 | VR_CTL_PHY | VR_CTL | DDR_REG_VDDQSNS | 71 |
| I444 | VR_CTL_PHY | VR_CTL | DDR_REG_VTTSNS | 71 |
| I728 | VR_CTL_PHY | VR_CTL | DDR_REG_PHASE_R | 71 |
| I776 | VR_CTL_PHY | VR_CTL | DDR_REG_UGATE_R | 71 |
| I729 | VR_CTL_PHY | SWITCHNODE | 1V5_SNUBBER | 71 |
| I726 | VR_CTL_PHY | VR_CTL | P1V8_REG_VFB | 71 |
| I727 | VR_CTL_PHY | VR_CTL | P1V8_REG_SYNC | 71 |
| I450 | VR_CTL_PHY | VR_CONTROL | P3V3S5_REG_BOOT | 70 |
| I452 | VR_CTL_PHY | VR_CONTROL | P3V3S5_REG_BOOT_R | 70 |
| I451 | VR_CTL_PHY | VR_CTL | P3V3S5_REG_FB | 70 |
| I453 | VR_CTL_PHY | VR_CTL | P3V3S5_REG_ISEN | 70 |
| I455 | VR_CTL_PHY | VR_CONTROL | P3V3S5_REG_LGATE | 70 |
| I454 | VR_CTL_PHY | VR_CTL | P3V3S5_REG_OCSET | 70 |
| I768 | VR_CTL_PHY | VR_CONTROL | P3V3S5_REG_VOUT1 | 70 |
| I770 | VR_CTL_PHY | VR_CONTROL | P3V3S5_REG_FSET1 | 70 |
| I458 | VR_CTL_PHY | VR_CONTROL | P3V3S5_REG_UGATE | 70 |
| I457 | VR_CTL_PHY | VR_CTL | P3V3S5_REG_SNUB | 70 |
| I459 | VR_CTL_PHY | VR_CONTROL | P5VS3_REG_BOOT | 70 |
| I461 | VR_CTL_PHY | VR_CTL | P5VS3_REG_FB | 70 |
| I462 | VR_CTL_PHY | VR_CTL | P5VS3_REG_ISEN | 70 |
| I463 | VR_CTL_PHY | VR_CONTROL | P5VS3_REG_LGATE | 70 |
| I464 | VR_CTL_PHY | VR_CTL | P5VS3_REG_OCSET | 70 |
| I769 | VR_CTL_PHY | VR_CTL | P5VS3_REG_FSET2 | 70 |
| I466 | VR_CTL_PHY | VR_CONTROL | P5VS3_REG_UGATE | 70 |
| I767 | VR_CTL_PHY | VR_CONTROL | P5VS3_REG_VOUT2 | 70 |
| I718 | VR_CTL_PHY | VR_CTL | VCCSA_CNTRL_INPUT1 | 69 |
| I719 | VR_CTL_PHY | VR_CTL | VCCSA_CNTRL_INPUT2 | 69 |
| I755 | VR_CTL_PHY | VR_CTL | VCCSA_CNTRL_INPUT2_R | 69 95 |
| I720 | VR_CTL_PHY | VR_CTL | VCCSA_OUT | 69 |
| I721 | VR_CTL_PHY | VR_CTL | VCCSA_GATE | 69 |
| I830 | VR_CTL_PHY | VR_CTL | VCCSA_REF | 69 |
| I831 | VR_CTL_PHY | VR_CTL | VCCSA_CRL | 69 |
| I723 | VR_CTL_PHY | VR_CTL | CPU_VCCSA_SENSE | 13 69 |
| I791 | VR_CTL_PHY | VR_CTL | VR_CPU_TM | 65 |
| I832 | VR_CTL_PHY | PM | 3V3R2V9_DPAPWR_ADJ | 82 97 |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| VID_PHY | * | 50_OHM_SE |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| VR_CTL | * | 0.35MM | ? |

# VR VID NET PROPERTIES

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

| | NET_TYPE PHYSICAL | SPACING | NET | |
|---|---|---|---|---|
| I771 | VID_PHY | VR_CTL_VIDS | CPU_VIDSCLK_R | 13 |
| I772 | VID_PHY | VR_CTL_VIDS | CPU_VIDALERT_L_R | 13 |
| I773 | VID_PHY | VR_CTL_VIDS | CPU_VIDSOUT_R | 13 |
| I491 | VID_PHY | VR_CTL_VIDS | CPU_VIDSCLK | 13 65 |
| I492 | VID_PHY | VR_CTL_VIDS | CPU_VIDALERT_L | 13 65 |
| I521 | VID_PHY | VR_CTL_VIDS | CPU_VIDSOUT | 13 65 |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| VR_CTL_VIDS | * | =4X_DIELECTRIC | ? |


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## T29 ELECTRICAL ROUTES

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| T29_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| T29 | * | =5X_DIELECTRIC | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| T29 | TOP,BOTTOM | =7X_DIELECTRIC | ? |

## T29 PCI-EXPRESS (SAME RULE AS PCIE)

## T29 SPI INTERFACE CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| T29_SPI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| T29_SPI | * | 0.2 MM | ? |

## T29 XTAL CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| T29_XTAL_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| T29_XTAL | * | =4X_DIELECTRIC | ? |

## T29 SMBUS INTERFACE CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| T29_SMB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| T29_SMB | * | =2x_DIELECTRIC | ? |

## GREEN CLOCK CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CLK_25M_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_25M | * | =5X_DIELECTRIC | ? |

## T29 BIAS CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| T29_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| T29_COMP | * | 0.2 MM | ? |

## T29 NET PROPERTIES

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| NO_TEST=TRUE | T29_90D | T29 | T29_R2D_C_P<3..0> | 78 84 86 |
| NO_TEST=TRUE | T29_90D | T29 | T29_R2D_C_N<3..0> | 78 84 86 |
| NO_TEST=TRUE | T29_90D | T29 | T29_D2R_C_P<3..0> | 84 85 |
| NO_TEST=TRUE | T29_90D | T29 | T29_D2R_C_N<3..0> | 84 85 |
| NO_TEST=TRUE | T29_90D | T29 | T29_R2D_P<3..0> | 84 |
| NO_TEST=TRUE | T29_90D | T29 | T29_R2D_N<3..0> | 84 |
| NO_TEST=TRUE | T29_90D | T29 | T29_D2R_P<3..0> | 78 84 86 |
| NO_TEST=TRUE | T29_90D | T29 | T29_D2R_N<3..0> | 78 84 86 |
| NO_TEST=TRUE | T29_90D | T29 | T29_R2D_C_F_P<3..0> | 84 |
| NO_TEST=TRUE | T29_90D | T29 | T29_R2D_C_F_N<3..0> | 84 |
| NO_TEST=TRUE | T29_90D | T29 | T29DPA_ML_P<3..0> | 84 85 |
| NO_TEST=TRUE | T29_90D | T29 | T29DPA_ML_N<3..0> | 84 85 |
| NO_TEST=TRUE | T29_90D | T29 | T29DPB_ML_P<3..0> | |
| NO_TEST=TRUE | T29_90D | T29 | T29DPB_ML_N<3..0> | |
| NO_TEST=TRUE | T29_90D | T29 | DP_A_EXT_AUXCH_P | 84 85 |
| NO_TEST=TRUE | T29_90D | T29 | DP_A_EXT_AUXCH_N | 84 85 |
| NO_TEST=TRUE | T29_90D | T29 | DP_SDRVA_AUXCH_C_P | 84 |
| NO_TEST=TRUE | T29_90D | T29 | DP_SDRVA_AUXCH_C_N | 84 |
| NO_TEST=TRUE | T29_90D | T29 | DP_SDRVB_AUXCH_C_P | |
| NO_TEST=TRUE | T29_90D | T29 | DP_SDRVB_AUXCH_C_N | |
| NO_TEST=TRUE | T29_90D | T29 | DP_B_EXT_AUXCH_P | |
| NO_TEST=TRUE | T29_90D | T29 | DP_B_EXT_AUXCH_N | |
| NO_TEST=TRUE | T29_90D | T29 | T29DPA_D2R1_AUXCH_P | 85 |
| NO_TEST=TRUE | T29_90D | T29 | T29DPA_D2R1_AUXCH_N | 85 |
| NO_TEST=TRUE | T29_90D | T29 | T29DPB_D2R3_AUXCH_P | |
| NO_TEST=TRUE | T29_90D | T29 | T29DPB_D2R3_AUXCH_N | |
| NO_TEST=TRUE | T29_90D | T29 | T29DPA_ML_C_N<0> | 84 85 |
| NO_TEST=TRUE | T29_90D | T29 | T29DPA_ML_C_P<0> | 84 85 |
| NO_TEST=TRUE | T29_90D | T29 | T29DPA_ML_C_N<2> | 84 85 |
| NO_TEST=TRUE | T29_90D | T29 | T29DPA_ML_C_P<2> | 84 85 |
| NO_TEST=TRUE | T29_90D | T29 | T29DPB_ML_C_N<0> | |
| NO_TEST=TRUE | T29_90D | T29 | T29DPB_ML_C_P<0> | |
| NO_TEST=TRUE | T29_90D | T29 | T29DPB_ML_C_N<2> | |
| NO_TEST=TRUE | T29_90D | T29 | T29DPB_ML_C_P<2> | |
| NO_TEST=TRUE | PCIE_85D | PCIE | PCIE_T29_R2D_P<3..0> | 86 |
| NO_TEST=TRUE | PCIE_85D | PCIE | PCIE_T29_R2D_N<3..0> | 86 |
| NO_TEST=TRUE | PCIE_85D | PCIE | PCIE_T29_R2D_C_P<3..0> | 18 86 |
| NO_TEST=TRUE | PCIE_85D | PCIE | PCIE_T29_R2D_C_N<3..0> | 18 86 |
| NO_TEST=TRUE | PCIE_85D | PCIE | PCIE_T29_D2R_P<3..0> | 18 86 |
| NO_TEST=TRUE | PCIE_85D | PCIE | PCIE_T29_D2R_N<3..0> | 18 86 |
| NO_TEST=TRUE | PCIE_85D | PCIE | PCIE_T29_D2R_C_P<3..0> | 86 |
| NO_TEST=TRUE | PCIE_85D | PCIE | PCIE_T29_D2R_C_N<3..0> | 86 |
| NO_TEST=TRUE | CLK_PCIE_90D | CLK_PCIE | PCIE_CLK100M_T29_P | 18 86 |
| NO_TEST=TRUE | CLK_PCIE_90D | CLK_PCIE | PCIE_CLK100M_T29_N | 18 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SRC_ML_C_P<3..0> | 83 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SRC_ML_C_N<3..0> | 83 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SRC_ML_P<3..0> | 83 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SRC_ML_N<3..0> | 83 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK0_ML_P<3..0> | 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK0_ML_N<3..0> | 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK0_AUXCH_P | 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK0_AUXCH_N | 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK0_ML_C_P<3..0> | 78 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK0_ML_C_N<3..0> | 78 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK0_AUXCH_C_P | 78 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK0_AUXCH_C_N | 78 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK1_ML_P<3..0> | 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK1_ML_N<3..0> | 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK1_AUXCH_P | 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK1_AUXCH_N | 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK1_ML_C_P<3..0> | 78 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK1_ML_C_N<3..0> | 78 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK1_AUXCH_C_P | 78 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SNK1_AUXCH_C_N | 78 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SRC_AUXCH_R_C_P | 83 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SRC_AUXCH_R_C_N | 83 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SRC_AUXCH_C_P | 83 86 |
| NO_TEST=TRUE | DP_85D | DISPLAYPORT | DP_T29SRC_AUXCH_C_N | 83 86 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVA_AUXCH_P | 84 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVA_AUXCH_N | 84 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVB_AUXCH_P | |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVB_AUXCH_N | |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVA_ML_C_P<3..0> | 84 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVA_ML_C_N<3..0> | 84 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVA_ML_P<3..0> | 84 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVA_ML_N<3..0> | 84 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVA_ML_R_P<3..0> | 84 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVA_ML_R_N<3..0> | 84 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVB_ML_C_P<3..0> | |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVB_ML_C_N<3..0> | |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVB_ML_P<3..0> | |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVB_ML_N<3..0> | |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVB_ML_R_P<3..0> | |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | DP_SDRVB_ML_R_N<3..0> | |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | T29_A_RSVD_N | 84 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | T29_A_RSVD_P | 84 |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | T29_B_RSVD_N | |
| NO_TEST=TRUE | T29_90D | DISPLAYPORT | T29_B_RSVD_P | |

## T29 NET PROPERTIES

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|---|
| | T29_SPI_55S | T29_SPI | JTAG_T29_TDI | 15 21 86 |
| | T29_SPI_55S | T29_SPI | JTAG_T29_TMS | 15 18 86 |
| | T29_SPI_55S | T29_SPI | JTAG_T29_TCK | 15 21 25 86 |
| | T29_SPI_55S | T29_SPI | JTAG_T29_TDO | 15 21 86 |
| | T29_SPI_55S | T29_SPI | T29_SPI_MOSI | 86 |
| | T29_SPI_55S | T29_SPI | T29_SPI_MISO | 86 |
| | T29_SPI_55S | T29_SPI | T29_SPI_CS_L | 86 |
| | T29_SPI_55S | T29_SPI | T29_SPI_CLK | 86 |
| | CLK_25M_55S | CLK_25M | SYSCLK_CLK25M_T29 | 79 86 96 |
| | CLK_25M_55S | CLK_25M | SYSCLK_CLK25M_T29_R | 86 96 |
| | T29_SMB_55S | T29_SMB | I2C_T29_SDA | 49 86 |
| | T29_SMB_55S | T29_SMB | I2C_T29_SCL | 49 86 |
| | CLK_25M_55S | CLK_25M | SYSCLK_CLK25M_SB | 79 |
| | CLK_25M_55S | CLK_25M | SYSCLK_CLK25M_ENET | 79 |
| | CLK_25M_55S | CLK_25M | ENET_CLK25M_XTALI_OSC | 36 79 |
| | CLK_25M_55S | CLK_25M | SYSCLK_CLK25M_T29_CLK | 79 |
| | CLK_25M_55S | CLK_25M | SYSCLK_CLK25M_T29 | 79 86 96 |
| | CLK_25M_55S | CLK_25M | SYSCLK_CLK25M_T29_R | 86 96 |
| | T29_XTAL_100D | T29_XTAL | SYSCLK_CLK25M_X2 | 79 |
| | T29_XTAL_100D | T29_XTAL | SYSCLK_CLK25M_X2_R | 79 |
| | T29_XTAL_100D | T29_XTAL | SYSCLK_CLK25M_X1 | 79 |
| | T29_55S | T29_COMP | T29_RSENSE | 86 |
| | T29_55S | T29_COMP | T29_RBIAS | 86 |
| | | T29_COMP | T29_A_BIAS | 82 84 85 |
| | | T29_COMP | T29_B_BIAS | |
| | | T29_COMP | DP_A_BIAS | 84 |

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# T29 CONSTRAINTS

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# PM NET PROPERTIES
# (PM, RESET, EN, PGOOD)

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| PM | * | * | 2:1_SPACING |
| PM_VTT | PM_VTT | * | 2:1_SPACING |
| PM_VTT | * | * | 3:1_SPACING |
| PM_VTT | GND | * | DEFAULT |
| PM | GND | * | DEFAULT |

| PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|
| I357 | PM | 4V5_REG_EN | 56 |
| I358 | PM | 3V42G3H_SHDN_L | 72 |
| I359 | PM | ALL_SYS_PWRGD_R | 5 32 64 |
| I360 | PM | ALL_SYS_PWRGD_SMC | 46 64 |
| I361 | PM | AP_PWR_EN | 20 25 33 |
| I362 | PM | AP_MINI_RESET_L | 33 |
| I363 | PM | AUD_I2C_INT_L | 20 62 |
| I364 | PM | AUD_IP_PERIPHERAL_DET | 20 61 |
| I365 | PM | AUD_IPHS_SWITCH_EN | 21 62 |
| I366 | PM | AUD_SPDIF_IN | 60 83 91 |
| I367 | PM | AUD_SPDIF_IN_CODEC | 56 83 |
| I368 | PM | BDV_BKL_PWM | 46 83 97 |
| I369 | PM | BL_PWM | 6 83 |
| I370 | PM | BL_EN | 6 81 |
| I371 | PM | BDV_BKL_PWM | 46 83 97 |
| I368 | PM | CK505_27MHZ_EN | 26 |
| I369 | PM | CPUVTT_REG_EN | |
| I370 | PM_VTT | CPUVTT_REG_PGOOD_R | 63 |
| I371 | PM | CPU_MEM_RESET_L | 11 32 |
| I372 | PM | CPU_PECI_R | 46 |
| I373 | PM_VTT | CPU_PWRGD | 11 21 25 |
| I374 | PM | CPU_RESET_L | 11 27 |
| I375 | PM | CPU_SKTOCC_L | 11 63 |
| I376 | PM | CPU_CATERR_L | 11 |
| I377 | PM | CPU_PECI | 11 21 46 |
| I378 | PM | CPU_PROCHOT_L | 11 47 65 |
| I379 | PM | CPU_THRMTRIP_L | 11 47 |
| I380 | PM | CPU_PROC_SEL | 11 19 |
| I381 | PM | DEBUG_RESET_L | 27 48 |
| I382 | PM | DDRVTT_EN | |
| I383 | PM | DP_INT_SPDIF_AUDIO | 81 83 |
| I384 | PM | DP_INTPNL_HPD | 81 83 |
| I385 | PM | 3V3R2V9_DPAPWR_ADJ | 82 95 |
| I386 | PM | DP_A_PWRDWN | 84 |
| I387 | PM | DP_A_PWRDWN_FET_R | 82 |
| I388 | PM | DP_A_PWRDWN_INV | 82 |
| I389 | PM | DPAPWRSW_HVEN_L_R | 82 |
| I390 | PM | DPAPWRSW_CT | 82 |
| I391 | PM | DPAPWRSW_ILIM | 82 |
| I392 | PM | DPAPWRSW_IFLT | 82 |
| I393 | PM | T29_A_HV_EN | 82 84 |
| I394 | PM | 3V3R2V9_DPBPWR_ADJ | |
| I395 | PM | DP_B_PWRDWN | |
| I396 | PM | DP_B_PWRDWN_FET_R | |
| I397 | PM | DP_B_PWRDWN_INV | |
| I398 | PM | DPBPWRSW_HVEN_L_R | |
| I399 | PM | DPBPWRSW_CT | |
| I400 | PM | DPBPWRSW_ILIM | |
| I401 | PM | DPBPWRSW_IFLT | |
| I402 | PM | T29_B_HV_EN | |
| I403 | PM | T29_PWR_EN | 18 80 97 |
| I404 | PM | T29_RESET_RTR_L | 80 86 |
| I405 | PM | LCD_BL_FILT | 83 |
| I406 | PM | LCD_BLK_ON_DLY | |
| I407 | PM | LCD_BL_PWM | 83 |
| I408 | PM | MXM_PNL_BL_PWM | 76 83 |

| PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|
| I225 | PM | ENET_PWR_EN | 20 25 36 |
| I227 | PM | ENET_LOW_PWR | 15 21 37 |
| I229 | PM | FW_RESET_L | 27 39 |
| I231 | PM | ENET_RESET_L | 27 36 |
| I233 | PM | FW_PME_L | 15 21 39 |
| I237 | PM | FW_PWR_EN | 15 21 |
| I235 | PM | FW_CLKREQ_L | 15 39 |
| I240 | PM | ISOLATE_CPU_MEM_L | 21 25 32 |
| I266 | PM | LPC_PWRDWN_L | 19 46 48 |
| I268 | PM | MEM_RESET_L | 30 31 32 89 |
| I269 | PM | MINI_CLKREQ_L | 15 33 |
| I270 | PM | MINI_RESET_L | 27 33 |
| I268 | PM | MXM_CLKREQ_L | 9 75 |
| I267 | PM | MXM_GOOD | 5 21 25 |
| I272 | PM | ODD_PWR_EN_L | 15 21 42 |
| I68 | PM | RTC_RESET_L | 18 27 97 |
| I48 | PM | RSMRST_PWRGD | 46 64 |
| I67 | PM | RTC_RESET_L | 18 27 97 |
| I310 | PM | S4_ENABLES | 63 |
| I260 | PM | SDCONN_STATE_RST_L | |
| I261 | PM | SDCONN_DETECT_BUF_L | 92 |
| I262 | PM | SDCONN_STATE_CHANGE | 20 25 45 |
| I263 | PM | SDCARD_RESET | 15 21 44 98 |
| I314 | PM | SDCARD_RESET_L | 44 |
| I315 | PM | SDCARD_PLT_RST_L | 27 44 |
| I316 | PM | SDCARD_PLT_RST_L_R | |
| I153 | PM | SMC_PM_G2_EN | 46 74 |
| I152 | PM | SMC_PM_G2_EN_R | 74 |
| I154 | PM | SMC_PM_G2_EN_L | 74 |
| I155 | PM | S5_DG_1 | 74 |
| I156 | PM | S5_MSFT_G1 | 74 |
| I415 | PM | USE_HDD_OOB_L | 20 51 |
| I416 | PM | HDD_OOB_1V00_REF | 51 |
| I417 | PM | SMC_ADAPTER_EN | 19 46 47 |
| I418 | PM | SMC_RUNTIME_SCI_L | 21 46 47 |
| I419 | PM | SMC_WAKE_SCI_L | 15 18 21 46 |
| I420 | PM | SMC_DELAYED_PWRGD | 47 64 |
| I421 | PM | SMC_LRESET_L | 27 46 |
| I422 | PM | SMC_RESET_L | 46 47 48 |
| I423 | PM | SMC_PROCHOT | 46 47 |
| I424 | PM | SMC_PROCHOT_3_3_L | 46 47 |
| I425 | PM | SMC_ONOFF_L | 46 47 |
| I426 | PM | SMC_MANUAL_RST_L | 47 |
| I299 | PM | SPI_DESCRIPTOR_OVERRIDE_L | 18 46 |
| I413 | PM | T29_PWR_EN | 18 80 97 |
| I409 | PM | T29_RESET_L | 27 80 |
| I410 | PM | T29_DP_PORTA_PWR_EN | 20 25 82 91 |
| I411 | PM | T29_DP_PORTA_PWR_EN_REG | 82 |
| I265 | PM_VTT | XDP_CPUPWRGD | |
| I264 | PM_VTT | XDP_DBRESET_L | 11 25 |
| I429 | PM_VTT | XDP_PWRGD | |
| I428 | PM | XDPPCH_PLTRST_L | 25 27 |
| I427 | PM | USB_HUB_SOFT_RESET_L | 20 25 34 |
| I182 | PM | VSYNC_DP_CONN | 6 81 |
| I183 | PM | VSYNC_DP | 81 |
| I184 | PM | VIDEO_ON | 81 |
| I844 | PM | VTT_REG_PGOOD_L | 63 |

| PHYSICAL | NET_TYPE SPACING | | |
|---|---|---|---|
| I272 | PM | PLT_RESET_L | 20 27 |
| I412 | PM_VTT | PLT_RESET_LS1V05_L | 11 |
| I273 | PM | PM_BATLOW_L | 15 19 46 |
| I274 | PM | PM_CLK32K_SUSCLK | 9 46 91 |
| I275 | PM | PM_CLK32K_SUSCLK_R | 9 19 91 |
| I277 | PM | PM_CLKRUN_L | 15 19 46 48 |
| I278 | PM | PM_PWRBTN_L | 19 25 46 |
| I279 | PM | PM_RSMRST_L | 27 46 |
| I276 | PM | PM_RSMRST_PCH_L | 19 27 |
| I138 | PM | PCH_SRTCRST_L | 18 |
| I137 | PM | PCH_INTVRMEN_L | 18 |
| I141 | PM | PCH_DSWVRMEN | 19 |
| I139 | PM | PCH_DF_TVS | 19 |
| I152 | PM | PCH_PROCPWRGD | 21 |
| I143 | PM | PCIE_WAKE_L | 19 33 36 78 |
| I142 | PM | PM_DSW_PWRGD | 19 |
| I140 | PM | PM_ASW_PWRGD | 19 64 |
| I150 | PM | PM_MEM_PWRGD_R | 11 |
| I160 | PM | PM_EN_DDR1V5_S3_REG | 63 71 |
| I167 | PM | PM_EN_DDRVTT_S0_REG | 32 63 71 |
| I168 | PM | PM_EN_P12V_S0_FET | 6 63 |
| I169 | PM | PM_EN_P1V05_S0_REG | 63 68 |
| I170 | PM | PM_EN_P1V05_S3_REG | |
| I174 | PM | PM_EN_P1V5_S0_FET | 63 73 |
| I172 | PM | PM_EN_P1V8_S0_REG | 63 71 |
| I173 | PM | PM_EN_P3V3_S0_FET | 63 73 |
| I175 | PM | PM_EN_P3V3_S3_FET | 63 73 |
| I171 | PM | PM_EN_P3V3_S5_REG | 70 |
| I176 | PM | PM_EN_P5V_S0_FET | 63 73 |
| I177 | PM | PM_EN_P5V_S3_REG | 63 70 |
| I178 | PM | PM_EN_PVCCSA_S0_REG_L | 64 |
| I820 | PM | PM_EN_VCCSA_S0_CPU | |
| I179 | PM | PM_EN_PVCORE_CPU | 63 65 |
| I180 | PM_VTT | PM_MEM_PWRGD | 11 19 97 |
| I181 | PM | PM_MXM_EN | 64 76 |
| I182 | PM | PM_PCH_PWRGD_R | 64 |
| I183 | PM | PM_PECI_PWRGD | 46 64 |
| I185 | PM | PM_PECI_PWRGD_R | 46 |
| I186 | PM | PM_PGOOD_DDR1V5_S3_REG | 5 63 71 |
| I187 | PM | PM_PGOOD_P1V05_S0_REG | 63 64 68 |
| I188 | PM | PM_PGOOD_P1V5_S0_FET | 11 64 73 |
| I189 | PM | PM_PGOOD_P1V8_S0_REG | 64 71 |
| I190 | PM | PM_PGOOD_P3V3_S0_FET | 63 64 73 |
| I191 | PM | PM_PGOOD_P3V3_S3_FET | 34 73 |
| I192 | PM | PM_PGOOD_P3V3_S5_REG | 27 64 70 |
| I193 | PM | PM_PGOOD_P5V_S0_FET | 63 64 73 |
| I194 | PM | PM_PGOOD_MINI | 33 |
| I195 | PM | PM_PGOOD_PVCORE_CPU | 5 25 64 65 |
| I196 | PM | PM_PGOOD_PVCCSA_S0_REG | 63 64 |
| I198 | PM | PM_PGOOD_P5V_S3_REG | 63 70 82 |
| I197 | PM | PM_PGOOD_PVAXG | 5 65 |
| I257 | PM_VTT | PM_MEM_PWRGD | 11 19 97 |
| I144 | PM | PM_MEM_PWRGD_L | 11 |
| I256 | PM | PM_MXM_PGOOD | 64 76 |
| I258 | PM | PM_PCH_PWRGD | 19 21 64 |
| I202 | PM | PM_SLP_S3_5V | 32 |
| I203 | PM | PM_SLP_S3_5V_L | 32 |
| I204 | PM | PM_SLP_S3_5V_R2 | 32 |
| I205 | PM | PM_SLP_S3_L | 5 19 26 32 36 46 47 63 82 |
| I206 | PM | PM_SLP_S4_L | 5 19 32 46 47 63 97 |
| I208 | PM | PM_SLP_S5_L | 5 19 46 47 63 |
| I207 | PM_VTT | PM_SYNC | 11 19 |
| I209 | PM | PM_SYSRST_L | 19 25 27 46 |
| I180 | PM | PM_SYS_PWRGD | 19 32 64 |
| I301 | PM_VTT | PM_THRMTRIP_L | 21 47 |
| I302 | PM | PM_SLP_S3_BUF_L | 63 |
| I303 | PM | PM_SLP_S4_1_L_R | 63 |
| I304 | PM | PM_SLP_S4_D_L | 32 |
| I305 | PM | PM_SLP_S4_L | 5 19 32 46 47 63 97 |
| I848 | PM | PGOOD_P1V5_S0_DLY | 11 |
| I307 | PM | PGOOD_1V8_S0_G1 | 64 |
| I308 | PM | PGOOD_1V8_S0_G2 | 64 |
| I309 | PM | PGOOD_P12V_S0 | 63 64 |
| I310 | PM | PGOOD_P1V8_S0 | 64 |
| I311 | PM | PGOOD_PCH_S0 | 5 64 |
| I312 | PM | PGOOD_PCH_S0_R | 64 91 |
| I313 | PM | PGOOD_SYSPWROK | 64 |
| I314 | PM | PGOOD_SYSPWROK_R | 64 |
| I315 | PM | POWER_BUTTON_L | 47 |
| I316 | PM | PEG_RESET_L | 9 27 |
| I431 | PM | PGOOD_CPU_S0 | 64 |
| I432 | PM | PGOOD_CPU_UNCORE | 64 91 |
| I433 | PM | PGOOD_5V_1V05_3V3 | 64 91 |
| I434 | PM | PGOOD_3V3_1V05 | 64 91 |
| I435 | PM | PGOOD_12V_S0_G1 | 64 |
| I436 | PM | PGOOD_12V_S0_G2 | 64 |
| I437 | PM | 9V_COMP_REF | 64 |
| I438 | PM | 12V_COMP_REF | 64 |
| I439 | PM | ALL_SYS_PWRGD | 64 91 |

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PM RESETS ENABLES PGOOD CONST

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# FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

## J4700 USB CAMERA

95 6 IN PP5V_S3 FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
92 44 IN USB_CAMERA_L_P FUNC_TEST=TRUE
92 44 IN USB_CAMERA_L_N FUNC_TEST=TRUE
92 44 IN USB_BT_L_P FUNC_TEST=TRUE
92 44 IN USB_BT_L_N FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
1 PP3V3_S3 TESTPOINT NEAR J4700
6 GROUND TESTPOINTS NEAR J4700

## J4750 USB CARD READER

97 44 21 15 IN SDCARD_RESET FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

## J4780 IR BOARD

92 44 IN USB_IR_L_P FUNC_TEST=TRUE
92 44 IN USB_IR_L_N FUNC_TEST=TRUE
95 44 IN PP5V_S3_IR_FLT FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J4780

## J4520 SATA ODD (HIGH SPEED)

46 42 IN SMC_ODD_DETECT FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
1 GROUND TESTPOINTS NEAR J4520

## J5551 ODD TEMP SENSOR

94 52 IN SNS_ODD_P FUNC_TEST=TRUE
94 52 IN SNS_ODD_N FUNC_TEST=TRUE

## J5600 ODD FAN

53 IN FAN_0_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH0_L FUNC_TEST=TRUE
95 53 IN PP12V_S0_FAN0_L FUNC_TEST=TRUE
53 IN FAN_0_GND FUNC_TEST=TRUE

## J5700 CPU FAN

54 IN FAN_2_PWR_L FUNC_TEST=TRUE
54 IN FAN_TACH2_L FUNC_TEST=TRUE
95 54 IN PP12V_S0_FAN2_L FUNC_TEST=TRUE
54 IN FAN_2_GND FUNC_TEST=TRUE
94 54 52 IN SNS_AMB_P FUNC_TEST=TRUE
94 54 52 IN SNS_AMB_N FUNC_TEST=TRUE

1 GROUND TESTPOINT NEAR J5700

## J5601 HD FAN

53 IN FAN_1_PWR_L FUNC_TEST=TRUE
53 IN FAN_TACH1_L FUNC_TEST=TRUE
95 53 IN PP12V_S0_FAN1_L FUNC_TEST=TRUE
53 IN FAN_1_GND FUNC_TEST=TRUE

## J5400 HDD TEMP SENSOR

94 51 42 IN HDD_OOB_TEMP_FILT FUNC_TEST=TRUE

1 GROUND TESTPOINTS NEAR J5400

## J5560 SKIN TEMP SENSOR

94 52 44 IN SNS_SKIN_LEFT_P FUNC_TEST=TRUE
94 52 44 IN SNS_SKIN_LEFT_N FUNC_TEST=TRUE
94 52 IN SNS_SKIN_RIGHT_P FUNC_TEST=TRUE
94 52 IN SNS_SKIN_RIGHT_N FUNC_TEST=TRUE

## J6602 AUDIO RIGHT SPEAKER

91 IN AUD_SPKR_OUTLO2R_POUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO2R_NOUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO1R_POUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO1R_NOUT FUNC_TEST=TRUE

## J6603 AUDIO LEFT SPEAKER

91 IN AUD_SPKR_OUTLO2L_POUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO2L_NOUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO1L_POUT FUNC_TEST=TRUE
91 IN AUD_SPKR_OUTLO1L_NOUT FUNC_TEST=TRUE

## J6600 AUDIO AUXILIARY CONNECTOR

2 TP'S

95 60 IN PP3V3_AUDIO_SPDIF_JACK FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
60 IN AUD_LI_DET_JACK FUNC_TEST=TRUE
60 IN AUD_LI_R_JACK FUNC_TEST=TRUE
60 IN AUD_LI_GND_JACK FUNC_TEST=TRUE
60 IN AUD_LI_L_JACK FUNC_TEST=TRUE
60 IN HS_MIC_HI_JACK FUNC_TEST=TRUE
60 IN AUD_HP_L_JACK FUNC_TEST=TRUE
60 IN AUD_HP_GND_JACK FUNC_TEST=TRUE
60 IN AUD_HP_R_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TYPEDET_JACK FUNC_TEST=TRUE
60 IN AUD_IP_PERPH_JACK FUNC_TEST=TRUE
60 IN AUD_HP_TIPDET_JACK FUNC_TEST=TRUE
60 IN AUD_SPDIFIN_JACK FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J6600

GND 17 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=17

95 6 IN PP3V3_S3 2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2

95 6 IN PP5V_S0 FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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