

# Compal Confidential

## ICL50/51, ICK70/71 Schematics Document

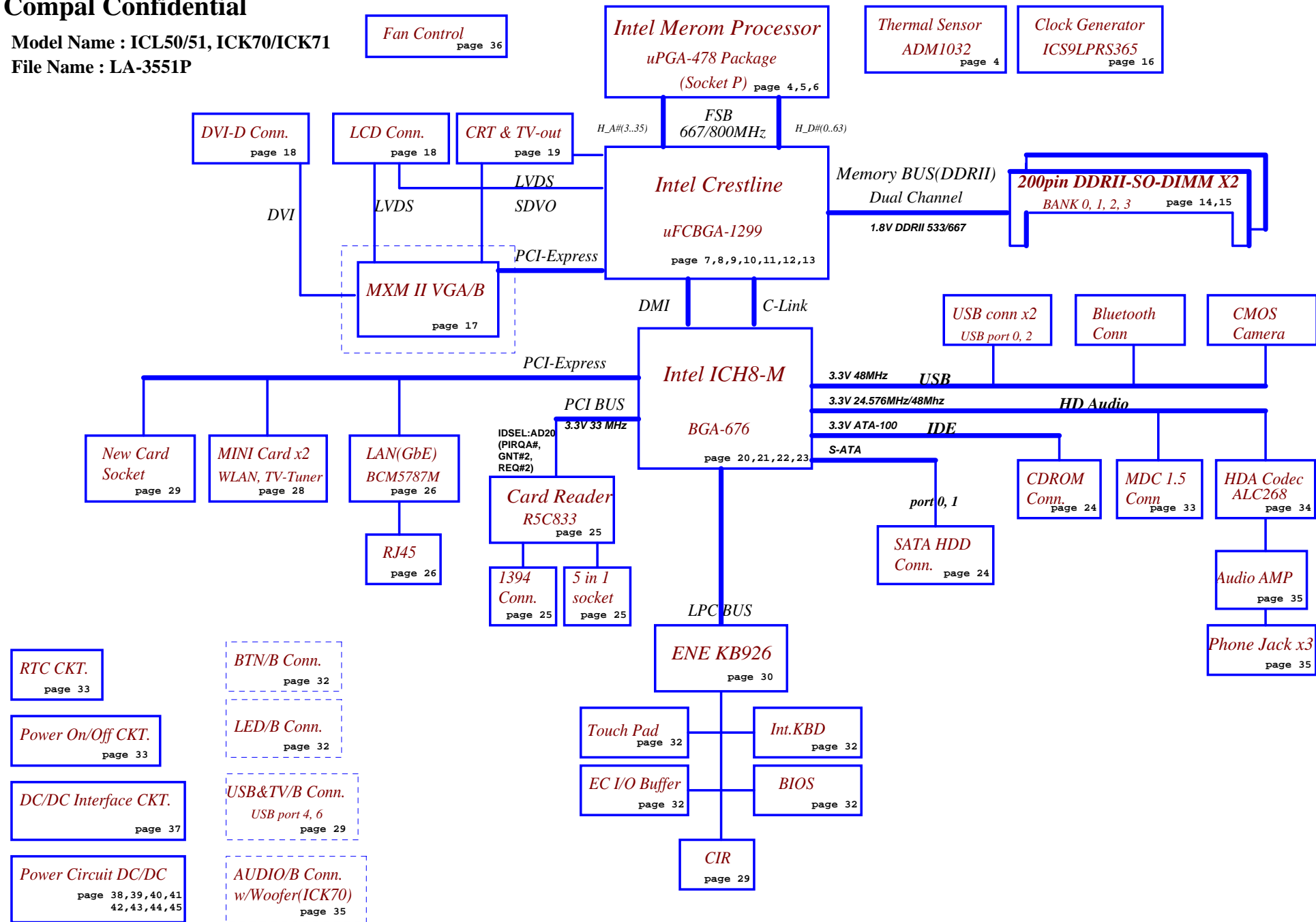
Intel Merom Processor with Crestline(PM965/GM965) + DDRII + ICH8M  
(With ATI MXM/B)

2007-4-20

REV:1A

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Issued Date	2007/04/04	Deciphered Date	2008/04/04	Title	Cover Page
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				ICL50/ICK70 M/B LA-3551P Schematic	
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**Model Name : ICL50/51, ICK70/ICK71**  
**File Name : LA-3551P**



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Issued Date	2006/12/25	Deciphered Date	2007/12/25	Title	Block Diagrams
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394/Card Reader	AD16	0	PIRQE PIRQG

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

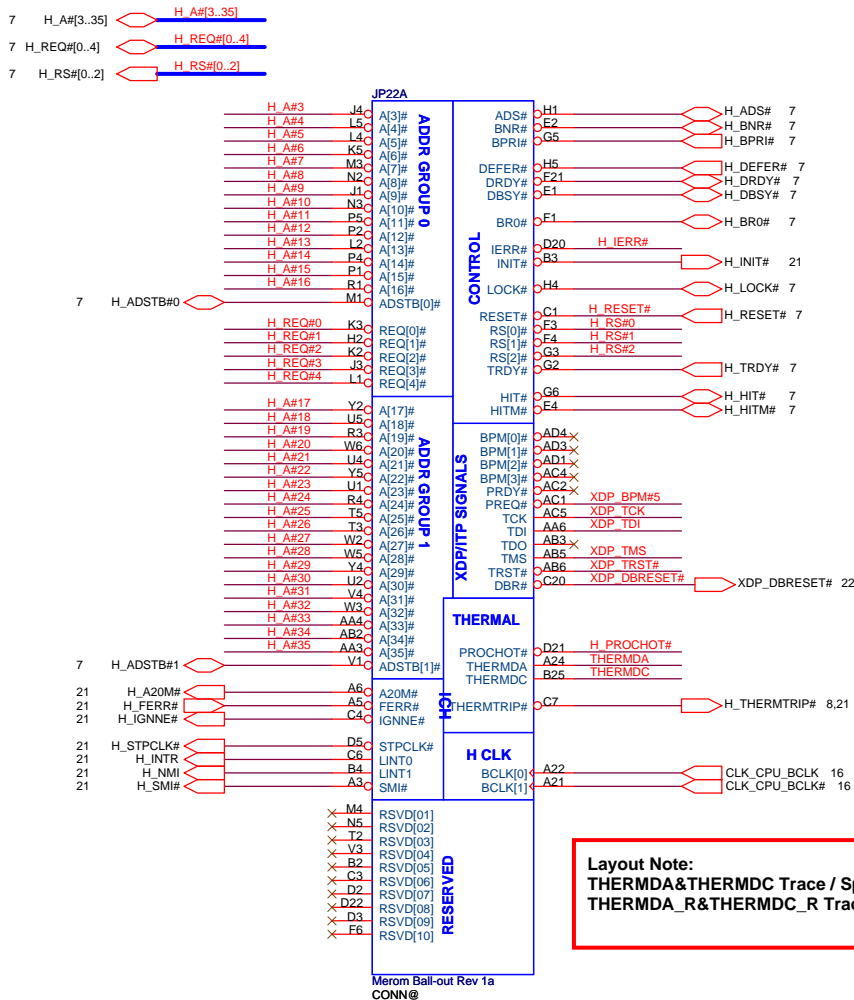
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

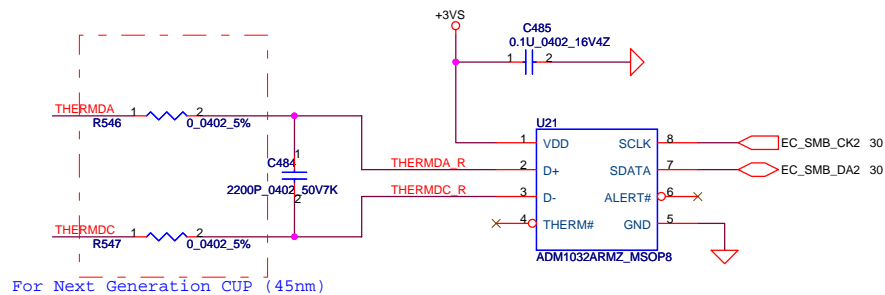
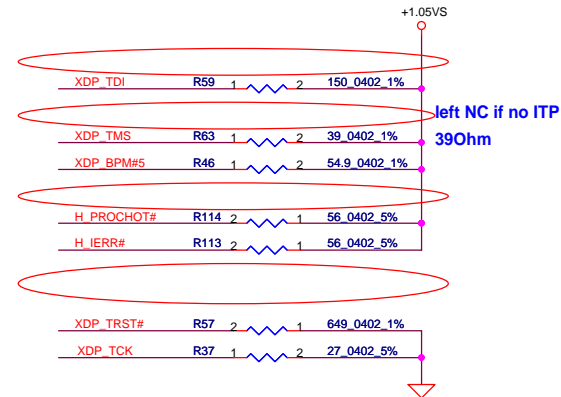
BTO Item	BOM Structure
Discrete	PM@
UMA	GM@

EC SM Bus2 address



Layout Note:  
THERMDA&THERMDC Trace / Space = 10 / 10 mil  
THERMDA\_R&THERMDC\_R Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	1	0	200
0	1	1	166

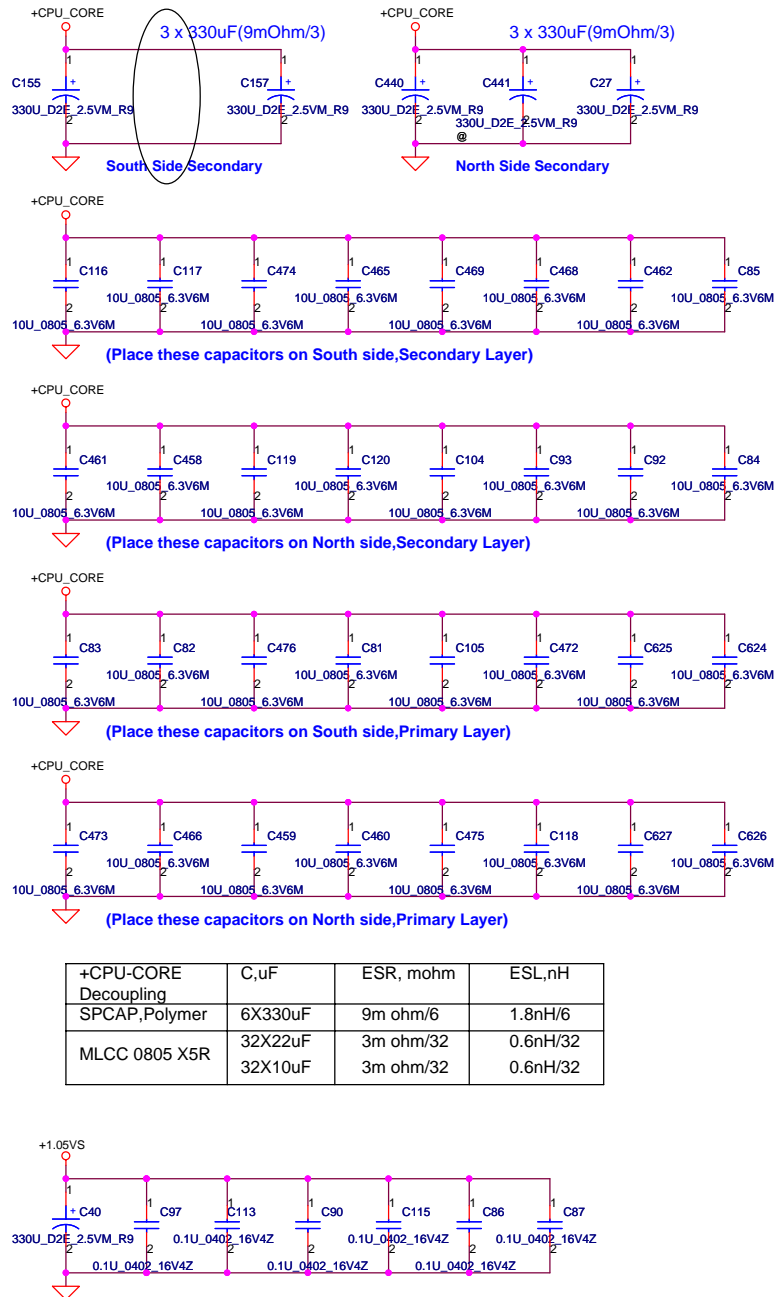


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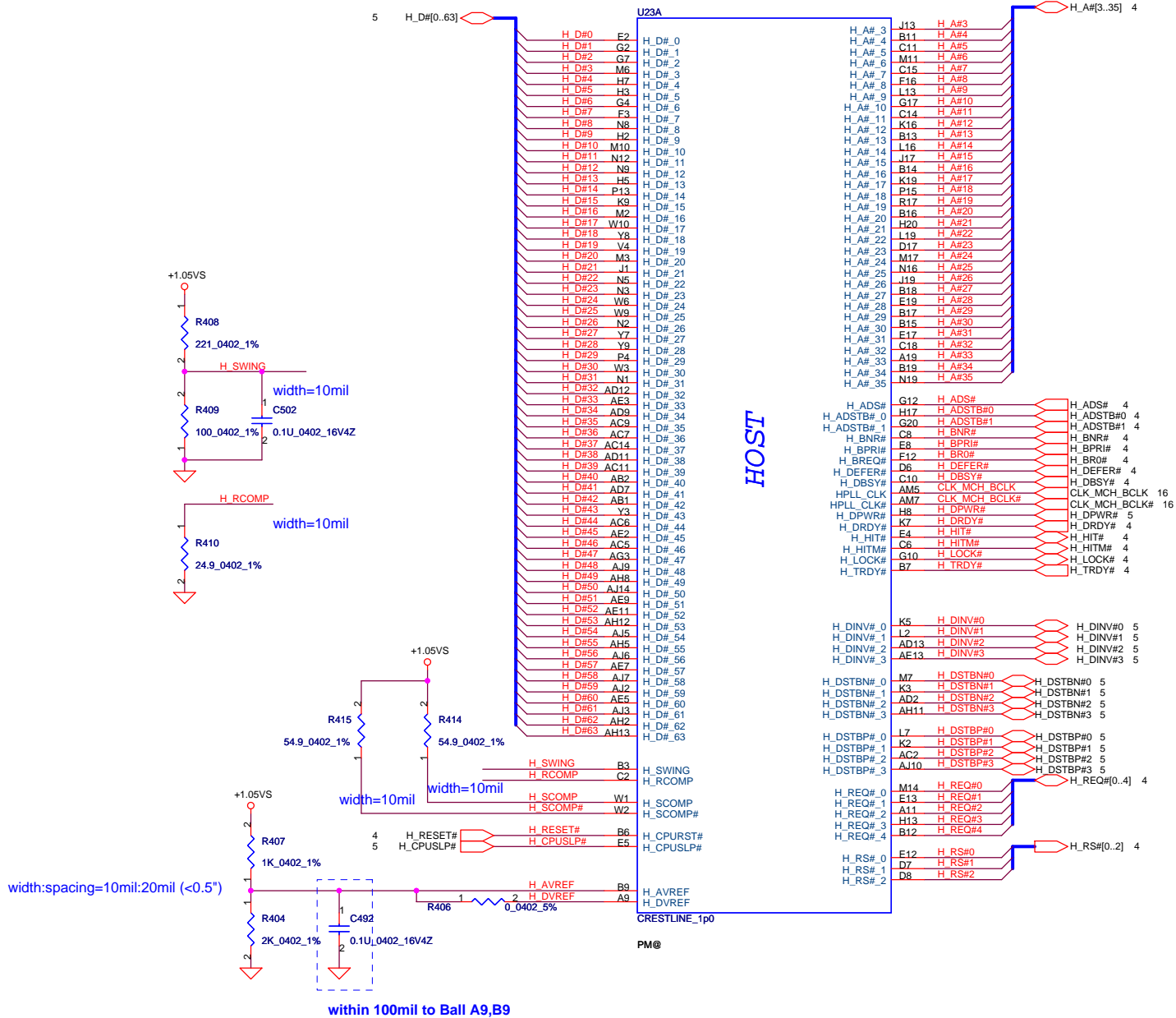


JP22D			
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA5
D11	VSS[029]	VSS[110]	AA8
D16	VSS[030]	VSS[111]	AA11
D19	VSS[031]	VSS[112]	AA14
D23	VSS[032]	VSS[113]	AA16
D26	VSS[033]	VSS[114]	AA19
E3	VSS[034]	VSS[115]	AA22
E6	VSS[035]	VSS[116]	AA25
E8	VSS[036]	VSS[117]	AB1
E11	VSS[037]	VSS[118]	AB4
E14	VSS[038]	VSS[119]	AB8
E16	VSS[039]	VSS[120]	AB11
E19	VSS[040]	VSS[121]	AB13
E21	VSS[041]	VSS[122]	AB16
E24	VSS[042]	VSS[123]	AB19
F5	VSS[043]	VSS[124]	AB23
F8	VSS[044]	VSS[125]	AB26
F11	VSS[045]	VSS[126]	AC3
F13	VSS[046]	VSS[127]	AC6
F16	VSS[047]	VSS[128]	AC8
F19	VSS[048]	VSS[129]	AC11
F2	VSS[049]	VSS[130]	AC14
F22	VSS[050]	VSS[131]	AC16
F25	VSS[051]	VSS[132]	AC19
G4	VSS[052]	VSS[133]	AC21
G1	VSS[053]	VSS[134]	AC24
G23	VSS[054]	VSS[135]	AD2
G26	VSS[055]	VSS[136]	AD5
H3	VSS[056]	VSS[137]	AD8
H6	VSS[057]	VSS[138]	AD11
H21	VSS[058]	VSS[139]	AD13
H24	VSS[059]	VSS[140]	AD16
J2	VSS[060]	VSS[141]	AD19
J5	VSS[061]	VSS[142]	AD22
J22	VSS[062]	VSS[143]	AD25
J25	VSS[063]	VSS[144]	AE1
K1	VSS[064]	VSS[145]	AE4
K4	VSS[065]	VSS[146]	AE8
K23	VSS[066]	VSS[147]	AE11
K26	VSS[067]	VSS[148]	AE14
L3	VSS[068]	VSS[149]	AE16
L6	VSS[069]	VSS[150]	AE19
L21	VSS[070]	VSS[151]	AE23
L24	VSS[071]	VSS[152]	AE26
M2	VSS[072]	VSS[153]	A2
M5	VSS[073]	VSS[154]	AF6
M22	VSS[074]	VSS[155]	AF8
M25	VSS[075]	VSS[156]	AF11
N1	VSS[076]	VSS[157]	AF13
N4	VSS[077]	VSS[158]	AF16
N23	VSS[078]	VSS[159]	AF19
N26	VSS[079]	VSS[160]	AF21
P3	VSS[080]	VSS[161]	A25
	VSS[081]	VSS[162]	AF25
		VSS[163]	

Merom Ball-out Rev 1a  
CONN@



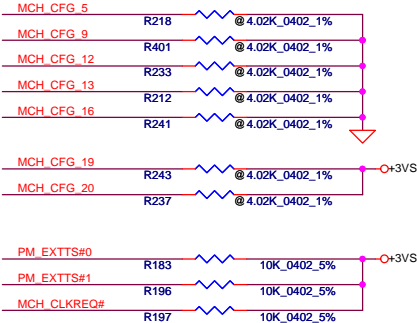
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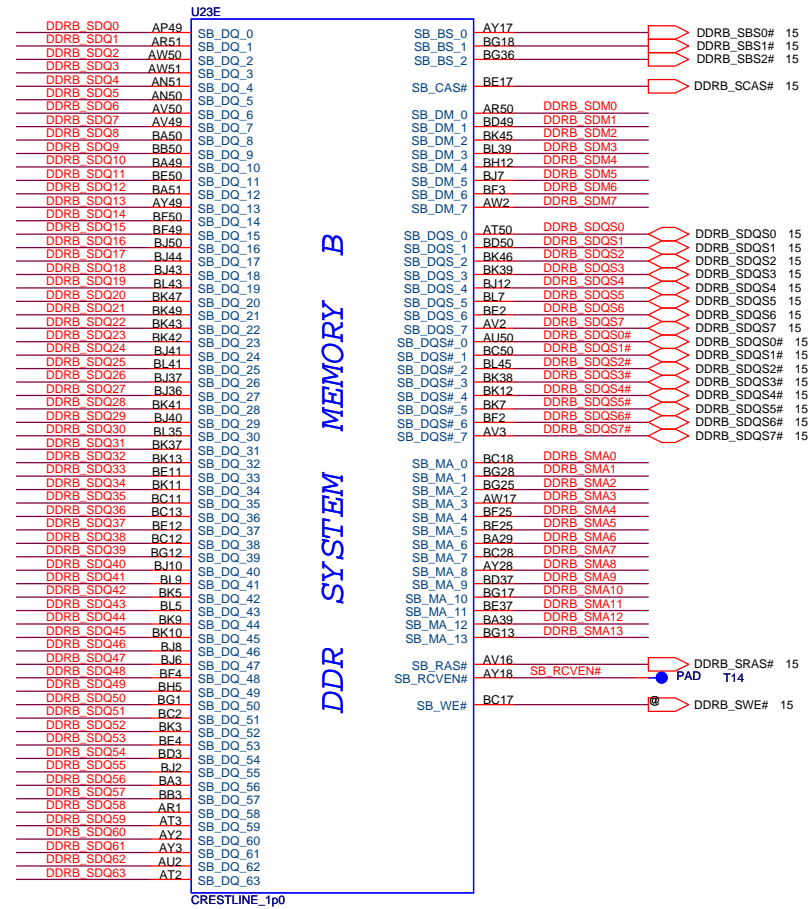
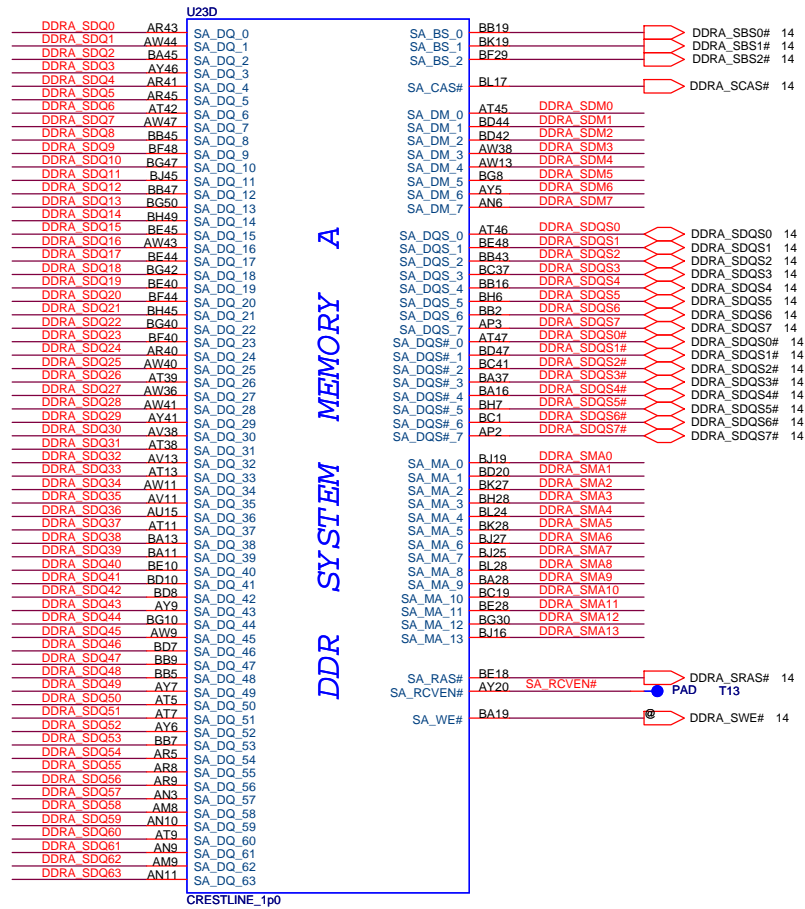
CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present



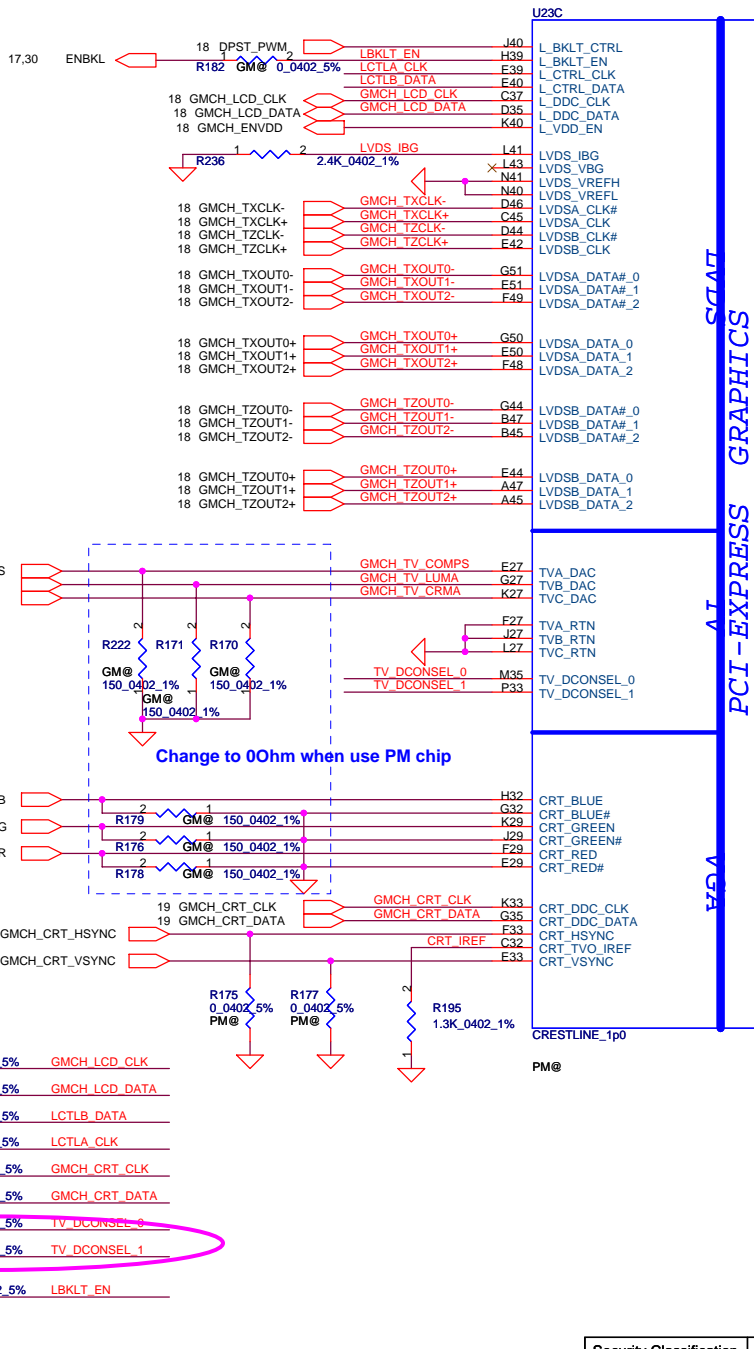


14 DDRA\_SDQ[0..63] <-- DDRA\_SDQ[0..63]  
14 DDRA\_SDM[0..7] <-- DDRA\_SDM[0..7]  
14 DDRA\_SMA[0..13] <-- DDRA\_SMA[0..13]

15 DDRB\_SDQ[0..63] <-- DDRB\_SDQ[0..63]  
15 DDRB\_SDM[0..7] <-- DDRB\_SDM[0..7]  
15 DDRB\_SMA[0..13] <-- DDRB\_SMA[0..13]



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PEG\_COMP  
PEG\_COMPO  
N43  
M43  
10mils  
R240  
24.9\_0402\_1%  
+1.05VS

PEG\_RX#\_0 J51 PCIE GTX C MRX N0  
PEG\_RX#\_1 L51 PCIE GTX C MRX N1  
PEG\_RX#\_2 T45 PCIE GTX C MRX N2  
PEG\_RX#\_3 T50 PCIE GTX C MRX N3  
PEG\_RX#\_4 T45 PCIE GTX C MRX N4  
PEG\_RX#\_5 U40 PCIE GTX C MRX N5  
PEG\_RX#\_6 Y44 PCIE GTX C MRX N6  
PEG\_RX#\_7 Y40 PCIE GTX C MRX N7  
PEG\_RX#\_8 AB51 PCIE GTX C MRX N8  
PEG\_RX#\_9 W49 PCIE GTX C MRX N9  
PEG\_RX#\_10 AD44 PCIE GTX C MRX N10  
PEG\_RX#\_11 AD40 PCIE GTX C MRX N11  
PEG\_RX#\_12 AG46 PCIE GTX C MRX N12  
PEG\_RX#\_13 AH49 PCIE GTX C MRX N13  
PEG\_RX#\_14 AG45 PCIE GTX C MRX N14  
PEG\_RX#\_15 AG41 PCIE GTX C MRX N15

PEG\_RX#\_0 J50 PCIE GTX C MRX P0  
PEG\_RX#\_1 L50 PCIE GTX C MRX P1  
PEG\_RX#\_2 M47 PCIE GTX C MRX P2  
PEG\_RX#\_3 U44 PCIE GTX C MRX P3  
PEG\_RX#\_4 T49 PCIE GTX C MRX P4  
PEG\_RX#\_5 T41 PCIE GTX C MRX P5  
PEG\_RX#\_6 W45 PCIE GTX C MRX P6  
PEG\_RX#\_7 W41 PCIE GTX C MRX P7  
PEG\_RX#\_8 AB50 PCIE GTX C MRX P8  
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PEG\_RX#\_11 AC41 PCIE GTX C MRX P11  
PEG\_RX#\_12 AH47 PCIE GTX C MRX P12  
PEG\_RX#\_13 AG49 PCIE GTX C MRX P13  
PEG\_RX#\_14 AH45 PCIE GTX C MRX P14  
PEG\_RX#\_15 AG42 PCIE GTX C MRX P15

PEG\_TX#\_0 N45 PCIE MTX GRX N0  
PEG\_TX#\_1 U39 PCIE MTX GRX N1 C188 1  
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PEG\_TX#\_4 R50 PCIE MTX GRX N4 C212 1  
PEG\_TX#\_5 T42 PCIE MTX GRX N5 C217 1  
PEG\_TX#\_6 Y43 PCIE MTX GRX N6 C229 1  
PEG\_TX#\_7 W48 PCIE MTX GRX N7 C240 1  
PEG\_TX#\_8 W38 PCIE MTX GRX N8 C246 1  
PEG\_TX#\_9 AD39 PCIE MTX GRX N9 C252 1  
PEG\_TX#\_10 AC46 PCIE MTX GRX N10 C261 1  
PEG\_TX#\_11 AC49 PCIE MTX GRX N11 C270 1  
PEG\_TX#\_12 AC42 PCIE MTX GRX N12 C277 1  
PEG\_TX#\_13 AH39 PCIE MTX GRX N13 C285 1  
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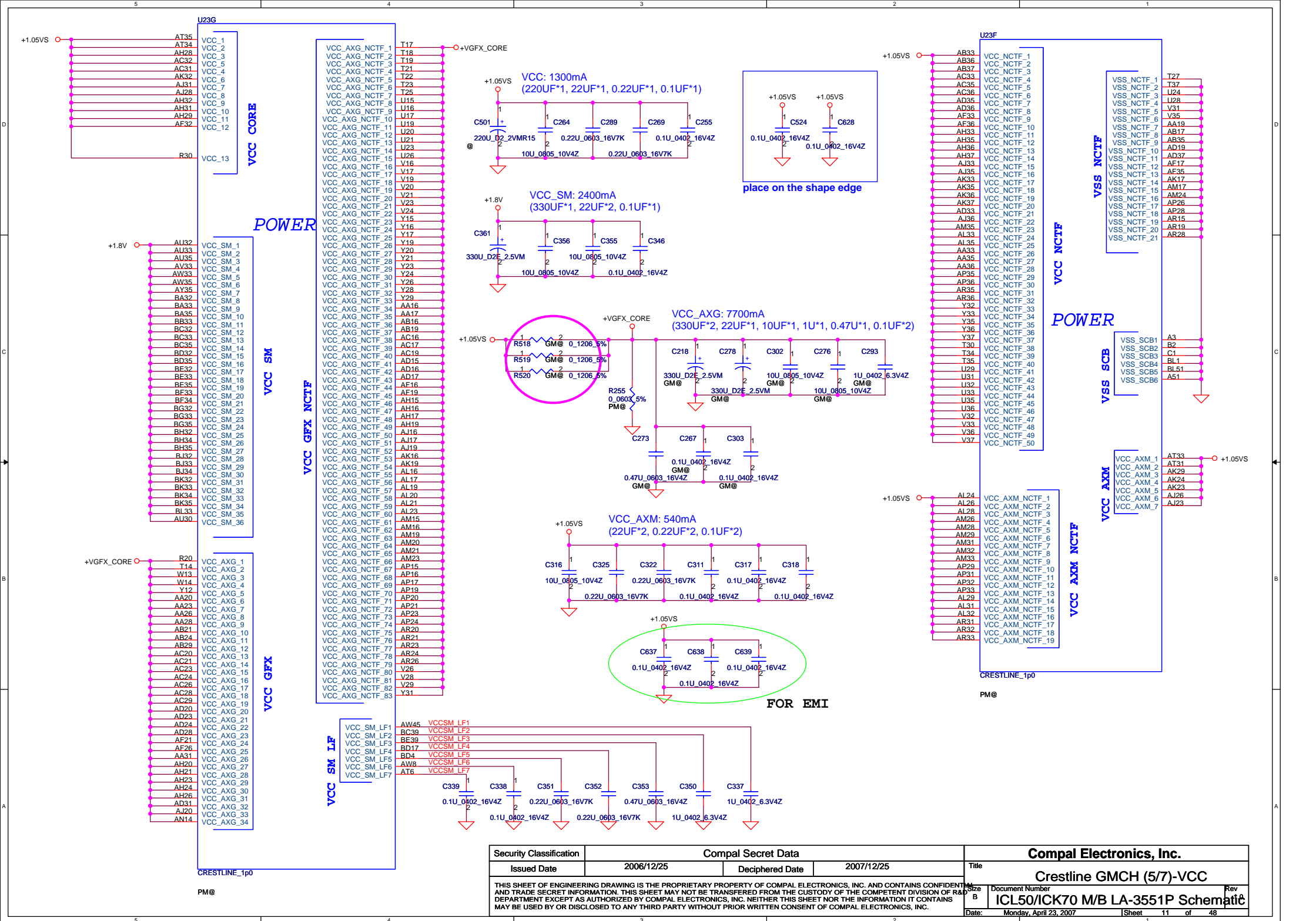
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PEG\_TX#\_4 R51 PCIE MTX GRX P4 C204 1  
PEG\_TX#\_5 U43 PCIE MTX GRX P5 C214 1  
PEG\_TX#\_6 W42 PCIE MTX GRX P6 C219 1  
PEG\_TX#\_7 Y47 PCIE MTX GRX P7 C232 1  
PEG\_TX#\_8 Y39 PCIE MTX GRX P8 C241 1  
PEG\_TX#\_9 AC38 PCIE MTX GRX P9 C248 1  
PEG\_TX#\_10 AD47 PCIE MTX GRX P10 C253 1  
PEG\_TX#\_11 AC50 PCIE MTX GRX P11 C263 1  
PEG\_TX#\_12 AD43 PCIE MTX GRX P12 C272 1  
PEG\_TX#\_13 AG39 PCIE MTX GRX P13 C283 1  
PEG\_TX#\_14 AE50 PCIE MTX GRX P14 C288 1  
PEG\_TX#\_15 AH43 PCIE MTX GRX P15 C297 1

PCIE\_MTX\_C\_GRX\_N[0..15] 17  
PCIE\_MTX\_C\_GRX\_P[0..15] 17  
PCIE GTX C MRX N[0..15] 17  
PCIE GTX C MRX P[0..15] 17

PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N0  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N1  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N2  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N3  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N4  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N5  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N6  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N7  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N8  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N9  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N10  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N11  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N12  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N13  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N14  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_N15

PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_P0  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_P1  
PM@ 0.1U\_0402\_16V7K PCIE\_MTX\_C\_GRX\_P2  
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				Date	Monday, April 23, 2007
				Sheet	10 of 48



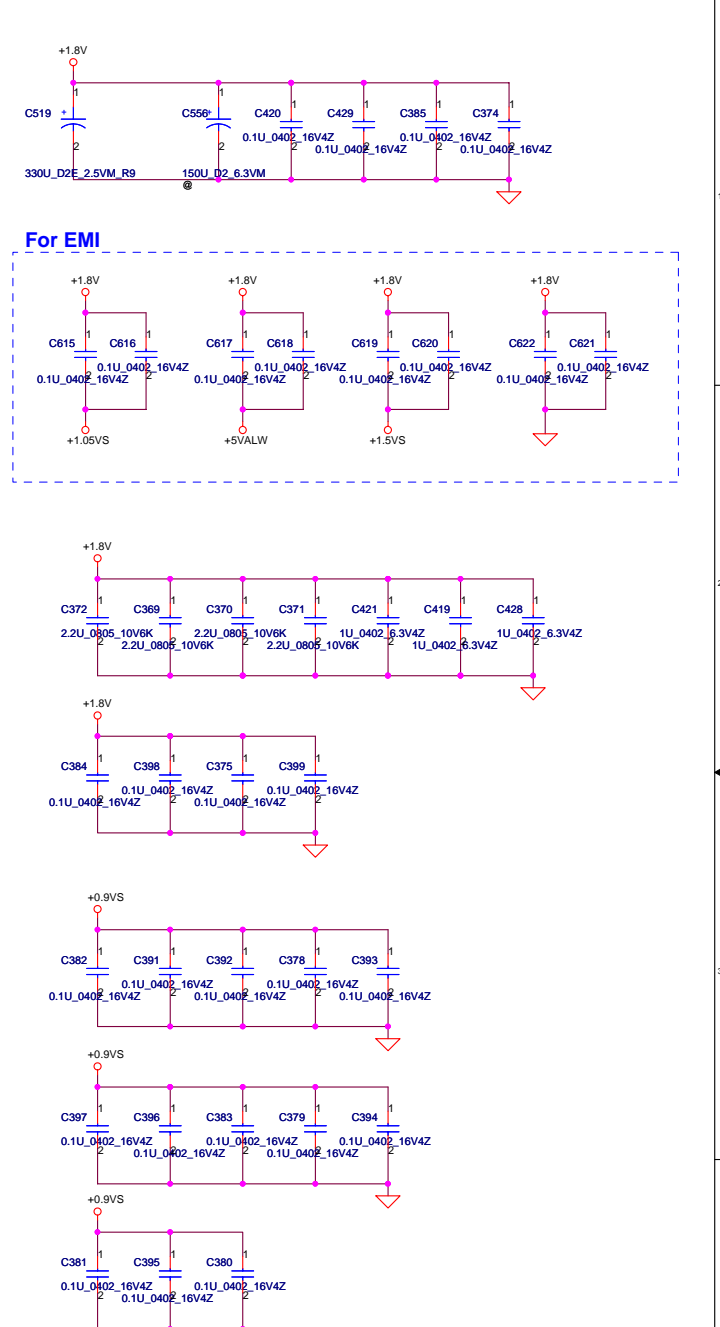
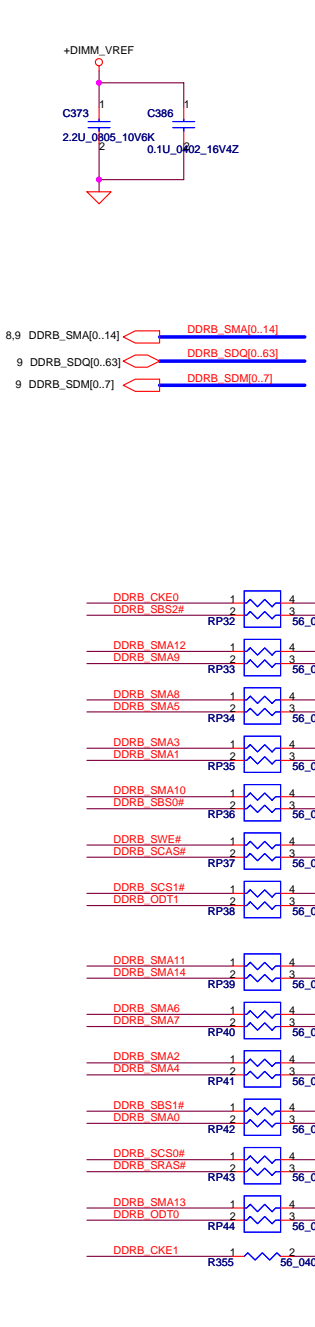
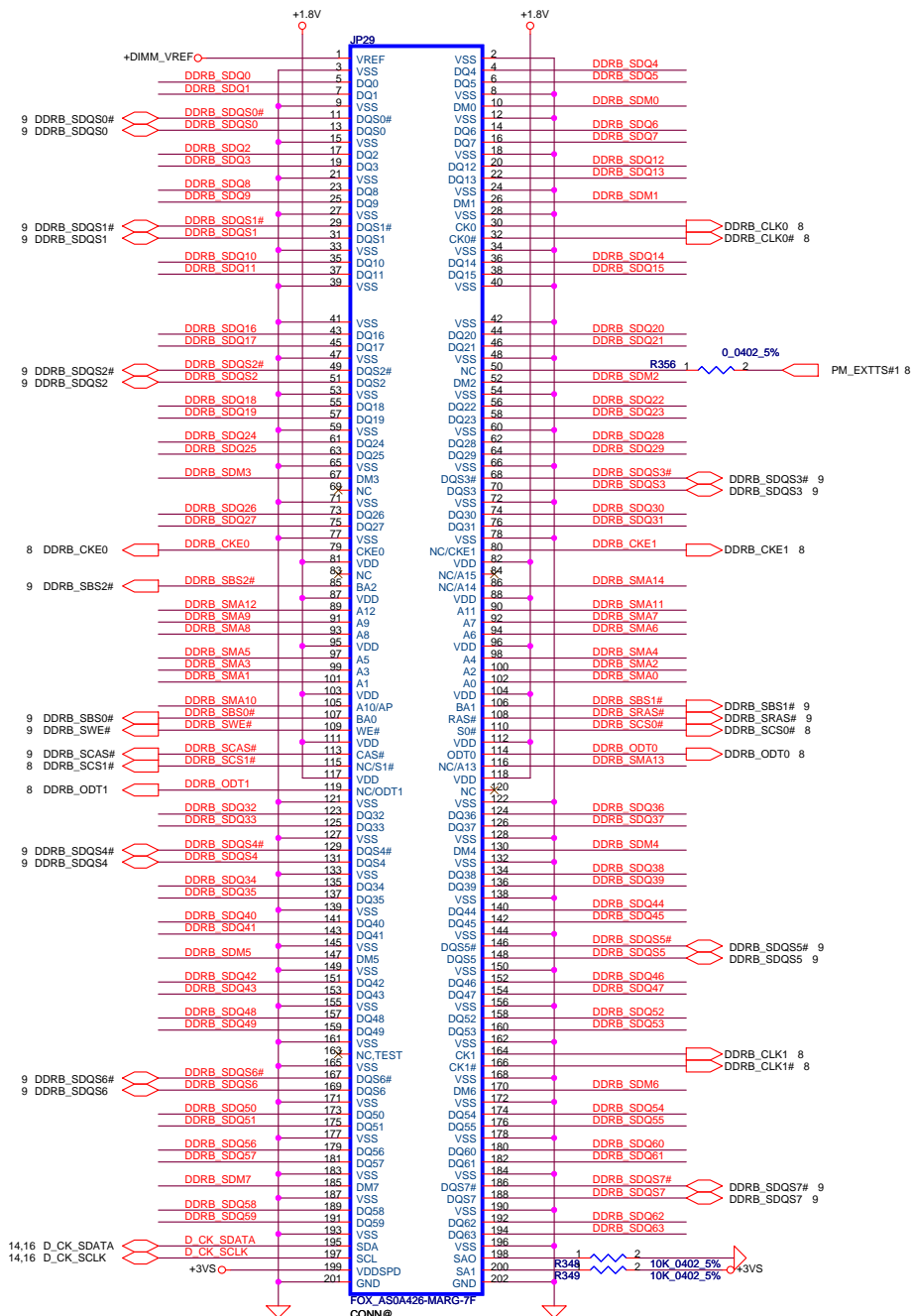


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					ICL50L/ICK70 M/B LA-3551P Schematic	
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DIMM1 REV H:9.2mm (BOT)

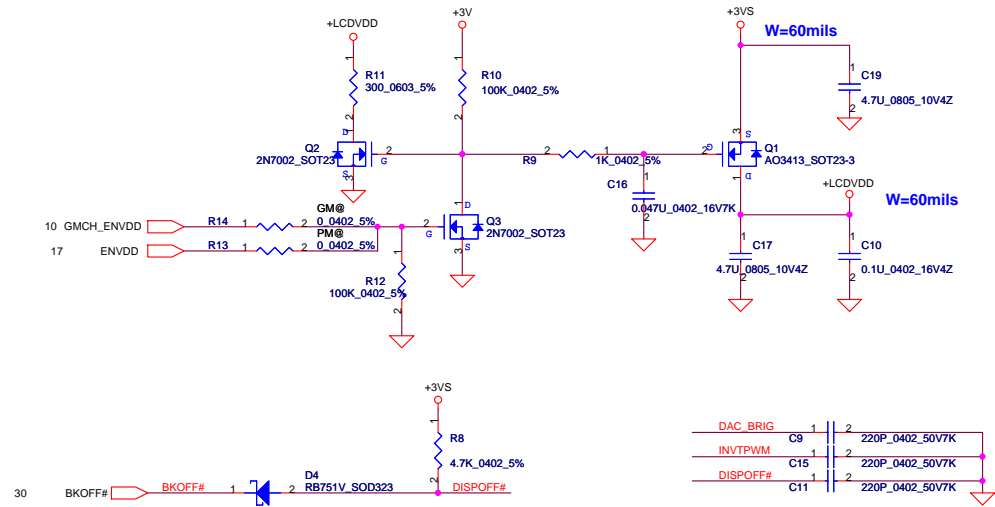
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/12/25	Deciphered Date	2007/12/25	Title	
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				Document Number	Rev
				ICL50/ICK70 M/B LA-3551P Schematic	
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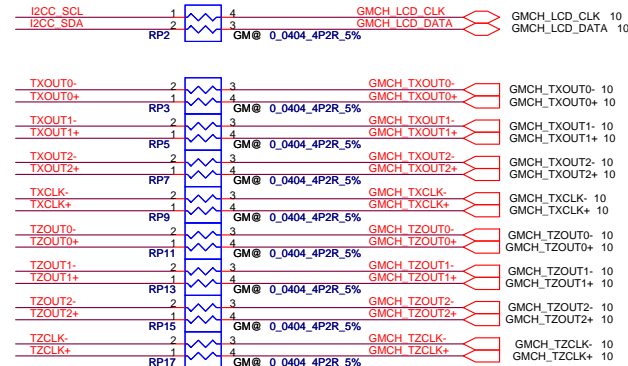
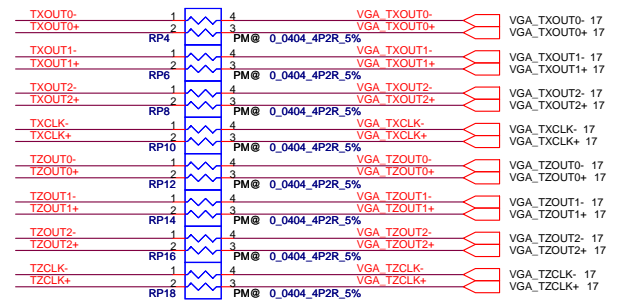
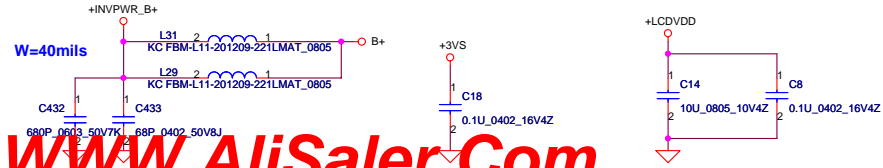
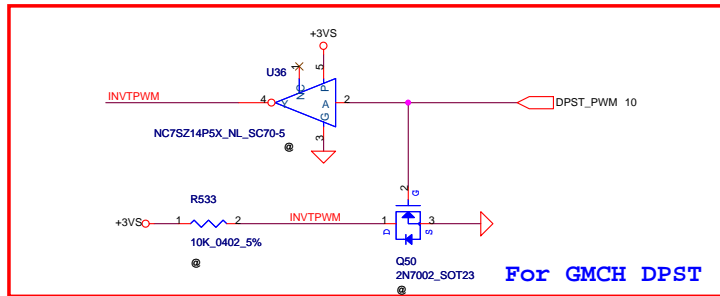
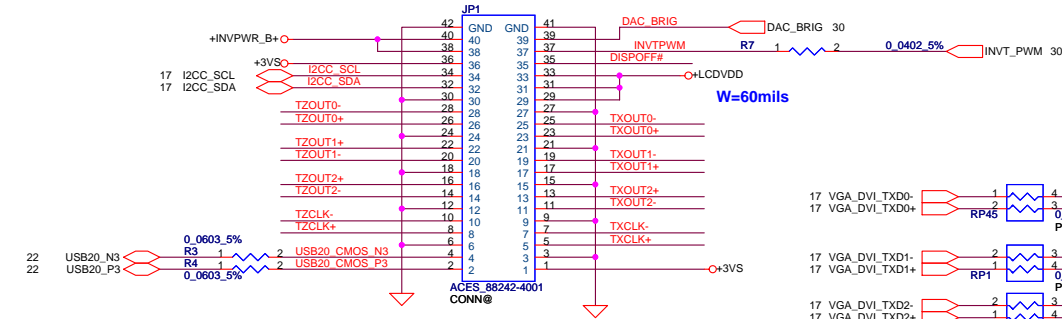


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				Document Number	
				ICL50/ICK70 M/B LA-3551P Schematic	
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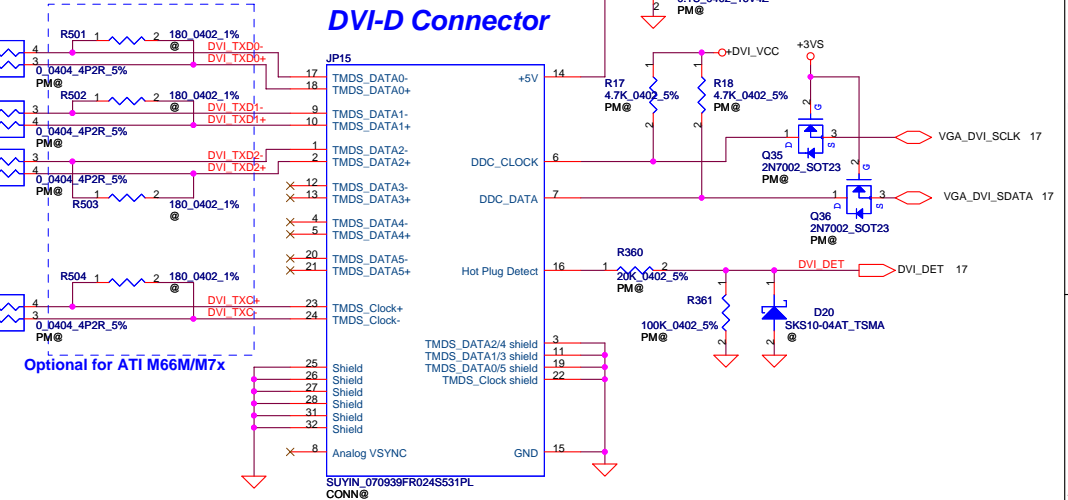
## LCD POWER CIRCUIT



## LCD/PANEL BD. Conn.

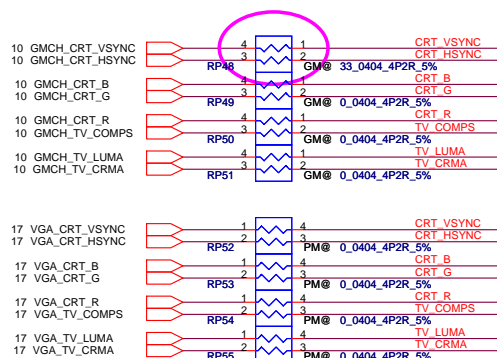


## DVI-D Connector



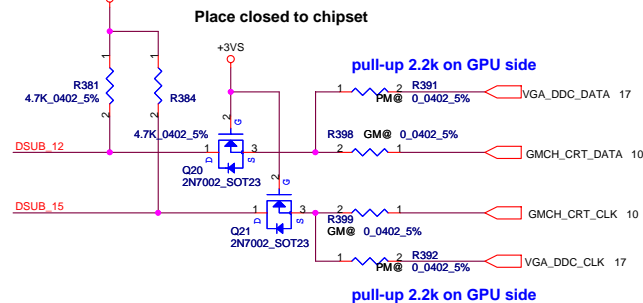
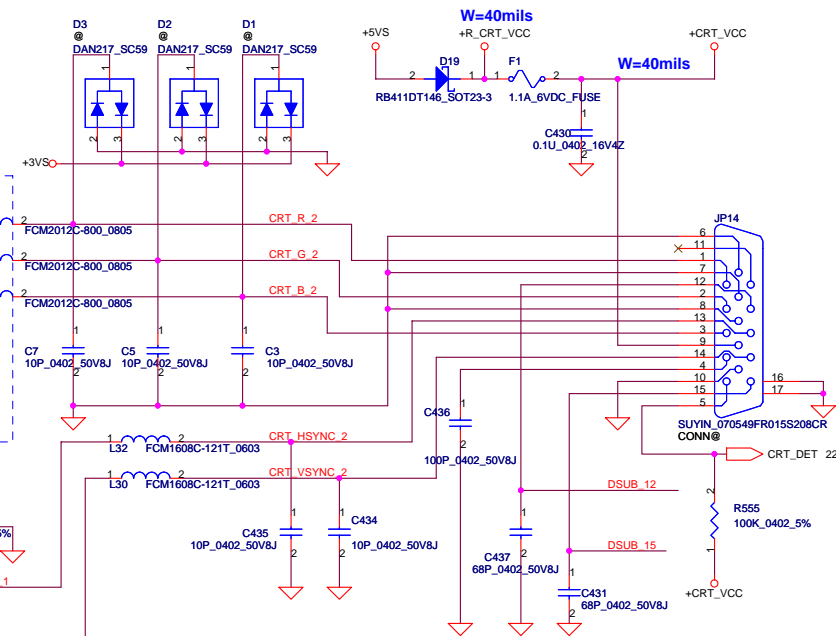
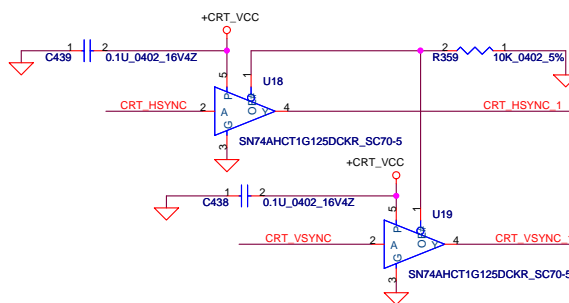
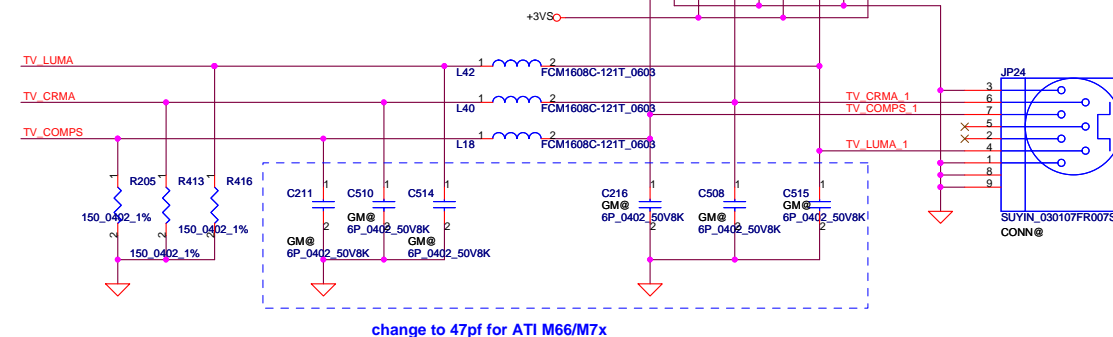
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						Document Number		Rev	
						ICL50/ICK70 M/B LA-3551P Schematic		18 of 48	
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# CRT Connector

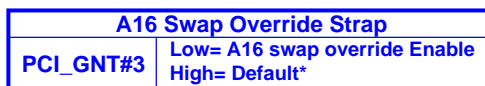
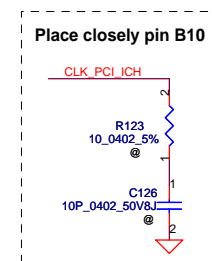
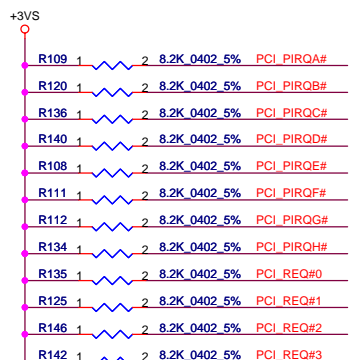


Place closed to chipset

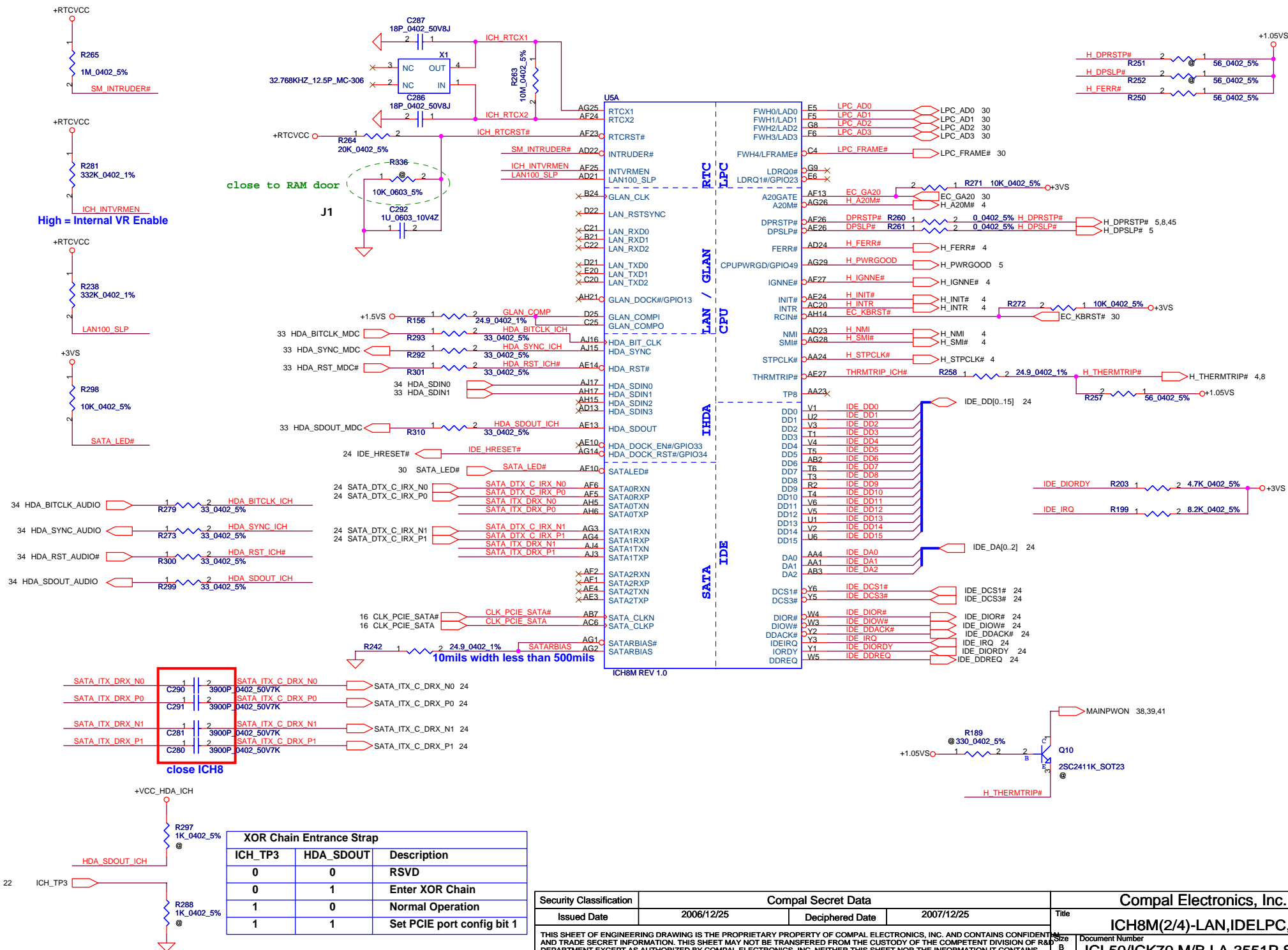
## TV-OUT Conn.

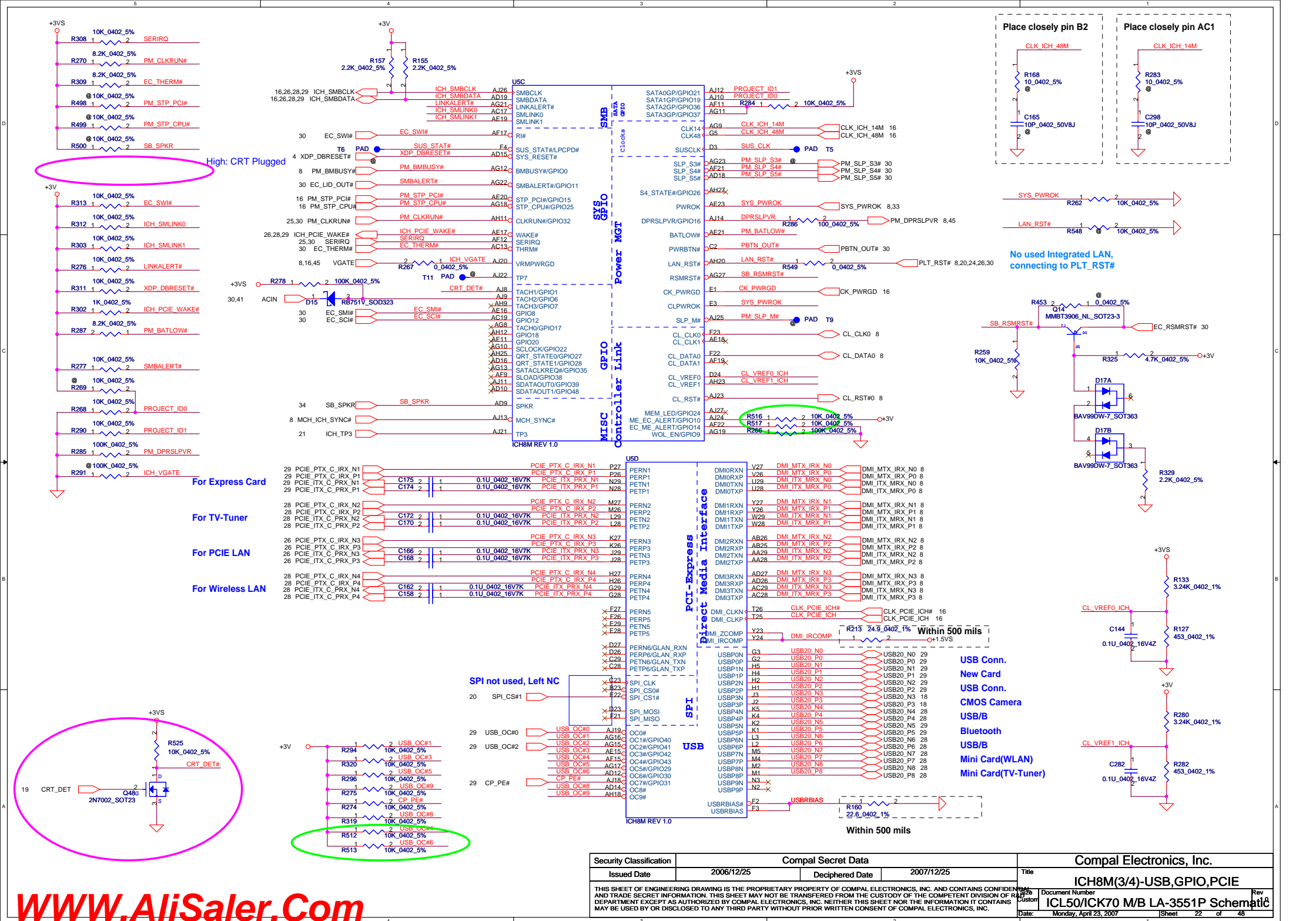


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				Document Number	Rev
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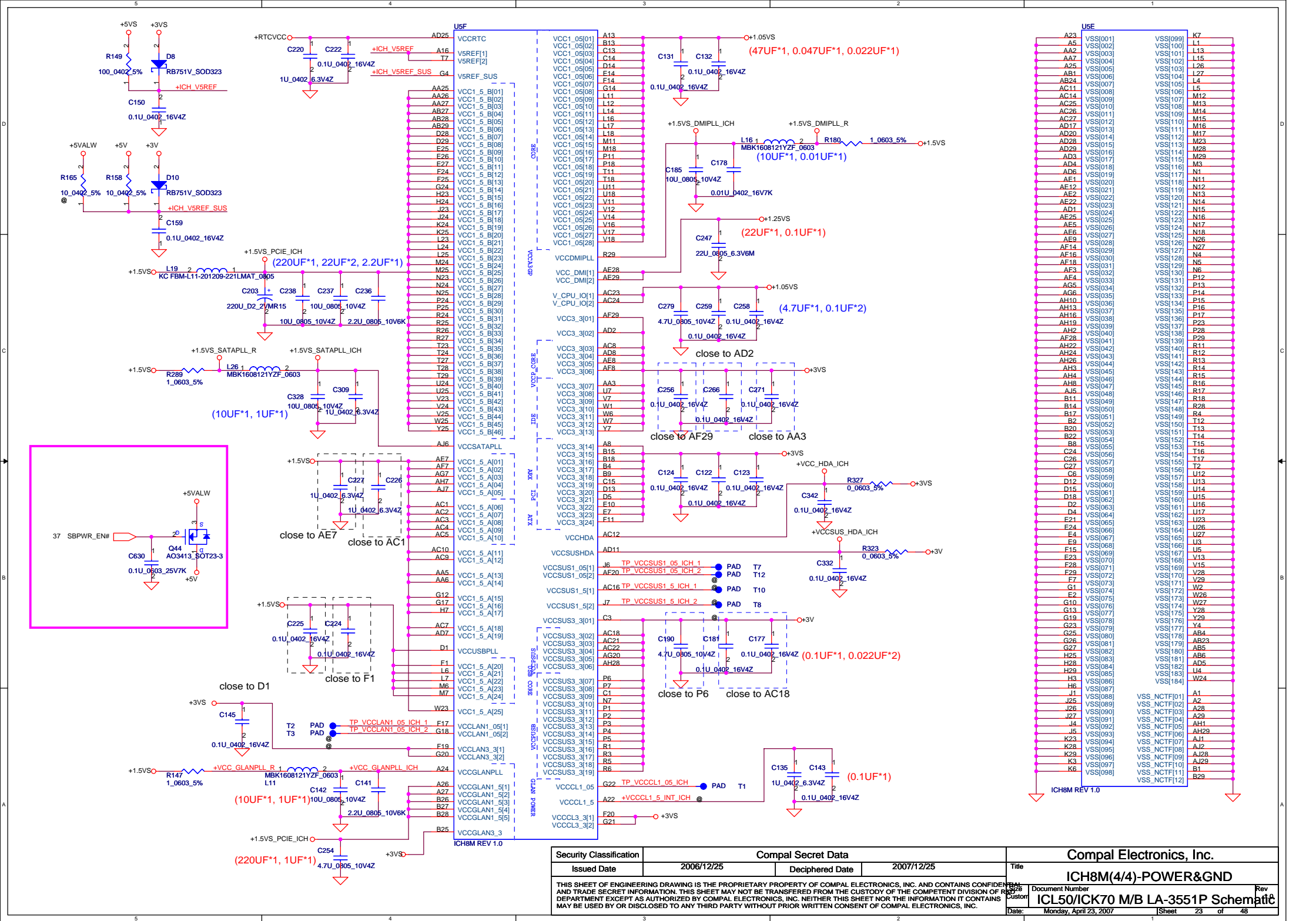


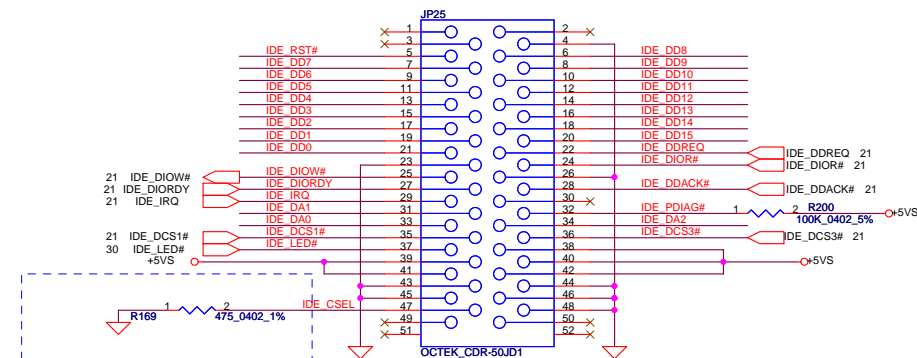
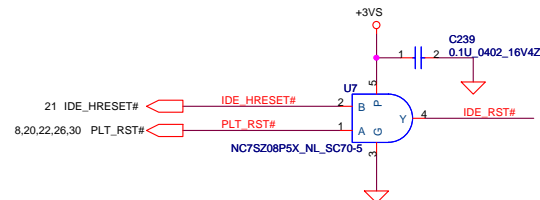
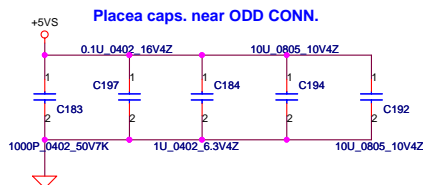
The diagram shows two inverters, U8 and U9, both of type NC7SZ08P5X\_NL\_SC70-5. Both inverters are powered by +3VS and ground. The input to both inverters is the PLT\_RST# signal. The output of U8 is connected to the PLT\_RST\_BUF# pin through a 100K\_0402\_5% resistor (R316). The output of U9 is connected to the PLTRST\_VGA# pin through a 100K\_0402\_5% resistor (R321). The output of U9 is also labeled PM@.



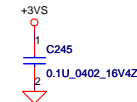
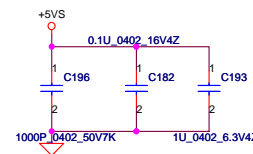




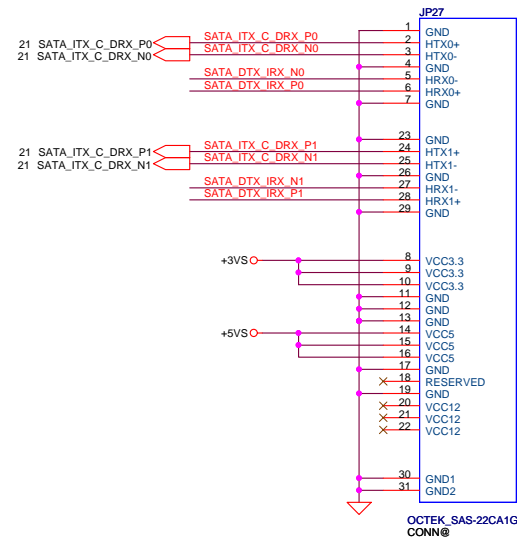
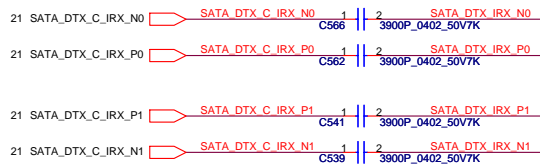




**IDE\_CSEL**  
Grounding for Master (When use SATA HDD)  
Open or High for Slaver (Normal)



## SATA HDD Conn.(SAS Connector)

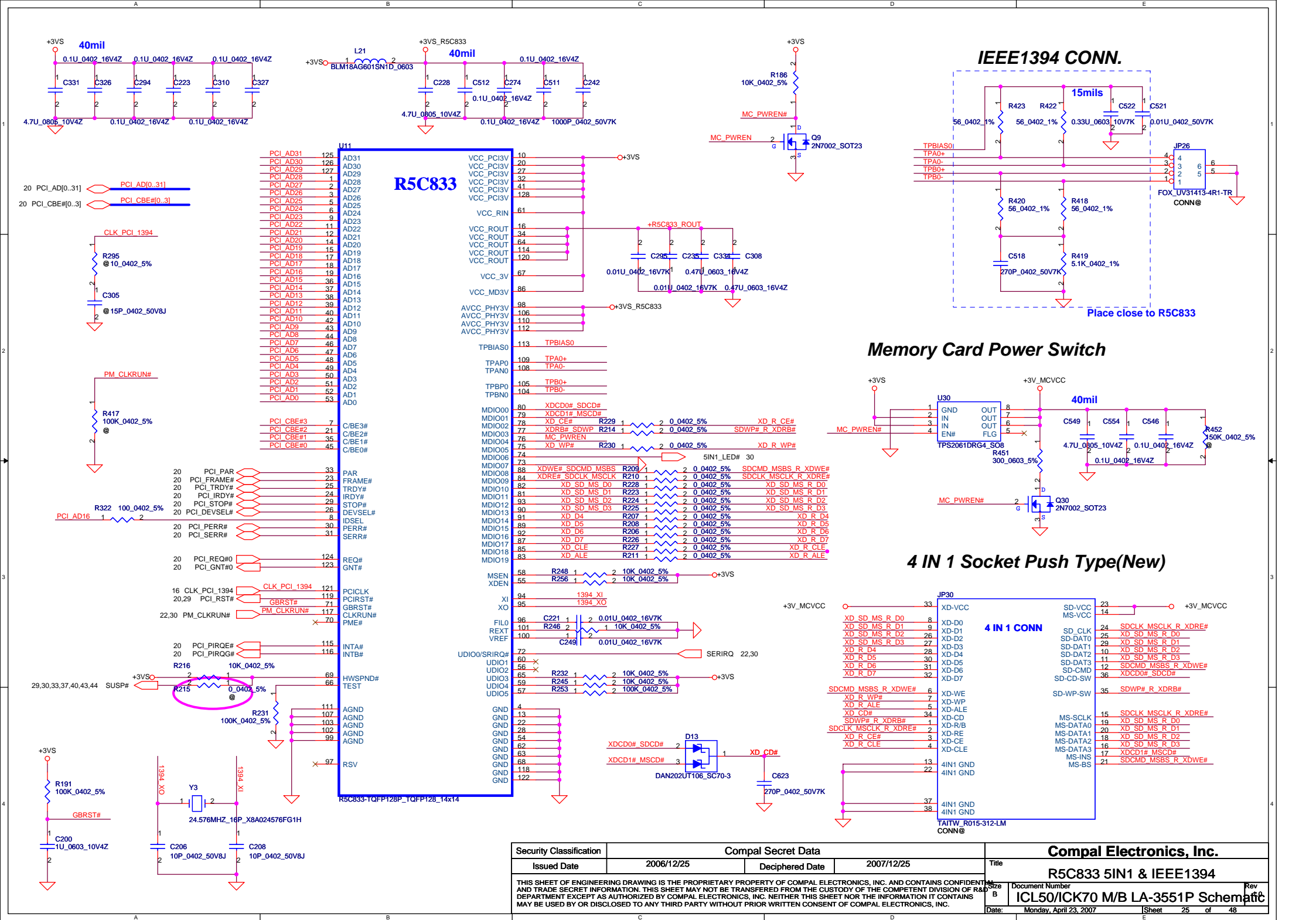


First HDD for 15.4"

2nd HDD for 17"

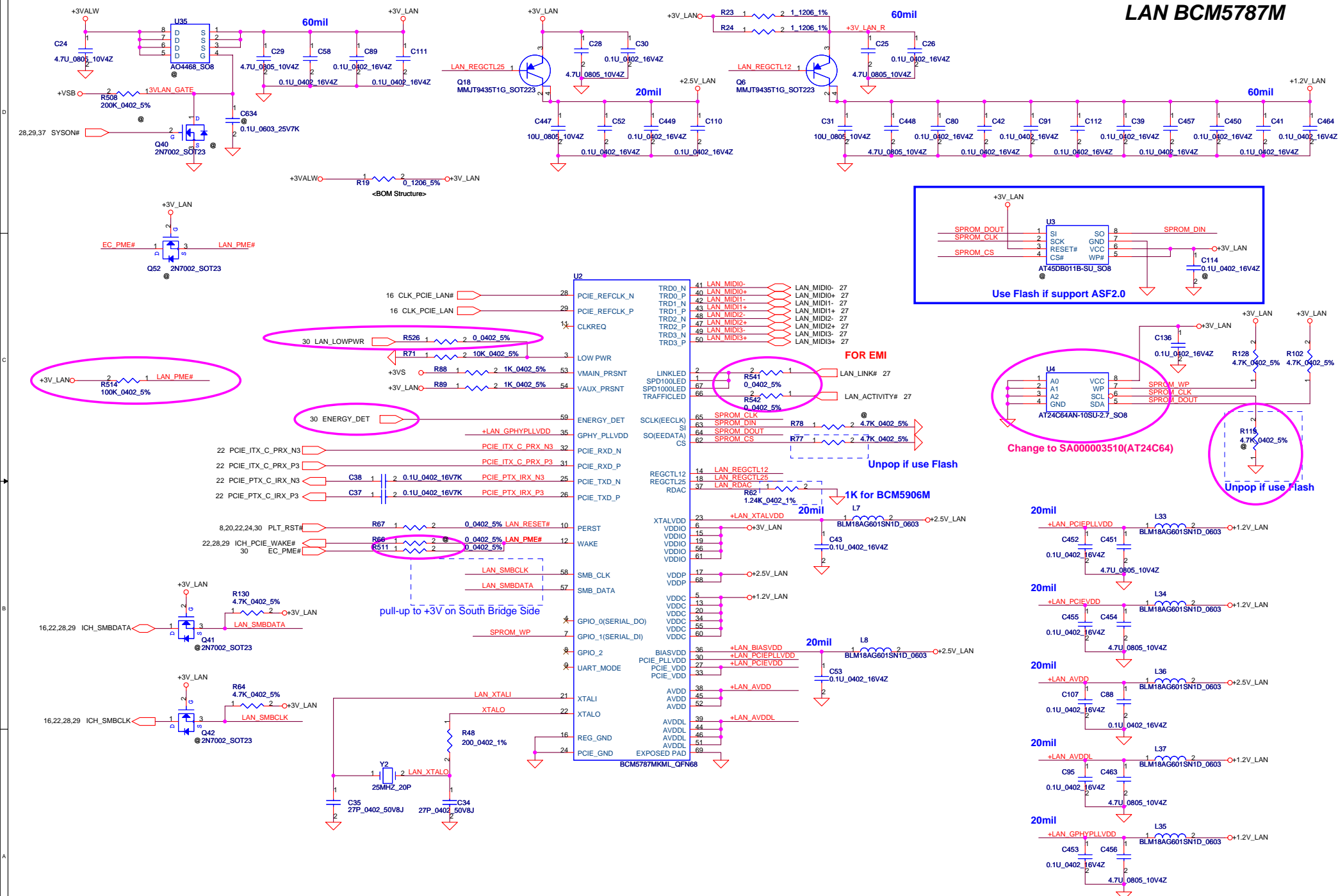
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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2006/12/25				2007/12/25				Title			
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Date: Monday, April 23, 2007				Rev				ICL50/ICK70 M/B LA-3551P Schematic			
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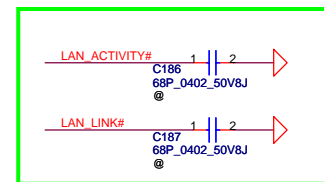


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				ICL50/ICK70 M/B LA-3551P Schematic	
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**LAN BCM5787M**

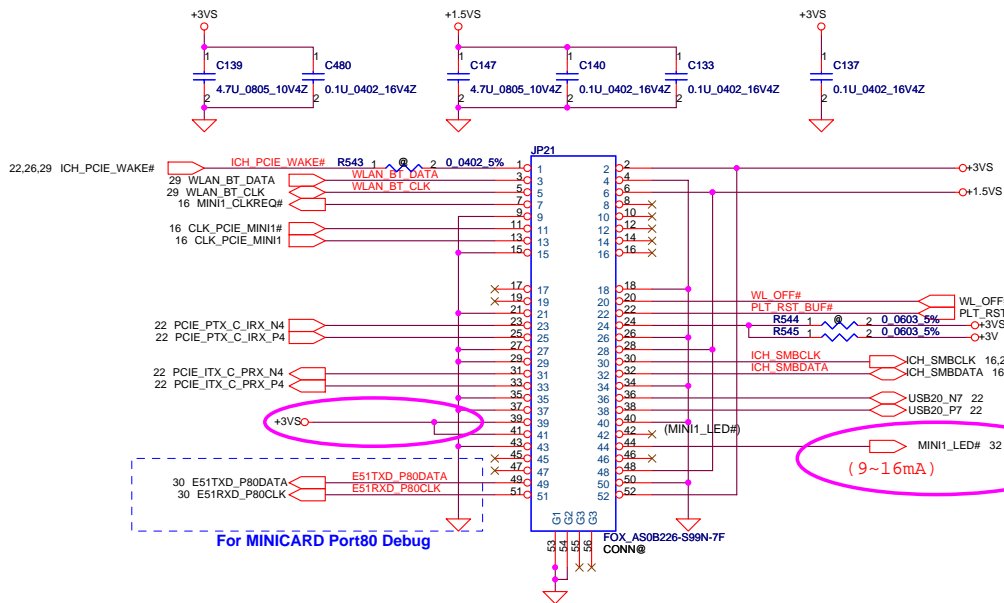


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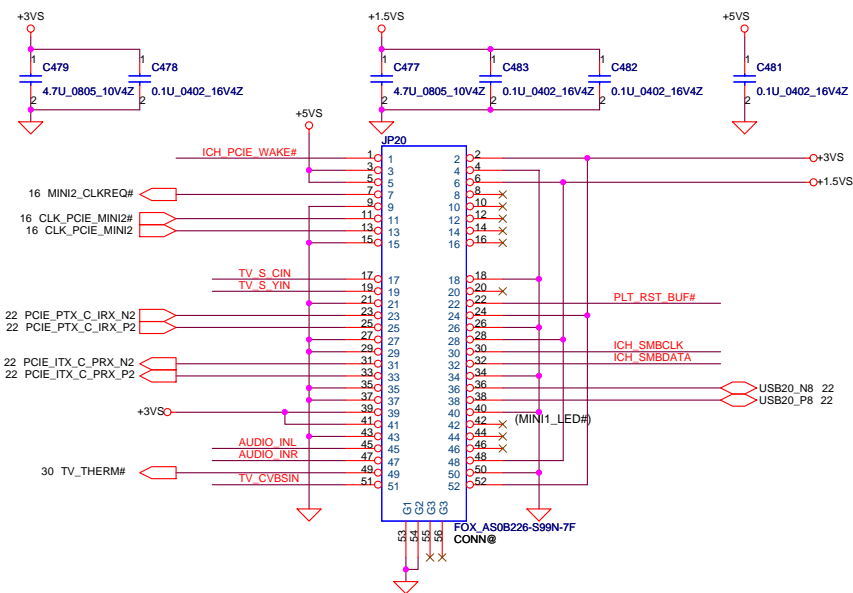
## For Wireless LAN



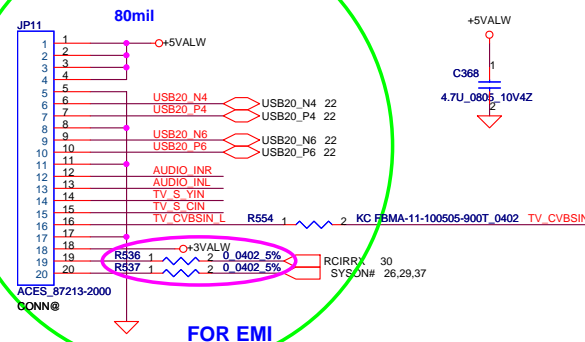
Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

## For TV-Tuner/HW MPEG



## To USB/B Connector

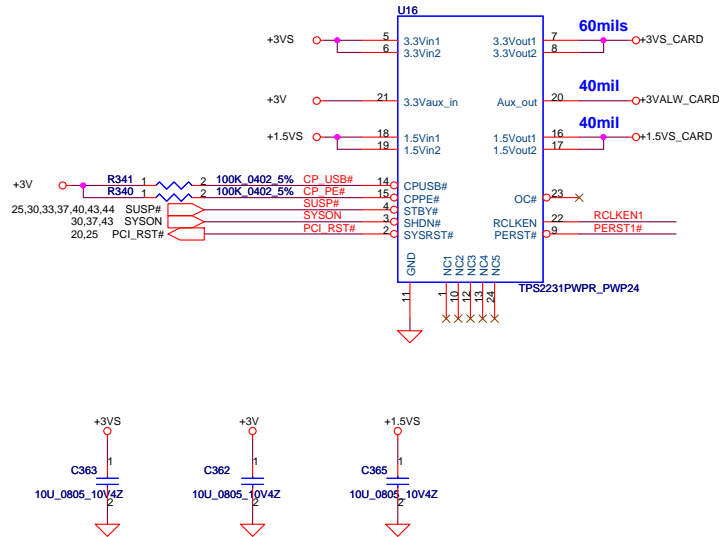


AV-IN Connector  
CIR

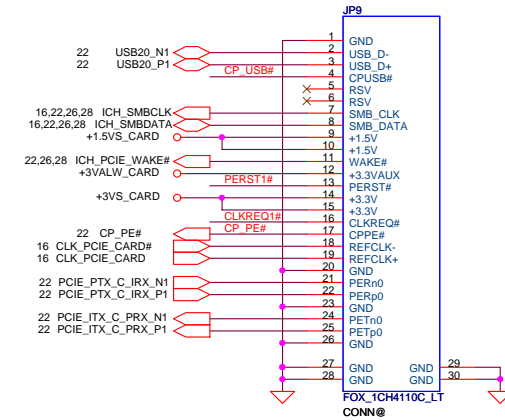
FOR EMI

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				Document Number	Rev
				ICL50/ICK70 M/B LA-3551P Schematic	
				Date: Monday, April 23, 2007	Sheet 28 of 48

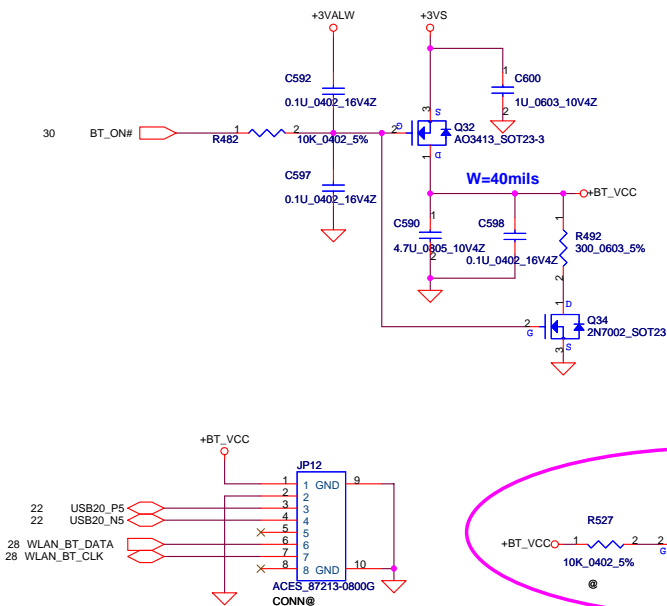
## New Card Power Switch



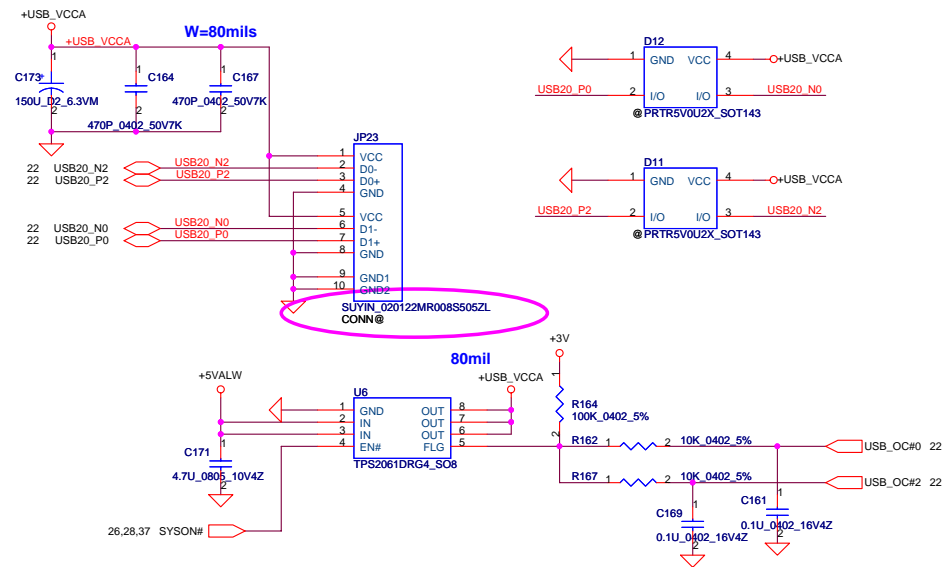
## New Card Socket (Left/TOP)



## Bluetooth Conn.



## USB CONN. (Stack-up Type)

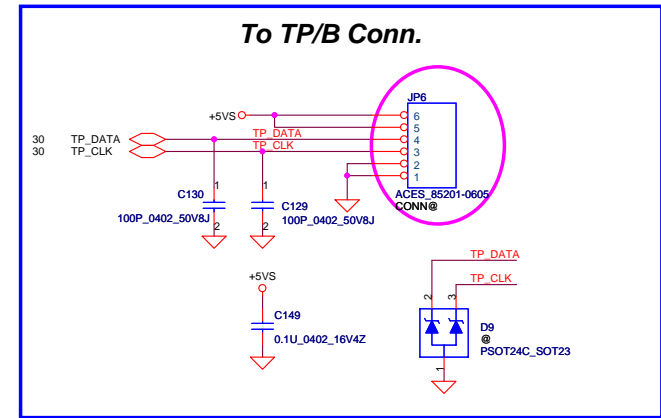
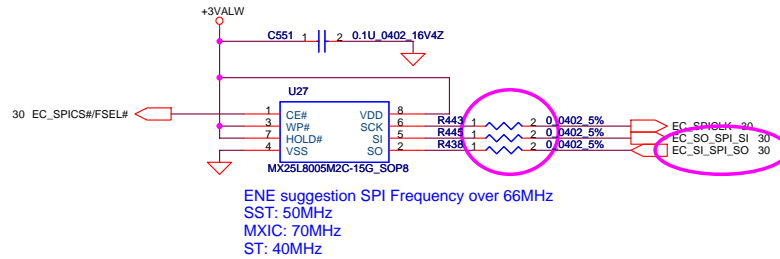
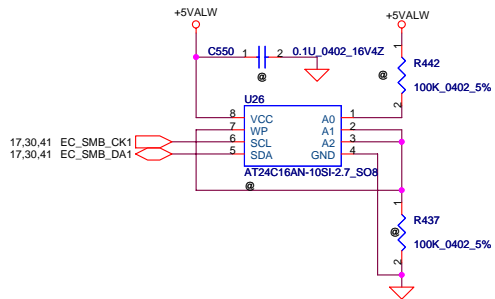


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				Document Number	ICL50/ICK70 M/B LA-3551P Schematic
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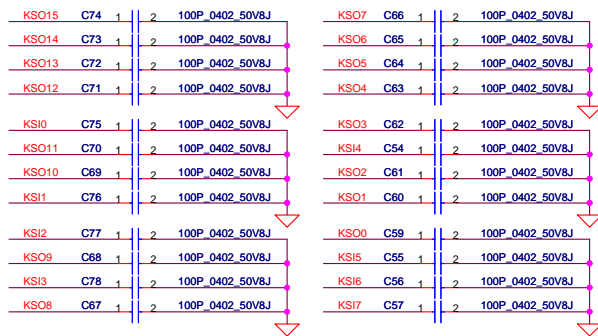
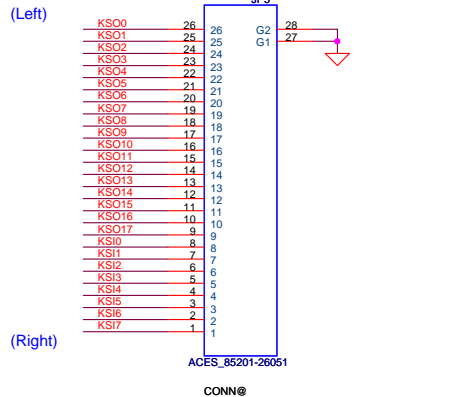




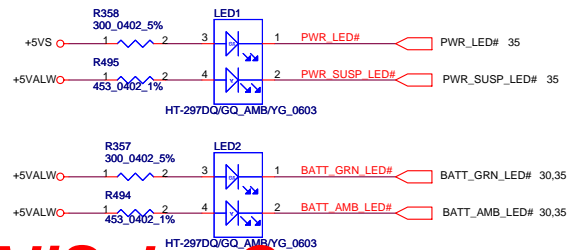
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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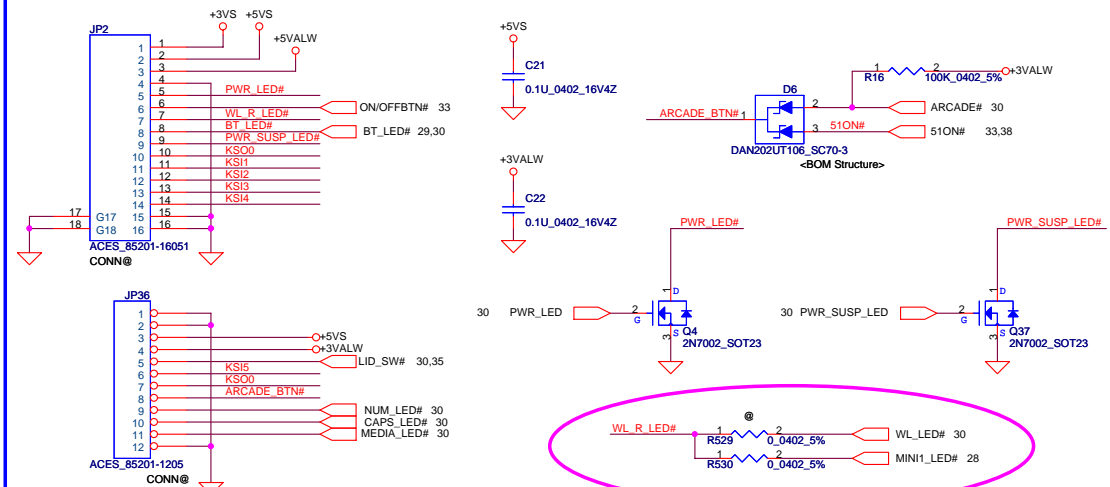
## INT\_KBD Conn.



## Compal Footprint

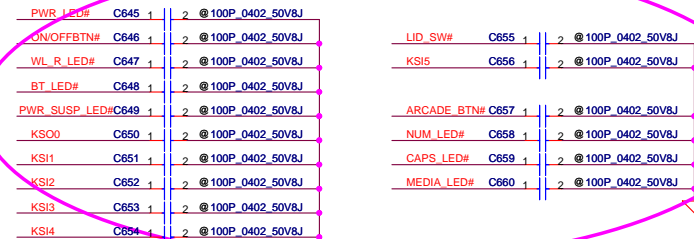


## To BTN/B Conn.



## FOR EMI

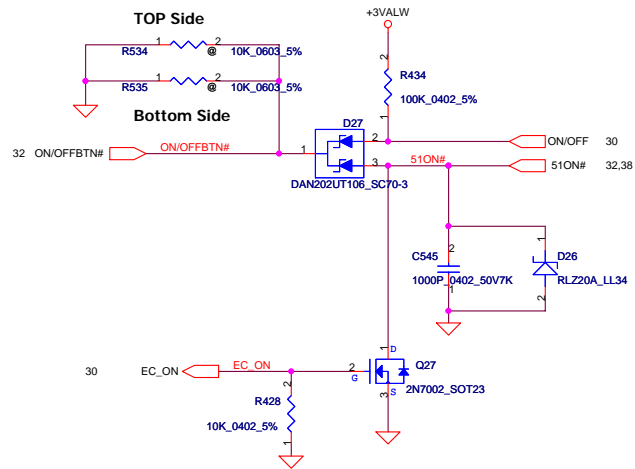
	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#



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Document Number				Rev
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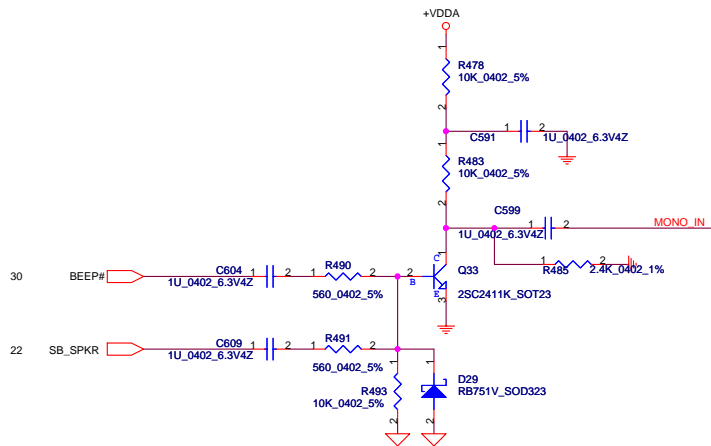
ON/OFF switch

[illegible]

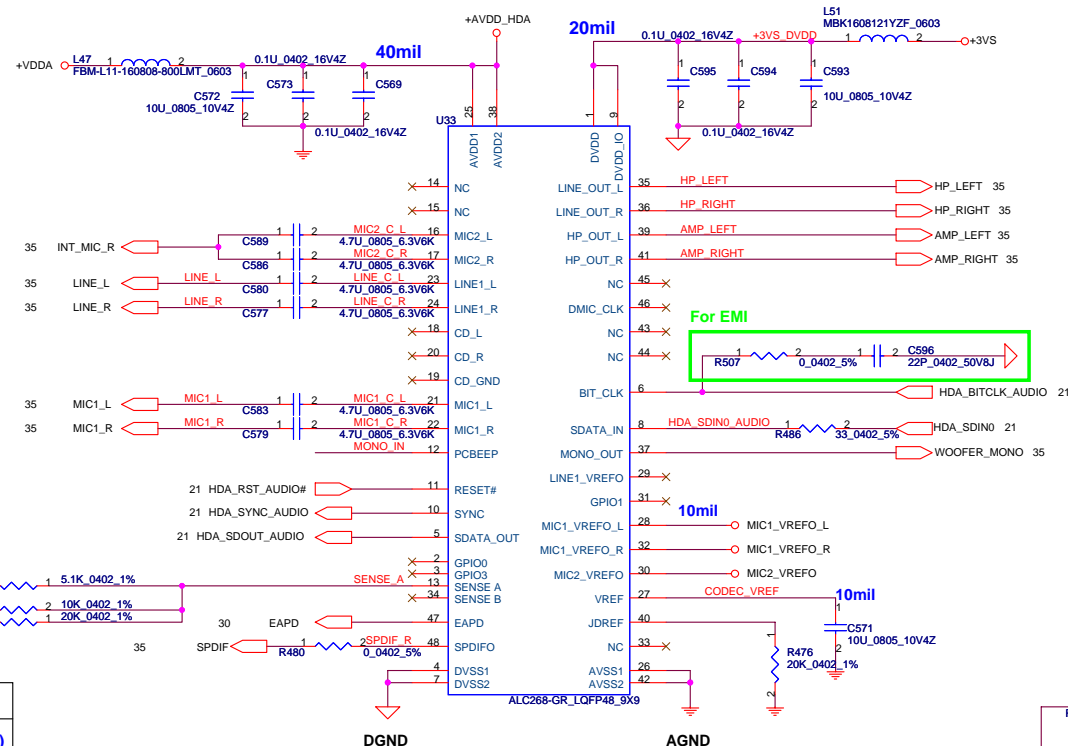
The top diagram shows the output to the South Bridge (SYS\_PWROK) and EC (EC\_PWROK). The middle diagram shows the output to the VS\_ON pin. The bottom diagram shows the output to the VGA\_ON pin. Each diagram includes input filters (R331, R328, R307), output capacitors (C300, C333, C330), and feedback components (R324, R318, R552).

**Change BATT1 P/N : SP093PA0200 (Panasonic)  
SP093MX0000 (MAXELL)**

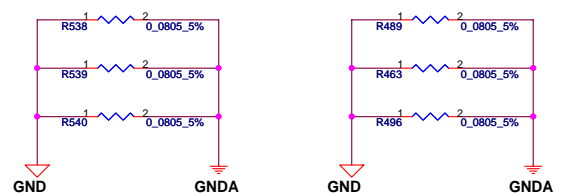
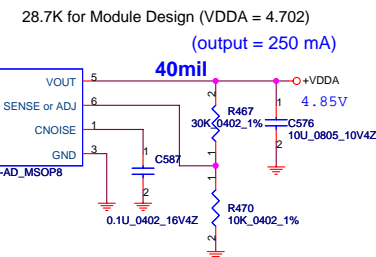
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/12/25	Deciphered Date	2007/12/25	Title	Power OK, Reset and RTC Circuit, TP
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				ICL50/ICK70 M/B LA-3551P Schematic	
Date	Monday, April 23, 2007		Sheet	33 of 48	



## HD Audio Codec



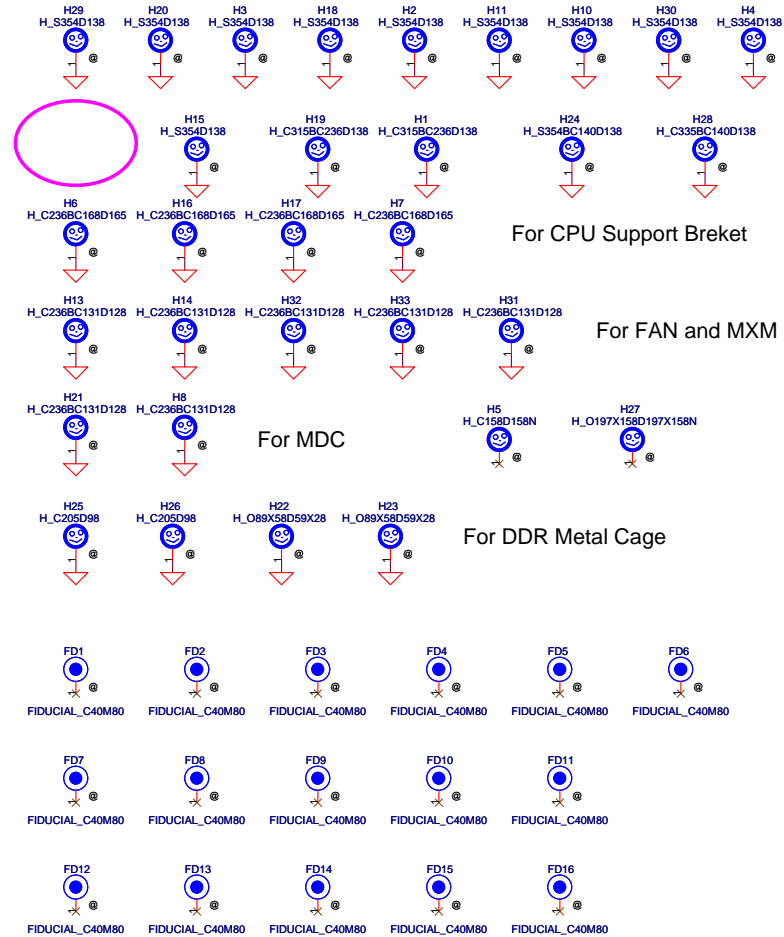
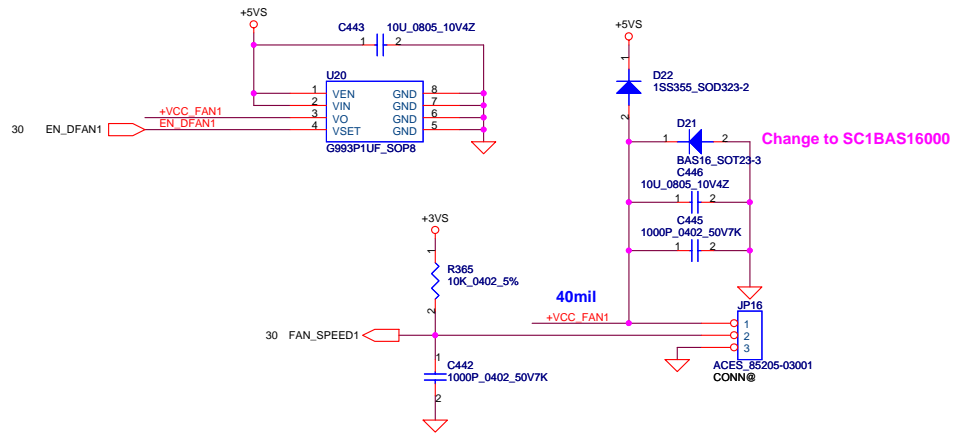
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



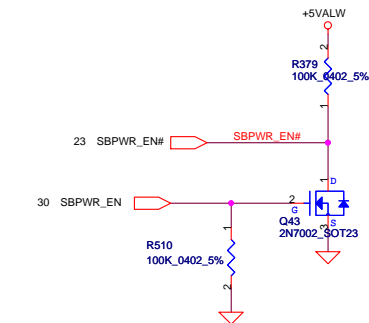
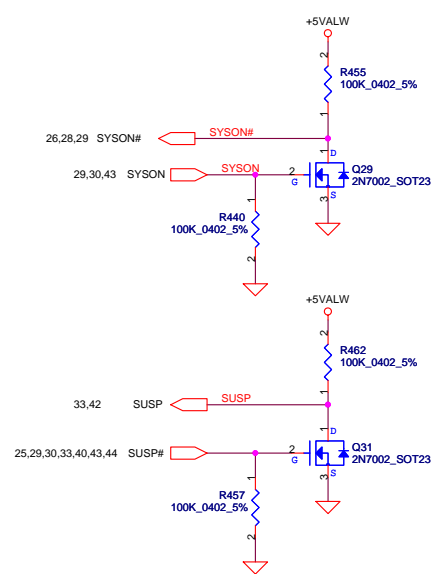
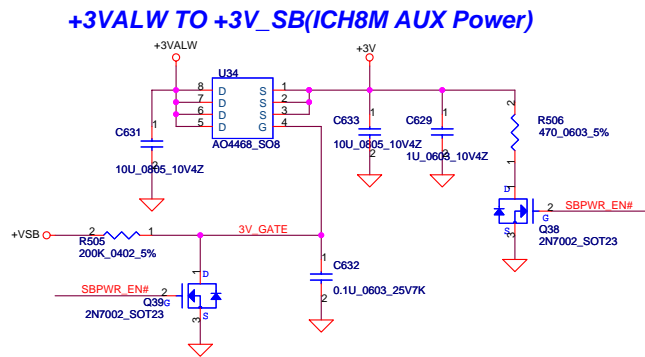
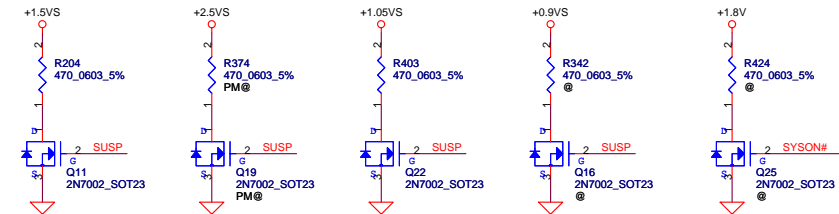
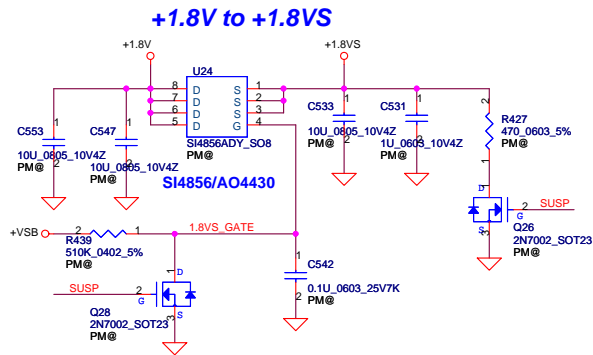
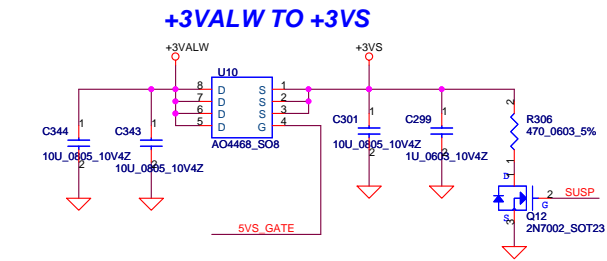
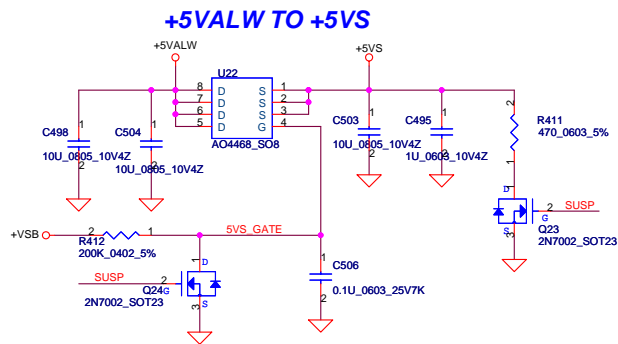
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/12/25				Deciphered Date			
2007/12/25				Title				HD Audio Codec ALC268			
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Date: Monday, April 23, 2007				Sheet 34 of 48				ICL50/ICK70 M/B LA-3551P Schematic			



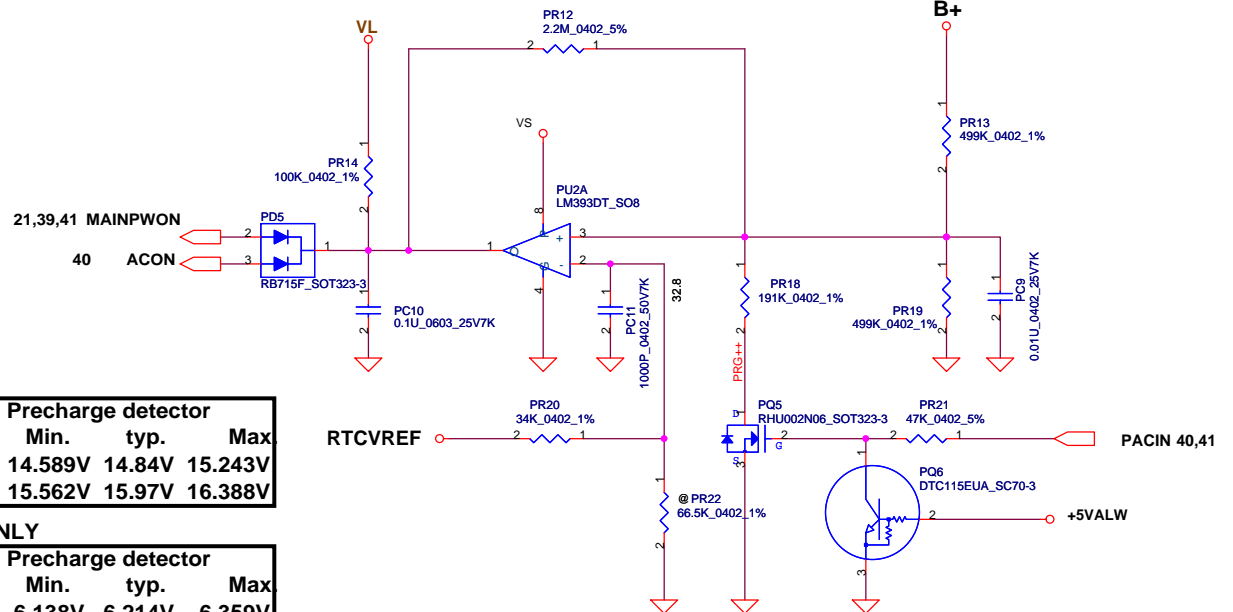
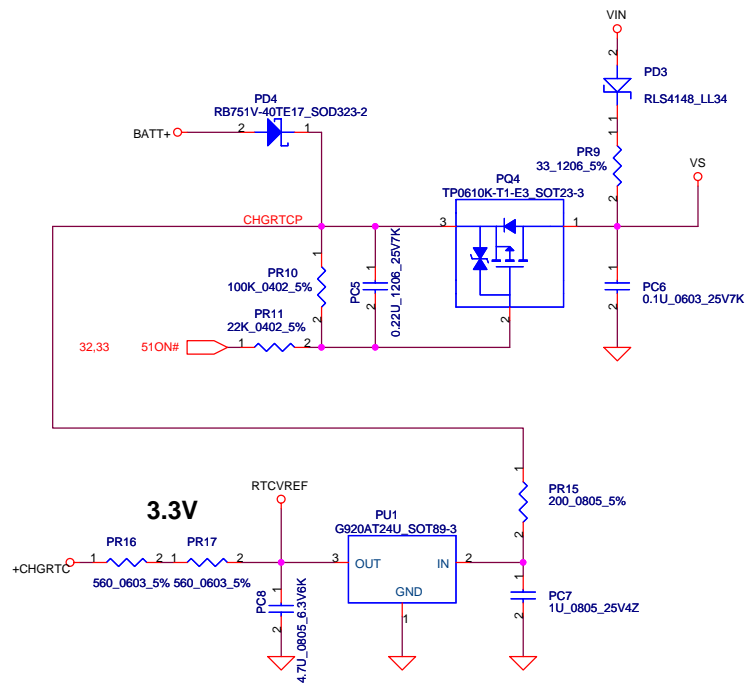
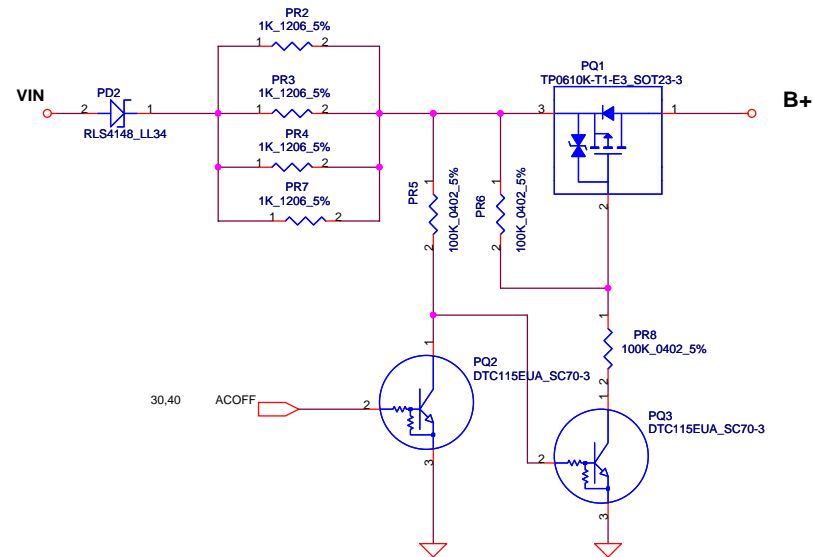
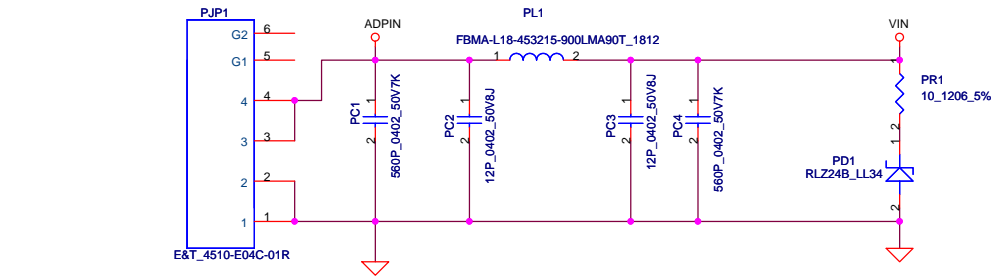
## FAN1 Conn



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Issued Date				2006/12/25				Deciphered Date			
2006/12/25				2007/12/25				Title			
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#### ACIN

	Precharge detector		
	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

#### BATT ONLY

	Precharge detector		
	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

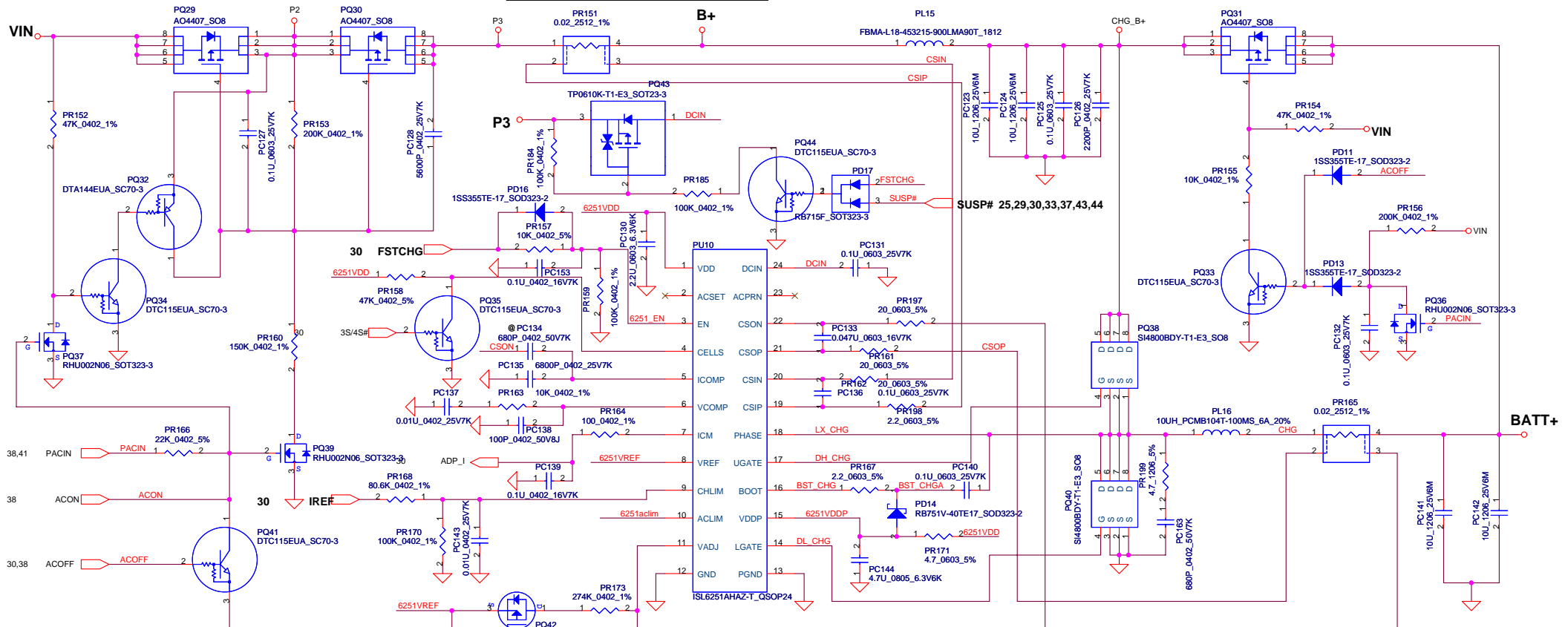
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/22	Deciphered Date	2007/08/22	Title	DCIN/DECTOR
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Size	B	Document Number	ICL50 / ICK70	Rev	1.0
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Iada=0~4.74A(90W)

ADP\_I = 19.9\*Iadapter\*Rsense

CP = 85%\*Iada ; CP = 4.07A



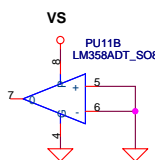
CP mode  
 $I_{input} = (1/0.02) * ((0.05 * V_{aclim}) / (2.39 + 0.05))$   
 where  $V_{aclim} = 1.502V$ ,  $I_{input} = 4.07A$   
 $V_{aclim} = 2.39 * ((10K / 152K) / ((5.76K / 152K) + (10K / 152K)))$   
 $= 1.502V$

CC=0.6~4.48A

IREF=0.7224\*Icharge

IREF=0.43V~3.24V

BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication		HIGH	HIGH	12.60V



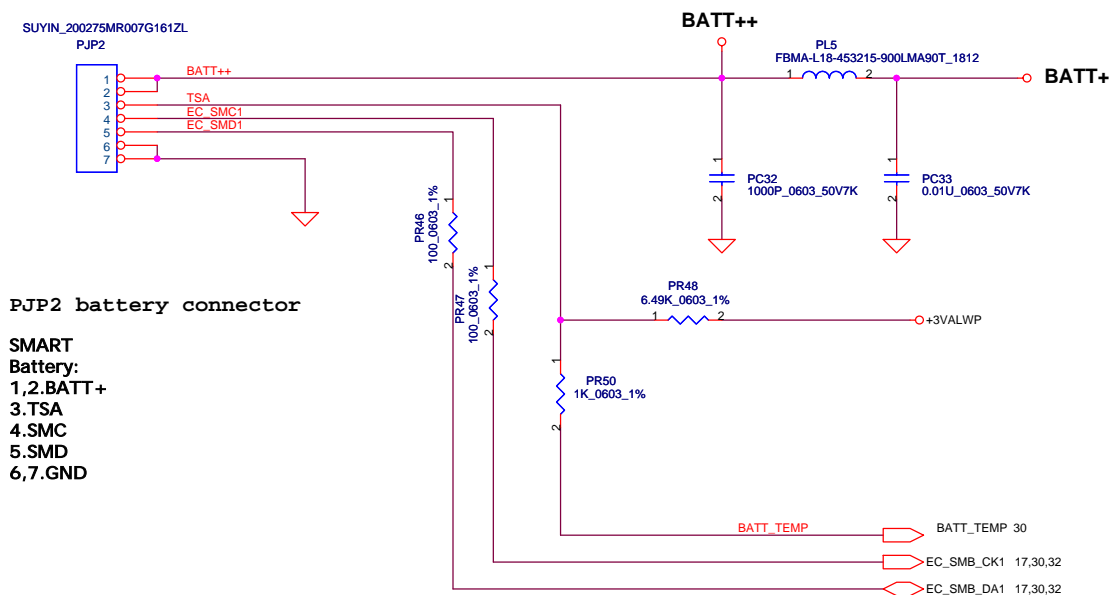
OVP voltage :  
 LI-4S :18.0V--BATT-OVP=2.677V  
 BATT-OVP=0.1487\*BATT+  
 LI-3S :13.50V--BATT-OVP=2.007V  
 BATT-OVP=0.1487\*BATT+

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				Date	Thursday, April 19, 2007
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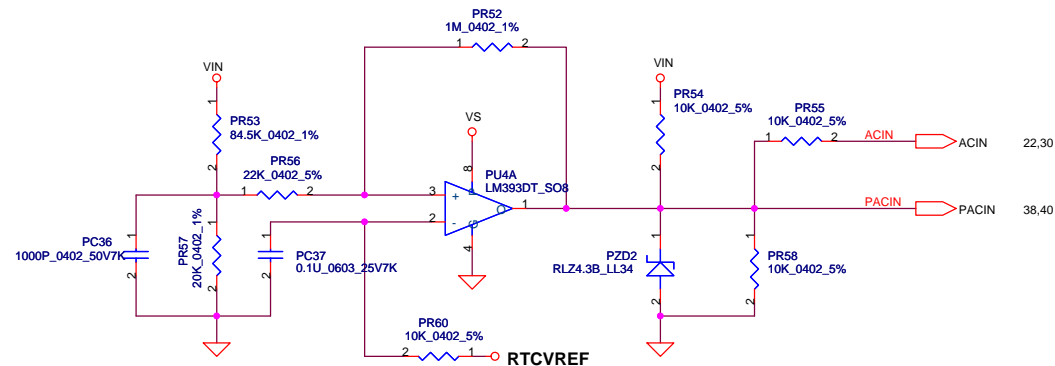
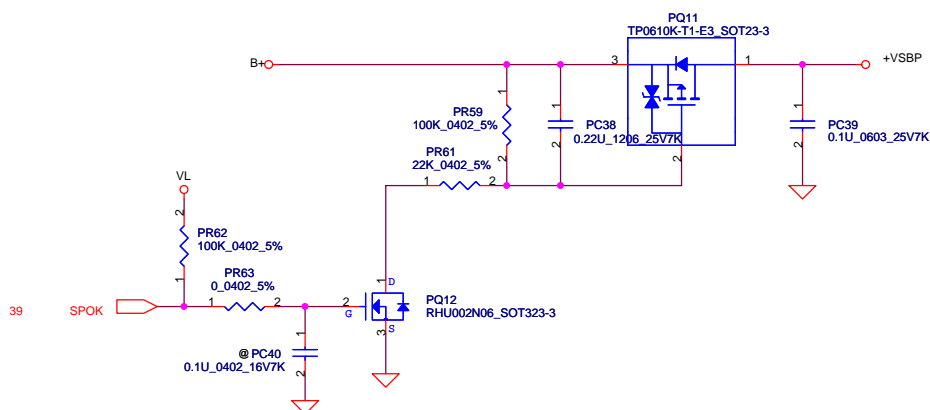
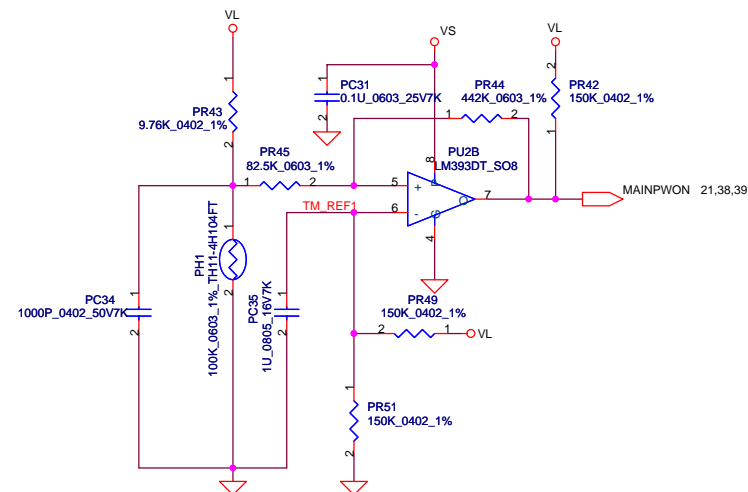
PH1 under CPU botten side :  
CPU thermal protection at 90 degree C  
Recovery at 70 degree C

SUYIN\_200275MR007G161ZL  
PJP2



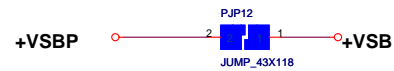
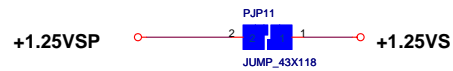
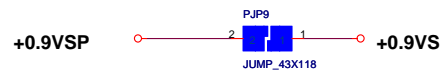
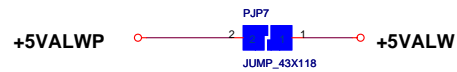
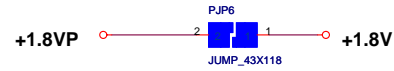
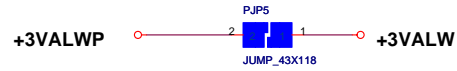
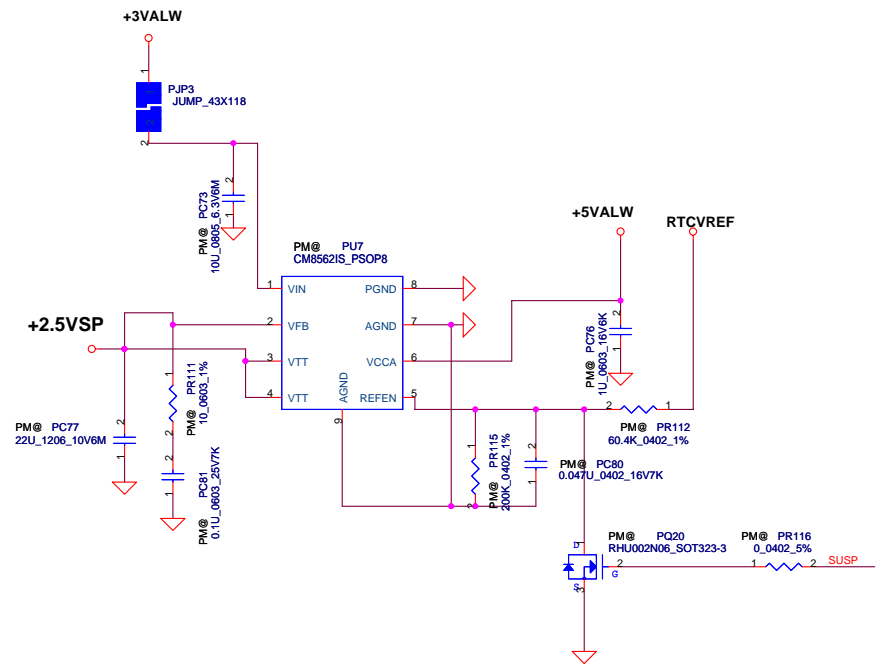
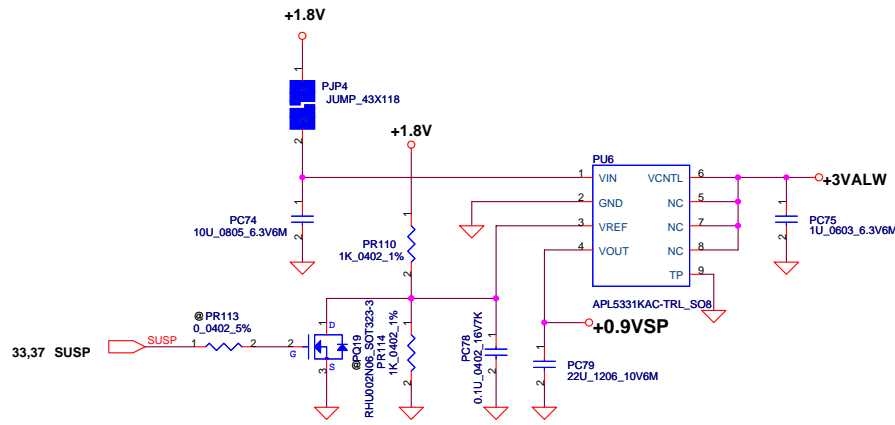
PJP2 battery connector

SMART  
Battery:  
1,2.BATT+  
3.TSA  
4.SMC  
5.SMD  
6,7.GND

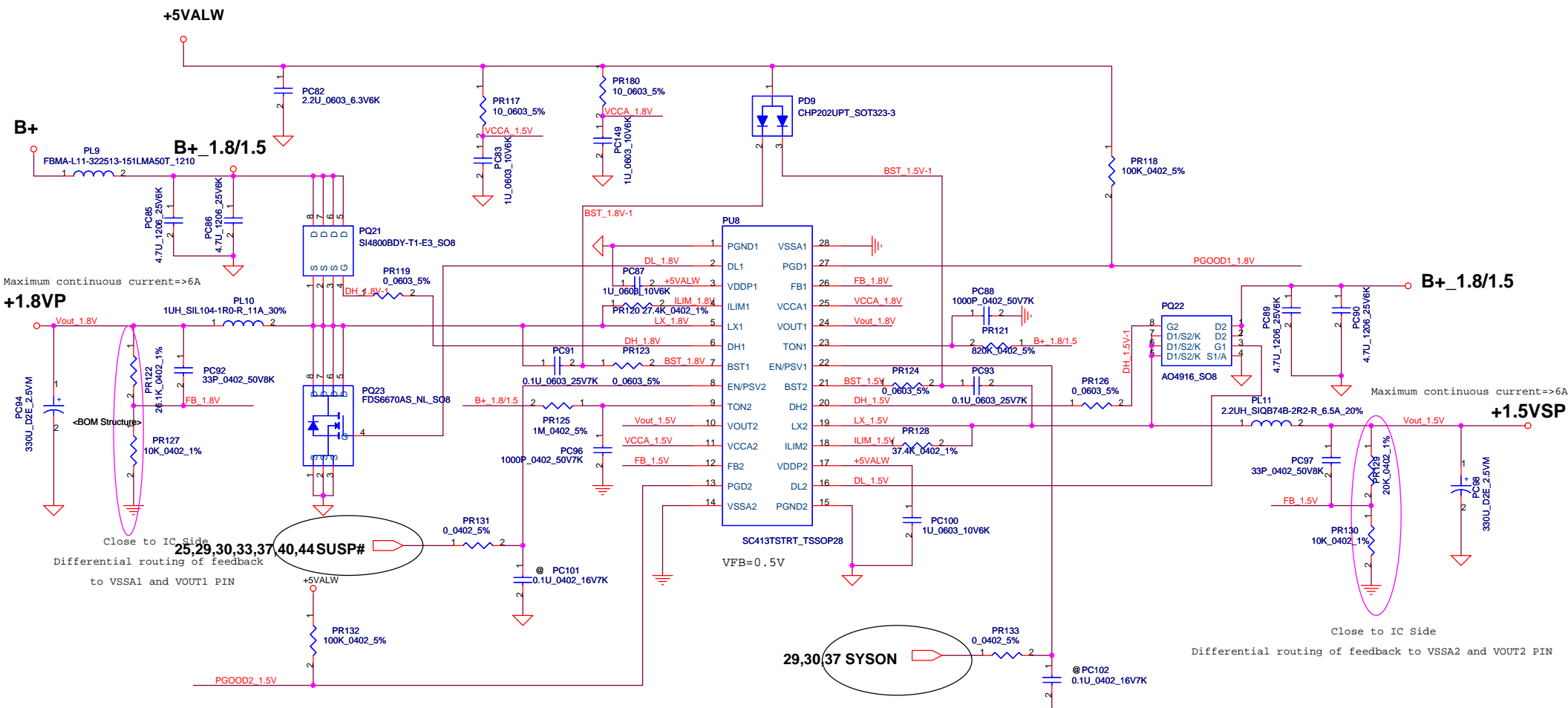


Vin Detector		
Min.	typ.	Max.
H-->L	16.976V	17.257V
L-->H	17.430V	18.384V

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				Date:	Thursday, April 19, 2007
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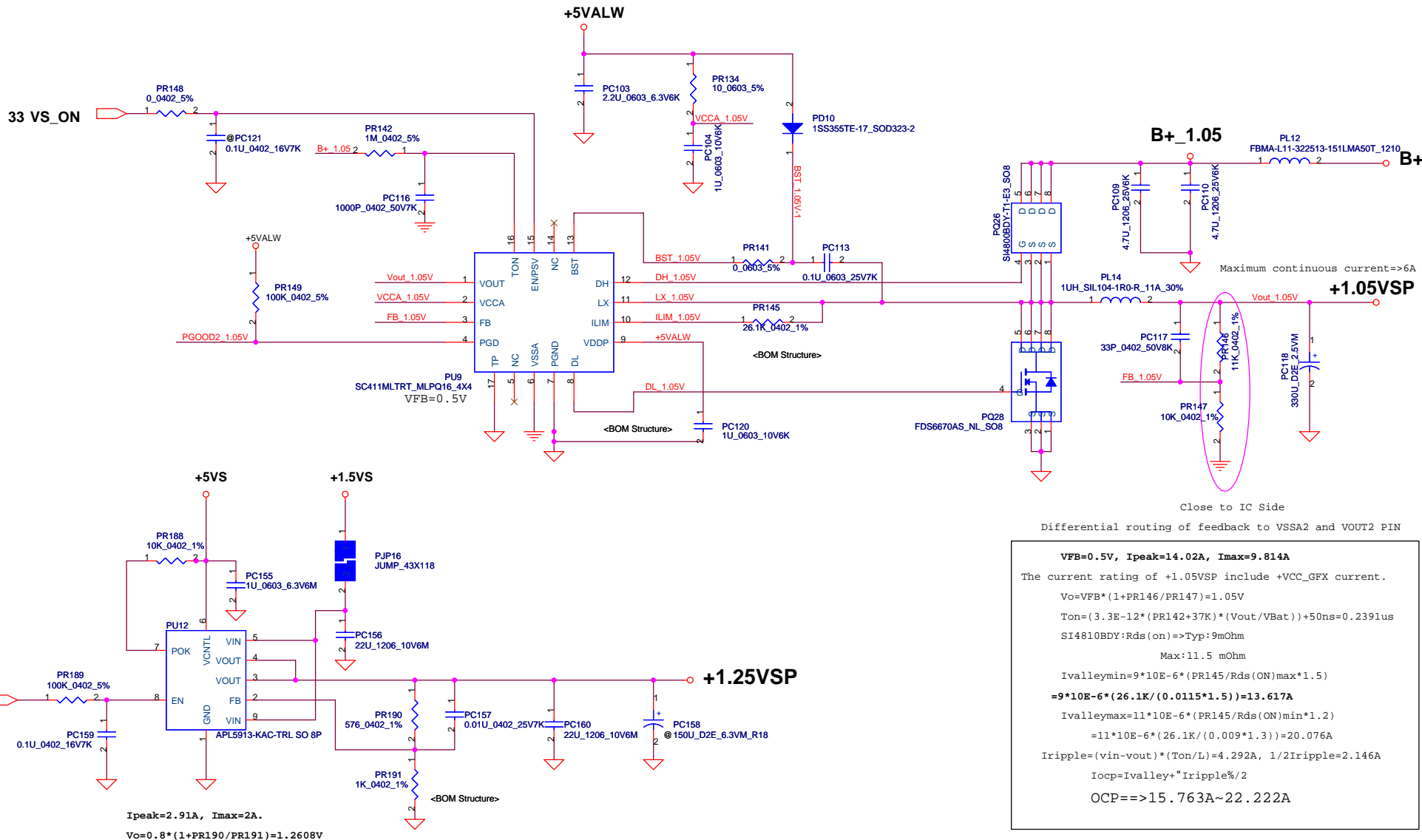
Security Classification		Compal Secret Data				<b>Compal Electronics, Inc.</b>			
Issued Date		2006/08/22		Deciphered Date		2007/08/22		Title	
								+0.9VSP/+2.5VSP	
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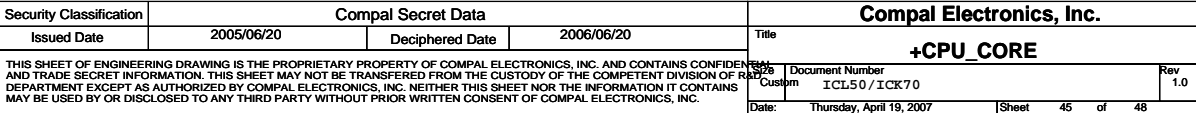
VFB=0.5V  
 $V_o = VFB * (1 + PR122 / PR127) = 1.805V$   
**Ipeak=11.73A, Imax=8.211A**  
 $Ton = (3.3E-12 * (PR121 + 37K) * (Vout / VBat)) + 50ns$   
 $= 3.3 * 10e-12 * (820K + 37K) * (1.8 / 19) + 50ns = 0.3179us$   
FDS6670AS:Rds(on)=>Typ:9 mOhm  
Max:11.5 mOhm  
 $I_{ocp} = I_{valley} + "I_{ripple} \% / 2$   
 $I_{ripple} = (vin - vout) * (Ton / L) = 5.467A, 1/2 I_{ripple} = 2.734A$   
 $I_{valleymin} = 10E-6 * (PR120 / Rds(ON))_{max} * 1.5$   
**= 9\*10e-6 \* (27.4K / 0.0115\*1.5) = 14.295A > 11.73\*1.2 = 14.076A**  
 $I_{valleymax} = 10E-6 * (PR120 / Rds(ON))_{typ} * 1.2$   
 $= 11*10e-6 * (27.4K / 0.009*1.2) = 27.907A$   
**OCP==>17.029A~30.641A**

VFB=0.5V  
 $V_o = VFB * (1 + PR129 / PR130) = 1.5V$   
**Ipeak=4.39A+2.91A=7.3A, Imax=7.3\*0.7=5.11A**  
 $Ton = (3.3E-12 * (PR125 + 37K) * (Vout / VBat)) + 50ns$   
 $= 0.3201us$   
AO4916 Rds(on)=>Typ:21 mOhm  
Max:27 mOhm  
**Ivalleymin=9\*E-6 \* (37.4K / 0.027\*1.4) = 8.904A > 7.3\*1.2 = 8.76A**  
 $I_{valleymax} = 11*E-6 * (37.4K / 0.021*1.1) = 17.809A$   
 $I_{ripple} = (vin - vout) * (Ton / L) = 2.546A, 1/2 I_{ripple} = 1.273A$   
 $I_{ocp} = I_{valley} + "I_{ripple} \% / 2$   
**OCP==>10.177A~19.082A**

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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	CPU_CORE high side MOS desine change	In order to prevent EOL of SI7840, change to SI7686.	0.1	45	Change PQ13 and PQ16 form SB578400080(S TR SI7840DP-T1-E3 1N SO8) to SB000008L80(S TR SI7686DP-T1-E3 1N SO8).	10/30/06	EVT
2	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ43 SB906100210( S TR TP0610K)	12/21/06	DVT
3	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ44 SB301150000(S TR DTC115EUA)	12/21/06	DVT
4	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD16 SC1SS355010( S DIO 1SS355) Delete PD12 SC1SS355010( S DIO 1SS355)	12/21/06	DVT
5	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PD17 SCSB715F000(S DIO RB715F)	12/21/06	DVT
6	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR184,PR185 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
7	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC153 SE076104K80(S CER CAP 0.1U 0402 16V K X7R)	12/21/06	DVT
8	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ45 SB502060000(S TR RHU002N06)	12/21/06	DVT
9	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PQ46 SB324110010(S TR 2SC411K)	12/21/06	DVT
10	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR183 SD034274380(S RES 1/16W 274K 0402 1%)	12/21/06	DVT
11	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR186 SD034100380(S RES 1/16W 100K 0402 1%)	12/21/06	DVT
12	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PR187 SD034200280(S RES 1/16W 20K 0402 1%)	12/21/06	DVT
13	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Add PC154 and PC146 SE075103K80(S CER CAP 0.01U K 25V X7R 0402)	12/21/06	DVT
14	Noise issue in S3 mode and idle mode.	In order to prevent noise issue in S3 mode and idle mode.	0.2	40	Add PC42 SF22004M210(S CAP 220U_25V_M)	12/21/06	DVT
15	For energy star SPEC request.	In order to for energy star SPEC request.	0.2	40	Change PR157 from SD028000080(s res 1/16w 0 0402 5%) TO SD0281000280(S RES 1/16W 10K 0402 5%)	12/21/06	DVT
16	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR34 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100380(S RES 1/16W 100K 0402 5%)	12/21/06	DVT
17	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PR35 SD028100380( S RES 1/16W 100K 0402 5%) to SD028200380(S RES 1/16W 200K 0402 5%)	12/21/06	DVT
18	Improve pre-charge power sequence	Improve pre-charge power sequence	0.2	39	Change PC28 from SE042104K80(S CER CAP 0.1U 25V K X7R 0603) to SE000005ZM8(S CER CAP 0.22U 25V K X7R 0603)	12/21/06	DVT
19	CPU MOSFET switching has interference.	Improve CPU switching interference.	0.2	45	Change PC69,PC70,PC71,PC72 from SE082221J80 to SE068102J80 (S CER CAP 1000P 25V J NPO 0402)	12/21/06	DVT
20	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PU7 SA085620080 from X63470BOL01.	12/21/06	DVT
21	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PQ20 SB502060000 from X63470BOL01.	12/21/06	DVT
22	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR111 SD014100A80 from X63470BOL01.	12/21/06	DVT
23	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR112 SD034604280 from X63470BOL01.	12/21/06	DVT

Compal Electronics, Inc.

Title			
PIR (PWR)			
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR115 SD034200380 from X63470BOL01.	10/30/06	EVT
2	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PR116 SD028000080 from X63470BOL01.	12/21/06	DVT
3	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC73 SE142475K80 from X63470BOL01.	12/21/06	DVT
4	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC76 SE135105K80 from X63470BOL01.	12/21/06	DVT
5	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC77 SE116226M80 from X63470BOL01.	12/21/06	DVT
6	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC80 SE076473K80 from X63470BOL01.	12/21/06	DVT
7	X63470BOL01 doesn't need +2.5VSP	Delete +2.5VSP from X63470BOL01.	0.2	42	Delete PC81 SE042104K80 from X63470BOL01.	12/21/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ25 SB548000310(S TR SI4800BDY).	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PQ27 SB548100020(S TR 4810BDY)	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PD10 from SC1P202U010 to SC1SS355010.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR135 SD034100380.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR140,SD013000080, PR150 SD028000080.	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR181 SD013100A80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR139 SD034150280.	12/27/06	DVT
15	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR144 SD034100280	12/27/06	DVT
16	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR137 SD034105280.	12/27/06	DVT
17	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PR138 SD028100480.	12/27/06	DVT
18	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC105,PC106 SE142475K80.	12/27/06	DVT
19	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC107,PC151 SE080105K80.	12/27/06	DVT
20	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC108 SE074102K80.	12/27/06	DVT
21	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC111 SE042104K80.	12/27/06	DVT
22	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC112 SE068330K80	12/27/06	DVT
24	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PL13 SH000008Y80.	12/27/06	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Delete PC114 SGA20221D30	12/27/06	DVT
2	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Change PU9 from SA00001FD80 to SA00001FB80	12/27/06	DVT
3	For SMT BOM convenient.	For SMT BOM convenient.	0.3	40	Change PD14 from SC1H751H010 to SC1B751V010.	12/27/06	DVT
4	Increase _1.5VSP OCP point	Increase _1.5VSP OCP point for +1.25VSP new solution.'	0.3	43	Change PR128 from SD034154280 to SD034374380.	12/27/06	DVT
5	Decrease +1.05VSP OCP point.	Decrease +1.05VSP OCP point.	0.3	44	Change PR145 from SD034324280 to SD034261280		DVT
6	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PU12 SA000015410.	12/27/06	DVT
7	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR188 SD034100280.	12/27/06	DVT
8	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR189 SD034100380.	12/27/06	DVT
9	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR191 SD034100180.	12/27/06	DVT
10	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PR190 SD034576080.	12/27/06	DVT
11	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC155 SE107105M80.	12/27/06	DVT
12	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC156, PC160 SE116226M80	12/27/06	DVT
13	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC157 SE075103K80.	12/27/06	DVT
14	Cost issue.	For cost down, change +1.25VSP solution.	0.3	44	Add PC159 SE076104K80.	12/27/06	DVT
15	Increase +1.5VSP output capacitor.	Increase +1.5VSP output capacitor.	0.3	43	Change PC98 from SGA20221D30 to SGA19331D00	12/27/06	DVT
16	Cost issue.	Cost issue.	0.3	44	Change PC118 from SGA20471D00 to SGA19331D00.	12/30/06	DVT
17	BOM issue.	BOM issue.	0.3	45	Change PH3, PH4 from SL210021F20 to SL200000200	12/30/06	DVT
18	Assembly issue.	Due to assembly hard, delete PC42.	0.3	45	Delete PC42 SM22004M210.	12/30/06	DVT
19	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE142475K80 to SE093106M80	01/04/06	DVT
20	Cost issue.	Cost issue.	0.4	42	Change PC73 from SE153106K80 to SE093106M80	01/04/06	DVT
21	Add pull high resister for VAGTE.	Add pull high resister for VAGTE.	0.4	45	Add PR89 SD034200180(S RES 1/16W 2K 0402 1%)	01/04/06	DVT
22	Delete PQ46	PQ46 has potential risk to cause system battery OVP.	0.4	40	Delete PQ46 SB324110010(S TR 2SC411K)	01/04/06	DVT
23	Material shipping issue.	Material shipping issue.	0.4	45	Change PC69, PC70, PC71, PC72 from SE068102J80 to SE074102K80	01/04/06	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Cost down	Cost down	0.5	40	Change PQ38 from SB548100020 to SB548000310.	03/09/07	PVT
2	Cost down	Cost down	0.5	40	Change PQ40 from SB548100020 to SB548000310.	03/09/07	PVT
3	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PR199 SD001470B80(S RES 1/4W 4.7 1206 +-5%)	04/01/07	Pre-MP
4	For EMI board band issue.	For EMI board band issue.	0.6	40	Add PC163 SE074681K80( S CER CAP 680P 50V K X7R)	04/01/07	Pre-MP
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