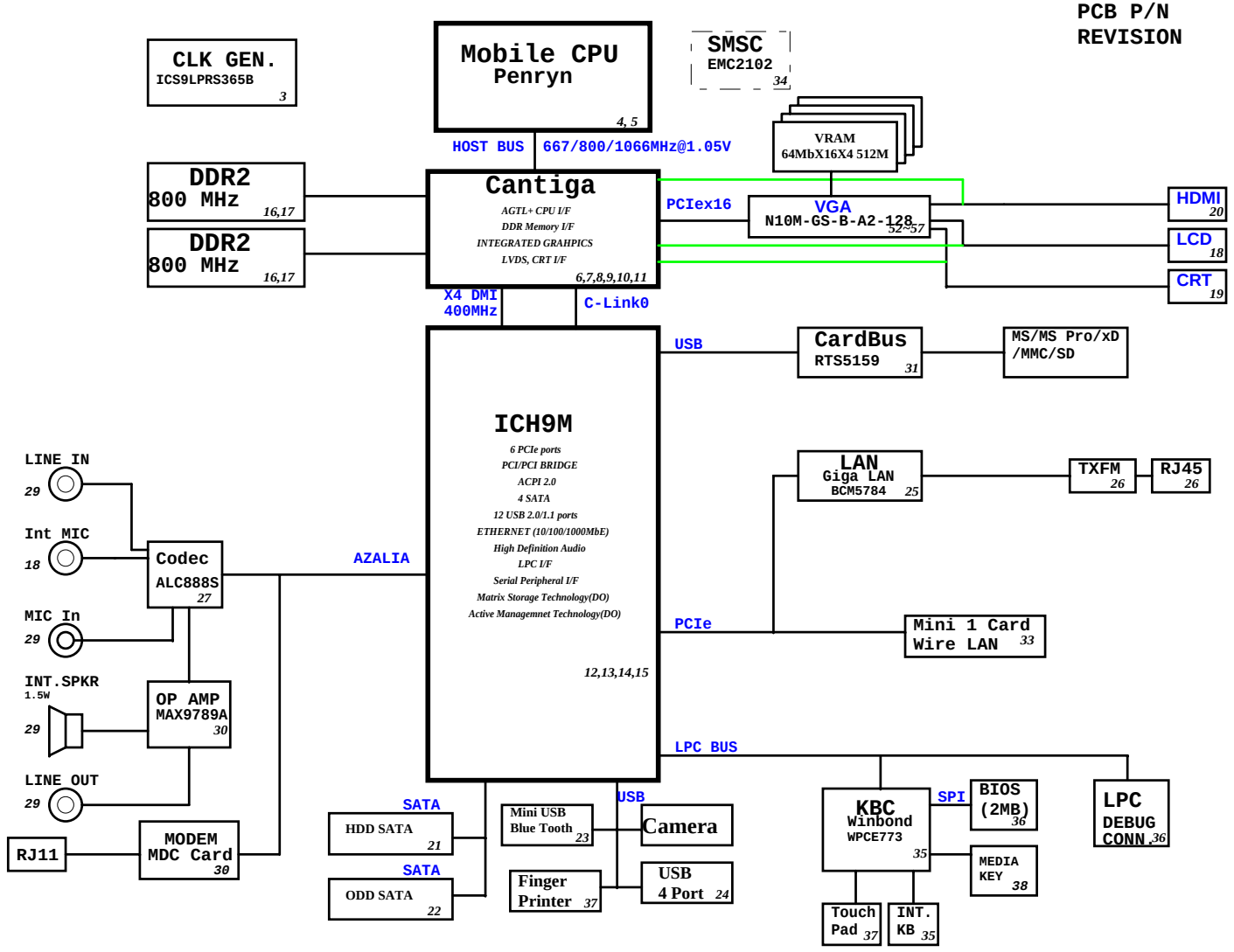
JV71-MV Block Diagram

Project code: 91.4FX01.001
PCB P/N : 48.4FX01.0SA
REVISION : 09242 -1



SYSTEM DC/DC
ISL62392 42

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC
TPS51124 43

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D5V_S3(12A)

RT9026 44

1D5V_S3	DDR_VREF_S3 (1.2A)

RT9018 44

1D5V_S3	1D1V_S0(2A)

TPS51117 45

DCBATOUT	FBVDD(4A)

CHARGER
ISL88731A 47

INPUTS	OUTPUTS
DCBATOUT	BT+

CPU DC/DC
ISL6266A 41

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A

VGA_CORE
RT8202A 47

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A

GFXCORE
ISL6263A 46

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

PCB STACKUP

TOP	———	L1
GND	———	L2
S	———	L3
S	———	L4
GND	———	L5
BOTTOM	———	L6

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
A2	JV71	-2

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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Title: Reference

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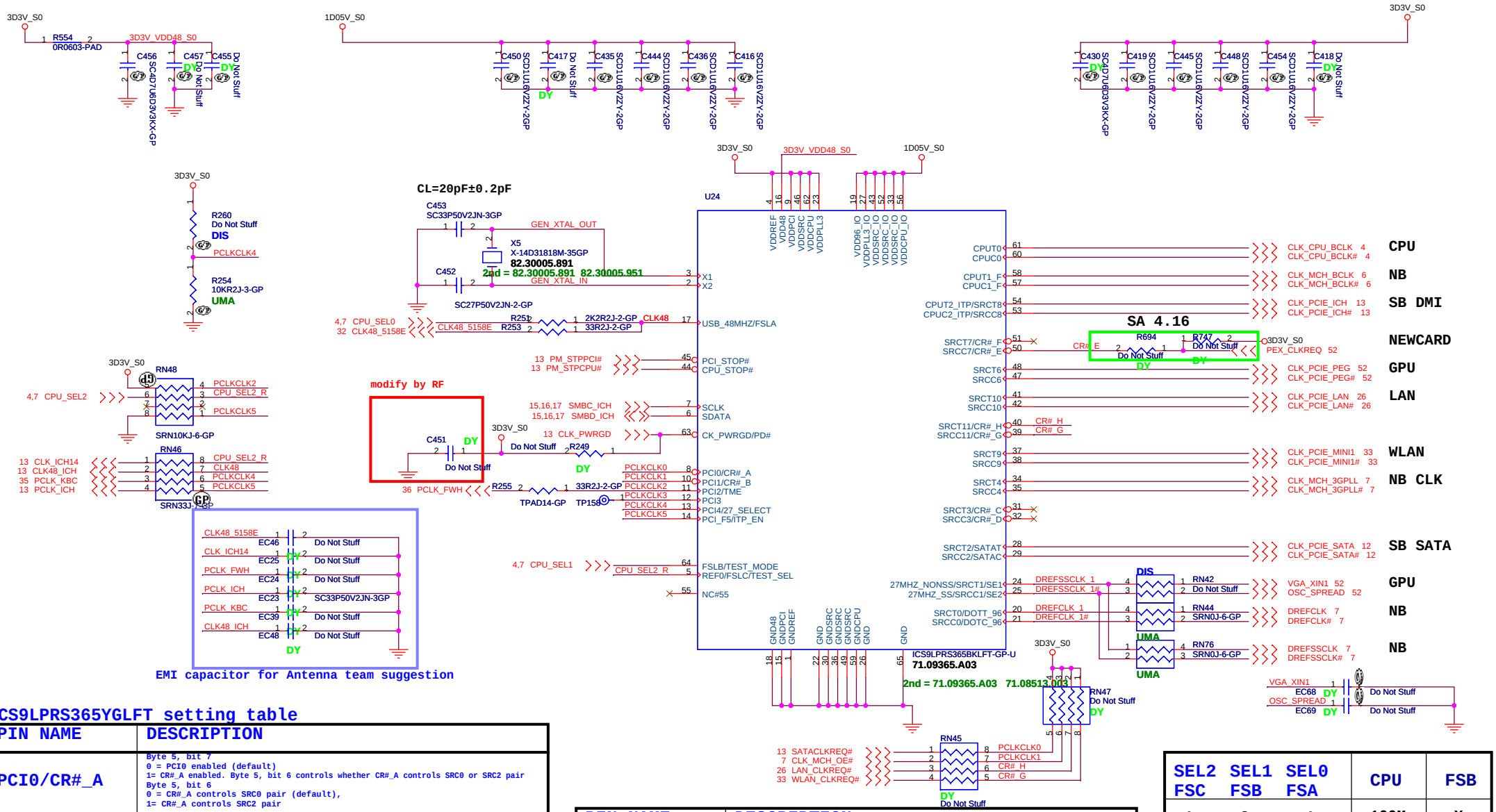

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: Clock Generator

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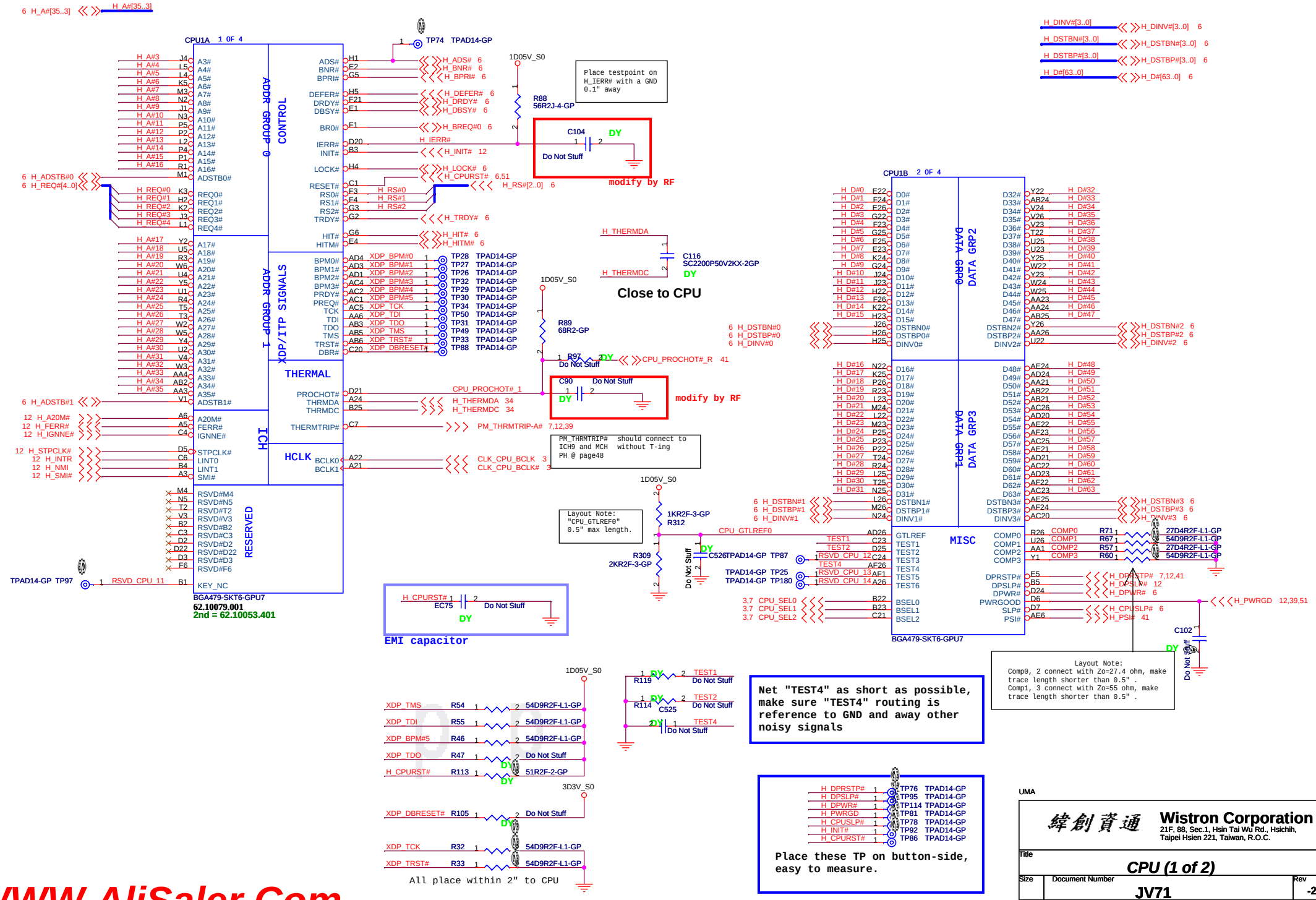

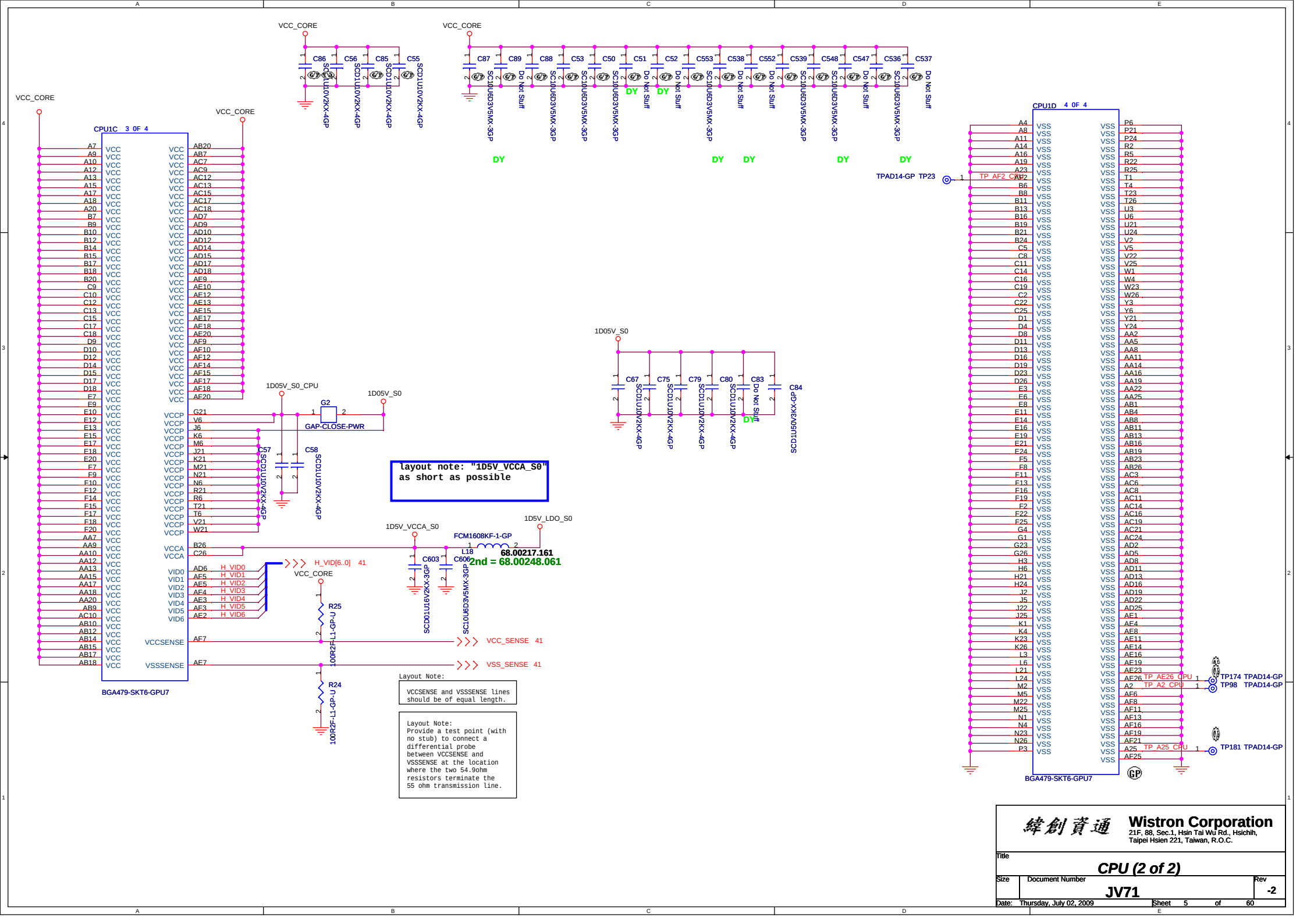

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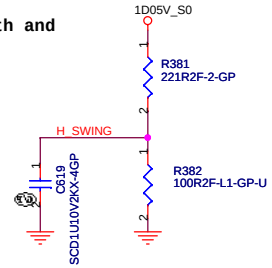
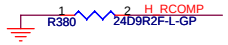
H_SWING routing Trace width and Spacing use 10 / 20 mil

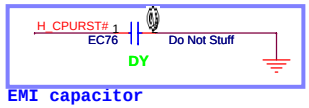
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



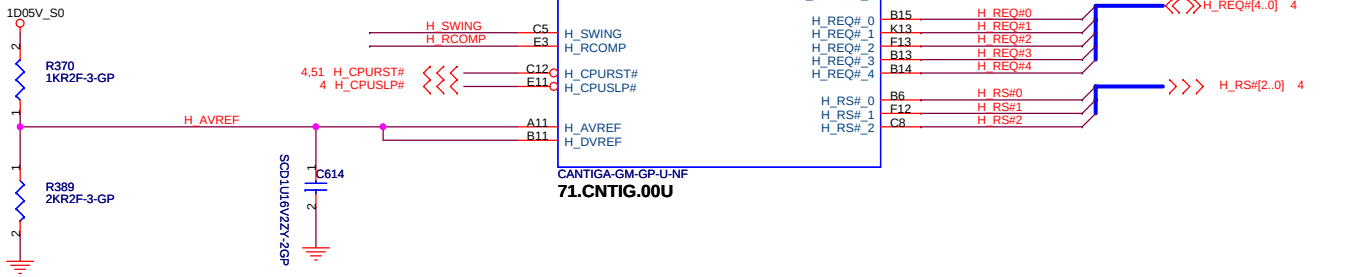
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



EMI capacitor



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Title	***Cantiga (1 of 6)***	
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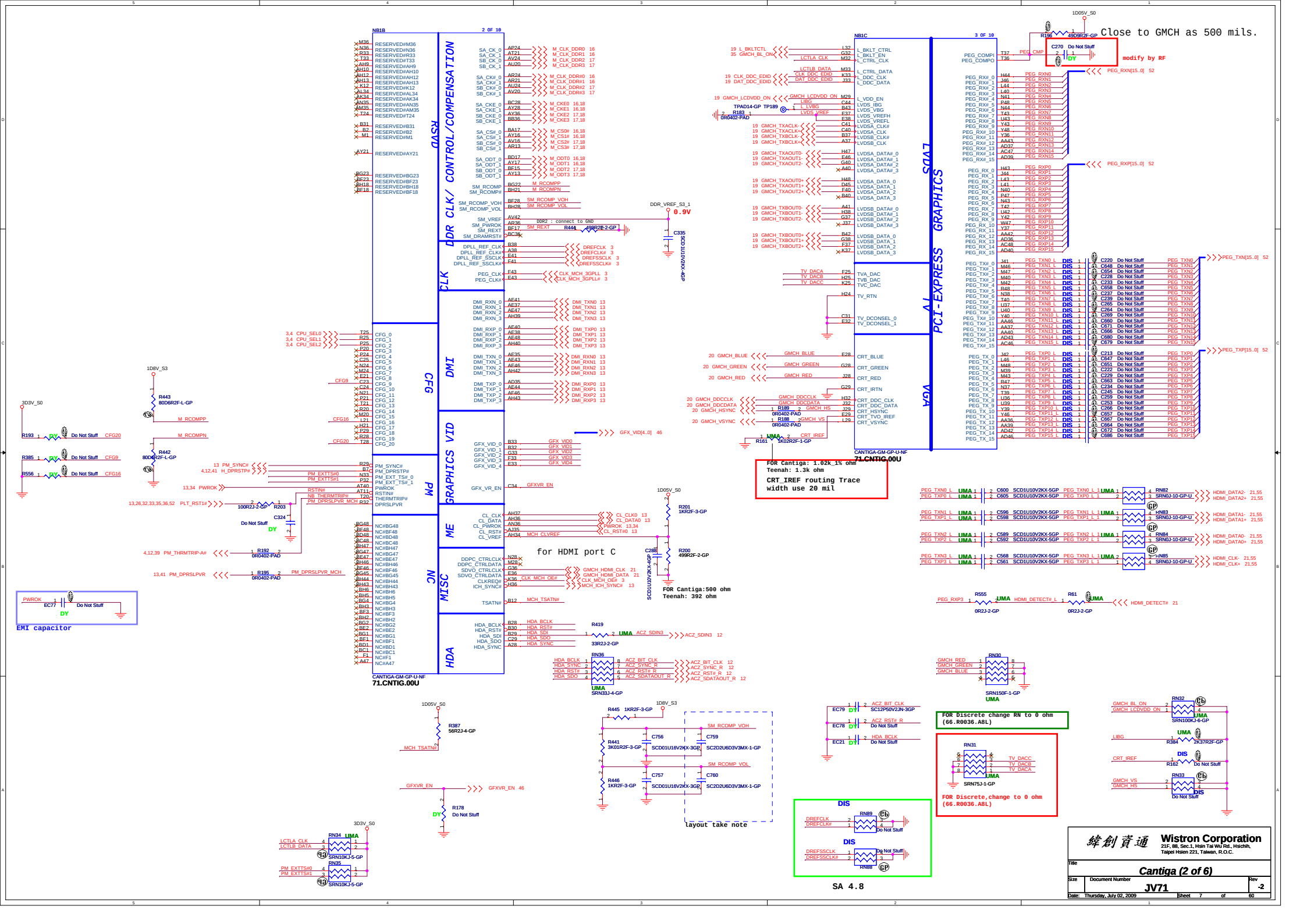
Close to GMCH as 500 mils.
modify by RF
FOR Cantiga 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
for HDMI port C
FOR Cantiga:500 ohm
Teenah: 392 ohm
layout take note
FOR Discrete change RN to 0 ohm (66.R0036.A8L)
FOR Discrete,change to 0 ohm (66.R0036.A8L)
EMI capacitor
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
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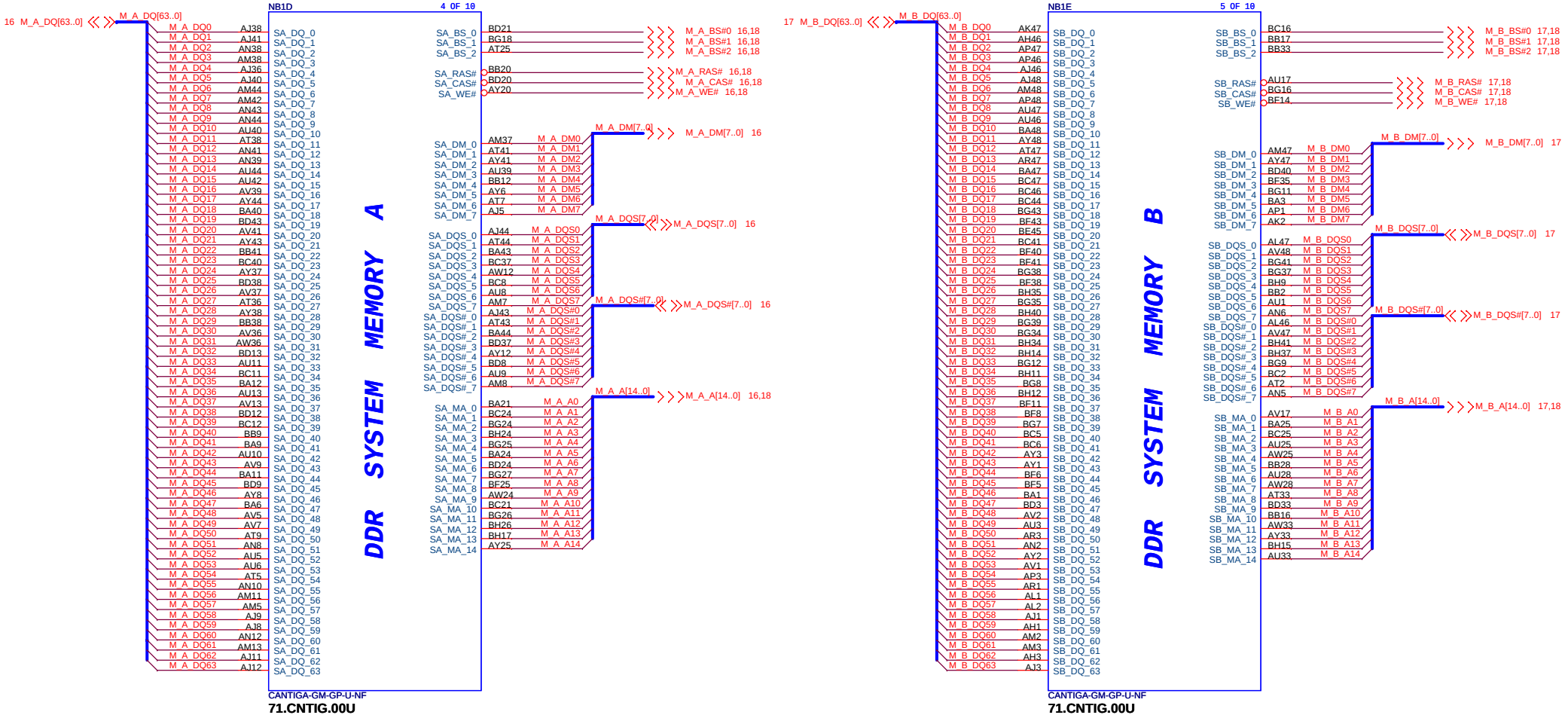
Cantiga (2 of 6)
JV71
Thursday, July 02, 2009
SA 4.8



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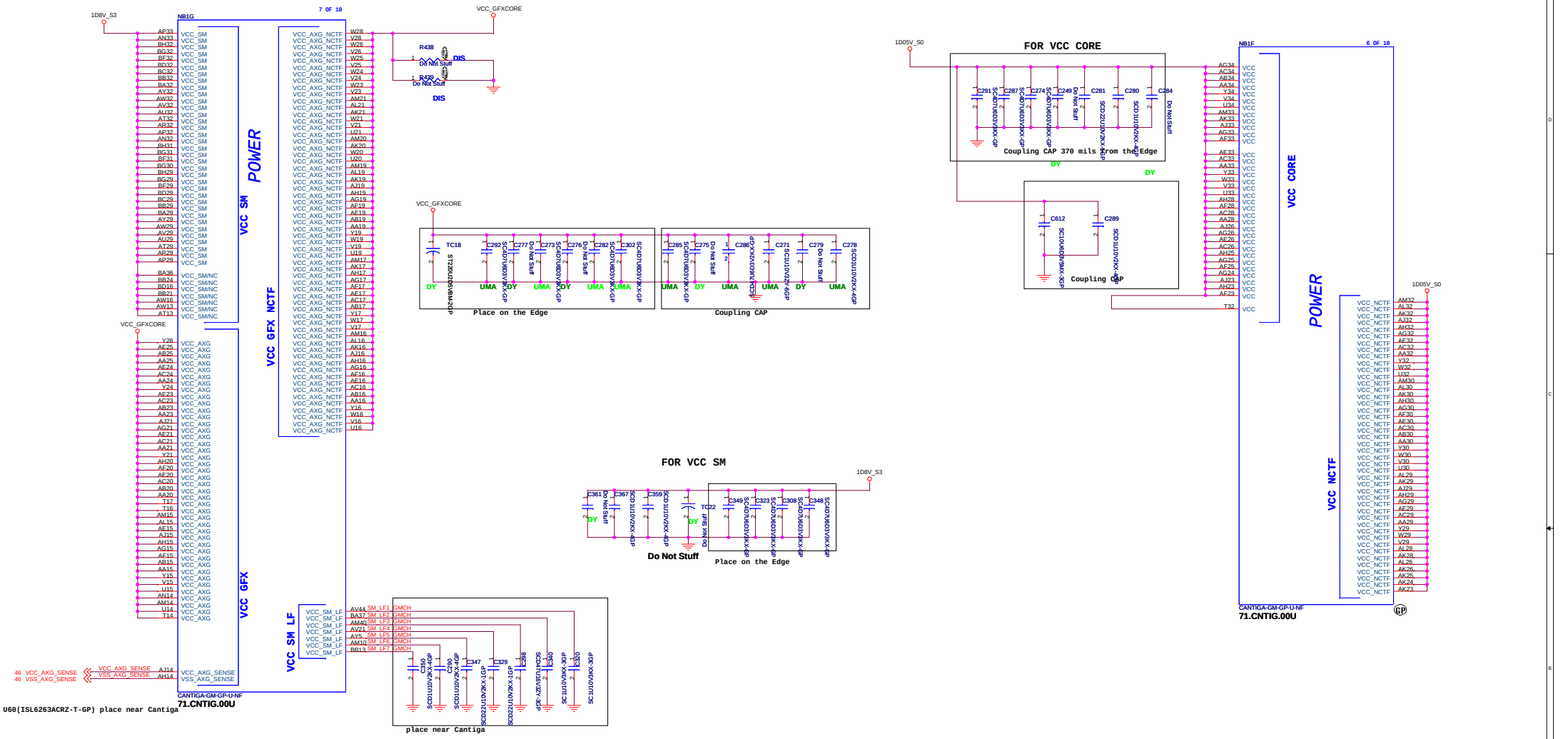

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Title	***Cantiga (4 of 6)***	
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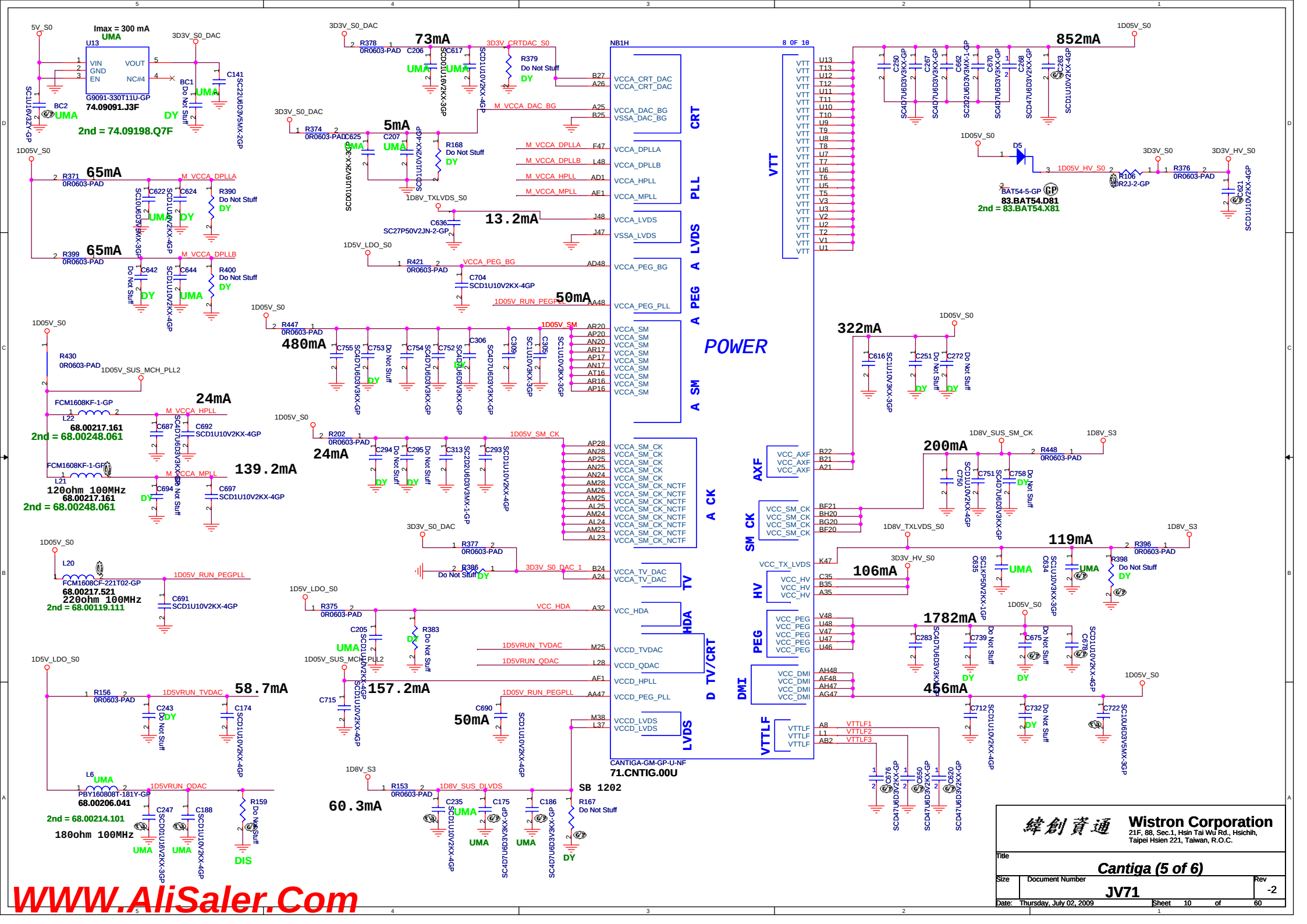
POWER
NB1H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
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Title
Cantiga (5 of 6)
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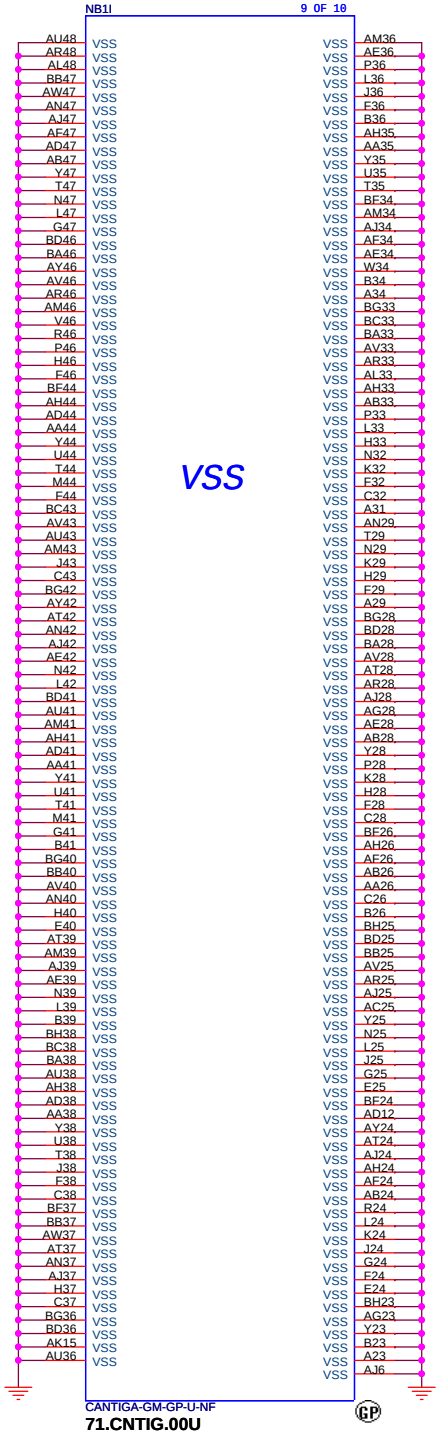

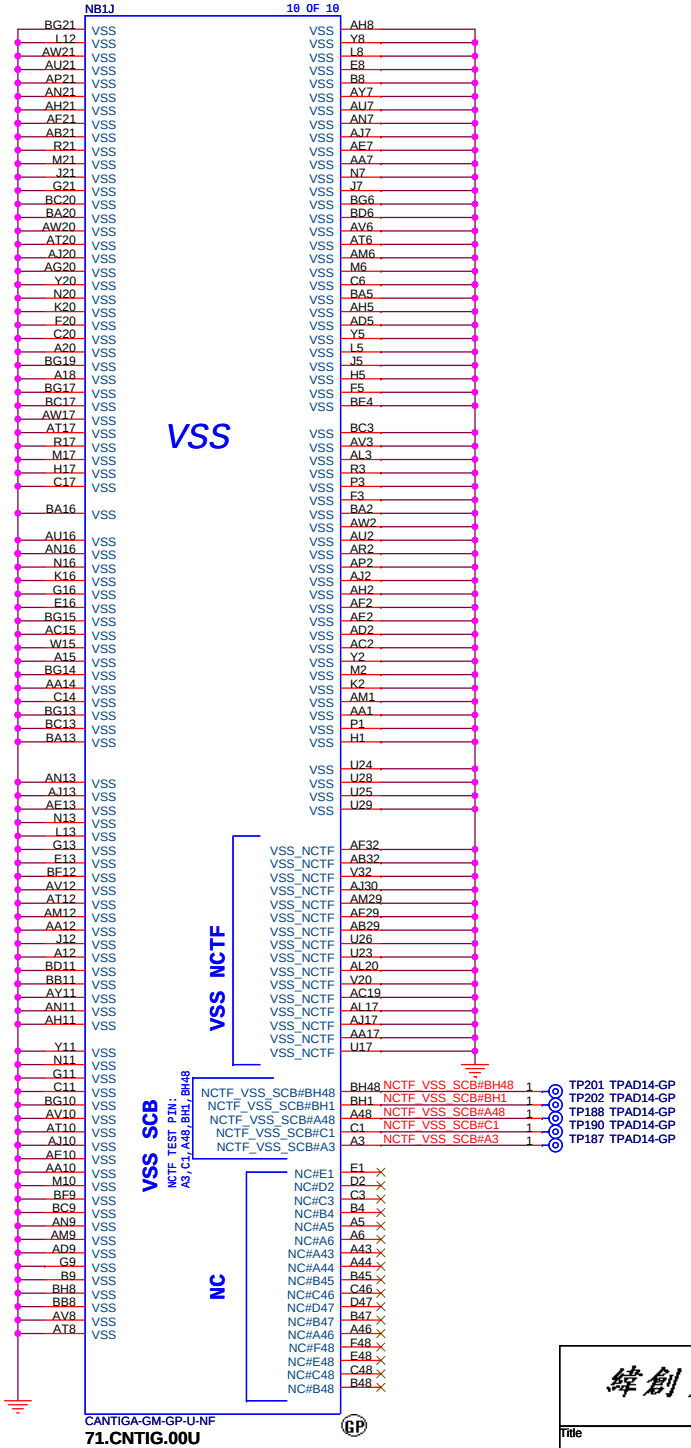

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Title: ***Cantiga (6 of 6)***

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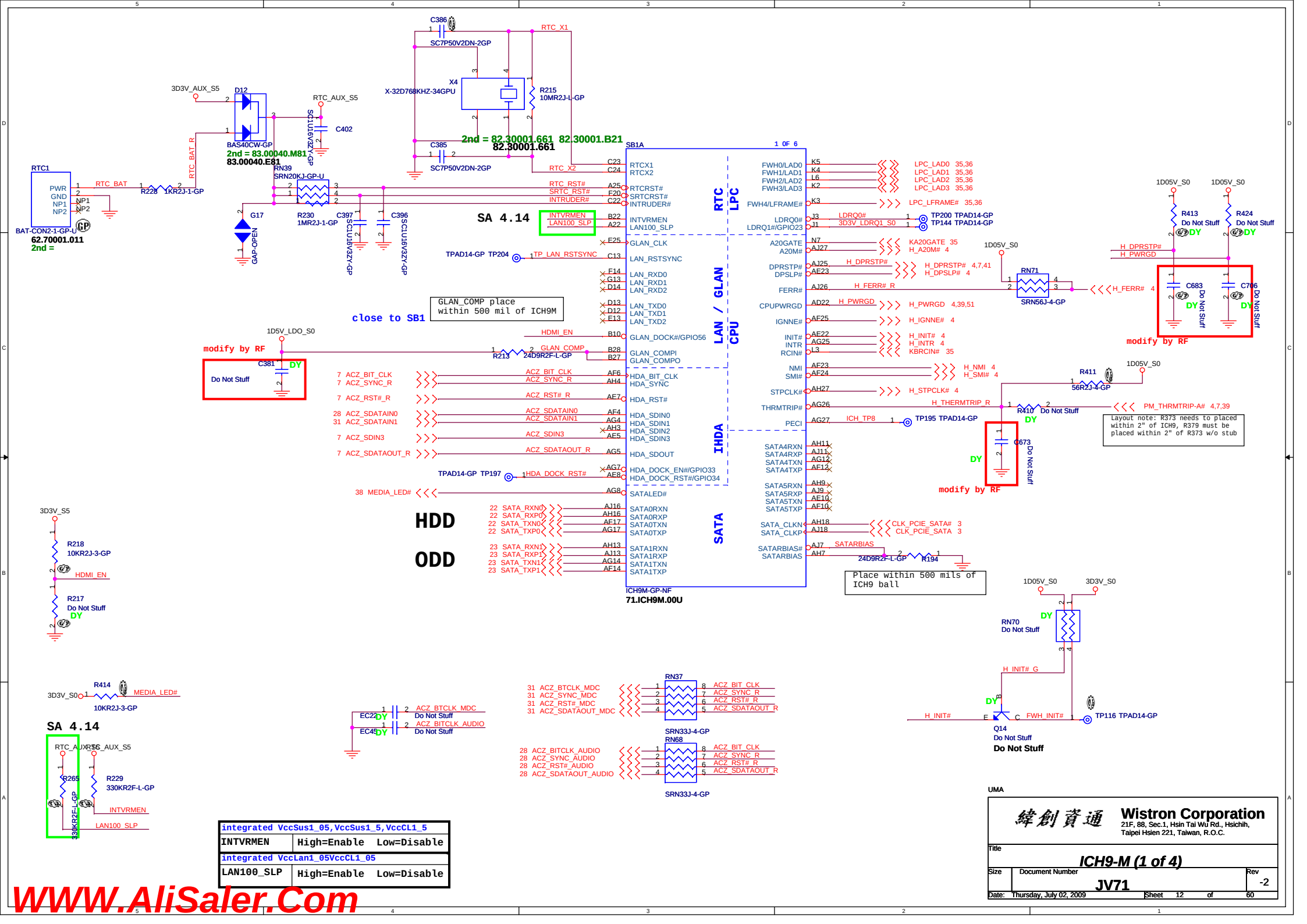
SB1A
1 0F 6
ICH9M-GP-NF
71.ICH9M.00U
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
HDD
ODD
SA 4.14
close to SB1
GLAN_COMP place within 500 mil of ICH9M
Place within 500 mils of ICH9 ball
modify by RF
Do Not Stuff
DY
2nd = 82.30001.661 82.30001.B21
82.30001.661
2nd = 83.00040.M81
83.00040.E81
62.70001.011
2nd =
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
UMA
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Title
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PCI_GNT#0 and SPI_CS1#
have weak internal Pull up

SB1B 2 OF 6

PCI

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31

REQ0# GNT0# REQ1#/GPIO50 GNT1#/GPIO51 REQ2#/GPIO52 GNT2#/GPIO53 REQ3#/GPIO54 GNT3#/GPIO55

C/BE0# C/BE1# C/BE2# C/BE3#

IRDY# PAR PCIRST# DEVSEL# PERR# PLOCK# SERR# STOP# TRDY# FRAME#

PLTRST# PCICLK PME#

PCI_REQ#0 PCI_REQ#1 PCI_REQ#2 PCI_REQ#3 PCI_IRDY# PCI_DEVSEL# PCI_PERR# PCI_LOCK# PCI_SERR# PCI_STOP# PCI_TRDY# PCI_FRAME# PCI_RST# R1 R216 2 0R0402-PAD PLT_RST1# 7,26,32,33,35,36,52 PCLK_ICH 3

C388 Do Not Stuff DY

Interrupt I/F

INT_PIRQA# INT_PIRQB# INT_PIRQC# INT_PIRQD# J5 E1 J6 C4

PIRQA# PIRQB# PIRQC# PIRQD#

PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5

INT_PIRQE# INT_PIRQF# INT_PIRQG# INT_PIRQH#

ICH9M-GP-NF
71.ICH9M.00U

SB1C 3 OF 6

15,26,33 SMB_CLK
15,26,33 SMB_DATA

SMBCLK SMBDATA LINKALERT#/GPIO60/CLGPIO4 SMLINK0 SMLINK1

SMB_LINK_ALERT#

RI# PM_RI# TPAD14-GP TP199 PM_SUS_STAT# DBRESET#

SUS_STAT#/LPCPD# SYS_RESET#

7 PM_SYNC#

PMSYNC#/GPIO0

SMB_ALERT#

SMBALERT#/GPIO11

3 PM_STPPCI# 3 PM_STPCPU#

STP_PCI# STP_CPU#

35 PM_CLKRUN#

CLKRUN#

26 PCIE_WAKE# 35 INT_SERIRQ 34 THRM#

WAKE# SERIRQ THRM#

34,41 VGATE_PWRGD

VRMPWRGD

SST

TACH1/GPIO1 TACH2/GPIO6 TACH3/GPIO7 GPIO8 LAN_PHY_PWR_CTRL/GPIO12 ENERGY_DETECT/GPIO13 TACH0/GPIO17 GPIO18 GPIO20 SCLOCK/GPIO22 GPIO27 GPIO28 SATACLKREQ#/GPIO35 SLOAD/GPIO38 SDATAOUT0/GPIO39 SDATAOUT1/GPIO48 GPIO49 GPIO57/CLGPIO5

SPKR MCH_SYNC# TP3 PWM0 PWM1 PWM2

SMB

SATA GPIO

SATA0GP/GPIO21 SATA1GP/GPIO19 SATA4GP/GPIO36 SATA5GP/GPIO37

AH23 SATA0GP AF19 SATA1GP AE21 ICH_GPIO36 AD20 ICH_GPIO37

RN72 SRN10KJ-6-GP

Clocks

CLK14 CLK48

H1 AF3 P1

CLK_ICH14 3 CLK48_ICH 3 PM_SUS_CLK 34

SYS GPIO

SLP_S3# SLP_S4# SLP_S5#

C16 E16 G17 PM_SLP_S3# 28,34,35,39,43,44 PM_SLP_S4# 35,43,44 PM_SLP_S5# TP203 TPAD14-GP

S4_STATE#/GPIO26 C10 S4_STATE# TP207 TPAD14-GP

PWROK G20 PWROK 7,34

Power MGT

DPRSLPVR/GPIO16 M2 PM_DPRSLPVR 1 R211 R212 100R2J-2-GP DY Do Not Stuff PM_DPRSLPVR 7,41

BATLOW# B13 PM_BATLOW# R

PWRBTN# R3 PWRBTN# ICH D8 BAS16-1-GP PM_PWRBTN# 35,51

LAN_RST# D20

RSMRST# D22 RSMRST# SB

CK_PWRGD R5 CLK_PWRGD 3

CLPWROK R6 PWROK 7,34

SLP_M# B16 PM_SLP_M# 1 TP148 TPAD14-GP

CL_CLK0 CL_CLK1 F24 B19 CL_CLK0 7

CL_DATA0 CL_DATA1 F22 C19 CL_DATA0 7

CL_VREF0 CL_VREF1 C25 A19 CL_VREF0_ICH

CL_RST0# CL_RST1# F21 D18 CL_RST#0 7

GPIO24/MEM_LED A16 ICH_GPIO24 1 TP153 TPAD14-GP

GPIO10/SUS_PWR_ACK C18 SUSPWRACK

GPIO14/AC_PRESENT C11 AC_PRESENT

GPIO9/WOL_EN C20 ICH_GPIO9 1 TP206 TPAD14-GP

GPIO

Controller Link

MISC

83.00016.B11 2nd = 83.00016.F11

3D3V_S0 R404 10KR2J-3-GP GAP-OPEN G78

TPAD14-GP TP196 TPAD14-GP TP122 ICH9_GPIO20 CLK_SEL1 AJ22

TPAD14-GP TP193 FP_ID AG19 35 EC_TMR AH21 35 ECSCI#_1 AG21 35 ECSWI# A21

R221 DY ICH_TP7 A20 Do Not Stuff

PSW_CLR# AE18 K1

3 SATACLKREQ# TPAD14-GP TP198 TPAD14-GP TP194 SATACLKREQ# PCB_VER0_SB AE19 PCB_VER1_SB AG22 MIC_SEL_1 AF21 NO_iTPM AH24 A8

7 MCH_ICH_SYNC# TPAD14-GP TP205 ICH_TP3 M7 AJ24 B21 AH20 AJ20 AJ21

GPIO049 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.

3D3V_S0 R226 3K24R2F-GP C409 SCD1U10V2KX-4GP R227 453R2F-1-GP 3D3V_S5

R220 100KR2J-1-GP 3D3V_S5

SA 4.14

RN73 SRN10KJ-6-GP

USB_OC#0 USB_OC#1 USB_OC#3

SB1D 4 OF 6

PCI-Express

PERN1 PERP1 PETP1 PETN1

PERN2 PERP2 PETN2 PETP2

PERN3 PERP3 PETN3 PETP3

PERN4 PERP4 PETN4 PETP4

PERN5 PERP5 PETN5 PETP5

PERN6/GLAN_RXN PERP6/GLAN_RXP PETN6/GLAN_TXN PETP6/GLAN_TXP

SPI_CLK SPI_CS0# SPI_CS1#/GPIO58/CLGPIO6 SPI_MOSI SPI_MISO

SPI

USB

OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO29 OC6#/GPIO30 OC7#/GPIO31 OC8#/GPIO44 OC9#/GPIO45 OC10#/GPIO46 OC11#/GPIO47

USBRBIAS USBRBIAS#

Direct Media Interface

DMI0RXN DMI0RXP DMI0TXN DMI0TXP

DMI1RXN DMI1RXP DMI1TXN DMI1TXP

DMI2RXN DMI2RXP DMI2TXN DMI2TXP

DMI3RXN DMI3RXP DMI3TXN DMI3TXP

DMI_CLKN DMI_CLKP

DMI_ZCOMP DMI_IRCOMP

USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P

ICH9M-GP-NF
71.ICH9M.00U

26 PCIE_RXN1 26 PCIE_RXP1 26 PCIE_TXN1 26 PCIE_TXP1

C363 SCD1U10V2KX-5GP C360 SCD1U10V2KX-5GP TXN1 TXP1

LAN

33 PCIE_RXN2 33 PCIE_RXP2 33 PCIE_TXN2 33 PCIE_TXP2

C369 SCD1U10V2KX-5GP C365 SCD1U10V2KX-5GP TXN2 TXP2

MINICARD1

DMI_RXN0 7 DMI_RXP0 7 DMI_TXN0 7 DMI_TXP0 7

DMI_RXN1 7 DMI_RXP1 7 DMI_TXN1 7 DMI_TXP1 7

DMI_RXN2 7 DMI_RXP2 7 DMI_TXN2 7 DMI_TXP2 7

DMI_RXN3 7 DMI_RXP3 7 DMI_TXN3 7 DMI_TXP3 7

CLK_PCIE_ICH# 3 CLK_PCIE_ICH 3

DMI_IRCOMP_R

R417 24D9R2F-L-GP 1D5V_LDO_S0

USBPN0 25 USBPP0 25 USBPN1 25 USBPP1 25 USBPN2 25 USBPP2 25 USBPN3 33 USBPP3 33 USBPN4 19 USBPP4 19

USBPN6 37 USBPP6 37 USBPN7 24 USBPP7 24

USBPN9 25 USBPP9 25

USBPN11 32 USBPP11 32

SA 4.14

25 USB_OC#0 25 USB_OC#1 25 USB_OC#9

USB_OC#0 USB_OC#1 USB_OC#3 USB_OC#4 USB_OC#5 USB_OC#6 USB_OC#7 USB_OC#8 USB_OC#9 USB_OC#10 USB_OC#11

USB_RBIAS_PN AG2 AG1 R415 22D6R2F-L1-GP

SPI_ICH_CS1# F23

These R need close SB within 600 mils

EMI capacitor

EC81 DY VGATE_PWRGD Do Not Stuff

EC80 DY CLK_PWRGD Do Not Stuff

RP1 SRN10KJ-L3-GP

PM_RI# PM_BATLOW# R ECSWI# PCIE_WAKE# SMB_ALERT# DBRESET# SUSPWRACK SMB_LINK_ALERT#

RP3 SRN8K2J-2-GP-U

PCI_TRDY# INT_PIRQG# PCI_REQ#0 INT_PIRQH# INT_PIRQB# PCI_PERR# PCI_REQ#3 PCI_IRDY#

RP4 SRN8K2J-2-GP-U

INT_PIRQD# PCI_LOCK# PCI_FRAME# PCI_REQ#2 PCI_DEVSEL# PCI_REQ#1 PCI_STOP#

RP2 SRN8K2J-2-GP-U

INT_PIRQC# INT_PIRQF# INT_SERIRQ PM_CLKRUN# INT_PIRQA# INT_PIRQE# ECSCI#_1 PCI_SERR#

RP5 SRN10KJ-L3-GP

USB_OC#4 USB_OC#9 USB_OC#5 USB_OC#8 USB_OC#7 USB_OC#10 USB_OC#6 USB_OC#11

RN40 SRN10KJ-5-GP

DY R222 Do Not Stuff AC_PRESENT RSMRST#_SB

35 RSMRST#_KBC D11 BAT54-5-GP R224 100KR2J-1-GP

83.BAT54.D81

2nd = 83.BAT54.X81

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINI1
4	CCD
5	NC
6	Finger Print
7	Blue Tooth
8	NC
9	USB1
10	NC
11	Cardreader

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

SA 4.14

MIC_SEL_1 DY R405 Do Not Stuff

ACZ_SPKR R434 DY Do Not Stuff

3D3V_S0

NO_iTPM PWROK RN38 SRN10KJ-5-GP

SPI_ICH_CS1# R225 DY Do Not Stuff

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

UMA

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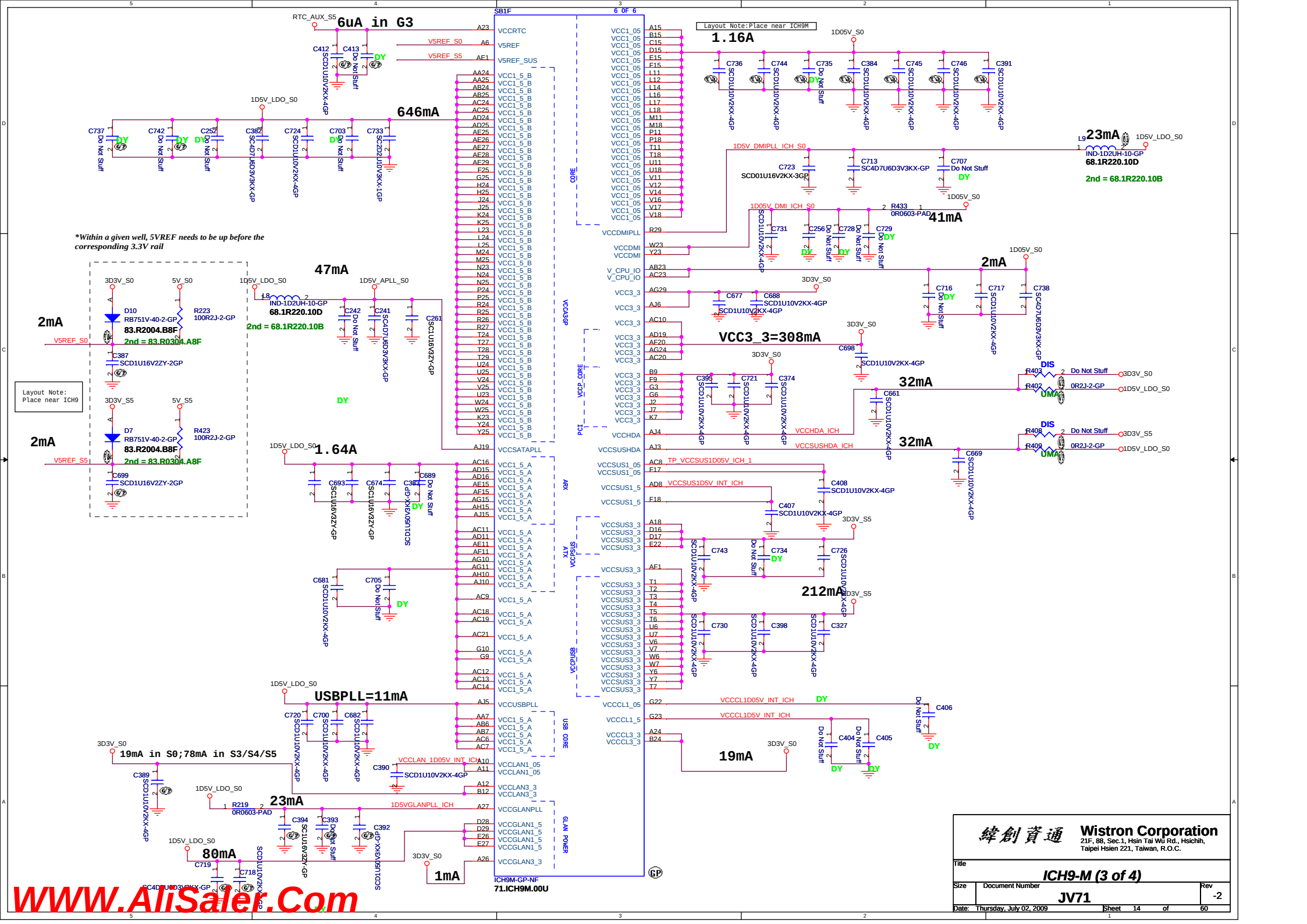
Title: ICH9-M (2 of 4)

Size: | Document Number: JV71 | Rev: -2

Date: Thursday, July 02, 2009 Sheet 13 of 60


SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
6uA in G3
1.16A
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
646mA
47mA
2mA
23mA
80mA
1mA
VCC3_3=308mA
212mA
32mA
41mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
2nd = 68.1R220.10B
2nd = 83.R0304.A8F
Do Not Stuff
DY
DIS
UMA
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ICH9-M (3 of 4)
JV71
Rev -2
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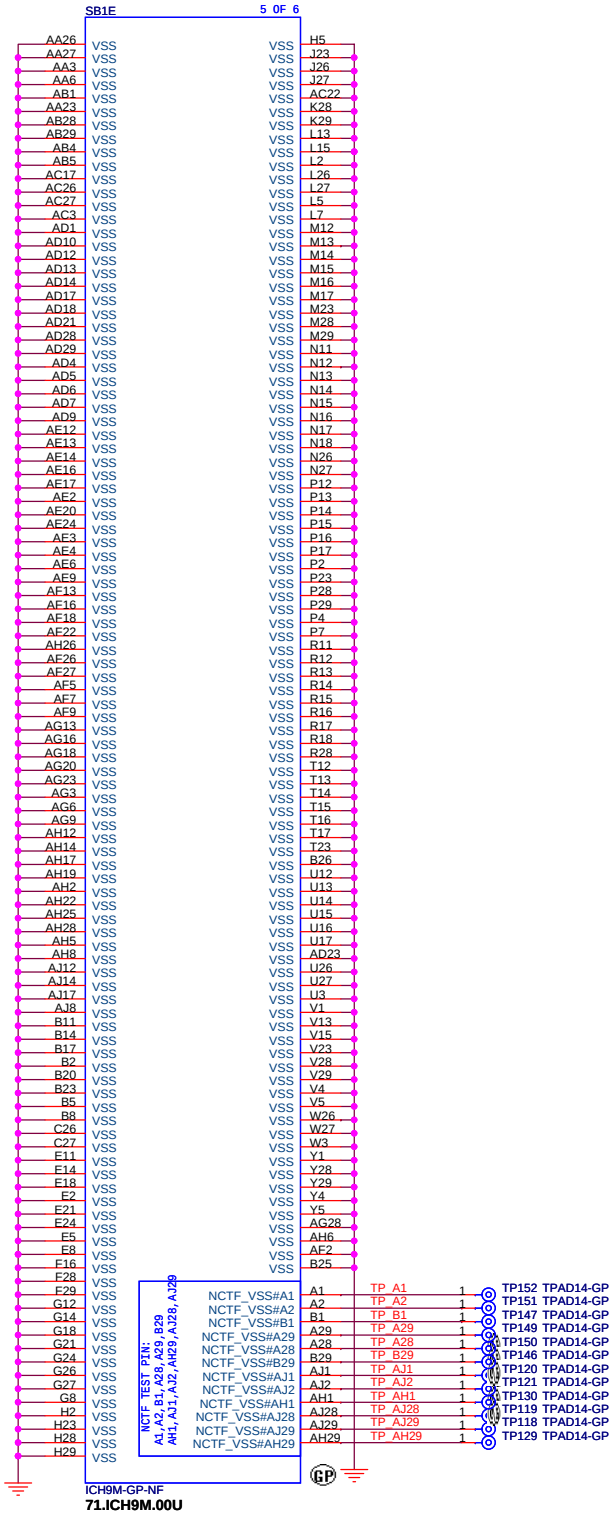
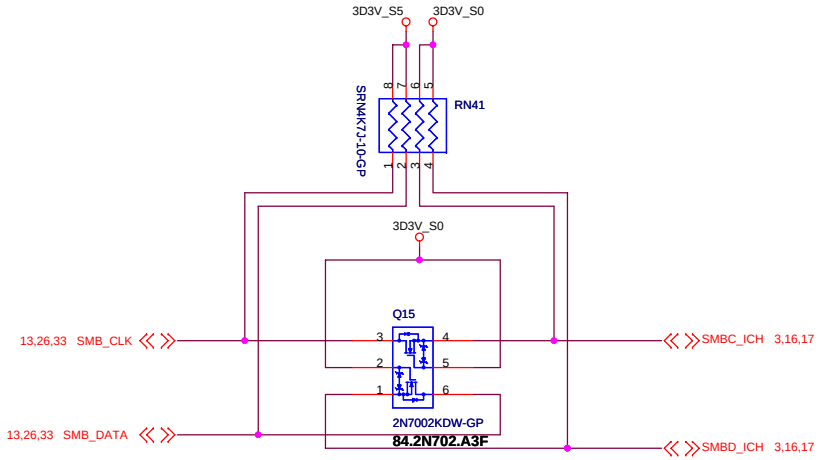
WWW.AliSaler.Com





SMBUS

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Title: *ICH9-M (4 of 4)*

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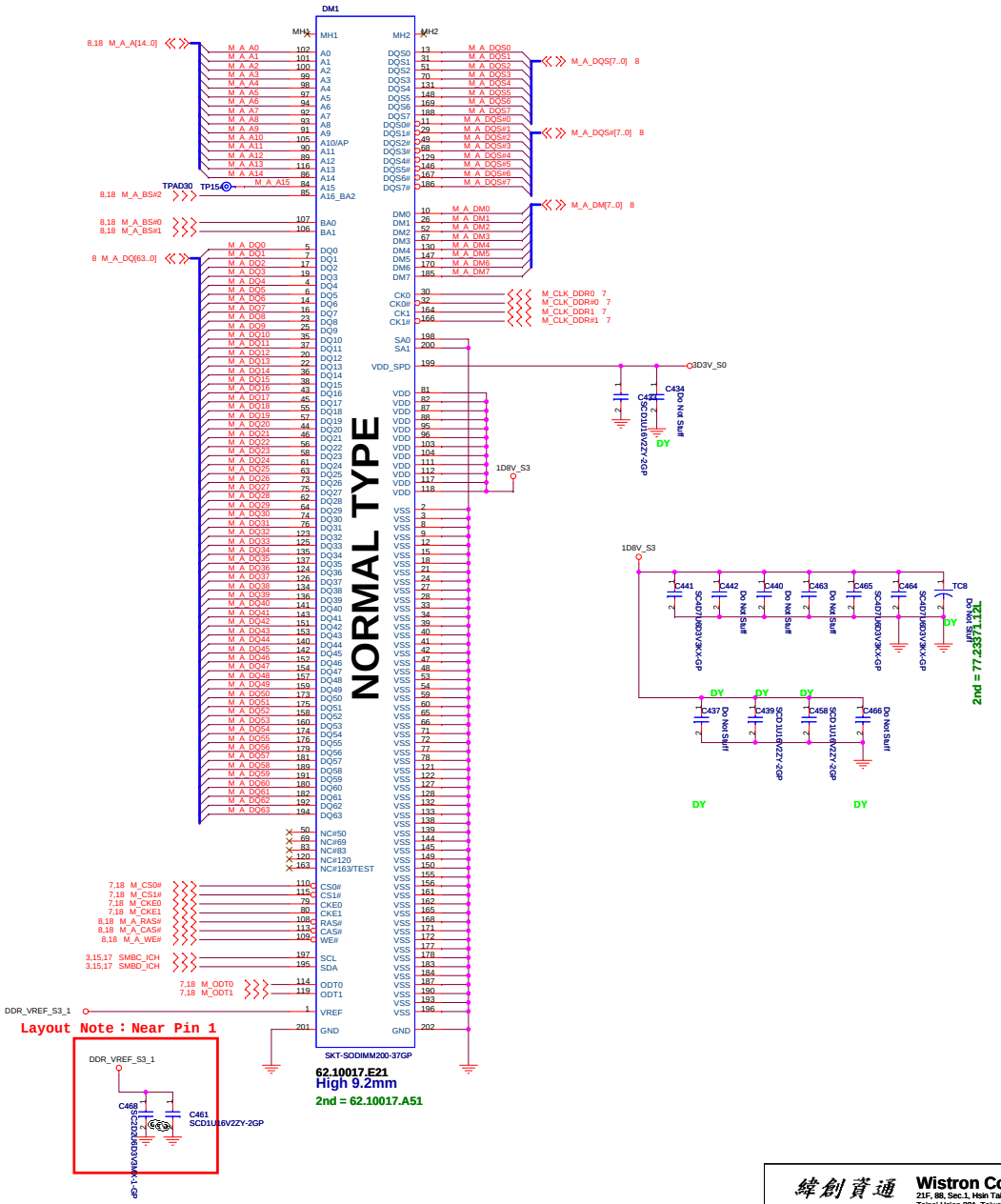
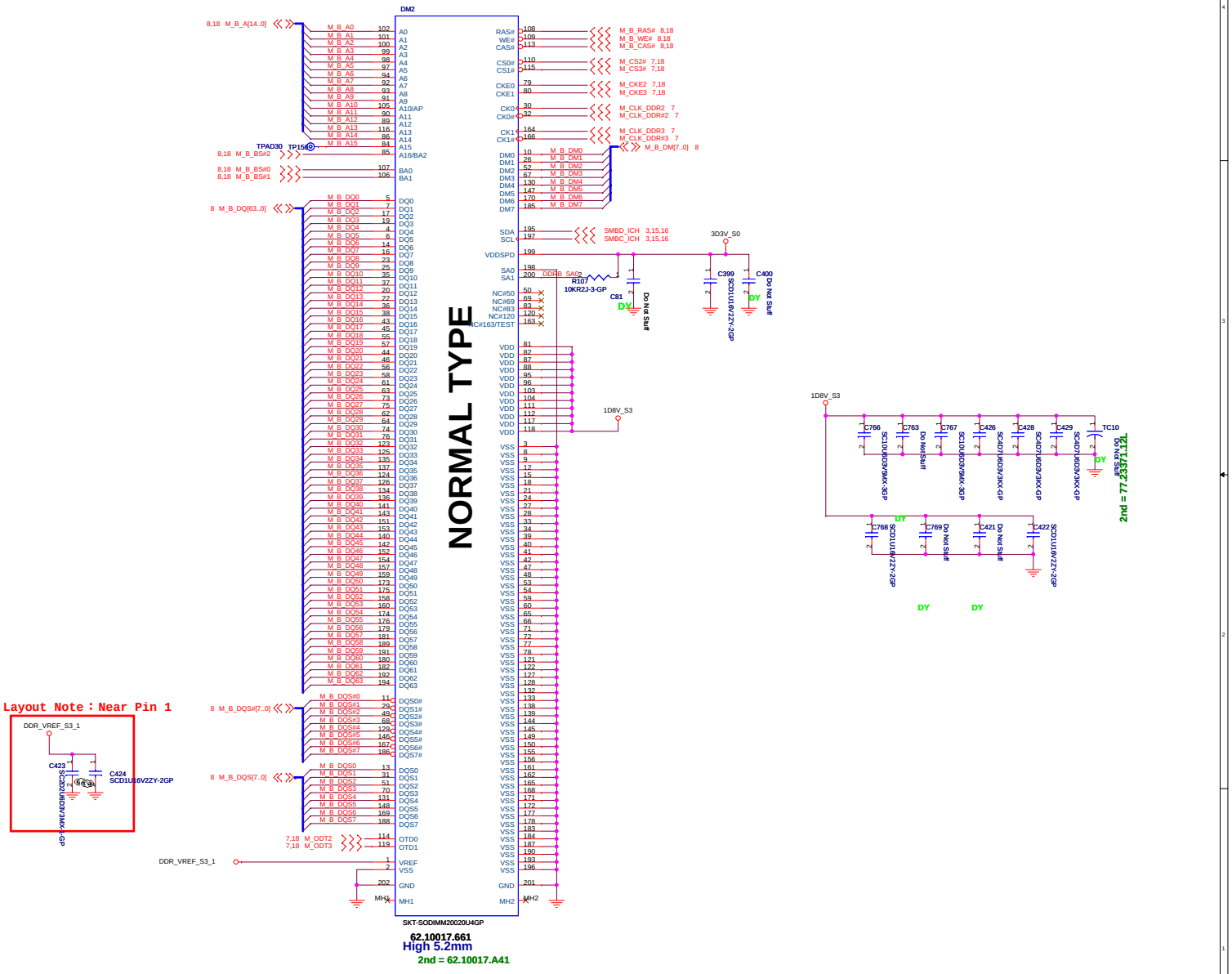
DDR2 SOCKET_1



緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR3 Socket			
Size	Document Number: JV71	Rev: -2	
Date: Thursday, July 02, 2009	Sheet 16 of 60		

DDR2 SOCKET_2



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Title	*DDR3 Socket2*	
Size	Document Number: JV71	Rev: -2
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PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S3

RN96 SRN56J-5-GP
M_CKE1 7,16
M_CKE0 7,16
M_A_BS#2 8,16

RN97 SRN56J-5-GP
M_B_A12
M_B_A8
M_B_A3
M_B_A5

RN98 SRN56J-5-GP
M_CKE2 7,17
M_B_A9
M_B_BS#2 8,17

RN43 SRN56J-5-GP
M_B_A1
M_B_A10
M_B_BS#0 8,17
M_B_RAS# 8,17

RN49 SRN56J-5-GP
M_B_A13
M_ODT2 7,17
M_CS2# 7,17

RN55 SRN56J-5-GP
M_B_BS#1 8,17
M_B_A0
M_B_A2
M_B_A4

RN54 SRN56J-5-GP
M_B_A6
M_B_A7
M_B_A11
M_B_A14

RN69 SRN56J-5-GP
M_B_WE# 8,17
M_B_CAS# 8,17
M_ODT3 7,17
M_CS3# 7,17

R190 S6R2J-4-GP
M_CKE3 7,17

RN90 SRN56J-5-GP
M_A_A13
M_A_BS#1 8,16
M_ODT0 7,16
M_CS0# 7,16

RN91 SRN56J-5-GP
M_A_A3
M_A_A10
M_A_BS#0 8,16
M_A_WE# 8,16

RN92 SRN56J-5-GP
M_A_RAS# 8,16
M_A_A0
M_A_A2
M_A_A4

RN93 SRN56J-5-GP
M_A_A12
M_A_A5
M_A_A9
M_A_A8

RN94 SRN56J-5-GP
M_A_A6
M_A_A7
M_A_A11
M_A_A14

RN95 SRN56J-5-GP
M_A_CAS# 8,16
M_A_A1
M_CS1# 7,16
M_ODT1 7,16

M_A_A[14..0] M_A_A[14..0] 8,16
M_B_A[14..0] M_B_A[14..0] 8,17

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S3

C378 C469 C420 C354 C355 C356 C380 C425 C477 C438 C459
SCD1U16V2ZY-2GP
Do Not Stuff

DY

C727 C725 C497 C495 C487 C484 C476 C489 C486 C462 C460
SCD1U16V2ZY-2GP
Do Not Stuff

DY DY DY DY

UMA

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Title: DDR 2 Termination Resistor

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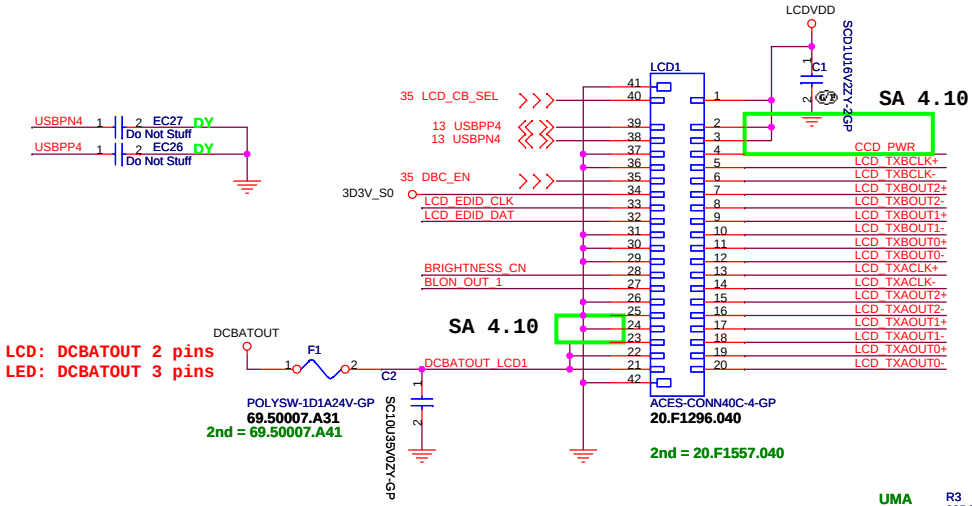
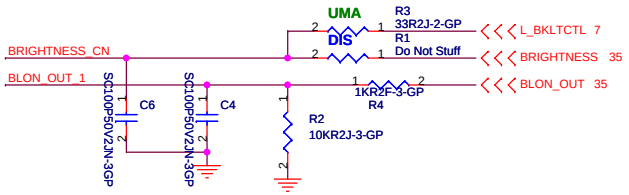
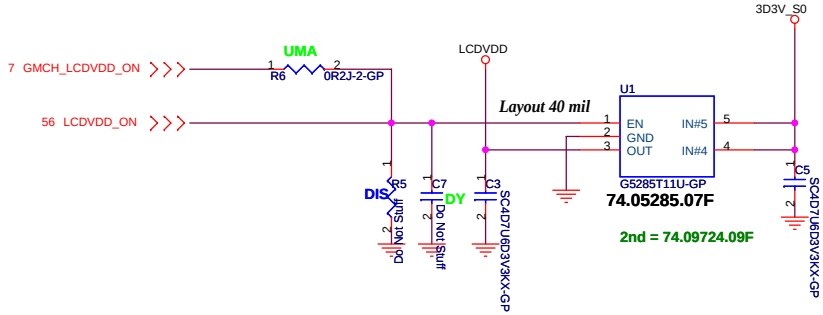
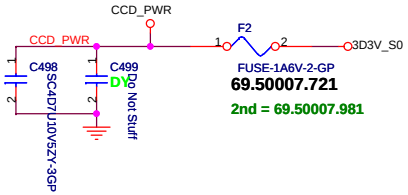
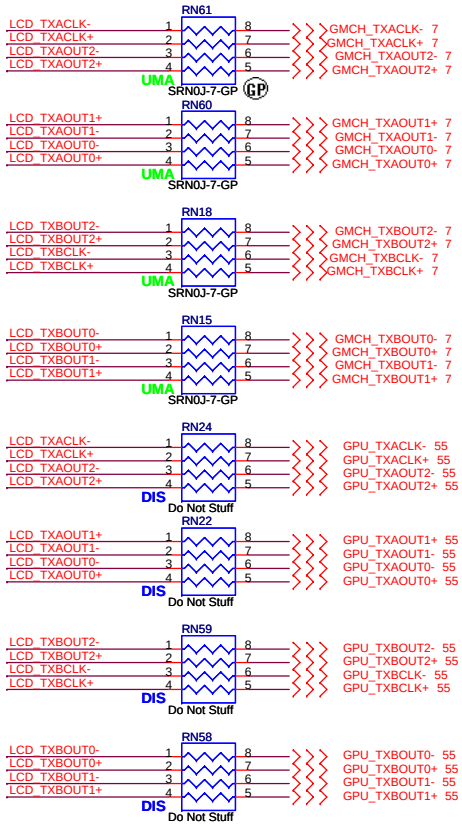
LCD/INVERTER/CCD CONN

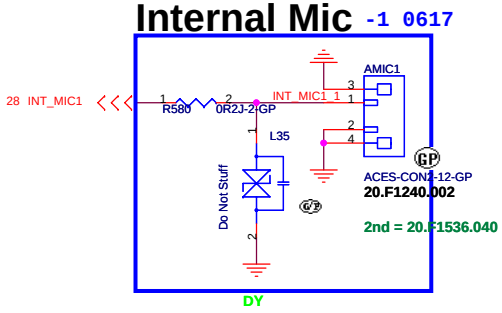


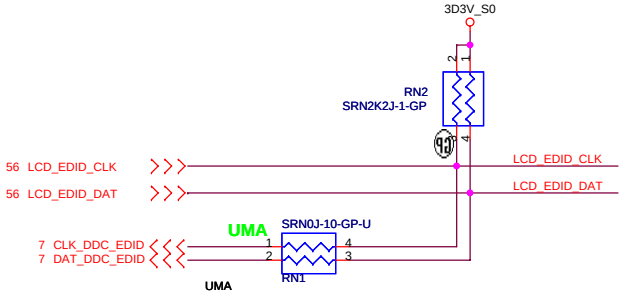












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Title	**LCD CONN**	
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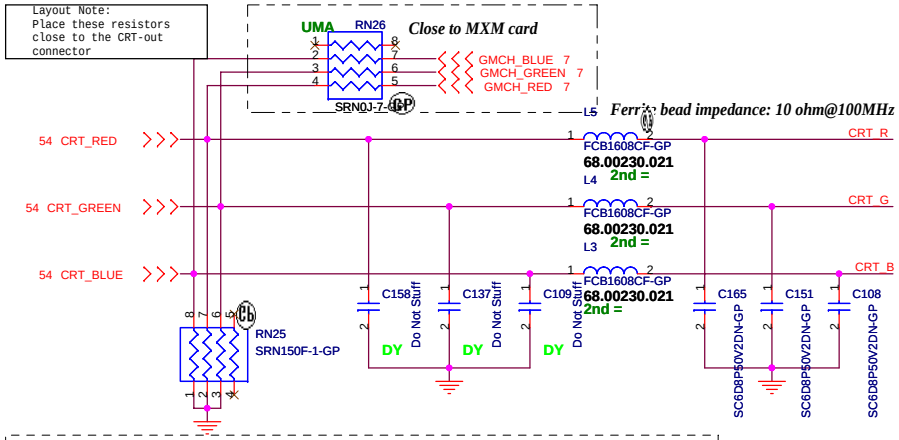
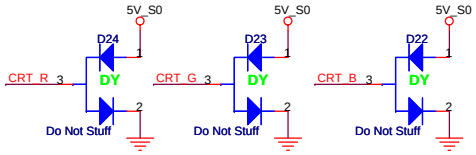
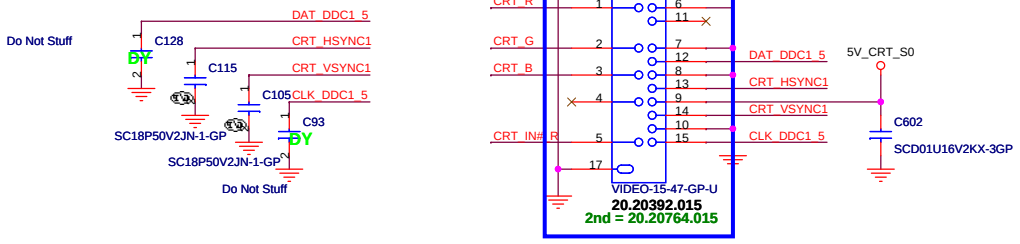
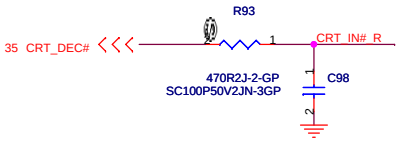


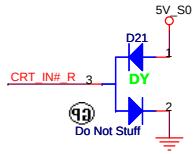
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



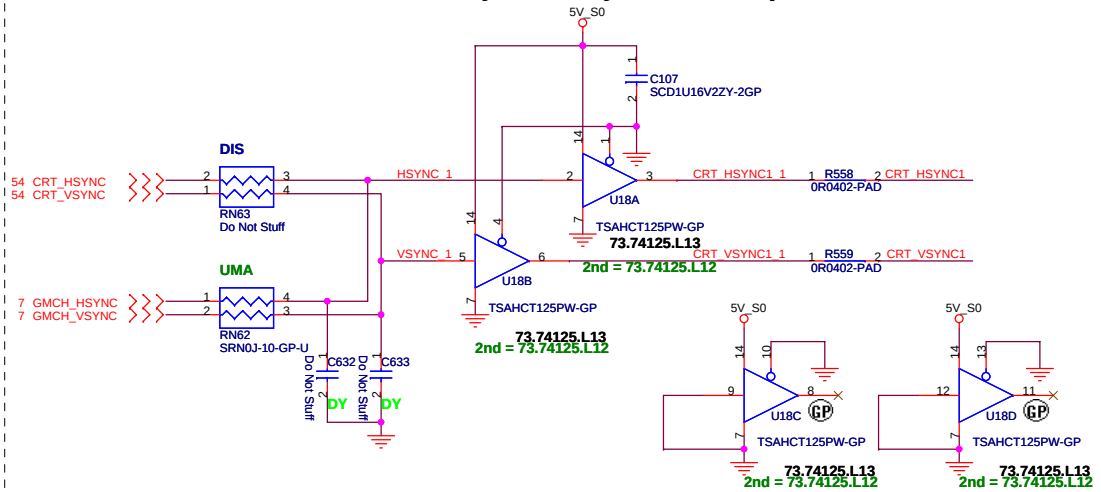
CRT I/F & CONNECTOR



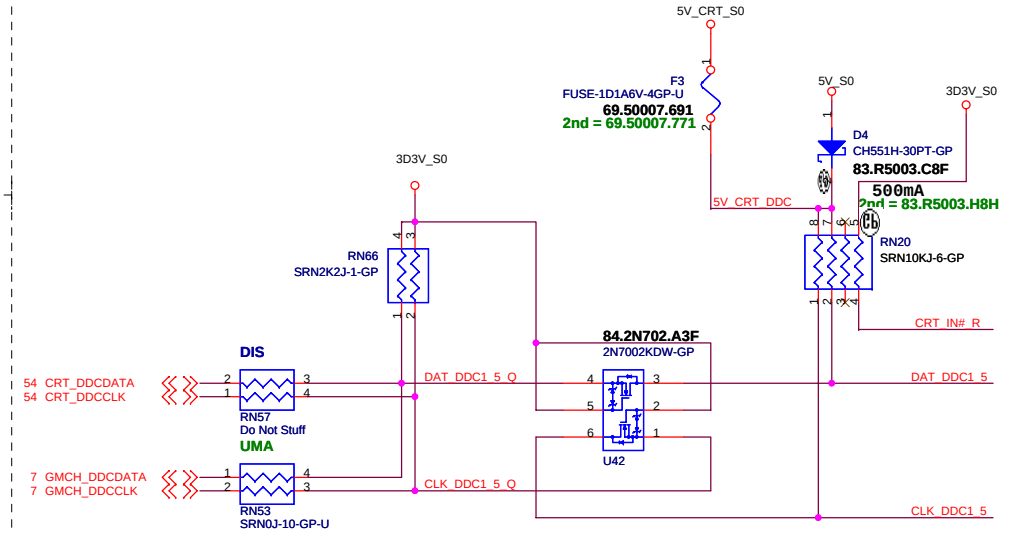




Hsync & Vsync level shift



DDC_CLK & DATA level shift



UMA

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Title	***CRT CONN***	
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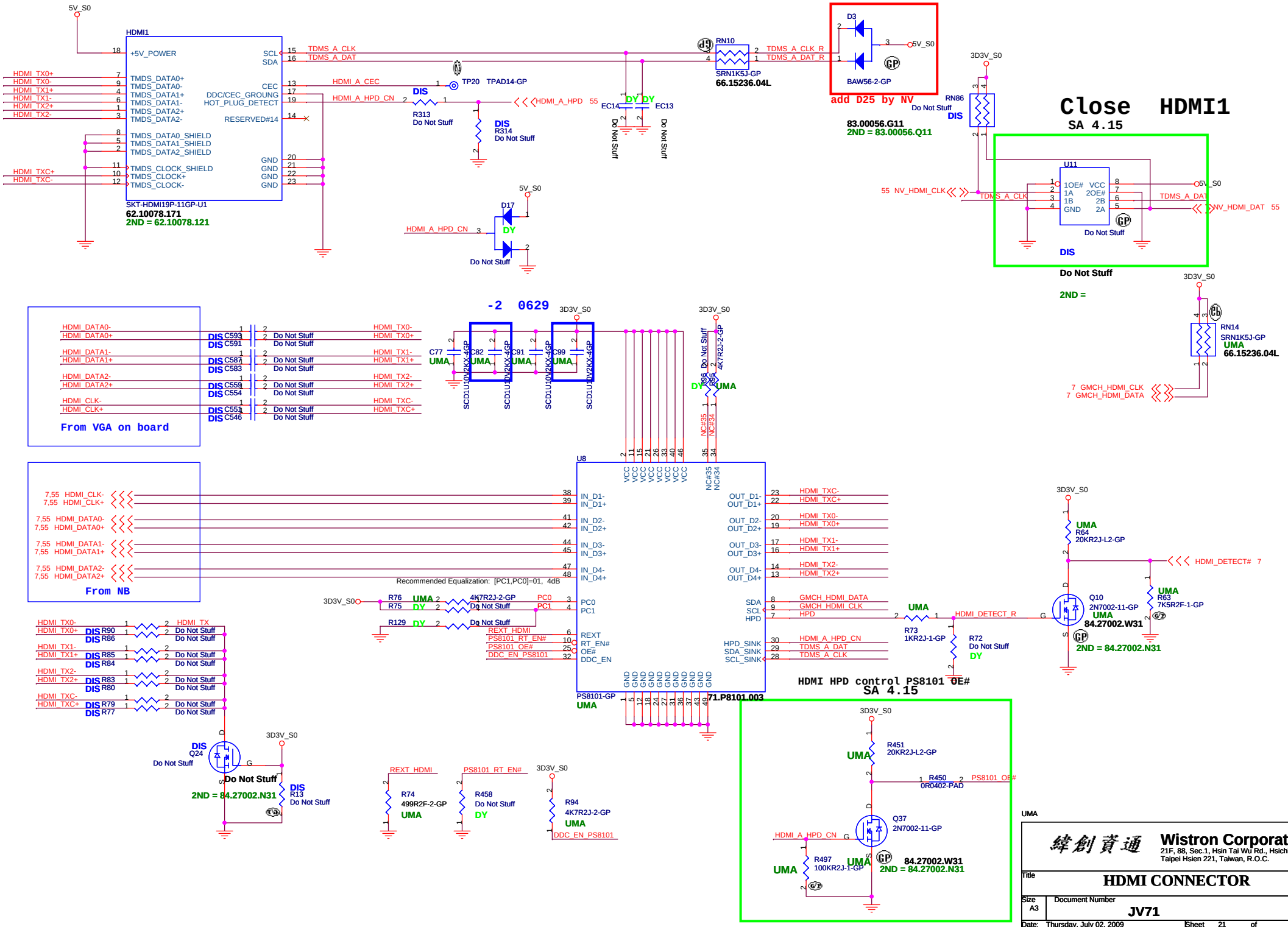
6 1 7 2 8 3 9 4 10 5


HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2ND = 62.10078.121
TP20 TPAD14-GP
RN10
SRN1K5J-GP
66.15236.04L
D3
BAW56-2-GP
add D25 by NV
83.00056.G11
2ND = 83.00056.Q11
RN86
Do Not Stuff
DIS
Close HDMI1
SA 4.15
U11
Do Not Stuff
DIS
Do Not Stuff
2ND =
RN14
SRN1K5J-GP
UMA
66.15236.04L
-2 0629
From VGA on board
From NB
U8
PS8101-GP
UMA
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
HDMI HPD control PS8101 OE#
SA 4.15
Q24
Do Not Stuff
2ND = 84.27002.N31
Q10
2N7002-11-GP
UMA
84.27002.W31
2ND = 84.27002.N31
Q37
2N7002-11-GP
UMA
84.27002.W31
2ND = 84.27002.N31
UMA
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Title
HDMI CONNECTOR
Size A3
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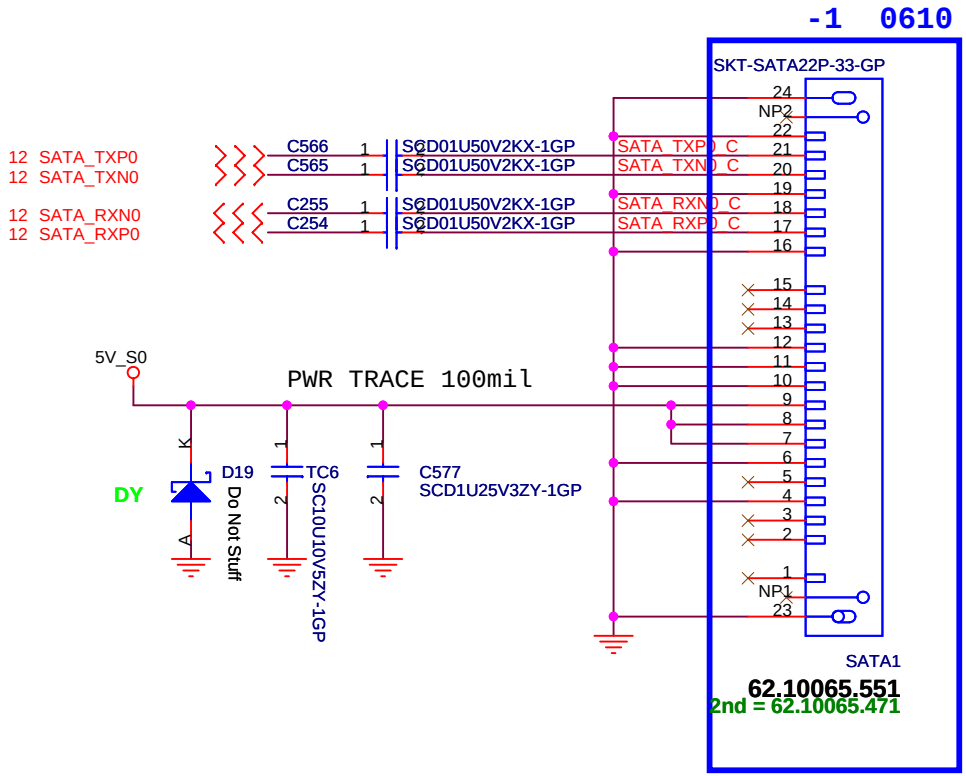
SATA Connector



UMA

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Title	HDD CONN	
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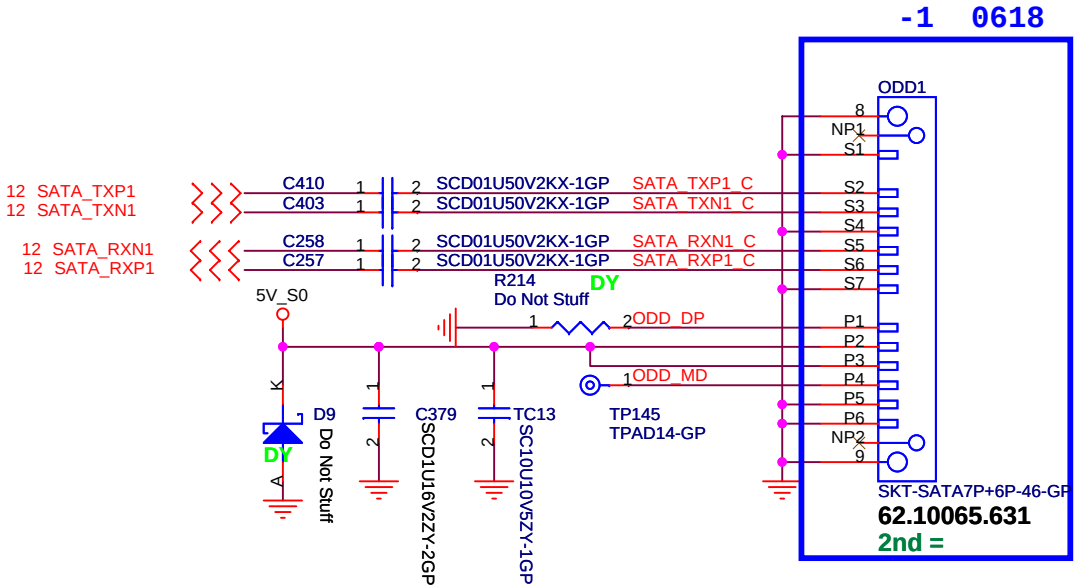
ODD Connector



UMA

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Title	***ODD***	
Size	Document Number **JV71**	Rev -2
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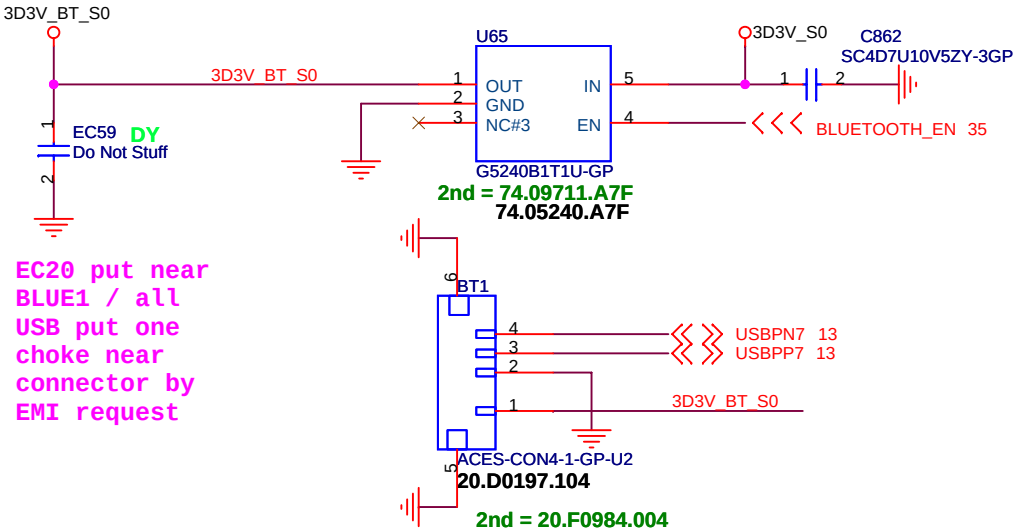
BLUETOOTH MODULE



UMA

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Title: ***BLUETOOTH***

Size	Document Number	Rev
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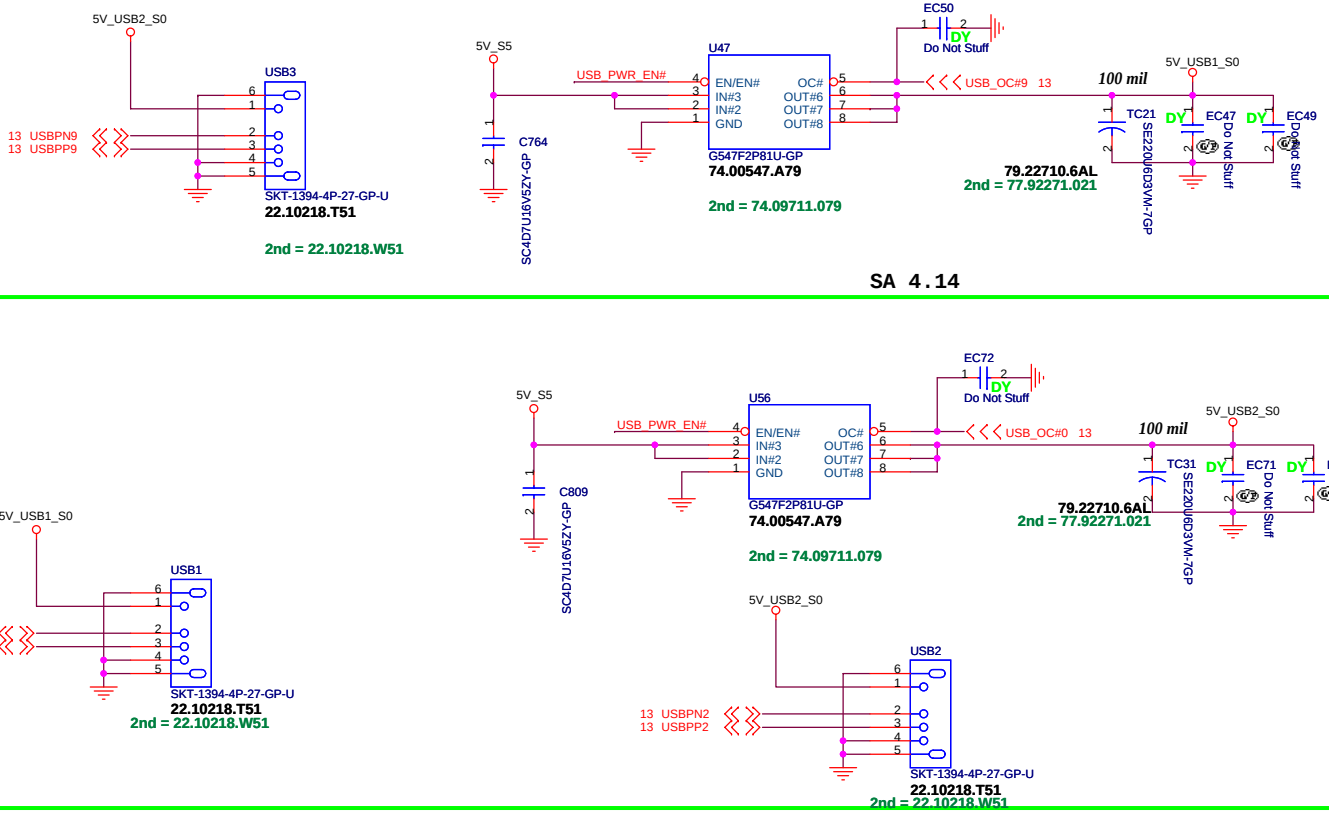

UMA

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Title		
USB CONN		
Size	Document Number	Rev
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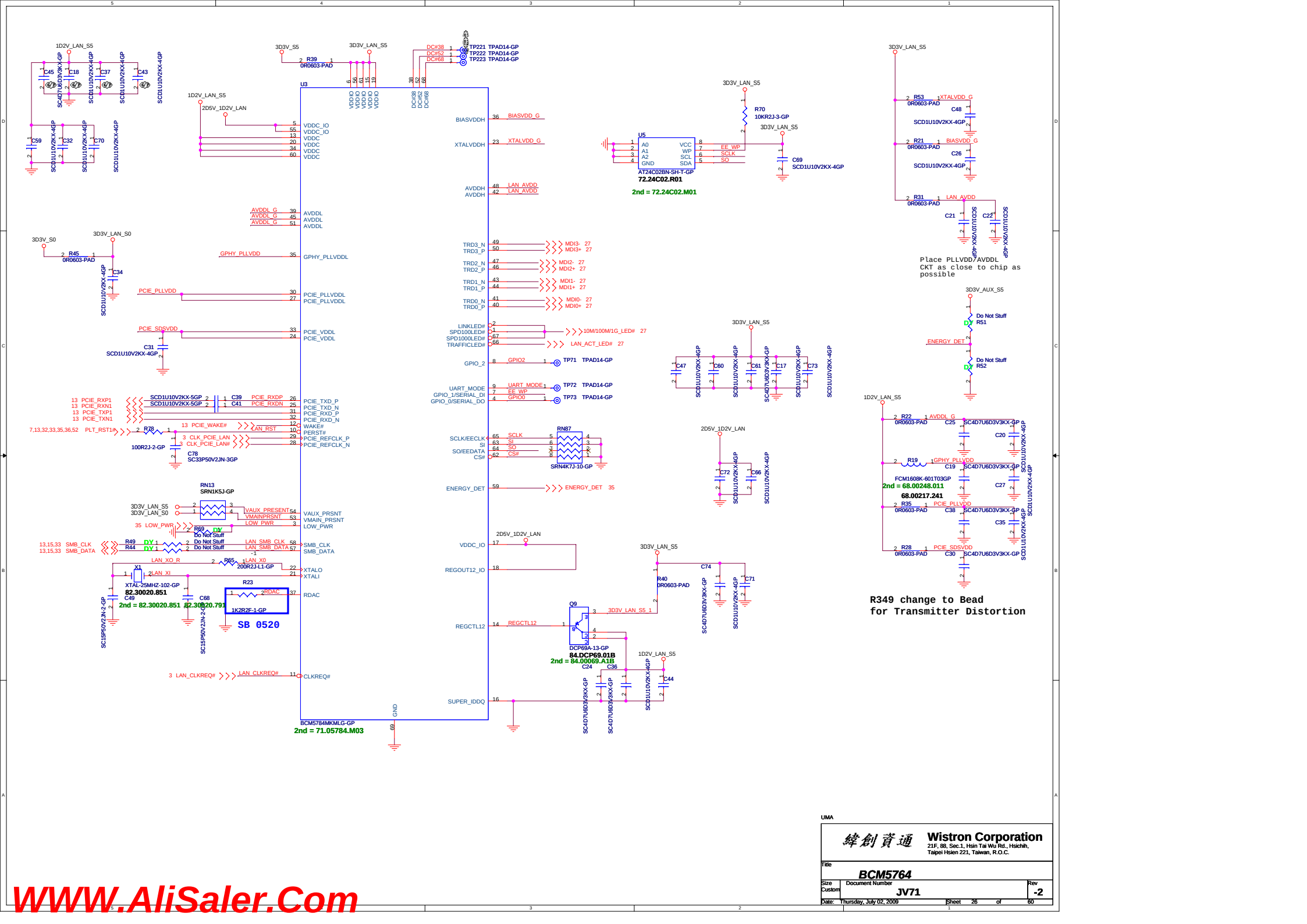
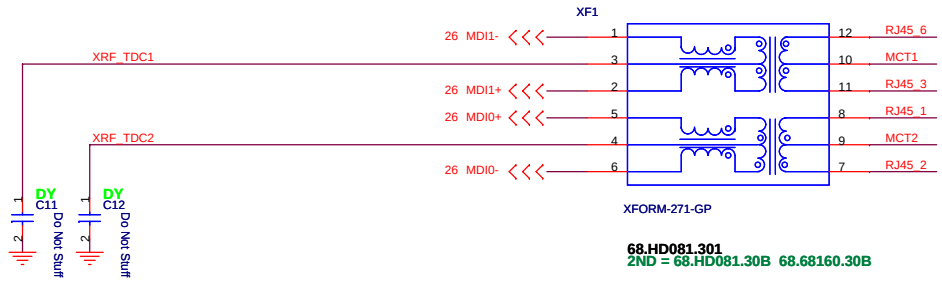


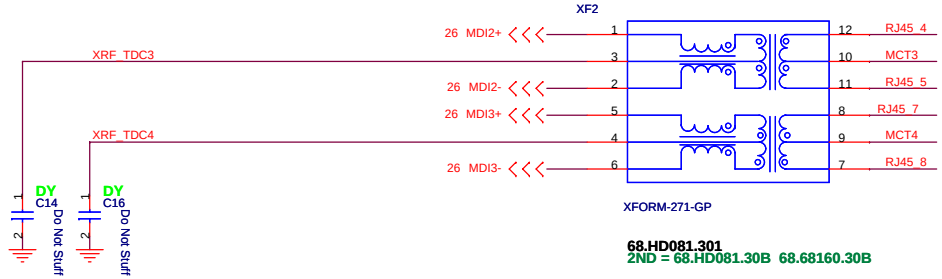
LAN Connector

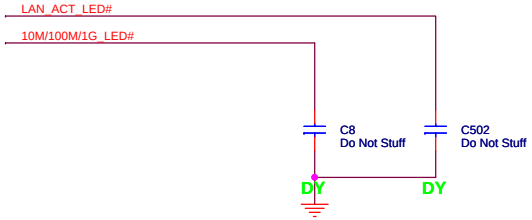
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

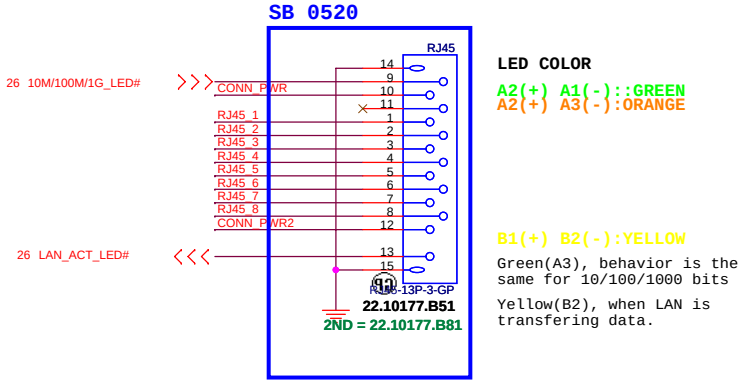
LAN Connector

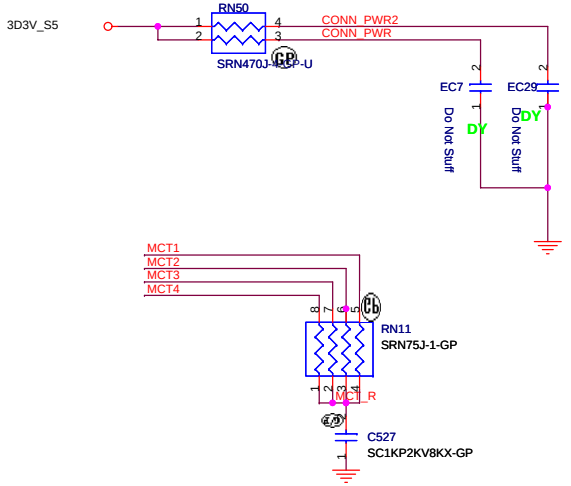
GIGA Lan Transformer











UMA

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Title: **LAN CONN**		
Size: A3	Document Number: JV71	Rev: -2
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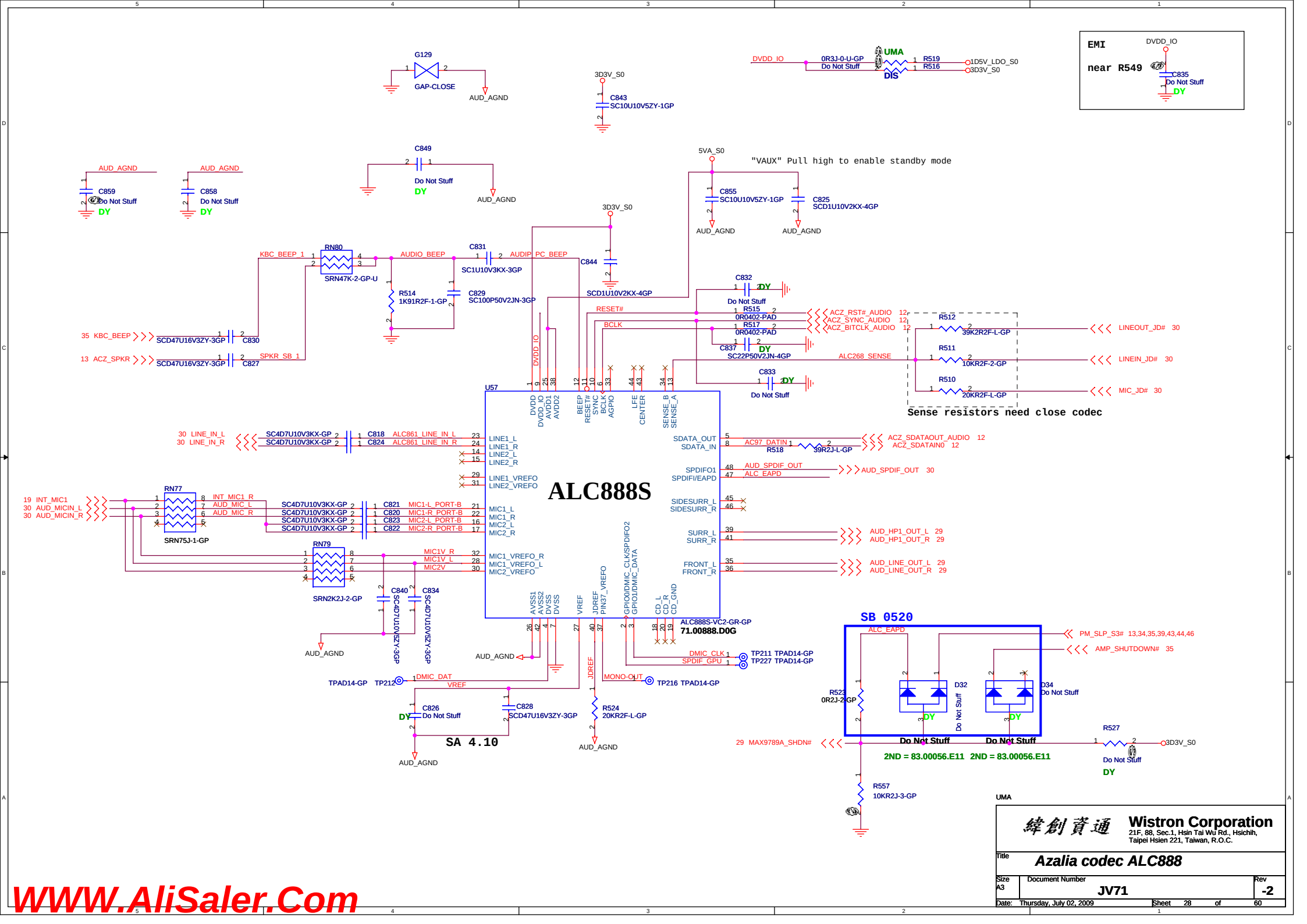
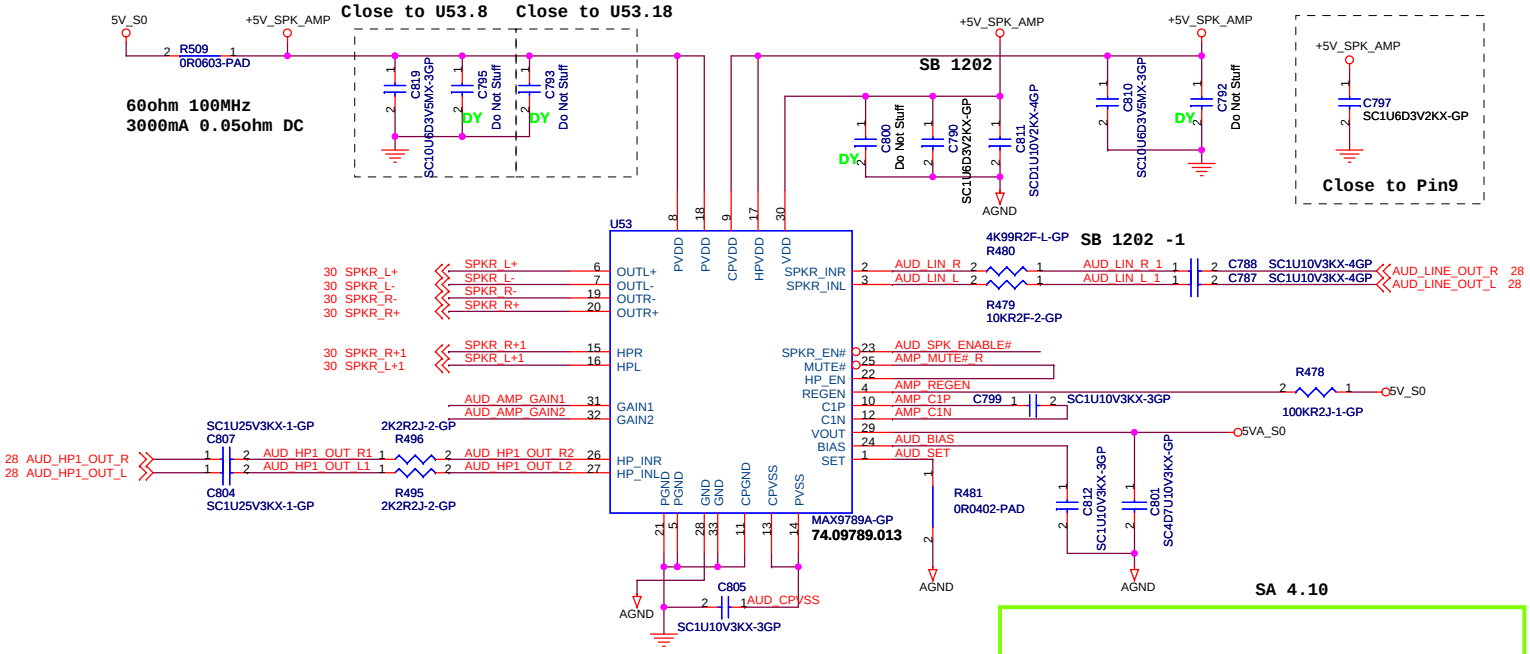
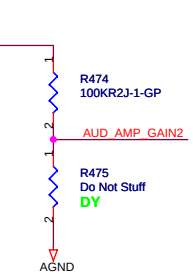
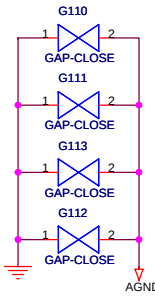
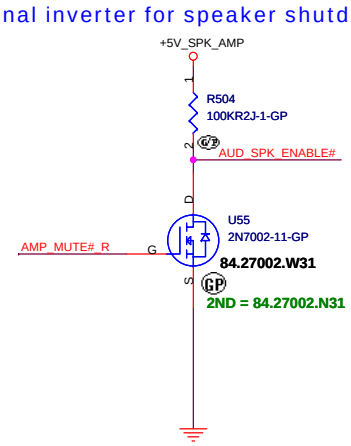






GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB





UMA

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Title	AUDIO AMP	
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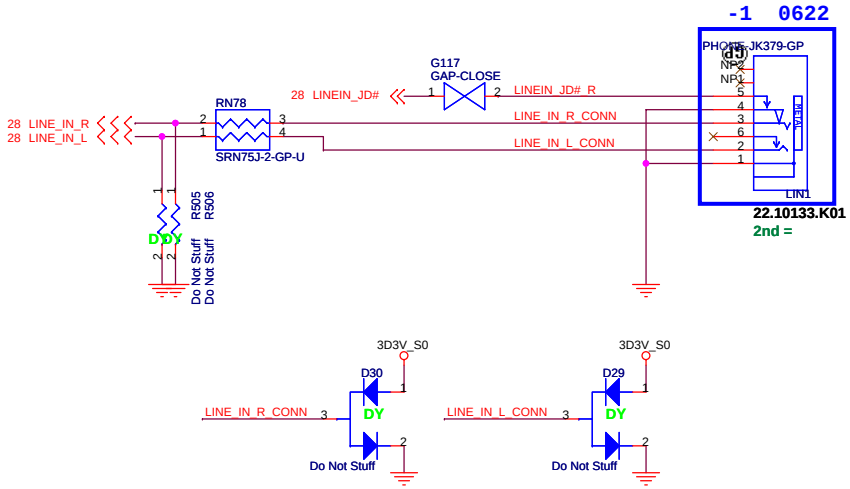
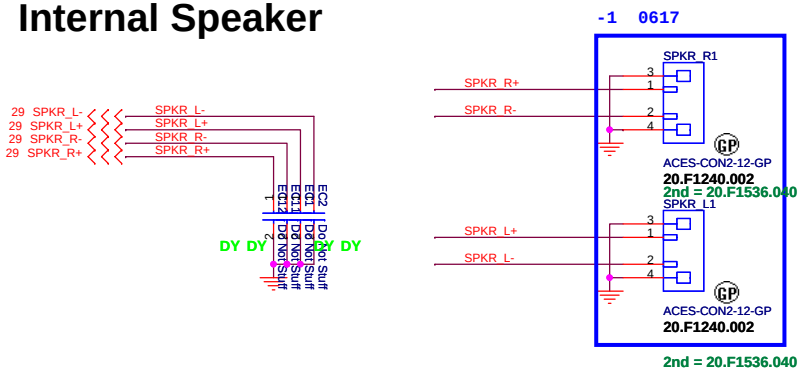
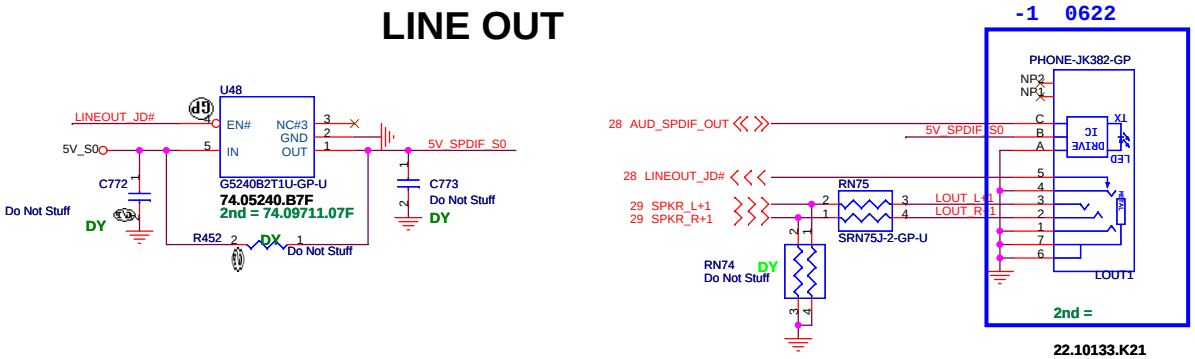
LINE IN

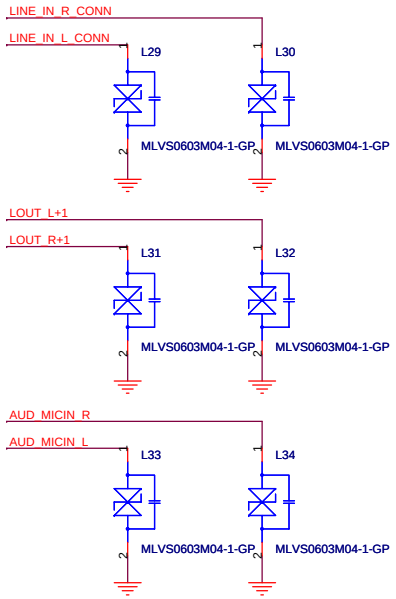


Internal Speaker

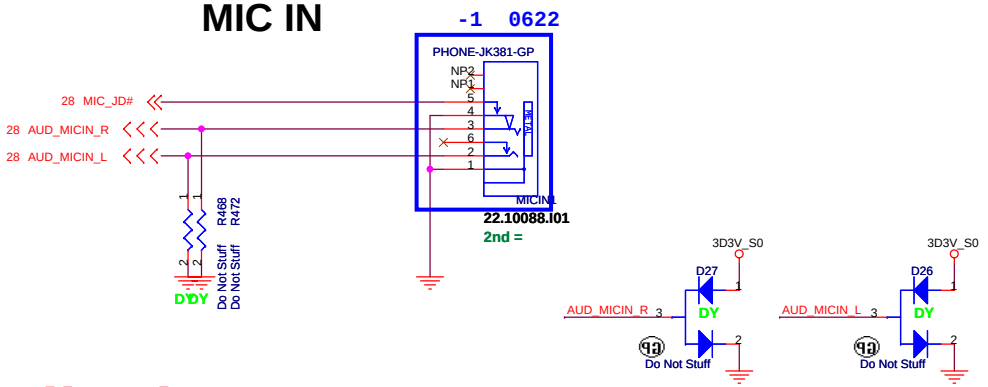


LINE OUT





MIC IN



UMA

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Title	AUDIO jack	
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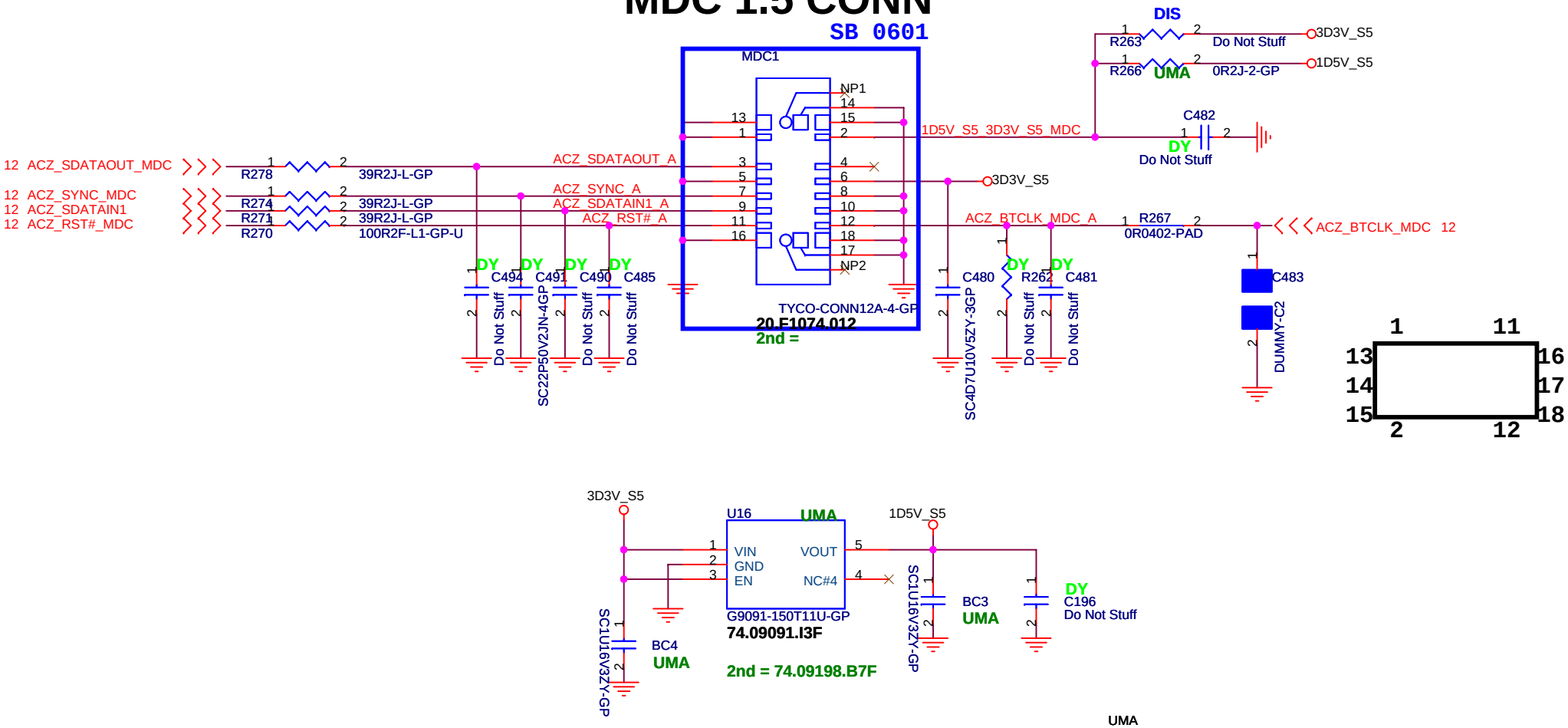
MDC 1.5 CONN

SB 0601



UMA

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Title	***MDC***	
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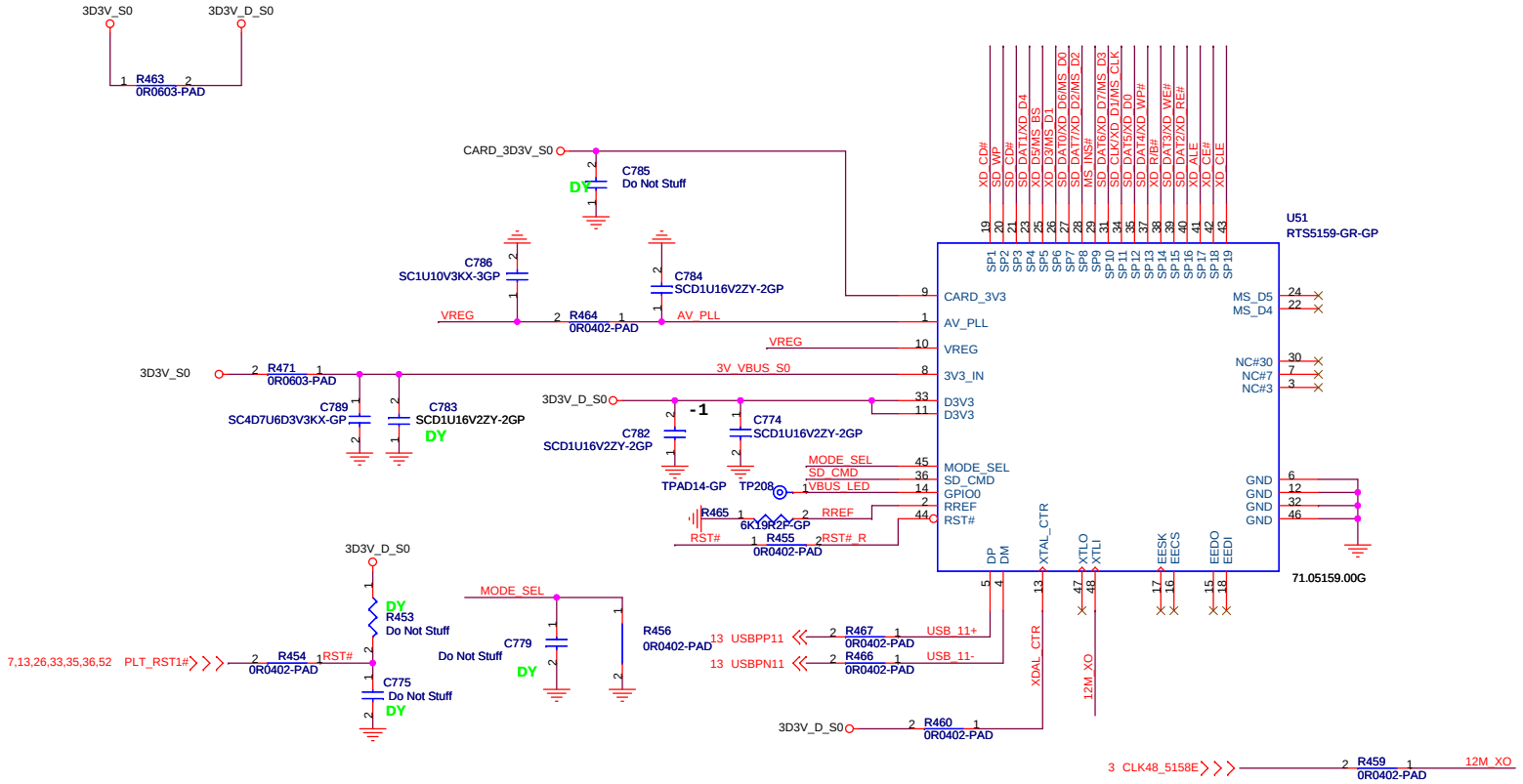

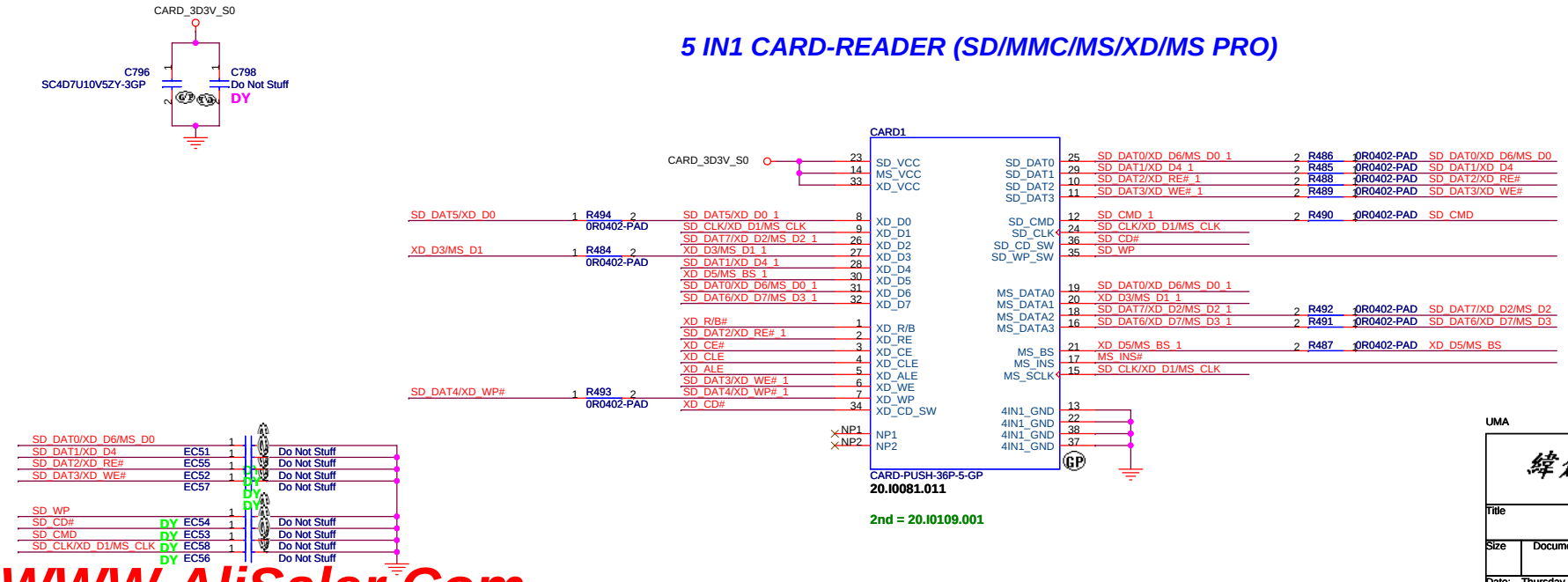

5 IN1 CARD-READER (SD/MMC/MS/XD/MS PRO)

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cardreader RTS5159*

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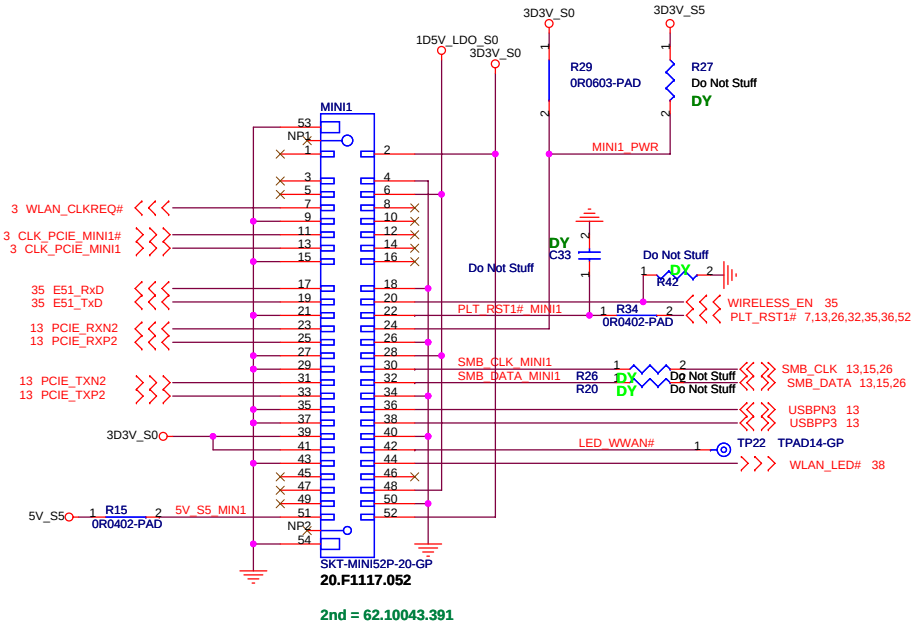
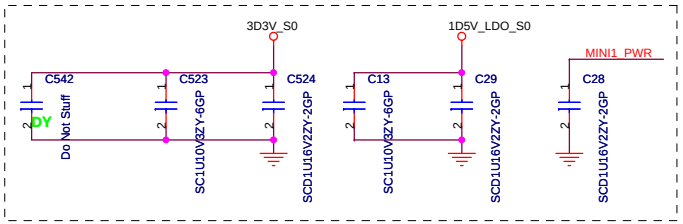
Mini Card Connector(WLAN)
Support debug-card



Place near MINI1



Mini Card Connector

UMA

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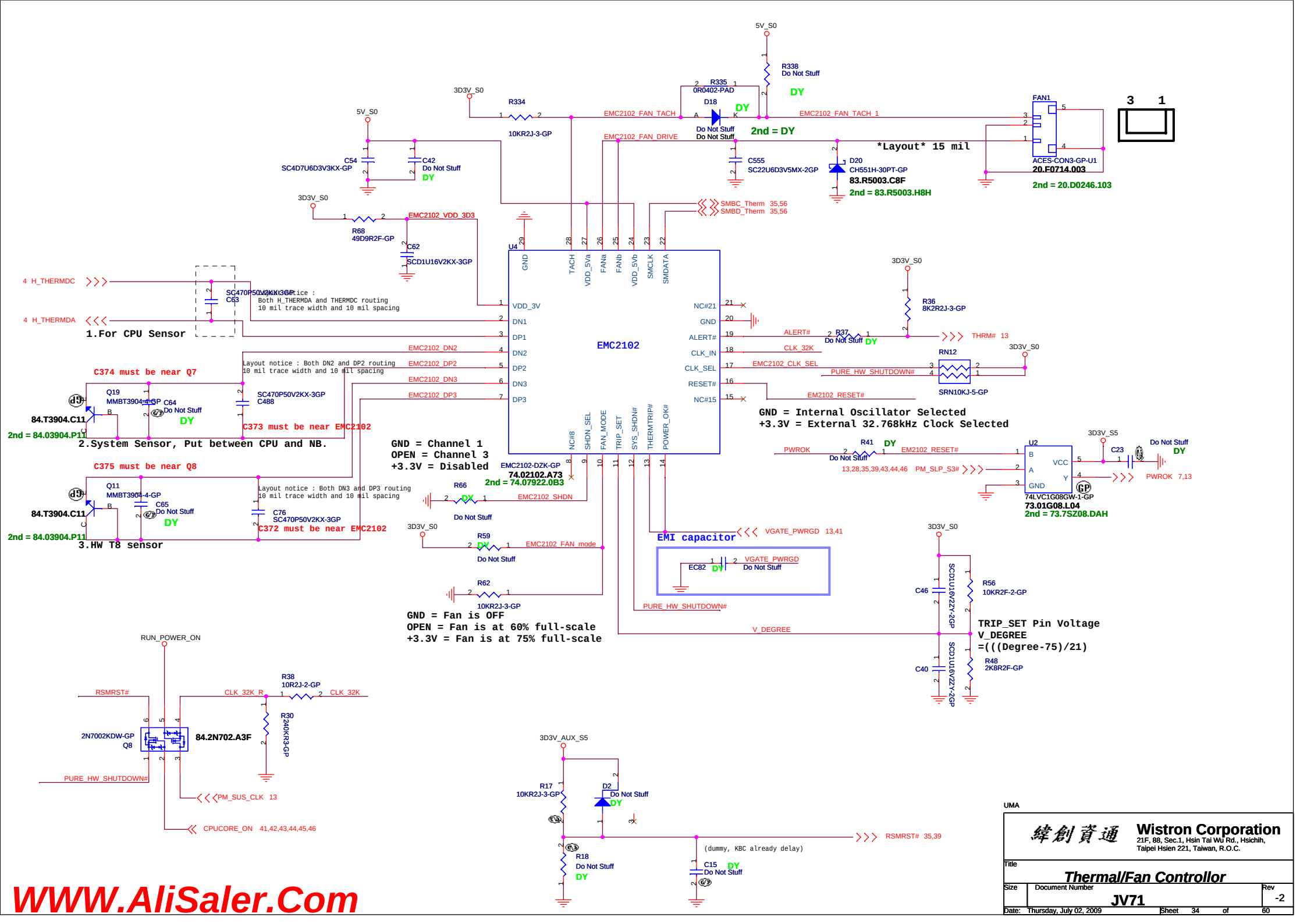
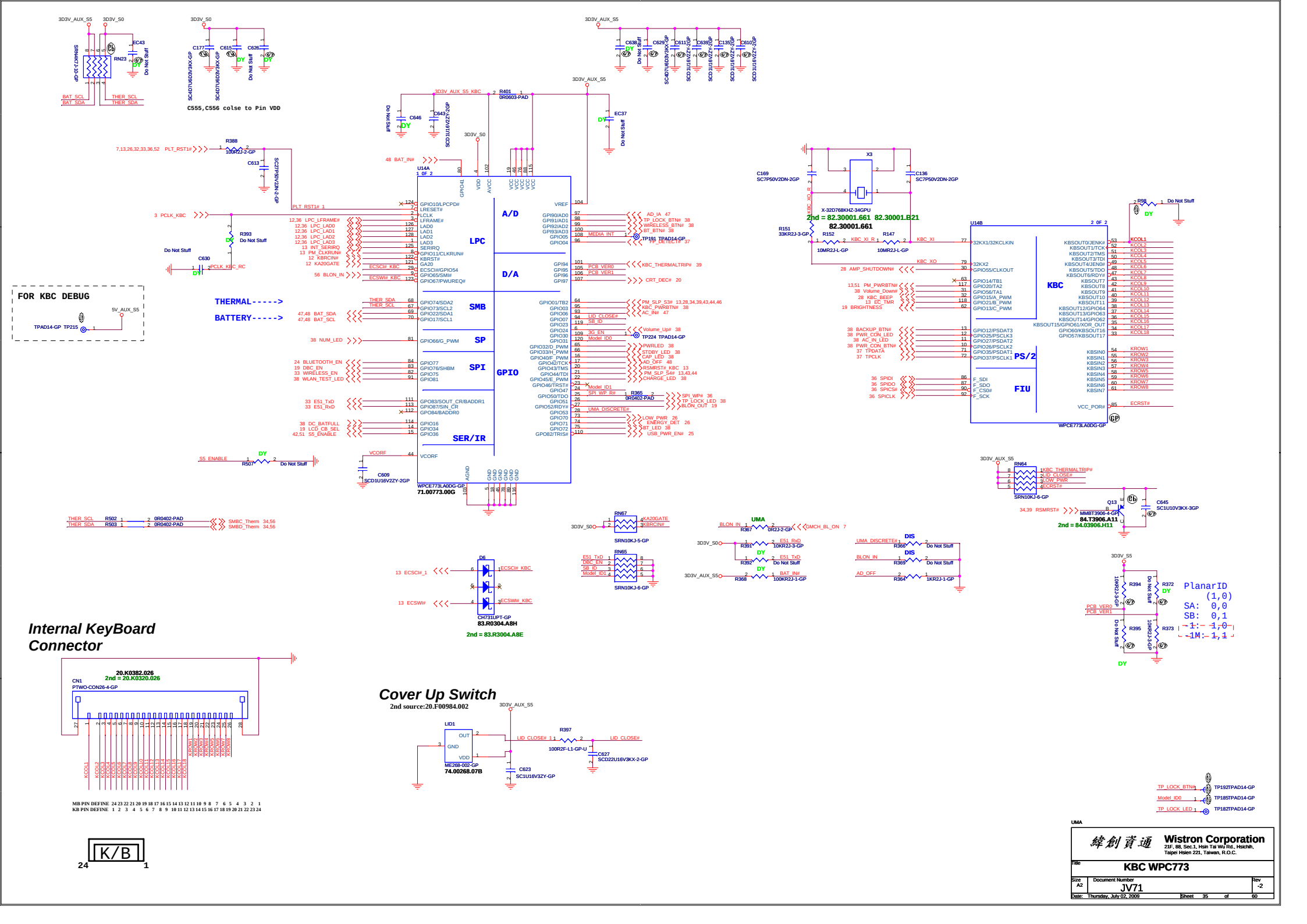
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD		
Size: A3	Document Number: JV71	Rev: -2
Date: Thursday, July 02, 2009	Sheet 33 of 60	




C555,C556 colse to Pin VDD
U14A
WPCE773LA0DG-GP
71.00773.00G
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
THERMAL----->
BATTERY----->
FOR KBC DEBUG
Internal KeyBoard Connector
20.K0382.026
2nd = 20.K0320.026
Cover Up Switch
2nd source:20.F00984.002
ME268-002-GP
74.00268.07B
CH731UPT-GP
83.R0304.A8H
2nd = 83.R3004.A8E
X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.661 82.30001.E21
KBC WPC773
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Size A2
Document Number JV71
Rev -2
Date: Thursday, July 02, 2009
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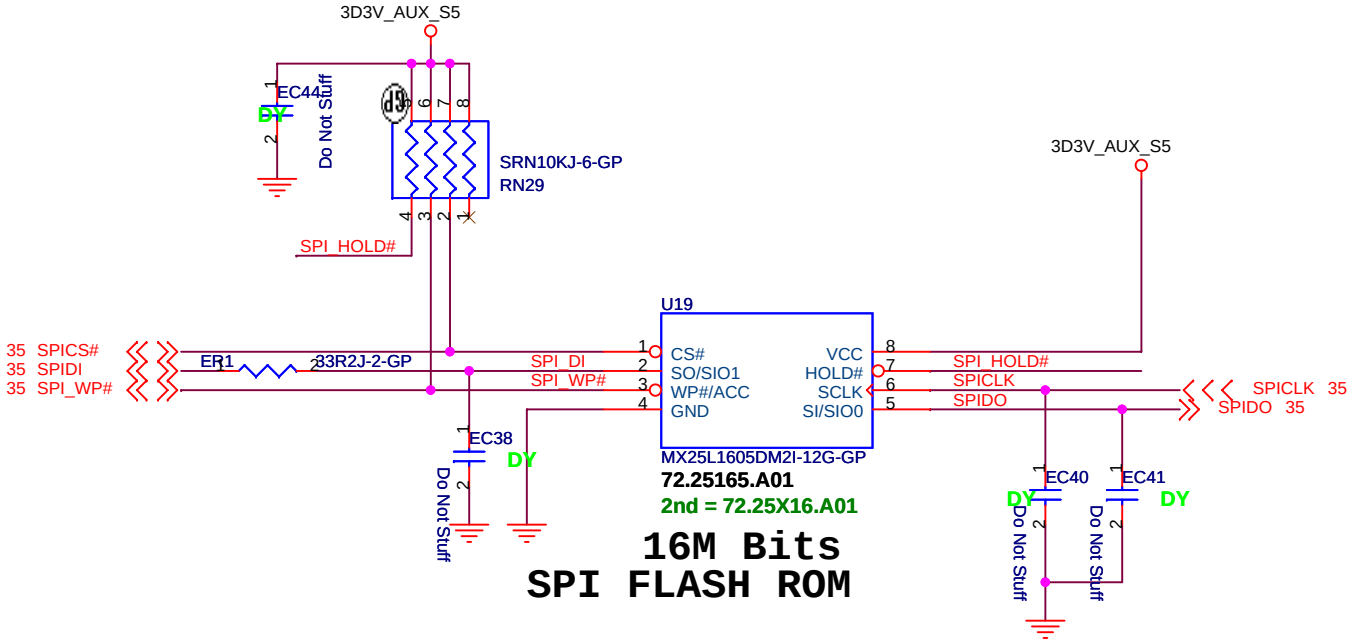
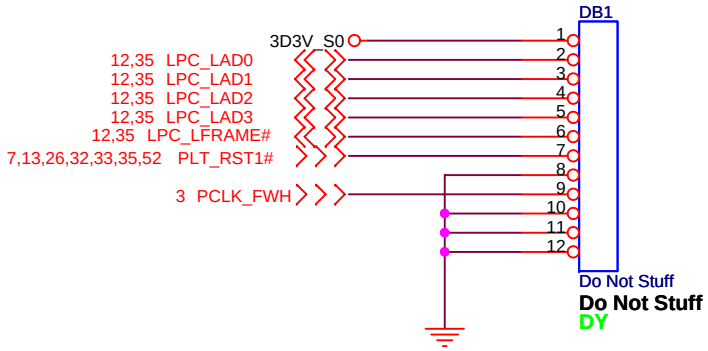


GOLDEN FINGER FOR DEBUG BOARD



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Title	***BIOS***	
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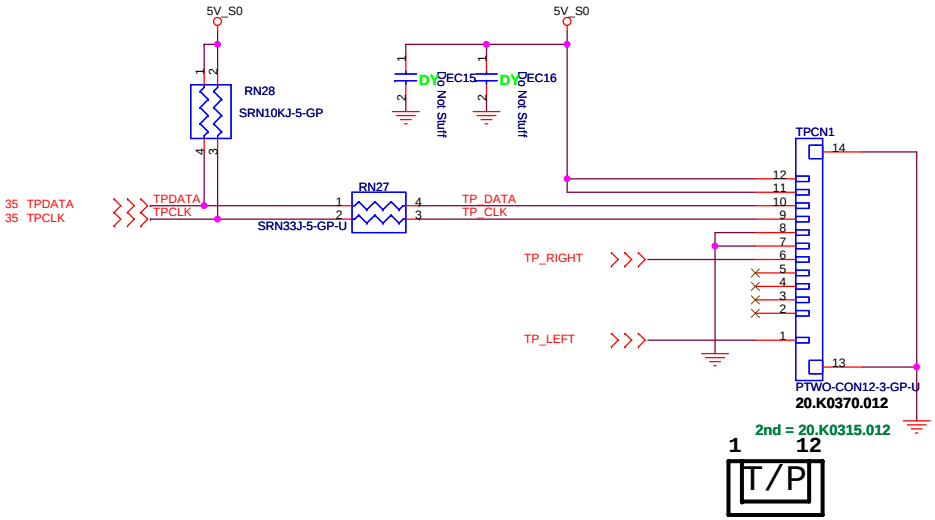
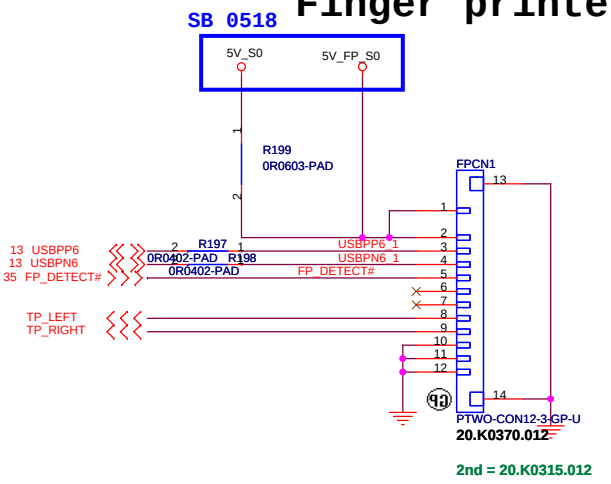
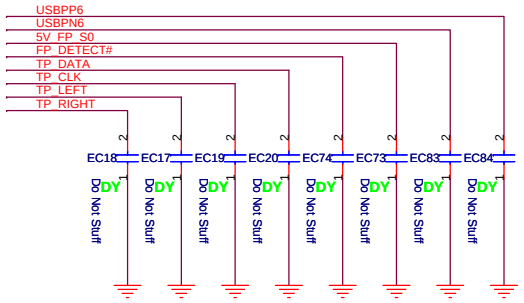
TOUCH PAD



Finger printer





UMA

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Title: Touch PAD and FP		
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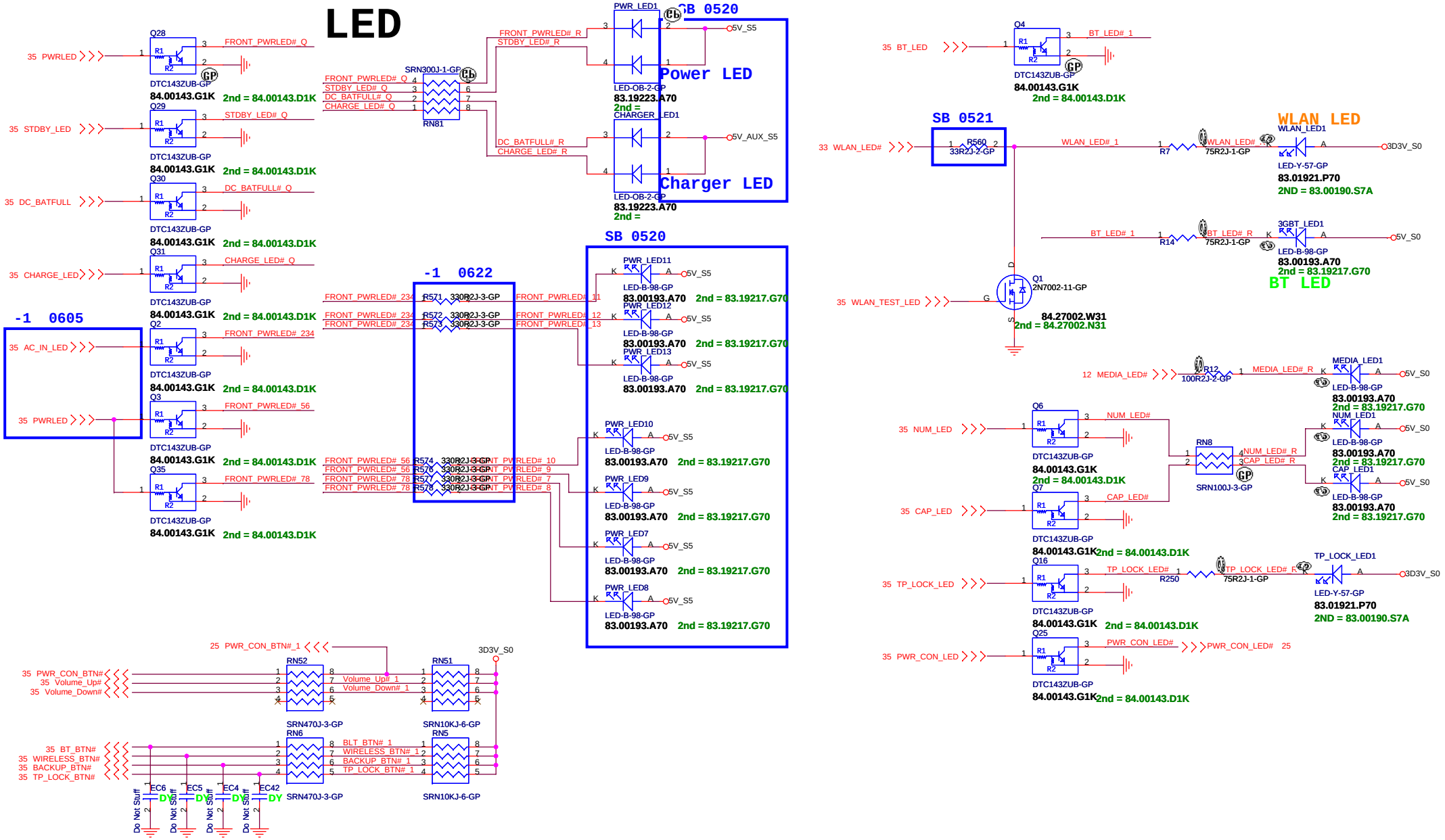
LED



UMA

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LED&POWERBD CONN

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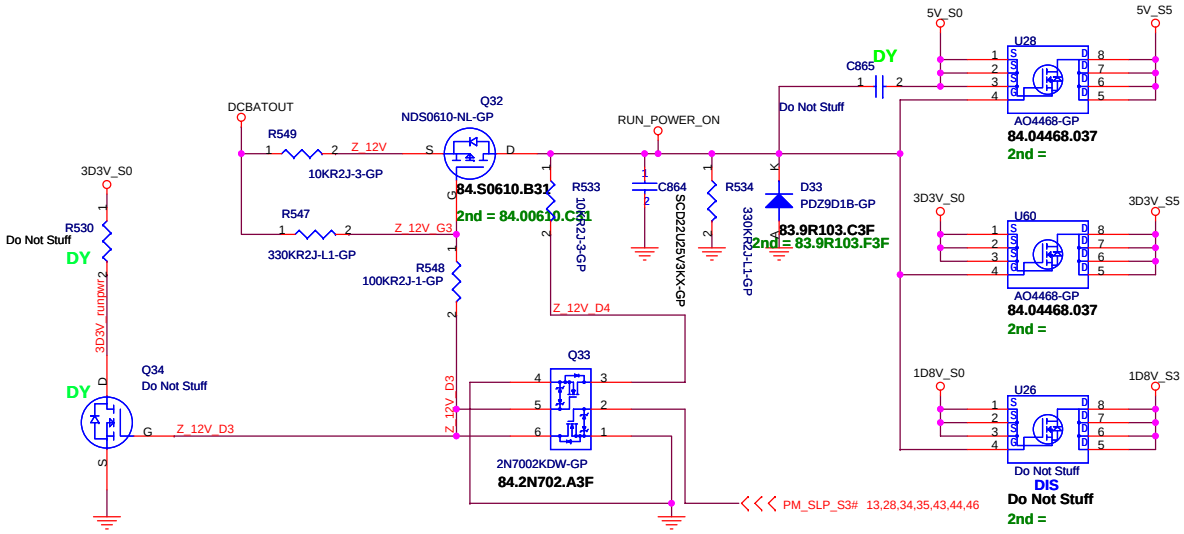
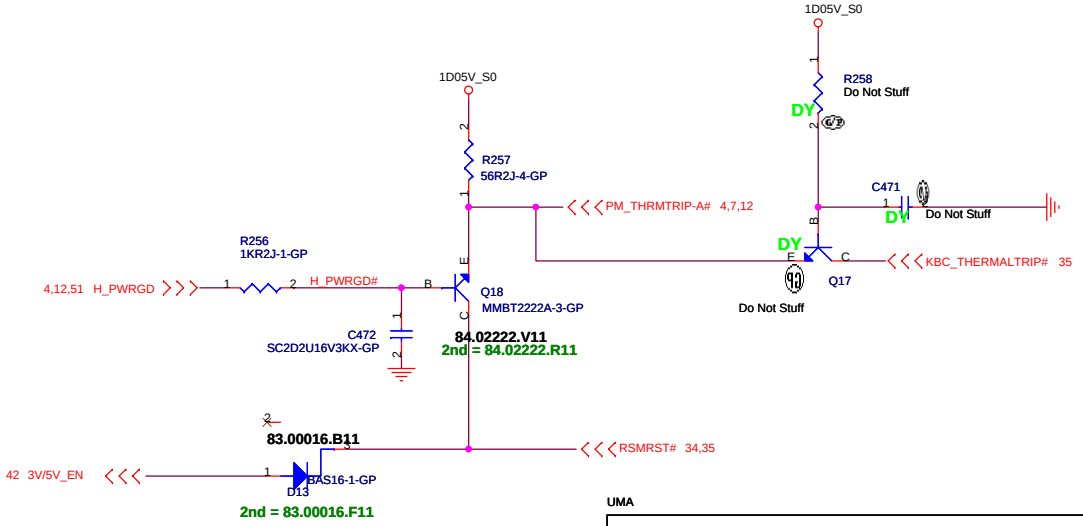
Run Power





UMA

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Title	RUN POWER and 3D3V_AUX_S5	
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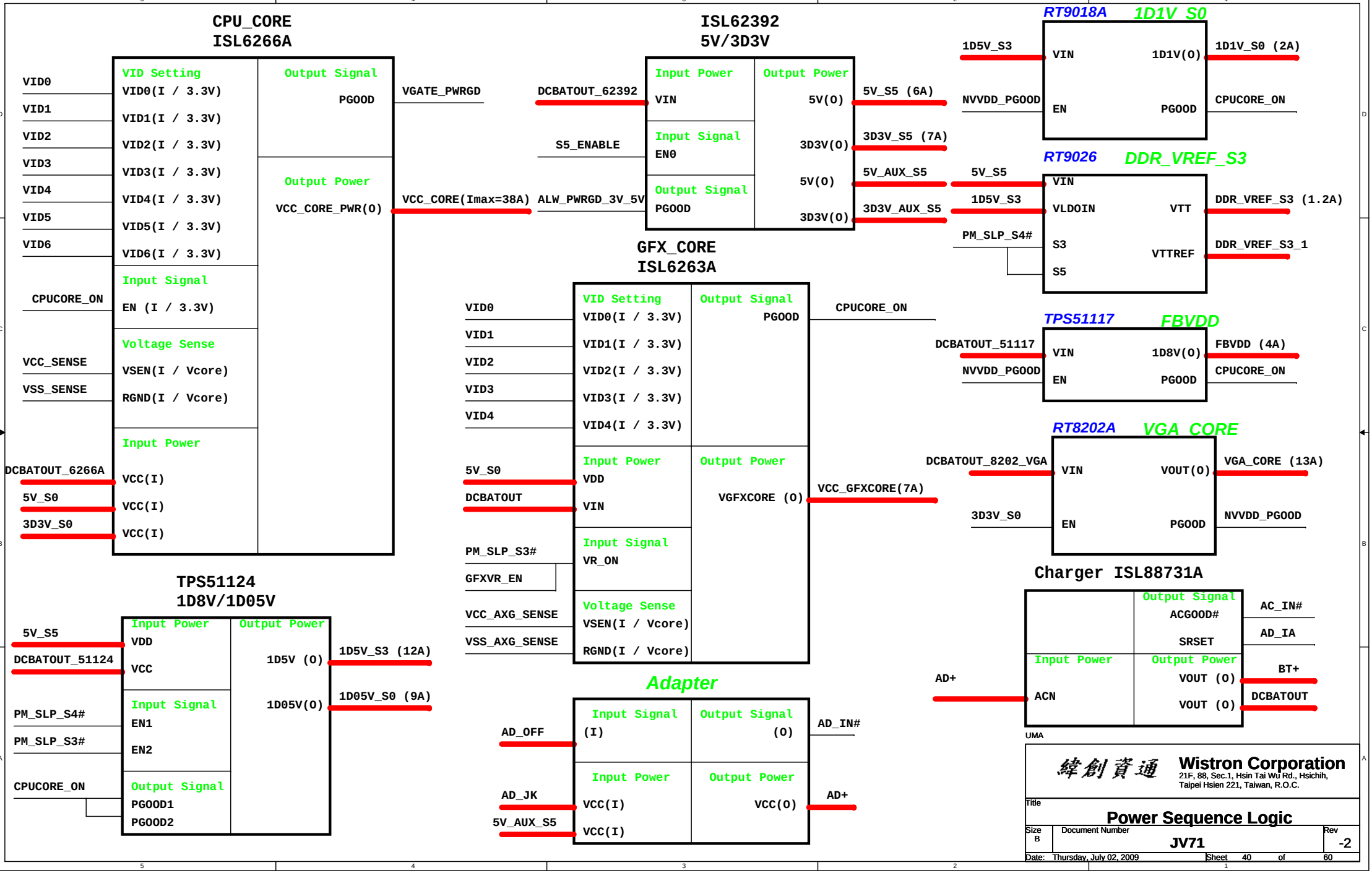
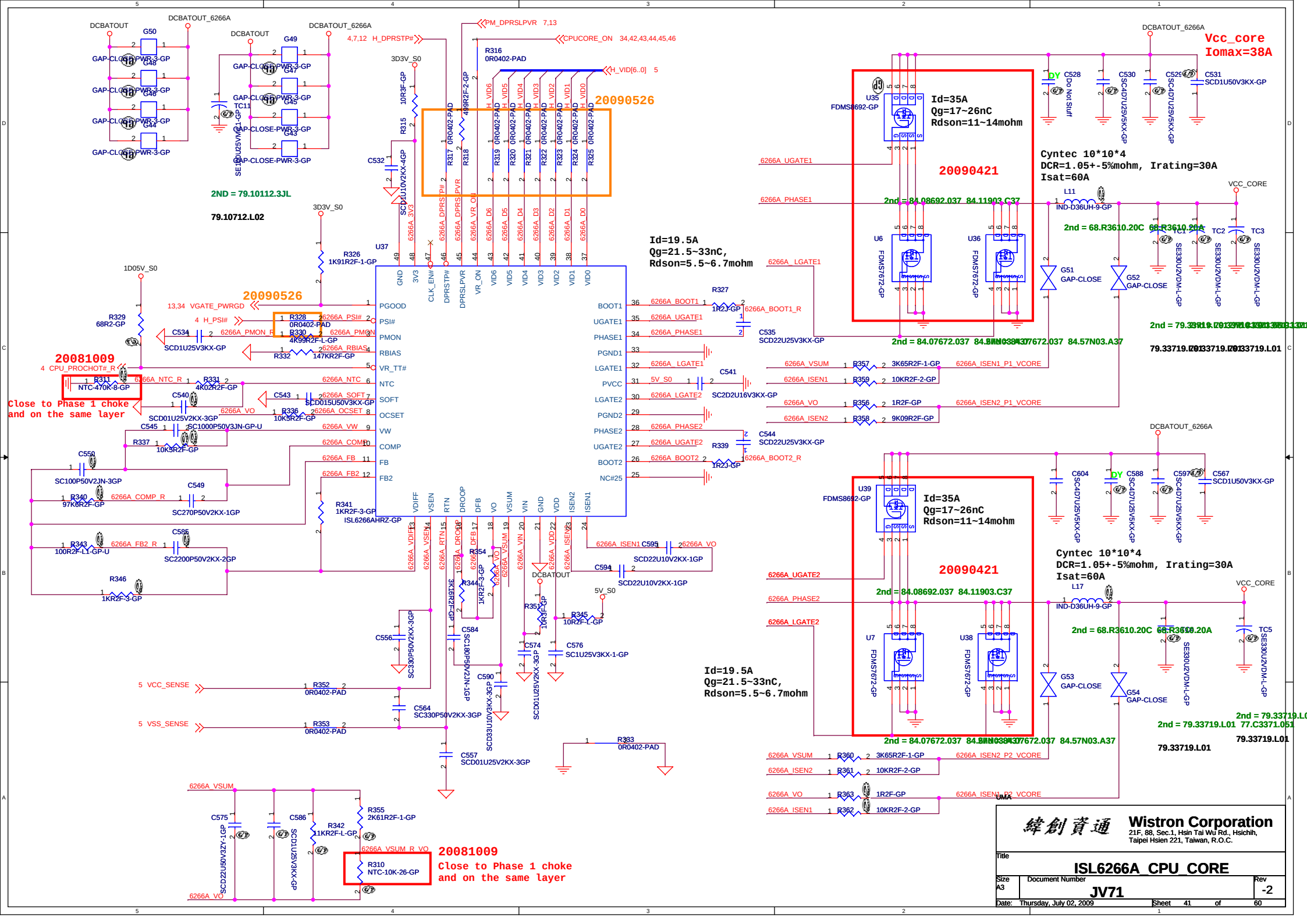
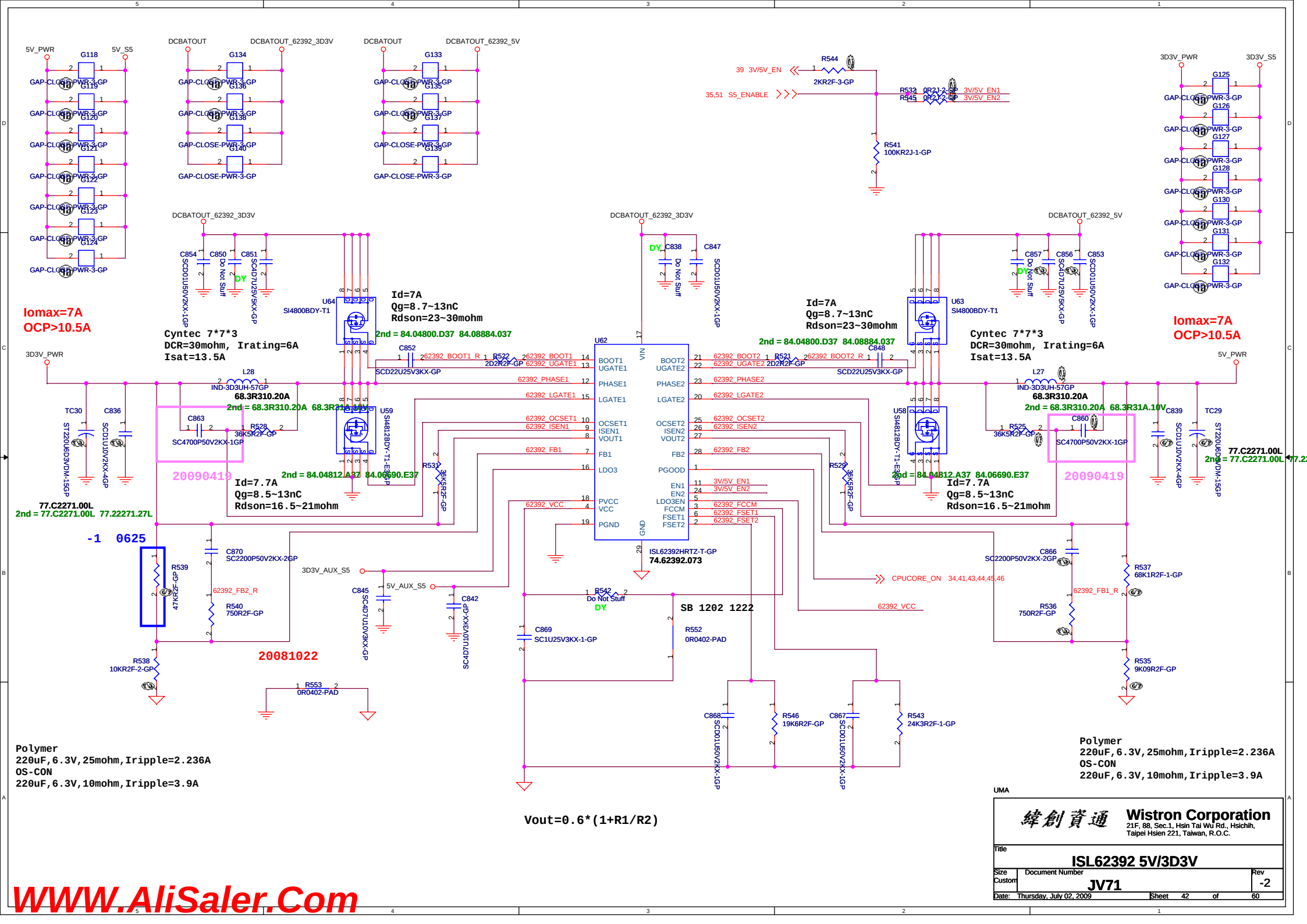



Vcc_core
Iomax=38A
Id=35A
Qg=17~26nC
Rdson=11~14mohm
20090421
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
20090526
20081009
Close to Phase 1 choke
and on the same layer
2ND = 79.10112.3JL
79.10712.L02
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A_CPU_CORE
JV71
Thursday, July 02, 2009



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL62392 5V/3D3V**

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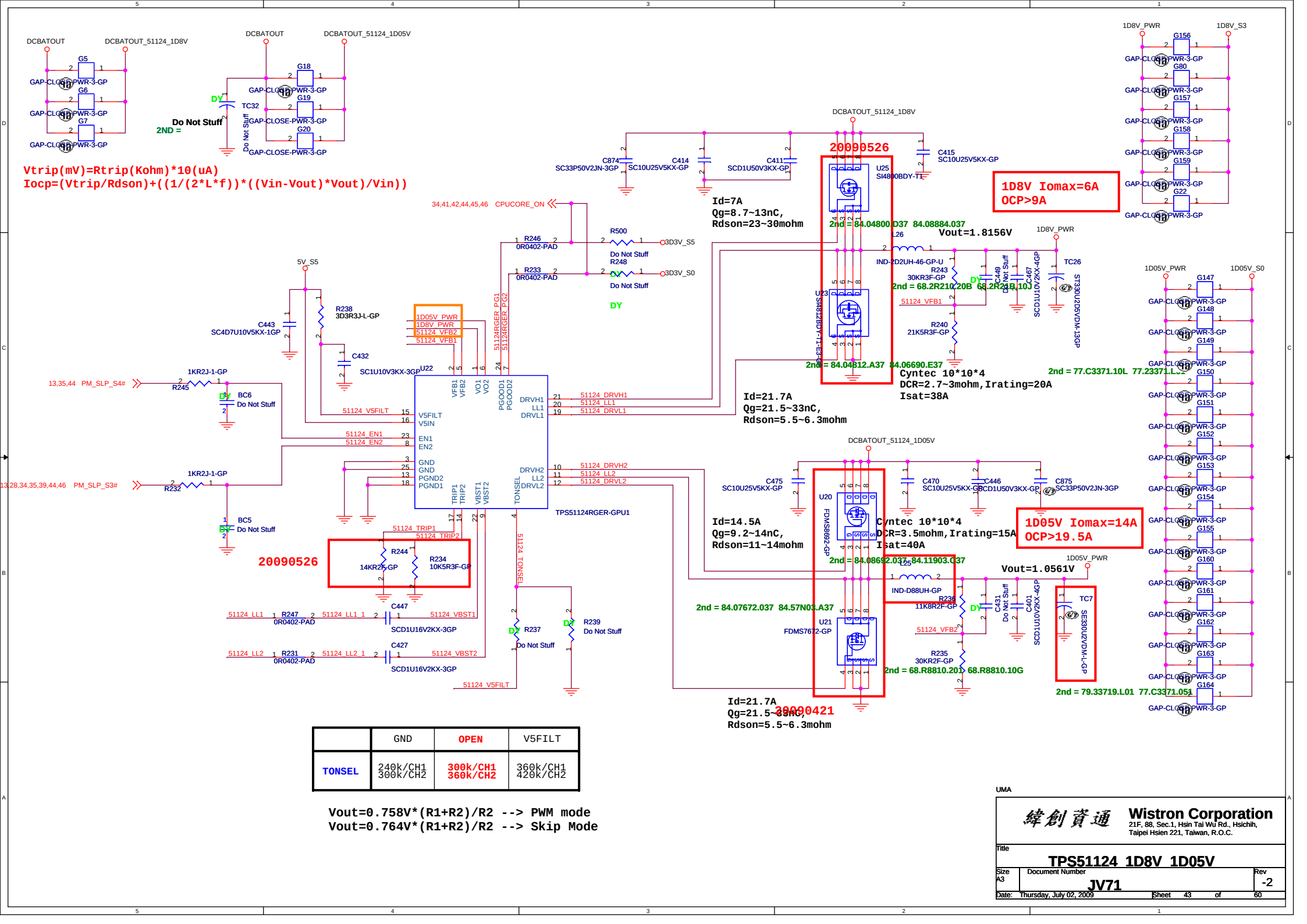
DCBATOUT
DCBATOUT_51124_1D8V
DCBATOUT_51124_1D05V
Do Not Stuff
2ND =
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
1D8V_PWR
1D8V_S3
1D05V_PWR
1D05V_S0
5V_S5
3D3V_S5
3D3V_S0
CPUCORE_ON
PM_SLP_S4#
PM_SLP_S3#
TPS51124RGER-GPU1
20090526
20090421
Id=7A
Qg=8.7~13nC,
Rdson=23~30mohm
1D8V Iomax=6A
OCP>9A
Vout=1.8156V
Cyntec 10*10*4
DCR=2.7~3mohm,Irating=20A
Isat=38A
Id=21.7A
Qg=21.5~33nC,
Rdson=5.5~6.3mohm
Id=14.5A
Qg=9.2~14nC,
Rdson=11~14mohm
Cyntec 10*10*4
DCR=3.5mohm,Irating=15A
Isat=40A
1D05V Iomax=14A
OCP>19.5A
Vout=1.0561V
Id=21.7A
Qg=21.5~33nC,
Rdson=5.5~6.3mohm
Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode
TONSEL
GND
OPEN
V5FILT
240k/CH1
300k/CH2
300k/CH1
360k/CH2
360k/CH1
420k/CH2
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51124 1D8V 1D05V
Size
A3
Document Number
JV71
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-2
Date: Thursday, July 02, 2009
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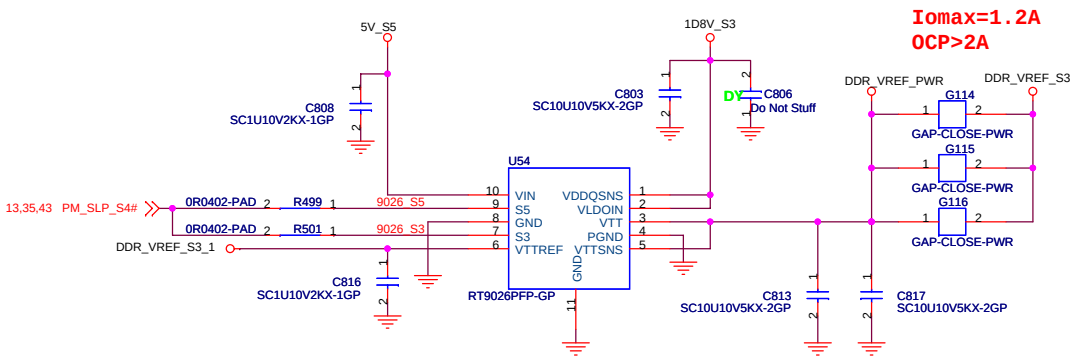

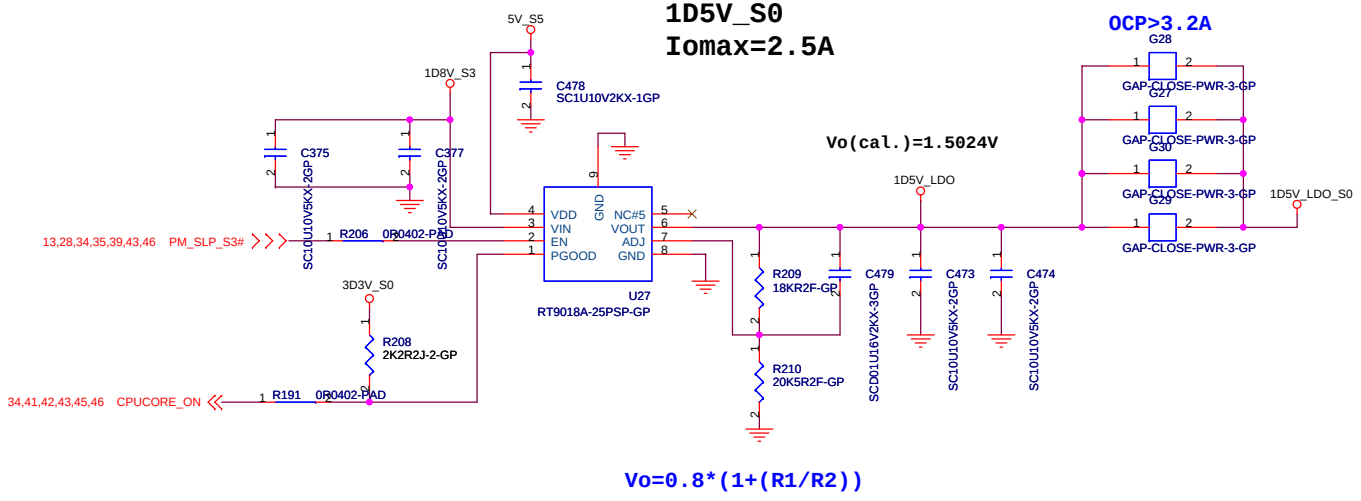

UMA

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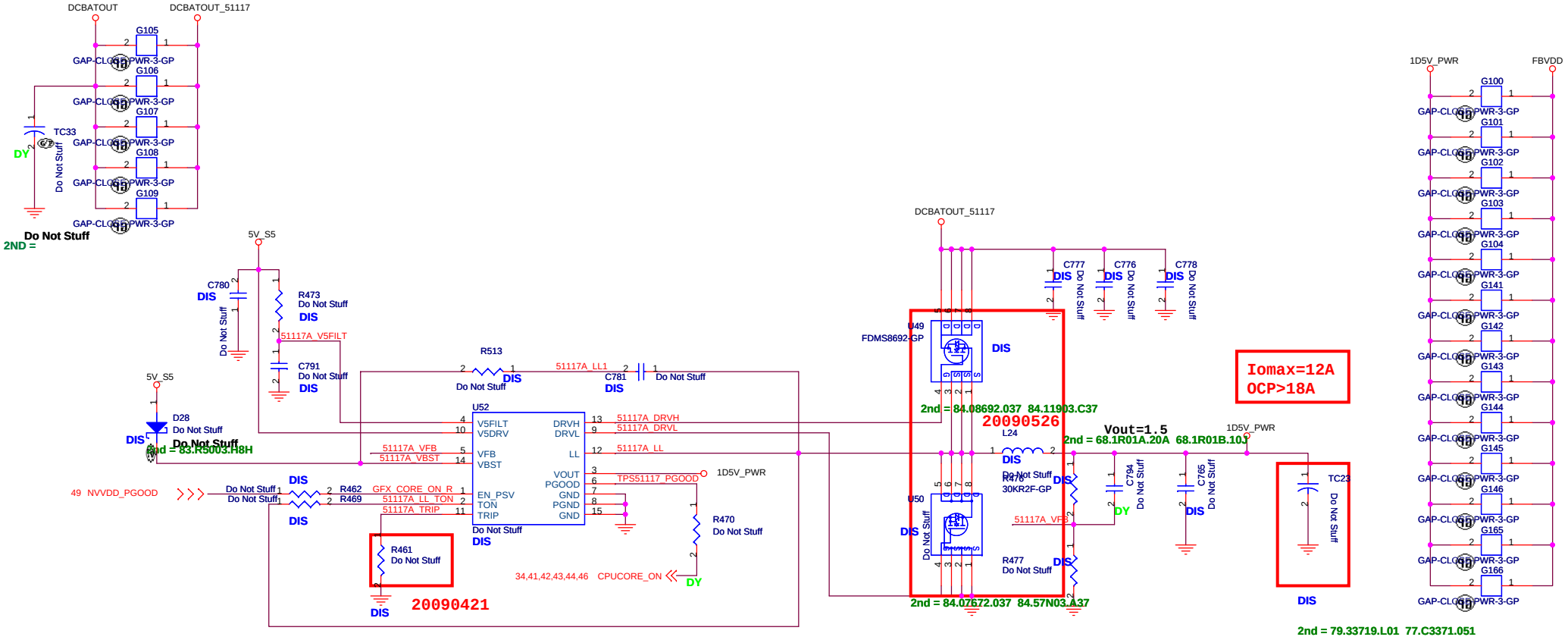
Title: 0D75V		
Size: A3	Document Number: JV71	Rev: -2
Date: Thursday, July 02, 2009	Sheet 44 of 60	



Vout=0.75V*(R1+R2)/R2

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51117_1D8V

Size: A3 | Document Number: JV71 | Rev: -2

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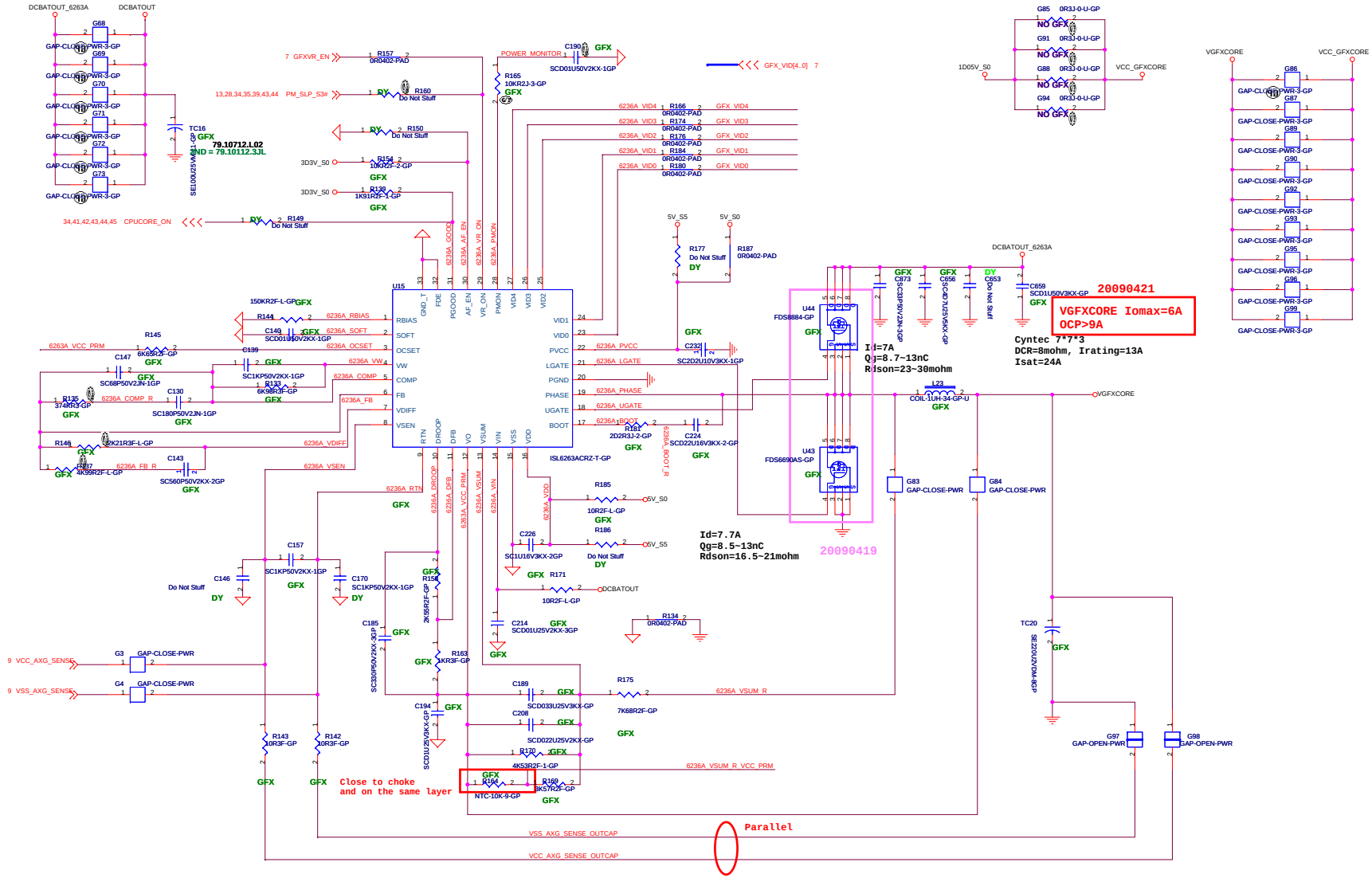

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6263A_GFX CORE

Size: Custom | Document Number: JV71 | Rev: -2

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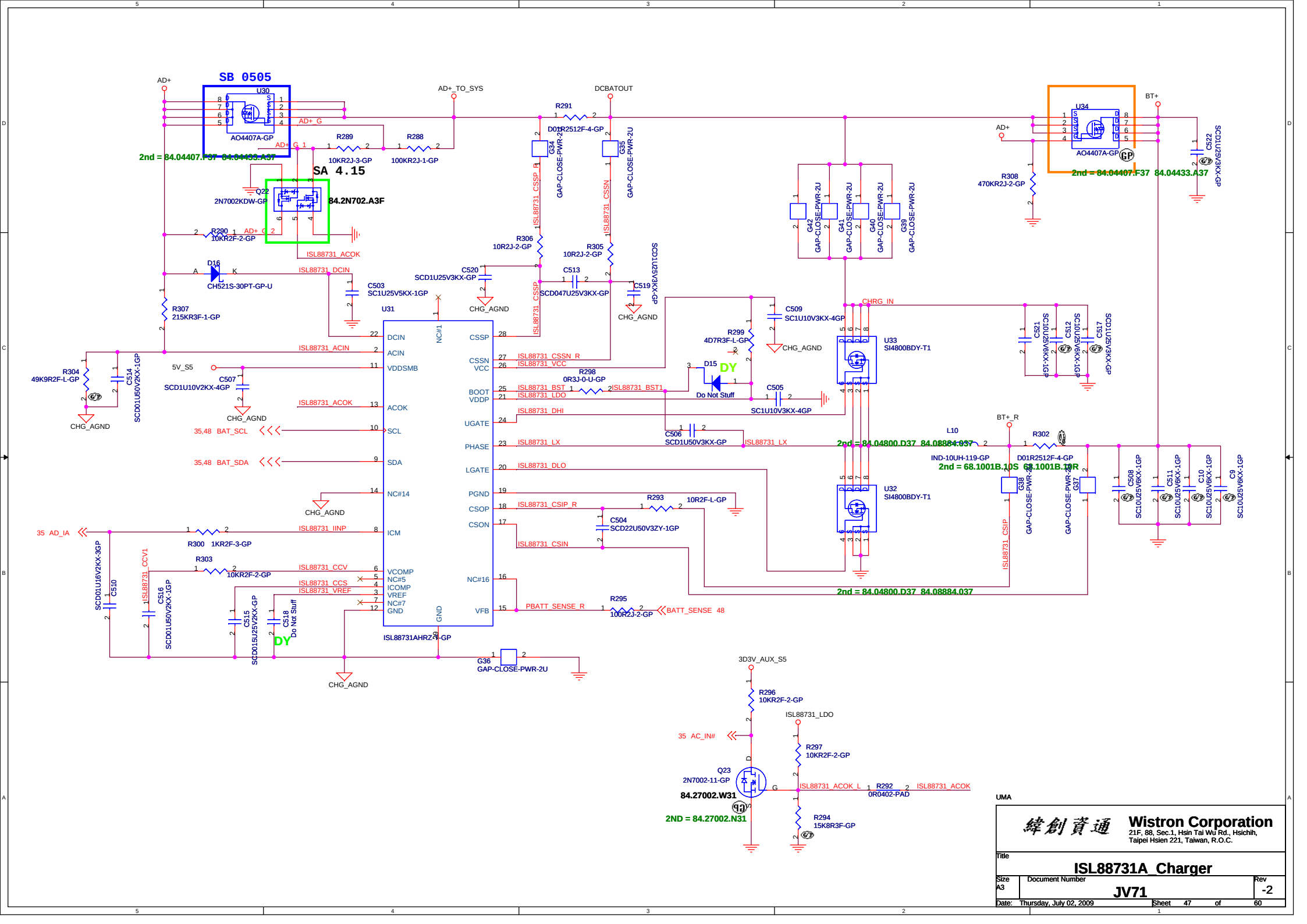
SB 0505
SA 4.15
84.2N702.A3F
2nd = 84.04407.F37 84.04433.A37
2nd = 84.04800.D37 84.08884.037
2nd = 68.1001B.10S 68.1001B.10R
2ND = 84.27002.N31
ISL88731AHRZ-T-GP
AO4407A-GP
2N7002KDW-GP
2N7002-11-GP
CH521S-30PT-GP-U
IND-10UH-119-GP
SI4800BDY-T1
Do Not Stuff
DY
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A_Charger
Size A3
Document Number
JV71
Rev -2
Date: Thursday, July 02, 2009
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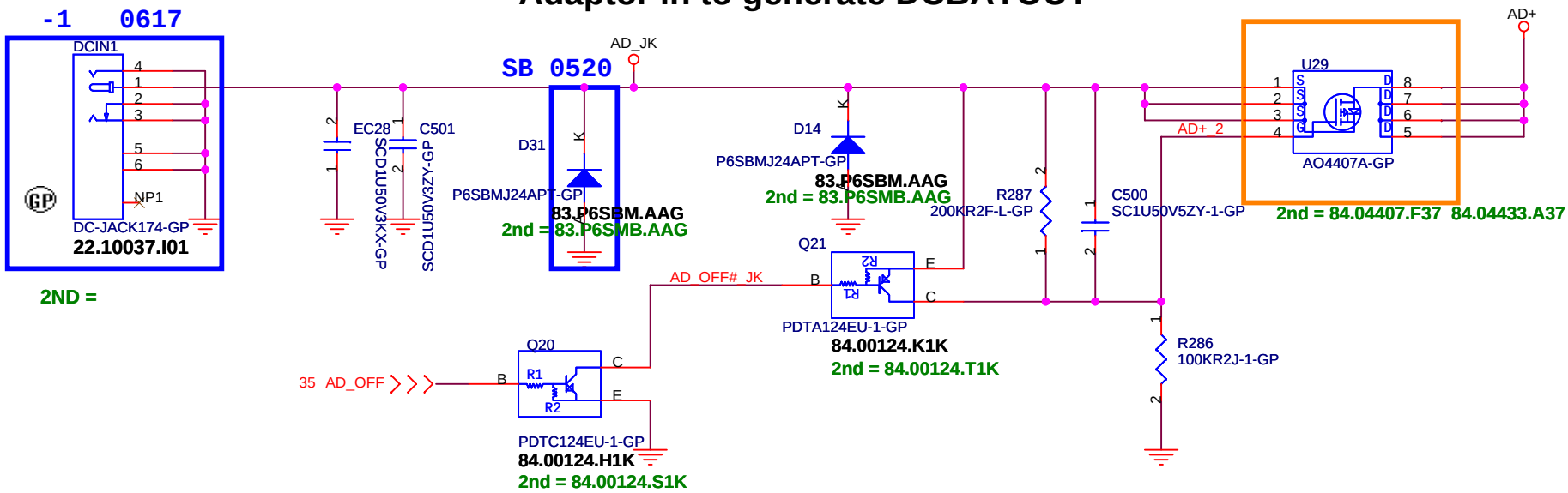
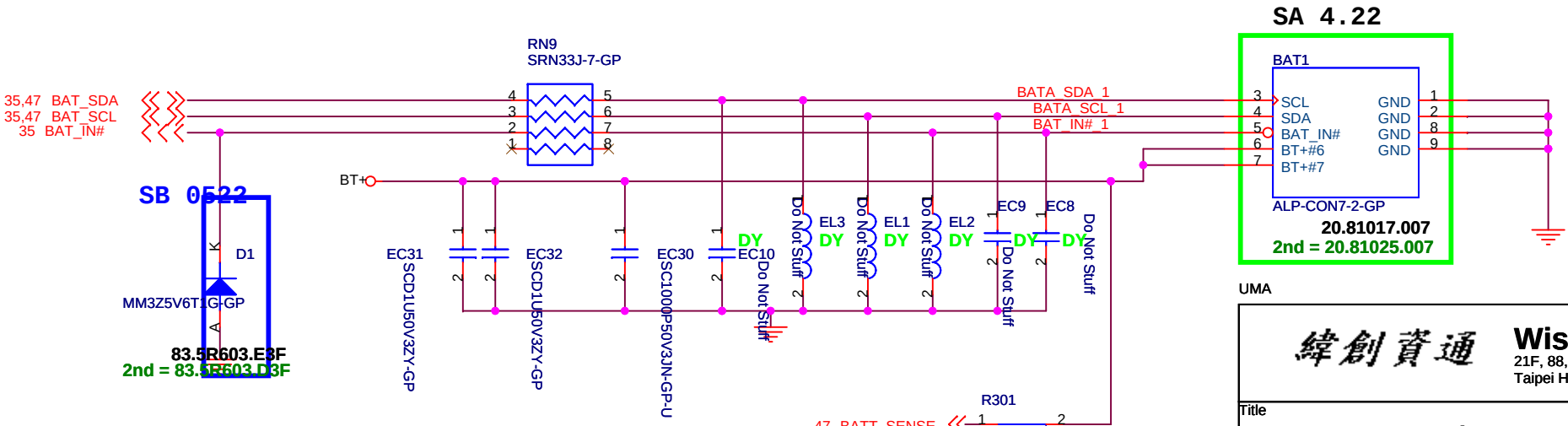
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

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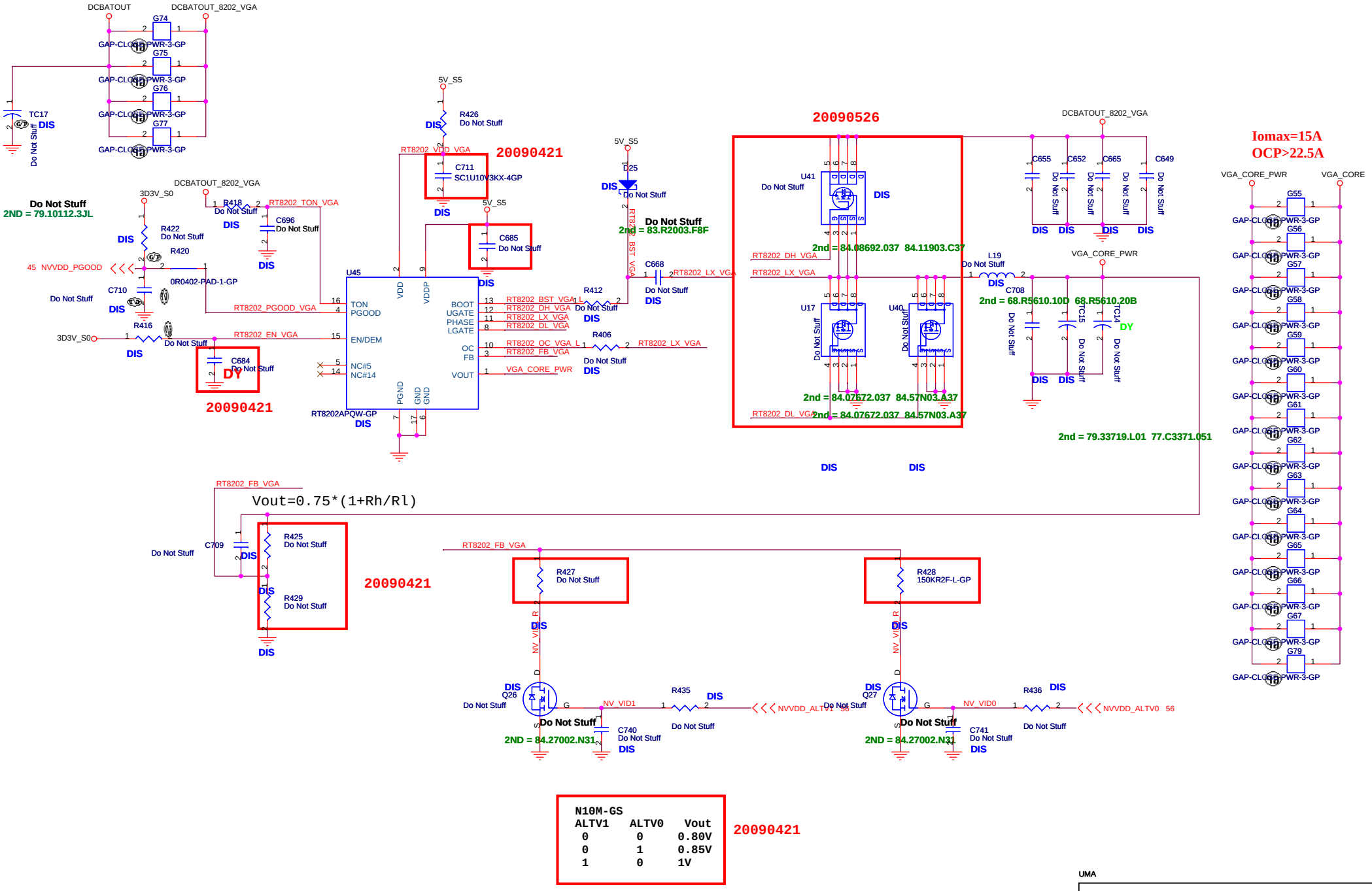
DCBATOUT
DCBATOUT_8202_VGA
G74
G75
G76
G77
GAP-CLOSE-PWR-3-GP
TC17
DIS
Do Not Stuff
5V_S5
R426
Do Not Stuff
RT8202_VDD_VGA
20090421
C711
SC1U10V3KX-4GP
C685
Do Not Stuff
3D3V_S0
R418
R422
R420
0R0402-PAD-1-GP
45 NVVDD_PGOOD
C710
C696
RT8202_TON_VGA
RT8202_PGOOD_VGA
RT8202_EN_VGA
R416
C684
DY
20090421
U45
TON
PGOOD
EN/DEM
NC#5
NC#14
VDD
VDDP
PGND
GND
BOOT
UGATE
PHASE
LGATE
OC
FB
VOUT
RT8202_BST_VGA
RT8202_DH_VGA
RT8202_LX_VGA
RT8202_DL_VGA
RT8202_OC_VGA_L
RT8202_FB_VGA
VGA_CORE_PWR
RT8202APQW-GP
D25
R412
R406
C668
Do Not Stuff
2nd = 83.R2003.F8F
20090526
U41
U17
U40
2nd = 84.08692.037 84.11903.C37
2nd = 84.07672.037 84.57N03.A37
L19
C708
2nd = 68.R5610.10D 68.R5610.20B
C655
C652
C665
C649
TC15
TC14
2nd = 79.33719.L01 77.C3371.051
Iomax=15A
OCP>22.5A
VGA_CORE_PWR
VGA_CORE
G55
G56
G57
G58
G59
G60
G61
G62
G63
G64
G65
G66
G67
G79
Vout=0.75*(1+Rh/Rl)
C709
R425
R429
20090421
R427
R428
150KR2F-L-GP
NV_VID1_R
NV_VID0_R
Q26
Q27
R435
R436
NV_VID1
NV_VID0
NVVDD_ALTV1 56
NVVDD_ALTV0 56
C740
C741
2ND = 84.27002.N31
N10M-GS
ALTV1 ALTV0 Vout
0 0 0.80V
0 1 0.85V
1 0 1V
20090421
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8202A VGA CORE
Size
A3
Document Number
JV71
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-2
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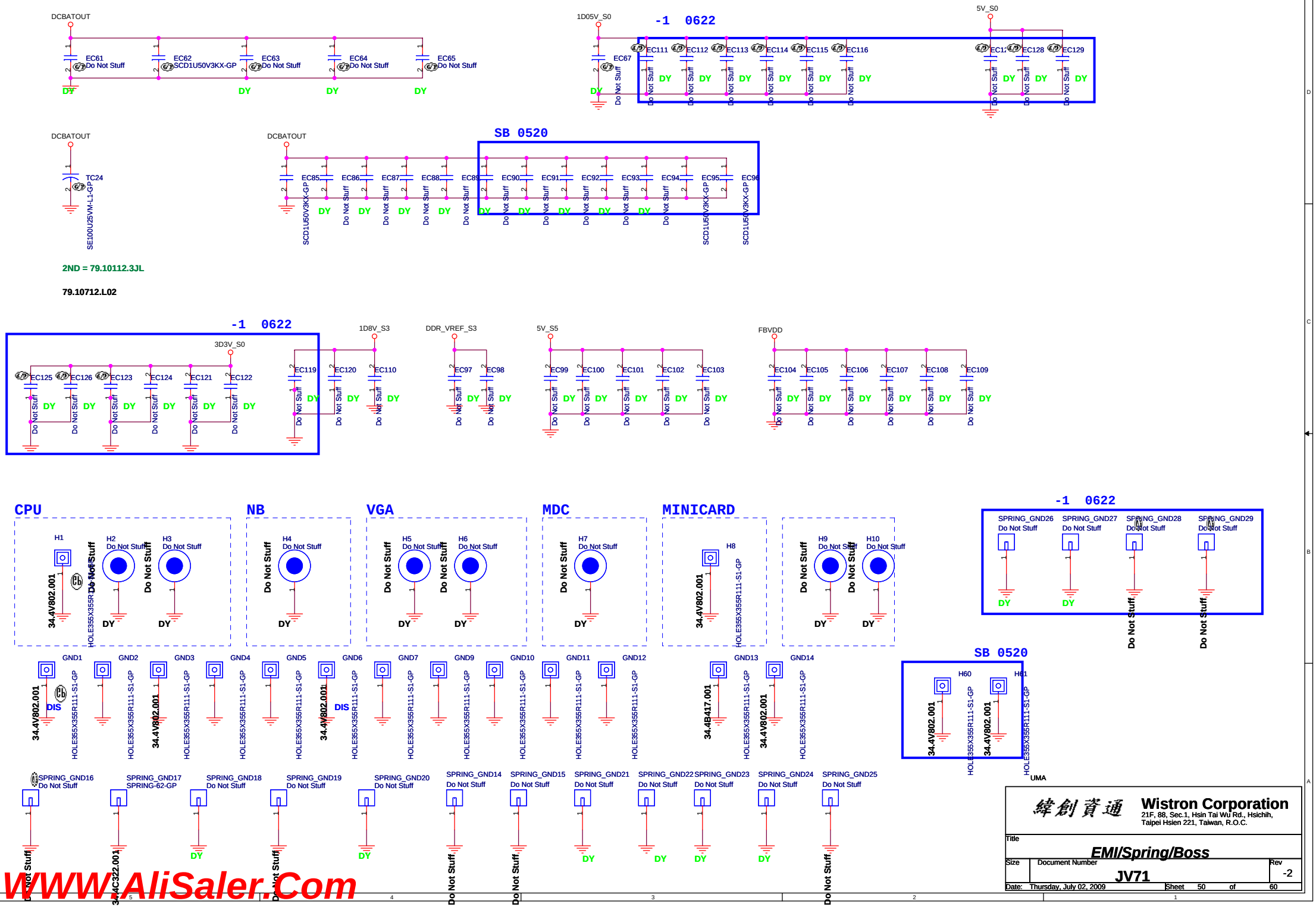
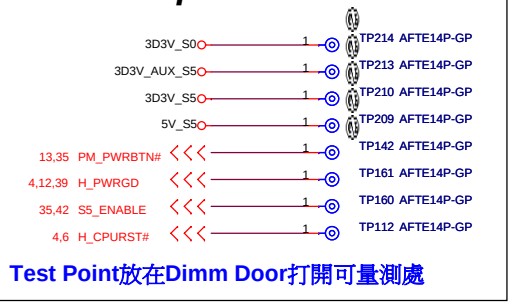


Check test point



Test Point放在Dimm Door打開可量測處

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Taipei Hsien 221, Taiwan, R.O.C.

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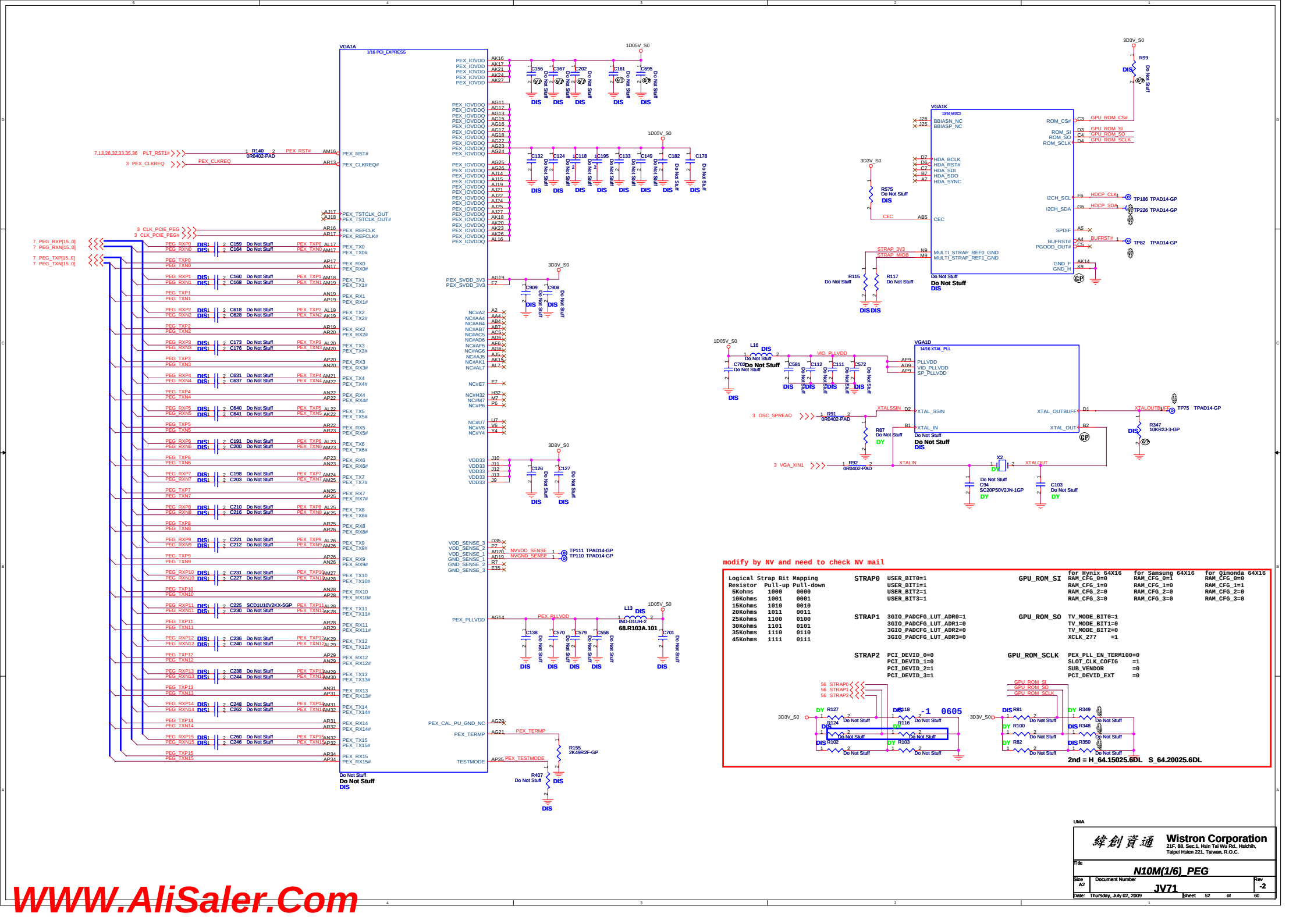

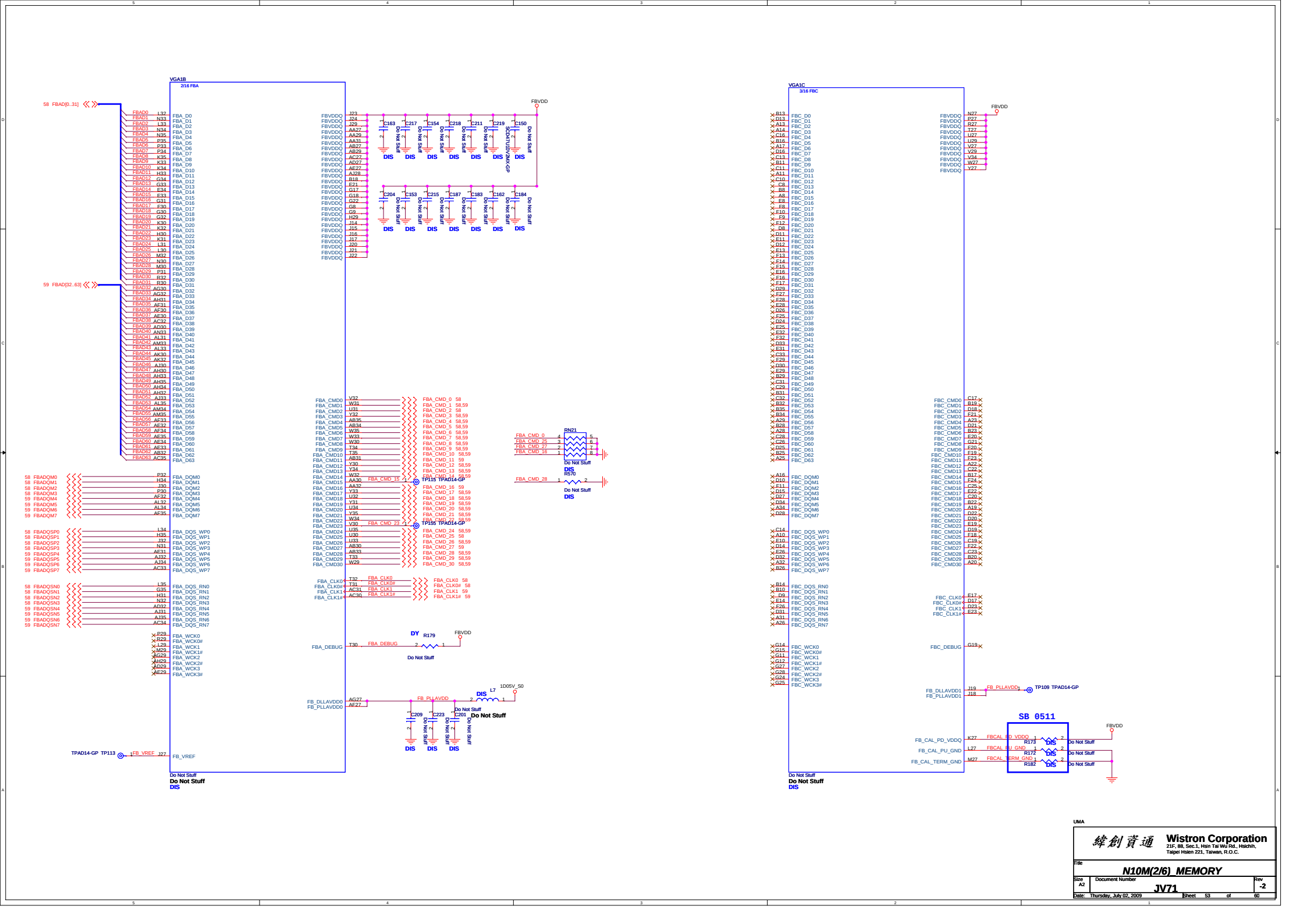
VGA1B
2/16 FBA
VGA1C
3/16 FBC
FBVDD
Do Not Stuff
DIS
SB 0511
TP109 TPAD14-GP
TP115 TPAD14-GP
TP195 TPAD14-GP
TPAD14-GP TP113
RN21
R570
R179
L7
1D05V_S0
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N10M(2/6)_MEMORY
Size
A2
Document Number
JV71
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-2
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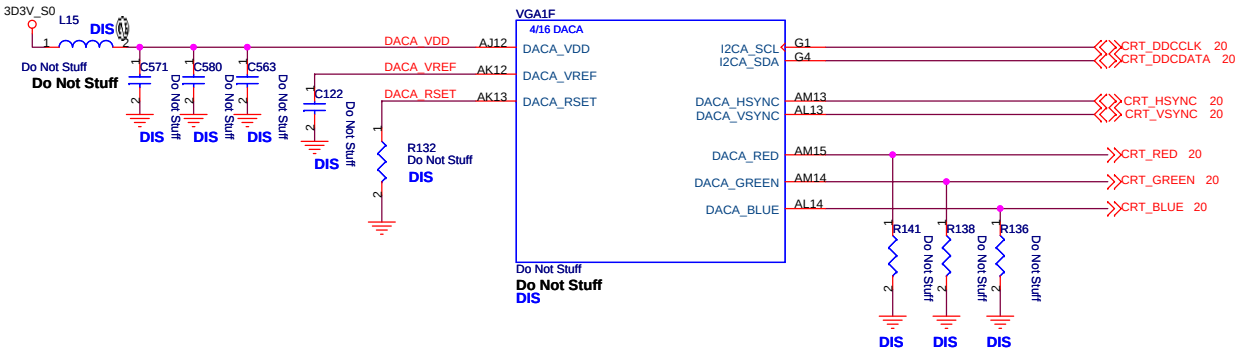

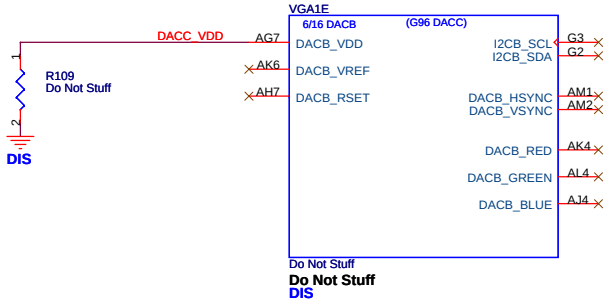

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N10M(3/6) DAC***

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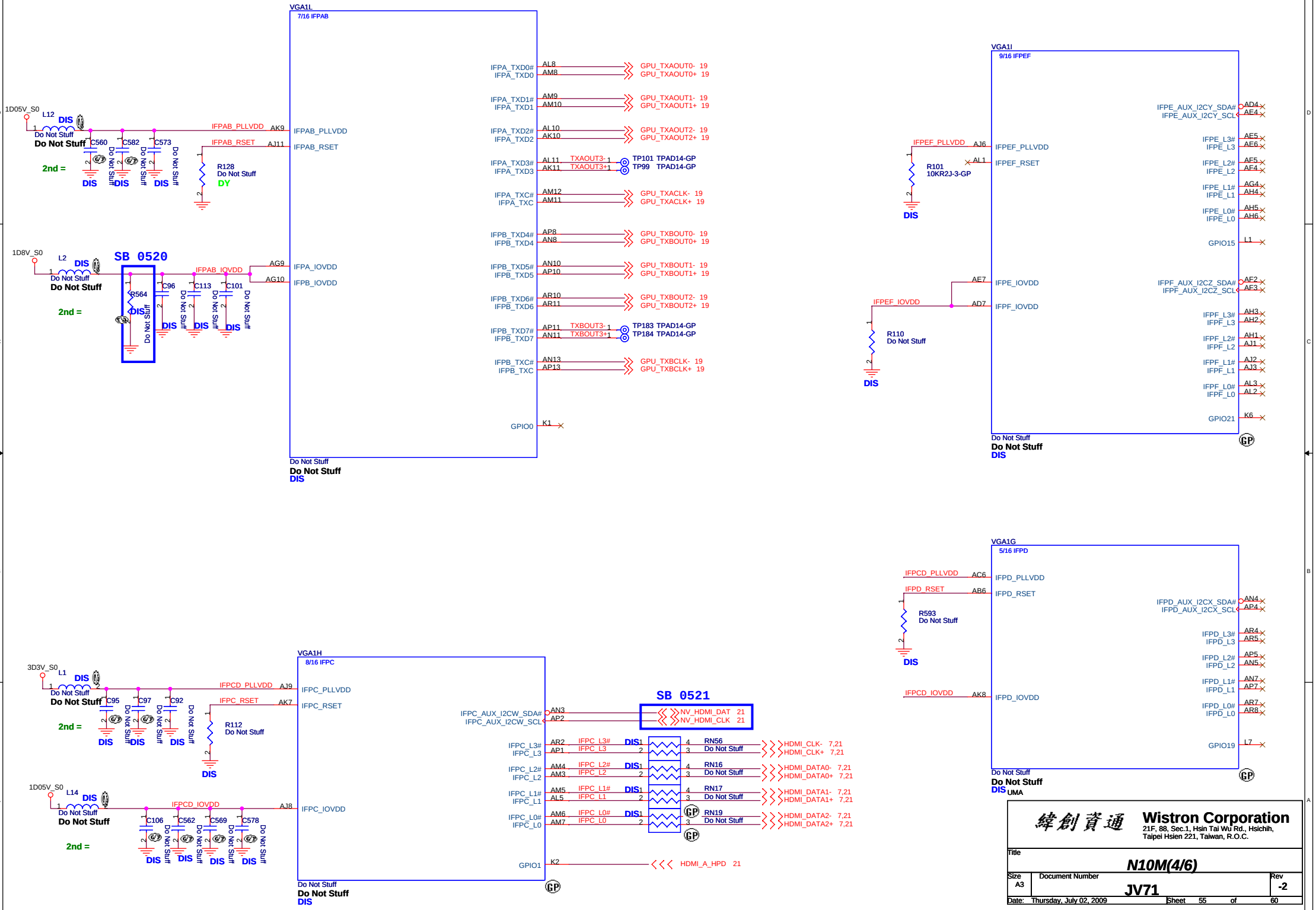
VGA1L
7/16 IFPAB
1D05V_S0
L12
DIS
Do Not Stuff
Do Not Stuff
C560
C582
C573
2nd =
DIS
IFPAB_PLLVDD
AK9
IFPAB_RSET
AJ11
R128
Do Not Stuff
DY
1D8V_S0
L2
SB 0520
IFPAB_IOVDD
AG9
AG10
R564
C96
C113
C101
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXD0#
IFPA_TXD0
AL8
AM8
GPU_TXAOUT0- 19
GPU_TXAOUT0+ 19
IFPA_TXD1#
IFPA_TXD1
AM9
AM10
GPU_TXAOUT1- 19
GPU_TXAOUT1+ 19
IFPA_TXD2#
IFPA_TXD2
AL10
AK10
GPU_TXAOUT2- 19
GPU_TXAOUT2+ 19
IFPA_TXD3#
IFPA_TXD3
AL11
AK11
TXAOUT3-
TXAOUT3+
TP101 TPAD14-GP
TP99 TPAD14-GP
IFPA_TXC#
IFPA_TXC
AM12
AM11
GPU_TXACLK- 19
GPU_TXACLK+ 19
IFPB_TXD4#
IFPB_TXD4
AP8
AN8
GPU_TXBOUT0- 19
GPU_TXBOUT0+ 19
IFPB_TXD5#
IFPB_TXD5
AN10
AP10
GPU_TXBOUT1- 19
GPU_TXBOUT1+ 19
IFPB_TXD6#
IFPB_TXD6
AR10
AR11
GPU_TXBOUT2- 19
GPU_TXBOUT2+ 19
IFPB_TXD7#
IFPB_TXD7
AP11
AN11
TXBOUT3-
TXBOUT3+
TP183 TPAD14-GP
TP184 TPAD14-GP
IFPB_TXC#
IFPB_TXC
AN13
AP13
GPU_TXBCLK- 19
GPU_TXBCLK+ 19
GPIO0
K1
Do Not Stuff
DIS
VGA1I
9/16 IFPEF
IFPEF_PLLVDD
AJ6
IFPEF_RSET
AL1
R101
10KR2J-3-GP
IFPEF_IOVDD
AE7
AD7
R110
Do Not Stuff
IFPE_IOVDD
IFPF_IOVDD
IFPE_AUX_I2CY_SDA#
IFPE_AUX_I2CY_SCL
AD4
AE4
IFPE_L3#
IFPE_L3
AE5
AE6
IFPE_L2#
IFPE_L2
AF5
AF4
IFPE_L1#
IFPE_L1
AG4
AH4
IFPE_L0#
IFPE_L0
AH5
AH6
GPIO15
L1
IFPF_AUX_I2CZ_SDA#
IFPF_AUX_I2CZ_SCL
AF2
AF3
IFPF_L3#
IFPF_L3
AH3
AH2
IFPF_L2#
IFPF_L2
AH1
AJ1
IFPF_L1#
IFPF_L1
AJ2
AJ3
IFPF_L0#
IFPF_L0
AL3
AL2
GPIO21
K6
Do Not Stuff
Do Not Stuff
DIS
GP
3D3V_S0
L1
DIS
Do Not Stuff
Do Not Stuff
C95
C97
C92
2nd =
IFPCD_PLLVDD
AJ9
IFPC_RSET
AK7
R112
Do Not Stuff
1D05V_S0
L14
C106
C562
C569
C578
IFPCD_IOVDD
AJ8
VGA1H
8/16 IFPC
IFPC_PLLVDD
IFPC_RSET
IFPC_IOVDD
IFPC_AUX_I2CW_SDA#
IFPC_AUX_I2CW_SCL
AN3
AP2
SB 0521
NV_HDMI_DAT 21
NV_HDMI_CLK 21
IFPC_L3#
IFPC_L3
AR2
AP1
RN56
Do Not Stuff
HDMI_CLK- 7,21
HDMI_CLK+ 7,21
IFPC_L2#
IFPC_L2
AM4
AM3
RN16
Do Not Stuff
HDMI_DATA0- 7,21
HDMI_DATA0+ 7,21
IFPC_L1#
IFPC_L1
AM5
AL5
RN17
Do Not Stuff
HDMI_DATA1- 7,21
HDMI_DATA1+ 7,21
IFPC_L0#
IFPC_L0
AM6
AM7
RN19
Do Not Stuff
HDMI_DATA2- 7,21
HDMI_DATA2+ 7,21
GPIO1
K2
HDMI_A_HPD 21
VGA1G
5/16 IFPD
IFPCD_PLLVDD
AC6
IFPD_RSET
AB6
R593
Do Not Stuff
IFPCD_IOVDD
AK8
IFPD_PLLVDD
IFPD_RSET
IFPD_IOVDD
IFPD_AUX_I2CX_SDA#
IFPD_AUX_I2CX_SCL
AN4
AP4
IFPD_L3#
IFPD_L3
AR4
AR5
IFPD_L2#
IFPD_L2
AP5
AN5
IFPD_L1#
IFPD_L1
AN7
AP7
IFPD_L0#
IFPD_L0
AR7
AR8
GPIO19
L7
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N10M(4/6)
Size
A3
Document Number
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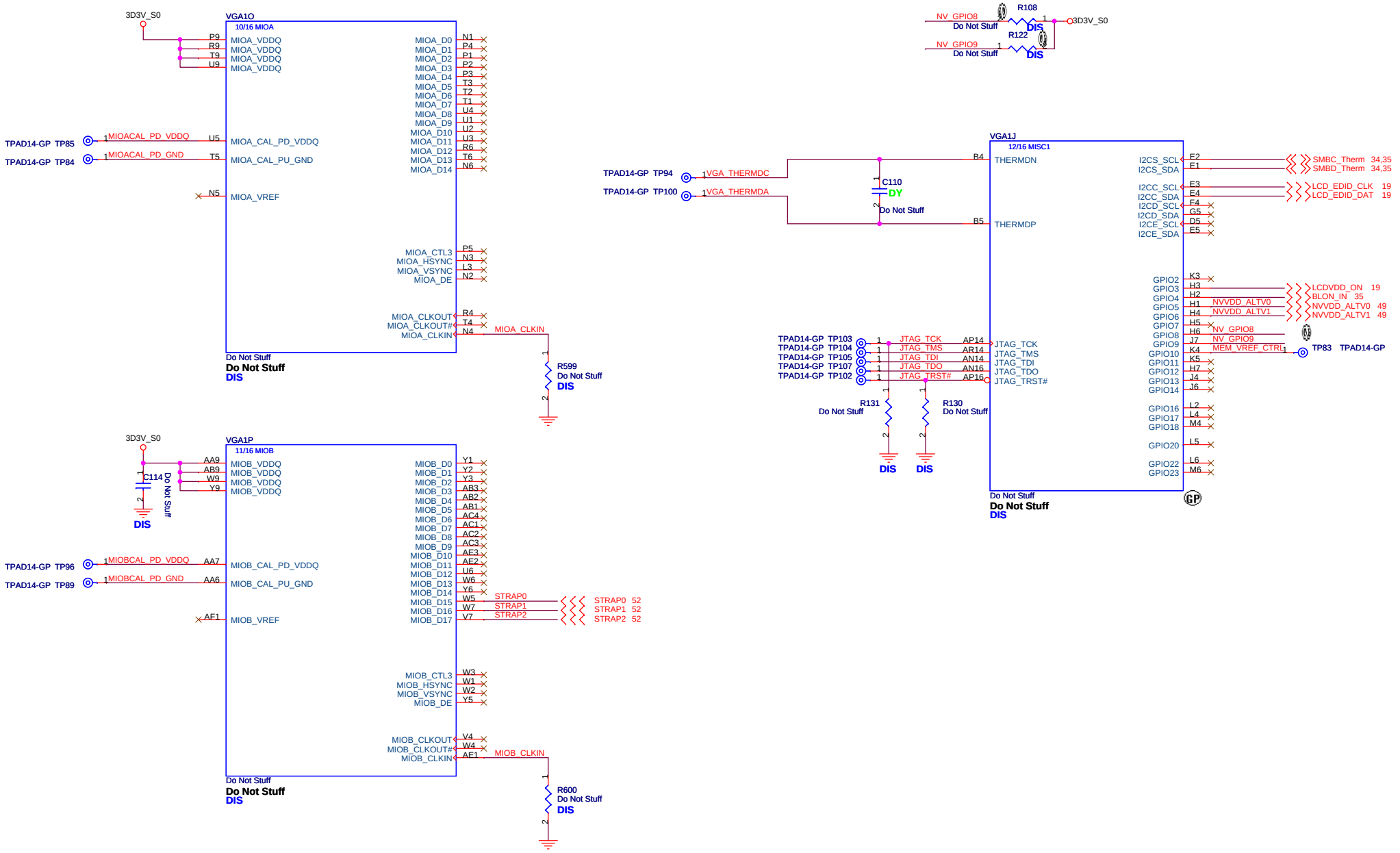

UMA

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Title	***N10M(5/6) MIO/ GPIO***	
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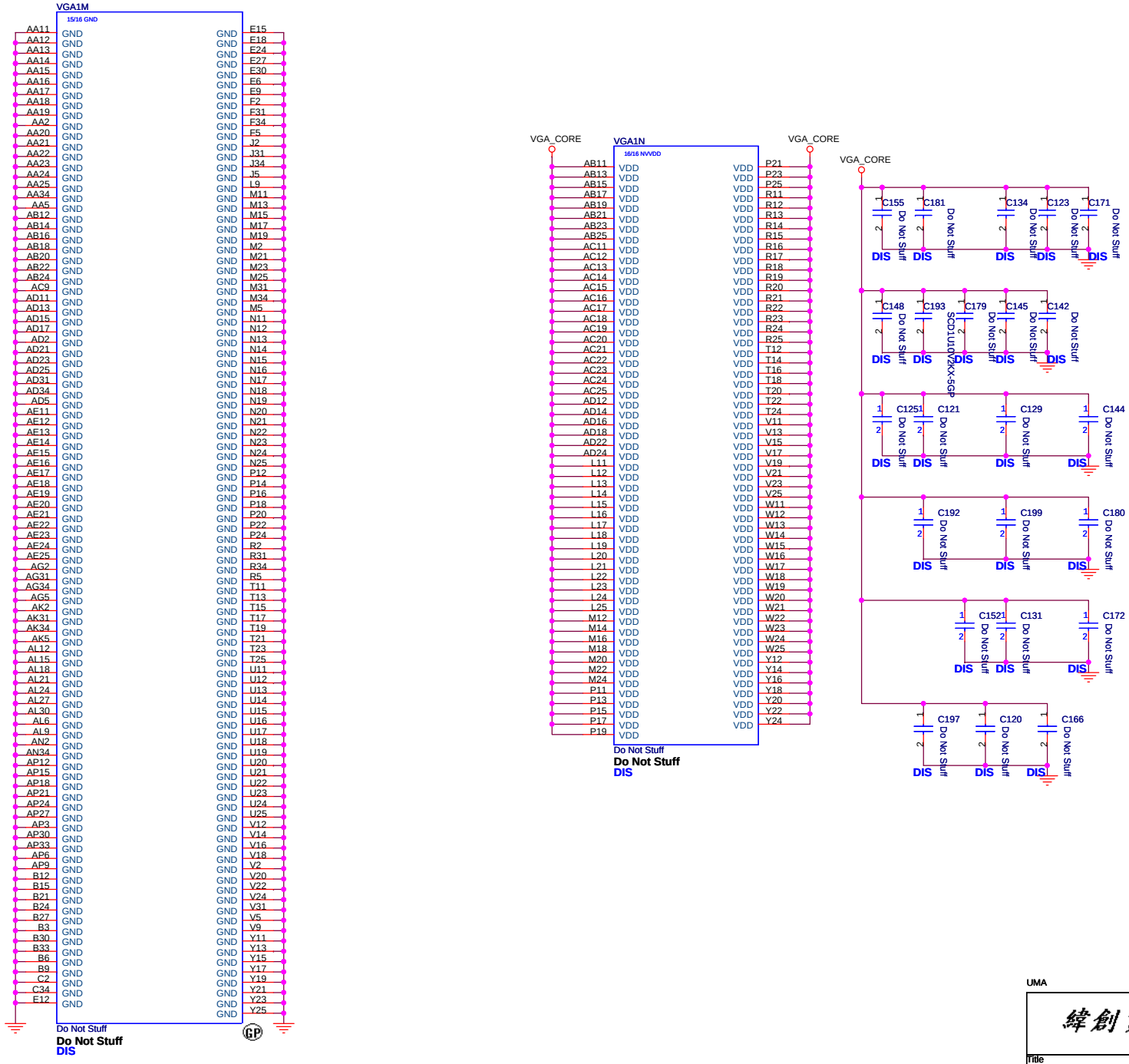

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N10M(6/6) POWER***

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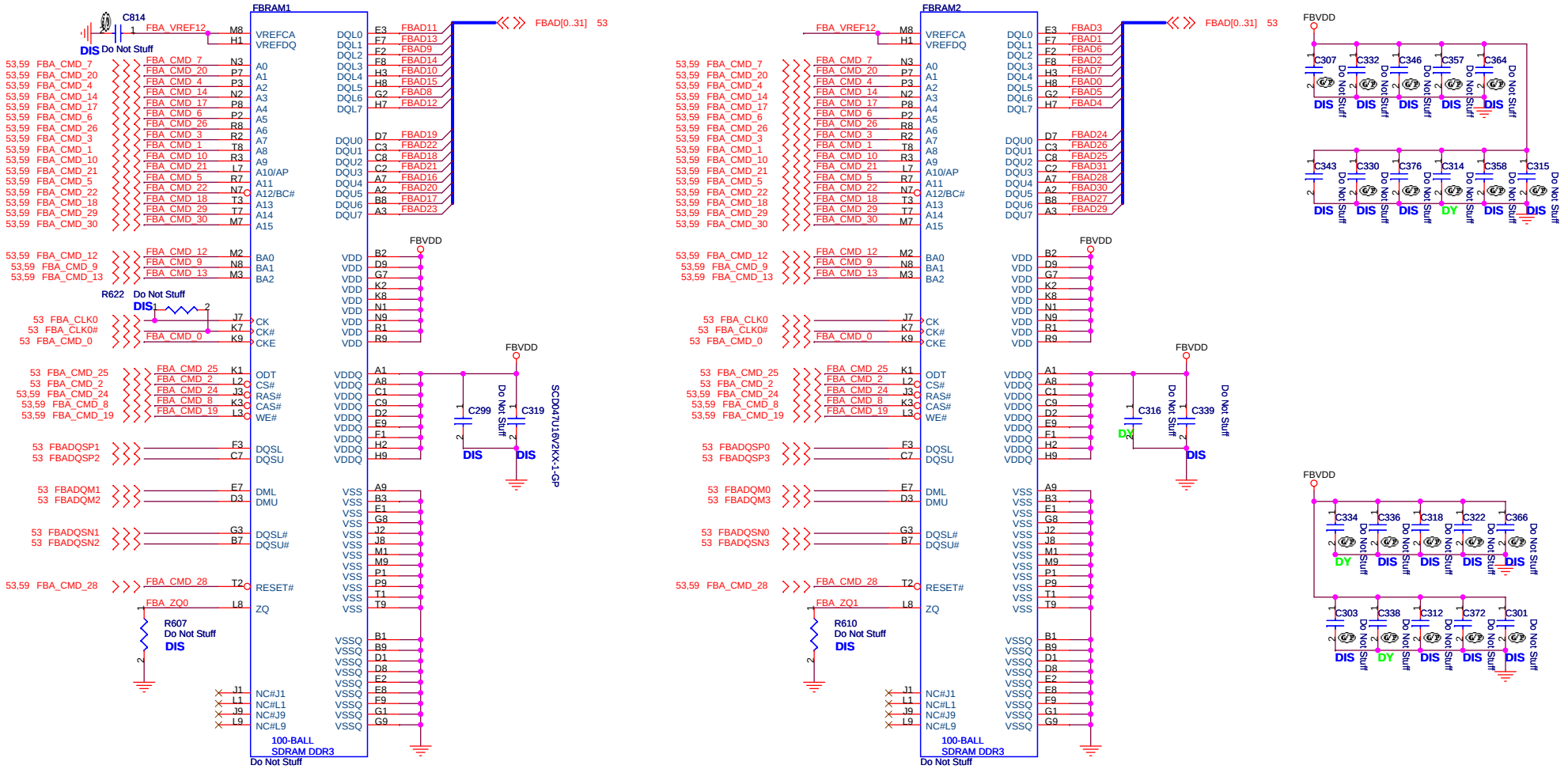


2ND = H_72.51G63.C0U S_72.41164.H0U

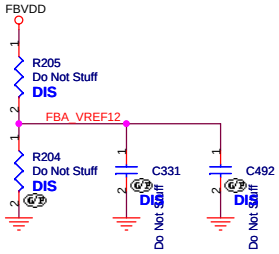
DIS

2ND = H_72.51G63.C0U S_72.41164.H0U

DIS

FB CMD mapping Mode C-N10M
<Mirror Mode>

DDR3 Power consumption 1.5V@800MHz
Hynix :IDD4W=220.4mA
Samsung :IDD7=150.4mA (calcurated)



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Title: ***VRAM(1/2)***

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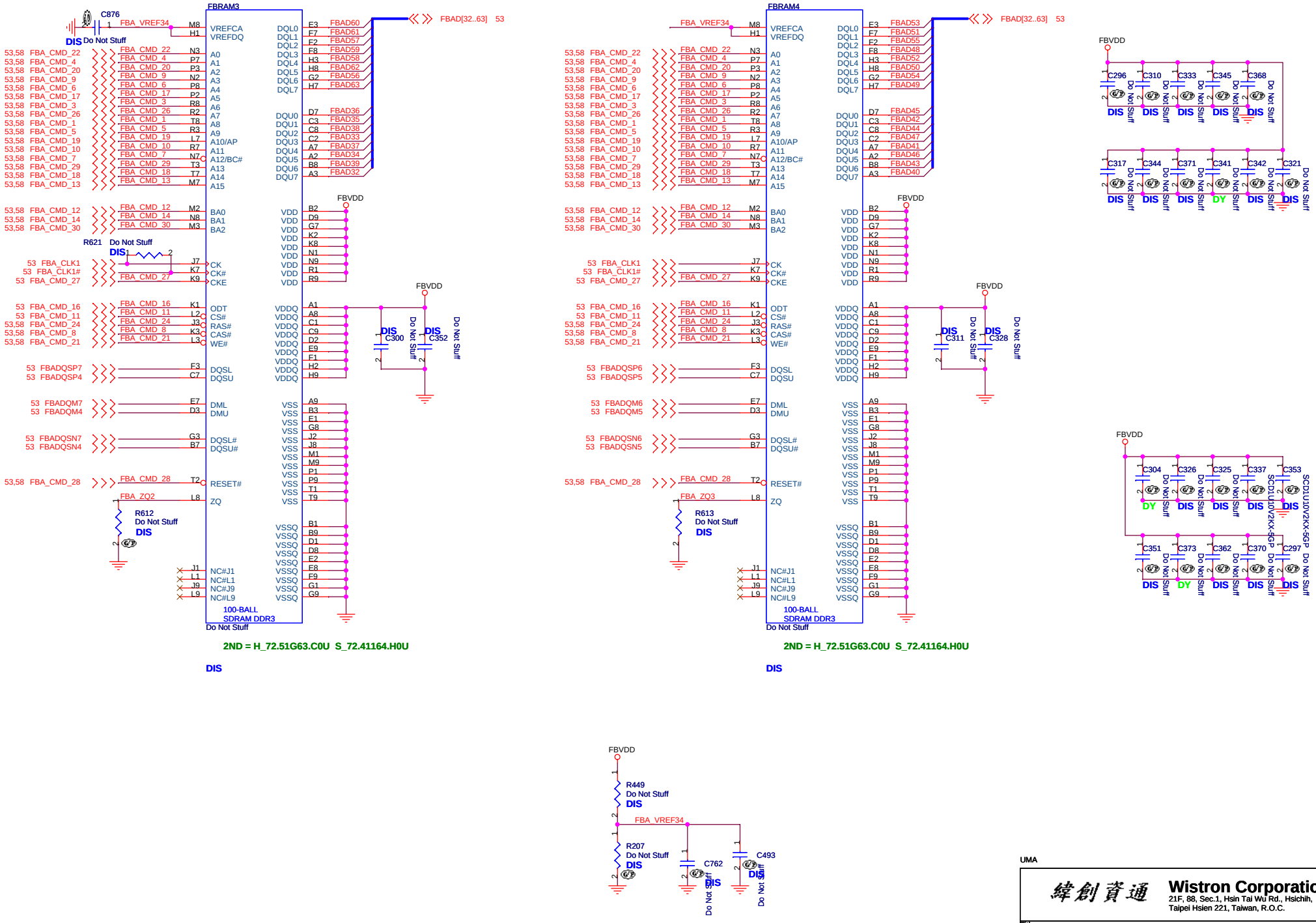
FBRAM3
FBRAM4
C876
DIS
Do Not Stuff
FBA_VREF34
FBAD[32..63] 53
FBVDD
R621
FBA_CLK1
FBA_CLK1#
FBA_CMD_27
FBA_CMD_16
FBA_CMD_11
FBA_CMD_24
FBA_CMD_8
FBA_CMD_21
FBADQSP7
FBADQSP4
FBADQM7
FBADQM4
FBADQSN7
FBADQSN4
FBA_CMD_28
FBA_ZQ2
R612
FBADQSP6
FBADQSP5
FBADQM6
FBADQM5
FBADQSN6
FBADQSN5
FBA_ZQ3
R613
C300
C352
C311
C328
100-BALL
SDRAM DDR3
2ND = H_72.51G63.C0U S_72.41164.H0U
C296
C310
C333
C345
C368
C317
C344
C371
C341
C342
C321
DY
C304
C326
C325
C337
C353
SCD1U10V2KX-5GP
C351
C373
C362
C370
C297
R449
R207
C762
C493
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VRAM(2/2)
Size A3
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SA SB SC -1

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HISTORY***

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